

Low-Power and Compact Time-Domain Analog Feature Extraction for ECoG Motor Intent Decoding

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ABSTRACT: Power consumption has become a key constraint in designing implantable Brain-Computer Interfaces (BCIs). For systems with a large number of channels, analog-to-digital conversion and Feature Extraction (FEx) are often the most power-hungry stage of the decoding pipeline. To address this bottleneck, we present a BCI processing chain using an ultra low-power compact analog Time-Domain (TD) Band-Pass Filter (BPF) bank to extract features from ElectroCorticoGraphy (ECoG) signals. First, we show that the frequency spread of TD BPF have little impact on the decoding accuracy. The proposed analog features are then assessed on a 5-class motor decoding task and achieve a decoding performance well above chance level, indicating that these features preserve discriminating information for multi-class decoding. The same features are then used for binary motor/idle detection task and performed as well as digital features, while consuming $\times 646$ less power, and $\times 75$ vs analog counterparts. In this setting, we also show that our system maintains robust accuracy even at high noise levels, highlighting a favorable trade-off when using lower power Analog ReadOuts (AROs). This paper overall demonstrates that TD Analog Feature Extraction (AFEx) can provide a good power-performance trade-off for binary tasks in low-power implantable BCI systems.

INTRODUCTION

Recent progress in BCI decoding methods has enabled increasingly powerful and complex systems that can accurately detect and decode motor intent for patients after spinal cord injury [1, 2]. These advances pave the way towards complete rehabilitative systems that could restore patients' autonomy. However, such demonstrations often focus on improving decoding accuracy and task complexity, rather than on constraints that are central to day-to-day use in a rehabilitative context, such as miniaturization and power reduction. This gap becomes critical for portable and implantable systems, where the power budget is limited. Integrating the hardware constraints early in the design process is therefore crucial to build practical systems for the patient.

Previous works have explored low-power techniques for BCI design [3], either by optimizing existing algorithms

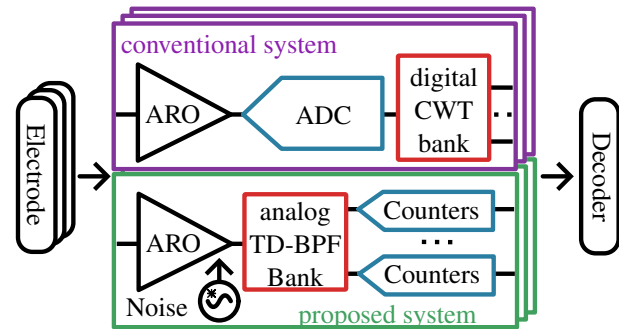


Figure 1: (a) Conventional BCI FEx Pipeline Compared to (b) Proposed Analog TD BPF Bank

and platforms, or by proposing custom Application Specific Integrated Circuit (ASIC) accelerators to reduce power. Such systems have been used for epileptic seizure detection [4], speech [5] and motor decoding [6].

Among invasive neural recording techniques, ECoG offers a trade-off between resolution and invasiveness, while providing stable recordings over time [7] which is required for long-term BCI implants.

In ECoG-based motor applications, motor decoding often relies on detecting changes in activity within specific frequency bands, making spectral representations attractive for such systems [3]. Extracting spectral features through digital signal processing can be done either in an external computer or directly in the implant [3]. This step can be costly in hardware, as it typically relies on Multiply-Accumulate (MAC) operations and memory accesses across channels and bands [8]. This motivates exploring alternatives such as analog approaches for lower-power operation.

Existing approaches reduce power by applying simplifications or by selecting subsets of inputs [9]. However, they remain tied to a continuous FEx mechanism that still consumes a constant amount of power. The AFEx approach, seen in [10] allows for a flat power reduction by extracting features before digitization. This reduces the amount of information to be sampled, as gestated in [11] and is therefore more power and silicon efficient. But [10] still uses regular analog filters, which require large biasing currents, resistors and capacitors to mitigate noise and process variations. This paper focuses on two

complementary directions to demonstrate potential power reduction in BCI processing. First, it introduces a parallel AFEx approach, a compact ultra-low-power TD BPF bank adapted from [12] and based on Injection-Locked Oscillators (ILOs) to estimate the per-band energy over a given time window as features, and compare their performance to Continuous Wavelet Transforms (CWTs) commonly used for BCIs using a baseline classifier. Then, the impact of different noise levels on the AROs on the system accuracy is studied to understand how power can be traded off with noise. The simulated ARO and FEx module are evaluated on real ECoG datasets.

MATERIALS AND METHODS

We evaluate the proposed low-power FEx framework in a realistic simulated setting. Fig. 1 summarizes the two processing flows considered in this work. In the baseline State-of-the-Art (SoA) system, ECoG signals are digitized after amplification by the ARO and features are extracted using digital processing. In our proposed pipeline, spectral features are extracted directly in the analog domain using a TD BPF bank, and only the resulting feature streams are digitized by accumulation. In both flows, the extracted features are fed to a SoA decoder for classification. The systems are evaluated using the same datasets and decoders, with different levels of noise.

FEx:

Most BCI decoding pipelines rely on intermediate representations, also called features, extracted from neural signals before applying a classifier or regressor, commonly known as the decoder. In practice, features summarize signal properties, such as spatial, spectral or temporal characteristics. In this work, we focus on spectral representations extracted from ECoG input signals. For our experiments, features were computed on either 100 ms (8DoF, Runner) or 80 ms (BCI-IV) time frames.

CWT Features: Wavelet-based representations are attractive for brain signal decoding, since wavelets act as time-localized band-pass filters. Moreover, the CWT provides flexible digital filters that can extract any set of frequency components, and this method has often been used for BCI FEx [13, 14].

The CWT relies on a convolution between an input signal and a wavelet. Given a discrete time signal $x[n]$, its CWT component at scale a and time shift τ is defined as:

$$W(a, \tau) = \sum_n x[n] \psi^* \left(\frac{n - \tau}{a} \right), \quad (1)$$

where ψ^* is the complex conjugate of a mother wavelet scaled by a factor of a to obtain a desired frequency component. To obtain features for BCI decoding, we can use the time-frequency coefficients to compute the mean energy at a frequency f_a within a given time window [2].

$$E_{a,T} = \frac{1}{|T|} \sum_{\tau \in T} |W(a, \tau)|^2, \quad (2)$$

where T denotes the time coefficients within the defined extraction window. In this work, the CWT-based energy

features are used as the reference digital baseline, against which we compare the proposed time-domain features extracted using the ILO filter bank.

Analog TD BPF Features: In this paper, a model of analog BPFs based on ILOs, as described in [12], is used. When locked to a reference clock ref , ILOs are forced to run at the ref frequency with a phase shift ϕ proportional to the difference between the natural frequency and the ref frequency. If modulated with an input voltage V_{in} , ILOs change their natural frequency, thus resulting in a voltage-to-time converter of DC gain G_{ILO} , with a low-pass filter property of cutoff frequency f_c . Embedding the ILO in a feedback loop with an integrator of gain G_{INT} results in an ultra-low power, low silicon area, bandpass phase modulated signal at injected signal frequency, of transfer function given in Eq. 3.

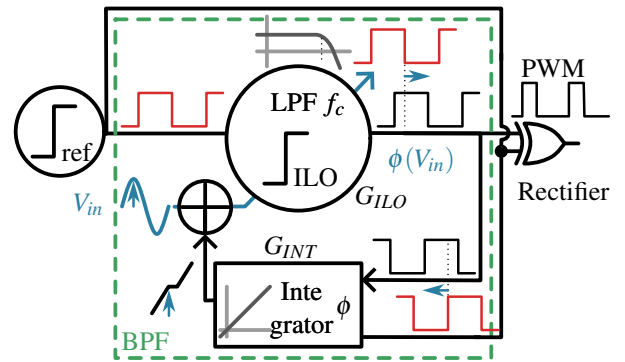


Figure 2: Block diagram of a TD Based ILO BPF and their associated transfer functions representation with the impact of the input signal in blue and the ref clock in red

$$H(s) = \frac{\phi}{V_{in}} = \frac{G_{ILO} \cdot s}{G_{INT} \cdot G_{ILO} + s + \frac{s^2}{2\pi f_c}} \quad (3)$$

The rectified output pulse width of the XOR gate is over-sampled and averaged to estimate the input signal energy in each spectral band. Here, the filter is simulated by discretizing Eq. 3 with a generalized bilinear transform.

To extract multi-band spectral features using these filters in a bank, a logarithmic scale was adopted, which simplifies design by keeping the quality factor constant thus limiting overlap between close bands.

ARO Noise Model:

ARO of BCIs prepare and amplify neural signals so that they can be processed by the FEx stage. They are typically designed to maintain high signal integrity, which necessitates high biasing currents. To reduce power, the signal degradation/power consumption trade-off is explored by introducing increasing levels of noise, and monitoring the decoding performance. To capture this trade-off with a simple model, we consider the input-referred noise of our system to be the sum of a white/thermal term, and a low-frequency/flicker term following a $1/f$ trend as shown in Eq. 4, which matches classical expected noise profiles at low frequencies.

$$\overline{V_i^2} = \overline{V_{thermal}^2} + \overline{V_{flicker}^2} \quad (4)$$

Based on analog amplifier simulations, the overall noise is dominated by flicker noise, as thermal noise density was estimated at $25 \text{ nV}/\sqrt{\text{Hz}}$. To fully cover the range of a typical ECoG signal Power Spectral Density (PSD), the flicker noise will vary from 0.46 to $29.8 \mu\text{V}_{\text{rms}}$ as shown in Fig. 3, plotted here from an electrode average over a session of the Runner dataset. For reference, the estimated noise level from the CINESIC ARO extrapolated noise profile [15] was also drawn. Using Fig. 3, when increasing noise, it can be expected that high frequency oscillations of the signal would be first degraded.

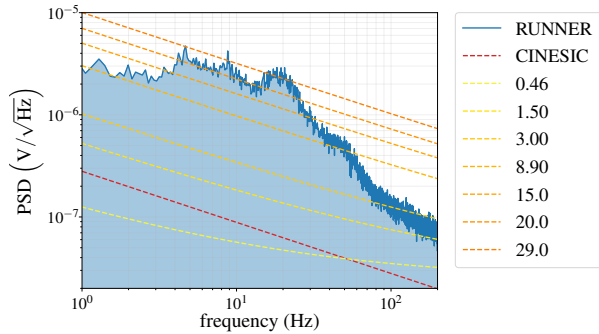


Figure 3: PSD of Simulated ARO Noise labelled in μV_{rms} compared to CINESIC [15] Noise and ECoG Signal Density

The original datasets were acquired with low-noise front-ends (CINESIC [15], SynAmps2 [16]). Their noise contribution will be considered negligible with respect to the noise added in our experiments.

Reference Decoder:

To isolate the impact of the FEx step on decoding metrics, we use a SoA decoder, previously used in a BCI, as baseline to show the impact on different FEx configuration. Classification tasks are the sole focus of this study, thus regressive decoders are omitted.

The model used is an Markov Switching Linear Model (MSLM) that accounts for the temporal structure of the features and state transitions [2]. At each step, the model computes the class likelihood from the feature vector using a linear mapping, followed by a softmax function to obtain observation probabilities. These observations are then combined with a Hidden Markov Model (HMM) with transition probabilities. Decoding is performed by estimating the most probable current state using the posterior. In practice, this temporal prior improves robustness in asynchronous decoding by stabilizing the state transitions. The model is composed of $9600 \times N$ parameters with N the number of classes, which are trained in pseudo-online using a Recursive Exponentially Weighted N-way Partial Least Squares (REW-NPLS) algorithm [17], which incrementally updates the linear model with new data. We used for training the two recommended sessions of the Runner and 8DoF datasets (amounting to respectively 12% and 10%). We collected the accuracy, recall, precision and F1 scores for each session to provide an average and standard deviation over the sessions. For BCI-IV, we followed the original split

yielding a single score.

Benchmark Datasets:

The datasets used in this paper were recorded during Motor Imagery (MI) or Motor Execution (ME) tasks.

8-Degrees of Freedom (8DoF) Virtual Avatar: The first dataset was obtained from a male participant with chronic traumatic quadriplegia following a complete C4-C5 spinal cord injury, and was previously used to develop an adaptive decoder [2]. It was recorded as a part of the “BCI and Tetraplegia” (ClinicalTrials.gov identifier: NCT02550522) clinical trial, approved by the Agency for the Safety of Medicines and Health Products and the ethical Committee for the Protection of Individuals. Two fully implantable WIMAGINE epidural devices were placed over the upper-limb sensorimotor cortices, each integrating a 64-electrode grid [18]. During the virtual-avatar experiment, the participant controlled a first-person avatar and performed motor-imagery commands (hand translation and wrist rotation), providing labelled data for a 5-class decoding task.

Runner 2-Class Task: We also took the Runner ECoG dataset recorded with the same WIMAGINE epidural implants and participant, to evaluate the decoding of binary motor intent. In this task, the participant viewed a third-person virtual avatar and was instructed to alternate between *walk* and *stop* commands. The avatar either walked at a fixed speed or remained stationary [2]. The recordings comprise approximately two hours of data acquired over multiple short sessions of 10 minutes each.

BCI Competition IV - 4: We also evaluated our approach on the BCI-IV dataset, an open-source ECoG dataset recorded from three epileptic patients performing finger motor execution [16]. Each trial is cued by a displayed word indicating which finger to flex, and signals are recorded from 62, 48, and 64 electrodes depending on the subject. This dataset provides a reproducible benchmark to assess robustness across patients, electrode layouts, implantation method, and sampling hardware.

Labels are provided as continuous 1D finger position traces rather than discrete classes. We convert them into one-hot encoded movement labels as shown in Fig. 4. The first step detects movement, the second avoids periodic Idle label during finger flexion, and the third monitors involuntary finger overlaps and either splits the uncertain labels in two if the overlap is contiguous, or removes it if one fully covers the other. For binary experiments, any detected finger movement is treated as a ‘Motor’ state, and the absence of movement as ‘Idle’.

Since the ECoG signals units are not specified, to keep consistence with the other datasets and to simplify the noise injection stage, a global scaling factor of $3 \times 10^{-9} \text{ V}$ per step was applied, thus considering the amplifier [16] to be in AC mode as described in its documentation.

Estimated Power Savings vs SoA:

To demonstrate the potential power savings of the whole pipeline, we will compare the proposed ARO and FEx improvements with SoA systems.

FEx: [12] uses the same AFEx studied here for au-

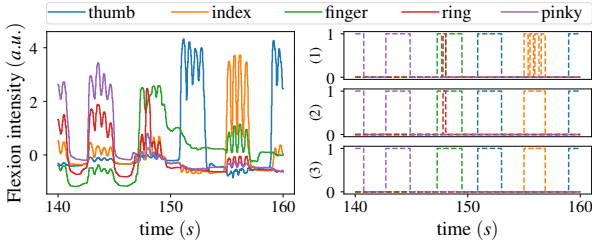


Figure 4: BCI-IV Label Cleaning Steps: (1) Movement Thresholding, (2) Gap Merging, and (3) Overlap Resolution

dio signals with 16 filters between 125 Hz and 5 kHz, and reports a power consumption of 0.820 μ W. ILO BPFs power scales with ref frequency, which will be on average $\times 20$ slower, if adapted to ECoG. Thus, the power per extracted feature would be around 3 nW. Only demonstrators extracting motor ECoG frequency band's energy reported in [3] will be studied. The average power consumption from [3] of ECoG based energy band FEx is 30 mW. This is highly due to outliers which are not based on ASIC implementations, but is still somewhat representative of the field. [6] uses digital FEx and consumes 295.4 μ W while extracting 64 features simultaneously, excluding decoding. The system using an AFEx approach [10] consumes 34.6 μ W for 32 features. This makes our system respectively $\times 4 M$, $\times 646$ and $\times 75$ more power efficient per extracted feature than its SoA counterparts.

ARO: To measure the impact of relaxing noise constraints, an extrapolation of the power/noise relation was done in Fig. 5 by harvesting ARO performances from [19]. It roughly follows an inverse power law of parameters mentioned in Fig. 5.

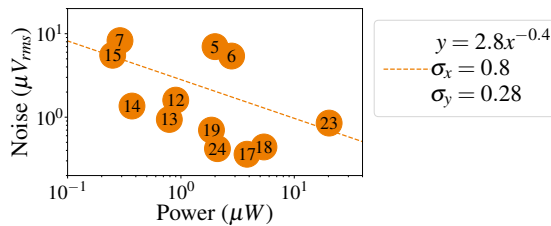


Figure 5: Power vs Noise Trend, with Citation # from [19]

RESULTS

We first evaluate FEx for multi-class decoding, by validating the impact of frequency spacing and then comparing analog BPF-based features to the digital CWT baseline. We finally focus on binary decoding, and evaluate the impact of AROs noise on the decoding accuracy.

Linear vs Log-Spaced Frequency Analysis:

As the analog filter bank extracts log-spaced frequencies, we preemptively evaluate the impact of frequency spacing using CWT-based features, to isolate its effect from the FEx method in Tab. 1. For that, we compare the linearly spaced baseline of 15 frequencies between 10 and

150 Hz in [2], to log-spaced configurations of 8 or 16 frequencies between 10 and 150 Hz or 200 Hz to evaluate the interest of higher frequency bands, used in [1].

Table 1: Frequency Impact on BCI Decoding (Runner Dataset)

Configuration	Acc. (%)	Rec. (%)	Prec. (%)	F1 (%)
linear (10-150Hz)	83.9 $\pm$ 5.8	81.5 $\pm$ 7.4	83.3 $\pm$ 5.4	81.6 $\pm$ 7.1
log-16 (10-150Hz)	84.8 $\pm$ 5.6	83.0 $\pm$ 6.8	84.1 $\pm$ 4.9	83.0 $\pm$ 6.5
log-8 (10-150Hz)	84.7 $\pm$ 5.6	82.3 $\pm$ 6.8	84.6 $\pm$ 4.6	82.6 $\pm$ 6.6
log-16 (10-200Hz)	84.6 $\pm$ 5.4	82.5 $\pm$ 6.9	84.0 $\pm$ 5.1	82.6 $\pm$ 6.5
log-8 (10-200Hz)	84.6 $\pm$ 5.8	81.9 $\pm$ 7.2	85.0 $\pm$ 4.5	82.3 $\pm$ 6.9

Across both the runner and 8DoF datasets, the different frequency configurations yielded similar performance distributions across sessions. As shown in Tab. 1, logarithmic provides a slight advantage over linear spacing on the runner dataset. Similarly, Tab. 2 shows that on the 8DoF dataset, the log-16 configuration slightly improved the decoding metrics. As a result, moving from linearly spaced to log-spaced frequencies has little to no impact on decoding performance, and the following results will compare the extraction methods.

Table 2: Frequency Impact on BCI Decoding (8DoF Dataset)

Configuration	Acc. (%)	Rec. (%)	Prec. (%)	F1 (%)
linear (10-150Hz)	79.9 $\pm$ 8.5	77.4 $\pm$ 8.8	75.3 $\pm$ 10.3	72.8 $\pm$ 11.6
log-16 (10-150Hz)	81.3 $\pm$ 7.5	78.2 $\pm$ 8.5	75.4 $\pm$ 10.4	73.9 $\pm$ 10.9
log-8 (10-150Hz)	80.1 $\pm$ 8.6	77.4 $\pm$ 8.8	75.1 $\pm$ 10.5	72.8 $\pm$ 11.6
log-16 (10-200Hz)	80.2 $\pm$ 8.3	77.4 $\pm$ 8.7	75.0 $\pm$ 10.5	72.9 $\pm$ 11.4
log-8 (10-200Hz)	79.3 $\pm$ 8.8	76.7 $\pm$ 9.2	73.9 $\pm$ 10.7	71.8 $\pm$ 11.9

Analog vs CWT Features:

We now compare analog log-spaced BPF features to the digital CWT baseline on 5-class and 2-class decoding.

8DoF dataset: Although decoding performance is degraded compared to the digital CWT baseline, all metrics remain significantly above chance level (20%), as shown in Tab. 3. The proposed analog BPF-based features thus preserve discriminative information in multi-class tasks, while loosing finer characteristics that allowed for higher performance classification. Moreover, the log-16 configuration shows a slight improvement compared to the log-8, highlighting non-redundant information across frequency bands. The intersession variance being higher also indicates that while they under-perform on average, there are still sessions where performances closely match. This indicates that further investigating may be needed to fully understand the mechanism behind this information loss.

Table 3: CWT vs Analog BPF BCI Decoding (8DoF dataset)

Configuration	Acc. (%)	Rec. (%)	Prec. (%)	F1 (%)
CWT	79.9 $\pm$ 8.5	77.4 $\pm$ 8.8	75.3 $\pm$ 10.3	72.8 $\pm$ 11.6
BPF log-16	69.2 $\pm$ 15.2	67.4 $\pm$ 12.3	68.9 $\pm$ 11.5	61.3 $\pm$ 15.6
BPF log-8	65.3 $\pm$ 16.2	65.6 $\pm$ 11.0	66.6 $\pm$ 12.7	57.9 $\pm$ 15.9

Runner Dataset: On the runner dataset, the analog BPF-based features achieve decoding performance closer to the digital CWT baseline, as shown in Tab. 4. This confirms that binary decoding can be achieved using the proposed analog features.

Table 5: Per-subject BCI-IV benchmark metrics for analog BPF configurations

Configuration	Subject 1 metrics				Subject 2 metrics				Subject 3 metrics			
	Acc. (%)	Rec. (%)	Prec. (%)	F1 (%)	Acc. (%)	Rec. (%)	Prec. (%)	F1 (%)	Acc. (%)	Rec. (%)	Prec. (%)	F1 (%)
BPF log-16	77.52	71.46	76.49	72.77	85.16	82.64	84.53	83.41	86.44	86.51	86.56	86.44
BPF log-8	74.32	70.73	71.42	71.03	84.56	81.92	83.89	82.72	87.96	88.06	88.22	87.95

Table 4: CWT vs Analog BPF BCI Decoding (Runner dataset)

Configuration	Acc. (%)	Rec. (%)	Prec. (%)	F1 (%)
CWT	83.9 ± 5.8	81.5 ± 7.4	83.2 ± 5.4	81.6 ± 7.1
BPF log-16	81.3 ± 6.9	79.4 ± 7.3	81.9 ± 6.3	79.0 ± 7.9
BPF log-8	80.6 ± 5.2	77.7 ± 7.6	80.6 ± 5.4	77.6 ± 7.4

BCI-IV Dataset: To generalize beyond the WIMAGINE implants, we repeated the same analysis on the all of BCI-IV subject’s. As shown in Tab. 5, analog BPF-based features enable above chance level binary decoding.

Noise robustness:

We then evaluate the robustness of AFEx by adding input noise to the analog front-end for both Runner and BCI-IV datasets. As illustrated in Fig. 6, the decoding accuracy remains relatively stable at low noise levels, with a progressive degradation as the $1/f$ noise amplitude increases. This trend is consistent across subjects and datasets, although the noise tolerance varies, indicating subject-dependent sensitivity that likely reflects differences in electrode coverage, signal quality, task type and engagement. Overall, these results support that the proposed TD AFEx remains usable under realistic front-end noise constraints and can enable power driven ARO design trade-offs across heterogeneous ECoG recordings.

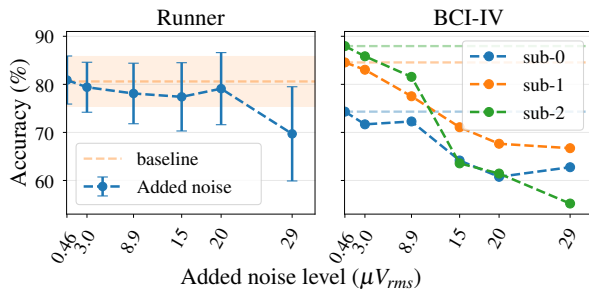


Figure 6: Accuracy of the Analog log-8 BPF Configuration Under Increasing Added $1/f$ Noise Compared to Baseline, with Runner’s Intersession Variance and BCI-IV 3 Subject’s Scores

DISCUSSION

Results show that log-spacing seem to offer a slight improvement ($\sim 1\%$) in decoding performance, which would make sense with classical brain wave sequencing [20]. The number of filter doesn’t seem to have a significant impact. The TD AFEx performs similarly as conventional digital features on binary classification tasks in a BCI flow, while being at least $\times 75$ more power efficient. The AFEx with the baseline decoder shows robustness to higher level of noise than measured in SoA AROs, meaning significant power savings can be made by relaxing noise requirements. Moreover, $1/f$ noise affects more

severely the signal high frequency components as shown in Fig. 3, meaning that these regions may not be crucial for binary motor/idle classification. By increasing the allowed noise 10 times, up to $\times 300$ power savings could be obtained based on Fig. 5 at the cost of a small performance degradation.

The generalizability of the decoding performances results is still to be shown by conducting the same experiments with an increased number of patients.

Given that about two third of the power of [6] is dedicated to the analog front end and FEx and the rest is allocated to decoding, this puts in perspective the potential savings at the scale of a whole BCI system.

CONCLUSION

In this paper, we propose an ILO-based filter bank to extract features from ECoG signals. The decoding showed similar performance as digital CWT features on binary motor intent decoding tasks. The features were also shown to be efficient for a 5-class decoding paradigm, exhibiting significantly above chance level accuracy. This approach consumes $\times 646$ less power than the best existing digital approach and $\times 75$ less power than analog counterparts. Finally, we studied the BCI pipeline robustness to noise on binary motor intent classification, and showed that if we can relax added noise level by $\times 10$ and save up to $\times 300$ power for a low performance cost. By combining these elements, we show the possibility of designing a competitive ultra-low power analog front end for motor intent detector.

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