Ko Odreitz, BSc

Power MOSFET Modeling for EMC Simulation

MASTER'S THESIS

to achieve the university degree of
Diplom-Ingenieur

Master's degree programme:
Elektrotechnik

submitted to
Graz University of Technology

Supervisor

Univ.-Prof. Dipl.-Ing. Dr.techn. Bernd Deutschmann

Institute of Electronics

Mentor

Dipl.-Ing. Michael Fuchs, BSc

Graz, May 2021

AFFIDAVIT

I declare that I have authored this thesis independently, that I have not used other than the declared sources/resources, and that I have explicitly indicated all material which has been quoted either literally or by content from the sources used. The text document uploaded to TUGRAZonline is identical to the present master's thesis.

Date, Signature

Abstract

This master thesis presents a universal behavioral SPICE model for power field-effect transistors. The proposed method allows to create simulation models very quickly by only using parameters which can be found in datasheets. In case no datasheet is available, measurement methods are presented in order to capture all required characteristics. Besides output and transfer characteristics, the body diode, the temperature behavior, the voltage-dependent stray capacitances and the bonding wires are taken into consideration as well. The suggested model is applied for modeling a superjunction and a silicon carbide MOSFET. For validation, the switching behavior of the generated models is compared to measurements, taking parasitic elements of the measurement setup into account. The manufacturer's SPICE models are included in the comparisons as well. The proposed model shows a good agreement and convinces especially with its simple structure, the flawless convergence behavior and short simulation times while maintaining complete control over the simulation model.

Keywords: SPICE model, behavioral model, superjunction, silicon carbide, power MOSFET

KURZFASSUNG

In dieser Masterarbeit wird ein universelles SPICE Modell von Leistungsfeldeffekttransistoren präsentiert, ohne dass Kenntnisse des internen Aufbaus oder der verwendeten Materialien von Nöten sind. Die vorgeschlagene Methode ermöglicht das Erstellen von individuellen Simulationsmodellen in kürzester Zeit, lediglich anhand von Parametern, die in üblichen Datenblättern zu finden sind. Messmethoden werden präsentiert, um die Modellierung auch gänzlich ohne Datenblatt zu ermöglichen. Neben der Ausgangs- und der Steuerkennlinie werden im Modell auch die Inversdiode, das Temperaturverhalten, die spannungsabhängigen Streukapazitäten und die Bonddrähte abgebildet. Anhand der empfohlenen Methode werden Modelle zu einem Superjunction- und einem Siliciumcarbid-MOSFET erstellt. Zur Validierung wird das Schaltverhalten der generierten Modelle mit Messungen verglichen, wobei parasitäre Elemente des Messaufbaus mitberücksichtigt werden. Die SPICE Modelle des Herstellers werden bei den Vergleichen miteinbezogen. Das vorgeschlagene Modell zeigt dabei eine gute Übereinstimmung und überzeugt vor allem mit dem simplen Aufbau, dem einwandfreien Konvergenzverhalten und kurzen Simulationszeiten bei gleichzeitiger vollständiger Kontrolle über das Simulationsmodell.

Schlagwörter: SPICE Modell, Verhaltensmodell, Superjunction, Siliciumcarbid, Leistungs-MOSFET

Contents

List of Figures

List of Abbreviations, Acronyms and Symbols

DUT	Device under test
EMC	Electromagnetic compatibility
FET	Field-effect transistor; equivalent to MOSFET
MOSFET	Metal–oxide–semiconductor field-effect transistor
RF	Radio frequency; frequencies typically above 9 kHz
SiC	Silicon carbide
SJ	Superjunction
VNA	Vector network analyzer
U in $[V]$	Used for both voltage and electric potential
$\wedge$	Logical AND
$\vee$	Logical OR
j	Imaginary unit
$\Re$	Real part of a complex number
$\Im$	Imaginary part of a complex number

1 Introduction

1.1 Motivation

In modern days, EMC (electromagnetic compatibility) simulations have become crucial in the field of power electronics. Considering EMC during the development process reduces the number of hardware prototypes since unexpected effects can be detected before manufacturing an electronic system. International regulations demand for EMC tests before selling an electronic device. Thus, a failed EMC test, which is both expensive and time consuming, can be avoided by performing EMC simulations beforehand.

During the current COVID-19 pandemic, the demand not just increased for consumer electronics, but the interest also surged for the electric vehicle industry [1], [2]. It is expected that the demand on electrical vehicles will further increase if governments will put more effort in order to reach international climate goals by encouraging consumers to buy new vehicles [3]. The electrical vehicle stock is just one example for the growing demand for power electronics. Different power semiconductor devices such as an insulated-gate bipolar transistor (IGBT) or a power metal–oxide–semiconductor field-effect transistor (MOSFET) are necessary to control high electric voltages and currents. The later one excels with high switching speeds to increase the efficiency. However, high du/dt and di/dt are also a root cause for conducted and radiated emissions which make a device less electromagnetic compatible.

According to CAM [4], 2.66 times more cars are recalled than newly registered in the first half of 2020. Often, the root cause is uncertain, but EMC problems are a realistic assumption [5]. In a typical scenario, an integrated circuit (IC) which is performing a fast switching digital operation is the source of electromagnetic emissions (EME) whereas sensible analog circuits like operational amplifiers (opamp), analog-to-digital converters (ADC) or digital-to-analog converters (DAC) are electromagnetically susceptible [6]. Often, the designer of an instrument must represent economic interests and thus shielding measures, additional PCB layers or even filter components are avoided. As the time to market is shrinking as well, the product should pass EMC tests at the first attempt. This makes highly accurate simulation models even more essential to help designers to estimate possible sources of EME. In a typical production cycle nowadays, several prototypes are fabricated until an electronic system is both efficient and electromagnetically compatible; in a future scenario, a simulation should provide a good preliminary estimate of the required filtering and shielding measures in advance in order to reduce the number of prototypes significantly.

1.2 Power MOSFET technology

In general, the power MOSFET and the ordinary MOSFET, which is mainly used in digital applications because of its high integrity, operate according to the same physical principles but differ in their geometrics [7]. As illustrated in Figure 2, a power MOSFET's source and drain connection are placed vertical from each other and add an additional lightly doped n– layer.

In this way, the structure behaves like a p–i–n diode, and the breakdown capability depends on the thickness and the doping level of the n– epitaxial layer (drift region). The thicker and more lightly doped, the higher voltages can be blocked [8]. In addition, a low on-resistance can be achieved due to numerous MOSFET cells connected in parallel while the vertical structure keeps the area consumption low. Therefore, a power MOSFET is an asymmetrical device but uses the same electrical symbol as the ordinary MOSFET in Figure 1 with the limitation that the source contact is always connected to bulk respectively body. The power MOSFET is described in great detail in chapter 6 in "Fundamentals of Power Semiconductor Devices" [9].

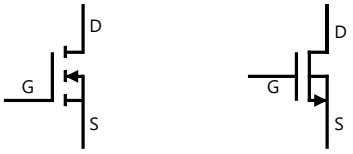


Figure 1: Two equivalent versions of the n-channel power MOSFET circuit symbol

In recent years, new power MOSFET technologies were established like superjunction (SJ), silicon carbide (SiC) and gallium nitride (GaN). The later ones replace the base material of pure silicon by a blend of silicon and carbon in the case of SiC. A variety of crystalline structures exist, but in general both SiC and GaN are considered as a wide-bandgap material. Therefore, higher electric field strengths are necessary to force these components into a breakdown condition. For this reason, SiC and GaN MOSFETs are capable to switch very high voltages.

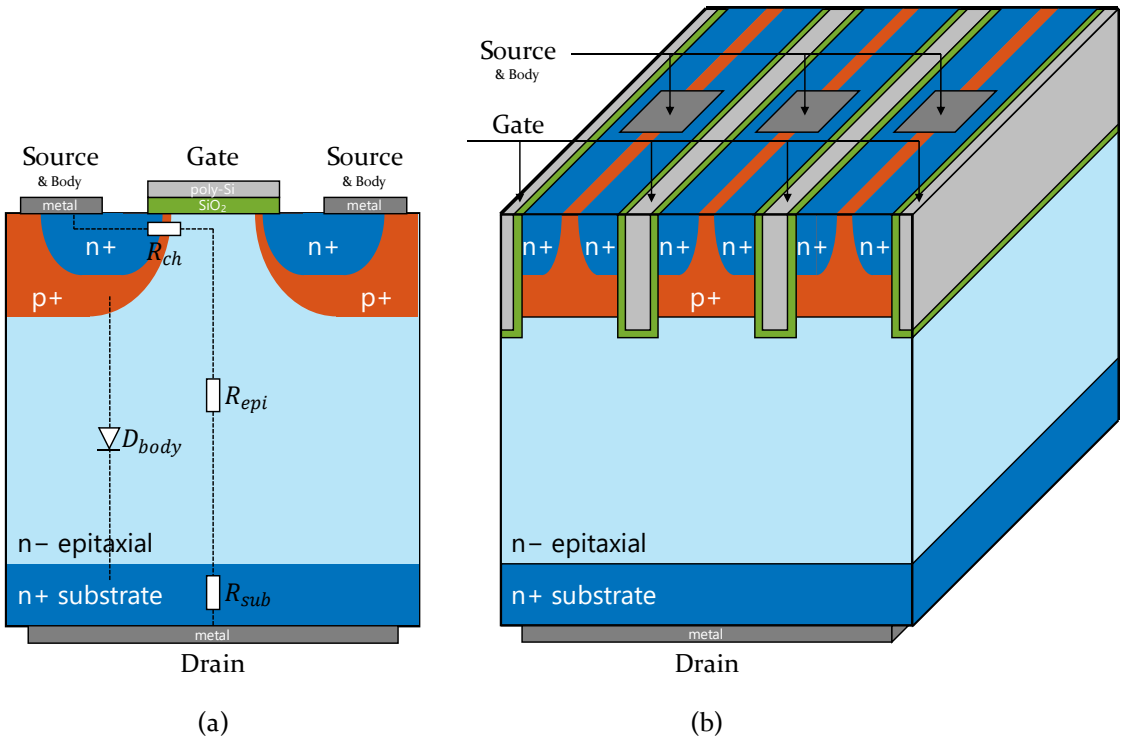


Figure 2: n-channel power MOSFET structure. (a) Planar gate. (b) Trench gate

The SJ technology on the other hand is a structural improvement of the power MOSFET. One drawback of the original power MOSFET is the high contribution of the epitaxial layer to the on-resistance due to its low doping profile. To overcome this problem, the epitaxial layer must be doped more heavily. However, by doing this, the breakdown capability decreases tremendously. So, power MOSFETs bring a tradeoff relationship between on-resistance and breakdown capability. As shown in Figure 3, the SJ FET replaces this epitaxial layer and utilizes alternating p-type and n-type regions with relatively high doping profile [10]. The higher doping reduces the on-resistance significantly whereas the stacked stripes guarantee a high breakdown capability.

A MOSFET should be in a high ohmic state if $U_{GS} = 0$. If $U_{DS} > 0$ is still applied, the drain connection becomes positively charged and afflicts free electrons in the adjacent n-regions. Those electrons get attracted and drift to the drain connection. At the same time, the source connection becomes negatively charged. Because source and body are shorted, the mobile holes inside the adjacent p-regions get attracted and drift towards the body connection. Therefore, the reversed biased body diode becomes depleted and no free charge carriers are available for conducting a current; not until a gate-source voltage U_{GS} is applied or breakdown occurs.

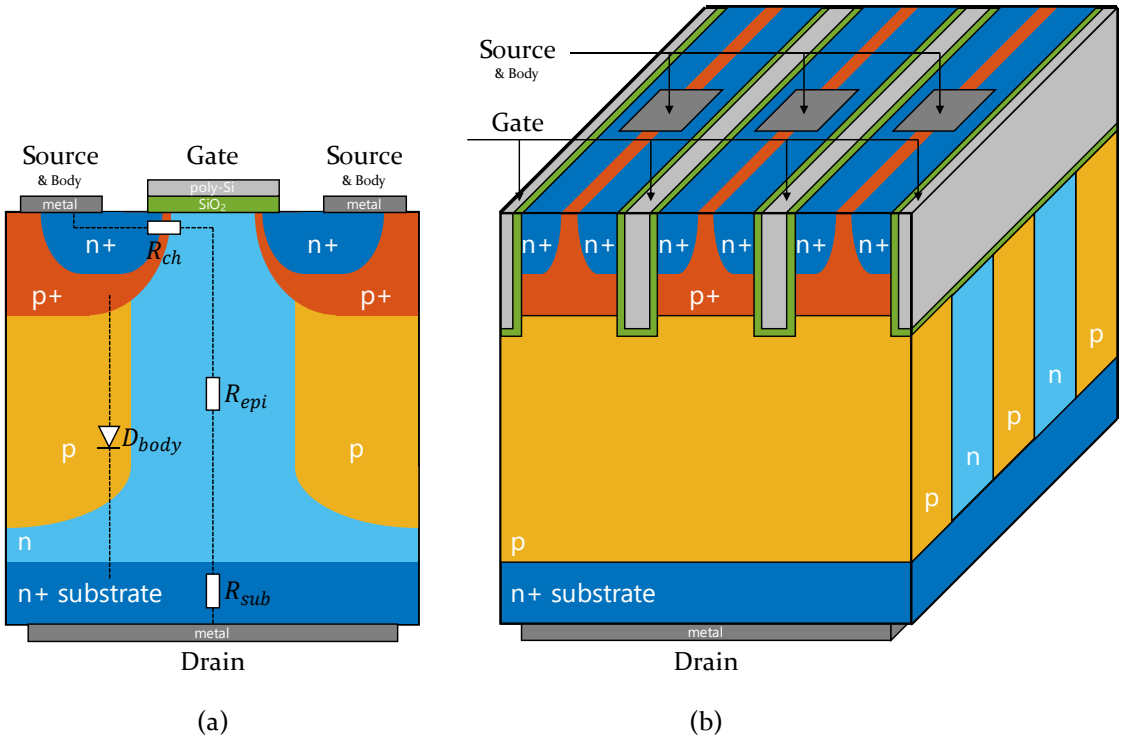


Figure 3: n-channel superjunction MOSFET structure. (a) Planar gate. (b) Trench gate according to Udrea et al. [11]

The gradient on how the depletion region expands differs in an SJ MOSFET. In normal power MOSFETs, the n– layer depletes vertically and a gradient of the potential can be recognized. The closer to the junction, the faster the potential changes because of the nonuniform distribution of the charge carriers. In contrast, SJ FETs use p-doped columns between the n-regions. Because these columns go down to the highly doped substrate, the depletion region expands laterally as well until all n-columns and p-columns become fully depleted. This leads to a uniform distribution of the electric field which is necessary to obtain a high breakdown capability [11], [12]. For this reason, a higher doping level in SJ MOSFETs reduces the on-resistance but does not reduce the achievable breakdown capability anymore [13]. At the time this thesis is written, there are no SiC MOSFETs with superjunction technology developed in a market ready state.

1.3 MOSFET models

For a microelectronic developer it is crucial to work with electronic simulation tools to spot design errors during the development phase. Semiconductor devices are usually described by a single model which consists out of the most relevant information. Most power MOSFET manufacturers provide such a model. However, those models are sometimes encrypted and non-editable. In addition, the provided models are often not accurate in their radio frequency (RF) behavior. So, a more suitable model is necessary for developers to increase the efficiency of their products and to pass EMC tests at the first go. This is the reason why a universal power MOSFET model is in demand.

In general, two different approaches exist when creating a MOSFET model. Historically first, the analytical approach was introduced which is more calculation intense. These first models are developed in parallel to the improvements in the semiconductor industry and deliver a physical representation of a semiconductor device [14]. Numerous parameters are needed to model the device based on formulas; a finite element analysis based on the MOSFETs geometry and material might be executed to estimate those parameters. However, such an analysis could be very time consuming, and a large number of parameters could significantly increase the simulation time which is an important factor in EMC simulations. Besides that, power MOSFET manufacturers usually do not provide detailed information about the semiconductor interiority of their products which complicates this modeling approach from a customer's perspective.

Therefore, the scope of this thesis is on behavioral models. In this approach, the device is treated as a black box where only the provided pins are accessible [14]. Thus, knowledge of the internal structure and the used materials is not required for modeling. However, this lack of linkage to the physical structure is also seen as a disadvantage. In addition, behavioral models could suffer from longer simulation times and could provoke convergence issues [15]. Moreover, the success of this approach highly depends on the datasheet information provided by the manufacturer and the accuracy of additional measurements if necessary.

1.3.1 SPICE software

The circuit simulation software SPICE (Simulation Program with Integrated Circuit Emphasis) was released by the University of California, Berkeley in 1973 [16]. Its newest version SPICE 3f.5 was released as open-source software back in 1993 [17]. The SPICE simulation software is still widely used but not as the original software. A lot of free and non-free software spinoffs extended the original SPICE core with numerous features at the expense of compatibility problems between different SPICE simulators. PSpice (PSpice, Cadence Design Systems, Inc., California, US), HSPICE (PrimeSim HSPICE, Synopsys, Inc., California, US) and LTspice (LTspice XVII, Analog Devices, Inc., Massachusetts, US) are some prominent examples for commonly used software tools. But other prominent software bundles utilize the SPICE core as well; like Advanced Design System (PathWave Advanced Design System (ADS) 2021, Keysight Technologies, Inc., California, US), SIMetrix (SIMetrix/SIMPLIS, SIMetrix Technologies Ltd., GB), PSIM (PSIM 2021A, Powersim, Inc., Maryland, US), or the circuit simulation tool of Altium Designer (Altium Designer 21, Altium Ltd., California, US).

In this thesis, all simulations are done in LTspice since this program is updated regularly and is available as freeware without restrictions to its features [18]. These properties make LTspice one of the most widely distributed SPICE software tools.

1.3.2 Level 1 MOSFET model

Just a few years after the MOSFET was invented in Bell Labs back in 1959 [19], H. Shichman and D. A. Hodges proposed a new equivalent circuit in 1968 [20]. This analytical model is nowadays known as Shichman-Hodges model or level 1 model which separates three modes of operation: the cutoff region (where $U_{GS} \leq U_{th}$), the linear region (where $U_{GS} > U_{th}$ and $U_{DS} < U_{GS} - U_{th}$) and the saturation region (where $U_{GS} > U_{th}$ and $U_{DS} \geq U_{GS} - U_{th}$).

$$I_{DS(cutoff)} = 0. \tag{1.1}$$

$$I_{DS(lin)} = \frac{\mu \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot \left[2 \cdot (U_{GS} - U_{th}) \cdot U_{DS} - {U_{DS}}^2\right] \cdot (1 + \lambda \cdot U_{DS}). \tag{1.2}$$

$$I_{DS(sat)} = \frac{\mu \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (U_{GS} - U_{th})^2 \cdot (1 + \lambda \cdot U_{DS}). \tag{1.3}$$

Due to the time in which their paper has been published, this model is not applicable for submicron channel lengths. However, it is still commonly used today as long as the channel length is not too short. This model considers the dimensions of the transistor by its width W and length L, the capacitance of the oxide layer C_{ox}, the mobility of the charge-carriers μ (electrons or holes) and the effect of the channel length modulation by the parameter λ. As source and bulk connections are shorted within a power MOSFET, the body effect is not considered in the formulas shown.

A large number of different analytical MOSFET models have been developed over the years (e. g. BSIM [21]), and to list and describe all of them would extend beyond the scope of this work. As it is impossible for a customer to estimate all parameters of a more complex analytical model, a universal behavioral model is in demand.

1.3.3 Behavioral MOSFET model

Looking at Figure 2, it can be seen that applying a drain-source voltage causes the corresponding majority charge carriers to drift towards the corresponding terminals. Thus, the non-conducting depletion region expands which reduces the capacitances C_{DS} and C_{GD}. This behavior is modeled by the very simple lumped-element model depicted in Figure 4. It consists out of a voltage-controlled current source, a diode and two voltage-dependent capacitors. Whereas C_{GD} and C_{DS} decrease the higher U_{DS} is, C_{GS} stays constant. Those capacitors are representing the stray capacitances between the connections and are essential to take the switching behavior of the MOSFET into account. As it is described in detail by McArthur [22] or Cittanti et al. [23], these capacitances will be charged and discharged during the switching process.

When switching on a MOSFET (i. e. to bring the MOSFET in its low-ohmic state), its gate-source voltage U_{GS} is not instantly changed, but the parasitic capacitances will be charged first as shown in Figure 5. During the subthreshold phase, C_{GS} is significantly larger than C_{GD} and thus more drive current will flow into C_{GS}. When the threshold voltage U_{th} is reached, the flow of the drain-source current I_{DS} increases rapidly and the drain-source voltage U_{DS} starts to decrease. As long U_{DS} decreases, C_{GD} increases. Therefore, most of the gate driving current will flow into the Miller capacitance C_{GD} which leads to the plateau region in Figure 5. Once U_{DS} reaches its minimum, C_{GD} is not changing anymore. So, further gate drive current will flow into both gate capacitances according to their values.

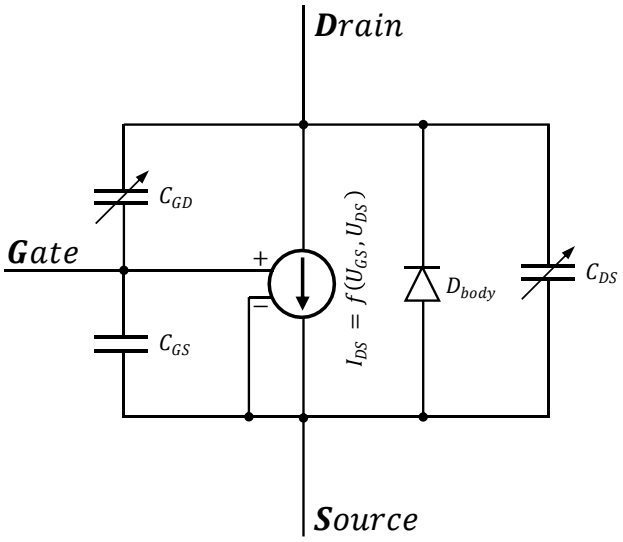


Figure 4: Simple behavioral model of a power MOSFET

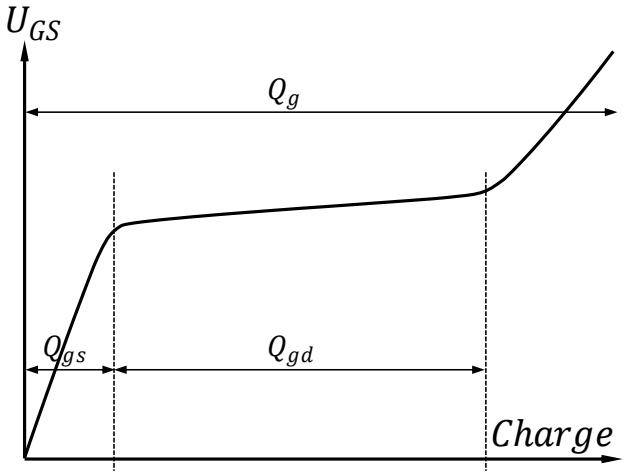


Figure 5: Exemplary gate-charge curve when switching on a MOSFET

1.3.4 Survey of existing approaches

An analytical model representing the switching losses of superjunction MOSFETs was elaborated in March 2016 [12]. Although this is not a complete SPICE model, it is worth mentioning because it addresses the special field distribution in superjunction MOSFETs and analyzes the switching behavior in detail.

Another analytical approach to model superjunction MOSFETs has been elaborated by Fairchild Semiconductor International, Inc. in May 2014 [15]. This model is fully SPICE compatible; however, this approach is based on the knowledge about various process parameters. Since this information is usually unknown to product developers, this thesis focuses on the creation of a universal behavioral model.

Researchers from the University of Stuttgart proposed a behavioral model for the use in transient EMC simulations in September 2017 [24]. The parasitic elements are determined via 3D simulations. Such a simulation, however, would require knowledge of the chip geometry. Hence, this approach employs a combined behavioral-analytic model.

One promising approach for modeling GaN high-electron-mobility transistors (HEMT) was presented by a group of German scientists in September 2019 [25]. The Curtice model [26] is adapted to fit the static characteristics. Further improvements are presented in order to include, for example, the temperature dependency, and the parasitic capacitances are modeled via lookup tables. The authors present a universal modeling procedure, but validation measurements are shown for a single GaN HEMT device only.

Another approach for modeling SiC MOSFETs was published by a Chinese research group in March 2018 [27]. The static characteristics are modeled using a modified version of the Shichman-Hodges model. The stray capacitances are determined using tangent functions since the capacitance changes of SiC FETs are not as complex as those of superjunction FETs.

The "Power Function Power MOSFET" (PFPM) model is an approach to create a more universal SPICE model by picking some coordinate points from the output-, transfer-, capacitances- and diode characteristics; proposed in August 2013 [28], [29]. This approach replaces the iconic formulas of the Schichman-Hodges model for the linear and saturation region by

$$I_{DS(lin)} = \frac{\sqrt{U_{DS}}}{R_{DS(on)}}, \tag{1.4}$$

$$I_{DS(sat)} = c \cdot (U_{GS} - U_{th})^r \tag{1.5}$$

respectively. The differentiation between those regions is not given by $U_{DS} = U_{GS} - U_{th}$ anymore but will be determined by the smaller number of Equation 1.4 and 1.5. One disadvantage of the PFPM model is that the parasitic capacitances shown in Figure 4 are formed by a simple power function which ensures convergence in SPICE but may not be a good enough approximation for the complex capacitance behavior of a superjunction MOSFET.

The Institute of Electronics at Graz University of Technology has published a way to generate behavioral superjunction MOSFET models in December 2020 [30], [31]. This method generates the static behavior similar to suggested in the PFPM model but uses lookup tables to include the parasitic capacitances. A model verification is only given by a simulation which compares the proposed model with the SPICE model provided by the manufacturer.

An LTspice online user group is working on power MOSFET models as well [32]. This community exploits the VDMOS model of LTspice and has developed a program which automatically generates a model after some inputs from the datasheet. However, this method is limited to the parameters which are specified within the LTspice model. For instance, the voltage-dependent capacitors of an SJ field-effect transistors usually show a more complex curve than the VDMOS model supports. Furthermore, this thesis approaches a more general SPICE model which does not ultimately depend on the predefined LTspice models.

1.4 Objective of this thesis

This thesis presents a new and easy way to create a universal behavioral model for power MOSFETs applied on a superjunction FET (IPL65R070C7 [33], Infineon Technologies AG, DE) and a silicon carbide FET (IMZ120R060M1H [34], Infineon Technologies AG, DE). Two different approaches are used to create a suitable SPICE model for simple circuit analyses which depicts the most important transient effects for further EMC considerations. First, by taking datasheet values only and second by capturing values with simple measurements.

The proposed model is created and simulated in LTspice and represents the following characteristics:

Static characteristics:

- Transfer characteristics
- Output characteristics
- Diode characteristics
- Temperature dependency

Dynamic elements:

- Voltage-dependent stray capacitances
- The inductive effect of the bonding wires

Both the generation of the proposed model and the recommended measurement methods are remarkable for their simplicity. If no datasheet is available, the MOSFET can be characterized by methods where only a few electronic instruments are needed, namely:

- two test circuits (explained in Chapter 2)
- a vector network analyzer (VNA)
- an oscilloscope (50 Ω inputs are required for transient verification measurements)
- a pulse generator
- an isolated power supply

Chapter 2 explains the general modeling procedure on the basis of an unknown DUT (device under test) to enable the reader to create their own model in their preferred SPICE software. Formulas are presented to reflect the static characteristics via controlled current sources while the dynamic elements are modeled via simple SPICE components and lookup tables. In addition, measurement setups to capture all relevant information are shown and explained in case no datasheet is available. Furthermore, LTspice test setups are illustrated to verify the created model.

Chapter 3 applies the proposed modeling procedure to create two models each for the SJ and the SiC MOSFET in LTspice. First, according to its datasheet parameters and second by the measured values. The measurement setups from Chapter 2 are applied to capture both static and dynamic behavior of the DUT. The measurement results are then compared with the graphs from the datasheets.

Chapter 4 validates the proposed power MOSFET model by comparing the simulations of the created models with measurements; gate-charge plots are created and transient measurements are performed. Comparisons are also made with the manufacturer's model. This chapter closes with two questions that can be explored in future studies.

Chapter 5 concludes this thesis and discusses the results obtained. Both, the areas of application of the model but also its limitations, are discussed; suggestions for future improvements of the model are noted. Advantages and disadvantages are summarized, and future challenges are explored.

2
METHODS

The first part of this chapter describes a universal circuit which is used to capture the static and transient behavior of a power MOSFET. After that, the general modeling procedure for any unknown DUT is presented to generate the proposed model illustrated in Figure 6. The last part shows the simulation test benches to validate the proposed models.

Section 2.1 starts off by presenting the universal test board which is regularly referenced in this thesis. An exemplary layout is given to highlight the special requirements to optimize this circuit in its radio frequency behavior.

Section 2.2 explains the procedure to model the static behavior by adapting the level 1 model.

Section 2.3 shows the depiction of the dynamic behavior with the help of lookup tables. A special property of the proposed model is that all stray capacitances depend on the drain-gate voltage. A measurement setup is presented in order to capture these capacitances, but also the parasitic elements of the bonding wires, through a single series of measurements.

Section 2.4 presents simulation test benches in order to verify the created models.

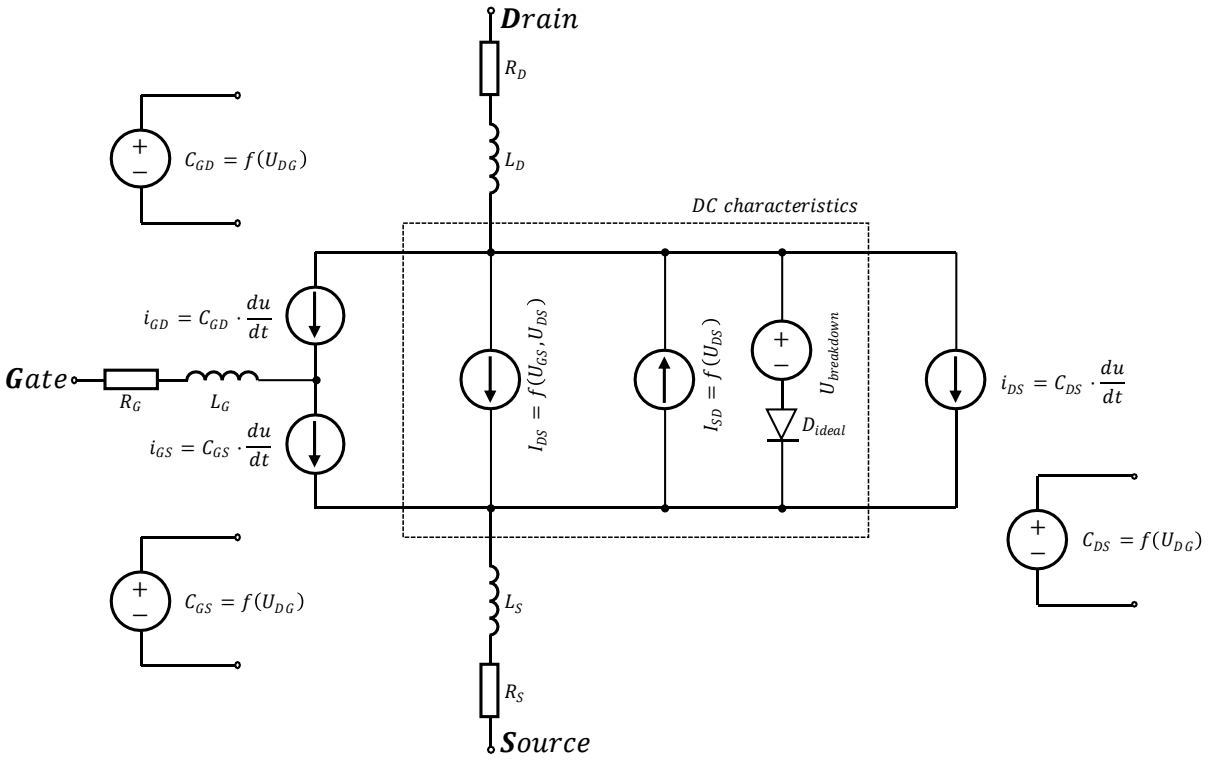


Figure 6: Proposed power MOSFET model

2.1 Universal test circuit

The basic circuit illustrated in Figure 7 is used to monitor gate, source and drain voltage potential of the power MOSFET, the device under test (DUT). Since the DUT is capable to switch very high currents above 100 A while withstanding more than 1000 V, special measures are necessary to capture RF components of the switching process. In addition, when the load R_{load} is shorted, it is necessary to keep the ON-time (i. e. the time span where the MOSFET is low-ohmic) very short. Otherwise, the very high currents would overheat the power MOSFET as no cooling device is attached to it. A proper heat sink could solve the heat problem but could cause unwanted RF coupling effects as well. This thesis concerns the modeling of the MOSFET including its package; the influence of a heat sink must be modeled separately, since its coupling behavior depends on the potential to which the heat sink is connected.

To keep the ON-time short, a pulse generator like an arbitrary waveform generator (AWG) is used to generate a short pulse with a pulse length of a few μs. This controlling signal is forwarded to the input pins of a gate driver to switch on a power MOSFET for just a few μs. A very large decoupling capacitor (200 μF in Figure 7) is needed to serve as a large charge carrier reservoir since very high currents may flow within the main current loop. By placing this decoupling capacitor as close as possible to the load and the 16.7 $m\Omega$ current sensing resistor, the loop area of the flowing current is kept as small as possible and thus keeps the inductance in the main current loop low. The flyback diode is a necessary safety measure.

A main selection criterion for the gate driver IC is that the device is capable to drive high currents of at least 4 A within very short rise and fall times in the ns range. Because of the steep edges, a high usable measuring bandwidth is necessary. This is the reason why an oscilloscope with 50 Ω termination resistors is used. Through the use of 50 Ω wave impedance cables, oscilloscope and cable are matched, and (ideally) no RF reflections occur at the termination resistor.

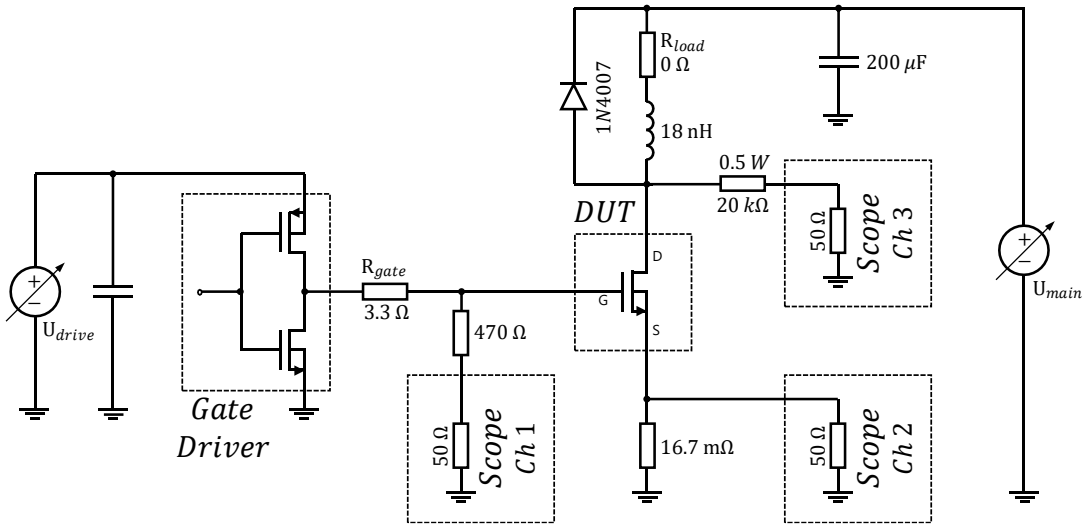


Figure 7: Schematic of the proposed test circuit

Channel 2 of the oscilloscope captures the voltage U_{source} across the 16.7 $m\Omega$ current sensing resistor. The current is then determined by Ohm's law; the resulting error caused by the 50 Ω input impedance is negligible. The selection of this sensing resistor is crucial. First, the resistance must be constant through a broad frequency range. This is achieved by connecting six 100 $m\Omega$ resistors in parallel which reduce the parasitic inductance [35]. Those resistors are placed symmetrically around an SMA connector, and the whole current sense construction is placed

directly on the opposite plane beneath the source pin of the DUT. Second, the current sensing resistor must survive short pulses with a lot of power. If the resistor dies with high resistance, the oscilloscope can be damaged irreparably.

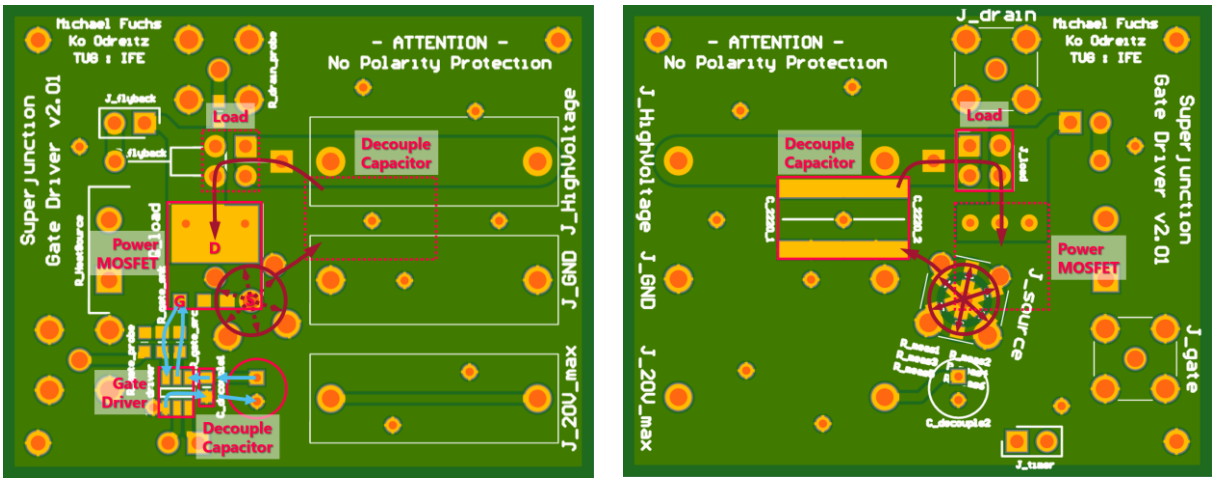
Channel 1 of the oscilloscope must be protected with a 470 Ω resistor since the input power of an 50 Ω oscilloscope must not exceed 0.5 W. Therefore, the measured value must be converted according to the voltage divider. One disadvantage of the simple circuit shown in Figure 7 is that the driving electronic is coupled galvanically with the main side. This leads to an interaction, and the voltage drop across the current sensing resistor is necessary to take into account by

$$U_{GS} = U_{gate(meas)} \frac{520}{50} - U_{source}. \qquad 2.1$$

Channel 3 of the oscilloscope must be protected as well. This resistor must be dimensioned considering the power consumption since a considerable amount of current will flow through the oscilloscope when the power MOSFET is in its OFF state. By placing a 20 $k\Omega$ resistor, this resistor must be capable to withstand 0.5 W when 100 V are applied. Here, a tradeoff must be done by sacrificing resolution of the measured signal. The drain-source voltage is calculated by

$$U_{DS} = U_{drain(meas)} \frac{20050}{50} - U_{source}. \qquad 2.2$$

Since this thesis pursues the goal of enabling EMC simulations, the layout must be optimized with respect to its RF behavior in order to be able to make better statements between simulation and measurement. Figure 8 shows an example where traces between decouple capacitors and components are designed as short as possible to keep the resulting loop areas as small as possible. With the help of vias, larger loops can be avoided. In addition, the power supply connections are placed next to each other to further minimize parasitic inductances. Also, the GND plane is designed over a large area on both planes to keep that plane as low-impedance as possible. If it is planned to heat up the DUT by an additional heating element, it is highly recommended to use a shielded component and to place an additional insulator within the thermal paste layer, and its voltage source should be isolated from the rest of the network. In general, the resulting parasitic inductances show a greater influence the faster the gate signal is switched, i. e. the lower the gate resistor is selected.



(a) (b)

Figure 8: Exemplary layout for the proposed test circuit on both planes. Zoom level: 150%. Dark red arrows indicate the current path of the main current side. (a) Top plane. Additional light blue arrows highlight the current path of the driving signal. (b) Bottom plane containing the six current sensing resistors

2.2 DC characteristics

The basic formulas of the Shichman-Hodges model are utilized to represent the transfer and output characteristics. Due to the fact that the internal geometry of a MOSFET is usually unknown from a customer's perspective, Equation 2.3 introduces $\beta = \mu \cdot C_{ox} \cdot W/L$. To achieve the saturation kink at high U_{GS} in Figure 9a, the Shichman-Hodges equations are expanded with Equations 2.4 and 2.5. While the former equation limits the rise of I_{DS}, the later equation smooths the kink by averaging the values within the range $U_{GS} \pm C$, e. g. $C = 0.1$. Regardless of whether the model is created via the datasheet or via measurements, the final model outputs the current from Equation 2.5 which is composed of Equations 2.3 and 2.4.

$$I_{DS(1)} = \begin{cases} 0, & U_{GS} \leq U_{th} \\ \frac{\beta}{2}\left[2(U_{GS} - U_{th})U_{DS} - {U_{DS}}^2\right](1 + \lambda U_{DS}), & U_{GS} > U_{th} \wedge U_{DS} < U_{GS} - U_{th} \\ \frac{\beta}{2}(U_{GS} - U_{th})^2(1 + \lambda U_{DS}), & U_{GS} > U_{th} \wedge U_{DS} \geq U_{GS} - U_{th} \end{cases}. \quad 2.3$$

$$I_{DS(2)} = \min\left\{\frac{{U_{DS}}^B}{A}, I_{DS(1)}\right\}. \quad 2.4$$

$$I_{DS(3)} = f(U_{DS}, U_{GS}) = \frac{I_{DS(2)}(U_{DS}, U_{GS} - C) + I_{DS(2)}(U_{DS}, U_{GS}) + I_{DS(2)}(U_{DS}, U_{GS} + C)}{3}. \quad 2.5$$

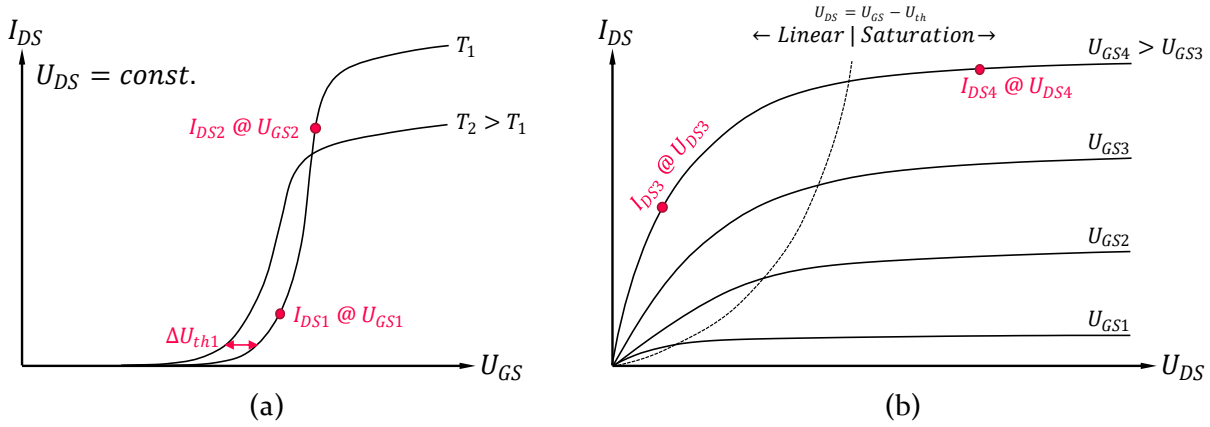


Figure 9: Typical DC behavior of a MOSFET. Red markings show the points to extract for the modeling process. (a) Transfer characteristics when a MOSFET is in saturation mode. (b) Output characteristics

The following twelve key values (eight if temperature dependency is neglected) must be captured from the graphs depicted in Figure 9. Such a diagram of the transfer and output characteristics can be found in any usual datasheet. If no datasheet is provided, the test circuit explained in Section 2.1 can be used to extract the needed values.

Grid points, which must be extracted from the transfer characteristics:

- I_{DS1} at U_{GS1} a bit after the threshold voltage
- I_{DS2} at U_{GS2} when a high amount of current flows but before the kink appears
- (optional) *warm* as variable for specifying a second temperature in °C
- (optional) ΔU_{th1} as an approximated difference of the threshold voltage between *warm* and "room" temperature. In general, this quantity contains a negative number.

Grid points, which must be extracted from the output characteristics:

- I_{DS3} at U_{DS3} within the linear region at very high U_{GS}
- (optional) $I_{DS3(warm)}$ at U_{DS3}; same as before but at $warm$ temperature
- I_{DS4} at U_{DS4} within the beginning of the saturation region with the same U_{GS} as before
- (optional) $I_{DS4(warm)}$ at U_{DS4}; same as before but at $warm$ temperature

Analyzing the saturation region in Equation 2.3, the three unknown parameters β, U_{th} and λ must be determined from two measuring points from the transfer characteristics in Figure 9a. So, the channel length modulation factor λ must be assumed first to obtain an explicit result for the other two variables. A simple estimation can be $\lambda = 0.001$. Thereafter, having two values for I_{DS} for two different U_{GS} allows to determine the unknown parameters

$$U_{th(cold)} = \frac{U_{GS2} - U_{GS1}\sqrt{\frac{I_{DS2}}{I_{DS1}}}}{1 - \sqrt{\frac{I_{DS2}}{I_{DS1}}}}, \tag{2.6}$$

$$\beta = \frac{2 \cdot I_{DS1}}{\left(U_{GS1} - U_{th(cold)}\right)^2}. \tag{2.7}$$

The optional temperature dependency can be reflected by adapting U_{th} with the modification factor ΔU_{th1}. The amplification factor β remains unaffected from this modification. Equation 2.8 is obtained after introducing the variable $temp$ as the actual temperature and assuming "room" temperature at $25°C$.

$$U_{th} = U_{th(cold)} + \Delta U_{th1} \cdot \frac{(temp - 25)}{(warm - 25)}. \tag{2.8}$$

Analyzing Equation 2.4, the two unknown parameters A and B must be determined from two measuring points from the output characteristics in Figure 9b. Having two values for I_{DS} for two different U_{DS} allows to determine these unknown parameters by

$$B_{(cold)} = \frac{\log\left(\frac{I_{DS4}}{I_{DS3}}\right)}{\log\left(\frac{U_{DS4}}{U_{DS3}}\right)}, \tag{2.9}$$

$$A_{(cold)} = \frac{{U_{DS3}}^{B_{(cold)}}}{I_{DS3}}. \tag{2.10}$$

The optional temperature dependency can be reflected by applying Equations 2.9 and 2.10 again but replacing I_{DS3} by $I_{DS3(warm)}$ and I_{DS4} by $I_{DS4(warm)}$. This leads to a new $B_{(warm)}$ to calculate a new $A_{(warm)}$. Equations 2.11 and 2.12 show the final temperature dependent variables A and B.

$$A = A_{(cold)} + \left(A_{(warm)} - A_{(cold)}\right) \cdot \frac{(temp - 25)}{(warm - 25)}. \tag{2.11}$$

$$B = B_{(cold)} + \left(B_{(warm)} - B_{(cold)}\right) \cdot \frac{(temp - 25)}{(warm - 25)}. \tag{2.12}$$

The body diode behavior shown in Figure 10 is modeled very similar to the transfer characteristics and is defined by

$$I_{SD} = \begin{cases} 0 & U_{SD} \leq U_{th2} \\ D \cdot (U_{SD} - U_{th2})^2 & U_{SD} > U_{th2} \end{cases}. \quad 2.13$$

Grid points, which must be extracted from the body diode characteristics:

- I_{SD1} at U_{SD1} a bit after the threshold voltage
- I_{SD2} at U_{SD2} when a high amount of current flows
- (optional) ΔU_{th2} as an approximated difference of the threshold voltage between *warm* and "room" temperature. In general, this quantity contains a negative number.

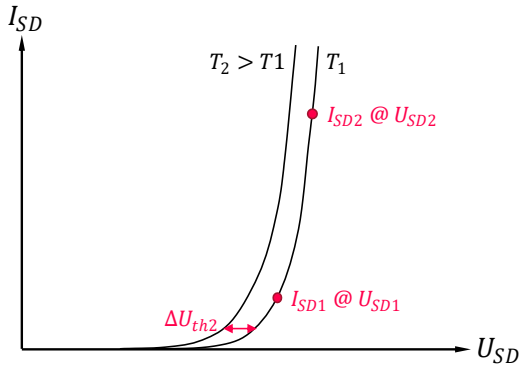


Figure 10: Typical body diode behavior of a MOSFET. Red markings show the points to extract for the modeling process

The parameter U_{th2} in Equation 2.13 is evaluated in the same way as shown in Equation 2.6 by just replacing U_{GS} by U_{SD} and I_{DS} by I_{SD}. The same is true for the amplification factor D which is evaluated as shown in Equation 2.7 after additionally inserting U_{th2} instead of $U_{th(cold)}$ and removing the multiplication factor 2. The optional temperature dependency is calculated in the same way as shown in Equation 2.8 by further replacing ΔU_{th1} by ΔU_{th2}.

Finally, the breakdown voltage is modeled by a series connection of an ideal diode and an ideal voltage source as it can be seen in Figure 6. This voltage source outputs the breakdown voltage. When U_{DS} exceeds that breakdown voltage, the ideal diode becomes conductive.

2.3 AC characteristics

The power MOSFET illustrated in Figure 11 shows the dynamic elements, i. e. the parasitic capacitors and inductances. Usually, power MOSFET datasheets provide the information of the stray capacitances with the parameters C_{iss} (input capacitance), C_{oss} (output capacitance) and C_{rss} (feedback capacitance). Therefore, if the datasheet values are taken to model the parasitic capacitances, these must be converted first according to Equations 2.14-2.16. Unfortunately, most datasheets do not provide information about the parasitic inductance of a power MOSFET since inductance generally appears as a phenomenon when current is flowing in loops.

$$C_{iss} = C_{GS} + C_{GD}. \quad 2.14$$

$$C_{oss} = C_{DS} + C_{GD}. \quad 2.15$$

$$C_{rss} = C_{GD}. \quad 2.16$$

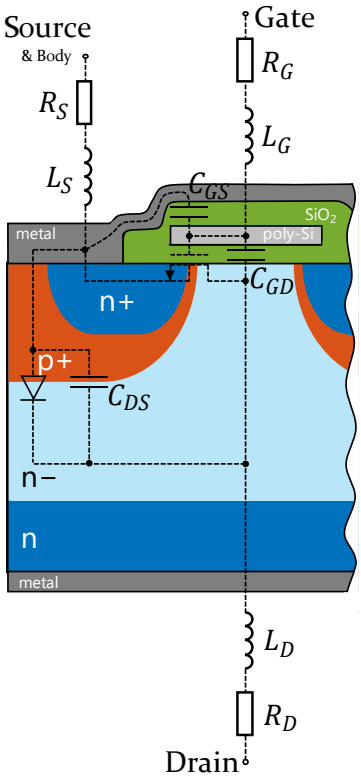


Figure 11: Equivalent circuit of a power MOSFET

The voltage-dependent capacitances C_{GD}, C_{DS} and C_{GS} are modeled via lookup tables. For this, Figure 6 shows the three voltage-controlled voltage sources, exceptionally[1] with the formula character C, $C_{GD} = f(U_{DG})$, $C_{DS} = f(U_{DG})$ and $C_{GS} = f(U_{DG})$ where the capacitance information to a specific U_{DG} is saved within a table. This approach is rather unique since usually these capacitances are set in dependence of the drain-source voltage. However, experiments in Subsection 4.3.4 indicate that the stray capacitances are not only dependent on the drain-source voltage but also whether the MOSFET is switched on or not. When C_{iss}, C_{oss}, and C_{rss} are measured with an LCR meter, the gate and source connection are usually shorted DC-wise while capacitances are shorted AC-wise depending on which parameter is measured. Datasheets thus specify stray capacitances with the MOSFET turned off, e. g. in [36]. This thesis assumes a linear dependency on the gate-source voltage, so that the stray capacitances depend on $U_{DG} = U_{DS} - U_{GS}$. The capacitances are treated as commonly seen in industry and literature[2]; only in SPICE the gate potential is used instead of the source potential. Capacitance values to voltages below $U_{DS} = 0\,V$ are assumed to be constant without slope which is performed by LTspice as default.

For instance, if $U_{GS} = 0\,V$ and $U_{DS} = 10\,V$ are applied, the voltage sources in SPICE look up in their tables to output the voltage defined by the user, e. g. $C_{GD} = 100\,pV$, $C_{DS} = 200\,pV$ and $C_{GS} = 300\,pV$. These voltages are passed to the three voltage-controlled current sources i_{GD}, i_{DS} and i_{GS} which multiply these voltages by the time derivative of the corresponding voltage drop. As an example, i_{GD} takes the value from C_{GD} and multiplies this voltage with the time derivative of the voltage drop between gate and drain. In this way, the electric current in Equation 2.17 is modeled under the assumption that the capacitance is not changing over time.

[1] In this thesis, voltage sources are usually identified by the formula symbol U. However, the lookup tables are an exception here; capacitance values are stored but these are output as voltage.

[2] Datasheets usually specify C_{iss}, C_{oss} and C_{rss} as a function of U_{DS}. In academic papers, C_{GS} is often assumed to be constant while C_{GD} depends on either U_{DG} or U_{DS}. However, C_{DS} is usually always expressed as a function of U_{DS}.

If parasitic resistances and inductances are modeled, the inner voltage drops must be considered because these elements are representing the bonding wires of the DUT. It should be noted that the use of lookup tables could negatively affect the convergence behavior of SPICE since a linear interpolation between the points results in non-differentiable points.

$$i_C = \frac{dQ}{dt} = \frac{dC}{dt} \cdot U(t) + C(t) \cdot \frac{dU}{dt}. \tag{2.17}$$

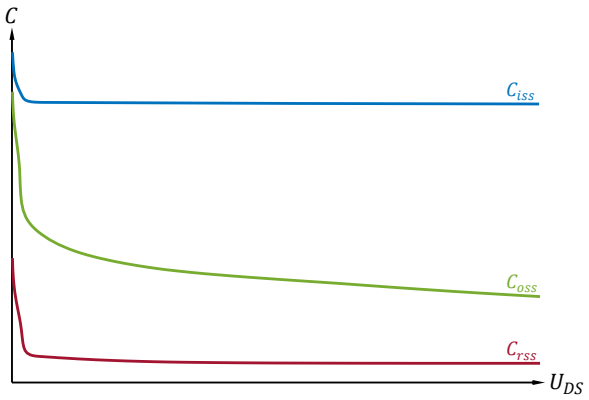


Figure 12: Typical voltage-dependent behavior of the parasitic capacitors of a power MOSFET. A superjunction MOSFET typically shows more complex curves as explained by Castro et al. [12]

If no datasheet is available or the information within the datasheet is not satisfying, the dynamic elements can be measured according to Liu et al. [37] and Fuchs et al. [31]. The measurement setup proposed by Fuchs et al. is implemented as shown in Figure 13. This setup has the advantage that a single measurement provides information about all stray capacitances and parasitic inductances. An isolated power supply is increasing U_{DS} stepwise whereas a VNA is capturing the scattering parameters (S-parameters) at gate and source for each step of U_{DS}. The captured S-parameters are then converted into impedance parameters (Z-parameters) by applying Equations 2.18 to 2.21. The transmission lines between VNA and DUT must show a 50 Ω wave impedance to avoid reflections. For safety reasons, each of the VNA input ports are secured by a 20 nF capacitor (DC block) which is capable to sustain high voltages up to 500 V.

$$Z_{11} = 50\,\Omega \cdot \frac{\left((1+S_{11})(1-S_{22}) + S_{12}S_{21}\right)}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}}. \tag{2.18}$$

$$Z_{12} = 100\,\Omega \cdot \frac{S_{12}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}}. \tag{2.19}$$

$$Z_{21} = 100\,\Omega \cdot \frac{S_{21}}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}}. \tag{2.20}$$

$$Z_{22} = 50\,\Omega \cdot \frac{\left((1-S_{11})(1+S_{22}) + S_{12}S_{21}\right)}{(1-S_{11})(1-S_{22}) - S_{12}S_{21}}. \tag{2.21}$$

Resistors with 1 $M\Omega$ are used as RF filters to guide the RF testing signals to the DUT. For accurate measurements, the filter elements must have a higher impedance than the internal stray capacitances. Experiments have shown that even geometrically small inductors exhibited their first resonance at relatively low frequencies and are thus unsuitable for the use up to the GHz range. That is why simple resistors are used as RF filter components in Figure 13. The parasitic capacitance of the filter is reduced by connecting the resistors in series.

The filter connecting the gate and source terminals of the MOSFET guarantees that the DUT remains turned off throughout the measurement. Nevertheless, a very small leakage current flows through the high-impedance drain-source channel. This current causes a voltage drop across the other two filters which must be taken into account when determining U_{DS}.

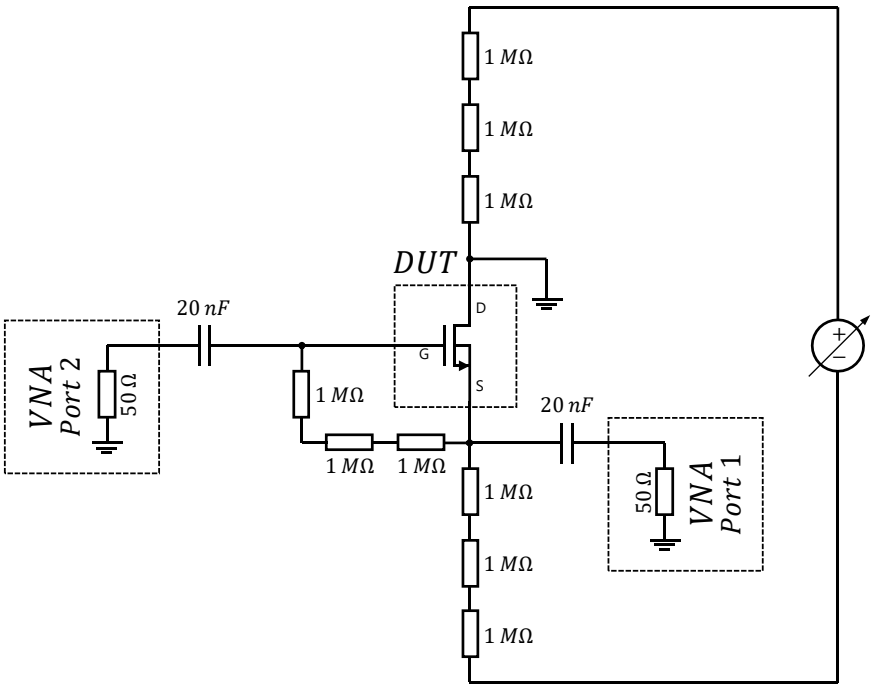


Figure 13: Setup to capture the AC characteristics of a MOSFET

All four Z-parameters show the shape of a typical RLC series connection impedance curve, i. e. at low frequencies, mainly the capacitances determine the impedance whereas the inductances dominate at high frequencies. Therefore, by inspecting the measuring points at low frequencies, the inductances and resistances shown in the simplified two-port network in Figure 14 can be neglected. The remaining capacitors form a delta (Δ) circuit. Thus, a Δ-Y transform is necessary to simplify the calculation [37]. If the measuring points are inspected at high frequencies, the inductances dominate which are already in Y configuration. In either case, as explained by Fuchs et al. [31], the Z-parameters can further be rewritten to determine Z_D, Z_G and Z_S respectively by

$$Z_D = Z_{12} \vee Z_{21}, \tag{2.22}$$

$$Z_G = Z_{22} - Z_{21} \vee Z_{22} - Z_{12}, \tag{2.23}$$

$$Z_S = Z_{11} - Z_{21} \vee Z_{11} - Z_{12}. \tag{2.24}$$

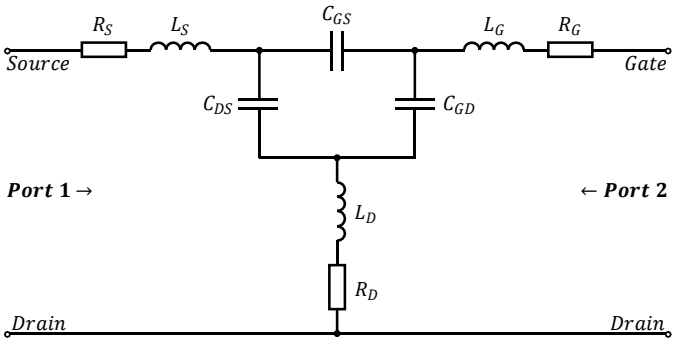


Figure 14: Simplified two-port network of the setup shown in Figure 13 considering ideal filter components

By taking the measurement points at low frequencies, the voltage-dependent capacitances can be calculated by putting Z_D, Z_G and Z_S into the Equations 2.25, 2.26 and 2.27.

$$C_{GD} = \frac{1}{2\pi f} \cdot \Im\left\{\frac{Z_S}{Z_G Z_D + Z_D Z_S + Z_G Z_S}\right\}. \quad 2.25$$

$$C_{DS} = \frac{1}{2\pi f} \cdot \Im\left\{\frac{Z_G}{Z_G Z_D + Z_D Z_S + Z_G Z_S}\right\}. \quad 2.26$$

$$C_{GS} = \frac{1}{2\pi f} \cdot \Im\left\{\frac{Z_D}{Z_G Z_D + Z_D Z_S + Z_G Z_S}\right\}. \quad 2.27$$

The parasitic inductances can be calculated by taking the measurement points at high frequencies and putting Z_D, Z_G and Z_S into the Equations 2.28, 2.29 and 2.30.

$$L_D = \frac{1}{2\pi f} \cdot \Im\{Z_D\}. \quad 2.28$$

$$L_G = \frac{1}{2\pi f} \cdot \Im\{Z_G\}. \quad 2.29$$

$$L_S = \frac{1}{2\pi f} \cdot \Im\{Z_S\}. \quad 2.30$$

Although parasitic resistances are not part of the AC characteristics, it is worth mentioning here as these can be calculated by taking the real part of Z_D, Z_G and Z_S.

$$R_D = \Re\{Z_D\}. \quad 2.31$$

$$R_G = \Re\{Z_G\}. \quad 2.32$$

$$R_S = \Re\{Z_S\}. \quad 2.33$$

2.4 Simulation test benches

The generated models need to be verified. The following characteristics can be quickly checked via simulations since this information is usually available in datasheets:

- Output characteristics: $I_{DS} = f(U_{DS}, U_{GS})$
- Transfer characteristics: $I_{DS} = f(U_{GS})$
- Diode characteristics: $I_{SD} = f(U_{SD})$
- Capacitances: $C_{iss} = f(U_{DS})$, $C_{oss} = f(U_{DS})$, $C_{rss} = f(U_{DS})$
- Gate-charge: $U_{GS} = f(Q_G)$

While the first characteristics have already been clearly described, the gate-charge plot requires further explanation. Figure 5 shows a typical gate-charge curve which can be achieved by the simple simulation setup shown in Figure 15 [32]. A typical datasheet clearly states at which I_{DS} and U_{DS} the gate-charge plot was recorded, and the setup in Figure 15 must be adapted accordingly.

The voltage at the gate connection is increased linearly. As long as the MOSFET is in its subthreshold region, nearly all current from the current source flows through the diode. If the MOSFET is then switched on, exactly as much current is driven through the MOSFET as it is defined in its current source. At the latest when the entire current of the current source flows through the DUT, the potential at the drain connection drops from the predefined test voltage U_{DS} down to $R_{DS(on)} \cdot I_{DS}$. For the final gate-charge plot, the current through the voltage source U_{GS} is integrated and plotted as x-axis.

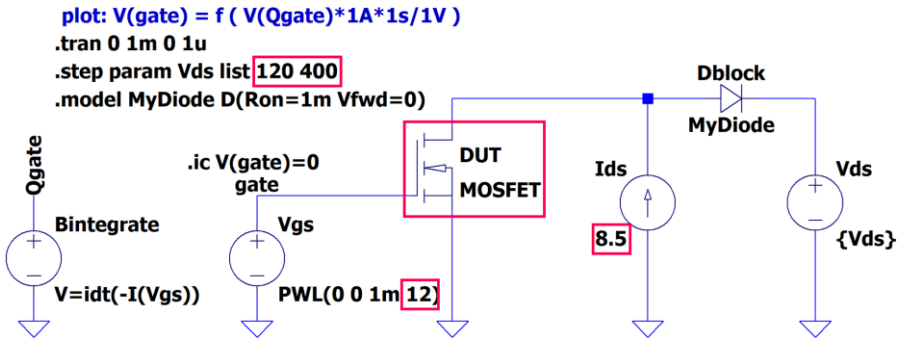


Figure 15: Proposed LTspice schematic to simulate the gate-charge plot. The red markings need to be adapted according to the gate-charge plot given in the datasheet

Whether or not a datasheet is provided, the following measurements are strongly recommended. The universal test circuit shown in Figure 7 can be adapted for different values (e. g. for R_{load}, R_{gate}, U_{gate} or U_{src}) to create different test conditions. The captured values for U_G, U_S and U_D can then be compared with the simulated values obtained by the test bench shown in Figure 16. The gate driver is assumed to be an ideal voltage source in this work. Both rise and fall time were analyzed with an oscilloscope and checked with the datasheet beforehand. However, if the manufacturer provides a model for the gate driver, it is recommended to use this model instead.

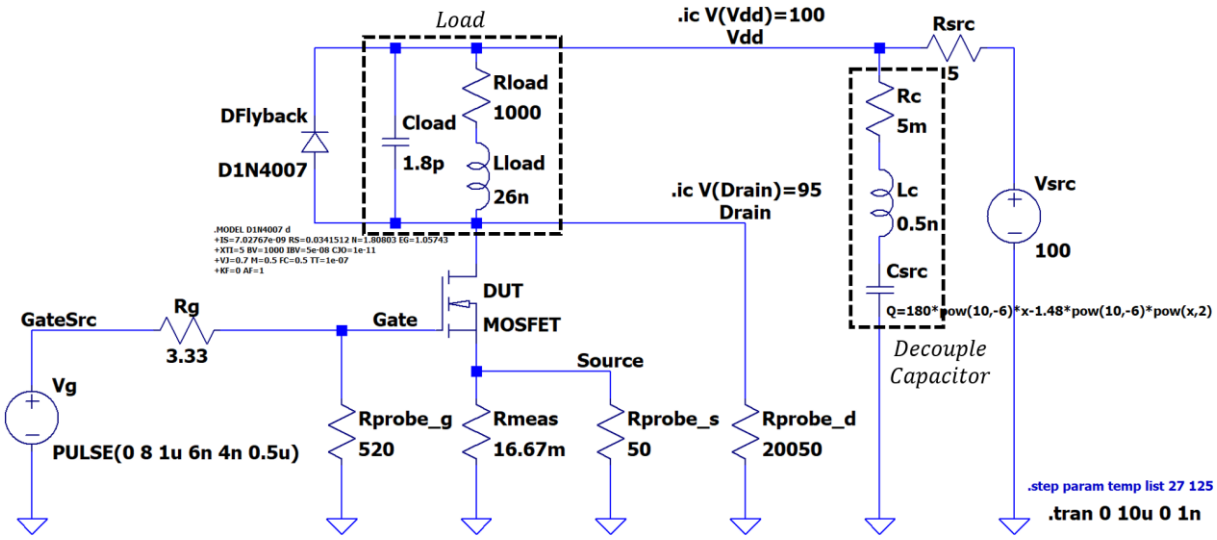


Figure 16: Proposed LTspice test bench to allow comparison between simulated and measured values. Exemplary lumped-element models for the load and the decouple capacitor are shown

Since this thesis pays special attention to the intended use for EMC simulations, the load and the decouple capacitor must be further analyzed by its frequency behavior. For this, 1-port and 2-port measurements according to Sandler [38] must be accomplished with a VNA.

In the case of the load, a simple 1-port measurement can be performed. In a 50 Ω system, the impedance can be calculated from the measured reflection coefficient Γ by using Equation 2.34. Further, the impedance can be utilized to find an appropriate equivalent lumped-element model.

$$Z_{DUT} = 50\,\Omega \cdot \frac{1+\Gamma}{1-\Gamma}. \qquad 2.34$$

In the case of the decouple capacitor, a 2-port shunt measurement is recommended. In a 50 Ω system, the impedance can be calculated from the measured S-parameters by

$$Z_{DUT} = 25\,\Omega \cdot \frac{S_{21}}{1-S_{21}}. \qquad 2.35$$

In this thesis, multilayer ceramic chip capacitors (MLCC) are used because they usually exhibit a low inductance. However, since normally a power MOSFET is operated at 100 V or higher, the voltage dependency of the ceramic decouple capacitor must be taken into account. A setup to capture the S-parameters with simultaneous change of the bias voltage of the capacitor is given in Figure 17. The resistors form an RF filter similar to the setup in Figure 13. However, the values for the resistances cannot be chosen higher without sacrificing additional waiting time because of the high capacitance of the DUT. According to Vishay Intertechnology, Inc. [39], surface-mounted resistors with high resistances tend to have higher parasitic capacitances. Therefore, the smallest 1 $k\Omega$ resistor is placed closest to the DUT because it has a larger impedance at very high frequencies than the largest 100 $k\Omega$ resistor. Ultimately, the capacitor can be modeled voltage-dependent by specifying the capacitance with an expression for the charge $Q = C \cdot U$.

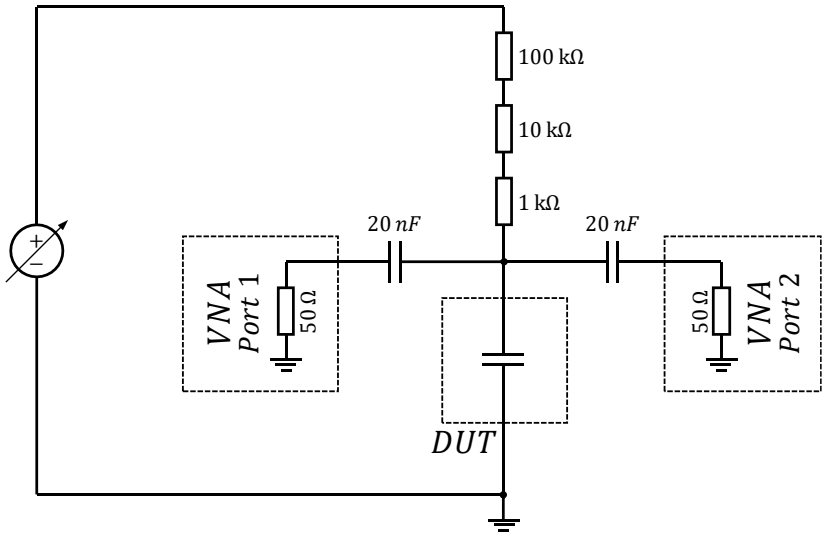


Figure 17: Setup to perform a 2-port shunt measurement with a variable bias voltage

3
Model Creation

In this chapter, the presented method is applied to create models for the superjunction [33] and the silicon carbide [34] field-effect transistor. Two versions are presented; first, a version by utilizing the key information of a datasheet, and second, by performing measurements with the test structure explained in Section 2.1. For the measurements, a 50 Ω, 500 *MHz* oscilloscope (MSO6054A, Agilent Technologies, Inc., California, US) was used. To power up the test circuit, two power supplies are required. The first power supply (SM660-AR-11, Delta Elektronika B.V., NL) was used for the main side and the other power supply (EL302T, Thurlby Thandar Instruments Ltd., GB) was supplying the gate driver (EiceDRIVER [40], Infineon Technologies AG, DE). A 555 timer IC (LMC555, Texas Instruments, Inc., Texas, US) configured as monostable multivibrator was used to generate the pulse for the gate driver. The current sensing resistor (ERJL03KF10CV, Panasonic Corp., JP) and the inductive load, an air coil (0806SQ-12NGLC, Coilcraft, Inc., Illinois, US), are characterized in Section 4.1. The models are created within the simulation software LTspice but MATLAB (MATLAB R2019a, The MathWorks, Inc., Massachusetts, US) is used to generate all plots. Figure 18 presents a created model from the proposed model in Figure 6. All model parameters can be found in the Appendix 7.2 in detail.

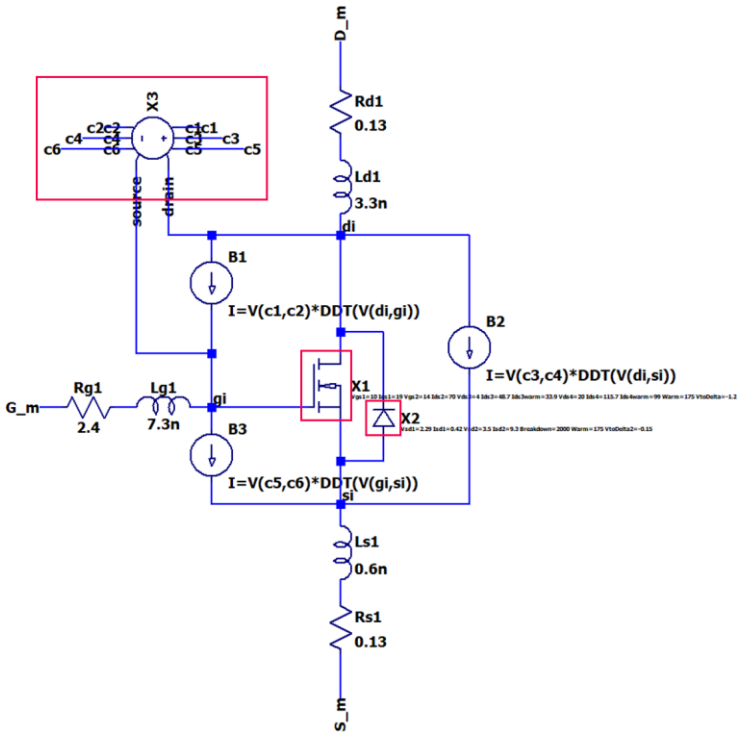


Figure 18: Proposed power MOSFET model in LTspice. Red rectangles indicate symbols which contain voltage-controlled subcircuits. The model for the IMZ120R060M1H SiC FET created via measurements is shown as an example. Note that the capacitances are determined using the voltage drop U_{DG} instead of U_{DS}

3.1 DC characteristics cont'd

In Figure 18, the two subcircuits relevant for the static characteristics are X1 and X2. The first subcircuit X1 contains an arbitrary behavioral current source which is responsible to output the current in Equation 2.5 and is depicted in Figure 19.

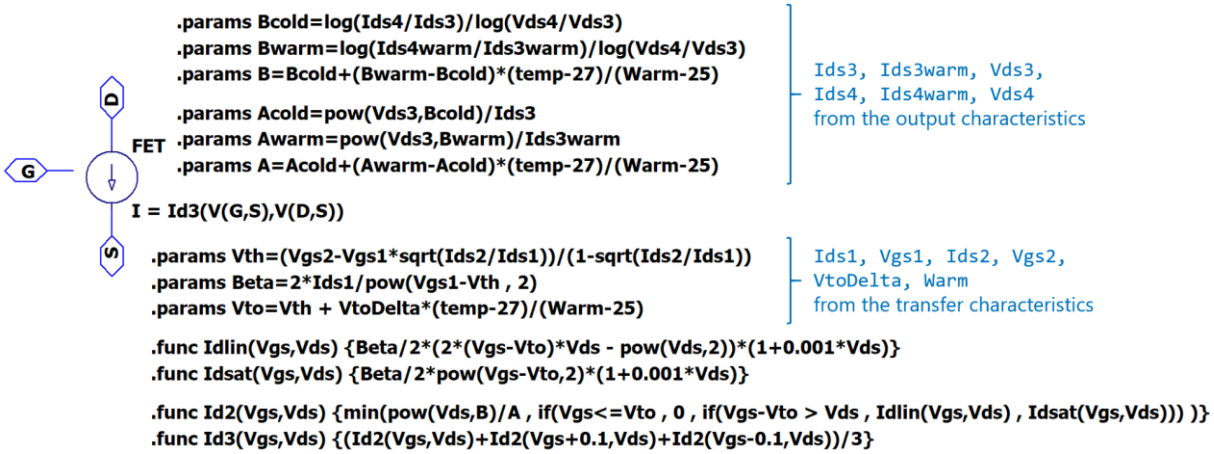


Figure 19: Arbitrary behavioral current source in LTspice in order to output the proposed formula for the DC current

As it is explained in Section 2.2, twelve parameters (eight if temperature dependency is neglected) are passed to the subcircuit. Figure 21 to Figure 24 show the corresponding graphs from where these parameters are taken from. The plots from the datasheets are additionally labeled in red at those locations where the corresponding parameters were extracted. Figure 20 and Figure 25 show the characteristics of the generated datasheet models. This model could be further expanded, e. g. by including the dependence of $R_{DS(on)} = f(I_{DS})$ mapped within the variable A in Equation 2.11 to provoke a slope in the saturated transfer characteristics.

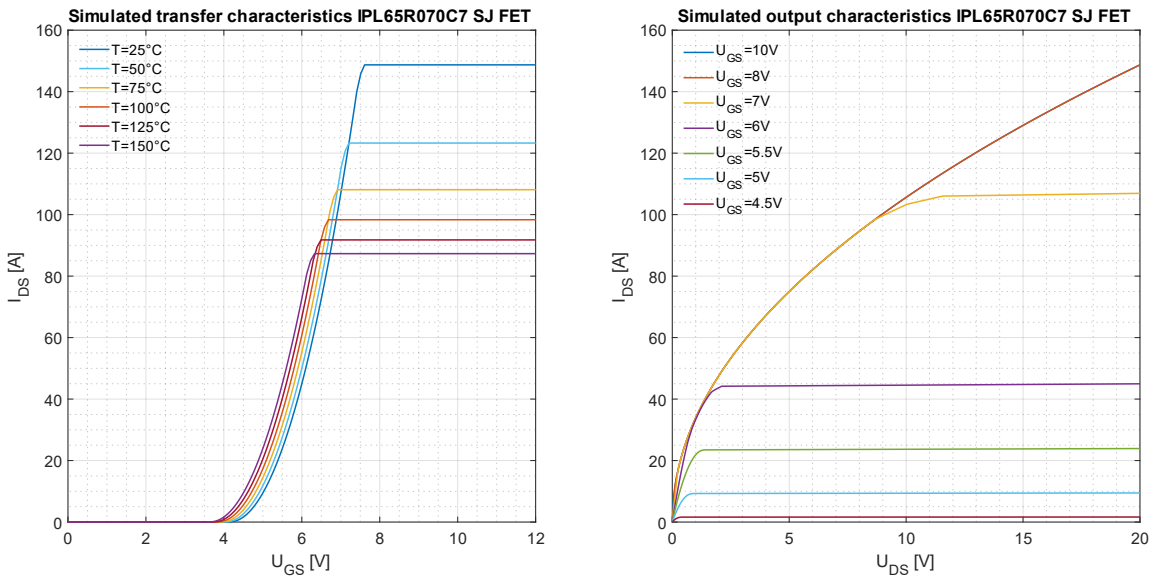


Figure 20: Characteristics of the simulated SJ MOSFET model based on the datasheet. (a) Transfer characteristics. (b) Output characteristics

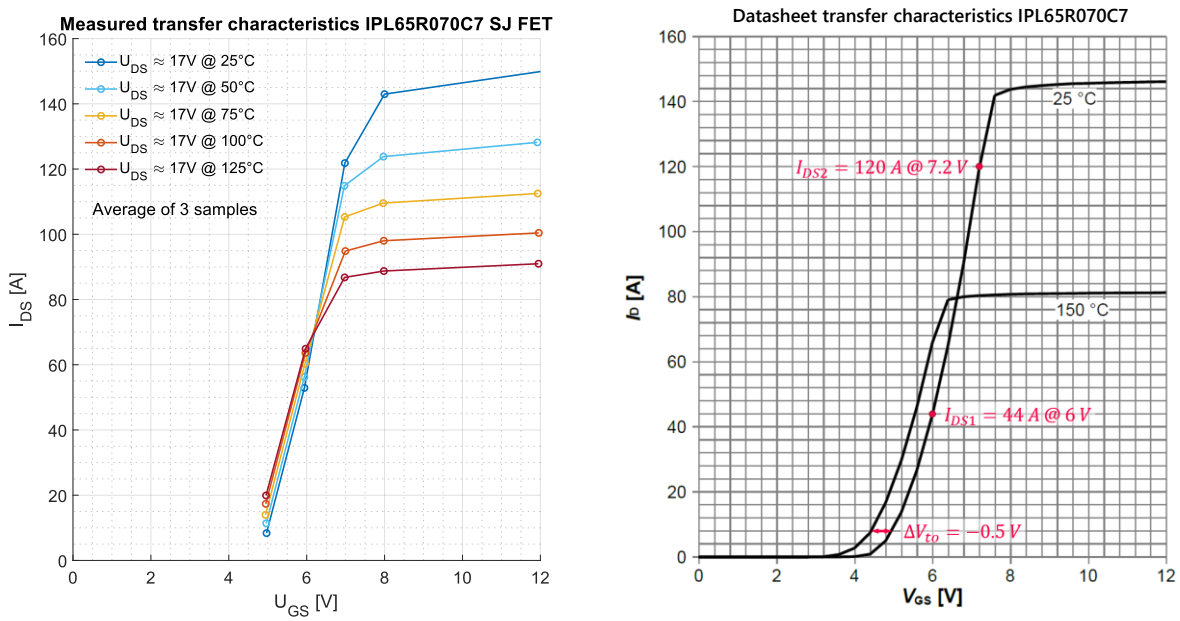


Figure 21: Transfer characteristics of the SJ MOSFET. (a) Measured at five different temperatures with the proposed test circuit. Average of 3 samples. (b) Plot taken from the datasheet at U_{DS} = 20 V [33] with red markings located at exemplary positions to extract the required information. Note that the drain-source voltage and the maximum temperature differs between the plots

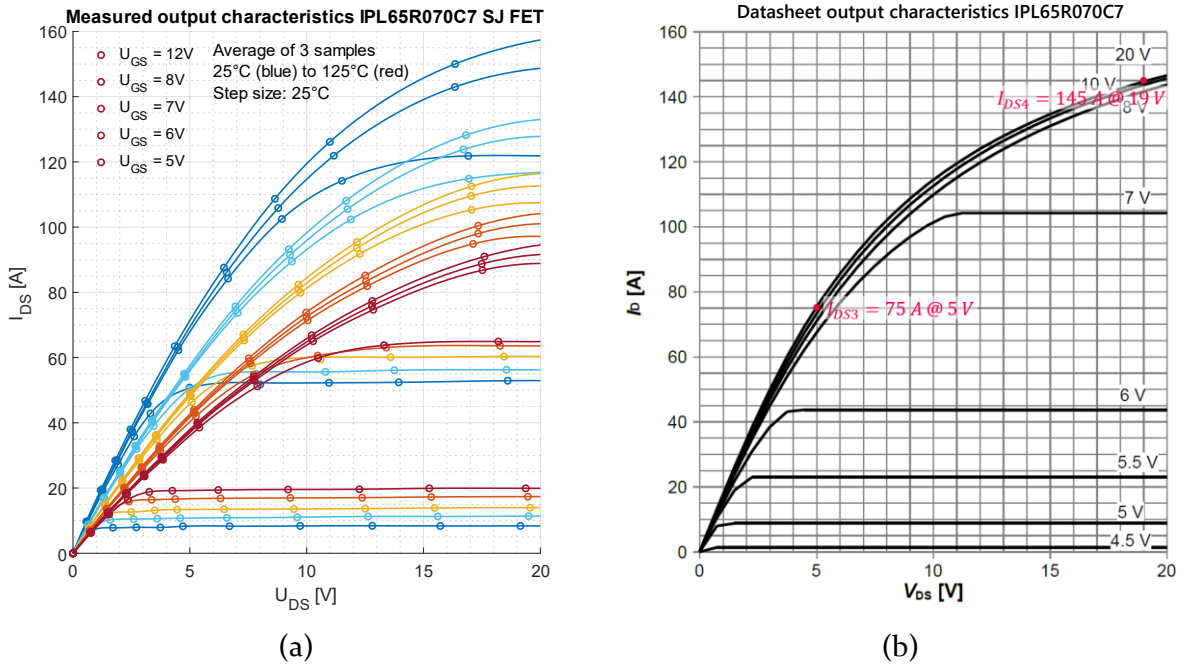


Figure 22: Output characteristics of the SJ MOSFET. (a) Measured at five different temperatures with the proposed test circuit. Average of 3 samples. (b) Plot taken from the datasheet at 25°C [33] with red markings located at exemplary positions to extract the required information

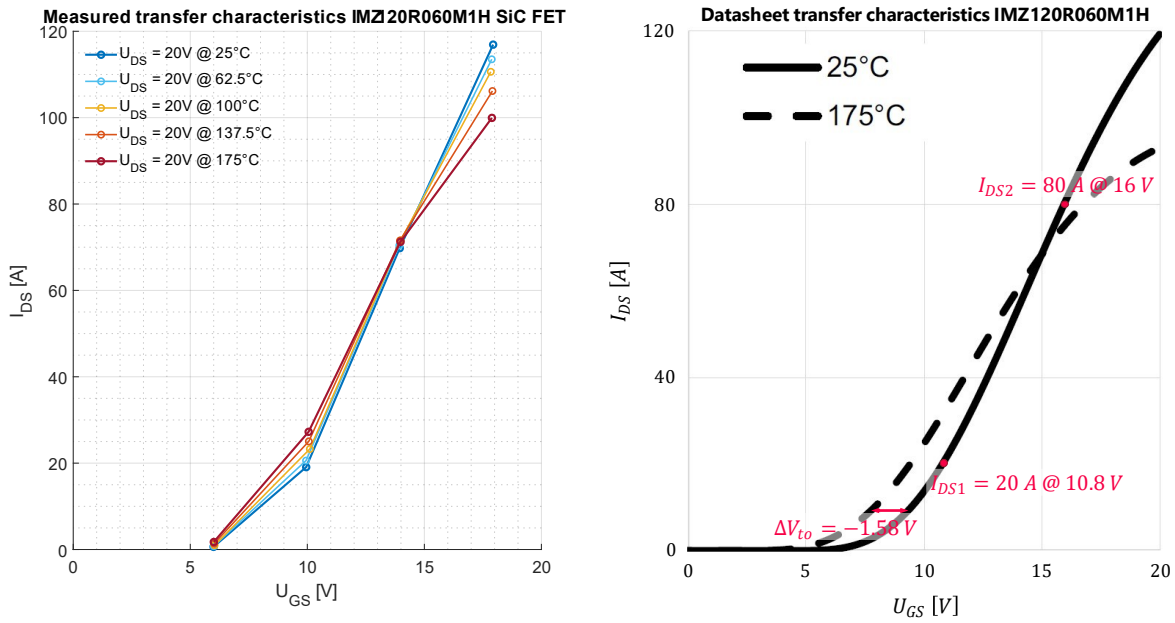


Figure 23: Transfer characteristics of the SiC MOSFET. (a) Measured at five different temperatures with the proposed test circuit. (b) Plot taken from the datasheet at U_{DS} = 20 V [34] with red markings located at exemplary positions to extract the required information

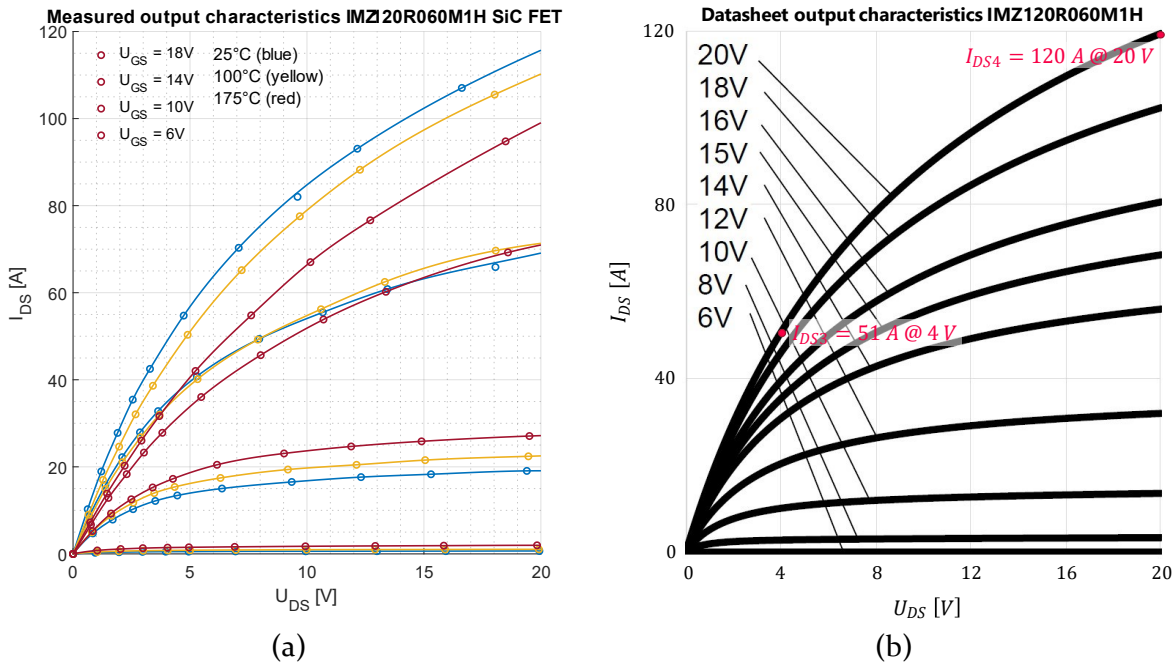


Figure 24: Output characteristics of the SiC MOSFET. (a) Measured at three different temperatures with the proposed test circuit. (b) Plot taken from the datasheet at 25°C [34] with red markings located at exemplary positions to extract the required information

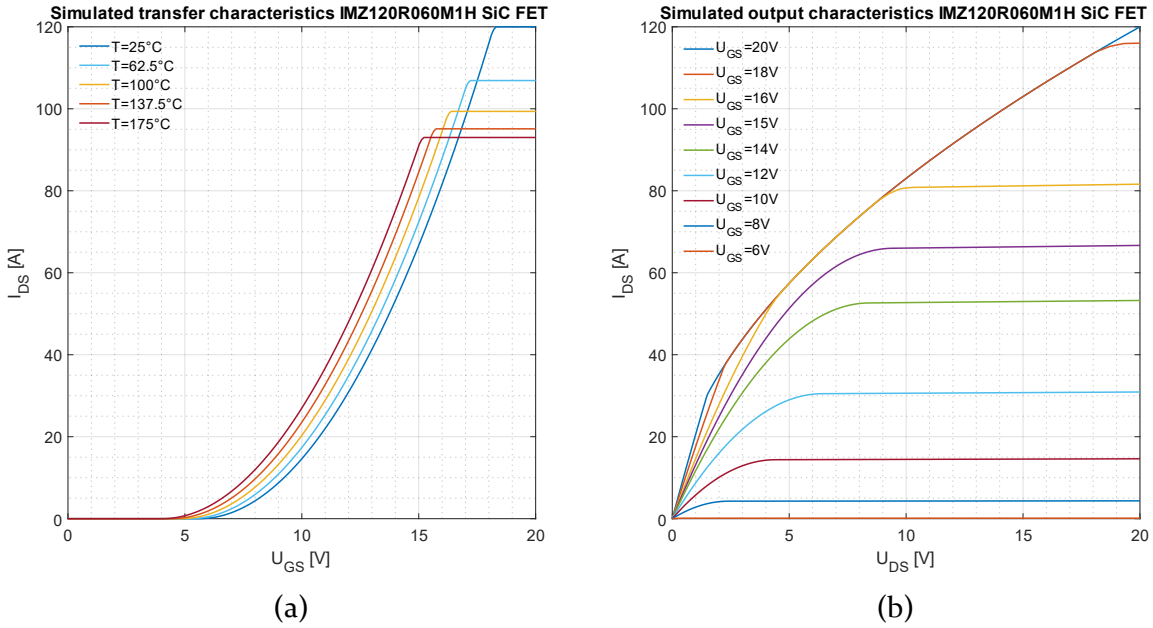


Figure 25: Characteristics of the simulated SiC MOSFET model based on the datasheet. (a) Transfer characteristics. (b) Output characteristics

Comparing Figure 20 (SJ) with Figure 25 (SiC), the limitations of the proposed model become apparent. Since the superjunction MOSFET is modeled very well right away, the SiC MOSFET model would require further finetuning. In this case, a higher channel length modulation factor λ would increase the slope of the output characteristics.

A deviation between datasheet and measured values can be noticed when analyzing Figure 21 to Figure 24. High currents are more affected by this deviation and show a higher current than the datasheet. The exact underlying cause is unclear, but it is believed that either the current sensing resistor generally differs slightly from 16.67 Ω, or high currents heat up that resistor and increase its value. Assuming that the same current is flowing, a higher voltage drop is captured at the sensing resistor. Thus, a higher value for the current is calculated. Section 4.3 shows transient measurements where this deviation can be noticed as well. A 1-port characterization of the current sensing resistor is shown in Figure 32ef.

The second subcircuit `X2` contains the body diode mapped as arbitrary behavioral current source shown in Figure 26. In addition, the breakdown voltage is simulated by the biased diode. The diode characteristics can be measured with the proposed test circuit illustrated in Figure 7 by inverse-biasing the main side. This power supply must be pulsed to prevent measurement errors caused by self-heating of the DUT. The diode current I_{SD} and the voltage U_{SD} can be measured with channel 2 and 3 of the oscilloscope in 1 $M\Omega$ mode.

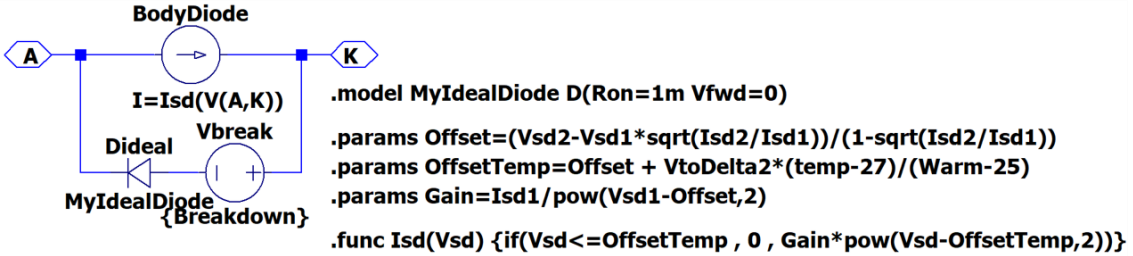


Figure 26: Arbitrary behavioral current source in LTspice as a representation for the body diode. The biased diode defines the breakdown voltage

Figure 27 shows reasonable results for the simulation models since the body diode is expressed by the simple Equation 2.13. Examining Figure 27c, it is noticeable that the characteristics for different temperatures cross at very high currents. Therefore, a change in temperature does not only change the threshold voltage but the slope as well. The Shockley diode equation also allows this change in slope. In this thesis, however, the slope is considered to be independent of temperature and thus is not modeled.

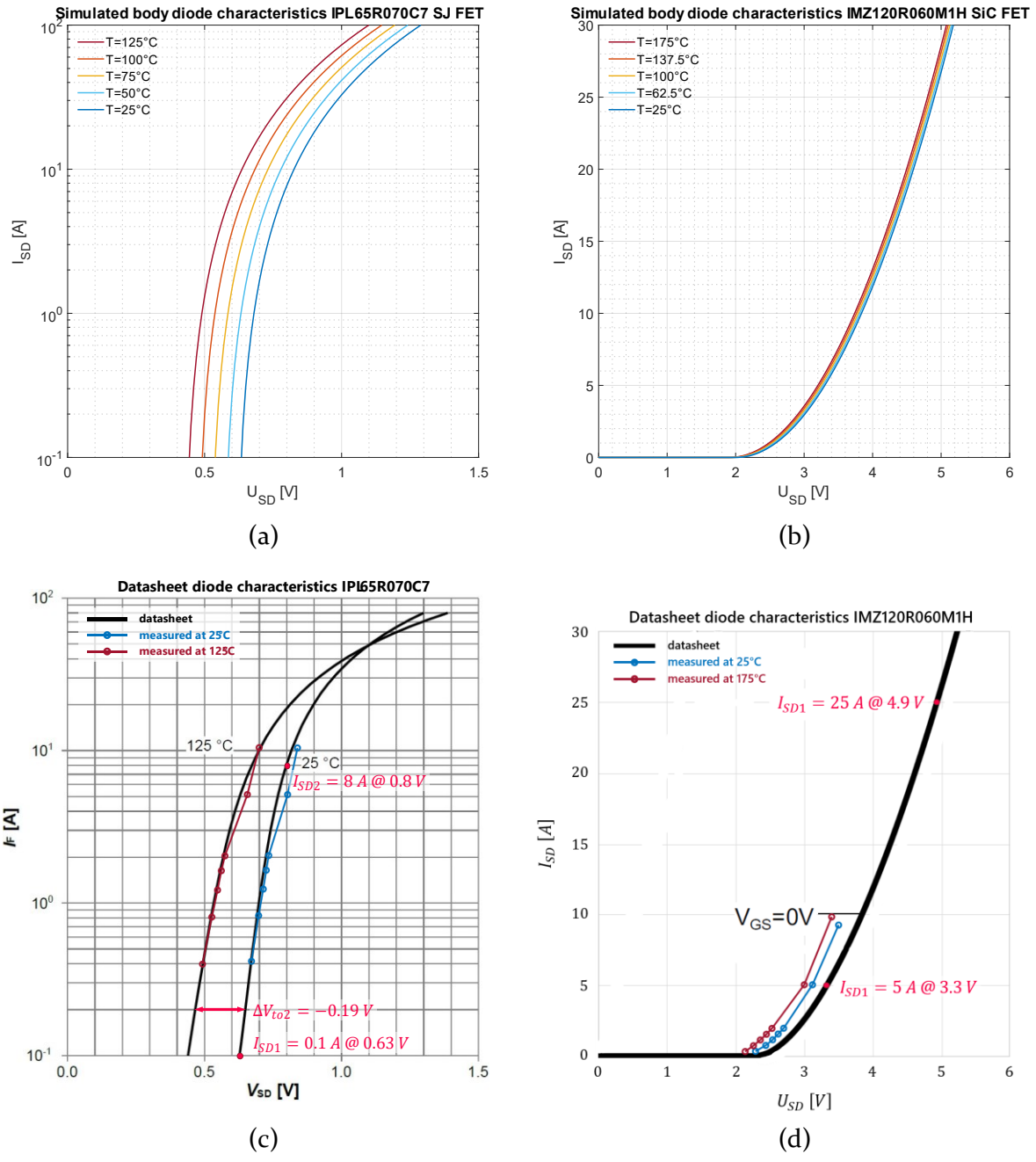


Figure 27: Characteristics of the body diode. The top graphs show the simulated models based on the datasheet. The bottom graphs show the measurement results overlayed on the datasheets [33], [34] with red markings located at exemplary positions to extract the required information. (a, c) SJ. (b, d) SiC

3.2 AC characteristics cont'd

In Figure 18, the subcircuit X3 is relevant for depicting the AC characteristics of the proposed model. This subcircuit includes three voltage-controlled voltage sources which are all controlled by the drain-gate voltage U_{DG}. In this section $U_{GS} = 0\,V$ is assumed. In this way, depending on U_{DS}, the corresponding values stored within the tables (C_{GD}, C_{DS} and C_{GS}) are forwarded to the voltage-controlled current sources depicted in Figure 18. These current sources are then driving the resulting currents according to Equation 2.17.

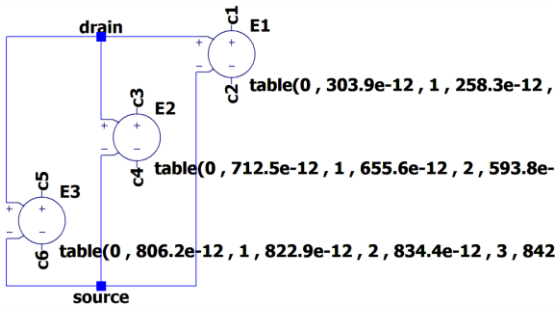


Figure 28: Voltage-dependent voltage sources in LTspice to output the capacitance values stored within their tables. Only a snippet of the tables is shown. Note that although the net is named "source", it is linked to the gate connection in Figure 18

To perform the measurement illustrated in Figure 13, a VNA (ZVL3 Network Analyzer, Rohde & Schwarz GmbH & Co. KG, DE) and an SMA calibration kit (TOSLKF50A-20, Anritsu K.K., JP) were used. The measured data for the superjunction MOSFET were kindly provided by Lukas Spielberger, BSc [31] shown in Figure 29a. The measured results for the silicon carbide MOSFET can be seen in Figure 29b. The formulas presented in Section 2.3 were applied. After subsequent measurements showed the same qualitative curve, extrapolation was performed from 30 V to 200 V.

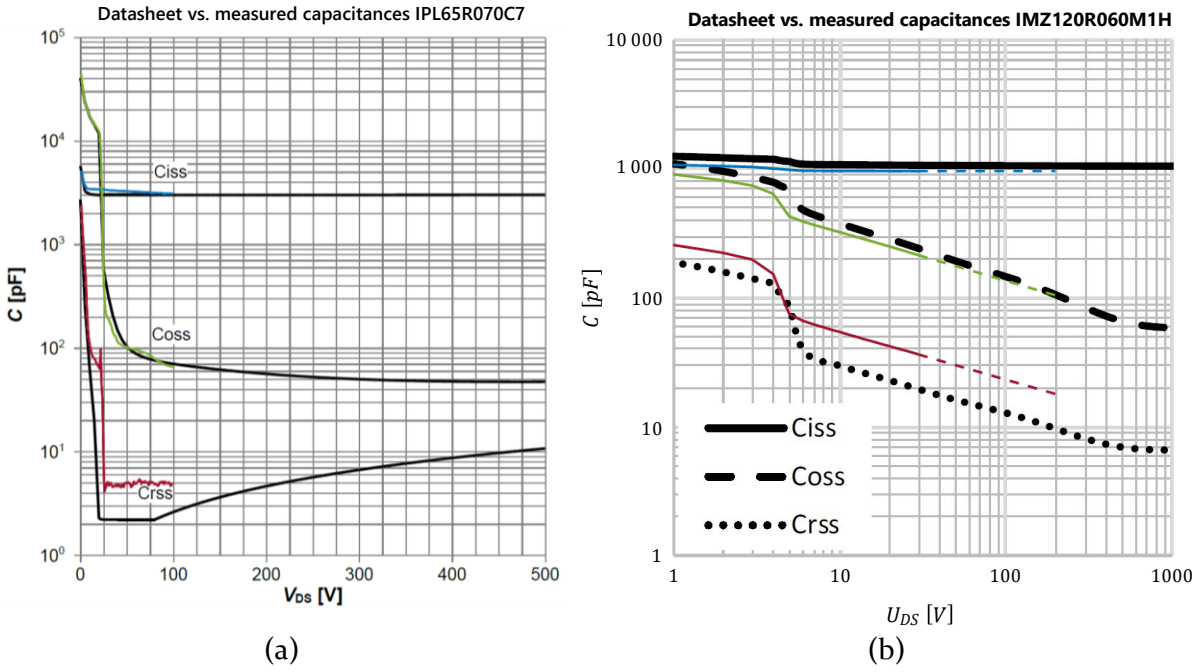


Figure 29: AC characteristics. The measurement results are overlayed on the datasheets. (a) SJ [33]. (b) SiC [34]. The dashed lines show an extrapolation of the measured values

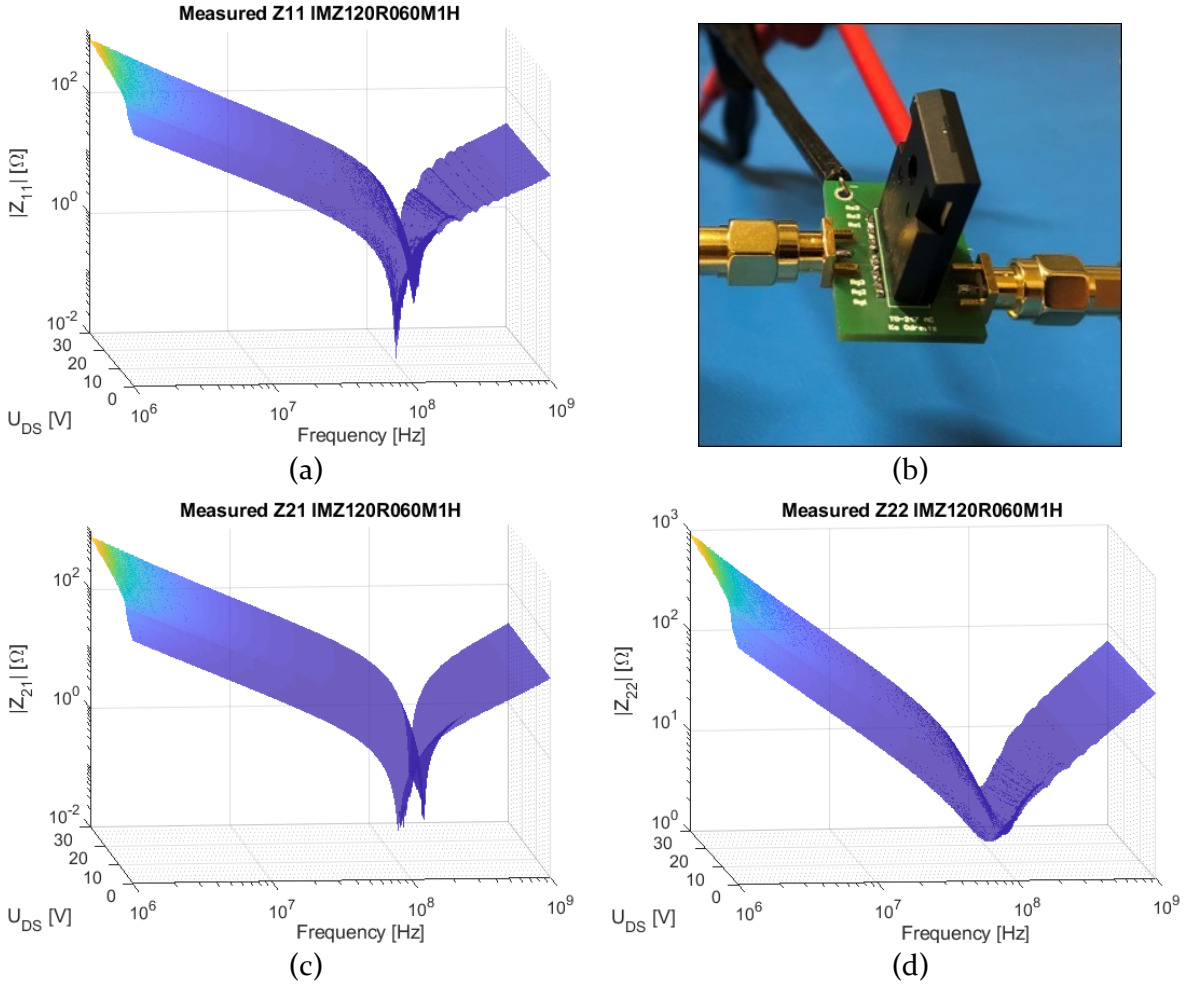


Figure 30: Measurement of the SiC FET AC characteristics. (a) Z11. (b) IMZ120R060M1H soldered on the test PCB presented in Figure 13 and connected to the VNA and power supply. (c) Z21. (d) Z22

Figure 30acd shows the Z-parameters of the SiC MOSFET after applying Equations 2.18-2.21 to the measured S-parameters. Sharp changings between $U_{DS} = 4\,V$ and $5\,V$ are visible which are caused by the voltage-dependent stray capacitances. These capacitances are calculated by taking the frequency points within the $1\,MHz$ range and applying the Equations 2.14-2.16 and 2.22-2.27.

The inductances of the bonding wires are calculated with the Equations 2.28-2.30. By observing Figure 31a, it becomes clear why the frequency points within the $1\,GHz$ range must be taken in order to obtain relatively constant values for the parasitic inductances. The presented gate inductance shows very small influence of the drain-source voltage and can be valued with $7.3\,nH$. This is the reason why the parasitic inductance of the proposed model is depicted without voltage-dependency as opposed to the capacitances.

The resistances of the bonding wires are determined with the Equations 2.31-2.33. Figure 31b shows the gate resistance as an example. Although no statement can be made within the low frequency range, a general frequency dependence is noticeable. However, this dependency is neglected, and the resistance is determined by selecting a value within the $10\,MHz$ to $100\,MHz$ frequency range. In case for the gate resistance, $2.4\,\Omega$ was chosen as the final model shows in Figure 18.

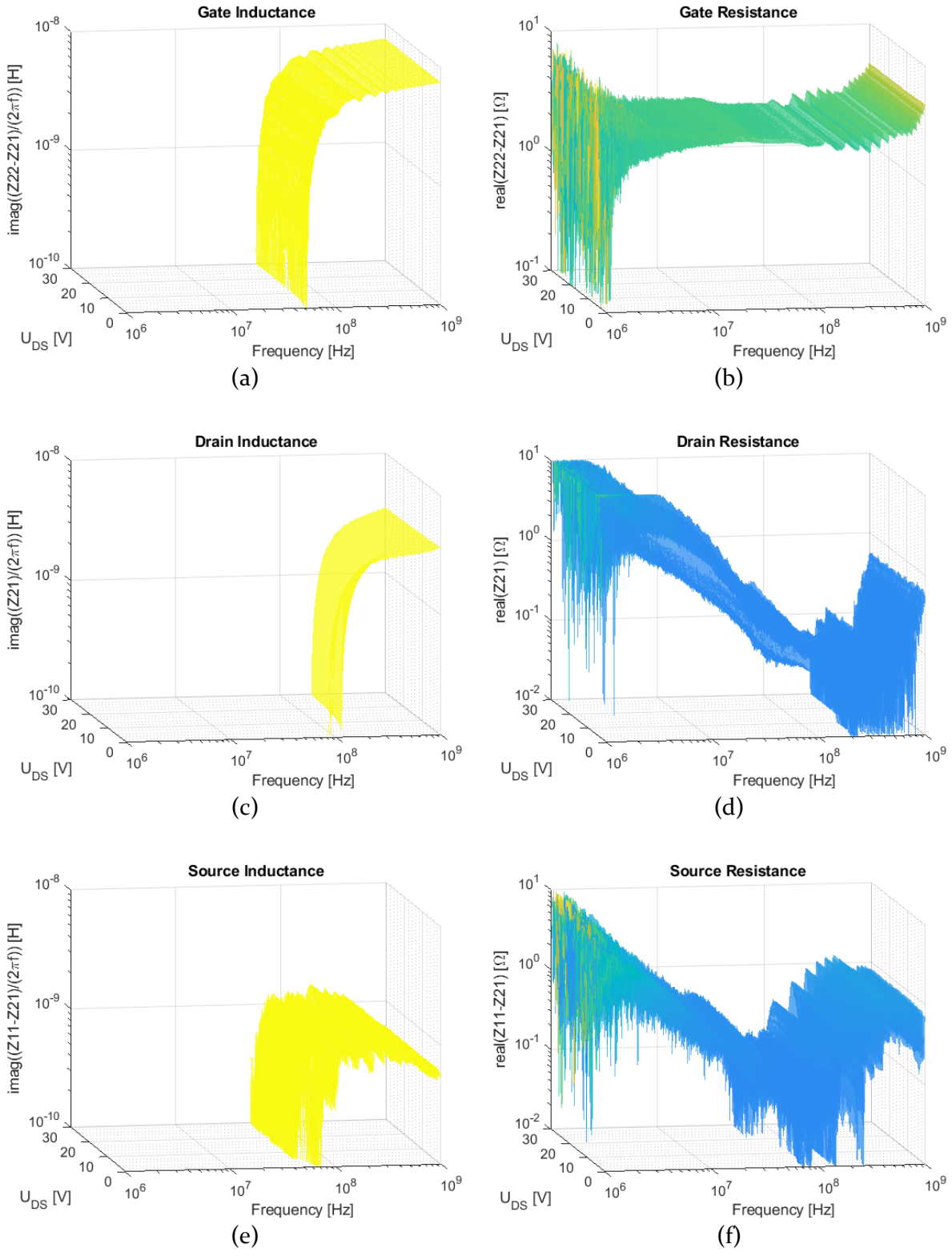


Figure 31: Calculation of the SiC FET characteristics of the bonding wires. (a) Gate inductance. (b) Gate resistance. (c) Drain inductance. (d) Drain resistance. (e) Source inductance. (f) Source resistance

4
MODEL VERIFICATION

The previous chapter presented the modeling procedure of a superjunction [33] and a silicon carbide [34] field-effect transistor by performing DC and AC analyses. This chapter verifies the created models by performing transient analyses by measurements and simulations. Two different load resistors were used: a 22 Ω and a 1000 Ω resistor. The first part of this chapter shows the characterization of passive components which is necessary to allow better comparisons between measurements and simulations. After that, the simulation test bench depicted in Figure 15 is used to create gate-charge plots to enable a comparison with the plots provided from the datasheets. Finally, transient measurements are compared with simulations performed with the test bench in Figure 16; first with a model fully generated by measurements, second with a model fully generated by the extracted values from the datasheet, and third, with the model provided from the manufacturer. The manufacturer does not provide a model for the analyzed SiC FET but recommends to use the IMBG120R060M1_L3 model instead [34]. For both power MOSFETs, the so-called level 3 (L3) model from the manufacturer was used [41].

4.1 Characterization of passive components

Two different loads, the current sensing resistor and the decouple capacitor, all built with surface-mounted components, were characterized with the help of the VNA in order to estimate their parasitic elements. 1-port measurements were performed to characterize the 1000 Ω and 22 Ω loads and the 16.67 $m\Omega$ current sensing resistor. Equation 2.34 shows the relation between the measured reflection coefficient Γ and the calculated impedance. The load is modeled as an RLC parallel circuit with resistance in series with the inductor as depicted in the simulation test bench in Figure 16; its impedance is determined by Equation 4.1. The current sensing resistor is modeled as RL series circuit, but this model is not considered in the simulation test bench since its inductance was determined with only 1 nH.

$$Z_{RL||C} = \frac{(R + j\omega L) \cdot \frac{1}{j\omega C}}{(R + j\omega L) + \frac{1}{j\omega C}} = \frac{R + j\omega L}{1 - \omega^2 LC + j\omega RC}. \qquad 4.1$$

Figure 32 shows the results of the 1-port measurements compared with the simulated lumped-element models. The load is modeled with 26 nH in series but its parallel capacitor differs; the 1000 Ω load includes 1.8 pF whereas the 22 Ω load is modeled with 1 pF. A statement about the current sensing resistor cannot be made since the dynamic range of the measuring device is not sufficient for the small 16.67 $m\Omega$ resistance, but a low inductance of 1 nH can be read out. Reducing the intermediate frequency (IF) filter bandwidth of the VNA could increase its

dynamic range. According to Sandler [38], a 2-port measurement is recommended to determine such low impedances. However, due to the special arrangement of the current sensing resistors, only a 1-port measurement was performed.

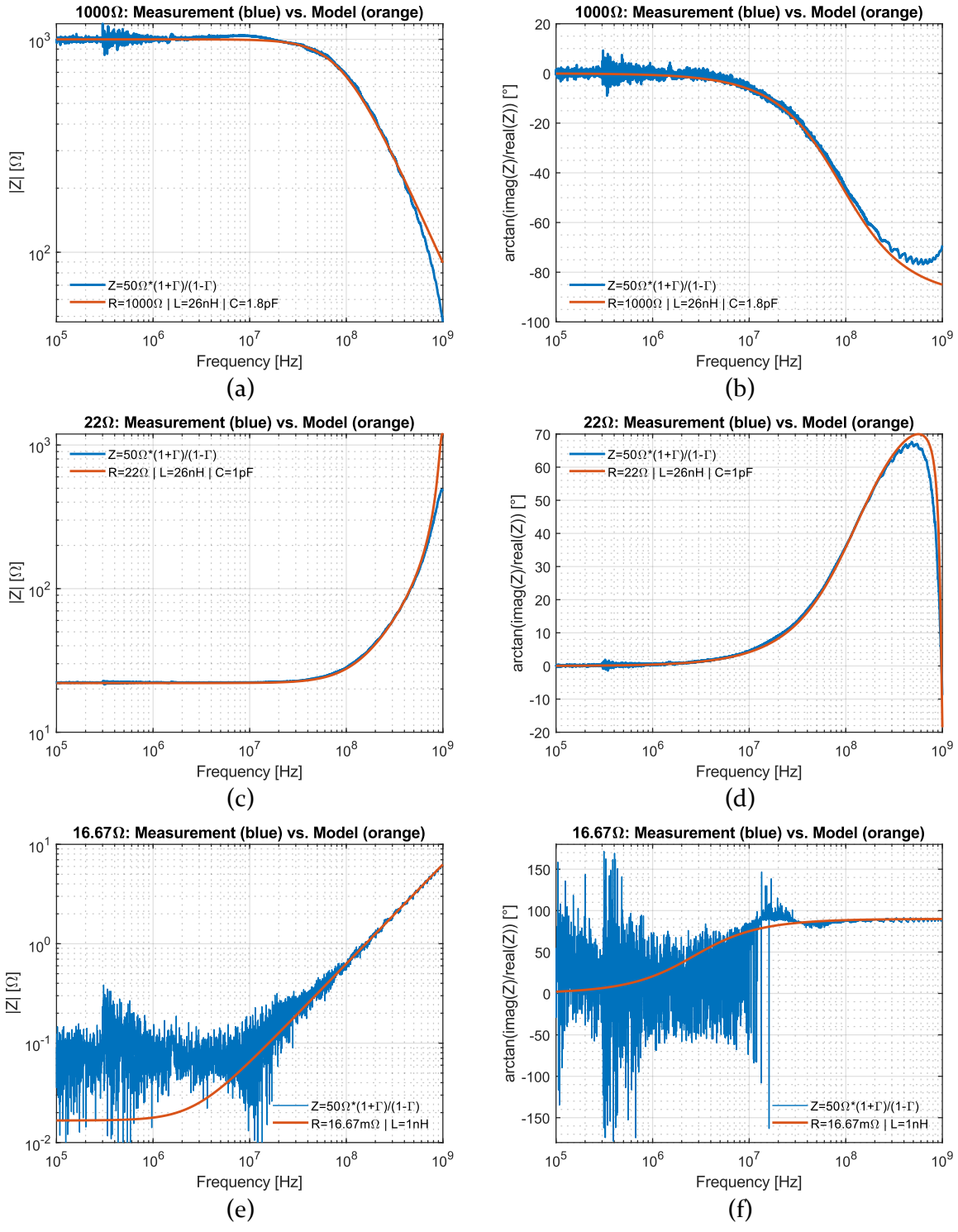


Figure 32: 1-port characterizations; left: impedance curves, right: phase plots. (a, b) 1000 Ω load. (c, d) 22 Ω load. (e, f) 16.67 mΩ current sensing resistor

Twenty X7S multilayer ceramic chip capacitors (CGA9N3X7S2A106K230KB, TDK Corp., JP) with 10 μF each were soldered together to form a big decoupling capacitor. Such a large capacitance is needed so that 100 A or more can flow through that capacitor and not through the power supply cables. Thus, the current loop can be kept small and the inductance minimized [42]. The same capacitor was soldered multiple times to avoid unwanted parallel resonant circuit effects. However, as shown in Figure 33abc, multiple peaks at the resonance frequency region can be observed. It is assumed that those are caused because of different lead lengths between the single components. The measurement setup is illustrated in Figure 17, and Equation 2.35 is applied to calculate the impedance of the DUT from the S-parameters.

A simple RLC series circuit is used to model the decouple capacitor. Ceramic capacitors show low parasitic inductance but exhibit a voltage dependency. As the impedance curves in Figure 33ab indicate, the modeled capacitance decreases from 180 μF to 32 μF when 100 V is applied. This voltage-dependency can be modeled by defining the capacitor via its charge Q as Equation 4.2 shows. This first-order approximation is considered as sufficient although a non-linear voltage behavior can be seen in Figure 33cd. Additionally, this model limits itself to 100 V.

$$Q = C \cdot U = 180\,\mu F \cdot U - 1.48\,\mu F \cdot U^2. \qquad 4.2$$

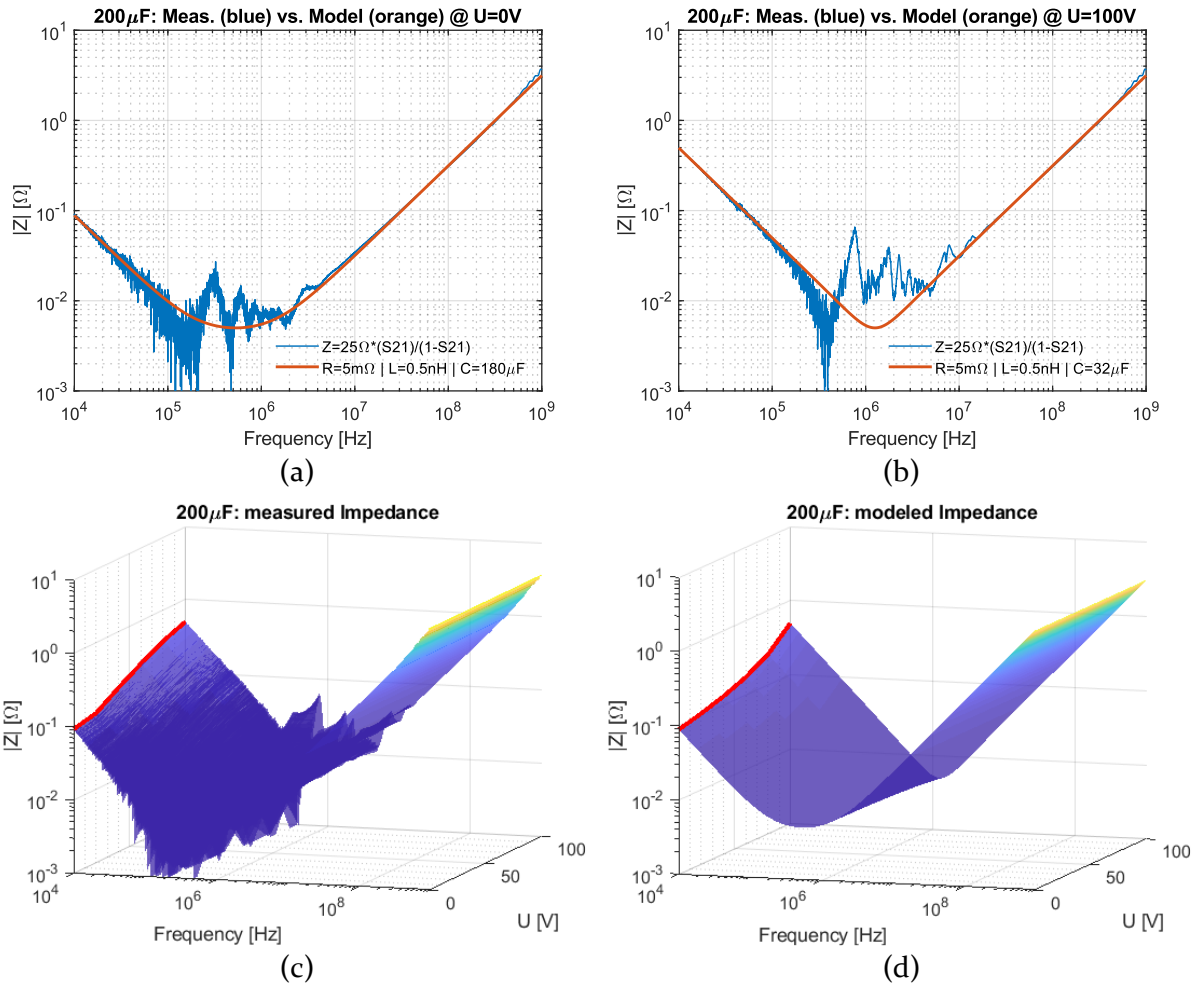


Figure 33: 2-port characterization of the decouple capacitor. (a) When no voltage is applied. (b) With 100 V applied. (c) Measured impedance; the voltage dependency at 10 kHz is of interest. (d) Modeled impedance

4.2 Gate-charge simulations

The simulation test bench shown in Figure 15 is used to generate the gate-charge plot for the created MOSFET models. The simulation results compared with the datasheet are shown in Figure 34.

Analyzing the gate-charge plot for the SJ FET, all models show very similar results. Both the model from the manufacturer and the self-made model based on measurements show very good agreement with the datasheet. The slope of the self-generated (green) model could be improved by finetuning its C_{rss} (Figure 29a). In general, the x-axes show that the switch-on process of the SiC FET is faster than that of the SJ FET since fewer charge carriers are required to exit the Miller plateau. Analyzing the plot for the SiC FET in detail, none of the models can depict the slope of the plateau phase well, but the self-made models show a significant better result compared to the manufacturer's model. In addition, the simulation with the manufacturer's model creates 110,068 time steps. In comparison, the model created with the datasheet or by performing measurements creates 132 or 208 time steps, respectively. Even though this is an extreme case, it can be demonstrated that shorter simulation times are achieved with the self-generated models.

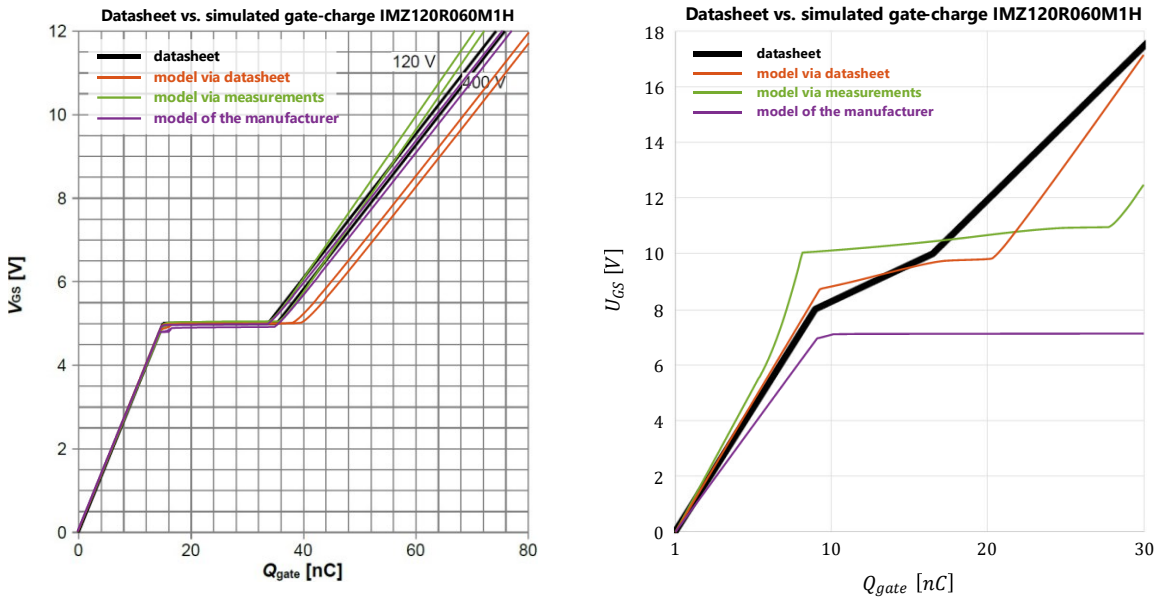


Figure 34: Simulated gate-charge plot compared with the datasheet. Green: model via measurements. Orange: model via datasheet. Purple: model from the manufacturer. (a) SJ [33]. (b) SiC [34]

4.3 Transient simulations

The transient simulations are the most important ones to verify since these enable future EMC considerations via simulation. Multiple measurements were performed with the test circuit presented in Section 2.1 with changings in various parameters. All plots in this section show the potentials referred to ground potential; additional measurement results can be found in the Appendix 7.1. The following color code is applied:

- Blue traces show the measurement results.
- Green traces show the simulation results of the model created via measurements.
- Orange traces show the simulation results of the model created via the datasheet.
- Purple traces show the simulation results of the model provided from the manufacturer.

The same gate driver was used for all measurements which can drive 4 A (source, rise time: 6.5 ns) and 8 A (sink, fall time: 4.5 ns) according to its datasheet [40]. In the simulation test bench depicted in Figure 16, 6 ns and 4 ns were chosen respectively. The test setup for the SiC FET is shown in Figure 35.

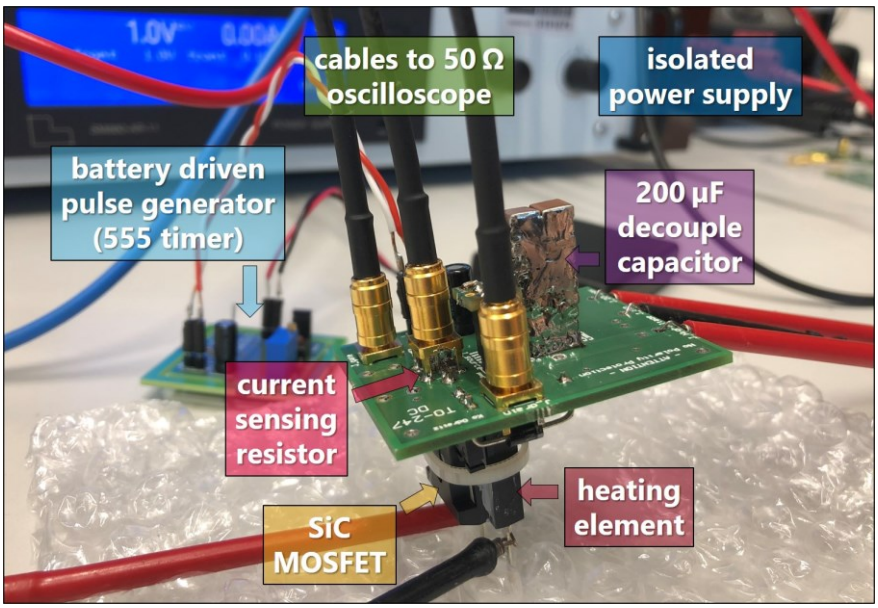


Figure 35: Photo of the universal test setup to capture the switching behavior of the SiC MOSFET

4.3.1 Superjunction MOSFET

Analyzing Figure 37 and Figure 38, very good agreement is achieved between the self-generated model via measurements and the manufacturer's model. The main difference between the model created via measurements and the model created via the datasheet is that the latter does not model the parasitic effect of the bonding wires since this information is usually not provided by a datasheet. However, it is exactly this consideration that makes the significant advantage of the model via measurements over the model via datasheet. Thus, it can be concluded that the information of the datasheet can be taken for a quick modeling, and the parasitic inductances of the bonding wires can be estimated with a few nH. For more accurate results, a hybrid approach might be considerable; the static behavior could be modeled with the help of the datasheet whereas the dynamic behavior is determined via the measurement method presented in Section 2.3. The switching processes can be categorized into several time segments [12], [22]. The following statements can be noted when analyzing Figure 37 and Figure 38 in more detail:

For the turn-on phase (times are related to the blue line):

In the initial condition, the drain pin of the MOSFET carries $\approx 100\,V$ whereas both gate and source potential are shorted to ground. The pulse generator produces a $1\,\mu s$ long pulse at $t = 0\,ns$.

Within the period $t = 0\,ns$ to $12\,ns$, the MOSFET is in its OFF state. The datasheet gives $3.5\,V$ as a typical value for the threshold voltage; the self-generated models even work with a threshold voltage of $4\,V$. However, observing the source pin in this time period, a significant current flow is noticed. The stray capacitances C_{GS} and C_{GD} are responsible for this since charge carriers must flow in the same moment when the gate voltage rises. Taking the dominant C_{GS} as an example, electrons drive from ground to this capacitance which results in a positive flow of current with its peak at $t = 3\,ns$. The much smaller C_{GD} on the other hand has very little impact on this time period.

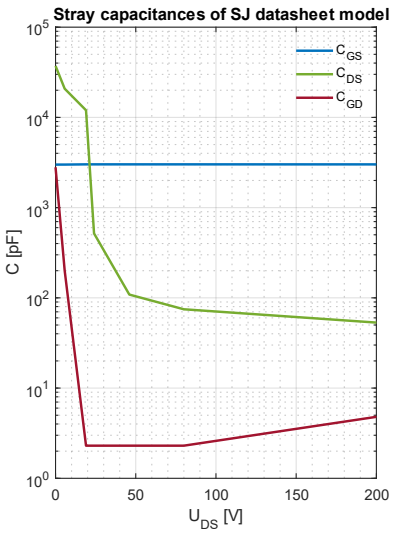


Figure 36: Modeled capacitances of the SJ datasheet model

Within the period $t = 12\,ns$ to $16\,ns$, the MOSFET is in its saturation mode. After the threshold voltage has been reached, a drain-source current starts to flow which causes U_{DS} to decrease due to the voltage drop across the load.

At $t = 16\,ns$, the drain-source voltage has already dropped below $20\,V$. From this point, the capacitance C_{GD} starts to increase rapidly as Figure 36 shows. This determines U_{GS} to stay nearly constant since most of the drive current flows into C_{GD}. This Miller plateau phase ends at $t = 50\,ns$. During this time period, the MOSFET moves from its saturation region to its linear region. A negative overshoot can be noticed, but none of the models is able to predict it which is very unwelcome in terms of future EMC considerations. At the same moment, the current overshoots but all models flatten this with the help of the capacitances. It is unclear whether the measured overshoot of the drain voltage actually occurs which is discussed further in Subsection 4.3.3.

For the turn-off phase (times are related to the blue line):

Discharging the gate follows the principles of charging the gate, but the order is the other way around. In case of Figure 37, the gate voltage is equal to $8\,V$, the drain voltage is a bit above $0\,V$, and a current of about $4.5\,A$ is flowing during the initial condition. It can be noticed that the measured current starts with a bit less than the simulated ones. It is assumed that the current sensing resistor slightly differs from $16.67\,\Omega$. In addition, the power MOSFET itself has heated up which slightly decreases the flow of current further.

Starting with $t = 1000\,ns$, the driver discharges C_{GS} and C_{GD} which are similar in capacity resulting U_{GS} and I_{DS} to decrease. Few moments later, U_{GS} decreased to a level that I_{DS} is causing too less voltage drop over the load which allows U_{DS} to increase. The very large C_{DS} starts now to charge and causes the gate potential to increase for a short moment. Another Miller plateau phase is now initiated which allows the current to drift further. However, this time the length of the plateau is mainly influenced by the load since charge carriers must flow through that load to charge C_{DS}. Figure 38 shows for example a very long time to turn off the MOSFET entirely when a $1000\,\Omega$ load is attached.

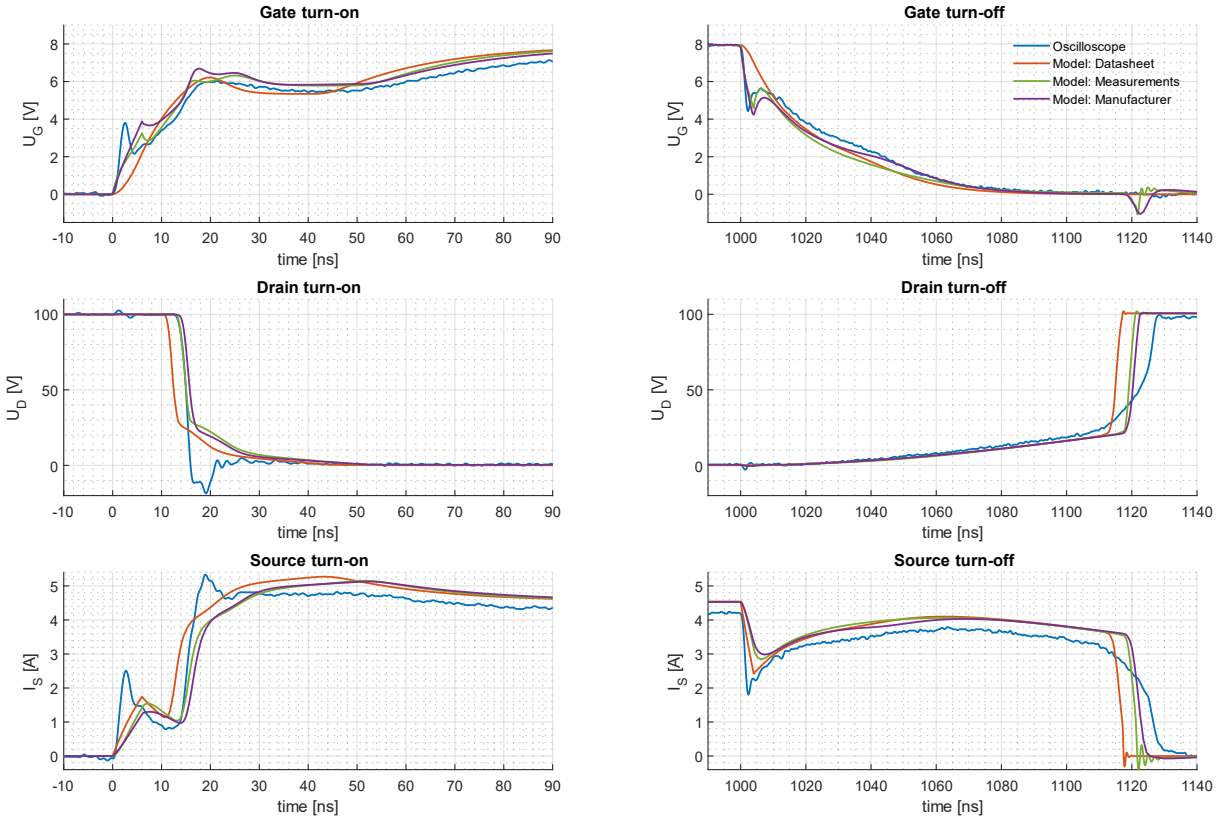


Figure 37: SJ FET transient simulations; U_{main} = 100 V, U_{gate} = 8 V, R_{gate} = 3.3 Ω, R_{load} = 22 Ω

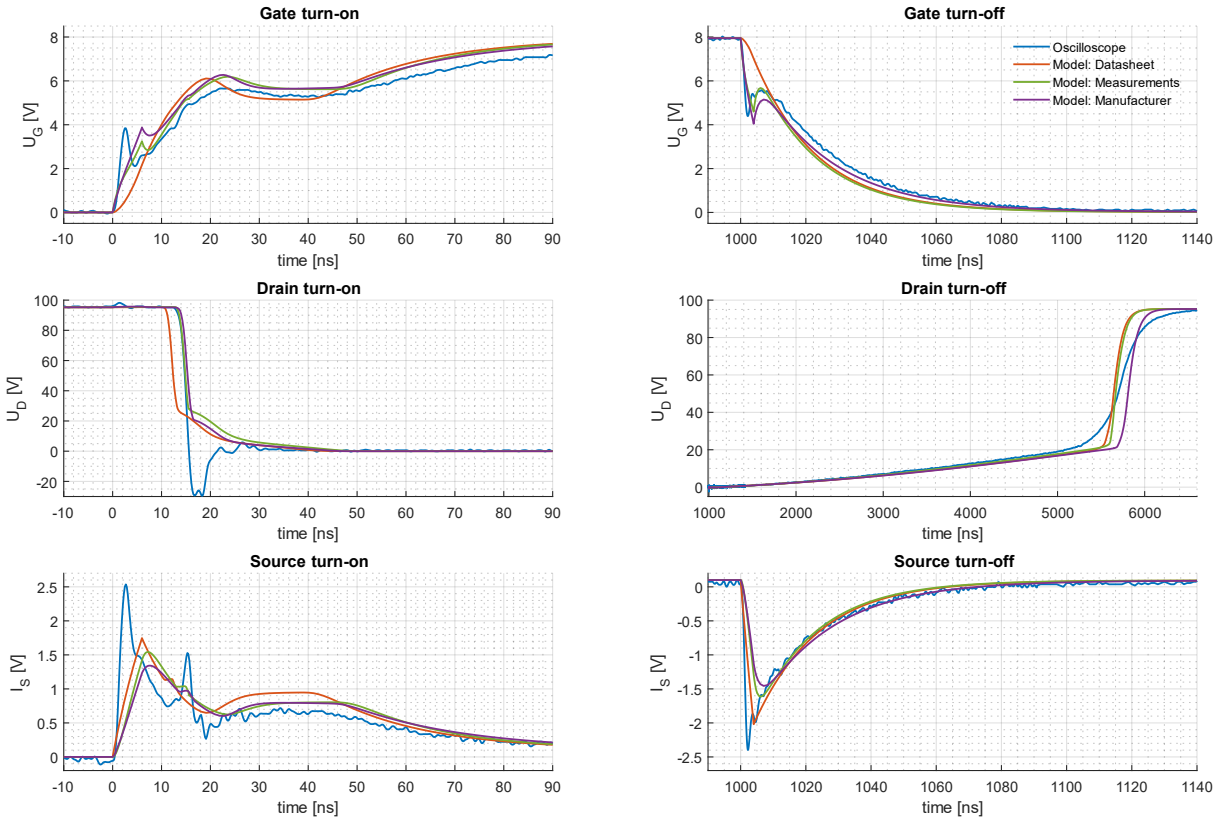


Figure 38: SJ FET transient simulations; U_{main} = 100 V, U_{gate} = 8 V, R_{gate} = 3.3 Ω, R_{load} = 1000 Ω

4.3.2 Silicon carbide MOSFET

The proposed modeling procedure especially convinces when the manufacturer is not providing a customized model. The self-generated SiC models show a better agreement to the measurements compared to the manufacturer's model in Figure 40 and Figure 41. However, fast transients, including overshoots, are not depicted by any model which may limit their use especially for EMC considerations. Further considerations about possible measurement errors are expressed in Subsection 4.3.3.

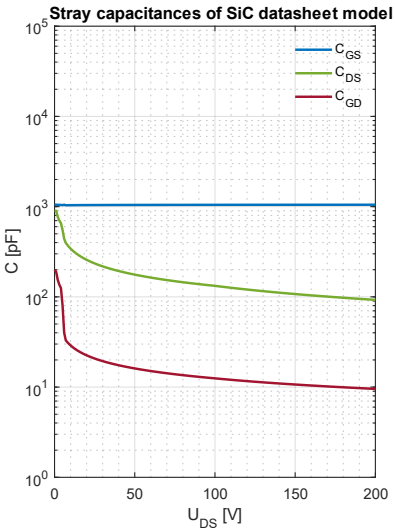


Figure 39: Modeled capacitances of the SiC datasheet model

Although superjunction transistors are known to have low stray capacitances because of its small size, this SiC MOSFET also has low capacitances as it can be seen in Figure 39. This leads to faster switching times, as it can be seen from the scaling of the x-axes in Figure 40 and Figure 41. Since the parasitic capacitances of the SiC transistor show quite simple curves, they could also be modeled with the help of a function e. g. as referenced in some existing approaches in Subsection 1.3.4 [27], [28], [32].

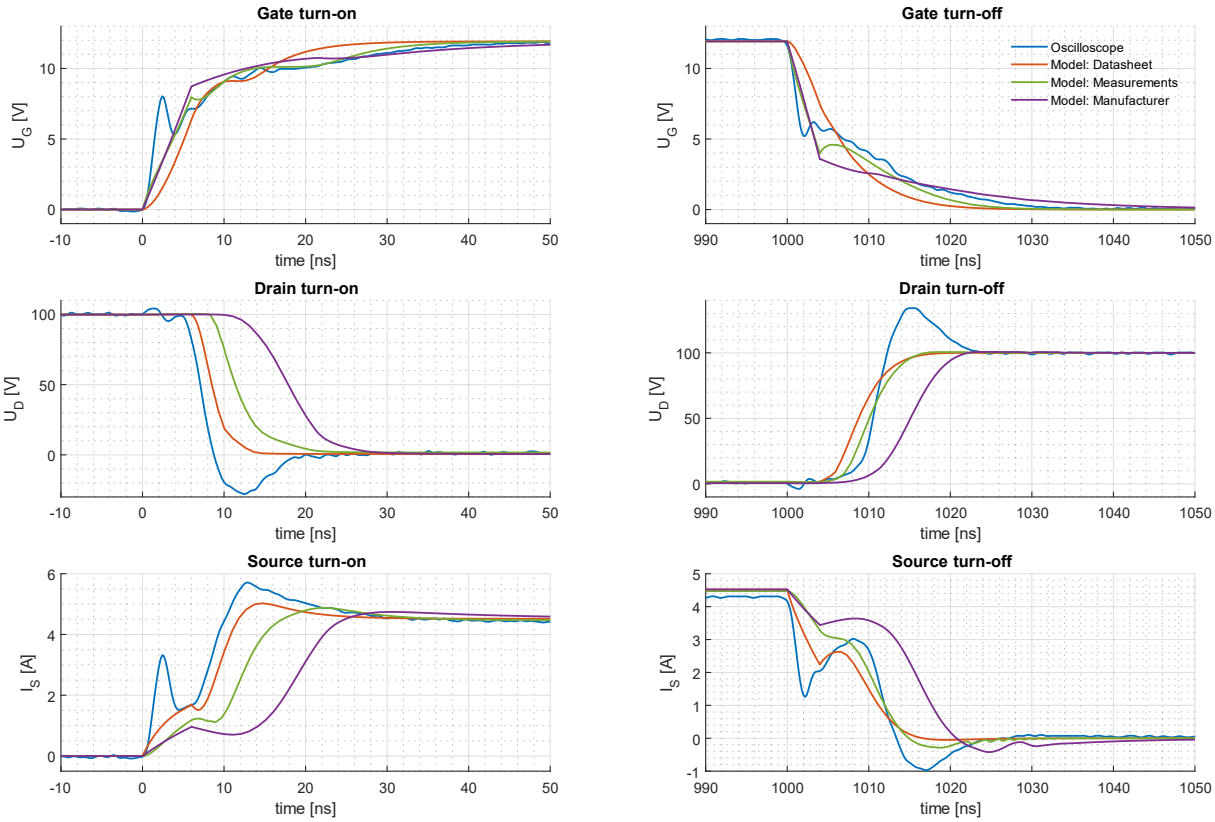


Figure 40: SiC FET transient simulations; U_{main} = 100 V, U_{gate} = 12 V, R_{gate} = 3.3 Ω, R_{load} = 22 Ω

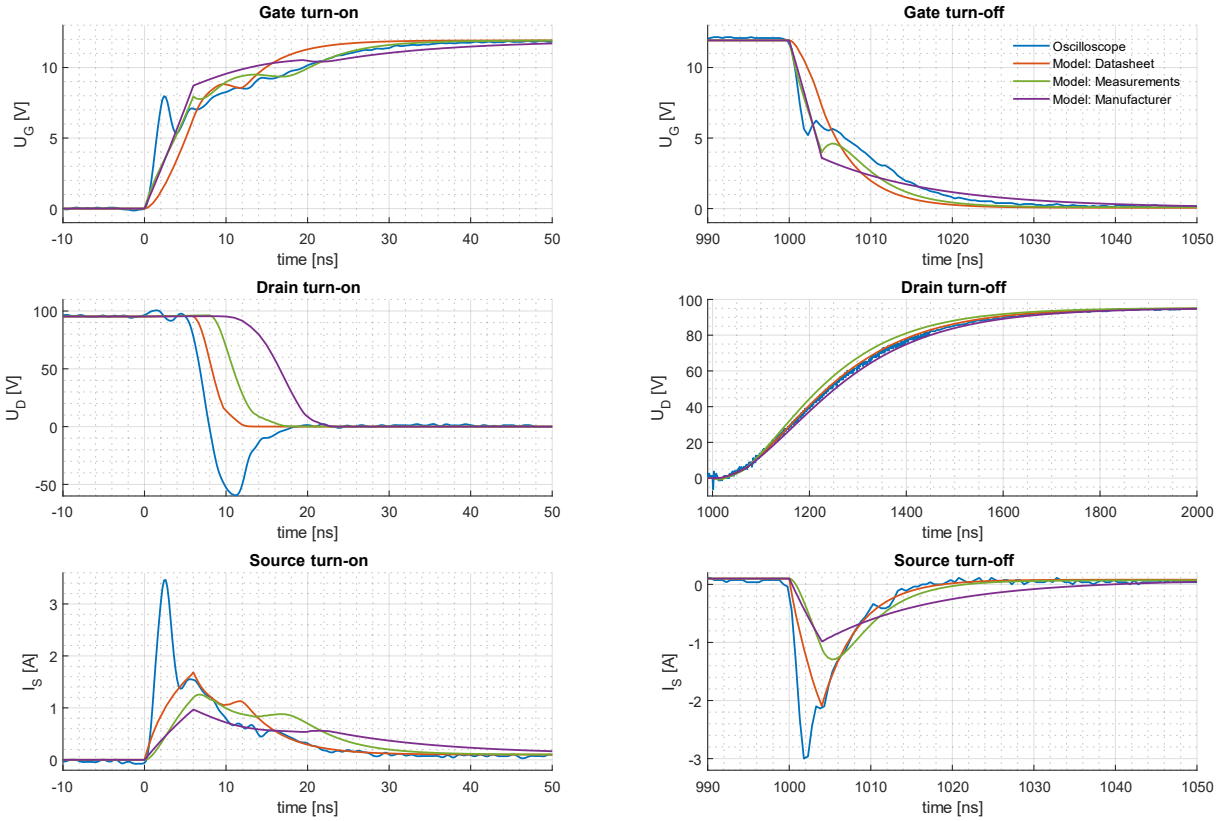


Figure 41: SiC FET transient simulations; U_{main} = 100 V, U_{gate} = 12 V, R_{gate} = 3.3 Ω, R_{load} = 1000 Ω

4.3.3 Possible error in the measuring system

All transient measurements, including those in the Appendix 7.1, exhibit a rather strange switching behavior. Figure 41 is used in the following attempt to describe that problem.

Most noticeable is the negative overshoot of the drain voltage at $t = 11\,ns$. It is assumed that this overshoot does not physically occur in this form since this would also change the direction of the current. On the contrary, if Figure 38 is examined as an example, a positive overshoot of the current can be noticed at that point in time. In addition, the shape of the curve does not match that of a classic overshoot where ringing with a specific frequency follows. An overshoot could also be caused by an impedance mismatch; depending on the reflection factor, overshoot or undershoot occurs. Since measuring cable and oscilloscope are matched with 50 Ω, such high overshoots are rather unusual. Nevertheless, the use of simple BNC-to-SMB cables (095-850-236M100, Amphenol Corp., Connecticut, US) should be pointed out here.

A more realistic explanation would be that this negative overshoot is caused by a coupling effect within the measuring loop. Since very high currents are switched within very short times, equivalent to a high di/dt, this switching behavior could couple into the measurement loop. This large measurement loop starts at the drain pin of the DUT, then continues through the SMB connector into the inner conductor of the measurement cable to the oscilloscope. Starting from the oscilloscope, the measurement loop is continued via the outer conductor of the measuring cable back to the same SMB connector. From there, the loop continues to the current sense resistor and ends at the source pin of the DUT. When examining Figure 8, it is noticeable that this measurement loop passes right next to the DUT, which enhances any coupling.

It is essential that future work resolve this overshoot; otherwise a satisfactory agreement between measurement and simulation model will not be possible. Experiments already showed that short-circuiting the current sensing resistor did not significantly improve the measurement. Therefore, a redesign of the universal test board would be a reasonable starting point. Ultimately, a mediocre agreement between measurement and model was achieved in this thesis.

4.3.4 Influence of the gate-source voltage on the Miller plateau

As described in Section 2.3, the voltage-dependent capacitances are modeled as a function of the drain-gate voltage $U_{GD} = U_{DS} - U_{GS}$. The reason for this decision is that the Miller plateau is not properly modeled if the stray capacitances depend on U_{DS} only. If the gate-source voltage is not taken into account, the plateau phase lasts much shorter as it is shown in Figure 42 and Figure 43. The additional consideration of the gate-source voltage results in a shift of the capacitance curves, i. e. the larger U_{GS} is, the larger the capacity C_{GD} and C_{DS} could be. In this test setup, the first capacitance mainly influences the switch-on process while the second capacitance is decisive for the switch-off process. The change in C_{GS} is negligible since its capacitance curve is relatively constant.

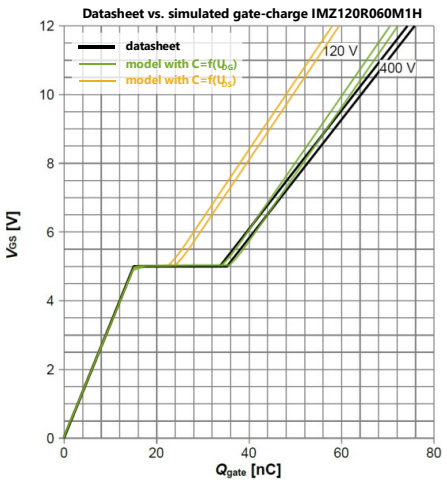


Figure 42: Simulated SJ gate-charge plot with different stray capacitances compared. Black: datasheet [33]. Green: depending on U_{DG}. Yellow: depending on U_{DS}

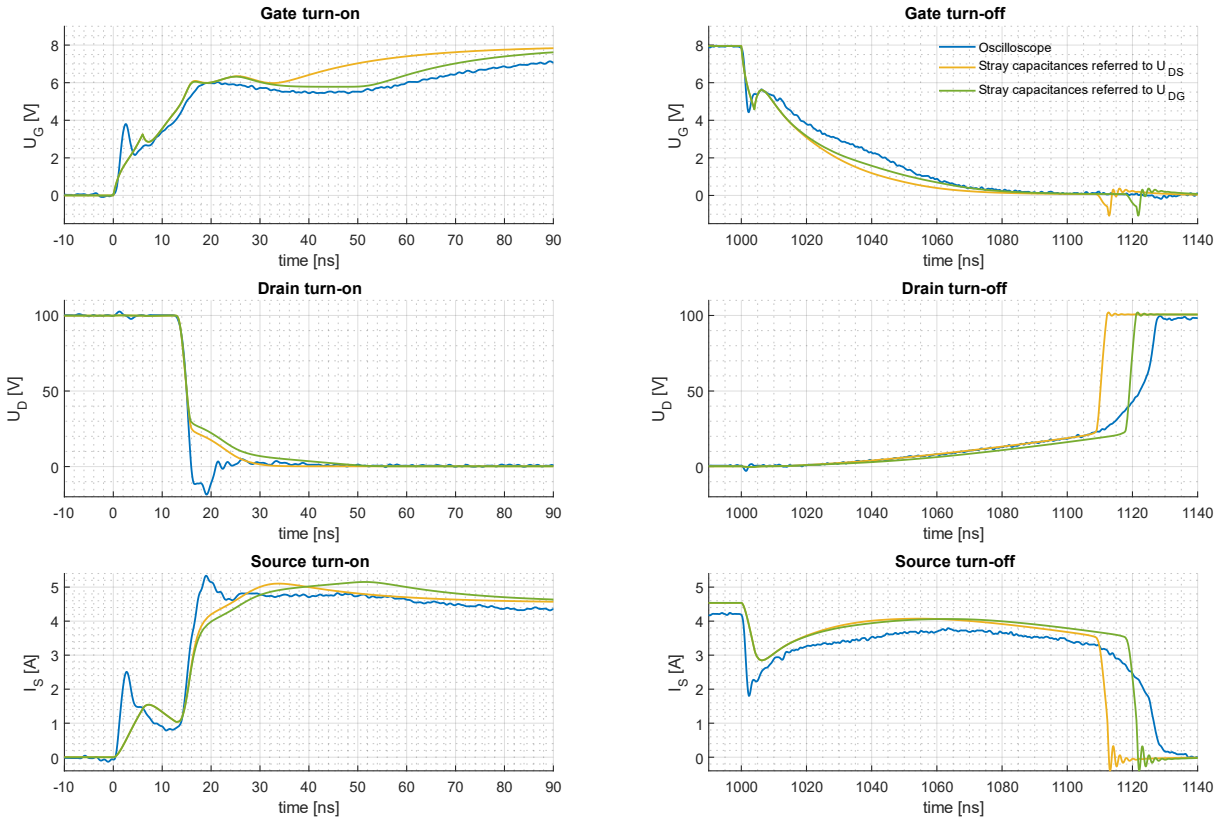


Figure 43: SJ FET transient simulations of the model created via measurements similar to Figure 37. The yellow curve models the stray capacitances depending on U_{DS} instead of U_{DG}

As already mentioned in Section 2.3, it is uncommon to set C_{GS} and C_{DS} as a function of U_{DG}. While it barely matters with the former because of the relatively constant capacitance curve, a dependence on U_{DS} seems more comprehensible with the latter. Ultimately, a consistent dependence on U_{DG} was decided in this thesis since this dependence showed a better agreement. Furthermore, this approach is a bit simpler to implement in LTspice compared to an individual solution.

Future studies need to be performed to determine the exact influence of the gate-source voltage to the stray capacitances since its impact was assumed to be linear in this thesis. This could be accomplished, for instance, by adapting the measurement circuit depicted in Figure 13. The middle 1 $M\Omega$ resistor of the gate-source RF filter could be replaced by an additional voltage source so that there is still an RF filter effect at both terminals. In this way, the gate-source potential can be influenced. Thus, the MOSFET can be turned on and off while the other two filters ensure that only a very small current can flow. As a result, the parasitic dynamic elements could be determined both as a function of U_{DS} and as a function of U_{GS}.

5
Discussion

In the first part of this master thesis, a new universal modeling method for power MOSFETs was presented. The formulas have been comprehensively described to allow the reader to create their own model in SPICE. For a quick modeling, only a datasheet is necessary. However, if no datasheet is available, or if it is to be verified, simple measurement methods have been thoroughly explained. In the second part of this work, the proposed method was applied in order to generate models for a superjunction and a silicon carbide MOSFET. Schematics of all LTspice subcircuits were fully shown to allow a quick modeling of a custom MOSFET. In addition, the measurement results of the test circuits were presented, which showed good agreement with the datasheet. Verification measurements were presented in the last part of this work. These showed satisfactory results as well; only a few differences were visible between the manufacturer's superjunction model and the self-generated model. The proposed model was particularly convincing for the silicon carbide MOSFET. This advantage is mainly based on the fact that the manufacturer does not provide an individual model for this MOSFET. Thus, it can be concluded that creating your own model is especially beneficial if the manufacturer does not offer one, or only for a similar component.

Furthermore, it can be assessed that not all the presented measurement techniques have to be carried out. If only an approximate model is needed, the parasitic bonding wires can be estimated with a few *nH* to already obtain very good results while the rest of the model is created with the help of the datasheet. For future EMC considerations however, the proposed model does not provide satisfying results yet. The very fast switching speeds and the overshoots are either represented only poorly or not at all by all models examined. Future work must be concerned with a more exact measurement setup as well as a more accurate modeling as these effects are most often responsible for EMC problems. Besides that, the proposed model does not yet represent all relevant effects like the dynamic temperature behavior. If more complex circuits are simulated, e. g. a half bridge inverter, the reverse recovery time must be modeled accurately.

However, the proposed model already shows a very good agreement compared with models from manufacturers while keeping complete control over the model. Further, the proposed model did not exhibit any convergence problems during this work, and due to the knowledge of the model's internal structure, convergence can be reasonably analyzed should problems appear in the future. Moreover, the presented models show significantly shorter simulation times; if the proposed model is turned on and off 500 times in an LTspice simulation, as it is performed in Figure 44, it will take a personal computer (AMD Ryzen™ 7 2700X 8x 3.70 GHz processor with 16 GB RAM on a Windows 10 operating system) approximately 22 seconds to simulate. In contrast, the same simulation with the manufacturer's SJ and SiC model takes 48 seconds and 82 seconds, respectively. Especially for very time-consuming EMC simulations, this time saving is favorable.

5.1 Outlook and challenges

Creating accurate models is crucial since this would enable predictive EMC considerations via simulations. This would not only increase the efficiency of electronic products but would also bring economic benefits if EMC test measurements are passed at the first attempt. The simulation test bench shown in Figure 16 could be adapted to enable fast Fourier transform (FFT) analyses. By switching the MOSFET numerous times and increasing the observed time window, FFT analysis can alert designers to potential design flaws before prototyping.

Instead of a straightforward FFT analysis in SPICE, the simulated time domain signal can also be fed to an EMI receiver simulation model. As it is described by Karaca et al. [43], a simulated EMI receiver computes the frequency spectrum based on the operation of a physical EMI receiver. In this way, the choice of the detector, for instance, can be taken into account, e. g. a quasi-peak detector which weights rare occurring signals weaker. Thus, an evaluation via an EMI receiver simulation model provides a result that can be compared with EMC measurements.

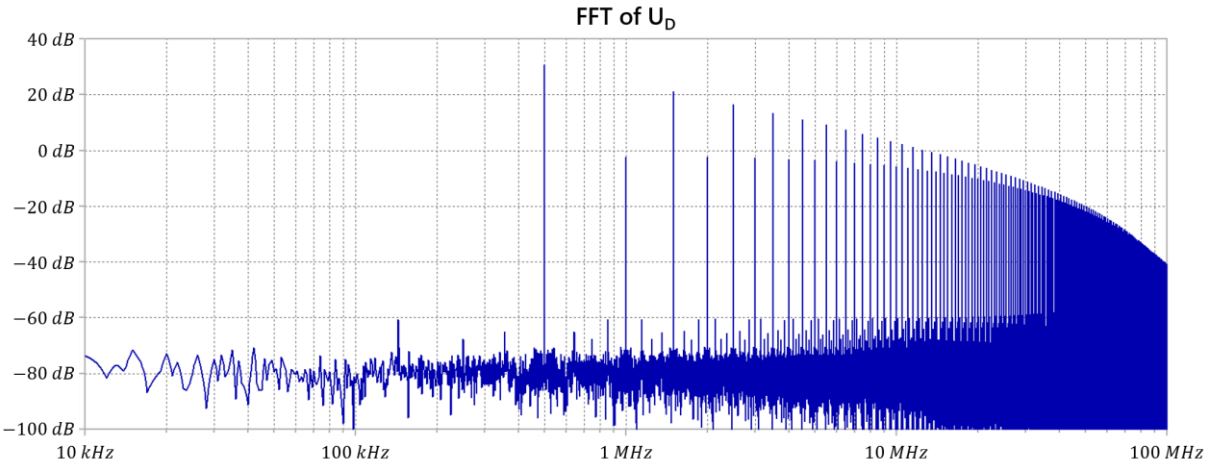


Figure 44: LTspice simulation of an exemplary FFT analysis of the universal test circuit with the self-created SiC model. The period of the gate signal is 2 µs, the duty cycle is 50% and the rise/fall time is 5 ns. The shown signal components are normalized to correspond to the time domain RMS amplitude

However, multiple challenges remain before EMC simulations become suitable for the everyday use of a product engineer. The presented modeling is just the tip of the iceberg; all electric components of a system must be characterized like gate driver and power supply. This is necessary not only to verify the simulation model with EMC measurements performed in a lab. Coupling effects between all components must be considered as well. This becomes even worse considering that in a real application the cable lengths between the components are greater. A cable harness of a vehicle, for instance, provokes multiple coupling effects which must be considered in future simulations.

5.2 Conclusion

In this thesis, a universal power MOSFET model for SPICE was proposed. The drain-source current is calculated analytically using the minimum between the Shichman-Hodges model and a root function. With the help of a square function, the current through the body diode is determined analytically, and a biased diode forms the breakdown voltage. The static temperature behavior is considered by linear scaling factors. In addition, the use of lookup tables enables to model the parasitic, nonlinear, voltage-dependent capacitances.

The proposed model is applied to generate models for a superjunction and a silicon carbide power MOSFET in LTspice. First, models were created using only characteristic values from the datasheet. Then, measurement methods were presented to determine those values necessary to generate a model if no datasheet is available. These measurements also provide information about the parasitic inductances and resistances of the bonding wires, which, however, could be estimated if the datasheet-only modeling procedure is chosen. For verification, all self-generated models were compared with those of the manufacturer; first, by comparing the simulated gate-charge plots with those from the datasheet, and second, by comparing the simulated and measured transient switching behavior. The load, the decouple capacitor and the current sensing resistor were characterized to determine their parasitic elements. Compared with the manufacturer's models, very good results were achieved with the proposed models. In terms of future EMC considerations, mediocre agreement was achieved.

To sum up, the proposed model is remarkable by its particular simplicity. A power MOSFET model can be created very fast without doing a single measurement and with a simple estimation of a few nH parasitic inductances for the bonding wires. Simulation times can be kept very low while maintaining complete control over the model. No special simulation settings are required, and not a single convergence error occurred during the entire work of this master thesis.

6
Bibliography

[1] "Global EV Outlook 2021," International Energy Agency, April 2021. [Online]. Available: https://www.iea.org/reports/global-ev-outlook-2021. [Accessed 4 May 2021].

[2] "E-Mobilität: Marktrends in den Kernregionen Europa und China im 1. Quartal 2021," Dr. Bratzel Center of Automotive Management GmbH & Co. KG, 26 April 2021. [Online]. Available: https://auto-institut.de/automotiveinnovations/emobility/e-mobilitaet-marktrends-in-den-kernregionen-europa-und-china-im-1-quartal-2021/. [Accessed 4 May 2021].

[3] "CO2 emissions from cars: facts and figures (infographics)," European Parliament, 18 April 2019. [Online]. Available: https://www.europarl.europa.eu/news/en/headlines/society/20190313STO31218/co2-emissions-from-cars-facts-and-figures-infographics. [Accessed 4 May 2021].

[4] "Rückruf-Trends der globalen Automobilhersteller in 2019/ 2020 (im Referenzmarkt USA)," Dr. Bratzel Center of Automotive Management GmbH & Co. KG, 28 July 2020. [Online]. Available: https://auto-institut.de/automotiveperformance/rueckruf-trends-der-globalen-automobilhersteller-in-2019-2020-im-referenzmarkt-usa/. [Accessed 4 May 2021].

[5] M. Zhang, "Demystifying EMC in an Electric Vehicle's Drive Unit," Interference Technology, 16 July 2020. [Online]. Available: https://interferencetechnology.com/demystifying-emc-in-an-electric-vehicles-drive-unit/. [Accessed 4 May 2021].

[6] B. Deutschmann, "ElectroMagnetic Compatibility," 2006.

[7] "Power MOSFET Basics," Alpha and Omega Semiconductor, 11 November 2009. [Online]. Available: http://www.aosmd.com/res/application_notes/mosfets/Power_MOSFET_Basics.pdf. [Accessed 4 May 2021].

[8] B. Van Zeghbroeck, "Principles of Semiconductor Devices, Chapter 4," University of Colorado Boulder, 2011. [Online]. Available: https://ece-www.colorado.edu/~bart/book/. [Accessed 4 May 2021].

[9] B. J. Baliga, Fundamentals of Power Semiconductor Devices, 2. ed., Cham: Springer Nature, 2019, pp. 283-520, doi: 10.1007/978-3-319-93988-9.

[10] T. Fujihira, "Theory of Semiconductor Superjunction Devices," in *Japanese Journal of Applied Physics,* vol. 36, no. 10, pp. 6254-6262, October 1997, doi: 10.1143/JJAP.36.6254.

[11] F. Udrea, G. Deboy and T. Fujihira, "Superjunction Power Devices, History, Development, and Future Prospects," in *IEEE Transactions on Electron Devices,* vol. 64, no. 3, pp. 713-727, March 2017, doi: 10.1109/TED.2017.2658344.

[12] I. Castro, J. Roig, R. Gelagaev, B. Vlachakis, F. Bauwens, D. G. Lamar and J. Driesen, "Analytical Switching Loss Model for Superjunction MOSFET With Capacitive Nonlinearities and Displacement Currents for DC–DC Power Converters," in *IEEE Transactions on Power Electronics,* vol. 31, no. 3, pp. 2485-2495, March 2016, doi: 10.1109/TPEL.2015.2433017.

[13] S. Havanur and P. Zuk, "Power MOSFET Basics, Understanding Superjunction Technology," Vishay Intertechnology, Inc., 21 April 2015. [Online]. Available: https://www.vishay.com/docs/66864/an849.pdf. [Accessed 4 May 2021].

[14] M. Turzynski and W. J. Kulesza, "A Simplified Behavioral MOSFET Model Based on Parameters Extraction for Circuit Simulations," in *IEEE Transactions on Power Electronics,* vol. 31, no. 4, pp. 3096-3105, April 2016, doi: 10.1109/TPEL.2015.2445375.

[15] J. Victory, D. Son, T. Neyer, K. Lee, E. Zhou, J. Wang and M. B. Yazdi, "A Physically Based Scalable SPICE Model for High-Voltage Super-Junction MOSFETs," *PCIM Europe 2014; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, Nuremberg, Germany, 2014, pp. 1-8. [Online]. Available: https://ieeexplore.ieee.org/document/6841327. [Accessed 4 May 2021].

[16] L. W. Nagel and D. O. Pederson, "SPICE (Simulation Program with Integrated Circuit Emphasis)," Berkeley EECS Department, April 1973. [Online]. Available: https://www2.eecs.berkeley.edu/Pubs/TechRpts/1973/22871.html. [Accessed 4 May 2021].

[17] D. O. Pederson, "Spice," Donald O. Pederson Center for Electronic Systems Design, 17 July 2007. [Online]. Available: https://ptolemy.berkeley.edu/projects/embedded/pubs/downloads/spice/index.htm. [Accessed 4 May 2021].

[18] "LTspice," Analog Devices, Inc., 9 May 2021. [Online]. Available: https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html. [Accessed 17 May 2021].

[19] D. Laws, "Who Invented the Transistor?," Computer History Museum, 4 December 2013. [Online]. Available: https://computerhistory.org/blog/who-invented-the-transistor/?key=who-invented-the-transistor. [Accessed 4 May 2021].

[20] H. Shichman and D. A. Hodges, "Modeling and simulation of insulated-gate field-effect transistor switching circuits," in *IEEE Journal of Solid-State Circuits,* vol. 3, no. 3, pp. 285-289, September 1968, doi: 10.1109/JSSC.1968.1049902.

[21] "BSIM Group," University of California, Berkeley, [Online]. Available: https://bsim.berkeley.edu/. [Accessed 4 May 2021].

[22] R. McArthur, "Making Use of Gate Charge Information in MOSFET and IGBT Data Sheets," Advanced Power Technology, LLC, 31 October 2001. [Online]. Available: https://www.microsemi.com/document-portal/doc_view/14697-making-use-of-gate-charge-information-in-mosfet-and-igbt-data-sheets. [Accessed 4 May 2021].

[23] D. Cittanti, F. Iannuzzo, E. Hoene and K. Klein, "Role of parasitic capacitances in power MOSFET turn-on switching speed limits: A SiC case study," *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, Ohio, US, 2017, pp. 1387-1394, doi: 10.1109/ECCE.2017.8095952.

[24] P. Hillenbrand, M. Beltle, S. Tenbohlen and S. Mönch, "Sensitivity analysis of behavioral MOSFET models in transient EMC simulation," *2017 International Symposium on Electromagnetic Compatibility - EMC EUROPE*, Angers, France, 2017, pp. 1-6, doi: 10.1109/EMCEurope.2017.8094762.

[25] A. Endruschat, C. Novak, H. Gerstner, T. Heckel, C. Joffe and M. März, "A Universal SPICE Field-Effect Transistor Model Applied on SiC and GaN Transistors," in *IEEE Transactions on Power Electronics,* vol. 34, no. 9, pp. 9131-9145, September 2019, doi: 10.1109/TPEL.2018.2889513.

[26] W. R. Curtice, "A MESFET Model for Use in the Design of GaAs Integrated Circuits," in *IEEE Transactions on Microwave Theory and Techniques,* vol. 28, no. 5, pp. 448-456, May 1980, doi: 10.1109/TMTT.1980.1130099.

[27] Z. Duan, T. Fan, X. Wen and D. Zhang, "Improved SiC Power MOSFET Model Considering Nonlinear Junction Capacitances," in *IEEE Transactions on Power Electronics,* vol. 33, no. 3, pp. 2509-2517, March 2018, doi: 10.1109/TPEL.2017.2692274.

[28] A. Adrian, "A Power MOSFET SPICE Model with Built-In Model Generator," in *High Frequency Electronics,* pp. 28-38, August 2013. [Online]. Available: https://www.highfrequencyelectronics.com/Archives/Aug13/1308_HFE_spice.pdf. [Accessed 4 May 2021].

[29] A. Adrian, "Power Function Power MOSFET SPICE model," 8 August 2013. [Online]. Available: http://www.andreadrian.de/pfpm/. [Accessed 4 May 2021].

[30] M. Fuchs, L. Spielberger, K. Odreitz and B. Deutschmann, "Fast and Simple Model Generation for Superjunction Power MOSFETs," in *E&I,* no. 138, pp. 48-52, 18 December 2020, doi: 10.1007/s00502-020-00860-3.

[31] M. Fuchs, L. Spielberger, C. Sygulla and B. Deutschmann, "A New Method for Measuring Parasitics of Super Junction Power MOSFETs," *2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe)*, Genova, Italy, 2019, pp. P.1-P.9, doi: 10.23919/EPE.2019.8915539.

[32] H. Sennewald, "Util.zip," LTspice@groups.io, 24 November 2019. [Online]. Available: https://groups.io/g/LTspice/files/z_yahoo/1_LTspiceFiles/Util.zip. [Accessed 4 May 2021].

[33] "IPL65R070C7," Infineon Technologies AG, CoolMOS Datasheet, 29 August 2017. [Online]. Available: https://www.infineon.com/cms/en/product/power/mosfet/500v-900v-coolmos-n-

channel-power-mosfet/650v-and-700v-coolmos-n-channel-power-mosfet/ipl65r070c7/. [Accessed 4 May 2021].

[34] "IMZ120R060M1H," Infineon Technologies AG, CoolSiC Datasheet, 11 December 2020. [Online]. Available: https://www.infineon.com/cms/en/product/power/mosfet/silicon-carbide/discretes/imz120r060m1h/. [Accessed 4 May 2021].

[35] A. L. J. Joannou and D. C. Pentz, "Miniature integrated co-axial current shunt for high frequency switching power electronics," University of Johannesburg, 2013. [Online]. Available: https://core.ac.uk/download/pdf/54204708.pdf. [Accessed 4 May 2021].

[36] "Power MOSFET Electrical Characteristics," Toshiba Corp., 26 July 2018. [Online]. Available: https://toshiba.semicon-storage.com/info/docget.jsp?did=13415. [Accessed 4 May 2021].

[37] T. Liu, R. Ning, T. T. Y. Wong and Z. J. Shen, "A new characterization technique for extracting parasitic inductances of fast switching power MOSFETs using two-port vector network analyzer," *2017 29th International Symposium on Power Semiconductor Devices and IC's (ISPSD)*, Sapporo, Japan, 2017, pp. 403-406, doi: 10.23919/ISPSD.2017.7988967.

[38] S. M. Sandler, Power Integrity. Measuring, Optimizing, and Troubleshooting Power Related Parameters in Electronics Systems, New York City: McGraw-Hill Education, 2014, pp. 109-149.

[39] "Frequency Response of Thin Film Chip Resistors," Vishay Intertechnology, Inc., 4 February 2009. [Online]. Available: https://www.vishay.com/docs/60107/freqresp.pdf. [Accessed 4 May 2021].

[40] "1EDN7511B," Infineon Technologies AG, EiceDRIVER Datasheet, 20 April 2018. [Online]. Available: https://www.infineon.com/cms/en/product/power/gate-driver-ics/1edn7511b/. [Accessed 4 May 2021].

[41] F. Stueckler, G. Noebauer and K. Bueyuektas, "Introduction to Infineon's Simulation Models Power MOSFETs," Infineon Technologies Austria AG, 7 February 2014. [Online]. Available: https://www.infineon.com/dgdl/Infineon-ApplicationNote_PowerMOSFET_SimulationModels-AN-v01_00-EN.pdf?fileId=5546d46250cc1fdf0151588db5ef1b18. [Accessed 4 May 2021].

[42] H. Hartl, E. Krasser, W. Pribyl, P. Söser and G. Winkler, Elektronische Schaltungstechnik: Mit Beispielen in PSpice, 1. ed., Munich: Pearson Studium, 2008, pp. 609-699.

[43] T. Karaca, B. Deutschmann and G. Winkler, "EMI-receiver simulation model with quasi-peak detector," *2015 IEEE International Symposium on Electromagnetic Compatibility (EMC)*, Dresden, Germany, 2015, pp. 891-896, doi: 10.1109/ISEMC.2015.7256283.

7
APPENDIX

7.1 Transient simulations cont'd

Further selected plots from Section 4.3 are presented here with each parameter swept at least once. The measurement setup is identical to that in chapter 4. The following parameters are considered as default unless otherwise indicated:

- $T = 25°C$
- $U_{main} = 100\,V$
- $U_{gate} = 8\,V\ (SJ)\ or\ 12\,V\ (SiC)$
- $R_{gate} = 3.3\,\Omega$
- $R_{load} = 22\,\Omega$

7.1.1 Superjunction MOSFET

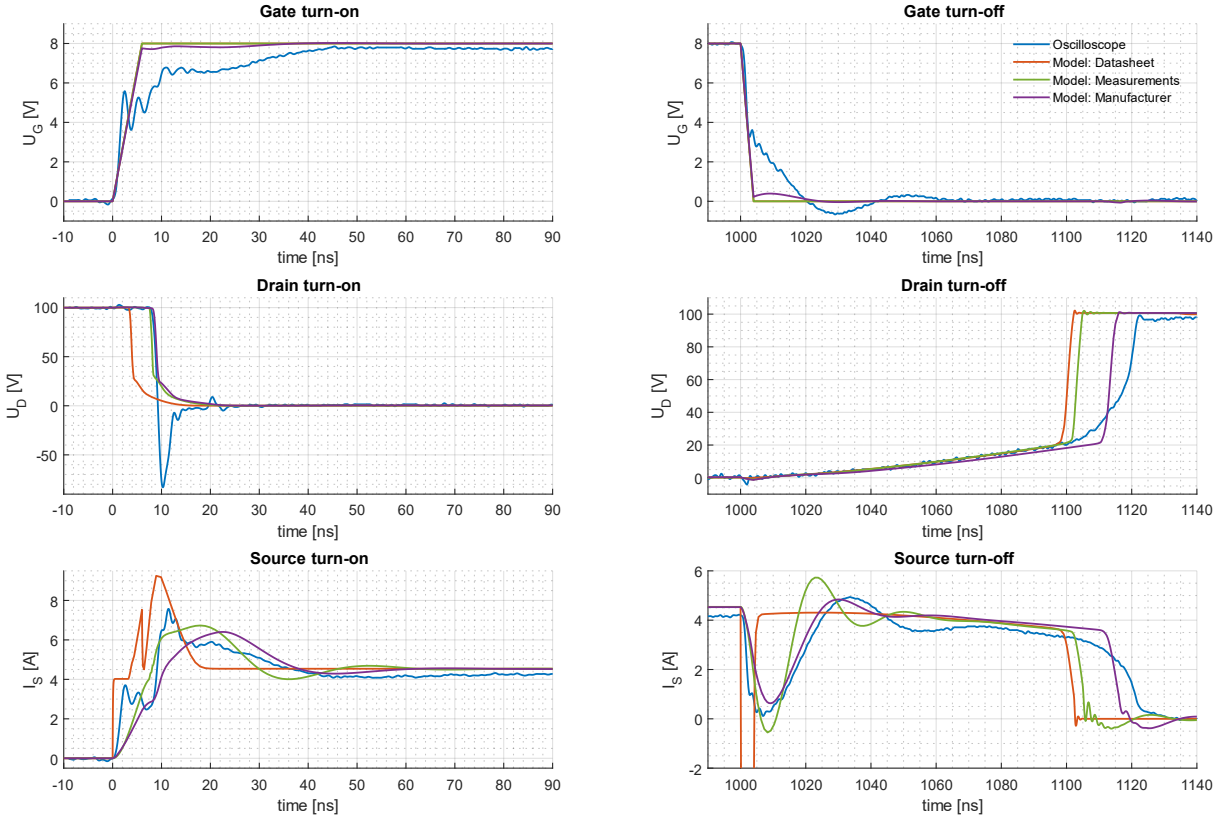


Figure 45: Transient simulations of the SJ FET with R_{gate} = 0 Ω

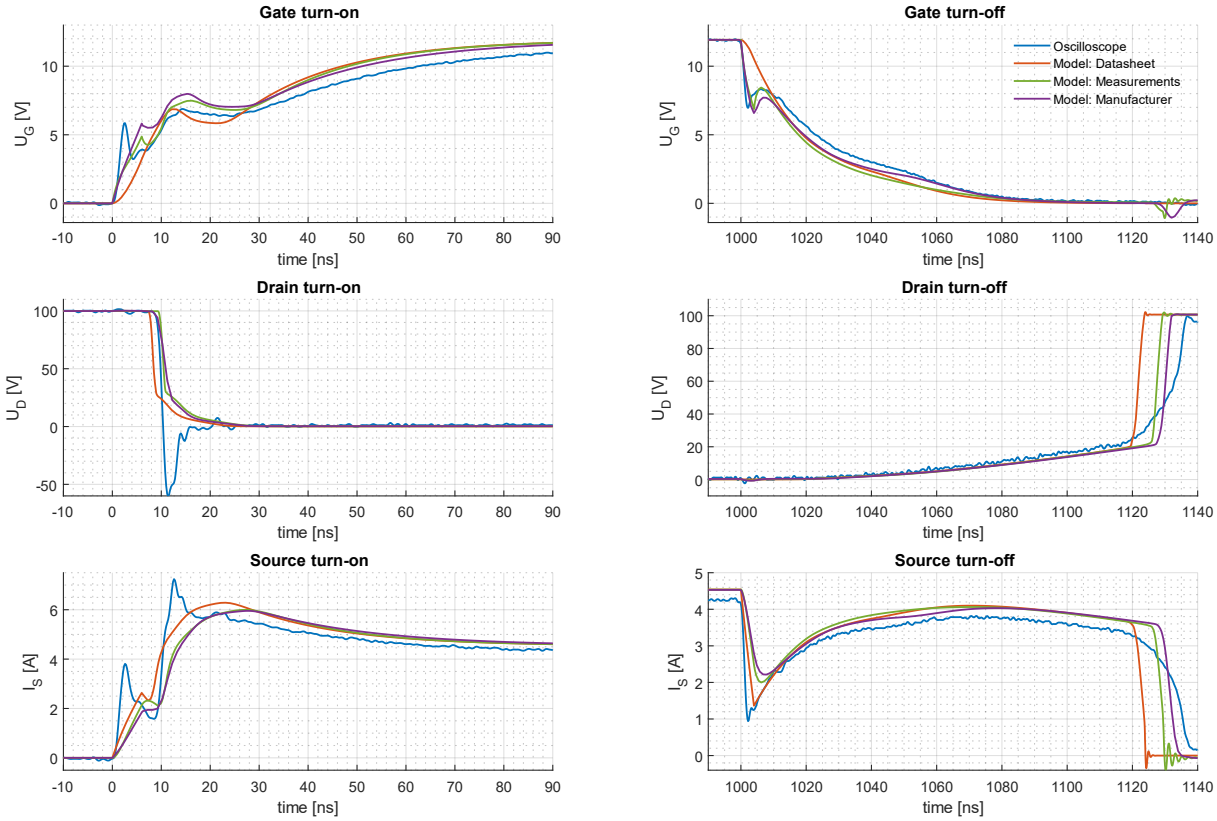


Figure 46: Transient simulations of the SJ FET with U_{gate} = 12 V

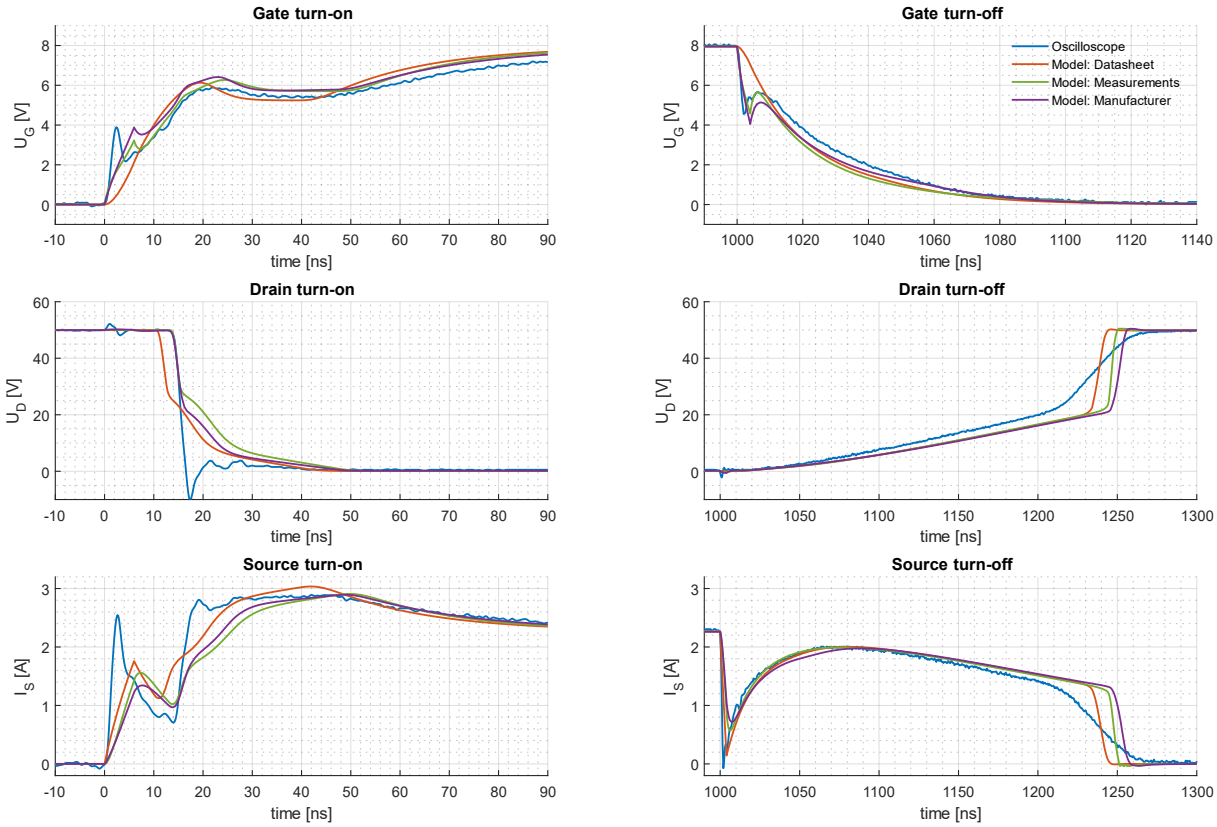


Figure 47: Transient simulations of the SJ FET with U_{main} = 50 V

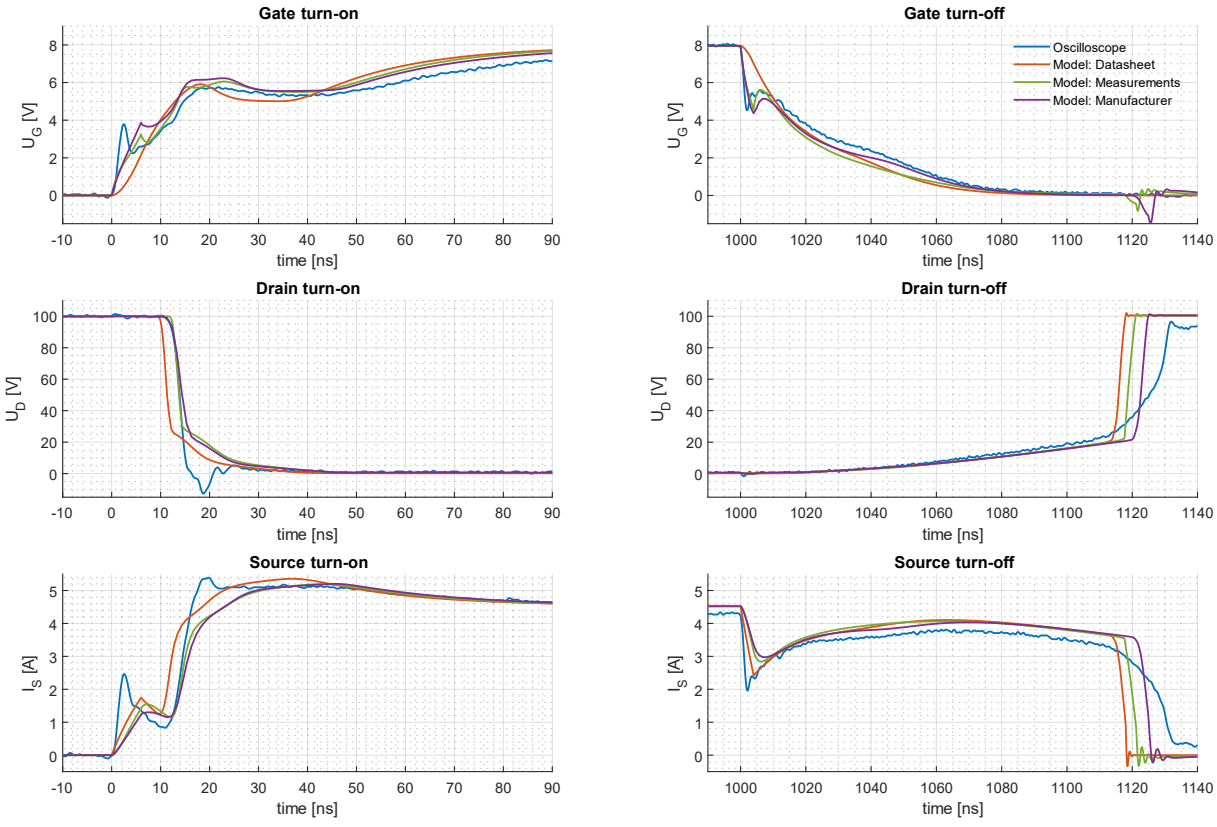


Figure 48: Transient simulations of the SJ FET with T = 125°C

7.1.2 Silicon carbide MOSFET

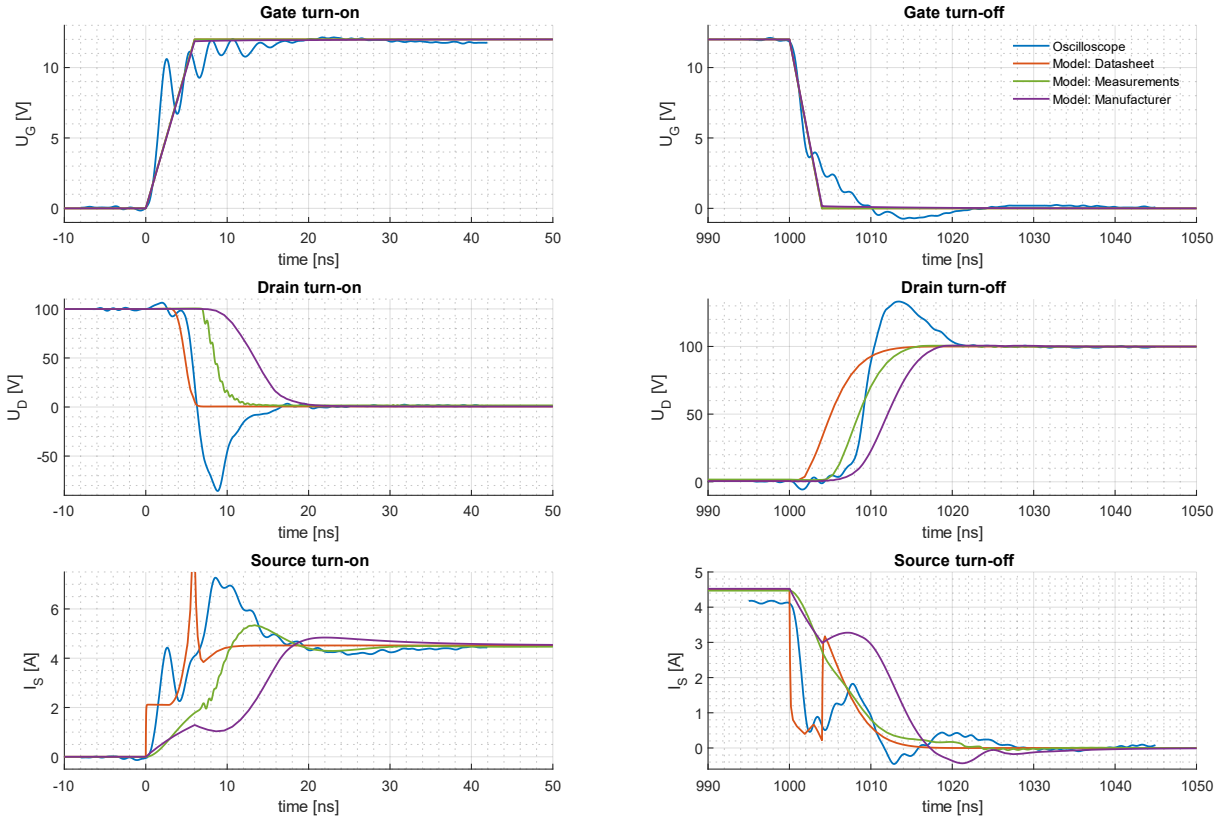


Figure 49: Transient simulations of the SiC FET with R_{gate} = 0 Ω

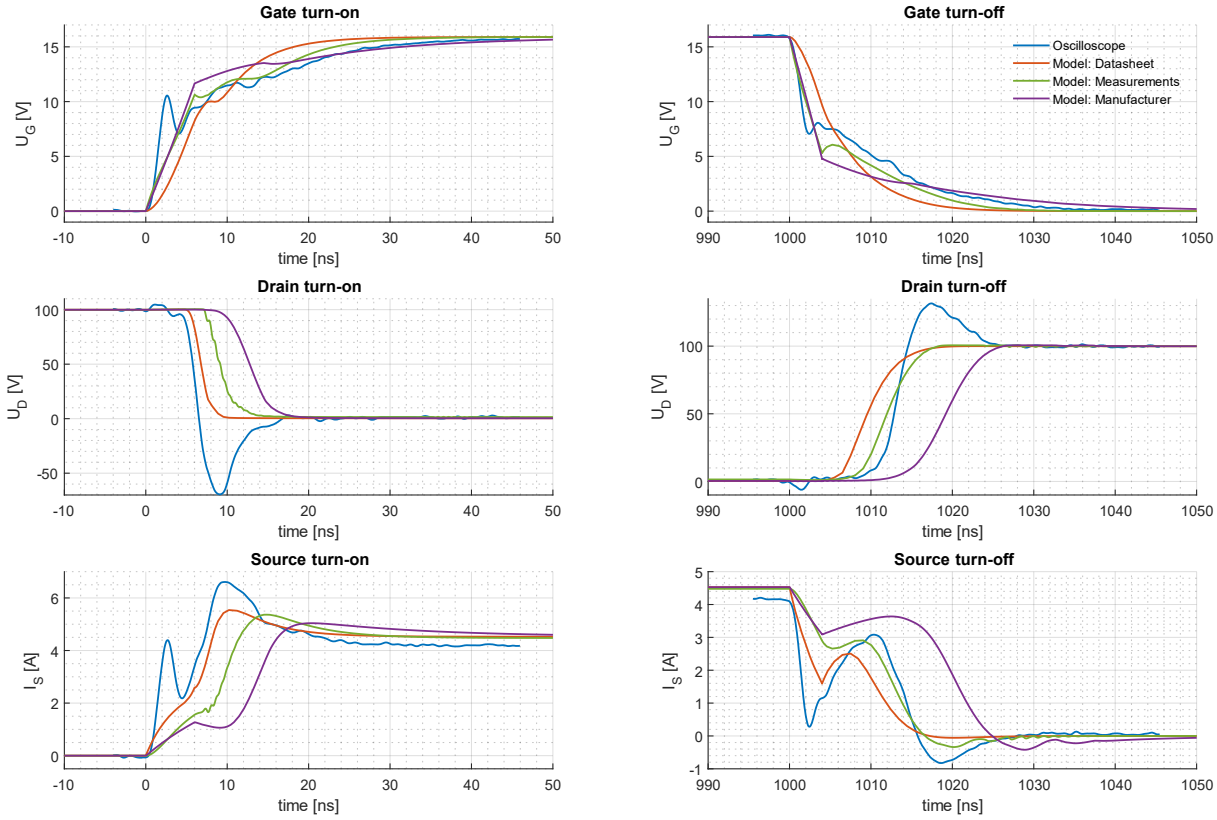


Figure 50: Transient simulations of the SiC FET with U_{gate} = 16 V

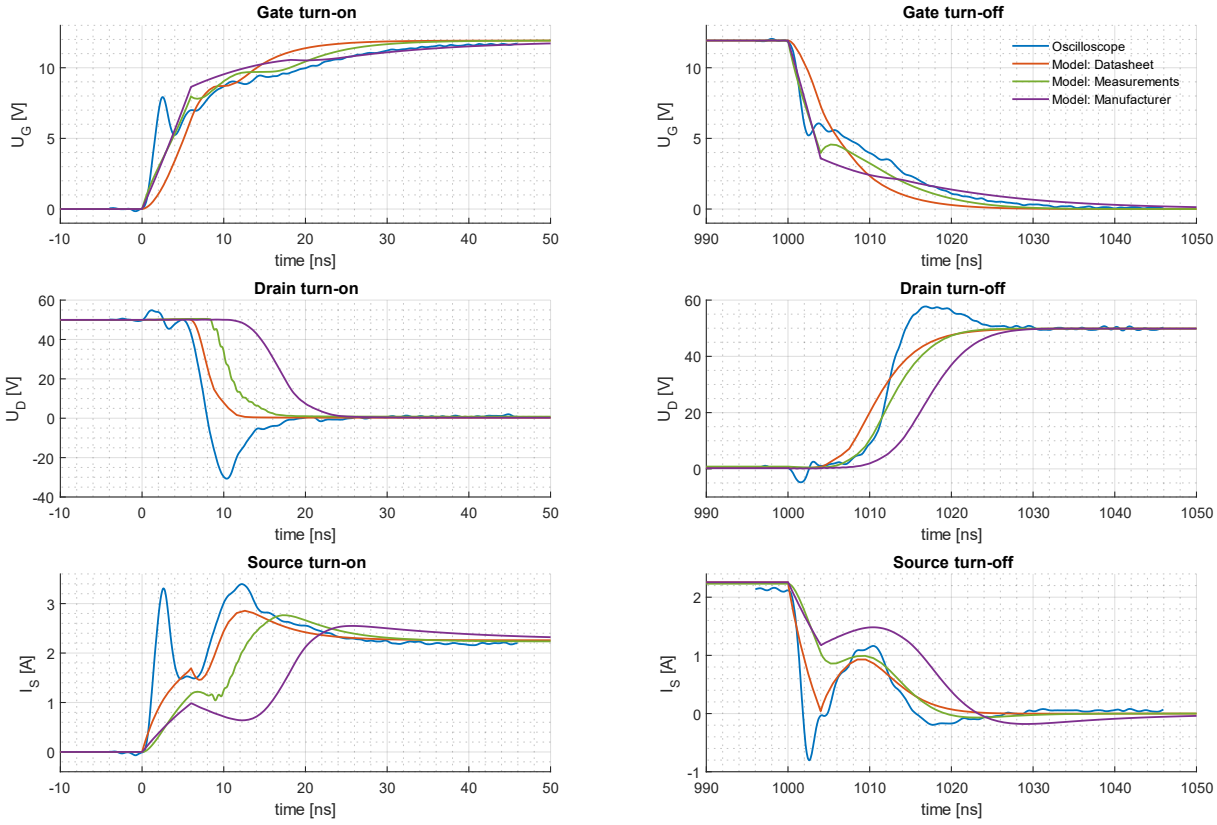


Figure 51: Transient simulations of the SiC FET with U_{main} = 50 V

7.2 Model parameters

All generated models and their parameters used in this thesis are summarized here.

7.2.1 Superjunction IPL65R070C7 datasheet model

Transfer and output characteristics:

```
Vgs1=6 Ids1=44 Vgs2=7.2 Ids2=120 Vds3=5 Ids3=75 Ids3warm=40 Vds4=19 Ids4=145 Ids4warm=89 Warm=125 VtoDelta=-0.4
```

Diode characteristics:

```
Vsd1=0.63 Isd1=0.1 Vsd2=0.8 Isd2=8 Breakdown=650 Warm=125 VtoDelta2=-0.19
```

Gate-drain capacitor:

```
table(0,2800.0e-12,1,1762.3e-12,2,1109.2e-12,3,698.1e-12,4,439.4e-12,5,276.6e-12,6,180.8e-12,7,129.3e-12,8,92.4e-12,9,66.0e-12,10,47.2e-12,11,33.7e-12,12,24.1e-12,13,17.2e-12,14,12.3e-12,15,8.8e-12,16,6.3e-12,17,4.5e-12,18,3.2e-12,19,2.3e-12,20,2.3e-12,21,2.3e-12,22,2.3e-12,23,2.3e-12,24,2.3e-12,25,2.3e-12,26,2.3e-12,27,2.3e-12,28,2.3e-12,29,2.3e-12,30,2.3e-12,31,2.3e-12,32,2.3e-12,33,2.3e-12,34,2.3e-12,35,2.3e-12,36,2.3e-12,37,2.3e-12,38,2.3e-12,39,2.3e-12,40,2.3e-12,41,2.3e-12,42,2.3e-12,43,2.3e-12,44,2.3e-12,45,2.3e-12,46,2.3e-12,47,2.3e-12,48,2.3e-12,49,2.3e-12,50,2.3e-12,51,2.3e-12,52,2.3e-12,53,2.3e-12,54,2.3e-12,55,2.3e-12,56,2.3e-12,57,2.3e-12,58,2.3e-12,59,2.3e-12,60,2.3e-12,61,2.3e-12,62,2.3e-12,63,2.3e-12,64,2.3e-12,65,2.3e-12,66,2.3e-12,67,2.3e-12,68,2.3e-12,69,2.3e-12,70,2.3e-12,71,2.3e-12,72,2.3e-12,73,2.3e-12,74,2.3e-12,75,2.3e-12,76,2.3e-12,77,2.3e-12,78,2.3e-12,79,2.3e-12,80,2.3e-12,81,2.3e-12,82,2.3e-12,83,2.3e-12,84,2.4e-12,85,2.4e-12,86,2.4e-12,87,2.4e-12,88,2.4e-12,89,2.4e-12,90,2.4e-12,91,2.5e-12,92,2.5e-12,93,2.5e-12,94,2.5e-12,95,2.5e-12,96,2.5e-12,97,2.6e-12,98,2.6e-12,99,2.6e-12,100,2.6e-12,101,2.6e-12,102,2.6e-12,103,2.6e-12,104,2.7e-12,105,2.7e-12,106,2.7e-12,107,2.7e-12,108,2.7e-12,109,2.7e-12,110,2.8e-12,111,2.8e-12,112,2.8e-12,113,2.8e-12,114,2.8e-12,115,2.9e-12,116,2.9e-12,117,2.9e-12,118,2.9e-12,119,2.9e-12,120,2.9e-12,121,3.0e-12,122,3.0e-12,123,3.0e-12,124,3.0e-12,125,3.0e-12,126,3.0e-12,127,3.1e-12,128,3.1e-12,129,3.1e-12,130,3.1e-12,131,3.1e-12,132,3.2e-12,133,3.2e-12,134,3.2e-12,135,3.2e-12,136,3.2e-12,137,3.3e-12,138,3.3e-12,139,3.3e-12,140,3.3e-12,141,3.3e-12,142,3.4e-12,143,3.4e-12,144,3.4e-12,145,3.4e-12,146,3.4e-12,147,3.5e-12,148,3.5e-12,149,3.5e-12,150,3.5e-12,151,3.6e-12,152,3.6e-12,153,3.6e-12,154,3.6e-12,155,3.6e-12,156,3.7e-12,157,3.7e-12,158,3.7e-12,159,3.7e-12,160,3.8e-12,161,3.8e-12,162,3.8e-12,163,3.8e-12,164,3.8e-12,165,3.9e-12,166,3.9e-12,167,3.9e-12,168,3.9e-12,169,4.0e-12,170,4.0e-12,171,4.0e-12,172,4.0e-12,173,4.1e-12,174,4.1e-12,175,4.1e-12,176,4.1e-12,177,4.2e-12,178,4.2e-12,179,4.2e-12,180,4.2e-12,181,4.3e-12,182,4.3e-12,183,4.3e-12,184,4.4e-12,185,4.4e-12,186,4.4e-12,187,4.4e-12,188,4.5e-12,189,4.5e-12,190,4.5e-12,191,4.5e-12,192,4.6e-12,193,4.6e-12,194,4.6e-12,195,4.7e-12,196,4.7e-12,197,4.7e-12,198,4.7e-12,199,4.8e-12,200,4.8e-12,300,6.8e-12,400,9.0e-12,500,11.0e-12,600,11.0e-12)
```

Drain-source capacitor:

```
table(0,37200.0e-12,1,33593.0e-12,2,30335.7e-12,3,27394.2e-12,4,24738.0e-12,5,22339.3e-12,6,20543.4e-12,7,19710.9e-12,8,18912.0e-12,9,18145.6e-12,10,17410.2e-12,11,16704.6e-12,12,16027.6e-12,13,15378.1e-12,14,14754.8e-12,15,14156.9e-12,16,13583.1e-12,17,13032.6e-12,18,12504.5e-12,19,11997.7e-12,20,6398.7e-12,21,3412.6e-12,22,1820.1e-12,23,970.7e-12,24,517.7e-12,25,482.2e-12,26,449.2e-12,27,418.5e-12,28,389.8e-12,29,363.1e-12,30,338.2e-12,31,315.1e-12,32,293.5e-12,33,273.4e-12,34,254.7e-12,35,237.2e-12,36,221.0e-12,37,205.8e-12,38,191.7e-12,39,178.6e-12,40,166.4e-12,41,155.0e-12,42,144.4e-12,43,134.5e-12,44,125.3e-12,45,116.7e-12,46,108.7e-12,47,107.5e-12,48,106.3e-12,49,105.2e-12,50,104.0e-12,51,102.9e-12,52,101.7e-12,53,100.6e-12,54,99.5e-12,55,98.4e-12,56,97.3e-12,57,96.3e-12,58,95.2e-12,59,94.2e-12,60,93.1e-12,61,92.1e-12,62,91.1e-12,63,90.1e-12,64,89.1e-12,65,88.1e-12,66,87.2e-12,67,86.2e-12,68,85.3e-12,69,84.3e-12,70,83.4e-12,71,82.5e-12,72,81.6e-12,73,80.7e-12,74,79.8e-12,75,78.9e-12,76,78.1e-12,77,77.2e-12,78,76.4e-12,79,75.5e-12,80,74.7e-12,81,74.5e-12,82,74.3e-12,83,74.1e-12,84,73.9e-12,85,73.7e-12,86,73.4e-12,87,73.2e-12,88,73.0e-12,89,72.8e-12,90,72.6e-12,91,72.4e-12,92,72.2e-12,93,72.0e-12,94,71.8e-12,95,71.6e-12,96,71.4e-12,97,71.2e-12,98,71.0e-12,99,70.8e-12,100,70.6e-12,101,70.4e-12,102,70.2e-12,103,70.0e-12,104,69.8e-12,105,69.6e-12,106,69.4e-12,107,69.2e-12,108,69.0e-12,109,68.8e-12,110,68.6e-12,111,68.4e-12,112,68.2e-12,113,68.0e-12,114,67.9e-12,115,67.7e-12,116,67.5e-12,117,67.3e-12,118,67.1e-12,119,66.9e-12,120,66.7e-12,121,66.5e-12,122,66.3e-12,123,66.1e-12,124,66.0e-12,125,65.8e-12,126,65.6e-12,127,65.4e-12,128,65.2e-12,129,65.0e-12,130,64.8e-12,131,64.7e-12,132,64.5e-12,133,64.3e-12,134,64.1e-12,135,63.9e-12,136,63.8e-12,137,63.6e-12,138,63.4e-12,139,63.2e-12,140,63.0e-12,141,62.9e-12,142,62.7e-12,143,62.5e-12,144,62.3e-12,145,62.2e-12,146,62.0e-12,147,61.8e-12,148,61.6e-12,149,61.5e-12,150,61.3e-12,151,61.1e-12,152,60.9e-12,153,60.8e-12,154,60.6e-12,155,60.4e-12,156,60.3e-12,157,60.1e-12,158,59.9e-12,159,59.7e-12,160,59.6e-12,161,59.4e-12,162,59.2e-12,163,59.1e-12,164,58.9e-12,165,58.7e-12,166,58.6e-12,167,58.4e-12,168,58.2e-12,169,58.1e-12,170,57.9e-12,171,57.7e-12,172,57.6e-12,173,57.4e-12,174,57.3e-12,175,57.1e-12,176,56.9e-12,177,56.8e-12,178,56.6e-12,179,56.5e-12,180,56.3e-12,181,56.1e-12,182,56.0e-12,183,55.8e-12,184,55.7e-12,185,55.5e-12,186,55.3e-12,187,55.2e-12,188,55.0e-12,189,54.9e-12,190,54.7e-12,191,54.6e-12,192,54.4e-12,193,54.3e-12,194,54.1e-12,195,54.0e-12,196,53.8e-12,197,53.7e-12,198,53.5e-12,199,53.4e-12,200,53.2e-12,300,43.2e-12,400,39.0e-12,500,36.0e-12,600,36.0e-12)
```

Gate-source capacitor:

```
table(0,3000.0e-12,1,3000.0e-12,2,3000.0e-12,3,3000.0e-12,4,3000.0e-12,5,3000.0e-12,6,3000.4e-12,7,3001.7e-12,8,3003.1e-12,9,3004.4e-12,10,3005.7e-12,11,3007.0e-12,12,3008.4e-12,13,3009.7e-12,14,3011.0e-12,15,3012.4e-12,16,3013.7e-12,17,3015.0e-12,18,3016.4e-12,19,3017.7e-12,20,3017.7e-12,21,3017.7e-12,22,3017.7e-12,23,3017.7e-12,24,3017.7e-12,25,3017.7e-12,26,3017.7e-12,27,3017.7e-12,28,3017.7e-12,29,3017.7e-12,30,3017.7e-12,31,3017.7e-12,32,3017.7e-12,33,3017.7e-12,34,3017.7e-12,35,3017.7e-12,36,3017.7e-12,37,3017.7e-12,38,3017.7e-12,39,3017.7e-12,40,3017.7e-12,41,3017.7e-12,42,3017.7e-12,43,3017.7e-12,44,3017.7e-12,45,3017.7e-12,46,3017.7e-12,47,3017.7e-12,48,3017.7e-12,49,3017.7e-12,50,3017.7e-12,51,3017.7e-12,52,3017.7e-12,53,3017.7e-12,54,3017.7e-12,55,3017.7e-12,56,3017.7e-12,57,3017.7e-12,58,3017.7e-12,59,3017.7e-12,60,3017.7e-12,61,3017.7e-12,62,3017.7e-12,63,3017.7e-12,64,3017.7e-12,65,3017.7e-12,66,3017.7e-12,67,3017.7e-12,68,3017.7e-12,69,3017.7e-12,70,3017.7e-12,71,3017.7e-12,72,3017.7e-12,73,3017.7e-12,74,3017.7e-12,75,3017.7e-12,76,3017.7e-12,77,3017.7e-12,78,3017.7e-12,79,3017.7e-12,80,3017.7e-12,81,3017.7e-12,82,3017.7e-12,83,3017.6e-12,84,3017.6e-12,85,3017.6e-12,86,3017.6e-12,87,3017.6e-12,88,3017.5e-12,89,3017.5e-12,90,3017.5e-12,91,3017.5e-12,92,3017.4e-12,93,3017.4e-12,94,3017.4e-12,95,3017.4e-12,96,3017.4e-12,97,3017.3e-12,98,3017.3e-12,99,3017.3e-12,100,3017.3e-12,101,3017.3e-12,102,3017.2e-12,103,3017.2e-12,104,3017.2e-12,105,3017.2e-12,106,3017.2e-12,107,3017.1e-12,108,3017.1e-12,109,3017.1e-12,110,3017.1e-12,111,3017.1e-12,112,3017.0e-12,113,3017.0e-12,114,3017.0e-12,115,3017.0e-12,116,3016.9e-12,117,3016.9e-12,118,3016.9e-12,119,3016.9e-12,120,3016.9e-12,121,3016.8e-12,122,3016.8e-12,123,3016.8e-12,124,3016.8e-12,125,3016.8e-12,126,3016.7e-12,127,3016.7e-12,128,3016.7e-12,129,3016.7e-12,130,3016.7e-12,131,3016.6e-12,132,3016.6e-12,133,3016.6e-12,134,3016.6e-12,135,3016.6e-12,136,3016.5e-12,137,3016.5e-12,138,3016.5e-12,139,3016.5e-12,140,3016.4e-12,141,3016.4e-12,142,3016.4e-12,143,3016.4e-12,144,3016.4e-12,145,3016.3e-12,146,3016.3e-12,147,3016.3e-12,148,3016.3e-12,149,3016.3e-12,150,3016.2e-12,151,3016.2e-12,152,3016.2e-12,153,3016.2e-12,154,3016.2e-12,155,3016.1e-12,156,3016.1e-12,157,3016.1e-12,158,3016.1e-12,159,3016.1e-12,160,3016.0e-12,161,3016.0e-12,162,3016.0e-12,163,3016.0e-12,164,3015.9e-12,165,3015.9e-12,166,3015.9e-12,167,3015.9e-12,168,3015.9e-12,169,3015.8e-12,170,3015.8e-12,171,3015.8e-12,172,3015.8e-12,173,3015.8e-12,174,3015.7e-12,175,3015.7e-12,176,3015.7e-12,177,3015.7e-12,178,3015.7e-12,179,3015.6e-12,180,3015.6e-12,181,3015.6e-12,182,3015.6e-12,183,3015.6e-12,184,3015.5e-12,185,3015.5e-12,186,3015.5e-12,187,3015.5e-12,188,3015.4e-12,189,3015.4e-12,190,3015.4e-12,191,3015.4e-12,192,3015.4e-12,193,3015.3e-12,194,3015.3e-12,195,3015.3e-12,196,3015.3e-12,197,3015.3e-12,198,3015.2e-12,199,3015.2e-12,200,3015.2e-12,300,3013.2e-12,400,3011.0e-12,500,3009.0e-12,600,3009.0e-12)
```

The capacity values were determined from the datasheet using the following grid points:

- U_{DS} = [0 5.7 19 24 46 80 200 300 400 500 600] V
- C_{iss} = [5800 3200 3020 3020 3020 3020 3020 3020 3020 3020 3020] pF
- C_{oss} = [40000 21000 12000 520 111 77 58 50 48 47 47] pF
- C_{rss} = [2800 200 2.3 2.3 2.3 2.3 4.8 6.8 9 11 11] pF

These interpolation points were used to generate equidistantly from $0\,V$ to $200\,V$ the corresponding capacitance values. Since the datasheet represents the y-axis logarithmically, whereas LTspice interpolates linearly, the capacitance values were determined using Equation 7.1, where x_1, x_2, y_1, y_2 represent the respective grid points.

$$\log(y) = \log(y_1) + (x - x_1) \cdot \frac{\log(y_2) - \log(y_1)}{x_2 - x_1} \qquad 7.1$$

7.2.2 Superjunction IPL65R070C7 measurement model

Transfer and output characteristics:

```
Vgs1=5 Ids1=8.4 Vgs2=7 Ids2=122 Vds3=4 Ids3=59 Ids3warm=31 Vds4=16 Ids4=149 Ids4warm=87 Warm=125 VtoDelta=-0.4
```

Diode characteristics:

```
Vsd1=0.67 Isd1=0.42 Vsd2=0.838 Isd2=10.374 Breakdown=2000 Warm=125 VtoDelta2=-0.179
```

It should be noted that the breakdown voltage is merely assumed here, since a corresponding measurement was not performed. The following values were kindly provided by Lukas Spielberger, BSc.

Gate-drain capacitor:

```
table(0.000000,2.341874e-09,1.000000,1.604460e-09,2.000000,1.110038e-09,3.000000,8.142343e-10,4.000000,6.111070e-10,5.000000,4.459437e-10,6.000000,2.481925e-10,7.000000,1.652405e-10,8.000000,1.257637e-10,9.000000,1.099527e-10,10.000000,9.771747e-11,11.000000,8.934123e-11,12.000000,8.342602e-11,13.000000,8.067785e-11,14.000000,7.870027e-11,15.000000,7.794177e-11,16.000000,7.285037e-11,17.000000,6.900152e-11,18.000000,6.858142e-11,19.000000,6.512145e-11,20.000000,6.291731e-11,21.000000,9.724112e-11,22.000000,4.367802e-11,23.000000,3.222732e-11,24.000000,9.230337e-12,25.000000,4.089770e-12,26.000000,4.373479e-12,27.000000,4.639561e-12,28.000000,5.022883e-12,29.000000,5.066422e-12,30.000000,4.688375e-12,31.000000,4.859137e-12,32.000000,4.990544e-12,33.000000,4.726585e-12,34.000000,4.542790e-12,35.000000,4.628558e-12,36.000000,4.606835e-12,37.000000,4.762866e-12,38.000000,4.783248e-12,39.000000,4.591186e-12,40.000000,4.830313e-12,41.000000,4.770585e-12,42.000000,4.573368e-12,43.000000,4.510856e-12,44.000000,4.783570e-12,45.000000,4.812384e-12,46.000000,4.531666e-12,47.000000,4.943696e-12,48.000000,4.943476e-12,49.000000,5.025566e-12,50.000000,4.898957e-12,51.000000,5.031941e-12,52.000000,4.974445e-12,53.000000,4.869836e-12,54.000000,4.551699e-12,55.000000,4.595497e-12,56.000000,4.784630e-12,57.000000,5.125083e-12,58.000000,4.863350e-12,59.000000,4.863987e-12,60.000000,4.932098e-12,61.000000,5.121731e-12,62.000000,5.194694e-12,63.000000,5.400436e-12,64.000000,5.243716e-12,65.000000,4.856574e-12,66.000000,5.082732e-12,67.000000,5.128853e-12,68.000000,5.003878e-12,69.000000,5.164721e-12,70.000000,5.040751e-12,71.000000,5.001310e-12,72.000000,5.009984e-12,73.000000,4.706607e-12,74.000000,5.101804e-12,75.000000,4.927552e-12,76.000000,5.084343e-12,77.000000,5.029491e-12,78.000000,5.007163e-12,79.000000,4.842401e-12,80.000000,4.842995e-12,81.000000,4.838723e-12,82.000000,4.775021e-12,83.000000,4.675590e-12,84.000000,4.750767e-12,85.000000,5.021415e-12,86.000000,5.075213e-12,87.000000,5.094309e-12,88.000000,4.932235e-12,89.000000,5.115678e-12,90.000000,4.874433e-12,91.000000,5.097741e-12,92.000000,4.996387e-12,93.000000,4.935169e-12,94.000000,4.919522e-12,95.000000,5.055047e-12,96.000000,4.859747e-12,97.000000,4.666106e-12,98.000000,4.838117e-12,99.000000,4.880274e-12,100.000000,4.857430e-12)
```

Drain-source capacitor:

```
table(0.000000,4.160703e-08,1.000000,3.385510e-08,2.000000,2.876916e-08,3.000000,2.547595e-08,4.000000,2.320327e-08,5.000000,2.151572e-08,6.000000,2.001145e-08,7.000000,1.891588e-08,8.000000,1.800016e-08,9.000000,1.720508e-08,10.000000,1.652883e-08,11.000000,1.593429e-08,12.000000,1.539111e-08,13.000000,1.488703e-08,14.000000,1.441532e-08,15.000000,1.396340e-08,16.000000,1.355191e-08,17.000000,1.317243e-08,18.000000,1.274676e-08,19.000000,1.224881e-08,20.000000,1.165256e-08,21.000000,8.152784e-09,22.000000,4.053687e-09,23.000000,1.399302e-09,24.000000,5.414786e-10,25.000000,3.052752e-10,26.000000,2.317709e-10,27.000000,2.052248e-10,28.000000,1.940428e-10,29.000000,1.871486e-10,30.000000,1.801639e-10,31.000000,1.719551e-10,32.000000,1.628064e-10,33.000000,1.526718e-10,34.000000,1.390643e-10,35.000000,1.317959e-10,36.000000,1.278413e-10,37.000000,1.246548e-10,38.000000,1.187354e-10,39.000000,1.114211e-10,40.000000,1.078362e-10,41.000000,1.055435e-10,42.000000,1.040464e-10,43.000000,1.027199e-10,44.000000,1.010873e-10,45.000000,1.001419e-10,46.000000,9.957722e-11,47.000000,9.856852e-11,48.000000,9.788907e-11,49.000000,9.704390e-11,50.000000,9.623279e-11,51.000000,9.559049e-11,52.000000,9.471080e-11,53.000000,9.423030e-11,54.000000,9.368896e-11,55.000000,9.311764e-11,56.000000,9.224711e-11,57.000000,9.151193e-11,58.000000,9.106429e-11,59.000000,9.069783e-11,60.000000,9.007273e-11,61.000000,8.933280e-11,62.000000,8.853880e-11,63.000000,8.804451e-11,64.000000,8.731101e-11,65.000000,8.699353e-11,66.000000,8.635403e-11,67.000000,8.579461e-11,68.000000,8.513194e-11,69.000000,8.449503e-11,70.000000,8.376158e-11,71.000000,8.267140e-11,72.000000,8.188589e-11,73.000000,8.115292e-11,74.000000,7.987931e-11,75.000000,7.882030e-11,76.000000,7.769709e-11,77.000000,7.662854e-11,78.000000,7.539719e-11,79.000000,7.430783e-11,80.000000,7.340402e-11,81.000000,7.210567e-11,82.000000,7.081914e-11,83.000000,6.987652e-11,84.000000,6.899305e-11,85.000000,6.806275e-11,86.000000,6.730048e-11,87.000000,6.634365e-11,88.000000,6.562709e-11,89.000000,6.483804e-11,90.000000,6.410536e-11,91.000000,6.344098e-11,92.000000,6.321210e-11,93.000000,6.269640e-11,94.000000,6.229893e-11,95.000000,6.189586e-11,96.000000,6.148399e-11,97.000000,6.141539e-11,98.000000,6.102987e-11,99.000000,6.072984e-11,100.000000,6.051851e-11)
```

Gate-source capacitor:

```
table(0.000000,2.780417e-09,1.000000,2.916731e-09,2.000000,2.991594e-09,3.000000,3.036194e-09,4.000000,3.076216e-09,5.000000,3.123204e-09,6.000000,3.217987e-09,7.000000,3.265326e-09,8.000000,3.287439e-09,9.000000,3.296091e-09,10.000000,3.304163e-09,11.000000,3.309717e-09,12.000000,3.311126e-09,13.000000,3.311314e-09,14.000000,3.309251e-09,15.000000,3.306308e-09,16.000000,3.305784e-09,17.000000,3.306266e-09,18.000000,3.302417e-09,19.000000,3.303463e-09,20.000000,3.304652e-09,21.000000,3.446480e-09,22.000000,3.351768e-09,23.000000,3.389566e-09,24.000000,3.374044e-09,25.000000,3.353404e-09,26.000000,3.334001e-09,27.000000,3.325256e-09,28.000000,3.319413e-09,29.000000,3.313864e-09,30.000000,3.309015e-09,31.000000,3.301076e-09,32.000000,3.295583e-09,33.000000,3.290893e-09,34.000000,3.288576e-09,35.000000,3.285788e-09,36.000000,3.280643e-09,37.000000,3.280662e-09,38.000000,3.274209e-09,39.000000,3.267542e-09,40.000000,3.260005e-09,41.000000,3.257897e-09,42.000000,3.259966e-09,43.000000,3.254928e-09,44.000000,3.247622e-09,45.000000,3.243833e-09,46.000000,3.247762e-09,47.000000,3.242634e-09,48.000000,3.237260e-09,49.000000,3.233882e-09,50.000000,3.230309e-09,51.000000,3.226686e-09,52.000000,3.225881e-09,53.000000,3.218316e-09,54.000000,3.218897e-09,55.000000,3.213170e-09,56.000000,3.207012e-09,57.000000,3.204103e-09,58.000000,3.204844e-09,59.000000,3.203733e-09,60.000000,3.199319e-09,61.000000,3.189369e-09,62.000000,3.188751e-09,63.000000,3.183954e-09,64.000000,3.184025e-09,65.000000,3.181597e-09,66.000000,3.175786e-09,67.000000,3.168215e-09,68.000000,3.165915e-09,69.000000,3.163043e-09,70.000000,3.160985e-09,71.000000,3.156588e-09,72.000000,3.147096e-09,73.000000,3.147649e-09,74.000000,3.140380e-09,75.000000,3.134497e-09,76.000000,3.130523e-09,77.000000,3.133865e-09,78.000000,3.122260e-09,79.000000,3.120505e-09,80.000000,3.121293e-09,81.000000,3.120316e-09,82.000000,3.112262e-09,83.000000,3.100930e-09,84.000000,3.103080e-09,85.000000,3.099339e-09,86.000000,3.100323e-09,87.000000,3.098784e-09,88.000000,3.090632e-09,89.000000,3.085585e-09,90.000000,3.078977e-09,91.000000,3.072628e-09,92.000000,3.072124e-09,93.000000,3.079042e-09,94.000000,3.074252e-09,95.000000,3.070332e-09,96.000000,3.069250e-09,97.000000,3.060021e-09,98.000000,3.060906e-09,99.000000,3.060927e-09,100.000000,3.060198e-09)
```

- Gate connection: $0.6\ \Omega + 3.5\ nH$
- Drain connection: $0\ \Omega + 0.2\ nH$
- Source connection: $0\ \Omega + 1\ nH$

7.2.3 Silicon carbide IMZ120R060M1H datasheet model

Transfer and output characteristics:

```
Vgs1=10.8 Ids1=20 Vgs2=16 Ids2=80 Vds3=4 Ids3=51 Ids3warm=31 Vds4=20 Ids4=120 Ids4warm=93 Warm=175
VtoDelta=-1.58
```

Diode characteristics:

```
Vsd1=3.3 Isd1=5 Vsd2=4.9 Isd2=25 Breakdown=1200 Warm=175 VtoDelta2=-0.1
```

Gate-drain capacitor:

```
table(0,200.0e-12,1,190.0e-12,2,154.1e-12,3,136.3e-12,4,125.0e-12,5,80.0e-12,6,40.0e-12,7,33.0e-12,8,31.4e-12,9,30.1e-12,10,29.0e-12,11,28.0e-12,12,27.1e-12,13,26.3e-12,14,25.6e-
12,15,25.0e-12,16,24.4e-12,17,23.9e-12,18,23.4e-12,19,22.9e-12,20,22.5e-12,21,22.1e-12,22,21.7e-12,23,21.4e-12,24,21.0e-12,25,20.7e-12,26,20.4e-12,27,20.2e-12,28,19.9e-12,29,19.6e-
12,30,19.4e-12,31,19.2e-12,32,18.9e-12,33,18.7e-12,34,18.5e-12,35,18.3e-12,36,18.2e-12,37,18.0e-12,38,17.8e-12,39,17.6e-12,40,17.5e-12,41,17.3e-12,42,17.2e-12,43,17.0e-12,44,16.9e-
12,45,16.7e-12,46,16.6e-12,47,16.5e-12,48,16.3e-12,49,16.2e-12,50,16.1e-12,51,16.0e-12,52,15.9e-12,53,15.8e-12,54,15.7e-12,55,15.5e-12,56,15.4e-12,57,15.3e-12,58,15.3e-12,59,15.2e-
12,60,15.1e-12,61,15.0e-12,62,14.9e-12,63,14.8e-12,64,14.7e-12,65,14.6e-12,66,14.5e-12,67,14.5e-12,68,14.4e-12,69,14.3e-12,70,14.2e-12,71,14.2e-12,72,14.1e-12,73,14.0e-12,74,14.0e-
12,75,13.9e-12,76,13.8e-12,77,13.8e-12,78,13.7e-12,79,13.6e-12,80,13.6e-12,81,13.5e-12,82,13.4e-12,83,13.4e-12,84,13.3e-12,85,13.3e-12,86,13.2e-12,87,13.2e-12,88,13.1e-12,89,13.0e-
12,90,13.0e-12,91,12.9e-12,92,12.9e-12,93,12.8e-12,94,12.8e-12,95,12.7e-12,96,12.7e-12,97,12.6e-12,98,12.6e-12,99,12.5e-12,100,12.5e-12,101,12.5e-12,102,12.4e-12,103,12.4e-
12,104,12.3e-12,105,12.3e-12,106,12.2e-12,107,12.2e-12,108,12.1e-12,109,12.1e-12,110,12.0e-12,111,12.0e-12,112,12.0e-12,113,11.9e-12,114,11.9e-12,115,11.8e-12,116,11.8e-12,117,11.8e-
12,118,11.7e-12,119,11.7e-12,120,11.6e-12,121,11.6e-12,122,11.6e-12,123,11.5e-12,124,11.5e-12,125,11.5e-12,126,11.4e-12,127,11.4e-12,128,11.4e-12,129,11.3e-12,130,11.3e-12,131,11.3e-
12,132,11.2e-12,133,11.2e-12,134,11.2e-12,135,11.1e-12,136,11.1e-12,137,11.1e-12,138,11.0e-12,139,11.0e-12,140,11.0e-12,141,10.9e-12,142,10.9e-12,143,10.9e-12,144,10.9e-12,145,10.8e-
12,146,10.8e-12,147,10.8e-12,148,10.7e-12,149,10.7e-12,150,10.7e-12,151,10.7e-12,152,10.6e-12,153,10.6e-12,154,10.6e-12,155,10.5e-12,156,10.5e-12,157,10.5e-12,158,10.5e-12,159,10.4e-
12,160,10.4e-12,161,10.4e-12,162,10.4e-12,163,10.3e-12,164,10.3e-12,165,10.3e-12,166,10.3e-12,167,10.2e-12,168,10.2e-12,169,10.2e-12,170,10.2e-12,171,10.2e-12,172,10.1e-12,173,10.1e-
12,174,10.1e-12,175,10.1e-12,176,10.0e-12,177,10.0e-12,178,10.0e-12,179,10.0e-12,180,10.0e-12,181,9.9e-12,182,9.9e-12,183,9.9e-12,184,9.9e-12,185,9.8e-12,186,9.8e-12,187,9.8e-
12,188,9.8e-12,189,9.8e-12,190,9.7e-12,191,9.7e-12,192,9.7e-12,193,9.7e-12,194,9.7e-12,195,9.6e-12,196,9.6e-12,197,9.6e-12,198,9.6e-12,199,9.6e-12,200,9.6e-12,400,7.3e-12,800,6.5e-
12,1000,6.5e-12)
```

Drain-source capacitor:

```
table(0,900.0e-12,1,900.0e-12,2,767.8e-12,3,699.6e-12,4,655.0e-12,5,550.0e-12,6,440.0e-12,7,397.0e-12,8,375.7e-12,9,357.9e-12,10,342.7e-12,11,329.4e-12,12,317.8e-12,13,307.5e-
12,14,298.2e-12,15,289.9e-12,16,282.3e-12,17,275.3e-12,18,268.9e-12,19,262.9e-12,20,257.4e-12,21,252.3e-12,22,247.5e-12,23,243.0e-12,24,238.8e-12,25,234.8e-12,26,231.0e-12,27,227.4e-
12,28,224.1e-12,29,220.8e-12,30,217.8e-12,31,214.8e-12,32,212.0e-12,33,209.4e-12,34,206.8e-12,35,204.3e-12,36,202.0e-12,37,199.7e-12,38,197.5e-12,39,195.4e-12,40,193.4e-12,41,191.4e-
12,42,189.5e-12,43,187.7e-12,44,185.9e-12,45,184.2e-12,46,182.5e-12,47,180.9e-12,48,179.4e-12,49,177.9e-12,50,176.4e-12,51,174.9e-12,52,173.5e-12,53,172.2e-12,54,170.9e-12,55,169.6e-
12,56,168.3e-12,57,167.1e-12,58,165.9e-12,59,164.7e-12,60,163.6e-12,61,162.5e-12,62,161.4e-12,63,160.3e-12,64,159.3e-12,65,158.3e-12,66,157.3e-12,67,156.3e-12,68,155.4e-12,69,154.4e-
12,70,153.5e-12,71,152.6e-12,72,151.7e-12,73,150.9e-12,74,150.0e-12,75,149.2e-12,76,148.4e-12,77,147.6e-12,78,146.8e-12,79,146.0e-12,80,145.3e-12,81,144.5e-12,82,143.8e-12,83,143.1e-
12,84,142.4e-12,85,141.7e-12,86,141.0e-12,87,140.3e-12,88,139.7e-12,89,139.0e-12,90,138.4e-12,91,137.8e-12,92,137.1e-12,93,136.5e-12,94,135.9e-12,95,135.3e-12,96,134.8e-12,97,134.2e-
12,98,133.6e-12,99,133.1e-12,100,132.5e-12,101,131.8e-12,102,131.2e-12,103,130.5e-12,104,129.8e-12,105,129.2e-12,106,128.6e-12,107,127.9e-12,108,127.3e-12,109,126.7e-12,110,126.1e-
12,111,125.5e-12,112,125.0e-12,113,124.4e-12,114,123.8e-12,115,123.3e-12,116,122.7e-12,117,122.2e-12,118,121.6e-12,119,121.1e-12,120,120.6e-12,121,120.1e-12,122,119.6e-12,123,119.0e-
12,124,118.6e-12,125,118.1e-12,126,117.6e-12,127,117.1e-12,128,116.6e-12,129,116.2e-12,130,115.7e-12,131,115.2e-12,132,114.8e-12,133,114.3e-12,134,113.9e-12,135,113.5e-12,136,113.0e-
12,137,112.6e-12,138,112.2e-12,139,111.8e-12,140,111.3e-12,141,110.9e-12,142,110.5e-12,143,110.1e-12,144,109.7e-12,145,109.3e-12,146,109.0e-12,147,108.6e-12,148,108.2e-12,149,107.8e-
12,150,107.4e-12,151,107.1e-12,152,106.7e-12,153,106.3e-12,154,106.0e-12,155,105.6e-12,156,105.3e-12,157,104.9e-12,158,104.6e-12,159,104.3e-12,160,103.9e-12,161,103.6e-12,162,103.2e-
12,163,102.9e-12,164,102.6e-12,165,102.3e-12,166,102.0e-12,167,101.6e-12,168,101.3e-12,169,101.0e-12,170,100.7e-12,171,100.4e-12,172,100.1e-12,173,99.8e-12,174,99.5e-12,175,99.2e-
12,176,98.9e-12,177,98.6e-12,178,98.3e-12,179,98.1e-12,180,97.8e-12,181,97.5e-12,182,97.2e-12,183,96.9e-12,184,96.7e-12,185,96.4e-12,186,96.1e-12,187,95.9e-12,188,95.6e-12,189,95.3e-
12,190,95.1e-12,191,94.8e-12,192,94.6e-12,193,94.3e-12,194,94.1e-12,195,93.8e-12,196,93.6e-12,197,93.3e-12,198,93.1e-12,199,92.8e-12,200,92.6e-12,400,64.7e-12,800,51.5e-12,1000,51.5e-
12)
```

Gate-source capacitor:

```
table(0,1050.0e-12,1,1050.0e-12,2,1047.5e-12,3,1046.0e-12,4,1045.0e-12,5,1040.0e-12,6,1050.0e-12,7,1037.0e-12,8,1037.5e-12,9,1038.0e-12,10,1038.4e-12,11,1038.8e-12,12,1039.1e-
12,13,1039.4e-12,14,1039.7e-12,15,1040.0e-12,16,1040.3e-12,17,1040.5e-12,18,1040.7e-12,19,1040.9e-12,20,1041.1e-12,21,1041.3e-12,22,1041.5e-12,23,1041.7e-12,24,1041.9e-12,25,1042.0e-
12,26,1042.2e-12,27,1042.3e-12,28,1042.5e-12,29,1042.6e-12,30,1042.7e-12,31,1042.9e-12,32,1043.0e-12,33,1043.1e-12,34,1043.2e-12,35,1043.3e-12,36,1043.5e-12,37,1043.6e-12,38,1043.7e-
12,39,1043.8e-12,40,1043.9e-12,41,1044.0e-12,42,1044.1e-12,43,1044.2e-12,44,1044.2e-12,45,1044.3e-12,46,1044.4e-12,47,1044.5e-12,48,1044.6e-12,49,1044.7e-12,50,1044.8e-12,51,1044.8e-
12,52,1044.9e-12,53,1045.0e-12,54,1045.1e-12,55,1045.1e-12,56,1045.2e-12,57,1045.3e-12,58,1045.3e-12,59,1045.4e-12,60,1045.5e-12,61,1045.5e-12,62,1045.6e-12,63,1045.7e-12,64,1045.7e-
12,65,1045.8e-12,66,1045.9e-12,67,1045.9e-12,68,1046.0e-12,69,1046.0e-12,70,1046.1e-12,71,1046.1e-12,72,1046.2e-12,73,1046.3e-12,74,1046.3e-12,75,1046.4e-12,76,1046.4e-12,77,1046.5e-
12,78,1046.5e-12,79,1046.6e-12,80,1046.6e-12,81,1046.7e-12,82,1046.7e-12,83,1046.8e-12,84,1046.8e-12,85,1046.9e-12,86,1046.9e-12,87,1046.9e-12,88,1047.0e-12,89,1047.0e-12,90,1047.1e-
12,91,1047.1e-12,92,1047.2e-12,93,1047.2e-12,94,1047.3e-12,95,1047.3e-12,96,1047.3e-12,97,1047.4e-12,98,1047.4e-12,99,1047.5e-12,100,1047.5e-12,101,1047.5e-12,102,1047.6e-
12,103,1047.6e-12,104,1047.6e-12,105,1047.7e-12,106,1047.7e-12,107,1047.8e-12,108,1047.8e-12,109,1047.8e-12,110,1047.9e-12,111,1047.9e-12,112,1047.9e-12,113,1048.0e-12,114,1048.0e-
12,115,1048.0e-12,116,1048.1e-12,117,1048.1e-12,118,1048.1e-12,119,1048.2e-12,120,1048.2e-12,121,1048.2e-12,122,1048.2e-12,123,1048.3e-12,124,1048.3e-12,125,1048.3e-12,126,1048.4e-
12,127,1048.4e-12,128,1048.4e-12,129,1048.5e-12,130,1048.5e-12,131,1048.5e-12,132,1048.5e-12,133,1048.6e-12,134,1048.6e-12,135,1048.6e-12,136,1048.7e-12,137,1048.7e-12,138,1048.7e-
12,139,1048.7e-12,140,1048.8e-12,141,1048.8e-12,142,1048.8e-12,143,1048.8e-12,144,1048.9e-12,145,1048.9e-12,146,1048.9e-12,147,1048.9e-12,148,1049.0e-12,149,1049.0e-12,150,1049.0e-
12,151,1049.0e-12,152,1049.1e-12,153,1049.1e-12,154,1049.1e-12,155,1049.1e-12,156,1049.2e-12,157,1049.2e-12,158,1049.2e-12,159,1049.2e-12,160,1049.3e-12,161,1049.3e-12,162,1049.3e-
12,163,1049.3e-12,164,1049.4e-12,165,1049.4e-12,166,1049.4e-12,167,1049.4e-12,168,1049.4e-12,169,1049.5e-12,170,1049.5e-12,171,1049.5e-12,172,1049.5e-12,173,1049.6e-12,174,1049.6e-
12,175,1049.6e-12,176,1049.6e-12,177,1049.6e-12,178,1049.7e-12,179,1049.7e-12,180,1049.7e-12,181,1049.7e-12,182,1049.7e-12,183,1049.8e-12,184,1049.8e-12,185,1049.8e-12,186,1049.8e-
12,187,1049.8e-12,188,1049.9e-12,189,1049.9e-12,190,1049.9e-12,191,1049.9e-12,192,1049.9e-12,193,1050.0e-12,194,1050.0e-12,195,1050.0e-12,196,1050.0e-12,197,1050.0e-12,198,1050.1e-
12,199,1050.1e-12,200,1050.1e-12,400,1052.7e-12,800,1053.5e-12,1000,1053.5e-12)
```

The capacity values were determined from the datasheet using the following grid points:

- U_{DS} = [0 1 4 5 6 7 100 400 800 1000] V
- C_{iss} = [1250 1240 1170 1120 1090 1070 1060 1060 1060 1060] pF
- C_{oss} = [1100 1090 780 630 480 430 145 72 58 58] pF
- C_{rss} = [200 190 125 80 40 33 12.5 7.3 6.5 6.5] pF

These interpolation points were used to generate equidistantly from $0\,V$ to $200\,V$ the corresponding capacitance values. Since the datasheet shows the capacitance in a double-logarithmic plot, whereas LTspice interpolates linearly, the capacitance values were determined using Equation 7.2, where x_1, x_2, y_1, y_2 represent the respective grid points.

$$\log(y) = \log(y_1) + (\log(x) - \log(x_1)) \cdot \frac{\log(y_2) - \log(y_1)}{\log(x_2) - \log(x_1)} \qquad 7.2$$

7.2.4 Silicon carbide IMZ120R060M1H measurement model

Transfer and output characteristics:

```
Vgs1=10 Ids1=19 Vgs2=14 Ids2=70 Vds3=4 Ids3=48.7 Ids3warm=33.9 Vds4=20 Ids4=115.7 Ids4warm=99 Warm=175
VtoDelta=-1.2
```

Diode characteristics:

```
Vsd1=2.29 Isd1=0.42 Vsd2=3.5 Isd2=9.3 Breakdown=2000 Warm=175 VtoDelta2=-0.15
```

It should be noted that the breakdown voltage is merely assumed here, since a corresponding measurement was not performed.

Gate-drain capacitor:

```
table(0,303.9e-12,1,258.3e-12,2,224.3e-12,3,198.7e-12,4,153.7e-12,5,75.2e-12,6,66.7e-12,7,62.4e-12,8,59.3e-12,9,56.6e-12,10,54.7e-12,11,52.6e-12,12,50.9e-12,13,49.5e-12,14,48.0e-12,15,46.9e-12,16,45.8e-
12,17,44.9e-12,18,43.9e-12,19,43.0e-12,20,42.3e-12,21,41.5e-12,22,40.8e-12,23,40.2e-12,24,39.6e-12,25,39.1e-12,26,38.6e-12,27,38.0e-12,28,37.5e-12,29,37.0e-12,30,36.4e-12,31,36.0e-12,32,35.6e-12,33,35.2e-
12,34,34.8e-12,35,34.4e-12,36,34.0e-12,37,33.7e-12,38,33.4e-12,39,33.0e-12,40,32.7e-12,41,32.4e-12,42,32.1e-12,43,31.9e-12,44,31.6e-12,45,31.3e-12,46,31.1e-12,47,30.8e-12,48,30.6e-12,49,30.4e-12,50,30.1e-
12,51,29.9e-12,52,29.7e-12,53,29.5e-12,54,29.3e-12,55,29.1e-12,56,28.9e-12,57,28.7e-12,58,28.5e-12,59,28.3e-12,60,28.2e-12,61,28.0e-12,62,27.8e-12,63,27.6e-12,64,27.5e-12,65,27.3e-12,66,27.2e-12,67,27.0e-
12,68,26.9e-12,69,26.7e-12,70,26.6e-12,71,26.4e-12,72,26.3e-12,73,26.2e-12,74,26.0e-12,75,25.9e-12,76,25.8e-12,77,25.7e-12,78,25.5e-12,79,25.4e-12,80,25.3e-12,81,25.2e-12,82,25.1e-12,83,25.0e-12,84,24.8e-
12,85,24.7e-12,86,24.6e-12,87,24.5e-12,88,24.4e-12,89,24.3e-12,90,24.2e-12,91,24.1e-12,92,24.0e-12,93,23.9e-12,94,23.8e-12,95,23.7e-12,96,23.6e-12,97,23.6e-12,98,23.5e-12,99,23.4e-12,100,23.3e-12,101,23.2e-
12,102,23.1e-12,103,23.0e-12,104,22.9e-12,105,22.9e-12,106,22.8e-12,107,22.7e-12,108,22.6e-12,109,22.6e-12,110,22.5e-12,111,22.4e-12,112,22.3e-12,113,22.3e-12,114,22.2e-12,115,22.1e-12,116,22.0e-
12,117,22.0e-12,118,21.9e-12,119,21.8e-12,120,21.8e-12,121,21.7e-12,122,21.6e-12,123,21.6e-12,124,21.5e-12,125,21.4e-12,126,21.4e-12,127,21.3e-12,128,21.2e-12,129,21.2e-12,130,21.1e-12,131,21.1e-
12,132,21.0e-12,133,20.9e-12,134,20.9e-12,135,20.8e-12,136,20.8e-12,137,20.7e-12,138,20.7e-12,139,20.6e-12,140,20.6e-12,141,20.5e-12,142,20.4e-12,143,20.4e-12,144,20.3e-12,145,20.3e-12,146,20.2e-
12,147,20.2e-12,148,20.1e-12,149,20.1e-12,150,20.0e-12,151,20.0e-12,152,19.9e-12,153,19.9e-12,154,19.8e-12,155,19.8e-12,156,19.7e-12,157,19.7e-12,158,19.6e-12,159,19.6e-12,160,19.6e-12,161,19.5e-
12,162,19.5e-12,163,19.4e-12,164,19.4e-12,165,19.3e-12,166,19.3e-12,167,19.2e-12,168,19.2e-12,169,19.2e-12,170,19.1e-12,171,19.1e-12,172,19.0e-12,173,19.0e-12,174,19.0e-12,175,18.9e-12,176,18.9e-
12,177,18.8e-12,178,18.8e-12,179,18.8e-12,180,18.7e-12,181,18.7e-12,182,18.6e-12,183,18.6e-12,184,18.6e-12,185,18.5e-12,186,18.5e-12,187,18.5e-12,188,18.4e-12,189,18.4e-12,190,18.3e-12,191,18.3e-
12,192,18.3e-12,193,18.2e-12,194,18.2e-12,195,18.2e-12,196,18.1e-12,197,18.1e-12,198,18.1e-12,199,18.0e-12,200,18.0e-12)
```

Drain-source capacitor:

```
table(0,712.5e-12,1,655.6e-12,2,593.8e-12,3,547.7e-12,4,490.9e-12,5,355.3e-12,6,327.4e-12,7,308.5e-12,8,293.5e-12,9,281.2e-12,10,270.9e-12,11,261.6e-12,12,253.5e-12,13,246.0e-12,14,239.4e-12,15,233.3e-
12,16,228.0e-12,17,222.8e-12,18,217.9e-12,19,213.6e-12,20,209.6e-12,21,205.6e-12,22,201.7e-12,23,198.2e-12,24,195.0e-12,25,191.9e-12,26,189.0e-12,27,186.0e-12,28,183.4e-12,29,181.0e-12,30,178.7e-
12,31,176.5e-12,32,174.4e-12,33,172.4e-12,34,170.4e-12,35,168.6e-12,36,166.8e-12,37,165.0e-12,38,163.4e-12,39,161.8e-12,40,160.2e-12,41,158.7e-12,42,157.3e-12,43,155.9e-12,44,154.5e-12,45,153.2e-
12,46,152.0e-12,47,150.7e-12,48,149.5e-12,49,148.4e-12,50,147.2e-12,51,146.1e-12,52,145.0e-12,53,144.0e-12,54,143.0e-12,55,142.0e-12,56,141.0e-12,57,140.1e-12,58,139.2e-12,59,138.3e-12,60,137.4e-
12,61,136.5e-12,62,135.7e-12,63,134.9e-12,64,134.1e-12,65,133.3e-12,66,132.5e-12,67,131.7e-12,68,131.0e-12,69,130.3e-12,70,129.6e-12,71,128.9e-12,72,128.2e-12,73,127.5e-12,74,126.9e-12,75,126.2e-
12,76,125.6e-12,77,125.0e-12,78,124.4e-12,79,123.8e-12,80,123.2e-12,81,122.6e-12,82,122.0e-12,83,121.5e-12,84,120.9e-12,85,120.4e-12,86,119.8e-12,87,119.3e-12,88,118.8e-12,89,118.3e-12,90,117.8e-
12,91,117.3e-12,92,116.8e-12,93,116.3e-12,94,115.9e-12,95,115.4e-12,96,114.9e-12,97,114.5e-12,98,114.0e-12,99,113.6e-12,100,113.2e-12,101,112.7e-12,102,112.3e-12,103,111.9e-12,104,111.5e-12,105,111.1e-
12,106,110.7e-12,107,110.3e-12,108,109.9e-12,109,109.5e-12,110,109.2e-12,111,108.8e-12,112,108.4e-12,113,108.0e-12,114,107.7e-12,115,107.3e-12,116,107.0e-12,117,106.6e-12,118,106.3e-12,119,105.9e-
12,120,105.6e-12,121,105.3e-12,122,104.9e-12,123,104.6e-12,124,104.3e-12,125,104.0e-12,126,103.7e-12,127,103.4e-12,128,103.1e-12,129,102.7e-12,130,102.4e-12,131,102.2e-12,132,101.9e-12,133,101.6e-
12,134,101.3e-12,135,101.0e-12,136,100.7e-12,137,100.4e-12,138,100.2e-12,139,99.9e-12,140,99.6e-12,141,99.3e-12,142,99.1e-12,143,98.8e-12,144,98.5e-12,145,98.3e-12,146,98.0e-12,147,97.8e-12,148,97.5e-
12,149,97.3e-12,150,97.0e-12,151,96.8e-12,152,96.5e-12,153,96.3e-12,154,96.1e-12,155,95.8e-12,156,95.6e-12,157,95.4e-12,158,95.1e-12,159,94.9e-12,160,94.7e-12,161,94.5e-12,162,94.2e-12,163,94.0e-
12,164,93.8e-12,165,93.6e-12,166,93.4e-12,167,93.2e-12,168,93.0e-12,169,92.7e-12,170,92.5e-12,171,92.3e-12,172,92.1e-12,173,91.9e-12,174,91.7e-12,175,91.5e-12,176,91.3e-12,177,91.1e-12,178,90.9e-
12,179,90.7e-12,180,90.5e-12,181,90.4e-12,182,90.2e-12,183,90.0e-12,184,89.8e-12,185,89.6e-12,186,89.4e-12,187,89.2e-12,188,89.1e-12,189,88.9e-12,190,88.7e-12,191,88.5e-12,192,88.4e-12,193,88.2e-
12,194,88.0e-12,195,87.8e-12,196,87.7e-12,197,87.5e-12,198,87.3e-12,199,87.2e-12,200,87.0e-12)
```

Gate-source capacitor:

```
table(0,806.2e-12,1,822.9e-12,2,834.4e-12,3,842.4e-12,4,859.9e-12,5,914.9e-12,6,907.7e-12,7,910.2e-12,8,912.2e-12,9,914.2e-12,10,916.0e-12,11,918.1e-12,12,918.9e-12,13,920.3e-12,14,921.0e-12,15,922.0e-
12,16,923.3e-12,17,923.2e-12,18,924.6e-12,19,924.6e-12,20,926.4e-12,21,925.6e-12,22,927.0e-12,23,926.8e-12,24,928.3e-12,25,928.3e-12,26,929.0e-12,27,929.4e-12,28,929.2e-12,29,929.4e-12,30,930.9e-
12,31,931.2e-12,32,931.5e-12,33,931.8e-12,34,932.1e-12,35,932.4e-12,36,932.7e-12,37,932.9e-12,38,933.2e-12,39,933.4e-12,40,933.7e-12,41,933.9e-12,42,934.1e-12,43,934.4e-12,44,934.6e-12,45,934.8e-
12,46,935.0e-12,47,935.2e-12,48,935.4e-12,49,935.6e-12,50,935.8e-12,51,936.0e-12,52,936.2e-12,53,936.4e-12,54,936.6e-12,55,936.7e-12,56,936.9e-12,57,937.1e-12,58,937.3e-12,59,937.4e-12,60,937.6e-
12,61,937.7e-12,62,937.9e-12,63,938.1e-12,64,938.2e-12,65,938.4e-12,66,938.5e-12,67,938.7e-12,68,938.8e-12,69,938.9e-12,70,939.1e-12,71,939.2e-12,72,939.4e-12,73,939.5e-12,74,939.6e-12,75,939.8e-
12,76,939.9e-12,77,940.0e-12,78,940.1e-12,79,940.3e-12,80,940.4e-12,81,940.5e-12,82,940.6e-12,83,940.7e-12,84,940.9e-12,85,941.0e-12,86,941.1e-12,87,941.2e-12,88,941.3e-12,89,941.4e-12,90,941.5e-
12,91,941.6e-12,92,941.7e-12,93,941.8e-12,94,941.9e-12,95,942.0e-12,96,942.1e-12,97,942.2e-12,98,942.3e-12,99,942.4e-12,100,942.5e-12,101,942.6e-12,102,942.7e-12,103,942.8e-12,104,942.9e-12,105,943.0e-
12,106,943.1e-12,107,943.2e-12,108,943.3e-12,109,943.4e-12,110,943.5e-12,111,943.6e-12,112,943.7e-12,113,943.7e-12,114,943.8e-12,115,943.9e-12,116,944.0e-12,117,944.1e-12,118,944.2e-12,119,944.2e-
12,120,944.3e-12,121,944.4e-12,122,944.5e-12,123,944.6e-12,124,944.6e-12,125,944.7e-12,126,944.8e-12,127,944.9e-12,128,945.0e-12,129,945.0e-12,130,945.1e-12,131,945.2e-12,132,945.3e-12,133,945.3e-
12,134,945.4e-12,135,945.5e-12,136,945.5e-12,137,945.6e-12,138,945.7e-12,139,945.8e-12,140,945.8e-12,141,945.9e-12,142,946.0e-12,143,946.0e-12,144,946.1e-12,145,946.2e-12,146,946.2e-12,147,946.3e-
12,148,946.4e-12,149,946.4e-12,150,946.5e-12,151,946.6e-12,152,946.6e-12,153,946.7e-12,154,946.8e-12,155,946.8e-12,156,946.9e-12,157,946.9e-12,158,947.0e-12,159,947.1e-12,160,947.1e-12,161,947.2e-
12,162,947.3e-12,163,947.3e-12,164,947.4e-12,165,947.4e-12,166,947.5e-12,167,947.6e-12,168,947.6e-12,169,947.7e-12,170,947.7e-12,171,947.8e-12,172,947.8e-12,173,947.9e-12,174,948.0e-12,175,948.0e-
12,176,948.1e-12,177,948.1e-12,178,948.2e-12,179,948.2e-12,180,948.3e-12,181,948.3e-12,182,948.4e-12,183,948.4e-12,184,948.5e-12,185,948.6e-12,186,948.6e-12,187,948.7e-12,188,948.7e-12,189,948.8e-
12,190,948.8e-12,191,948.9e-12,192,948.9e-12,193,949.0e-12,194,949.0e-12,195,949.1e-12,196,949.1e-12,197,949.2e-12,198,949.2e-12,199,949.3e-12,200,949.3e-12)
```

- Gate connection: $2.4\ \Omega + 7.3\ nH$
- Drain connection: $0.13\ \Omega + 3.3\ nH$
- Source connection: $0.13\ \Omega + 0.6\ nH$