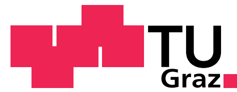

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Simulation and verification of a simple circuit over a high frequency range with DPI method

Master's Thesis

to achieve the university degree of

Master of Science

Master's degree programme: Elektrotechnik

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Signature

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Abstract

The direct power injection (DPI) method is used as a standard to determine the immunity of an electronic Integrated Circuit (IC) to conducted electromagnetic Radio Frequency (RF) disturbance in a frequency range from 150 kHz to 1 GHz. The aim of this thesis is to extend the DPI-test standard to a frequency range of 150 kHz-6 GHz and provide an accurate simulation model for pre tape out simulation of upcoming ICs. This is important because a faster communication between electronic devices leads to a faster switching and more noise in the higher frequency domain. The model includes parasitic elements of the chip and printed circuit board (PCB) environment. For verification, the test chip is tested up to 6 GHz using the extended DPI standard. Following, the results of the model and measurement are compared.

It is possible to create a DPI test board which fits the extended DPI-test standard. A decoupling network is found that has over 400 Ω over the whole frequency range and 50 Ω transmission lines are designed that have an attenuation over -3 dB. The measurement is done in two steps from 150 kHz to 1 GHz and from 2 MHz to 6 GHz and compared with the simulation results. The simulation tends to the measurement results for lower insertion power levels close to 9 dBm and lower frequencies up to 100 MHz. For higher power levels and frequencies the simulation is inaccurate. Nevertheless a simulation test bench and a measurement setup are created which could be used for upcoming theses.

Kurzfassung

Die Direct Power Injection (DPI)-Methode wird als Standard zur Bestimmung der Störfestigkeit einer integrierten Schaltung (IC) gegenüber leitungsgebundener elektromagnetischer Hochfrequenz (HF)-Störung in einem Frequenzbereich von 150 kHz bis 1 GHz verwendet. Das Ziel dieser Arbeit ist es, den DPI-Test-Standard auf einen Frequenzbereich von 150 kHz-6 GHz zu erweitern und ein genaues Simulationsmodell für die Pre-Tape-Out-Simulation kommender ICs bereitzustellen. Dies ist wichtig, da eine schnellere Kommunikation zwischen elektronischen Geräten zu einem schnelleren Schalten und mehr Rauschen im höheren Frequenzbereich führt. Das Modell beinhaltet parasitäre Elemente des Chips und der Leiterplattenumgebung (PCB). Zur Verifikation wird der Testchip bis zu 6 GHz unter Verwendung des erweiterten DPI-Standards getestet. Anschließend werden die Ergebnisse des Modells und der Messung verglichen.

Es ist möglich, eine DPI-Testplatine zu erstellen, die dem erweiterten DPI-Teststandard entspricht. Es wird ein Entkopplungsnetzwerk gefunden, das über den gesamten Frequenzbereich über 400 Ω hat und es werden 50 Ω Übertragungsleitungen entworfen, die eine Dämpfung über -3 dB haben. Die Messung wird in zwei Schritten von 150 kHz bis 1 GHz und von 2 MHz bis 6 GHz durchgeführt und mit den Simulationsergebnissen verglichen. Die Simulation stimmt bei niedrigeren Störleistungen bis 9 dBm und niedrigeren Frequenzen bis 100 MHz mit den Messergebnissen bis auf einen geringen Fehler überein. Für höhere Leistungspegel und Frequenzen ist die Simulation ungenau. Nichtsdestotrotz wurde ein Simulationsprüfstand und ein Messaufbau erstellt, der für kommende Diplomarbeiten verwendet werden kann.

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1 State of the Art

1.1 Introduction

In this thesis a Direct Power Injection (DPI) Method measurement will be performed and for this reason several papers about DPI-Method and the current DPI test-standard are observed. Papers on modelling have also been examined and are briefly summarized here.

1.2 Motivation

The motivation behind this thesis lies in the increasing communication speeds between electronic devises and its impact on electromagnetic immunity. To recognize this behaviour at an early stage in development, a model is made and the DPI measurement is simulated. As a test subject a simple band-gap-reference circuit of a test-chip is taken. A printed circuit board (PCB) for the DPI measurement is made and for modelling purposes a parasitic extraction of this test-chip is done by Cadence Assura. Cables, transmission lines and the PCB itself are calculated by a finite element tool and also from the manufacturer of the PCB to have a 50Ω impedance $Z0$ System. This data is also used for simulation to get better parasitic behaviour. Later the simulation and the measurement are compared.

1.3 Direct Power Injection Method

The DPI Method is described in the Standard IEC-62132-4 [6]. This standard describes a method to measure the immunity of integrated circuits in the presence of conducted radio frequency (RF) disturbances. The RF-power is directly applied to a single pin or a group of pins having the same circuitry and layout. A capacitor shall be used, which performs as a DC block to avoid supplying DC current into the output of the RF signal generator and the amplifier. To avoid RF interference to the power supply of the IC under test, decoupling networks (DCNs) having high RF- impedances are used. The principle hardware test setup for the DPI method is shown in figure 1.1. The disturbance signal is provided by a frequency variable RF-Generator, which is connected to RF amplifier. At the RF injection port on the printed circuit board (PCB) the disturbance is connected to one or more pins of the device under test (DUT). Between RF amplifier and DC-block is a bi directional coupler (BDC) which makes it possible to measures the forward and the reflected power with power meters. The RF-signal enters port 1 of the BDC and comes out of port 2 undisturbed. On port 3 and 4 power meters can measure the forward power P_{for} and the reflected power P_{ref}. The forward power is the power the electromagnetic wave carries to the DUT.

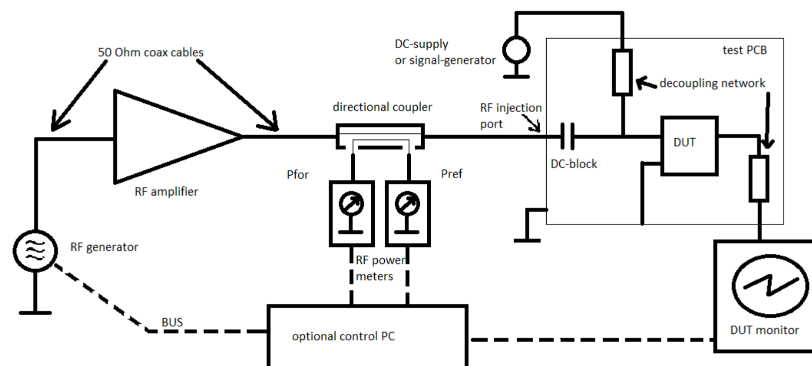


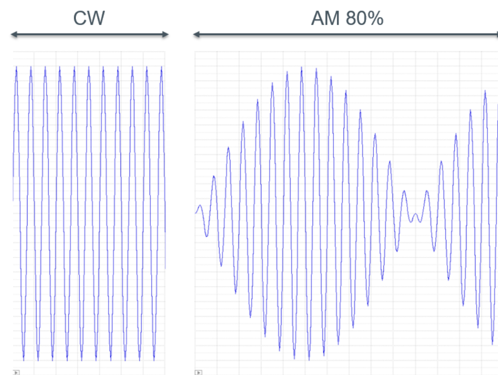
Figure 1.1: IEC 62132-4 block diagram [6]

The disturbance signal and other general conditions and definitions are defined in IEC62132-1:2015 [7]. The signal is either a continuous wave

(CW) or an amplitude modulated (AM) signal (see in figure 1.2). The basic requirement, when carrying out an immunity test, is that the peak power of the AM test signal shall have the same peak power as the unmodulated signal, regardless of the modulation index m (see equations 1.1 and 1.2). If an AM is chosen, the AM signal has a frequency of 1 kHz and carries the RF-signal.

$$P_{AM-Peak} = P_{CW-Peak} \tag{1.1}$$

$$P_{AM} = P_{CW} \cdot \frac{2+m^2}{2(1+m)^2} \tag{1.2}$$



Note! For example: 80% AM modulation (m=0,8) results in: $P_{AM} = 0{,}407 \times P_{CW}, m = \frac{(Max-Min)}{(Max+Min)}$

Figure 1.2: RF-signal when RF peak power level is maintained

The DPI specific measuring method [6] is performed via a sequence of frequency steps and measurement level steps. Figure 1.3 shows the flow chart sequence of the specific HF-power feed.

At each frequency to be tested, the forward power supplied to the DUT starts at low levels, for example 20 dB below the forward power specified for the measurement. The level can then be increased in steps until a malfunction is observed or the specified forward power level is reached. Each power level must be applied to the IC (dwell time) long enough to allow the IC to react (for example: if time functions are included in the DUT). The recommended default value for the power level steps can be 0.5 dB. The default values for the frequency steps and the dwell time are defined in IEC

62132-1 [7].

In addition, power stepping can be started at a fixed forward power level and the level can be decreased in steps until the desired function or the lowest forward power level is reached. This procedure significantly reduces the total duration of the measurement procedure for a very interference-resistant DUT.

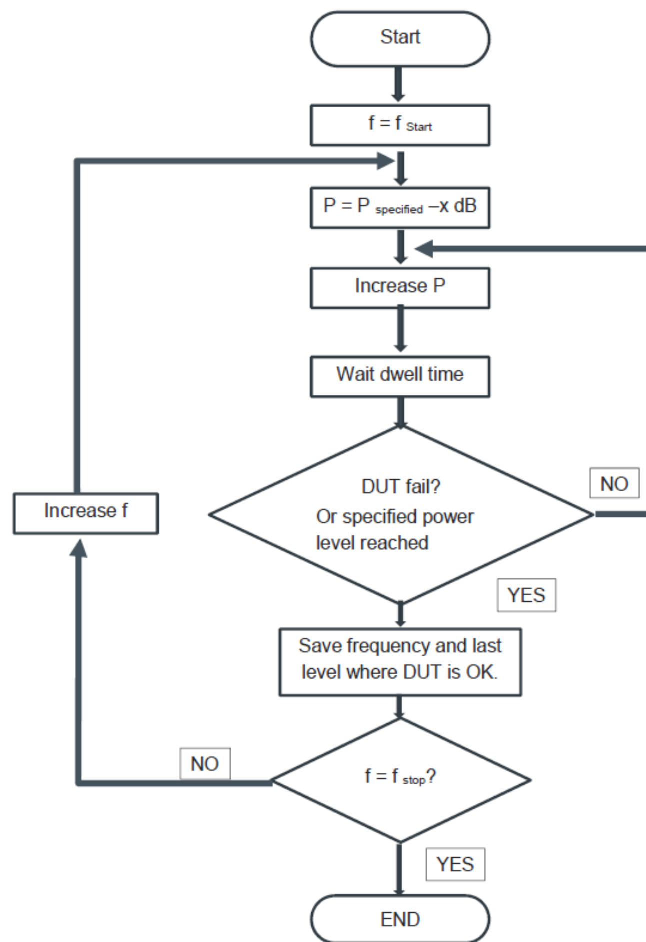


Figure 1.3: Flow chart of the DPI method

1.4 Design of high frequency DPI method

"Design of a 20 GHz DPI method for SOIC8" [8]
This paper describes a way to introduce a DPI measurement over 20 GHz on a normal FR4 PCB, due to proposed interesting conducted immunity issues above 1 *GHz*. The most interesting part of this paper for this thesis is the PCB Modelling chapter. It suggests to not put the needed periphery on the PCB, but off board. This approach provides good re-usability of the board, as the peripherals can be changed to accommodate each DPI test (see at Figure 1.4). In order to know the transmitted power, it is proposed to measure all S-parameters of all modules, cables/adapters that interconnect them. Small outline integrated circuit (SOIC) is a package form of a chip. The number 8 describes the number of pins the integrated circuit has.

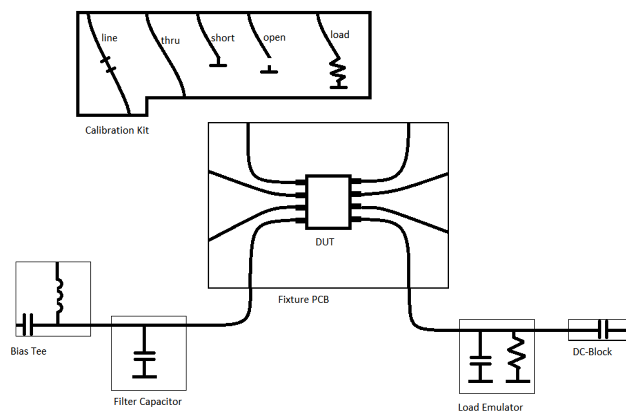


Figure 1.4: DUT fixture with example periphery. Signal generator and directional coupler not shown.

1.5 PCB design

To get an idea of DPI-Method measurement, it is good to start with the design of the DPI-test PCB. The paper by Andrea Lavarda and Bernd Deutschmann serves as the first source of information: "Enhancement of

the DPI method for IC immunity characterization" [9] This paper focuses on how to optimize the DPI test bench for highly reflective low voltage devices under test (DUTs). The injection network and decoupling network are described with a reference to the IEC standard. The decoupling network should have an impedance over 400Ω over the whole frequency range, which is shown in the example schematic in figure 1.5 and the impedance plot shown in figure 1.6. The DC block capacitor protects the RF-generator from DC-currents which could lead otherwise to its destruction. The paper gives tips how to accomplish the task of creating such networks and test boards.

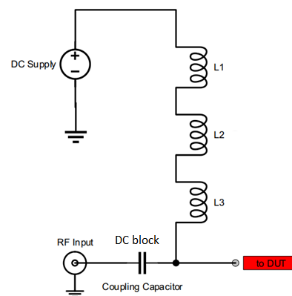


Figure 1.5: Injection network example

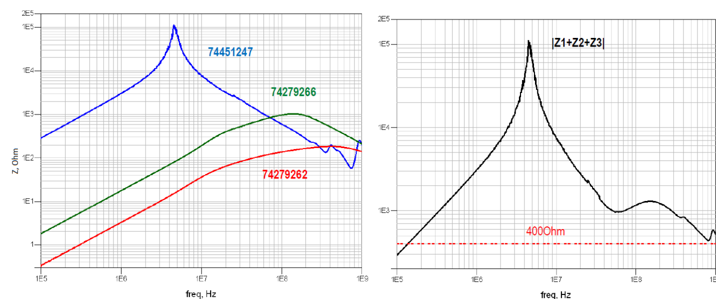


Figure 1.6: Impedance of example injection networks

1.6 50 Ohm Impedance Lines

For transmitting RF-signals well defined transmissions lines are needed. The basics of the calculation of transmission lines, in particular coplanar waveguide with ground (see in figure 1.7) can be be found in the book *Transmission Line Design Handbook*.

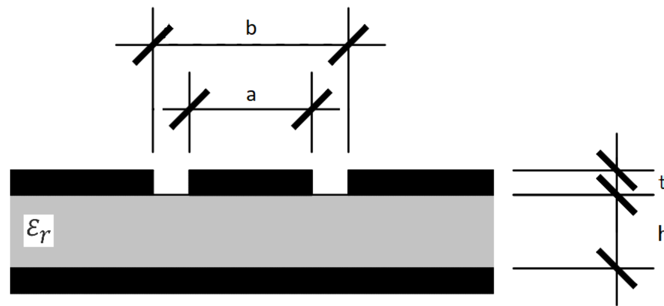


Figure 1.7: Coplanar waveguide with ground cross section

$$Z_0 = \frac{\eta_0}{2.0\sqrt{\epsilon_{eff}}} \cdot \frac{1.0}{\frac{K(k)}{K(k')} + \frac{K(k_1)}{K(k_1')}} \tag{1.3}$$

$$k = \frac{a}{b} \tag{1.4}$$

$$k' = \sqrt{1.0 - k^2} \tag{1.5}$$

$$k_1' = \sqrt{1.0 - k_1^2} \tag{1.6}$$

$$k_1 = \frac{tanh(\frac{\pi a}{4.0h})}{tanh(\frac{\pi b}{4.0h})} \tag{1.7}$$

$$\epsilon_{eff} = \frac{1.0 + \epsilon_r \frac{K(k')}{K(k)} \frac{K(k_1)}{K(k_1')}}{1.0 + \frac{K(k')}{K(k)} \frac{K(k_1)}{K(k_1')}} \tag{1.8}$$

The recursive equations $K(k)$ were originally mentioned first by Miller in the article "Inductance formula for a single-layer circular coil"[10].

To calculate the complete elliptic integral of th first kind, start the calculation with the initial values a_0, b_0 and c_0 and iterate until $c_N = 0$ to within the desired accuracy.

$$a_0 = 1.0 \tag{1.9}$$
$$b_0 = \sqrt{1.0 - k^2} \tag{1.10}$$
$$c_0 = k \tag{1.11}$$
$$K(k) = \frac{\pi}{2 \cdot a_N} \tag{1.12}$$
$$\tag{1.13}$$

$$a_n = \frac{a_{n-1} + b_{n-1}}{2} \tag{1.14}$$
$$b_n = \sqrt{a_{n-1} \cdot b_{n-1}} \tag{1.15}$$
$$K(k) = \frac{\pi}{2 \cdot a_N} \tag{1.16}$$
$$\tag{1.17}$$

This equations should be enough for a rough design of the transmission line. It can be calculated using an online calculator (see at [4]). To be more precise than this calculations in this work a calculation program is used by the manufacturer of the PCB designed in this thesis. For the boards which are designed in this thesis a resistance of 49.89 Ω is calculated by the manufacturer of the board.

1.7 Band gap reference

Band gap references are designed to produce a stable voltage output that is stable over temperature change and can be used by other circuits as a reference. In figure 1.8 a first order current mirror based band gap reference as mentioned in the Paper "Design of an improved bandgap reference in 180nm CMOS process technology" [2] is shown. This band gap reference is similar to the used band gap in this thesis. The band gap consists of two poly resistors $R1$ and $R2$, three diode connected vertical PNP bipolar transistors denoted by Q1, Q2 and Q3, five MOS transistors denoted by $M1$, $M2$, $M3$, $M4$ and $M5$. The current mirror is designed to bias all three bipolar junction transistors with identical currents using the other PMOS transistors $M3$, $M4$ and $M5$.

$$V_{REF} = V_{BE3} + \frac{R_2}{R_1} \cdot ln(N) \cdot V_T \tag{1.18}$$

With equation 1.18 the output voltage V_{REF} can be calculated. The negative temperature co-efficient of V_{BE3} is compensated by the second term with scaling factor $R2/R1 \cdot ln(N)$ and the thermal voltage V_T which are proportional to absolute temperature in nature.

At DPI tests usually the supply of the band gap is disturbed and the the extent of the DC-shift of the output voltage is taken as abort condition.

Figure 1.8: Band gap reference

2 Test structures

To get knowledge about the behaviour of different passive devices like capacitors, inductors and ferrites a test board is developed. For measuring, a vector network analyser (VNA) from Rohde & Schwarz is used. With the gathered knowledge a DPI Measurement Board is designed.

2.1 Component test board

The designed test board includes an on board calibrating kit. It has several test structures for testing the different components mentioned above. Additionally various SMA connectors and component setups can be tested with this test board. Figure 2.1 shows the schematic of PCB. To get a good frequency behaviour, Rogers 4350 material is used. 50 Ω Impedance lines are calculated with Altium and for verification with the calculator of the manufacturer (Polar Instruments). In order to be able to place different components with different footprints on the printed circuit board, the solder mask was omitted. In order to get smaller PCBs without cutting devices, scoring was done at the separation lines between the on board calibration kit and the test structures for single components and between the DCN test structures. The board can be observed in figure 2.2 and 2.3.

2.1.1 On board calibration

To get rid of parasitic inductances introduced by SMA-coaxial cables, connectors and transmission lines, a calibration of the VNA must be done. To be more precise, an on-board calibration standard is created. This calibration

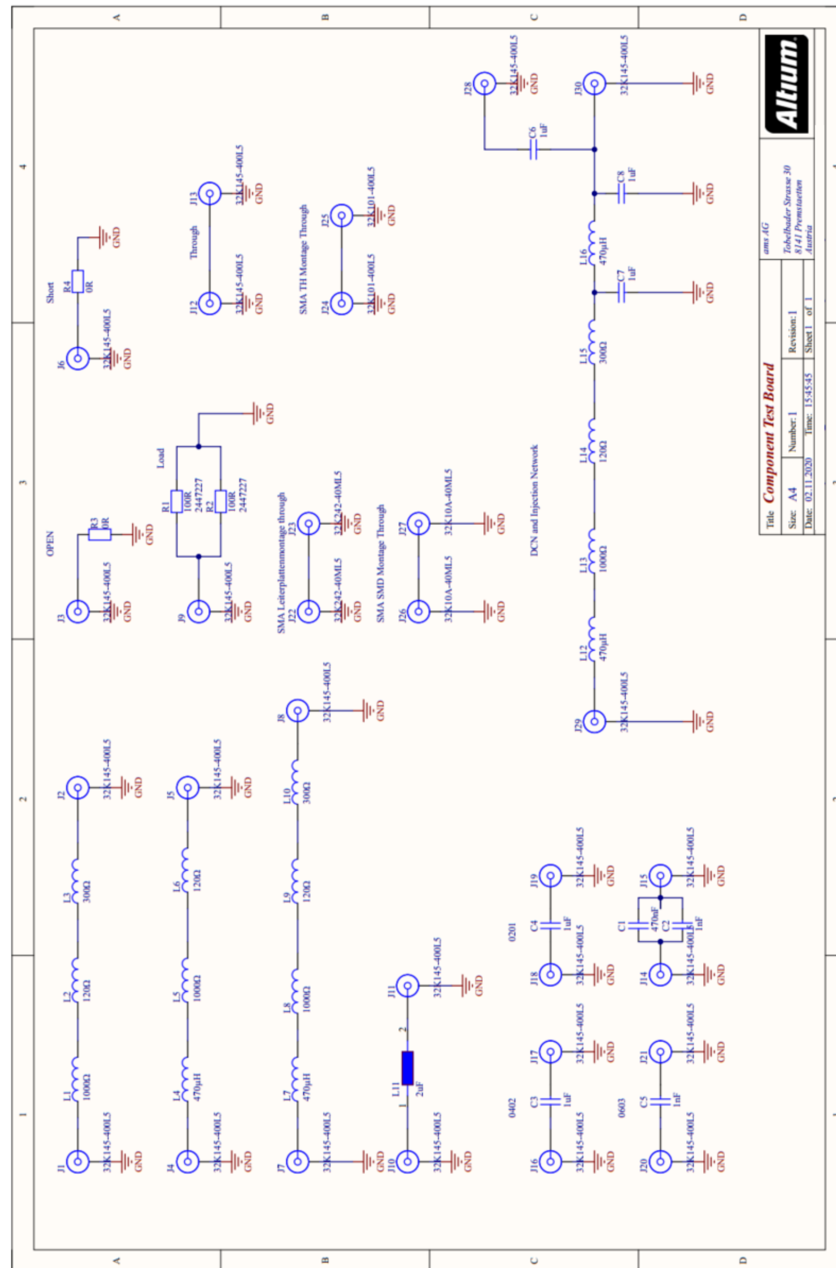


Figure 2.1: Schematic of component test board

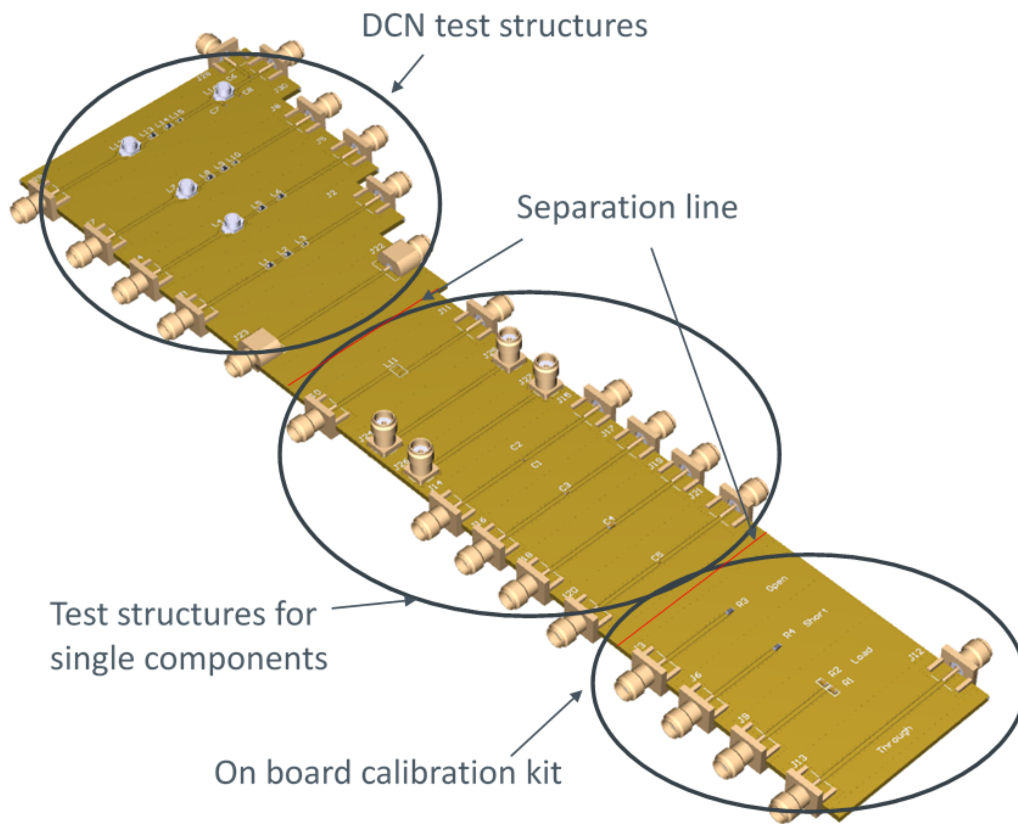


Figure 2.2: 3D Model of component test board

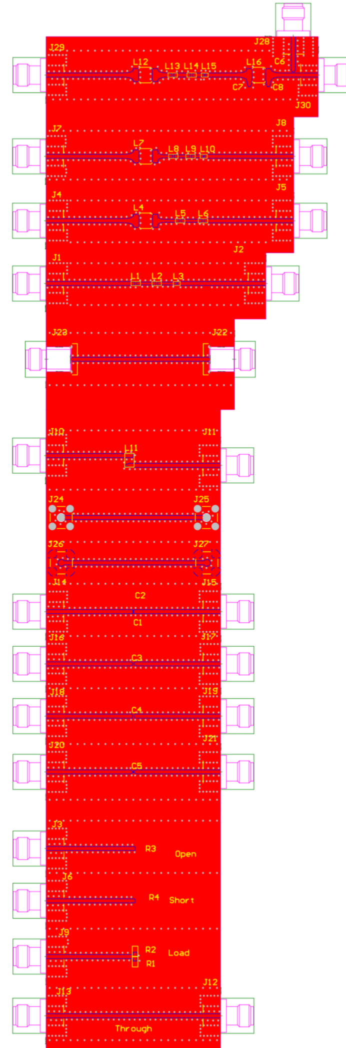


Figure 2.3: Component test Board

standard allows to measure at the pins of different devices and guaranties to get their behaviour without parasitics.

- OPEN:

From SMA connector over 25.5 mm transmission line to an open end.

- SHORT:

From SMA connector over 25.5 mm transmission line to a short to ground.

- LOAD:

From SMA connector over 25.5 mm transmission line to two 100 Ω resistors to ground. (Two 100 Ω resistors to get better 50 Ω result)

- THROUGH:

From SMA connector over 50 mm transmission line to a SMA connector.

The basics of this calibration method can be read in the book *Grundlagen der vektoriellen Netzwerkanalyse* [5] in chapter 3.3.3 $Streifenleitungs$ $Kalibrierstandards$.

2.1.2 S-Parameters of components and setups of components

As described in the standard IEC-62132-1 [7] the DC power supply has to be protected by an impedance of 400 Ω over the whole frequency range from 150 kHz to 6 GHz. For this reason different components are examined on their frequency behaviour. In the coming chapters and sections simulations were done to see which parts come into question (See chapter 3 section 3.1).

An inductor ($ATC506WLSM2R00KT277T$) from American-Technical-Ceramics mentioned in [8] is chosen to be the first test subject. It is soldered onto the component test board and after the calibration of port 1 and 2 of the VNA with the on board calibration kit, the S-parameters are measured. The full frequency range of the VNA is used for this measurements. The S-parameters of the measurement can be observed in figure 2.4. $S11$ and $S22$

showing the measured reflection of port 1 and 2 and $S12$ and $S21$ shows the measured attenuation from port 1 to port 2 and vice versa. To get the impedance of this part, some post processing must be done. Calculation of the impedance is possible in different ways. For this thesis the measured S-parameters are saved as a touchstone file and loaded into a spice simulation program. More specific the data is loaded into a schematic element (NPORT see at chapter 3 section 3.2) which recreates the behaviour of the real world component. The schematic of this simulation test bench is shown in figure 2.5. There is an AC-source with a 50 Ω resistor in series to the NPORT element and in series to this element is also a 50 Ω resistor to terminate it correctly. The resistors are necessary to provide the 50 Ω system in which the S-parameters are also measured. The AC-Source is swept from 100 kHz to 6 GHz and the impedance is then calculated with equation 2.1

$$Z(f) = \frac{(V_{out} - V_{in})}{I_{R0}} \tag{2.1}$$

At frequencies higher than 35.237 MHz the impedance of this special coil is above 400 Ω.

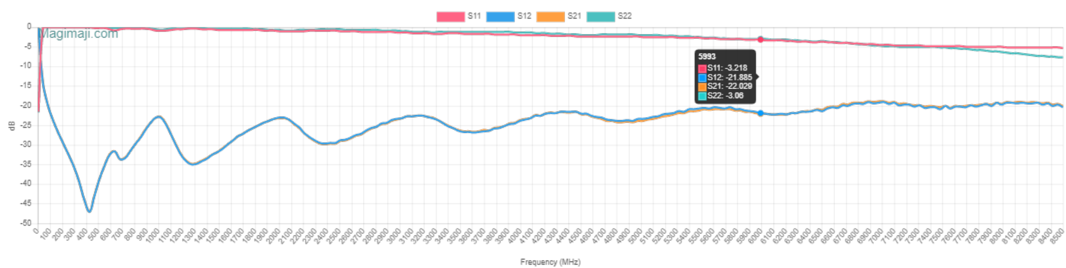


Figure 2.4: S-Parameters $ATC506WLSM2R00KT277T$

Analogous to this procedure, other components were also examined. The next component is a ferrite from Wuerth Electronics (Article number: 74269244182). The S-parameters of this component are shown in figure 2.7. To get the impedance the same test bench as for the inductor is used (figure 2.5). The only difference is that the S-parameters of the ferrite are used. Figure 2.8 shows the impedance of the ferrite. Above a frequency of 9.7949MHz the impedance is higher than 400Ω.

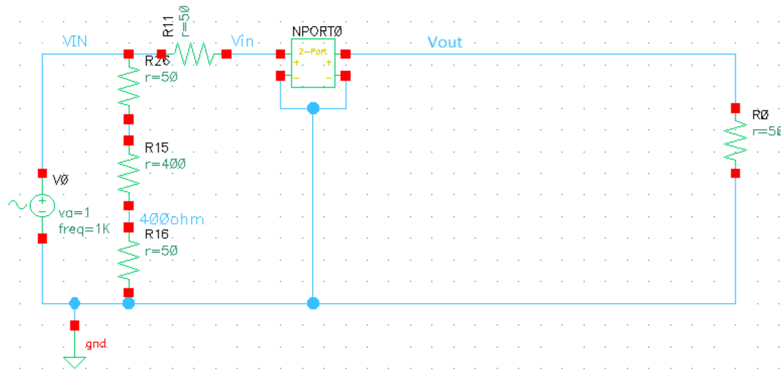


Figure 2.5: S-Parameters to impedance test bench

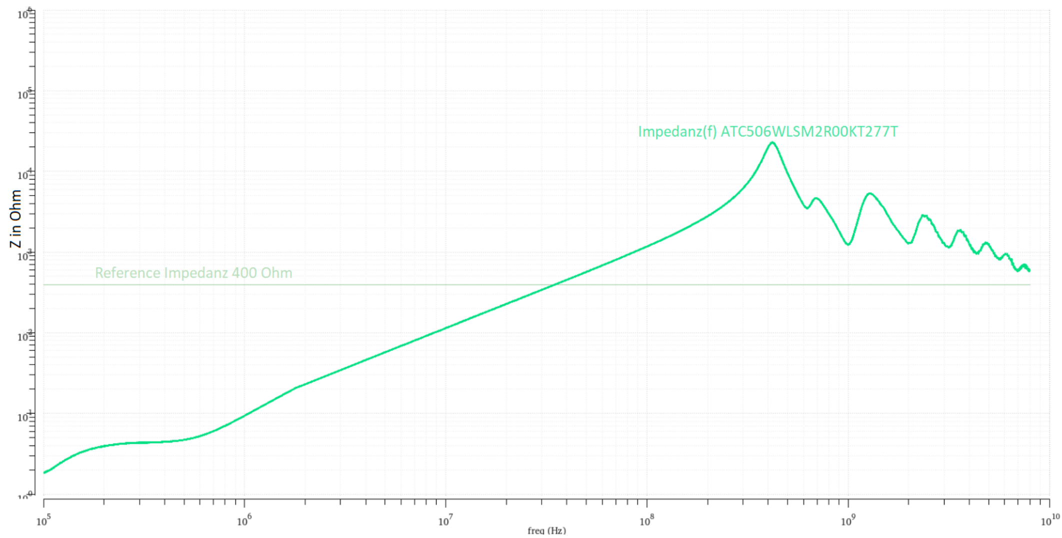


Figure 2.6: Impedance *ATC506WLSM2R00KT277T*

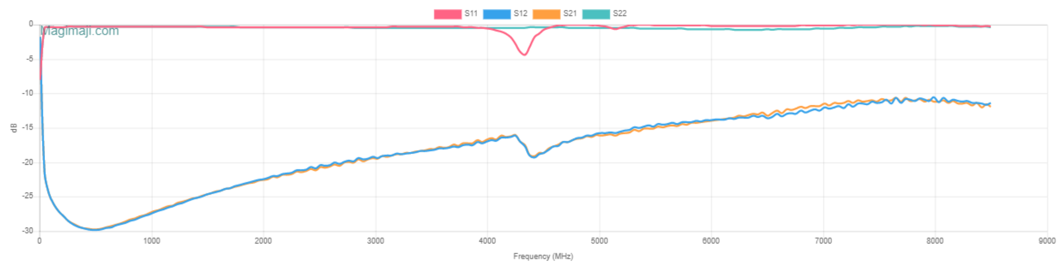


Figure 2.7: S-Parameters Wuerth Ferrite 74269244182

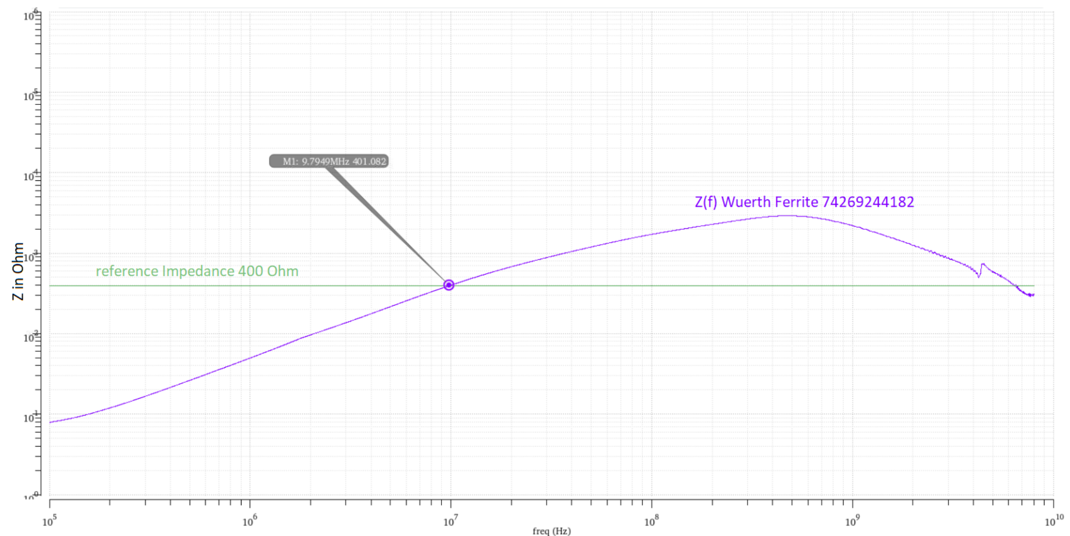


Figure 2.8: Impedance Wuerth Ferrite 74269244182

At DPI measurements at ams before this thesis a DCN that was measured up to 1 GHz was used. This previous DCN has an inductor in series with two ferrites also in series. The inductor from Wuerth Electronics (Article number 74451247) is high resistive in the lower frequency region. In series with the ferrite 74269244182 and the already known inductor 74451247 a better new DCN is formed. With the same measurement and post processing procedure as before, an impedance over 400 Ω in the required frequency region is obtained (see figure 2.9). As a comparison the previous DCN is also measured and calculated as shown in figure 2.10 where Z_L1+Ferrite is the new DCN and Z_L1+L2+L3 is the previous DCN (see table 2.1). The previous DCN fits also the requirements of the DPI Method but has a lower impedance at higher frequencies. The simulation data of the previous DCN shows a worse impedance behaviour with an impedance less than 400 Ω above 1 GHz (see in chapter 3).

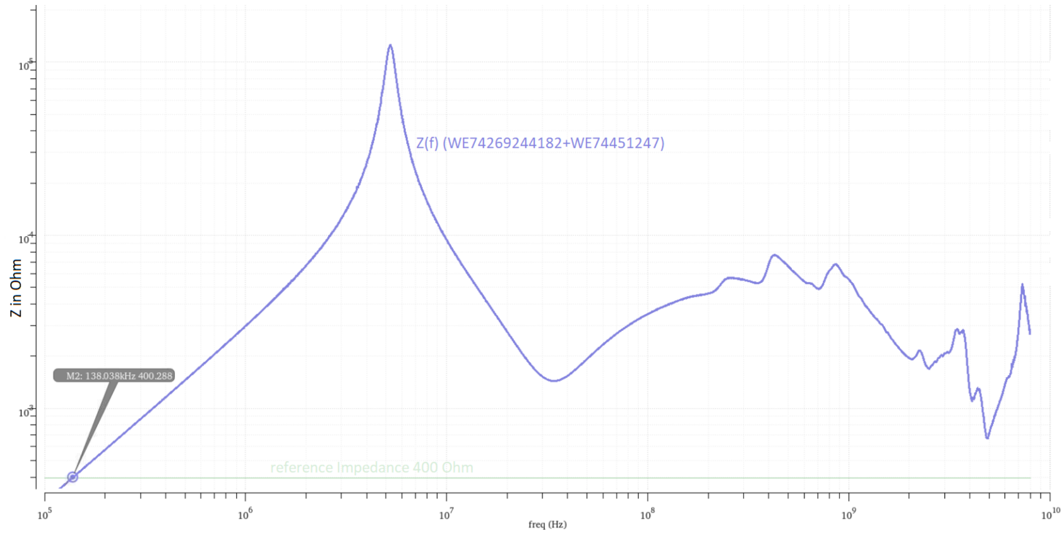


Figure 2.9: Impedance of Wuerth ferrite 74269244182 in series with Wuerth inductor 74451247

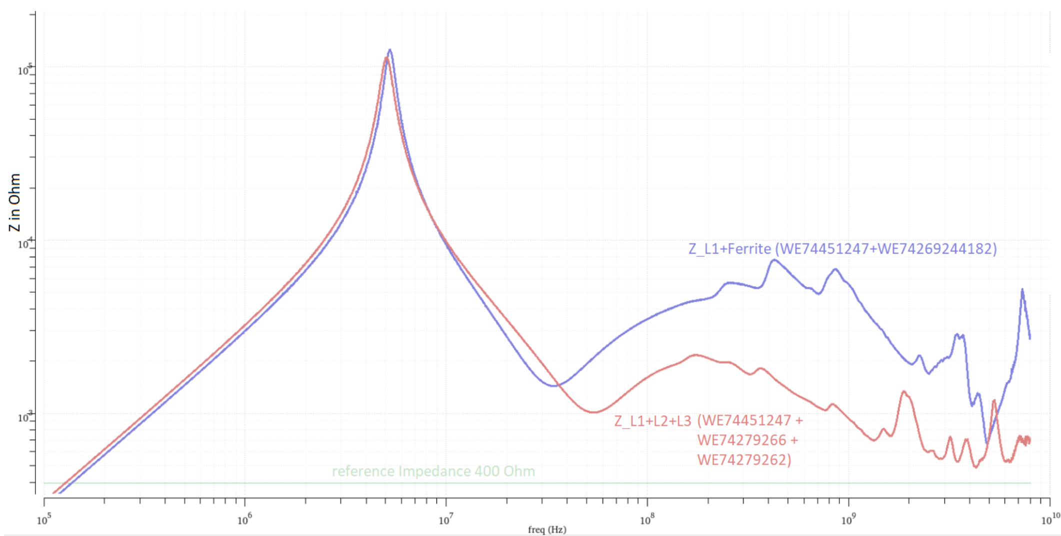


Figure 2.10: Impedance of previous DCN (Z_L1+Ferrite) vs New DCN (Z_L1+L2+L3)

	previous DCN	newDCN
impedance name	Z_L1+L2+L3	Z_L1+Ferrite
components used	WE74451247, WE74279266, WE74279262	WE74451247, WE74269244182

Table 2.1: DCN

The injection network consists of of the DCN which decouples the DC-supply voltage from the interference signal with a DC block capacitor. A special broad-band capacitor from Murata Electronics (935151723510) is used as a DC-block, it distributes the RF interference signal to the pin under test and protects the output of the signal source from DC currents. The advantage of this capacitor is seen in its S-parameters. There is nearly zero attenuation and very little reflection at the frequencies of interest (see figure 2.11). That means that RF-signals have nearly no resistance over the capacitor but DC signals can not pass.

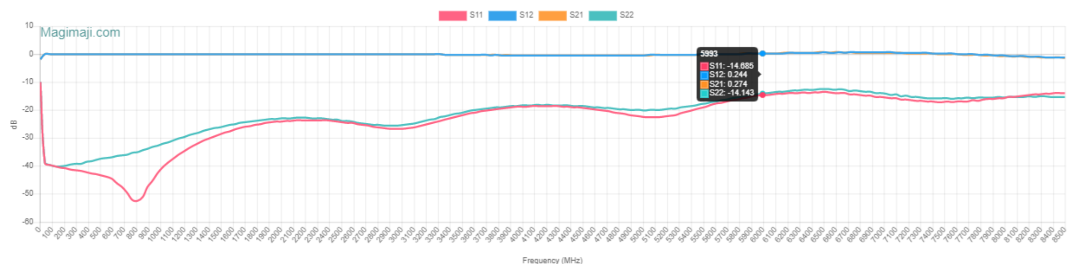


Figure 2.11: S-Parameters broadband capacitor

2.2 DPI - Board

2.2.1 Layout and design

With the knowledge gained from section 2.1.2 the DPI board is designed. The challenge of this design is to distribute the interference signal to the device under test (DUT) without much losses. For this reason the shape of the PCB is chosen to be an octagon see figure 2.12. The schematic of the DPI - Board can be observed in figure 2.13. The band gap reference has the following pins: VDDA, VSSA, VREF, BG_DNPS. The "other Pins" pin symbolises all other not used pins of the test chip. For this thesis only the VDD pin is loaded with an interference signal. VSSA aswell as "other Pins" are connected to ground. BG_DNPS is the connection to the guard ring of the band gap and is connected to the supply voltage VCC over a DCN to protect the supply from unwanted RF disturbance. The output VREF is connected over a $0\,\Omega$ resistor to a SMA connector.

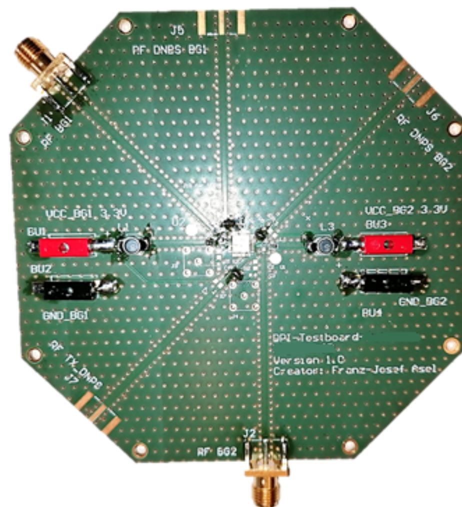


Figure 2.12: DPI-test board

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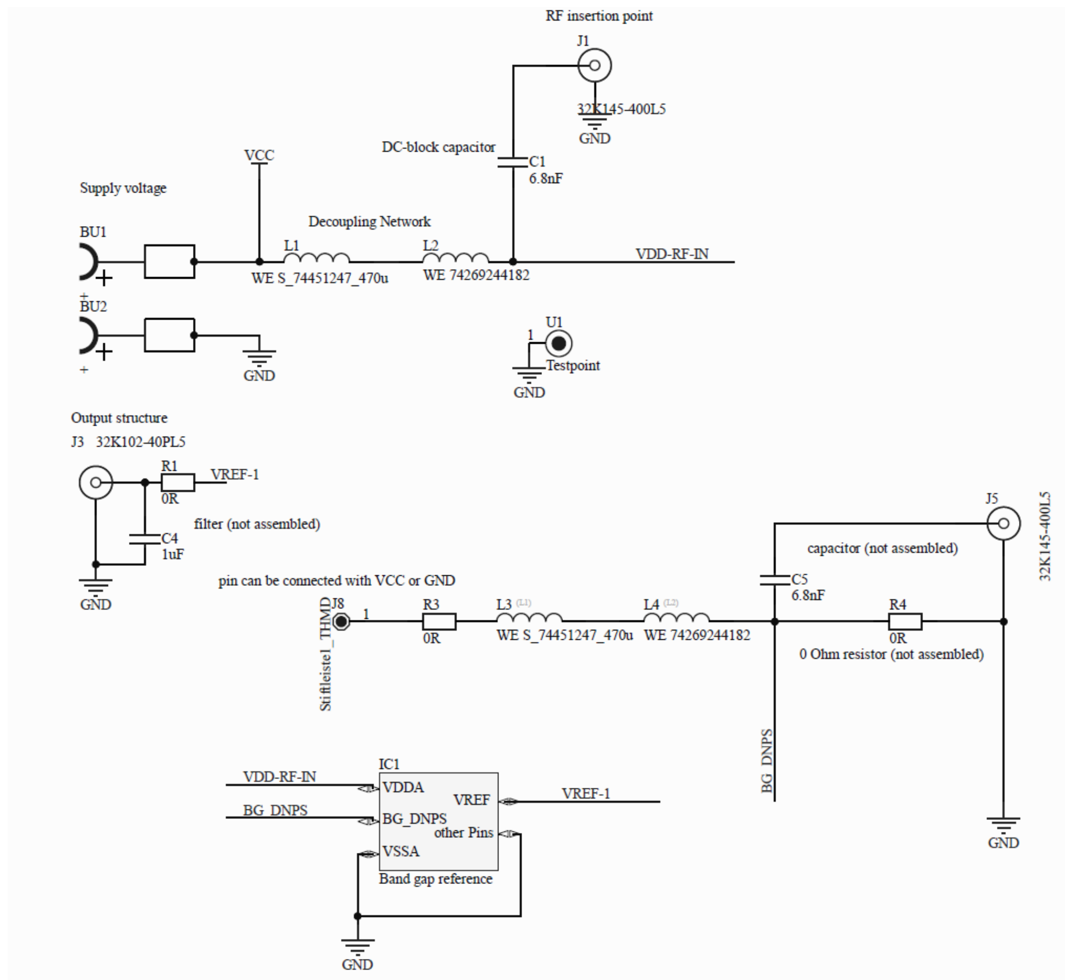

Figure 2.13: Schematic of DPI-test board

2.2.2 Measurement

The theory of the measurement is described in chapter 1 section 1.3. An amplifier is required for measurements between 150 kHz and 1 GHz as the signal generator cannot supply the required power at frequencies under 2 MHz. For this measurement also an bi directional coupler (BDC) and a power meter is used to read the applied forward power. However, for frequencies above 2 MHz the signal generator is able to drive the required power and can read the forward power by itself. Therefore the second measurement from 2 MHz to 6 GHz is made with the signal generator, but without an additional external amplifier. To obtain comparable results, the measurements are started with a power of 0 dBm and increased by 1 dBm steps until 12 dBm is reached. 12 dBm is the maximum power at which the chip is not permanently damaged. Usually there is an failure criterion which stops the measurement and starts the next frequency, but all data is recorded during this measurement. Later an failure criterion can still be applied. In chapter 4 the results of the measurement and simulation are compared and discussed.

The supply voltage is 3.3 V. The measured output signal is the output of the band gap VREF. The expected waveform of the output signal is a sinusoidal AC voltage with a DC-voltage component. The signal is measured over at least 10 periods with an oscilloscope and the DC-voltage is calculated with the averaging function of this device. The DC- voltage is required to see the DC voltage shift of VREF at all applied RF frequencies and powers.

For measurement results of figure 4.1 and 4.2 an automated measurement program is used. The measurement setting time of this program depends on the external devices communication speed and the used control loop. The time is longer the more external equipment is used like power meters and amplifiers, if just the RF generator and the oscilloscope are used, less devices communicate and no control loop is used and for this reason the measurement is done faster. To speed up the measurement a lower frequency resolution is chosen for measurements with more external equipment.

For verification purposes, the measurements for 10 and 12 dBm are repeated. VREF is loaded with 1 $M\Omega$ and 10 pF to simulate the load of an oscilloscope probe head and to because of the same load model in the simulation. The

Measurement setup name	used devices	output load
1 GHz setup	RF-generator, BDC, amplifier, oscilloscope power meter power supply control program	input impedance of oscilloscope
6 GHz setup	RF-generator, oscilloscope power supply control program	input impedance of oscilloscope
Multimeter setup	RF-generator, multimeter power supply	10 pF in parallel with 1 MΩ and parallel input impedance of multimeter

Table 2.2: Measurement setups

DC voltage is measured with a multimeter Agilent U1232A that has an input impedance of 11.18 $M\Omega$. To protect the multimeter from RF-disturbances a bias tee is switched between output of the Band gap and input of the multimeter. Bias tees are three port network devices. The internal circuit is similar to the injection network described in figure 1.5. It has an DC-port which is protected from RF-signals an RF-port protected from DC signals and a RF and DC port. The measurement is done at the DC-port and output of the band gap is connected to the RF and DC port, the RF port is not connected. The measurement is performed in 10 uniform frequency steps per decade from 1 MHz to 6 GHz. This measurement is done manually.

The different setups are explained in table 2.2.

In figure 2.14 you can see the measurement setup for 2 MHz to 6 GHz. For the measurement from 150 kHz to 1 GHz the amplifier and the BDC are used as described in figure 1.1.

To be sure that the board fits all requirements of the IEC $62132 - 1$ [7] standard a measurement of the transfer function of one of the transmission lines is done. All the other transmission lines are equal in length and are considered to behave in the same way. All parts are assembled on the DPI-board except the test chip. The measurement set-up is shown schematically

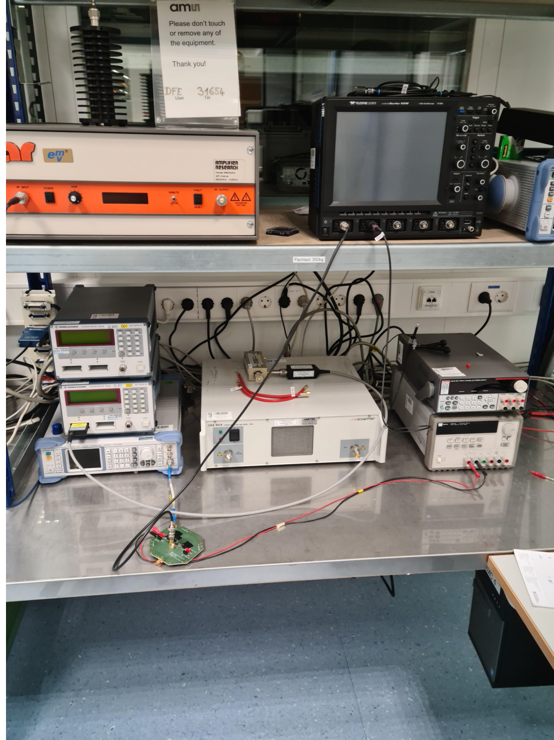

Figure 2.14: Measurement setup for 2 MHz to 6 GHz

in figure 2.15. The VNA is calibrated with two calibration kits, port 1 for SMA connectors and port 2 for ground-signal pico probe with a pitch of 900 μ. Calibration kit for port 1: ZV-Z135 and for port 2 with the pico probe from GBB Industries INC.: CS11. The unknown through is done near the SMA connector with cut up transmission line to prevent reflections (see in figure 2.16). The whole setup can be observed in figure 2.17. The result of this measurement can be observed in figure 2.18. The attenuation is not under the $-3\ dB$ limit of the standard and and thus the PCB is suitable for further measurements.

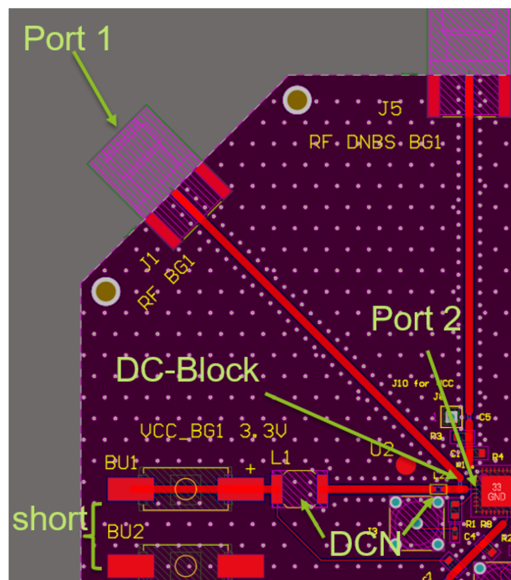

Figure 2.15: Schematically measurement setup for transmission function

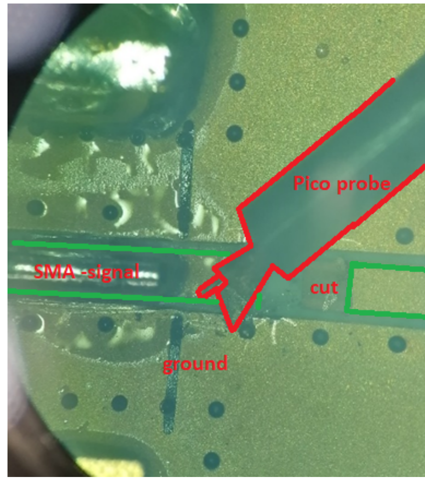

Figure 2.16: Calibration unknown through

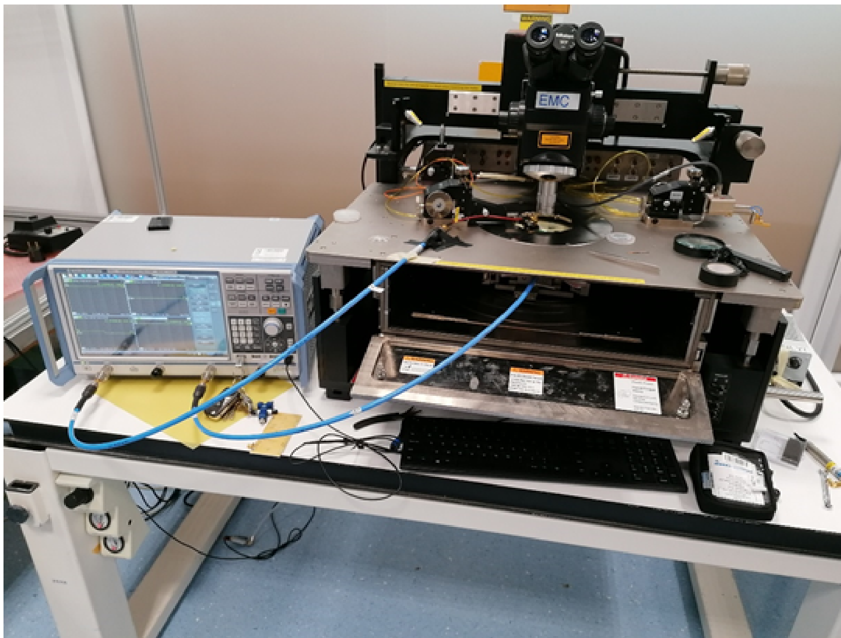

Figure 2.17: measurement setup for transmission function

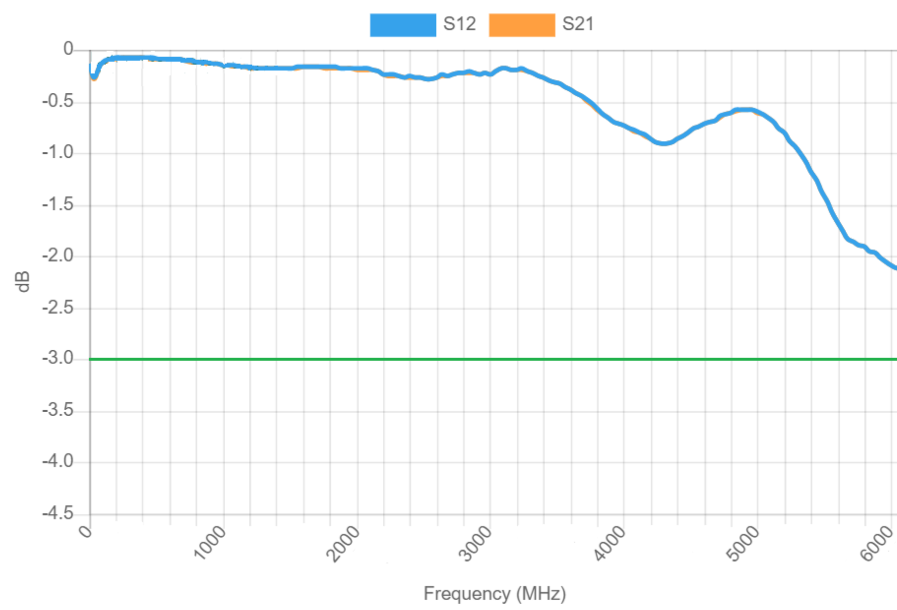

Figure 2.18: Transmission function of 50 Ω transmission line

3 Modelling and simulation

For modeling the DPI method the spice program named "Cadence virtuoso assembler" is used. In this spice model the DCN and a parasitic extraction of the test - chip is implemented. For the output, the input impedance model of an oscilloscope is used.

3.1 DCN

To get knowledge about characteristic impedance of ferrites, inductors and capacitors a component test board is constructed (see chapter 2 section 2.1). But the question is which components to be used. Luckily manufacturers provide spice models of their components. First the previous DCN components are simulated. The schematic can be observed in figure 3.1 and with the simulated voltages and currents the impedance of this DCN is calculated with equation 2.1. The result of this simulation is shown in figure 3.2. Each components impedance is shown and also the impedances of the components connected in series. The series impedance Z_{ges} is lower than 400 Ω at 30 MHz to 45 MHz and at frequencies higher than 1 GHz. This behaviour is not equivalent to the measuring result shown in figure 2.10. The explanation is that this spice models are just valid for one predefined frequency and only an approximation of the remaining impedance behaviour. The reason why no S-parameters are used is simple, those are not supplied by the manufacturer for all components. This simulation is done before the measurement of the previous DCN and for this reason a DCN is made which fits the requirement of the DPI method. The component which is searched for shall have a high impedance at higher frequencies. The ferrite from Wuerth 74269244182 has this properties as you can see in figure 3.3 where the impedance of the model of the ferrite and the measured

impedance of the ferrite are shown. Both lines have a similar impedance frequency behaviour, which proves that the model is accurate enough for designing a DCN. In the next step the model of inductor 74451247 and the ferrite 74269244182 is connected in series to get an impedance over 400 Ω. This network is simulated and compared again with its measured values (see figure 3.4). In the simulation a negative resonance peak leads to an impedance under 400 Ω between 30 and 40 MHz, but in the measurement this resonance peak has an much higher impedance over 400 Ω. It could be that the inaccuracies in the models of second order of the components cannot model the exact behaviour of the real circuit.

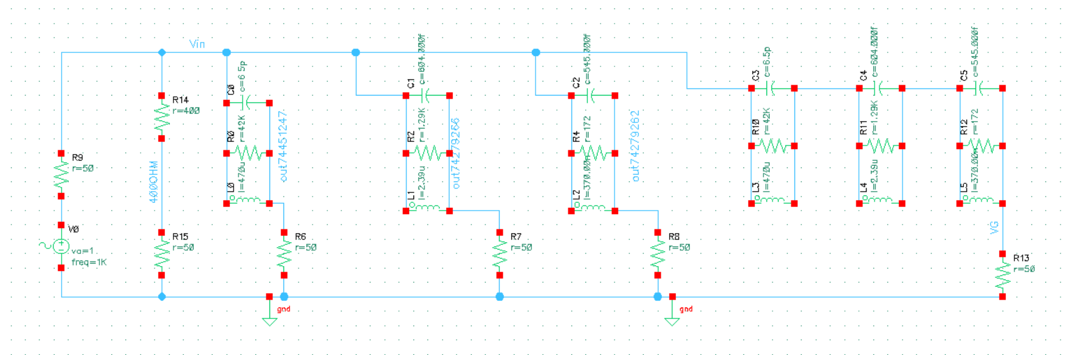

Figure 3.1: Simulation schematic for previous DCN

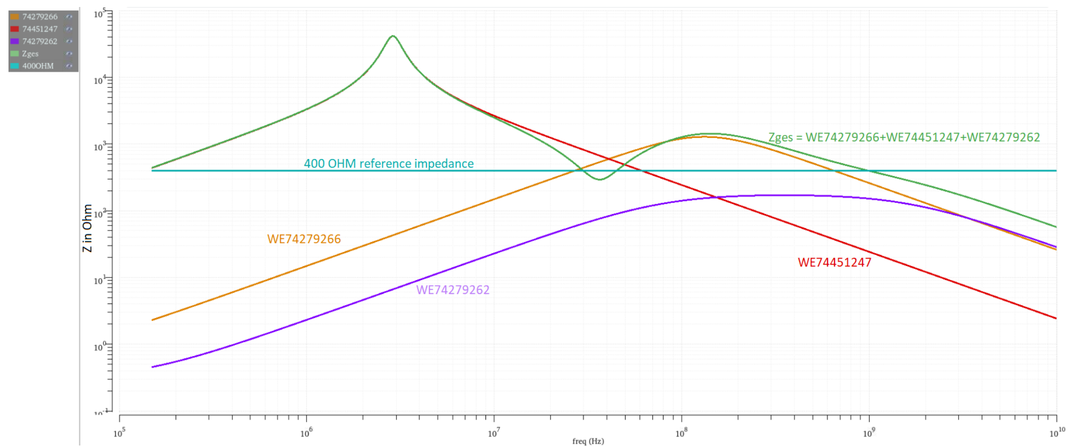

Figure 3.2: Simulation results for previous DCN

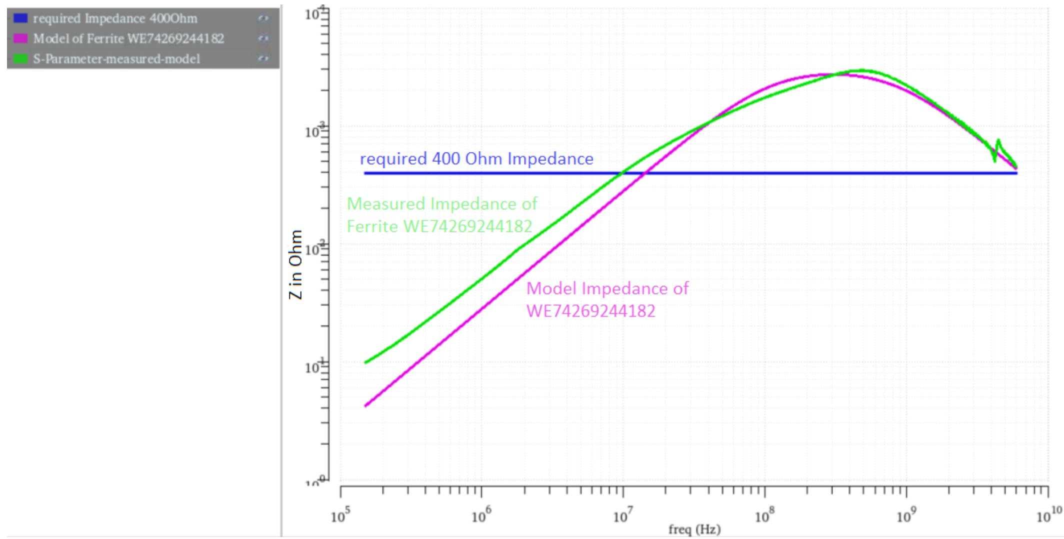

Figure 3.3: Simulation results ferrite 74269244182 model vs measurement

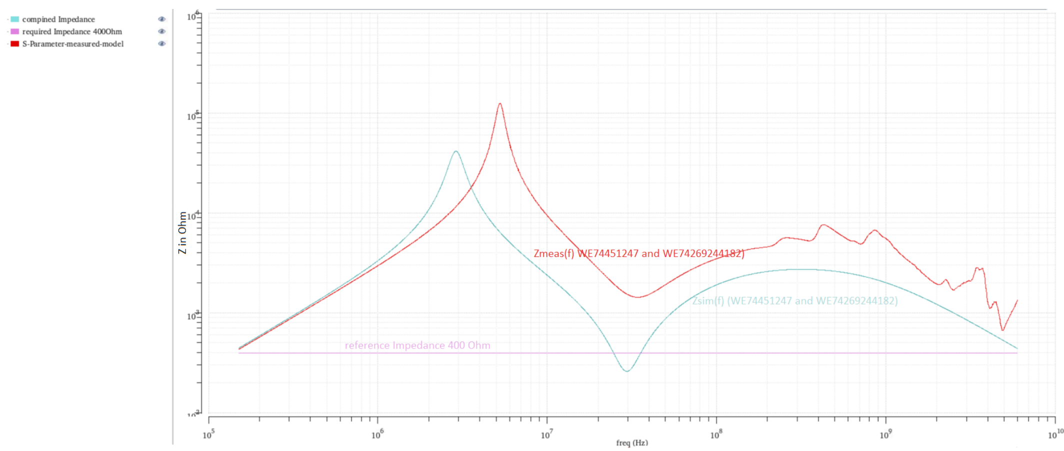

Figure 3.4: Simulation results ferrite 74269244182 and inductor 74451247 model vs measurement

3.2 S-Parameters

The S-Parameters can be obtained by either simulating the spice model of the desired components with a sp analyses or by measuring with a network analyser. To create simulation models including S-parameters, nPORT elements are used. In this element a touchstone file can be loaded and interpolated with different interpolation methods. For this thesis the interpolation method "bbspice broad-band spice" is used. The best explanation is found at cadence community website [3]: *"The bbspice interpolation method generates the S-parameters macro models suitable for transient simulation. bbspice uses rational fitting with passivity and causality enforcement, and stores the generated models for later use."* The presentation *Advanced S-Parameter Modeling with Broadband SPICE Technology* [1] informs over pros and cons of this interpolation method.

3.3 Test chip

To simulate an electromagnetic immunity test, like a DPI method, the test board with all its periphery like the injection network as well as the device under test must be known in one or a other way. That means there must be some kind of model or measurement done to be able to compare data and get results out of them. For this thesis a well known test chip is used. The schematic and layout as well as a physical piece of this test chip is in the company and can be used for experiments.

3.4 Parasitic extraction

The test chip consists of various independent blocks, where here in this work only the band gap block is used as verification of the model and for simulation. This simple band gap circuit is just a small part of the chip, but it is perfect for this simulation and verification usage. Nevertheless in order to obtain a more accurate model than just the schematic, a parasitic extraction is performed to get the behaviour of parasitic elements in combination with

the circuit. In this process the resistive and capacitive parasitic elements introduced through drawing the layout are calculated and added to the schematic model of the chip. There are several other types of extraction like just resistive, or just capacitive, or even inductive extraction combined with resistive and capacitive extraction and crosstalk extraction. The drawback of this approach is that the model gets more complex the more schematic elements and layout elements like guard rings are in the chip. This results in a longer simulation time than without any parasitics. So just a RC Extraction is done for this thesis. To extract the parasitics from the layout two tools in cadence Virtuoso Layout Suite L called Assura and Quantus are needed. First a layout versus schematic (LVS) check by Assura is done and then the extraction is done by Quantus.

3.5 Testbench

3.5.1 Schematic

The schematic is composed of the test chip with the parasitic extraction data included, nPORT elements which are loaded with measured S-parameters of the DCN and the DC-block capacitor, a PORT cell which is the RF-source, DC source and a simple load model which simulates the input of an oscilloscope. The port cell is used for the unique output power adjustment feature, which simplifies the simulation setup. All pins of the chip which are not used are connected to ground. The schematic can be observed in figure 3.5.

3.5.2 Simulation settings

As the first step a DC-analysis is done do see if under undisturbed conditions the simulation creates the same output voltage as the measured pendant. In the next step a transient analyses is chosen. The accuracy of the analyses is set to ”liberal”, this means the analyses is fast but less accurate. This balancing is done to speed up the large number of computationally intensive

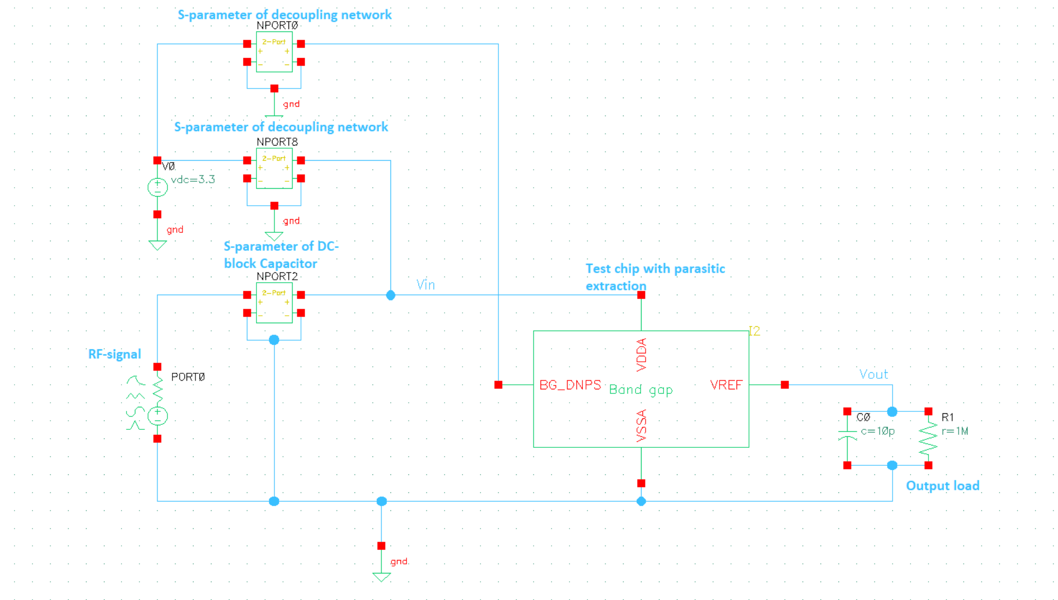

Figure 3.5: Schematic of the test bench

simulations. After a settling time of at least 12 μs the signal reaches a voltage level near the the settled voltage. In the next step the average over at least 10 periods of the output signal is taken by the program to see the DC voltage shift under disturbed conditions. For lower frequencies the settling time is longer because of the longer periods. The period T is calculated with equation 3.1, where f is the frequency. For a frequency of 150 kHz T equals 6.666 μs, so after a settling time of 35 μs the output signal is saved and the average is calculated for another 66.6 μs (10 periods). For higher frequencies the settling time is shorter. The frequency is swept in 10 linear steps for a decade beginning from 150 kHz to 1 GHz and the insertion RF-power is swept from 1 dBm to 12 dBm in 1 dBm steps.

$$T = \frac{1}{f} \tag{3.1}$$

3.6 Simulation of PCB with a field solver

The transmission lines of the DPI measurement board are calculated with a field solver program to predict the transmission function in form of the S-parameter S12. Ground vias are inserted to get a better behaviour of this lines. If placed wrong there could be attenuation spikes in the transmission function of the line (see in figure 3.6). If placed in a regular way like in the finished PCB there are no attenuation spikes (see in figure 2.18). (The calculation of this transfer function is done by supervisor Bernhard Weiss and is thankfully provided for this thesis.)

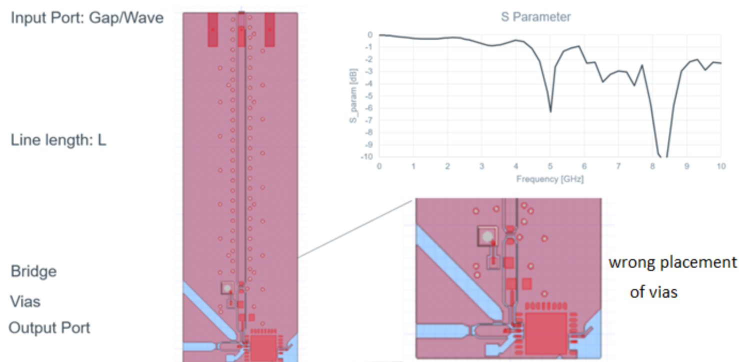

Figure 3.6: Transmission line calculation with field solver

4 Comparison of results

In the following chapter the results of the measurement and simulation will be discussed and compared to each other.

4.1 Results measurements

The measurement setup is discussed at at chapter 3 section 2.2.2. The first measurement is done from 150 *kHz* to 1 *GHz* and can be observed in figure 4.1.

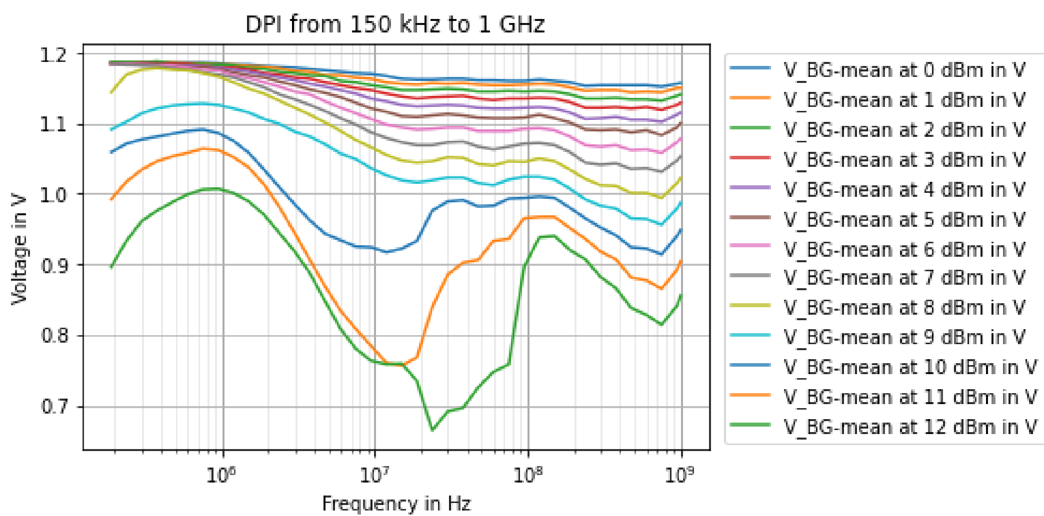

Figure 4.1: Measurement from 150 kHz to 1 GHz

The next measurement is done from 2.5 MHz to 6 GHz. In figure 4.2 it can be seen that at higher input power the output signal of the band gap is declining, but with rising frequency also the output voltage rises again.

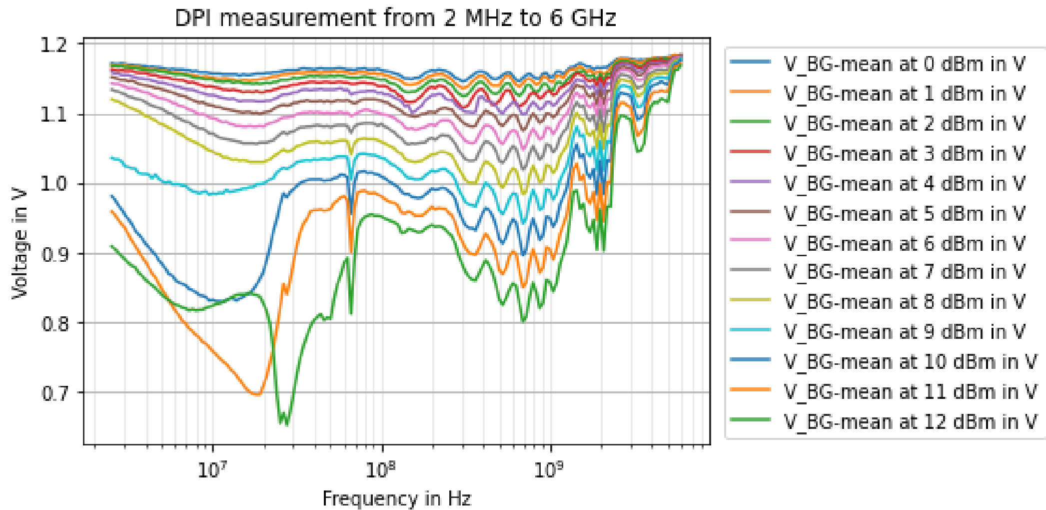

Figure 4.2: Measurement from 2.5 MHz to 6 GHz

To have a comparison between this measurements, selected curves are superimposed. Figure 4.3 and figure 4.4 are showing that there are some differences due to the higher frequency resolution and a different measurement setups. For this reason a $3rd$ measurement is done with the same frequency generator but with an 10 pF capacitor and a 1 $M\Omega$ resistor as load at band gap output parallel to ground. This load simulates the input impedance of the used oscilloscope of the previous measurement setup to get the same behaviour of the circuit. A bias tee is put in series between multimeter and output to protect the input of the multimeter from RF-disturbances. The results of this measurement can be observed in Figure 4.5 where the two measurements from above are also superimposed.

The negative spike in figure 4.5 at 3 MHz of the band gap voltage measured with a multimeter is a result of a resonance between the band gap, the output capacitance of the DPI board and the input capacitance of the measuring device. The shift of the resonance peak towards higher frequencies can be observed clearly in figure 4.6 between the multimeter measurement

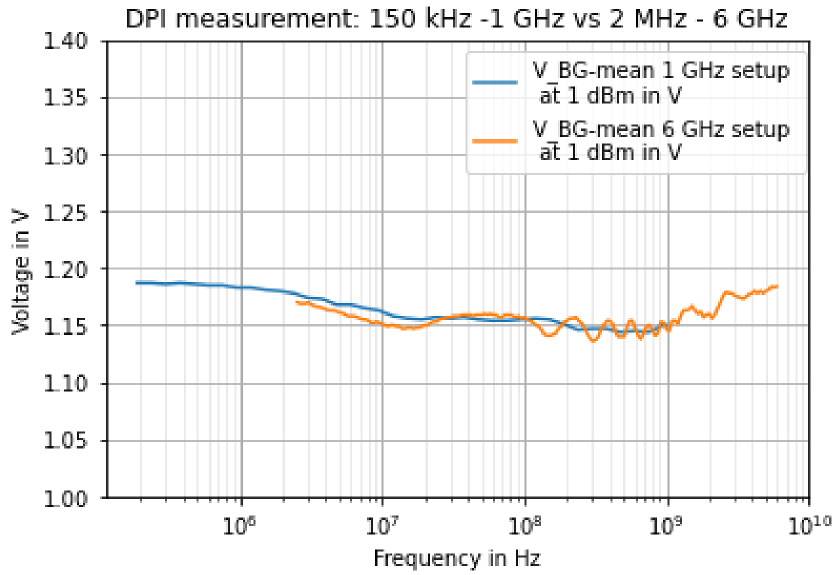

Figure 4.3: DPI measurement: 150 kHz to 1 GHz vs 2.5 MHz to 6 GHz at 1 dBm insertion power

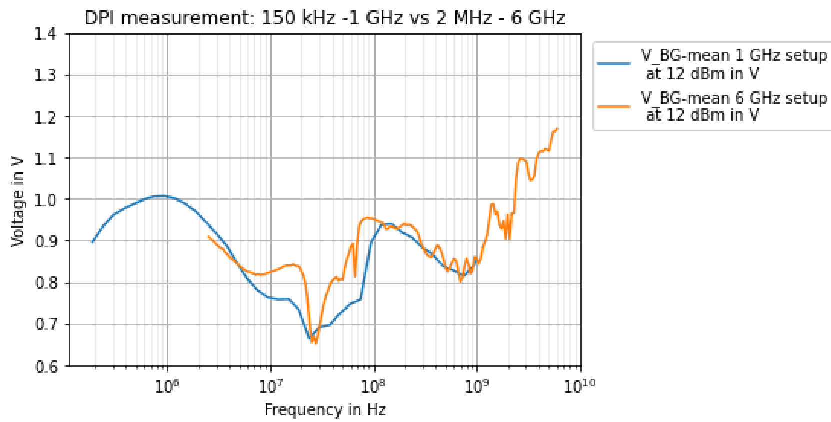

Figure 4.4: DPI measurement: 150 kHz to 1 GHz vs 2.5 MHz to 6 GHz at 12 dBm insertion power

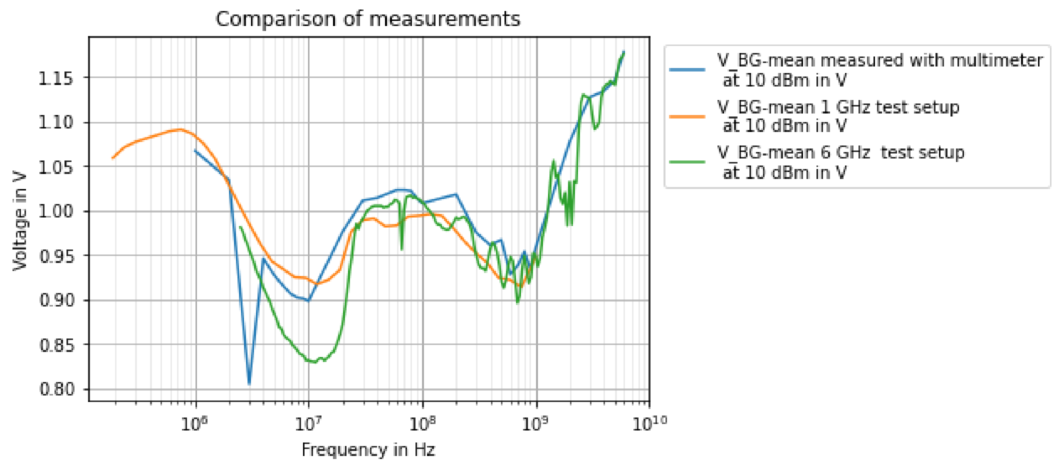

Figure 4.5: Comparison of measurements at 10 dBm

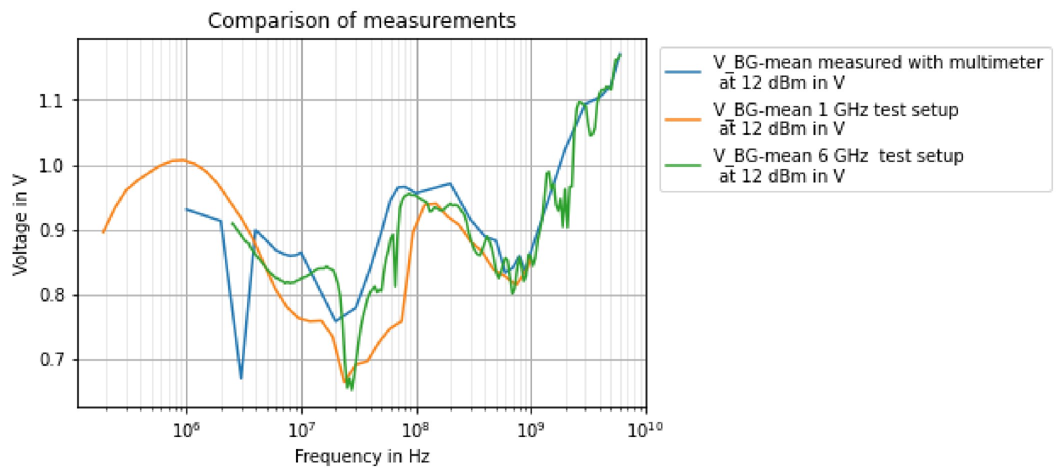

Figure 4.6: Comparison of measurements at 12 dBm

and the high resolution 6 GHz test setup measurement. This means that there is at each measurement a slightly different load impedance. All those measurements are valid, but for comparison reasons only the automated measurements are taken into account because more measurements are done and data processing for this measurements is much easier.

4.2 Results simulation

The test bench and simulation settings can be found in chapter 3 section 3.5. The results can be observed in figure 4.7. At the higher frequencies the simulation program throws simulation errors due to the sheer amount of data. For example if a calculation step is $10ps$ long for a 6 GHz signal, the computation of 10 μs has 1000000 calculation steps alone for the computing of the settling time of the curve, but there are at each calculation step other calculations like interpolations and memory operations are done. The computation time for this model of a voltage point at 6 GHz lasts over 12h. The curves tend to behave the same way for DPI-levels up to 9 dBm, for higher DPI-levels the curves differ from the tendency in having a much lower output voltage and greater spikes than the previous simulations. The comparison between measurement and simulation will be done in the next section. At high frequencies the curves tend to the DC-Voltage of 1.2 V.

4.3 Comparison

4.3.1 Comparison of DPI-simulation and DPI-measurement

In this section the measurement and the simulation will be compared for each DPI-level. As mentioned in section 4.2 are there simulation errors at some plots. The errors occur only at frequencies higher than 1 GHz and have the values of 0.7 V each. The similarity between simulation and measurement can be seen in figures 4.8 to 4.16 at frequencies lower than 100 MHz. At frequencies higher than 100 MHz the simulation curves tend more to the DC output voltage of 1.2 V. The curves with DPI-levels higher than 9

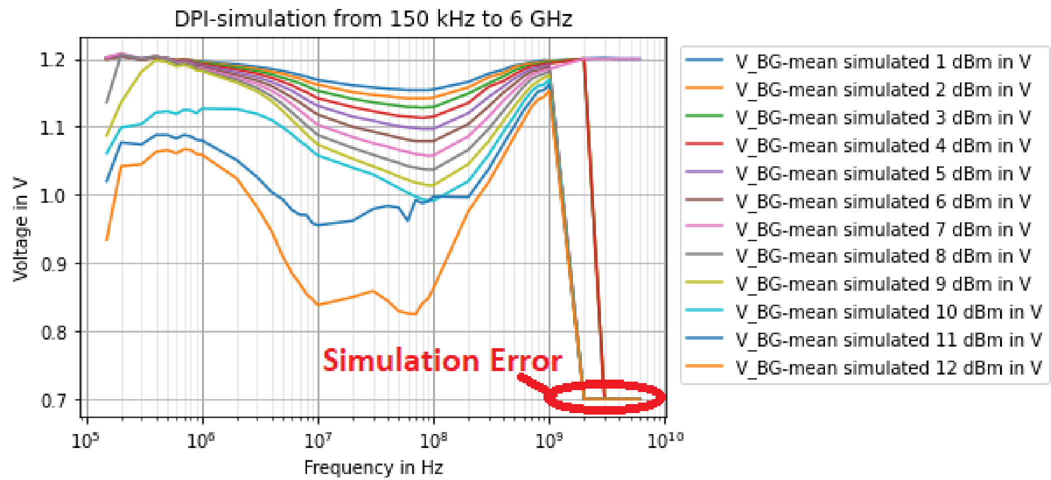

Figure 4.7: Simulation results

dBm differ the most from the measurement with exception of the simulation curve with DPI-level of 12 *dBm* in figure 4.19. This simulation curve behaves similar to the measurement but also oversees the resonance peak between 20 *MHz* and 30 *MHz*. An exact explanation why the simulation does not fit the measurement is not found yet. There are several options like non-linearities in the electro static discharge (ESD) structure of the chip, or some substrate effects that are not modelled by the parasitic extraction, or imprecise models of the transistors in the band gap, or even wrong models which can not be accurate for signals up to 2.5 *V* peak to peak.

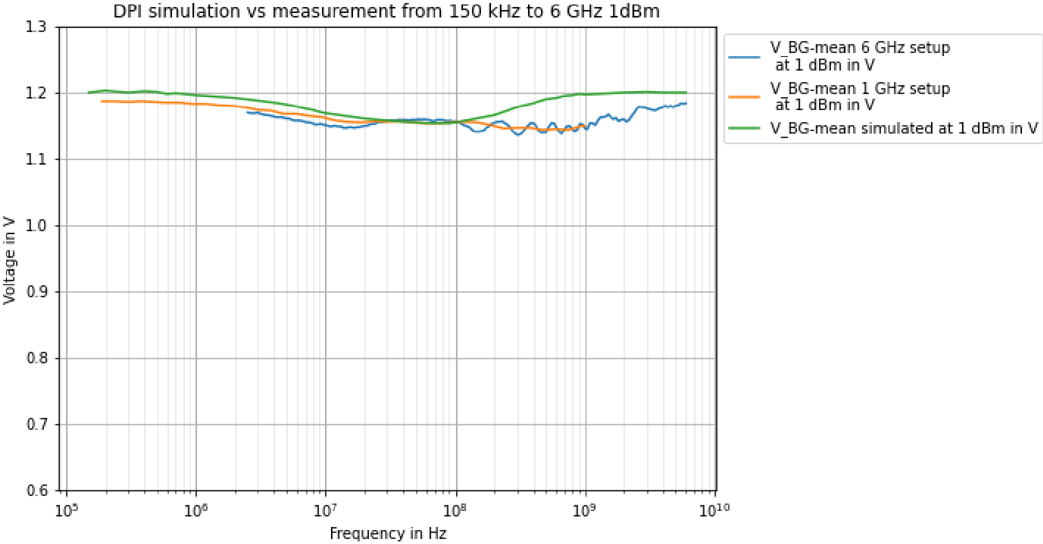

Figure 4.8: DPI-simulation vs DPI measurement at 1 dBm

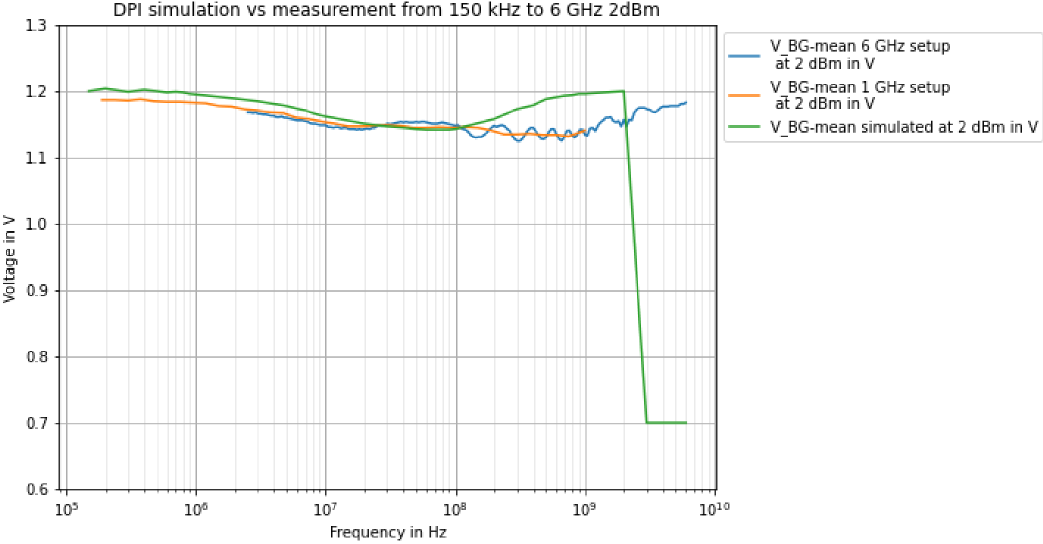

Figure 4.9: DPI-simulation vs DPI measurement at 2 dBm

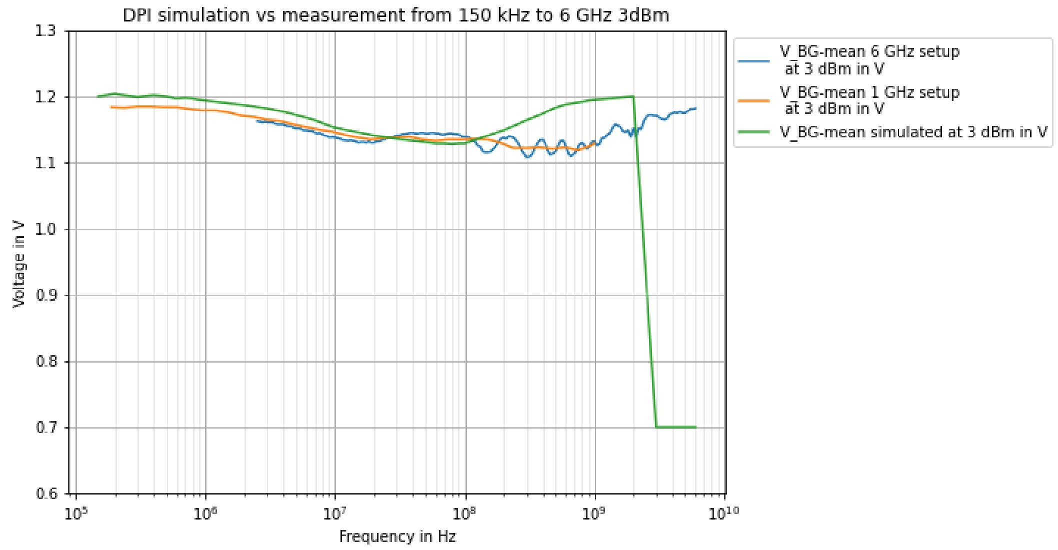

Figure 4.10: DPI-simulation vs DPI measurement at 3 dBm

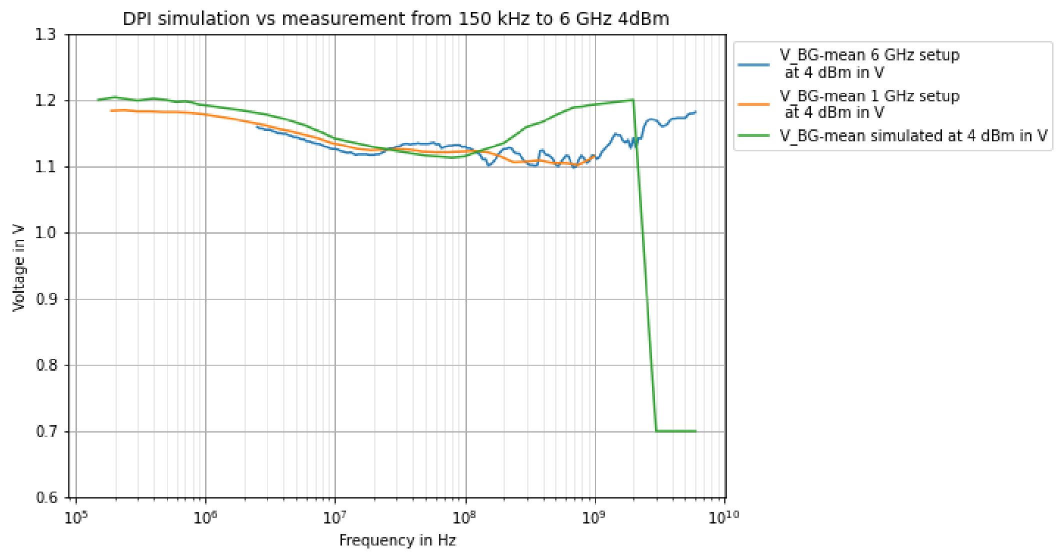

Figure 4.11: DPI-simulation vs DPI measurement at 4 dBm

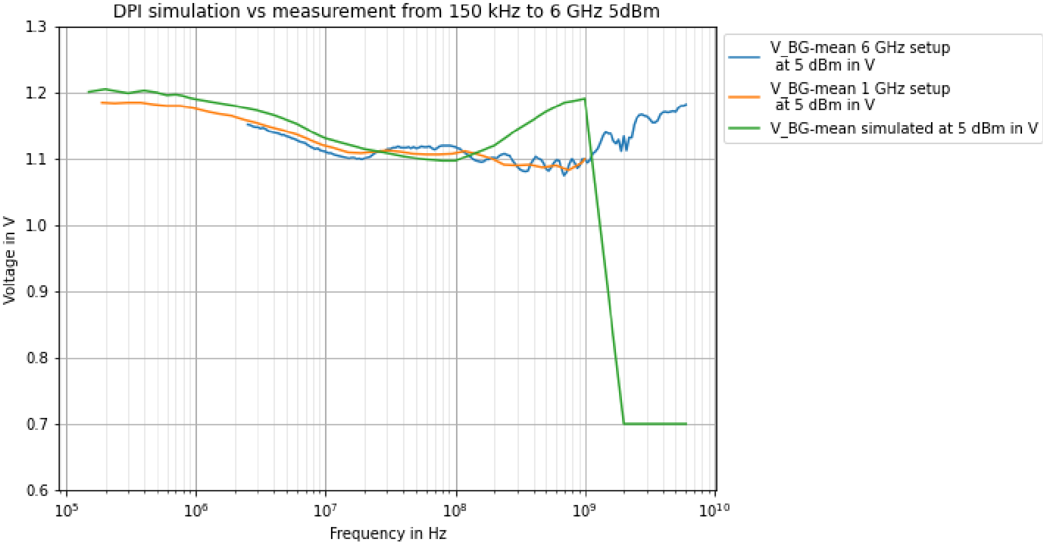

Figure 4.12: DPI-simulation vs DPI measurement at 5 dBm

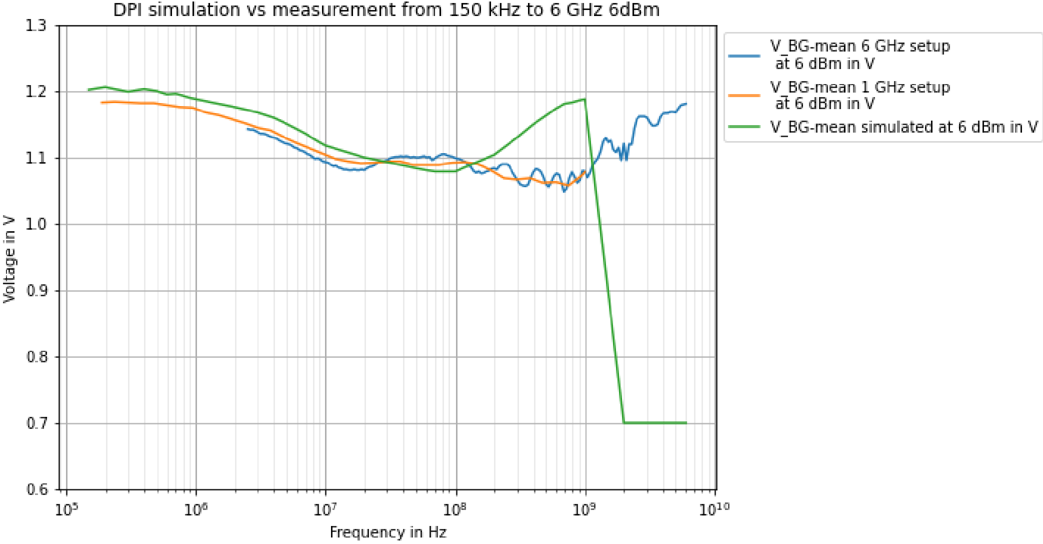

Figure 4.13: DPI-simulation vs DPI measurement at 6 dBm

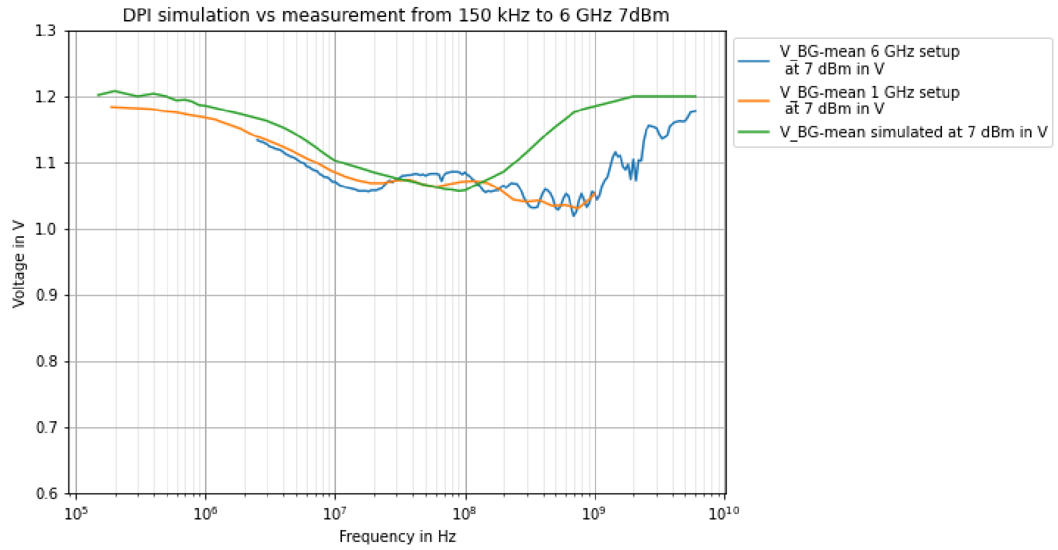

Figure 4.14: DPI-simulation vs DPI measurement at 7 dBm

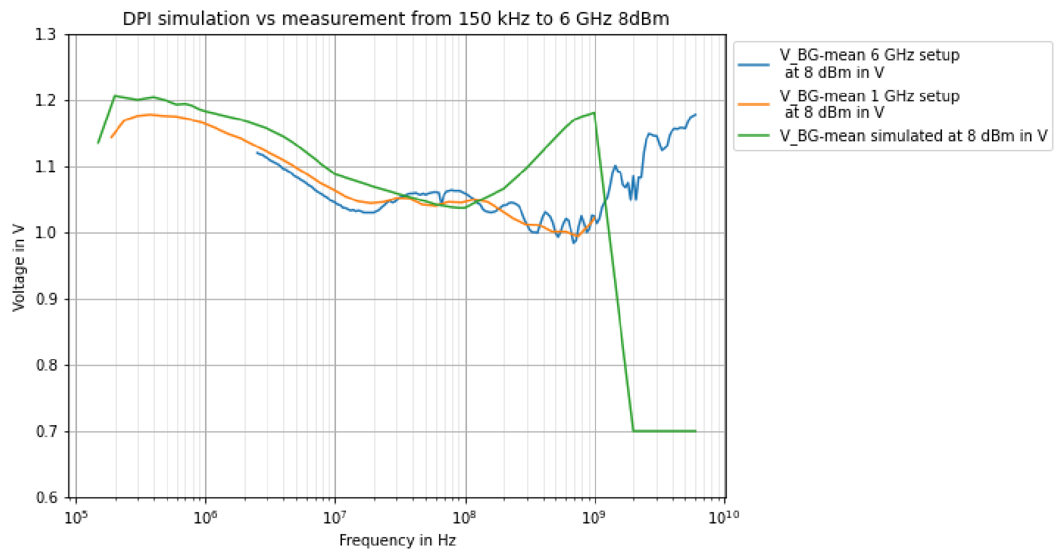

Figure 4.15: DPI-simulation vs DPI measurement at 8 dBm

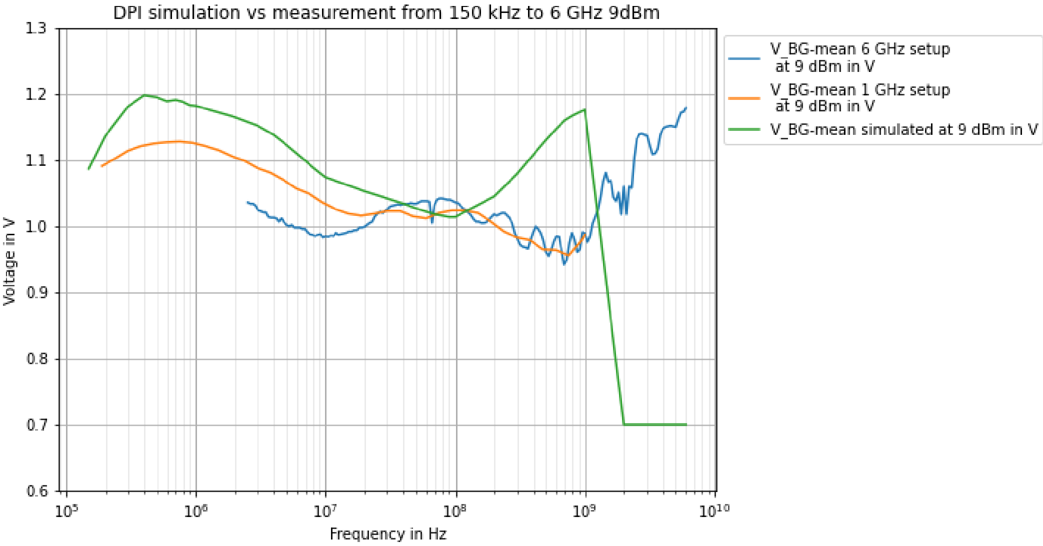

Figure 4.16: DPI-simulation vs DPI measurement at 9 dBm

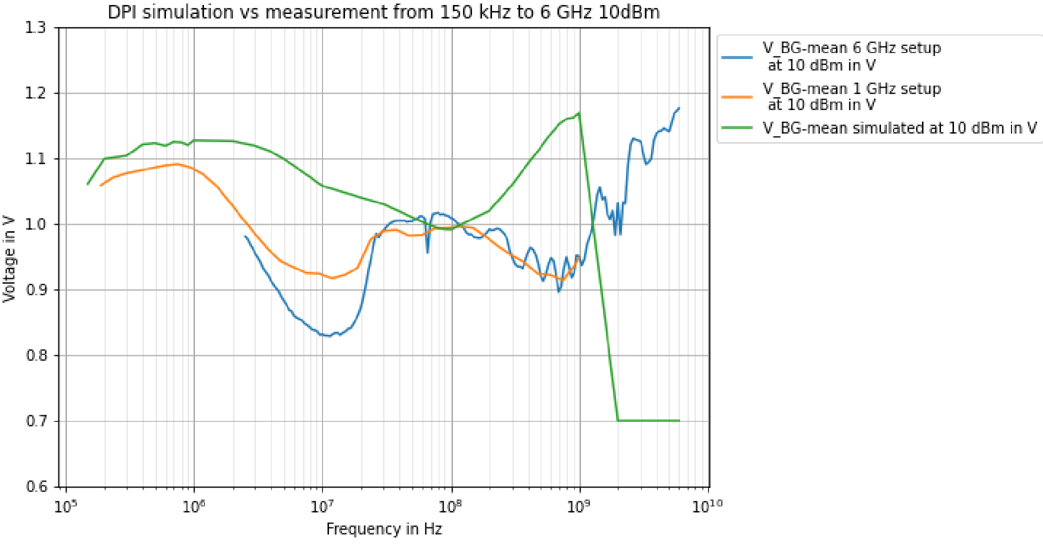

Figure 4.17: DPI-simulation vs DPI measurement at 10 dBm

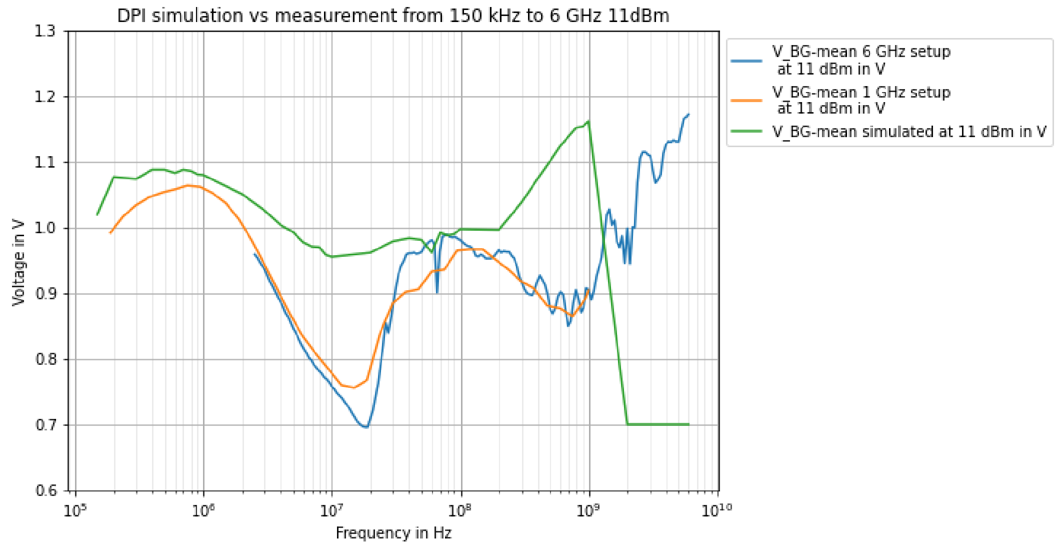

Figure 4.18: DPI-simulation vs DPI measurement at 11 dBm

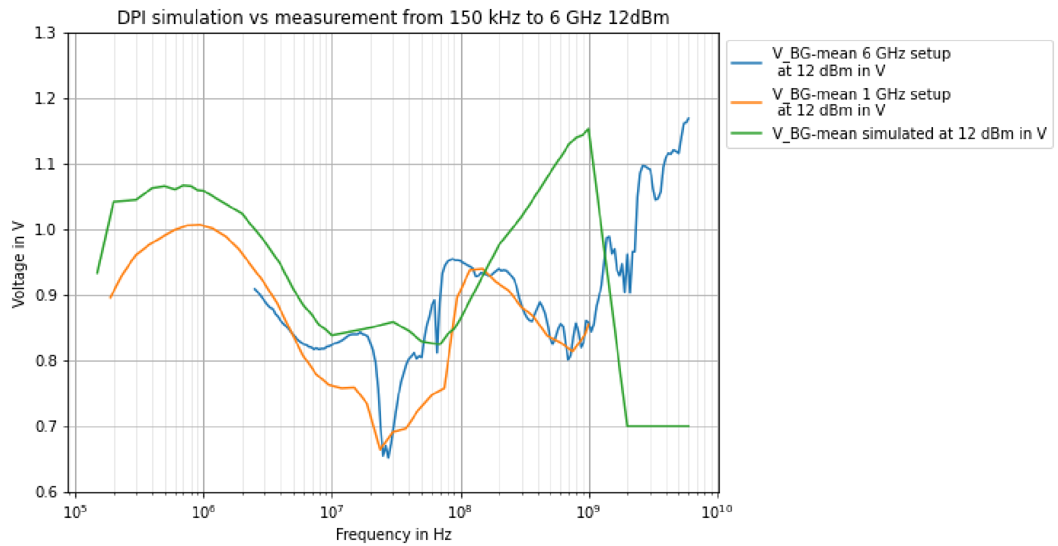

Figure 4.19: DPI-simulation vs DPI measurement at 12 dBm

4.3.2 Comparison of input interference signal measurement and simulation

To verify the previous result, the RF-interference signals are examined. The measurement setup is the same as for the DPI measurement, but now the interference signal is measured with an active probe on the BG_VDD pin of the test chip and at the output of the band gap. Three DPI-levels are examined (10 dBm, 11 dBm and 12 dBm) for two frequencies 10 MHz and 1 GHz. For comparison also the simulation signals are shown in the following figures. There is no phase information between the curves in the following plots. For the measurement at 1 GHz the active probe has an impedance of just 100 Ω, thus the signal is affected with this load. At 10 MHz the probe has 19.83 $k\Omega$ which is not affecting the input signal very much.

The input interference signals shown in figures 4.20 to 4.22 are showing that the simulation signal is smaller than the measured signal. The signals have a high amplitude due to the fact that the transmission line is not terminated with an 50 Ω termination, instead there is a unknown input resistance of the DUT. The differences of simulation and measurement could come from non linearity effects which are not supported by the model. A crosstalk extraction could lead to better results. At figures 4.23 to 4.25 the measured signal quality is bad because of the active probe impedance and the resolution of the oscilloscope. No accurate information can be obtained about this measurements.

For the comparison of the output signal at figures 4.26 to 4.29 it can be said that there is a bigger DC part in the simulation curves but a smaller amplitude. This leads to an higher average output voltage. One can conclude that the spice model for higher frequencies and high amplitudes is not correct.

In general the frequencies and waveforms of simulation and measurement fit to each other.

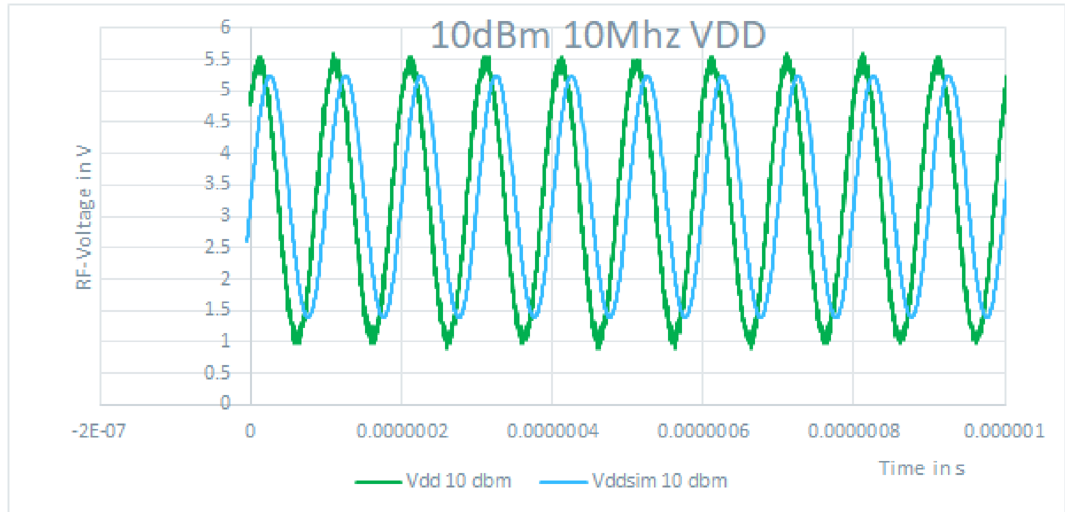

Figure 4.20: DPI measurement of interference signal vs simulation, 10 dBm, 10 MHz

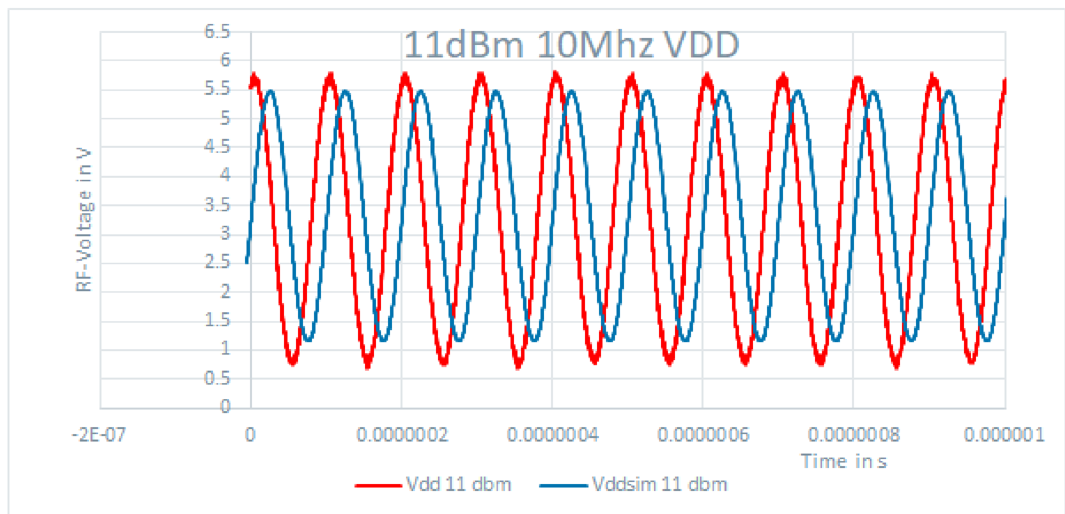

Figure 4.21: DPI measurement of interference signal vs simulation, 11 dBm, 10 MHz

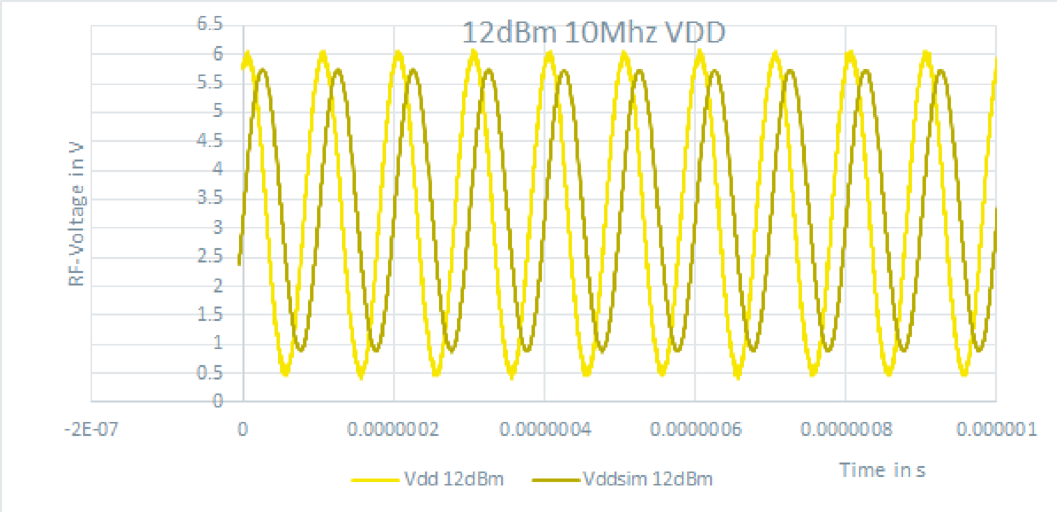

Figure 4.22: DPI measurement of interference signal vs simulation, 12 dBm, 10 MHz

Figure 4.23: DPI measurement of interference signal vs simulation, 10 dBm, 1 GHz

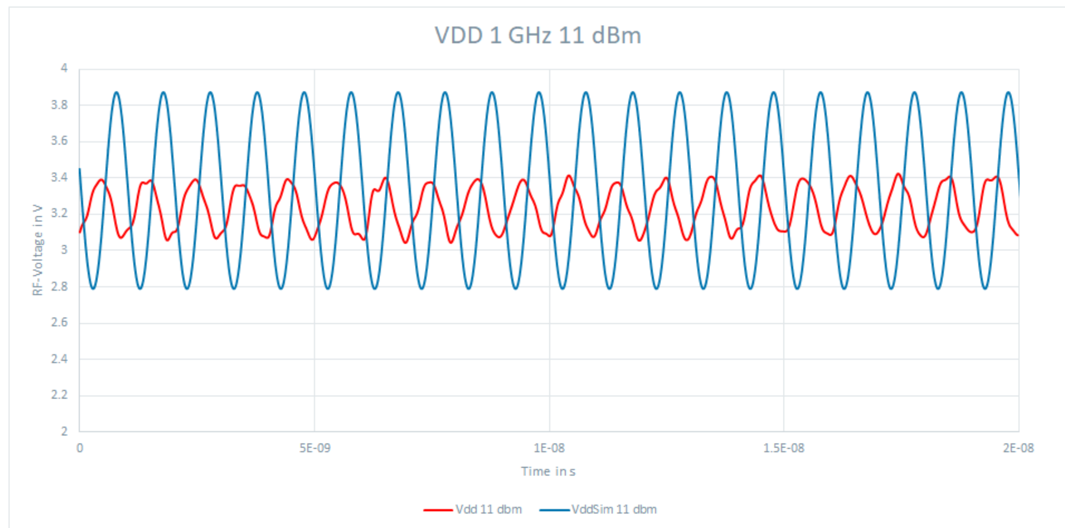

Figure 4.24: DPI measurement of interference signal vs simulation, 11 dBm, 1 GHz

Figure 4.25: DPI measurement of interference signal vs simulation, 12 dBm, 1 GHz

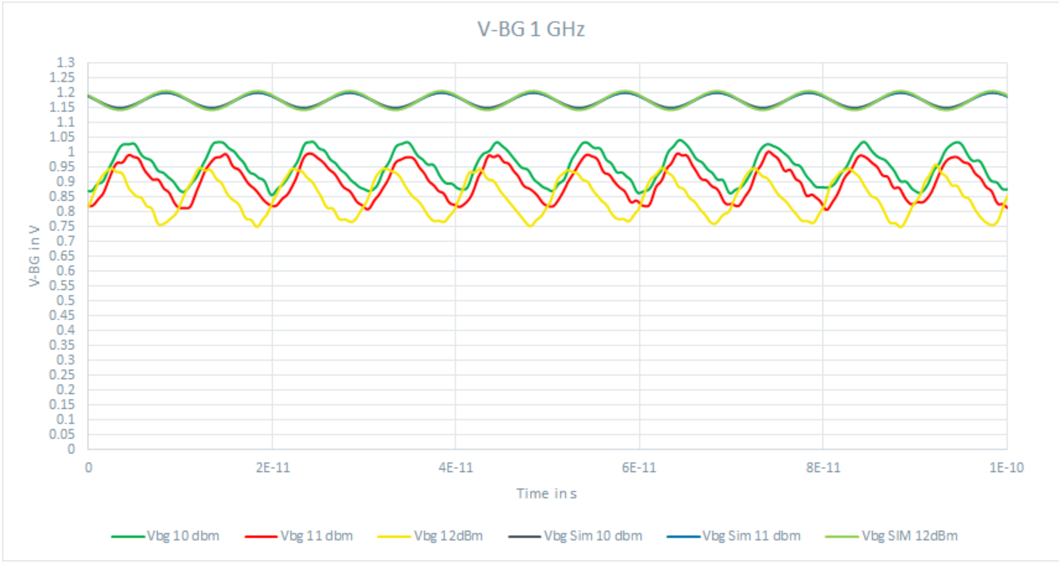

Figure 4.26: DPI measurement of V_BG vs simulation of V_bg, 1 GHz

Figure 4.27: DPI measurement of V_BG vs simulation of V_bg, 10 MHz, 10 dBm

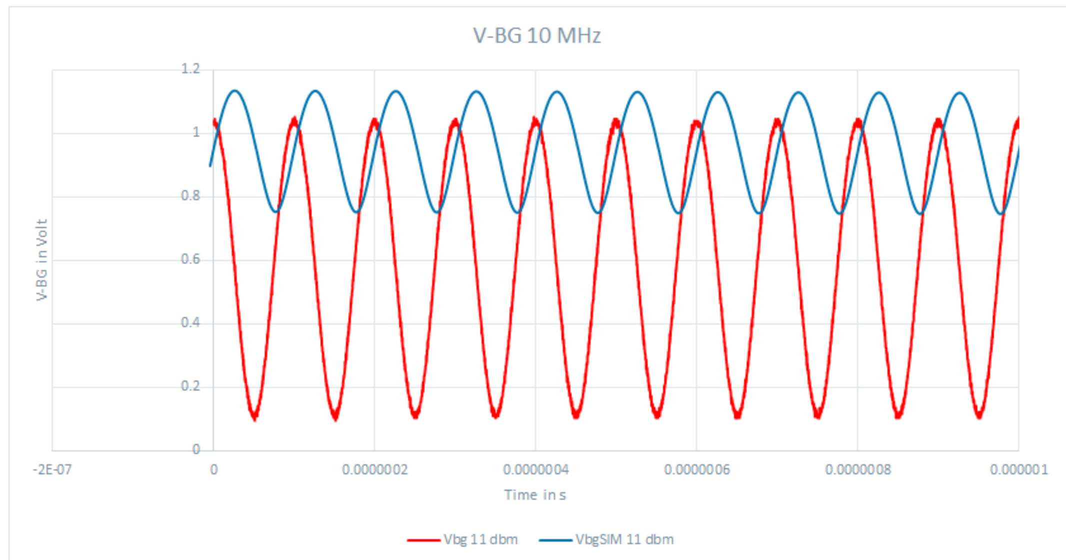

Figure 4.28: DPI measurement of V_BG vs simulation of V_bg, 10 MHz, 11 dBm

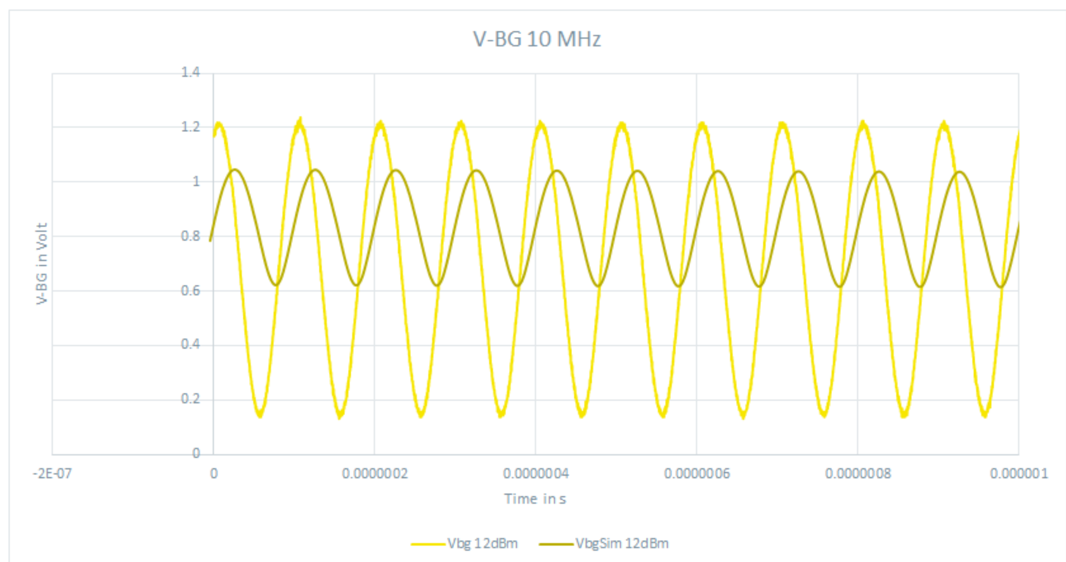

Figure 4.29: DPI measurement of V_BG vs simulation of V_bg, 10 MHz, 12 dBm

5 Conclusion

In this thesis several topics are examined and discussed. The main focus lies on getting information about DPI-tests, building up test structures for protection circuits, building up the DPI-measurement board, DPI measurement, simulation of the DPI test and finally comparison of results between measurement and simulation.

Test structures:

Several components are tested like broadband capacitors, inductors and ferrites. The found information is used to build up a decoupling network, which is used in DPI tests and bias tees. The challenge behind it lies in finding this components and in there frequency behaviour. The impedance of the network must be higher than 400 Ω over the whole used frequency range by the DPI test. The broadband capacitor is used to have very little influence for RF-Signals and blocks DC-Signals.

DPI-measurement board

The board is designed in a way that the insertion path has not more than $-3\ dB$ attenuation at the insertion pin of the chip. The DCN protects the DC supply from RF-interference signals. A special rogers 4350-1 material is used for the manufacturing process. Shielding vias are applied to prevent ground bounce and shield the 50 Ω traces. Ground to ground vias are placed even over the whole board.

Measurement:

The measurement is done with two test setups. The reason for this is, that the used power amplifier and bi directional coupler are limited to

frequencies up to 1 *GHz*. For higher frequencies the signal generator is able to provide the needed power by itself. The measurement is done with a program that automates the measurement and is provided by ams AG. There is no failure criterium set to interrupt the measurement for better comparison with the simulation later on. The measurement setup must be done very carefully and precise to avoid measurement differences.

Simulation:

In the simulation part of the thesis modelling of the parasitics plays an important role. The simulation program is able to compare layout and schematic and calculates resistive and capacitive passive parasitic elements and adds them to the schematic. The most challenging part of this section is to get all data needed. The test bench for the DPI-simulation consists of n-port elements with S-parameters from the DCN and DC-block capacitor. As load a 1 $M\Omega$ resistor and 10 *pF* capacitor are set in parallel to ground to model the input impedance of an oscilloscope. As RF-source an port element is used. With this element it is possible to set power levels with an variable. At the DPI-simulation itself, the output signal of the band gap reference is averaged after settling time over several periods. The biggest challenge is the long computing time of each curve.

Comparison:

For low frequencies up to 100 *MHz* and low power levels up to 9 *dBm* the simulation is tends to be similar to the measurement. For higher frequencies it seems like the simulation curves tend to the DC-voltage. For higher powers the simulation is also in lower frequency domain inaccurate. There could be several reasons why the simulation does not fit the measurement. To list a few: an insufficient model of the IC, the package was not considered, the substrate coupling was not considered, maybe the PCB is not modelled correct for high frequencies or maybe the output load does not fit.

Conclusion:

It is possible to create a DPI setup that works up to 6 *GHz* and do not

violate the IEC standard. The comparison between measurement and simulation shows that for low power and low frequencies the model of the test is accurate enough to predict difficulties. For higher frequencies and powers the model is inaccurate.

A base was done for new tests and to find out why the simulation does not fit the measurement. Maybe following theses will discover a solution.

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