Graz University of Technology

Master thesis

PVT robust, ultra-low-power limiting amplifier & RSSI for a 125kHz ASK receiver

In a tire pressure monitor system application

conducted at the
Institut of electronics
Graz University of Technology, Austria

in co-operation with

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Above all, my parents and family who gave me the opportunity to study, financially support and who raised me on an open-minded education.

Abstract

The topic of this thesis is the design and simulation of a ultra low power limiting amplifier and received signal strength indicator (RSSI) with regard to process, voltage, and temperature (PVT) variations. The design is described for a 0.120 µm CMOS process. The limiting amplifier & RSSI is demodulating an amplitude shift keying (ASK) modulated signal with a carrier frequency of 125kHz.

Due to the required ultra low power consumption, most transistors operate in weak inversion. Especially in respect to PVT variations for the design, the weak inversion operating point is challenging. A lot of publications deal with limiting amplifiers operating at a higher frequency, thus these amplifiers consume a decade more current and the transistors can operate in strong inversion. The design presented in this thesis differs from these approaches.

Starting with the idea of a new architecture for a limiting amplifier and a reference design, the thesis gives an overview of new different architectures of gain stages and rectifiers for the specified ultra low power consumption, AC gain, noise and bandwidth. All these parameters are investigated with respect to PVT variation, to establish a PVT robust RSSI current.

A new limiting amplifier architecture is designed and simulated, starting with validating the RSSI current with respect to variation of process corners and temperature. An offset control for the limiting amplifier with a specific bandwidth and stability is implemented. The design is optimized with respect to the current consumption for a specified noise. The most important parameters of the new design are validated in Monte Carlo simulations at different temperatures.

The new limiting amplifier fulfills all the specifications. The design is compared to an reference design, which has similar performance parameters. Some parameters like area, current consumption are slightly deteriorated but the most important parameter: the carry detect threshold variation is significantly improved for the new limiting amplifier design.

Statutory Declaration

I declare that I have authored this thesis independently, that I have not used other than the declared sources/resources, and that I have explicitly marked all material which has been quoted either literally or by content from the used sources.

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Contents

1 Introduction

1.1 Tire pressure monitor systems

A tire pressure monitor system (TPMS) is a sensor system for measuring tire pressure of a vehicle. The system warns the driver or displays the pressure, if the pressure is too low. With a proper tire pressure, the vehicle saves gas and is safer for driving [1]. There are direct and indirect ways of measuring the pressure of the tire. Figure 1.1 shows a direct TPMS sensor located at the valve of a tire.

Figure 1.1: Direct TPMS system [1]

Indirect systems measure, for example, the rotational speed with an ABS system. A lower pressure decreases the diameter of the tire, therefor the rotational speed for equal car speed is higher [1]. Direct systems have higher precision but they are more expensive due to additional components. Additionally, within direct systems there is often also a temperature sensor and an acceleration sensor. For modules inside the tire, two different kind of power supplies can be found: battery or energy-harvesting power source. The most common power supply in the TPMS application is a battery driven source.

[1] `http://www.tpms-sensor.de/i/obrazky/KAP_tpms-sensors.jpg`; Access date: March, 16 2017

Infineon already sells direct TPMS products ("SP..." product family) successfully. All these sensor system products measure the pressure directly inside the tire and they are supplied by a battery that should last for more than 10 years. For communication, the system has a low frequency receiver (LFRX) and a radio frequency transceiver (RFTX). This work concentrates on the LFRX. The power consumption of the whole chip has to be very low for the high battery life cycle. In a common operation, the LFRX requires a large share of the batteries energy because the LFRX is constantly waiting for an input signal to wake up the whole chip.

1.2 LFRX

The received signal is amplitude-shift key (ASK) modulated. The LFRX works at a carrier frequency of 125kHz, thus the antenna is a high inductance coil, which is soldered on a PCB board with the CMOS chip. The receiver block of the chip has to detect a carrier and demodulate the ASK signal into a digital signal. The block diagram of the LFRX is shown in figure 1.2.

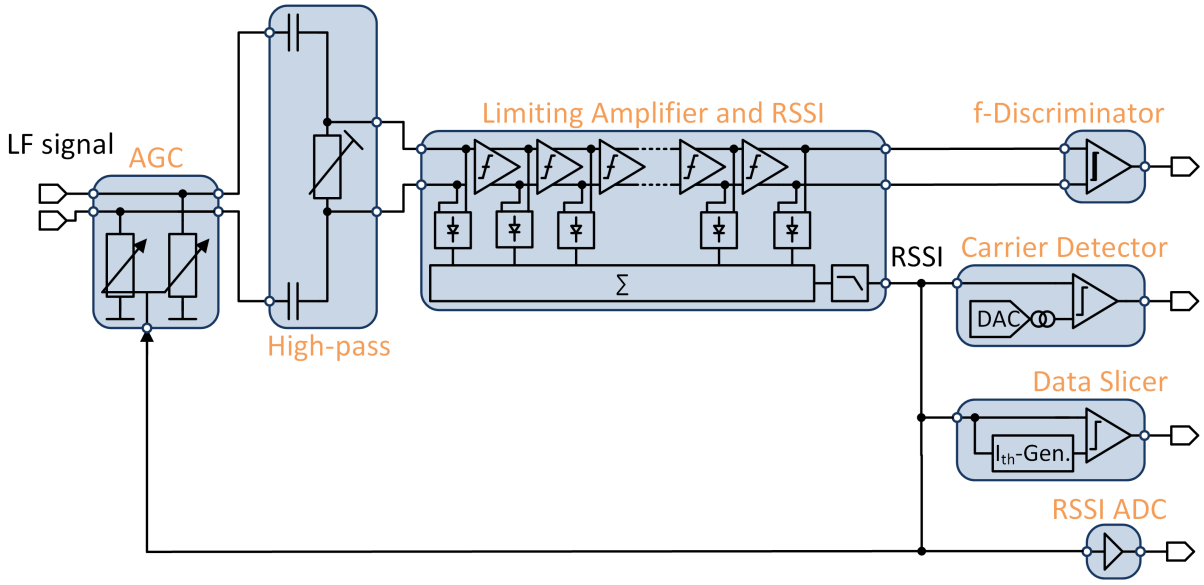


Figure 1.2: Block diagram of the LFRX

There is an automated gain control (AGC) attenuator at the input, which can damp the input signal at different levels and protects the input of the chip from large voltages. A high-pass filter is placed after the AGC for damping low frequencies and DC components of the signal.

The core of the receiver is a limiting amplifier & RSSI (received signal strength indicator) also called logarithmic or clipping amplifier. The limiting amplifier & RSSI block has a logarithmic transfer function. Inside the limiting amplifier & RSSI is a low-pass filter to get the envelope of the signal.

The frequency discriminator verifies the right carrier frequency, the data slicer demodulates the ASK signal with an accurate duty cycle and the carrier detector verifies the right signal level. There is also an analog-to-digital converter (ADC) for digitalizing the RSSI signal. Some of these blocks are described in more detail in chapter 2.

1.3 Limiting Amplifier & RSSI

A limiting amplifier & RSSI is a basic building block for communication systems [2]. This block consists of a number of cascaded **gain stages** to get a high gain. After each gain stage there is a **rectifier**. All the rectified currents are summed up in one point. The summed currents are low-pass filtered to get the envelope of the RSSI current signal. The limiting amplifier generates a current with an amplitude that is logarithmic proportional to the input voltage. This is necessary to distinguish between different input voltage levels with a high dynamic range. The RSSI signal can be used to demodulate a ASK signal, to detect a carrier with the right amplitude or it can be fed into an ADC. The digitalized RSSI signal can than be used for example to determine the position of the sensor [1].

1.4 Objective of this thesis

This work concentrates on the limiting amplifier & RSSI without the low-pass filter of the LFRX. There are tight restrictions in power consumption for the design of the LFRX. A lot other specifications for accuracy of the circuit are given by the customer or concept department. The circuit has to fulfill the specifications within temperature, process variation, mismatch and supply voltage (PVT). Obviously a high yield for the product and for the LFRX block is required. This tight specifications are challenging for the design of the circuit, especially when transistors operate in weak inversion which is required for low power consumption. In weak inversion a lot of parameters are highly dependent on process and temperature. These effects have to be compensated by the design.

A reference design exists and is briefly discussed. Much work has already been done in designing a limiting amplifier and rectifier that fulfills all given criteria. The objective of this thesis is to provide an overview of new, different architectures for gain stages and rectifiers with respect to all modeled PVT variations. A new limiting amplifier with different architecture is designed, simulated, and compared to the reference design.

2

Limiting amplifier & RSSI basics and specification

2.1 Limiting Amplifier & RSSI

Figure 2.1 shows a limiting amplifier & RSSI in detail. It is common to cascade a number of differential gain stages to achieve a logarithmic transfer function of the limiting amplifier. There is a full wave rectifier which converts voltage into a rectified current (transconductance) after each gain stage. Additionally one rectifier is placed in front of the first stage to enhance the dynamic range. All currents of each rectifier are summed up at a single point. A low-pass filter generates the envelope of the rectified current. This current is called RSSI signal or RSSI current. The limiting amplifier consists of N gain stages and N+1 rectifiers.

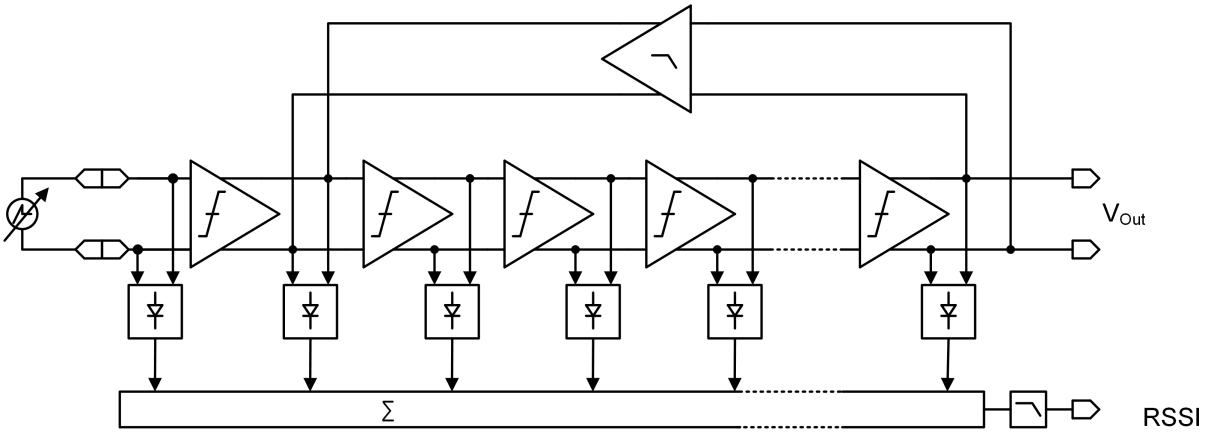


Figure 2.1: Block diagram of a limiting amplifier with offset compensation

Due to mismatch, there is an offset voltage that is amplified with the high gain of the limiting amplifier. A high voltage at the output caused by the offset voltage will most likely saturate the whole amplifier. A DC feedback is needed to cancel the offset. The offset compensation block (on top of the gain cells in figure 2.1) is a differential low-pass filter and a cross coupled differential pair. The cross coupled differential pair converts the offset voltage into a current, which is subtracted from the first stage, thus generating a voltage that counters the offset voltage. The feedback path is closed after the first stage because it is easier to add or subtract currents rather than voltages. The transfer function in the frequency domain of the system is described in more detail in subsection 2.7 on page 21.

2.1.1 Logarithmic amplification

In a certain range ($vin \approx 10mV - 100mV$ for the blue curve, $vin \approx 0.1\mu V - 100mV$ for the red curve) the RSSI current is proportional to the logarithmic input voltage as can be seen in figure 2.2. The logarithmic amplification is needed to cover the high dynamic range of input signal levels with high accuracy. A limiting amplifier compared to an AGC can also handle a larger dynamic range while consuming less power [3]. Due to a small input signal the last amplifier clips first. At rising input signal, more stages will saturate. In this way a piecewise linear approximation of the logarithmic function with high dynamic range is reached. Figure 2.2 shows the RSSI currents of different ideal limiting amplifier models with a fixed number of ideal gain stages (N = 7) and ideal rectifiers (N+1 = 8). In the different models of the limiting amplifier the single gain stages have the gain of $A_s = 2 - 12$. The rectifiers clip at 1A and have transconductance of 1S. The more gain the single gain stages have, the larger is the dynamic range of the limiting amplifier & RSSI.

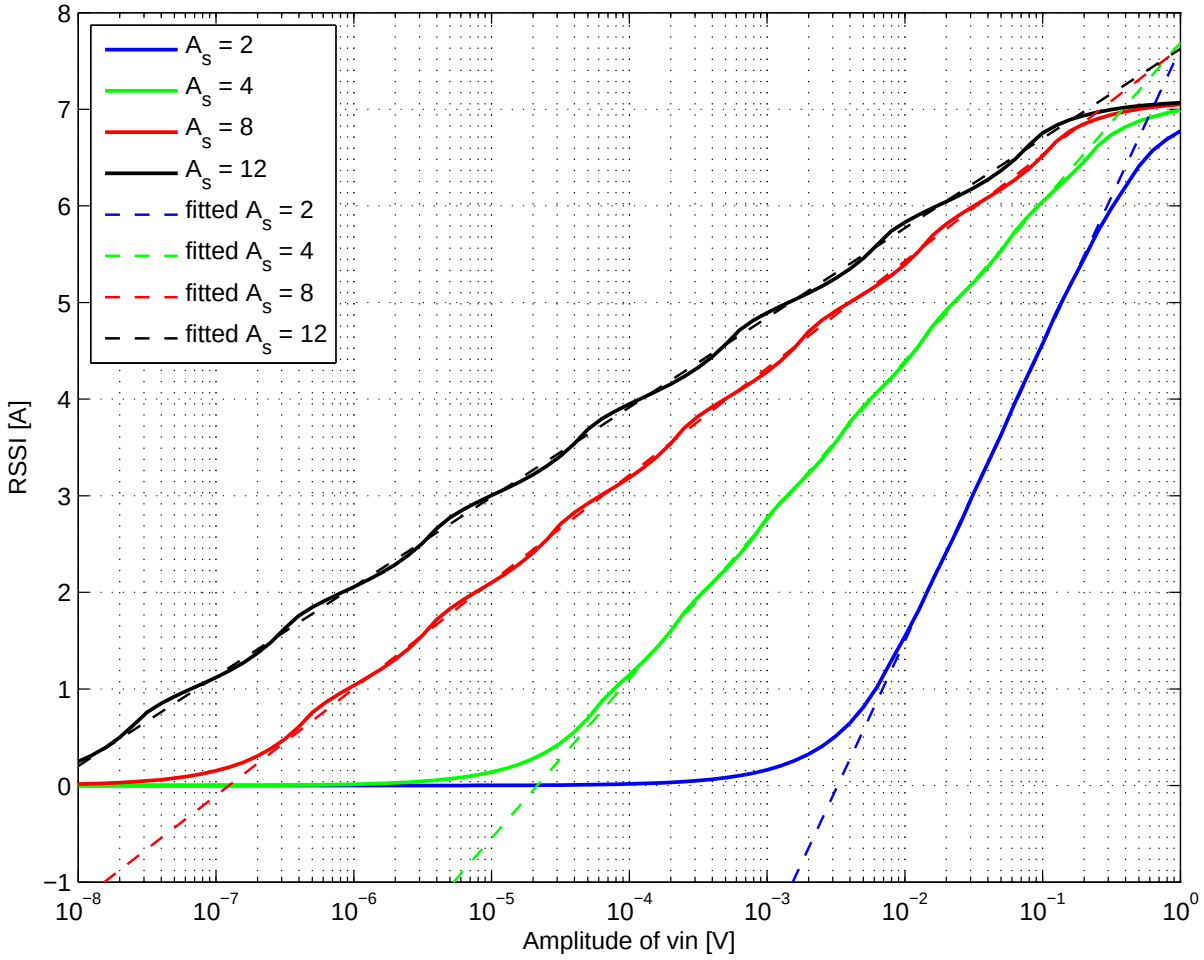


Figure 2.2: RSSI of a limiting amplifier with different gain of a single stage

The sensitivity of the amplifier is determined by the lowest input signal that can be detected. All input signals with an amplitude can be detected, for which the RSSI is close to the fitted logarithmic function. This point is determined by the gain of the single gain stages and the number of stages (described in more detail in section 2.3). Furthermore the point is limited by the noise of the limiting amplifier as described in section 2.6.

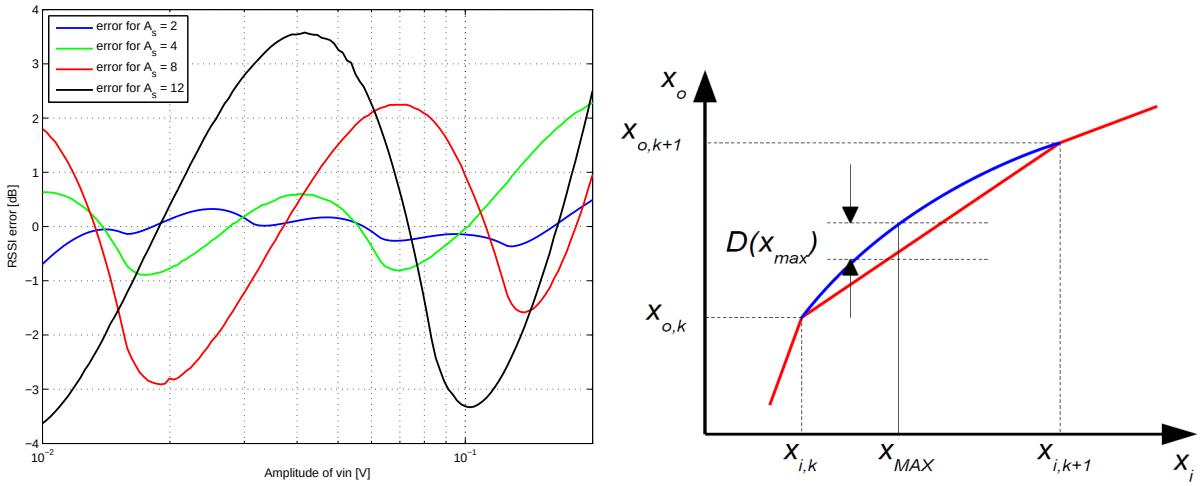
2.1.2 RSSI error

The maximum error, also called ripple, is the difference between the RSSI of an limiting amplifier and an ideal fitted logarithmic function in a certain range (Figure 2.2, $vin \approx 10mV - 100mV$ for blue curve, $vin \approx 0.1\mu V - 100mV$ for red curve). Theoretically the maximum error in dB can be calculated by equation 2.1 from [3] or the maximum error in V by equation 2.2 from [4] where A_s is the gain of a single gain stage and V_S is the clipping level of a single gain stage.

$$max\_Error\_1 = \frac{10\left[(-1+\sqrt{A_s}+A_s)log_{10}(A_s) - (A_s-1)log_{10}\left(A_s^{\frac{3A_s-1}{2A_s-2}}\right)\right]}{A_s-1} \tag{2.1}$$

$$max\_Error\_2 = V_S \cdot \left[\frac{ln\left(\frac{A_s-1}{ln(A_s)}-1\right)}{ln(A_s)} + \frac{1}{A_s-1}\right] \tag{2.2}$$

Figure 2.3(a) shows the RSSI error in the range of $vin = 10mV - 200mV$ of the input voltage for different gains of a single stage. Each low-pass filtered RSSI current is fitted with an ideal logarithmic function by the least square method (figure 2.2 dashed lines or figure 2.3(b) blue line). The error of the RSSI is higher for a larger gain compared to a smaller gain of the single gain stages (figure 2.3(a)).



(a) RSSI error of a limiting amplifier with different gains (b) Piecewise linear approximation of a log function [5] of a single stage

Figure 2.3: RSSI error of a limiting amplifier

Figure 2.3(b) from [5] shows the maximum distance ($D(x_{max})$) between a ideal logarithmic function (blue) and a piecewise linear approximation (red) with a linear x-axis. The maximum distance is a figure for the maximum error.

Since all the real gain stages and rectifiers are not perfectly linear and not clipping at a well defined point ($x_{i,k}$), as shown in figure 2.3(b) the theoretical calculation (equation 2.1 and equation 2.2) is a simplification but sufficient for estimating a RSSI error. With a circuit simulator the error can be determined more precisely by considering all the nonlinearities of the gain stages and the rectifiers.

2.1.3 Cliping behavior

The gain stage has a positive and a negative output voltage clipping level (V_S). This mens the output voltage does not exceed this voltage value. If the rectifier clips it provides the maximal output current. Here the combination of a gain stage with rectifier load, as shown in figure 2.4, is considered. There are different possibilities of clipping behavior:

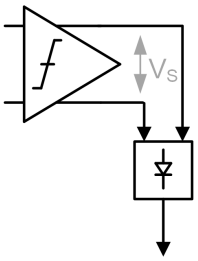


Figure 2.4: Gain stage with rectifier load

- Gain stage clips before the rectifier
- Rectifier clips before the gain stage
- Gain stage and rectifier clip at the same level of input signal

If the gain stage clips before the rectifier, then a temperature stable output voltage clipping level V_S of the gain stage is important for a temperature stable RSSI. In the second case the rectifier clips before the gain stage. In this case the clipping current of the rectifier should be temperature stable. In this case V_S is referred to the input clipping voltage of the rectifier because it is lower than the output clipping voltage of the gain stage. In the third case where both clip at the same input level, both clipping levels should be temperature constant. In the design of the thesis the rectifier clip before the gain stage clip due to the amplification of the gain stage the temperature unstable voltage clipping level of most gain stages. The clipping current of the rectifier can easily be limited by a temperature stable bias current (I_B) of the rectifier. Clipping is described in more detail for gain stages in chapter 4.1.4 on page 41 and for rectifier in chapter 5.1.1 on page 63.

2.2 Modes of operation

There are different modes of operation for the LFRX. The most important modes for the design are the carrier detect mode and datagram mode.

2.2.1 Carrier detect mode

In the carrier detect mode most blocks of the chip are in a sleep mode and the LFRX is waiting for a valid psurereamble carrier signal. The chip wakes-up, if there is a valid carrier preamble. Three additional criteria can be selected, which the signal has to satisfy: signal level, pulse duration or width, and frequency.

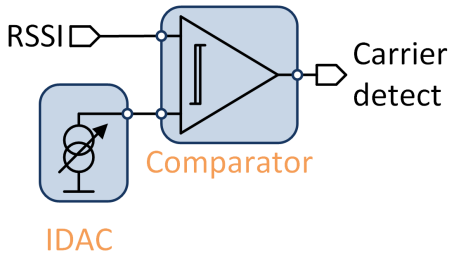


Figure 2.5: Carrier detect comperator with trimmed threshold

There is a frequency discriminator to detect the specified frequency. The pulse duration can be checked digitally. The RSSI current is compared with a reference current from an IDAC (current digital analog converter) shown in figure 2.5 to check the specified signal levels.

The threshold value from the IDAC can be trimmed, such that process or mismatch effects can be compensated and the tight specifications are satisfied. These amplitude levels are specified by the application such that the chip does not wake up by an electromagnetic interferer or another TPMS sensor near the target sensor.

Figure 2.6 shows the amplitude within the pulse width criteria that has to be satisfied. There must not be any detection of a carrier for a shorter time than the no detect time (t_{nodet}) or signals with smaller amplitude than the no detect signal amplitude (S_{nodet}). Between the no detect and the detect amplitude level (S_{det}) a detection can be possible. This region leaves some room for nonidealities of the design. If the signal exceeds the S_{det} amplitude and if there is a pulse width greater than the detection width (t_{det}), then detection of the carrier is mandatory.

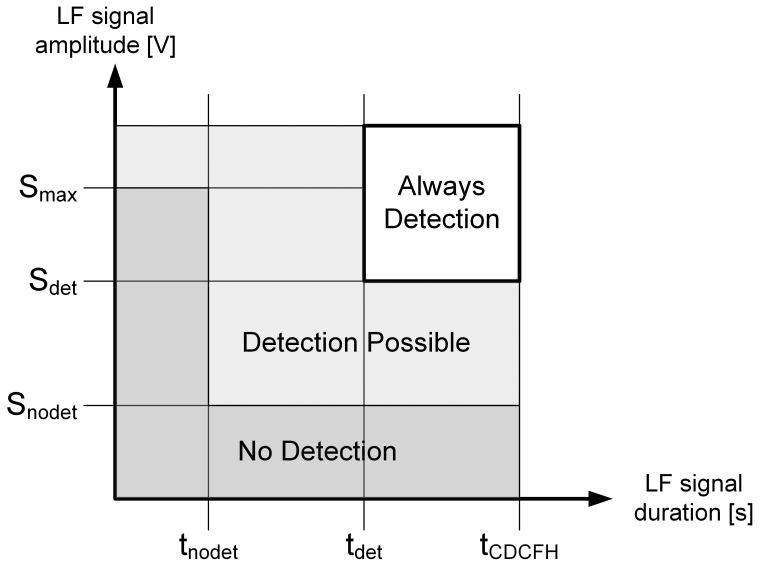


Figure 2.6: Conditions for signal level detection

The specification of voltage levels for this design in the carrier detect mode is:

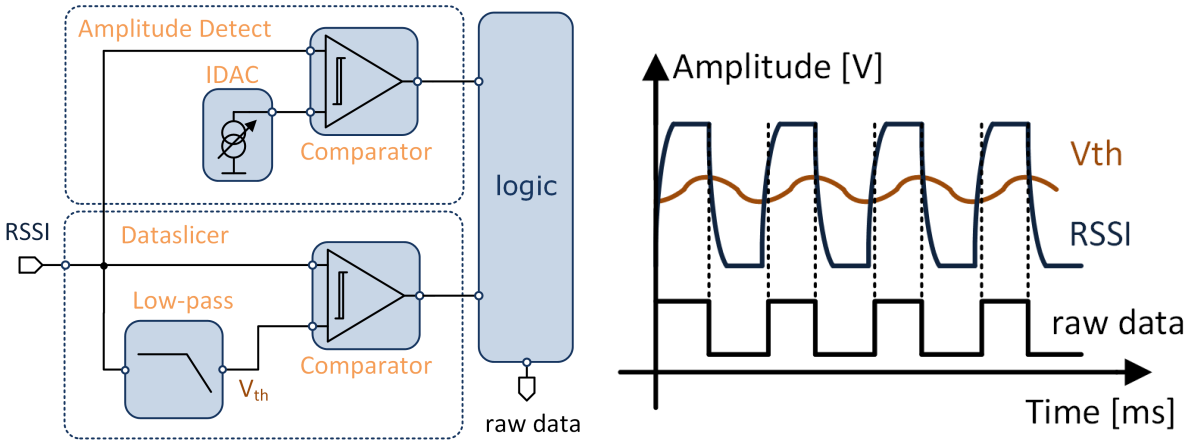
- Signal level: $S_{nodet,pp} = 4mV$, $S_{det,pp} = 12mV$
- Pulse width: $t_{det} = 700\mu s - 1300\mu s$
- Frequency: min: 115kHz typ: 125kHz max: 135kHz

The specifications in this example yield an accuracy of $20 \cdot log_{10}(12mV/4mV) \approx 9.5dB$ for the signal amplitude. These levels are different for each customer but show the tightest specifications for the limiting amplifier design. Further this criterion has to be satisfied in the full temperature range and for a $C_{PK} \approx 1.5$, so 99.9994% of the chips.

2.2.2 Datagram mode

The ASK signal is demodulated to digital data in the datagram mode. Figure 2.7(a) shows the block for the demodulation of the datagram. The figure shows the amplitude detector and the data slicer. For the demodulation of the datagram, a dynamic threshold (V_{th}) is generated with a low-pass filter and compared to the RSSI signal by the data slicer. The dynamic threshold is generated for a proper duty cycle of the demodulated signal. Figure 2.7(b) shows the transient signals of the demodulation.

The amplitude detector verifies the amplitude of the RSSI signal in the datagram mode. The IDAC value can be set manually. The comparator demodulates all input signals that can be detected by the LFRX. With additional noise random bits with different pulse width appear to the digital logic. The raw digital datagram signal can be filtered by digital logic with the specified pulse length t_{det}. A logic operation generates a valid digital data signal at the output.



(a) Block diagram of datagram mode

(b) Transient demodulation of datagram

Figure 2.7: Datagram block diagram and transient demodulation scheme

In the datagram mode, signals below $S_{nodet} = 100\mu V$ must not be detected and signals above $S_{det} = 1mV$ have to be detected. Hence, $S_{nodet} = 100\mu V$ gives the lower limit of the signal that can be decoded. This parameter is also important for the minimum gain of the limiting amplifier. The specification for the datagram mode amplitudes is more relaxed ($20log_{10}(1mV/100\mu V) = 20dB$) in this design compared to the carrier detect amplitude levels.

2.3 AC Gain

The AC gain of the limiting amplifier can be linked directly to the RSSI of the limiting amplifier, thus it has to be PVT stable for a PVT stable RSSI.

The lowest signal which can be detected ($S_{nodet,pp}$) and the clipping voltage where the first gain stage or rectifier clips determine the minimum voltage gain of the whole limiting amplifier ($A_{limiter}$ equation 2.3). Assuming an $V_S \approx 100mV$ (input voltage clipping level of a rectifier in weak inversion chapter 5.1.1 on page 63) yields a gain of 60dB. The S_{nodet} and the S_{det} thresholds leave some room for PVT variations of the RSSI and thus the gain. The gain for a single gain stage is given in equation 2.4. Thus N = 8 gain stages require a gain of 8.57dB each.

$$A_{limiter} \approx \left(\frac{V_S}{S_{nodet,pp}}\right) = 20log_{10}\left(\frac{100mV}{100\mu V}\right) = 60dB \tag{2.3}$$

$$A_s = \sqrt[N]{A_{limiter}} = \sqrt[8]{1000} \approx 2.68 = 8.57dB \tag{2.4}$$

The dynamic rage, assuming 1dB absolute RSSI error, covered by A_s and N can be calculated by equation 2.5 from [4]. The result from this equation is smaller than the simple approximation of the dynamic range: $20log_{10}A_s^N$.

$$RSSI_{dynamic\_range,dB} = 20log_{10}A_s\left(N + 1 - log_{As}\left[\frac{2}{A_s}\left(\frac{20log_{10}A_s}{\pi}\right)^2\right]\right) \tag{2.5}$$

2.4 Bandwidth

The bandwidth of a single amplifier (BW_s), assuming a single pole approximation of the transfer function ($A_s(s)$), can be written in the form of equation 2.7 from [5].

$$A_s(s) = \frac{A_{s0}}{1 + \frac{s}{p}} \tag{2.6}$$

$$BW_s = f_{-3dB} = \frac{1}{2\pi \cdot \frac{1}{fp}} = \frac{1}{2\pi R_{out} C_L} \tag{2.7}$$

The bandwidth of cascaded amplifiers can be determined by solving the transfer function $A_{limiter}(s)$ (equation 2.8) of the limiting amplifier to $\frac{A_{s0}^N}{\sqrt{2}}$ leading to equation 2.9.

$$A_{limiter}(s) = A_{s0}^N(s) = \frac{A_{s0}^N}{(1 + \frac{s}{fp})^N} \stackrel{!}{=} \frac{A_{s0}^N}{\sqrt{2}} \tag{2.8}$$

$$BW_{limiter} = BW_s \cdot \sqrt{\sqrt[N]{2} - 1} \tag{2.9}$$

The -3dB low-pass bandwidth of the limiting amplifier is given in the specifications at a minimum of $BW_{limiter} = 150kHz$. A limiting amplifier with N = 7 gain stages and the specified bandwidth requires the bandwidth of equation 2.10 for a single gain stage.

$$BW_s = \frac{BW_{limiter}}{\sqrt{\sqrt[N]{2} - 1}} = \frac{150kHz}{\sqrt{\sqrt[7]{2} - 1}} \approx 465kHz; \qquad fp \approx 2\pi \cdot 465kHz = 2.92 \cdot 10^6 \frac{rad}{s} \tag{2.10}$$

2.5 Supply Voltage and power consumption

2.5.1 Supply Voltage

The chip is supplied by a battery. An LDO (Low dropout regulator) with a reference voltage generated by a bandgap, scales the battery voltage down to 1.5V. The 1.5V supply voltage can have a minimum output voltage of 1.35V and a maximum output voltage of 1.65V due to process, mismatch, temperature, and load current variations.

2.5.2 Power consumption

In the **carrier detect mode**, a maximum power consumption for the whole limiting amplifier is specified with $I_{TOT} = 1.1\mu A$. Lower power consumption is desirable. During the **datagram mode**, more current is specified because this mode is only active when there was a valid carrier preamble before.

$$P = N \cdot V_{DD} \cdot I_B \propto N \cdot GBW^2 = N \cdot \left(A_{limiter}^{1/N} \cdot \frac{1}{\sqrt{\sqrt[8]{2} - 1}} \cdot BW_{limiter} \right)^2 \tag{2.11}$$

$$I_B = \frac{I_{TOT}}{N} \tag{2.12}$$

The overall power consumption of the gain stages (equation 2.11 from [6]) is proportional to the gain bandwidth (GBW) of a single gain stage and the number of stages. In [3], [6] and [7] the number of stages is directly related to the power consumption for a given bandwidth. The minimum of equation 2.11 with the given bandwidth reveals the ideal number of N = 4.48 gain stages. In this design thermal noise of the gain stages is the dominant factor for power consumption as can be seen in the following chapters. The maximum RSSI error is an additional restricting factor, which determines the number of stages and therefore the power consumption.

2.6 Noise

The noise specification is given by the concept department but must not exceed the level of the lowest signal detection possible. The noise specification can be derived by the specified bit error rate (BER) and the sensitivity of the receiver. A limiting amplifier changes the SNR_{in}/SNR_{out} ratio as stated in [8]. The noise of all gain stages is mostly rectified in the last stage. The additional noise brings up the bottom line of the RSSI curve (figure 2.2). The integrated input referred noise at room temperature is specified by $S_I = 100\mu V$.

2.6.1 Noise factor

The noise of the first gain stage is the most critical one as stated in the Friis formula (equation 2.13) from [9]. The noise factor F of the whole cascaded system is composed of the noise factor of all cascaded systems. In the equation, F_N is the noise factor and A_{sN} is the gain of a single gain stages.

$$F = F_1 + \frac{F_2 - 1}{A_{s1}} + \frac{F_3 - 1}{A_{s1}A_{s2}} + ... + \frac{F_n - 1}{\prod_{N=1}^{n-1} A_{sN}} \tag{2.13}$$

2.6.2 Effective noise bandwidth (ENBW)

With the effective noise bandwidth of the amplifier it is possible to calculate the integrated input referred noise. This can be done by integrating the transfer function over the whole frequency range. In equation 2.14 the ENBW is normalized to the gain to compare a cascaded low-pass to an ideal brick wall low-pass filter as it is done in [10].

$$ENBW = \frac{1}{A_0^2} \int_{f=0}^{\infty} |A(f)|^2 df \tag{2.14}$$

Table 2.8 shows the B-factor of N cascaded first order real pole filters. The f_{-3dB} bandwidth of the cascaded filter can be determined by equation 2.9. The B factor compares the low-pass filter to an ideal brick wall filter with the cutoff frequency of f_{-3dB}.

N	Slope dB/dec	B
1	-20	$\pi/2 \cdot f_{-3dB}$
2	-40	$1.220 \cdot f_{-3dB}$
3	-60	$1.155 \cdot f_{-3dB}$
4	-80	$1.129 \cdot f_{-3dB}$

N	Slope dB/dec	B
5	-100	$1.114 \cdot f_{-3dB}$
6	-120	$1.105 \cdot f_{-3dB}$
7	-140	$1.098 \cdot f_{-3dB}$
8	-160	$1.094 \cdot f_{-3dB}$

Figure 2.8: Table for ENBW factor for cascaded filters [10]

For a cascaded real pole low-pass filter the ENBW can be calculated as in equation 2.15.

$$ENBW\_LP = B \cdot f_{-3dB} \tag{2.15}$$

For a cascaded high-pass filter the ENBW is stated in equation 2.16

$$ENBW\_HP = \frac{f_{-3dB}}{B} \tag{2.16}$$

The ENBW of a band-pass filter can be calculated by equation 2.17. For a non-symmetrical band-pass filter, the B-factor of the low-pass can be different to the B-factor of the high-pass.

$$ENBW\_BP = f_{LP-3dB} \cdot B_{LP} - \frac{f_{HP-3dB}}{B_{HP}} \tag{2.17}$$

2.6.3 Output referred noise

The integrated output referred noise power (S_{out}) is the integral of the output noise power density ($S_{out}(f)$) over the entire frequency range. $S_{out}(f)$ is the product of input referred power noise density ($S_{in}(f)$) the magnitude of the squared transfer function $A^2(f)$ (equation 2.18).

$$S_{out} = \int_{f=0}^{f=\infty} S_{out}(f) df = \int_{f=0}^{f=\infty} S_{in}(f) \cdot A^2(f) df \tag{2.18}$$

The integrated output referred noise can be simulated with a PNOISE (Periodic steady state noise) simulation with the whole frequency range or simple AC noise simulation. This noise can be observed at the output of the amplifier. The gain of different amplifiers can vary such that the output referred noise varies as well. It is more common to compare the input than the output referred noise density of different amplifiers.

2.6.4 Input referred white noise

The input referred noise power of white noise can be calculated for a simple low-pass filter by dividing the output noise power (S_{out}) by the transfer function of the amplifier and multiplying by the ENBW (equation 2.19). With the noise summary tool from Spectre it is possible to integrate the noise of the amplifier over the ENBW to get the input referred noise of the limiting amplifier. The ENBW integration frequencies must be specified by hand.

$$S_{in} = \frac{S_{out}(f)}{A^2(f)} \cdot ENBW = S_{in}(f) \cdot ENBW \tag{2.19}$$

The input referred noise can be determined by a PNOISE simulation because of the nonlinear behavior (clipping) of the circuit. An input signal of the lowest input sensitivity (S_{sign}) is applied. This is the geometric mean of the no-detect and the detect amplitude (equation 2.20).

$$S_{sign} = \sqrt{S_{nodet,pp} \cdot S_{det,pp}} \approx 750\mu V \tag{2.20}$$

2.7 Offset Compensation

Mismatch of the gain stage transistors create an offset voltage. This voltage is amplified with the large gain of the limiting amplifier. This amplified offset voltage is most likely to drive the limiter into saturation. With a feedback path, the DC offset voltage can be subtracted and the output will not saturate. Figure 2.9 shows the well known block diagram of a system G(s) with feedback where F(s) is the feedback path (offset subtracter) and L(s) is the forward path (limiting amplifier). The DC offset voltage is subtracted by an active low-pass filter. In [11] an implementation of an offset cancellation block for a limiting amplifier is described in more detail and some stability analysis is performed. Two major implementations of the offset compensation block are discussed (differential pair and chopper amplifier).

2.7.1 Transfercharacteristic

The offset subtracter is a first-order low-pass amplifier with a low cutoff frequency ($f_{-3dB,F}$) such that the LF signal is not damped in the closed loop and the DC offset is fully fed back.

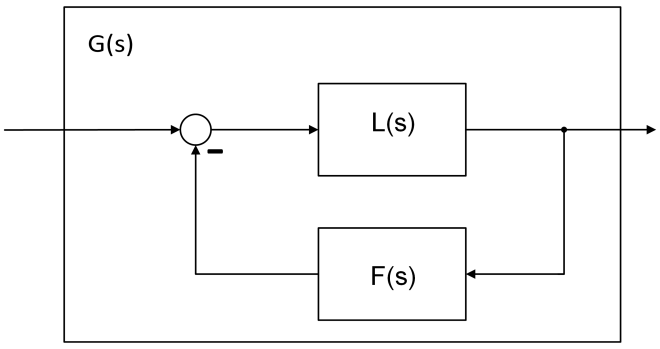


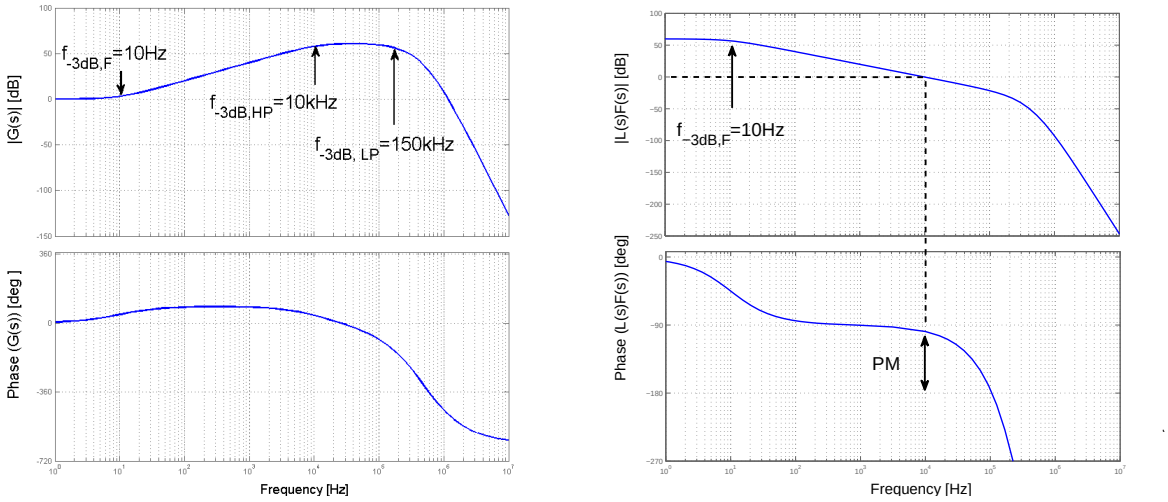
Figure 2.9: Blockdiagram of a system with closed loop

For a linear time-invariant (LTI) system (figure 2.9) with a closed loop the transfer function is stated in equation 2.21.

$$G(s) = \frac{L(s)}{1 + L(s)F(s)} \tag{2.21}$$

Low cutoff frequency of the feedback path increases phase margin and the stability of the system. High damping by a high gain of the feedback path (A_{0F}) is also desirable but will lead to a lower phase margin. The feedback low-pass filter acts as high-pass for the closed loop

transfer function. The overall transfer function G(s) is a band-pass, as can be seen in the Bode plot of figure 2.10(a). The -3dB cutoff frequency of the high-pass ($f_{-3dB,HP}$) is specified at a maximum of 80kHz for the limiting amplifier.



(a) Bode plot of the closed loop G(s)

(b) Bode plot of the open loop F(s)L(s)

Figure 2.10: Bodeplot of the systems transfer functions

The Bode diagram for the transfer functions of equation 2.22 is shown in figure 2.10. In this diagram L(s) is a first order low-pass cascaded N=7 times. The gain of a single stage of $A_{0L} = \sqrt[7]{1000} \approx 2.68$ is chosen, resulting in a limiter gain of 60dB (from equation 2.4). The pole frequency ($p_L = 2.92 * 10^6 rad/s$) is derived in equation 2.10 for a specified $f_{-3dB,LP} \approx 150kHz$ of the the limiter. The pole of the feedback low-pass filter is set to $p_F = 62.8 rad/s$, such that the specified high-pass cutoff frequency for the limiting amplifier $f_{-3dB,HP}$ is not exceeded. The $f_{-3dB,HP} \approx 10kHz$ from the simulation is within the specifications.

$$L(s) = \left(\frac{A_{0L}}{1 + \frac{s}{p_L}} \right)^7; \quad F(s) = \frac{A_{0F}}{1 + \frac{s}{p_F}} \tag{2.22}$$
$$p_L = 2.92 \cdot 10^{-6} rad/s; \quad p_F = 2\pi \cdot f_{-3dB,F} = 2\pi \cdot 10Hz \approx 62.8 rad/s; \quad A_{0F} = 1$$

2.7.2 Stability

There are different methods to ensure BIBO (bounded input bounded output) stability of the LTI systems. The Nyquist criterion is the most common one considering the open loop gain and phase (F(s)L(s)) of the system. If there is a positive phase margin (PM in equation 2.23 and in figure 2.10(b)) the system is stable. This is not a criterion for total stability but is a good indicator [11]. Further more the circuit is nonlinear, whereas the linear stability consideration is an estimation for stability.

$$PM = \angle F(s)L(s)|_{0dB} + 180° \tag{2.23}$$

The Middlebrook double injection technique [12] can be used in simulation to determine the transfer function of the open loop path. The negative feedback path is transformed into the Norton and Thevenin equivalent.

2.7.3 Settling time

Settling time due to offset

The LFRX operates in a pulsed mode to save power. A certain settling time of approximately 2ms is specified for the LFRX. The settling time estimation ($V(t) = [0.0\ to\ 0.99] * V_{max}$) for a simple RC low-pass first order is stated in equation 2.25. This shows the settling time is proportional to the pole frequency. An offset cancellation with a low frequency pole has a high settling time.

$$V_{out}(t) = V_{max} \cdot (1 - e^{\frac{-t}{\tau}}) \tag{2.24}$$

$$t_{settle} = \tau \cdot ln(1 - 0.99) \approx \tau \cdot 4.6 \tag{2.25}$$

In the limiting amplifier a regulation loop damps the offset voltage. Open loop settling takes place until the capacitance of the output voltage is charged to the value of the input offset voltage ($V_{OS,in}$) divided by the gain (A_{OS}) of the offset regulation [11]. Figure 2.11 shows the settling time of two systems with the same closed loop transfer functions. The only difference is the clipping voltage ($V_s = 2V$) of the forward path (red line). This difference implies that nonlinear clipping can enhance the settling time compared to a linear system with the same pole frequency (blue line).

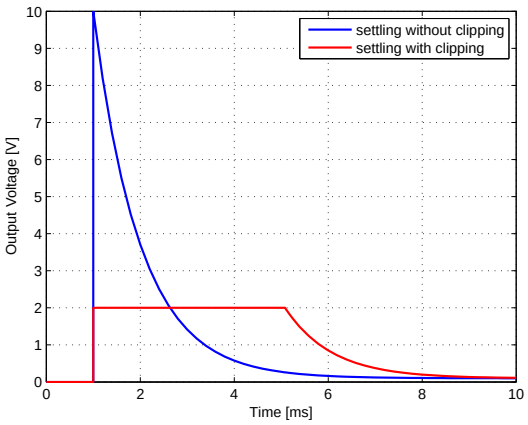


Figure 2.11: comparision of settling with and without clipping output voltage

Settling time due to common mode voltage

Also the common mode voltage has to settle. The output of the gain stage with the load capacitance has to reach the operating common mode voltage within the settling time. The limiting factor of the settling is the bias current of the gain stage and the load capacitance at the output.

Start-up circuit

With a start-up circuit the poles can be shifted to a higher pole frequency for reaching a faster settling time for the offset voltage as shown in [11]. The system stability in with the shifted poles has to be granted. The common mode voltage can be reached faster by pre-loading the load capacitance close to the nominal common mode voltage.

2.8 Other specifications

2.8.1 Temperature

In the temperature range of -40°C - 125°C the chip has to satisfy all the criteria specified by the customer. In simulations, temperature corners of -50°C - 150°C are used to guarantee a temperature stable design.

2.8.2 Process

The circuit is implemented in a standard N-well $0.120\mu m$ technology. The transistors used for the design are thick oxide transistors with a minimum length of $L_{min} = 400nm$. This transistors have good noise performance and a high threshold voltage, which is important for the design as can be seen in the following chapter 3. The circuit is also simulated over the process corners, here denoted by **nom**, **fast**, **slow**, **sf** (slow, fast) and **fs** (fast, slow). nom is the nominal or typical corner. Fast and slow corner are the corners where NMOS and PMOS have less or enhanced threshold voltage. sf is the process corner where NMOS has a larger and the PMOS has a smaller threshold voltage. fs is the process corner for which NMOS and PMOS have a threshold voltage in the opposite direction of sf.

2.8.3 Area

In total, the area of limiting amplifier with offset compensation must not be greater than $0.4(mm)^2$. The entire chip has a much larger area, such that the specification for area in a certain range is not such an important factor for the design.

2.9 Summarized Specifications

This chapter summarizes the most important specifications and the functionalities of the chip. Most of these specifications are explained in the previous chapter. The specifications are defined by the concept department, the costumers demand, or a norm for automotive products.

- min. supply voltage 1.35V, typical 1.5V, max 1.65V
- $I \leq 1.1\mu A$ current consumption for the limiting amplifier & RSSI with offset control
- $S_{det} = 4mV$–$12mV$ carrier detection for wake up (depending on customer)
- $S_{det} = 100\mu V$–$1mV$ demodulation of datagram (depending on customer)
- process, supply voltage and temperature (PVT) stable
- temperature range from T= -40°C – 125°C, (T = -50°C - 150°C in simulation)
- gain $A_{limiter} \approx 60dB$, maximal RSSI error +-5 dB
- rms of input referred voltage noise: $S_I \leq 100\mu V$
- offset subtraction
- band-pass: maximum. $f_{-3dB,HP} = 80kHz$; minimum $f_{-3dB,LP} = 180kHz$
- $t_{settle} \leq 2ms$ settling time

3 Weak inversion

3.1 MOS transistor in weak inversion

Due to the required ultra low power consumption of the design, most of the transistors operate in the weak inversion. This operation point is also called subthreshold because the gate-source voltage V_{GS} is smaller than the threshold voltage V_{TH}. In this operation point the current transport mechanism is rather diffusion than drift [13]. Without a bulk-source voltage ($V_{BS} \approx 0$) the drain-source current I_{DS} is an exponential function of V_{GS} stated in equation 3.1 from [14].

$$I_{DS} = I_0 \cdot e^{\frac{V_{GS}-V_{TH}}{\eta U_T}} \cdot \left(1 - e^{-\frac{V_{DS}}{U_T}}\right) \tag{3.1}$$

In equation 3.1, V_{DS} is the drain-source voltage and I_0 is a process and temperature dependent parameter stated in equation 3.2. U_T is the temperature voltage ($U_T \approx 25.8mV$ at T=27°C equation 3.3), V_{TH} is the threshold voltage of an MOS transistor, and η is the substrate factor described in the next section 3.2.

$$I_0 = \mu_0(T) \cdot C_{ox} \cdot \frac{W}{L} \cdot 2\eta \cdot U_T^2 = \beta \cdot 2\eta \cdot U_T^2 \tag{3.2}$$

$$U_T = \frac{k_B \cdot T}{q} = \frac{1.38 \cdot 10^{-23} J/K \cdot (273+27)K}{1.602 \cdot 10^{-19} C} \approx 25.8mV \tag{3.3}$$

Equation 3.4 from [15] is an approximation for the threshold voltage where Φ_{ms} is the difference of the work functions of polysilicon gate and the silicon substrate (also related to flat band voltage). Φ_F is the fermi potential, Q_{dep} is the depletion charge, and C_{ox} the oxide capacitance per area. Several other parameters effecting the threshold voltage are included in the BSIM model [16].

$$V_{TH}(T) \approx \Phi_{ms} + 2\Phi_F + \frac{Q_{dep}}{C_{OX}} \tag{3.4}$$

The threshold voltage is mainly temperature dependent, due to the temperature dependency of the fermi potential [15].

3.2 η, subthreshold slope, and subthreshold swing

In equation 3.5, η ($\eta = \frac{1}{\kappa}$) also referred to as **substrate factor**, is the coupling factor of the oxide and the depletion capacitance (C_{ox} and C_{dep}) of the transistor [17]. Subthreshold slope (S in equation 3.6 from [14]) is often given in the process manual, with the unit of mV per decade. The subthreshold swing is the inverse of the subthreshold slope.

$$\eta = \frac{C_{ox} + C_{dep}}{C_{ox}} = 1 + \frac{C_{dep}}{C_{ox}} \approx 1.2 - 1.7 \tag{3.5}$$

$$S = \eta \frac{kT}{q} \cdot ln(10) \cdot 1/dec \tag{3.6}$$

η is slightly dependent on the operating point of the transistor [17]. Furthermore η varies for different processes with typical values close to 1.3. The factor is typically a little higher (0.1 - 0.2) for PMOS transistors compared to NMOS transistors [17]. The temperature coefficient of η is in most cases negligible (for practical values below $0.001\frac{1}{K}$ [14]) but can be significant for temperatures below approximately -100°C [17].

The subthreshold slope is temperature dependent and can be seen as gradient of I_{DS} to V_{GS} in figure 3.1 at different temperatures with a logarithmic y-axis scale.

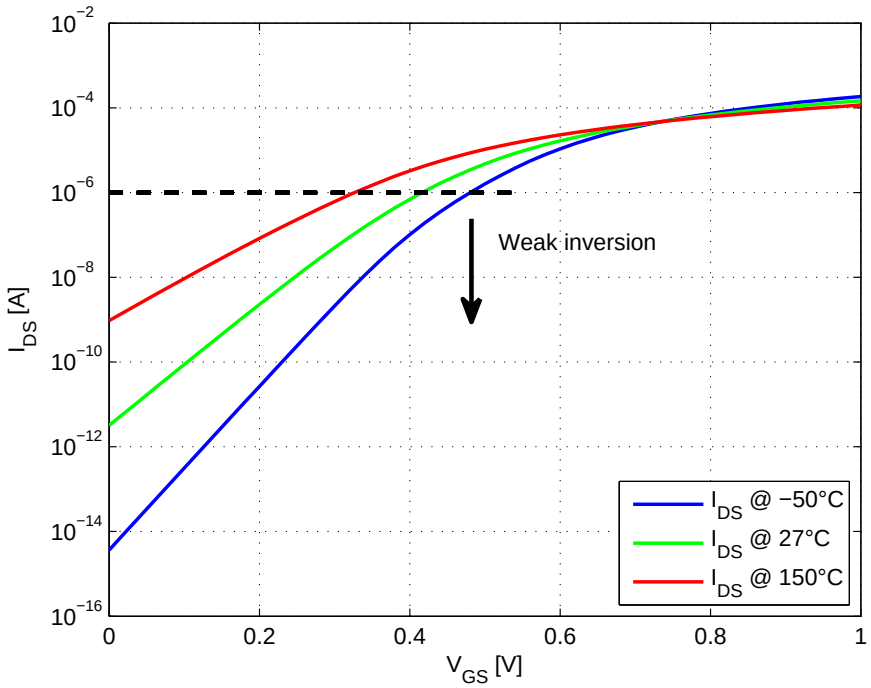


Figure 3.1: Transfer characteristic of an NMOS with $W/L = 5u/1u$, $V_{BS} = 0$, $V_{DS} = 1V$ at different temperatures

Figure 3.1 shows the transfer characteristic of an NMOS transistor at different temperatures. The I_{DS} is exponentially dependent on the V_{GS} in weak inversion. For a fixed V_{GS} the I_{DS} is larger for higher temperatures in weak inversion due to smaller threshold voltage and U_T. The slope of the curves in weak inversion is larger at low temperature due to the temperature dependent U_T in the denominator of the exponential function of equation 3.1. In strong inversion, the temperature dependency of the mobility (equation 3.8) is dominant [18].

3.3 Inversion coefficient (IC)

A good indicator for the mode of operation for a transistor is the inversion coefficient as stated in equation 3.7 from [17].

$$IC = \frac{I_{DS}}{I_0(T) \cdot \left(\frac{W}{L}\right)} \tag{3.7}$$

At an $IC \lesssim 0.1$ the transistor is operating in weak inversion. Moderate inversion is defined in the range of $0.1 \lesssim IC \lesssim 10$ and strong inversion at $IC \gtrsim 10$. Setting the $IC \approx 0.1$ and the $W/L = 5$ and $I_0(T) = 1.6\mu A$ at 27°C of the NMOS from figure 3.1 in equation 3.7, the transistor operates in weak inversion when biased with a current of $I_{DS} \lesssim 800nA$.

In SPICE models, the mobility (μ) reduction due to temperature is modeled as in equation 3.8 with a nonlinear temperature coefficient BEX. BEX is a process dependent parameter of approximately -1.5. As the $I_0(T)$ is temperature dependent due to $U_T^2(T)$ and $\mu_0(T)$ (equation 3.8), $I_0(T)$ is directly proportional to $T^{-(BEX+2)}$ [17, p.59].

$$\mu(T) = \mu_0 \, (T)^{BEX} \tag{3.8}$$

If the transistor is biased with a temperature constant current of I_{DS}, then the inversion coefficient is proportional to approximately $T^{-0.5}$. When the transistor is biased with a proportional to absolute temperature (PTAT) current (chapter 3.7.2), then IC is proportional to $T^{0.5}$. This results in a slight dependency on the operating mode due to the temperature, depending on the bias current of the transistor.

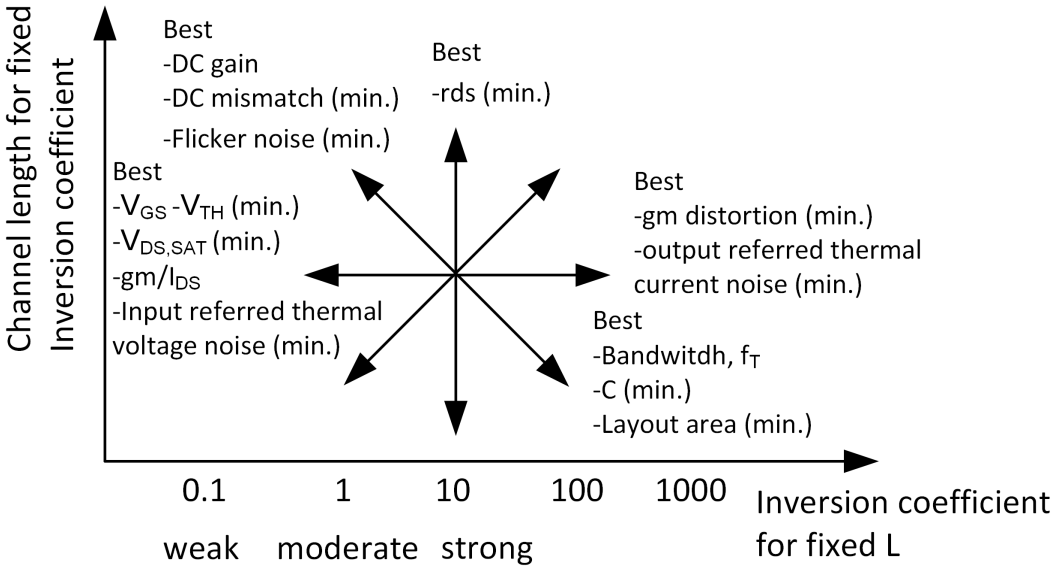


Figure 3.2: Performance paramters over IC and channel length [17]

In [17] a design method for moderate and weak inversion is given. It is mainly based on the IC. Figure 3.2 shows several performance parameters of a MOS over the IC and L for a fixed bias current of a transistor.

3.4 Models for MOS transistors operated in weak inversion

3.4.1 EKV model

The EKV model named after their inventors Enz, Krummenacher and Vittoz was developed for low power designs [13] [17]. This model is charge based and accurate for all modes of operation from weak to strong inversion. The current transfer function is modeled by equation 3.9 (simplified version) from [14].

$$I_{DS} = I_0 \cdot ln^2 \left(1 + e^{\frac{V_{GS}-V_{TH}}{2\eta U_T}}\right) \tag{3.9}$$

Putting this equation in the IC equation 3.7 the inversion coefficient can be calculated by the source voltage of equation 3.10 [17].

$$IC = (W/L)^{-1} \cdot ln^2 \left(1 + e^{\frac{V_{GS}-V_{TH}}{2\eta U_T}}\right) \tag{3.10}$$

3.4.2 BSIM model

As the BSIM3 and BSIM4 is a threshold-based model, where weak inversion compared to strong inversion is modeled with different equations. The transition between those regimes (moderate inversion) is modeled by curve fitting. The behavior of this model and many parameters is detached from the physical background.

3.4.3 Model validity

The simulated, model based performance of circuits operating in the weak inversion often deviate from the real performance of the circuit. Inaccuracies of models can be the root cause for this behavior. Model parameters influencing the behavior in this operating regime are often not accurately extracted because it is difficult to measure such small currents for a device biased in weak inversion. For most circuits or applications, the performance in weak inversion is less important. Other leakage currents like: gate induced drain leakages (GIDL), gate to channel leakage and reversed biased diode leakage from source and bulk to drain tend to be negligible in subthreshold region [14].

3.5 Small signal domain for weak inversion saturation

3.5.1 Saturation - active region

To ensure that the transistor is the active region, such that I_{DS} is almost independent of V_{DS}, V_{DS} has to be large enough that the $1 - e^{\frac{V_{DS}}{U_T}}$ term of equation 3.1 is close to one leads to equation 3.11. A $V_{DS,SAT} \gtrsim 4 \cdot U_T$ is a good approximation for saturation [14]. The small signal output conductance is the derivative of equation 3.1 with respect to V_{DS} as stated in equation 3.12. With increasing V_{DS}, g_{DS} approaches zero. There is also the drain induced barrier lowering (DIBL) effect, which increases the output resistance proportional to the length of the transistor as discussed in section 3.5.3.

$$I_{DS} \approx I_0 \cdot e^{\frac{V_{GS}-V_{TH}}{\eta U_T}}; \qquad for\ V_{DS,SAT} \gtrsim 4 \cdot U_T \tag{3.11}$$

$$g_{DS} = \frac{dI_{DS}}{dVds} = \frac{I_0}{U_T} \cdot e^{\frac{V_{GS}-V_{TH}}{\eta U_T}} \cdot e^{\frac{-V_{DS}}{U_T}} \tag{3.12}$$

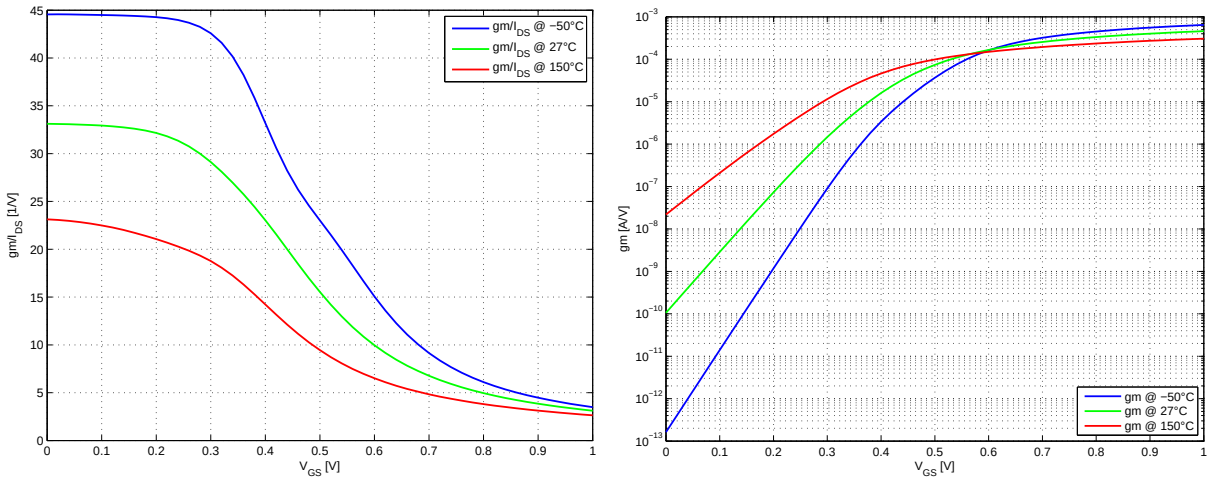
3.5.2 Transconductance (gm)

gm for the weak inversion active region is stated in equation 3.13. With a higher temperature, the transconductance decreases at a constant bias current, because U_T increases. η has also a small positive temperature coefficient [14], which is negligible in most cases.

$$gm = \frac{dI_{DS}}{dV_{GS}} = I_0 \cdot \frac{W}{L} \cdot e^{\frac{V_G-V_s}{\eta U_T}} \cdot [1 - e^{-\frac{V_{DS}}{U_T}}] \cdot \frac{1}{\eta U_T} = \frac{I_{DS}}{\eta U_T} \tag{3.13}$$

$$\frac{gm}{I_{DS}} = \frac{1}{\eta U_T} \tag{3.14}$$

According to equation 3.14, $\frac{gm}{I_{DS}}$ stays constant in weak inversion for a fixed temperature, which is shown in figure 3.3(a) on the left side. For T = -50°C and $\eta \approx 1.2$, $\frac{gm}{I_D}$ is approximately 43, for T= 150°C the ratio is approximately 23, which fits quite well to the simulated curves of figure 3.3(a) left side. On the right side of figure 3.3(a) the quadratic relation between $\frac{gm}{I_{DS}}$ and V_{GS} for strong inversion is shown. Figure 3.3(b) shows gm as function of V_{GS}, which is an exponential function in weak inversion.



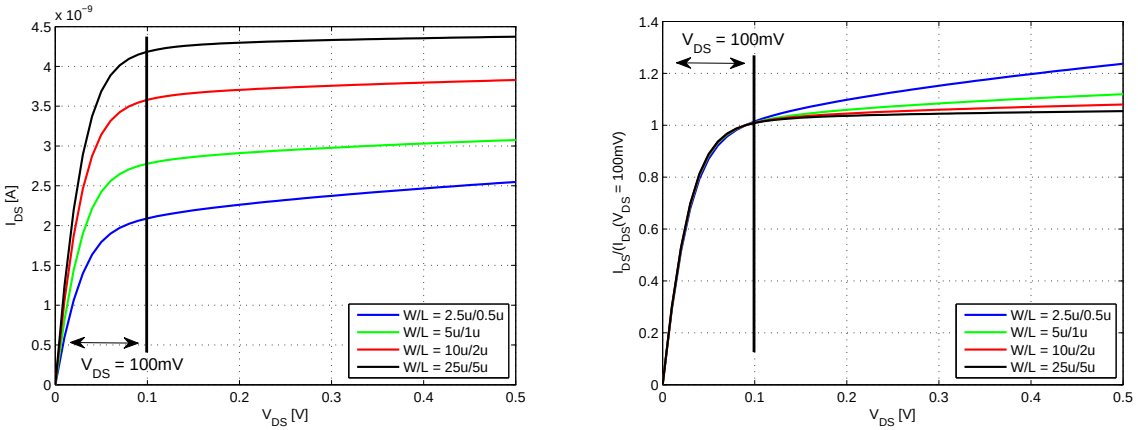
(a) gm/I_{DS} as function of V_{GS}

(b) gm as function of V_{GS}

Figure 3.3: gm graphs for NMOS with $W/L = 5\mu m/1\mu m$, $V_{BS} = 0$, $V_{DS} = 1V$ at different temperatures

3.5.3 Output conductance (gds)

In strong inversion, the output conductance is increased by channel length modulation (CML) [15]. In weak inversion, DIBL is the most important short channel effect that lowers the output resistance of a short channel MOS [14] [17]. When V_{DS} increases, V_{TH} decreases, which leads to an increased current. Figure 3.4(a) shows the simulated output characteristic of different NMOS with fixed $W/L = 5$ in weak inversion ($V_{GS} = 200mV,\ V_{TH} \approx 427mV - 447mV$).



(a) Output current with $V_{GS} = 200mV$

(b) Normalized output current

Figure 3.4: Output current characteristic with constant $W/L = 5$

For small length, the g_{DS} in saturation ($V_{DS} > 4 \cdot U_T$) is large (gradient of the current to V_{DS}). The output conductance decreases with increasing L. The different geometries of the devices influence the V_{TH}, which leads to a different current due to a fixed V_{GS}. Figure 3.4(b) show the normalized output current $\left(\frac{I_{DS}(V_{DS})}{I_{DS}(V_{DS}=100mV)}\right)$ to the current at $V_{DS} = 0.1V$. g_{DS} is directly proportional to the current in weak inversion as stated in [14].

The output conductance is modeled with the $DVTDIBL \approx 0.008 - 0.012V/V$ and the $DVTDIBLEXP \approx 3$ (SPICE level 3) parameter of equation 3.15 from [17]. This effect is proportional to the inverse channel length of the transistor.

$$g_{ds} \approx gm \cdot \left(-DVTDIBL \cdot \left(\frac{L_{min}}{L}\right)^{DVTDIBLEXP}\right) \tag{3.15}$$

3.6 Back gate effect

With a bulk-source voltage (V_{BS}), the back gate effect adds an additional term to the equation 3.11, which leads to equation 3.16 from [13] or [19] for the active region in weak inversion. The small signal back gate transconductance (gmb) for weak inversion is stated in equation 3.17 from [17]. The effect of gmb on the noise is discussed in chapter 3.9.2.

$$I_{DS} \approx I_0 \cdot e^{\frac{V_{GS}-V_{TH0}}{\eta U_T}} \cdot e^{(\eta-1)\frac{V_{BS}}{\eta U_T}} \tag{3.16}$$

$$gmb \approx gm \cdot (\eta - 1) \tag{3.17}$$

In strong inversion, the back gate effect is modeled by shifting the threshold voltage [17] [18].

3.7 Temperature effects

3.7.1 Threshold voltage

The temperature dependence of the threshold voltage is mostly due to the drift of the Fermi potential (ϕ_F) and the drift of the carrier density. Equation 3.18 is derived by [14] where V_{G0} is the extrapolated bandgap voltage.

$$\frac{dV_{TH}}{dT} = \frac{\eta - 0.5}{T} \cdot (\phi_F - V_{G0}) \approx -2.5\frac{mV}{K} ... \ -1\frac{mV}{K} \tag{3.18}$$

$$V_{TH}(T) = V_{TH0} + TCV \cdot (T - T_0) \tag{3.19}$$

This can also be modeled using equation 3.19 where TCV is -1mV/K ... -2.5mV/K and V_{TH0} the threshold voltage at T_0.

3.7.2 Constant gm biasing

The temperature dependence of a bias current ($I_{DS}(T)$) can be denoted by a temperature coefficient (TC in equation 3.20). To get a temperature constant gm, the derivative of the transconductance with respect to temperature can be set to zero as in equation 3.21. A current with the temperature coefficient as U_T is called PTAT current. By biasing the transistor with a PTAT current, gm stays constant. A PTAT current can easily be generated with a current reference described in chapter 3.10.3.

$$I_{DS}(T) = I_{D0} \cdot (1 + TC \cdot (T - T_0) \tag{3.20}$$

$$gm(T) = \frac{I_{DS}(T)}{\eta U_T(T)} = \frac{I_{D0} \cdot (1 + TC \cdot (T - T_0))}{\eta k_B T/q}$$

$$\frac{dgm}{dT} = \frac{(k_B T/q) \cdot I_{D0} \cdot TC - I_{D0} \cdot (1 + TC \cdot (T - T_0)) \cdot k_B/q}{(\eta k_B T/q)^2} \stackrel{!}{=} 0 \tag{3.21}$$

$$T \cdot TC = (1 + TC \cdot (T - T_0))$$

$$TC = \frac{1}{T0} \approx \frac{1}{300K} @ 27°C \approx 3.33 \cdot 10^{-3}\frac{1}{K} \tag{3.22}$$

In the thesis the reference temperature $T_0 = 300K$ is used, leading to a TC for constant gm stated in equation 3.22. The constant gm is important for a temperature constant bandwidth in the gain stages of the limiting amplifier. The bandwidth (f_{-3dB}) of a single transistor is stated in equation 3.23. For an approximately constant capacitance over temperature ($C_{GS} + C_{GD}$), the bandwidth will stay constant for a constant gm over temperature.

$$f_{-3dB} \approx \frac{gm}{2\pi(C_{GS} + C_{GD})} \tag{3.23}$$

3.7.3 Saturation Voltage

In weak inversion, a MOS transistor has the smallest saturation voltage ($V_{DS,SAT}$) [17], so it is suitable for low voltage designs. In strong inversion, the $V_{DS,SAT}$ must be greater than the overdrive voltage. If the saturation voltage is exceeded, the transistor is in the active region and acts as voltage controlled current source with a certain output resistance. For T = -50°C and 150°C the temperature voltage ranges between 19mV and 36mV. The saturation voltage with $V_{DS,SAT} \approx 4 \cdot U_T$ is between $V_{DS,SAT} \approx 80mV - 150mV$.

3.8 Mismatch

Identical structures with the same layout on a real chip do not have exactly the same characteristics due to small differences in physical parameters. The physical variations can be summarized in V_{TH}, η and $\beta = \mu \cdot C_{OX} \cdot \frac{W}{L}$. The dominant factor for mismatch is the variation of V_{TH}. The deviation of β and η is negligible in most cases [14].

The current matching of a current mirror is derived in [14]. The current mismatch normalized to the bias current is stated in equation 3.24.

$$\begin{aligned}\frac{\sigma(\Delta I_{DS})}{I_{DS}} &= \sqrt{\sigma^2(\Delta\beta) + \left(\frac{gm}{I_{DS}} \cdot \sigma(\Delta V_{TH})\right)^2} = \sqrt{\sigma^2(\Delta\beta) + \left(\frac{1}{\eta U_T} \cdot \sigma(\Delta V_{TH})\right)^2} \\ &\approx \frac{gm}{I_{DS}} \cdot \sigma(\Delta V_{TH}) \end{aligned} \tag{3.24}$$

The gate source voltage mismatch is stated in equation 3.25 from [14].

$$\begin{aligned}\sigma(\Delta V_{GS}) &= \sqrt{\sigma^2(\Delta V_{TH}) + \left(\frac{I_D}{gm} \cdot \frac{\sigma(\Delta\beta)}{\beta}\right)^2} = \sqrt{\sigma^2(\Delta V_{TH}) + \left(\eta U_T \cdot \frac{\sigma(\Delta\beta)}{\beta}\right)^2} \\ &\approx \sigma(\Delta V_{TH}) \end{aligned} \tag{3.25}$$

Weak inversion is thus not appropriate when current matching is required for example in current mirrors, but it can be beneficial for voltage matching in a differential pair, for example, if $\sigma(\Delta\beta)$ has a significant impact on the mismatch [20]. The offset of a differential pair can be reduced to a minimum value dominated by the threshold voltage mismatch ($\sigma(\Delta V_{TH})$) as in equation 3.25.

In the process manual the mismatch constant A_{VTH} and A_β of a NMOS and PMOS transistor can be found. $\sigma^2(\Delta V_{TH})$ of a transistor is indirectly proportional to the area of the transistor as stated in equation 3.26. In most cases the mismatch constant of a PMOS transistor is slightly higher, compared to a NMOS transistor [17]. The magnitude of A_{VTH} and A_β depends on the process and in most processes A_β is at least smaller than half of the A_{VTH} [17]. This leads to negligible $\sigma(\Delta\beta)$.

$$\sigma(\Delta V_{TH}) = \frac{A_{VTH}}{\sqrt{WL}}; \qquad \frac{\sigma(\Delta\beta)}{\beta} = \frac{A_\beta}{\beta\sqrt{WL}} \tag{3.26}$$

3.9 Noise in weak inversion

The noise of a transistor can be modeled with the equivalent circuit diagram shown in figure 3.5. The output referred noise ($S_{out}(f)$ of equation 2.18) or the input referred noise ($S_{in}(f)$ of equation 2.19) are power spectral densities. This power spectral density can be a squared voltage noise density ($S_{U^2}(f)$) or a squared current noise density ($S_{I^2}(f)$).

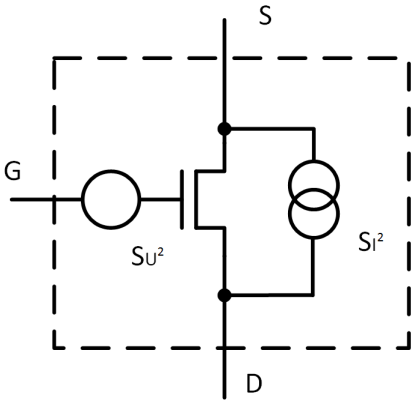


Figure 3.5: Simple noise model for a transistor

The power spectral density of the noise for a transistor in saturation can be transformed from a current source at the output (S_{I^2}) to a voltage source at the input (S_{U^2}) by equation 3.27.

$$S_{U^2} \approx \frac{S_{I^2}}{gm^2} \tag{3.27}$$

The power spectral density of the noise can either be a current source S_{I^2} in parallel to the channel or a voltage source S_{U^2} at the gate (gate referred voltage noise).

The noise for a transistor in weak inversion saturation consists mainly of two parts like for a transistor in strong inversion saturation: **flicker noise** and **channel noise**.

3.9.1 Flicker noise

Flicker noise or so-called $\frac{1}{f}$-noise can be modeled by equation 3.28 (carrier density fluctuation model) from [14] [15] [17] [21]. This model is also referred as McWorther model and it is independent of the inversion or the operating point. K_F is a process and device dependent parameter. For SPICE models $K_{F,SPICE}$ is often given, which results in differences to equation 3.28 ($K_F = K_{F,SPICE} \cdot C_{OX}$). The α-parameter is in the range of 0.7-1.2 [17].

$$\frac{S_{U^2,F}(f)}{df} = \frac{K_F}{C_{OX}^2 \cdot WL \cdot f^{\alpha}} \tag{3.28}$$

A larger area is the main factor to minimize the 1/f noise. Typically PMOS transistors have a smaller K_F-parameter than NMOS. The Hooge model (carrier mobility fluctuation) is another model for flicker noise that takes the operation point into account. An additional term can be modeled slightly dependent on the operating point as in the BSIM model [16]. This model and measurements in [17] show that flicker noise increases with increasing inversion coefficient.

3.9.2 Channel noise

Channel noise in a MOS is caused by **thermal noise** for a transistor operating in strong inversion or **shot noise** dominating when the transistor is operating in weak inversion [17]. Shot noise is white noise and can be modeled by a current noise power density as in equation 3.29 [14] [22].

$$\frac{S_{I^2,C}}{df} = 2qI_{DS} \tag{3.29}$$

Frequency independent white noise density due to channel noise is stated in equation 3.30 for squared current noise density or in equation 3.31 for squared voltage noise density [17] [21] [22].

$$\frac{S_{I^2,C}}{df} = 4k_BT \cdot (gm + gmbs) \cdot \gamma = 4k_BT \cdot gm \cdot \eta \cdot \gamma \tag{3.30}$$

$$\frac{S_{U^2,C}}{df} = \frac{S_{I^2}}{gm^2} = \frac{4k_BTgm \cdot \eta \cdot \gamma}{gm^2} = \frac{4k_BT \cdot \eta \cdot \gamma}{gm} \tag{3.31}$$

The γ-factor is the thermal noise coefficient, which is bias dependent. The parameter has the values: $\gamma \approx 2/3$ for strong inversion, $\gamma \approx 1/2$ for weak inversion, and $\gamma = 1$ for linear conduction. With $\gamma \approx 1/2$, the thermal noise density resolves to equation 3.32 and 3.29 in weak inversion. This is valid for long channel devices with $V_{BS} \approx 0V$ and moderate doping [17].

$$\frac{S_{U^2,C}}{df} = \frac{2qk_B^2T^2\eta^2}{I_{DS}} \tag{3.32}$$

There are also other noise sources, for example, gate or bulk resistance which are negligible in most cases [23]. To scale the gate referred channel noise in weak inversion, the only parameter is gm, which is set by the current of the transistor. If the transistor has a temperature constant gm over temperature ratio (chapter 3.7.2), the input referred noise is directly proportional to the temperature. PMOS compared to NMOS have a slightly higher substrate factor, which leads to a lower gm and a larger gate referred input noise density.

The **BSIM4** models thermal noise with equation 3.33 [16]. This equation takes also more parameters of the operation point by the channel charge Q_{inv} into account.

$$\frac{S_{I^2,C}}{df} = \frac{4k_BT}{R_{ds} + \frac{Leff^2}{\mu_{eff}|Q_{inv}|}} \cdot NTNOI \tag{3.33}$$

$$Q_{inv} = W_{active}L_{active}C_{oxeff}NF\left[V_{gseff} - \frac{A_{bulk}V_{dseff}}{2} + \frac{A_{bulk}^2V_{dseff}^2}{12 \cdot (V_{gsteff} - \frac{A_{bulk} \cdot V_{dseff}}{2})}\right]$$

Short channel effects for white noise

There are different theories (e.g. hot carrier, mobility reduction, or velocity saturation) for excess noise summarized in [22] for short channel devices. These theories try to explain increased white noise in short channel transistors compared to long channel transistors. For short channel devices the NTNOI of the BSIM or the γ parameter is increased from 1 to 2-3 depending on the V_{DS}.

3.9.3 Overall noise power density

The overall noise power spectral density is the sum of the flicker- and of the channel noise power spectral density of the transistor. As none of the noise sources are correlated, the power densities have to be summed up as stated in equation 3.34. Non-correlated white noise sources (equation 3.35) and Non-correlated flicker noise sources also have to be summed up, respectively (equation 3.36).

$$S_{U^2} = S_{U^2,C} + S_{U^2,F} \tag{3.34}$$

$$S_{U^2,C} = S_{U^2,C1} + S_{U^2,C2} + ... + S_{U^2,Cn} \tag{3.35}$$

$$S_{U^2,F} = S_{U^2,F1} + S_{U^2,F2} + ... + S_{U^2,Fn} \tag{3.36}$$

3.9.4 Basic circuit examples for white noise power density

White noise differential pair

As in [15] the squared output voltage white noise density ($S_{U^2,C,O}$) of a differential pair with a resistor R_D as load can be expressed by equation 3.37. While η is included in equation 3.37, it is not considered in [15]. The output noise can be transformed into the input noise by dividing through the squared gain ($gm^2 \cdot R_D^2$) leading to equation 3.38.

$$\frac{S_{U^2,O}}{df} = 2 \cdot I_n^2 \cdot R_D^2 + 2 \cdot U_n^2(R_D) = 8kT \cdot (\gamma gm\eta \cdot R_D^2 + R_D) \tag{3.37}$$

$$\frac{S_{U^2,I}}{df} = 8kT \cdot \left(\frac{\gamma\eta}{gm} + \frac{1}{gm^2 \cdot R_D}\right) \tag{3.38}$$

White noise current mirror

The squared current white noise density ($S^2_{I,M1+M2}$) of a current mirror with a scaling factor of 1:B is stated in equation 3.41. The current of M2 is the multiplied current of M1 by B. The noise density is composed of the noise from the two transistors ($S^2_{I,M1}$ and $S^2_{I,M2}$) with gm1 and gm2.

$$\frac{S_{I^2,M1}}{df} = 4k_BT\gamma\eta gm1 = \frac{4k_BT\gamma\eta gm2}{B} \tag{3.39}$$

$$\frac{S_{I^2,M2}}{df} = 4k_BT\gamma\eta gm2 = 4k_BT\gamma\eta gm1 \cdot B \tag{3.40}$$

$$\begin{aligned}\frac{S_{I^2,M1+M2}}{df} &= I^2_{n,1}(f) \cdot B^2 + I^2_{n,2}(f) = 4k_BT\gamma\eta gm1 \cdot B^2 + 4k_BT\gamma\eta gm1 \cdot B \\ &= 4k_BT\gamma\eta gm1 \cdot B^2 \left(1 + \frac{1}{B}\right) = 4k_BT\gamma\eta gm2 \cdot (B+1)\end{aligned} \tag{3.41}$$

For a low current noise, gm1 and gm2 should be low. This low current noise can be reached by operating the transistors with a low IC, which is also beneficial for current matching of the mirror. Also the input current should be higher than the output current for a low current noise density. This increased input current can be reached by a low scaling factor B.

3.10 Basic circuitry weak inversion

3.10.1 Differential pair

The difference of the current ($\Delta I = I_1 - I_2$) of a differential pair in weak inversion is stated in equation 3.46 [14]. The derivation assumes an input differential voltage V_{ID} as the difference of the input voltages (equation 3.42).

$$V_{ID} = V_{INP} - V_{INN} \tag{3.42}$$

$$\frac{I_1}{I_2} = e^{\frac{V_{INP}-V_{INN}}{\eta U_T}} = e^{\frac{V_{ID}}{\eta U_T}} \tag{3.43}$$

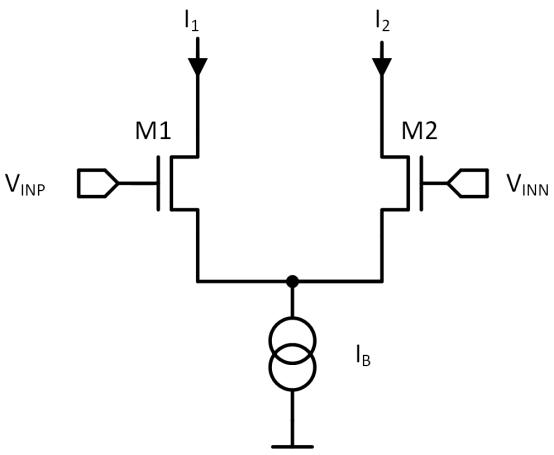
$$I_B = I_1 + I_2;\ I_2 = \frac{I_B}{1 + e^{\frac{V_{ID}}{\eta U_T}}} \tag{3.44}$$

$$\Delta I = I_1 - I_2 = \frac{I_B}{1 + e^{\frac{-V_{ID}}{\eta U_T}}} - \frac{I_B}{1 + e^{\frac{V_{ID}}{\eta U_T}}} \tag{3.45}$$

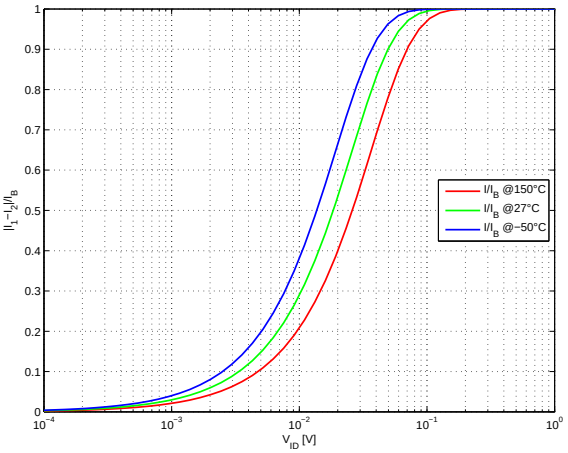
$$\Delta I = I_1 - I_2 = I_B \cdot tanh\left(\frac{V_{ID}}{2\eta U_T}\right) \tag{3.46}$$

With an input signal of $V_{ID} = 2\eta U_T \cdot arctanh(\frac{0.99 \cdot I_B}{I_B}) \approx 5.3 \cdot \eta U_T$, almost all (99%) of the bias current (I_B) flows over a single branch. The value $V_{ID} \approx 5.3 \cdot \eta U_T$ is referred to the clipping voltage V_S of differential pair based transconductance rectifier (chapter 5.1.1 on page 63).

In figure 3.6(b) ΔI over V_{ID} at different temperatures and logarithmic x-axis is shown. At a constant V_{ID}, ΔI is lower at higher temperatures.



(a) Differential pair with no load



(b) $\Delta I/I_B$ of a differential pair in weak inversion for different temperatures

Figure 3.6: Differential pair in weak inversion

gm is the partial derivative of the output current to the input voltage. The small signal gm of the differential pair is temperature constant if it is biased with a PTAT current.

$$gm = \frac{d(I_1 - I_2)}{dV_{ID}} = \frac{I_B}{2\eta U_T} \frac{1}{cosh\left(\frac{V_{ID}}{2\eta U_T}\right)^2} \tag{3.47}$$

3.10.2 Didode connected load operating in weak inversion

A diode connected load operating in weak inversion has the small signal conductance of equation 3.48. Because gds is dependent on $V_{DS} = V_{GS}$, this voltage has to be large enough that the transistor stays in saturation and gds is small enough for this approximation.

$$g = gm + gds \approx gm \tag{3.48}$$

For a transistor operating in weak inversion, V_{DS} has to be at least $V_{DS,sat} \gtrsim 4 \cdot U_T$ to stay saturated. For 150°C and the fast process corner, V_{GS} can get lower than $4 \cdot U_T$ and the transistor does not remain saturated.

For the further design, thick oxide transistors with high threshold voltage are used. This leads to an higher V_{GS} for a given current, hence a diode is more likely to stay in saturation for fast process corner and T= 150°C. Even with high threshold voltage transistors, a diode connected load operating deeply in week inversion (low IC) does not stay saturated at 150°C fast.

Two possible approaches shown in figure 3.7 can be used to solve this problem.

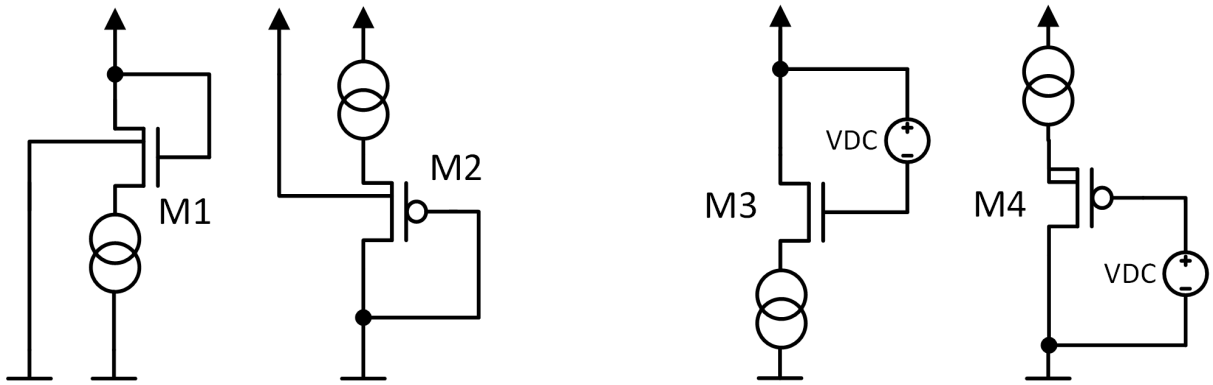


Figure 3.7: Possible approaches for saturated diode connected loads

Additional voltage between gate and bulk

On the left-hand side of figure 3.7, the bulk is connected to V_{DD} for a PMOS (M2) and V_{SS} for a NMOS (M1) diode connected load. The source voltage and an additional V_{BS} shifts the threshold voltage (equation 3.49) as described in [18]. With higher threshold voltage, also V_{GS} is increased if the MOS is biased with a fixed current. Or according to equation 3.16, V_{GS} is increased with additional V_{BS} for a constant current.

$$V_{TH}(V_{BS}) = V_{TH0} + \gamma(\sqrt{|2\Phi_F - V_{BS}|} - \sqrt{2\Phi_F}) \tag{3.49}$$

Furthermore, with additional V_{BS}, gmb of the diode is added to the the small signal output conductance of the diode (equation 3.50).

$$g = gm + gds + gmbs \approx gm + gmbs \approx \eta \cdot gm \tag{3.50}$$

Additional voltage between gate and drain

The right-hand side of figure 3.7 shows another possibility to solve the saturation problem. An additional DC voltage between gate and drain, increases the gate potential for a PMOS (M4), which leads to an higher source voltage for a fixed bias current. Thus V_{DS} is increased and the diode is more likely to stay saturated at 150°C and fast process corner. The same approach can be used for a NMOS (M3) transistor.

3.10.3 Constant gm cell

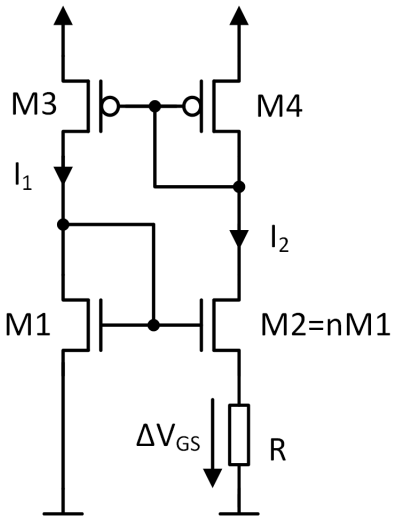
A simple circuit from [24] for extracts a PTAT current if the transistors operate in weak inversion. Figure 3.8 shows the schematic and transfer function of a constant gm cell. There are two current mirrors (M1-M2 and M3-M4). The current mirror of M3-M4 has a stable operating point if $I_1 = I_2$ (blue curve, figure 3.8(b)). The second current mirror has a scaling of $M2 = n \cdot M1$. $M2$ has a source degenerating temperature constant resistance R. M1-M2 and R have the current transfer function of the green curve. The intersection of the two functions is the stable operating point of the circuit. Solving equation 3.16 and equation 3.16 for V_{GS1} and V_{GS2} leads to $\Delta V_{GS} = V_{GS1} - V_{GS2}$ over the resistor of equation 3.51.

$$\Delta V_{GS} = \eta U_T \cdot ln(I_1/I_{01}) + V_{TH1} - \eta U_T \cdot ln(I_2/I_{02}) - V_{TH2} - (\eta - 1)\Delta V_{GS} \tag{3.51}$$

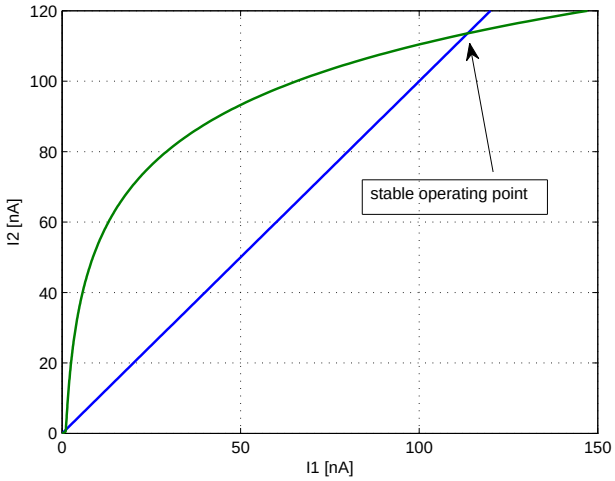
$$\approx U_T \cdot ln(n \cdot I_1/I_2) \tag{3.52}$$

$$I_2 = I_1 = \frac{\Delta V_{GS}}{R} = \frac{U_T}{R} \cdot ln(nI_1/I_2) \tag{3.53}$$

With $I_{02} = n \cdot I_{01}$ and $V_{TH1} \approx V_{TH2}$ the equation of ΔV_{GS} can be simplified to equation 3.52. This leads to the current of equation 3.53. The circuit is self-starting if the leakage of M2 is larger than that of M1 such that the loop gain is greater than one [24].



(a) Constant gm cell



(b) Transfer functions of the current mirrors M1-M2 (green), M3-M4 (blue)

Figure 3.8: Constant gm current generation

The accuracy of the cell is mainly dependent on the temperature constant resistor [9] but can be improved through different methods. The constant gm current cell has already be designed for the chip with some improvements to reach a higher accuracy. The output current is trimmed to 10nA. The current of the constant gm cell (equation 3.54) has a temperature coefficient of $TC_{PTAT} = 3300 ppm/K$ for T0 = 27°C . Due to mismatch, the TC has a standard deviation of $\sigma(TC) \approx 100\ ppm/K$.

$$I_{PTAT} = I_0 \cdot (1 + TC_{PTAT} \cdot (T - T_0)) \tag{3.54}$$

On chip and for the design there is also a bandgap current with a nominal TC of -30ppm/K. Ideal current sources with the respective TC and $\sigma = 100\ ppm/K$ are used for simulation.

4 Gain stage circuits

4.1 Introduction to gain stage circuits

The main challenge of the gain stage design is to establish a gain that is PVT stable at given power, bandwidth, and noise specifications. For comparison of different gain stage circuits the same performance parameters of each stage, explained in subsection 4.1.2 - 4.1.5 are considered. The investigations on different single gain stages are presented in the following chapters (4.2 - 4.8). In table 4.1 on page 62 the parameters of the single gain stages are summarized. The investigations for different rectifiers are presented in chapter 5 beginning on page 63. The results are used to predict the behavior of the limiting amplifier composed of gain stages and rectifiers. The implementation of the limiting amplifier is shown in chapter 7.

4.1.1 Testbench

Monte Carlo simulation of several cascaded amplifiers as in a limiting amplifier cannot be done without an offset cancellation block because an offset voltage will most likely drive the last gain stages into saturation. The offset cancellation block has an influence on different parameters of the limiting amplifier. This block has to be implemented and optimized in a different way for different gain stages. So it is more reasonable to simulate the single gain stages first and then use the results to predict the behavior of the entire limiting amplifier.

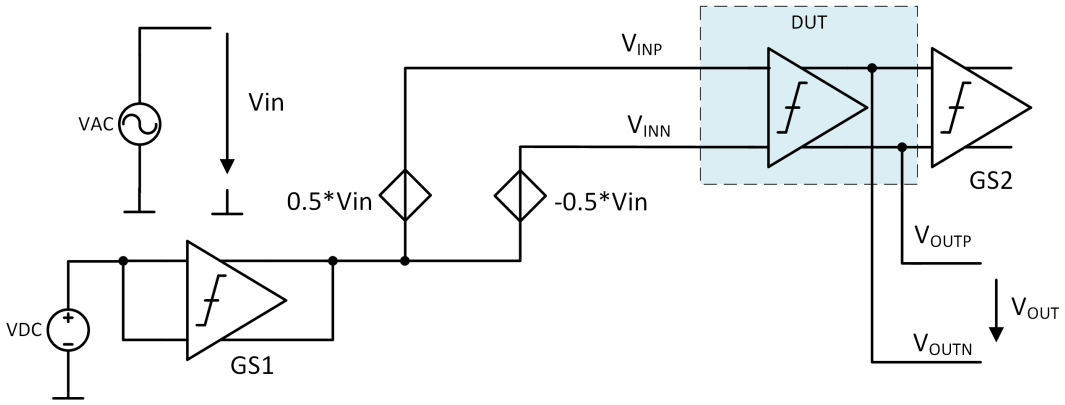


Figure 4.1: Schematic for testbench for a single gain stage

Figure 4.1 shows the test bench for a single gain stage (device under test DUT). One gain stage (GS1) is for the common mode voltage of the previous stage. The input of GS1 is connected to VDC. For a PMOS (as shown in figure 4.1) the voltage is $VDC = 0V$ (ground), for an NMOS differential input pair the voltage is $VDC = VDD$ (supply voltage). The second stage (GS2) is the capacitive load of the DUT gain stage. The in- and output voltages are fully differential voltages.

4.1.2 Small signal gain variation

Small signal or AC gain (A_s) variation due to mismatch of a single gain stage is evaluated at a frequency of 125kHz with a Monte Carlo simulation and a process corner variation over the temperature range from -50°C to 150°C. The AC gain is fixed to approximately $A_s \approx 2$ at 27°C and the nom process corner. The gain stages are all biased with an ideal PTAT bias current ($I_B = 40nA,\ TC_{IB} = 3300ppm/K,\ \sigma(TC_{IB}) = 100ppm/K$) to compare also bandwidth and noise for fixed power consumption. In this chapter non integer current ratios for biasing the gain stage and loads are used, which are generated with ideal current sources.

Gain drift over temperature

The most important parameter is the gain drift over temperature, which is in most cases different for different process corners. The first dimensioning is used to optimize for a minimal gain drift over the given temperature range at all process corners. The maximum normalized gain difference over temperature (ΔA_s) is calculated by equation 4.1. The ΔA_s-parameter is used for comparing a linear and also nonlinear TC of the gain for different gain stages. A linear TC of the gain can be calculated by equiuation 4.2.

$$\Delta A_s = \frac{max(A_s(T)) - min(A_s(T))}{A_s(T = 27°C)} \cdot 100\% \tag{4.1}$$

$$TC(A_s) = \frac{\frac{A_s(T)}{A_s(T=27°C)} - 1}{T - T_0} \tag{4.2}$$

$TC(A_s)$ of the gain has influence on the TC of the RSSI. A limiting amplifier, for example, composed of two gain stages with the same gain ($A_s = A_{s1} = A_{s2}$) and a TC of $TC_1 = TC_2$, the limiter gain as function of temperature is stated in equation 4.3.

$$\begin{aligned} A_{limiter}(T) &= A_{s1}(T) \cdot A_{s2}(T) = A_{s10}(1 + TC_1(T - T_0))A_{s20}(1 + TC_2(T - T_0)) \\ &= A_{s0}^2(1 + TC(T - T_0))^2 = A_{s0}^2(1 + 2TC(T - T_0) + TC^2(T - T_0)^2) \end{aligned} \tag{4.3}$$

$$A_{limiter}(T) \approx A_{s0}^N \cdot (1 + N \cdot TC(T - T_0)) = A_{s0}^N \cdot (1 + TC_{limiter}(T - T_0)) \tag{4.4}$$

$$TC_{limiter} \approx N \cdot TC \tag{4.5}$$

A quadratic term ($TC^2(T - T_0)^2$)) is introduced. This nonlinear term can be neglected if the TC is sufficiently small and $TC^2(T - T_0)^2 \approx 0$ is valid. The linear $TC_{limiter}$ for N stages of the limiter is approximately N times the TC of the single stage (equation 4.5).

The goal of the dimensioning is to minimize the temperature coefficient of a single gain stage, which minimizes the overall temperature coefficient of the limiting amplifier gain and the TC of the RSSI.

Absolute gain variation

The variation of gain due to mismatch and process variations is important for the lowest signal level, which has to be detected in the datagram mode. If the gain of the limiting amplifier decreases below the noise level, then the signal will not be detected. This can be avoided if the limiter has a higher gain than the minimum gain, which is needed for the lowest signal level to be detected. Thus this parameter is not as important as the temperature stability of the gain. A Monte Carlo simulation of 1000 runs at the temperatures of -50°C, 27°C and 150°C is performed. The probability distribution of the gain is approximated with a normal Gaussian distribution. The mean value ($\mu(A_s)$) of the gain, the standard deviation ($\sigma(A_s)$), and the relative standard deviation $\left(\frac{\sigma(A_s)}{\mu(A_s)}\right)$ are calculated. Also the minimum and maximum gain ($A_{s,min}$ and $A_{s,max}$) of the Monte Carlo simulation for different gain stages are shown in the table 4.1.

4.1.3 -3dB Bandwidth

With a given bias current of $I_B = 40nA$, the low-pass bandwidth of a single stage (BW_s) has to be at least 465kHz. This bandwidth is calculated by using equation 2.9 for a limiter with N = 7 stages and the -3dB bandwidth ($f_{-3dB,LP}$) of the whole limiter is specified at 150kHz. For $A_s = 2$, $N = 10$ stages are required for a gain of $A_{limiter} = 60dB$. The single gain stage bandwidth of $BW_s \gtrsim 560kHz$ is required (equation 4.6).

$$f_{-3dB,s} = BW_s = \frac{BW_{limiter}}{\sqrt{\sqrt[N]{2} - 1}} = \frac{150kHz}{\sqrt{\sqrt[10]{2} - 1}} \approx 560kHz \tag{4.6}$$

At higher single stage gain, the number of gain stages needed for the gain decreases and so the bandwidth required for a single stage decreases as well. With fewer gain stages, a higher RSSI error is implicated as described in chapter 2.1.2. For a single stage the gain bandwidth product stays constant. A high bandwidth of the gain stage is important to decrease the bias current and to optimize the power consumption of the limiting amplifier.

Capacitive load

The capacitive load of the gain stage (C_L) for a gain stage in a limiting amplifier is the sum of the input capacitance of the rectifier (C_{rect}), the input capacitance of the gain stage ($C_{GS,in}$) and the capacitance of the gain stage output node ($C_{GS,out}$) stated in equation 4.8. In the simulation the test bench of figure 4.1 considers only $C_{GS,in}$ of the following gain stage as well as $C_{GS,out}$ (equation 4.9). The C_{rect} of the rectifier further reduces the overall bandwidth of the gain stage and the bandwidth of the limiting amplifier. The input capacitance of the rectifier is not known yet and can be optimized to increase the over all bandwidth.

$$BW_{single} = \frac{1}{2\pi \cdot C_L \cdot \frac{1}{gm}} \tag{4.7}$$

$$C_L = C_{rect} + C_{GS,in} + C_{GS,out} \tag{4.8}$$

$$C_L \approx C_{GS,in} + C_{GS,out} \tag{4.9}$$

To get a constant bandwidth over temperature, all gain stages are biased with an ideal PTAT current of TC = 3300ppm/K. This bias current leads to a constant gm (chapter 3.7.2) over temperature and hence, to an approximately temperature constant bandwidth. The bandwidth of a single gain stage is evaluated with an AC simulation.

4.1.4 Transient response

Using a transient simulation, the large signal behavior of the gain stage at the nominal process at the minimum and maximum temperature is shown in a figure for each gain stage. The differential input a signal with a frequency of $f = 125kHz$ and an amplitude of $\hat{V}_{ID} = 1V$ is applied to the gain stage. The investigations in the next subsections show the large signal response is strongly temperature dependent. The reasons for the temperature dependent large signal differential output voltage are the temperature dependent output current of a differential pair (chapter 3.10.1) and the biasing with a PTAT current required for constant bandwidth. Furthermore, the large signal transient response is dependent on the load of the differential pair. With small input signals, the gain stages are approximately linear but with larger input signals the gain stages clip. The clipping is an absolute nonlinear process depending on many parameters.

Clipping voltage

The gain stage is clipping if almost all the current flows over one branch of the differential pair of the gain stage. In weak inversion, the gain stage and the rectifier based on a differential pair clips at a differential input voltage of $V_{ID} \approx 5.3\eta U_T$ (chapter 3.10.1). The highest single-ended output voltage is then limited to a certain value ($V_s = R_{load} \cdot I_B$). The lowest voltage is then approximately $V = R_{load} \cdot I \approx R_{load} \cdot 0A = V_{SS}$ for NMOS input transistors or V_{DD} for PMOS input transistors. The clipping output voltage of the gain stage has to be larger than the clipping input voltage of the rectifier for a temperature stable output current as described in chapter 2.1.3. The condition leads to an differential output voltage of the gain stage of equation 4.10.

$$V_{ID} \approx V_S \gtrsim 5.3\eta U_T \tag{4.10}$$

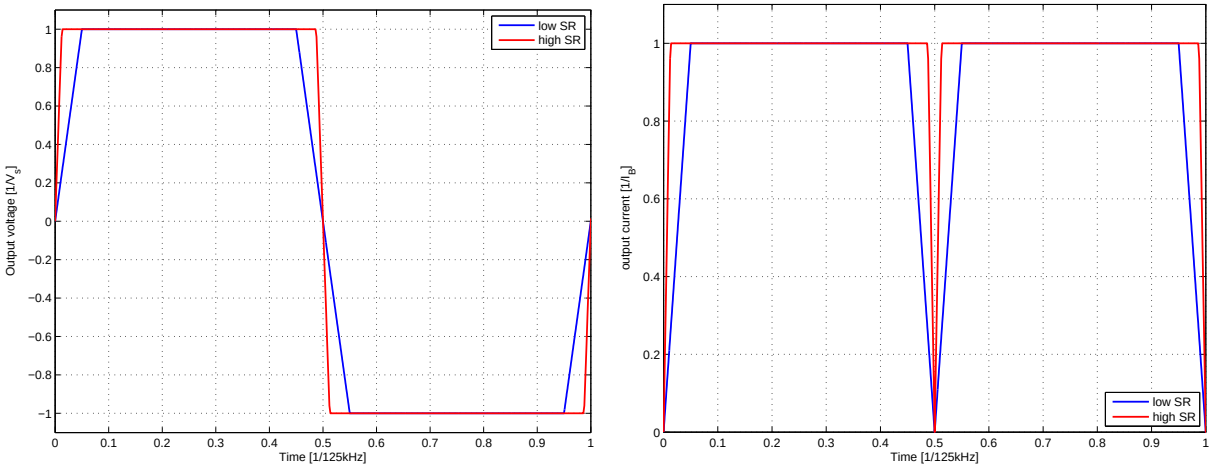
The differential clipping output voltage of the gain stage should be larger than $V_S \gtrsim 5.3\eta U_T$. This means $V_S \gtrsim 270mV$ at 150°C and $V_S \gtrsim 140mV$ at -50°C.

Slew rate (SR)

The maximal change of the output voltage over time is limited by the slew rate, which is given by the current of the differential pair and the capacity of the output voltage node (equation 4.11). If the SR of the sinusoidal input voltage (equation 4.12 where $\hat{V}$ is the amplitude) is larger than the SR of the gain stage (equation 4.11) then the slew rate of the gain stage is limited to SR_{GS} of the gain stage.

$$SR_{GS} = \frac{dV(t)}{dt} = \frac{I}{C_{load}} \tag{4.11}$$

$$SR = max\left(\frac{dV_{IN}(t)}{dt}\right) = max(\hat{V} \cdot 2\pi f \cdot cos(2\pi f t)) = \hat{V} \cdot 2\pi f \tag{4.12}$$



(a) Clipping output voltage with different SR

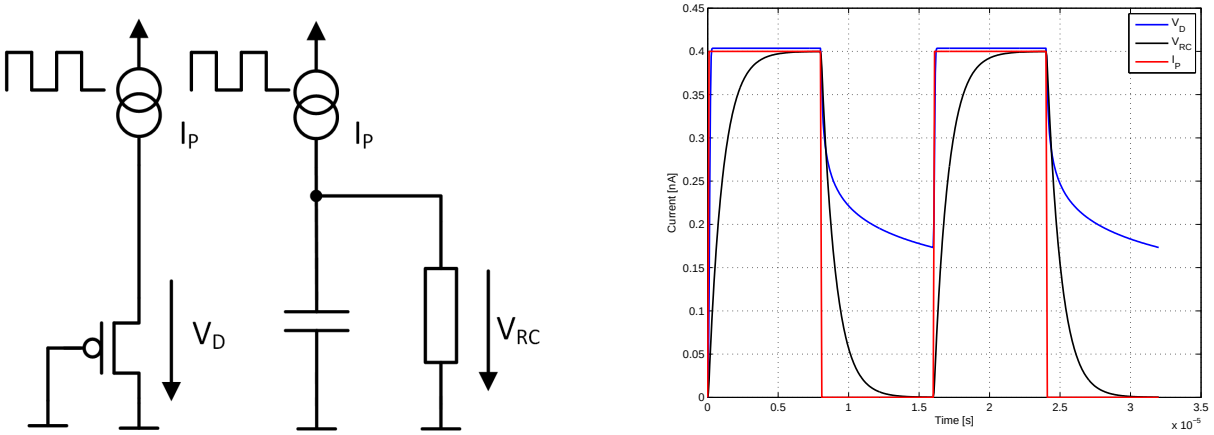
(b) Rectified output voltage with different SR

Figure 4.2: Comparison of different slewrates of the gain stage

Figure 4.2(a) shows a model for a clipping output voltage of a gain stage with different slew rates. The output current is larger at a gain stage with larger slew rate as shown in figure 4.2(b). Because the output voltage of the gain stage is the input for the rectifier, the RSSI current of the limiting amplifier is dependent on the slew rate of the gain stage. The slew rate dependency of the RSSI is considered as second order effect for the temperature stability of the RSSI.

Nonlinear load

Since most investigated gain stages have a nonlinear diode load, the rise- and fall-times are investigated in figure 4.3. For a linear load resistance the rise- and fall-time (related to slew rate) are equal (V_{RC}, black line). For nonlinear loads the rise- and fall-time can be different (V_D, blue line). The voltage across the diode while discharging of the capacitor is different compared to the charging because of the exponential current to voltage relation of the diode operating in weak inversion.



(a) Pulsed current source with different loads

(b) Transient response for different loads

Figure 4.3: Comparison linear and nonlinear load

Common mode voltage

All the gain stages are based on differential pairs. The load and the bias current determine the common mode voltage of the output. The common mode voltage also changes over temperature and with different process corners. The minimum value of the common mode voltage for a NMOS gain stage is at the maximum temperature of 150°C and fast process corner. The maximum common mode voltage is at -50°C slow corner where the threshold voltage is increased.

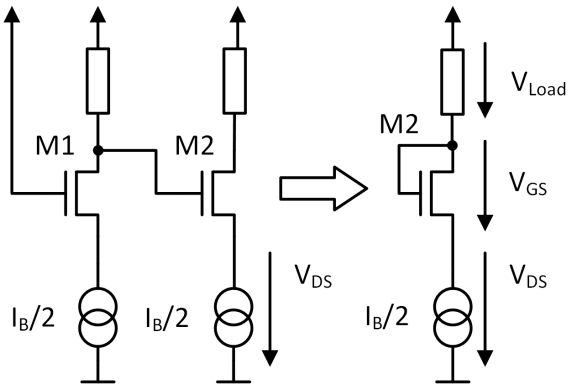


Figure 4.4: Common mode voltage for cascaded gain stages

The input voltage of the gain stages have the common mode voltage of the previous stage output voltage, because there is no AC coupling between the stages. With no input signal applied, the differential pair can be simplified to one branch with half bias current of a differential pair (figure 4.4, left side). For the voltage drop over the current source (V_{DS}) of M2, the circuit can be further simplified (figure 4.4, right side) with V_{GS} of the diode because all gain stages are equal they have the same common mode voltage.

4.1.5 White noise

In most limiting amplifiers, white noise is the most dominating noise source in the design because the offset subtractor damps flicker noise. The integrated input and output referred noise of the limiting amplifier is mainly caused by the white noise. The noise comparison for a single gain stage is performed for an input referred voltage noise density at a frequency of f = 125kHz. In the final limiting amplifier design, flicker noise is also considered. The input referred voltage noise density is one of the most important parameters for the power consumption in this design as can be seen in the final limiting amplifier design of chapter 7.5. Each gain stage is also optimized for noise by dimensioning.

Noise contributors

The input referred white noise voltage density of a single transistor can be calculated by equation 3.31. The output referred white noise voltage density of a differential stage with a diode connected load ($g = gm2$) is stated in equation 4.13. The input referred white noise voltage density is the output referred noise divided by the squared gain $\left(A_s^2 = \frac{gm1^2}{gm2^2}\right)$ as equation 4.14 shows.

$$\frac{S_{U^2,out}(f)}{df} = 8kT\eta\left(\gamma_1\frac{gm1}{gm2^2} + \frac{\gamma_2}{gm2}\right) \tag{4.13}$$

$$\frac{S_{U^2,in}(f)}{df} = 8kT\eta\left(\frac{\gamma_1}{gm1} + \gamma_2\frac{gm2}{gm1^2}\right) = 8kT\eta\frac{1}{gm1}\left(\gamma_1 + \frac{\gamma_2}{A_s}\right) \tag{4.14}$$

In equation 4.14, it is obvious that the input voltage noise contribution of the load transistor is divided by the gain. With a gain of $A_s >> 1$ in most cases, the input referred noise of the input transistors is larger than the noise of the load. For the summed noise of different gain stage circuit with a different load, every noise contributor has to be considered and added. All gain stages are biased with a fixed current and an AC noise simulation is performed. For all gain stages input referred noise density is evaluated at f = 125kHz at 27°C.

Transconductance

Also with a low inversion coefficient (moderate to weak inversion), gm is slightly dependent on the W/L of the transistor. The input transistor has to be deep in weak inversion with a low IC for a high gm1 at a fixed bias current. A high W/L ratio will lower the IC (equation 3.7) and the transistor has the highest gm and thus the lowest voltage noise for a given current.

As shown in chapter 3.10.2, a diode connected load transistor with high W/L will not stay in saturation for the fast process and 150°C temperature corner. For the load diode, the proposed solutions from chapter 3.10.2 can be applied to get a high W/L ratio for low noise and for staying saturated at the fast process and 150°C temperature corner. For the input transistor, the back gate effect can be exploited. In addition with an applied V_{BS}, the substrate factor decreases slightly [17], which leads to a lower input referred voltage noise density. This phenomena is also investigated in [23] for MOS operating in weak inversion.

4.2 Triode load gain stage

Figure 4.5 shows a simple gain stage circuit: A NMOS differential pair with PMOS load transistor acting in the triode region as a resistor. The gain can be controlled by a bias voltage of M3 and M4 which is created by a PMOS diode (M5) with a bias current (I_{Bias}). The PMOS load diode (M3,M4) has a large length, which is required for a certain output resistance. The small signal gain is stated in equation 4.15.

$$A_0 = gm_{NMOS} \cdot (Ron_{PMOS} \mid\mid rds_{NMOS}) \approx gm_{NMOS} \cdot Ron_{PMOS} \tag{4.15}$$

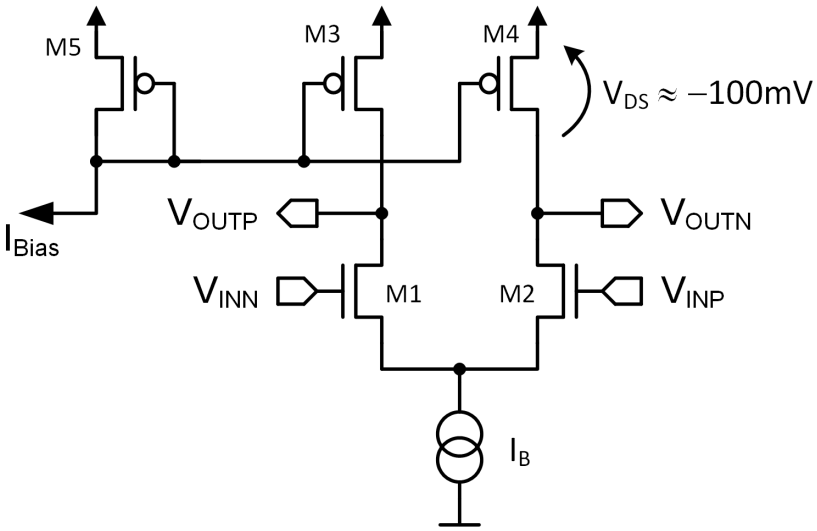
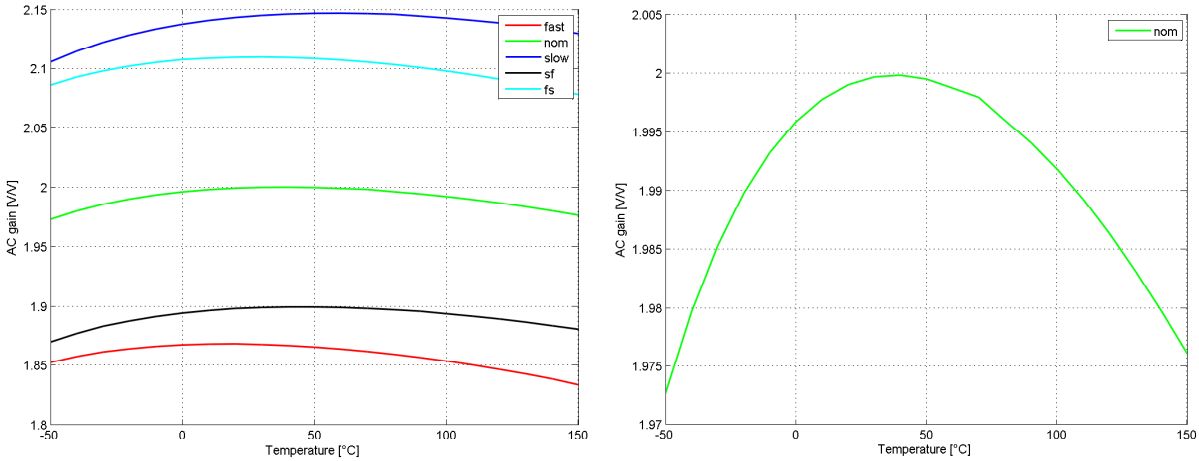


Figure 4.5: Schematic of regulated gain stage with triode load

4.2.1 Small signal gain variation

Figure 4.6(a) shows the variation of gain over the temperature for different process corners. Different process corners have a significant influence on the absolute gain, hence the temperature coefficient of the gain cannot be observed any more. In figure 4.6(b) the gain of the nom process is shown. The gain has a linear and nonlinear temperature coefficient. The linear temperature coefficient is corner dependent. The maximum gain drift (equation 4.1) is approximately $\Delta A_s \approx 1.3\%$. The shifted gain due to different process corners is caused by the variation of the PMOS load threshold voltage, which leads to a variation of the R_{on}.

In 1000 Monte Carlo runs with mismatch and process variation, the simulation reveals a relative standard deviation of $\frac{\sigma(A_s)}{\mu(A_s)} \approx 1.4\%$ at 27°C. For an accurate gain, the PMOS load and the NMOS input transistor have to match. The gain mainly depends on two parameters: Ron of PMOS (linear, strong inversion) and the gm of NMOS (saturation, weak inversion). These two parameters do not correlate with each other. The models may not cover all different combinations for gain variations. There might also be a different drift of the PMOS and NMOS over time when the device is stressed with temperature or current.



(a) A_{125} over temperature for different process corners W/L load = 0.6u/20u

(b) A_{125} over temperature with nominal process corners W/L load = 0.6u/20u

Figure 4.6: A_{125} variation with process corners and temperature

To compensate the nonlinear temperature coefficient and the gain variations, a **gain regulation** is implemented, which controls the bias current of the load diode M5 and thus the R_{on} of the triode load [25]. A DC test signal is applied to a copy of a single gain stage and the DC gain is compared to a desired gain value. If the gain is to low, R_{on} of the load is enhanced and if the gain is to high then R_{on} is reduced by increasing the current of the bias diode. The regulation block is implemented with a chopper amplifier because very small gain variations have to be compensated and a small offset of the regulator will lead to a gain offset. Achieving high accuracy and low offset for the regulation block makes a difficult design especially for low power circuits.

4.2.2 -3dB Bandwidth

The bandwidth of the gain stage can be primarily determined by gm of the input- and the capacitance of the load transistor. To achieve a low gain drift over temperature, the load transistor has to be sufficiently long. The long load diode has a large capacitive load. A compromise of gain drift over temperature and bandwidth has to be found. With the given $W/L = 0.6\mu m/20\mu m$, the gain stage has sufficient bandwidth of $f_{-3dB} \approx 660kHz$. A bandwidth of approximately $f_{-3dB} \approx 1MHz$, with half of the length of the load diodes can be achieved, but this is more then doubling the gain drift over temperature.

4.2.3 White noise

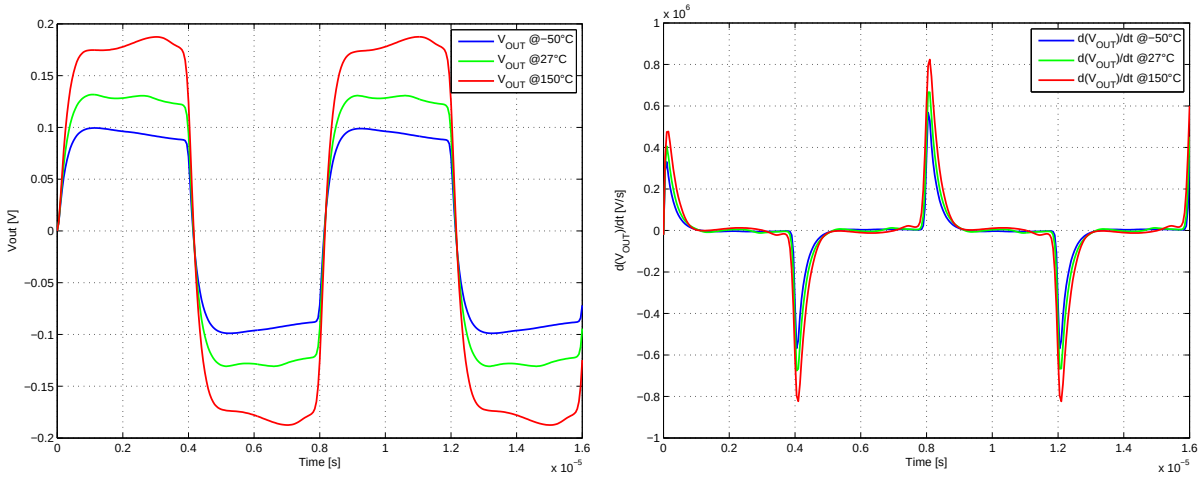
The load diode acts in linear regime so the γ_2 factor (equation 4.14) for thermal noise is increased to $\gamma_2 \approx 1$. The noise of the load transistor is twice as high as a transistor in weak inversion. The input referred white noise density of equation 4.14 with $\gamma_2 = 1$ and $A_s = 2$ simplifies to equation 4.16.

$$S_{U^2,in}(f) \approx 8kT\frac{1}{gm1}\left(\gamma_1 + \frac{\gamma_2}{A_s}\right) \approx 8kT\frac{1}{gm1}\left(0.5 + \frac{1}{A_s}\right) = 8kT\frac{1}{gm1} \tag{4.16}$$

In simulation, the gain stage shows a very good noise performance. The input referred white noise density at f = 125kHz is approximately $S_{U^2,in}(f) \approx 257\frac{nV}{\sqrt{Hz}}$.

4.2.4 Transient response

Figure 4.7 shows the transient differential output voltage of the gain stage. The single-ended upper clipping level is given by V_{DD}. The lower voltage clipping level is determined by the current of the differential pair, the R_{on} and the supply voltage. Due to PTAT biasing current, the common mode voltage is lower at higher temperatures. The clipping levels are also higher at high temperature. With a larger bias current, the voltage drop over a linear load is larger at high temperatures. The single-ended lower voltage clipping level is 1.4V at -50°C. At 150°C, the clipping voltage level is 1.33V at the nominal process corner. The common mode voltage varies from 1.45V (-50°C) to 1.4V (150°C).



(a) Transient response at different temperatures

(b) dVout/dt at different temperatures

Figure 4.7: Transient response of the regulated gain stage with different temperatures

The different clipping level at the temperature corners leads to a temperature dependent output current of the rectifier if the rectifier is not clipping first. The clipping voltage of the gain stage varies similar to a PTAT voltage because the gain stage is biased with a PTAT current. Because the input clipping voltage for the rectifier is also a PTAT voltage, these two effects compensate the RSSI error at different temperatures. The clipping voltage levels are almost constant over process corners and vary with a maximum of 40mV from slow to fast.

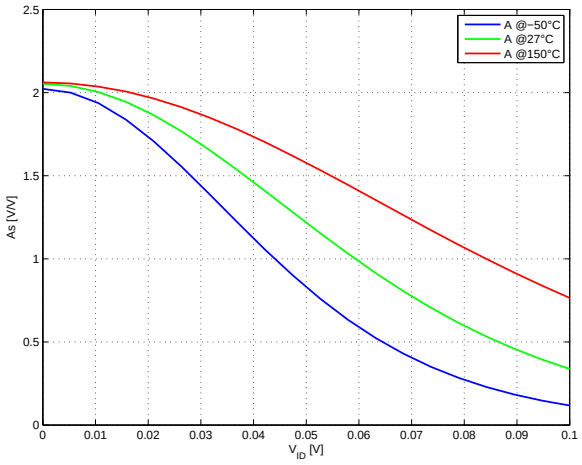


Figure 4.8: Gain A_s over differential input volage V_{ID}

Figure 4.8 shows the gain over the input voltage. The gain is decreasing with increasing differential input voltage. The output voltage over the load is approximately linear, in the range where the load is in the linear range (strong inversion). The output current of the input differential pair is a hyperbolic tangent function as stated in equation 3.46. This function is approximately linear if the input voltage is in the range of a few U_T.

4.3 Two diodes load gain stage

Figure 4.9 shows the schematic of the gain stage with two diodes load. The gain can be calculated by equation 4.17. Because all transistors have equal current, they have an equal operating point resulting in equal gm and gds. The gain of 2 is a good approximation for a sufficient small output conductance gds of the diode connected load and the input transistor.

$$A_0 = gm \cdot rout = gm \cdot \left(\frac{1}{gm/2 + gds/2 + gds} \right) = gm \cdot \left(\frac{2}{gm + gds + 2gds} \right)$$
$$\approx \frac{2 \cdot gm}{gm} \approx 2 \tag{4.17}$$

A significant disadvantage of this stage is that only a gain of $A_{max} \approx 2$ can be implemented. With a limiting amplifier of 60dB, this means that 10 gain stages have to be used. There is no room for optimization with respect to the number of instances. The stage cannot be built with NMOS because the second stacked NMOS diodes back gate effect would lower the gain to less then 2. This is even worse for a limiting amplifier design.

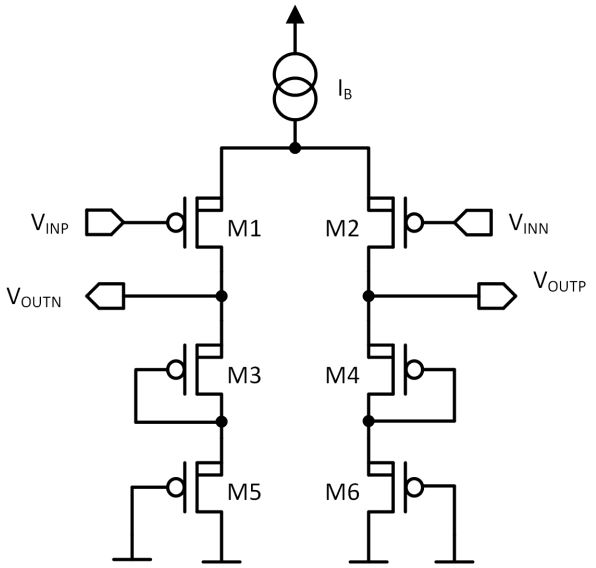
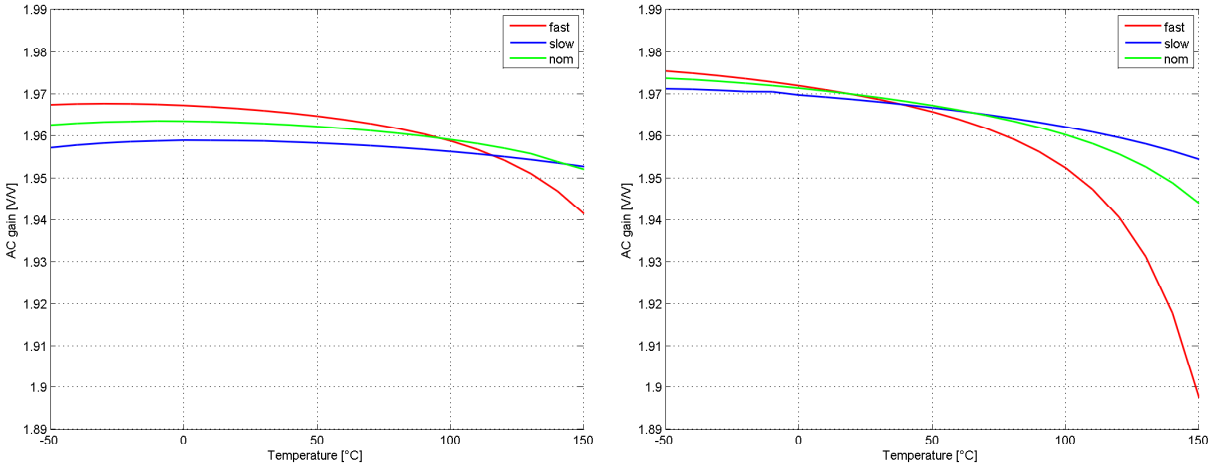


Figure 4.9: Gain stage with two diodes load, $W/L = 5\mu m/2\mu m$

4.3.1 Small signal gain variation

In figure 4.10, the gain drift over temperature for different process corners is shown. The slope of the gain drift is dependent on the process corner. At the fast process corner (red curve) the gain decreases at higher temperatures because the gds of the diodes increases due to low V_{DS}. For low gain drift over temperature a high V_{DS} is required. A low W/L ratio increases the V_{GS} and the V_{DS} of the transistors. The maximum gain drift over temperature with $W/L = 5\mu m/2\mu m$ is $\Delta A_s \approx 1.25\%$. With $W/L = 5\mu m/1\mu m$ the gain drift is higher with $\Delta A_s \approx 4\%$ compared to lower W/L.

The gain stage has good matching and temperature properties. The relative standard deviation of the gain with a Monte Carlo simulation at 27°C is low with $\left(\frac{\sigma(A_s)}{\mu(A_s)} \approx 0.1\%\right)$ because all transistors are equal PMOS and have an equal current density.



(a) A_{125} over temperature with different process corners $W/L = 5\mu m/2\mu m$

(b) A_{125} over temperature with different process corners $W/L = 5\mu m/1\mu m$

Figure 4.10: AC gain over temperature

4.3.2 -3dB Bandwidth

The two load diodes have parasitic diode from well to substrate, which is not modeled within the standard model. An extra diode is added to the schematic for simulation. This slightly reduces the bandwidth of the gain stage. The bandwidth with the substrate diode is approximately $f_{-3dB} \approx 750kHz$ at $W/L = 5\mu m/2\mu m$. At a $W/L = 5\mu m/1\mu m$, a bandwidth of approximately $f_{-3dB} \approx 1.1MHz$ is reached.

4.3.3 White noise

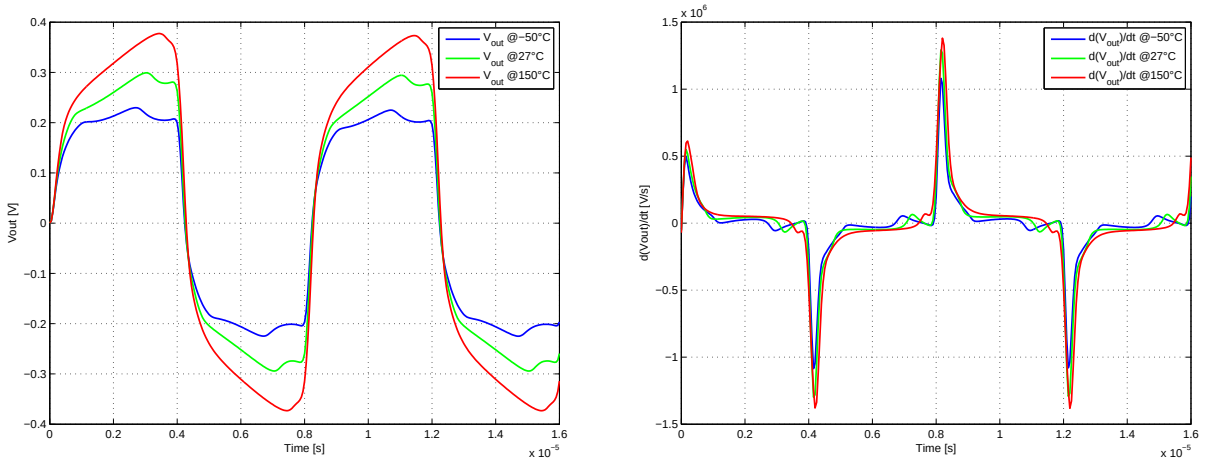
The input referred white noise density of this gain stage can be calculated by equation 4.18.

$$S_{U^2,in}(f) = 8kT\frac{1}{gm1}\left(\gamma_1 + \frac{\gamma_2}{A}\right) \approx 8kT\frac{1}{gm1}\left(0.5 + \frac{0.5}{A}\right) = 8kT\frac{1}{gm1}\cdot 0.75 \tag{4.18}$$

PMOS transistors have a higher η, which increases $S_{U^2,in}(f)$ compared to NMOS transistors. The simulated input referred noise density is high with $S_{U^2,in}(f) \approx 327\frac{nV}{\sqrt{Hz}}$ at a $W/L = 5\mu m/2\mu m$ compared to the other gain stages. A higher W/L ratio slightly increases the gm because the transistors are not operated with a very low IC. An input referred noise density of approximately $S_{U^2,in}(f) \approx 318\frac{nV}{\sqrt{Hz}}$ with a $W/L = 5\mu m/1\mu m$ is achieved. On the other hand with increased W/L, a larger gain drift over temperature is implicated.

4.3.4 Transient response

The transient response with large input signal of the gain stage is shown in figure 4.11(a). The upper clipping levels are given by the common mode level minus the supply, which is at -50°C higher. The signal is nonlinear due to loading and unloading of nonlinear diode as shown in figure 4.3(b). The single-ended upper clipping voltage is $V_s \approx 0.9V$ at -50°C and $V_s \approx 0.6V$ at 150°C. The lower clipping voltages are $V_s \approx 0.25V$ at 150°C and $V_s \approx 0.65V$ at -50°C respectively.



(a) Transient response at different temperatures

(b) dVout/dt at different temperatures

Figure 4.11: Transient response of the two diodes load gain stage at different temperatures

Common mode voltage

The common mode output voltage at low temperatures and slow process corner increases especially for lower W/L. Because all gain stages have the same common mode voltage at the output, the V_{DS} left for the current source at a $W/L = 5\mu m/2\mu m$ can be determined by equation 4.19.

$$V_{DS} = V_{DD} - 3 \cdot V_{GS} = 1.5V - 3 \cdot 460mV = 120mV \tag{4.19}$$

The V_{GS} of one diode with the bias current is approximately 460mV at -50°C slow. Thus a voltage of $V_{DS} = 120mV$ remains for the bias current source for (a $W/L = 5\mu m/1\mu m$ results in $V_{DS} = 217.5mV$). With the minimum specified supply voltage ($V_{DD,min} = 1.35V$), the current source will not stay saturated. The same problem occurs at the rectifier.

To reduce the circuits voltage headroom of the load diodes, the diodes can be folded with a current source like in [3] or as shown in chapter 4.7 of this thesis.

A level shifter, which shifts the output voltage to a lower level, could also solve the problem. The level shifter has to shift the common mode voltage to a minimum voltage level, $V_{DS,SAT} \approx 4\eta U_T$ at the drain source of the input transistor. The shifting voltage V_x is stated in equation 4.20.

$$\begin{aligned} V_{GS} - V_x &\geq V_{DS,SAT} \\ V_x &\leq V_{GS} - V_{DS,SAT} \end{aligned} \tag{4.20}$$

$V_{DS,SAT}$ and V_{GS} vary with temperature in the opposite direction. Also V_{GS} is dependent on the process corner. Additional circuitry has to be implemented. This is not investigated further because the gain stage has a bad noise performance.

4.4 Unfolded diode load gain stage

Figure 4.12 shows the schematic of this gain stage. There is a differential pair with load diode and a current source. In [15, p.125] this architecture is shown for an NMOS pair in strong inversion to reduce the voltage headroom of the diode and to enhance the gain. With additional current source, less current is flowing through the load diode (M3, M4) than through the input transistor (M1, M2). In weak inversion, the gm is directly proportional to the current. With the current related gm ratios, a small signal gain of equation 4.21 is established. This gain is temperature stable if the current sources have an equal temperature coefficient.

$$A_0 = \frac{gm1}{gm2 + gds1 + gds2 + gds_{CS}} \approx \frac{gm1}{gm2} = \frac{I_{D1}}{I_{D3}} = \frac{I_B/2}{I_{D3}} = \frac{I_B/2}{I_B/2 - I_{CS}} \tag{4.21}$$

The unfolded diode load gain stage is biased with $I_{D1} = I_B/2 = 20nA$ and the gain current set to $I_{CS} = 10nA$ for a gain of 2. The load transistors width is half of the width of the input transistor for an equal current density. The current source is implemented by an NMOS current mirror.

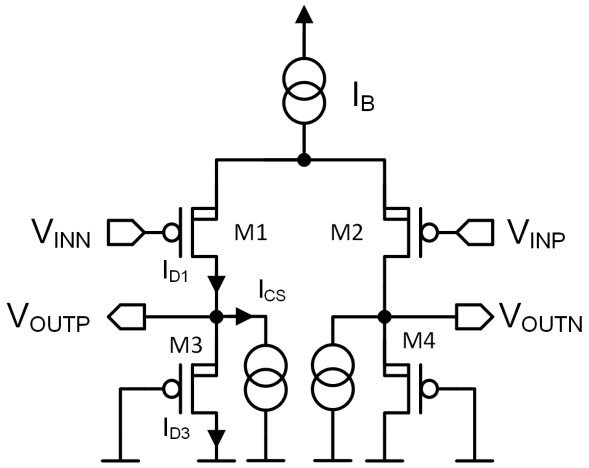


Figure 4.12: Schematic of the unfolded diode load gain stage

4.4.1 Small signal gain variation

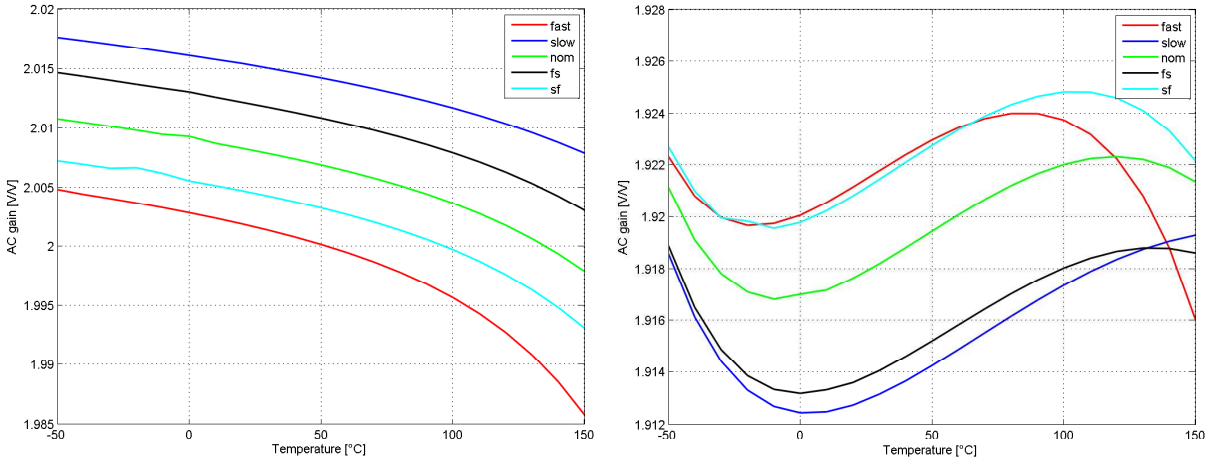
The input transistors should have equal current densities (equal IC) to achieve a small gain drift over temperature. This can be done by scaling of W/L. If the input and the load transistor have the same current densities, equation 4.22 is valid. With scaling over the width (L1 = L3), the width of the load is given with $W3 = W1/A_0$. If the transistors have different current densities, but equal length, W3 and W4 is scaled by k (equation 4.23) and k is unequal A_0.

$$\frac{W1}{L1 \cdot I_{D1}} = \frac{W3}{L2 \cdot I_{D3}} = \frac{W3}{L3 \cdot \frac{I_{D1}}{A_0}} \tag{4.22}$$

$$W3 = W1/k \tag{4.23}$$

The gain variation over temperature is shown in figure 4.13(a). The temperature coefficient is almost linear and changes slightly with different process corners. The maximum drift over temperature is $\Delta A_s = 1.4\%$ at the fast process corner due to the output conductance gds of the load, input and the current source transistors. The current source operates with high IC for low current noise and good matching properties. $V_{DS,SAT}$ for a transistor with higher IC is increased.

A low common mode voltage at 150°C fast appears to the current source due to the load diode. Thus the current source transistor is close to the linear conduction due to increased $V_{DS,SAT}$ and has increased output conductance. Figure 4.13(b) shows the gain drift over temperature for different current densities of the load and the input transistor. Various effects for gain drift, for example, drift of gm1, gm2 or gds superimpose. A low $W1/L1 = 2\mu m/4\mu m$ ratio is implemented to increase V_{GS} of the load and the input transistors. This low W/L ratio leads to a lower gain drift over temperature especially for the fast process corner.



(a) A_{125} with $W1/L1 = 2\mu m/4\mu m$, k = 2

(b) A_{125} with $W1/L1 = 2\mu m/4\mu m$, k = 4/3

Figure 4.13: Gain over temperature at different process corners

A Monte Carlo simulation of 1000 runs shows a relative standard deviation of the AC gain of $\frac{\sigma}{\mu} = 1.5\%$ at 27°C. For a low gain variation, the tail current source and the current source for the gain have to match. A good current matching can be achieved with large area and a high overdrive voltage (low gm, high IC). With a high IC, $V_{DS,SAT}$ decreases. This can lower the gain especially at the 150°C fast corner. The gain gets less because with a low common mode output voltage, the current source draws less current.

4.4.2 -3dB Bandwidth

With the given bias current, the bandwidth of the gain stage is $f_{-3dB} \approx 940kHz$, which is large compared to other gain stages. Even the large length of the current source ($W/L = 0.6\mu m/40\mu m$) does not lower the bandwidth of the gain stage significantly.

4.4.3 White noise

The current source of the gain stage is an additional noise source of the gain stage. This source is implemented by an NMOS current mirror. The diode of the current mirror (1/B factor) does not affect the summed noise because the noise is a common mode noise. Low gm (gm_{CS}) for low current noise (equation 3.41) can be achieved by a small W/L ratio, which is also beneficial for current mismatch. The current mirror transistors operate in strong inversion (high IC). The current noise of the current source is stated in equation 4.24.

$$S_{I^2} = 4kT\gamma gm_{CS} \cdot (B+1) \approx 4kT\gamma gm_{CS} \tag{4.24}$$

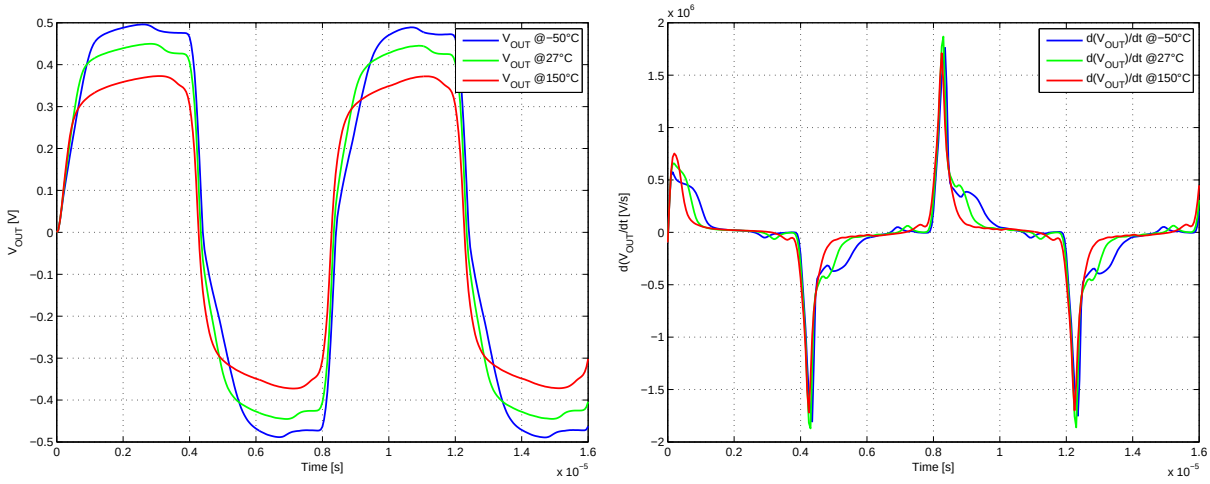
$$S_{U^2,in}(f) = 8kT\frac{1}{gm1}\left(\gamma_1 + \frac{\gamma_2}{A} + \frac{\gamma_{CS} gm_{CS}}{gm1}\right) \tag{4.25}$$

The input referred voltage noise density can be calculated by adding significant all noise sources to the output referred voltage noise density and divided by the squared input transconductance conductance ($gm1^2$) as stated in equation 4.25.

The gain stage showed in simulation a large input referred noise density of $S_{U^2,in}(f) \approx 370\frac{nV}{\sqrt{Hz}}$. With bulk of the input transistors connected to VDD, the noise can be lowered to $S_{U^2,in}(f) \approx 360\frac{nV}{\sqrt{Hz}}$. The large noise is caused by the low W1/L1 of the input and load transistors and the higher noise density of a PMOS compared to a NMOS. A higher W1/L1 ratio decreases noise but increases gain drift over temperature.

4.4.4 Transient response

Figure 4.14 shows the transient response of the gain stage at different temperatures. The lowest single-ended clipping voltage of the gain stage is VSS. The upper single-ended clipping voltage is temperature dependent, for -50°C at $V_s \approx 500mV$ and for 150°C at $V_s \approx 350mV$. The differential output voltage is is shown in figure 4.15(a).



(a) Transient response at different temperatures

(b) dVout/dt at different temperatures

Figure 4.14: Transient output signal of the unfolded diode load gain stage

The single-ended output voltage is stated in equation 4.26 under the condition that M3 is saturated (V_{OUTP} *and* $V_{OUTN} \geq 4\eta U_T$). This is the resolved equation 3.11 for a saturated transistor in weak inversion. The differential output voltage can be stated by equation 4.28.

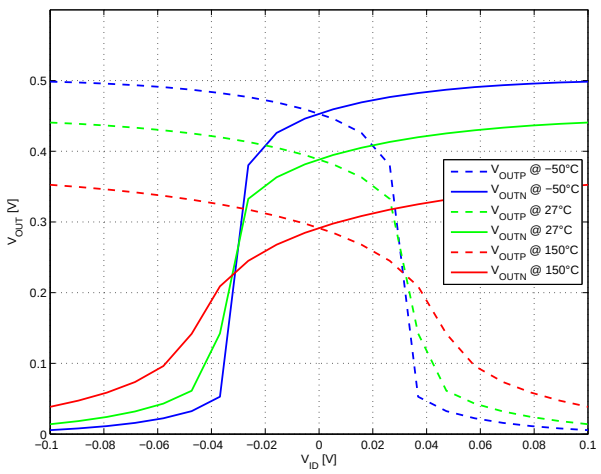
$$V_{OUTP} = \eta U_T \cdot ln\left(\frac{I_{D3}}{I_0}\right) = \eta U_T \cdot ln\left(\frac{I_B/2 - I_{CS}}{I_0}\right) \tag{4.26}$$

$$I_{D1} = \frac{I_B}{1 + e^{\left(\frac{V_{ID}}{\eta U_T}\right)}} = \frac{I_B}{1 + e^{x}}; \quad I_{D2} = \frac{I_B}{1 + e^{\left(\frac{-V_{ID}}{\eta U_T}\right)}} = \frac{I_B}{1 + e^{-x}} \tag{4.27}$$

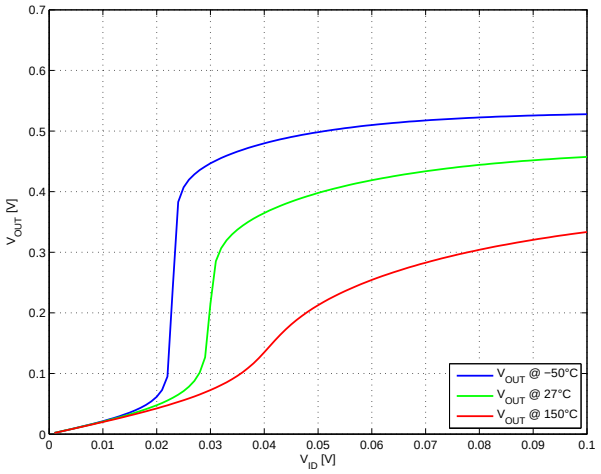
$$\begin{aligned} V_{OUT} = V_{OUTP} - V_{OUTN} &= \eta U_T \left[ln\left(\frac{\frac{I_B}{1+e^{x}} - I_{CS}}{I_0}\right) - ln\left(\frac{\frac{I_B}{1+e^{-x}} - I_{CS}}{I_0}\right)\right] \\ &= \eta U_T ln\left(\frac{\frac{I_B}{1+e^{x}} - I_{CS}}{\frac{I_B}{1+e^{-x}} - I_{CS}}\right) \end{aligned} \tag{4.28}$$

The large signal differential output voltage is nonlinearly dependent on the input voltage as can be seen in figure 4.15(b). The output voltage increases rapidly with increasing V_{ID} when

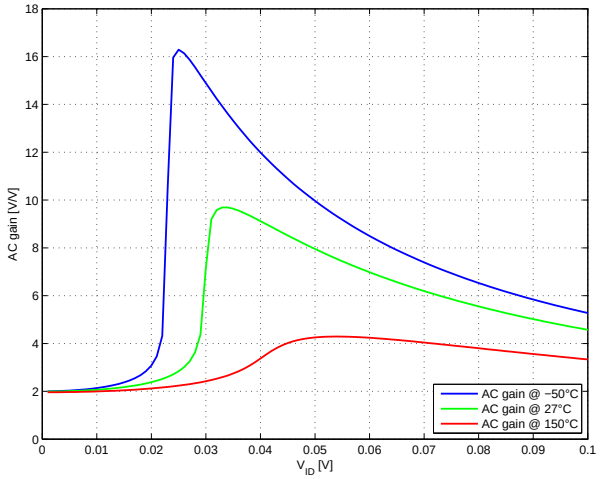
almost no more current is flowing at one side of the load diode (figure 4.15(d)). V_{OUT} stays almost constant (clipping) with further increasing V_{ID}.



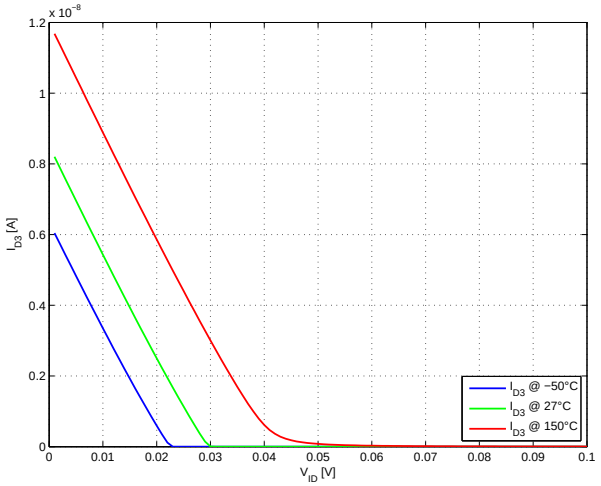
(a) Single-ended output voltages as function of V_{ID}



(b) Differential output voltage as function of V_{ID}



(c) Gain as function of V_{ID}



(d) Diode current as function of V_{ID}

Figure 4.15: Gain stage behavior over DC differential input voltage V_{ID}

The DC gain over the differential input voltage (figure 4.15(c)) is at the maximum, where almost no more current flows through the diode (figure 4.15(d)). For a small input voltage the gain stays constant. When the gain stage is unbalanced with an input voltage of $V_{ID} \approx \eta U_T$ (equation 4.29), there is almost no more current flowing over one diode. This differential input voltage depends on the bias currents of the gain stage. As the RSSI error is larger for larger gain values, the nonlinear gain contributes to a larger RSSI error.

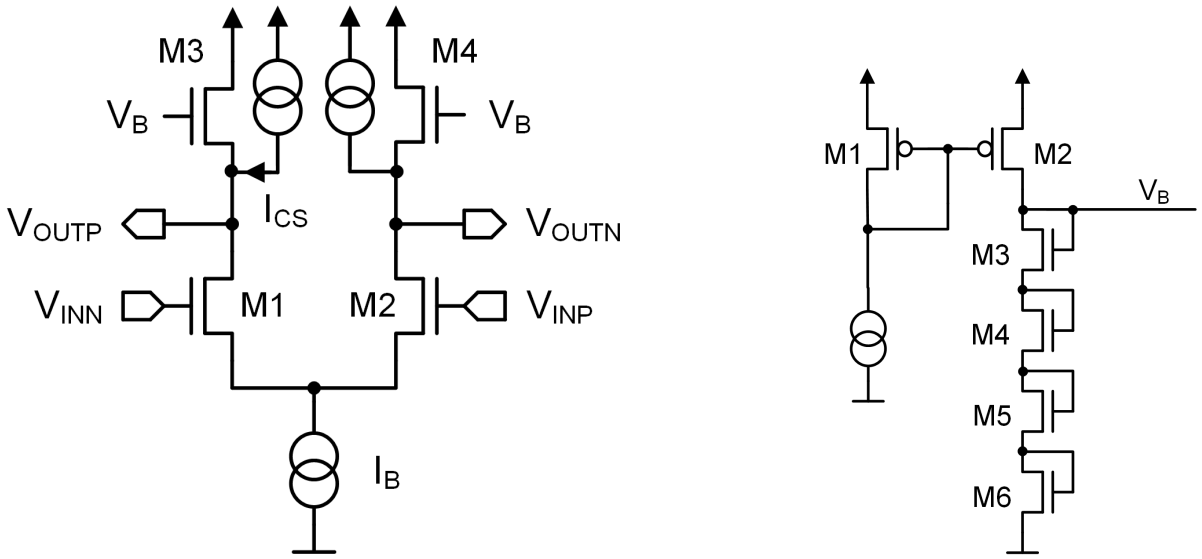
$$V_{ID} \leq 2\eta U_T \cdot arctanh\left(\frac{2 \cdot I_{D3}}{I_B}\right) = 2\eta U_T \cdot arctanh\left(\frac{1}{2}\right) \approx 2\eta U_T \cdot 0.55 \approx \eta U_T \tag{4.29}$$

4.5 Unfolded diode load noise optimized

The schematic of the noise optimized unfolded diode load gain stage is shown in figure 4.16. The small signal gain is stated in equation 4.30. The bulk of the NMOS diode (M3, M4) cannot be connected to the source due to the process limitations. This adds the bulk source transconductance to the gain, which is weakly dependent on the bulk source voltage [17]. The backgate effect increases the threshold voltage of the NMOS transistor and so the diode stays in saturation for the fast 150°C corner. V_B increases V_{DS} of the load diodes (M3, M4). In the small signal gain subsection 4.5.2 and in the transient response subsection 4.5.4, the purpose of the bias voltage V_B of figure 4.16(b) is explained in more detail.

$$\begin{aligned} A_0 &= \frac{gm_1}{gm_3 + gmbs_3 + gds_1 + gds_3 + gds_{CS}} \approx \frac{gm_1}{gm_3 + gmbs_3} = \frac{gm_1}{gm_3\eta} \\ &= \frac{I_B/2}{(I_B/2 - I_{CS}) \cdot \eta} \end{aligned} \tag{4.30}$$

For a fixed gain of 2 the I_{CS} has to be higher due to the η. The I_{CS} is set to 12nA for a gain of $A_0 \approx 2$ ($\eta \approx 1.2$).



(a) Unfolded diode load gain stage noise optimized

(b) Gate bias voltage V_B generation

Figure 4.16: Schematic of unfolded diode load gain stage noise optimized

4.5.1 White noise

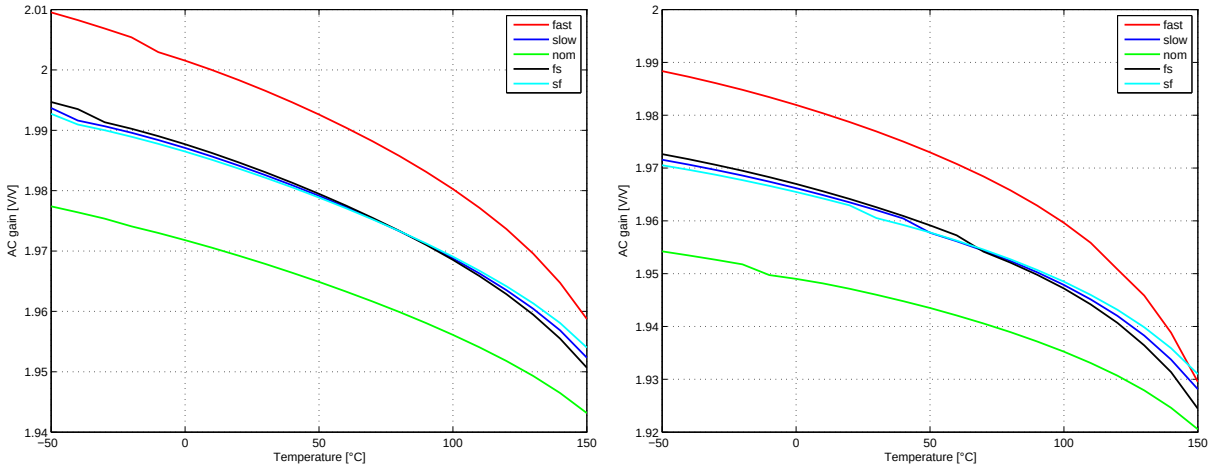
The gain stage is build in NMOS because the substrate factor for NMOS is slightly lower than for PMOS transistors. Furthermore, the back gate effect increases the threshold voltage of the NMOS transistor. Despite with large W/L the load diode and the input transistor stays in saturation for the 150°C fast corner. The input transistor ($W1/L1 = 8\mu m/1\mu m$) and the load diode ($W3/L3 = 4\mu m/1\mu m$) can be operated in deep weak inversion, thus they have the highest gm for a given current. This means the MOS has the lowest white noise. The PMOS current source has a low $W/L = 0.4\mu m/30\mu m$, which leads to low gm and low current noise. The gain stage showed a input referred noise density of $S_{U^2,in}(f) \approx 264\frac{nV}{\sqrt{Hz}}$. With a larger length of the input and load ($L = 2\mu m$) the input referred noise is approximately $S_{U^2,in}(f) \approx 275\frac{nV}{\sqrt{Hz}}$.

4.5.2 Small signal gain variation

In figure 4.17 the gain drift over temperature for different process corners is shown. The gain drift can be minimized by reducing V_B at the gate of the NMOS. This reduction increases V_{DS} of the current source and the load transistor. At the 150°C fast corner, the gain drop is less with higher V_{DS} due to less gds of the current source. A maximum gain drift of $\Delta A_s \approx 2.5\%$ at the fast process corner can be reached.

Generating V_B, as shown in figure 4.16(b), is dependent on the supply voltage and process corners. The voltage will be VDD if the V_{GS} of the load is large. At the fast 150°C corner V_B is at the minimum ($VDD - V_B \approx 1.5V - 1.2V \approx 0.3V$). For the minimum supply voltage of VDD = 1.35V the gain drift can be seen in figure 4.17(b).

Also the gain variation can be minimized by a larger L. With a $W1/L1 = 8\mu m/2\mu m$, the gain variation is $\Delta A_s \approx 2\%$. A larger L has the drawback of increased noise and reduces the bandwidth of the gain stage.



(a) A_{125} with $W/L = 8\mu m/1\mu m$, VDD =1.5V (b) A_{125} with $W/L = 8\mu m/1\mu m$,VDD =1.35V

Figure 4.17: Gain variation over temperautre

A Monte Carlo simulation of 1000 runs shows a standard deviation of the AC gain of $\frac{\sigma}{\mu} = 1.2\%$ at 27°C. Like for the unfolded PMOS diode the tail current source and the current source for the gain have to match for low gain variation. A good matching is achieved with large area and a high overdrive voltage of the load current source.

4.5.3 -3dB Bandwidth

The gain stage has a very large bandwidth of approximately at 1.4MHz with $W1/L1 = 8\mu m/1\mu m$. With $W1/L1 = 8\mu m/2\mu m$, the bandwidth of the gain stage is reduced to approximately 1MHz.

4.5.4 Transient response

The transient response is similar to the PMOS unfolded diode load gain stage. The minimum single-ended output voltage with a high $W3/L3$ of the load diode is too low for the rectifier to clip before the gain stage at the fast 150°C corner. The clipping voltage can be increased by a lower gate voltage than VDD for the load diode, namely V_B. When the rectifier clips before the gain stage the output current is independent of the clipping voltage of the gain stage, which varies over temperature. Clipping the rectifier before the gain stage leads to a more temperature stable RSSI. As $V_{ID} = V_S = 5.3 \cdot \eta U_T$ (voltage to clip the rectifier) increases with temperature, also V_{GS} of the load diode increases.

4.6 Unfolded diode load with rectifier gain stage

The circuit of the noise optimized unfolded diode load gain stage (chapter 4.5) is modified by additional PMOS transistors (M3, M6) as shown in figure 4.18, to combine a gain stage and a rectifier in one circuit. The idea of the circuit is based on the rectifier of [3], where the principle of rectification is similar. In this chapter the properties of the gain stages are discussed and in the chapter 5.6 the rectifiers properties are shown.

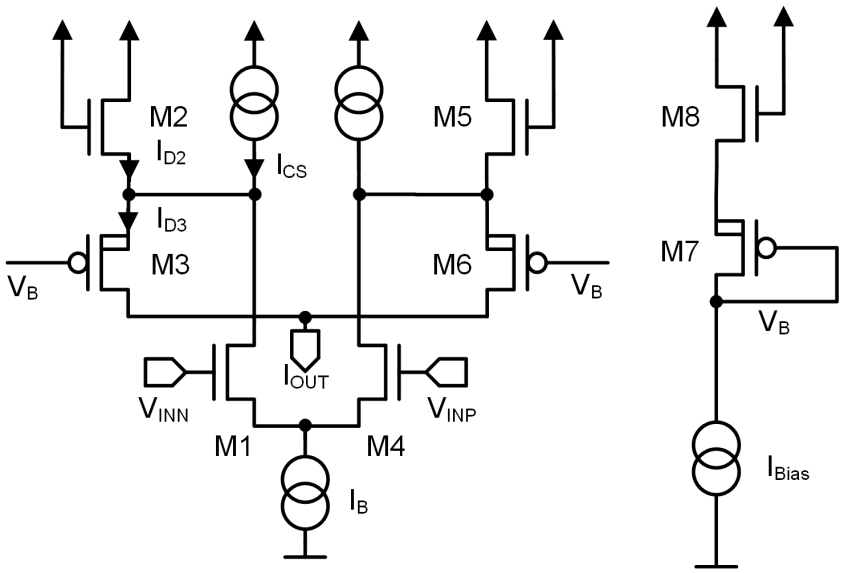


Figure 4.18: Switching rectifier with biasing circuit

The PMOS (M7) of the biasing circuit (figure 4.18 right side) acts as a current mirror with an NMOS diode (M8) at the source. The NMOS load diode (M2, M5) and PMOS (M3, M6) of the gain stage and the bias circuit NMOS/PMOS (M8, M7) have the same geometry. If the same current is flowing at the NMOS load diode and the NMOS of the bias circuit, the same current flows at the PMOS of the gain stage and the PMOS of the bias circuit (I_{Bias}). Additional current through the NMOS load diode leads to less V_{GS} of the PMOS (M3 or M6), so less current through the PMOS. This additional voltage can switch the PMOS almost off. The off current cannot be controlled very well because the PMOS is never switched off completely. A higher voltage is required to switch the PMOS off more properly.

The small signal gain of the circuit is mainly determined by the NMOS load diode ($gm2 + gmbs2 = \eta_N gm2$) the PMOS load ($gm3 = \frac{I_{D3}}{\eta_P U_T}$) and the input transistor (gm1) as stated in equation 4.31.

$$A_0 = \frac{gm1}{gds1 + gm2 + gmbs2 + gds2 + gds_{CS} + gm3 + gds3} \approx \frac{gm1}{gm2 + gmbs2 + gm3} \tag{4.31}$$

$$= \frac{gm1}{\eta_N gm2 + gm3} = \frac{I_B/2}{\eta_N U_T \cdot \left(\frac{I_{D2}}{U_T} + \frac{I_{D3}}{\eta_P U_T}\right)} = \frac{I_B/2}{\eta_N \left(I_{D2} + \frac{I_{D3}}{\eta_P}\right)} \tag{4.32}$$

gm3 has a minor influence on the gain, if the current of the PMOS (I_{D3}) is much smaller than the current of the load diode (I_{D2}, equation 4.32).

Because the PMOS cannot be switched off completely, the current and hence gm2 and gm3 are not well defined. gm2 is mainly determined by $I_{D2} \approx \frac{I_B}{2} - I_{CS}$ similar to the unfolded diode load gain stage. Despite some additional current is flowing over the PMOS, which is depending on the I_{Bias}. This results in an enhanced current of $I_{D2} = \frac{I_B}{2} - I_{CS} + I_{D3}$. The additional current is less then $2I_{Bias}$, thus the current consumption of the gain stage is less than $I_B + 2I_{Bias}$.

4.6.1 Small signal gain variation

Figure 4.19 shows the gain variation over temperature for different process corners. The simulations are performed with a load current of $I_{CS} = 13nA$ and a bias current source of $I_{Bias} = 2nA$. A $W1/L1 = 8\mu m/1\mu m$ of the input transistors, $W2/L2 = 4\mu m/1\mu m$ load and $W3/L3 = 1\mu m/3\mu m$ for the PMOS are chosen. $W3/L3$ does influence the gain significantly but with longer transistors, less gain drift over temperature is observed in the simulation. The gain stage shows a maximum gain drift at the fast process corner of $\Delta A_s \approx 3.5\%$. Also here various effects as described at the previous gain stage have an influence on temperature drift of the gain. A trade-off between current consumption, noise, and gain variation has to be made. With a length of the input and load transistor of $L = 2\mu m$, the gain drift can be minimized to $\Delta A_s \approx 2\%$.

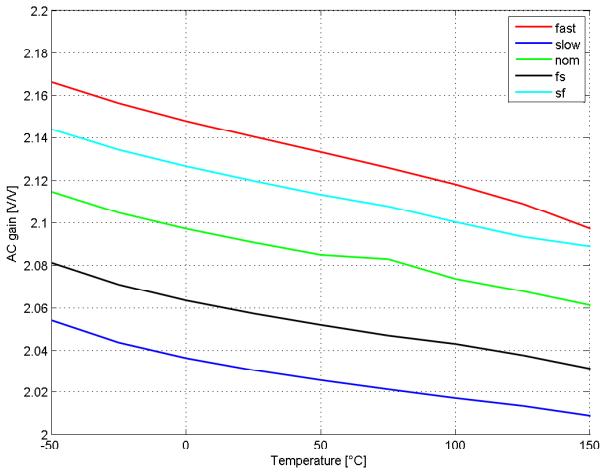


Figure 4.19: Gain variation over temperautre with different process corners

A Monte Carlo simulation of 1000 runs revealed a relative gain variation of approximately $\frac{\sigma}{\mu} \approx 1.7\%$.

4.6.2 -3dB Bandwidth

A bandwidth of $f_{-3dB} \approx 1.38MHz$ can be reached ($W1/L1 = 8\mu m/1\mu m$, $W2/L2 = 4\mu m/1\mu m$, $W3/L3 = 1\mu m/3\mu m$). For the limiting amplifier & RSSI design, there is no C_{GD} miller capacitance of the rectifier as load for the gain stage. This is a great advantage of the circuit in terms of bandwidth. The bandwidth shrinks to $f_{-3dB} \approx 1.0MHz$ when the length of input and load transistors is doubled ($W1/L1 = 8\mu m/2\mu m$, $W2/L2 = 4\mu m/2\mu m$, $W3/L3 = 1\mu/3\mu m$).

4.6.3 White noise

The gain stage has a white noise density of $S_{U^2,in}(f) \approx 270\frac{nV}{\sqrt{Hz}}$. With longer the input transistors ($W/L = 8\mu m/2\mu m$) and the load transistor a white noise density of $S_{U^2,in}(f) \approx 280\frac{nV}{\sqrt{Hz}}$ is reached.

4.6.4 Transient response

The gain stage shows a maximum clipping voltage at 150°C that is smaller than $V_s = 5.35 \cdot \eta U_T$ to fully clip the next rectifier. To solve this issue for a limiter design & RSSI design the clipping voltage V_s can be increased by an additional voltage at the gate of the load diode as was done at the unfolded diode load noise optimized gain stage.

4.7 Folded diode load NMOS

As [3] suggests, the diode loads (M3, M4) can be folded to a current source as shown in figure 4.20. The gain determined by the bias current of the differential pair and the current of the load, which can be set by the folding current I_F (equation 4.33). $2I_F$ is the current consumption of the gain stage and I_B the bias current of the differential pair. $2I_F$ is set to 40nA for the fixed current consumption.

$$A_0 = \frac{gm1}{gm2 + gds2 + gds1 + gds_{cs}} \approx \frac{I_B}{2 \cdot I_L} = \frac{I_B}{2 \cdot (I_F - \frac{I_B}{2})} = \frac{I_B}{2I_F - I_B} \tag{4.33}$$

$$I_B = \frac{A_0 \cdot 2I_F}{1 + A_0} = 2/3 \cdot 2I_F \approx 27nA \tag{4.34}$$

For a gain of 2 a bias current $I_B = 27nA$ is chosen. This bias current leads to a gain of $A_0 \approx 2.07$. An additional voltage V_B at the source of the diodes is added for the DC operating point. In subsection 4.7.5 it is briefly described how V_B can be generated. The bias current source (I_B) requires $V_{DS,SAT}$ and the input transistor a V_{GS}. A $W1/L1 = 8\mu m/1\mu m$ of the input transistors and a $W2/L2 = 4\mu m/1\mu m$ for the load diodes is chosen. This leads to equal current densities (equal IC) of the load and input transistors.

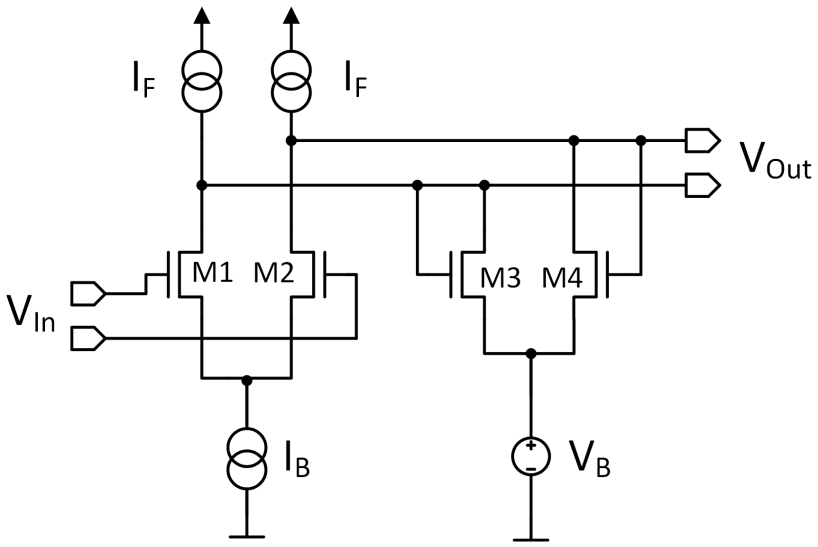


Figure 4.20: Folded diode gain stage

4.7.1 Small signal gain variation

Without the DC voltage V_B at the source of the load diode and a high $W3/L3$, the current source and the load diode will not stay saturated at 150°C fast process corner. With the $V_B = V_{BS}$ (bulk of the NMOS device is fixed to ground) the V_{TH} and the $V_{GS} = V_{DS}$ of the diode is increased. With enough V_B the load diode and the current source will stay saturated at 150°C fast. The small signal gain is not influenced because V_{BS} stays constant with a differential AC input signal ($dV_{BS} = 0$). This assumes a low ohmic voltage source at the source of the load diodes.

The maximum gain drift over temperature with $V_B = 500mV$ is approximately $\Delta A_s \approx 2\%$ at fast process corner. The relative gain variation due to mismatch is approximately $\frac{\sigma(A_s)}{\mu(A_s)} \approx 1\%$.

4.7.2 -3dB Bandwidth

With the given dimensions, the gain stage has a bandwidth of $f_{-3dB} \approx 1MHz$. The bandwidth depends slightly on the source voltages (V_B) of the load diode and the process corner.

4.7.3 White noise

In most cases the input transistors of the differential pair are the main contributors for noise. The folding current $2I_F$ of this gain stage is the current consumption of the gain stage. This current has to be larger than the I_B. The current through the input transistors is $I_B \approx 2/3 \cdot 2I_F$ (equation 4.34). White noise power in weak inversion is indirectly proportional to gm or the current of the transistor (equation 3.31). With a gain of 2 and a fixed bias current, the input referred white noise power density of the input transistors is increased by the factor of 3/2 (equation 4.35).

$$S_{U^2,in}(f) \propto 1/I_B = \frac{1 + A_0}{A_0} \cdot 1/2I_F = \frac{3}{2} \cdot 1/2I_F \tag{4.35}$$

The $\frac{A_0}{1+A_0}$ factor is dependent on the gain with higher gain the factor gets less. On the other hand a larger gain implicates a larger RSSI error. With a gain of e.g. $A_s \approx 3$ ($I_B \approx 30nA$) the gain stage has still a white noise factor of $\frac{A_0+1}{A_0} \approx 1.33$. A simulation shows a white noise density of $S_{U^2,in}(f) \approx 345nV/\sqrt{Hz}$. Also with a gain of 3, a white noise density of $S_{U^2,in}(f) \approx 305nV/\sqrt{Hz}$ can be achieved but this is increased compared to other gain stages.

4.7.4 Transient response

Similar to the unfolded diode load gain stage the gain is getting larger with additional DC input voltage (figure 4.15(c)). This gain enhancement occurs when there is almost no more current through the load diode. This gain peaking also leads to a larger RSSI error.

4.7.5 Source voltage

The source voltage for the load diodes (V_B) has to be generated. A buffer has to provide a low ohmic DC voltage. For the simulation an ideal voltage source is used. There are also other possibility to shift the common mode voltage. Due to bad noise performance the gain stage is not further investigated.

4.8 Other circuits

4.8.1 Strong inversion gain stage

A gain stage can be implemented by operating all transistors in strong inversion like the limiting amplifier of [3] [6] [7] [11] [26] or other publications. The gain is determined by a gm ratio of the input differential pair and a load diode. In strong inversion gm, thus the gain can be set by W/L of the input and load transistors.

With a specified current of 40nA and the minimum width, the length of the transistors has to be sufficiently long to get into strong inversion. The capacitance of the transistors in the technology is large and the bandwidth would be not sufficient any more. A combination of the input transistors in weak inversion and load diode in strong inversion reveals a high temperature dependency of the gain. This is due to the different temperature behavior of gm in weak and strong inversion as described in chapter 3.2.

To use a larger bias current for the gain stage would also operate the transistors in strong inversion, but will consume more current and current consumption of the limiting amplifier has already a tight specification for current consumption.

4.8.2 Gain stage with current mirror

In [6] and [7] there is a current mirror between input and load transistor like in a current conveyor OTA. In [7] also two load diodes in serious are used. This structure has more voltage headroom ($2 \cdot V_{GS} + 1 \cdot V_{DS,sat}$) as the two diodes load gain stage but has the drawback of enhanced current consumption due to additional current paths. The structure reveals either a low bandwidth or increased noise for the given bias current.

4.9 Summarized gain stages parameters

4.9.1 Parameter table - gain stages

All parameters for the compared gain stages from simulation are summarized in table 4.1. This parameters are described in more detail in the introduction chapter 4.1.

	triode	two diodes	unfolded	unfolded noise opt.	unfolded with rect.	folded
input transistor	NMOS	PMOS	PMOS	NMOS	NMOS	NMOS
load transistor	PMOS	PMOS	PMOS	NMOS	N + P MOS	NMOS
$\mu(A_s)$ V/V	2.03	1.96	2.01	2	2.09	2.03
rel. std. $\frac{\sigma(A_s)}{\mu(A_s)} \cdot 100\%$	1.4%	0.1%	1.5%	1.2%	1.7%	1%
rel. drift ΔA_s	1.3%	1.25%	1%	2.5%	3.0%	2%
$A_{s,max} - A_{s,min}$	2.08-1.91	1.99-1.98	2.28-1.92	2.31-1.91	2.38-1.95	2.23-1.90
$f_{-3dB,s}/kHz$	660	750	940	1400	1100	1000
$\frac{S_{U^2,in}(125kHz)}{df} / \frac{nV}{\sqrt{Hz}}$	260	327	370	264	280	345
gain linearity	+	+	-	-	-	-
$V_S \gtrsim 5.3\eta U_T$	✗	✓	✗	✓	✓	✓
$V_S(T) \propto U_T(T)$	✓	✗	✗	✗	✗	✗

Table 4.1: Table for comparison of different gain stages

In table, the sign for gain linearity indicates if the small signal gain over large signal input voltage is increased (-), stays constant or decreases (+). The - sign directly indicates an increased RSSI error. The row $V_S \gtrsim 5.3\eta U_T$ shows if the clipping voltage is larger then $5.3\eta U_T$ to fully clip the rectifier. The last row indicates if the clipping voltage is a PTAT voltage.

4.9.2 Summary - gain stage parameters

Gain drift over temperature

Each gain stage had a gain drift over temperature, which is less than 3 % at all process corners. This leads to a limiting amplifier with 10 stages that has less gain drift then 2.8dB over 200°C. This is sufficient for a temperature stable output RSSI caused by gain drift over temperature.

Bandwidth

All gain stages with the fixed bias current have a sufficient bandwidth, which is larger than $f_{-3dB,s}/kHz \gtrsim 560kHz$, required for the design. The rectifier will further reduce the bandwidth in a limiting amplifier design except for the unfolded diode load with rectifier gain stage.

White noise

The substrate factor η is larger for PMOS compared to NMOS then expected. This leads to an increased input referred white noise voltage density of the gain stages with PMOS input differential pairs compared to NMOS input differential pairs.

4.9.3 Conclusion - gain stage circuits

A figure of merit can be defined with the given parameters. Though there are only the **triode load**, the **unfolded diode load noise optimized** and the **unfolded diode load gain stage with rectifier**, which have a the best noise performance for a given power consumption. Because the overall power consumption of this limiting amplifier design is mainly dependent on the white noise (chapter 7.5), it is reasonable to use these gain stages for a limiting amplifier design.

5 Rectifier circuits

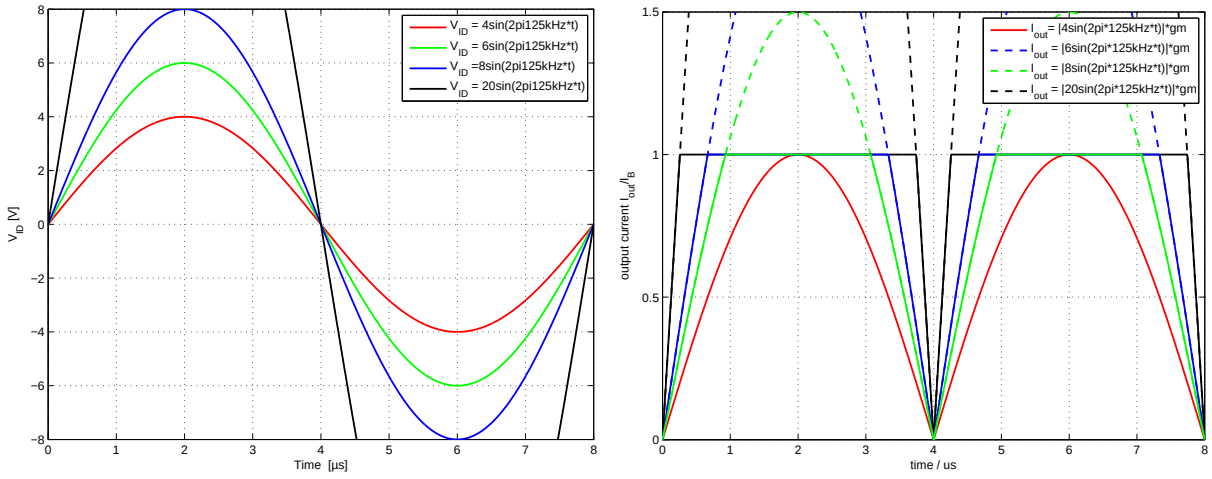
5.1 Introduction to rectifier circuits

This chapter gives some theoretical aspects of rectifier circuits. In the chapters 5.2 - 5.6 different circuits for rectifiers are shown. A full wave rectifier has to convert the differential output voltage of the gain stages to a rectified current. All shown circuits are based on differential pairs. This is necessary to convert a differential voltage signal into a current that is proportional to the input voltage. The most important parameter for comparison is the temperature stability of the output current. The output current is plotted for each rectifier as function of DC input voltage. Additionally the integrated output current in dependency of the amplitude input signal with a frequency of 125kHz is shown. In the time domain the amplitude of V_{ID} has to be larger for the integrated maximum output current of the rectifier compared to the amplitude of the DC input voltage (chapter 5.1.1).

5.1.1 Ideal clipping rectifier

Rectifying and clipping in time domain

In figure 5.1(a), different amplitudes ($V_{ID} = 4V - 20V$) of differential input voltages for an ideal rectifier are depicted. Figure 5.1(b) shows the output current of an ideal clipping rectifier for different input voltages, where gm is the transconductance of the rectifier. Without clipping, the amplitude of the output current from an ideal rectifier is increasing with the magnitude of the input voltage (dotted lines). With clipping, the rectifier current (continuous lines) gets to the maximum current (I_B) when a certain input voltage is exceeded.



(a) Sinusoidal input voltages with different amplitudes

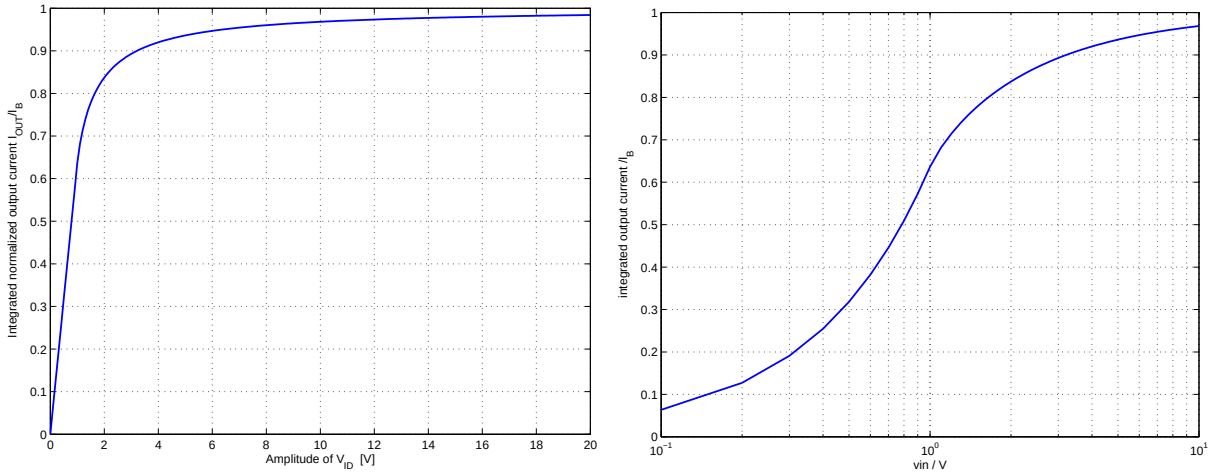
(b) Output current of ideal clipping rectifier

Figure 5.1: Ideal clipping rectifier in the time domain

This ideal model assumes a non differentiable current signal at the zero crossing of the input voltage, therefore it is a simplification. An other discrepancy to the ideal model is steepness of the gain stages output voltage, which is limited to the slew rate of the gain stage.

DC component of rectified clipped output current

The RSSI is the low-pass filter output current of the rectified clipping sinusoidal. An ideal low-pass filter is the integral of the sinusoidal signal over one period. Figure 5.2 shows the integrated output current as a function of input voltage from $\hat{v} = 0\text{V}$ to 20V. The integrated current increases with input amplitudes as can be seen in figure 5.2(a) on a linear scale. Due to a larger input voltage signal of the rectifier, the rising and falling edge are steeper thus the integrated current is larger (figure 5.1(b)) despite clipping of the rectifier. The x-axis scale of figure 2.6(b) for the integrated output current is logarithmic.



(a) Integrated output current as function of input voltage

(b) Integrated output current as function of logarithmic input voltage

Figure 5.2: Intgrated output current as function of input voltage

The clipping voltage of the input signal from the gain stage has no impact on the output current, as long as the rectifier is clipping first. Because the clipping voltage level of a real gain stage varies with temperature, the rectifiers output current should clip before the gain stages output voltage clips. If the slew rate of a real gain stage does not change with temperature, then there will be no temperature dependency of an ideal rectifier.

5.1.2 Ideal rectifier in the frequency domain

The Fourier series of an ideal rectified sine wave in the frequency domain is stated in [27]. The amplitude of the fundamental is shifted to the double frequency. The frequency spectrum has just even multiples of the fundamental frequency as can be seen in equation 5.3.

$$U = |sin(\omega t)| \tag{5.1}$$

$$\begin{aligned} a_0 &= \frac{1}{\pi}\int_{-\pi}^{0} -sin(\omega t)d(\omega t) + \frac{1}{\pi}\int_{0}^{\pi} sin(\omega t)d(\omega t) = \frac{4}{\pi} \\ a_n &= \frac{2}{\pi}\int_{0}^{\pi} sin(\omega t)cos(n\omega t)d(\omega t) \\ &= -\frac{4}{\pi}\cdot\frac{1}{n^2-1} \end{aligned} \tag{5.2}$$

$$\begin{aligned} |sin(\omega t)| &= \frac{2}{\pi} - \frac{4}{\pi}\sum_{n=0,2,4,\ldots}^{\infty}\frac{cos(n\omega t)}{n^2-1} \\ &= \frac{4}{\pi}\left(\frac{1}{2} - \frac{cos(2\omega t)}{3} - \frac{cos(4\omega t)}{15} - \ldots\right) \end{aligned} \tag{5.3}$$

The amplitude of the DC signal is $\frac{2}{\pi}$. An ideal rectifier has to have infinite bandwidth. At the zero crossing the rectified sinusoidal signal is non differentiable. These high frequency components are damped by a finite bandwidth of a real rectifier. However the summed RSSI current of all rectifiers is low-pass filtered, thus the integrated current of the transient simulation from a single rectifier is investigated. The bandwidth of the rectifier does not contribute to the amplitude of the DC current.

5.1.3 Input capacitance

The input capacitance of the rectifier is an additional load capacitance of the gain stage. It is important to minimize the input capacitance of the rectifier for the overall bandwidth of the limiting amplifier. The gain stages require less current for a given bandwidth if the rectifier has a smaller input capacitance. An AC simulation with resistors at the input can be used to determine the bandwidth (f_{-3dB}). With equation 5.4 the input capacitance can be determined.

$$C_{IN} = \frac{1}{2\pi}\cdot f_{-3dB}\cdot R_{IN} \tag{5.4}$$

The input capacitance is also slightly dependent on the common mode input voltage $C_{IN}(V_{CM})$, which is given by the gain stage. Another limiting factor for the size of the input transistor is the length to achieve a certain output resistance and a negligible leakage current when turned off. For matching a minimum area of the input transistors of the rectifier is required.

5.1.4 Large signal temperature dependent output current

A rectifier in CMOS technology does not have a temperature stable output current on the large signal transfer function. Especially when the rectifier is operated in weak inversion a temperature dependent current depending on the large signal input voltage will be generated. Theoretically it is possible to bias the rectifier in strong inversion but this has some drawbacks for this design, which are discussed in the following.

Weak inversion
As shown in chapter 3.10.1 the large signal output current of a differential pair in weak inversion is not temperature constant (equation 5.5). The output current is dependent on the hyperbolic tangent of the large signal input differential voltage divided through U_T. The rectified, summed up RSSI current is then also temperature dependent.

$$\Delta I = I_B \cdot tanh\left(\frac{V_{ID}}{2\eta U_T}\right) \tag{5.5}$$

The output current has an equal temperature coefficient as the bias current, if a large V_{ID}, which is clipping the rectifier or no V_{ID} is applied at the input. If the rectifier is unbalanced but not clipping, the output current has smaller temperature coefficient as the bias current.

Strong inversion
In strong inversion the output current of a differential pair is stated in equation 5.6 from [15].

$$\Delta I = \begin{cases} \frac{1}{2}\mu(T)C_{ox}\frac{W}{L} \cdot V_{ID} \cdot \sqrt{\frac{4 \cdot I_B}{\mu(T)C_{ox}\frac{W}{L}} - V_{ID}^2} & \text{for } |V_{ID}| \leq \sqrt{\frac{2 \cdot I_{Bias}}{\mu(T)C_{ox}\frac{W}{L}}} \\ I_B & \text{for } |V_{ID}| \geq \sqrt{\frac{2 \cdot I_{Bias}}{\mu(T)C_{ox}\frac{W}{L}}} \end{cases} \tag{5.6}$$

The dominating effect of the temperature dependent output current in strong inversion is mobility reduction [18]. By biasing the differential pair or the rectifier with a current of the same TC as $\mu(T)$, the temperature dependency can be compensated. In this case the RSSI current has the same TC as $\mu(T)$ and I_B. This concept is implemented in [28]. It is not possible to operate the rectifier deeply in strong inversion (high IC) in this design, using a low bias current because the length has to be large and the rectifier represents an additional capacitive load of the gain stage. This would reduce the bandwidth of the limiting amplifier for the specified power consumption. When the differential input pair is unbalanced one transistor gets into weak inversion and it is almost switched off. This zero crossing of the input voltage also generates a current with different temperature coefficient. The rectifier needs a high IC that the off-current has a minor influence.

5.1.5 Temperature compensation

Biasing

In strong inversion using a bias current with the temperature coefficient of $\mu(T)$ can compensate the temperature effects on the output current of the rectifier [28]. In weak inversion the rectifiers temperature coefficient cannot be compensated by a bias current.

Current mixing

The RSSI current is the summed output current of the rectifiers, which are based on the output current of a differential pair (chapter 3.10.1, figure 3.6(b)). Thus the temperature coefficient of the RSSI is lower than that of the bias current, if the rectifier is unbalanced. A reference current with a lower temperature coefficient can be used for the RSSI carrier detect comparator or for the datagram demodulation to compensate the temperature error. By mixing a PTAT (I_{PTAT}) with a bandgap (I_{BG}) current, a current with lower temperature coefficient than PTAT can be created. Figure 5.3 shows the schematic of a current mixing block.

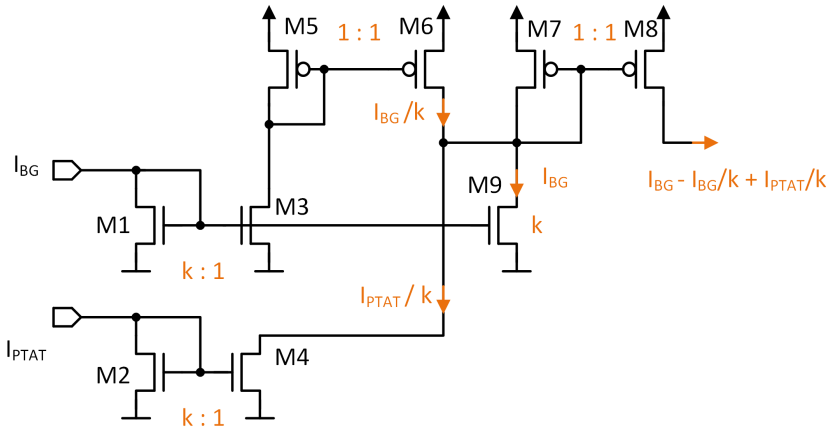


Figure 5.3: Schematic for current mixing

This circuit sums current according equation 5.7, if the two currents have the same I_0. The k-ratio is set by the M1-M3-M9 and M2-M4 current mirrors. Since $TC_{BG} \approx 0$, the mixed current can be simplified as stated in equation 5.8. A 1/k-times smaller temperature coefficient than TC_{PTAT} can be implemented. As TC_{BG} and TC_{PTAT} varies with process and mismatch, also $\sigma(TC_{MIX})$ varies (equation 5.9). The COV(BG, PTAT) (covariance) is used because the two currents are correlated to each other. In simulation $\sigma(TC_{MIX})$ is larger than the single variances. Further mismatch of I_0 and mismatch of the M1-M3-M9 and M2-M4 current mirrors creates additional mismatch of TC_{MIX}.

$$\begin{aligned} I_{MIX}(T) &= I_{BG} - I_{BG}(T)/k + I_{PTAT}(T)/k \\ &= I_0 * (TC_{BG} * (T - T_0)) + I_0/k \cdot ((TC_{PTAT} - TC_{BG})(T - T_0)) \qquad (5.7) \\ &\approx I_0 \cdot \left(1 + \frac{TC_{PTAT}}{k}(T - T_0)\right) = I_0\,(TC_{MIX}(T - T_0)) \qquad (5.8) \end{aligned}$$

$$\sigma\,(TC_{MIX}) = \sqrt{\sigma^2(TC_{PTAT}) + \sigma^2(TC_{BG}) + 2COV(TC_{PTAT}, TC_{BG})} \qquad (5.9)$$

In a reference design better results for the carrier detect threshold voltage are achieved by using an equal bias current for the rectifier and the carrier detect- and datagram comparator with no additional mixed current.

5.2 Gilbert cell rectifier

The Gilbert cell is a mixer or multiplier used for modulating a signal with another signal. It is also possible to rectify a signal if the two differential inputs are shortened. Figure 5.4 shows a gilbert cell with NMOS transistors, at which both inputs are shortened.

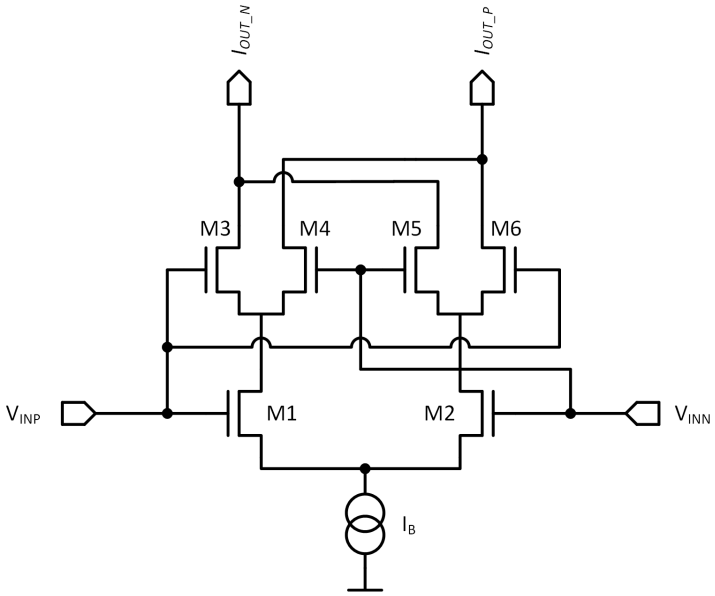


Figure 5.4: Schematic of the gilbert cell rectifier with shortened differential inputs

The lower two NMOS (M1 and M2) are not saturated ($V_{DS,SAT} \gtrsim 4 \cdot U_T$, equation 3.11), without applied input voltage. With positive increasing V_{ID}, more current is flowing at M1. M2 is limiting the current because it gets saturated. There will be a temperature dependency of the output current depending on V_{ID} due to the upper saturated transistors (M3-M6). The transient output currents of the gilbert cell at three different amplitudes of differential input voltage with 125kHz is shown in figure 5.5.

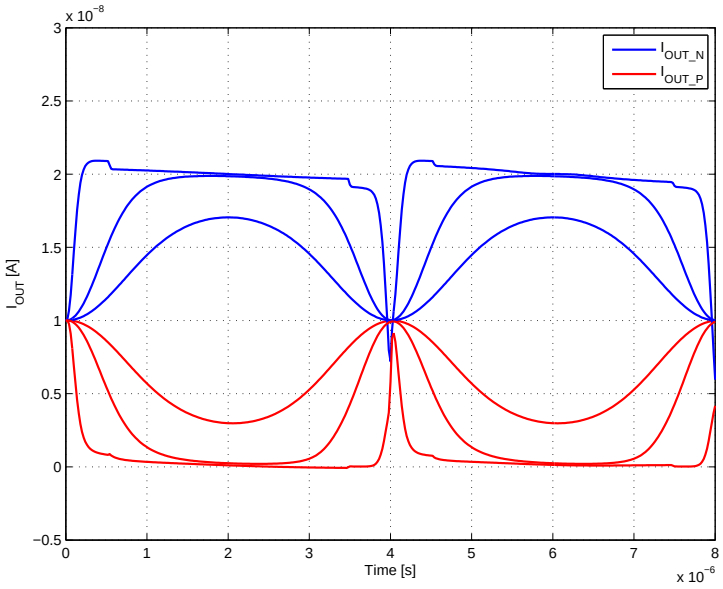
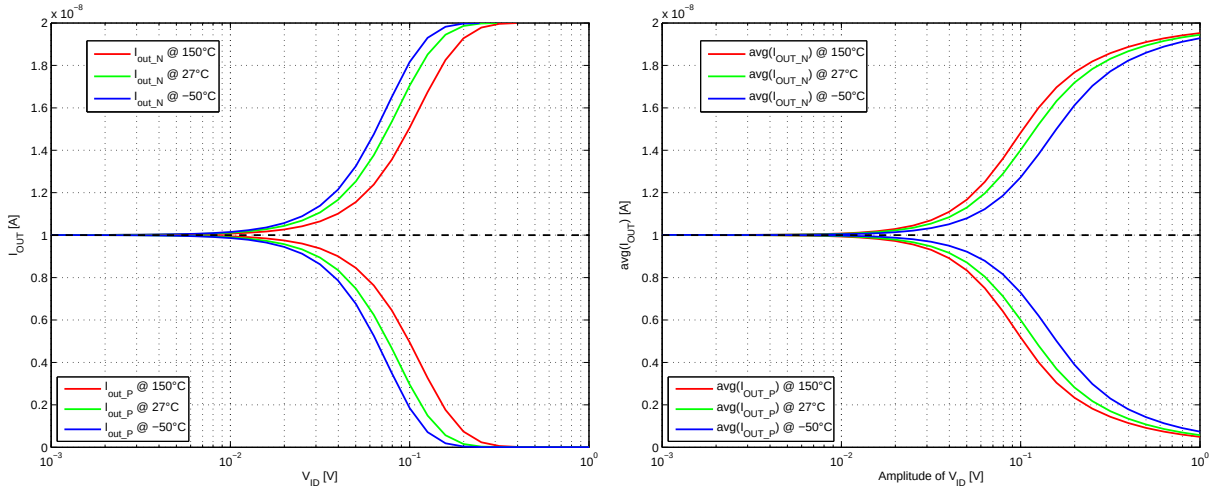


Figure 5.5: I_{OUT_P} and I_{OUT_N} over time

I_{OUT_N} (blue) increases and I_{OUT_P} (red) decreases with a positive differential input voltage. With large differential signals at the input the I_{OUT_N} has a slightly different behavior than the I_{OUT_P} mirrored to half of the bias current. This rectifier is implemented in a reference design but only one current branch (I_{OUT_N} or I_{OUT_P}) is used for the carrier detect comparator, which reveals better results than using both branches.

Figure 5.6(a) shows the DC output current of the gilbert cell as function of a DC input voltage and different temperatures. When the rectifier is unbalanced the current is depending on temperature with a negative temperature coefficient. For higher temperatures there is less current ($|\Delta I_{OUT}|$) compared to low temperature at equal V_{ID}.



(a) DC output current over input voltage

(b) Averaged output current over amplitude of a 125kHz input voltage

Figure 5.6: Comparison DC and transient output current of the gilbert cell

Figure 5.6(b) shows the integrated transient output current of the rectifier over the amplitude of a 125kHz input signal applied. The rectifier shows a similar behavior as in the DC domain.

5.3 Diode mirror with current source rectifier

This rectifier is briefly described in [6]. The two current sources of figure 5.7 are PMOS transistors. Each of the sources provides a current of I_R. The load of the differential pair is a diode current mirror (M1-M3, M2-M4). The rectifier is biased such that there is some current flowing over the diodes (I_{D1} and I_{D2}). The two currents are summed up to the rectified output current.

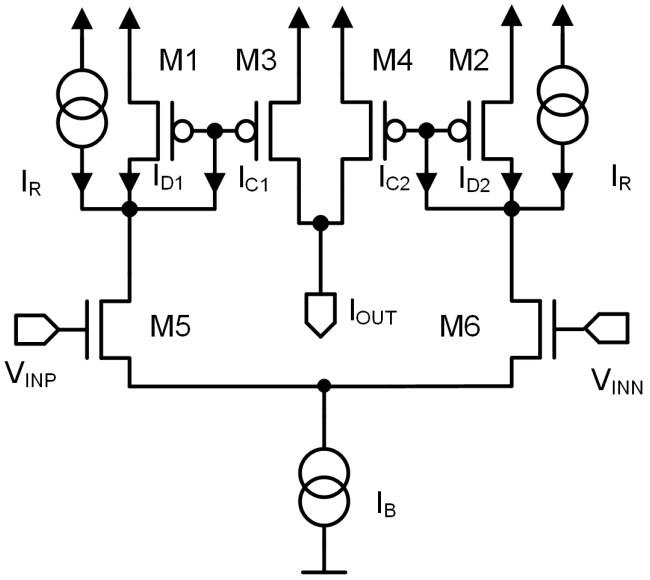


Figure 5.7: Schematic of diode mirror with current source rectifier

The output current is at its minimum (equation 5.10) when no differential input voltage is applied to the rectifier. One current source is switched off when a large V_{ID} is applied to the rectifier. For this case the output current is at the maximum, stated in equation 5.11.

$$I_{OUT,min} = I_B - 2 \cdot I_R \tag{5.10}$$

$$I_{OUT,max} = I_B - I_R \tag{5.11}$$

If there is a small positive V_{ID}, I_{OUT} stays constant at $I_{OUT,min}$ because I_{D1} increases and I_{D2} decreases at the same rate. Both currents are summed with the two PMOS current mirror transistors. I_{OUT} stays constant until there is a V_{ID} large enough that no more current flows through one diode (equation 5.12). The circuit starts to rectify when an input differential voltage larger than equation 5.12 is applied.

$$V_{ID} \geq 2\eta U_T \cdot arctanh\left(\frac{I_{D1} + I_{D2}}{I_B}\right) = Vmin \tag{5.12}$$

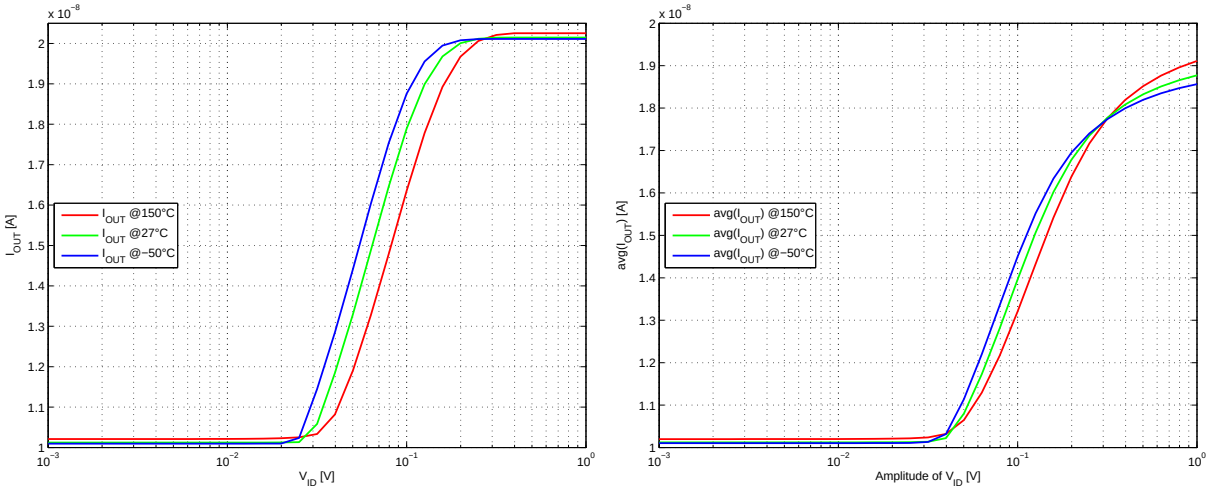
A larger differential input voltage than $Vmin$ is rectified to a single ended output current with an offset current (equation 5.13). In this operating range the rectifiers output current is directly proportional to the input voltage.

$$I_{OUT} = \begin{cases} I_{D1} - I_R = \frac{I_B}{1+e^{\frac{-V_{ID}}{\eta U_T}}} - I_R & \text{for } V_{ID} \gtrsim Vmin \\ I_{D2} - I_R = \frac{I_B}{1+e^{\frac{V_{ID}}{\eta U_T}}} - I_R & \text{for } V_{ID} \lesssim -Vmin \end{cases} \tag{5.13}$$

The output current over the whole range of the input voltage is stated in equation 5.14. The output current when the rectifier is rectifying and the output current lower than the maximum, the output current is temperature dependent, due to the U_T in the exponential function.

$$I_{OUT} = \begin{cases} I_{D1} + I_{D2} - 2 \cdot I_R = I_B - 2 \cdot I_R & \text{for } |V_{ID}| \lesssim Vmin \\ \frac{I_B}{\left(1+e^{\frac{-|V_{ID}|}{\eta U_T}}\right)} - I_R & \text{for } Vmin \lesssim |V_{ID}| \lesssim 4 \cdot U_T \\ I_{D1} + I_{D2} - I_R = I_B - I_R & \text{for } |V_{ID}| \gtrsim 4 \cdot U_T \end{cases} \tag{5.14}$$

The DC output current at different temperatures of the rectifier is shown in figure 5.8(a). In the range of $Vmin \lesssim |V_{ID}| \lesssim 4 \cdot U_T$ the output current is less at higher temperatures.



(a) DC output current over input voltage

(b) Averaged output current over amplitude of a 125kHz input voltage

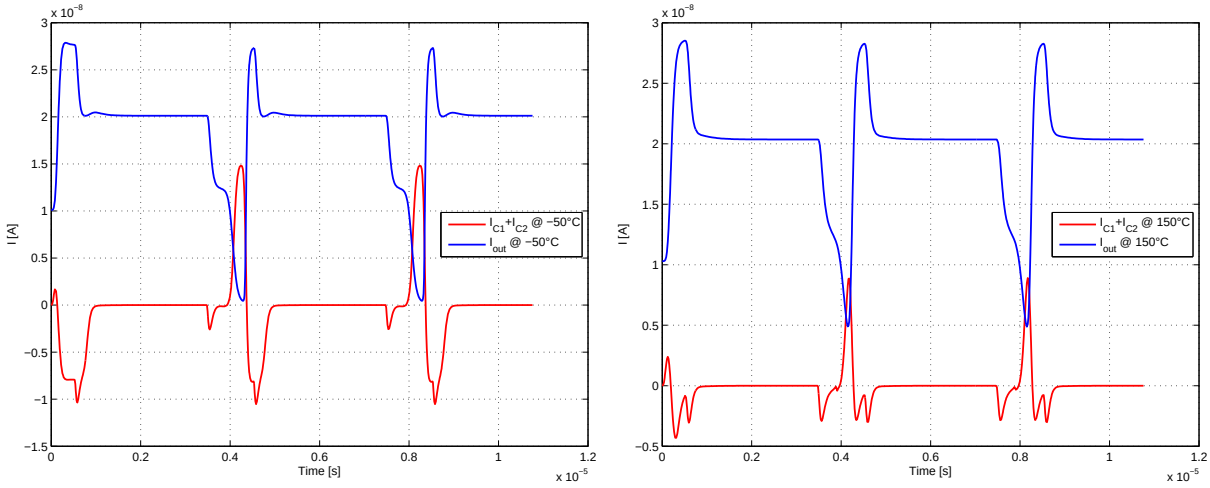
Figure 5.8: Comparison DC and transient output current of the diode mirror with current source rectifier

Figure 5.8(b) shows the output current with a 125kHz signal applied. In the transient simulation with high V_{ID} there is a compensating factor of less current at higher temperatures. In this region the rectifier provides more output current at high than at low temperatures.

If the rectifier is completely unbalanced or clipped, almost no current is flowing over one diode. At the zero crossing of the input signal the gate source capacitance of that diode is loaded from zero until a certain V_{GS} such that almost all current flows over that diode. V_{GS} is temperature dependent and can be calculated from equation 3.1.

To load the diodes capacitance (M1-M3 or M2-M4) to a certain V_{GS}, charge is transfered to the gate capacitance as can be seen in figure 5.9 at two different temperatures. The blue curve shows I_{OUT} over time. The red curves are the parasitic currents ($I_{C1} + I_{C2}$), flowing at the gate capacitances of the current mirror. The parasitic current is subtracted from the drain current of M1 and M2, which is mirrored to the output. This subtraction of the parasitic current leads to less integrated output current I_{OUT} of the rectifier.

More charge is flowing into the gate capacitance (red line) at low temperature (figure 5.9(a)) than at high temperature (figure 5.9(b)). This parasitic current is subtracted from the output current (blue line). Thus there is a smaller integrated current at lower temperature at the output than at high temperature with a large input signal (figure 5.8(b)).



(a) Output current and parasitic current at -50°C

(b) Output current and parasitic current at 150°C

Figure 5.9: Transient currents at different temperatures with $V_{ID} = 1V$

The effect of the redistribution charge depends mainly on the capacitance, the slew rate and V_{GS} of the current mirror. V_{GS} of the diode load is dependent on temperature, process corners and bias current. With a fixed bias current, V_{GS} is different at different process corners due to threshold voltage variations. If the rectifier is biased with higher current the loading/unloading of the capacitance takes shorter time. For more current across the diode, V_{GS} is increased slightly because of the exponential current to voltage behavior. The ratio of lost charge to the overall output charge when the slope changes is smaller with higher bias current. If the rectifier is biased with a PTAT current, the redistribution of charge takes longer for a smaller temperature because there is less current at lower temperatures and the slew rate is smaller.

The capacitance of the mirror, which is directly proportional to the area of the mirror has influence on the averaged output current. To minimize the effect the area of the current mirror can be scaled down. A $W/L = 0.8\mu m/5\mu m$ for the PMOS current mirror is used as a compromise between minimizing this effect by area and the matching of the mirror.

5.4 Differential pair against common mode rectifier

A modified differential pair (M1, M2) with current mirror (M4,M5) load, shortened output and a third input transistor (M3) can be used for rectifying a signal [11]. The schematic is shown in figure 5.10. The differential pair is unbalanced to the common mode voltage of the inputs (V_{CM}). If the input transistors work perfectly linearly, there is no rectified signal until no more current is flowing over one of input transistors. At that point the rectifier starts to rectify and one branch of the differential pair is then steered against the common mode voltage.

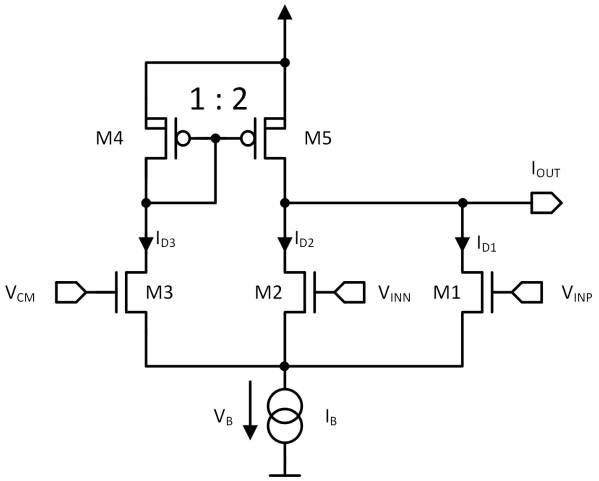


Figure 5.10: Differential Pair Rectifier with Common Mode compensation

The differential pair has a current mirror load so the currents can be subtracted like in equation 5.17. With a positive V_{ID} there is more current flowing through one input transistor as the other transistor is blocking. The overall sum of the two currents ($I_{D1} + I_{D2}$) is larger with an applied input voltage. The derivation of the output current (equation 5.18) is done like in [14] for a simple differential pair.

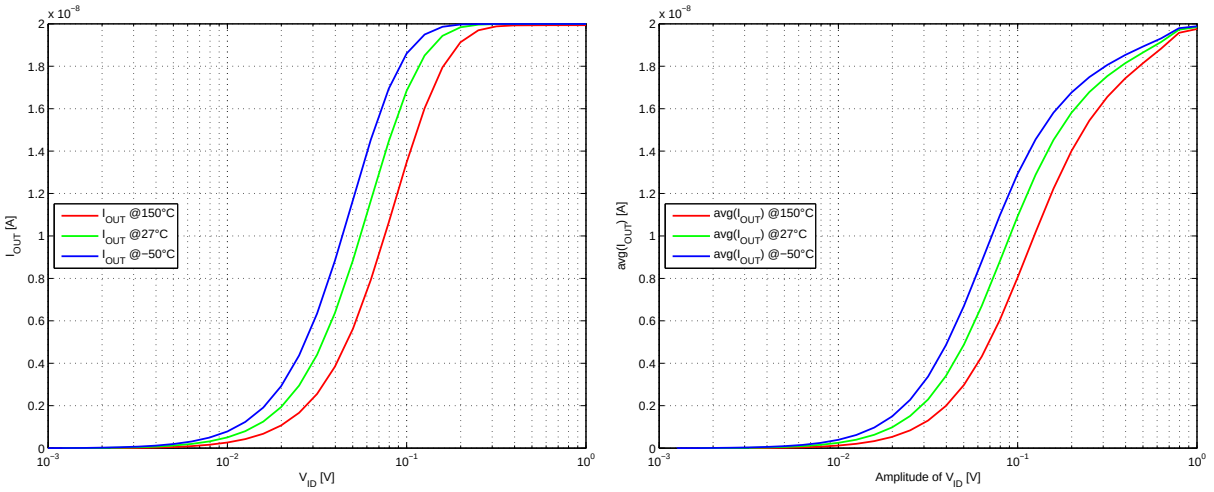
$$I_{D1} = I_0 \cdot \frac{W}{L} \cdot e^{\frac{V_{ID}+V_{CM}-V_B}{\eta U_T}}; \quad I_{D2} = I_0 \cdot \frac{W}{L} \cdot e^{\frac{-V_{ID}+V_{CM}-V_B}{\eta U_T}};$$
$$I_{D3} = I_0 \cdot \frac{W}{L} \cdot e^{\frac{V_{CM}-V_B}{\eta U_T}} \tag{5.15}$$
$$\frac{I_{D1}}{I_{D2}} = e^{\frac{2V_{ID}}{\eta U_T}}; \quad \frac{I_{D3}}{I_{D1}} = e^{\frac{-V_{ID}}{\eta U_T}}; \quad \frac{I_{D3}}{I_{D2}} = e^{\frac{V_{ID}}{\eta U_T}} \tag{5.16}$$

$$I_{D1} = \frac{I_B}{1 + e^{-2x} + e^{-x}}; \quad x = \frac{V_{ID}}{\eta U_T}$$
$$I_{D2} = \frac{I_B}{1 + e^{2x} + e^{x}}; \quad I_{D3} = \frac{I_B}{1 + e^{x} + e^{-x}}$$
$$I_{out} = I_{D1} + I_{D2} - 2 \cdot I_{D3} \tag{5.17}$$
$$= I_B \cdot \left(\frac{1}{1 + e^{2x}} + \frac{1}{1 + e^{-2x} + e^{-x}} - \frac{2}{1 + e^{x} + e^{-x}} \right)$$
$$= I_B \cdot \left(1 - \frac{3}{2 \cdot cosh(x) + 1} \right) \tag{5.18}$$

The cosh(x) function is an even function and the output current is also an even function. The circuit works as rectifier. The transconductance is stated in equation 5.19. Also this rectifier provides less current at high temperatures in the linear range.

$$gm = \frac{I_{out}}{dV_{ID}} = \frac{I_B}{\eta U_T} \frac{6 \cdot sinh(x)}{(2 \cdot cosh(x) + 1)^2} \tag{5.19}$$

Figure 5.11(a) shows the dc output current for different temperatures as function of the DC input voltage. At $V_{ID} = 0V$ there is no output current. The maximum output current is the bias current. The minimum and maximum current is temperature independent. In the linear operating region of the rectifier there is a temperature dependent output current due to the $x = \frac{V_{ID}}{\eta U_T}$ inside the cosine hyperbolic function of equation 5.18.



(a) DC output current over input voltage

(b) Averaged output current over amplitude of a 125kHz input voltage

Figure 5.11: Comparison DC and transient output current of the differential pair against common mode rectifier

Figure 5.11(b) shows the integrated output current over the amplitude of a 125kHz differential input voltage.

One disadvantage of the rectifier is that the common mode of the input voltage has to be generated. This can be done for one gain stage or for all gain stages. Not only mismatch of the differential input transistors but additionally mismatch of the common mode voltages of the gain stages will generate a DC current.

5.5 Unbalanced differential pair rectifier

The circuit is first mentioned in [28] and also many other publications for limiting amplifiers & RSSI like [6] or [7] use this rectifier. The unbalanced differential pair rectifier is built of two differential pairs (M1 and M2, M3 and M4) with different W/L ratios. gm of the larger transistor ($k \cdot W/L$) is increased because more current flows over the larger transistor.

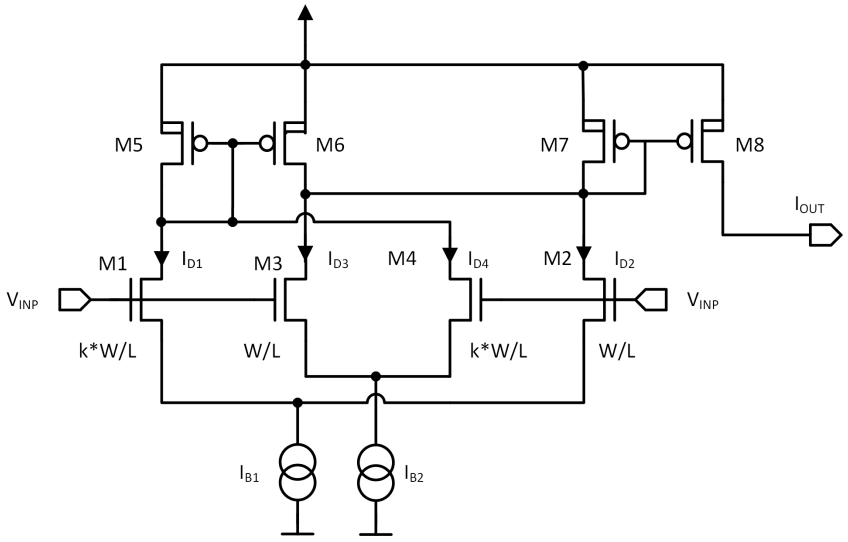


Figure 5.12: Schematic of the unbalanced differentialpair [26]

The outputs of the pairs are shortened and the currents are subtracted from each other (equation 5.22). The large signal output current for strong inversion is derived in [28]. I_{OUT} of the rectifier is stated in equation 5.24 for weak inversion. I_{OUT} until zero with increasing V_{ID}, thus this is an inverting structure. The delta-current range depends on k, with high k the delta-current is approximately $2I_B$.

$$I_B = I_{B1} = I_{B2} = I_{D1} + I_{D2} = I_{D3} + I_{D4} \tag{5.20}$$

$$I_{D1} = \frac{I_B}{k+1}; \quad I_{D4} = \frac{k \cdot I_B}{k+1} \tag{5.21}$$

$$I_{OUT} = I_{D1} - I_{D2} + I_{D3} - I_{D4} \tag{5.22}$$

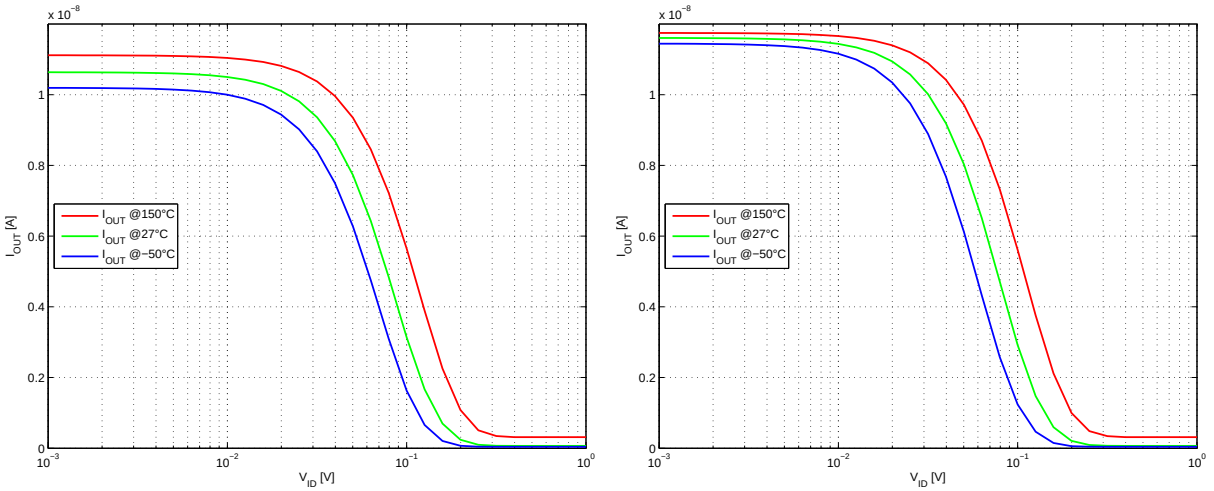
$$\Delta I1 = I_{D1} - I_{D2} = I_B \left(\frac{1}{1 + \frac{1}{k} e^{\frac{V_{ID}}{\eta U_T}}} - \frac{1}{1 + k e^{\frac{-V_{ID}}{\eta U_T}}} \right)$$

$$\Delta I2 = I_{D4} - I_{D3} = I_B \left(\frac{1}{1 + \frac{1}{k} e^{\frac{-V_{ID}}{\eta U_T}}} - \frac{1}{1 + k e^{\frac{V_{ID}}{\eta U_T}}} \right) \tag{5.23}$$

$$I_{OUT} = \Delta I1 + \Delta I2 = 2I_B \left(\frac{k}{k + e^{\frac{V_{ID}}{\eta U_T}}} - \frac{1}{k e^{\frac{V_{ID}}{\eta U_T}} + 1} \right) \tag{5.24}$$

The output current of equation 5.24 is an even function for $k \neq 1$ and $k \neq 0$. Also the output current is temperature dependent because the exponential function is dependent on the large signal differential input voltage and the thermal voltage. I_{OUT} equals approximately $2I_B(\frac{k-1}{k+1})$ without applying an differential input voltage. With a bias current of $2I_B = 20nA$ and k =4 the output current is approximately $I_{OUT} \approx 2I_B \cdot \frac{4-1}{4+1} = 12nA$.

Equation 5.21 assumes the input transistors have an equal operating point. This is approximately valid, if the transistors a operated deeply in weak inversion (low IC) or deeply in strong inversion (high IC). With small input voltages, the rectifier will generate a temperature dependent current as can be seen in 5.13(a) on the left side.



(a) I_{OUT} of a unbalanced differential pair rectifier with DC input voltage W/L = 2, k=4

(b) I_{OUT} of a unbalanced differential pair rectifier with DC input voltage W/L = 8, k=4

Figure 5.13: comparison DC and transient output current

To achieve a low inversion coefficient for a given bias current ($2I_B = 20nA$) the W/L ratio has to be very high to operate deeply in weak inversion or very low for strong inversion. This means for weak inversion a W/L = 8, L_{min} is used for the simulations. If the input transistors operate deeper in weak inversion, the temperature dependency of the DC current decreases as can be seen in figure 5.13(b). For a high W/L, even with L_{min} the capacitive load of the rectifier is to large for the gain stage with a certain bias current to satisfy the bandwidth specifications for a receiver.

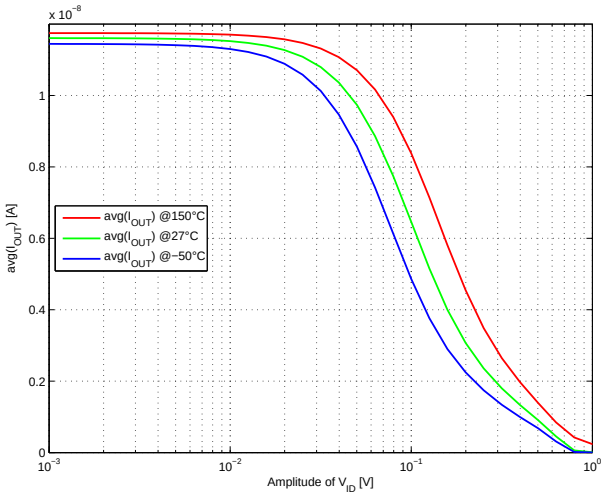


Figure 5.14: averaged ouputcurrent W/L = 8, k=4

Another possibility to operate deeply in weak inversion is to bias the rectifier with a very low current. This is not investigated due to the questionable model validity when biased with a smaller current (chapter 3.4.3) and possible cross talk to high ohmic nodes.

5.6 Unfolded diode load with rectifier gain stage

The topology has the same structure as the unfolded gain stage, except for the PMOS. So it can be used as gain stage and as rectifier at the same time. The gain stage properties of this circuit are described in chapter 4.6. Here, the principle and the characteristics of the rectifier are described. Less current flows at one side of the differential pair (M1) with a positive V_{ID} applied, thus there will be also less current at the NMOS load diode (M2). On this side, $|V_{GS}|$ of the PMOS (M3) increases and more current flows over the PMOS leading to an larger I_{OUT}. On the other side, more current flows into the differential pair (M4). This additional current flows at the NMOS diode (M5) into the differential pair. This reduces $|V_{GS}|$ of the PMOS (M6), which is almost switched off. In total I_{OUT} increases with increasing $|V_{ID}|$.

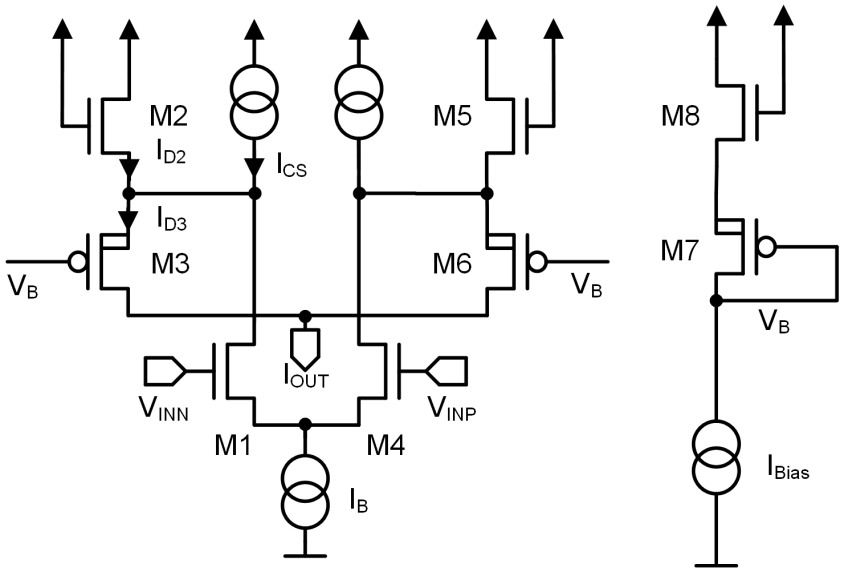
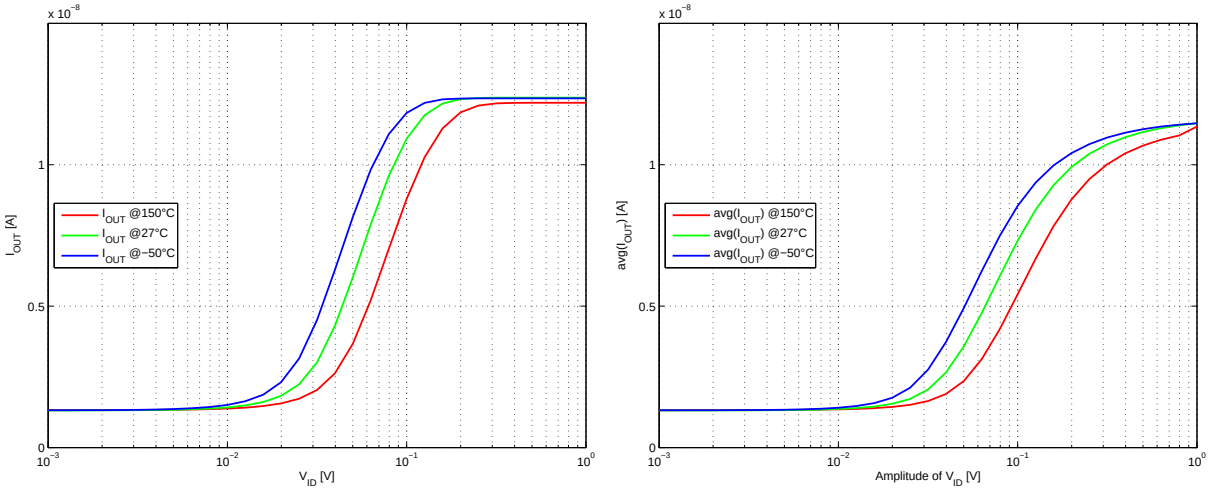


Figure 5.15: Schematic of unfolded diode load with rectifier gain stage

Figure 5.16 shows the output current (I_{OUT}) as a function of V_{ID} at different temperatures. The PMOS is never switched off completely because this requires a very low V_{GS}.



(a) DC output current over input voltage

(b) Integrated output current over amplitude of a 125kHz input voltage

Figure 5.16: Comparison of DC and transient I_{OUT} of the unfolded diode load with rectifier gain stage

The NMOS diode in the biasing circuit creates the gate potential (right side figure 5.15) and the source potential of the PMOS (M3, M6) is determined by the NMOS load diode. A small current flows without V_{ID} at the PMOS switch with $W/L = 1\mu m/3\mu m$ as shown in figure 5.16. When additional current flows in or out of the differential pair, it switches either the PMOS on or off as mentioned in [3].

The current consumption of the unfolded diode load with rectifier gain stage is determined by the biasing current, which is set to $I_B = 40nA$ for the gain stage comparison (chapter 4). The maximum output current (current of the load current source I_{CS}) is flowing when the differential pair is completely unbalanced. I_{CS} is set to 13nA, such that the gain stage has a gain of $A_s \approx 2$.

The rectifier has also a temperature dependent output current. When the gain stage or rectifier is unbalanced and not clipped less current is flowing at high temperature. A limiting amplifier design with the circuit reveals very high bandwidth but also a temperature dependent RSSI. Thus it is not further investigated for this thesis.

5.7 Conclusion - rectifier

Temperature dependent output current
All rectifiers have a temperature dependent output current caused by the unbalanced input differential pair operated in weak inversion. This leads to a temperature dependent RSSI current when an input signal is applied because the limiting amplifier is composed of rectifiers. In the case that the rectifiers are balanced (no input voltage), the output current stays temperature constant for most of the investigated rectifiers. Also when clipping, most investigated rectifiers generate a temperature constant output current.

Diode mirror with current source rectifier
The diode mirror with current source rectifier has a compensating effect when it is clipped with a sinusoidal signal. This effect can be exploited to generate a more temperature constant RSSI current. For the further limiting amplifier design, this rectifier showed more temperature stable output current than other rectifiers.

6

Initial limiting amplifier & RSSI concept

6.1 PMOS limiting amplifier

The initial idea of the master thesis was the limiting amplifier design with the unfolded PMOS diode load gain stage (chapter 4.4) and the diode mirror current source rectifier (chapter 5.3) because gain stage and rectifier have the same structure. Figure 4.19 shows the schematic of the gain stage in parallel to the rectifier. The gain stage has PMOS load diodes (M5, M6) for a good matching between input PMOS and load diodes, the rectifier has NMOS diodes (M7, M8) for the output current mirror. Gain stage and rectifier are biased with equal currents ($I_{B1} = I_{B2}$) and have an equal load current source ($I_{R1} = I_{R2}$).

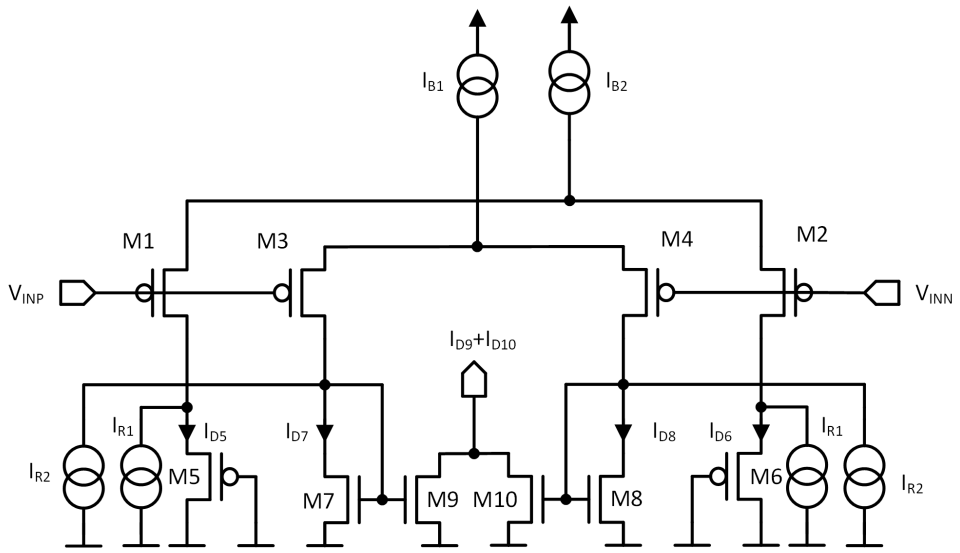
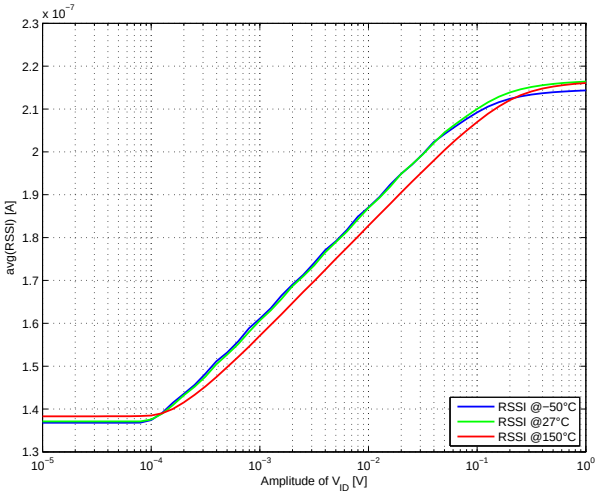


Figure 6.1: Schematic of PMOS unfolded diode load gain stage and diode mirror with current source rectifier

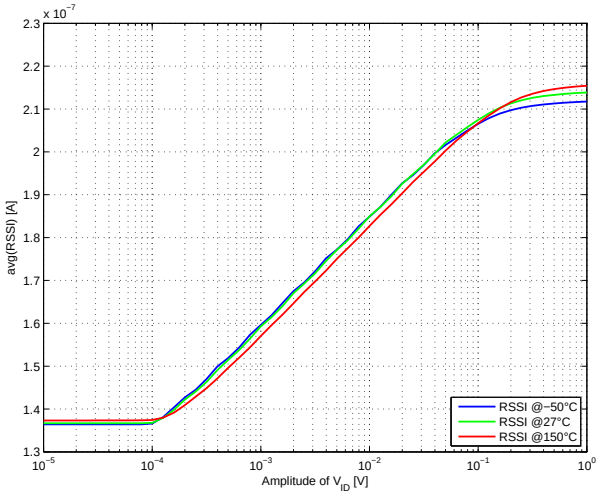
The rectifier starts to rectify when no more current flows at one side of the gain stages diodes ($I_{D5} = 0$ or $I_{D7} = 0$), this is the point where the gain stage clips. At that point the gain stage exceeded the gain maximum over large signal input voltage (shown in figure 4.15(c)). This reduction of gain lowers the RSSI ripple caused by large gain.

6.2 Low-pass filtered RSSI - process corner simulation

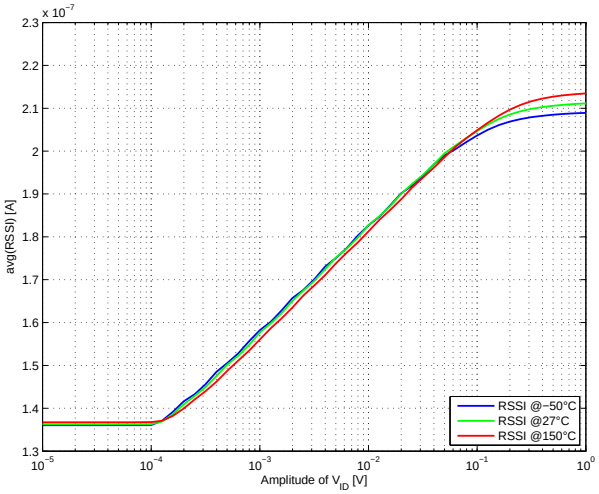
The first simulation result shows a good temperature stability of the RSSI current at all process corners. Figure 6.2 shows the low-pass filtered RSSI current with a logarithmic amplitude of the input voltage at -50°C (blue), 27°C (green) and 150°C (red) at different process corners. The goal is to generate a temperature constant, logarithmic RSSI current at all process corners. The tightest specifications are for the carrier detection amplitude of the input signal (chapter 2.2.1).



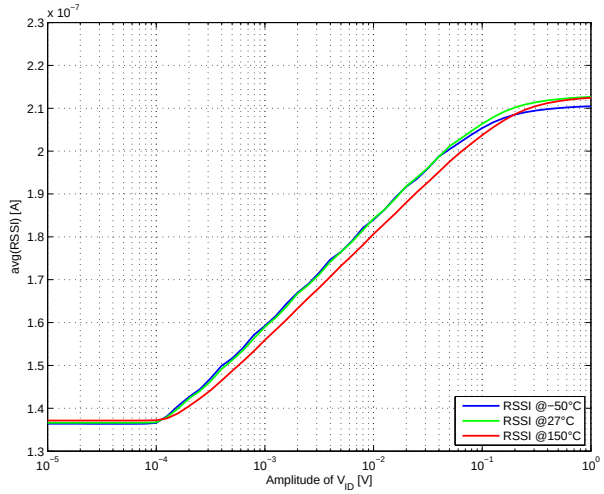
(a) RSSI at fast process corner



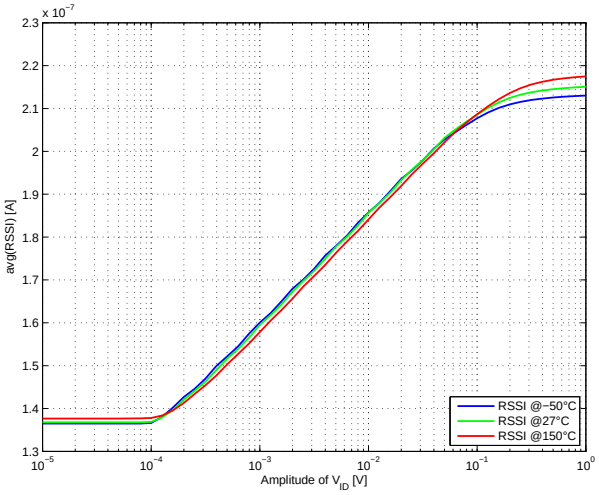
(b) RSSI at nom process corner



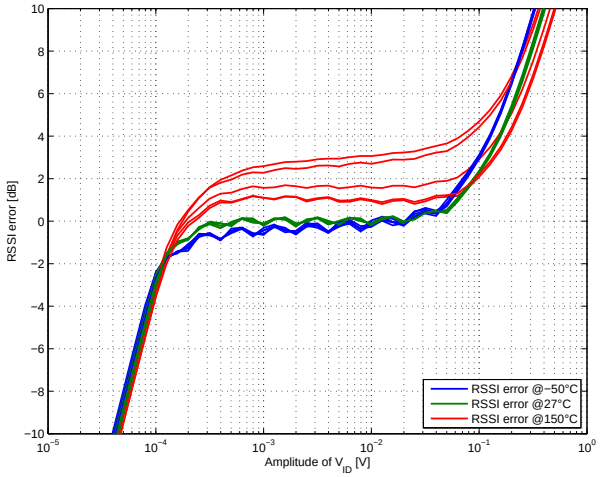
(c) RSSI at slow process corner



(d) RSSI at SF process corner



(e) RSSI at FS process corner



(f) RSSI error for all corners

Figure 6.2: Low-pass filtered RSSI current at different process corners

6.2.1 PVT effects on RSSI

At the fast (figure 6.2(a)) and the sf corner (figure 6.2(d)) at 150°C, the RSSI current is smaller than the RSSI current at 27°C. The clipping output voltage of the gain stage at the 150°C fast corner is too small to fully clip the rectifier (chapter 4.4). A possible solution to fully clip the rectifier at 150°C fast is to increase the gate potential of the load diode. The RSSI error is the difference to an ideal fitting log-function as described in chapter 2.1.2. In the worst case, the RSSI error is approximately 3dB at 150°C and the fast process corner (figure 6.2(f)).

The redistribution of charge at the gate source capacitor of the rectifiers current mirror is compensating less current at higher temperatures of the differential input pair (chapter 5.3). The RSSI is higher at high temperatures and can be seen in the figures 6.2(a) - 6.2(e) at a $vin > 100mV$ when all rectifier are clipping.

6.2.2 Biasing effects on RSSI

The rectifiers and the gain stages are biased with an same PTAT current. This PTAT current for the gain stages is required for a temperature constant bandwidth of the limiting amplifier. The RSSI current and the reference current for the carrier detect comparator are also PTAT currents as shown in figure 6.3. The TC of the PTAT RSSI current can be referred to a temperature constant RSSI current (I_0) by calculating the temperature independent current $I_0 = \frac{I(T)}{(1+TC(T-T_0))}$. This is also done in figure 6.2 to compare the RSSI PTAT currents at different temperatures.

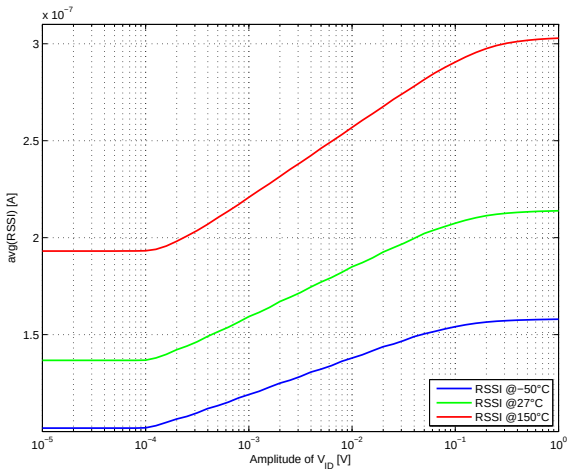


Figure 6.3: PTAT RSSI at nom process corner

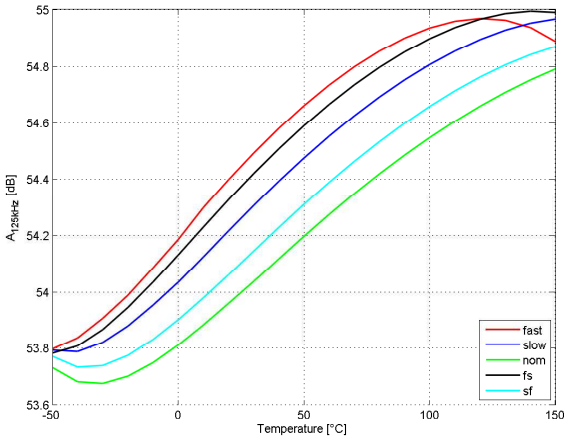


Figure 6.4: AC limiter gain over temperature at different process corners

6.2.3 Small signal gain - Process corner simulation

A maximum drift of $\Delta A_{125kHz} = 55dB - 53.8dB = 1.2dB$ over 200°C at fast process corner is shown in figure 6.4. The transistors in this example are not biased deeply in weak inversion and the current densities (chapter 4.4, page 52) of the gain stages and rectifiers input and load diode are not equal.

6.2.4 Noise performance of the PMOS gain stage

As already seen in chapter 4.4 the noise of the PMOS gain stage is larger mainly due to the higher subthreshold slope of PMOS compared to NMOS. The next chapter shows the design of an improved limiting amplifier with NMOS input pair for better noise performance.

7 Improved limiting amplifier & RSSI

7.1 NMOS limiting amplifier

Due to the lower noise of the NMOS gain stage structure, the gain stages and the rectifiers are built with NMOS input transistors. Figure 7.1 shows the schematic of the NMOS limiting gain stage and rectifier cells. In this schematic gain stage and rectifier are drawn separately, because the rectifier and gain stage are biased with different currents.

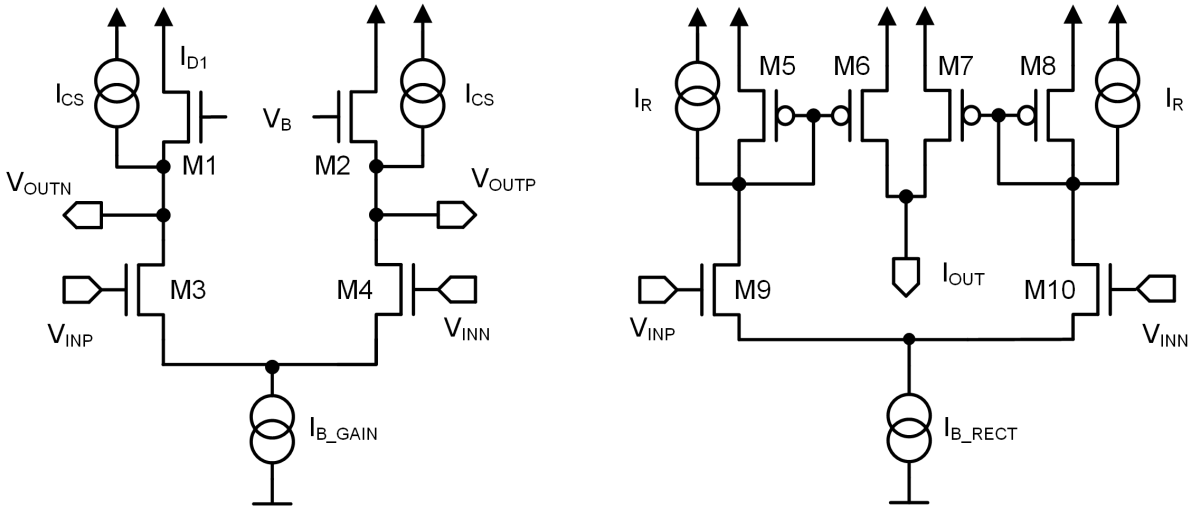


Figure 7.1: Schematic of noise optimized NMOS unfolded diode load gain stage and diode mirror with current source rectifier

The gate voltage of the NMOS diode (V_B) is lower than V_{DD}. The voltage is generated as shown in chapter 4.5. The purpose is to increase the clipping voltage of the gain stage and to clip the rectifier at all temperatures and process corners (described in section 7.3.1). A buffered 1.2V bandgap voltage of the chip could also be used as well for a lower gate voltage.

7.2 Biasing currents for gain stage and rectifier

The single gain stages are biased with a PTAT current of $I_{0,B\_gain} = 30nA$. The current of the load current source is set to $I_{0,CS} = 10nA$, leading to an AC gain of a single gain stage stated in equation 7.1 and a limiter gain with N = 8 stages of equation 7.2. An AC simulation at 27°C, nom a limiter with N = 8 stages shows a sufficient bandwidth of $f_{-3dB,LP} \approx 185kHz$.

$$A_{S0} \approx \frac{I_{B\_GAIN}/2}{I_{D1} \cdot \eta} \approx \frac{I_{B\_GAIN}/2}{(I_{B\_GAIN}/2 - I_{CS}) \cdot \eta} \approx \frac{15n}{(15n - 10n) \cdot 1.2} \approx 2.5 \tag{7.1}$$

$$A_{0limiter} \approx 20 \cdot log_{10}(A_{S0}^{n}) \approx 20 \cdot log_{10}(2.5^{8}) \approx 63.7dB \tag{7.2}$$

The rectifiers are biased with a bandgap current 7.3 . The simulated RSSI error over temperature is smaller when the rectifiers are biased with a bandgap current compared to a PTAT bias current (chapter 5.3 shows that the compensation effect of the rectifier is increased with a bandgap bias current compared to a PTAT bias current).

$$I_{BG}(T) = I_0 \cdot (1 + TC_{BG} \cdot (T - T_0)) \tag{7.3}$$

The bias current for the rectifiers is set to $I_{0,B\_RECT} = 30nA$ and the rectifying current to $I_{0,R} = 10nA$. For the simulation ideal bias currents are used. The TC of the bandgap is $TC_{BG} \approx 0ppm/K$ and has the same standard deviation as the PTAT current ($\sigma(TC_{BG}) = \sigma(TC_{PTAT}) = 100ppm/K$, chapter 3.10.3).

Bias current scaling

Figure 7.2 shows the schematic of the bias current scaling for the gain stage. The input current is given with $I_{IN} = 10nA$ from a constant gm cell or a bandgap respectively. As the gain stage is biased with a PTAT current and the rectifier with a bandgap current, the scaling can be different and the circuit has to be implemented for each bias current.

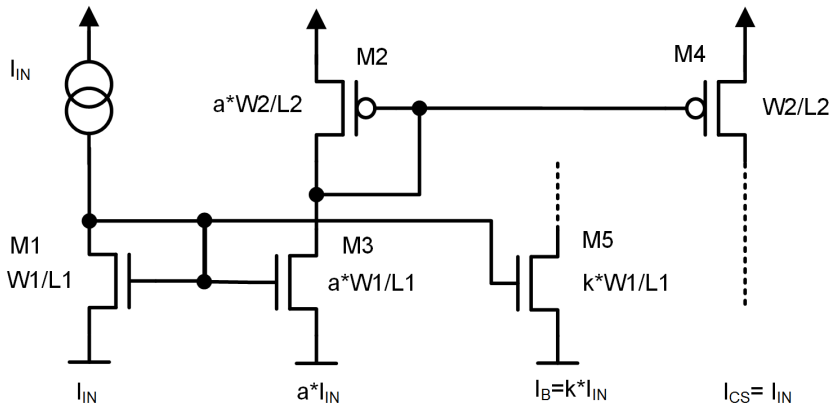
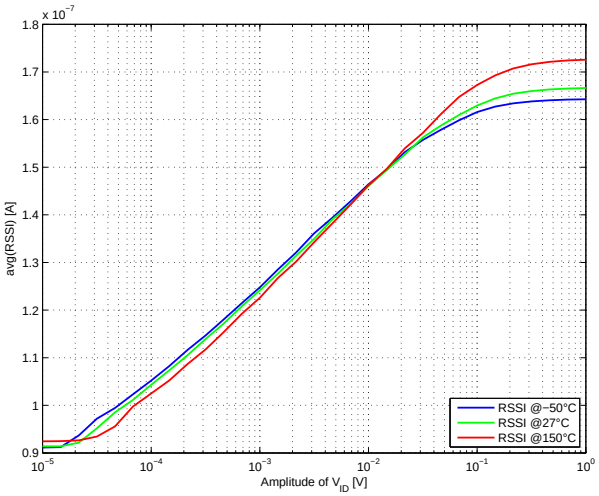


Figure 7.2: Schematic for bias current generation for the gain stage

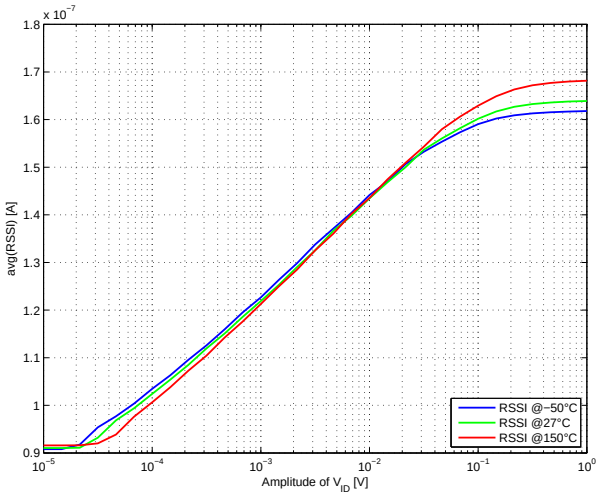
The NMOS current sink (M3) has also a cascode, which is not shown in figure 7.2. NMOS unit transistors with minimum width ($W1/L1 = 0.6\mu m/40\mu m$) and PMOS unit transistors with minimum width ($W2/L2 = 0.6\mu m/40\mu m$) are used. a, b and k are integer values for scaling with unit transistors. The scaling can be set by k. a is a factor greater than one for better matching of the PMOS current mirror. This consumes a factor of a times current. A non-integer current factor for the gain of the gain stage has to be implemented by either using non-unit transistors, which can result in poor matching or different a-factors of the NMOS and PMOS current mirror.

7.3 Low-pass filtered RSSI - process corner simulation

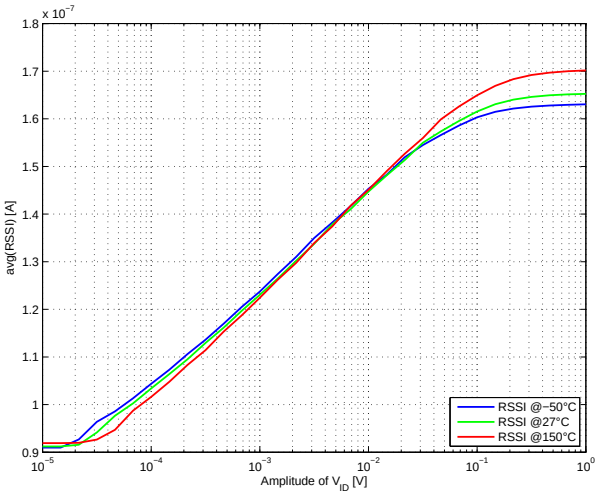
The simulation results of the low-pass filtered RSSI current is shown in figure 7.3. The RSSI current is temperature stable in the range of $100\mu V < vin < 100mV$ at all process corners. The gain stages are biased with a PTAT current for a temperature constant bandwidth. The rectifiers were biased with a temperature constant bandgap current. This minimizes the temperature effects on the rectifiers output current as described in chapter 5.3 or temperature effects on the RSSI in the following subsection 7.3.1.



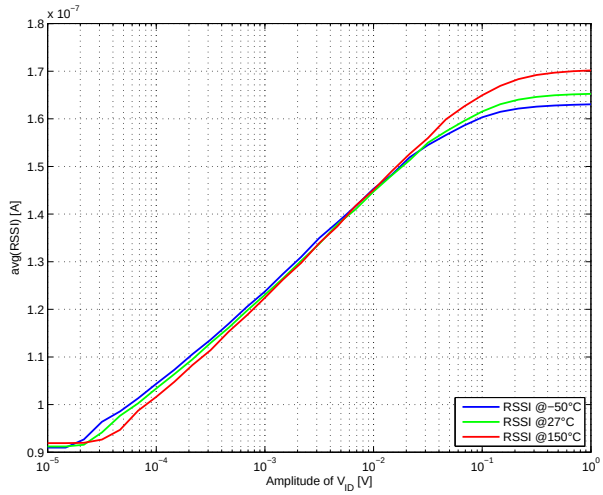
(a) RSSI at fast process corner



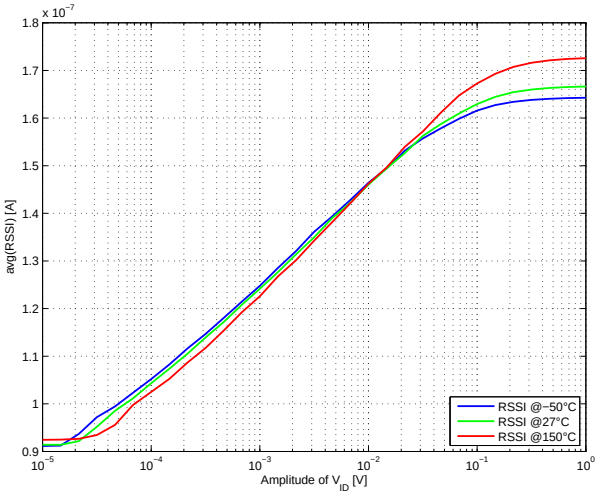
(b) RSSI at nom process corner



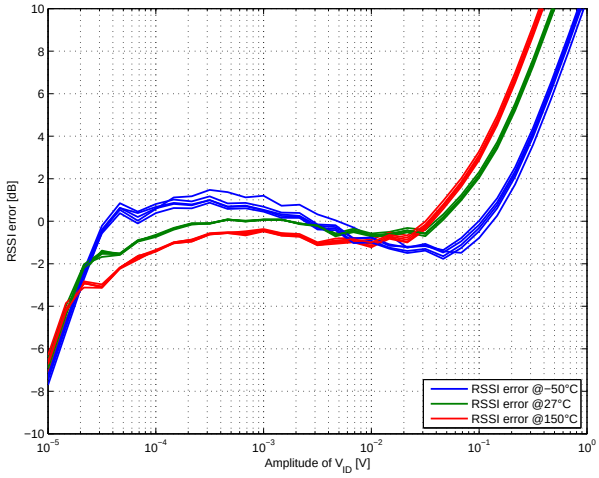
(c) RSSI at slow process corner



(d) RSSI at SF process corner



(e) RSSI at FS process corner



(f) RSSI error for all process corner

Figure 7.3: Low-pass filtered RSSI current at different process corners for the NMOS limiting amplifier

7.3.1 PVT effects on RSSI

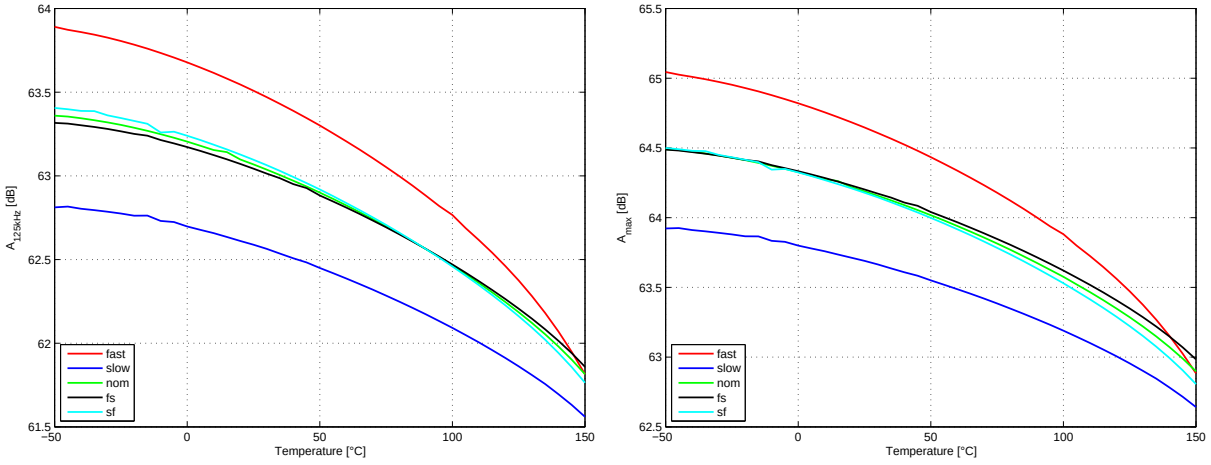
The NMOS gate voltage (V_B) of the load diode is a few hundred mV lower than VDD. The absolute value depends on the temperature. With the additional V_B the output clipping voltage of the gain stage is increased particularly at high temperatures and low V_{TH} of the NMOS load diode. At 150°C fast the clipping voltage without an additional gate voltage is less than $|V_S| \approx 5.3\eta U_T$. $|V_S| \geq 5.3\eta U_T$ is required to fully clip the rectifier at any temperature. Because the maximum output clipping voltage decreases with temperature due to decreasing threshold voltage of the load diode and $V_S \approx 5.3\eta U_T$ increases with temperature. The problem of the non-clipping rectifiers occurs only at high temperatures and fast process corner.

Another temperature effect on the RSSI is the redistribution charge at the gate source capacitor of the rectifiers current mirror. This effect is compensating less current at higher temperatures of the unbalanced differential input pair. The RSSI is higher at high temperatures and can be seen in the figures 7.3(a) - 7.3(e) at a $vin > 100mV$ when all rectifier are clipping. This compensation effect for the rectifier is also described in chapter 5.3.

The RSSI error is plotted in figure 7.3(f). In the dynamic range of $100\mu V < vin < 100mV$ the magnitude of RSSI error is below 2dB. The gradient of the fitted function is 2nA/1dB.

7.3.2 Small signal gain - process corner simulation

For a number of 8 gain stages, the AC gain of a single stage is $A_{0S} \approx 2.31$ (equation 7.1). This leads to a limiter gain of $A_{0limiter} = 20 \cdot log(2.31^8) \approx 58.2dB$ (equation 7.2). The small gain of a single gain stage is leading to a large number of gain stages. This also improves the RSSI ripple. On the other hand, the gain peaking in the large signal response of the gain stage, described in chapter 4.4.4 leads to an additional RSSI error or ripple ($RSSI\_ripple < 1dB$) compared to a more linear gain stage.



(a) Gain at f = 125kHz

(b) Maximum gain A_{max}

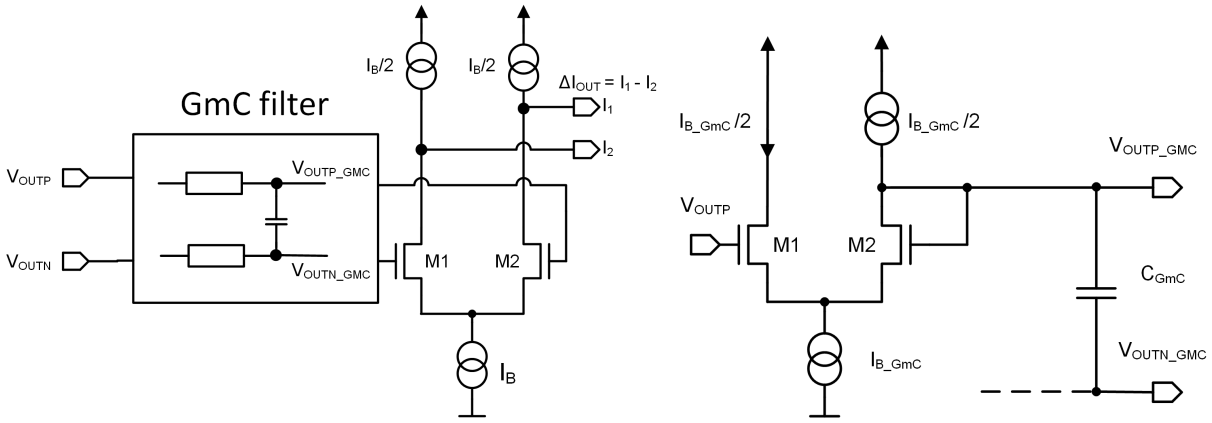
Figure 7.4: Corner simulation of small signal gain over temperature

Figure 7.4 shows the AC gain of the limiting amplifier over temperature at different process corners. The gain at a frequency of 125kHz of the limiting amplifier (A_{125kHz}) is shown in figure 7.4(a). The maximum gain over temperature of the limiting amplifier (A_{max}) is shown in figure 7.4(b). Both gain values are quite similar because of the sufficient bandwidth of the limiting amplifier. The maximum gain drop over temperature of the limiting amplifier is approximately $\Delta A \approx 2dB$. The gain is slightly larger than $A_{0limiter} \approx 63.7dB$ because the subthreshold slope is not exactly $\eta = 1.2$ but a bit lower.

7.4 Offset Control

As already mentioned in chapter 2.1, mismatch will lead to the saturation of the limiting amplifier due to high gain. To counteract saturation, an offset control is implemented. The structure of the limiting amplifier with offset control is shown in figure 2.1 of chapter 2.1.

Figure 7.5(a) shows the schematic of the offset control block. The offset control consists of a cross connected differential pair and a low-pass filter with low cutoff frequency. The input of the offset control is connected to the output of the last gain stage from the limiting amplifier (V_{OUTN} and V_{OUTP}). The low-pass filter is a GmC filter shown in figure 7.5(b).



(a) Schematic of the offset control block

(b) Schematic of a single ended GmC filter

Figure 7.5: Schematic of offset control and a single ended GmC filter

Other possibilities for offset cancellation are AC coupling of the single gain stages or a chopper amplifier offset compensation [11]. The coupling capacitors for AC coupling have to be large for such a low cutoff frequency, which consumes to much area.

7.4.1 Offset subtraction

The differential pair (M1, M2) of figure figure 7.5(a) will be unbalanced with a DC offset voltage. The differential pair is cross connected to the output of the first gain stage. The delta current ($\Delta I_{out} = I_1 - I_2$) generates a voltage difference on the load of the first gain stage and thus a voltage difference. The feedback loop is closed and the subtractor damps voltages at low frequencies.

The voltage gain of the offset control (A_F) can be calculated by transconductance of the offset control gm_F and the load conductance of the first gain stage ($g_{load} \approx \frac{1}{gm_{Diode}}$, equation 7.4). In weak inversion gm of a MOS is proportional to the current and the gain can be calculated by the current ratios of the offset control and the load diode. $-A_F$ is the offset voltage gain in the closed loop transfer function shown in figure 7.6.

$$A_F = gm_F \frac{1}{g_{load}} \approx gm_F \cdot \frac{1}{gm_{Diode} + gmbs_{Diode}} = \frac{I_B/2}{\eta I_{D1}} \tag{7.4}$$

The differential pair has a current source with a current of $I_B/2$ as load. The common mode voltage is defined due to the load diode of the first gain stage. Without the additional current source the additional DC current ($I_B/2$) will lower the gain of the first gain stage.

7.4.2 Low-pass GmC filter

A single-ended GmC filter as shown in figure 7.5(b) is used, for the low cutoff frequency of F(s). The outputs of the two GmC filters (V_{OUTP} similar to V_{OUTN}) are connected to a capacitor ($C_{GmC} = 20pF$). This results in a pseudo differential structure. A simple OTA with current source load ($I_{B\_GMC}/2$) is connected as follower or unity gain configuration. gm and so $f_{-3dB,GmC}$ can be very low when the OTA is biased with a low current (equation 3.47).

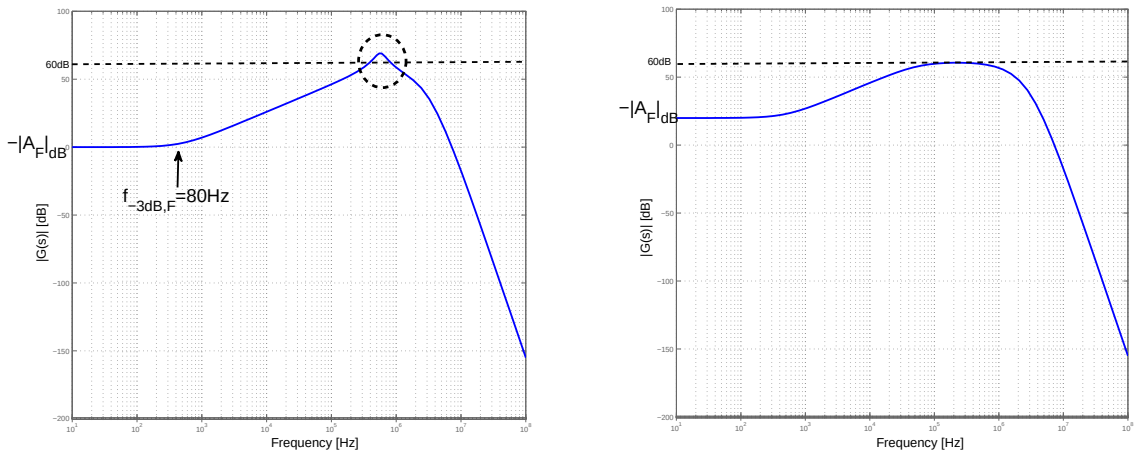
$$f_{-3dB,GmC} = \frac{1}{2\pi \cdot 2RC} = \frac{1}{2\pi \cdot 2\frac{C_{GmC}}{gm_{OTA}}} = \frac{1}{2\pi \cdot 2\frac{C_{GmC}}{gm/2}} \tag{7.5}$$

$$= \frac{1}{2\pi \cdot 2\frac{C_{GmC} \cdot \eta U_T}{I_{B\_GmC}/4}} = \frac{I_{B\_GmC}}{2\pi \cdot 8C_{GmC} \cdot \eta U_T} \tag{7.6}$$

The dominant pole of the GmC filter can be approximated by equation 7.5 for a differential structure. A current source at the output instead of a current mirror is used to lower gm_{OTA} to $gm/2$ of the differential pair. Using $gm = gm1 = I_{DS}/(\eta U_T) = I_{B\_GmC}/(2\eta U_T)$ for an unbalanced differential pair leads to equation 7.6.

7.4.3 Closed loop transfer function of limiting amplifier

As already introduced in chapter 2.7.1, the transfer function of the limiting amplifier is a band-pass filter. The same matlab model for the limiter with 8 stages is used here for the simulation of closed loop magnitude. The following model parameters are used for the simulation. The pole frequency of the feedback path of chapter 2.7.1 ($f_{-3dB,F} = 10Hz$) is multiplied by 8 ($p_F \approx 62.8rad/s \cdot 8 \approx 502.4rad/s$ of $f_{-3dB,F} = 80Hz$). Thus the maximum high-pass cutoff frequency is also shifted from $f_{-3dB,HP} = 10kHz$ to $f_{-3dB,max,HP} = 80kHz$ to meet the specifications.



(a) $A_F = 1$ high forward path gain

(b) $A_F = 0.1$ lower forward path gain

Figure 7.6: Closed loop magnitude of limiter with offset control

The magnitude of the closed loop model can be seen in figure 7.6(a). The open loop transfer function still has a positive phase margin (PM $\approx 25°$) but magnitude of the closed loop exceeds the gain of 60dB. The low phase margin increases the magnitude of the closed loop transfer function. Thus the minimum and maximum pole frequencies as given in the specifications ($f_{-3dB,max,HP} = 80kHz$ and $f_{-3dB,min,LP} = 180Hz$) cannot be implemented without an increase of the magnitude of the transfer function.

In figure 7.6(b) the gain of the feedback is lowered to $A_F = 0.1$ with the same pole frequency as in the previous simulation. This makes the transfer function more stable (PM $\approx 84°$) and there is no increase of magnitude in the transfer function. A lower bandwidth of the feedback path $f_{-3dB,F}$ also decreases $f_{-3dB,max,HP}$, which also increases the phase margin and the bandwidth of the bandpass.

A larger bandwidth of the limiting amplifier increases integrated input referred noise. $f_{-3dB,HP}$ is determined by simulation of the limiter with the offset control block. The bandwidth is used to calculate the integrated input referred noise. In the next sections (chapter 7.5 - 7.6) the noise optimization is done before the dimensioning of the offset control (chapter 7.7).

7.4.4 White Noise vs. offset voltage gain A_F

The offset control contributes to the noise of the limiting amplifier. The main part of the noise is caused by the subtractor. This can be minimized by a high bias current of the differential pair of the subtractor (I_B figure 7.5(a)). On the other hand, a high bias current will lead to a high damping of the DC offset voltage. For a high damping of the DC offset voltage the cutoff frequency of the offset subtractor has to be low for a sufficient phase margin. For a limited capacitor of the GmC filter, due to restricted area, the only possible scaling for a low cutoff frequency is the bias current of GmC filter (I_{B_GmC}). For a low cutoff frequency, a capacitor of 20pF and a bias current of $I_{B\_GmC} = 1nA$ is used. A smaller bias current is not used because of possible cross talk and settling problems.

7.5 Noise optimization

7.5.1 Integrated white noise approximation

The ENBW for a bandpass filter is stated in equation 2.17. The ENBW combined with equation 2.19 for the integrated input referred white noise of a band-pass filter as stated in equation 7.7. This is an approximation for the integrated input referred noise of the limiting amplifier if white noise is dominating.

$$S_I^2 = S_I^2(f) \cdot ENBW = S_I^2(f) \cdot \left(f_{-3dB,LP} \cdot B_{LP} - \frac{f_{-3dB,HP}}{B_{HP}} \right) \tag{7.7}$$

As the limiting amplifier has a high order (N = 8), B_{LP} is close to 1.1 (table 2.8) and the high-pass filter B_{HP} is approximately $\pi/2$ due to a first order high-pass from the feedback path. With the specified minimum and maximum f_{-3dB} cutoff frequencies ($f_{-3dB,max,HP} = 80kHz$, $f_{-3dB,min,LP} = 150kHz$) and the simulated input referred noise at 27°C of the limiting amplifier $\left(S_I(f = 125kHz) \approx 310 \frac{nV}{\sqrt{Hz}} \right)$, the integrated input referred noise is stated in equation 7.8.

$$\begin{aligned} S_I &\approx S_I(f = 125kHz) \cdot \sqrt{\left(f_{-3dB,LP} \cdot B_{LP} - \frac{f_{-3dB,HP}}{\pi/2} \right)} \\ &\approx 310 \frac{nV}{\sqrt{Hz}} \cdot \sqrt{150kHz \cdot 1.1 - \frac{80kHz}{\pi/2}} \approx 104.7\mu V \end{aligned} \tag{7.8}$$

The noise of the limiting amplifier has to be decreased because the approximation of the integrated input referred white noise with the minimum bandwidth is already exceeding the specification. The bandwidth of the limiting amplifier can be determined by simulation with the offset control. As shown in chapter 7.4.3 the minimum specified bandwidth cannot be

implemented without an increase of the magnitude from the closed loop transfer function. Thus the bandwidth of the limiting amplifier has to be increased, which also increases S_I. Additionally including flicker noise will increase S_I as well. A second order high-pass filter can decrease flicker noise of the first stage if this is is necessary for the design.

7.5.2 White noise distribution & optimization

The white noise of the whole limiting amplifier is composed of the single gain stage noise and the noise of the rectifiers. As already mentioned flicker noise and the noise of the rectifiers can be neglected for this design of the limiting amplifier. The input referred white noise density ($S_i^2(f)$) of a single gain stage (in further context denoted as $\dot{S}_i^2$) is indirectly proportional to the bias current and the transconductance of each gain cell (I_s and gm_s equation 7.9).

$$S_i^2(f) = \dot{S}_i^2 \propto 1/I_s \propto 1/gm_s \tag{7.9}$$

A integer number of gain stages (H) is placed in parallel to reduce the noise. So gm_s is summed up and the noise for H parallel structures is indirectly proportional to H as stated in equation 7.10. The parallel stages also increase the total current consumption of the limiting amplifier (equation 7.11). For a fixed current the noise has to be optimized by $H[n]$. In this context n = 1, 2, ..., N is the position of the gain stage in the cascaded limiting amplifier and n = 1 is the first gain stage.

$$\dot{S}_I^2(H) \propto 1/(gm_s \cdot H) \tag{7.10}$$

$$\sum_{n=1}^{N} H[n] \cdot I_s = I \tag{7.11}$$

All cascaded single gain stages have an equal input noise density of $\dot{S}_i^2[n] = \dot{S}_i^2[n=1] = \dot{S}_i^2[n=2] = ... = \dot{S}_i^2[n=N]$ and gain of $A[n] = A[n=1] = A[n=2] = ... = A[n=N]$. The noise of the single gain stages has to be referred to the input of the limiting amplifier. The input noise $\dot{S}_i^2[n]$ of the n-th stage is divided through the squared gain of the stages before leading to the input referred noise $\dot{S}_I^2[n]$ (equation 7.12).

$$\dot{S}_I^2[n] = \frac{\dot{S}_i^2[n]}{A^{2(n-1)}} \tag{7.12}$$

The summed input referred noise density ($\dot{S}_{I\_all}^2$) with H[n] parallel stages can be stated in equation 7.13.

$$\dot{S}_{I\_all}^2 = \sum_{n=1}^{N} \dot{S}_I{}^2[n] \propto \sum_{n=1}^{N} \frac{1}{A^{2(n-1)} \cdot H[n]} \tag{7.13}$$

The minimum of $\dot{S}_{I\_all}^2$ for a sum over H[n] is found by using the greedy algorithm and is stated in equation 7.14. X has to be chosen such that the current consumption (equation 7.11) is not exceeded.

$$H[n] = A^{X-(n-1)} \tag{7.14}$$

The implemented limiting amplifier has N = 8 cascaded stages and a single stage gain of $A \approx 2.5$. For a fixed current consumption, the last gain stages can be implemented just with one instance. In this design, the first 3 gain stages (n =1,2,3) gain stages have parallel instances with regard to the optimum of equation 7.14 and not exceeding the total current consumption ($I \leq 1.1\mu A$). This leads to equation 7.15.

$$H[n] = A^{3-(n-1)} \tag{7.15}$$

The optimum from the equation is, the first gain stage has $H[n = 1] = 2.3^3 \approx 16$ parallel instances, the second has $H[n = 2] = 2.5^2 \approx 6$ and the third has $H[n = 3] = 2.5^1 = 3$ parallel instances. All other stages have no parallel instance. This results in a total current consumption of the limiting amplifier without rectifier of equation 7.16.

This high number of gain stages exceeds the maximum power consumption of the limiting amplifier. With 720nA the optimization with the greedy algorithm reveals for the total sum of 24 gain stages the following distribution: $H[n = 1] = 12$, $H[n = 2] = 5$, $H[n = 3] = 2$, $H[n = 4] = 1$, ...

$$\begin{aligned} I &= I_s \cdot \sum_{n=1}^{N} H[n] = I_s \cdot (12 + 5 + 2 + 1 + 1 + 1 + 1 + 1) \\ &= I_s \cdot 24 = 30nA \cdot 24 = 720nA \end{aligned} \tag{7.16}$$

7.6 Dimensioning of parallel instances - simulation results

Without parallel instances - input referred noise density at f = 125kHz
The input referred white noise density of the whole limiting amplifier is too large for a limiting amplifier design ($S_I(f) \approx 310nV/\sqrt{Hz}$). The noise of first stage ($S_I(f) \approx 270nV/\sqrt{Hz}$) is the largest contributor to the summed noise density of the limiting amplifier.

With parallel instances - input referred noise density at f = 125kHz
With the given parallel instance numbers from section 7.5.2, an AC noise simulation is done. An input referred noise density of $S_I(f) = 110nV/\sqrt{Hz}$ at 27°C is reached without offset control. The offset control is biased with a large current, so it contributes with a small part to the summed input referred noise. The limiting amplifiers summed input referred noise density, simulated with the implemented block in the next section, is $S_I(f) = 113.7nV/\sqrt{Hz}$. The white noise density of the limiting amplifier is approximately equal to a reference design. The integrated input referred noise can be determined with $f_{-3dB,HP}$ and $f_{-3dB,LP}$ after implementing the offset control (section 7.7).

7.7 Dimensioning of the offset control

7.7.1 Gain of feedback path A_F

The cross-connected differential pair is biased with $I_B = 80nA$ PTAT current for a constant gm over temperature like the bias current for the gain stages. A_F, the feedback path gain, can be calculated by equation 7.4 for no parallel instances of the first gain stage. The factor H[n = 1] is added (equation 7.17) for the parallel instances of the first stage. The values set in the equation, which results in a $A_F \approx -5.1dB$.

$$A_F \approx \frac{I_B/2}{\eta I_{D1} \cdot H[n=1]} \approx \frac{80nA/2}{1.2 \cdot 5nA \cdot 12} \approx 0.556 \approx -5.1dB \tag{7.17}$$

7.7.2 -3dB pole frequency of feedback path $f_{-3dB,F}$

The GmC filter is biased with $I_{B\_GmC} = 1nA$ and a capacity of $C_{GmC} = 20pF$. This leads to a pole frequency of the feedback path (from equation 7.6) stated in equation 7.18.

$$f_{-3dB,F} \approx \frac{I_{B\_GmC}}{2\pi \cdot 8C_{GmC} \cdot \eta U_T} \approx \frac{1nA}{2\pi \cdot 8 \cdot 20pF \cdot 1.2 \cdot 26mV} \approx 31.9Hz \tag{7.18}$$

7.7.3 AC noise simulation results

The closed loop transfer function and $f_{-3dB,HP}$ is simulated with the offset control in an AC simulation, resulting in $f_{-3dB,HP} \approx 10.6kHz$ and $f_{-3dB,LP} \approx 195kHzkHz$. The integrated white noise can be determined by inserting $S_I(f = 125kHz)$ and f_{-3dB} in equation 7.8 for each run. This results in equation 7.19.

$$S_I = 113.7nV/\sqrt{Hz} \cdot \sqrt{\left(195kHz \cdot 1.1 - \frac{10.6kHz}{\pi/2}\right)} \approx 51.8\mu V \tag{7.19}$$

The integrated input referred noise AC simulation results are not very accurate due to non linear behavior of the limiter. The overall noise is almost clipping the last rectifier of the limiting amplifier. Never the less, the small signal noise simulation is a good tool for comparing the different limiting amplifier structures and for noise optimization.

7.7.4 Transient noise simulation results

From a transient noise simulation, the RMS (root mean square) value of the integrated output referred noise (S_O) can be calculated with the output noise ($S_O^2(t)$) using equation 7.20. Assuming a linear limiting amplifier, the input referred noise can be calculated by dividing the output referred noise by the gain of the limiting amplifier (equation 7.21) .

$$S_O = \sqrt{\frac{1}{t1 - t0} \cdot \int_{t0}^{t1} S_O^2(t)dt} \tag{7.20}$$

$$S_I = S_O/A_{limiter}(f = 125kHz) \approx 280.7mV/64dB \approx 167.5\mu V \tag{7.21}$$

The simulation time for transient noise has to be at least $T = 1/fmin$, where $fmin$ is the minimum noise frequency that has no more influence on the integrated noise.

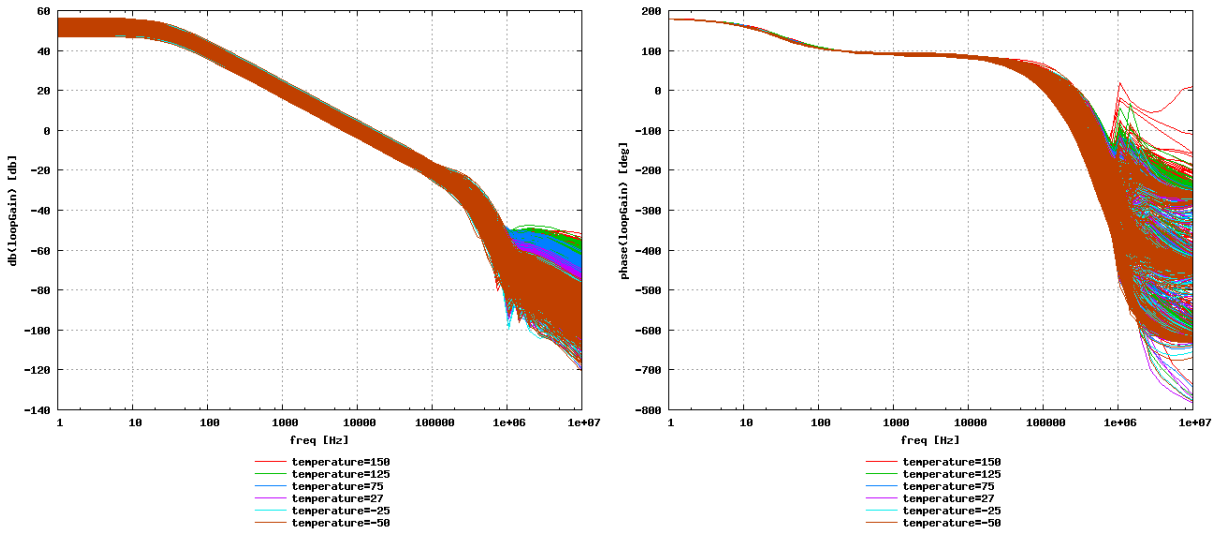
In subsection 7.10 a transient simulation with an amplitude modulated input signal shows the demodulated RSSI output current.

7.8 Monte Carlo - AC simulation results

For the evaluation of the AC parameters 500 AC, AC_noise, and AC_stb Monte Carlo runs are done at the temperature points of: -50°C, -25°C, 27°C, 75°C, 125°C and 150°C. Different AC parameters of the limiting amplifier & RSSI design are shown in the following subsections.

7.8.1 AC stability open loop - simulations results

Figure 7.7 shows the open loop transfer function of the limiting amplifier at all simulated temperatures. The magnitude of the open loop transfer function is shown on the left side (sub-figure 7.7(a)) and the phase on the right side (sub-figure 7.7(b)).



(a) Open loop gain of limiting amplifier

(b) Open loop phase of limiting amplifier

Figure 7.7: Monte carlo simulation of the open loop transfer function at all temperatures

The phase margin as stated in equation 2.23 is determined with the gain and phase of the open loop transfer function for a stability indication. Figure 7.7 shows the distribution of phase margin on a normal probability plot. Phase margin has s minimum at low temperatures but is still sufficiently large.

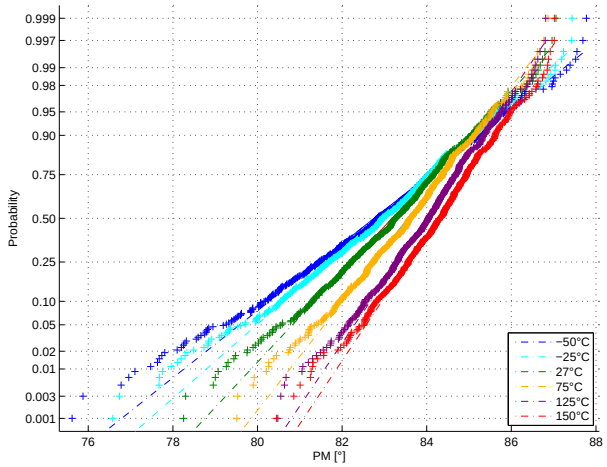


Figure 7.8: Normal probability plot of phase margin of the limiting amplifer with offset control

7.8.2 AC limiter closed loop -3dB frequencies - simulation results

Figure 7.9 shows the closed loop gain of the limiting amplifier of all Monte Carlo runs at all temperatures.

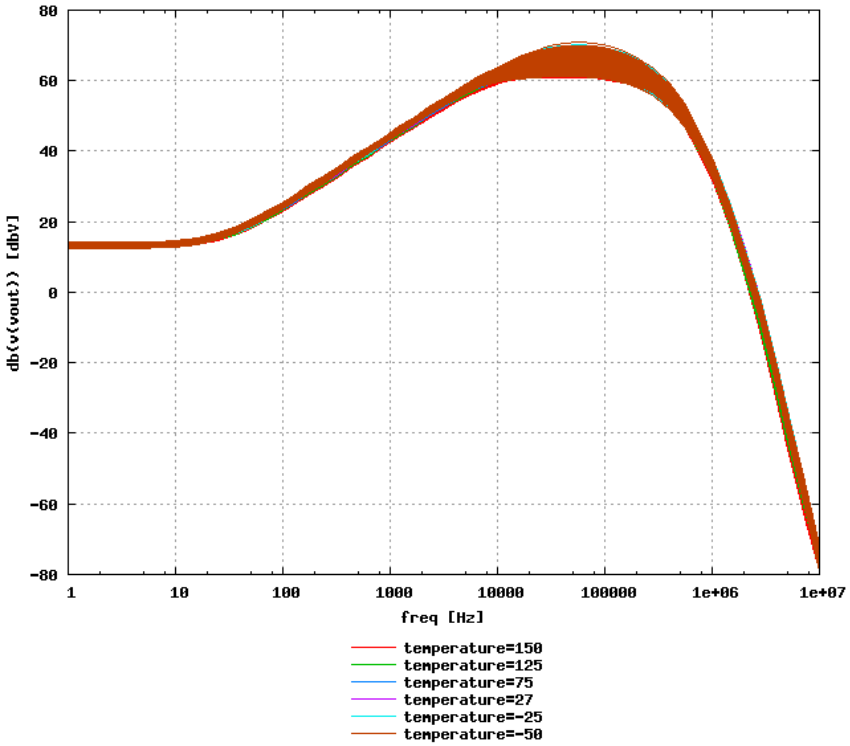
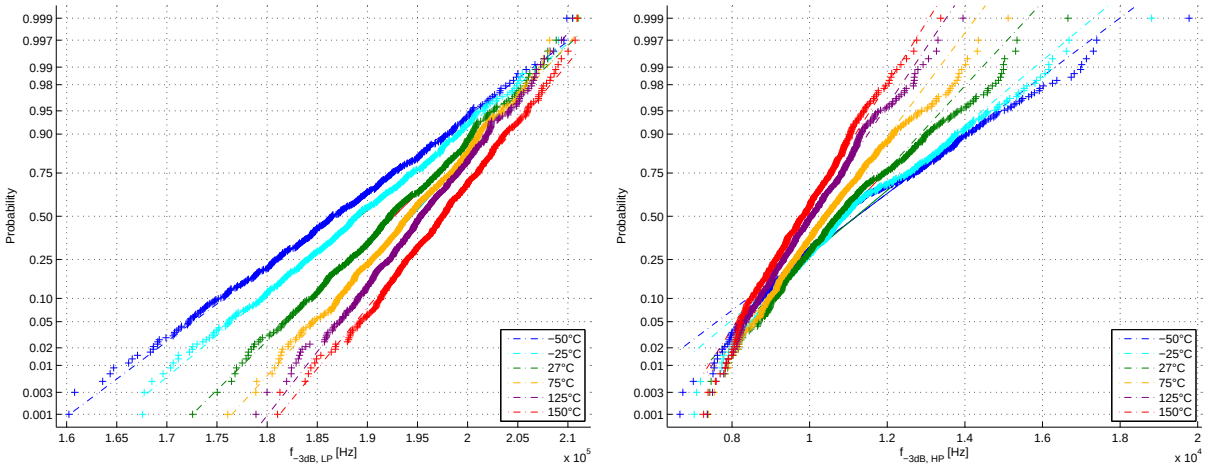


Figure 7.9: Closed loop magnitude of the limiting amplifier

From the closed loop magnitude $f_{-3dB,LP}$, $f_{-3dB,HP}$, A_{max} and A_{125kHz} are determined. This values are shown in the next plots. In figure 7.10 shows the f_{-3dB} of the closed loop limiting amplifier in a normal probability plot.

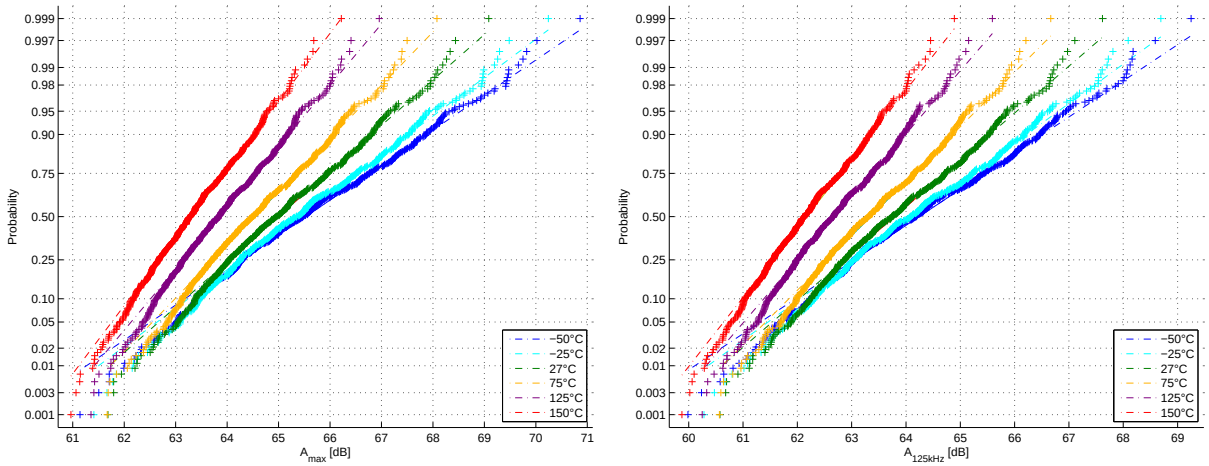


(a) Low-pass filter $f_{-3dB,LP}$

(b) High-pass filter $f_{-3dB,HP}$

Figure 7.10: Normal probability plots of band-pass filter frequencies at different temperatures

The distribution of the maximum gain (A_{max}) is shown in figure 7.11(a) and the distribution of the gain at 125kHz (A_{125}) in figure 7.11(b).



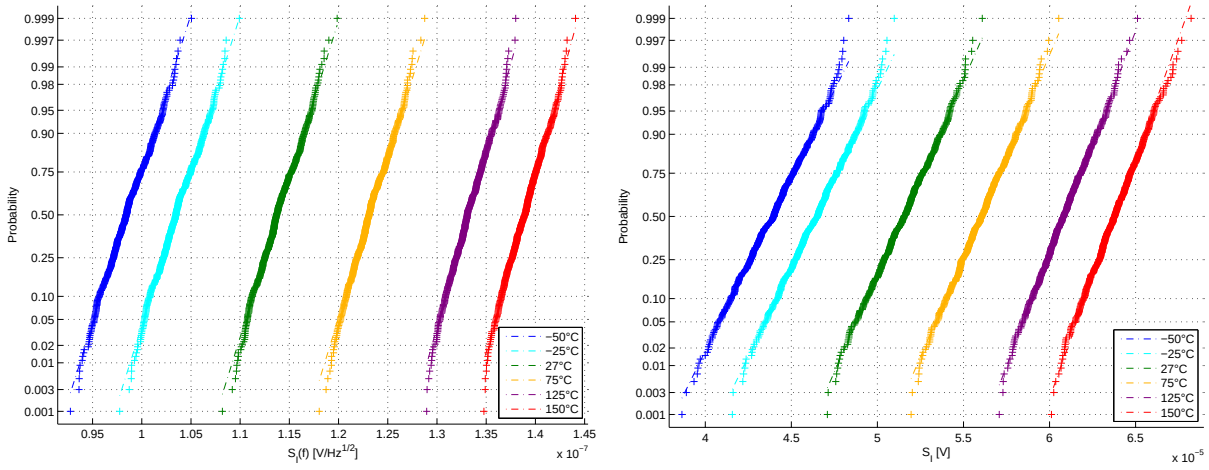
(a) Maximal limiter gain (A_{max})

(b) Limiter gain at 125kHz (A_{125})

Figure 7.11: Normal probability plot of AC gain at different temperatures

7.8.3 AC noise - simulation results

An AC noise Monte Carlo simulation is done and the input referred noise density at f = 125kHz is measured. The noise density on a normal distribution plot is shown in figure 7.12(a).



(a) Input referred noise density at f = 125kHz

(b) Integrated input referred noise

Figure 7.12: Normal probability plot of AC gain at different temperatures

The integrated input referred noise (S_I) can be calculated for each Monte Carlo run. This is done by inserting the simulated parameters ($S_I(f)$, $f_{-3dB,LP}$ and $f_{-3dB,HP}$) in equation 7.8 for each run. The distribution of the integrated input referred noise at different temperatures is shown in figure 7.12(b).

7.9 Monte Carlo - transient simulation for carrier detect threshold

The statistical variation due to mismatch of the RSSI is evaluated by a transient Monte Carlo simulation. It is necessary to simulate the limiting amplifier with the offset control because an offset voltage caused by mismatch would drive the limiter into saturation. The carrier detect threshold voltage $S_{det}(T)$ is the most difficult specification to fulfill. $S_{det}(T)$ varies with different Monte Carlo runs and additionally over temperature. Thus the threshold voltage is trimmed at T=27°C for each chip to meet the specifications. The next subsection describes how the trimming of the carrier detect threshold is evaluated in the simulation.

7.9.1 Trimming of carrier detect threshold $S_{det}(T)$

The RSSI is fed to a comparator, which compares the RSSI current to the trimmed reference current (figure 2.5). The reference current is a measured RSSI current of the limiting amplifier at 27°C and trimmed to the input signal of the arithmetic mean of the detection limits (equation 7.22) as specified in chapter 2.2.1.

$$S_{det}(T = 27°C) = \sqrt{S_{nodet,pp} S_{det,pp}} = \sqrt{12mV \cdot 4mV} \approx 7mV \tag{7.22}$$

The trimming to the arithmetic mean allows the largest tolerance of threshold voltage variation over temperature to the upper and lower specified detection limit. The evaluation of the carrier detection with the trimmed reference current is done by post processing.

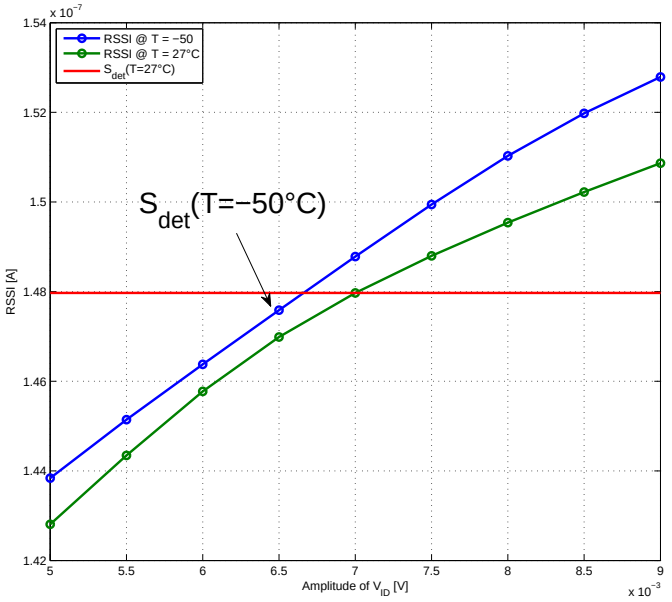


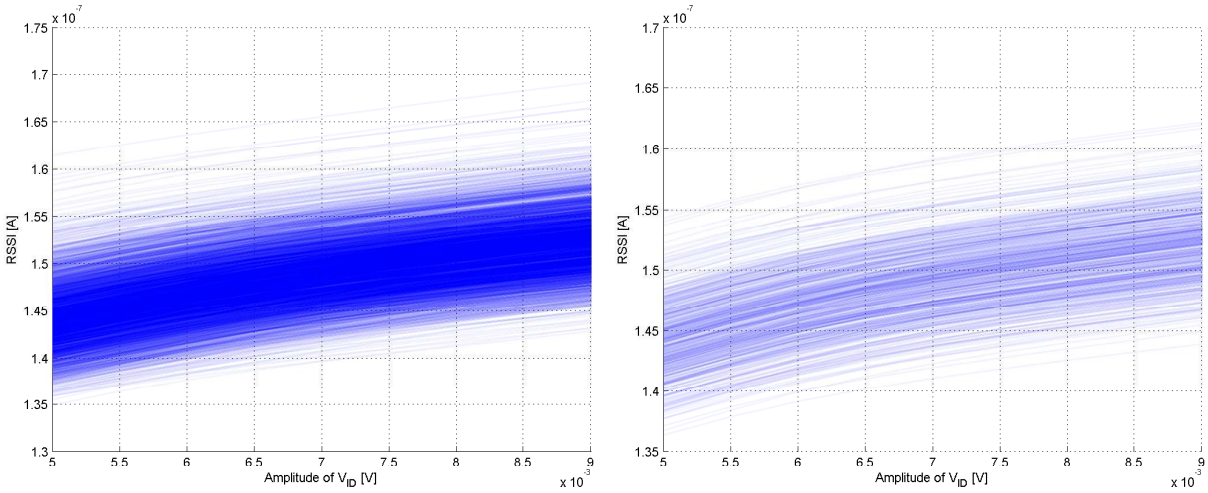
Figure 7.13: Evaluation of carrier detect threshold

Figure 7.13 shows the RSSI at T=-50°C (blue) and at T=27°C (green) for one Monte Carlo run. The reference for the carrier detect comparator is the trimmed RSSI current at 27°C and at $\hat{v}_{in} = 7mV$ (red horizontal line). The crossing of the reference current and the RSSI is the carrier detect threshold voltage. Due to limited resolution of $\hat{v}_{in}$ at this point $S_{det}(T)$ cannot be calculated exactly. The data point of the $\hat{v}_{in}$ with the minimum distance (absolute value of difference) of the reference current and the RSSI at different temperatures is the carrier detect threshold voltage with limited resolution. In this example the carrier detect threshold is at $S_{det}(T = -50°C) = 6.5mV$ because at $\hat{v}_{in} = 6.5mV$ the distance of the reference current data

point and the RSSI data point at T=-50°C is the smallest. This evaluation approach assumes an ideal comparator. The calculation for the carrier detect threshold is done for each Monte Carlo run and each temperature.

7.9.2 Simulation results - carrier detect threshold

Figure 7.14 shows the RSSI currents of the limiting amplifiers in the simulated voltage range of $\hat{v}_{in} = 5mV - 9mV$ with an increment of $\Delta\hat{v}_{in} = 0.5mV$ at the different temperatures (T=-50°C, -25°C, 27°C, 75°C, 125°C, 150°C). This Simulation has already 27000 runs for 6 Temperature, 9 input voltages and 500 Monte Carlo runs.



(a) RSSI at all temperatures and all Monte Carlo runs

(b) RSSI at 27°C and all Monte Carlo runs

Figure 7.14: Monte carlo simulation of RSSI

The distribution of the carrier detect threshold voltage at T=150°C (red) and T=-50°C (blue) and a $\Delta\hat{v}_{in} = 0.5mV$ can be seen in figure 7.15.

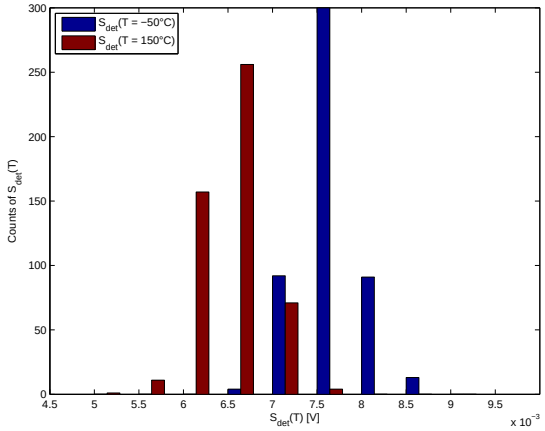
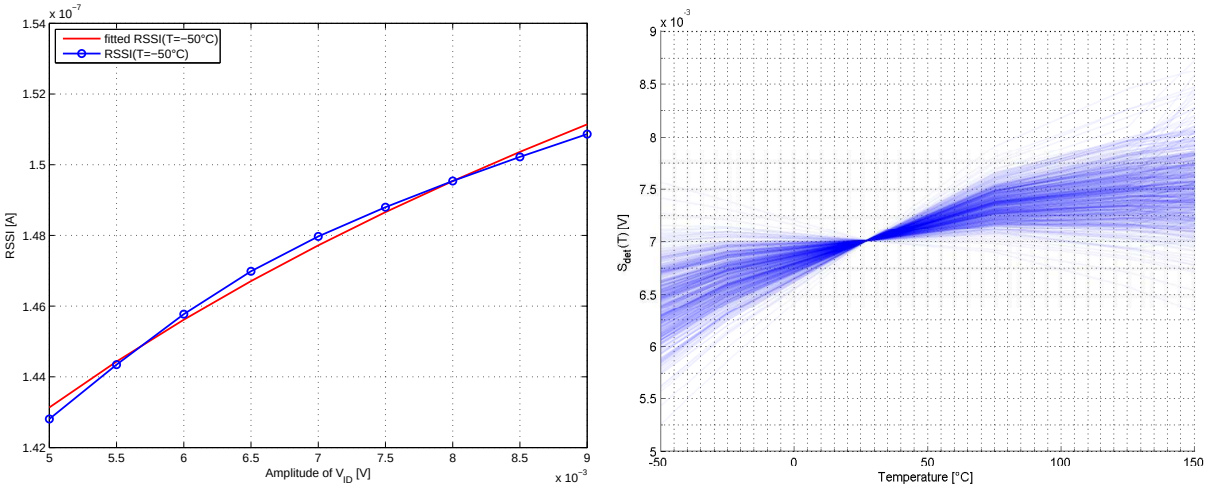


Figure 7.15: Histogram of Monte carlo simulation for carrier detect threshold at T= -50°C and T=150°C

The simulated RSSI is fitted in the logarithmic domain with a linear function for a higher resolution and to improve the accuracy of the carrier detect threshold voltage. This is shown in figure 7.16(a) for the RSSI at T=-50°C and one Monte Carlo run. The crossing point of the trimmed reference current and the fitted RSSI function is taken as the carrier detect threshold voltage. Still there is an error between the data points (simulated RSSI) and the fitted RSSI

function. However this error is assumed to be much smaller than the error due to the limited input voltage resolution.

The fitting is implemented for all RSSI of each Monte Carlo run at each temperature. Figure 7.16(b) shows the carrier detect threshold over temperature for all Monte Carlo runs. All lines cross at the trimming point of T= 27°C and $\hat{v}_{in} = 7mV$. The largest deviation of $S_{det}(T)$ is at the temperature corners (T=-50°C and T=150°C). The mean value of $S_{det}(T = 150°C)$ is larger $\hat{v}_{in}$ compared to the mean value of $S_{det}(T = -50°C)$.

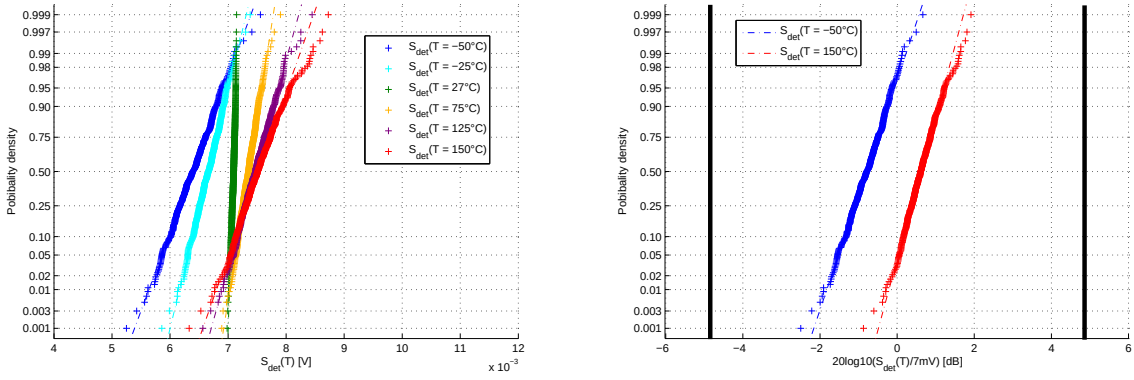


(a) Simulated RSSI (blue) and fitted RSSI (red)

(b) carrier detect threshold over temperature for all runs

Figure 7.16: Monte Carlo simulation results of fitted carrier detect threshold

Figure 7.17(a) shows the normal probability plot of Monte Carlo simulation for carrier detect threshold voltage at all simulated temperatures on a linear x-axis scale. The green data points are distributed at a vertical line with a small error due to the fitted function because all runs are trimmed to $S_{det}(T = 27°C) = 7mV$.



(a) Linear x-axis scale

(b) Logarithmic x-axis scale

Figure 7.17: Normal probability plot of Monte carlo simulation for CD threshold

Figure 7.17(b) shows the distribution of $S_{det}(T)$ at 150°C and -50°C in a normal probability plot with logarithmic x-axis scale. The black bars in the diagram show the specification maximum and minimum ($\hat{v}_{in} = 4mV - 12mV$). This shows the $S_{det}(T = -50°C)$ and $S_{det}(T = 150°C)$ is approximately symmetrically centered within the specifications for 500 Monte Carlo runs.

7.10 Evaluation of datagram detection threshold

7.10.1 Specification for datagram detection

As already mentioned in chapter 2.2.2, the limiter operating in the datagram detection mode has the following specifications for the amplitude of the input data signal: data signals with amplitudes smaller than $S_{nodet} = 100\mu V$ must not be detected and signals with larger amplitude than $S_{det} = 1mV$ have to be detected. The arithmetic mean of the specification is stated in equation 7.23.

$$S_{det,nom} = \sqrt{S_{nodet,pp} S_{det,pp}} = \sqrt{1mV \cdot 0.1mV} \approx 316.2\mu V \tag{7.23}$$

There are also other specifications for S_{nodet} and S_{det} with larger amplitudes possible. In this case a comparator is used to detect the specified signal amplitudes.

7.10.2 Datagram simulation with transient noise

Figure 7.18 shows the demodulated datagram at three different input amplitudes of a transient simulation at 27°C with noise. The RSSI low-pass data filter is an ideal first order low-pass with $f_c = 12kHz$.

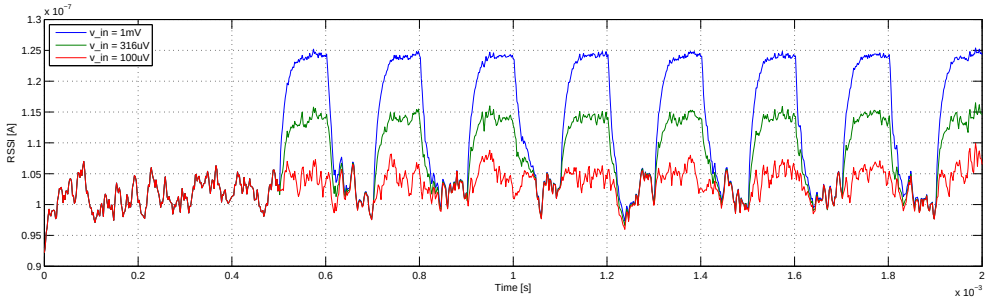


Figure 7.18: Demodulated datagramm with noise and different amplitudes of input signal

Ideally, signals with larger amplitude of the arithmetic middle of the specifications can be demodulated by the data slicer as described in chapter 2.2.2. Input signal with an amplitude lower than $v\_in = 100\mu V$ (red line) cannot be distinguished from the noise floor.

7.10.3 Gain and noise from AC simulation

AC simulation results can be used to predict the behavior of the limiting amplifier in the datagram mode. All results from the Monte Carlo - AC simulations can be additionally used for validation of the specifications. Noise and gain of the limiting amplifier is not deviating much with mismatch and process variation, thus the datagram detection amplitudes will not deviate much from the nominal case.

7.10.4 Further evaluation for datagram mode

The datagram mode can be evaluated with a more detailed transient noise simulations. Including the datagram demodulation block, the bit error rate (BER) can be determined by simulation. This requires a long simulation time and resources for a meaningful result.

7.11 Comparison to a reference design

Most of the parameters like bandwidth, gain, and noise are almost equal for the two designs. These parameters are not significantly different as can be seen in table 7.1. The most important performance parameters: carrier detect threshold variation, current consumption, and area are compared for the optimized designs.

7.11.1 Limiting amplifier designs

The reference design consists of the triode load gain stage (chapter 4.2) without gain regulation and a gilbert cell rectifier (chapter 5.2). In the reference design, the gain depends on a ratio of gm and Ron of a NMOS and a PMOS device. This can have disadvantages, if the models do not fit to reality and Ron is not correlated to gm. As the gain is directly influencing the RSSI, the stability of the gain is very important.

In this new design the gain of the limiting amplifier is created by a gm ratio of the same device (chapter 4.5). This gm ratio is process, mismatch and temperature robust, even if the model is deviating from reality. The rectifier used in this design (described in chapter 5.3) has a compensation effect on a the temperature dependent current of a rectifier in weak inversion. This is reducing the RSSI error over temperature.

7.11.2 Area

The overall area of the limiting amplifier is dominated by the area of $C_{GmC} = 20pF$ capacitor ($A \approx 9000(\mu m)^2$) in the offset control. The reference design has a total area of $A \approx 10400(\mu m)^2$. The new design occupies an area of $A \approx 12100(\mu m)^2$. Mainly the larger area in the new design is needed for the large current sources of the gain cells. This large current source transistors are required for good matching and less noise of the gain stage.

7.11.3 Current consumption vs. noise

The new design compared to the old design consumes approximately $(1.12/1.02-1)\cdot 100\% \approx 10\%$ more current. The current consumption can be further lowered by reducing the parallel stages (section 7.5.2), which is leading to increased noise. The integrated input referred noise of the reference design is larger compared to the new design.

7.11.4 carrier detect threshold

The carrier detect threshold variation of the new design in the logarithmic domain ($\sigma(S_{det}(T)|_{dB})$) is lower compared to the reference design.

The largest variation of the carrier detect threshold $\sigma(S_{det}(T)|_{dB})$ is at T=-50°C. The simulated carrier detect threshold is normally distributed on a logarithmic scale (figure 7.17(b)) within a significance level of 5% of the Anderson-Darling-test.

For a yield estimation, a lot of more simulation runs or a high yield simulation would be required to verify the distribution of the carrier detect threshold voltage.

7.11.5 Comparison table

Table 7.1 shows the compared parameters of two different limiting amplifier designs.

	reference design	new design
gain stage	triode load	unfolded diode load
input / load transistor	NMOS / PMOS	NMOS / NMOS
number of gain stages N	7	8
rectifier	gilbert cell	diode mirror with current source
$\mu(A_{limiter}(f = 125kHz))$ /dB	60.5	63.4
rel. std. $\frac{\sigma(A_{limiter})}{A_{limiter}} \cdot 100\%$	3.8 %	4.7 %
rel. drift $\Delta A_s/dB$	3	2.2
$f_{-3dB,LP}/kHz$	162.5	192
$f_{-3dB,HP}/kHz$	10.8	40.4
input referred noise density $\frac{S_{U^2,in}(f=125kHz)}{df}/\frac{nV}{\sqrt{Hz}}$	129	113.7
integrated input referred noise $S_{U^2,in}/\mu V$	60.2	51.8
current consumption I (T=27°C) $/\mu A$	1.02	1.12
area of limiting amplifier & RSSI + area of offset control $/(\mu m)^2$	1400 + 9000	3100 + 9000
carrier detect threshold variation $\sigma(S_{det}(T)\|_{dB})$ /dB	0.715	0.436
max. |RSSI error| over corner and temp. /dB	4	3
$FOM \cdot 10^6/(dB \cdot (\mu m)^2 \cdot \mu A)$	132	169

Table 7.1: Table for comparison of limiting amplifier designs

7.11.6 Figure of merit

In this design the most important parameters are summarized in a figure of merit (FOM). The most important parameters for this design are: area, current consumption, and carrier detect threshold variation. These parameters are multiplied, leading to a FOM of equation 7.24.

$$FOM = \frac{1}{A \cdot \sigma(S_{det}(T)|_{dB}) \cdot I} \tag{7.24}$$

Due to much lower $\sigma(S_{det}(T)|_{dB})$, the new design has a better FOM (table 7.1) compared to the reference design.

8 Summary and Outlook

8.1 Summary of thesis

An overview of the specifications for the limiting amplifier design is given in **chapter 2**. Due to the required ultra low power consumption, it is necessary to discuss the weak inversion operation of a MOS transistor explained in **chapter 3**.

In the main part of the thesis, different structures of gain stages (**chapter 4**) and rectifiers (**chapter 5**) are investigated with special regard to ultra-low-power, AC gain, noise, bandwidth, and PVT robustness of the design. Some of the gain stages and rectifiers, presented in this thesis have a different architecture than the ones, described in the mentioned publications for limiting amplifiers ([3] [4] [5] [6] [7] [26]). The developed limiting amplifier of this thesis operates at a lower frequency and consumes a some magnitude less current, $1.1\mu A$ instead of several mA, compared to the limiting amplifier in these publications.

In **chapter 6** a new architecture of gain stages and rectifiers are chosen for a new design and the architecture is briefly described. The design and simulation of an improved limiting amplifier is explained in **chapter 7**. The RSSI current of the new design is investigated with respect to variation process corners and temperature. An offset control is implemented with special focus on bandwidth and noise. For a fixed current consumption, a noise optimization of the limiting amplifier is done. Some AC parameters of the structures are validated in a Monte Carlo simulation at different temperatures. A transient Monte Carlo simulation with variation of temperature is examined to evaluate the variation of the carrier detect threshold voltage, which is the most critical parameter of the design. By post processing the results of the simulation are verified with respect to the specification of the design. The evaluation of the datagram mode is investigated with a transient noise simulation.

The designed limiting amplifier fulfills all the specifications. The new design is compared to a reference design, which has similar performance parameters. Some parameters for the new limiting amplifier design like area, current consumption are slightly deteriorated but the carrier detect threshold variation and the RSSI error are significantly improved.

8.2 Outlook - limiting amplifier & RSSI

8.2.1 More simulations

Before the new design is implemented on a test chip or a product some more simulations have to be done, to verify that the design satisfies all the given specifications. The most important simulations that have to be done before implementation are listed here:

- Top level simulation of carrier detection with bandgap, trimmed currents and comparator
- Detailed transient noise simulation for datagram demodulation
- Simulation with parasitic extraction of layout
- Transient start-up time of the limiting amplifier

Because some simulations like top level, detailed transient noise and simulation with parasitic layout take a lot effort (layout is not done yet), these simulations are not concluded in this work. The transient start up of the circuit has to be investigated as well. By additional circuitry the poles can be shifted to get a faster settling and the large C_{GmC} capacitor can be pre-charged to reduce the settling time. This is already implemented in the reference design and can be also applied with minor changes for the new design.

8.2.2 Further optimization

The **current consumption** of the whole limiting amplifier can be improved by using fewer parallel gain stages. This will lead to increased noise of the limiting amplifier. For this scenario a more detailed noise evaluation of the datagram demodulation has to be done.

The **area** of the offset control capacitor can be optimized. As the required low cutoff frequency is indirectly proportional to the capacity and gm of the GmC filter, gm can further be lowered by a lower bias current. Thus for the same cutoff frequency less area can be used. The bias current for the OTA is already very low at $I_{B\_GmC} = 1nA$. Further reducing the bias current can increase the cross-talk to high ohmic nodes or inaccurate transistor models in this operating point can differer from the simulated behavior.

8.2.3 Physical implementation on a chip

The real behavior of the new limiting amplifier design can be verified with a test chip. Most transistor models focus on the accuracy of strong inversion rather than weak inversion. Thus the real performance of the design (weak inversion) may differ more from the expected or simulated performance than the performance of design in strong inversion.

8.2.4 Other structures

The large intrinsic bandwidth of the unfolded diode load with rectifier gain stage (chapter 4.6 and chapter 5.6) could be used at applications for which a higher bandwidth is required. In such a design bandwidth and not noise (as in the design of this thesis) can be the dominating factor for the current consumption. The architecture also shows good simulation results when operated in strong inversion with adapted dimensioning.

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