Philipp Tomaschitz, BSc

Concept and Development of an NFC Power Source

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Supervisor

Ass.Prof. Dipl.-Ing. Dr.techn. Peter Söser
Institute of Electronics

Dipl.-Ing. Christoph Steffan, BSc
Infineon Technologies Austria AG

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Affidavit

I declare that I have authored this thesis independently, that I have not used other than the declared sources/resources, and that I have explicitly indicated all material which has been quoted either literally or by content from the sources used. The text document uploaded to TUGRAZonline is identical to the present master's thesis.

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Kurzfassung

Die verfügbare elektrische Leistung in passiven NFC Transpondern ist durch die limitierte Sendeleistung des Lesegerätes begrenzt. Wenn ein solcher passiver NFC Transponder einen zu hohen Laststrom aufnimmt, kann es in ihm zu Spannungseinbrüchen und auch zu Verbindungsabbrüchen kommen. Diese unerwünschten Ereignisse können deshalb durch Regelung der maximalen Leistungsaufnahme des passiven NFC Transponders verhindert werden.

Ein integrierter Spannungsregler für passive NFC Transponder wird in dieser Arbeit vorgestellt. Neben einer geregelten Ausgangsspannung zwischen 1.1 V und 4.2 V für nachfolgende Schaltungen bzw. Lasten, kann noch der Spannungsabfall an der Eingangsspannung zwischen 2.5 V und 4.4 V geregelt werden. Ein Linearregler ohne externer Stützkapazität mit einem PMOS Transistor als Stellglied wird zum Regeln der Ausgangsspannung verwendet. Der Spannungsabfall am Eingangspin wird durch Vergleichen mit einer Referenzspannung erkannt, wodurch das Referenzsignal des Linearreglers angepasst wird. Der Entwicklungsprozess dieses analogen Reglers und die Verifikation anhand unterschiedlicher Simulationen werden in dieser Arbeit vorgestellt.

Die NFC Power Source ist in einem 130 nm Standard Infineon CMOS Doppelwannenprozess implementiert und benötigt ungefähr 0.049 mm^2 Chipfläche. Ein Ruhestrom von 35 μA ist für den regulären Betrieb der Schaltung notwendig. Ein stabiles Verhalten der beiden Regelschleifen kann für einen Lastwiderstand von 1 kΩ mit Lastkapazitäten zwischen 20 nF und 500 nF garantiert werden. Mindestens eine 160 pF große Lastkapazität muss an den Ausgang geschlossen werden, falls kein Lastwiderstand verbunden ist. Anhand dieser Spezifikationen eignet sich die vorgestellte Schaltung hervorragend als Spannungsregler für passive NFC Transponder.

Abstract

The available electrical power in passive NFC devices is limited due to the finite transmission power of the reader device. If such a passive NFC device consumes a too large load current, the NFC field is overloaded which causes an under-voltage brown out of the NFC tag and a connection abort to the reader device. It is possible to prevent these unwanted occurrences by controlling the maximum consumed power of the passive NFC device.

A fully integrated power management solution for passive NFC devices is implemented in this thesis. Besides a regulated output voltage between 1.1 V and 4.2 V for following circuits or loads, a voltage decrease on the input pin of the Power Source can be controlled between 2.5 V and 4.4 V. A capacitor-less low-dropout voltage regulator with a PMOS transistor as pass device is used to control the output potential to the defined level. The decrease of the input voltage is detected by comparing it with a reference potential and correspondingly adjust the reference node of the low-dropout voltage regulator. The development process of this analog control circuit and the verification based on several simulations are shown in this thesis.

The NFC Power Source is implemented in a 130 nm standard twin well Infineon CMOS process and consumes about 0.049 mm^2 chip area. A quiescent current of 35 μA is necessary to supply the circuit during active operation. A stable behavior for both control loops can be guaranteed with a load of 1 kΩ in parallel to a load capacitor with a capacity between 20 nF and 500 nF. A minimum capacitive load of 160 pF is necessary to operate the circuit without a resistive load. Related to these specifications, the proposed circuit is perfectly convenient as a power management unit for passive NFC devices.

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Chapter 1

Motivation

In recent years, RFID (Radio-Frequency Identification) systems have been widely used for a variety of applications. Contactless payment systems, access control, animal identification and electronic passports are just a few areas where this technique is used [1]. The NFC (Near Field Communication) standard prevailed especially for mobile devices and is nowadays implemented in almost every smartphone. Besides the main application areas of NFC products, which are contactless payment and data transfer, also sensor interfaces [2] and other passive electronic devices are gaining importance. These passive applications are supplied with energy from the smartphones NFC reader device via the antenna's electromagnetic field [1]. Due the limited amount of electrical power, which can be provided by these, an energy storage like a capacitor can be implemented in the passive application. Another use case for an energy storage device is to provide a power supply to the passive device, also when the NFC field is gone or out of range. Charging an empty energy storage device through the field can overload it and might cause connection problems. The field is also unwanted stressed by current peaks and load currents which are caused by switching operations or load jumps in the passive application.

A fully integrated on-chip voltage regulator to protect the NFC field of the smartphone from overloading is implemented in this thesis. The voltage regulator - in this thesis named Power Source - allows the passive device to charge high capacity capacitors through the NFC field and prevents there also the visibility of unwanted current changes. To combine the whole power management for these applications in one circuit, the Power Source should also provide a regulated output pin.

These two occurrences are the motivation to develop the NFC Power Source. Besides the analog transistor level design also the layout is implemented in this thesis. To make the circuit adaptive and usable for a wide range of different applications, the maximum input power and the potential of the output voltage are implemented adjustable.

Chapter 2

Introduction

This introductory chapter gives an overview of the implementation of the NFC Power Source within the NFC system. The specifications of this circuit and the provided signals of the analog front-end are defined. Several state-of-the-art concepts are discussed in the last part of this chapter and the need of a new concept is shown. In the outline, a short overview of the following chapters of the thesis is presented.

2.1 Application Overview

The Power Source is, like mentioned in the motivation, implemented as a power management unit in a passive NFC device. An overview of the complete system is presented in figure 2.1. Energy for the system is provided through the reader device of the smartphone. The analog front-end in the inductive coupled passive device can extract sufficient power from the magnetic field to ensure proper operation. Therefore, it can be seen as link between the high frequency transmission channel and the implemented functions of the passive device. A detailed explanation and schematic of the analog front-end design can be found at page 318 in [1]. The Power Source is following the analog front-end. The circuit is supplied through it with a constant DC (Direct Current) voltage between 3.3 V and 4.5 V. The load of the Power Source is either an energy storage device like a capacitor or an additional electrical circuit. To meet the requirements for a wide variety of load applications, the output voltage of the Power Source can be adjusted by the digital block of the NFC tag.

The whole technical and physical background for an NFC system is presented in [1] and is not described in any more detail in this thesis.

Besides the supply potentials V_{in}, $V_{DD,digital}$ and ground, some additional signals are provided from the analog front-end and the digital block to the Power Source. All digital signals use a positive logic with 0 V and 1.2 V. $V_{DD,digital}$ is permanently supplied with 1.2 V. To prevent the load capacitor from discharging when the NFC field is not available and the capacitor is charged, an enable signal is implemented in the digital block. The Power Source must exhibit high impedance if the enable signal is logical low. Two separate 5 Bit signals $set_{V,in}$ and $set_{V,out}$ define the level of input- and output voltage in 100 mV

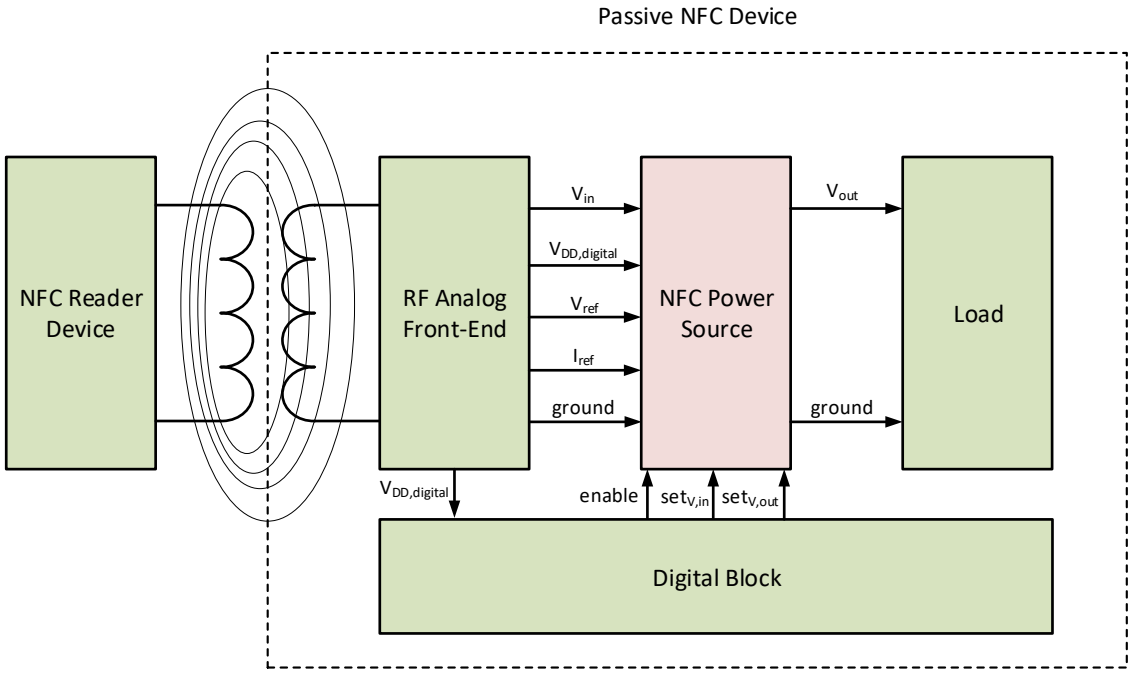

Fig. 2.1: Power Source - Application. The NFC Power Source inside the passive NFC device is implemented in this thesis.

steps of the Power Source. A reference table for setting the different voltage levels is attached in the appendix in table A.1 and B.1. A stable reference voltage V_{ref} with 1.2 V and a 1 μA bias current I_{ref} is also provided by the front-end to the Power Source.

To save costs and to make the circuit also usable for a wide range of different applications, a fully integrated solution should be sought. This means, that the use of external components like decoupling capacitors is not possible. The used technology is a 130 nm standard twin well CMOS (Complementary Metal Oxide Semiconductor) Infineon process with an additional polysilicon layer.

2.1.1 Modeling of the Analog Front-End

Because the Power Source is supplied by the analog front-end, this must be also considered in the design process. Therefore, a model to describe the electrical behavior of it is necessary. The analog front-end model is presented in figure 2.2 and comprises a DC voltage source V_{supply} and a serial internal resistance R_{source} which represents the load current dependent voltage drop across the source.

To calculate the source resistance of the analog front-end model, the provided power through the NFC field of smartphones in the passive NFC device must be known. Therefore, measurement results of three different standard commercially available smartphones are shown in table 2.1. As it is depicted, the provided power varies strongly between the presented models and is also dependent from the used analog front-end. In this thesis, the

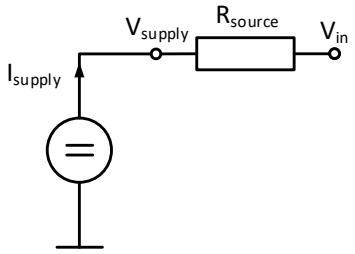

Fig. 2.2: Analog Front-End - Equivalent Circuit Diagram. The analog front-end is modeled by a DC voltage source and a series resistor.

provided electrical power P_{supply} is set to 100 mW.

Smartphone Model	**Provided Electrical Power**
Mobile Phone 1	40.25 mW
Mobile Phone 2	11.59 mW
Mobile Phone 3	125.56 mW

Table 2.1: The electrical power in the passive NFC device which can be provided by different smartphone models.

R_{source} can be calculated by the voltage and current relation of the electrical power in a circuit. The source resistances are calculated for $V_{supply} = 3.3\,V$ and 4.5 V.

$$P_{supply} = V_{supply} \cdot I_{supply} = \frac{V_{supply}^2}{R_{source}} \tag{2.1}$$

$$R_{source} = \frac{V_{supply}^2}{P_{source}} = \frac{3.3\,V^2}{100\,mW} = 109\,\Omega \tag{2.2}$$

With the same way of evaluation, $R_{source} = 203\,\Omega$ for a supply voltage of 4.5 V.

A more powerful analog front-end leads to a decrease of the internal source resistance and the voltage drop across it.

2.1.2 Modeling of the Load

The Power Source should be able to charge capacitors with a capacity larger than 1 μF. In this case, the load is modeled by a capacitor. Additional electrical circuits, which can also be a load type, are represented by a parallel connection of a resistive-capacitive circuit. To ensure stable operation with this particular type of load, it is necessary to define the minimum output capacitance and resistance limits for the Power Source output pin which is done in chapter 6.

2.2 Requirements for the NFC Power Source

The main idea to develop such a Power Source is to prevent large load currents from overloading the NFC field. This happens when the current consumption of the load and Power Source is too high for the analog front-end which leads to an under-voltage brown out of the NFC tag and further to a connection abort to the NFC reader device.

To prevent this unintentional drop in voltage, the Power Source controls the maximum output power of the analog front-end by controlling their lower limit of the input voltage V_{in} to a defined value which also controls the maximum voltage drop across R_{source}. This means, that the input voltage regulation of the Power Source is enabled when V_{in} decreases below the defined limit due to a too large current I_{supply} through R_{source}. The lower limit of V_{in} is realized adjustable between 2.5 V and 4.2 V in 100 mV steps to make the Power Source adaptable to different V_{supply} and P_{supply} levels. Of course, the transient response of the input voltage regulation must be fast enough to ensure that the analog front-end never gets overloaded. The potential of the output voltage V_{out} is also realized adjustable between 1.1 V and 4.2 V in 100 mV steps to provide different output levels. It should be noted, that the maximum output voltage can not be higher than V_{in} minus a voltage drop V_{drop} across the Power Source.

2.3 State-of-the-Art Concepts

Other ICs (Integrated Circuits) also offer similar functions like the NFC Power Source. The power management functions of the input- and output pins of two state-of-the-art IC solutions are compared with the Power Source in table 2.2.

IC Solution 1	**IC Solution 2**	**Power Source**
unregulated output voltage	adjustable regulated output voltage	adjustable regulated output voltage
unregulated input voltage	current regulated input	maximum input current is defined with the input voltage drop

Table 2.2: Comparison between state-of-the-art ICs and the Power Source.

IC solution 1 has an unregulated input- and output pin. Therefore, the circuit has no possibility to control the input power consumption or the output voltage level. In contrast to this, the second IC solution provides an adjustable output voltage with a low-dropout regulator and a current regulated input pin. This is realized by an additional linear regulator which limits the charging voltage and fixes the input current to a predefined value.

2.4 Why a new Concept?

As discussed in section 2.3, circuits with different concepts to manage the maximum load current of a low power voltage source are available. In IC solution 2, the predefined current

limit can be too high or too low which results in an over- or under-loading of the voltage source. The circuit presented in this thesis makes it possible to adjust the maximum consumed input power individually to the specifications of the application. Therefore, the Power Source is a multi functional power management circuit which is usable for a wide range of different applications and power levels.

2.5 Outline

After defining the functions and specifications of the Power Source, the concept of the control loop and a block diagram of the implemented circuits in the Power Source is introduced in the next chapter. The design considerations to implement the circuits are done in chapter 4. In this chapter, the functions of each block are explained and the frequency behavior of the control circuits is investigated. The next chapter shows the transistor level design of the most important circuit blocks and also gives a guideline into the design procedure. Besides that, also the final layout and a floorplan is presented in this chapter. The verification of the Power Source is done in chapter 6 on the base of simulation results with nominal process parameters. Also the minimum and maximum specifications of the loads for a stable operation are discussed there. Monte Carlo simulations are used to investigate the circuit behavior also for process and mismatch variations. A conclusion of the final design of the Power Source is shown in chapter 7. In the last part of this thesis, an outlook is presented where further improvements and investigations are discussed.

The transistor level design is implemented in the CADENCE Virtuoso EDA (electronic design automation) platform. All simulations are done with the internal CADENCE Spectre simulator. The evaluation of the simulation results are realized with MATLAB.

Chapter 3

Concept of the Power Source

The Power Source concept, developed by the specifications mentioned in the last chapter, is shown here. Before the concept is introduced, some considerations about the used output voltage regulator need to be made. After defining the most suitable topology, the concept is introduced. A block diagram of the whole Power Source gives an overview of the implemented circuit blocks. The control loop with all involved circuit elements is shown in the last part of this chapter for a better understanding of the control behavior of the Power Source.

3.1 Considerations for the Concept

As the topology of the output voltage regulator significantly affects the structure of the concept and the behavior of the Power Source, it is important to give a short overview of the available ones. Due to that enumeration, the most suitable topology for this application is chosen in this section.

3.1.1 Output Voltage Regulator Topology

To fulfill the given specifications from chapter 2, the proposed topology for the output voltage regulator is an LDO (Low-Dropout Voltage Regulator). In [3] the two main types of on-chip voltage regulators are discussed. The comparison between a switched inductor buck converter and an LDO shows that this kind of voltage regulator is more suitable for fully integrated circuits due to the lack of external components like inductors. The working principle of such a circuit is discussed in section 4.1.

3.1.2 Choosing the Right Pass Device

Because of the used CMOS technology, the pass device can be either an NMOS (n-Type Metal-Oxide-Semiconductor Field-Effect) or a PMOS (p-Type MOS) transistor. Both have significant impact on the characteristics of the voltage regulator. Choosing the correct pass devices is therefore an important step in the concept phase of the Power Source. In [4], all advantages and disadvantages of the possible pass devices are discussed. The

result of this research is summarized in the following enumeration.

NMOS Transistor as Pass Device:

- Common drain configuration (Source Follower) leads to a current independent gain of nearly one and no additional phase shift
- Charge pump necessary to achieve a low dropout voltage
- Higher charge carrier mobility results in smaller device dimensions

PMOS Transistor as Pass Device:

- Additional gain stage in the LDO due to the common source configuration of the pass device
- Gain and phase shift depend on the load current and therefore stability is more difficult to achieve
- No charge pump needed for low dropout voltages

At the first look, an NMOS pass device looks like the more comfortable solution for a stable LDO but the charge pump makes it unattractive [3][4]. However, the specifications demand an output voltage of 4.2 V. Accordingly, a gate potential referenced to ground, provided by a charge pump, greater than this voltage would be necessary. In the used process, this voltage could exceed the maximum ratings. Therefore, a PMOS transistor is chosen as the pass device for the Power Source.

3.2 Concept and Control Behavior

The before discussed circuit elements are essential for the concept because they have a strong impact on the used blocks inside the Power Source. Figure 3.1 shows the block diagram of the NFC Power Source. The pins placed on the dashed line of the schematic represent the input and output pins of the circuit. All other signals are generated inside the Power Source. The supply voltages $V_{DD,analog}$, $V_{DD,digital}$ and ground, the bias currents and the enable signals are not connected for a better clarity in this block diagram. As the enable signal is a digital signal, the potential must be shifted via a level shift circuit from $V_{DD,digital}$ to $V_{DD,analog}$ to make it usable for the analog blocks, which are supplied via $V_{DD,analog}$. The reference buffer prevents the implemented circuits from loading the reference voltage signal. To transform the digital 5 Bit signals $set_{V,in}$ and $set_{V,out}$ into 32 binary signals related to $V_{DD,analog}$, thermometer-decoders with subsequent level shift circuits are implemented. NMOS current mirrors distribute the bias current I_{ref} in the bias-block into different ratios inside the circuit. The power path in the Power Source leads from V_{in} to V_{out} via the pass device. Through the ground pin, all blocks inside the Power Source use the same reference potential as the analog front-end. A $V_{DD,analog}$-switch disconnects all analog blocks from their supply voltages when enable is logical low. Basically, the Power Source consists of an IVR (input voltage regulator - red color) and an OVR (output voltage regulator - blue color) which are separated by a decoupling device. They define the control behavior of the Power Source.

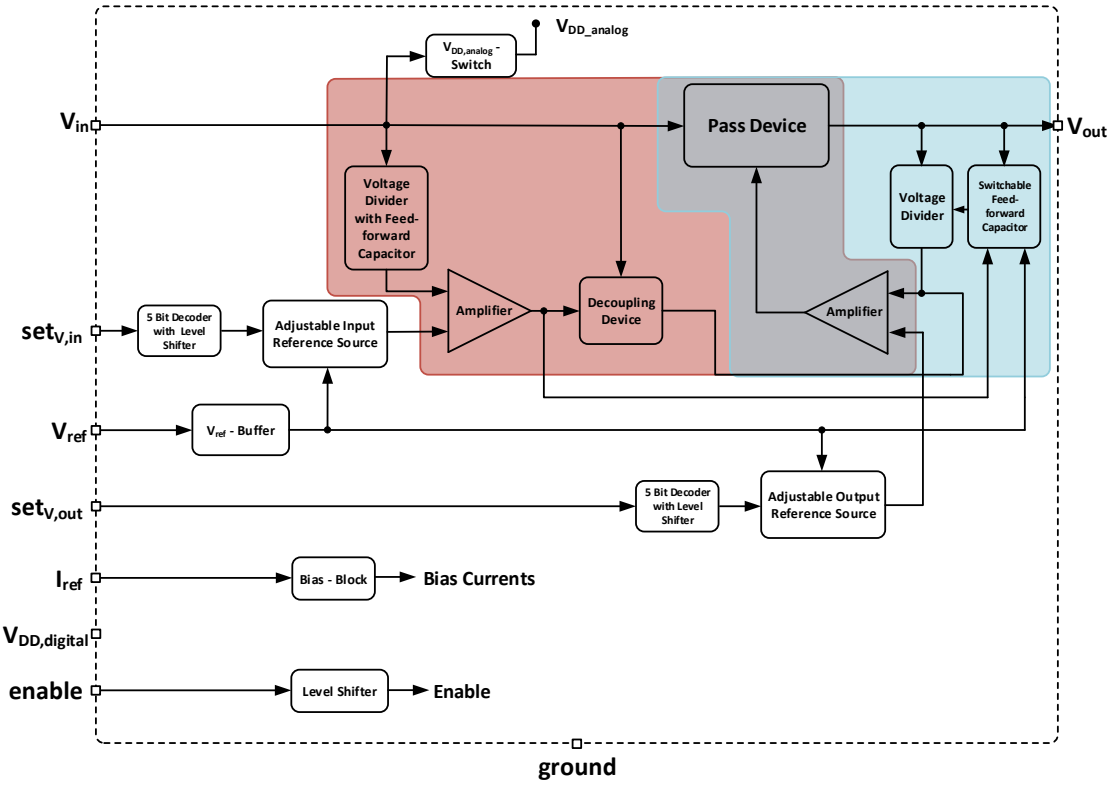

Fig. 3.1: Power Source - Block Diagram. Block diagram of the Power Source concept with all external signals. The internal bias currents, $V_{DD,analog}$, $V_{DD,digital}$ and the enable signal connections are not visible. The blue shape represents the output voltage regulator and the red one the input voltage regulator.

To understand the working principle of the Power Source, the control loop must be explained separately. A block diagram of the loops with all involved circuit elements is shown in figure 3.2. The pass device is the actuator in the loop. First, the output voltage control loop is investigated and the input voltage regulator is neglected. This can be assumed when V_{in} is above the defined limit by $V_{ref,in}$ and the input voltage divider. In this case, the decoupling device is closed and can not affect the reference signal of the OVR. Task of the output voltage regulator is to provide a regulated potential on the output pin of the circuit. This output voltage is defined by the reference voltage $V_{ref,out}$ and the ratio of the respective voltage divider. As the pass device only reduces the input potential, V_{out} is in normal operation below V_{in}. Due to negative feedback with the amplifier and the pass device, the output potential is kept at the defined voltage level. When V_{in} falls below the set input limit, the IVR amplifier opens the decoupling device which increases the reference potential of the OVR. The pass device acts now like before, when V_{out} is too high, and closes until V_{in} is equal to the defined input voltage limit. The internal source resistance of the analog front-end also affects the behavior of the Power Source but is not considered in this block diagram because it is not a part of the implemented circuit.

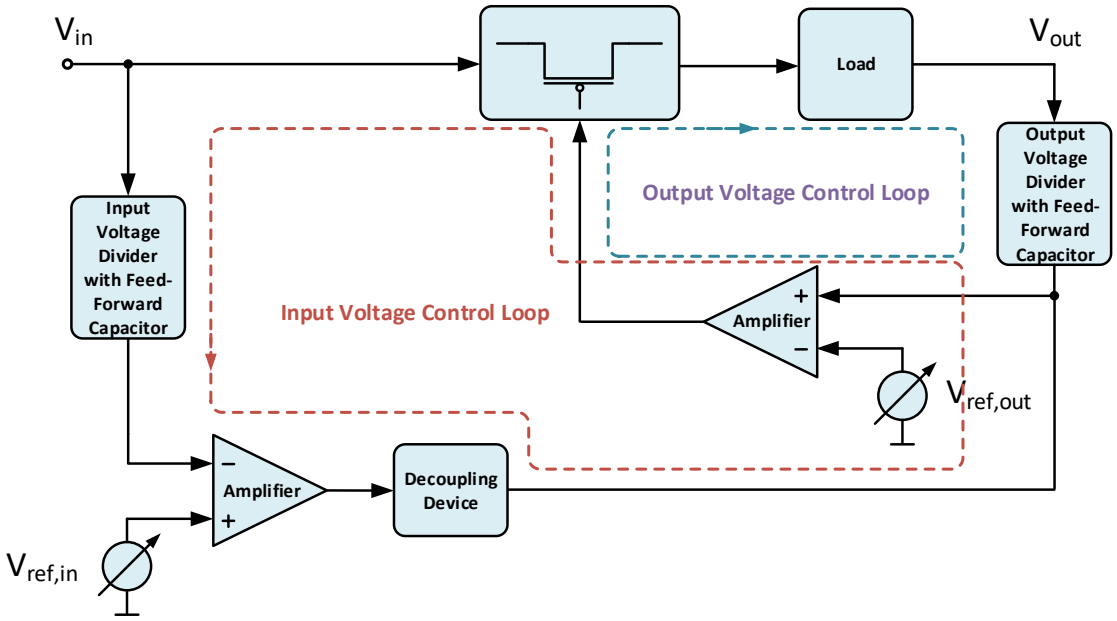

Fig. 3.2: Power Source - Control Loops. Block diagram of the control loops in the Power Source. The pass device is the actuator and controlled by the output voltage regulator. If V_{in} drops below the defined value, the input voltage regulator manipulates the output voltage control loop via the decoupling device.

The concept presented in this chapter allows to understand the working principle of the Power Source. Two separate control loops define the voltage levels via one PMOS transistor. The decoupling device connects both loops when the input voltage regulator needs to be active. If not, this element separates both loops. Achieving stability in the input voltage control loop might be an issue because of the signal flow through two amplifier stages. It can be seen that the loops only have an impact on the respective voltages which is important for further considerations.

Chapter 4

Design Considerations for the Power Source

Before the transistor level design is discussed, some considerations on the design are presented. This chapter gives an overview of the working principle and the frequency behavior of the used circuits of the Power Source. First of all, the output voltage regulator is described. This leads directly to the input voltage regulator. The next step is to combine both circuits to achieve the Power Source control behavior. Considerations to achieve stability, based on pole/zero analysis, are also done. After that, the adjustable voltage limits, the pass device, the switchable feed-forward capacitor and the enable function are observed.

4.1 Output Voltage Regulator

As mentioned before in section 3.1.1, a low-dropout regulator is used as output voltage regulator in the Power Source. To understand the working behavior of the circuit, the function of this circuit is explained in this section.

4.1.1 Low-Dropout Regulator Working Principle

An LDO is a closed loop system. The typical topology of this circuit, introduced in [5], is shown in figure 4.1. This kind of output voltage regulator consists of an error amplifier, a pass device (in this thesis a PMOS transistor) and a voltage divider at the output. Typically, the bulk of the PMOS transistor is connected to V_{in}, which is usually the highest potential in this circuit. This is an important information for the in section 4.5 discussed consideration.

The output voltage V_{out} gets divided via the two resistors based on equation 4.1 to the potential V_x.

$$V_x = V_{out} \cdot \frac{R_2}{R_1 + R_2} \tag{4.1}$$

This voltage is compared by the error amplifier with a stable reference voltage V_{ref}. The

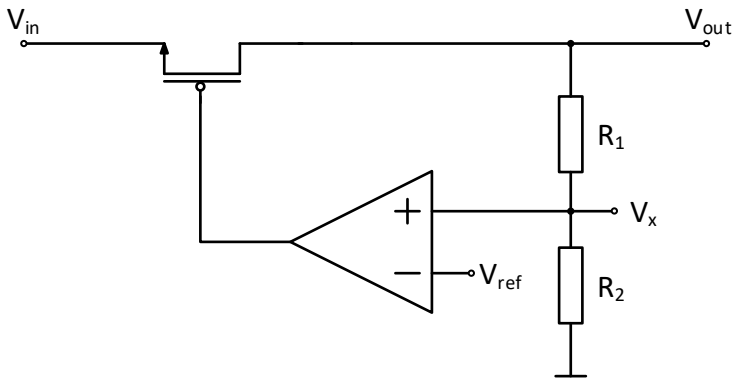

Fig. 4.1: LDO - Working Principle. The error amplifier tries to keep V_x equal to V_{ref} due to negative feedback with the pass device.

potential difference between V_{ref} and V_x is ideally kept at 0 V due to negative feedback. Therefore, V_{out} is described with following equation:

$$V_{out} = V_{ref} \cdot \frac{R_1 + R_2}{R_2} \tag{4.2}$$

To control the output voltage, the LDO sources enough current through the PMOS transistor to achieve the defined potential at the output pin. In this case, the closed loop system acts like a voltage source. The minimum drain-source voltage of the pass device, where the LDO works properly, is also called dropout voltage V_{do}. If the difference between V_{in} and V_{out} is smaller than V_{do}, the pass device is not able to source enough current and is forced into linear region. Thus, this type of operation is also called dropout region [5]. The minimum input voltage to ensure proper operation is defined with following equation:

$$V_{in,min} = V_{out} + V_{do} \tag{4.3}$$

4.1.2 Low-Dropout Regulator with an External Decoupling Capacitor

In a closed loop system, the phase margin is always an indicator for stability. The system is stable, if the phase shift at the unity gain frequency (where the gain is 0 dB) is less than $-180\,^\circ$ [6]. One method to achieve a stable LDO concept is to connect a high capacity capacitor C_{load} to the output [7]. The large capacitor leads to the dominant pole at this node. A model with all capacitors and resistors is necessary to begin with the AC analysis. The schematic for this circuit is shown in figure 4.2. The parasitic pass device capacitances are simplified and combined into one capacitor C_{PMOS} between the pass device gate and AC ground (this potential is at a constant DC voltage during the AC analysis and can be seen as a virtual ground potential during this analysis).

As proposed in [8], every node with a capacitance represents one pole. To simplify the calculation of the poles, the error amplifier in this schematic is assumed to be a one-stage amplifier and other parasitic capacities are neglected. Therefore, only two poles are left over for this evaluation. It is assumed that the LDO is in an operating point, where the

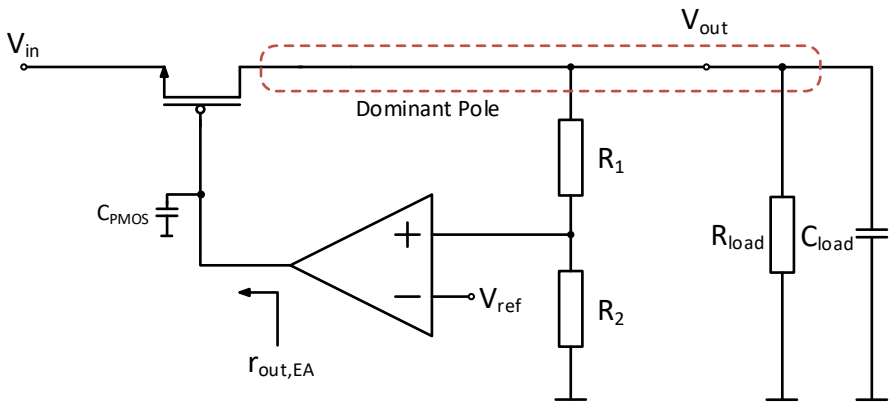

Fig. 4.2: LDO with External Capacitor. The output node with the large external capacitor creates the dominant pole. The second pole is located between the pass device and the error amplifier.

regulator works in proper operation and equation 4.3 is fulfilled. The dominant pole is defined by the large output capacitor with:

$$p_1 \approx \frac{1}{2 \cdot \pi \cdot C_{load} \cdot r_{out}} \tag{4.4}$$

With

$$r_{out} = R_{load} \parallel (R_1 + R_2) \parallel r_{DS,PMOS} \tag{4.5}$$

Where $r_{DS,PMOS}$ is the drain-source resistance of the pass device. The non-dominant pole can be described with:

$$p_2 \approx \frac{1}{2 \cdot \pi \cdot C_{PMOS} \cdot r_{out,EA}} \tag{4.6}$$

Where $r_{out,EA}$ represents the output resistance of the error amplifier. Another important parameter of the system is the open loop DC gain A_{DC}:

$$A_{DC} = A_{EA} \cdot A_{FB} \cdot A_{PMOS} \tag{4.7}$$

Where A_{EA} represents the amplifier gain, A_{PMOS} the current dependent gain by the transconductance of the common source stage of the pass device and the output resistance r_{out} and A_{FB} the gain which results from the feedback circuit and is defined by following equation:

$$A_{FB} = \frac{V_{ref}}{V_{out}} \tag{4.8}$$

The open loop transfer function $A_{OL}(s)$ is determined by opening the loop between the output of the error amplifier and the gate of the pass device. To evaluate the AC behavior, a sinusoidal signal is sent into the loop at the gate of the pass device. The response of the whole system on this signal is observed at the amplifiers output. This is repeated for several frequencies and results in the frequency-dependent transfer function of the system. All transfer functions of the following voltage regulators are determined with this method,

by opening the feedback loop between the pass device and the error amplifier. For the schematic presented in figure 4.2, the open loop transfer function results in:

$$A_{OL}(s) \approx \frac{A_{EA} \cdot A_{FB} \cdot A_{PMOS}}{(1 + s \cdot C_{load} \cdot r_{out}) \cdot (1 + s \cdot C_{PMOS} \cdot r_{out,EA})} \tag{4.9}$$

4.1.3 Capacitor-less Low-Dropout Regulator

Another commonly used LDO structure is the so called capacitor-less LDO (CL-LDO) [9]. When the large external capacitor is removed, the pole on this node moves to a higher frequency. In this approach, the gate of the pass device becomes the dominant pole of the system.

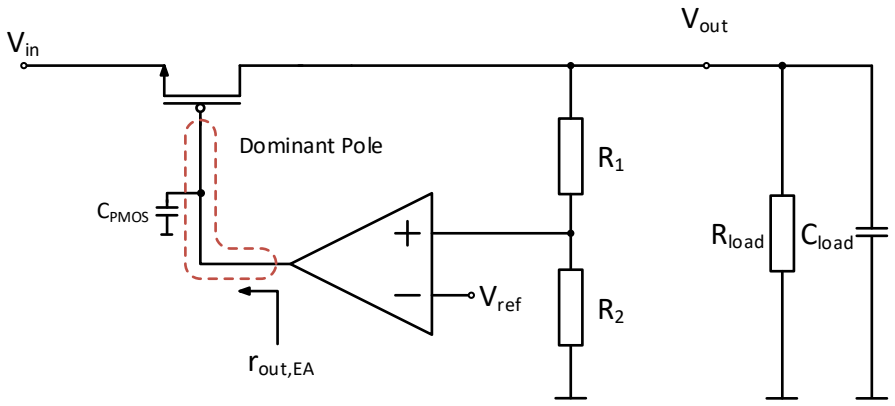

Fig. 4.3: Capacitor-less LDO. The node between the pass device and the error amplifier creates the dominant pole. The other pole is located at the output node.

The resulting poles of this structure are equal to the poles of the LDO with an external capacitor. Thus, both pole frequencies are defined by equation 4.4 and 4.6. The difference is in the frequency of the poles. Pole p_2 is now dominant and p_1 the non-dominant pole. Therefore, also the transfer function can be expressed like in formula 4.9. A disadvantage of this structure is, that achieving stability is difficult. Some compensation methods are discussed in section 4.4.

4.1.4 Proposed Low-Dropout Regulator Topology for the Power Source Application

In the last two sections the main structures of LDOs were discussed. The CL-LDO comes without an external decoupling capacitor which makes it attractive for fully integrated solutions. On the other hand, achieving a stable behavior is more difficult without the external capacitor. Despite this disadvantage, the capacitor-less topology is used as output voltage regulator in this thesis. The advantage of the missing capacitor outweighs. Of course, if the load capacitance gets too large, the location of the dominant pole changes. This is the case when the Power Source charges high capacity capacitors. Therefore, the output voltage regulator of the Power Source is designed to work stable without an

external decoupling capacitor but also needs to be stable when such a load capacitance is connected to the output pin.

4.2 Input Voltage Regulator

If a real voltage source provides a load current, the source voltage decreases due to the internal source resistance. To regulate this voltage decrease, a circuit is needed which controls the load current through the source resistance. This behavior is the working principle of the input voltage regulator. This circuit consists, like the low-dropout regulator, of an error amplifier, a pass device and a voltage divider. The difference is, that the input voltage regulator uses the input potential as control signal where a decrease causes the pass device to close. Since the current is reduced due to the closed pass device, also the voltage drop across the source resistance decreases.

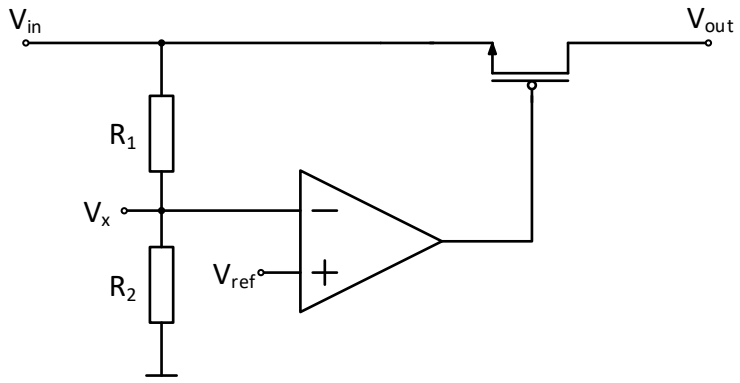

Fig. 4.4: Input Voltage Regulator - Working Principle. If the input voltage V_{in} decreases, the error amplifier closes the pass device to reduce the load current.

The maximum voltage decrease of V_{in} is defined by the input voltage limit $V_{in,limit}$ and can be calculated with:

$$V_{in,limit} = V_{ref} \cdot \frac{R_1 + R_2}{R_2} \tag{4.10}$$

If V_{in} sinks below $V_{in,limit}$, the potential between the voltage divider V_x decreases below V_{ref} and the error amplifier closes the PMOS transistor which results in a smaller load current. Thus, the voltage drop across the source resistance decreases and the circuit tries to regulate the input voltage to the level calculated by equation 4.10. By controlling the input potential to a constant value, also the voltage drop across the source resistance remains constant. Therefore, the control circuit consumes and provides a constant current and can be seen as current source.

As the input voltage regulator is in principle a flipped LDO, also the frequency behavior is nearly the same. The difference is in the direction of action. The regulator affects the input voltage of the circuit and not the output voltage. An equivalent circuit diagram of the input voltage regulator with a load capacitor and resistor is presented in figure 4.5. The supply voltage source can be replaced during the AC analysis in an operating point,

where the regulator works properly, by its ideal source resistance. Thus, the voltage source can be shorted. R_{source} represents the internal source resistance of the supply circuit.

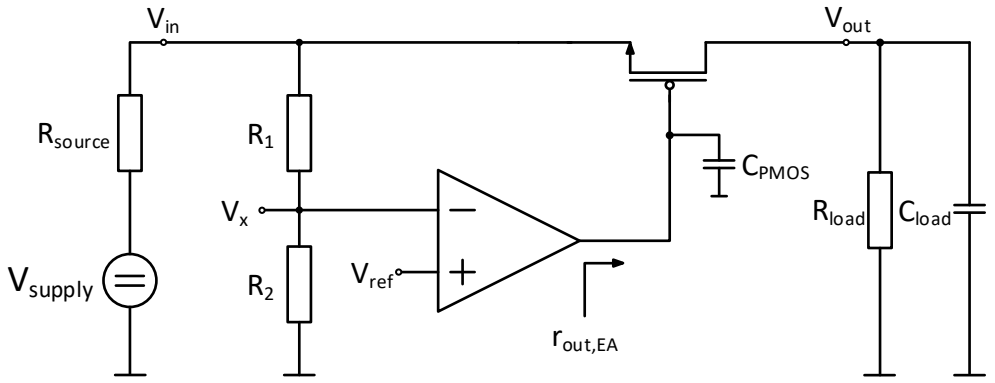

Fig. 4.5: Input Voltage Regulator - Pole Analysis. The schematic of the input voltage regulator with the connected load and the supply circuit with an internal source resistance R_{source}.

The calculation of the first pole is equivalent to the low-dropout voltage regulator due to the output resistance of the error amplifier $r_{out,EA}$ and the capacity of the pass device C_{PMOS}. This pole is defined by:

$$p_1 \approx \frac{1}{2 \cdot \pi \cdot C_{PMOS} \cdot r_{out,EA}} \tag{4.11}$$

The investigation of the impact of the load capacitor is more complex. A small signal model to calculate the transfer function from the gate of the pass device to the input pin is needed to evaluate the impact of the load capacitor on the input voltage regulator. This model is presented in figure 4.6. The error amplifier and the parasitic capacitor C_{PMOS} are not included in this calculation due to the already known transfer function of this circuit part.

The resistor networks in this circuit are simplified into R_{IN} and R_{OUT}, where R_{IN} represents the resistance $R_{source} \parallel (R_1 + R_2)$ and $R_{OUT} = R_{load}$. The open loop transfer function is defined by $\frac{v_{in}}{v_{out,EA}}$ where $v_{out,EA}$ is at the gate of the PMOS transistor and v_{in} at the input node. To determine the transfer function, an AC signal is applied in a DC operating point to the circuit at $v_{out,EA}$ and evaluated at the node v_{in}. By solving this transfer function, a zero and a pole is introduced and can be described with:

$$p_2 \approx \frac{R_{OUT} + r_{DS,PMOS} + R_{IN} + g_{m,PMOS} \cdot R_{IN} \cdot r_{DS,PMOS}}{2 \cdot \pi \cdot C_{load} \cdot R_{OUT} \cdot (r_{DS,PMOS} + R_{IN} + g_{m,PMOS} \cdot R_{IN} \cdot r_{DS,PMOS})} \tag{4.12}$$

Where $r_{DS,PMOS}$ represents the small signal drain-source resistance and $g_{m,PMOS}$ the transconductance of the pass device.

$$z_1 \approx \frac{1}{2 \cdot \pi \cdot C_{load} \cdot R_{OUT}} \tag{4.13}$$

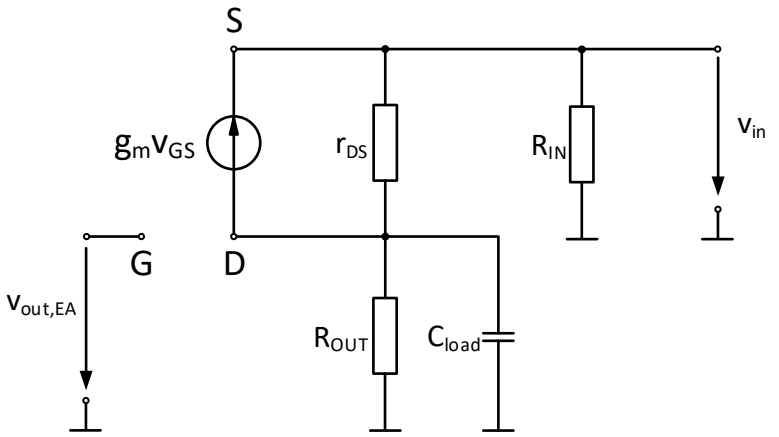

Fig. 4.6: Input Voltage Regulator - Small Signal Model. The small signal model of the input voltage regulator to determine transfer function from the gate of the pass device to the input node of the circuit.

The complete derivation is available in appendix C. The resulting poles and zeros are located nearly at the same frequency. Simulations showed, that the zero is placed few hertz below the pole frequency. Both cancel out each other and can be neglected for the further design process. In this configuration also the pass device behaves like an additional load current dependent gain stage. This gain is derived with the before discussed transfer function and is described by:

$$A_{PMOS} \approx \frac{g_{m,PMOS} \cdot R_{IN} \cdot r_{DS,PMOS}}{r_{DS,PMOS} + R_{OUT} + R_{IN} + g_{m,PMOS} \cdot R_{IN} \cdot r_{DS,PMOS}} \tag{4.14}$$

When p_2 and z_1 are neglected, the open loop transfer function $A_{OL}(s)$ of the system can be expressed as:

$$A_{OL}(s) \approx \frac{A_{EA} \cdot A_{FB} \cdot A_{PMOS}}{1 + s \cdot C_{PMOS} \cdot r_{out,EA}} \tag{4.15}$$

Where A_{FB} is the gain of the voltage divider circuit and determined by the ratio between V_{ref} and V_{in}. A_{EA} represents the gain of the error amplifier.

4.3 Combination of Input- and Output Voltage Regulator

To achieve the Power Source function, the output- and the input voltage regulator must be combined into one circuit which is the crux in this consideration. To reduce the voltage drop across the whole Power Source, a solution with one pass device is important. It is also necessary, that the input voltage regulator has priority over the LDO to prevent the input voltage from sinking below the predefined value.

The idea to combine both circuits is, that the input voltage regulator manipulates the low-dropout voltage regulator if the load current is too high for the voltage source. This can be achieved by controlling the potential between the output voltage divider and the

positive input pin of the error amplifier of the output voltage regulator. In the system approach, the input voltage control loop interacts with the pass device only if the input voltage has dropped below the defined level. As a result, the Power Source switches automatically from constant output voltage mode to constant current mode regulated by the IVR. It is not possible to connect the amplifier output of the IVR directly to this node because the amplifier would constantly regulate this node potential. To prevent this unwanted behavior, the two circuits must be decoupled by an additional transistor stage. This topology is a source follower in order to reduce the impact on the gain and stability of the input voltage control loop. The resulting topology is shown in figure 4.7. The decoupling device is the NMOS transistor.

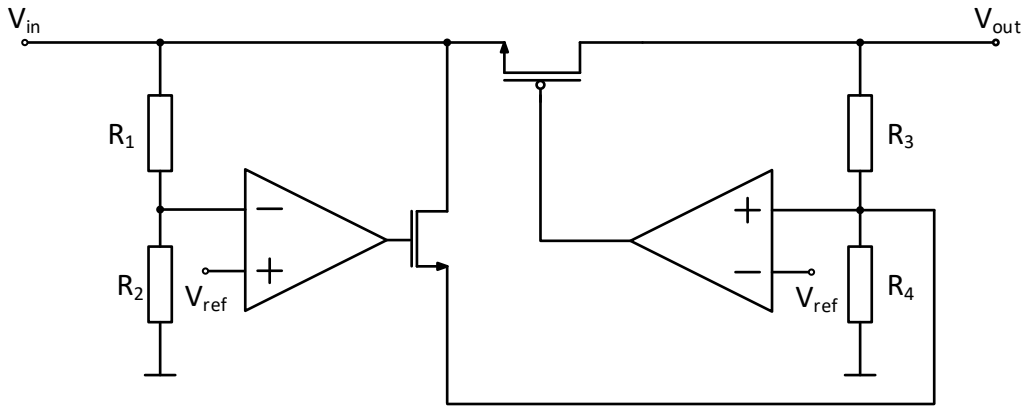

Fig. 4.7: Power Source - Working Principle. If V_{in} decreases, the IVR forces the LDO circuit to close the pass device by increasing the potential between R_3 and R_4 by the NMOS transistor (decoupling device).

If the input voltage is higher than the defined limit from formula 4.10, then the input voltage regulator is not active and the NMOS transistor is closed. In this case, the input voltage control loop has no influence on the low-dropout regulator. Thus, the output voltage is defined like in equation 4.2. When the load current increases and V_{in} decreases beneath the defined potential, the error amplifier of the input voltage regulator opens the NMOS transistor. This leads to a voltage increase over R_4 and the error amplifier of the LDO starts to close the pass device.

4.4 Pole/Zero Compensation of the Power Source

Theoretically, the in section 4.3 introduced Power Source works as expected but several aspects require further investigations to achieve the final circuit. The key issue in this design is to achieve a stable system without an external capacitor, as discussed in [10]. Therefore, some compensation techniques are needed for the final concept.

First of all, the output voltage regulator needs to be stabilized. Two different methods are proposed in [10] and [11]. One of them is to introduce a feed-forward capacitor C_{ff2} in parallel to the resistor between the output voltage and the feedback signal of the LDO. This leads to an additional pole-zero pair, which can help to increase the phase margin of

the system. The other way to achieve stability is to introduce a miller capacitance C_c at the pass device. This method makes the pole on the amplifier output more dominant and can also introduce a left half plane zero by adding a resistor R_c to the miller capacitor. Because the IVR is a flipped LDO, this structure needs also a compensation technique. The feed-forward capacitor C_{ff1} between input node and the feedback signal of the input voltage regulator is introduced. A problem is, that the input voltage regulator is linked with the pass device via the LDO. Therefore, the stability of this loop also depends on the LDO. One drawback of the feed-forward capacitor of the LDO is, that the input voltage regulator sees it as additional frequency pole. In the final circuit, the feed-forward capacitor is needed for the LDO but undesired if the input voltage regulator is active. Thus, the capacitor is made switchable. If the input voltage control loop is active, the switch between the feed-forward capacitor and the feedback signal is opened. If the output voltage regulator is active, the switch is closed and the capacitor is connected with the node. The final circuit of the input- and output voltage regulator of the Power Source is presented in figure 4.8.

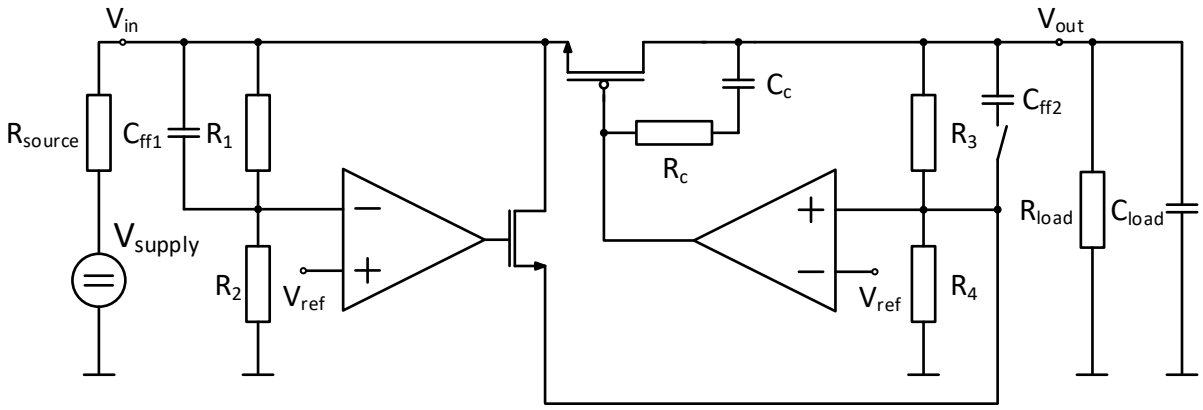

Fig. 4.8: Power Source - Topology with Pole Compensation. By introducing several pole compensation methods like feed-forward capacitors and a miller capacitor, both control loops can be stabilized.

4.4.1 Pole/Zero Analysis of the Compensated Output Voltage Regulator

By adding several methods to compensate the poles of the Power Source, zeros are introduced which also affect the pole locations. The impact of these methods on poles and zeros of the output voltage regulator of the Power Source are discussed in this section. The circuit to investigate, derived from the Power Source concept out of figure 4.8, is presented in figure 4.9. Due to a stable DC voltage, the supply voltage V_{supply} can be shorted during the AC analysis.

The dominant pole is, like for the CL-LDO, located between the error amplifier and the pass device. Because of the inverting amplifier structure of the PMOS transistor, the miller capacitor C_c is enhanced by the gain of the pass device at this node due to the miller effect [12]. The parasitic capacities of the PMOS transistor and high frequency poles are neglected. Referring to [13], the dominant pole is defined by following relation:

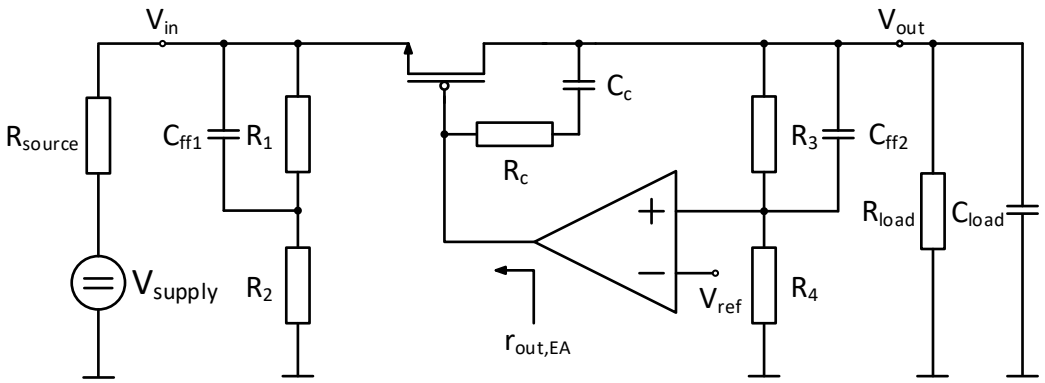

Fig. 4.9: Power Source - Compensated OVR. The circuit of the pole compensated Power Source in a DC operating point where the output voltage regulator is active.

$$p_1 \approx \frac{1}{2 \cdot \pi \cdot C_c \cdot r_{out,EA} \cdot g_{m,PMOS} \cdot r_{out}} \tag{4.16}$$

With:

$$r_{out} = r_{DS,PMOS} \parallel [((R_1 + R_2) \parallel R_{source}) + ((R_3 + R_4) \parallel R_{load})] \tag{4.17}$$

When $(R_1 + R_2) \gg R_{source}$ and $(R_3 + R_4) \gg R_{load}$, equation 4.17 can be approximated to:

$$r_{out} \approx r_{DS,PMOS} \parallel (R_{source} + R_{load}) \tag{4.18}$$

By adding a series resistor R_c to the miller capacitor, the zero from C_c can be shifted from the right half plane to the left [12] which leads to a desirable phase shift. The zero resulting from the miller compensation [11] is defined by:

$$z_1 \approx \frac{1}{2 \cdot \pi \cdot C_c \cdot \left(\frac{1}{g_{m,PMOS}} - R_c\right)} \tag{4.19}$$

The pole on the output node, referring to [13], is defined by:

$$p_2 \approx \frac{1}{2 \cdot \pi \cdot C_{load} \cdot \{[r_{DS,PMOS} + ((R_1 + R_2) \parallel R_{source})] \parallel [((R_3 + R_4) \parallel R_{load})]\}} \tag{4.20}$$

The feed-forward capacitor introduces a pole and zero [11]:

$$p_3 \approx \frac{1}{2 \cdot \pi \cdot C_{ff2} \cdot (R_3 \parallel R_4)} \tag{4.21}$$

$$z_2 \approx \frac{1}{2 \cdot \pi \cdot C_{ff2} \cdot R_3} \tag{4.22}$$

The DC gain of the output voltage regulator results from the product of the three gain stages error amplifier, voltage divider and pass device. Therefore, the open loop DC gain can be described with equation 4.7.

As presented in this section, the output voltage regulator has three poles and two zeros which can be adjusted in the design process. Technically, each pole leads to a $-90\,^\circ$ phase shift and every zero on the left half plane to a $+90\,^\circ$ phase elevation [6]. A design with a phase margin with more than $+45\,^\circ$ should be possible which is a minimum requirement for a stable operation of a system [6].

4.4.2 Pole/Zero Analysis of the Compensated Input Voltage Regulator

The signal path of the input voltage regulator passes the error amplifier and the pass device of the low-dropout voltage regulator. Therefore, a stable LDO design is a key issue to achieve stability in this control loop. As mentioned before, C_{ff2} is disconnected from the signal path if the input voltage regulator is active which prevents an additional pole at this node. The input voltage regulator uses like the low-dropout voltage regulator a feed-forward capacitor as compensation method. The impact of the used methods on the poles and zeros is derived with the circuit in figure 4.10. All relevant circuit elements for the input voltage control loop are shown there. As discussed before in section 4.2, the resulting pole and zero of the load capacitor are neglected because of the small difference in their frequencies and the negligible small impact on the overall frequency behavior. V_{supply} can be assumed to be shorted to ground during the AC analysis.

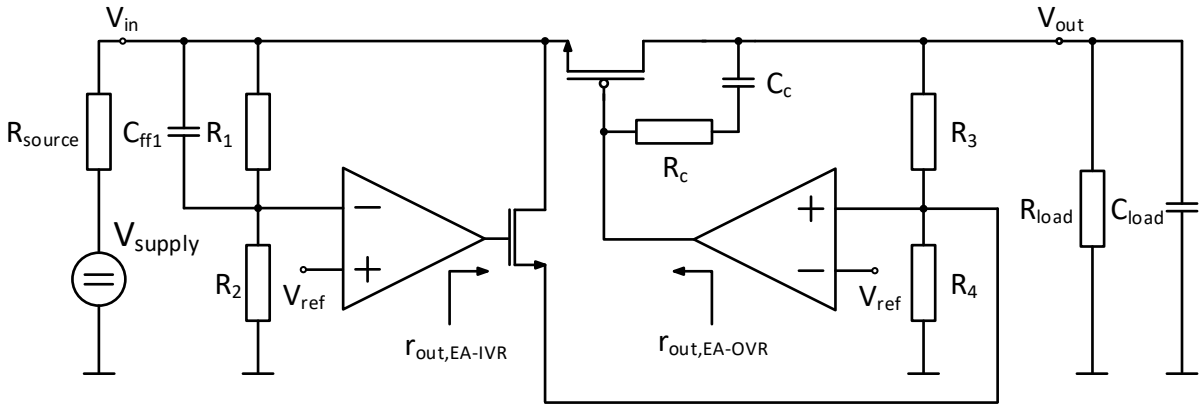

Fig. 4.10: Power Source - Compensated IVR. The circuit of the pole compensated Power Source in a DC operating point where the input voltage regulator is active.

As in the sections before, it is assumed that both error amplifiers are one stage circuits and parasitic capacities are neglected.

The pole between pass device and the error amplifier of the LDO is presented in equation 4.23 and can be derived by resolving the transfer function of the error amplifier and the pass device.

$$p_1 \approx \frac{1}{2 \cdot \pi \cdot C_c \cdot (r_{out,EA-OVR} + R_c + r_{out})} \tag{4.23}$$

Where r_{out} is equal to:

$$r_{out} = [r_{DS,PMOS} + ((R_1 + R_2) \parallel R_{source})] \parallel [(R_3 + R_4) \parallel R_{load}] \tag{4.24}$$

Due to the large dimensions of the pass device, this pole is the one which occurs at the lowest frequency in the input voltage regulator. Therefore, this pole is the dominant one in the circuit. The zero, which occurs due to the resistance of R_c and the capacitor C_c can be neglected in the design process, because of the high frequency. Since these components are connected to the output pin of the Power Source and the missing miller effect, the capacity is far too small to create a zero at a relevant frequency.

The non-dominant pole is introduced by the output node of the input voltage regulators error amplifier:

$$p_2 \approx \frac{1}{2 \cdot \pi \cdot r_{out,EA-IVR} \cdot C_{EA-IVR}} \tag{4.25}$$

Where C_{EA-IVR} represents the capacitance on the output node of the amplifier. As for the low-dropout voltage regulator, the feed-forward capacitor introduces a pole and a zero:

$$p_3 \approx \frac{1}{2 \cdot \pi \cdot C_{ff1} \cdot (R_1 \parallel R_2)} \tag{4.26}$$

$$z_1 \approx \frac{1}{2 \cdot \pi \cdot R_1 \cdot C_{ff1}} \tag{4.27}$$

In the design process, the zero introduced in equation 4.27 is the one which can be adjusted to achieve the best phase margin for the input voltage control loop.

The DC gain of the input voltage regulator is defined with:

$$A_{DC} = A_{EA-IVR} \cdot A_{EA-OVR} \cdot A_{PMOS} \cdot A_{FB} \tag{4.28}$$

Where the gain A_{PMOS} of the PMOS transistor is defined in equation 4.14. The gain of the feedback divider is determined by the ratio between the reference voltage of the input voltage error amplifier and the input potential of the circuit.

To ensure, that the dominant pole is located between the pass device and the output voltage error amplifier, the dominant pole of the input voltage error amplifier should be placed at a higher frequency than the dominant one of the error amplifier from the LDO. Normally, this is not a problem because of the different dimensions of the pass device and the decoupling transistor.

The dominant pole of the input voltage control loop is located at a higher frequency that the one of the output voltage control loop. This can be seen by comparing equation 4.23 with 4.16 and is due to the missing miller effect, which does not affect the input voltage side of the regulator. Thus, the input voltage control loop is faster than the output voltage control loop. By connecting two amplifiers in series, the overall transfer function is determined by the product of the two individual ones. Therefore, the slower amplifier is dominating the overall system behavior. In the case when the used amplifiers have two poles, the non-dominant pole of the input voltage error amplifier should be located at a higher frequency than the one of the output error amplifier in order to reduce the impact of the pole in the total frequency behavior of the loop.

The transfer function of the input voltage control loop is described by one zero and three poles. If the pole introduced by the feed-forward capacitor is located above the unity

gain frequency of the control loop, then the overall transfer function is not affected by it. Thus, two poles and one zero describe the frequency behavior of the input voltage regulator and achieving a phase margin larger than 45 ° should be possible. The stability of the input voltage regulator might be more difficult to attain than for the low-dropout regulator because of the combination of two control circuits. In the design process, the before discussed considerations must be taken into account.

4.5 Pass Device with Bulk Regulation

It should be considered, that the fixed bulk connection of the pass device to the input pin as shown in figure 4.8 is not possible for the Power Source. The PMOS transistor discharges a charged load capacitor in this configuration, if the input potential is one diode voltage below the output voltage, via the body diode. Therefore, a bulk regulation is necessary to automatically connect the bulk potential of the pass device to the highest voltage level in the Power Source. Such a circuit is shown in figure 4.11 and is realized by connecting two PMOS devices between the bulk potential and the source- and drain voltages [14].

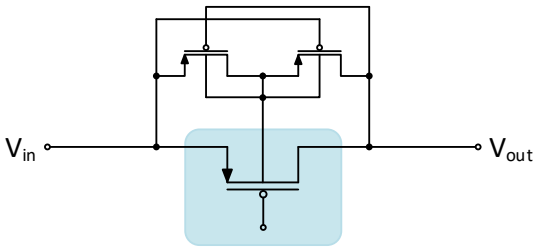

Fig. 4.11: Pass Device - Bulk Regulation. The bulk potential of the blue marked pass device is automatically connected to the highest voltage level.

4.6 Enable Function

The regulated bulk potential discussed before is also useful for the enable function. If this signal is logical low, the pass device gate is pulled up by a transistor to the regulated bulk potential to prevent the load from discharging. This is also possible without an applied voltage on the input pin of the Power Source. In section 5.1, the transistor level design of the pass device with the implemented enable function is presented.

Besides closing the pass device, the enable signal is used to achieve a power down mode in all circuit blocks to prevent a quiescent current through the Power Source. Thus, the $V_{DD,analog}$-switch is introduced. This switch is build up like the pass device circuit with bulk regulation. Due to a level shift circuit, the digital enable signal is shifted to this regulated bulk potential. Because of that, it is ensured that the switch can also be opened when the Power Source is not supplied. By opening the switch, all analog blocks are in a power down state and only a leakage current flows through the supplied circuits.

4.7 Adjustable Reference Voltages of the Error Amplifiers

To adjust the voltage levels on the input- and output pin, a solution that does not affect the poles by changing the output resistance of the system should be sought. This is realized by varying the reference voltages of the amplifiers with programmable voltage dividers. The topology of this circuit implementation is shown in figure 4.12. As discussed in the concept, 32 digital signals are provided by the demodulator to control the output voltage and the limit of the input voltage. Only one of the 32 signals is active at a time. A resistive ladder, consisting of 33 resistors, is supplied via the buffered reference voltage V_{ref}. Between every node of two resistors, one NMOS transistor for one control signal is placed to tap the different potentials. In this topology, nearly no current passes the transistors because of the connection of the outputs $V_{ref,in}$ and $V_{ref,out}$ to the high impedance amplifier inputs.

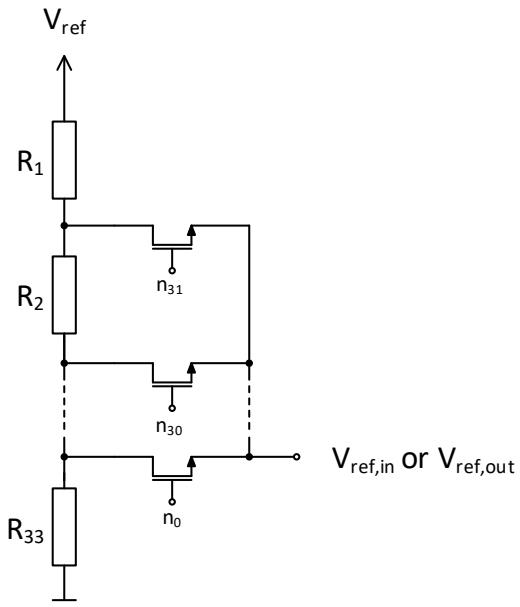

Fig. 4.12: Variable Voltage Reference Source - Working Principle. The circuit behaves like a potentiometer. Only one control signal is active which changes the divider ratio.

The total resistance of this resistive ladder should be as large as possible to reduce the quiescent current. In section 5.2.1, the calculations to dimension these circuits are done.

4.8 Switchable Feed-Forward Capacitor

The trigger to disconnect the feed-forward capacitor is the input voltage regulator. Therefore, the input pin of a comparator is connected directly to the output of the IVR error amplifier of the Power Source. This signal is compared to a reference potential, that should be higher than the lowest output voltage of this error amplifier. The inverting output of the comparator is connected to the gate of an NMOS switch, which is implemented be-

tween the capacitor and the input pin of the error amplifier. To precharge the feed-forward capacitor when the IVR is active, a voltage buffer is implemented to prevent loading of the variable output reference source. This procedure is essential, because of connecting an uncharged capacitor leads to an unwanted charging process which is visible in the output voltage of the Power Source. As the other output of the comparator, also the non-inverting one is connected to the gate of an NMOS transistor which works as switch and connects the feed-forward capacitor to the voltage buffer output when the input potential is below the defined limit and the input voltage regulator is active. The circuit for the switched feed-forward capacitor is presented in figure 4.13.

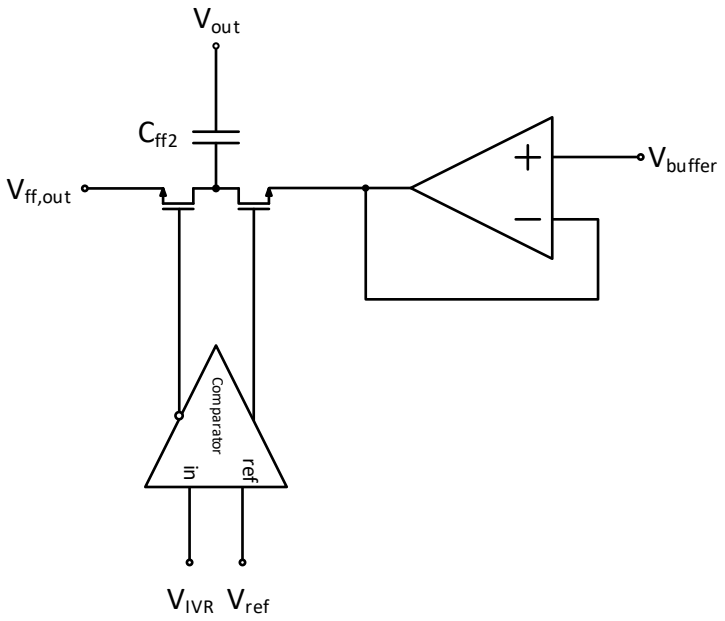

Fig. 4.13: Switched Feed-Forward Capacitor - Working Principle. If the IVR circuit is not active, the capacitor is connected to $V_{ff,out}$. If V_{IVR} is larger than V_{ref}, the feed-forward capacitor is charged by the buffer circuit to V_{buffer}.

In the design considerations, the most important mathematical relations between the circuit blocks of the Power Source are presented. The next step is to design all circuits on transistor level with the correct dimensioning of each device. Design considerations are an important step for the design process which can be seen as a kind of top-level design. The aim in this chapter is to understand how the circuit blocks and control loops relate to each other and which functions they have to fulfill.

Chapter 5

Design Process of the Power Source

The transistor level design process of the Power Source based on the discussed design considerations is explained in this chapter. At the end of this chapter, the implementation of all design blocks of the Power Source on transistor level is shown. First, the full pass device design with the enable feature is implemented. After that, the implementation of the output voltage regulator is derived. Based on this design, the input voltage regulator is implemented. In the last part, the top-level schematic and the final layout is shown.

5.1 Pass Device Implementation with Power Down Circuit

Due to the strict requirement of no quiescent current through the Power Source when no supply voltage is provided, a logic must be implemented to guarantee a closed pass device. The transistors M_1 and M_2 provide the regulated bulk voltage for M_{PD} as discussed in section 4.5. The transistor level implementation of the pass device with bulk regulation and power down circuit is presented in figure 5.1. If the enable signal is logical low, M_3 is opened and the inverter, consisting of M_5 and M_6 provides a logical high output which closes M_4 and pulls the pass device gate to the regulated bulk potential. Therefore, the pass device is closed due to a gate- source voltage of 0 V. In that case, only a leakage current passes M_{PD}. In the other case, when enable is logical high, M_3 is closed and M_4 is opened. Thus, the gate potential is defined by the output voltage of the LDO error amplifier. A logical signal disable is provided by the inverter also for other circuits. This signal is logical high when enable is logical low, also when the Power Source is not connected to an external supply voltage and a charged capacitor is connected at the output pin due to the regulated bulk potential. With this signal, it is possible to use PMOS transistors as power down switches. As nearly no load current passes the mentioned transistors M_1 - M_6, they can be designed with the minimal process dimensions.

The requirements on the PMOS pass transistor are to ensure a minimum area consumption at 200 mV voltage drop across it for the largest possible output current. The first step in the design process is to calculate the maximum output current I_{max} for the in chapter

2 defined 100 mW source. It is a fact that the largest load current occurs at the lowest output voltage. Therefore, $V_{out,min}$ is like discussed in chapter 2 set to 1.1 V.

$$P_{supply} = V_{out,min} \cdot I_{max} \tag{5.1}$$

$$I_{max} = \frac{P_{supply}}{V_{out,min}} = \frac{100\,mW}{1.1\,V} = 90\,mA \tag{5.2}$$

The W/L- ratio of the pass device M_{PD} is designed by setting V_{in} to the lowest available input potential of 3.3 V. After that, V_{out} is fixed in the simulation to 3.1 V by an ideal voltage source to ensure a 200 mV drop across the PMOS transistor. After that, the width of the device is increased until a current of 90 mA flows through it. To minimize the transistor area, the length of the device is set to the lower process limit which results in a larger leakage current when the pass device is closed.

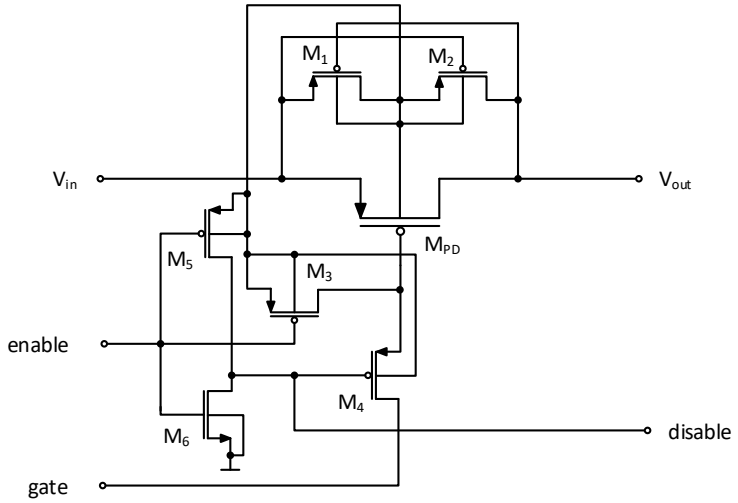

Fig. 5.1: Pass Device - Transistor Level Implementation. If the enable signal is logical low, the gate of the pass device is pulled to the regulated bulk voltage and closed.

5.2 Output Voltage Regulator Design

Since the pass device is now implemented, the design process of the output voltage regulator can start. The first step in this procedure is to define the resistors of the adjustable reference source and the output voltage divider. The development process of the output voltage regulator is referred to section 4.4.1 and figure 4.9. As the total resistance of R_3 and R_4 has a direct impact on the location of the poles, this must also be considered. The most important consideration for the ratio between R_3 and R_4 is the introduction of the feed-forward capacitor C_{ff2}. A large ratio leads to a large difference between the frequencies of the zero and pole, which are introduced by the feed-forward capacitor regarding equation 4.22 and 4.21. If they are not separated widely, the effect of the zero is barely

noticeable, because of the direct following pole. On the other hand, a large resistor ratio means that the adjustable reference source must adapt V_{ref} in very small steps to achieve the 100 mV steps at the output pin. Therefore, a trade off between all considerations has to be made. Due to that, the adjustable voltage reference source is designed to adapt the output voltage of it in 10 mV steps which leads to a ratio of $\frac{R_3}{R_4} = \frac{9}{1}$ to achieve the designated 100 mV steps at the output. The total resistance of R_3 and R_4 must not be too small to minimize the quiescent current. To prevent the charged load capacitor for discharging via the two resistors, an enable switch is implemented. This transistor closes the current path when the enable signal is logical low.

5.2.1 Adjustable Output Reference Source Design

The adjustable output reference source, introduced in section 4.7 and figure 4.12, is implemented to vary the input voltage of the error amplifier. As presented in section 4.7, the circuit can be seen as a resistor with an adjustable divider ratio. This circuit is supplied with 1.2 V via the reference buffer. Due to the predefined output potentials between 1.1 V and 4.2 V in 100mV steps and the ratio of the output divider, the resistor values of R_1 to R_{33} can be calculated. Because of the output voltage divider ratio, the potential on the output of the reference $V_{ref,out}$ must be between 110 mV and 420 mV. Therefore, the step size of the output potentials $\Delta V_{ref,out}$ is 10 mV. For the calculation, a step size between the resistors ΔR must be defined. Defining the upper resistance in a node as R_{up} and the resistance to ground as R_{down}, they can be expressed by the following equations:

$$R_{up} = \frac{V_{ref} - V_{ref,out}}{\Delta V_{ref,out}} \cdot \Delta R \tag{5.3}$$

$$R_{down} = \frac{V_{ref,out}}{\Delta V_{ref,out}} \cdot \Delta R \tag{5.4}$$

With the equations 5.3 and 5.4, R_1 and R_{33} are defined. The remaining resistors between them have a resistance of ΔR.

The switches are dimensioned to the minimum width and length, due to a very small current that flows into the gate of the amplifier.

5.2.2 Error Amplifier Design

By defining the resistors, also the input voltage levels of the error amplifier are defined. Therefore, implementing the error amplifier of the output voltage regulator is the next step in the design process. Due to the smallest output voltage of the adjustable reference source with 110 mV, a topology of an amplifier is needed which can be operated with such a low input common mode voltage level. Thus, a folded cascode OTA (Operational Transconductance Amplifier) structure with a PMOS input pair is chosen. In figure 5.2, the schematic of this circuit is shown. The requirements on the amplifier are a high DC gain to reduce the error in the output voltage and a large phase margin with the pass device as load. Because the provided supply voltage of the circuit depends on the input voltage of the Power Source, a stable operation of a supply voltage $V_{DD,analog}$ between

2.5 V and 4.5 V must be guaranteed. Another requirement for the error amplifier is to close the pass device strictly when a capacitor is charged to the defined output voltage potential to prevent an overcharging of the device. Because of the used structure, the output voltage is limited to two saturation voltages of the transistors M_5 and M_7 below $V_{DD,analog}$. Therefore, M_{10} and M_{11} are designed to source only a small current through the cascode output branches. If the transistors M_4 - M_7 are dimensioned correctly, a high output potential V_{out} forces them from saturation region into linear region which is necessary to close the pass device. A small output current leads also to a large output resistance of the circuit which is necessary to make the pole between pass device and amplifier dominant. M_3 sources a 2 μA current to ensure a high unity gain frequency with the input pair consisting out of M_1 and M_2. Typically, the input pair is designed with larger dimensions to decrease the offset voltage of the amplifier.

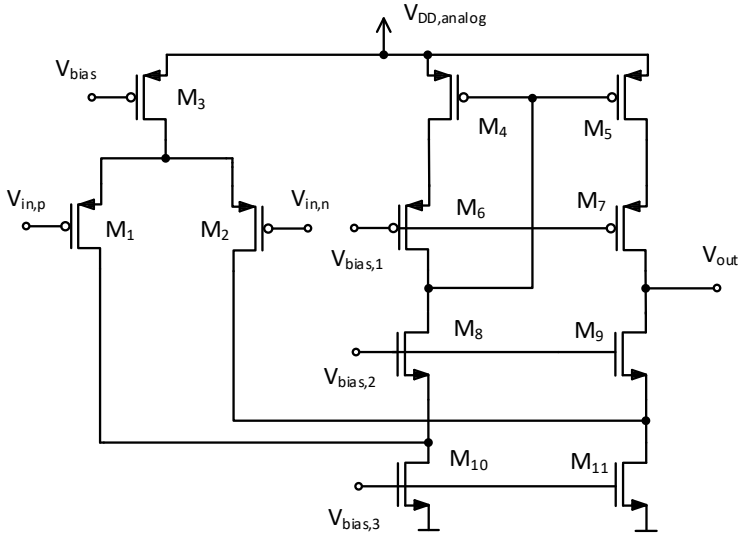

Fig. 5.2: Folded Cascode OTA. Used amplifier structure in the Power Source.

To verify the AC behavior of the circuit, a test bench is needed. The DC operating point of the circuit is determined by negative feedback. During the AC simulation, the OTA is operated in an open loop configuration with a load capacitor of 3 pF which represents the miller- and the gate capacitance of the pass device. The input common mode level in this simulation is set to 400 mV. To evaluate the bode plot, the CADENCE stability analysis function is used. In figure 5.3, the bode plot simulated with nominal process models for both $V_{DD,analog}$ limits is shown. As visible in figure 5.3, the unity gain frequency is 1 MHz for both supply voltage levels. The phase margin is 89 °, also for both voltage corners. 63 dB DC gain is enough to minimize the error, in combination with the other amplifying circuit parts, at the output voltage level to a negligibly small value.

5.2.3 Feed-Forward Capacitor

The feed-forward capacitor defines the frequency of the pole and zero introduced by it. To achieve the best result in the phase margin, the frequency with the highest phase shift

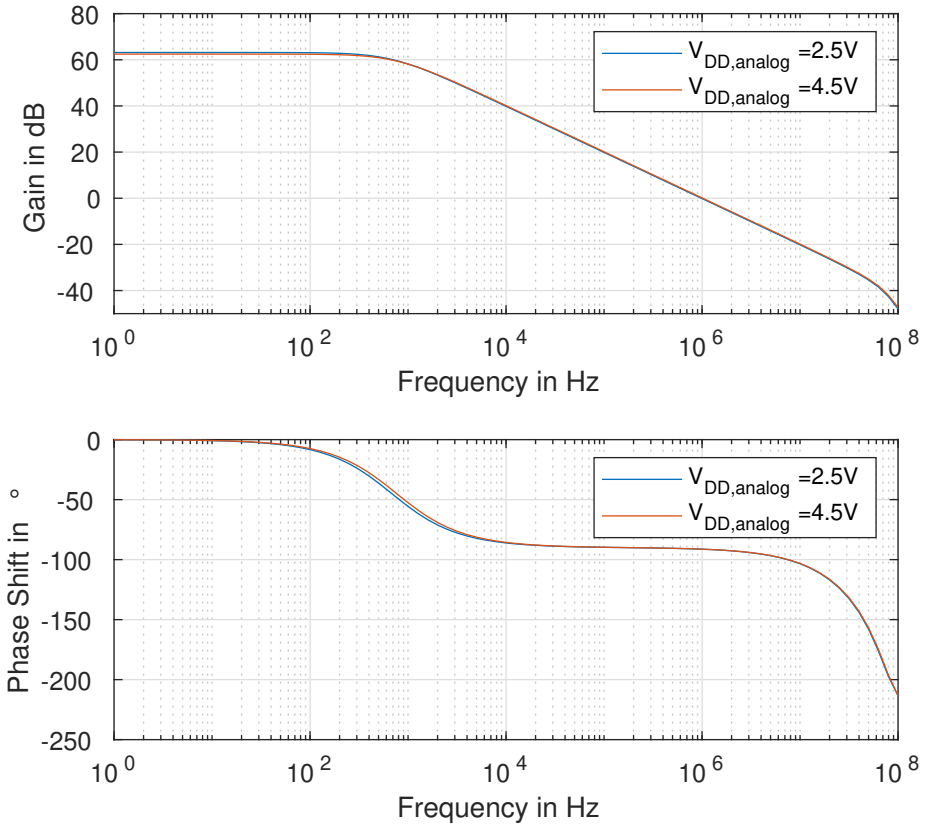

Fig. 5.3: Folded Cascode OTA - Bode Plot. The open loop bode plot of the implemented error amplifier simulated over the supply voltage corners for a 3 pF load capacitor.

must be placed on the unity gain frequency of the output voltage regulator. The value of C_{ff2} is determined by sweeping the capacitor and measuring the phase margin with a load resistor R_{load} of 1 kΩ in parallel connection to a load capacitor C_{load} of 100 nF. Since the capacitor is only switched off when the input voltage regulator is active, the design of the switching logic is discussed later in section 5.4.

5.2.4 Miller Compensation of the Pass Device

To guarantee a stable behavior of the closed loop output voltage regulator, it is necessary to introduce also another pole compensation method. By introducing a resistor R_c and a capacitor C_c between the output node of the amplifier and the output pin of the voltage regulator, a zero is introduced. C_c is designed to be as small as possible. A large capacitance on the output node of the error amplifier decreases the unity gain frequency and therefore the control speed. As can be seen in equation 4.19, the value of R_c must be greater than $\frac{1}{g_{m,PMOS}}$ to shift the zero to the left half plane and to the desired frequency. The aim is, to locate the zero near the unity gain frequency of the closed loop transfer function of the output voltage regulator. A nested loop sweep for C_c and R_c was performed

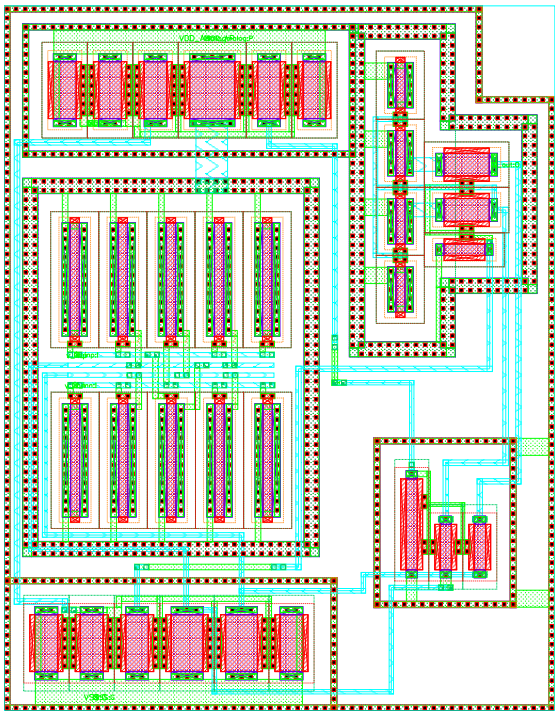

Fig. 5.4: Folded Cascode OTA - Layout ($31\,\mu m \times 24\,\mu m$).

in simulation to find the best fitting values which fulfill the before described requirements.

5.3 Input Voltage Regulator Design

The input voltage regulator is designed similar to the output voltage regulator. The design process is related to section 4.4.2. Since the input voltage limits of V_{in} are also adjustable in 100 mV steps, the ratio of the input voltage divider, consisting of R_1 to R_2, is also set to $\frac{9}{1}$. The total resistance should not be too small to prevent a high quiescent current. Therefore, the output voltage of the adjustable input reference source is between 250 mV and 440 mV, also adjustable in 10 mV steps. Also in this signal path, a switch is implemented which prevents a current consumption via both resistors when a supply voltage is connected to the input pin and the enable signal is logical low. To be able to use the same type of decoder as for the input voltage reference source and nearly the same voltage divider structure, the range of the output voltage is modified from 130 mV to 440 mV. The values of the implemented resistors are evaluated by equations 5.3 and 5.4. It should be noted, that a proper operation of the Power Source can only be guaranteed for input voltage limits equal to or greater than 2.5 V.

As for the output voltage error amplifier, the implemented error amplifier for the input voltage control loop is a folded cascode OTA with a PMOS input pair. In that case, the load of the OTA is only the gate capacitance of the decoupling NMOS device. This NMOS transistor is designed to ensure operation in saturation when the input voltage regulator is active. In this design approach, the dimensions are at the minimum process limit.

Therefore, this capacitance is far smaller than the one of the pass device which results in a faster amplifier configuration with the same implementation out of section 5.2.2. To decrease the unity gain frequency and increase the phase margin, the bias current of the amplifier is reduced and an additional load capacitor is added to the output node. This capacitor is varied until the phase margin of the input voltage control loop is at a maximum. It must be considered that the dominant pole of the input voltage control loop should be located between the pass device and the error amplifier of the output voltage regulator. Therefore, the load capacitor should not be too large to ensure that the dominant pole of the input voltage error amplifier is above the dominant pole frequency of the output voltage error amplifier. The unity gain frequency of this configuration is designed, as discussed in section 4.4.2, to be above the unity gain frequency of the error amplifier of the output voltage regulator. This has the advantage that the non-dominant pole is not relevant for the entire transfer function.

The feed-forward capacitor is determined with the same method as discussed in section 5.2.3.

5.4 Switchable Feed-Forward Capacitor

After designing the input voltage regulator, the switchable feed-forward capacitor can be implemented. This procedure is referred to section 4.8. As mentioned, the trigger signal to disconnect the capacitor of the reference node is the output voltage of the input error amplifier. This is realized with a time continuous comparator which compares the two voltage levels and provides an inverted and non-inverted output. The potential of the reference signal of the comparator is defined via a voltage divider. There, the buffered reference voltage is divided to a voltage level which is above the lowest output potential of the error amplifier.

5.4.1 Time Continuous Comparator Design

The implemented comparator is presented in figure 5.5. Basically, it consists of a differential stage and two inverters which provide a high gain at the output. To prevent instability of the circuit near the threshold voltage, a hysteresis is introduced by positive feedback. This is realized by an additional current path into the differential pair by opening an NMOS transistor via the inverter structure. The hysteresis is shown in figure 5.6. V_{up} represents the sweep from 300 mV to 500 mV and V_{down} the inverse one. The simulation of the curve is made with nominal process models and a threshold voltage of the comparator of 400 mV. As recognizable, the hysteresis is symmetric on the positive and negative sweep. The steep signal edge when the output level switches indicates a high open loop gain of the circuit. The layout of the comparator is presented in figure 5.7. The input pair and the current mirrors are surrounded by dummy-transistors to ensure a better matching of the two devices. The total chip are of this circuit is $26\,\mu\text{m} \times 20\,\mu\text{m} = 520\,\mu\text{m}^2$.

5.4.2 Voltage Buffer Design

To prevent loading of the external reference source and the adjustable output reference source, a voltage buffer is introduced. Two buffer circuits are implemented in the whole

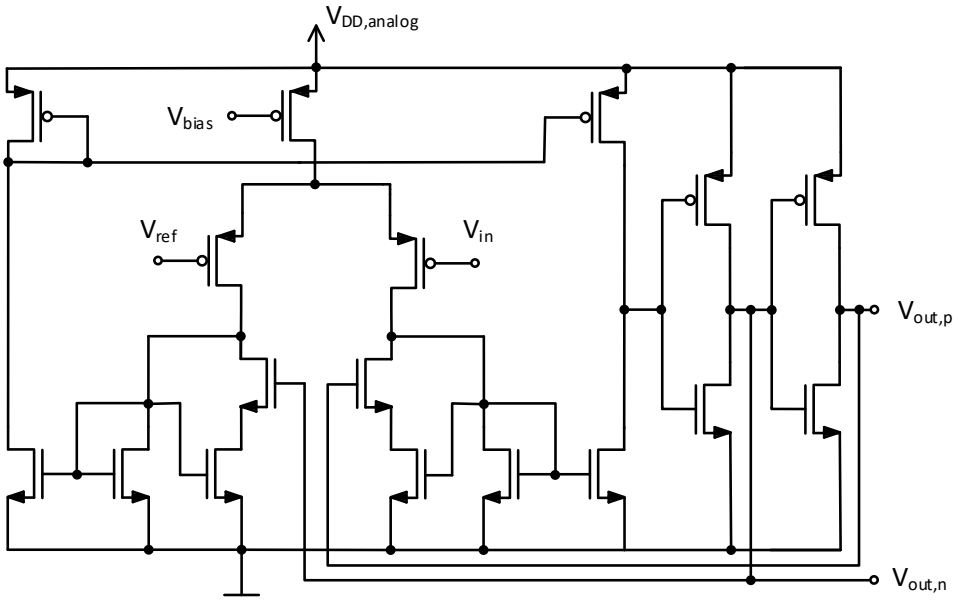

Fig. 5.5: Time Continuous Comparator. Schematic of the comparator with a hysteresis and positive feedback.

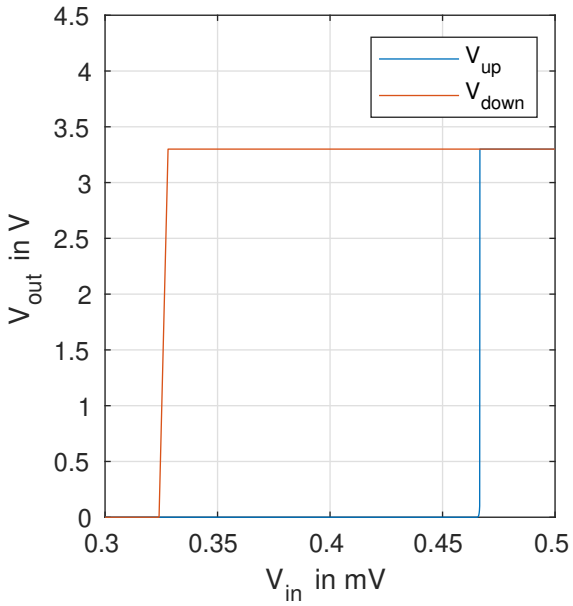

Fig. 5.6: Time Continuous Comparator - Hysteresis. Hysteresis of the time continuous comparator at a reference voltage of 400 mV and a supply voltage of 3.3 V.

Power Source. To develop a circuit for both applications, the specifications of the input- and output voltage need to be investigated first. If the circuit is implemented to precharge

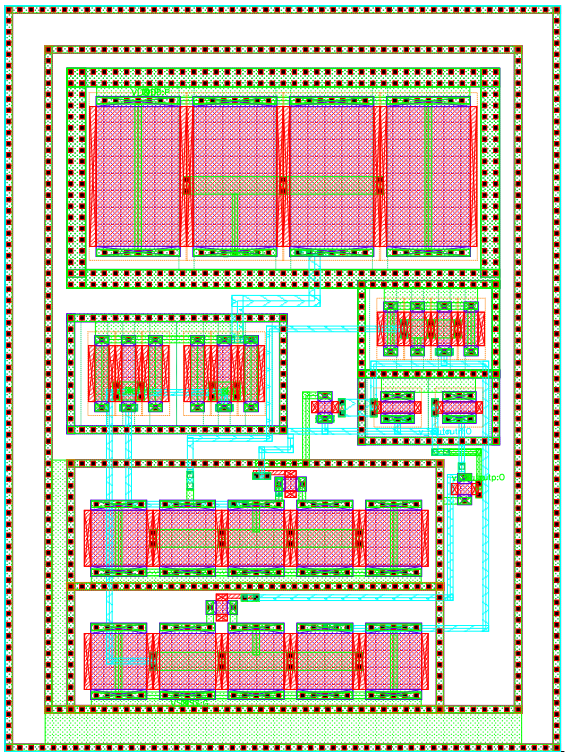

Fig. 5.7: Time Continuous Comparator - Layout ($26\,\mu$m $\times$ $20\,\mu$m).

the feed-forward capacitor of the LDO, the input potential of the buffer varies between the output voltages of the adjustable output reference source. Thus, a folded cascode OTA with a PMOS transistor input pair is chosen to fulfill the requirements of the low input voltage potential. If the buffer is used with that configuration as reference voltage buffer, the gain of the circuit is significantly reduced due to the resistive load. Therefore, a low ohmic voltage output class A stage is implemented in the buffer. This stage follows directly to the cascode stage of the amplifier and is compensated by a series connection of a capacitor and a resistor.

5.5 Top-Level Schematic and Layout of the Power Source

Some basic circuits of the Power Source are not described in more detail. These blocks are the 5 Bit decoder, a level shift circuit and a bias block.

The decoder converts a 5 Bit input signal into a thermometer code with 32 output signals with standard NAND and NOR gates. Following the decoder, 32 level shift circuits are implemented to shift the logical high signal from $V_{DD,digital}$ to $V_{DD,analog}$. Due to the used NMOS transistor in the adjustable reference sources, the inverting output of the level shift circuit is used as output signal.

As mentioned before, a level shift circuit shifts a logic level of a signal to a higher one. These circuits are usually implemented to shift the level of a digital signal to the analog supply voltage, which is usually above the digital one. Digital circuits are often imple-

mented with thin oxide minimum sized transistors, which are supplied with a lower supply voltage then analog circuit blocks, to save chip area and to reduce the power losses.

To gain robustness of bias current sensitive circuits, such as amplifiers or comparators, a bias current is distributed instead of voltages. This is done with so called bias blocks. This circuit basically consists of current mirrors, which provide the reference current to the other circuit blocks. To provide variant currents, NMOS transistors with different $\frac{W}{L}$-ratios are used in the bias block.

The top-level schematic of the Power Source is presented in figure 5.8. All implemented circuit blocks and signals are shown, except the enable/disable signal path and the reference currents, provided by the bias blocks. To prevent a charged load capacitor from discharging via the output voltage divider, an NMOS transistor is closed when the enable signal is logical low. This transistor is implemented between R_4 and ground. An equal transistor is also used under the input voltage divider between R_2 and ground to minimize the quiescent current of the Power Source when the enable signal is logical low.

In figure 5.9, the layout of the Power Source is shown. In comparison to the full size of the circuit, the pass device consumes only a small chip area. Both adjustable reference voltage sources require about half of the overall chip area. A large part of the total chip area is used by the high ohmic poly resistors. They are necessary to that extend to minimize the quiescent current in the circuit. In total, the consumed chip area of the NFC Power Source in this 130 nm process is $255\,\mu\text{m} \times 194\,\mu\text{m} = 0.049\,\text{mm}^2$. The floorplan of the layout is presented in figure 5.10.

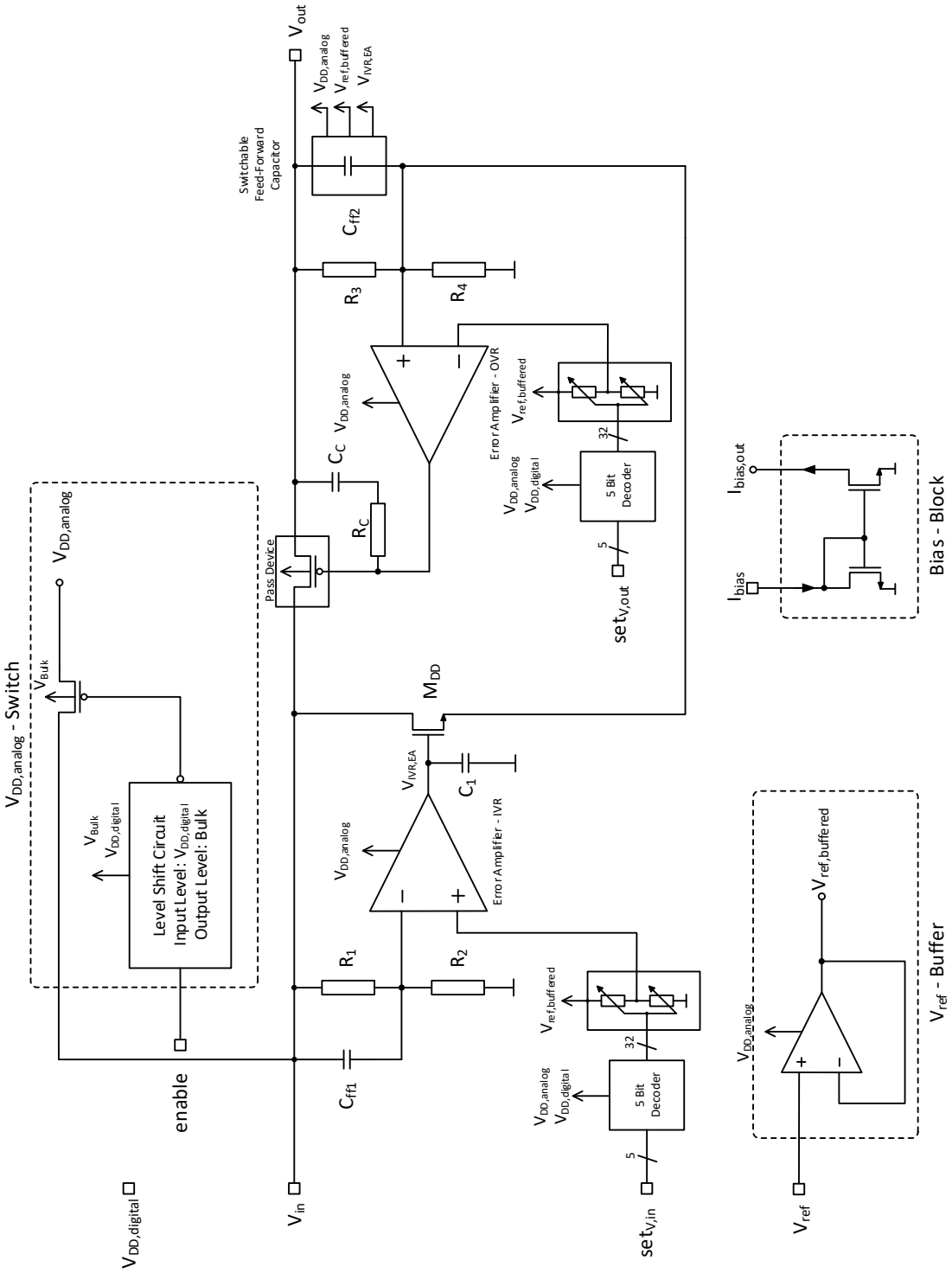

Fig. 5.8: Power Source - Top-Level Schematic. The circuit blocks inside the Power Source are presented in this figure. The enable- and bias current connections are not visible.

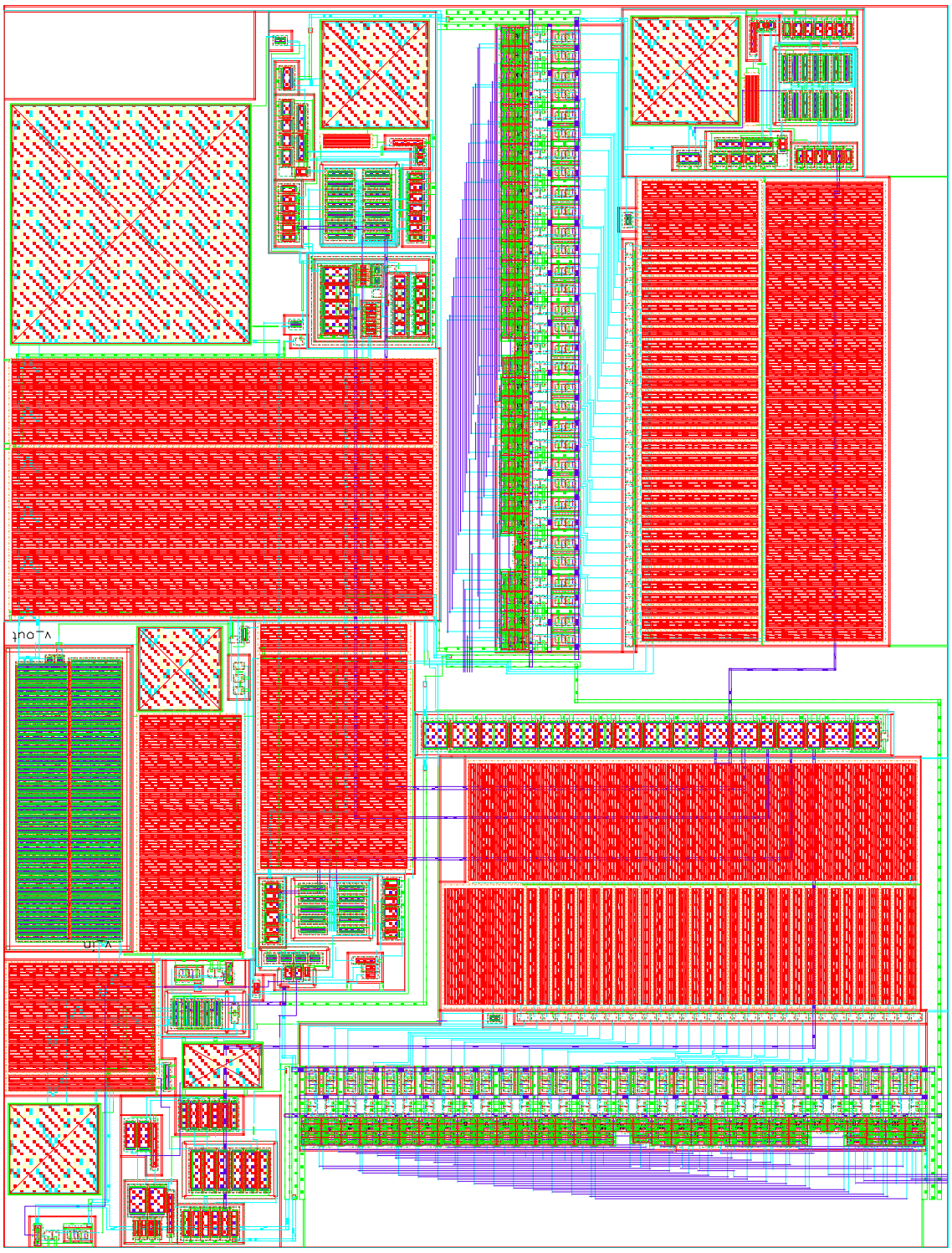

Fig. 5.9: Power Source - Layout ($255\,\mu\text{m} \times 194\,\mu\text{m}$).

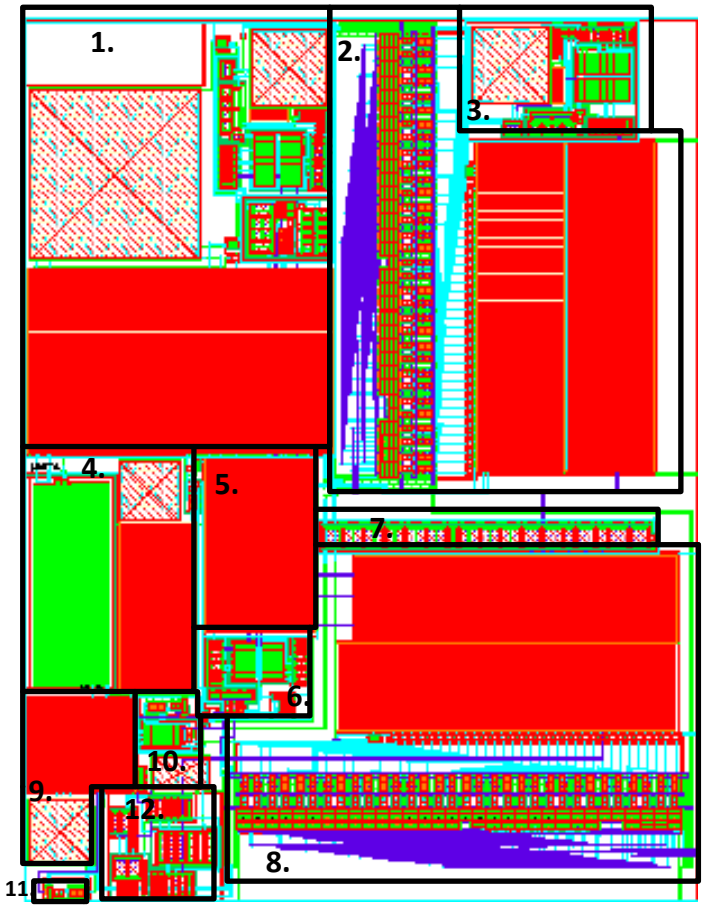

Fig. 5.10: Power Source - Floorplan of the Layout. 1. Switchable Feed-forward Capacitor; 2. Adjustable Output Reference Source; 3. Reference Voltage Buffer; 4. Pass Device with Compensation; 5. Output Voltage Divider; 6. Error Amplifier - OVR; 7. Bias Block; 8. Adjustable Input Reference Source; 9. Input Voltage Divider with Feed-forward Capacitor; 10. $V_{DD,Analog}$ - Switch and Load Capacitor for the IVR; 11. Level Shift Circuit for the Enable Signal; 12. Error Amplifier - IVR

Chapter 6

Verification and Simulation

The verification of the implemented circuit is made in this chapter. This is done with transient- and AC simulations for each control loop based on a suitable test bench. To ensure proper operation of the Power Source in an application, the limits of the load capacitors and resistors are evaluated in this chapter. Process and mismatch variations are considered in Monte Carlo simulations. The circuit behavior at different temperature levels is investigated with corner simulations.

6.1 Test Bench

A test bench is needed to verify the transient- and the AC behavior of the Power Source. The test bench provides a periphery which is identical to the application of the circuit. As discussed in chapter 1, a parallel connection of a resistor R_{load} and a capacitor C_{load} represents the load. The analog front-end is modeled by a voltage source V_{supply} and an internal source resistance R_{source}. All external signals from the digital block and the analog front-end are provided by ideal voltage- and current sources. To simulate the transient short circuit behavior of the Power Source, a large and not charged capacitor C_{sim} can be connected in parallel to the load network via a switch. Besides voltage- and current sources, also the resistors, capacitors and switches of the external periphery are ideally modeled components. The test bench of the Power Source is presented in figure 6.1. All simulations in this chapter except the Monte Carlo and corner simulations in section 6.4 are executed with nominal process models .

6.2 AC-Analysis of the Power Source

The AC simulations of the Power Source are used to describe the frequency behavior of the circuit. The main information out of this analysis is the stability of the circuit and the load characteristics, where a stable operation can be guaranteed. It must be considered, that this type of simulation is made in one DC operating point of the circuit. Therefore, more AC simulations are necessary to describe the behavior of the Power Source for all different types of the output voltages and input voltage limits.

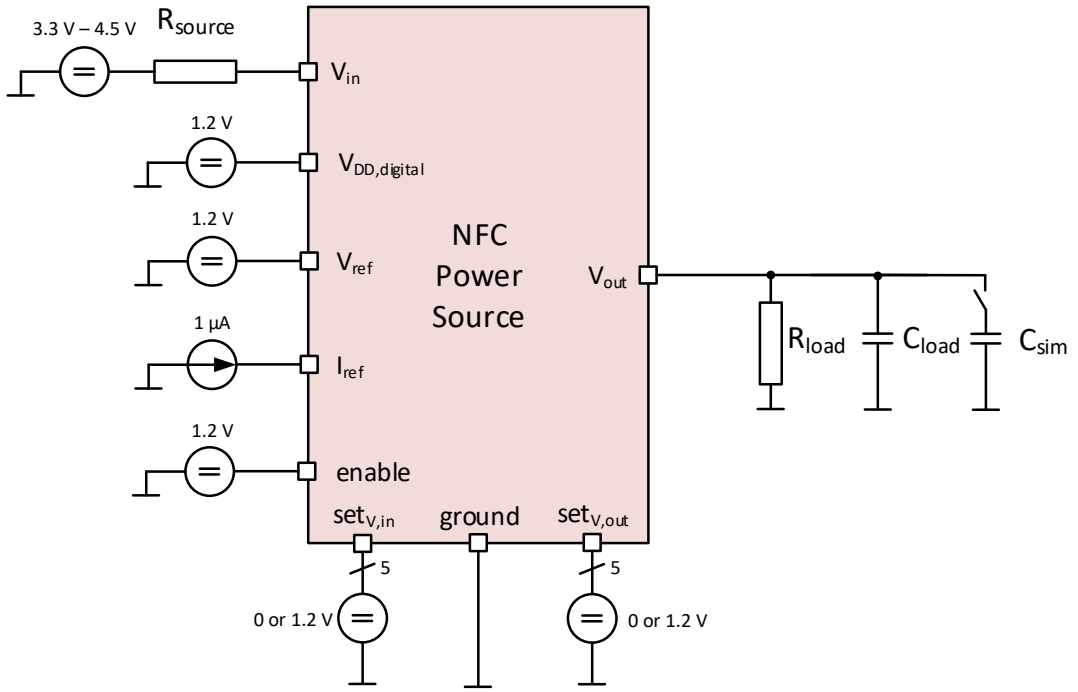

Fig. 6.1: Power Source - Test Bench. The external periphery to verify the Power Source.

6.2.1 Output Voltage Control Loop

To analyze the output voltage control loop it must be ensured that the input voltage regulator is not active and the LDO works in the regulation region. As discussed in section 4.1, this is fulfilled when equation 4.3 is valid. The dropout voltage of the output voltage regulator is load current dependent. Therefore, a generalized value for this voltage cannot be given. In figure 6.2, the behavior regarding the input potential of the LDO of the Power Source is presented. The dropout voltage and the different regions of operation of the implemented circuit for various load currents and an output voltage of 1.1 V are shown in figure 6.2. The dropout voltage is the difference between the black reference line, which represents a 0 V dropout voltage, and the input potential where the LDO can provide the desired output voltage. For small load currents, the dropout voltage is a few millivolts and for a load current of 100 mA nearly 600 mV. As discussed in [5], an LDO can be operated in three different regions. The regulation region is the desired one. There, the input voltage is high enough to ensure that the LDO can provide the desired output voltage. The region, where the output voltage cannot be reached is called dropout region. For a higher load current, also the dropout voltage increases due to the larger voltage drop across the pass device. The last remaining region of operation is the off region where the pass device is closed due to the small gate source voltage. To determine this chart, the input voltage regulator must be deactivated by disconnecting the signal path between the decoupling device and the output voltage regulator. The supply voltage of the Power Source $V_{DD,analog}$ is fixed to an ideal voltage source with 3.3 V to provide stable operation of all analog blocks. The dropout voltage is an essential parameter of the Power Source

and must be considered when the circuit is implemented in the application.

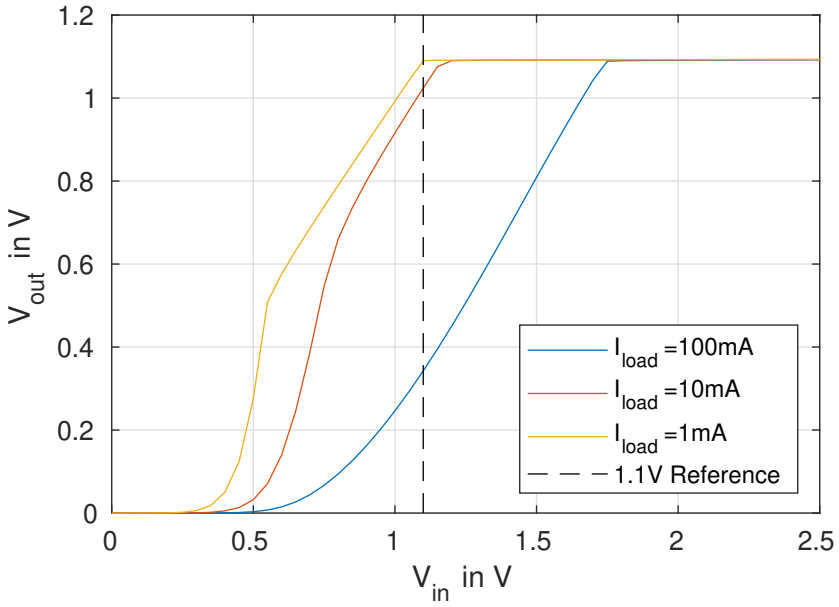

Fig. 6.2: Output Voltage Regulator - Dropout Voltage. The load current dependent dropout voltage of the Power Source with deactivated input voltage regulator and a fixed $V_{DD,analog}$ potential at 3.3 V. V_{out} is defined by the adjustable output reference source to 1.1 V.

If the before discussed assumptions are valid and the output voltage regulator of the Power Source is in the regulation region, the bode plot of this control loop can be determined. As discussed in section 4.1.2, the AC behavior of an LDO was determined by opening the feedback path between the error amplifier and the pass device. The test bench switch between the output pin and C_{sim} is opened and a 100 nF load capacitor is connected. To determine the AC behavior for different load currents, R_{load} is varied between 1 kΩ and 10 kΩ to simulate two different levels of loading of the Power Source. The circuit is supplied with 3.3 V and R_{source} is set to 109 Ω, referring equation 2.2. To ensure that the input voltage regulator is not active during this simulation, the voltage limit is defined to 2.5 V. V_{out} is set to 1.1 V. In figure 6.3, the simulation results are presented. By increasing the load current, the open loop gain of this control loop is enhanced. A higher current through the pass device reduces the drain-source resistance of it which normally results in a decrease of the gain. Besides the resistance, the transconductance g_m is increased by the larger current. Also the error amplifier changes its parameters by changing the load resistor. For low output currents, the output voltage of the error amplifier is very high which forces the upper cascode transistor into linear region. Thus, the gain of the error amplifier is significantly reduced due to a low output resistance. Due to the parameter changes in the pass device and the error amplifier, the gain of the output voltage regulator is reduced when a large load resistor is connected to the Power Source. By investigating the bode plot, it is recognizable that the poles of the system also change their positions. Due to the decreasing transconductance and the output resistance of the error amplifier,

the dominant pole is shifted to a higher frequency. The non-dominant pole on the output node of the Power Source is pushed down to a lower position due to the increasing load resistance. Thus, the dominant- and the non dominant pole approach with decreasing load current. Therefore, the stability of the output voltage regulator depends also on the provided load current. This behavior is opposite to that of a conventional LDO structure without miller compensation which typically increases the stability with a decreasing load current [15]. To guarantee a stable operation, a maximum output resistance needs to be defined which is investigated later in this chapter.

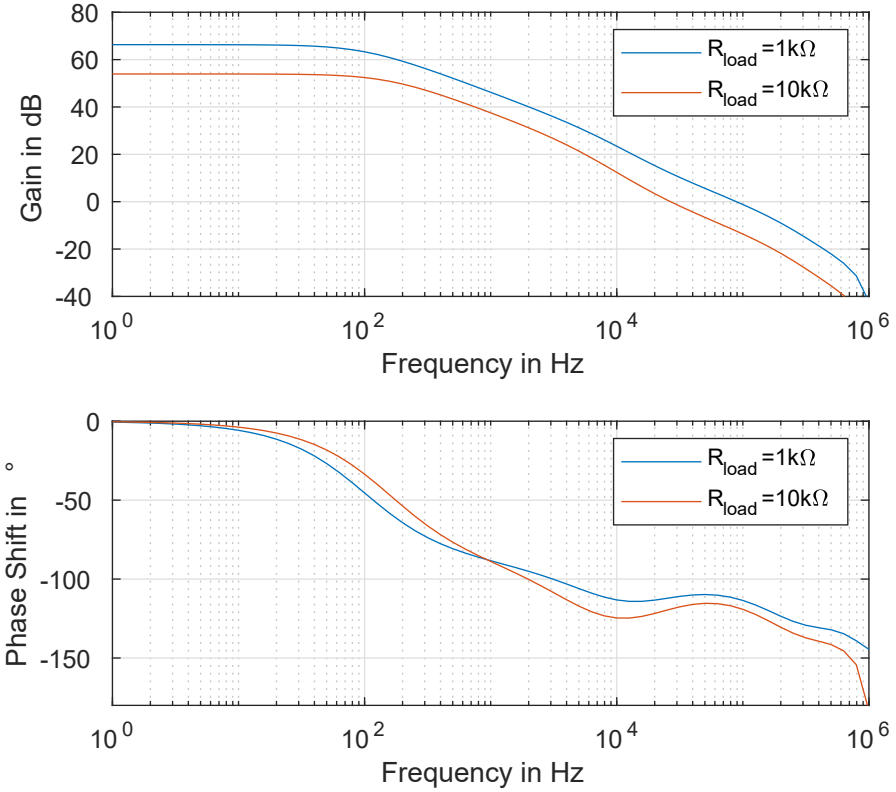

Fig. 6.3: Output Voltage Regulator - Bode Plot for Different Load Currents. The frequency behavior of the output voltage regulator simulated for different load currents and a 100 nF capacitance at the output. The supply voltage level is set to 3.3 V and the output potential to 1.1 V.

As it is also possible to supply the Power Source with different voltages, the AC behavior of the output voltage regulator for different supply voltages needs to be investigated. The simulation results of the AC behavior for a supply voltage of 3.3 V and 4.5 V are shown in figure 6.4. During this simulation, the resistance of the load resistor is set to 1 kΩ and the load capacitor to 100 nF. The value for the internal source resistance is defined with 109 Ω for both supply voltages due to a better comparability of the bode plots. As in the previous simulation, the input voltage limit is defined to 2.5 V.

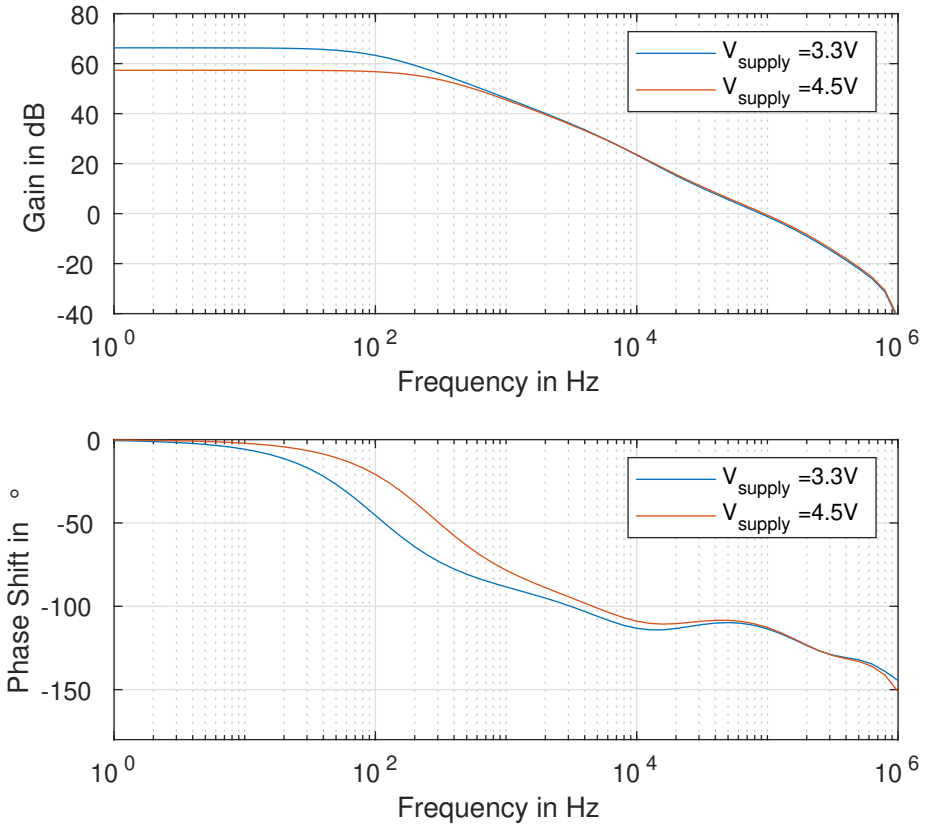

Fig. 6.4: Output Voltage Regulator - Bode Plot for Different Supply Voltages. The frequency behavior of the output voltage regulator simulated for different supply voltages and a fixed load of 100 nF and 1k Ω at the output. The voltage on the output pin is defined with 1.1 V.

By increasing the supply voltage of the Power Source, the open loop gain in the output voltage control loop decreases and the dominant pole is shifted to a higher frequency. Since the transconductance and the drain-source resistance of the pass device shows only a slight increase, the parameters of the error amplifier must change. The output resistance of the folded cascode circuit decreases when the input voltage of the Power Source increases. This occurs due to the higher output voltage of the error amplifier. Therefore, also the open loop gain of the control loop increases when the supply voltage is reduced. The dominant pole is shifted to a higher frequency because of the before discussed decrease of the output resistance.

6.2.2 Input Voltage Control Loop

To evaluate the AC behavior of the input voltage control loop, it is necessary to bring the Power Source in a DC operating point, where this control loop is active. This is done by connecting a correct dimensioned load resistor to the output pin. This resistance

multiplied with the maximum load current needs to be smaller than the output voltage of the low-dropout voltage regulator in order to keep it deactivated. The Power Source behaves like a current source when this is fulfilled and consumes a constant load current from the supply voltage source which is defined by:

$$I_{max} = \frac{V_{supply} - V_{in,limit}}{R_{source}} = I_{load} + I_{quiescent} \tag{6.1}$$

Where $I_{quiescent}$ is the consumed quiescent current of the Power Source and $V_{in,limit}$ the defined voltage limit where the input voltage control loop is activated. The current I_{load} is the constant current on the output pin of the circuit. If the load current is below the limit defined in equation 6.1 due to a large load resistor or a charged load capacitor, the input voltage regulator is deactivated and the output voltage control loop gets active.

The bode plots of the input voltage control loop are determined the same way as discussed before in section 6.2.1. First, the frequency behavior of the Power Source for different load currents is investigated. They are achieved by defining several input voltage limits of the input voltage control loop. In the simulation results presented in figure 6.5, two input voltage limits of 2.5 V and 3.0 V are defined. The supply voltage source provides a 3.3 V DC voltage with a source resistance of 109 Ω. On the output pin of the Power Source, a 50 Ω and 100 nF load is connected in parallel to ground. For the sake of completeness, it should be noted that the output voltage of the LDO is defined with 2.5 V. With both input potential limits, a maximum current of respective 7.4 mA and 2.8 mA is provided by the supply voltage source which can be calculated with equation 6.1. The gain of the input voltage control loop is slightly increased by a higher load current. Besides the gain, the frequency of the dominant pole decreases when the input voltage limit is reduced. A lower input voltage limit leads to more current which decreases the potential on the output pin of the error amplifier in the low-dropout regulator in order to increase the gate source voltage of the pass device. Both occurrences are indicated by the increasing output resistance of the error amplifier in the output voltage control path. When only a small load current passes the pass device, the amplifier needs to provide a higher output potential which leads to an unsymmetrical operating point in the output stage. As the small signal output resistance of amplifiers is determined by a parallel connection of the two branches between the output node and ground or the supply potential, this parameter is determined by the smallest one. A larger current leads also to an increase of the transconductance of the pass device which also increases the open loop gain.

To evaluate the behavior of the circuit to changes in the load resistance, nearly the same test bench setup is used as before. The input voltage limit is defined at 3.0 V for a supply potentials of 3.3 V. This simulation is evaluated for a 50 Ω and 500 Ω load in parallel to a 100 nF capacitor. Both bode plots are presented in figure 6.6. As recognizable, the DC open loop gain is nearly unaffected due to the changing load resistors. However, by increasing the resistance on the output pin, the phase margin is strongly affected. The unity gain frequency and the phase margin of the control loop remain unaffected. By increasing the load resistance the dominant pole is pushed to a lower frequency. Besides this, the non-dominant pole is not affected by this increase and remains nearly constant at the same position. Besides the impact on the pole frequencies, also a zero is recognizable

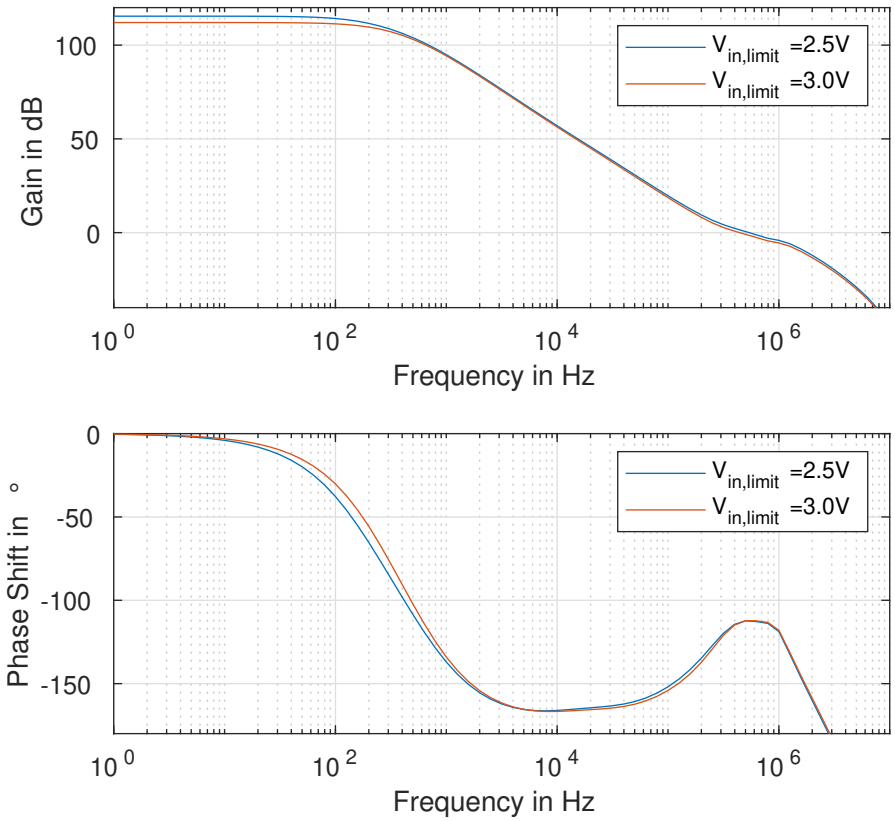

Fig. 6.5: Input Voltage Regulator - Bode Plot for Different Load Currents. The frequency behavior of the input voltage regulator simulated for different load currents, defined by setting the input voltage limit of the regulator to 2.5 V and 3.0 V. A higher load current pushes the dominant pole frequency to a lower one and increases the DC gain.

introduced by increasing the resistance of the load resistor. This zero is defined in equation 4.13 and gets visible due to the large load resistor. Besides the zero, also the pole from equation 4.12 is pushed to a higher position because of the increase of the load resistance. Therefore, a significant difference in the phase between both frequencies is visible.

As discussed in chapter 4, the impact of the load capacitor on the input voltage regulator is significantly small and can be neglected. By decreasing this capacitor, the pole zero pair is shifted to a higher frequency but still not affects the phase margin or unity gain frequency. Thus, no further investigations of it are necessary.

6.2.3 Load Characterization

The Power Source is not able to guarantee proper operation for all types of loads. Therefore, the minimum and maximum load resistors and capacitors needs to be defined to

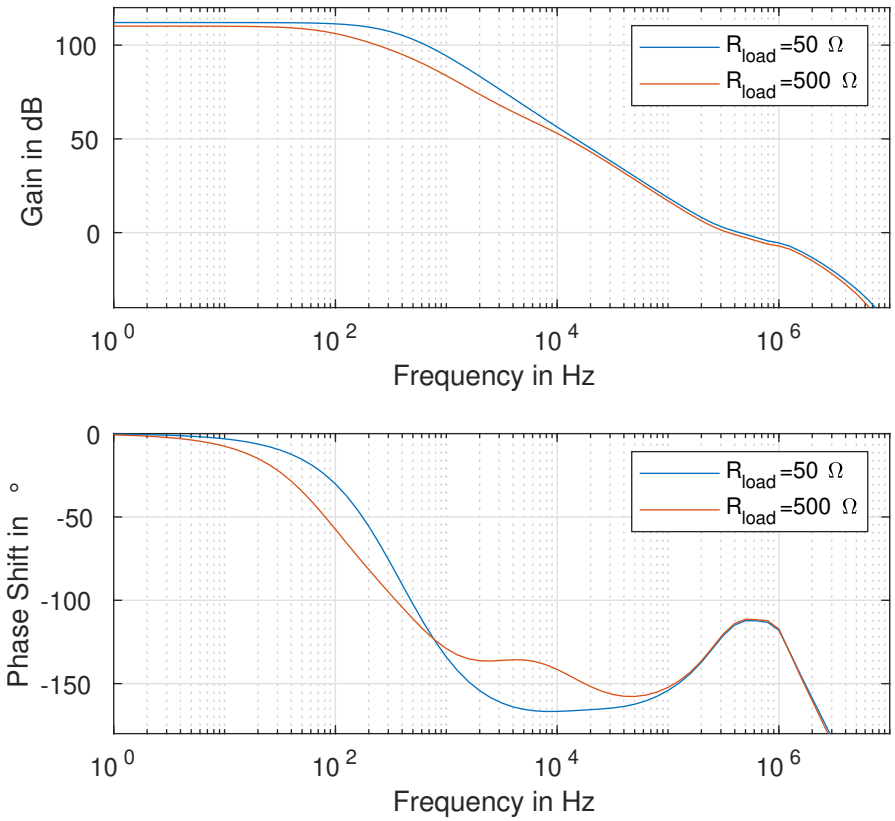

Fig. 6.6: Input Voltage Regulator - Bode Plot for Different Load Resistors. The frequency behavior of the output voltage regulator simulated for different load resistors and a fixed load capacitor of 100 nF. By increasing the resistor, the dominant pole frequency is pushed to a lower one and the non-dominant one increases due to the decreasing output resistance of the input error amplifier which also reduces the gain.

ensure that the phase margin is always larger than 45 ° which is the minimum criterium for stability. All the following simulations are evaluated with ideally modeled loads and nominal process models for the Power Source at room temperature. The test bench is build up equivalent to the set up in section 6.2.1. AC simulations are done with different load types and the load size as a function of the phase margin is plotted as result. The results are evaluated at a DC operating point, where the output voltage regulator is active and the output voltage is controlled by the low-dropout regulator. It is necessary to use the correct calculated internal source resistance for the respective supply voltages.

First, the AC behavior for different load capacitors is investigated. Only a load capacitor is connected to the output pin of the Power Source for these simulations. The phase margin is determined for the upper- and lower voltage corner of the Power Source. For a supply voltage of 3.3 V, the output voltage is defined with 1.1 V and the input voltage

limit is set to 2.5 V. The other supply voltage corner is simulated for an output voltage of 4.2 V and a lower input voltage limit of 2.5 V. By increasing the output voltage of the Power Source, the minimum required load capacitor to achieve stability increases. The simulation result is shown in figure 6.7. Based on this result, the minimum load capacitor to achieve a phase margin of at least 45 ° is 160 pF. By increasing the capacitance at the output node, the non-dominant pole frequency is pushed to lower frequencies. If this capacitance is large enough, the non-dominant pole frequency is below the frequency of the pole between the pass device and the error amplifier of the output voltage regulator and gets dominant. This process is visible in the simulation result as peak in the phase margin. By reaching a certain point of capacitance on the output node, the phase margin remains constant at nearly 90 ° due to the low unity gain frequency of the Power Source. If the load capacitor increases, the unity gain frequency of the output voltage regulator is reduced because of the shifted frequency pole.

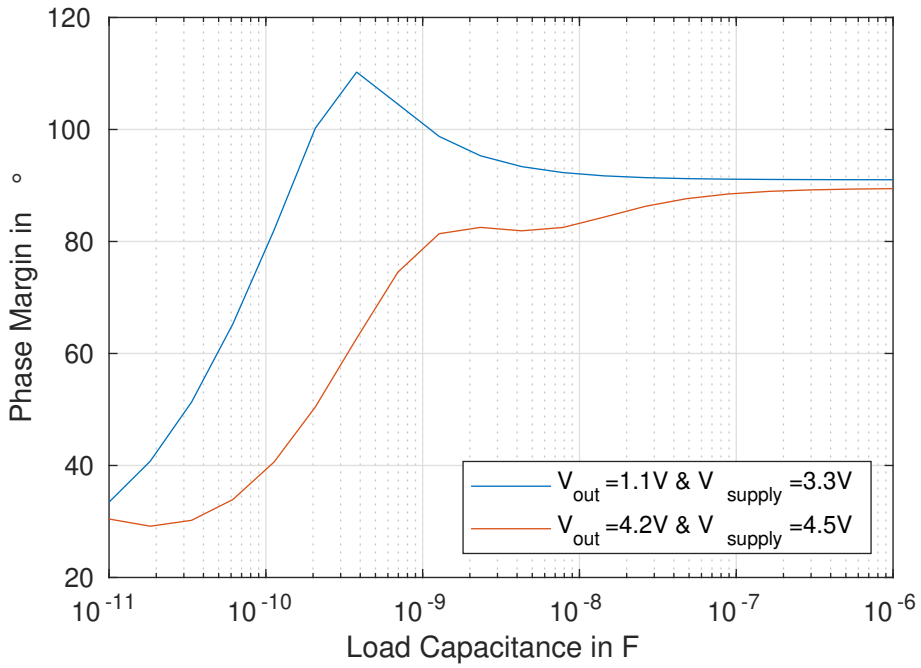

Fig. 6.7: Load Characterization - Phase Margin as Function of the Load Capacitance. By increasing the output voltage of the Power Source, the minimum required load capacitance for a stable operation increases.

The next characterization is done by varying the load resistor. In that case, no load capacitor is connected to the output pin of the Power Source. As discussed before in this chapter, the stability decreases with the load current. Therefore, the phase margin is reduced by increasing the load resistor. The phase margin is at the critical point at 45 ° if the load current is below 3.8 μA. This point occurs with an output voltage of 1.1 V at a load resistance of 290 kΩ if the circuit is supplied with 3.3 V and is also proved in other operating points.

It is not possible to adopt this minimum load characterizations if both load types are com-

bined to a parallel network consisting of a resistor and a capacitor. Therefore, additional simulations are necessary to determine the circuit behavior for combined loads. In the first analysis, the load resistor is fixed to 1 kΩ and the capacitor in parallel to the resistor is varied. In figure 6.8, the simulation results for two operating points are presented. The first one is evaluated with an output voltage of 1.1 V and a supply voltage of 3.3 V. In this operating point, the smallest load current passes the Power Source due to the small output voltage. If the load current increases by defining a higher output potential of 3.5 V, the phase margin also increases. Therefore, the minimum capacitance of the load capacitor is defined by investigating the phase margin as function of the load capacitance for the smallest possible load current. In the first section of the curve in figure 6.8, the non-dominant pole- and the unity gain frequency of the Power Source decreases with increasing load capacitance. Therefore, also the phase margin of the system is reduced. On a certain point, the non-dominant pole is at the frequency of the introduced zeros. At this point, the phase margin increases until the load capacitor is too large and the non-dominant pole gets pushed below the zeros. There, the phase margin strongly decreases and the Power Source gets unstable. With a fixed load resistor of 1 kΩ, the circuit is stable for load capacitors $< 150\,\text{pF}$ and $20\,\text{nF} < C_{\text{load}} < 500\,\text{nF}$.

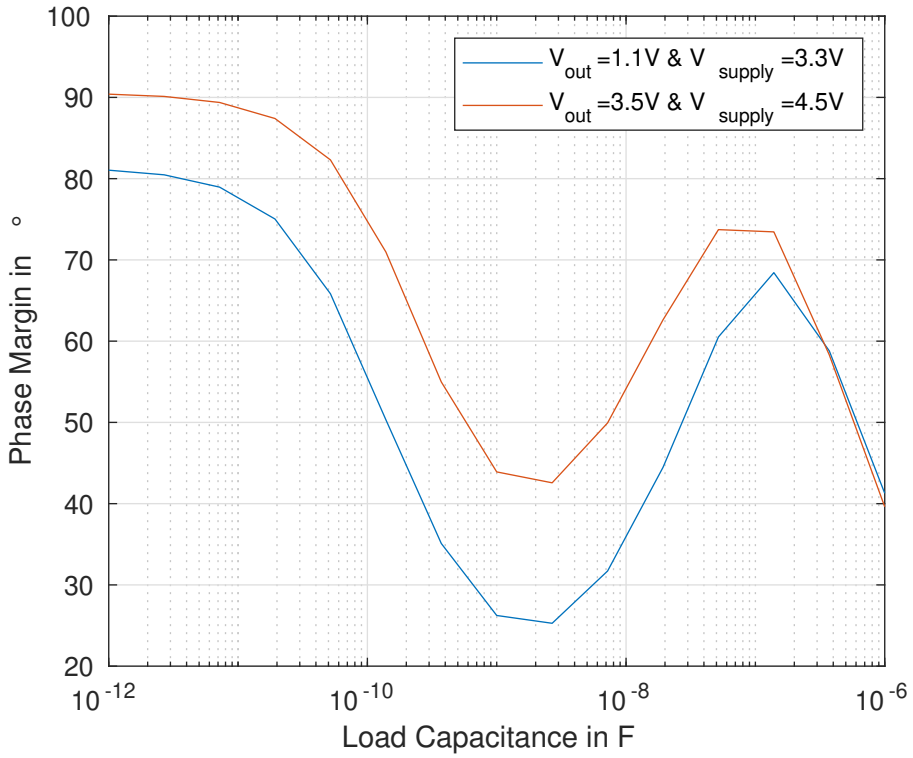

Fig. 6.8: Load Characterization - Phase Margin as Function of the Load Capacitance with a Fixed Load Resistor. The minimum load capacitance is defined with the lower curve which is simulated with the smallest load current.

In the last section of the load characterization, the load current dependency of the phase

margin with a fixed load capacitor is evaluated. During this evaluation, the maximum allowed load current in the DC operating point where the capacitor is fully charged must not exceed the limit to activate the input voltage regulator. Therefore, the maximum load current is defined by:

$$I_{max} - I_{quiescent} > I_{load} \tag{6.2}$$

This equation can be rewritten as:

$$\frac{V_{supply} - V_{in,limit}}{R_{source}} - I_{quiescent} > \frac{V_{out}}{R_{load}} \tag{6.3}$$

If equation 6.3 is fulfilled when the load capacitor is fully charged, the output voltage regulator of the Power Source is active and controls the output potential. By increasing the load current above this limit, the input voltage regulator is activated. The quiescent current is discussed in chapter 7. As expected, the phase margin is reduced if the resistance of the load resistor decreases. For a load capacitor of 100 nF, the phase margin is above 45 ° for all load currents.

6.3 Transient Simulations

Transient simulations of the Power Source are necessary to observe the short circuit behavior of it. If an uncharged high capacity capacitor is connected to the output pin during operation, it must be ensured that the input voltage drop of the Power Source is small enough to prevent the analog front-end from an under-voltage brownout. Another important information out of this analysis is the settling behavior of the Power Source.

6.3.1 Short Circuit Behavior

For the transient analysis of the Power Source, a load capacitor with 100 nF and a load resistor with 1 kΩ is connected in parallel to the output as shown in the test bench in figure 6.1. The short circuit is simulated by connecting an empty 100 μF capacitor C_{sim} in parallel to the output pin during operation. The in figure 6.9 presented simulation results are simulated for two different operating points. The red curves are evaluated with an output voltage of 2.0 V and an input voltage limit of 2.5 V. For the blue curves, an output voltage of 3.5 V is used with a lower input voltage limit of 3.7 V. The Power Source is supplied in both cases with 4.5 V via R_{source} with 203 Ω. In a), the short circuit control signal is shown. If this signal is logical high, C_{sim} is connected in parallel to the output pin and the ground potential which simulates a short circuit of the Power Source. The input voltages are determined by the defined limit, if the current from the supply source causes a too large voltage drop across R_{source} as visible in b). During the charging process of C_{load} and the short circuit, the input potential is determined by the input voltage control loop. In c), the output potential of the Power Source is shown which gets pulled down if the short circuit occurs. When the load current decreases below $I_{max} - I_{quiescent}$ due to the charged capacitor, the input potential rises until $V_{supply} - R_{source} \cdot I_{supply}$ is reached. The

in d) presented current represents the current through the pass device which consists of the load current and the quiescent current passing the output voltage divider. During the slope when the short circuit control signal changes between low and high, a recognizable settling behavior occurs. For the red curve, this process takes about 7 μs and for the blue one 20 μs due to the larger output potential. This point is critical for the Power Source. First of all, a short circuit occurs at the output pin. Thus, the input voltage regulator is activated and the switchable feed-forward capacitor is disconnected from the signal path. These procedures can not happen infinitely fast which leads to a visible settling behavior in the input voltage. Another important parameter for this behavior is the phase margin and unity gain frequency of the input voltage control loop which defines the speed and overshoot of the regulator and are limited. Therefore, the settling time and -amplitude of the input voltage depends on the parameters of the input voltage control loop but also on the provided electrical power on the output pin and decreases by reducing the load current or the output potential. The settling time of the output voltage is discussed in the following section.

6.3.2 Settling Behavior of the Output Voltage

The settling time of the output voltage regulator depends mainly on the size of the load capacitor and -resistor, the output voltage and the maximum allowed load current due to the input voltage regulator. If the load is defined by a resistor and a capacitor, the voltage on the output pin increases according to:

$$v_{out}(t) = R_{load} \cdot I_{load} \cdot \left(1 - e^{-\frac{t}{\tau}}\right) \tag{6.4}$$

With $\tau = R_{load} \cdot C_{load}$ and $I_{load} = I_{max} - I_{quiescent}$. Equation 6.4 is valid until $v_{out}(t)$ reaches the desired output potential of the LDO. Then the output voltage regulator is activated and controls $v_{out}(t)$. This happens due to the increasing potential between the output voltage divider during the charging process. The input voltage control loop fixes this potential to a constant value which is equal to the reference voltage of the error amplifier. If $v_{out}(t)$ increases, the decoupling device sources less current to keep this potential constant. If this voltage is larger than the reference potential of the error amplifier due to the charging process, the decoupling transistor and the pass device are closed which results in a decreasing load current. Therefore, the input voltage regulator is deactivated and the LDO takes over the output voltage regulation. If the output potential of the LDO is set higher than the product of $R_{load} \cdot I_{load}$, the regulator gets never active and the voltage on the output pin increases to $v_{out}(t \to \infty) = R_{load} \cdot I_{load}$. The small overshoot of the output voltage during the charging process in the red curve in c) in figure 6.9 occurs due to the small output voltage of the LDO compared to the product of $R_{load} \cdot I_{load}$ which results in a fast charging process. As the change between both control loops can not happen infinitely fast, the input voltage control loop overcharges the load capacitor. Since a load resistor is connected in parallel, the capacitor discharges until the output potential of the low-dropout voltage regulator is reached at the output pin. If no external load resistor is connected to the Power Source, the capacitor starts to discharge via the large resistance of the output voltage divider. Therefore, the discharge current is smaller which results in a longer period where the load capacitor is charged to a higher voltage than the desired

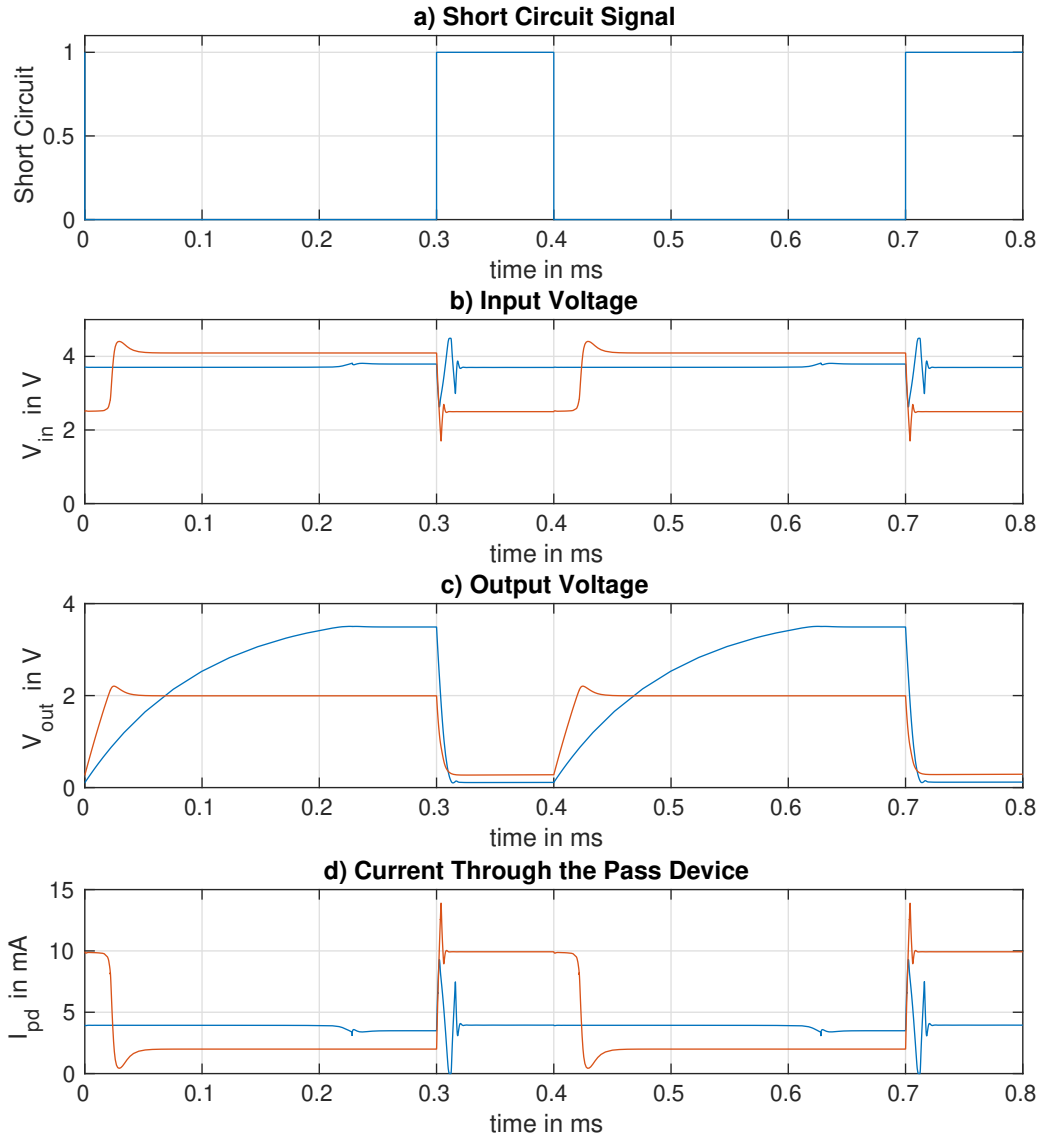

Fig. 6.9: Transient Analysis - Short Circuit Behavior. The transient short circuit behavior of the Power Source when a large capacitor is connected in parallel to the load for two different output voltages and input voltage limits with a supply voltage of 4.5 V. a) represents the short circuit control signal. In b), the input voltage of the Power Source is shown for a limit of 2.5 V (red) and 3.7 V (blue). The output voltages 2.0 V (red) and 3.5 V (blue) are shown in c). In the sub figure d), the respective current through the pass device for both operating points is shown. This current represents the load current and the quiescent current through the output voltage divider.

output voltage. If only the load capacitor is connected to the output pin, the charging curve is linear until the desired output voltage of the low-dropout regulator is reached.

6.4 Monte Carlo and Temperature Corner Simulations

The last part of the circuit verification is done with so called Monte Carlo and corner simulations. In the Monte Carlo simulation, the process models include process- and mismatch variations which are important due to the changing behavior of the circuit. Different ambient temperatures of the Power Source are simulated with corner simulations. As usual for consumer electronics, the temperature corners are $-20\,°C$, $27\,°C$ and $80\,°C$. The most important information from these analyses are the effects on the phase margins of the control loops and the output voltage or input voltage limit of the Power Source.

The Power Source is supplied during these simulations with 3.3 V via a source resistance of $109\,\Omega$. The output voltage is set to 2.0 V and a load resistor of $1\,k\Omega$ is connected in parallel to a 100 nF load capacitor to the output pin. To ensure that the output voltage control loop is active during the first simulations, the input voltage limit is set to 2.5 V. All simulation results for the output voltage regulator are shown in table 6.1.

Parameter	Minimal	Mean	Maximum	Standard Deviation
Phase Margin $27\,°C$	$66.30\,°$	$70.15\,°$	$72.47\,°$	$1.286\,°$
Phase Margin $-20\,°C$	$64.42\,°$	$68.80\,°$	$71.57\,°$	$1.496\,°$
Phase Margin $80\,°C$	$68.27\,°$	$71.52\,°$	$73.52\,°$	$1.064\,°$
V_{out} $27\,°C$	1.910 V	1.992 V	2.100 V	36.98 mV
V_{out} $-20\,°C$	1.913 V	1.992 V	2.097 V	36.43 mV
V_{out} $80\,°C$	1.906 V	1.989 V	2.102 V	37.79 mV

Table 6.1: Monte Carlo and corner simulation results for the output voltage regulator.

To simulate the input voltage regulator, the load resistance is reduced to $100\,\Omega$ in order to activate the control circuit. The simulation results are presented in table 6.2.

Parameter	Minimal	Mean	Maximum	Standard Deviation
Phase Margin $27\,°C$	$52.70\,°$	$64.41\,°$	$70.91\,°$	$3.143\,°$
Phase Margin $-20\,°C$	$45.70\,°$	$58.61\,°$	$67.36\,°$	$3.977\,°$
Phase Margin $80\,°C$	$59.42\,°$	$68.2\,°$	$76.10\,°$	$3.764\,°$
$V_{in,limit}$ $27\,°C$	2.249 V	2.495 V	2.699 V	73.05 mV
$V_{in,limit}$ $-20\,°C$	2.239 V	2.496 V	2.706 V	75.78 mV
$V_{in,limit}$ $80\,°C$	2.259 V	2.494 V	2.691 V	70.42 mV

Table 6.2: Monte Carlo and corner simulation results for the input voltage regulator.

As recognizable, the standard deviations of the input voltage regulator are almost twice as large as the deviations of the output voltage control loop. The reason for this is that the input voltage control loop passes two error amplifiers. Therefore, the offset of this control loop is nearly twice as large as the offset of the low-dropout voltage regulator.

Chapter 7

Conclusion

The presented concept of the NFC Power Source in this thesis is a fully integrated power management solution for NFC applications. This circuit combines two separate control loops into one stable system which makes it easier to implement it in an IC. The Power Source is adaptable to different types of loads and supply sources due to the adjustable voltage limits on the output- and input pin. The basis of the Power Source is a low-dropout voltage regulator and a PMOS transistor as pass device. A flipped LDO is used as input voltage regulator to detect a decrease of the input potential. The output of this control circuit is connected to the gate of a NMOS transistor which pulls the input potential of the output voltage error amplifier to the input voltage of the Power Source, if the load current causes a too large decrease of it. Several pole compensation methods are necessary to achieve a stable operation for both control loops.

The circuit is supplied with voltages between 3.3 V and 4.5 V from a 100 mW voltage source and is able to provide regulated output potentials from 1.1 V to 4.2 V in 100 mV steps. The Power Source can control the maximum voltage decrease on the input pin from 2.5 V to 4.4 V, also in 100 mV steps. During operation, the Power Source consumes a maximum quiescent current of 35 μA. With a load capacitor of 100 nF, the circuit can guarantee a stable operation for all load currents. If no load resistor is connected to the output pin, a minimum 160 pF load capacitor is needed to achieve a stable operation. If a resistor is connected at the output pin, a minimum load current of 3.8 μA is necessary to achieve at least a phase margin of 45 °. In table 7.1, a comparison between the parameters of the input voltage- and the output voltage regulator, simulated in a typical operating point, is done.

The transistor level design of the Power Source is implemented in a 130 nm standard CMOS process where the circuit consumes about 0.049 mm^2 chip area. The verification is done with Monte Carlo and corner simulations.

Parameter	**Output Voltage Regulator**	**Input Voltage Regulator**
Type of Load	1 kΩ and 100 nF	
Output Voltage	2.5 V	
Input Voltage Limit	3.0 V	
Supply Voltage Level	3.3 V	
Quiescent Current	31 μA	
Open Loop Gain	73 dB	112 dB
Phase Margin	71 °	66 °
Unity Gain Frequency	102 kHz	421 kHz

Table 7.1: Comparison between the parameters of both control loops.

Chapter 8

Outlook

The presented concept and design in this thesis shows a good control behavior for both voltages. Of course, there is room for some improvements in the implemented circuit which are discussed in this outlook. Besides that, a test chip is necessary to investigate and measure the real behavior of the circuit. After a full verification in the laboratory, the Power Source should be implemented in a passive NFC device. Since the test bench presented in this thesis is only a simplification of the whole application, an implementation of the Power Source in a fully-modeled test bench, consisting of an NFC reader device and an analog front-end, is necessary. Based on this test bench, the impact of the control behavior of the Power Source on the whole system needs to be investigated.

The Power Source works properly in stationary operating conditions. If the output pin is shorted to ground, the input voltage regulator needs some time to control the voltage on the input pin. To minimize the settling time, the input voltage control loop needs to react faster. This can be achieved by increasing the unity gain frequency of both error amplifiers. To reduce the voltage overshoot during the regulation, also the phase margin of the whole input voltage control loop needs to be increased by improving the pole compensation methods or introducing new ones.

To reduce the leakage current through the pass device, if a load capacitor is charged and the circuit is disconnected from a supply potential, the length of the transistor should be increased. The pass device is quite small in comparison to the remaining layout of the Power Source. Therefore, this improvement should not increase the chip area strongly. In the implemented design, the leakage current is about 116 nA if the load capacitor is charged to 4.2 V and the input pin is connected to ground.

Appendix A

Input Voltage Limits - Pin Configuration

Input Voltage Limit	**5 Bit Decoder - Digital Input**				
	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
1.3 V	0	0	0	0	0
1.4 V	0	0	0	0	1
1.5 V	0	0	0	1	0
1.6 V	0	0	0	1	1
1.7 V	0	0	1	0	0
1.8 V	0	0	1	0	1
1.9 V	0	0	1	1	0
2.0 V	0	0	1	1	1
2.1 V	0	1	0	0	0
2.2 V	0	1	0	0	1
2.3 V	0	1	0	1	0
2.4 V	0	1	0	1	1
2.5 V	0	1	1	0	0
2.6 V	0	1	1	0	1
2.7 V	0	1	1	1	0
2.8 V	0	1	1	1	1
2.9 V	1	0	0	0	0
3.0 V	1	0	0	0	1
3.1 V	1	0	0	1	0
3.2 V	1	0	0	1	1
3.3 V	1	0	1	0	0
3.4 V	1	0	1	0	1
3.5 V	1	0	1	1	0
3.6 V	1	0	1	1	1
3.7 V	1	1	0	0	0
3.8 V	1	1	0	0	1
3.9 V	1	1	0	1	0
4.0 V	1	1	0	1	1
4.1 V	1	1	1	0	0
4.2 V	1	1	1	0	1
4.3 V	1	1	1	1	0
4.4 V	1	1	1	1	1

Table A.1: The input voltage limit can be defined by the five digital inputs of the Power Source.

Appendix B

Output Voltage - Pin Configuration

Output Voltage	**5 Bit Decoder - Digital Input**				
	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
1.1 V	0	0	0	0	0
1.2 V	0	0	0	0	1
1.3 V	0	0	0	1	0
1.4 V	0	0	0	1	1
1.5 V	0	0	1	0	0
1.6 V	0	0	1	0	1
1.7 V	0	0	1	1	0
1.8 V	0	0	1	1	1
1.9 V	0	1	0	0	0
2.0 V	0	1	0	0	1
2.1 V	0	1	0	1	0
2.2 V	0	1	0	1	1
2.3 V	0	1	1	0	0
2.4 V	0	1	1	0	1
2.5 V	0	1	1	1	0
2.6 V	0	1	1	1	1
2.7 V	1	0	0	0	0
2.8 V	1	0	0	0	1
2.9 V	1	0	0	1	0
3.0 V	1	0	0	1	1
3.1 V	1	0	1	0	0
3.2 V	1	0	1	0	1
3.3 V	1	0	1	1	0
3.4 V	1	0	1	1	1
3.5 V	1	1	0	0	0
3.6 V	1	1	0	0	1
3.7 V	1	1	0	1	0
3.8 V	1	1	0	1	1
3.9 V	1	1	1	0	0
4.0 V	1	1	1	0	1
4.1 V	1	1	1	1	0
4.2 V	1	1	1	1	1

Table B.1: The output voltage of the Power Source can be defined with the five digital inputs.

Appendix C

Input Voltage Regulator - Transfer Function

The transfer function is derived with the small signal model shown figure 4.6. The parameters g_m and r_{DS} are equal to $g_{m,PMOS}$ and $r_{DS,PMOS}$. The signal v_{in} in this derivation equals $v_{out,EA}$ and v_{out} is equivalent to the signal v_{in}.

First, Kirchhoff's current law is applied to the output node which results in following equation:

$$g_m \cdot v_{in} - g_m \cdot v_{out} = \frac{v_{out}}{R_{IN}} + \frac{v_{out}}{r_{DS}} - \frac{v_x}{r_{DS}} \tag{C.1}$$

Where v_x is the voltage between the drain pin of the pass device and ground and is defined by:

$$v_x = i_x \cdot \frac{R_{OUT}}{1 + s \cdot C_{load} \cdot R_{OUT}} \tag{C.2}$$

i_x can be derived by applying Kirchhoff's law to this node:

$$i_x = -g_m \cdot v_{in} + g_m \cdot v_{out} + \frac{v_{out}}{r_{DS}} - \frac{v_x}{r_{DS}} \tag{C.3}$$

$$i_x = -g_m \cdot v_{in} + g_m \cdot v_{out} + \frac{v_{out}}{r_{DS}} - \frac{i_x \cdot R_{OUT}}{r_{DS} \cdot (1 + s \cdot C_{load} \cdot R_{OUT})} \tag{C.4}$$

$$i_x \cdot \left(1 + \frac{R_{OUT}}{r_{DS} \cdot (1 + s \cdot C_{load} \cdot R_{OUT})}\right) = -g_m \cdot v_{in} + g_m \cdot v_{out} + \frac{v_{out}}{r_{DS}} \tag{C.5}$$

$$i_x = \frac{\frac{v_{out}}{r_{DS}} + g_m \cdot v_{out} - g_m \cdot v_{in}}{1 + \frac{R_{OUT}}{r_{DS} \cdot (1 + s \cdot C_{load} \cdot R_{OUT})}} \tag{C.6}$$

Therefore, v_x is represented by:

$$v_x = \frac{\frac{v_{out}}{r_{DS}} + g_m \cdot v_{out} - g_m \cdot v_{in}}{1 + \frac{R_{OUT}}{r_{DS} \cdot (1 + s \cdot C_{load} \cdot R_{OUT})}} \cdot \frac{R_{OUT}}{1 + s \cdot C_{load} \cdot R_{OUT}} \tag{C.7}$$

With v_x, equation C.1 can be rewritten as:

$$\begin{aligned} g_m \cdot v_{in} - g_m \cdot v_{out} = \frac{v_{out}}{R_{IN}} + \frac{v_{out}}{r_{DS}} \\ - \frac{\frac{v_{out}}{r_{DS}} + g_m \cdot v_{out} - g_m \cdot v_{in}}{1 + \frac{R_{OUT}}{r_{DS} \cdot (1 + s \cdot C_{load} \cdot R_{OUT})}} \\ \cdot \frac{R_{OUT}}{1 + s \cdot C_{load} \cdot R_{OUT}} \cdot \frac{1}{r_{DS}} \end{aligned} \tag{C.8}$$

By doing some math, this equation can be rewritten as:

$$g_m \cdot v_{out} - g_m \cdot v_{out} = \frac{v_{out}}{R_{IN}} + \frac{v_{out}}{r_{DS}} \tag{C.9}$$

$$- \frac{v_{out} \cdot (R_{OUT} + g_m \cdot R_{OUT} \cdot r_{DS})}{r_{DS}^2 \cdot (1 + s \cdot C_{load} \cdot R_{OUT}) + R_{OUT} \cdot r_{DS}} \tag{C.10}$$

$$+ \frac{v_{in} \cdot (g_m \cdot R_{OUT} \cdot r_{DS})}{r_{DS}^2 \cdot (1 + s \cdot C_{load} \cdot R_{OUT}) + R_{OUT} \cdot r_{DS}} \tag{C.11}$$

The transfer function is calculated by solving this equation to $\frac{v_{out}}{v_{in}}$:

$$\boxed{\frac{v_{out}}{v_{in}} = \frac{g_m \cdot R_{IN} \cdot r_{DS} \cdot (1 + s \cdot C_{load} \cdot R_{OUT})}{(r_{DS} + R_{OUT} + R_{IN} + g_m \cdot R_{IN} \cdot r_{DS}) \left(1 + s \cdot \frac{C_{load} \cdot R_{OUT} \cdot (r_{DS} + R_{IN} + g_m \cdot R_{IN} \cdot r_{DS})}{r_{DS} + R_{OUT} + R_{IN} + g_m \cdot R_{IN} \cdot r_{DS}}\right)}} \tag{C.12}$$

The zero of this function is described with:

$$\boxed{z = \frac{1}{2 \cdot \pi \cdot C_{load} \cdot R_{OUT}}} \tag{C.13}$$

And the pole is defined by:

$$\boxed{p = \frac{r_{DS} + R_{OUT} + R_{IN} + g_m \cdot R_{IN} \cdot r_{DS}}{2 \cdot \pi \cdot C_{load} \cdot R_{OUT} \cdot (r_{DS} + R_{IN} + g_m \cdot R_{IN} \cdot r_{DS})}} \tag{C.14}$$

The DC gain is defined by:

$$\boxed{A_{DC} = \frac{g_m \cdot R_{IN} \cdot r_{DS}}{r_{DS} + R_{OUT} + R_{IN} + g_m \cdot R_{IN} \cdot r_{DS}}} \tag{C.15}$$

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