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Characterization of Thin Titanium Nitride Layers in Through Silicon Via Technology

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Abbreviations

BEOL	**B**ack-**E**nd **O**f **L**ine
BGA	**B**all **G**rid **A**rray
BWM	**B**ack **W**afer **M**ask
CMOS	**C**omplementary **M**etal-**O**xide **S**emiconductor
CVD	**C**hemical **V**apour **D**eposition
CRA	**C**lean **R**oom **A**tmosphere
DRIE	**D**eep **R**eactive **I**on **E**tching
EDX	**E**nergy **D**ispersive **X**-Ray Spectroscopy
EELS	**E**lectron **E**nergy **L**oss **S**pectroscopy
FA	**F**ailure **A**nalysis
FAB	**Fab**rication Facility
FEOL	**F**ront-**E**nd **O**f **L**ine
FFT	**F**ast **F**ourier **T**ransformation
FIB	**F**ocused **I**on **B**eam
HAR	**H**igh **A**spect **R**atio
ILD	**I**nter **L**evel **D**ielectric
MOCVD	**M**etal **O**rganic **C**hemical **V**apour **D**eposition
PAS	**Pas**sivation
PB	**P**urge **B**ox
PECVD	**P**lasma **E**nhanced **C**hemical **V**apour **D**eposition
PT	**P**lasma **T**reatment
PVD	**P**hysical **V**apour **D**eposition
RDL	**R**edistribution **L**ayer
SEM	**S**canning **E**lectron **M**icroscopy
TDMAT	**T**etrakis(**dim**ethyl**a**mino)**t**itanium
TEM	**T**ransmission **E**lectron **M**icroscopy
TSV	**T**hrough **S**ilicon **V**ia
UTEOS	**U**ndoped **T**etra**e**thyl**o**rthos**i**licat
WT	**W**afer **T**ype
XPS	**X**-Ray **P**hotoelectron **S**pectroscopy

Abstract

Chemical vapor deposited titanium nitride (CVD TiN) used as contact liner and diffusion barrier in through silicon via (TSV) technology has been characterized by means of 4-point probe sheet resistance measurements, scanning electron microscopy (SEM), transmission electron microscopy (TEM), electron energy loss spectroscopy (EELS) and x-ray photolectron spectroscopy (XPS). It has been found that TiN forms different Ti bonds like $TiSi_2$ and TiO_2 at TiN / SiO_2 interfaces. Furthermore, it has been shown that the plasma densification step during the TiN deposition, which is crucial for good final properties of the CVD TiN, does not or only partially affect the CVD TiN at TSV side walls. This results in insufficiently dense TiN with high resistance and resistance increase during exposure to clean room atmosphere, high carbon contaminations as well as bad adhesion and barrier properties inside TSVs, which can ultimately lead to defects like the known volcano effect.

Kurzfassung

Chemisch gasphasenabgeschiedenes Titan Nitrid (CVD TiN) welches als Kontaktschicht und Diffusionsbarriere in Silizium Durchkontakten (englisch Through Silicon Via, TSV) verwendet wird, wurde mittels 4-Punkt Schichtwiderstandmessung, Rasterelektronenmikroskopie (REM), Transmissionselektronenmikroskopie (TEM), Elektronenenergieverlustspektroskopie (EELS) und Röntgenphotoelektronenspektroskopie (XPS) charakterisiert. An der TiN / SiO_2 Grenzfläche konnten verschiedene Titanverbindungen wie $TiSi_2$ und TiO_2 nachgewiesen werden. Weiters konnte gezeigt werden, dass der Plasmadensifizierungsschritt während der TiN Abscheidung, welcher wichtig für gute Eigenschaften der finalen TiN Schicht ist, das TiN an der Seitenwand des TSVs gar nicht oder nur wenig beeinflusst. Dies resultiert in undensifiziertem TiN mit hohem Schichtwiderstand und Schichtwiderstandsanstieg bei Lagerung in Reinraumatmosphäre, hohem Kohlenstoff gehalt sowie schlechten Haft- und Barriereeigenschaften, was letztendlich zu Defekten wie dem bekannten "Volcano-Effekt" führen kann.

Contents

Chapter 1

Introduction

1.1 Introduction

In 1965 Gordon Moore predicted a trend which is today known as Moore's Law. This law states, that the number of transistors on a wafer will double every two years while the price per transistor stays constant [1]. One of the main reasons Moore's Law stays true since the 1970s is the constant scaling of transistors to smaller sizes. However, this downscaling trend, and therefore Moore's Law, can not sustain forever. Materials properties, tools, processing and physical limitations are examples for factors that constrain further miniaturization of semiconductor devices [2]. The concept of further persuing Moore's Law and finding solutions to these difficulties and further increase the performance, is called *More Moore* [2]. Another trend in modern microelectronics is the *More Than Moore* [3] approach, which focuses on the functional diversification of semiconductor-based devices, for example the interaction with sensors and other additional systems via 3D- and wafer level integration [3].

One technology that follows the *More Than Moore* approach is the so-called *Through Silicon Via* (TSV) technology. Through silicon vias are holes through Silicon (Si) wafers, creating a galvanic connection between the two sides of the wafers [4]. These vias connect for example complementary metal-oxide semiconductors (CMOS) to sensors through wafers, avoiding complex wiring.

These vertical interconnects have high aspect ratios (HAR) and are typically filled with an insulating dielectric layer with a metallization layer, consisting of a bi - or multilayer stack of functional materials, on top [5]. The insulation layer, typically silicon dioxide (SiO_2), isolates the TSVs from the substrates and nearby TSVs. The metallization layer, which consist of a thin diffusion barrier layer/contact liner, an adhesion/nucleation layer and the conduction metal, ensures electrical contact between the devices [5, 4]. The barrier layer/contact liner, typically titanium nitride (TiN) or tantalum nitride (TaN), which is normally only a few nm thin, ensures good adhesion and contact between the TSV isolation layer/devices and the conduction metal. Additionally, it prevents the diffusion of metal and other contaminating elements into the dielectric and substrate [5]. The conduction metal, tungsten (W) or copper (Cu) provides electrical connections by either filling TSVs completely (filled TSV) or only partially (open TSV) with the metal.
At *austrianmicrosystems AG* (*ams AG*) open TSVs with an aspect ratio of 5:1, silicon dioxide as insulation layer, a titanium layer for adhesion, titanium nitride as barrier layer/contact liner and tungsten as conduction layer are processed and developed. A good understanding and knowledge of these layers and their processing are crucial for creating functional TSVs.

The few nm thin titanium nitride film in the metallization stack plays a crucial role in the functionality of the TSVs. It works as glue between the insulation/titanium layer and the conduction metal and prevents contamination of the substrate and dielectric. Bad adhesion and contaminations can lead to delaminations of layers and electrical failures. Thus the processing and the final properties like sheet resistance, crystal structure, layer thickness and purity of the TiN film are important for the quality of the final TSV.

This thesis aims for a better understanding of the TiN barrier layer and its behaviour inside TSVs. Different deposition procedures of the TiN, environmental influences on the thin layer and its impact on the metal layer growth and stability are investigated by means of various characterization methods like sheet resistance measurement, scanning electron- and transmission electron microscopy (SEM [6], TEM [7]), energy electron loss spectroscopy (EELS [8]) and x-ray photoelectron spectroscopy (XPS [9]).

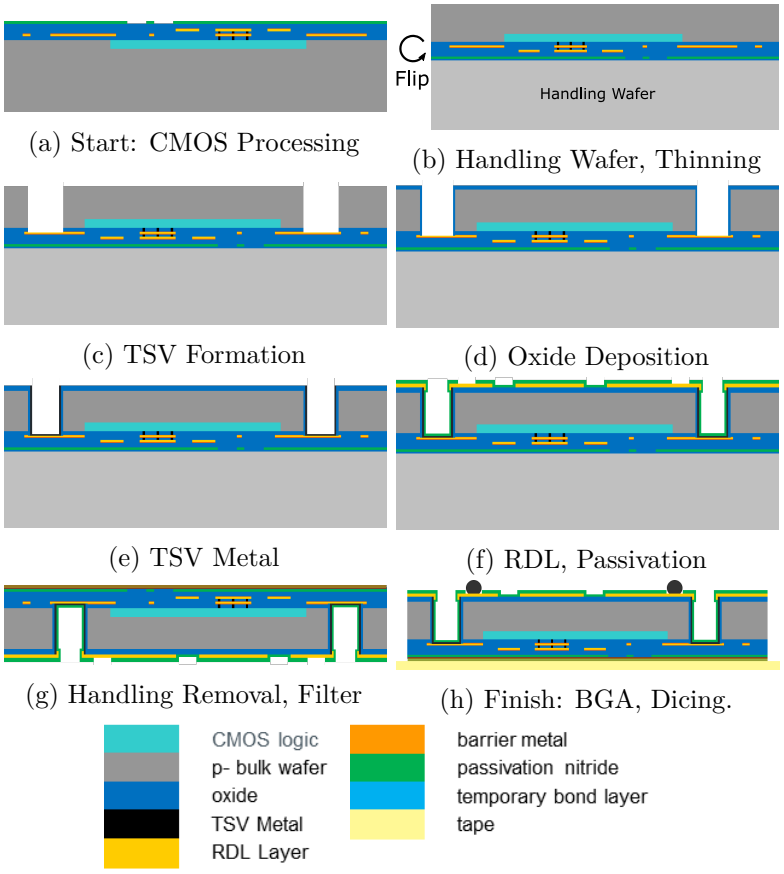
Chapter 2

Fundamentals

2.1 Through Silicon Vias. Basics and Processing

Through silicon vias (TSVs) are vertical interconnects, electrically connecting the backside and frontside of a silicon wafer. This connection is used to stack devices and create 3D - structures. There are a variety of different approaches for processing TSVs which are characterized by, for example the order of the TSV process with respect to wafer processing, 3D - Bonding method and wafer thinning. At the "*Via-First*" approach, TSVs are created before the front-end of line (FEOL) device fabrication. TSVs processed after the FEOL but before the back-end of line (interconnect process, BEOL) are called "*Via-Middle*" TSVs [4].

austrianmicrosystems AG develops TSVs with a diameter of $d_{TSV} = 40\ \mu m$ and a depth of $h_{TSV} = 200\ \mu m$ (TSV40) with a so - called "*Via-Last*" approach, where the TSVs are created after the whole CMOS process is finished (after BEOL). An illustration of the TSV "*Via-Last*" process flow can be seen in figure 2.1.1. The single steps will be explained in detail in the following sections.



(a) Start: CMOS Processing

(b) Handling Wafer, Thinning

(c) TSV Formation

(d) Oxide Deposition

(e) TSV Metal

(f) RDL, Passivation

(g) Handling Removal, Filter

(h) Finish: BGA, Dicing.

(i) Colour Code

Figure 2.1.1: TSV Process flow. From Processed CMOS to Finished TSV Device

2.1.1 TSV Formation

After the CMOS wafer is processed (fig. 2.1.1a), the TSV fabrication starts by bonding and thinning of the wafer and the formation of the TSVs. The final CMOS wafer is very thin and thus difficult to handle. Therefore the CMOS wafer is temporarily bonded to a handling wafer to facilitate the handling during processing. After the handling wafer is bonded, the whole wafer is flipped over so the backside of the device wafer, where the TSVs are formed, can be worked on (fig. 2.1.1b).

After the device wafer is bonded it is thinned to the desired thickness of 200 μm and a resist is deposited in a spin-coating process followed by lithographic exposure and development to create the backside wafer mask (BWM) for the TSVs. The TSVs are then etched into the silicon with a deep reactive ion etching (DRIE) process (*Bosch Process*) [10] which is a repeating cycle of three steps to create anisotropic etched holes with high aspect ratios (fig. 2.1.1c). First the silicon is isotropically etched with sulfur hexafluoride (SF_6), followed by a deposition of octafluorocyclobutane (C_4F_8) as side wall passivation. As third and last step, the passivation at the bottom is sputtered by ion bombardment of the etching gas, so the silicon is set free to be etched again with SF_6. These three steps are repeated until the desired depth or an etch-stop layer is reached. Figure 2.1.2 illustrates the DRIE process. 2.1.2a shows the etching of the Si with SF_6, 2.1.2b the deposition of the C_4F_8 side wall passivation and 2.1.2c the removal of the passivation layer at the bottom. At the TSV process the etching stops as soon as the silicon dioxide (SiO_2) layer of the inter-level dielectric (ILD) on the CMOS side is reached.

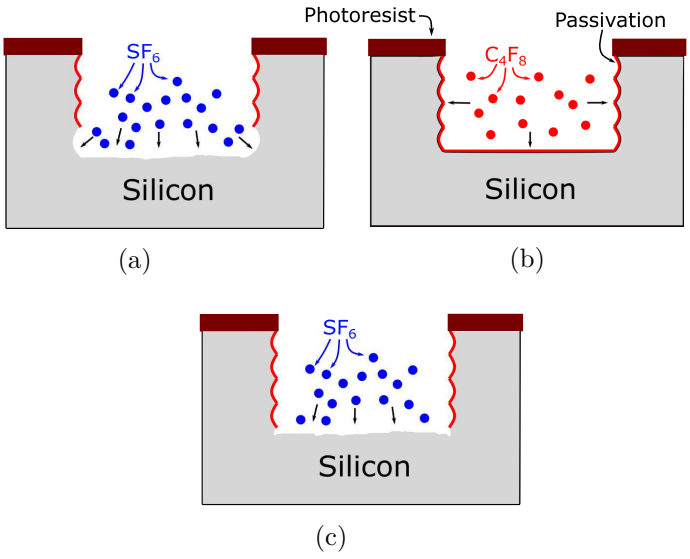
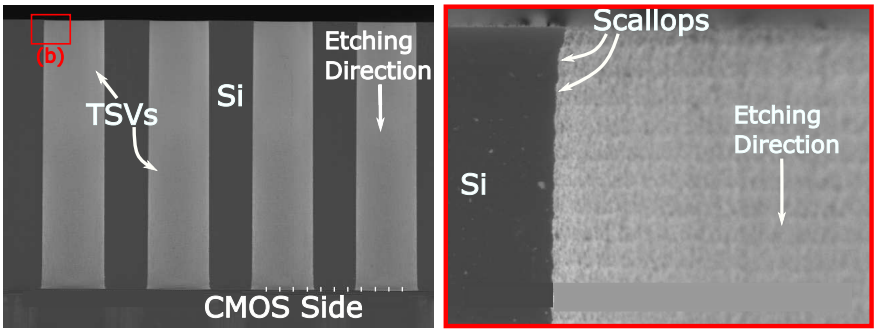


Figure 2.1.2: Illustration of the Bosch Process for etching holes into silicon wafers. (a) Etching into the silicon with SF_6 (b) deposition of the C_4F_8 passivation layer (c) removal of the passivation layer at the bottom.

Due to the cycle of discontinuing etching, rough scallops at the side wall are created. After the DRIE process is finished, the newly formed TSVs are

cleaned to remove remaining chemicals from the etching process. Residuals of the cleaning agents can get stuck at the scallops which consequently can cause delaminations of the following isolation layer. Figure 2.1.3 shows a SEM cross section image of four TSVs after the DRIE process and a close-up of the top corner of one of the TSVs (red box), revealing the scalloped side wall.



(a) (b)

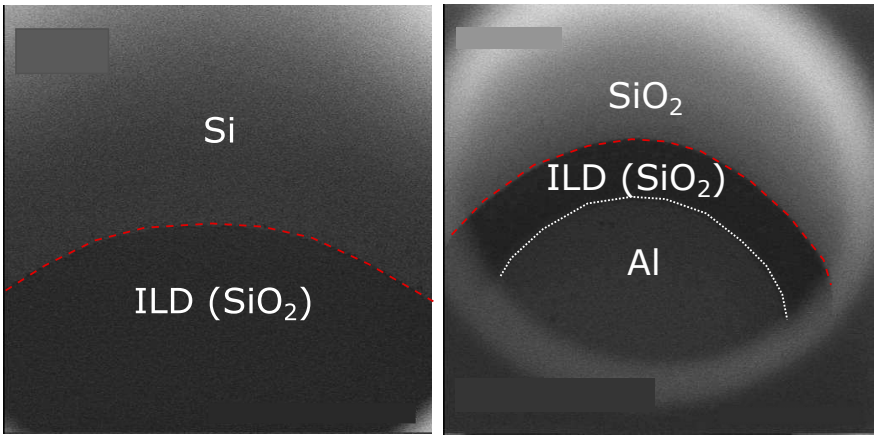
Figure 2.1.3: Cross section of TSVs after the Bosch process. (a) Full view of the TSVs after finished etching. (b) Close-up of the rough side wall scallops at the top corner of the TSV.

In 2.1.3a, four TSVs (bright), side by side, after the DRIE process are visible. The etching starts at the backside of the wafer (TSV top) and stops at the CMOS side. The TSVs are separated by the silicon which was protected by the photo resist during the DRIE. The repeating isotropic etching of the Si produces the in 2.1.3b visible scallops throughout the whole via.

2.1.2 Insulating Layer

The next step is the deposition of the insulating dielectric SiO_2 layer. Deposited via plasma enchanced chemical vapour deposition (PECVD) [11] using undoped tetraethylorthosilicat (UTEOS) as precursor, the purpose of the layer is the electrical isolation between the silicon substrate and the TSV metal. The dielectric constant (κ), leakage current and breakdown voltage are main criteria for a good insulation [12]. The step coverage of the deposited SiO_2 is very poor ($\approx$ 6:1). Consequently, the oxide at the top side walls of the TSVs is much thicker compared to the oxide on the bottom

side walls. Due to the already processed CMOS and its metal layers, the SiO_2 CVD and all other following depositions are performed at moderate temperatures in a range of $200 - 400\ °C$ to avoid damaging the device [5]. After the deposition, the SiO_2 at the bottom (CMOS side) and the underlying ILD are etched in order to set the metal layer, typically aluminium (Al), of the CMOS free (fig. 2.1.1d). Figure 2.1.4 shows SEM images of a TSV bottom after the through silicon and bottom oxide etch.



(a) (b)

Figure 2.1.4: SEM image of the side wall and bottom of a TSV after (a) the Bosch process with stop at the ILD oxide (b) insulation layer deposition and bottom oxide etch.

In order to see the bottom of the TSVs in the SEM, the wafers are tilted by 6°. After the DRIE process, the ILD oxide lays open (2.1.4a). The red dashed line indicates the edge between the Si and the ILD. An example of a TSV after the deposition of the isolation oxide and opening of the CMOS metal is shown in 2.1.4b. The red dashed line and the white dotted line indicate the TSV oxide/ILD and ILD/CMOS metal interface, respectively.

2.1.3 TSV Metallization: Contact Liner, Barrier Layer

Titanium nitride (TiN) is a widely used material in semiconductor industry due to it's favourable properties like low resistivity, good mechanical and chemical characteristics as well as good barrier properties and step coverage [5, 13, 14]. Typically before the TiN, titanium (Ti) as adhesive layer is

deposited via physical vapor deposition (PVD) [15], followed by the TiN as diffusion barrier and TSV metal contact [16]. Compared to CVD, PVD has a bad step coverage in HAR vias, therefore it is assumed that the PVD Ti does not cover the side walls inside the TSVs sufficiently and only the CVD TiN is deposited.

Metal organic CVD (MOCVD) [17] is used to deposit TiN inside TSVs, using tetrakis(dimethylamino)titanium (TDMAT) as precursor for the deposition. TDMAT is brought onto the substrate and into the TSV via a bubbler system, using either molecular hydrogen (H_2) or molecular nitrogen (N_2) as carrier gas. The reaction on the surface is triggered by temperature (pyrolysis) and can be described by following chemical equation [5]:

$$Ti[N(CH_3)_2]_4 \longrightarrow TiN(C,N) + HN(CH_3)_2 + hydrocarbons \qquad (2.1.1)$$

TiN is deposited in a two-step cycle. The first step is the deposition of 5 nm TiN, followed by a plasma treatment (PT) step, which reduces the TiN thickness to approximately 2.5 nm. This N_2/H_2 - plasma densification step reduces carbon (C) and hydrogen (H) contaminations inside the layer, enhances its adhesive properties for the following tungsten (TSV metal), reduces the sheet resistance significantely, reduces the oxygen incorporation during air exposure and increases the chemical stability of the TiN film. [5, 18, 19].
The final film thickness is dependent on the number of cycles. For TSVs at *ams AG*, three iterations of TDMAT pyrolysis and densification steps are performed, resulting in a final layer thickness of approximately $7 - 9$ nm. Treatment time, plasma power and chamber pressure during the plasma step are some of the main parameters which impact the sheet resistance and the final properties of resulting TiN layer [18, 19].

2.1.4 TSV Metallization: TSV Conduction Metal

At *ams AG* chemical vapor deposited tungsten (W) is used as conduction metal (2.1.1e). The underlying TiN layer works as seed layer and has good adhesion to W [5]. In order to reduce C contaminations on the TiN and enhance the adhesion to the W even more, typically a H_2 anneal step is

performed before W is deposited.

The deposition of W is a multiple step process where the first step is the deposition of an approximately 40 nm thick W - nucleation layer, to improve the growth and quality of the following bulk W. The CVD process for this nucleation layer includes the reduction of tungsten hexafluoride (WF_6) with silane (SiH_4) [5].

$$3SiH_4 + 2WF_6 \longrightarrow 2W + 3SiF_4 + 6H_2 \tag{2.1.2}$$

The next step is the deposition of approximately 400 nm bulk W. Precursor is again WF_6 and as reduction gas H_2 is used [5].

$$WF_6(vapor) + 3H_2(gas) \longrightarrow W(solid) + 6HF(gas) \tag{2.1.3}$$

Flow of the WF_6 and temperature of the substrate are crucial factors for the deposition rate [5].

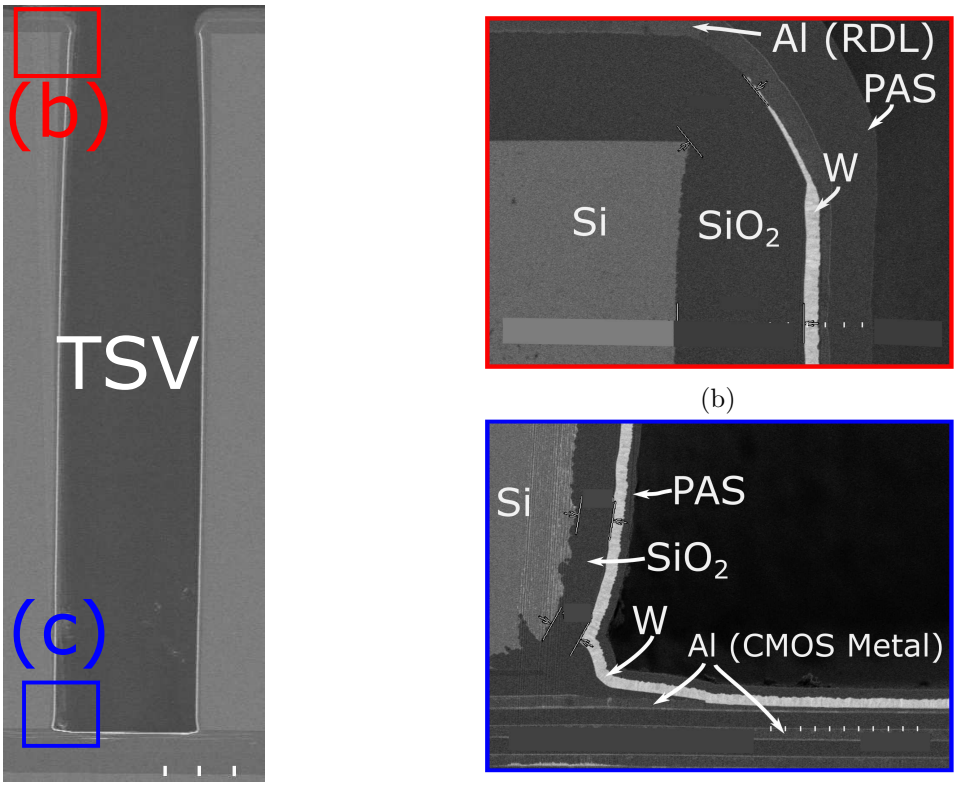
At last a W etch back, performed after the finished bulk W deposition, removes the W layer from the substrate surface outside of the TSVs, to ensure electrical isolation between surrounding TSVs [5].

W is not only deposited on the wafers but also on the side walls inside the deposition chamber. With rising film thickness due to the constant processing of wafers, high stress in the W on the chamber side walls occurs. This consequently results in delamination of the W from the chamber side walls, leaving undesired W particles inside the chamber. To avoid this, a chamber clean using NF_3 is performed after a specific count of processed wafers, removing the W from the side walls. After the clean, the side walls get seasoned with a fresh thin W layer before the next deposition, to guarantee similar chamber conditions for all wafers.

2.1.5 TSV Finish

After the metallization of the TSV is done, the last steps in the TSV process are the deposition of a structured redistribution layer (RDL, Al) to create

the desired connections, deposition of a silicon nitride (Si_3N_4) passivation layer (PAS), to protect underlying layers (2.1.1f) and the removal of the handling wafer (2.1.1g). With addition of a ball grid array (BGA) and dicing of the wafer (2.1.1i), the TSV and wafer process is finish.
SEM images of a cross section from a finished TSV40, after metallization (2.1.1e), RDL and PAS deposition (2.1.1f), can be seen in figure 2.1.5.



(a) (b) (c)

Figure 2.1.5: (a) Full view of a TSV cross section (b) Close up of the top side of the TSV (c) close up of the bottom side (CMOS side)

SiO_2, W, Si as well as the passivation layer, the RDL on top (2.1.5b) and CMOS metal (2.1.5c) at the bottom are visible and distinguishable, although the thin Ti and TiN layers are not visible at this magnification.
As discussed in section 2.1.2, CVD SiO_2 has a poor step coverage, this can be seen in figures 2.1.5b and 2.1.5c. The SiO_2 at the top is much thicker compared to the SiO_2 at the bottom.

2.2 TSV Defects

A variety of different failure mechanisms can cause defects inside TSVs during or post processing, resulting in degradation of TSV properties and in total TSV fails. In this section, some known and prominent defects and its sources are described.

2.2.1 Notching Effect

The notching effect (also footing effect) is a phenomenon of the DRIE process during the formation of the TSVs (section 2.1.1). When the SF_6 plasma which is used for the etching reaches the insulating SiO_2 layer on the CMOS side of the wafer (ILD), horizontal Si etching along the Si/SiO_2 interface occurs. Free electrons of the plasma have little to no directionality and get stuck in the rough, scalloped Si side wall, while the majority of the positively charged ions reach the SiO_2 surface and stay there. The negatively charged Si side wall and the positively charged surface of the insulator create an electric field, deflecting incoming etching ions to the side wall edge between Si and SiO_2 creating a notch [10]. An example of the notching effect can be seen in figure 2.2.1. The red dashed line indicates the Si/SiO_2 interface where the notch starts to form. The scallops on the side wall are due to the DRIE process, as described in section 2.1.1. Notches can alter the mechanical properties and act as defect source as, for example, the cleaning efficiency on the negative slope can be poor [10].

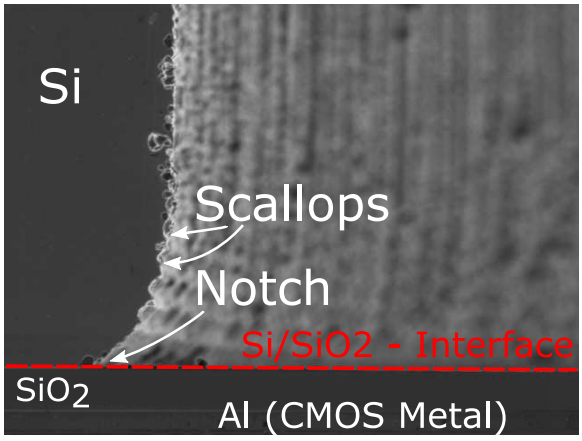


Figure 2.2.1: TSV cross section: Notching effect at TSV Bottom (CMOS Side, see figure 2.1.3a)

Reduction of the notching can be achieved by avoiding creation of charge separation and electric fields by pulsing the substrate bias with either radio - or low frequency, which discharges and neutralizes affected areas [10].

2.2.2 Volcano Effect

As discussed in section 2.1.3, the TiN layer works as diffusion barrier. Its barrier properties are especially crucial for prohibiting fluorine (F) diffusion into the underlying Ti layer. If during the W deposition WF_6 is able to diffuse through the TiN barrier into the Ti, WF_6 reacts with Ti and forms high resistance titanium fluorides (TF_x), either non-volatile TiF_3 or volatile TiF_4 [20]. The reaction can be described for example with following equation [21]:

$$2Ti + WF_6 \longrightarrow 2TiF_3 + W \tag{2.2.1}$$

The formation of TiF_X includes a volume expansion and therefore stress inside the layer. Due to the stress, the overlaying TiN barrier can rupture and open a path for more WF_6 to reach the Ti, creating a volcano-shaped amalgam of W, TiN, Ti and TiF_X, resulting in defects like delamination and complete electric failures of the TSVs [16, 22, 23]. An example of such a defect can be seen in figure 2.2.2:

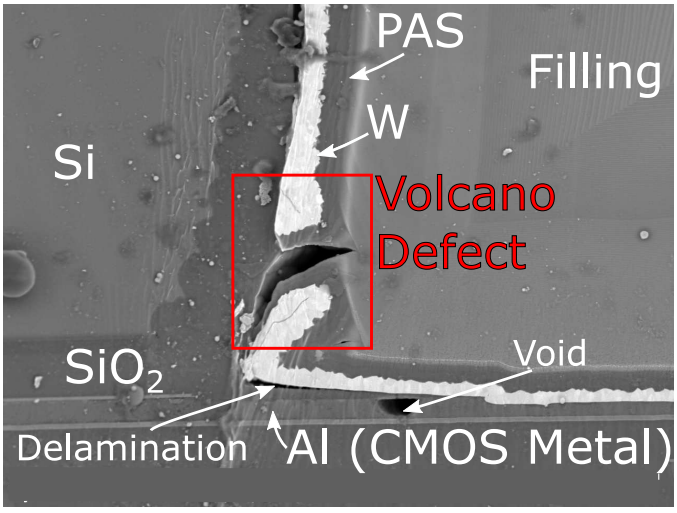


Figure 2.2.2: TSV cross section: Volcano effect at the TSV bottom side wall

The red square highlights the area where the volcano effect occurs. The W layer is visibly cracked open due to high stress in the underlying layers and partial delamination can be seen. The PAS deposited after the W film tore apart, thus some of the silicon nitride was deposited underneath the W. Beside the ruptured W and the delamination, also a void in the CMOS metal is visible, which is the result of cleaning agents from following cleaning steps reaching the Al through the cracked W, indicating that the failure occurs during the W deposition. The filling of the TSV shown in the image acts as help and stabilizer for the cross section preparation.

Beside the WF_6 from the W deposition, another possible F source could be the NF_3 etching gas used for the chamber clean which is described in section 2.2.2, where some of the F resides inside the chamber at ceramic parts after the chamber clean. Therefore the order of wafers in respect to when they were processed after the chamber clean might impact the quality of the TSVs. For example, wafers processed directly after the chamber clean (1^{st} wafers after clean), are exposed to a higher concentration of residual F compared to following wafers (for example 8^{th} wafer after clean).

2.2.3 Delamination and Cracks

During TSV processing several steps are crucial for the creation of defects like delamination and cracks.
Some possible sources for delaminations have already been discussed in the previous chapters, for example residual polymers at the side wall scallops from the clean after the DRIE process, which can cause delaminations of the dielectric (see section 2.1.2), or the volcano effect, which can cause the W to delaminate due to TiF_3 induced stress inside the Ti and TiN layers (see section 2.2.2).

Another source for delamination is the TiN itself. As discussed in section 2.1.3, the plasma treatment (densification) step improves the adhesion to the following CVD W, by removing C contaminations from the film [5]. No or insufficient plasma treatment (PT) can therefore lead to degrading adhesion properties and consequently delaminations of the W layer from the TiN.

Beside delamination, high stress inside the W layer can cause cracks which results in increased resistance and electric failures [5]. An example of a cracked W layer and delamination in the TSV is presented in figure 2.2.3:

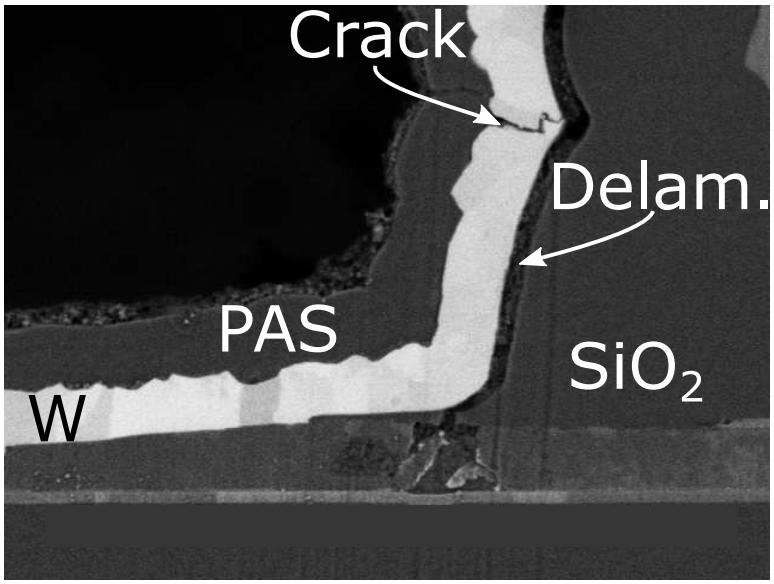


Figure 2.2.3: TSV cross section: Crack and delamination at the TSV bottom (CMOS side)

The figure depicts a cross section of a TSV at the CMOS (bottom) side. The TiN delaminates from the SiO_2 and creates a void between these two layers. Also a stress crack inside the W layer directly at the deepest point of a scallop recess is visible.

2.2.4 Oxidation

During the metallization of TSVs, long queue times at air have to be avoided. In particular the vacuum break time after the TiN deposition and before the W deposition is minimized, to avoid oxidation and contamination of the TiN film. Oxidation reaction of TiN occurs in different steps and can take place at room temperature, creating titanium dioxide (TiO_2, negative Gibbs energy formation ΔG) at the surface [13, 24].

$$TiN + O_2 \longrightarrow TiO_2 + \frac{1}{2}N_2 \tag{2.2.2}$$

Beside surface oxidation, oxygen contamination is also possible through the underlying SiO_2 layer [25]. This oxidation through the SiO_2 layer can ultimately lead to the volcano effect (described in section 2.2.2) by WF_6 diffusing through the TiN and reacting with TiO_2 at the TiN / SiO_2 interface, forming TiF_x [26]:

$$WF_6(g) + TiO_x(s) \rightarrow WO_xF_{2+y} + TiF_{4-y}(g) \tag{2.2.3}$$

The temperature at vacuum break as well as the general quality and the procession of the TiN layer are influencing parameters for the oxidation process [13, 24].

Contrary to the conducting TiN, TiO_2 is an insulator, increasing the overall resistance of the film stack. This newly formed TiO_2 also influences the adhesion to the W, resulting in delaminations at worst [5, 13].

Chapter 3

Experiment Preparation and Execution

Some of the defects described in section 2.2 are directly related to the TiN layer and its processing. Aim of this thesis and its experiments is to understand how different treatment and processing of the thin TiN film affects its properties inside the TSVs as well as in general on blank, unstructured test wafers. Main focus of the experiments lies on the plasma treatment (PT) during the TiN deposition and the oxidation/contamination behaviour.

3.1 Design of Experiment

A variety of differently processed and treated wafers were produced during this work. An overview is presented in 3.1, including wafer type (structured/unstructured), deposited layers and post processing treatments. In total 27 wafers were processed with differences in received plasma treatment, storage during vacuum break (clean room atmosphere/N_2 purge box), process order in respect to the CVD W chamber clean (1st/8th wafer after chamber clean), H_2 anneal before the W deposition and substrate layer for the TiN (SiO_2, Si, Al, Si_3N_4).

Table 3.1: Processed wafers. WT...wafer type; SL...substrate layer for TiN; PT...plasma treatment; CRA...clean room atmosphere, PB...purge box; NUC...W nucleation layer only, FULL...full 400 nm W deposition, HALF...200 nm W deposition; 1st/8th...1st or 8th wafer after W chamber clean; *...Two wafers processed; '...Three wafers processed.

Sample	WT	SL	PT	TiN Ageing	W - Layer	1st/8th
1	Blank	Th. SiO_2	YES	-	NUC	1st
2	Blank	Th. SiO_2	YES	-	NUC	8th
3*	Blank	Th. SiO_2	YES	CRA	NUC	-
4'	Blank	Th. SiO_2	YES	PB	-	-
5	Blank	Th. SiO_2	NO	-	NUC	1st
6	Blank	Th. SiO_2	NO	-	NUC	8th
7*	Blank	Th. SiO_2	NO	CRA	NUC	-
8'	Blank	Th. SiO_2	NO	PB	-	-
9	Bulk TSV	CVD SiO_2	YES	-	FULL	-
10	Bulk TSV	CVD SiO_2	NO	-	FULL	-
11	Bulk TSV	CVD SiO_2	YES	CRA	FULL	-
12	Bulk TSV	CVD SiO_2	NO	CRA	FULL	-
13	CMOS Device	CVD SiO_2	NO	-	HALF	-
14	CMOS Device	CVD SiO_2	YES	-	HALF	-
15	Blank	Al	NO	-	NUC (-H_2)	-
16	Blank	Si	YES	-	NUC	-
17	Blank	Si_3N_4	NO	-	NUC	-
18	Blank	CVD SiO_2	YES	-	NUC	-
19	Blank	Th. SiO_2	YES	-	NUC	-
20	Blank	Th. SiO_2	YES	-	NUC	-
21	Blank	Th. SiO_2	YES	-	NUC	-

After processing, the wafers were investigated by various analysis methods. Used methods were sheet resistance measurements, scanning electron microscopy (SEM), transmission electron microscopy (TEM), electron energy loss spectroscopy (EELS) and X-ray photo-electron spectroscopy (XPS). Sheet resistance measurements and SEM were performed inside the clean room/fabrication facility (FAB) at *ams AG*. TEM and EELS were done by the company internal failure analysis department (FA) and the *Austrian Centre for Electron Microscopy and Nanoanalysis FELMI-ZFE* located in Graz. For the XPS measurements, the samples were send to *SGS Institut*

Fresenius GmbH in Dresden. The analysis for each sample can be extracted from table 3.2.

Table 3.2: Sample analysis methods. SR...sheet resistance; SEM...scanning electron microscopy; TEM...transmission electron microscopy; EELS...electron energy loss spectroscopy; XPS...X-ray photo-electron spectroscopy; *...Two wafers processed; '...Three wafers processed.

Sample	SR	SEM	TEM	EELS	XPS
1	-	-	-	-	YES
2	-	-	-	-	YES
3*	YES	-	YES	YES	YES
4'	YES	-	-	-	-
5	-	-	-	-	YES
6	-	-	YES	YES	YES
7*	YES	-	-	-	YES
8'	YES	-	-	-	-
9	-	YES	-	-	-
10	-	YES	-	-	-
11	-	YES	-	-	-
12	-	YES	-	-	-
13	-	YES	YES	YES	-
14	-	YES	YES	YES	-
15	-	-	-	-	YES
16	-	-	-	-	YES
17	-	-	-	-	YES
18	-	-	-	-	YES
19	-	-	-	-	YES
20	-	-	-	-	YES
21	-	-	-	-	YES

Sheet resistance measurements are done to see how the resistance of the differently processed TiN layers behave in different environments (clean room atmosphere, purge box). SEM and TEM images reveal the general condition of the layers (cracks, delaminations, ...), while TEM is mandatory to analyse the few nm thin TiN layer and measure its thickness. In addition to the thickness measurements, the chemical composition can be identified using in-situ EELS. XPS depth profiling gives insight about chemical composition of the layer stack, oxidation state and conditions at the interfaces.

Some failures and defects have been seen predominantly at the wafer edges. Therefore, some samples for SEM, TEM and EELS investigations were taken from the edge (approximately $2-3$ *cm* away from the maximum wafer radius) of the respective samples. For the XPS measurements, only samples from the center of the wafers were investigated.

3.2 Experiment Execution

3.2.1 Starting Material

Depending on the experiment, different wafers were used as starting material. In table 3.1 the starting wafers (WT) are specified. *Blank* means blank, unstructured Si dummy wafers with thermally grown SiO_2 on top. *Bulk TSV* are TSV wafers with SiO_2 layer but without processed CMOS while *CMOS Device* wafers do have fully processed CMOS devices, similar to the standard process flow (fig. 2.1.1). The substrate layer (SL) specifies the layer the CVD TiN was deposited on.

3.2.2 Wafer Processing

For every experiment TiN and W were deposited using CVD systems. The TiN deposition was done in an *Applied Materials Endura® VHP PVD* system, depositing 3 x 5 nm TiN. Depending on the experiment, the deposition was either done with or without a plasma treatment step after each 5 nm TiN deposition cycle. Except for sample 13, no PVD Ti adhesion layer prior to the TiN was deposited. Tool for the PVD Ti is the same as for the TiN, although the deposition is done in a different chamber.

After the TiN deposition, W was deposited in an *Applied Materials Centura® 200 mm* system. Either the full W layer, only half of the layer or just the nucleation layer was deposited. During the W deposition for sample 15, no H_2 anneal before the deposition was performed, for every other sample the anneal step was done.

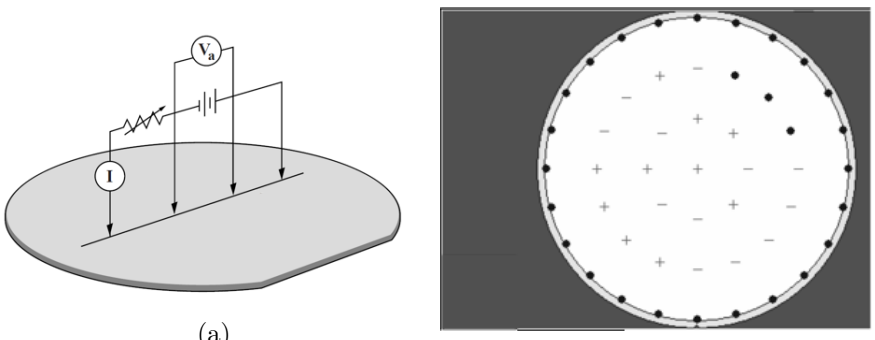
In order to prepare samples for further analysis, after the W deposition a Si_3N_4 passivation layer on samples 13, 14 was deposited while for sample 17 the passivation layer was deposited as substrate layer for the TiN. On

sample wafer 15, a 500 nm aluminium (Al) layer was deposited on top of the thermally grown SiO_2 using an aluminium-copper ($AlCu$) alloy. Samples 13, 14 and 18 got an additional CVD SiO_2 layer (UTEOS, see section 2.1.2). Samples 13 and 14 got the deposition after TSV formation and sample 18 in addition to the thermally grown oxide (th. SiO_2). All depositions were performed in *Applied Materials Centura® 200 mm* systems.

3.2.3 Measurements and Analysis

Sheet Resistance Measurements

For samples 3, 4, 7 and 8, the TiN sheet resistance (R_S) was measured over a period of time. As marked in tables 3.1 and 3.2, samples 3 and 4 as well as 7 and 8 were processed in batches of two (3.1, 3.2; 7.1, 7.2) and three (4.1, 4.2, 4.3; 8.1, 8.2, 8.3) wafers, respectively. The measurements were done on a *KLA-Tencor OmniMap® RS-100 Resistivity Mapping Guide* with a 4-point probe. In total 49 points across the whole wafer were measured. In figure 3.2.1 the measurement circuit and the measured points on the wafers are illustrated.



(a) (b)

Figure 3.2.1: TiN sheet resistance measurement. (a) measurement circuit. (b) measurement points. [27]

At the 4 point probe measurement, a constant current I flows through the outer two points of the 4 needles as shown in figure 3.2.1a. This current induces a voltage (V_a) across the circuit which is measured between the inner

two points. The sheet resistance R_S can then be calculated using *Ohm's Law* and a geometric correction factor [27]:

$$R_S = \left(\frac{\pi}{ln(2)}\right)\frac{V_a}{I} = 4.532\frac{V_a}{I} \tag{3.2.1}$$

If the layer thickness d_{TiN} of the TiN layer is known, also the resistivity ρ_{TiN} of the film can be calculated via:

$$\rho_{TiN} = R_S * d_{TiN} \tag{3.2.2}$$

The measurement tips were made of tungsten, had a radius of $r_{tip} = 40\ \mu m$, a needle spacing of $S = 0.6\ mm$ and a loading of $L = 100\ g$.

In total 10 wafers were investigated with sheet resistance measurements (see tables 3.1 and 3.2). Five wafers with PT TiN (3.1, 3.2, 4.1, 4.2, 4.3) and five wafers with TiN without PT (7.1, 7.2, 8.1, 8.2, 8.3). Two of each of the five wafers were stored in clean room atmosphere (CRA; 3.1, 3.2, 7.1, 7.2) and two were stored in a N_2 purge box (PB; 4.1, 4.2, 8.1, 8.2) for over 300 h, respectively. The measurements were done in small time intervals directly after the TiN deposition and spaced to bigger intervals later on. For the two remaining wafers (4.3, 8.3), only an initial measurement and a measurement after 24 h stored in PB were done, to reduce the PB break and exposure to CRA.

Optical and Scanning Electron Microscopy

Some samples were investigated by optical microscopy and scanning electron microscopy (SEM) inside the wafer fabrication facility (FAB) after processing. The optical microscope used was a *Leica INS3000 DUV Defect Inspection* system.
SEM used for the investigations was a *Applied Materials SEMVISION^{TM} G2 Defect Analysis* system which included a focused ion beam (FIB) [28] system and energy dispersive x-ray spectroscopy (EDX) [29]. Beam settings and parameters were set to be suitable for the respective investigations. Since the measurements were done in the FAB, no additional preparations of the samples were needed.

Transmission Electron Microscopy and Electron Energy Loss Spectroscopy

Samples 3, 6, 13 and 14 were investigated by transmission electron microscopy (TEM) for imaging the samples in nano-scale resolution and electron energy loss spectroscopy (EELS) to gather informations about the chemical compositions. Wafer centre and wafer edge of samples 3 and 6 were investigated by the company internal failure analysis department (FA) using a *JEOL JEM-2800 Transmission Electron Microscope* equipped with a *Gatan* electron energy loss spectrometer. From each, sample 13 and 14, one TSV from the wafer edge was send to the *Austrian Centre for Electron Microscopy and Nanoanalysis FELMI-ZFE* in Graz for TEM and EELS investigations of the top and the bottom side walls inside the TSVs. Tool used was an *FEI Tecnai F20* TEM.
In order to investigate the samples with TEM, they had to be prepared. For the blank wafers 3 and 6, thin lamellas were cut out (FIB cut) from the wafer center and wafer edge, respectively. The TSVs from samples 13 and 14 were pre-prepared at the internal FA and the final lamella preparations were done at *FELMI-ZFE*.

X-Ray Photo-electron Spectroscopy

Samples 1 - 3, 5 - 7 and 15 - 21 were send to *SGS Institut Fresenius GmbH* in Dresden for x-ray photo-electron spectroscopy (XPS) depth profile analysis. The measurements were carried out on a *Physical Electronics PHI Quantera II*. During the XPS depth profile analysis, the layers of the sample stack were analysed by repeated cycles of Ar^+ ion sputtering (removal of material by ion bombardment [30]), followed by a XPS full survey scan to determine the chemical composition of the stack. The expected layer stacks of the analysed samples can be seen in figure 3.2.2:

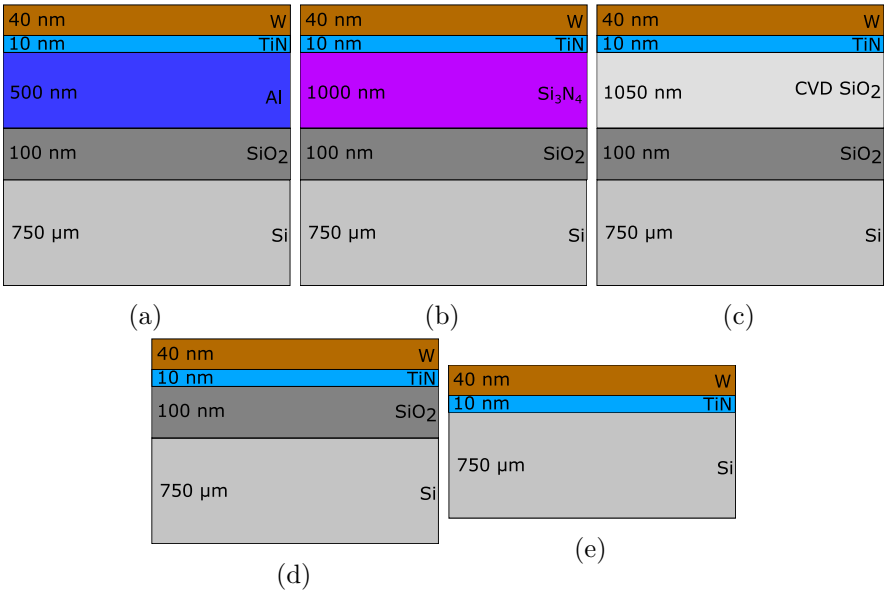


Figure 3.2.2: Layer Stack illustrations of (a) Samples 15 (b) Sample 17 (c) Sample 18 (d) Samples 1-3, 5-7, 19-21 (e) Sample 16

The thickness of the respective layers in each sample stack are approximated. For each sample, only the wafer centres were investigated. The wafers were cleaved into suitable squares and then send to Dresden for analysis.

Chapter 4

Result Evaluation

4.1 Sheet Resistance Measurements

Before splitting the wafers and storing them in clean room atmosphere and the purge box, an initial sheet resistance measurement was done for all wafers. Table 4.1 show the results of the initial measurements.

Table 4.1: Initial sheet resistance measurement. t_D...time after TiN deposition in h; $\overline{R_S}$...mean sheet resistance in $\frac{\Omega}{sq}$

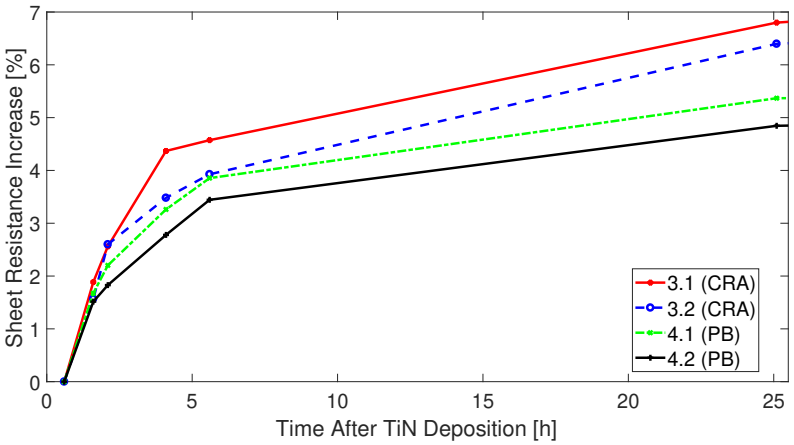
Sample	Storage	t_D $[h]$	$\overline{R_S}$ $[\frac{\Omega}{sq}]$
3.1	CRA	0.6	305.66
3.2	CRA	0.6	307.15
4.1	PB	0.6	300.72
4.2	PB	0.6	306.22
4.3	PB	0.4	242.64
7.1	CRA	1.8	$3.26 \text{x} 10^4$
7.2	CRA	1.8	$3.29 \text{x} 10^4$
8.1	PB	1.8	$2.83 \text{x} 10^4$
8.2	PB	1.8	$3.11 \text{x} 10^4$
8.3	PB	0.4	$2.21 \text{x} 10^4$

One can already see that the CVD TiN samples without PT have an initial sheet resistance about 100x higher compared to the PT TiN wafers. According to equation 2.1.1 a reason for the significantly higher resistance is that the untreated wafers contain C and H contaminations which originate mainly from the TDMAT precursor (see section 2.1.3).

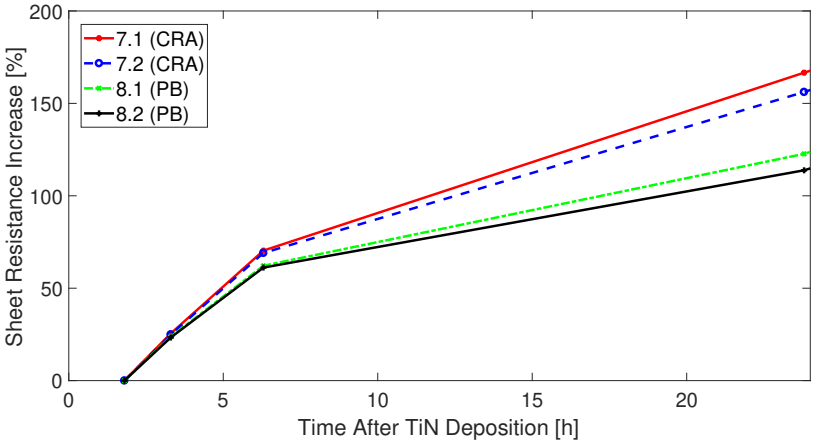
The time between deposition and first measurements (t_D) varies between the different samples. For example the wafers of samples 7.1, 7.2, 8.1, 8.2 had a higher t_D compared to sample 8.3. During this time, all wafers were stored in clean room atmosphere. Consequently, a longer waiting time before the initial R_S measurements resulted in higher initial R_S for identically processed wafers.

After the initial measurements data points were collected with increasing intervals, beginning with a measurement at approximately 0.5 h after the initial values were taken, up to several hours intervals for the last sheet resistance readouts. Figure 4.1.1 show the increase of the mean sheet resistance (average of all 49 measurement points) for samples 3.1, 3.2, 4.1 and 4.2 after 24 h.

The results show that the TiN sheet resistance of wafers stored in a PB increase at a slower rate compared to wafers stored in CRA for PT and no PT wafers, respectively. The environment inside the PB is about 100% N_2 (small concentrations of O and C are possible) while CRA contains 78.08% N_2 and 20.94% O_2 [31]. Thus, O from the atmosphere can be accounted to the difference in sheet resistance increase.
Beside the higher initial resistance, the resistance of samples without PT (fig. 4.1.1b) also increased at a higher rate. For example, after about 24 h, PT wafers (fig. 4.1.1a) show an average R_S increase of 6.6% and 5.1% for CRA and PB stored wafers, respectively, while the wafers without PT showed an average increase of 161.4% and 118.2%. As mentioned in section 2.1.5, the PT increases the density of the TiN film. Consequently, films without PT show lower density and are more susceptible to O and N inclusions from the atmosphere.
The percentage of the difference between CRA and PB stored wafers after 24 h is comparable with 22.6% for samples 3.1, 3.2, 4.1, 4.2 and 26.7% for samples 7.1, 7.2, 8.1, 8.2.



(a) CVD TiN with PT, Samples 3.1, 3.2 and 4.1, 4.2



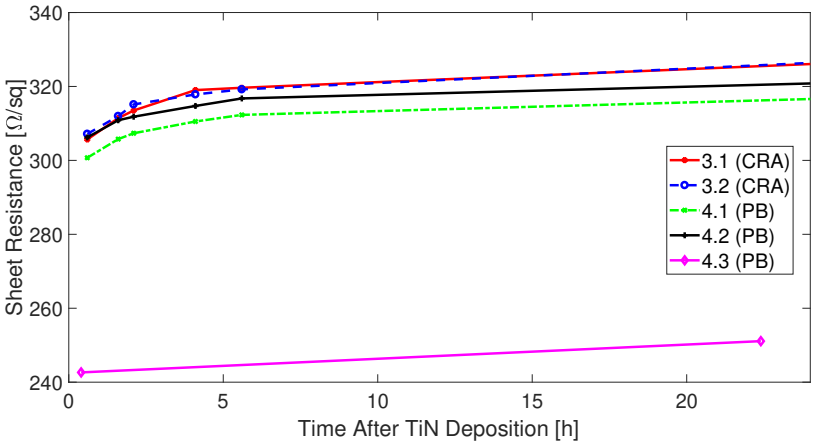
(b) CVD TiN without PT, Samples 7.1, 7.2 and 8.1, 8.2

Figure 4.1.1: Mean sheet resistance increase after 24 h. (a) PT wafers 3.1, 3.2 (CRA) and 4.1, 4.2 (PB). (b) no PT wafers 7.1, 7.2 (CRA) and 8.1, 8.2 (PB).

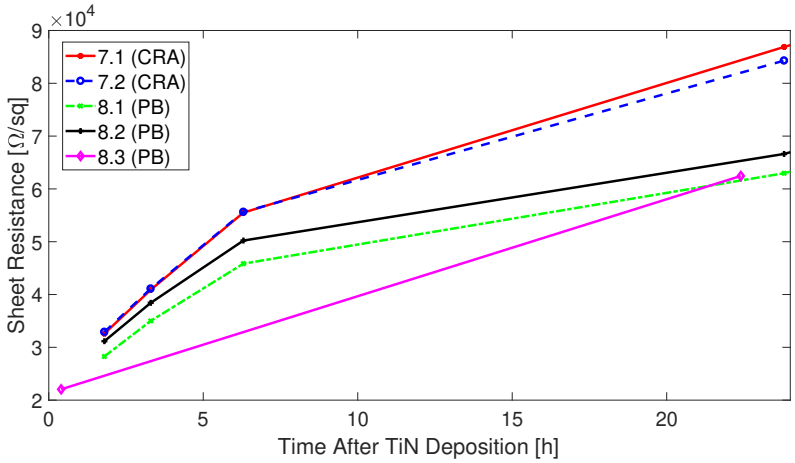
The mean sheet resistance for samples 4.3 and 8.3, where only an initial and a 24 h measurement was done in order to avoid the PB break during the readouts, as well as the results of the other eight samples after 24 h are plotted in figure 4.1.2.

Additionally to the lower initial sheet resistance (see tab. 4.1), due to the shorter queue time before the initial measurement, the results show that for wafer 4.3 (PT, 4.1.2a), the increase in sheet resistance after 24 h is significantly lower compared to the CRA stored wafers (3.1, 3.1) and the PB

stored wafers with PB breaks during the R_S measurements (4.1, 4.2). Wafer 8.3 (no PT, 4.1.2b) exhibits after 24 h a R_S value comparable to the results of the wafers stored in PB (8.1, 8.2), but lower compared to the CRA stored wafers (7.1, 7.2).



(a) CVD TiN with PT, Samples 3.1, 3.2 and 4.1, 4.2, 4.3

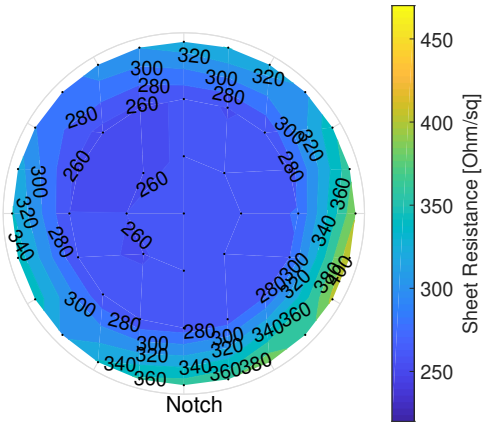


(b) CVD TiN without PT, Samples 7.1, 7.2 and 8.1, 8.2, 8.3

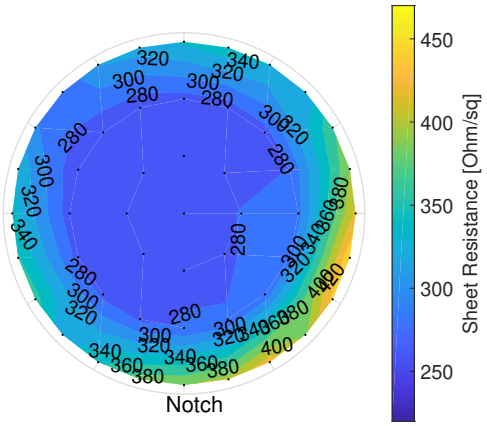
Figure 4.1.2: Mean sheet resistance after 24 h. (a) PT wafers 3.1, 3.2 (CRA) and 4.1, 4.2, 4.3 (PB). (b) no PT wafers 7.1, 7.2 (CRA) and 8.1, 8.2, 8.3 (PB).

From the results in figures 4.1.1 and 4.1.2 it can be conclude that the rate of R_S increase can be lowered using N_2 purge boxes, but not be avoided.

All results presented above refer to the mean sheet resistance of all 49 measured points of each wafers. Figures 4.1.3 and 4.1.4 show the sheet resistance wafer map of samples 3.1 and 7.1 after the initial measurement and after 5 h, respectively. The black dots indicate the points on the wafer where a R_S measurement was performed.

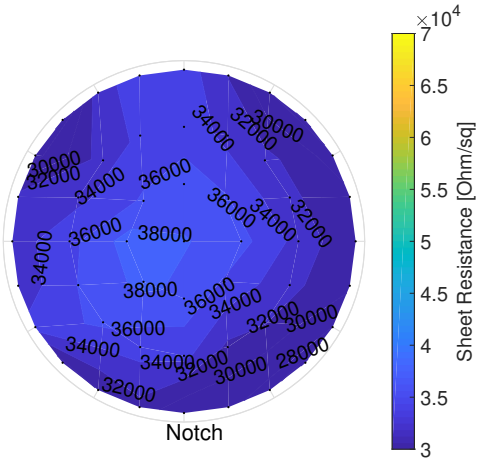


(a) Initial

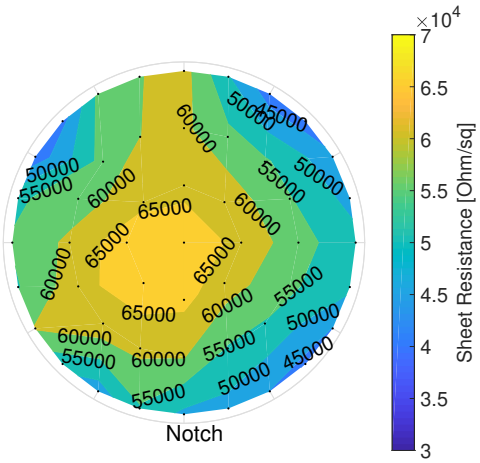


(b) 5 h

Figure 4.1.3: Sample 3.1 (PT) R_S wafer map contour plot. (a) Initial measurement (b) After 5 h in CRA



(a) Initial



(b) 5 h

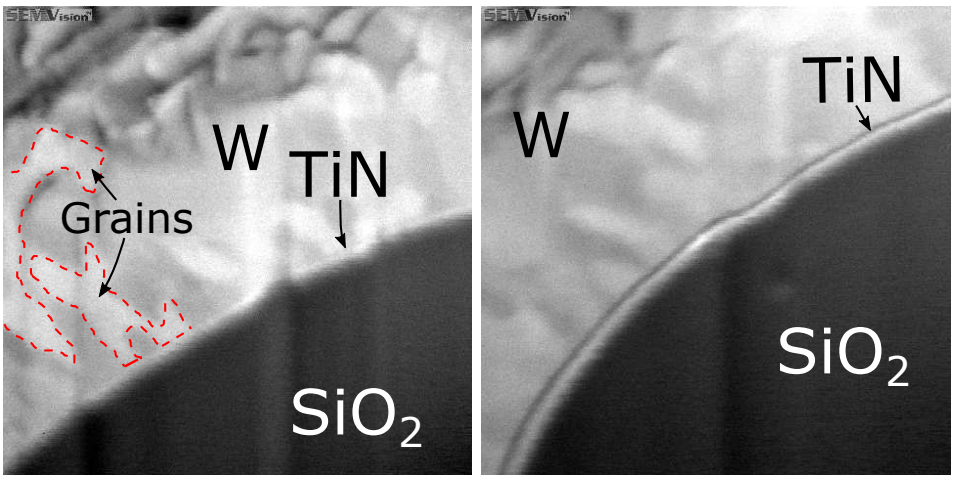
Figure 4.1.4: Sample 7.1 (no PT) R_S wafer map contour plot. (a) Initial measurement (b) After 5 h in CRA

The PT Wafer 3.1 (4.1.3) shows higher resistance at the edges of the wafers while the wafer without PT (4.1.4) exhibit higher R_S in the wafer center. These patterns are also visible for the other PT (3.2, 4.1, 4.2, 4.3) and no PT (7.2, 8.1, 8.2, 8.3) wafers. Variations in the final TiN layer thickness, geometry of the deposition chamber and general chamber conditions during the deposition are influencing the resulting sheet resistance pattern on the wafers.

From the contour plots it is apparent that the rate of R_S increase is comparable for wafer center and edge. For example, the initial measurement of the PT wafer 3.1 (4.1.3a) yielded R_S values of 260 Ω/sq and 360 Ω/sq at the wafer center and near the wafer notch (edge), respectively. After 5 h (4.1.3b) the resistance at the wafer center and near the notch increased to 280 Ω/sq and 380 Ω/sq, respectively. The increase at both areas is 20 Ω/sq. For the untreated wafer (4.1), R_S values of 38000 Ω/sq and 30000 Ω/sq for wafer center and near the notch, after the initial measurement (4.1.4a) and 65000 Ω/sq and 55000 Ω/sq for wafer center and near the notch, after 5 h, were measured. The increases of 27000 Ω/sq at the wafer center and 25000 Ω/sq near the notch are comparable.

4.2 Bulk TSVs

Figure 4.2.1 displays SEM images of TSVs, taken approximately 2 cm from the wafer edges, with FIB - cuts at the top corner of samples 11 and 12 (tab. 3.1), which were stored in CRA for 5 h before the W was deposited.



(a) (b)

Figure 4.2.1: SEM images from the top of bulk TSVs with (a) PT TiN + 400 nm W (sample 11) (b) TiN without PT + 400 nm W (sample 12).

As indicated in the image, the layer stack consists of the bulk W layer on top, the CVD TiN and a SiO_2 layer (dark area) on top of a Si substrate.

With its characteristic grain structure (fig. 4.2.1a, red dashed lines indicate grains and grain boundaries) the W can be identified easily while the dark area below can be assigned to the SiO_2 layer. The line nicely visible in figure 4.2.1b between the W and the SiO_2 is the CVD TiN layer while the bright area between the TiN and the SiO_2 can be assigned to interface effects. The CVD TiN layer can also be seen in figure 4.2.1a, although only very faintly. The difference in visibility of the TiN layers in the two SEM images can be attributed to the difference in densification and thus layer thickness of the PT sample (sample 11) and the untreated sample (sample 12).

After the SEM investigations, samples 9 to 12 received a thermal treatment, where the wafers were heated above 200 °C. During the treatment, the W layer of the samples without plasma treatment (samples 10 and 12) peeled off. In figure 4.2.2a a photograph of a wafer is presented where the W layer is peeling off the surface. The optical microscope image in figure 4.2.2b reveals that the W around the TSVs (black circles) seems to be intact. This could be an indicator that the W inside the TSVs at the top side walls is also intact, possibly due different stress situations of the W in the cylindrical geometry of the TSVs.

(a) (b)

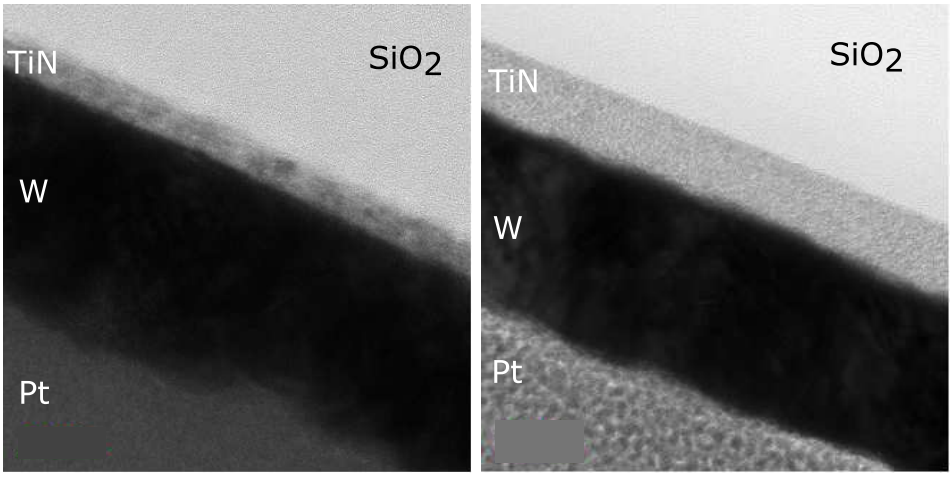
Figure 4.2.2: Bulk TSV wafer with CVD TiN without plasma treatment (sample 12). (a) Wafer as seen after heat treatment (b) microscope view of the wafer

The delamination and peeling of the W was only seen on wafers without PT TiN, which obviously demonstrates that the plasma treatment improves the adhesive properties of the TiN significantly. As mentioned in section 2.1.3, the plasma treatment is densifying the TiN layer and in addition removing/reducing the C and H contaminations improving adhesion.

4.3 TEM and EELS Investigations

4.3.1 Unstructured Wafer Samples

A comparison of a PT CVD TiN (sample 2) layer to an untreated CVD TiN (sample 6) layer by means of TEM imaging is presented in figure 4.3.1. To avoid the W peeling as described in the previous section, only the W nucleation layer (see section 2.1.4) has been deposited. The lamellas for the analysis were taken from the wafer edge. The wafers were processed as 8^{th} wafer after the clean of the W deposition chamber.



(a) Sample 2 (PT) (b) Sample 6 (no PT)

Figure 4.3.1: TEM image of (a) Plasma treated CVD TiN (sample 2) (b) CVD TiN without plasma treatment (sample 6).

Beside the expected layer stack (as in fig. 3.2.2d) also platinum (Pt) used for the lamella preparation on top of the W is visible. From the TEM images one can already see two main differences between the two differently processed TiN films. First of all, the layer which did not receive PT, 4.3.1b, has a

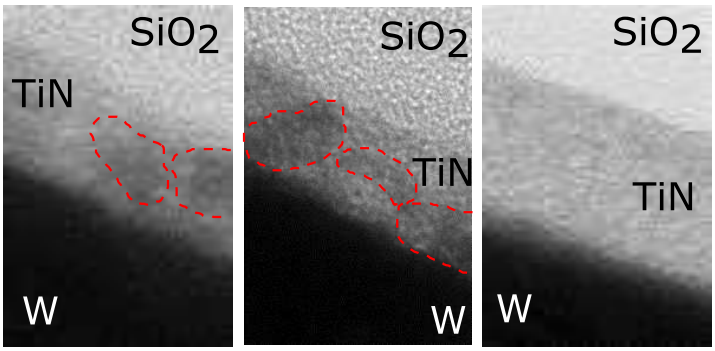
visibly higher film thickness compared to the PT TiN (fig. 4.3.1a). The average thickness at the wafer edge is about 7.5 nm ± 0.3 nm for the PT wafer (sample 2) and 15.9 nm ± 1.1 nm for the sample without PT (sample 6). As mentioned in section 2.1.3, the plasma treatment densifies the TiN and reduces its thickness. The TEM data reveals that the thin film gets reduced to half of its original thickness. In addition to the edges of the wafers, also the wafer centres, a wafer which was processed as 1st wafer after the W chamber clean (sample 1) and a sample which was stored > 100 h in clean room atmosphere before the W deposition (sample 3) were investigated with TEM. The corresponding layer thickness of each TiN layer is summarized in table 4.2.

Table 4.2: Average TiN layer thickness of selected unstructured wafer samples. $\overline{d}_{TiN}$...average TiN layer thickness in nm, σ...standard deviation in nm

Sample	Location	$\overline{d_{TiN}}$ $[nm]$	σ $[nm]$
1	Center	8.3	0.4
1	Edge	7.9	0.5
2	Edge	7.5	0.3
3	Center	7.9	0.9
3	Edge	7.0	0.6
6	Center	15.5	1.4
6	Edge	15.9	1.1

No apparent differences in film thickness between center/edge and 1st/8th wafer after chamber clean were seen. With equation 3.2.2, the resistivity of the TiN film can be calculated, using the mean R_S of the initial sheet resistance measurements of sample 3.1 and sample 7.1 (tab. 4.1) and the thickness information of this section.
For the PT TiN (sample 3.1), a value of $\rho_{3.1} = 227.72$ $\mu\Omega cm$ is calculated. The sample with the lowest vacuum break before the initial R_S measurement (sample 4.3) yields an average resistivity of $\rho_{4.1} = 178.8$ $\mu\Omega cm$. These values are comparable to literature data for thin TiN films but are still a magnitude higher compared to the resistivity of bulk TiN ($\rho_{Bulk} = 30$ $\mu\Omega cm$) [25, 32]. Since the initial sheet resistance of the samples without plasma treatment is two magnitudes higher (tab. 4.1), also the resistivity is two magnitudes higher compared to PT wafers (for example: $\rho_{7.1} = 55400$ $\mu\Omega cm$).

The second visible difference between figures 4.3.1a and 4.3.1b is the solid state of the TiN. The dark spots (indicated by the dashed red lines) in the PT TiN film are nano-crystallized grains with sizes of 2 to 5 nm with different crystal orientations. Close-ups of the TiN layer for samples 2, 3 and 6 are shown in figure 4.3.2.



(a) Sample 2 (b) Sample 3 (c) Sample 6

Figure 4.3.2: TEM image of (a) PT CVD TiN (sample 2) (b) aged PT CVD TiN (sample 3) (c) CVD TiN without PT (sample 6).

The plasma treatment step initializes crystal growth in the amorphous MOCVD deposited $TiN(C,N)$ matrix (see section 2.1.3). The N^+ ions of the plasma penetrate the deposited TiN. Due to exchange reactions the ions replace the loosely bound N of the TDMAT and form strong bonds to the Ti, initialising crystal growth. Thus, the nitrogen in PT CVD TiN primarily originates from the plasma and not the TDMAT [25].

The crystal growth continues as long as there is an amorphous matrix and stops as soon the grains touch each other. The transformation from an amorphous to a poly-crystalline film also explains the big difference in sheet resistance (and resistivity) of the differently treated films (see section 4.1). The final resistivity (electron scattering) of the film is mainly dependent on the grain size, contaminations of oxygen and carbon in the grain boundaries and the residual amorphous matrix [25].

The crystallization of the film also enhances the adhesion properties, since adsorption to a denser, crystalline surface is more favourable than to an amorphous one. This, together with the expected high C concentration could

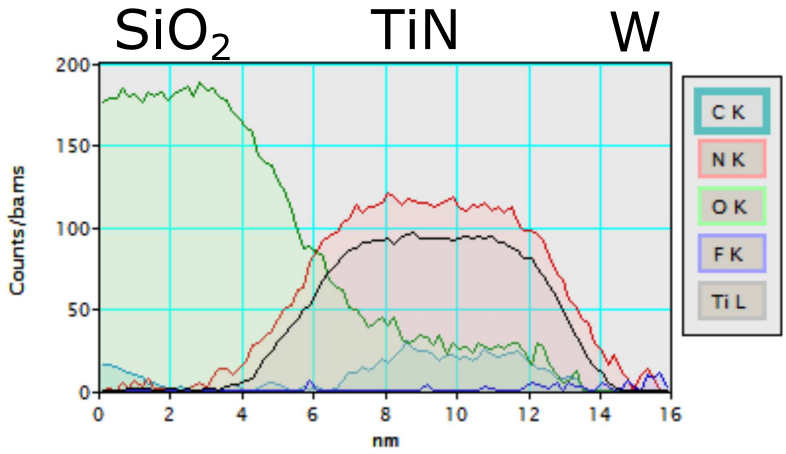
explain the delamination/peeling behaviour of the bulk TSV samples with untreated TiN (see section 4.2).

The results of EELS line scans for samples 2, 3 and 6 are plotted in figure 4.3.3 below. During a line scan, EELS spectra are collected at points along a defined line. The length of this line is outlined on the x-axis of the plots. The line starts in the SiO_2 (first EELS spectrum) and ends in the W (last EEL spectrum) (as indicated in the plot). Each spectrum along the points of the line contains information about the chemical composition at that point. The y-axis outlines the counts of the detected electrons with energies characteristic to the respective elements. Although EELS nicely reveals the chemical composition of the layer stack, quantitative information is more difficult to obtain.

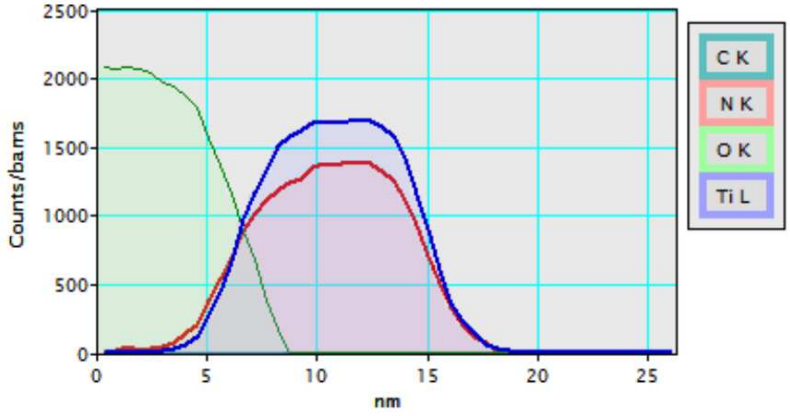
No F or O contaminations inside the TiN layers were found. Also no oxygen due to surface oxidation (see section 2.2.4) at the W side (right side) of the aged TiN sample (figure 4.3.3a) can be seen. It is possible that the O resides along the grain boundaries of the nano-crystals [25] and that the concentration is below the detection limit of the EEL spectrometer.

The C signal in figure 4.3.3c stems primarily from the sample preparation, so that no valid statement about C contamination can be made while the C signal visible in 4.3.3a could indicate residual C from the TDMAT.

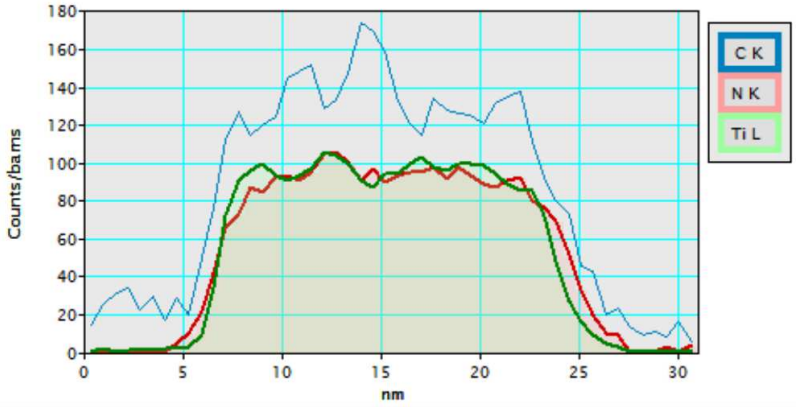
Also the difference in the layer thickness of the TiN between the PT samples (4.3.3a and 4.3.3b) the sample without PT (4.3.3c) is again visible.



(a) Sample 2



(b) Sample 3

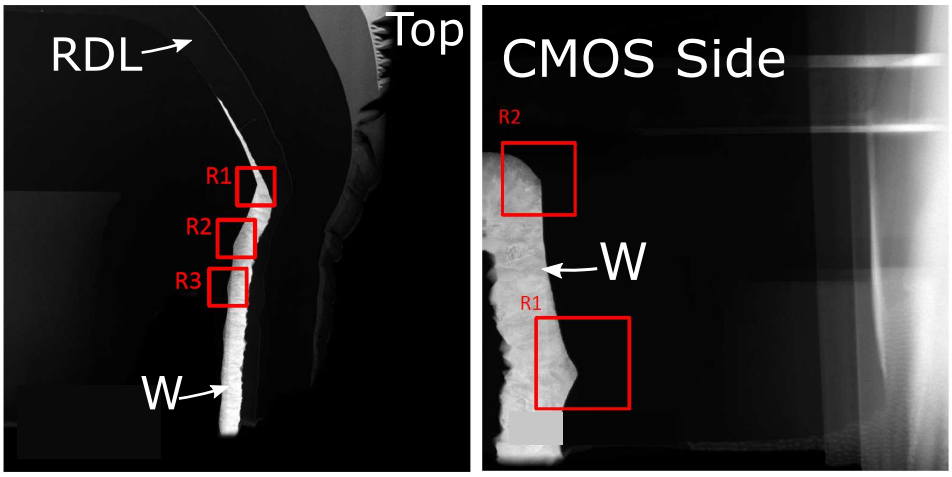


(c) Sample 6

Figure 4.3.3: EELS of samples (a) PT TiN, 8^{th} - wafer (b) PT TiN CRA aged (c) no PT TiN, 8^{th} - wafer

4.3.2 TSV Side Walls

Fully processed TSV samples (CMOS Device) with PVD Ti, plasma treated TiN and full W deposition were investigated via TEM and EELS at *FELMI ZFE*. Top and Bottom (CMOS side) of the side wall of samples from the center and edge of the wafers, were investigated. Figure 4.3.4 displays TEM images of the top (4.3.4a) and bottom (4.3.4b) of the samples from the wafer edge.



(a) Top (b) Bottom

Figure 4.3.4: Cross section TEM of process of record (POR, see chapter 2) TSVs. (a) Top side TSV (see fig. 2.1.3a) (b) Bottom (CMOS side). R1 to R3 indicate areas where EELS and TiN film thickness measurements were done.

The red areas indicate the regions of interest where EELS line scans and TiN thickness measurements were done. Both, the crests and recesses of the scallops at each areas were investigated. Results of the EELS (axes outline the same as in figure 4.3.3) investigations of area R1 from the top sample (4.3.4a) are shown in figure 4.3.5.

The green lines indicate the area where a line scan was performed. The TiN at the top side of the crest (4.3.5a) exhibits metallic Ti at the SiO_2 side, which can be attributed to the the PVD Ti. The TiN thickness on this side is approximately 7 nm, which is comparable to the TiN thickness of the blank samples with plasma treated TiN (see table 4.2). Figure 4.3.5b shows the spectrum right below the crest, at the beginning of the

first recess. Only very little PVD Ti is visible at the SiO_2 side and the TiN thickness of 15 nm is comparable to TiN which did not receive plasma treatment (see table 4.2). Compared to figure 4.3.5a, figure 4.3.5b also contains higher C concentrations and shows indications of F inside the TiN film.

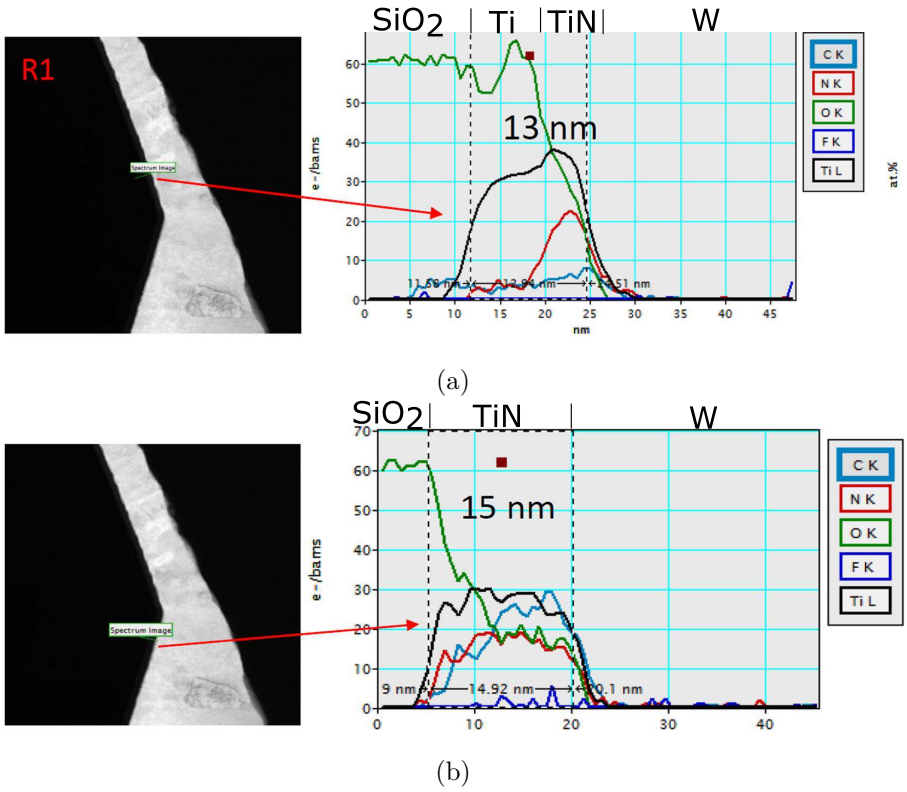


Figure 4.3.5: TEM and EELS spectra of top TSV sample (4.3.4a); area R1 (a) line scan above crest (b) line scan beneath crest

The EELS spectra of the bottom side wall of the sample taken from the wafer edge at area R2, are presented in figure 4.3.6. No metallic Ti is observed and the TiN thickness at around 10 nm is slightly above the values for PT TiN 4.2.

Each of the 4 samples showed similar results: PT TiN with metallic PVD Ti at the SiO_2 side above the first crest. At the top side wall of the TSVs, below the first big crest, thickness measurements of the TiN layers imply that the PT is not effective here. At the bottom side wall no metallic Ti can be found and the TiN thickness seems to be reduced either due to non-conformality of

the CVD TiN deposition, or partial densification from the PT. The average TiN film thickness for all samples can be seen in table 4.3.

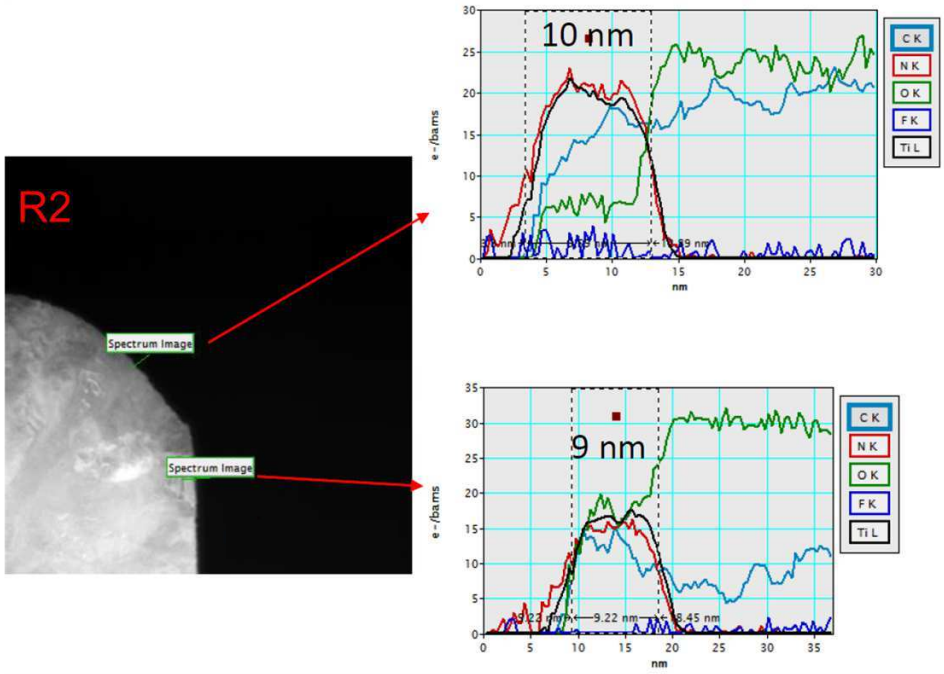


Figure 4.3.6: TEM and EELS spectra of the TSV bottom sample (4.3.4b); area R2

Table 4.3: Average TiN layer thickness inside process of record TSVs. $\overline{d}_{TiN}$...average TiN layer thickness in nm, σ...standard deviation in nm

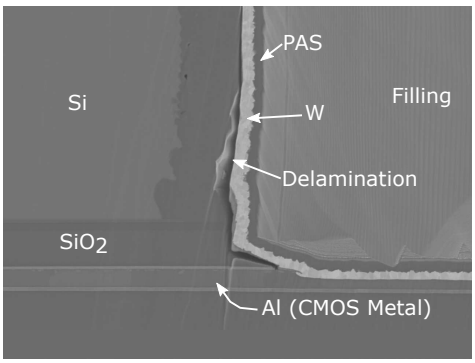
Sample	Location	$\overline{d_{TiN}}$ $[nm]$	σ $[nm]$
Top	Edge	15.7	1.5
Bottom	Edge	10.1	1.2
Top	Center	15.5	1.4
Top	Center	16.6	1.3
Bottom	Center	9.6	1.0

The results confirms that the PVD Ti does not reach the (top and bottom) side walls of the TSV, as mentioned in section 2.1.3, and suggest that the PT is not effective. Consequently, thin, untreated TiN without underlying

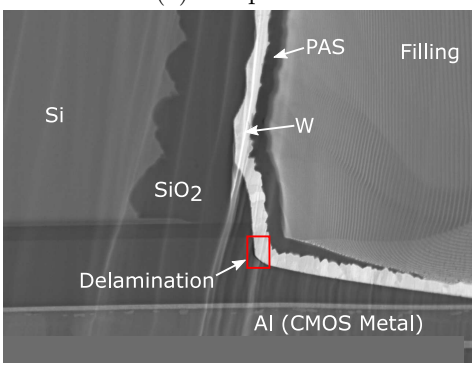
Ti seems to be deposited.

To confirm this, top and bottom side walls of TSVs from the wafer edges of samples 13 (CMOS device, PVD Ti + untreated TiN) and 14 (CMOS device, PT TiN without PVD Ti) were investigated.

As mentioned in section 3.2.3, the samples were pre-prepared at *ams AG* before the lamella preparation and TEM/EELS investigations at *FELMI-ZFE*. Cross section SEM images of the bottom corners (CMOS Side) of TSVs from both samples are presented in figure 4.3.7.



(a) Sample 13



(b) Sample 14

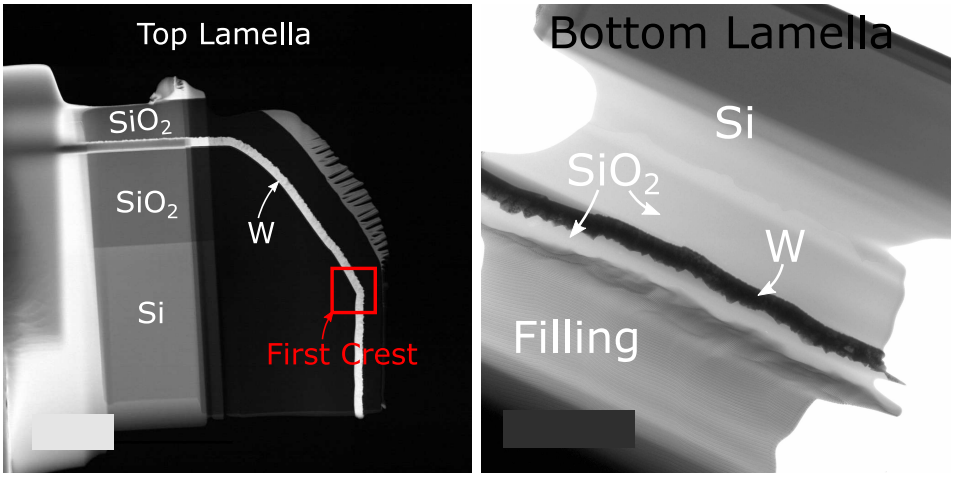
(c) Sample 14, Full

Figure 4.3.7: Cross section SEM image of (a) Bottom Corner (CMOS Side) of sample 13 (b) Bottom Corner (CMOS Side) of sample 14. (c) Cross section of a whole TSV from sample 14.

Both samples show delaminations of the W layer. However, the sample without PT TiN (sample 13; fig. 4.3.7a) clearly shows a higher degree of

delamination compared to the sample with PT TiN (sample 14; fig. 4.3.7b). This once more verifies the enhancement of the adhesion properties due to the plasma.

Figure 4.3.7c displays a full cross section of a TSV from sample 14, indicating the areas (red boxes) where the lamellas for the TEM investigations are prepared from. Since delaminations (voids) are difficult to investigate with TEM due to undesired filling of the voids with contaminations, the lamellas for the investigations were taken from areas where seemingly no delaminations occur. For sample 13, the delaminations reach up to 50 μm, measuring from the bottom of the TSV (as indicated in the figure). For comparability, also the lamellas for sample 14 were prepared from this area (50 μm from bottom) of the respecting TSV. Full overview of the prepared top lamella for sample 13 and bottom lamella for sample 14 are presented in figure 4.3.8.



(a) (b)

Figure 4.3.8: Lamellas for TEM and EELS investigations for samples 13 and 14. (a) Top lamella of sample 13. (b) Bottom side wall (50 μm) Lamella of sample 14.

W, Si and SiO_2 as well as the filling for the bottom lamella are easily distinguishable in the images. For the top lamellas (fig. 4.3.8a) the main region of interest is the first crest and the transition into the TSV and the

beginning of the side wall (red square).

Close up images of the top and bottom lamellas for both samples (13 and 14), as seen in figure 4.3.9, reveal the Ti and TiN layers. The corresponding TiN thickness measurements for the various areas are listed in table 4.4.

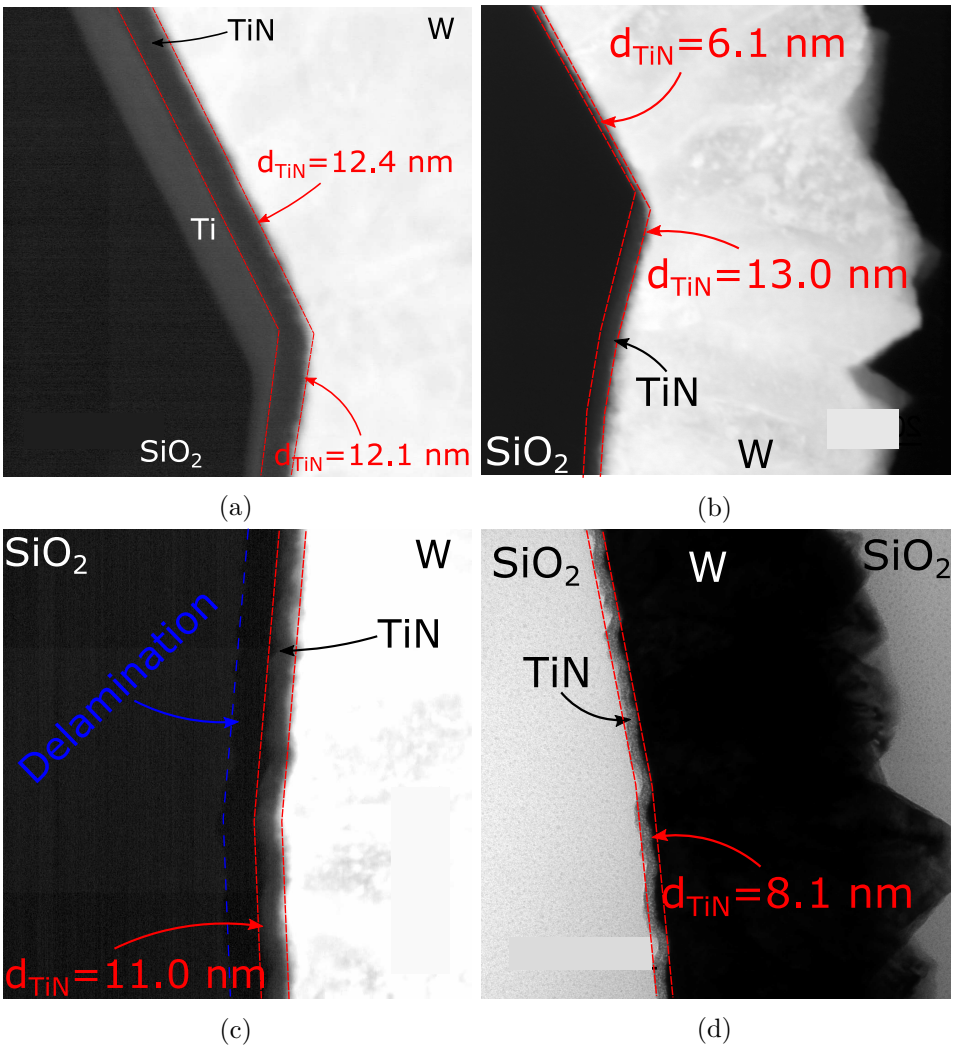


Figure 4.3.9: TEM TiN layer investigation for top and bottom lamellas of sample 13 and 14. (a) Sample 13 top (b) sample 14 top (c) sample 13 bottom side wall (d) sample 14 bottom side wall.

Table 4.4: Average TiN layer thickness inside TSVs of sample 13 (no PT, PVD Ti) and sample 14 (PT, no Ti). Location...location of measurements inside TSV, AC...Above Crest, BC...Below Crest; $\overline{d}_{TiN}$...average TiN layer thickness in nm, σ...standard deviation in nm

Sample	Location	$\overline{d_{TiN}}$ $[nm]$	σ $[nm]$
13	Top (AC)	12.4	0.5
13	Top (BC)	12.2	0.7
13	Bottom	11.0	1.4
14	Top (AC)	6.1	0.8
14	Top (BC)	13.0	0.9
14	Bottom	8.1	1.0

The TiN layer is highlighted by the dashed red lines for every sample. Figures 4.3.9a and 4.3.9b nicely show the difference of the TiN layer between the sample without PT (sample 13) and the sample with PT (sample 14). The TiN layer thickness for sample 13 does not change after the first big crest, reaching the vertical side wall of the TSV, while sample 14 shows the same behaviour as the samples seen figure 4.3.5. The TiN before the first crest has half the thickness (6.1 nm) of the TiN below the first crest (13.0 nm tab. 4.4, fig. 4.3.9b).
Beside the TiN, also the PVD Ti can be seen for sample 13 (fig. 4.3.9a, bright layer between TiN and SiO_2). However, in contrast to the PT TiN of sample 14 the Ti thickness is reduced significantly from 17.4 $nm \pm$ 0.6 nm to 8.1 $nm \pm 0.7$ nm when reaching the vertical side wall of the TSV as a consequence of the bad step coverage of PVD processes in HAR structures.

As already seen in figure 4.3.7, the bottom sample without PT TiN (fig. 4.3.9c) shows severe delaminations (between the blue and red dashed line). Obviously, the delaminations develops at the SiO_2/TiN interface and the TiN/W stack appears fully intact. Also no more PVD Ti can found, similar to fig. 4.3.6.
The TiN thickness of sample 13 is reduced by about 10% (11.0 nm) compared to the layer thickness at the top, which suggests a total step coverage of approximately 87% throughout the whole TSV. Sample 14 exhibits a TiN layer thickness slightly thinner (8.1 nm) compared to the sample without PT, indicating densification. However, as seen from the TEM images and

thickness measurements of unstructured samples (fig. 4.3.1, tab. 4.2), where the PT is completely effective, the layer thickness of the PT TiN film is densified to half of its original deposited thickness. Consequently, a TiN layer thickness of 5 nm to 6 nm at the bottom side wall would be expected if the densification was fully effective here.

For the bottom side wall lamella of sample 14 also a fast fourier transformation (FFT) analysis at a point of the TiN was performed. The corresponding result of the FFT measurement is depicted in figure 4.3.10. The sharp bright spots seen in the pattern indicate crystal structure of the TiN with a calculated lattice constance of approximately 0.19 nm, which is close to the lattice constant of TiN in the (200) plane ($a_{200} = 0.21$ nm [33]) which does have the lowest surface energy [34]. As revealed in figure 4.3.2, PT TiN forms nano-crystals with different orientations while untreated TiN has an amorphous nature. Consequently, the FFT measurements suggest that the TiN film at the bottom side walls is affected by the PT.

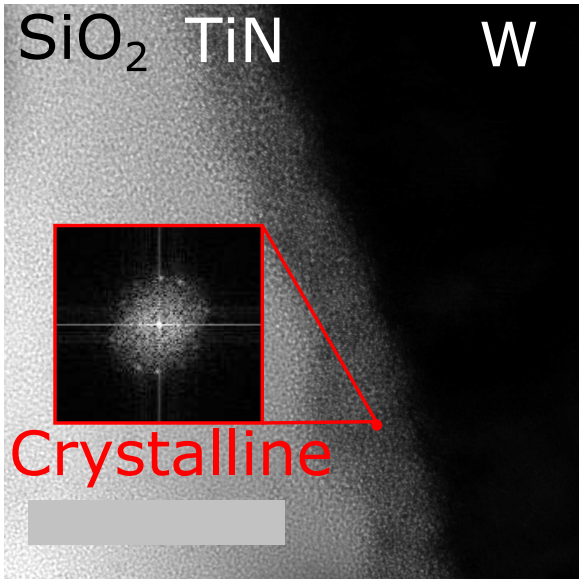


Figure 4.3.10: TEM image and FFT image of TiN layer for the bottom side wall sample of sample 14

In summary: The TiN is not affected at all at the Top side walls of the TSVs partial densification can be observed at the bottom side walls. This partial

densification can still contain residual contaminations in form of C and H from the TDMAT and could also have a negative effect on the diffusion barrier properties of the thin film.

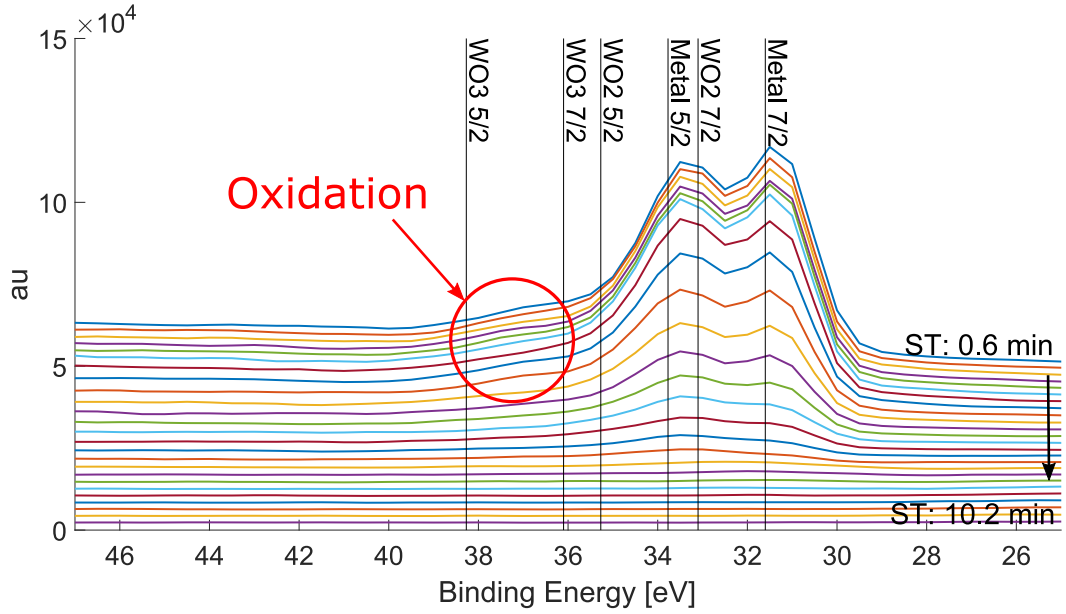
4.4 XPS Depth Profile Analysis

Figure 4.4.1 shows the XPS spectra of tungsten W4f region (electrons from the f-orbital of the N-Shell) and titanium Ti2p region (electrons from the p-orbital of the L-shell) of sample 1 (PT, 1st wafer after chamber clean; see table 3.1) after every sputter cycle. ST denotes the sputter time, where each sputter cycle took 0.2 minutes, starting from 0 minutes (first sputter cycle starting at the W side, see figure 3.2.2) to 10 minutes (last sputter cycle, stopping in Si). The black arrows indicates the sputter direction (from W to Si). The horizontal lines show binding energies of known compositions. 7/2, 5/2 and 3/2, 1/2 denote total angular momentum j of the components of W and Ti due to spin-orbit splitting. The spin-orbit splitting is due to the interaction between the spin angular momentum ($s = \pm 1/2$) and the orbital angular momentum (l; p $\rightarrow l = 1$, f $\rightarrow l = 3$) with $j = l + s$. This leads to a split into two energy levels (for example Ti2p: $l = 1,\ s = \pm\frac{1}{2} \rightarrow j = l + s = \frac{1}{2}\ (s = -\frac{1}{2}),\ \frac{3}{2}\ (s = +\frac{1}{2}))$ [35].

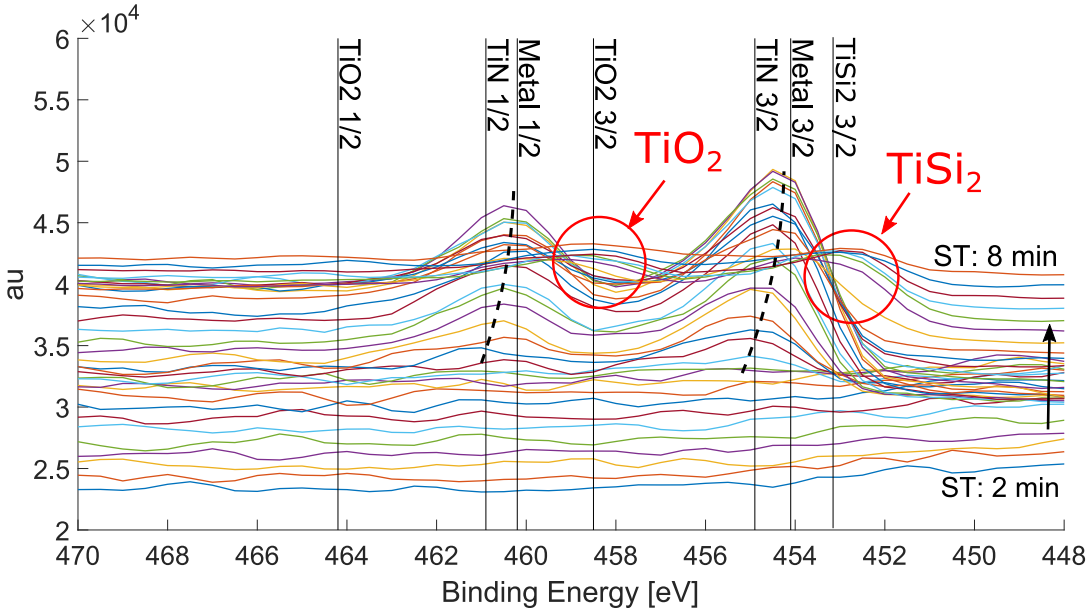
The $W4f$ spectra (4.4.1a) nicely show the W metal peaks (31.6 eV and 33.8 eV [36]). The small shoulder at the higher binding energy side (red circle, around 38 eV, near WO_3), and the overlap of the metal 5/2 and WO_2 7/2 peak, indicate oxidation of the W on the surface area. Thus W is present in form of metal, WO_2 and/or WO_3.

As seen in the $Ti2p$ spectra (4.4.1b), Ti is mostly present as nitride (TiN, 454.9 eV and 460.9 eV [37]). At higher sputter cycles, reaching the interface to the SiO_2, the energies of the detected electrons shift to lower binding energies (black dashed line), indicating interface reactions. At the interface to the SiO_2 (near 8 min of ST) two new peaks appear. The peak around 458.2 eV could be attributed to TiO_2 [37] and the one at 453.2 eV suggests the presence of titanium silicide ($TiSi_2$) [38], indicating a mixture of TiO_2

and $TiSi_2$ at the TiN / SiO_2 interface.



(a) W4f



(b) Ti2p

Figure 4.4.1: Sample 1: XPS Spectra for each sputter cycle of the (a) W4f (b) Ti2p signal

Peaks in XPS spectra can not be assigned to a specific binding energy but have an uncertainty which can cause overlaps of different peaks and make it difficult to distinguish peaks. In table 4.5, selected Ti2p peaks and their uncertainties are listed.

Table 4.5: Ti2p XPS peaks of selected titanium compounds. $\overline{BE}$...mean binding energy in eV; σ...standard deviation in eV

Compound	$\overline{BE}$ $[eV]$	σ $[eV]$	Ref.
Ti	453.9	0.3	[39]
TiN	455.1	0.3	[40]
TiO_2	458.7	0.2	[39]
$TiSi$	353.3	0.4	[40]

A small peak at the TiN / SiO_2 in the Si2p spectra shown in figure 4.4.2 also indicates the pesence of $TiSi_2$. Beside the prominent Si (99.1 eV) and SiO_2 (103.5 eV) peaks [41], also a small peak close to 98.3 eV, right before the SiO_2 peak starts (TiN / SiO_2 interface), is visible, which could be assigned to the $TiSi_2$ [38].

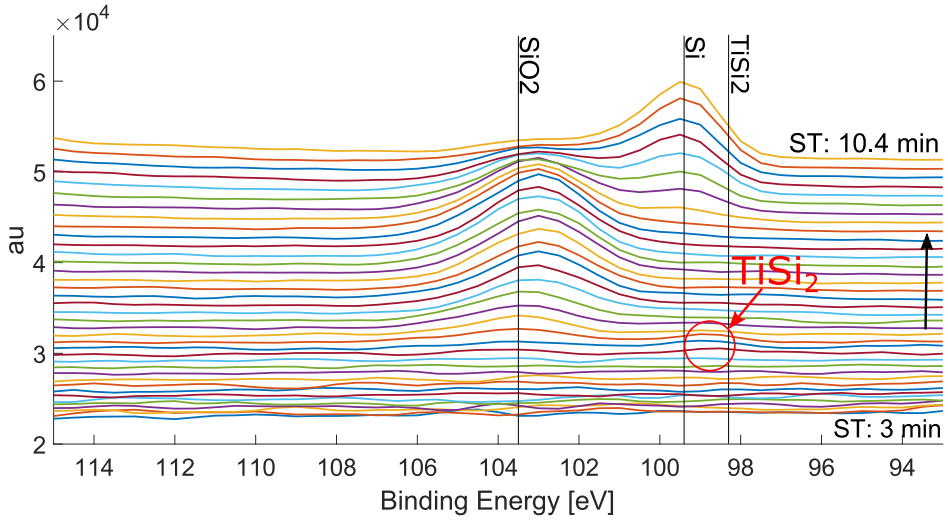


Figure 4.4.2: Sample 1: XPS Spectra for each sputter cycle of the Si2p

The respective depth profile analysis for sample 1 is plotted in figure 4.4.3. Due to roughness and scattering effects the signals do smear together.

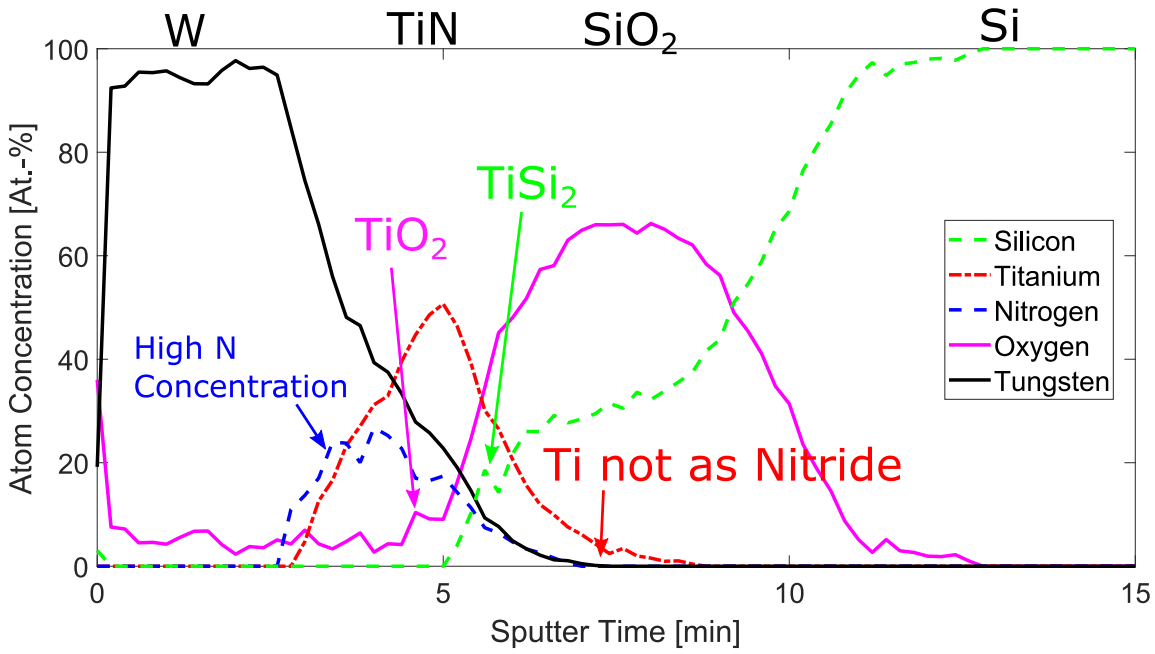
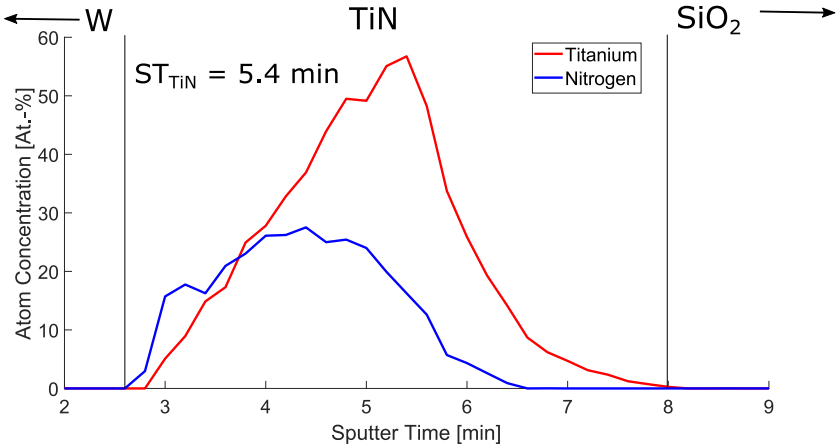


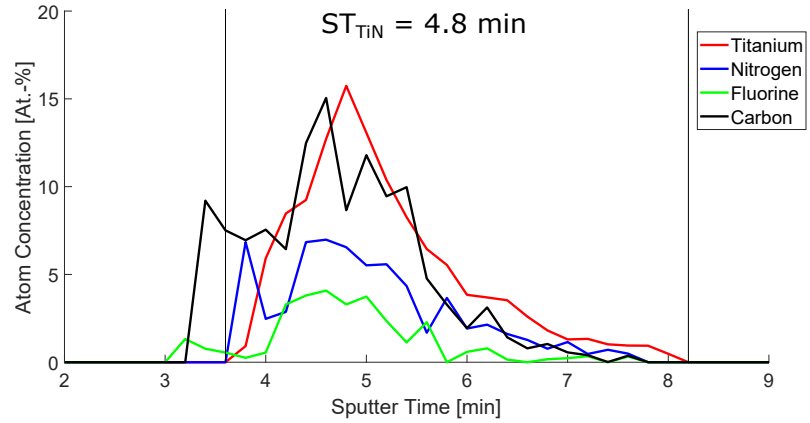
Figure 4.4.3: Sample 1: XPS depth profile

In the profile, a higher nitrogen content is detected at the W / TiN interface and, as seen in figure 4.4.1b, at the SiO_2 interface, Ti appears not as nitride. The small spikes of Si and O at the TiN / SiO_2 interface could indicate $TiSi_2$ and TiO_2, respectively. The W and SiO_2 layers are the same for all samples, so only the TiN will be discussed in more detail.

Figure 4.4.4 shows the depth profiles from the TiN layer of sample 2 (PT, 8^{th} after chamber clean) and sample 6 (no PT, 8^{th} wafer after chamber clean).



(a) Sample 2



(b) Sample 6

Figure 4.4.4: Sample 1: XPS depth profile of (a) plasma treated TiN, 8$^{\text{th}}$ wafer (b) un-treated, 8$^{\text{th}}$ wafer

Beside the higher N concentration at the W interface and the N free Ti components at the SiO_2 interface in both samples, one can see that the untreated sample (4.4.4b) has high concentrations of carbon and fluorine inside the TiN layer. These contaminations can also be seen for the other untreated samples, 5 and 7. The PT samples (1, 2 and 3) do not exhibit any signs of C or F contamination.

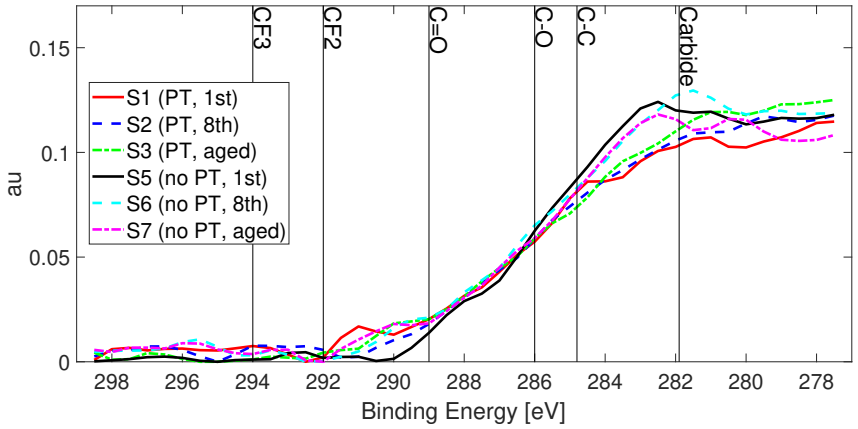
The C contamination mainly results from the TiN deposition as explained in section 2.1.3. TDMAT is used as precursor and according to equation 2.1.1, TiN layers with high amounts of loosely bound C remains in the

untreated amorphous TiN film. However, during the plasma treatment with the H/N-plasma, H^+ ions enter the TiN film and react with the C, forming volatile hydrocarbons like methane (CH_4) and ethane (C_2H_6), reducing the C contamination inside the thin layer [25]. Consequently, no or very low amounts of C remain in the PT TiN.

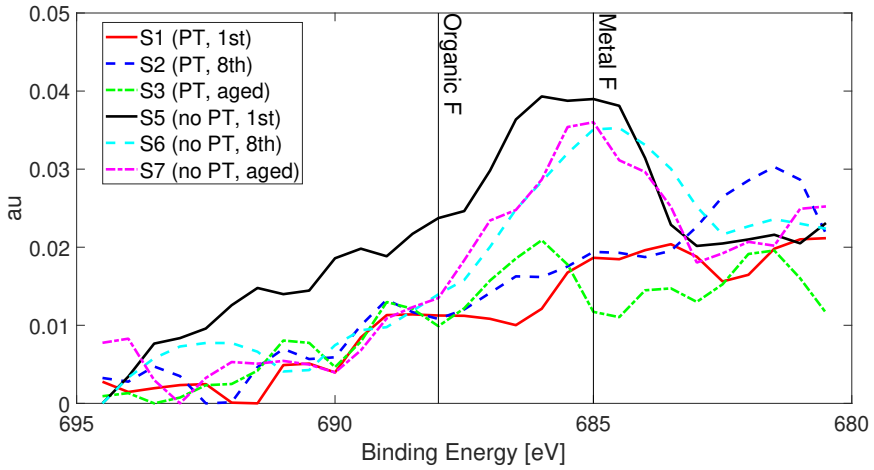
On the other hand, the F contamination mainly originates from the WF_6 precursor gas used for the W deposition (see section 2.1.4) but also contaminations due to remaining F radicals from the W chamber clean (NF_3), which can reside at ceramic parts inside the deposition chamber, are possible. As found in section 4.3, PT TiN consists, contrary to amorphous untreated TiN, of nano-crystalline grains, which enhance the barrier properties against WF_6 and F diffusion. Consequently no F can be found in the PT TiN.

The TEM investigations have proven that layer thickness of $\approx 15\ nm$ for untreated TiN is significantly higher as found for the PT TiN ($\approx 8\ nm$). Though as seen in the plots, the time it takes to get through the TiN (ST_{TiN}) is comparable for both samples. This may also be explained by weaker bonding of the Ti to the N due to the amorphous nature of the untreated TiN and the additional contaminating elements as described above, which results in a higher sputter rate compared to the denser, crystalline PT TiN.

In order to improve the signal to noise ratio in the C1s and F1s core level region, a mean spectrum for both areas has been calculated by averaging all spectra for each sputter cycle. The corresponding spectra of the C1s and F1s region for each sample can be extracted from figures 4.4.5a and 4.4.5b.



(a) C1s



(b) F1s

Figure 4.4.5: Mean spectra over all sputter cycles of samples 1 to 3 and 5 to 7 for the (a) $C1s$ (b) $F1s$ signals

Obviously the untreated samples (5, 6 and 7) show carbon (4.4.5a, around 283 eV) and fluorine (4.4.5b, 685 eV) signals, while the treated samples (1, 2 and 3) do not show any signs of these contaminations. Carbon is predominantly found as inorganic carbide (TiC, 281.9 eV) inside the TiN film. Fluorine is found to be metallic (685 eV), indicating possible TiF_x formation. As mentioned in section 2.2.2, the formation of TiF_x leads to fails and delaminations of the metallization layers. This effect usually occurs when WF_6 diffuses through the TiN in the underlying Ti (or TiO_2) layer. However, the XPS data of the CVD TiN films evidently show a mixture of

metallic Ti, TiO_2, $TiSi_2$ at the TiN / SiO_2. Consequently, the formation of TiF_x can also occur when no Ti is deposited underneath the CVD TiN, as it is the case inside TSVs as shown in section 4.3.

In the F1s spectra in figure 4.4.5b, sample 5 shows a slightly higher F concentration compared to samples 6 and 7. Sample 5 was processed as 1st wafer after the NF_3 chamber clean (W deposition). It is expected that directly after the chamber clean, the F contamination inside the chamber is high and that 1st wafers after the clean are exposed to a higher F concentration.

Beside for C1s and F1s also mean spectra for the Ti2p region of samples 15 to 21 (see tab. 3.1) are plotted in figure 4.4.6. The peaks for TiN can be seen in all samples and TiO_2 and metallic $Ti/TiSi_2$ peaks for samples 18, 19, 20 and 21 are detectable (red circles). However, these peaks are not visible for samples 15, 16 and 17. The difference between these two batches of samples is the substrate layer for the TiN. TiN layers for Samples 18 to 21 were deposited on SiO_2 while for samples 15 (TiN on Al), 16 (TiN on Si) and 17 (TiN on Si_3N_4) the substrate layer did not contain O. This observation could suggest that the formation of TiO_2 and $TiSi_2$ a SiO_2 or at least a O containing substrate is needed.

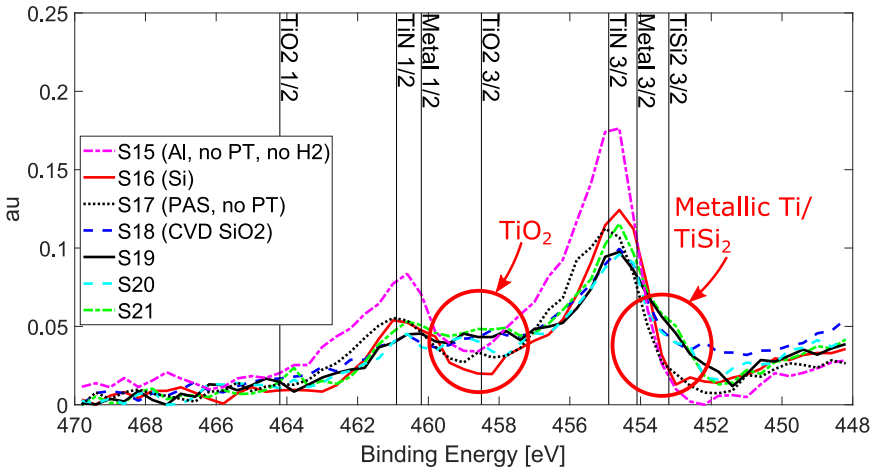
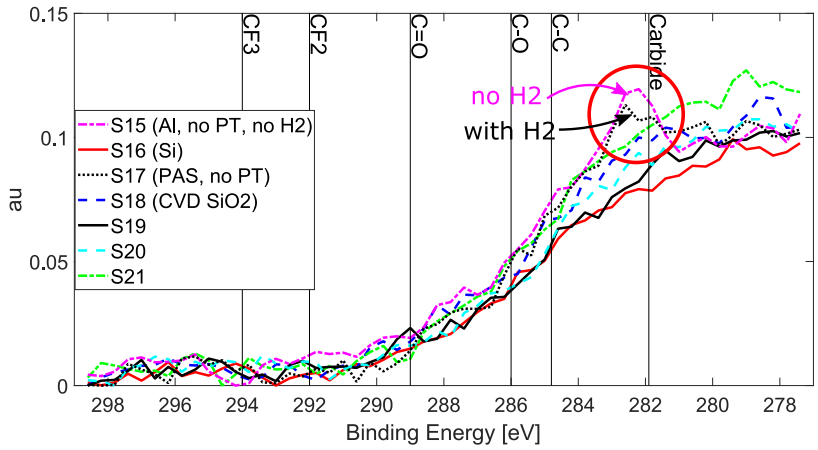
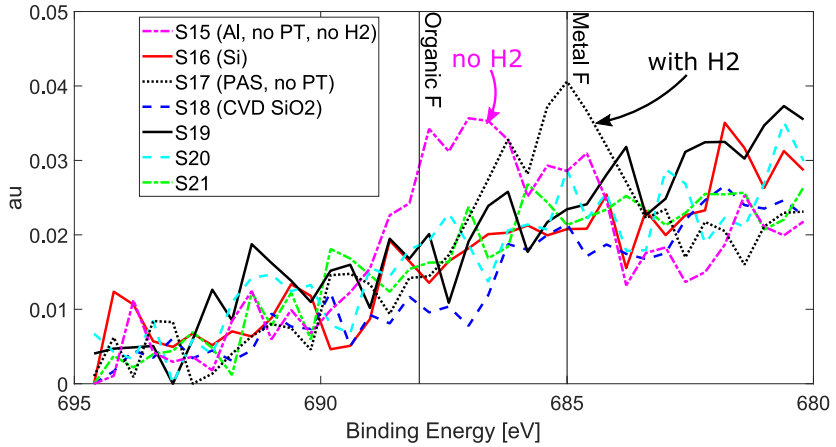


Figure 4.4.6: Ti2p Mean Spectra for samples 15 to 21

The C1s and F1s mean spectra of samples 15 to 21, plotted in figure 4.4.7, once again show C and F contaminations for samples without PT (samples 15 and 17).



(a) C1s



(b) F1s

Figure 4.4.7: Mean spectra over all sputter cycles of samples 15 to 21 for the (a) $C1s$ (b) $F1s$ signals

C (fig. 4.4.7a) is again primarily bound as carbide. For sample 15 no H_2 anneal step prior to the W nucleation deposition was performed. The higher C concentration in sample 15 compared to sample 17 (red circle) could indicate that the $H2$ anneal slightly reduces the C contamination at the TiN surface, which possibly enhances the adhesion to the following W.

The F (fig. 4.4.7b) spectra show differences in binding energies for sample 15 and 17. Sample 17 exhibits predominately metallic F (TiF_x or WF_6) while sample 17 contains a high peak at higher binding energies together with a smaller peak near the metallic F binding energy. The peak at around 687 eV could be assigned to organic F although also $F-O$ and $F-F$ bonds can be assigned to this binding energy [42]. Subsequently this could suggest that the H_2 anneal prior to the W deposition somehow impacts the formation of organic F during the W deposition.

On samples which were stored in clean room atmosphere for over 100 h (samples 3 and 7), one would expect to find oxygen at lower binding energies corresponding to metal oxides at the W / TiN interface (see section 2.2.4). Interestingly, no O signal was found in this area of any sample. As an example, the $O1s$ spectra for sample 7 are shown in figure 4.4.8. Although the long ageing time of the sample and the clearly measurable increase in the sheet resistance (see section 4.1), no other signal can be seen beside the peaks corresponding to the SiO_2 (532.9 eV). It is possible that the O concentration on the surface and/or inside the layers is too low to be detected but enough to increase the resistance of the thin film.

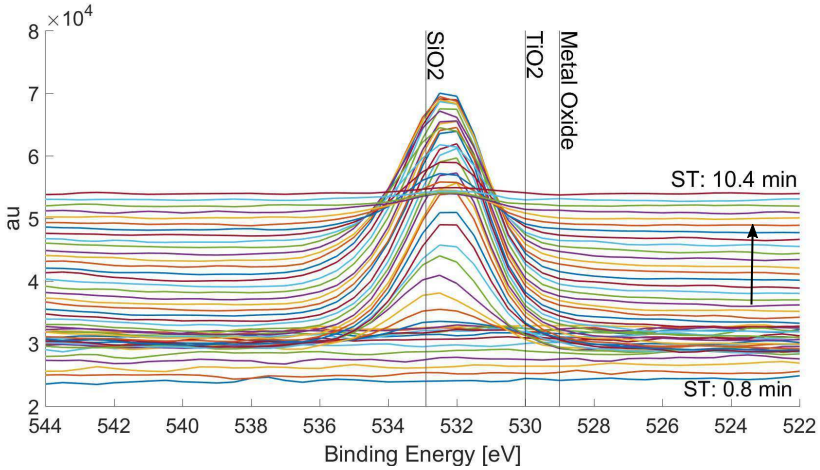


Figure 4.4.8: Sample 7: XPS O1s signal

Chapter 5

Summary and Discussion

5.1 Summary and Discussion

Wafers with CVD TiN with differences in received plasma treatment, storage before W deposition, H_2 anneal before W deposition, substrate layer and wafer structure were processed (tab. 3.1) and investigated by means of SEM, TEM, EELS, XPS and 4-point sheet resistance measurements (tab. 3.2).

Table 4.1 and figures 4.1.1, 4.1.3 and 4.1.4 in section 4.1 show that the sheet resistance of PT CVD TiN shortly after the deposition is approximately two magnitudes (100x) lower compared to CVD TiN which has not received PT. According to equation 2.1.1, untreated TiN contains high concentrations of C from the TDMAT precursor, which was also confirmed by XPS measurements as presented in figures 4.4.4b, 4.4.5 and 4.4.7. PT also involves densification to about half of the original deposited thickness and crystallization of the TiN film as shown in figures 4.3.1, 4.3.2 and in table 4.2. Thus, PT CVD TiN contains nano-crystalline grains with different crystal orientations while untreated CVD TiN is an amorphous, less dense, C contaminated film, which gives rise to the significant difference in sheet resistance. The final sheet resistance/resistivity of the PT CVD TiN is dependent on the size of the nano-crystalline grains, number of grain boundaries and residual amorphous matrix.

Beside the higher initial sheet resistance, figures 4.1.2, 4.1.3 and 4.1.4 also show that the rate in sheet resistance increase is higher for untreated TiN

(70% after 5 h) compared to PT TiN (5% after 5 h). Additionally, wafers stored in N_2 atmosphere increase at a lower rate. For dense crystalline PT TiN, O can only diffuse through the grain boundaries between the nano-crystalline grains. The O at the grain boundaries create new scattering sites for electrons and therefore increase the resistance. For untreated TiN, O can diffuse throughout the whole film into the less dense film, increasing the resistance more quickly.
Storing wafers after the TiN deposition in a N_2 purge box can slow down the sheet resistance increase but not avoid it, as seen in figures 4.1.1 and 4.1.2, indicating that not only O but also N can be accounted to the increase of the sheet resistance.

Thermal treatment of TSV wafers with PT TiN (fig. 4.2.1a) and no PT TiN (4.2.1b) including 400 nm bulk W on top resulted in delamination/peeling of the W from the samples with untreated TiN. Images of these delaminations are presented in figure 4.2.2. W around and at the top side wall of the TSVs (4.2.2b) seems to be intact, which could be due different stress situations near at and in the TSV structures.

XPS depth profile analysis as plotted in figures 4.4.1b, 4.4.2 and 4.4.3 revealed TiO_2 as well as metallic Ti and/or $TiSi_2$ at the TiN / SiO_2 interface. Figure 4.4.6 shows that this components only occur when CVD TiN is deposited on SiO_2. Reactions between TiN and SiO_2 at the interface could lead to this mixture of differently bound Ti.
N seems to be shifted to the W / TiN interface as seen in figures 4.4.3 and 4.4.4. Exposure to atmosphere and/or rearrangements of the N inside the TiN layer could be possible explanations.

Figures 4.4.4b, 4.4.5 and 4.4.7 nicely show C and F contaminations in untreated CVD TiN. C stems from the CVD TiN precursor TDMAT while F can be assigned to the WF_6 precursor the W deposition. However, figure 4.4.5b reveals higher F concentrations for the wafer which was processed as 1^{st} wafer after the W chamber clean with NF_3 at the W deposition compared to the wafer processed as 8^{th} after the clean. Consequently this would suggest that right after the W chamber clean the concentration of residual F from the cleaning agents, which can reside at ceramic parts inside the deposition

chamber, is high, resulting in higher F contaminations inside the TiN.
The peak positions for C as seen in 4.4.5a and 4.4.7a indicate that C is bound as carbide. A H_2 anneal prior to the W deposition seems to slightly reduce the C contaminations (4.4.7a) possibly by reducing the surface contaminations, which ultimately also would enhance the adhesion properties. The F peaks as seen in figures 4.4.5b and 4.4.7b can be assigned to metallic F in form of TiF_x and/or WF_6. Figure 4.4.7b shows a shift to higher binding energies for the sample which was processed without H_2 anneal before the W deposition. This shift indicates that beside metallic F also organic F or $F-F$ and $F-O$ components are present, which could be due to surface contaminations which can react with F before diffusing into the TiN.

Samples with CVD TiN which were stored in clean room atmosphere for several hours before the W deposition did not exhibit high O concentrations at the W / TiN interface as revealed by EELS (4.3.3b) and XPS (4.4.8), despite the clearly measurable increase in sheet resistance. One possible explanation could be that the resulting O contamination due to air exposure is below the detection limit for the detectors but still high enough to increase the sheet resistance.

Figure 4.3.7 shows that inside TSVs delaminations of W from the side walls occur starting from the bottom (CMOS side) of the TSVs for PT as wells as no PT TiN samples. However, the untreated sample (fig. 4.3.7a) exhibits a significantly higher degree of delamination compared to the PT TiN sample,(fig. 4.3.7b) which evidently shows again the better adhesion properties of PT TiN and also reveals that the PT does affect the side walls inside TSVs.

Thickness measurements from TEM and EELS investigations of top and bottom side walls of PT TiN and no PT TiN samples as presented in figures 4.3.4a, 4.3.4b, 4.3.5, 4.3.6 and 4.3.9 as well as tables 4.3 and 4.4 evidently show that the PT only fully affects the TiN before the vertical side walls of the TSVs and that the TiN right below the first crest is not affected by the PT at all. However, further down in the TSV at the side walls the TiN seem to be crystalline and thus affected by the plasma as shown by the FFT seen in figure 4.3.10. Anyhow, comparison of TiN film thickness of PT and no PT TiN (tab. 4.4) show that the PT TiN is not half the thickness of

the untreated TiN and consequently not fully densified. This could leave less dense areas or paths in the TiN where F can diffuse through into the underlying layers.

Figures 4.3.5 and 4.3.9a together with figures 4.3.6 and 4.3.9c clearly show that the PVD Ti, which works as adhesion layer, is only deposited at the top side walls and does not reach the side walls deeper in the TSVs at all as a result of the bad step coverage of the PVD process for HAR trenches. The volcano effect explained in section 2.2.2 refers to WF_6 diffusion through the CVD TiN into the PVD Ti or TiO_2 forming TiF_x (see eq. 2.2.1 and 2.2.3). Interestingly, the volcano effect (delamination/cracks) occurs predominantly at the bottom side walls, where CVD TiN lies on top of SiO_2. However, at the top side walls of the TSVs where the TiN has still PVD Ti as underlying layer and the TiN is not affected by the PT at all, no volcano effect can be observed.
A possible explanation could be the higher layer thickness of the untreated CVD TiN at the top of the TSVs compared to the film thickness of the partially densified TiN at bottom side wall (tab. 4.4). More F can diffuse through the less dense parts of the thinner TiN at the bottom side walls reacting with the metallic Ti or TiO_2 which forms at the TiN / SiO_2 interface creating TiF_x and resulting in the volcano effect which ultimately leads to delaminations, cracks and complete electric failures.

Chapter 6

Conclusion

6.1 Conclusion

Full effectiveness of the H_2/N_2 - plasma treatment during the deposition of the CVD TiN contact liner and diffusion barrier in TSVs is a crucial process and does determine functionality and quality of the final TSVs.

Removal of C by the H_2 component of the plasma and induced crystallization by the N_2 component as wells as densification of the film to about half its original deposited thickness results in reduction of sheet resistance of about two magnitudes, a significantly lower degradation of sheet resistance at atmosphere, enhanced adhesion properties and an improvement of the barrier properties against F diffusion. Storing wafers after the TiN deposition before the W deposition in a N_2 atmosphere also contributes to slower sheet resistance degradation, which could prolong the maximum vacuum break time.

Thickness measurements during TEM investigations of the TiN layer on unstructured wafers and inside TSVs let suggest that the TiN is not affected by the plasma treatment at the top side walls of the TSVs and only partially affected at the bottom side walls. Because the side walls are not fully affected, the TiN films at these areas are not fully densified, have high resistivity which increases heavily during the exposure at atmosphere before the W deposition, contain C and less dense areas. Consequently, this leads to worse adhesion properties and the possibility of F containing materials like WF_6

diffusing through the TiN into the underlying layers where F can react with metallic Ti and TiO_2 which forms at the TiN SiO_2 interface leading to formation of TiF_x and volcano defects. Increasing the time and/or bias during the plasma treatment could help to fully densify the TiN layers.

Higher TiN layer thickness could be the reason why no delaminations/volcano effect can be seen at the top side walls where PVD Ti is still present. Consequently, increasing the total deposited thickness of the TiN, could also prevent F to diffuse through the TiN at the bottom side walls.

List of Figures

List of Tables

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