Monolithic Ultra-Low Power Solar Harvester with High Dynamic MPPT Algorithm

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Abstract

Energy harvesting can enhance economical and ecological issues of systems, for example by supporting battery lifetime. Thinking about autonomously operating sensor systems, energy harvesting can even enable such devices to become self-sustaining. The higher the level of integration gets, the lower the production steps and cost becomes. Therefore, a real advantage of energy harvesting would be a self sustaining wireless sensor node that leaves the FAB fully functional. A reduction of the bill of materials would have been achieved which could outperform battery powered systems.

Carried out in the Cooperative Research and Exploration Department of the Infineon Design Center Graz and the University of Technology Institute of Electronics, this work was done by myself covering literature study, development of comparable concepts, design for test in chip layout and schematic, and dissemination to the scientific community. Driven by the above mentioned motivation, the proof of concept for a monolithic energy harvesting chip was set to be the research focus. Due to the relatively high power density of light and the fact that a p-n junction will produce photo-current, a solar harvesting chip was developed. Following the idea of being competitive to a battery, the energy harvesting test chips are produced in a standard 130 nm single n-well CMOS process. No additional or special masks are necessary. At the beginning of this work, the feasibility of the CMOS process to form a sufficiently working solar cell was analyzed. Due to the absence of products requiring monolithic harvesting approaches, the number of publications regarding on-chip solar cells was relatively small and still is. Considering the most important publications on this topic, a test chip serving only for empirical observations on solar cells was designed, see chapter 2.3. A functional solar cell structure was found and results have been published to the community, which also concluded the first requirement for the proof of concept. Knowing the characteristics and the restrictions of the CMOS process regarding the solar cell, a concept for an on-chip DC/DC converter was developed. Scientific publications on highly efficient monolithic DC/DC converters have been adapted to meet the ultra-low power requirements. Regarding the charge pump, the main research contribution to the development of ultra-low power designs is the capacitor driver circuit, which combines level shifting and parasitic charge recycling at a minimum design overhead, see chapter 4.2. The DC/DC converter is further continuously operated by an ultra-low power maximum power point tracking algorithm (MPPTA) which was also developed, published and patented within this work. The novelty disseminated to the community covers the concept, circuit and adoption of the perturbation and observation (P&O) approach to meet ultra-low power demands of monolithic designs.

The final test-chip is a monolithic solar energy harvester chip that contains solar cells, a DC/DC converter and a maximum power point tracking algorithm. Regarding the solar cell, a fill factor (FF) of 78 % is achieved which is comparable to State-of-the-Art (SOTA). An output voltage of 4.2 V is generated at a minimum input power of 0.65 µW, which is lower than the data reported recently in this field of research. The maximum output power is determined by the solar cell area and ranges up to 40 µW/mm^2 under natural light conditions. The concept of the tracking algorithm is based on analytic findings regarding the solar

cells and the charge pump. The analytic analysis is published to the scientific community and points out, that the popular fraction of the open circuit voltage (FOC) MPPTA has considerable disadvantages for monolithic solar harvesters. A concept and implementation of an autonomously operating harvesting systems for ultra-low power devices was developed, which differs from SOTA implementations. It is shown, that SOTA concepts are not suited for monolithic ultra-low power harvesting systems and that the developed design can improve the overall efficiency.

Kurzfassung

Energy Harvesting kann elektronische Systeme sowohl wirtschaftlicher als auch ökologischer machen, wenn beispielsweise deren Batterielaufzeit verlängert wird. Speziell bei autonom arbeitenden Sensorsystemen kann durch Harvesting ein energieautarker Zustand erreicht werden. Dabei gilt, wie bei den meisten Systemen, dass mit fortschreitender Integration sowohl die Produktionsschritte als auch die Produktionskosten sinken. Im Idealfall würde das Sensorsystem als Ein-Chip Lösung inklusive Energy Harvesting und Energiespeicher die Produktion verlassen. Die Bill-of-Materials wäre so gering, dass der Sensorknoten trotz größerer Chipfläche zu einem herkömmlichen Batterie betriebenen System konkurrenzfähig sein könnte.

Die Arbeit wurde in der „Cooperative Research and Exploration“ Abteilung des Infineon Design Centers Graz sowie an der Technischen Universität Graz am Institut für Elektronik durchgeführt. Im Zuge der Arbeit habe ich Literaturstudie betrieben, sowie die Entwicklung von vergleich- und testbaren Konzepten für monolithische Harvester auf Basis der vorhandenen wissenschaftlichen Literatur erarbeitet. Die Konzepte wurden vom mir analytisch untersucht, schaltungstechnisch sowie in Chiplayout umgesetzt und der Scientific Community durch Veröffentlichungen zugänglich gemacht. Getrieben durch die oben genannte Motivation wurde der wissenschaftliche Fokus dieser Arbeit auf die Machbarkeit eines vollständig integrierten autonomen Harvesting Systems gesetzt. Aufgrund der hohen Leistungsdichte im Vergleich zu anderen Energiequellen und wegen der Eigenschaft von P-N Übergängen Fotostrom zu erzeugen, wurde beschlossen einen vollständig in Silizium integrieren Solar Harvester zu bauen. Um eine konkurrenzfähige Alternative zu den etablierten mit Batterie betriebenen Sensorknoten zu bieten, wurde ein günstiger 130 nm single n-well standard CMOS Prozess verwendet. Es wurden keine zusätzlichen Masken oder spezielle Prozessschritte verwendet. Zu Beginn dieser Arbeit wurde untersucht, ob mit den zuvor genannten Voraussetzungen eine on-Chip Solarzelle hergestellt werden kann und wie hoch die erzielbare Leistungsdichte ist. Da im Bereich von monolithischen Solar Harvestern noch keine nennenswerte Anforderung durch Anwendungen vorhanden ist, gab und gibt es noch vergleichbar wenige wissenschaftliche Veröffentlichungen zu diesem Thema. Unter Rücksichtnahme der jüngsten Veröffentlichungen über on-Chip Solar Zellen habe ich diese Arbeit damit begonnen einen Testchip zu designen, der ausschließlich Solarzell-Strukturen beinhaltet. Die Strukturen sind so ausgelegt, dass die beschriebenen Effekte aus der Literatur nachvollzogen werden können sowie vergleichbar zu einem Referenzsystem veröffentlicht werden können. Auf Basis der gewonnen Messdaten des Solar-Testchip wurde eine funktionierende Zellen-Geometrie empirisch ermittelt. Die elektrischen Eigenschaften dieser Solarzelle führten dann zu dem weiteren Konzept des DC/DC Konverters. Wissenschaftliche Veröffentlichungen zum Thema hocheffiziente monolithische DC/DC Konverter wurden an die ultra-low Power Anforderungen adaptiert. Die Ladungspumpe betreffend waren die wesentlichen wissenschaftlichen Beiträge das Konzept sowie das Design der Treiber. Es wurde eine Treiber-Schaltung entwickelt, die Level-Shifting sowie Ladungsrecycling aus parasitären Kondensatoren mit minimalem Schaltungsaufwand umsetzt und damit für ultra-low Power Anwendungen mit on-Chip Solar Zellen zugänglich macht. Der Betrieb der Ladungspumpe wird dabei durch einen kontinuierlich arbeitenden ulra-low power Maximum Power Point Tracking Algorithmus geregelt. Der Tracking Algorithmus wurde

ebenfalls im Zuge dieser Arbeit entwickelt und ist durch ein Patent geschützt. Die publizierte Neuheit des perturbation and observation (P&O) Ansatz lieg wiederum in der ultra-low Power Umsetzung, welche für einen monolithischen Harvester notwendig ist.

Der finale Prototypen-Testchip ist ein monolithischer Harvester der neben den on-Chip Solarzellen einen DC/DC Konverter und einen Maximum Power Point Tracking Algorithmus integriert hat. Die Solarzellen haben einen Fill Factor von 78 % was ein vergleichbares Resultat zu State-of-the-Art Zellen darstellt. Die maximale Ausgangsspannung von 4.2 V wird bereits ab einer Eingangsleistung von 0.65 µW erzeugt. Die maximale Ausgangsleistung wird durch die Größe der Solarfläche bestimmt und erreicht bei hellem Tageslicht bis zu 40 µW/mm². Der Tracking Algorithmus und der DC/DC Konverter sind nach den gewonnen Erkenntnissen aus einer analytischen Untersuchung konzipiert und implementiert. Erkenntnisse aus der analytischen Untersuchung zum Thema Maximum Power Point Tracking in monolithischen Systemen wurden der wissenschaftlichen Community zur Verfügung gestellt und zeigen sehr deutlich, dass der populäre fraction of the open circuit voltage (FOC) maximum power point tracking algorithm (MPPTA) in diesem Zusammenhang entscheidende Nachteile besitzt. Auf Grund des ultra-low Power Designs unterscheidet sich die gesamte Implementierung deutlich von State-of-the-Art Systemen.

Acknowledgments

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Special thank also goes to Dipl.-Ing. Gerald Holweg who is the lead manager of the pre-development team Cooperative Research and Exploration (CRE) at the Infineon Design Center Graz (DCGR). Gerald always encouraged me to bring my ideas to silicon. Without his support many opportunities to work on research topics would not exist at the DCGR.

I also want to thank my colleagues from the CRE. Some of you I know for many years now. I always enjoyed the good discussions on important and sometimes less important topics and I highly appreciate the funny and respectful company. As every one of you is open-minded and an expert in her or his field of research, CRE creates an environment in which we all benefit from each other. I hope this atmosphere can be held up for others joining future CRE.

∞ patience is a virtue ∞

Christoph Steffan

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Acronyms

f_{MPP}	frequency at maximum power point
CCO	current controlled oscillator
CP	collection probability
CP	charge pump
DCR	design rule check
DSP	digital signal processor
DUT	device under test
ECR	electrical rule check
FAB	semiconductor fabrication plant
FF	fill factor
FOC	fraction of the open circuit voltage
FOM	figure of merit
IDAC	current output digital to analog converter
IOT	Internet of Things
LVS	layout versus schematic check
MEMS	micro-electro-mechanical systems
MPP	maximum power point
MPPT	maximum power point tracking
MPPTA	maximum power point tracking algorithm
NIR	near infrared
NMOS	N-channel metal–oxide–semiconductor field-effect transistor
NPLC	number of power line cycles

P&O	perturbation and observation
PCM	process control monitoring
PMOS	P-channel metal–oxide–semiconductor field-effect transistor
PSub	p-doped substrate
PWM	pulsewidth modulation
RMS	root mean square
SoI	silicon on isolator
SOTA	State-of-the-Art
STI	shallow trench isolation
T&H	track and hold
UV	ultra violet
WSN	wireless sensor node

Chapter 1

Introduction

At beginning of this chapter the motivation for building a monolithic solar harvesting chip is given. Other power source besides solar irradiance are listed and pros/cons are shortly discussed. The most important scientific publications for this work in the fields of research about ultra-low power harvesting and maximum power point tracking are introduced. Further the results of this work are presented in an overview. The overview gives an impression on how the work started with the research question about the feasibility of a monolithic all-CMOS harvesting chip. At the end of the introduction chapter the achieved performance of the latest harvester test-chip is presented. ■

1.1 Motivation

The motivation for energy harvesting is to enhance the lifetime of an electronic system which is not connected to the power grid and therefore has to supply itself. Under best case conditions the life time of such a system is not determined by the supply but by other degradation. By expanding the lifetime, these power grid independent systems can add more value to their economic viability. A prominent application example is structural health monitoring where stress and strain is often a parameter of interest which can be measured by a wireless sensor node (WSN). An example of a WSN strain gauge is shown in Fig. 1.1. Due to its size, this type of health monitoring can make use of a battery which lasts for about one decade [1]. The relatively long lifetime of such systems is typically achieved by short active modes followed by long idle or deep-sleep. As a result the achievable sampling rate decreases with lifetime.

While large scale WSN can make use of batteries which can last for one decade, an application driven miniaturization of a WSN is typically not able to achieve this lifetime. Some applications, for example implantable sensor systems, require small dimensions compared to environmental or structural monitoring. The reduced size consequently reduces the available energy, because the energy density of a battery stays almost constant. On the other side, the load current requirement on the battery is not changing when miniaturized. Writing or reading a controllers memory, operation of the sensor/transducer, or transmitting/receiving data at a certain data rate requires the very same amount of energy, regardless of the WSNs size. As a consequence the recharging of the energy storage becomes more interesting

Figure 1.1: Wireless strain gauge from Resensys [1] mounted on a bridge.

for highly miniaturized systems. Meaning, that the economic benefit of energy harvesting systems for hand-held size WSNs is questionable if the system can operate for one decade.

Another aspect, however, that should not be overseen here, is the ecologic idea of increased battery life even for hand-held sized low power systems. One example of a very popular battery powered system is the TV remote control. Only to change the TV channels in Portuguese households, 23 million batteries are required every year. (*This Information was provided within the guest lecture "Energy-Efficient Future Wireless Communications" held by Professor Nuno Borges Carvalho, from University of Aveiro, Portugal, at the Technical University of Graz in the year 2017.*). The need for batteries will dramatically increase when following the ideas of the Internet of Things (IOT), where WSNs determine a major part of the IOT environment. Although early expectations regarding the number of communication nodes within the IOT have not been met and scaled back [2], the power supply of autonomously operating nodes is still a challenge. Miniaturized systems can benefit the most from energy harvesting, because of the before mentioned scaling of energy density of the storage device. The highest level of miniaturization is achieved if the WSN is integrated as system in package or even monolithic. Therefore this work focuses on the feasibility of energy harvesting at the highest possible level of integration. As a starting point the different power sources are compared. In Table 1.1 solar, thermal, ambient RF, and piezoelectric sources are listed. When focusing on miniaturization the achievable power density of the transducer that converts the incoming energy into electrical energy is the most important value. As table 1.1 depicts, the solar cell outperforms all other sources by orders of magnitude. Meaning, that the monolithic integration of a typically sized silicon chip, which contains a solar cell, is a feasible solution to achieve real energy autarky. It should also be mentioned that depending on the application also piezoelectric cantilever beams can be integrated as micro-electro-mechanical systems (MEMS) structures. The amount of converted power however is yet not able to compete with a silicon solar cell.

Table 1.1: Comparison of different power sources [3]

	Solar Energy	**Thermal Energy**	**Ambient RF Energy**	**Piezoelectric Energy**	
				Vibration	Push Button
Power Density	100 mW/cm²	60 µW/cm²	0.2 nW/cm² - 1 µW/cm²	200 µW/cm³	50 µJ/N
Output	0.5 V Si cell 1.0 V a-Si cell	-	3-4 V (open circuit)	10-25 V	100-10000 V
Available Time	Day time (4-8 h)	Continuous	Continuous	Activity dependent	Activity dependent
Weight	5-10 g	10-20 g	2-3 g	2-10 g	1-2 g
Pros	Large amount of energy Well developed tech.	Always available	Antenna can be integrated onto frame Widely available		Well developed tech. Light weight Small volume
Cons	Need large area Non-continuous Orientation issue	Need large area Low power Rigid and brittle	Distance dependent Depending on available power source	Need large area Highly variable output	Low conversion efficiency Highly variable output

1.2 State of the Art

This work can be split into two main parts, which are the on-chip solar cells and the on-chip energy harvesting. The on-chip solar cells as a part of a monolithic harvester are not very common yet. Therefore a state of the art overview of the most important publications is given in chapter 2.3.1, where the results of this work are directly compared to other publications.

Energy harvesting, however, is a topic that has been published more often. Also the idea of building a monolithic solar harvester has been presented before by Lee et al. [4] SSC 2013, or by Kanago et al.[5] 2012, unfortunately no further description about the solar cell and its performance has been made in both publications. Ayazian et al. [6] BCAS 2012, and Guilar et al. [7] VLSI 2009, have both presented a monolithic sensor platform and a solar cell in CMOS, respectively. Both focus on solar performance and do not have a DC/DC converter. Their demo applications are directly powered by the solar cell voltage (approx. 500 mV). Another important work about highly integrated solar harvesters is published by Chen et al. ISSCC [8] ISSCC 2011. They presented a sensor platform in a stacked chip design, that comprises also a fully integrated charge pump which generates 3.6 V. These before mentioned publications are described in more detail at the end of this work in the comparison section 5.1, because they are the most important publications regarding the system design. Their achieved performances regarding the solar operation and the harvesting part are compared to the achieved results of this work. It should also be mentioned that no commercial monolithic solar harvester chip exists at the time this work is written (to the best knowledge of the author). Commercially available harvesting chips are on the market, however they need at least two orders of magnitude more power to perform startup than designs [9, 10, 11,

12, 13] which have been presented at technical research conferences recently. Regarding efficiencies of the power conversion or the tracking efficiency of their maximum power point tracking algorithm (MPPTA)s, commercial product chips are an important measure and therefore also shortly described as well as compared to this work in the comparison section 5.1.

Another important field of research is the MPPTA. Liu et al. [14] (cited by 60, April 2018) describe a perturbation and observation technique to find the maximum power point (MPP). The basic idea of the perturbation and observation (P&O) technique is to change a setting of the converter, in this case the DC/DC converter, and to observe the response of the system. By having the information about the perturbation, which was intentionally induced by the MPPTA, the observation tells the algorithm whether the perturbation shall be kept or if it was counterproductive. Once the system has found the correct MPP, the P&O algorithm will still perturb the system. Therefore Liu et al. have presented an algorithm that reduces the perturbation steps the closer the MPP is reached. This implementation was done on a digital signal processor (DSP) which operated a boost converter suited to handle several amperes. In this case the processing power of the DSP was negligible.

Tse et al. [15] (cited by 103, April 2018) have published a P&O MPPTA that operates fully analog. They modulate the duty-cycle of the switching frequency of a 10 Watt boost converter with a small sinusoidal signal. Observed is the response of the solar cell voltage due to the input resistance modulation of the converter. By knowing the relation of the modulated voltage and the averaged solar voltage the maximum power point of the cell is found. They achieve tracking efficiencies between 91.7 % and 98.9 %.

Kim et al. [16] (cited by 41, April 2018) have published a low lower MPPTA for solar cells which maximizes the solar output power. They sense the solar voltage and current and maximize the power. Their motivation was to reduce the power of the MPPTA, because it requires a non-negligible amount of power. A hill climbing algorithm is presented, which uses successive approximation to reach the MPP. To save power, the algorithm is not continuously operating. Using the SAR principle they reduced the time to find the correct MPP by 69.4 %. A total power consumption of the algorithm of 4.6 µW and a tracking efficiency of 99 % is presented.

1.3 Overview on the Monolithic Harvester Chip

The main difference of this work to other publications is the focus on the ultra-low power harvesting efficiency of the monolithic system. Meaning that the system efficiency as a whole is observed and optimized. Therefore the solar cells are optimized empirically, see chapter 2. The DC/DC converter is optimized for ultra-low power operation, see chapter 4. Also a MPPTA is developed based on analytic findings regarding the combination of silicon solar cells and an on-chip charge pump, see chapter 3.

At the beginning of this work, the most prominent question was if the single n-well CMOS process allows implementing a p-n junction that can operate as solar cell, generating sufficient

power per area. After achieving first positive results from a solar test chip, the sketch from Fig. 1.2 was drawn. However, it should be mentioned here, that a solar cell as device is not intended in this process and therefore the solar test chip and all following solar devices are produced with several thousand design rule check (DRC) and electrical rule check (ERC) errors per cell. This issue and resulting problems are addressed in the conclusion of chapter 2.

In Fig. 1.2 it can be seen, that a silicon battery is implemented in the chips substrate. An energy storage device is mandatory in combination with ultra-low power harvesting, because the peak power of data transmitting for example cannot be handled by the harvester. The sketched silicon battery was developed in cooperation between the Technical University of Graz and Infineon Austria. Battery development supporting characterization measurements have been carried out in parallel to this work, proofing that the battery could serve well as storage and peak power source. The co-integration of the harvester and the silicon battery however was not part of this work and is not done yet. Hence, the prototype harvester-chip requires an external energy storage device and serves only as proof of concept.

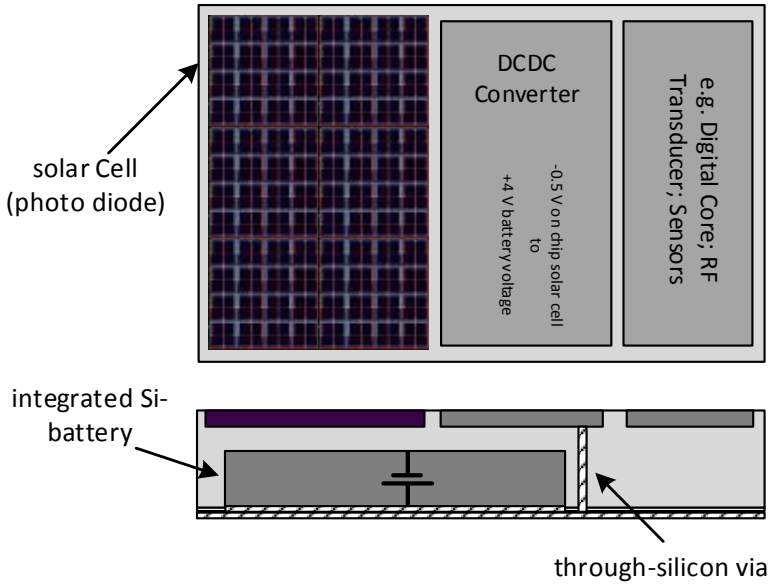


Figure 1.2: First conceptual sketch of a monolithic solar harvester chip, which contains energy storage in the substrate. The anode of the rechargeable silicon battery is the chip substrate and the cathode is connected to the DC/DC converter using a through-silicon-wire.

The first harvesting system test chip (PDC3) is depicted in Fig. 1.3. This test chip amounts to an area of 1 mm^2 and combines a solar array, a DC/DC converter, and a MPPTA. It senses the output voltage of the converter and closes a low-side switch if the output voltage has reached 4.2 V. This option is used to switch-on an off-chip demo application which is

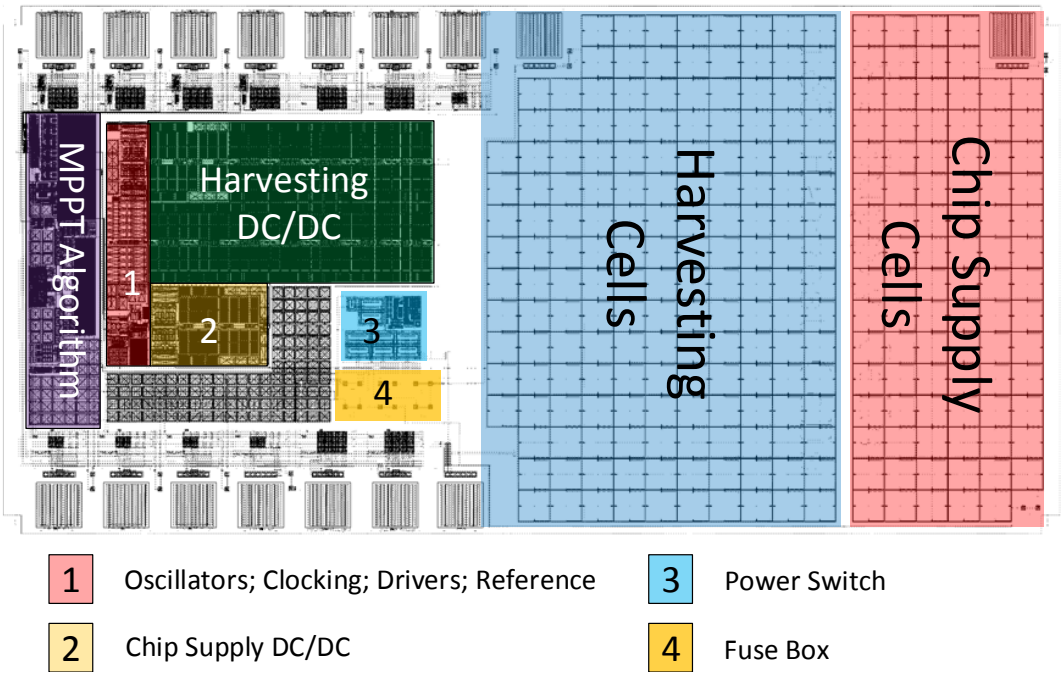


Figure 1.3: Layout and legend of PDC3. This was the first monolithic solar harvester test-chip. The solar performance was as expected but the MPPTA had minor stability issues under strong light irradiance.

then powered by the before charged output capacitor. The power switch is operated by a dynamic comparator.

Some Specifications of PDC3:

- Tape out February 2016 in a standard single n-well CMOS 130 nm process
- 0.98mm² total Chip Area
- 0.396mm² total Solar Area
- Delivers 47 nA to 3.5 µA at 3 V depending on light condition
- High dynamic range ultra-low power MPPT algorithm
- MPPT algorithm is universal – not bound to PV cells as source

The area marked as ”fuse box” serves as safety feature by shorting all on-chip supplies to the substrate. The reason for this short-circuits is to keep the harvester disabled during the manufacturing process. All tape-outs have been made using a shared reticle, meaning that the harvester chips are surrounded by other designs. Till now, it is not observed if one or two harvester chips per placement would interact with the process or other chips if they start to operate while the wafer is still processed. The working harvester would perform startup, after metal layer 4 is processed, meaning every harvester chip would start reference sources, two oscillators, the MPPTA, and a charge-pump which produces 4.2 V. To prevent this issue, fuses

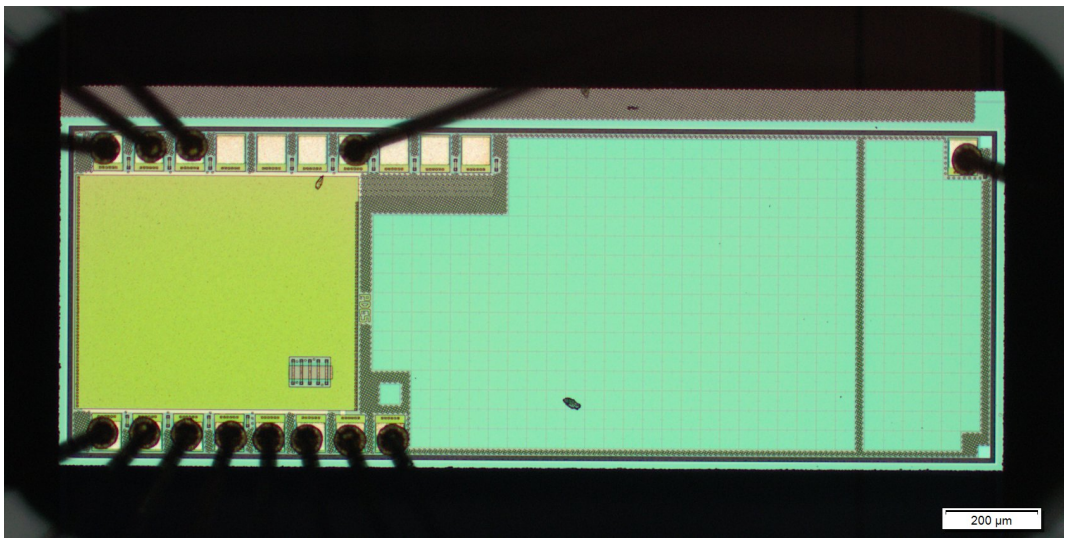


Figure 1.4: Chip photography of PDC5. On the left side of the chip is the charge pump and the maximum power pint tracking algorithm underneath a metal shielding layer. On the right side is the solar array.

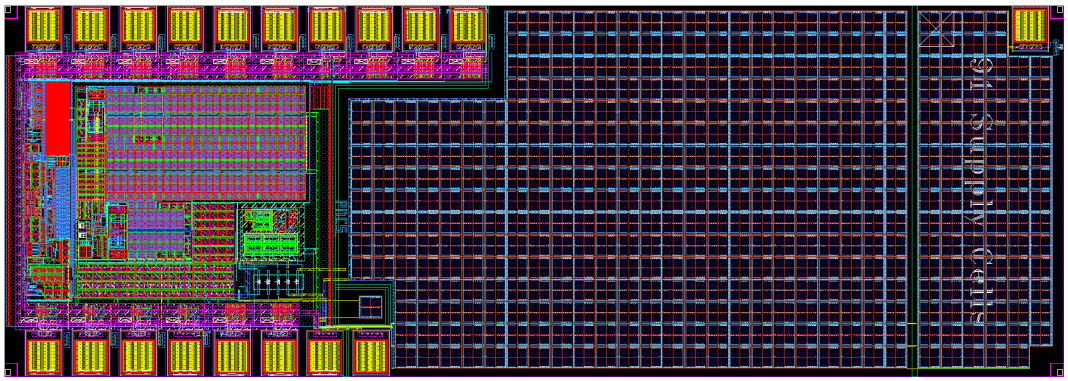


Figure 1.5: Chip layout of PDC5.

have been designed, which have to be laser cut after dicing. It shall be mentioned that PDC3 started to harvest the microscope light of the laser-cutter after the last laser fuse was cut. An externally connected 100 µF capacitor was charged by harvesting the bundled microscope light. However, the MPPTA of PDC3 had stability problems under strong irradiation as it occurs under direct natural sunlight. Therefore, PDC4,5, and 6 have also been taped-out during this work. Changes of the MPPTA are described in section 3. A chip photo and a layout view of PDC5 can be seen in Fig. 1.4 and 1.5, respectively.

Chapter 2

On-Chip Solar Cell

The content of the following chapter is partly published in [17] (own publications).

In this chapter the on-chip photo diode, also named on-chip solar cell, is introduced and discussed in detail. Possibilities which are given in the used CMOS process to form an on-chip solar cell are depicted. Further, a short introduction to the photo effect is also given at the beginning of this chapter. It might be useful for a better understanding of the measurement results. It shall be mentioned, that the focus of this work was not to maximize the solar-efficiency in general by using state-of-the-art techniques like stacked junctions, anti-reflective rough surfaces or by introducing other materials than available in the standard CMOS process. It is demanding to utilize only masks and process options that are available in the used CMOS process, without any additional effort. This ensures a final system which can be produced in a standard low cost process. The most important mechanisms necessary to understand the measurement results of the on-chip solar cells are taken from literature and explained in the beginning of this chapter. Within this work, different solar cells have been taped out on a test chip. The necessary layout layers and considerations to form a pure p-n junction in the used CMOS process are discussed. Regarding to current publications, a variation of the doping concentration and different junction geometries have been tested. The chapter concludes with measurement results from a test chip, which leads to the final system concept of the monolithic harvester. ■

2.1 Solar Cell Operation

From the operation principle point of view, there is no difference between a photodiode and a solar cell. It is the application that demands the specifications which finally define the nomenclature of these devices. Hence, the term photo diode is used in this chapter to also describe the harvesting solar cell. Basically the semiconductor solar cell is built by a p-n junction. Exposing this junction to high energy particles or photons can generate a photocurrent by escalating charge carriers into the conduction band.
Valence band electrons in silicon can be escalated to the conduction band by particles or photons with an energy greater than the band gap of silicon (E_g), which is 1.12 eV at 300 K and 1.17 eV at 0 K. This band gap corresponds to wavelengths shorter than 1107 nm, see equation (2.1.1).

Table 2.1: Electro Magnetic Spectrum - The visible and NIR spectrum can be used

			Far Infrared		NIR		Ultra Violet		γ-Ray
	Radio and Micro Waves			Mid Infrared		Visible Light		X-Ray	
λ	10km	1m	1mm	50um	3um	780nm	380nm	1nm	10pm
f	300 kHz	300 MHz	300 GHz	6 THz	100 THz	385 THz	789 THz	300 PHz	30 EHz

$$\lambda = \frac{h \cdot c}{E_g} \approx \frac{6.626\,10^{-34}\,[Js] \cdot 299792458\,[m/s]}{1.12 \cdot 1.60212\,10^{-19}\,[J]} \approx 1107\,nm \tag{2.1.1}$$

where λ is the wavelength, h is Planck's constant, c is the speed of light, and E_g is the energy band gap of silicon. As a result, no photocurrent is generated if the incident light wavelength exceeds the near infrared (NIR) regime. However, short ultra violet wavelengths up to very long wavelengths in the NIR regime will produce an electron hole pair. An overview of the electromagnetic spectrum and the typically used names for the frequency ranges are given in table 2.1. The charge carriers escalated into the conduction band are free to conduct current and need to be collected by the external circuit before they recombine.

The built-in voltage across the p-n junction depletion region results in an electric field with a maximum at the junction and no field outside of the depletion region. Any applied reverse bias adds to the built in voltage and results in a wider depletion region. The electron-hole pairs generated by photos are swept away by drift in the depletion region and are collected by diffusion from the un-depleted region. The current generated is proportional to the incident light or radiation power.
The light is absorbed according to the absorption coefficient α [cm^{-1}]. The absorption coefficient is high for short wavelengths and decreases for longer wavelengths entering the red and NIR region, see equation 2.1.2.

$$\alpha = \frac{4\pi k}{\lambda}\ [cm^{-1}] \tag{2.1.2}$$

where λ is the wavelength and k is the material and wavelength dependent extinction coefficient. The extinction coefficient table for silicon can be found in [18]. Hence, high energy photons such as UV, are absorbed superficial after entering the solar cell in a thin top surface layer. Silicon appears opaque to these short wavelengths. The absorption coefficient α is zero for wavelengths longer than 1107 nm. The inverse of α is the average distance a photon travels through the semiconductor before it gets absorbed.

According to the absorption coefficient, a charge carrier generation rate can be derived introducing the intensity. The intensity exponentially decreases with the distance the photon traveled in the material, see equation 2.1.3. Using a simplification it is assumed, that a decrease in intensity is caused only by the absorption, which generates an electron hole pair.

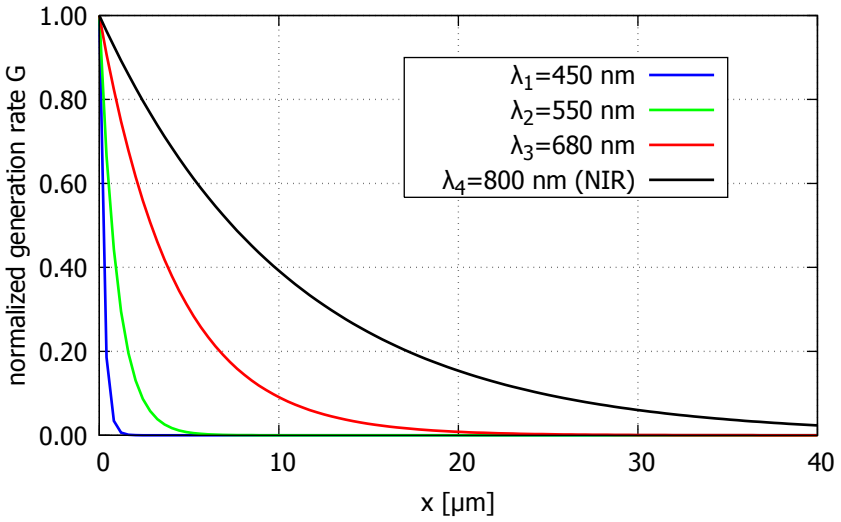


Figure 2.1: Normalized charge carrier generation rate for different wavelengths as function of the penetration depth (x). The cell surface corresponds to x=0.

Table 2.2: Parameters used for the collection probability functions in Fig. 2.1. α is calculated for the given wavelength using k from [18].

λ [nm]	k	α [cm $^{-1}$]
450	0.149	41682
550	0.044	10079
680	0.013	2398
800	0.006	937

$$I = I_0 e^{-\alpha x} \tag{2.1.3}$$

where I is the intensity, I_0 is the incoming intensity at the surface, α is the absorption coefficient and x is the photon penetration depth. Following the before made assumption, that a decreasing intensity is caused by absorption, the derivative of the intensity is related to the charge carrier generation rate. This generation rate (G) is related to α and therefore related to the wavelength and the average distance (x), the photon travels in silicon [19].

$$G(x) = \alpha N_0 e^{-\alpha x} \tag{2.1.4}$$

where N_0 is the incoming photon flux and x is the distance from the surface the photon has traveled.

In Fig. 2.1 it can be seen how the charge carrier generation rate rapidly drops with the average traveling distance (x) in silicon. Also the strong dependency of the wavelength on the average traveling distance is depicted. Photons with higher energy of the ultra violet and

blue spectrum are absorbed directly under the surface, while the low energy NIR portion of the light will be absorbed over a longer distance. Considering a black body radiator, for example the sun, or a light source close to it, which has a continuous spectrum, the charge carrier generation rate has to be integrated over the wavelength. This results in a charge carrier generation rate which is 4 to 5 orders of magnitude higher at the surface than it is deeper in the bulk. However, the junction doping layer thickness is typically set to be less than 1 µm ([19],[20]), due to the generation rate drop.

Besides the charge carrier generation rate, also the recombination mechanisms affect the solar cell operation. Three different charge carrier recombination mechanisms take place:

Auger Recombination increases for high doping and high charge carrier densities [21].

Radiative Recombination is a mechanism that basically affects direct band gap materials. It is almost negligible for Si solar cells.

Shockley-Read-Hall Recombination is caused by defects. It does not affect un-defected silicon [22].

Due to high dopant concentrations, which are typically used for a standard CMOS process, the main recombination mechanism is the Auger recombination. The n-well implant is doped by a density of approximately 10^{17} to 10^{18} [cm^{-3}]. Therefore, the Auger recombination effects the whole recombination process by more than 95 %, while radiative recombination contributes with approximately 1 % [23]. The doping density of the p-diffusion is 10-times higher than the concentration of the n-well, which makes the Auger recombination even more dominant.

The recombination additionally depends on the position in the silicon. At the front and back surface, the recombination is higher than inside the bulk. Although the charge carrier generation rate is much higher close to the surface, the generated charge carriers will also recombine more likely. By using a proper surface passivation, the surface recombination can be reduced. However, to estimate the overall solar performance the probability of a generated charge carrier to contribute to the photocurrent has to be taken into account. To do so, the collection probability (CP) is introduced.

The CP is a mathematical probability function, used to calculate the probability of a generated charge carrier to contribute to the photocurrent. As the recombination mechanisms also depend on the doping levels and surface passivation and because of the additional complexity due to doping gradients across the cell, the CP offers a more convenient way of calculation. Due to the electric field inside the junction the CP is unity, because a generated electron hole pair gets separated immediately. Outside the junction the CP starts do drop. Following the n-well from the surface to the junction, a non-uniform doping profile is used to achieve the specified device properties. Considering this doping profile and the recombination mechanisms, the analytic calculation of the CP is not constructive. However, it shall be shown how the overall photocurrent density can be expressed using the CP and the charge carrier generation rate G.

$$J = q\int_0^L G(x)\,CP(x)\,dx = q\int_0^L \left[\int \alpha(\lambda)\,N_0 e^{-\alpha(\lambda)x} d\lambda\right] CP(x)\,dx \tag{2.1.5}$$

where J is the photocurrent density, q is the electron charge, and L is the vertical thickness of the solar cell respectively the die. As shown in equation 2.1.5, the overall current is the product of the generation rate and the collection probability. Although the generation rate has a maximum at G(0), see Fig. 2.1, a thin junction at the surface will produce less photocurrent than a junction deeper in the bulk, because CP(0) is almost zero.

2.2 Solar Cells in the Single n-well CMOS Process

The 130 nm single n-well CMOS process, which is used in this work utilizes a p-doped substrate. In areas without n-well implant, a p-well is automatically generated, which has a higher doping concentration than the p-doped substrate (PSub). It is worth noting that neither a schematic model nor in layout a photodiode was offered by the process, during the time this work was done. Therefore, only a rough estimation regarding the performance was possible in the presilicon phase using the theory described in chapter 2.1.

The process basically offers three junctions to form a photo diode, which are

n-Diffusion to p-Substrate the junction is close to the surface and the diffusion is highly doped; this benefits recombination; a negative voltage with respect to PSub is build up under illumination

p-Diffusion to n-Well the junction is close to the surface also utilizing the highly doped diffusion; again a low efficiency is expected; generating a positive voltage with respect to PSub; this junction is further named D_1; see Fig. 2.2

n-Well to p-Substrate the junction is 1 to 2 µm deep in the bulk; negative voltage with respect to PSub; this junction is further named D_2; see Fig. 2.3

The n-diffusion to PSub junction was sorted out for further performance investigations, because it combines two disadvantages. Firstly, a low photo current density caused by the low CP is expected, and secondly, a negative voltage with respect to ground arises. While the low CP is only a performance issue, the negative voltage that arises across the n-diffusion junction can hardly be further processed if a monolithic harvester is used. Connecting n-diffusion built solar cell to an N-channel metal–oxide–semiconductor field-effect transistor (NMOS), which is placed on the same substrate, will result in an forward biased source bulk diode. This parasitic diode associated with the NMOS utilizes the same n-diffusion. Hence, it is assumed, that the built-in voltages of the junctions are the same causing a forward bias condition in the parasitic diode, which cannot be neglected.

The p-diffusion junction is a more promising solar cell, because of the positive voltage with respect to the n-well implant. Fig. 2.2 shows the n-well connected to PSub, which gives a positive voltage at p-diffusion with respect to PSub. Even stacking of the diodes to generate

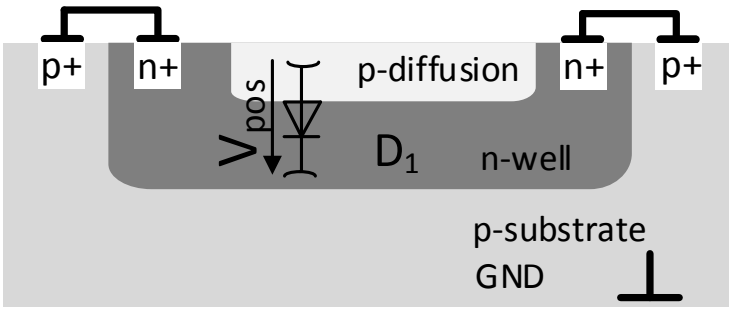


Figure 2.2: Cross section sketch of the process, using the p-diffusion to generate a photocurrent. The substrate has ground potential and the n-well is tied to ground by metal contacts. Diode D_1 is formed by the p-diffusion to n-well junction.

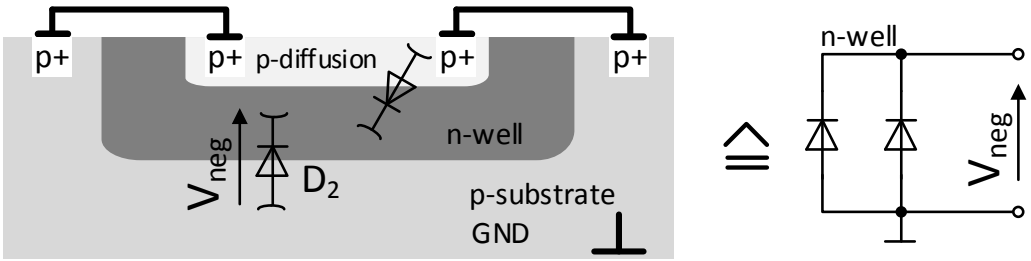


Figure 2.3: Cross section sketch of the CMOS process, using the n-well implant to generate a photocurrent. In addition the p-diffusion is grounded, which connects D_1 in parallel to D_2. The PSub is per definition ground.

a higher voltage is possible for the D_1 junctions, if the well implant is not connected to ground. Further considerations on diode stacking are given in section 2.2.1. The fact, that a positive voltage can be handled straight forward, made this junction the preferred power source for fully integrated harvesting systems according to [6, 24, 25].

Nevertheless, regarding the generated power per area, the n-well implant to PSub junction (D_2) performs better. The higher generated power per area is caused by the location deeper in the bulk and by the lower doping concentration of the n-well. Due to the junctions location deeper in the bulk, the surface recombination is lower, hence more generated charge carriers can contribute to the photocurrent. Also the Auger recombination is lower due to the reduced doping concentration of the n-well compared to the p-diffusion. Despite the main advantage of D_2 delivering the higher power density it also comes with two major disadvantages. Series stacking is not possible due to the common substrate. Consequently the delivered voltage is limited to one forward bias voltage. Secondly, D_2 generates a negative voltage with respect to PSub. This negative voltage is the reason, why this junction was not used as on-chip power source for monolithic systems in recent publications. Handling the negative voltage requires additional circuit effort which might be the reason why D_2 gets described as parasitic solar cell although it performs better than D_1. A combination of D_1 and D_2 for energy harvesting

was only described in theory by [13] or built as two chip solution [7]. Fig. 2.3 shows a sketch of D_1 and D_2 in parallel connection which would be the preferred connection scheme regarding power efficiency.

2.2.1 Series Stacking versus DC-DC Up-Conversion

The basic function of the monolithic harvester is to generate an output voltage, that can be used to supply the on-chip system. Due to the gap between the delivered power and the necessary power for an on-chip system a storage device acting as energy reservoir has to be charged. State-of-the-art batteries typically have 1.8 to 4.2 as charge-finish voltages. However, when utilizing a capacitor the energy stored in the device is a quadratic function of the voltage. In both cases (battery or capacitor), the voltage that builds up across a single p-n junction (approximately 400 mV to 480 mV) is not high enough for further use.

As already described in the introduction, the monolithic harvester therefore utilizes a charge pump to generate a higher output voltage instead of series stack of p-n junctions. Stacked photo-diodes for high voltage generation have been reported by [26] using a silicon on isolator (SoI) process, where sapphire is utilized to insulate the junctions from each other. A standard single n-well CMOS process does not offer a possibility to fully insulate the junctions. Due to the common substrate only the diffusion junction (D_1) can be stacked in series. Fig. 2.4 shows a cross section sketch of two series connected diodes. This structure would already double the input voltage V_{pos}. A concept using two and three D_1 diodes in series to generate 0.8 V and 1.3 V respectively was presented by Law and Bermak in [27].

However, a series connection of D_1 always leads to losses caused by D_2, as can be seen in Fig. 2.4. The second well implant introduces the parasitic loss junction D_2 which needs to be compensated by the previous stage.

A theoretical example of a series stacked diode circuit is depicted in Fig. 2.5. D_1 is drawn in black and the parasite D_2, which needs to be compensated, in red. In the depicted circuit M diodes are connected in series to generate the desired output voltage. The parasitic diode D_2 which is inherently attached to every D_1 also generates a photocurrent. The major drawback is, that the two currents flow in opposite directions which reduces the output current. Assuming natural light or at least a light source which does not consist of ultra violet (UV) wavelengths only, the photocurrent of D_2 is higher than the photocurrent generated by D_1. Equation 2.2.1 introduces the factor K to build the relation of the two photocurrents. As a result, the parasitic photocurrent has to be compensated by the previous stage using K+1 times D_1, assuming K is greater than 1.

$$I_{D2} = K I_{D1} \tag{2.2.1}$$

$$\eta = \frac{M}{\sum_{i=1}^{M} (K+1)^i} \tag{2.2.2}$$

Using the theoretical circuit from Fig. 2.5 the efficiency η can be derived, see equation 2.2.2.

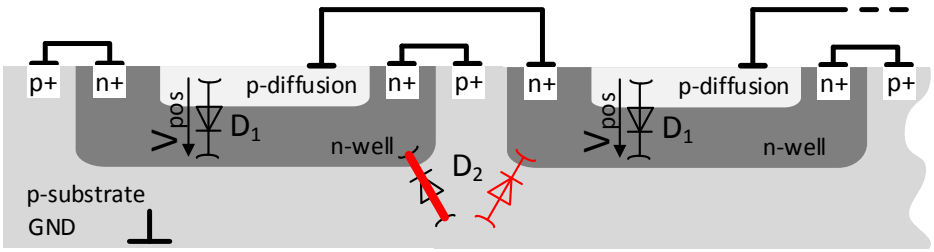


Figure 2.4: Cross section sketch of 2 photodiodes D_1 in series connection. Only the first parasitic junction D_2 can be shorted to ground.

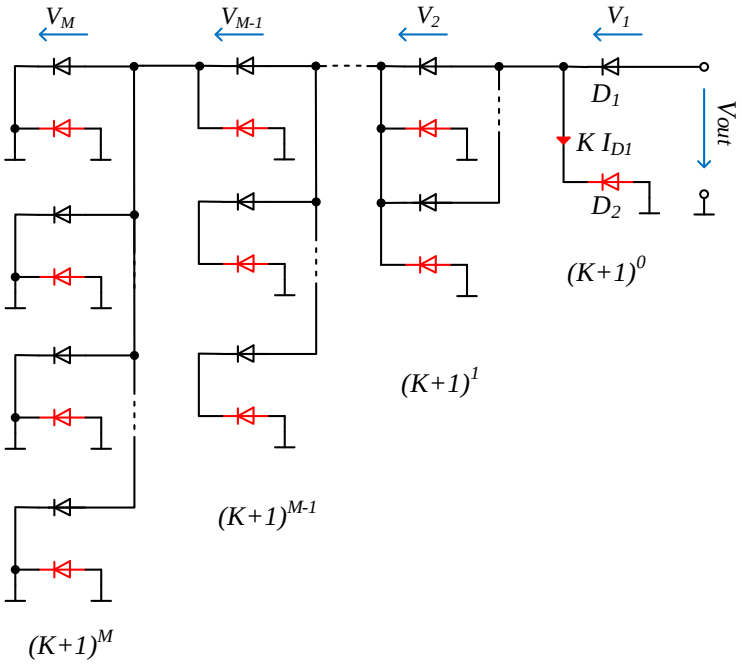


Figure 2.5: Schematic of M photodiodes D_1 in series connection to generate V_{out}. For every added series connected D_1, K times the number of previous photodiodes needs to be added to compensate the current loss caused by D_2(red)

Solutions of equation 2.2.2 are depicted in Fig. 2.6. Firstly it can be seen that the efficiency rapidly drops with the number of series connections (M). Secondly the efficiency is also heavily affected by the current relation factor K as Fig. 2.6 also depicts. In case of harvesting energy into a lithium based energy storage, at least ten diodes would need to be stacked in series (red line in the diagram) to achieve the necessary voltage.

In [27] Law and Bermak have published data of their process where K is approximately 7. Measurements performed on my first test chip have shown that K equals 16 under sunlight condition in the used process. Detailed measurement results for the value of K are given in

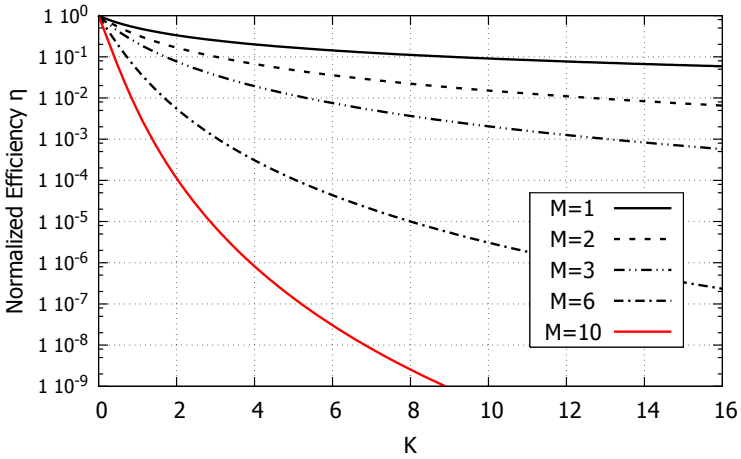


Figure 2.6: Efficiency of series stacked diffusion junctions D_1 as a function of the current relation K. The number of series connection is denoted by M.

section 2.3. Due to the high effort to compensate the current loss of the parasitic junction D_2 the efficiency loss makes series stacking an unfeasible approach for the process I had to work with. The efficiency expression is calculated by relating the output power to the total installed power including the effort to compensate the parasitic losses.

Therefore, a system design was chosen where D_2 is not seen as parasitic element but as harvesting source connected in parallel to D_1. Thus a significant efficiency improvement is obtained in comparison to [27]. Further a DC-DC converter is used to boost the diode voltage to a suitable output voltage using only parallel connected junctions. In this case M equals 1 and the total installed power is also the power that is fed to the DC-DC converter. Based on my scientific investigations it is pointed out that even if the DC/DC converter efficiency is in a low percent regime, the overall efficiency is orders of magnitude higher than it would be with the series stacking technique.

2.3 Solar Cell Test Chip

To investigate the eligibility of the 130 nm single n-well process to form a proper solar cell, I designed a first test-chip. Relying on recent publications, which are shortly presented in the next section 2.3.1, it was a common-sense approach to observe different geometrical junction structures. By increasing the junction area that is obtained per chip area, the generated power should be maximized, so the idea. In the first place my test-chip should offer the possibility to investigated how much photocurrent and power per area can be obtained by the p-n junctions. Another aspect to be covered by the test-chip was the influence of the geometry and doping which was also investigated in related work for example by Ferri, Chen, and Ghosch [24, 13, 28]. Based on this test chip results, a decision about the future design and the feasibility of a monolithic harvester in our CMOS process was made. To answer this fundamental questions for the used process, an actual test-chip was necessary, because no

data regarding the parameters of interest for energy harvesting was available. Real-world measurement results under environmental conditions should then also be used for modelling of the solar cell. However, in contrast to the related work, my test-chip also held structures that allowed to observe the influence of the passivation layer as well as a simple rectangular geometry which is used as reference design for geometry variations. Detailed information on the test structures and the test-chip is given in section 2.3.2.

2.3.1 Related work - On-Chip Solar Cells

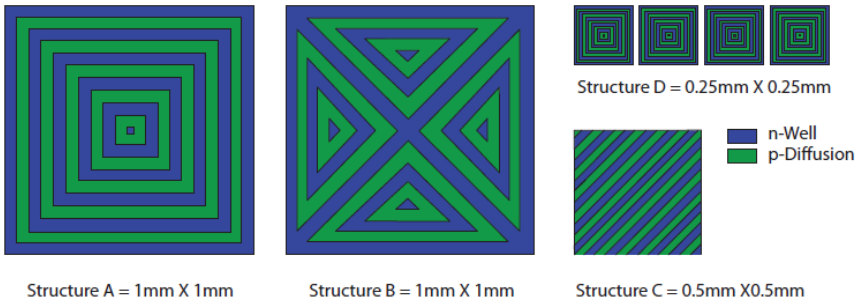
Related work regarding on-chip solar harvesting and cell optimization has not been published frequently. Typically, on-chip optical devices are used for coupling, data transmission, and as image sensors. In these applications the outer quantum efficiency is not the main concern as speed or noise optimizations are in the foreground, respectively. However, three examples which show different approaches for on-chip solar cell optimizations are summarized in Fig. 2.7.

M. Ferri et al. [24] have published a geometry study shown in Fig. 2.7a. The best solar performance is achieved with structure C. A simple rectangular diffusion area serving as reference for comparison to the different geometries is not implemented on their test-chip. Hence, an increase of the efficiency due to a special shaping cannot be proven. However, a dependency of the geometry regarding the achieved power per area of is clearly shown. Further an outlook on block level is given on how an unregulated monolithic harvesting system without maximum power point tracking algorithm (MPPTA) could be implemented on a single die using the p-diffusion to n-well junction. Their measurement results show a conversion efficiency of the presented cell structures for their harvesting diodes (junction D_1) between 2.26 % and 3.02 %. The parasitic diode (junction D_2) shows an efficiency between 9.45 % and 17.64 % on the presented test-chip. However, junction D_2 is not considered as harvesting device, because of the resulting n-well implant potential below ground. Therefore D_2 is marked as parasitic diode although it is outperforming D_1 and is shorted to PSub.

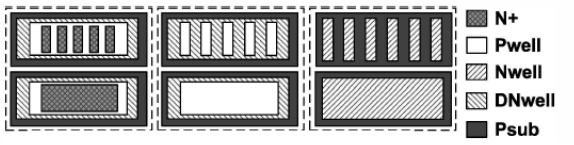
Table 2.3 shows measurement results of the cell structures from Fig. 2.7a. A significantly higher photocurrent efficiency for the n-well implant compared to the diffusion is measured.

These results are explained by the junction position deeper in the bulk and the associated higher collection probability function (see chapter 2.1).

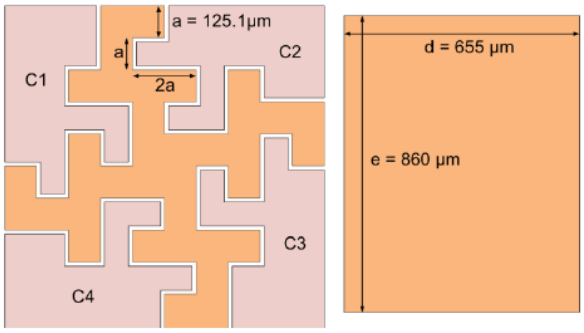
Zhiyuan Chen et al. [13] present an optimization investigation with focus on the lateral photocurrent referring to Fig. 2.7b. Detailed insights in the used 0.18 µm process regarding the design rules are given, because of the importance for the lateral photocurrent. Their intension was to make use of the lateral junction which should add additional lateral photocurrent. Therefore, the implant depth and the minimum design-rule distance for neighboring junctions are the key specifications, because they determine if the overall junction area can be increased. It is observed, that the structure using the N+ diffusion generates the highest photocurrent in the used process. The explanation for this observation is given by the fact, that this diffusion allows the narrowest gaps. Therefore, the shape inherently induces the largest junction area



(a) Different geometries and relatively large cells which all utillize the diffusion to implant junction. All implemented in a 0.35 µm CMOS process. Picture taken from Ferri et al. [24]



(b) All junctions of the deep n-well process have been tested. Additional use of the lateral photocurrent was the purpose of this structure. Picture taken from Chen et al. [13]



(c) Koch fractal structure. The diffusion (orange) has a relatively large perimeter to increase the lateral junction. Picture taken from Ghosh et al. [28]

Figure 2.7: Related work examples from recent publications regarding on-chip solar cells. Basically different doping options and geometries have been tested.

per chip area. Unfortunately, no measurement results have been published, to best knowledge of the author. Especially measurements which compare their lateral junction segmentation to a simple rectangular continuous shape would have been very beneficial. Without this data a prediction of photocurrent increase at another CMOS process with different design rules is not possible.

Suvradip Ghosh et al. [28] introduce a fractal shaped junction, see Fig. 2.7c, implemented in a standard 0.5 µm CMOS process. The presented shape is a quadric Koch fractal after the first iteration. Basically the idea was to maximize the perimeter of the structure to gain as much side-wall junction area as possible. In comparison to a simple rectangle which has the same surface area, the presented Koch fractal induces a three times larger perimeter resulting in a three times larger side-wall area. The solar cell is described for the dedicated use of energy harvesting. Hence the p-diffusion to n-well implant is chosen, because it delivers the convenient positive voltage with respect to substrate ground. The cell depicted in 2.7c

Table 2.3: Solar Cell Efficiencies taken from [24] referring to Fig. 2.7a

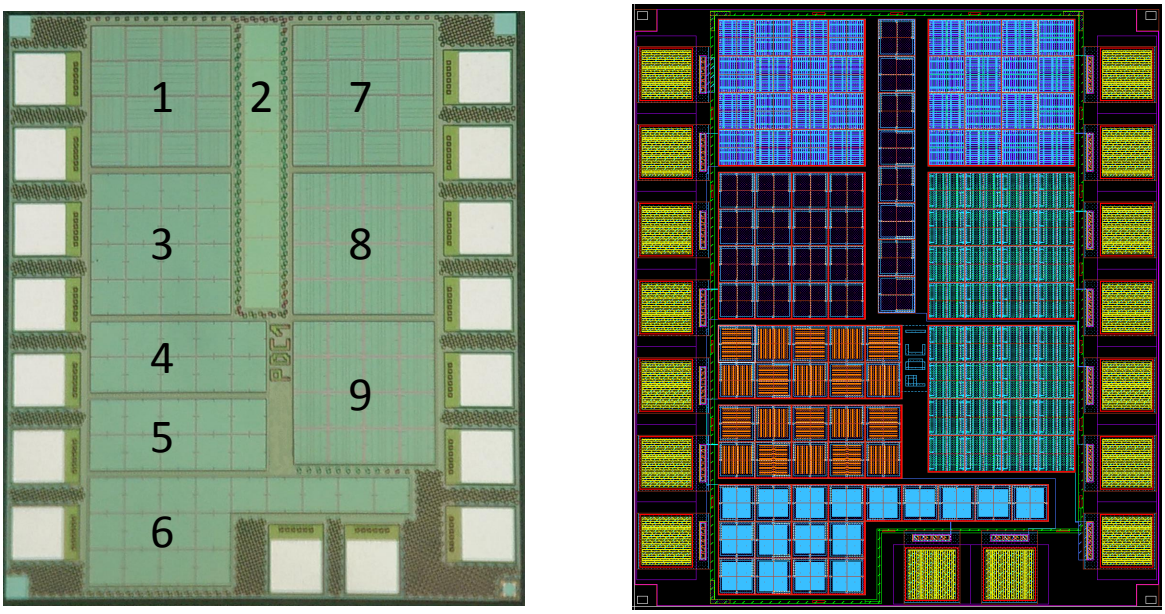
Structure	Harvester with floating Parasite	Harvester with shorted Parasite	Parasite with floating Harvester	Harvester parallel with Parasite
A	2.91 %	0.44 %	9.45 %	9.45 %
B	3.02 %	0.44 %	15.12 %	15.12 %
C	2.91 %	1.04 %	17.64 %	17.01 %
D	2.26 %	0.56 %	11.9 %	12.6 %

has an active p-diffusion area of $0.5633\,\mathrm{mm}^2$ (orange). It is compared to a rectangle patch which has the same area (on the right side of the picture). Their measurement results show that additional side-wall junction area leads to 6% improvement compared to the rectangle patch.

Remarks to the Koch fractal structure:
The overall chip area, that is covert by the quadric Koch fractal ($0.5633\,\mathrm{mm}^2$) from [28], amounts to $1.565\,\mathrm{mm}^2$. Meaning that in comparison to a rectangle p-diffusion patch, which requires the occupied silicon area of $1.565\,\mathrm{mm}^2$, the first iteration fractal clearly does not improve the efficiency. A p-diffusion rectangle patch on the same chip area would outperform the fractal by 264 %. However, the fractal approach could be made more practical by implementing more and finer structures.

Conclusion on Related Work On-chip Solar Cells

From chapter 2.1 and the described solar cell designs in the related work chapter it is clear, that the n-well implant to p-substrate should be used as main harvesting source for a highly miniaturized monolithic design. Therefore I have chosen this diode as the main solar cell for further scientific investigations presented in the following chapter. Also a dependence on the geometry regarding the solar efficiency was presented in the before introduced related work. Hence different geometries have to be tested for the used CMOS process. However, it is shown that structures which make use of the lateral junction can additionally increase the solar efficiency as long as the design rules allow the lateral junctions to be narrow enough to increase the surface area. Unfortunately, none of the publications about on-chip solar cells do give any information regarding the used surface passivation or the metal layer stack. The passivation is the top layer of the surface, which mainly defines the reflection of the cell. The metal stack gives a hint on the distance from the actual solar cell to the chip surface. Further, the presented solar cells have been tested by using different light sources, which do not allow a direct performance comparison. For future comparison, the solar cells of this work have also been characterized under natural sunlight conditions. Using sunlight on a clear day and giving information about the place, date and time is a proper way to characterize solar cells, if no solar emulation test-bench is available [29]. To compare different designs, solar test facilities typically also keep the temperature of the device under test (DUT) stable. If the temperature can not be kept stable it is useful to measure the DUT temperature



(a) PDC1 chip photo. The test chip contains 9 different solar cell arrays.

(b) PDC1 chip layout. The different colors of the arrays are given by the geometries and the layout layers used. Reference structures 2 and 3 appear simply dark, bebcuse they do not use any special shaping of the diffusion or implant.

Figure 2.8: Solar cell test chip "PDC1". The chip size of the test chip is 600 µm x 684 µm

as the miniaturized solar cells change their temperature fast according to the illumination conditions. Based on the results mainly from [24, 28, 13] I have designed a first test chip containing different solar cells utilizing the implant and diffusion junctions as well as different geometries at the minimum design rule distances.

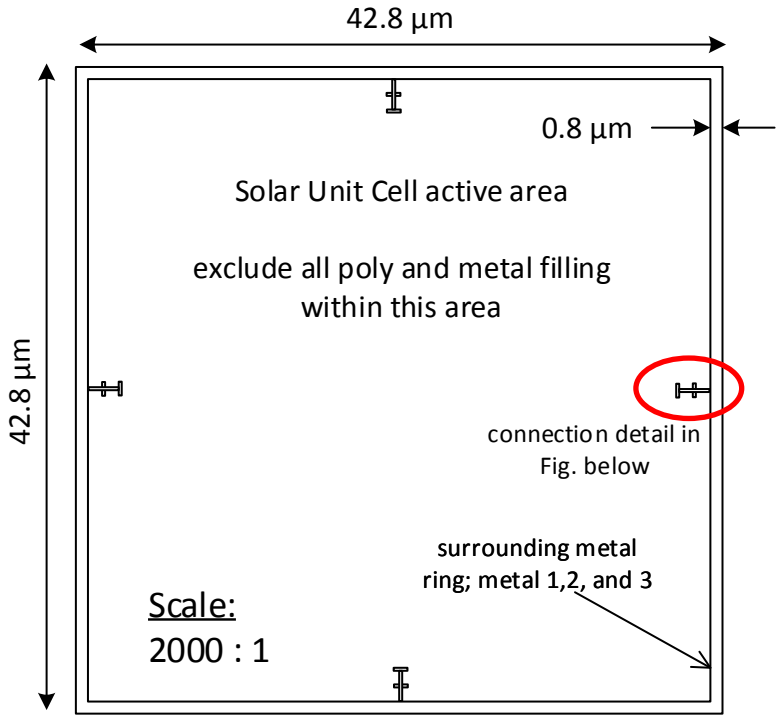
2.3.2 Solar Cell Test Chip - PDC1

The first test chip of this work is the PDC1. Building this test-chip was done in the layout editor only, because the CMOS process does not support solar cells. Doe to the fact that I had to design the cells layer by layer without having a standard model and without the possibility to run proper design check as design rule check (DCR), electrical rule check (ECR), and layout versus schematic check (LVS), the layout of this test-chip was very time consuming. For that reason, I have decided to introduce the reader shortly to the mask layers of the process, see chapter 2.3.3, which are necessary to form a simple p-n junction in a CMOS process. Covering different geometries designed a the minimum allowed widths as well was implementing a reference structure which is mandatory for comparison, a total number of 9 different solar cells was necessary. These 9 cell structures allow to investigate the assumptions on geometries published recently plus novel investigations on the passivation. It shall be mentioned that my research work performed with this test-chip was cited by Mr. Pretl et

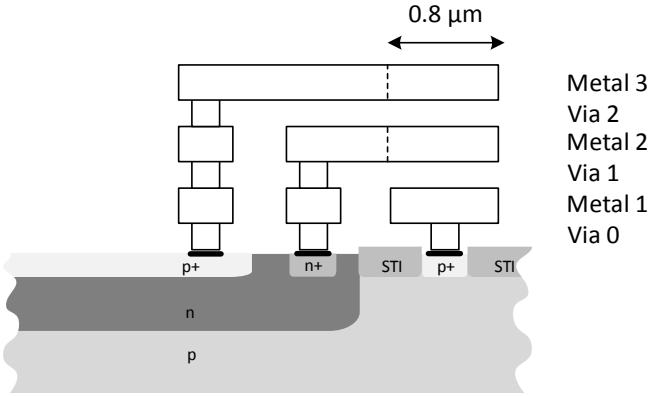
al. [30] regarding the power densities. The test-chip was part of a shared reticle tape out in the 130 nm CMOS process without flash option. In Fig. 2.8 the 600 µm x 684 µm sized PDC1 is depicted as micrograph and in layout view. The nine different solar cell structures are numbered in Fig. 2.8a and will further be named structure 1 to 9. All structures are built using 42.8 µm x 42.8 µm sized unit solar cells. For example: Structure 1 is built by a 4x4 array of the before mentioned unit cells. Every unit cell is surrounded by a 0.8 µm thick metal ring to collect the photo current from the different junctions. In Fig. 2.9a an unit cell in scale 2000 : 1 is depicted. The area within the metal current collector ring is marked as active and is different for all 9 structures.

A connection detail of the metal layer to junction composition is depicted in Fig. 2.9b. Due to compatibility reasons, all unit cells follow the same metal alignment:

- Substrate connected to metal 1
- n-implant connected to metal 2
- p-diffusion connected to metal 3



(a) Solar unit cell in scale 2000:1. Every unit cell is surrounded by a 0.8 µm wide metal current collector ring. The layout allows placing of unit cells next to each other providing the correct connection automatically.



(b) Metal connections to the differently doped areas. Substrate is always on metal 1, n-well is always on metal 2, and p+ is always on metal 3. Depending on the n-well and p+ structure, the inner connection wiring can look different. [Drawing not in scale]

Figure 2.9: Connection detail of the solar unit cell. Using equal sized, quadratic unit cells which all follow the depicted connection scheme allows a simple chip layout and compatibility between unit cells and different structures.

2.3.3 Mask Description and Unit Cell Layouts

RX The RX mask is mainly used to mark an area for active devices. Hence no shallow trench isolation (STI) is produced but highly doped n+ or p+ diffusion. Therefore the whole solar unit cell area is marked as active, because the STI is expected to additionally shield the light, while further no diffusion or contact can be placed.

NOSD An area marked as active prepares the area for an active device. In the case of the used CMOS process these active devices are P-channel metal–oxide–semiconductor field-effect transistor (PMOS), NMOS, substrate involving capacitors, and diodes. All of these devices utilize either an n+ or p+ diffusion in the well which is only blocked by the polysilicon gate. To suppress the diffusion in an active area without using polysilicon the NOSD (no source drain) is used. As this mask is a blockage layer for n+- and p+- source/drain implant, it is the only possibility to generate a p+ to n-well junction.

NOLDD In an active area, usually diffusion doping is used to create a source or drain contact. Therefore, a halo implant is automatically generated at the edge of every diffusion, because the typical use case is to create a MOS transistor in an active area. To avoid this halo implant, the NOLDD (no lightly doped drain) mask is used across the entire active area. This measure ensures a p-n junction that appears on the chip as it is drawn in layout.

OP This mask prevents the silicide generation. As it is a negative e.g. blocking mask, it is left open in areas where ohmic contacts are placed. Silicide has a metallic shining and shows a reflectance for the optical wavelengths between 50% and 65%, depending on the annealing temperature [31]. The silicide block in non-contact areas also reduces the charge carrier recombination. Otherwise, a highly doped compound, as which silicide can be seen, would cover the solar cells surface also in areas without contacts. This would benefit the Auger recombination.

BF is a blocking mask for the p-diffusion which is used to reduce coupling of sensitive and noisy areas on chip. Therefore the BF layer is also often called BFMOAT, because the noise aggressor on the chip can get surrounded by a high ohmic moat. In areas which are covered by the BFMOAT layer, no p-well is generated. As a result, the substrate remains lightly p-doped. For our solar test chip, this lightly doped area below the n-well implant was of interest, because a wider depletion region, ranging into the substrate is expected.

D1/DV The DV mask marks the opening of the topmost polyimide passivation. In areas where the shape is drawn, the passivation gets an opening. This mask is typically used to open pads for wire bond or for laser-cut fuses. In the case of the solar cell, the DV mask is used across the entire solar area as long as the test chips are ordered with polyimide at the chip surface. If no polyimide is ordered, the D1 mask replaces the DV mask. In this case, the chip is protected only by the Nitride/Oxide hard-passivation.

BP The shape blocks the n+ source/drain. It identifies the PMOS, p+ junctions, and substrate contact areas.

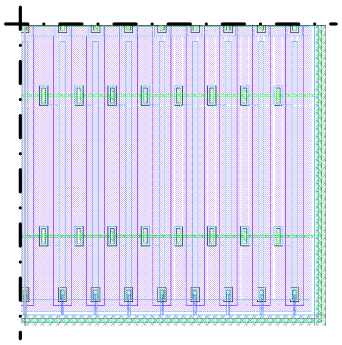
NW Is drawn to generate n-well regions.

Layout layers for the metal line generation as well as layers, which prevent the metal and polysilicon filling structures, are not drawn in the detailed descriptions of Fig. 2.10 to Fig. 2.13 for clarity reasons. In a nutshell, the single n-well STI CMOS process requires 17 layers drawn in layout to generate a simple p-n junction, which shall operate as a solar cell.

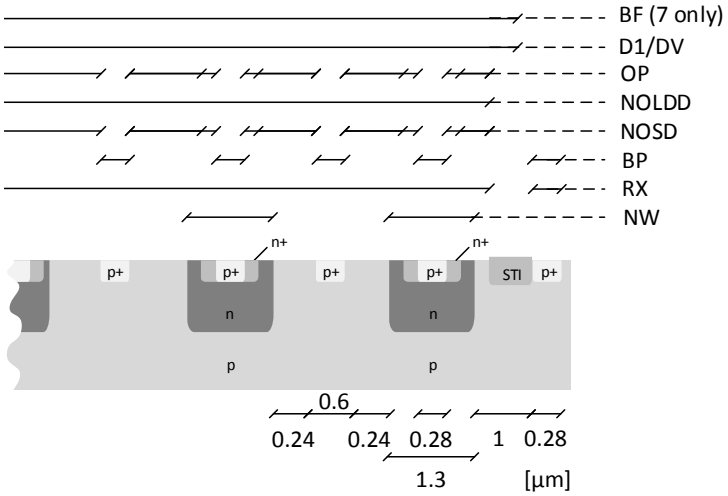
Detailed Structure Description

Structures 1 and 7

Cells structures 1 and 7 are built with 17 parallel n-well implant strips using the narrowest allowed gap between implants. In the middle of every implant is a p-diffusion strip to form the D1 junction. To collect the photocurrent, additional p-implants are set in the substrate between the n-wells. The current collection of the n-wells is done, using n-diffusions in the middle section of the cell. Structure 7 differs from structure 1 by using the BF mask. Basically the idea was to have a p-substrate with much lower doping density generating a wider depletion region ranging into the substrate. This increase in depletion region was primarily tested, because of the higher charge carrier collection probability within. Both cell arrays are built by 16 unit cells, respectively.



(a) Symmetric layout quarter of the unit cell.

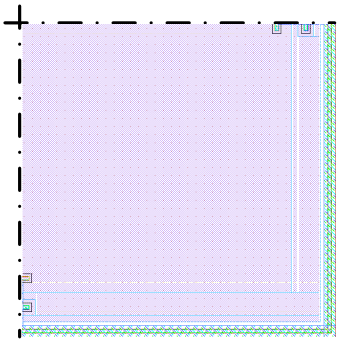


(b) Mask stack

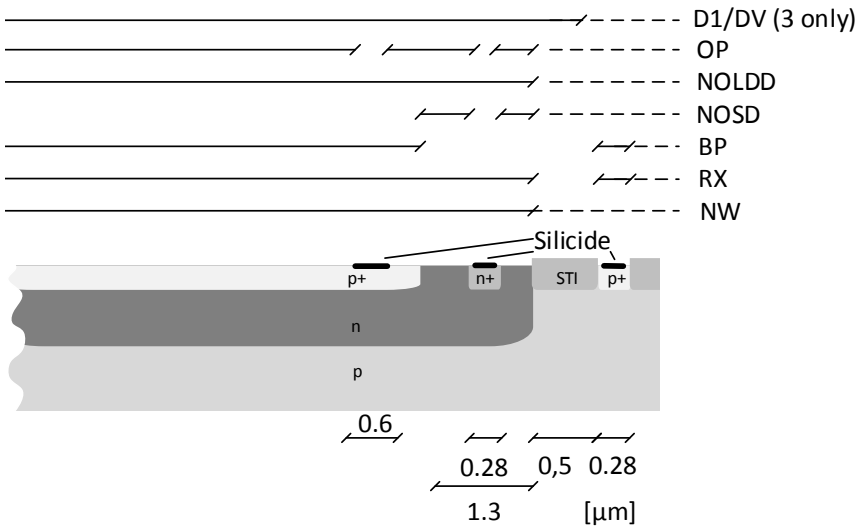
Figure 2.10: Layout quarter and mask stack of structures 1 and 7

Structures 2 and 3

The geometries of 2 and 3 are kept simple. As all other test structures, they also use the quadratic n-well implant. Centered in the n-well is a quadratic p-implant rectangle without any additional shaping for increased lateral junction area. Structure 3 should serve as reference design for later comparison to the cut-out diffusions. It was intended to measure the impact of increased sidewall junction area regarding the efficiency of the solar cells, as published for other processes. Structure 2 is basically the same cell as structure 3. The difference is only the passivation opening on top of structure 2. In Fig. 2.8a a slight color difference from structure 2 to all other cells can be seen, which is caused by the passivation opening. The purpose of this cell is to show the impact of the additional passivation layer on top of the cell in comparison to reference structure 3.



(a) Symmetric layout quarter

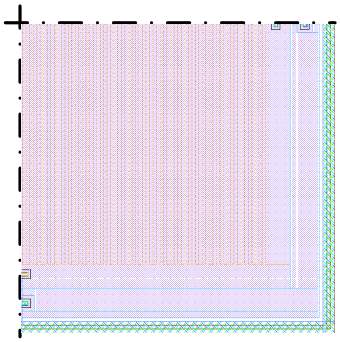


(b) Mask stack

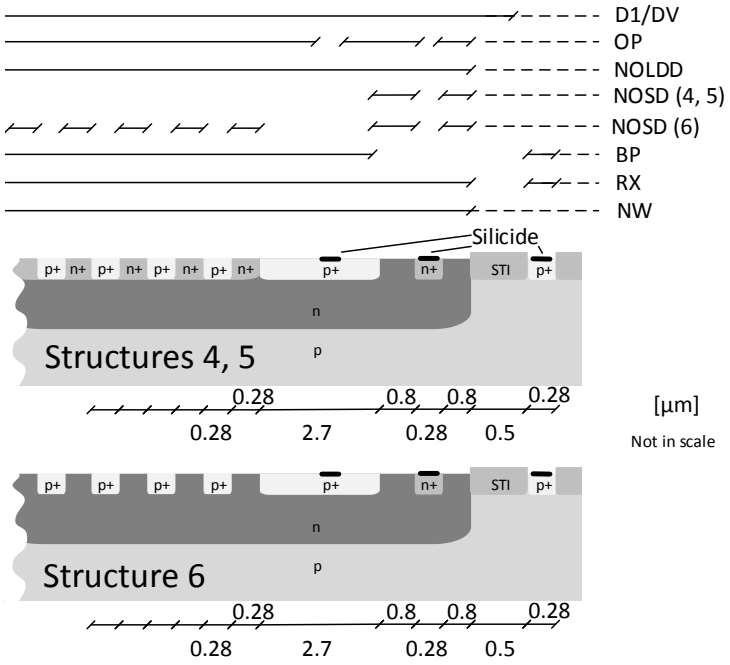
Figure 2.11: Layout quarter and mask stack of structures 2 and 3

Structures 4, 5, and 6

These structures again have a 40.7 µm x 40.7 µm n-well implant which has a 30.8 µm square p-diffusion in the center. The p-diffusion has cut-out stripes using the minimum allowed gaps and widths. The main difference to structure 6 is the NOSD mask. For 6 the NOSD mask is also cut like the p-diffusion. In this case no n+ is generated. The difference between 4 and 5 is basically only the cut-out geometry. Structure 4 uses closed cuts while structure 5 has digitated p-diffusion geometry. However, all p-diffusions are connected by metal contacts.



(a) Symmetric layout quarter

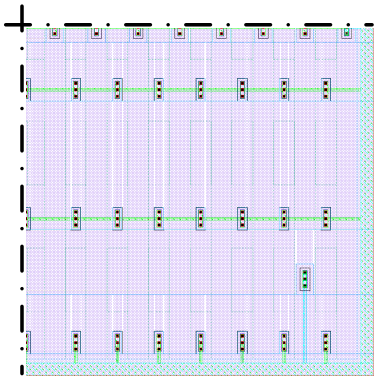


(b) Mask stack

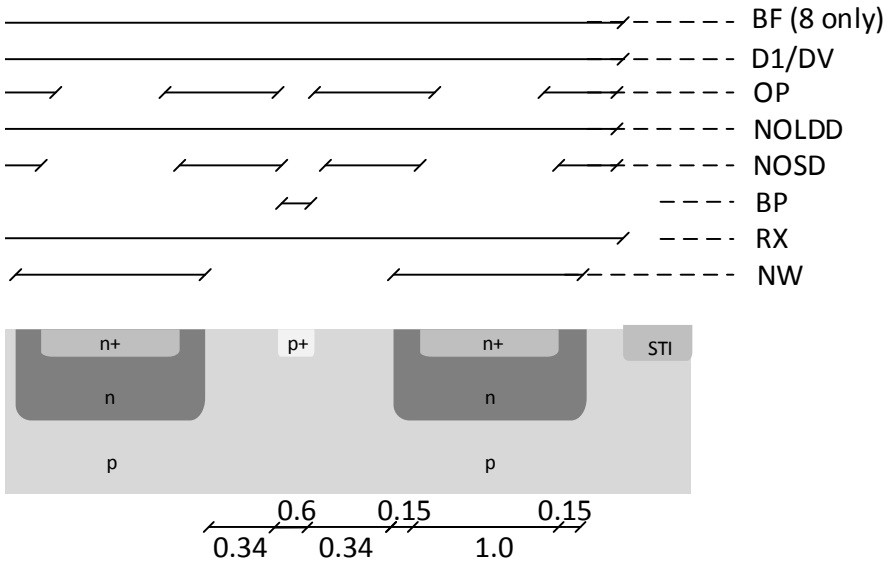
Figure 2.12: Layout quarter and mask stack of structures 4, 5, and 6

Structures 8 and 9

These are the only structures, which do not have a p+ diffusion on the n-well. Both use the same n-well pattern, which is basically the 40.7 µm x 40.7 µm n-well with 60 additional cut-outs. The rectangle cut-outs are equally distributed across the well using the minimum allowed spacing. The purpose of this cell array is to show the impact of an increased lateral area of the n-well to substrate junction. Furthermore, structure 8 has the BF mask to form a lighter substrate doping.



(a) Symmetric layout quarter



(b) Mask stack

Figure 2.13: Layout quarter and mask stack of structures 8 and 9

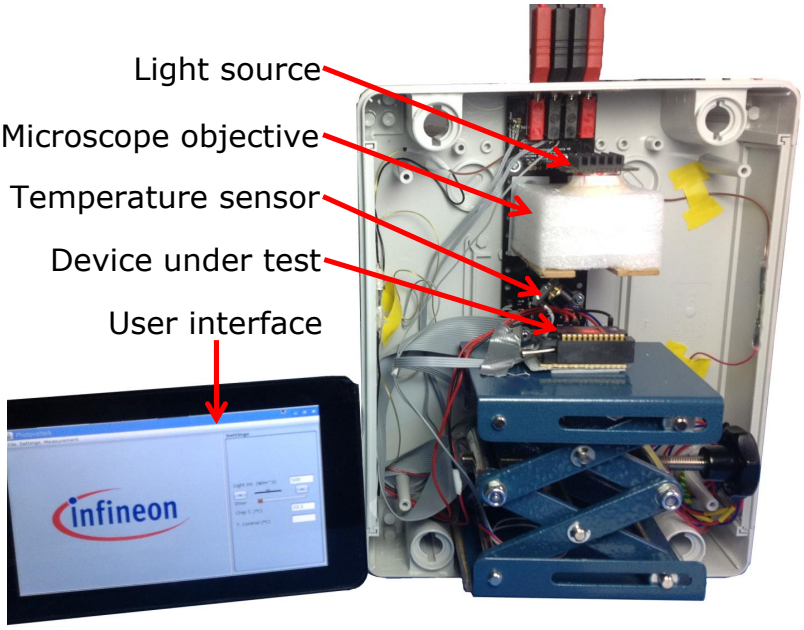


Figure 2.14: Photovoltaic characterization setup showing the measurement enclosure (right) and the controlling user interface (left). During measurement the housing is closed. Picture from [32].

2.3.4 Solar Test Setup

The solar test setup build is based on the standardized setup described in *IEC 60904-1:2006 Photovoltaic devices - Part 1: Measurement of photovoltaic current-voltage characteristics* and also on the *ISO 9845-1 Reference solar spectral irradiance at the ground at different receiving conditions*. Nomenclature and general requirements for a solar test setup have been adopted. The IEC 60904-1:2006 *Describes procedures for the measurement of current-voltage characteristics of photovoltaic devices in natural or simulated sunlight. Lays down basic requirements for the measurement, defines procedures for different measuring techniques in use and shows practices for minimising measurement uncertainty.*[*] A photo of the solar test setup with opened enclosure is depicted in Fig. 2.14. The test setup was built as a part of a Bachelor Thesis [32] supervised during this work.

Derived requirements for the test setup of this work are

- Proper selection of light sources
- Possibility to use different light sources
- Regulated irradiance
- Reproducible results

[*] Abstract from IEC 60904-1:2006

Light sources have been selected to cover a spectrum from ultra violet (UV) to near infrared (NIR). Due to redundant measurement results, the wavelengths of the blue and green source have been sorted out from the results section of this work. In table 2.4 the light sources and their corresponding wavelengths are depicted. All sources have been characterized in terms of their lower and upper half width, respectively, using an "USB-650 Red Tide Spectrometer". The lower and upper half widths are the wavelengths of the spectrum at which the spectral curve has doped to 50 % its peak value.

Table 2.4: Selected light sources and measured corresponding wavelengths at half width intensity.

Light Source	λ_l [nm]	λ_u [nm]
UV LED	393	407
Blue LED	453	467
Green LED	507	533
Red LED	623	637
NIR LED	930	950
White LED	430	620

Where λ_l and λ_u are the lower and upper wavelength, respectively, of the measured full width half maximum spectrum.

Regarding the measurement technique typically two different characterization methods are used by solar test laboratories. The first is a pulsed light measurement. This setup uses a light source, which is switched on only for short periods in which the measurement is done. The second method uses steady state light. The advantage of the pulse method over the steady state method is the reduced heating of the DUT (DUT refers to the solar cell test chip) caused by sunlight simulators. A reduction of the solar cell heating generally benefits the reproducibility of the measurement results. For the solar cell tests is this work, a precise measurement in the nA and sub mV scale is mandatory, because of the low power levels that are achieved. Accurate measurements in this scale already require precision measurement equipment as well as a reduction of the noise floor by setting a proper value for the number of power line cycles (NPLC) parameter to at least 1. The small enclosure, in which the setup is built, also warms up during a complete characterization process. Although warming inside the enclosure, it was decided to use no active cooling fan to keep the enclosure totally sealed, because of dust and uncontrolled light contamination. For constant temperature of the DUT an active cooling and heating socket for test chip is built and used for longer test runs. The heating and cooling is done by a Peltier element in combination with an H-bridge. The H-bridge allows switching between cooling and heating by changing the current direction through the Peltier element. A 10 bit pulsewidth modulation (PWM) signal is used to control the heating and cooling power, respectively. A contactless IR thermometer measures the solar cells temperature and a PI-controller is used to set the duty cycle of the PWM. Besides the temperature also the position of the chip has influences on the measurement results. To minimize this influence the distance between the light source and the DUT is set to the same value after changing the source or the DUT. In addition to the distance also the position on

the height adjustable table falsifies the results. Therefore, a collimating lens is placed between the light source and the DUT to create a homogeneous light spot.

For reproducibility also the light sources have been characterized in terms of their irradiated light power and spectrum. This is typically done by using power-calibrated equipment suitable for the given wavelength. By knowing the irradiated power per area the outer quantum efficiency of the solar cells can be calculated. However, calibrated equipment was neither available at university nor at Infineon during the time this work was done, therefore an uncalibrated spectrometer was used. To overcome this problem a known light source namely a 1000 W tungsten light bulb in a defined distance of 255 mm was observed with the uncalibrated spectrometer. The measured light bulb spectrum and the intensity given in units of counts, see Fig.2.15, where further used to derive a calibration coefficient for the spectrometer. In a first attempt the irradiance of the light bulb was calculated using the following equations:

$$A = 4\pi r^2 \qquad ; \qquad P'_{bulb} = \frac{P_{bulb}\,\eta}{A} \qquad ; \qquad P'_{bulb} = \frac{P_{bulb}\,\eta}{4\pi r^2} \tag{2.3.1}$$

Where A is the surface of the light propagation, which is assumed to be spherical, r is the distance between the spectrometer and the tungsten filament, P'_{bulb} is the irradiated light power, P_{bulb} is the electrical power, and η is the efficiency of the light bulb. In a next step, the irradiated power is used to calculate the calibration coefficient κ, which converts the units of counts over the wavelength into Watt per m^2. The integration is done numerically with MATLAB based on the measured spectrum data.

$$P'_{bulb} = \int_{\lambda_1}^{\lambda_2} p(\lambda) d\lambda\, \kappa \tag{2.3.2}$$

Where λ_1 and λ_2 are lower and upper wavelength-bounds of the measured spectrum, $p(\lambda)$ represents the numerically measured data from the spectrometer, and κ is the proportional coefficient.

$$P'_{LED} = \int_{\lambda_1}^{\lambda_2} p(\lambda) d\lambda\, \kappa \tag{2.3.3}$$

After κ is known, the optical power generated by the LED light sources can be calculated using the measured spectra, see equation 2.3.3. The results of this method, however, where not used to characterize the solar cells efficiency. Reconsidering the measurement method lead to the assumption, that the uncertainty of the calculation would produce a non-negligible error and therefore absolute efficiencies of the solar cells have not been published and are no part of this work. Instead, another commonly used figure of merit (FOM), namely the fill factor (FF), was published and is used in this work to describe and compare the solar performance. A comparison of the different solar cell structures can be made without knowing the generated power per area when using the same settings and light sources. Another problem of the above described calibration method is the assumption of κ of the spectrometer being constant

for different wavelengths. This assumption is also an approximation, because the sensor of the spectrometer has a wavelength dependent sensitivity. A first oder approximation of the uncertainty is given in equation 2.3.4 assuming the following values:

- $P_{bulb} = 1000\,W \pm 20W \equiv \pm 2\,\%$
- $\eta = 0.02 \pm 30\%$
- $r = 0.255\,m \pm 10\,mm \equiv \pm 4\,\%$

$$\Delta P'_{bulb} = \left|\frac{\partial P'_{bulb}}{\partial P_{bulb}}\Delta P_{bulb}\right| + \left|\frac{\partial P'_{bulb}}{\partial \eta}\Delta \eta\right| + \left|\frac{\partial P'_{bulb}}{\partial r}\Delta r\right| \tag{2.3.4}$$

Resulting in a total uncertainty error of approximately 9.75 Watt per m^2 which corresponds to a relative error of 39.8 % for the calibration source. Due to this large uncertainty, the solar cell efficiency is not measured and the fill factor, see chapter 2.3.5, is used to compare the cells of this work to others.

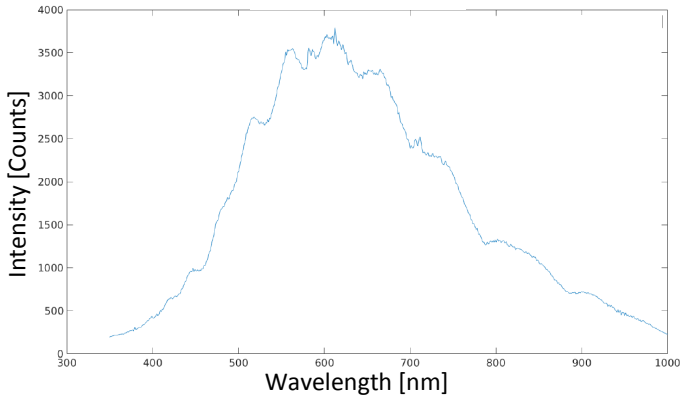


Figure 2.15: Spectrum of a 1000 W tungsten light bulb. Intensity is given in counts, because the spectrometer is uncalibrated.

Another consequence of the expected large uncertainty of the irradiation measurement is that the characterization of different solar cell types is related to the electrical power. Instead of using the irradiated power per area, the electrical power of the LED light sources is the highly reproducible sweep parameter of the setup.

After a complete measurement cycle at different incoming light intensities the automated control program writes the data into a matrix. A visualization of the total measurement cycle results is plotted in Fig. 2.16. The data shows characterization of one solar cell type at one specific light source.

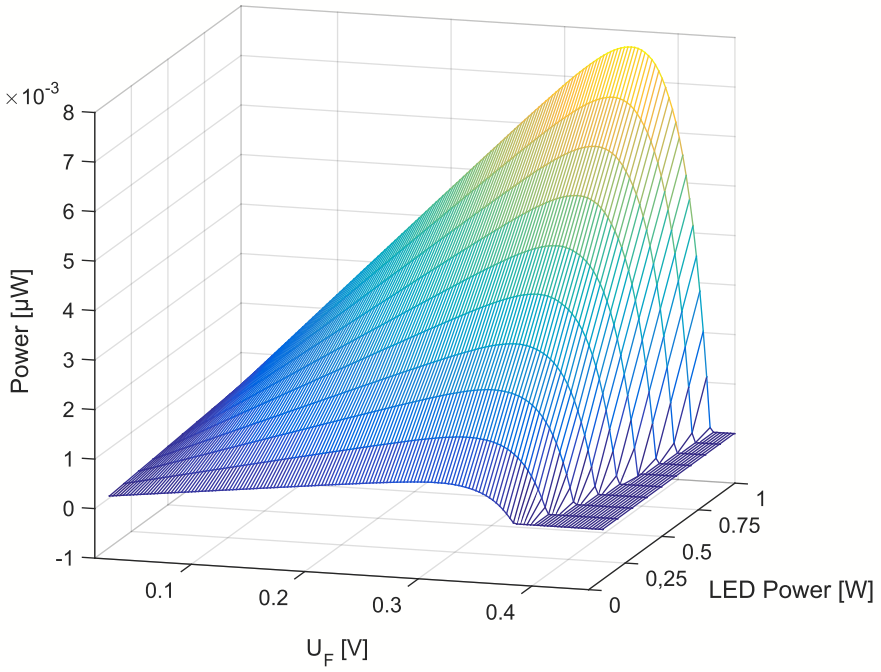


Figure 2.16: Measurement result visualized by the automated MATLAB script showing the solar cell output power as function of the forward voltage and the electrical input power of the light source. Controlling the measurement equipment as well as data processing is done by the MATLAB script

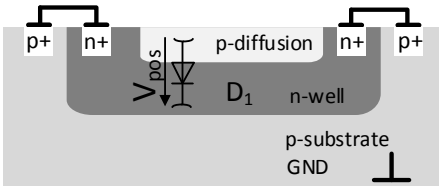
2.3.5 PDC1 Measurement Results

All measurements are performed at room temperature, if not explicitly stated otherwise. Basically two different connection schemes can be used, see Fig. 2.17. The supply connection shorts the n-well to ground, Fig. 2.17a. In this connection scheme the resulting voltage is positive and can directly be used to supply the harvester itself. Structures 4, 5, and 6 are designed to find the best performing device for this supply connection. Due to the limited number of pads on this small test chip, structure 4, 5, and 6 therefore share the same bond pad for the n-well connection. The supply connection makes use of the p-diffusion to n-well junction D_1.

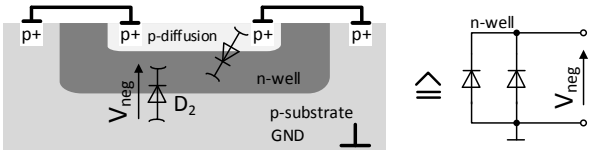
The harvesting connection scheme, see Fig. 2.17b, connects D_2 and D_1 in parallel to increase the generated photocurrent. In this connection scheme the resulting voltage is negative with respect to ground and can only be used as harvesting source by taking additional effort.

Neglecting the sign of the generated voltage both connection schemes produce electrical power. Hence, all measurements in this work regarding the on-chip solar performance use

the active sign convention, resulting in a positive number of the power flowing out of the solar cells for both schemes.



(a) Positive output voltage connection. D_2 is shorted. This configuration is further named as supply connection sheme.



(b) Negative output voltage connection. D_2 and D_1 are in parallel to increase the overall power. This configuration is further named as harvesting connection scheme.

Figure 2.17: Harvesting and supply connection scheme used for the solar performance measurements. Using the active sign convention both connection schemes deliver a positive power value.

Harvesting Connection Scheme

Structures 8 and 9 are using a grid like cut-out n-well as depicted in Fig. 2.13b. In comparison to 1 and 7 the n-well openings are much smaller and narrower. However, 8 and 9 deliver at 0 Volts a short circuit current in the same order of magnitude as the other harvesting cells do. Increasing the voltage across the junction, linearly decreases the photocurrent for both structures, see Fig.2.18. Because of the low voltage range the output power is not comparable to those of the other harvesting cells on PDC1.

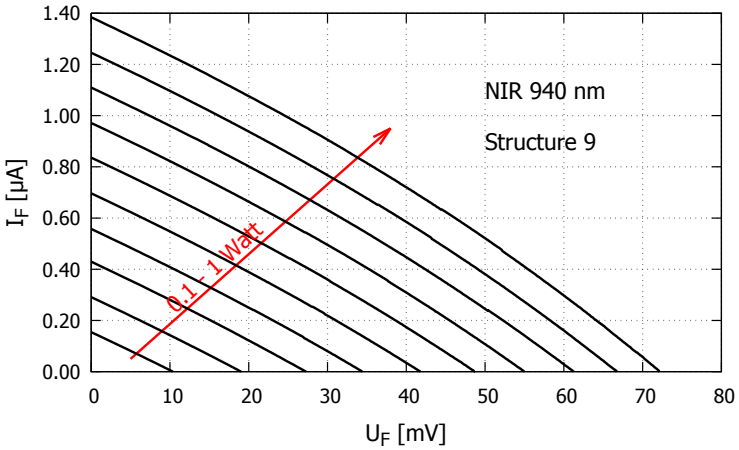


Figure 2.18: Photocurrent as function of the forward voltage measured at structure 9. Structure 8 shows a similar behavior. The short circuit current scales linearly with illumination power, while the UI curve is also almost linear. NIR light source from 100 mW to 1 W.

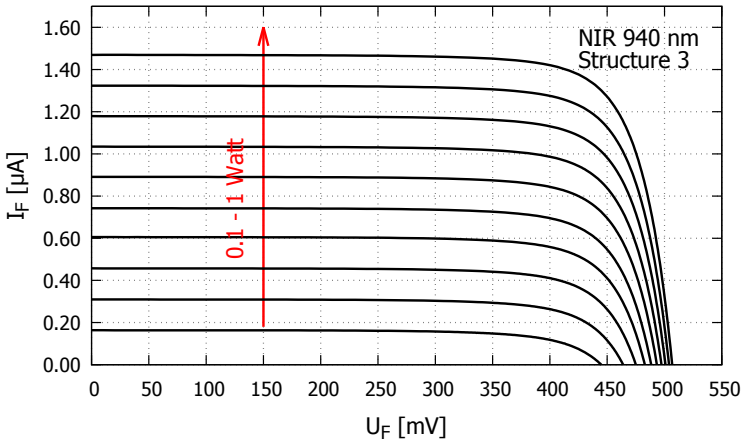


Figure 2.19: Photocurrent as function of the forward voltage measured at structure 3. NIR light source from 100 mW to 1 W.

The low performance of structures 8 and 9 can be modeled by an ohmic path between the two cell terminals. A parallel shunt resistor in the range of approximately 51 kΩ would lead to the very same characteristic on a working cell. The resistive parallel path does not depend on voltage. Further no influence on the resistance caused by the illumination is observed. Therefore, a layout problem generating this resistive shunt path is most likely the reason for the performance problem, while a latch-up is unlikely. The resistive shunt path parallel to the junction is most likely generated in the narrow n-well cut-outs. In this cut-out areas the p-diffusion contact is placed. Hence, in every n-well cut-out there is also a silicide block opening, which is drawn slightly larger than the contact area. It is assumed that the ohmic path between the substrate and the n-well is caused by the narrow width between the n-well junction and the silicide block opening. For comparison, the UI curve of the reference structure 3 is depicted in Fig. 2.19. Because of performance problems of 8 and 9, the harvesting connection scheme is tested only with structures 1, 2, 3, and 7, depicted in Fig. 2.22 to Fig. 2.25. It should be mentioned here that all 9 solar unit cells violate several design rules of the process, because the solar cell is not designated as a device on a CMOS chip.

To compare the harvesting cells 1, 2, 3, and 7 only the maximum power point (MPP) as a function of the illumination is depicted in Fig. 2.22 to Fig. 2.25. The MPP of every structure is calculated by the UI values and normalized to 1 mm^2. In Fig. 2.20 the output power as a function of the cell voltage under NIR light is depicted in detail. The MPP for every illumination condition is marked with a red circle.

The characterization measurements of the cells also show a strong dependency on the connection of the neighboring cell structures. For floating neighbor cells the output power is significantly higher than for grounded neighboring cells. It is assumed that grounded cells structures drain photocurrent from the structure under test. However, the influence of the neighbor structures also shows a dependency on the wavelength. Therefore characterization

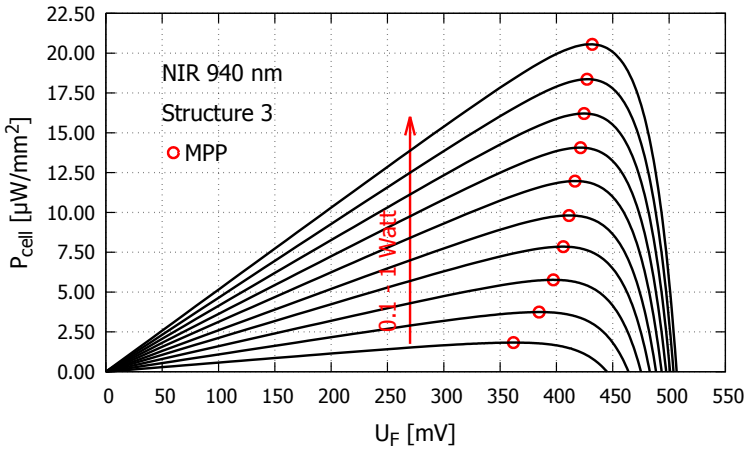
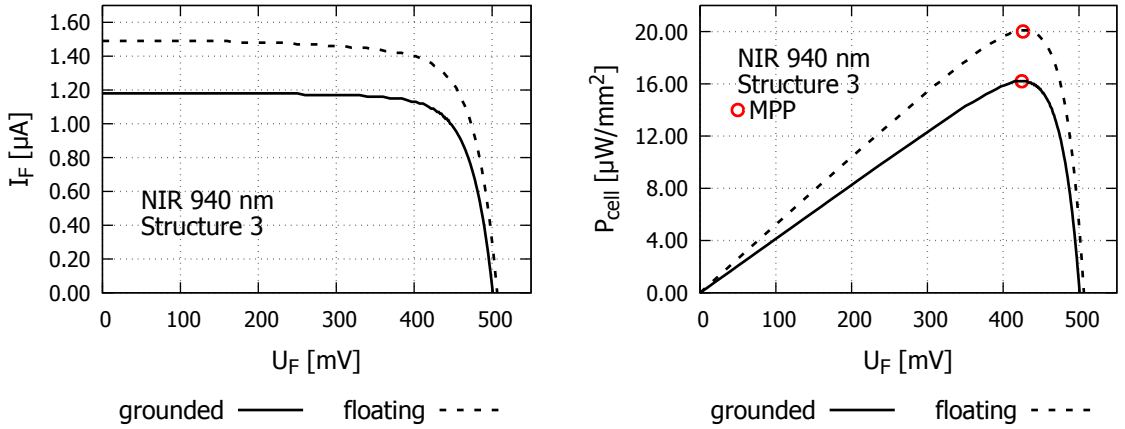


Figure 2.20: Output power as function of the forward voltage measured at reference structure 3. The red circles indicate the MPP for a given LED input Power. NIR light source from 100 mW to 1 W and grounded neighboring cell structures.

measurements for floating and for grounded neighboring cell structures using different wavelengths are made. In Fig. 2.21 the influence of the neighbors is depicted in detail for structure 3 at constant illumination.



(a) The connection of the neighboring cells mainly influences the photocurrent, while the open circuit voltage remains.

(b) The MPP is significantly reduced by grounded neighbors.

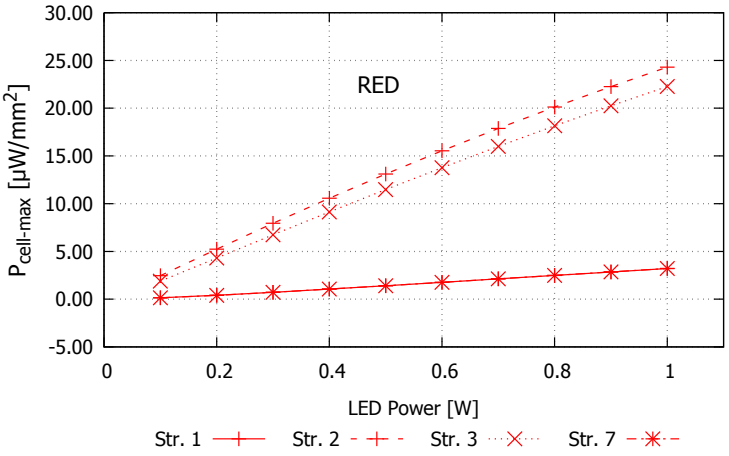
Figure 2.21: Comparison of structure 3 under same environmental conditions between grounded and floating neighboring solar cells. NIR LED at 800 mW.

Fig. 2.21a shows the short circuit photocurrent reduction from 1.5 µA to 1.2 µA if neighboring structures are grounded. The open circuit voltage is not affected by the neighbors, which leads to the assumption of before mentioned current draining by grounded surrounding cells. A

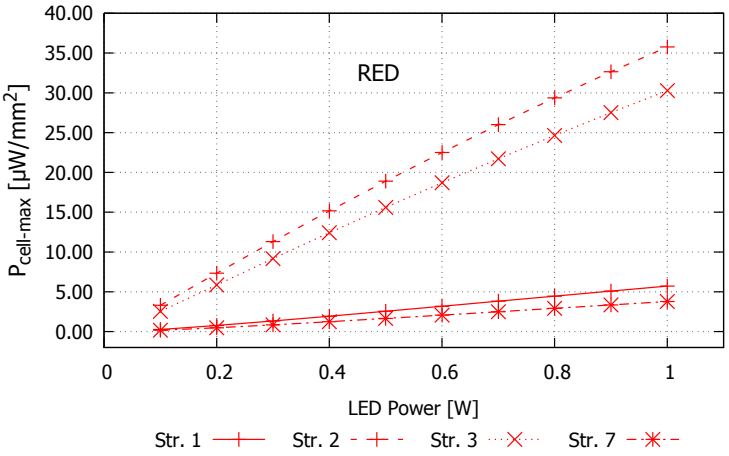
comparison of the MPP measurements support the assumption of drained current, because the MPP is also not shifted in voltage. While the MPP remains on the same voltage, the amount of generated power decreases significantly. Hence, the environment of the solar area on a monolithic harvester chip has to be designed avoiding narrow implants.

Besides the significant power reduction another effect caused by the neighboring cells is observed. While structures 1, 2, 3, and 7 have different efficiencies, respectively, these differences become negligible if the surrounding cells are shorted. Structures 1 and 7, which differ only in the use of the BF mask see 2.3.3, show the same efficiency for all tested wavelengths if the neighbor cells are shorted. Under floating conditions structure 1 (without BF mask) is always better performing than structure 7. Therefore, the lightly doped substrate which is used for structure 7 will not be utilized for the monolithic harvesting chip.

Structures 2 and 3 which were initially placed on the test chip to serve as reference cells, have the best performance. Depending on the wavelength, the output power is 5 to 7 times higher at the simple reference structures compared to the best non-reference structure. They do not have narrow placed junctions or close ohmic contacts, which should make use of the lateral photocurrent. Structure 2 also has no hard-passivation opening. The purpose of structure 2 was to measure the effect of additional absorption in the hard-passivation layer. See 2.3.3 for mask details. However, as measurement results show, the overall best performance is achieved by the reference structure 2 utilizing the hard-passivation coating on top. For long wavelengths in the NIR and red part or the light spectrum and also for the mixed spectrum white LED, the hard-passivation significantly increases the cell's efficiency, see Fig. 2.22, Fig. 2.23, and Fig. 2.25. Measurements using short length UV light show better efficiency for structure 3 over structure 2, see Fig. 2.24. A FOM increase of 3.2 % at NIR and a decrease of 0.7 % at UV is observed, see Fig. 2.33. Under UV light the overall achieved output power is reduced by approximately 90 % compared to long wavelengths which makes the advantage of structure 3 for the harvesting purpose negligible. The increased over all efficiency of the hard passivated structure 2 over structure 3 is most likely caused by the anti-reflective property. The anti-reflection property of the hard-passivation, which is also a function of layer thickness, matches the requirements for wavelengths longer than the tested UV light. In Fig. 2.8a a slight color difference can be seen comparing structures 2 and 3 caused by the hard-passivation. The other effect the passivation can have on the solar cell is the impact on the charge carrier lifetime until recombination reported among others by [33]. For our test chip the reported charge carrier lifetime extension due to passivation is the minor effect, because the passivation is on top of the metal layer stack and the silicon oxide in a distance approximately 6 µm from the junction.

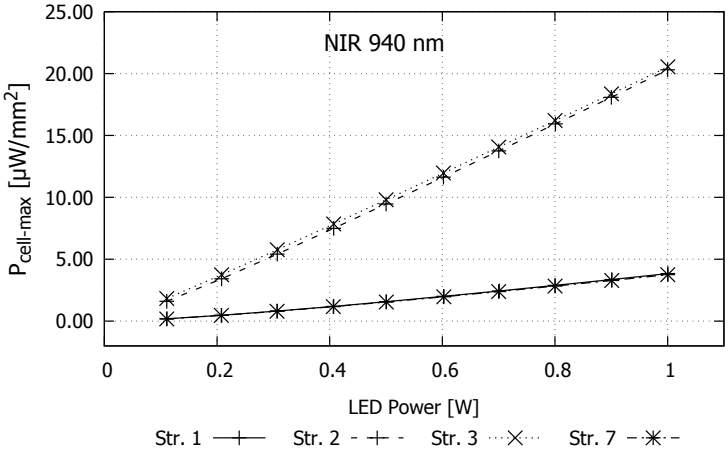


(a) Area related solar output power with grounded neighboring cells

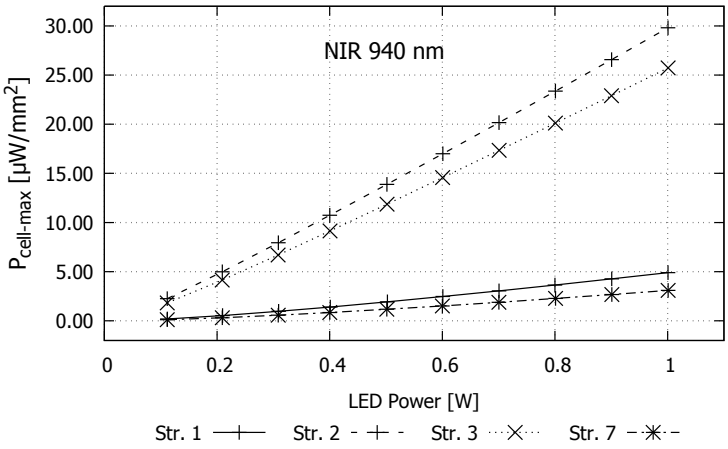


(b) Area related solar output power with floating neighboring cells

Figure 2.22: Solar cell structure response to red LED light normalized to one mm^2. The connection of neighboring solar cell structures strongly influences the measurement results. Measured in harvesting connection scheme.

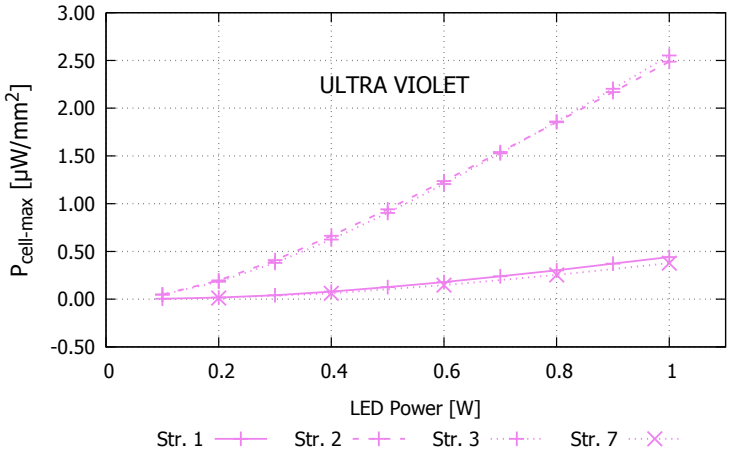


(a) Area related solar output power with grounded neighboring cells.

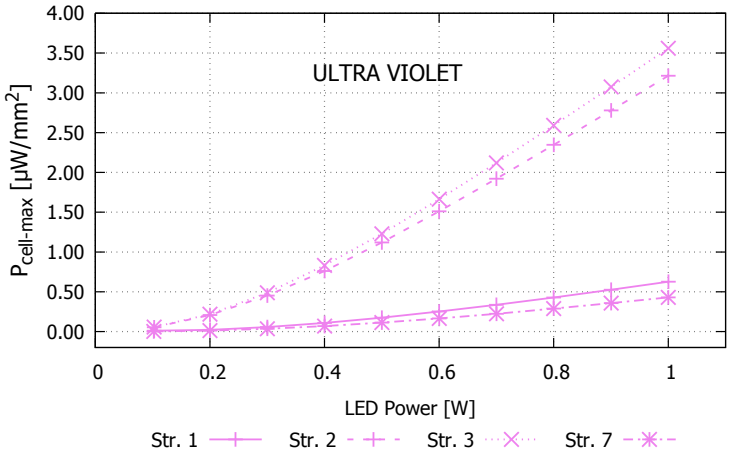


(b) Area related solar output power with floating neighboring cells

Figure 2.23: Solar cell structure response to NIR LED light normalized to one mm^2. The connection of neighboring solar cell structures strongly influences the measurement results. Measured in harvesting connection scheme.

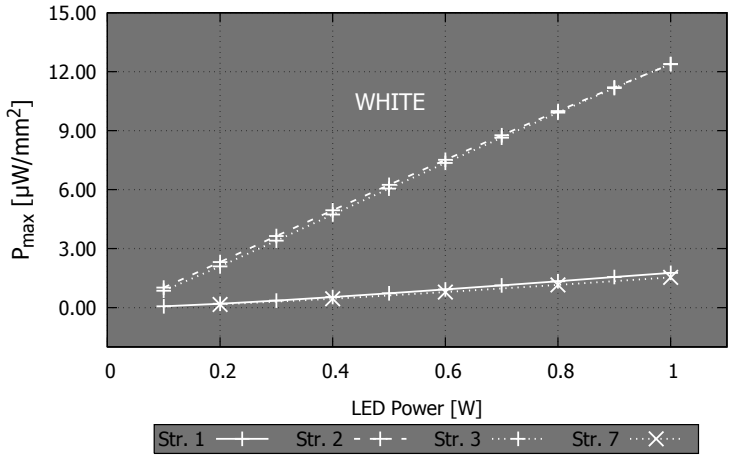


(a) Area related solar output power with grounded neighboring cells

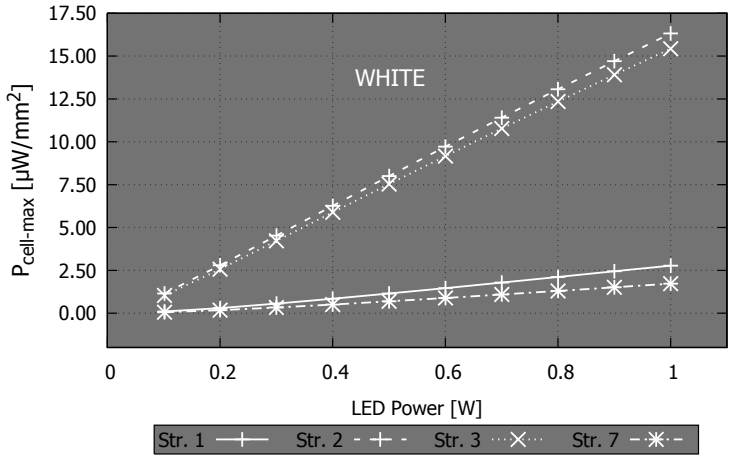


(b) Area related solar output power with floating neighboring cells

Figure 2.24: Solar cell structure response to UV LED light normalized to one mm^2. The connection of neighboring solar cell structures strongly influences the measurement results. Measured in harvesting connection scheme.



(a) Area related solar output power with grounded neighboring cells



(b) Area related solar output power with floating neighboring cells

Figure 2.25: Solar cell structure response to white LED light normalized to one mm^2. The connection of neighboring solar cell structures strongly influences the measurement results. Measured in harvesting connection scheme.

Due to the significantly higher performance of structures 2 and 3 further measurements will only be done with these cells, because these structures will also be used for the monolithic harvester chip. The harvesting connection scheme, see Fig. 2.17b, in which D_2 and D_1 are connected in parallel was assumed to produce the highest power output per area. However, there are two other possibilities to connect the p-diffusion in addition to the proposed harvesting connection scheme. The first is a floating p-diffusion and the second is a connection of p-diffusion and n-well. A comparison of the harvesting connection scheme to the floating diffusion and the diffusion to well connection is given in Fig. 2.26. The before mentioned connection schemes are tested using light sources from NIR to UV and are normalized to the power generated by the harvesting connection scheme, see 2.3.5. Where $P_{Harv-Conn}$ is the output power using harvesting connection, $P_{Diff-Float}$ is the output power with floating p-diffusion, and $P_{Diff-Well}$ is the output power with p-diffusion connected to n-well.

$$\frac{P_{Diff-Float}}{P_{Harv-Conn}} \cdot 100 \qquad \text{and} \qquad \frac{P_{Diff-Well}}{P_{Harv-Conn}} \cdot 100 \tag{2.3.5}$$

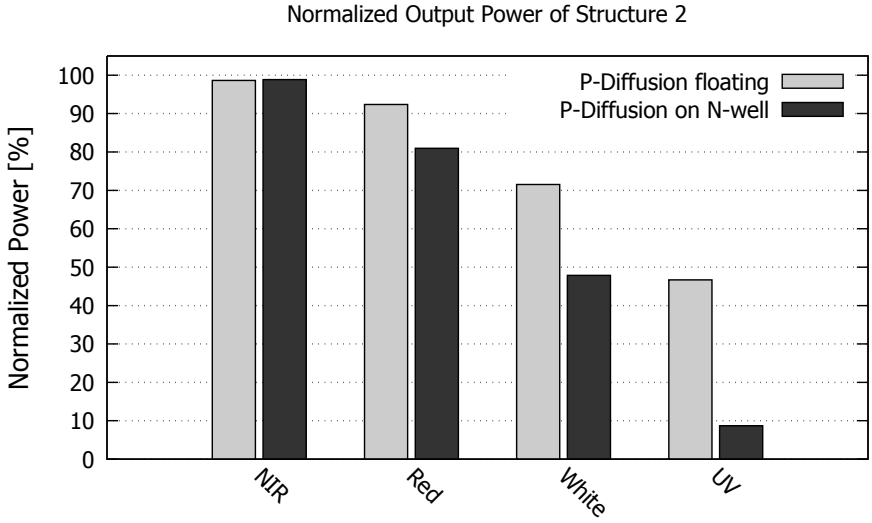


Figure 2.26: Output power of structure 2 normalized to the harvesting connection scheme, see (2.3.5). For longer wavelengths with high penetration depths the diffusion on the surface has less effect while for short wavelengths D_1 in parallel to D_2 is mandatory.

The normalized output power depicted in Fig. 2.26 shows a significant loss in output power performance for short wavelengths if the p-diffusion is not connected to the substrate. Due to the higher penetration depths of longer wavelengths the parallel connection of D_1 and D_2 becomes negligible in the NIR regime. For UV light an output power reduction to less than 50% for floating p-diffusion and to less than 10% for diffusion shorted to n-well is observed. These results lead to the design decision of using both junctions in parallel to cover the full light spectrum with highest possible efficiency.

Fill Factor - FOM

To compare the performance of the on-chip solar cells of this work to cells of other publications or to State-of-the-Art (SOTA), the fill factor (FF) is used. Besides the output power normalized to the area also the FF is an established figure of merit (FOM), as published by Green [34] among others. While efficiency measurements require a calibrated light source and test environment, the FF is strongly influenced by parallel and series resistances, and the ideality factor of the cell itself. It is also widely independent from the incoming light power. Therefore the FF is used to determine and compare the performance of the solar cells produced in the CMOS process to other publications, because efficiency measurements are barely available for ultra-low power CMOS solar cells. The FF is calculated by dividing the maximum power point value by the virtual power given by the open circuit voltage multiplied by the short circuit current, see 2.3.6.

$$\frac{P_{MPP}}{P_{virtual}} \cdot 100 = \frac{U_{MPP} \cdot I_{MPP}}{V_{OCV} \cdot I_{SC}} \cdot 100 = \frac{A_1}{A_2} \cdot 100 \qquad [\%] \tag{2.3.6}$$

Where U_{MPP} and I_{MPP} are the voltage and current at maximum output power respectively, V_{OCV} is the open circuit voltage, and I_{SC} is the short circuit current. Hence, a FOM ≤ 1 can be achieved and an ideal lossless solar cell would have a FF equal to 1.

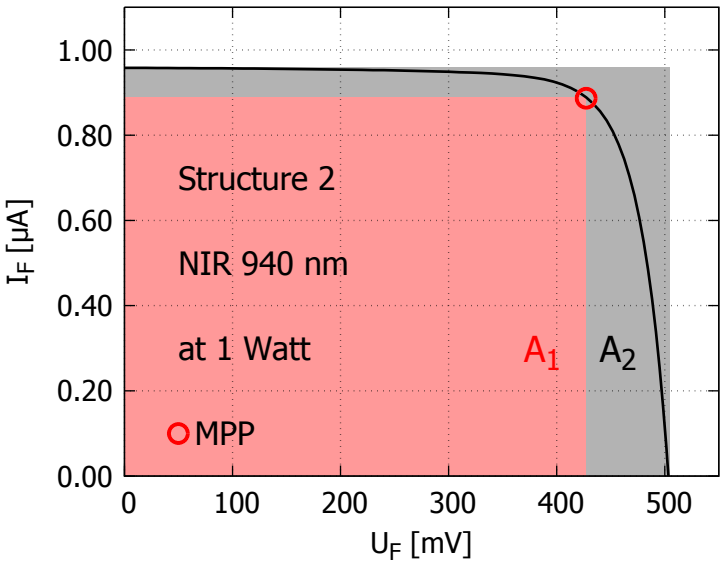


Figure 2.27: The FF according to 2.3.6 of structure 2 under NIR 940 nm at 1 Watt LED power is 78.6 %. Measured at harvesting connection scheme and floating neighbor cells. $U_{MPP} = 0.427\,V$, $I_{MPP} = 0.8887\,\mu A$, $U_{OCV} = 0.5045\,V$, and $I_{SC} = 0.9580\,\mu A$

The highest reported FF values depicted in 2.28 are not fabricated in a CMOS process. To achieve FF values as reported in [35, 36, 37], solar cell optimized processes are used. However,

in comparison to published data of the CMOS solar cells from [7], the best structures of this work show a significantly higher performance. In Fig. 2.28 measurement results from structure 2 in harvesting connection are depicted.

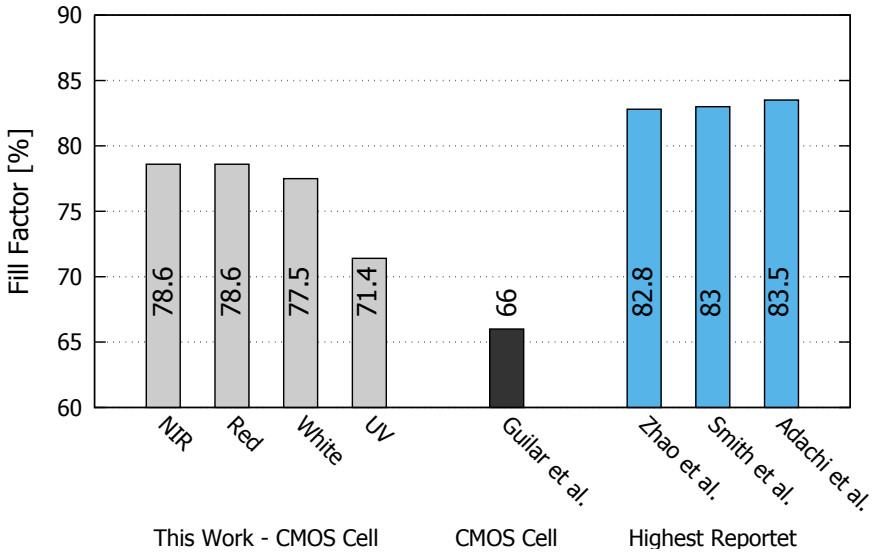


Figure 2.28: Fill factor comparison of structure 2 to other CMOS solar cells [7], and to highest reported values of multi-layer cutting edge solar cells [35], [36], [37].

Supply Connection Scheme

The supply connection scheme, see Fig. 2.17a shorts the n-well to ground. In this configuration only the p-diffusion is used and the much higher photocurrent generated by the n-well implant is shorted. The resulting voltage of the diffusion with respect to substrate is positive, which allows a direct use as supply for low-voltage and low-power circuits as well as for startup. Similar to the tested harvesting connection scheme, measurement results show a significantly better performance at the implemented test structures 2 and 3. Detailed measurement results are given below. Structure 4 and Structure 5 are not taken into account, because the delivered output power is too low. Both structures (4 and 5) have an ohmic connection between the p-diffusion to n-well in the order of 1 MΩ. Structure 4 and structure 5 are both implemented with an area of 0.01788 mm^2 delivering an short circuit current of approximately 0.1 µA per 0.01 mm^2 under 1 W red LED light. This short circuit current is in the same order of magnitude as the current of structure 2 and 3. Hence, the before mentioned 1 MΩ parallel path, which is most likely introduced by the narrow placed contacts, reduces open circuit voltage and therefore the output power to an unusable level.

Structures 2, 3, and 6 deliver an output power in a range which can be used to supply on-chip circuits. Measurement results of the maximum power points related to the incoming light power and wavelengths are depicted in Figs. 2.29 to 2.32.

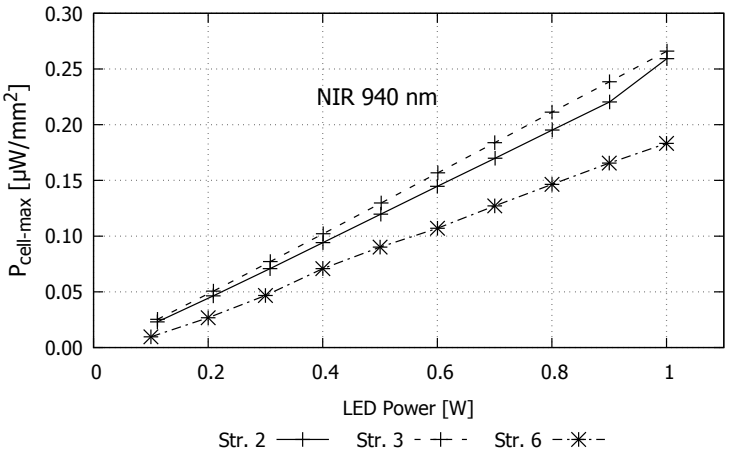


Figure 2.29: Positive Supply Connection NIR

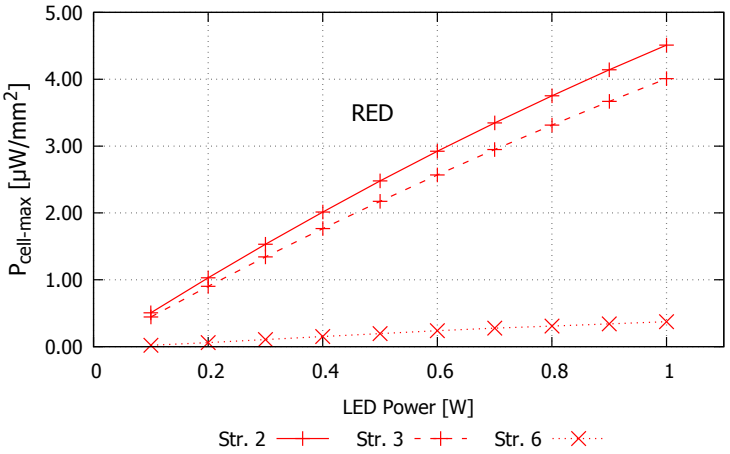


Figure 2.30: Positive Supply Connection Red

Comparing results from Fig. 2.32 to Fig. 2.24b shows that the short wavelength part, according to the theory of penetration depth, is harvested almost only by the close surface junction. For longer wavelengths the efficiency of the supply connection scheme decreases by a factor of 5 to 6 for red light and by a factor of approximately 100 for NIR wavelengths. Tested under natural sunlight, the difference between supply connection and harvesting connection amounts to approximately a factor of 16, see Fig. 2.35. Natural sunlight results have been measured during summertime without clouds, in June, Graz, Austria at noon.

In Fig. 2.33 the FF of structures 2, 3, and 6 for different wavelengths are depicted. For structures 2 and 3 the FOM is again comparable to SOTA and other publications on CMOS solar cells, as it also is using the harvesting connection. Structure 6, although it outperforms 4 and 5, also has a low ohmic parallel shunt resistance, resulting in the much lower output

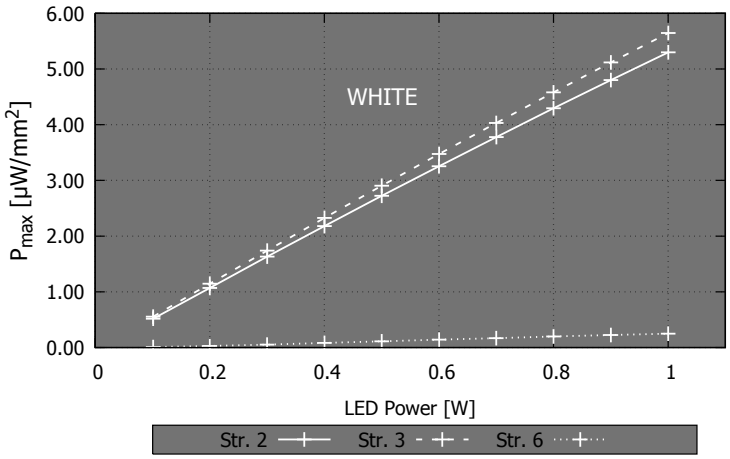


Figure 2.31: Positive Supply Connection white

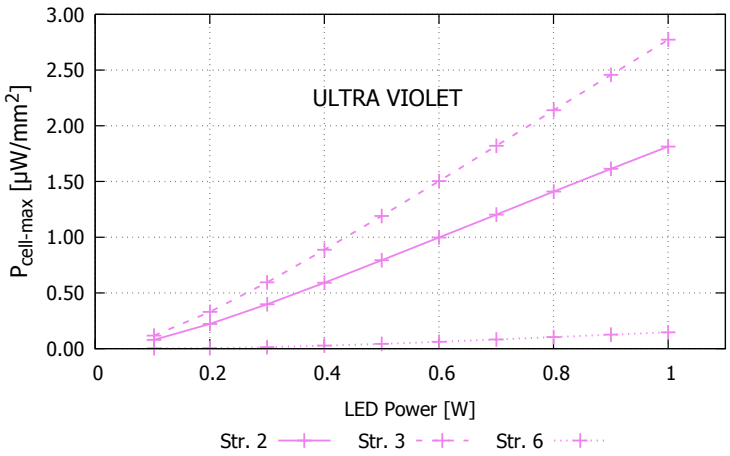


Figure 2.32: Positive Supply Connection UV

power per area as well as a FF below 30%.

Conclusion

Concluding the measurement results for the harvesting and the supply connection scheme, structure 2 is further used as harvesting power source for the monolithic harvesting approach. The narrow junctions as well as the lightly doped substrate cell versions had major disadvantages in terms of efficiency caused by the low open circuit voltage. Characterization measurements of the harvesting diodes D_2 without D_1 in parallel show a similar result of structure 2 and 3 outperforming all other cells. The performance measurements under UV light showed a 50 % higher efficiency at structure 3 compared to structure 2 in supply

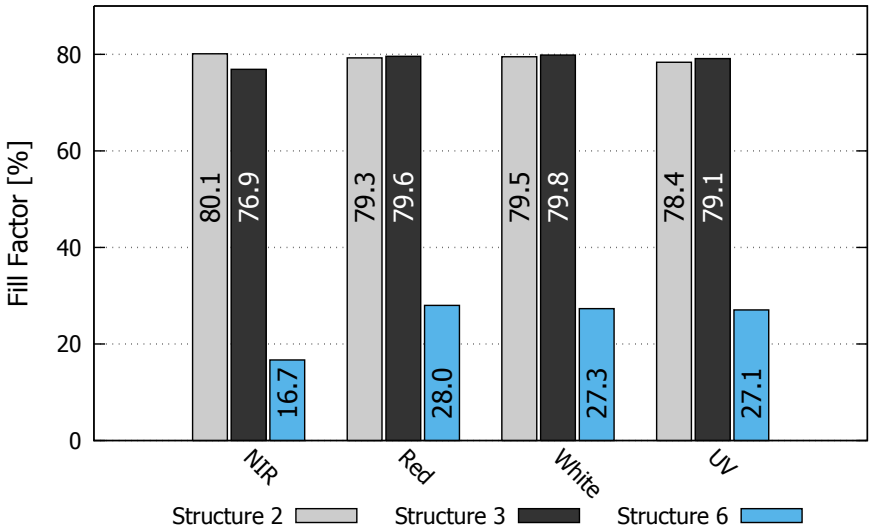


Figure 2.33: Fill factor comparison of structure 2, 3, and 6 for different wavelengths. The difference between structure 2 and structure 3 is the hard-passivation opening of structure 3. The hard-passivation on structure 2 increases the FF when shifting to the red portion of the incoming light.

connection scheme. This behavior, which is caused by the hard-passivation, could further be used in a stand-alone self-sustained UV dosimeter or IoT sensor node. However, the overall performance in terms of generated electrical output power per area of structure 2 is significantly higher than on all other tested structures regarding the harvesting application. The harvesting connection scheme, using both junctions in parallel, leads to an improved efficiency. Due to the wavelength dependent penetration depth the harvesting connection improves the sensitivity for a higher wavelength bandwidth. A FOM comparison to other publications shows that the harvesting cell can compete with standard commercial solar panels in harvesting as well as in supply connection. The direct comparison to other published CMOS solar cells, [7], where a FF was given, shows an improvement of more than 12 %, which leads to the conclusion that the used 130 nm single n-well process also benefits the solar operation. The passivation layer on structure 2 is normally used as additional protection of the chip surface. As measurement results showed, the passivation also increases the output power of the harvesting connection scheme. A higher relative difference between cells 2 and 3 is observed for the supply connection caused by the passivation layer, which mainly affects the UV light. Depending on the application that defines the operating place and therefore the light conditions the passivation can be opened above the supply cells, leading to a higher output power, see Fig. 2.35.

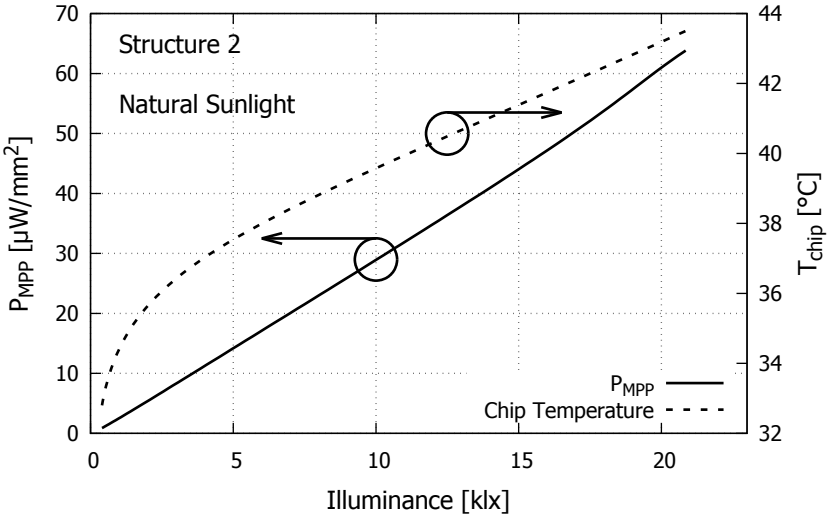


Figure 2.34: Maximum output power of structure 2 under natural sunlight as function of illuminance. As the chip heats up when exposed to sunlight, leading to an decreased efficiency, the temperature is also given.

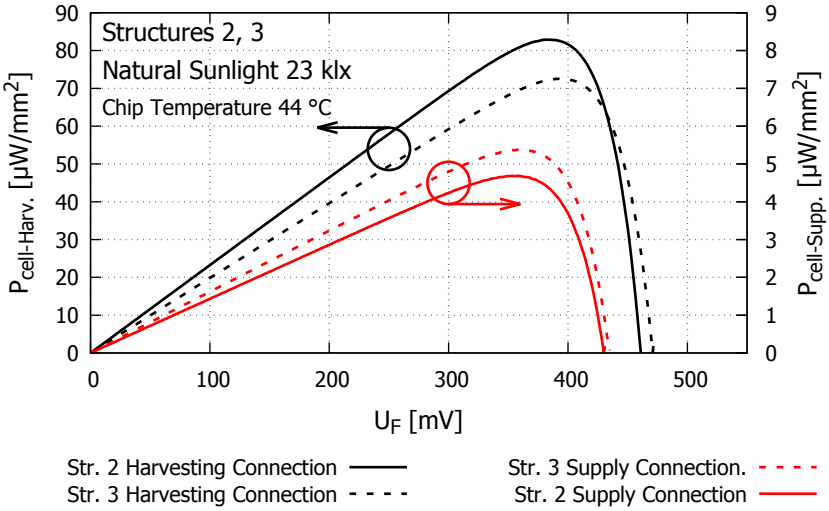
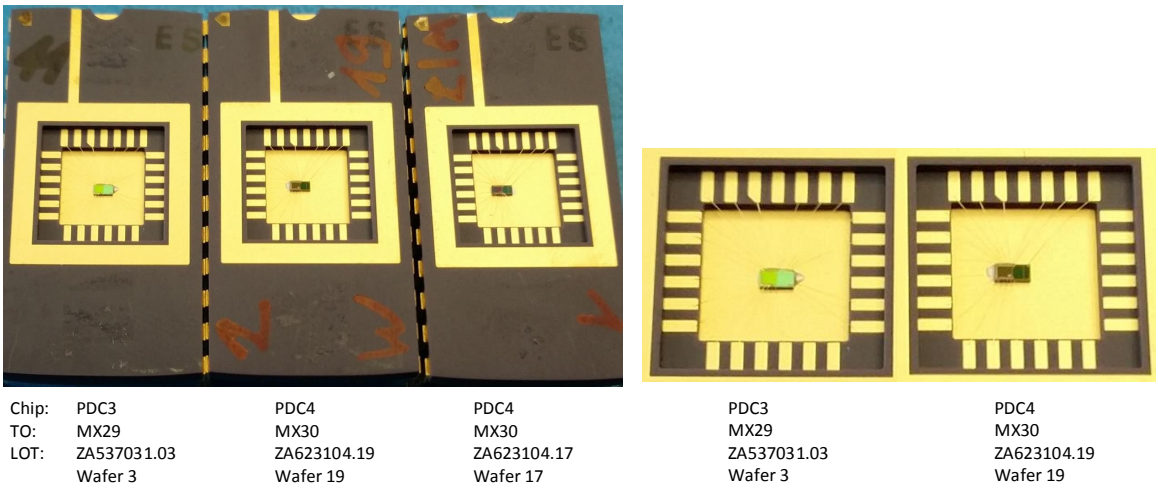


Figure 2.35: UI characteristic of structures 2 and 3 under natural sunlight. The harvesting connection scheme Str. 2 produces approx. 16 times more power per area than Str. 3 in supply connection. The difference between structure 2 and structure 3 is the hard-passivation opening of structure 3. Dotted lines show hard-passivation openings.

2.3.6 The Color Problem

The test chips for the solar cells and the monolithic harvester where always taped out as part of a multi-project wafer or also named shared reticle wafer. Shared reticle tape-out runs are named using the prefix MX followed by the tape-out number. The first test chip of this work was taped out on MX28 which was the solar test chip only, measurement results of this chip are given in section 2.3.2. Based on the findings of the MX28 run, the first monolithic harvester was designed for MX29. The test chip from MX29 is called PDC3.

PDC3 already uses the solar cell structure 2 in a solar array covering half of the chip, while on the other half an early version of the integrated DC/DC converter and the tracking algorithm is placed. By cutting laser fuses, the solar array of PDC3 can be disconnected from the DC/DC converter, which allows characterizing the solar array without interference of the circuit part. Regarding the solar performance the solar-only test chip PDC1 from MX28 and the first monolithic harvester chip PDC3 from MX29 deliver the same output power per area. Achieving the same solar performance at different tape-out runs further supported the idea of on-chip solar cells because of their reproducibility.



(a) PDC3 (MX29) on the left side and PDC4 (MX30) from two different wafers on the right side. PDC4 chips have a brownish color, while PDC3 chips appear blue-green.

(b) Detail micrograph of PDC3 versus PDC4. The newer PDC4 delivers significantly less power in harvesting connection scheme.

Figure 2.36: Surface color difference of two shared reticle tape-outs using the very same layout and mask setup. Photos are taken under same light conditions and same angle.

Due to bug fixing at the maximum power point tracking algorithm and efficiency improvements for the DC/DC converter the PDC3 test chip from MX29 was redesigned to version PDC4 and re-taped on the MX30 reticle run. Changes are made only at the circuit part of the chip, while the solar area uses again an array of structure 2 solar cells. The PDC4 solar arrays are again connected to the circuit part of the chip via laser cut fuses to keep the possibility to measure both parts of the chip separately. Although no layout changes of the solar cell and also no changes regarding the mask order where made, the solar performance of the

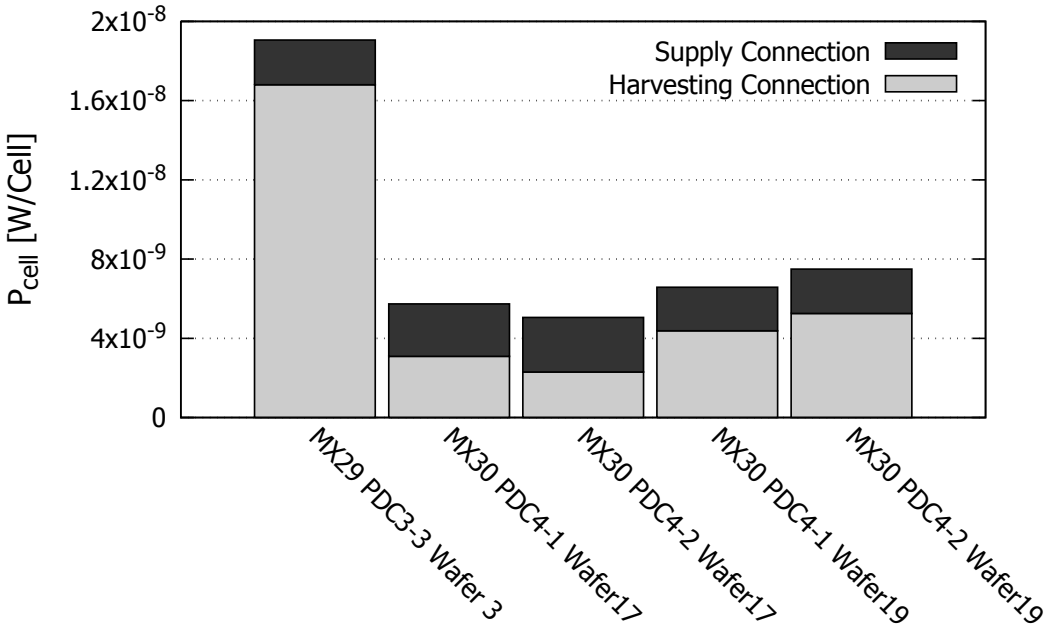


Figure 2.37: Solar performance comparison of test chips from MX29 to MX30.

MX29 and MX30 tape-out runs is significantly different. The first obvious difference can be seen in Fig. 2.36, showing the chip respectively the wafer color. Dies from MX28 and MX29 appear in a blue-green color, while dies from MX30 and ongoing tape-outs appear brownish. The most likely reasons for the color difference, which are different light sources, different die background, or a different surface passivation are eliminated. The additional polyimide passivation, which could cause the surface color change was not ordered on either of the test chips nor processed referring to the semiconductor fabrication plant (FAB) experts. After reviewing the tape-out data together with process experts the conclusion was drawn, that the color difference is caused by a layer thickness change, which does not affect the circuits. The optical properties of the dies however, are significantly different for the test chips from MX30 onwards, as can be seen in Fig. 2.37 and table 2.5.

According to the measurement results, the harvesting connection scheme performance is strongly reduced while the supply connection scheme benefits from the color change. This result leads to the assumption, that the layer thickness change mainly affects the longer wavelengths portion which is collected by the deeper n-well to substrate junction. The diffusion junction of MX30 wafer number 19 achieves results close to MX29, while MX30 wafer number 17 delivers 17 % to 22 % more power per area. The harvesting cell output power is reduced down between 18 % to 31 %.

Table 2.5: Absolute and relative solar performance comparison of MX29 and MX30 test chips. Harvesting and supply connection scheme tested separately.

TO / Name	MX29 PDC3	MX30 PDC4	MX30 PDC4	MX30 PDC4	MX30 PDC4	
LOT	ZA537031.03	ZA623104.17	ZA623104.17	ZA623104.19	ZA623104.19	
Supply	2.26 n	2.65 n	2.75 n	2.20 n	2.24 n	[W/Cell]
Connection	100	117	122	97	99	[%]
Harvesting	16.8 n	3.09 n	2.30 n	4.38 n	5.25 n	[W/Cell]
Connection	100	18	14	26	31	[%]

Conclusion

In this chapter several scientific investigations of on-chip solar cells have been summarized. According to literature, the effects of different wavelengths regarding the penetration depth and the charge carrier collection probability have been characterized for the used CMOS process. The overall solar cell performance has been investigated in terms of different connection schemes and geometries. Additional to recent publications, also the impact of the hard-passivation on the solar performance has been investigated. It was observed, that the hard-passivation opening is not necessary, if the on-chip solar cell is operated under natural light or at least if the light source is not limited to blue or UV. The achieved FF of the solar cell is also a good indicator for the trade-off between metal contact area and junction area. While a too small contact area increases the contact resistance a too large area shield the light. In this work the FF of the best performing solar cell is 78 % which leads to the assumption, that the solar cell size for a single cell was correctly chosen. It was also shown, that a smaller segmentation of the doping implants, using the minimum widths of the process is not generally beneficial in for on-chip solar cells. However, in contrast to recent publications an un-segmented reference cell has also been implemented which outperformed the segmented structures. Based on the performance studies, which have been carried in an specially designed micro solar cell test environment, a solar cell geometry called structure 2 was chosen for further use. Findings of this first part of the work have also indicated that efficient solar cells with SOTA performance can be produced in the single n-well 130 nm CMOS process. Regarding reproducibility, however, the on-chip solar cell as a device and the process need to be qualified for a productive application. For a proof of concept and the performed scientific investigations, the reproducibility of the solar cell among one production run was sufficient. Measurements performed in the controlled environment revealed the fact, that the used CMOS process subjects large fluctuations of its optical properties. Layer thicknesses would need to be part of process control monitoring (PCM) structures and the solar cell as device needs to be designed according to the existing and new design rules and tolerances. For this work and as a proof of concept however, the on-chip solar cell performs sufficiently. An efficiency change up to 22 % between two production runs clearly indicates the potential for possible future devices which could be implemented using a CMOS process. The findings of this chapter have been presented to an expert audience at the 45th European Solid-State Device Research Conference ESSDERC.

Chapter 3

Maximum Power Point Tracking

The following chapter is based on my scientific investigations regarding maximum charge transfer and implementation possibilities which where presented at the 60th IEEE International Midwest Symposium on Circuits and Systems in Boston MA [11]. The ultra-low power circuits and the principal of operation has been patented [38] (own publications).

In the first part of this chapter the analytic solution for a maximum power transfer from an on-chip solar cell to an energy harvesting interface is presented. A simplified solar cell and charge pump model is used to derive the underlying mathematical equations. Solutions of this differential equation are further used to find the optimum charge pump settings regarding dependencies of the output voltage, illumination, and the parasitic capacitors.

Based on the findings of the theory part, a proper maximum power point tracking algorithm is developed. The implementation of the tracking algorithm is described part wise on transistor level in the second part of this chapter. Measurement results and the tracking efficiency are discussed at the end of the chapter. The power consumption of the developed maximum power point tracking algorithm is the lowest reported so far and is therefore cited by Mr. David Newell et al. in the IEEE Transactions on Power Electronics [39].

For test and optimization of the tracking algorithm, I have built three different test chips, covering the concept, design, and layout. Due to the versatile adoption of the algorithm it is also used for a thermo harvesting approach that was developed within the Seventh Framework Programme funded EU Project "NanoCaTe - Nano-carbons for versatile power supply modules [40]. ■

3.1 Theory of Maximum Charge Transfer

At the beginning it shall be mentioned, that the loss mechanisms which are described later in this chapter are valid for this setup only. Very similar results, however, can be expected if an on-chip charge pump harvests from another power-limited source. In this case the power source is an on-chip solar cell that requires a setup capable of charging at a negative input voltage. The losses which are analytically investigated in this chapter are reduced to the

losses caused by parasitic capacitors. For this analytic investigations it is also assumed that the charge pump does not use diodes to prevent the charge from flowing backwards, but switches with negligible voltage drop. This assumption holds also for the real implementation of the charge pump. Detailed information on the charge pump and the necessary circuitry that was developed in this work is given in chapter 4.

The maximum power transfer from the on-chip solar cells to the output of the harvester can also be described as the capability of the circuit to transfer the maximum possible charge per time to the output into a given voltage. In case of a fully integrated design, the DC/DC converter utilizes a charge pump, in which capacitors get charged at the input source and discharged into the output. The analytic solution of this charge transfer problem uses simplified models of the solar cell and the charge pump to find the optimal parameters to operate the converter.

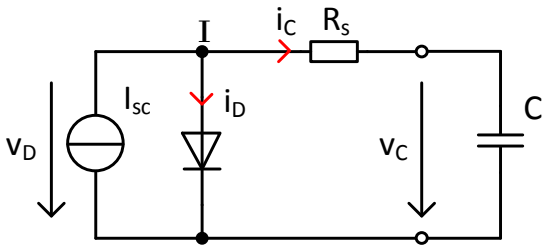


Figure 3.1: Simplified equivalent circuit of a single pn-junction solar cell. This circuit refers to (3.1.1).

$$i_C = I_{SC} - i_D = I_{SC} - i_0 \cdot \left[e^{\frac{(v_C + i_C \cdot R_s) \cdot q}{n \cdot k \cdot T}} - 1 \right] \tag{3.1.1}$$

The simplified solar cell is modeled as depicted in Fig.3.1. Equation (3.1.1) describes the output current of the solar cell as a function the output voltage, where I_{SC} is the short circuit current, R_S is the series resistance, i_0 is the reverse bias saturation current, T is the absolute temperature, n is the ideality factor, and k is Boltzmann's constant. For better handling of the analytic solution the effect of the series resistor R_S is neglected and therefore the short circuit current of the cell is drawn in parallel to the diode. The expression kT/q is later combined to the temperature voltage v_t. Neglecting the minor voltage drop across R_S and connecting a capacitor to the solar cell, the circuit in Fig.3.2 is obtained. It can be seen that the minor impact of R_S is neglected while the main losses of the on-chip capacitors described by α are introduced. Further discussions on the losses follow. The charge pump model of this theoretical approach contains only one capacitive element (inside dashed line) which represents the sum of all pump capacitors summarized at the first stage. Therefore the output voltage is not multiplied and can be understood as a proportional fraction of the real multi-stage charge pump output voltage. Practically, the first stage of the charge pump converts the negative input voltage to a positive voltage, which is for the theoretical observation obsolete.

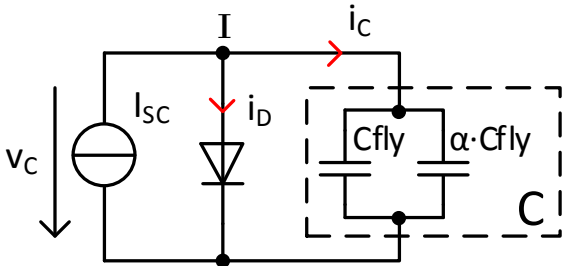


Figure 3.2: Simplified equivalent circuit of the solar cell charging a capacitor. This circuit refers to (3.1.3) which is the equation that describes the currents in node I.

To find a solution of the maximum power transfer problem the current through the capacitor i_C in Fig. 3.2 needs to be expressed, see equation 3.1.2.

The current equation for node I from Fig. 3.2 can be written as:

$$i_C = I_{SC} - i_D \tag{3.1.2}$$

Using (3.1.1) and (3.1.2), differential equation 3.1.3 is obtained.

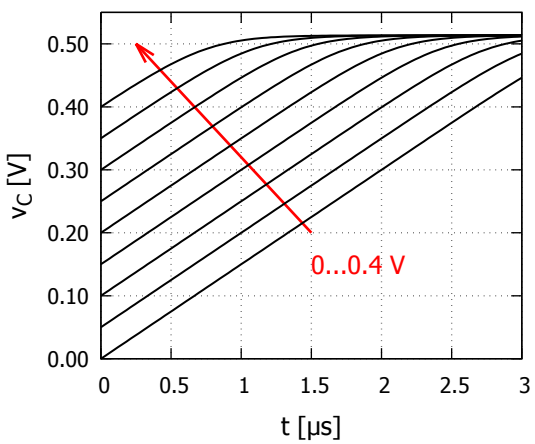
$$i_C = C\frac{dv_c}{dt} = I_{SC} - i_D = I_{SC} - i_0 \cdot \left[e^{\frac{(v_C + i_C \cdot R_s) \cdot q}{n \cdot k \cdot T}} - 1 \right] \tag{3.1.3}$$

The solution of the fist-order nonlinear ordinary differential equation (3.1.3) gives the voltage and current of the capacitor as functions of time. Therefore, the charge transfer as well as the power delivered into the charge pump capacitors as functions of time and further as functions of switching frequency can be calculated. In (3.1.4) the solution of (3.1.3) is depicted. Variable "X" determines the initial condition of the start voltage of the capacitor: $v_C(0) = X$.

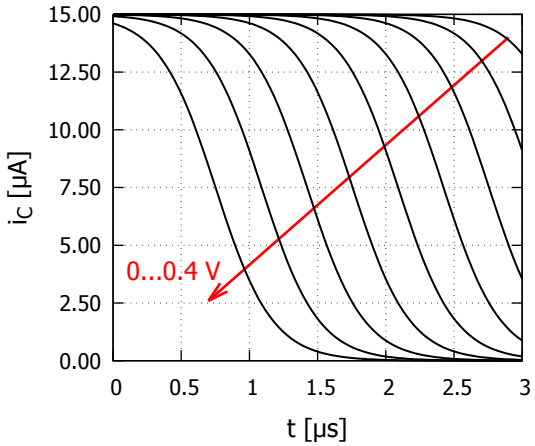
$$v_C = \frac{1}{C}\left[-Cv_t\, n\, log\left[\frac{i_0 e^{\left(-\frac{i_{SC} log(Sub)}{i_{SC}+i_0} - \frac{i_0 log(Sub)}{i_{SC}+i_0} + \frac{i_{sc} t}{Cu_t n} + \frac{i_0 t}{Cu_t n} \right)} + 1}{i_{sc} + i_0} \right] - Cv_t n\, log\,(Sub) + i_{SC} t + i_0 t \right] \tag{3.1.4}$$

where "Sub" is used to substitute a repetitive term of 3.1.4 to enhance readability.

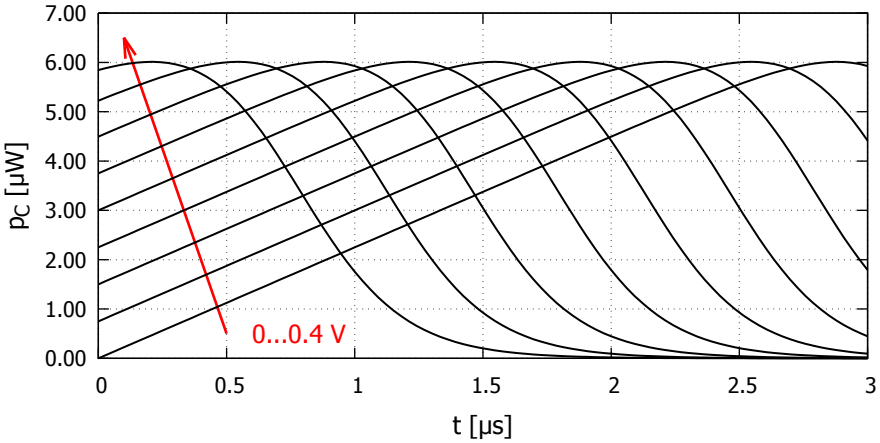
$$Sub = (-i_{SC} - i_0)\left(\frac{i_0}{i_{SC} + i_0} - e^{-\frac{X}{v_t n}}\right)$$



(a) Transient capacitor voltage v_C for start voltages $v_C(0)$=0...0.4 V. Solution of (3.1.4).



(b) Transient capacitor current i_C for start voltages $v_C(0)$=0...0.4 V. Solution of (3.1.3) and (3.1.4) neglecting the series restistor R_s.



(c) Transient power p_C for start voltages $v_C(0)$=0...0.4 V. Multiplication of (3.1.3) and (3.1.4).

Figure 3.3: Transient voltage v_C, current i_C, and power p_C of the capacitor from Fig. 3.2 Solutions of differential equation (3.1.4). For all charts: $C = 100\,pF$, $I_{SC} = 15\,\mu A$

In Fig. 3.3 solutions of (3.1.4) are depicted for different initial conditions from $v_C(0) = 0...0.4\,V$. The transient power form the solar cell into the charge pump capacitor is shown in Fig.3.3c. The power maximum is achieved after very different time periods, shifting to longer charging times with decreasing initial conditions which correspond to start voltages of the capacitor. In addition to initial conditions also the effect of parasitic capacitors must be taken into

account to obtain the optimum switching frequency of the charge pump. In the used process, capacitors with high relative capacitance do have a considerable portion of parasitics amounting up to 40 %. Consequently additional terms have to be introduced to the theory solution to cover initial conditions and parasitics: One term is the load impedance, which is assumed to be much smaller than the source impedance. This is the realistic case when charging a battery or a capacitor at the output. As a result the charge pump capacitor is discharged much faster when it is connected to the output than it is charged at the input. Therefore it can be assumed, that the start voltage $v_C(0)$ which is the initial condition of (3.1.4) is directly related to the output voltage, because the capacitor can only be discharged to the present output voltage.

Fig. 3.2 already indicates the second additional term to be assumed, which is the non-negligible parasitic capacitor. In contrast to the charge pump capacitor, which transports its stored energy to the output, the parasite gets shorted to ground in every switching period wasting its stored energy. As a result, the initial condition of the parasite is always zero. Before the charge phase starts the pump capacitor, holding $v_C(0^-) = V_{out}$, and the parasite, holding $v_C(0) = 0\,V$, get connected in parallel which lowers the effective start voltage of the pump capacitor seen by the source (3.1.8). Due to the parallel connection of the capacitors a first amount of energy is lost. The factor α is used to set the fraction of the parasitic capacitance to the flying charge pump capacitance, see 3.1.5.

$$\alpha = \frac{C_{par}}{C_{fly}} \tag{3.1.5}$$

Assumed initial conditions and terms for the single stage charge pump:

- The charge pump output is discharged to V_{out} before every CP clock cycle. This is the case if a low-impedance load is connected to the output.

$$v_{Cfly}(t = 0) = V_{out} \tag{3.1.6}$$

- The parasitic capacitor $\alpha \cdot C_{fly}$ is totally discharged at the beginning of every clock cycle.

$$v_{\alpha \cdot Cfly}(t = 0^-) = 0 \tag{3.1.7}$$

- Leading to the initial condition of v_C for (3.1.3).

$$v_C(t = 0^+) = \frac{V_{out}}{1 + \alpha} \tag{3.1.8}$$

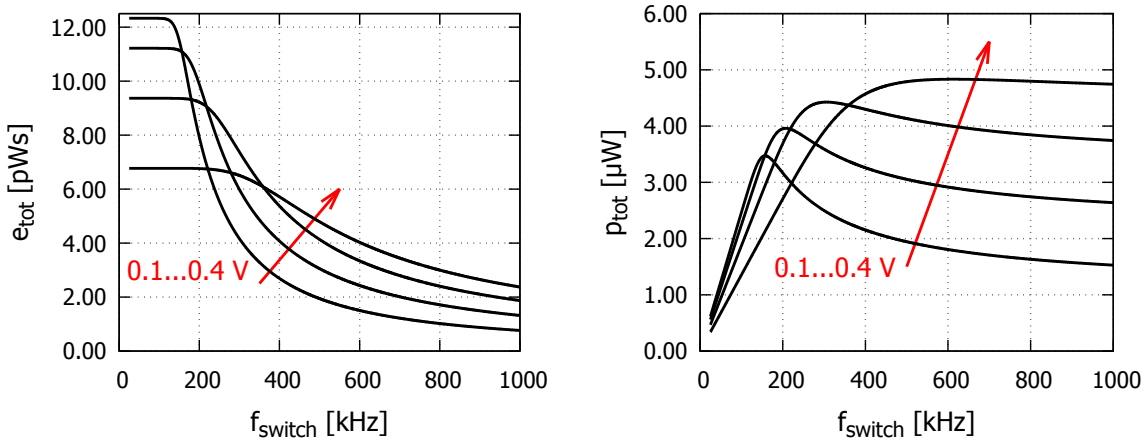
- The output capacitance is at least three orders of magnitude larger than the total installed charge pump capacitance. As a result the output voltage can be assumed to be constant after one clock cycle by introducing a negligible error.

In the next calculation step the total stored energy, which is transferred from the source into the sum of both capacitors, as a function of the switching period is calculated using (3.1.9). The initial conditions for $v_C(0)$ and $i_C(0)$ are corrected using (3.1.8). Due to 50 % duty cycle of f_{switch} the upper integral boundary T corresponds to half of the switching period and is also corrected for the frequency dependent plots.

$$e_{tot}(T) = \int_0^T v_C(t) i_C(t) dt \quad where \quad T = \frac{1}{2 f_{switch}} \tag{3.1.9}$$

The power flowing from the solar cell to the capacitors is calculated in (3.1.10) using (3.1.9).

$$p_{tot}(T) = \frac{1}{2T} \int_0^T v_C(t) i_C(t) dt \tag{3.1.10}$$



(a) Total energy transferred from the source to the charge pump per switching period as function of the converter frequency using (3.1.9).

(b) Total power flowing from the source to the charge pump as function of the converter frequency using (3.1.10).

Figure 3.4: Solutions of the energy and power flow equations from the source into the pump. The lowering of the initial capacitor voltage due to the parasite is accounted. For both charts: C = 100 pF I_{SC} = 15 µA α = 0.35 $v_C(0^+)$=0.1...0.4 V.

Fig. 3.4 shows the total stored energy and the power transferred from the source to the charge pump as a function of the switching frequency. As Fig. 3.4a depicts, at low frequencies the energy strictly follows the quadratic dependency on the capacitor voltage. This behavior is observed due to the long charging time of the capacitor at low frequencies, at which the capacitor is always charged to the maximum energy it can receive for the given voltage difference. The monotonic reduction of the energy per switching cycle for higher frequencies is caused by the decreasing voltage difference $v_C(T) - v_C(0)$ at which the capacitor gets charged. Therefore, the highest energy per cycle is transferred for a low initial voltage $v_C(0)$ which corresponds to a low output voltage of the converter. Fig. 3.4b shows the effective power flowing from the source to the charge pump capacitor as a function of switching frequency.

At lower initial voltage $v_C(0)$ this power has a clearly developed and narrow maximum power point which gets shifted towards higher frequencies if the converter output voltage increases. For the initial condition $v_C(0) = 0.4\,V$ which is close to open circuit voltage of the solar cell, the maximum power point vanishes. In this case the wrong assumption could be made, that for higher output voltages the converter frequency has to be set just above a certain minimum value to transfer the maximum power form the source to the output. This wrong assumption is made, because only the power flowing form the source to converter input is calculated and depicted in Fig. 3.4b, neglecting the energy that gets wasted in the parasitic capacitor. As a consequence the power that can theoretically be transported to the output of the charge pump has to be calculated accounting for the parasitic losses.

To determine the portion of the input power which is transferred to the output of the charge pump, the losses caused by the parasitic capacitor need to be known. By subtracting the lost parasitic energy from the total consumed energy the real throughput is calculated. In a first step, the remaining energy which stays in the flying capacitor after it is connected to the output is calculated. Energy remains in the flying capacitor, because it can only be discharged to the present output voltage ($v_C(0^+) = V_{out}$). The energy stored in a capacitor is generally calculated using (3.1.11).

$$E = \frac{C \cdot U^2}{2} \tag{3.1.11}$$

After the flying capacitor is connected to the input, the parasite, which holds no charge, is also connected in parallel to the flying capacitor lowering their common initial voltage to the expression given in (3.1.8). Due to this parallel connection a first amount of electrical energy $e_{\text{parallel-losses}}$, see 3.1.12, which is independent of the switching frequency is lost by the common voltage lowering. A second amount of energy is lost due to the parasitics, which depends on the switching frequency. Equation 3.1.13 summarizes all parasitic losses, where frequency dependent and independent parts are depicted separately.

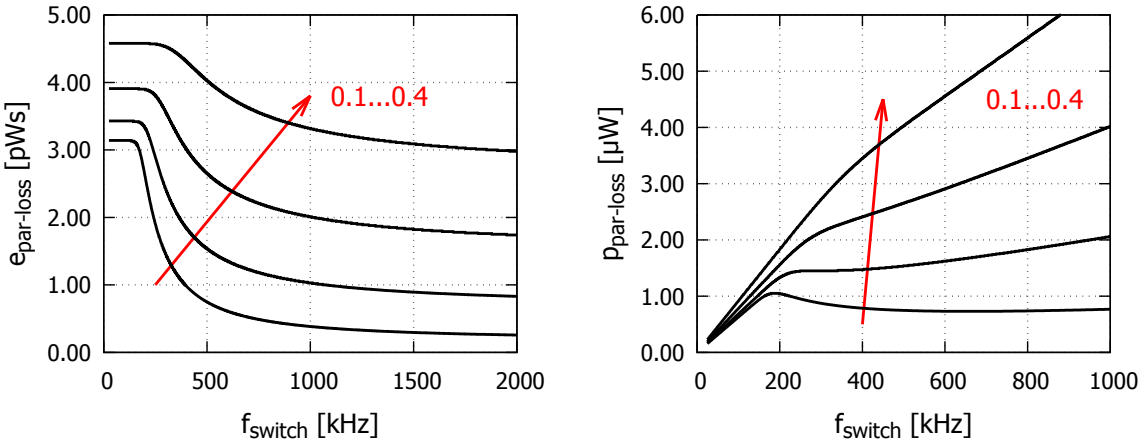
$$e_{parallel-losses} = \frac{C_{fly} \cdot V_{out}^2}{2} - \frac{(C_{fly} + C_{par}) \cdot (\frac{V_{out}}{1+\alpha})^2}{2} = \frac{C_{fly} \cdot V_{out}^2 \cdot (\frac{\alpha}{1+\alpha})}{2} \tag{3.1.12}$$

$$e_{parasitic-loss}(f) = \frac{\alpha \cdot C_{fly} \cdot (v_C(1/f_{switch})^2 - v_C(0^+)^2)}{2} + e_{par}(0^+) + e_{parallel-losses} \tag{3.1.13}$$

$$e_{par}(0^+) = \frac{\alpha \cdot C_{fly} \cdot \left(\frac{V_{out}}{1+\alpha}\right)^2}{2} \tag{3.1.14}$$

$$p_{parasitic-loss}(f) = f \cdot e_{parasitic-loss} \tag{3.1.15}$$

Figures 3.5a and Fig. 3.5b show solutions of (3.1.13) and (3.1.15), respectively. As Fig. 3.5b depicts, the power losses do have local maxima for low frequencies at low output voltages. However, the parasitic losses continuously increase with switching frequency. Therefore, the output power of the converter will also have a local maximum, because the input power shows a settling behavior for increasing frequencies, see Fig. 3.4b.



(a) Total energy stored in the parasitic capacitor as a function of switching frequency and different output voltages.

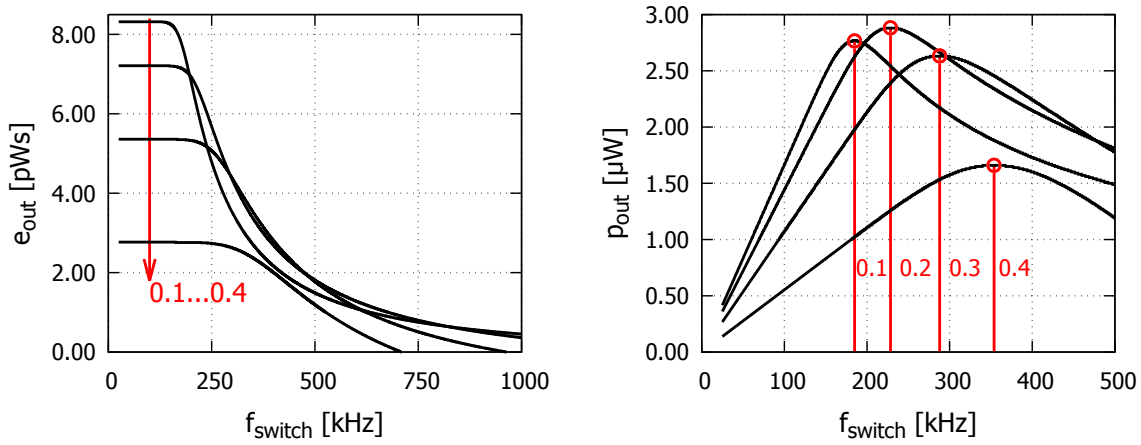
(b) Total power flowing from the source to the parasitic capacitor as function of the converter frequency using (3.1.10).

Figure 3.5: Solutions of the energy and power flow from the source to the parasitic capacitor. For both charts: $C = 100\,pF$, $I_{SC} = 15\,\mu A$, $\alpha = 0.35$, $v_C(0^-)$=0.1...0.4 V

In Fig. 3.6 the output energy as well as the output power as functions of the converter frequency are depicted. While the energy per period clearly reduces with increasing switching frequency, the output power has a local maximum at a specific switching frequency. The local power maxima are indicated with vertical red lines and circles, see Fig. 3.6b, for output voltages between 0.1 V and 0.4 V.

Due to the narrowing of the output power function for low output voltages the correct frequency at maximum power point (f_{MPP}) is an important value to prevent power losses caused by the charging process of the load capacitor. Using the same input parameters as used in Fig. 3.6b a constant frequency held at the maximum power point for 0.4 V would reduce the output power at 0.1 V by 32 %. Consequently, a maximum power point tracking algorithm needs to adjust the switching frequency of the charge pump during the charging process of an output load-capacitor. Besides the output voltage, the f_{MPP} also depends on the illumination of the solar cell which determines the short circuit current (I_{SC}) as well as on the open source voltage of the cell, Further, an adjustment of f_{MPP} is necessary for different values of α.

In Fig. 3.7, Fig. 3.8, and Fig. 3.9 those dependencies of the optimal switching frequencies are depicted. Additionally also the fraction of the open circuit voltage (FOC) is shown,



(a) Remaining energy getting transported to the output as function of switching frequency.

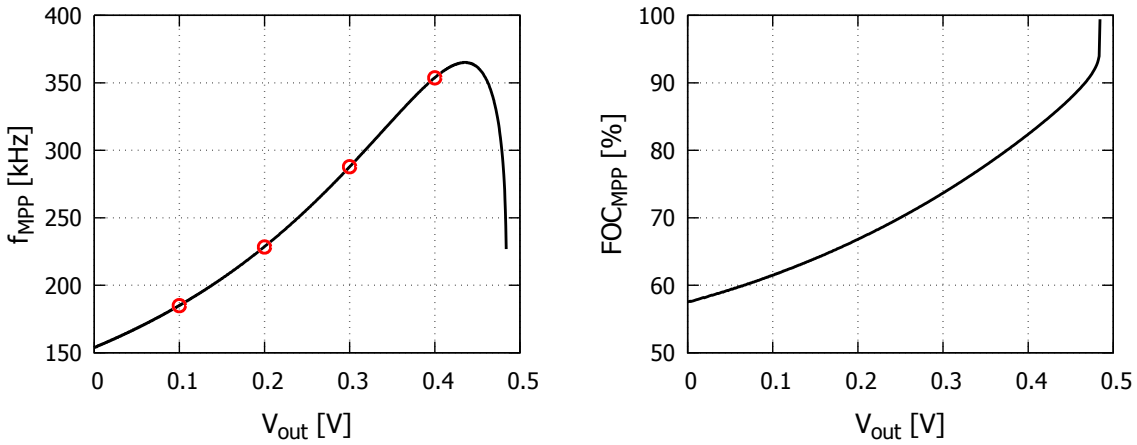
(b) Output power as function of the switching frequency. The vertical red lines indicate the optimum frequency for a given output voltage $v_C(0)$ to achieve maximum output power.

Figure 3.6: Test conditions for both charts: $C = 100\,\text{pF}$, $I_{SC} = 15\,\mu\text{A}$, $\alpha = 0.35$, $v_C(0)$=0.1...0.4 V

because state-of-the-art harvesting chips typically use this method to determine the optimum frequency by holding the FOC at a predefined constant value. However, keeping the FOC at a constant value is not applicable for the case of an integrated DC/DC converter, as analyzed in this theory section. The fraction of the open circuit voltage is calculated using the root mean square (RMS) value of v_C (3.1.16). Due to the time dependency of the input voltage, which follows a curve depicted in Fig. 3.3a, the RMS value of v_C is used for the fraction.

$$FOC_{MPP} = \frac{v_{C-MPP-RMS}}{v_{C-OCV}} = \frac{\sqrt{f_{MPP} \cdot \int_0^{1/f_{MPP}} v_C(t)^2 dt}}{v_C(t \to \infty)} \tag{3.1.16}$$

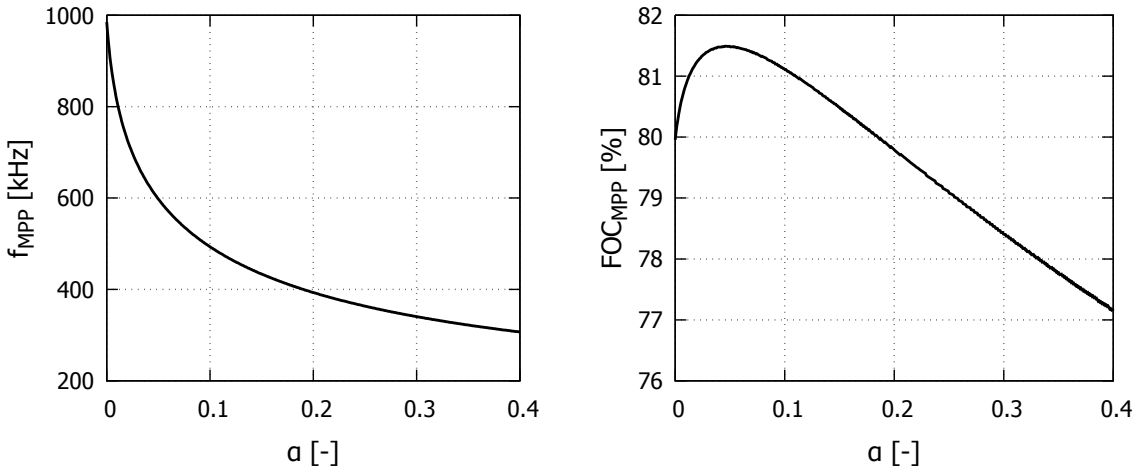
Comparing Fig. 3.7, Fig. 3.8, and Fig. 3.9, it can be seen, that the present output voltage influences the optimum FOC the most. Further, f_{MPP} is not a monotonic function of V_{out}, while it is for α and I_{SC}, which makes it more difficult to implement a simple analog tracking algorithm. The results of this section have been double checked using a MATLAB Simulink model which contained a parallel as well as a series resistor at the solar cell. However, as the currents are relatively small and the contact resistances on chip are low, the losses are negligible, which is verified by the numeric solution of the Simulink



(a) f_{MPP} as function of the output voltage. The red circles correspond to the values depicted in Fig.3.6b.

(b) FOC to reach maximum output power calculated with the RMS value of v_C.

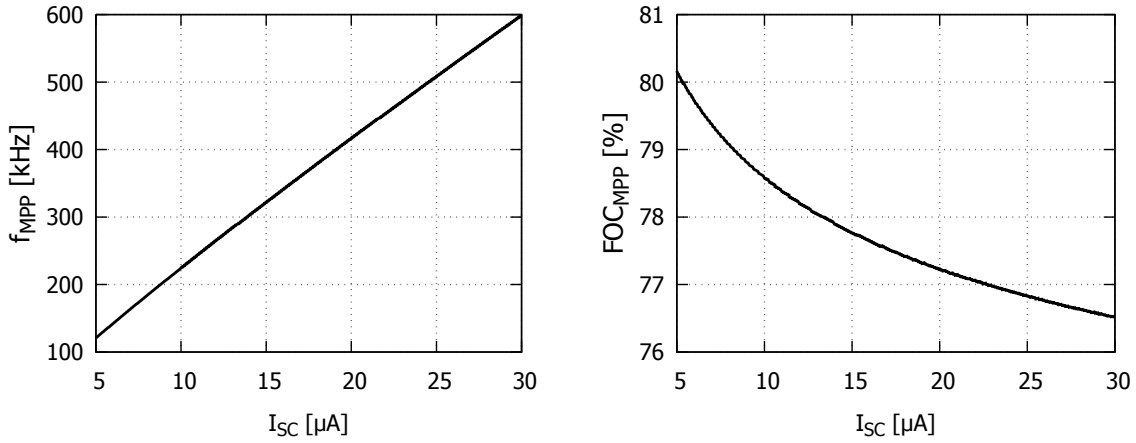
Figure 3.7: Optimum frequency and FOC as functions of the output voltage. During charging of a load capacitor the charge pump clock would need to follow this frequency. For both charts: $C = 100\,pF$, $I_{SC} = 15\,\mu A$, $\alpha = 0.35$



(a) f_{MPP} as function of the parasitic capacitance fraction α.

(b) FOC to reach maximum output power calculated using the RMS value of v_C as function of the parasitic capacitance fraction α.

Figure 3.8: Optimum frequency and FOC as functions of α. For both charts: C=100 pF $I_{SC} = 15\,\mu A$, $v_C(0) = 0.35\,V$.



(a) f_{MPP} as function of the short circuit current, which depends on the illumination of the solar cell.

(b) FOC to reach maximum output power calculated using the RMS value of v_C as function of the short circuit current I_{SC}.

Figure 3.9: Optimum frequency and FOC as functions of the short circuit current I_{SC}. For both charts: $C = 100\,\text{pF},\ \alpha = 0.35,\ v_C(0) = 0.35\,\text{V}$

model.

3.1.1 Conclusion

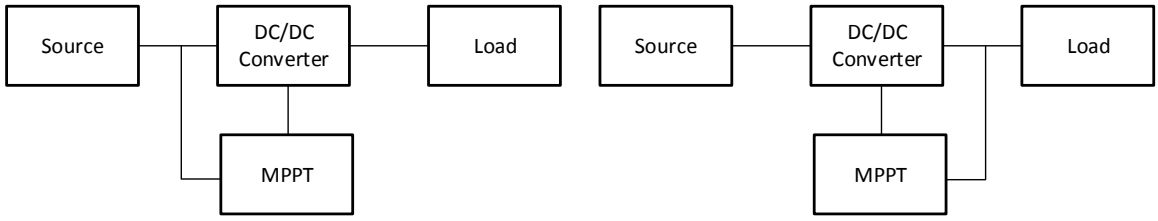
The solutions of the theoretical solar cell model in combination with a simplified charge pump and parasitics showed the impact of the output voltage, the illumination, and α on the optimal switching frequency. Especially the output voltage, which is changing during the charge process of a battery or an output capacitor forces the f_{MPP} to change by a factor of approximately 2 under the very same illumination conditions. Illumination conditions require f_{MPP} to be adapted within a factor of approximately 10. Hence, the optimal frequency for outdoor conditions would produce a negative output power even under bright indoor conditions due to parasitic losses.

Another finding of the analytic observation is the fact, that the input power is no direct indicator for the output power of the converter in the given monolithic setup. However, state-of-the-art approaches typically observe the input power by comparing the loaded source voltage to the open circuit voltage (FOC). This approach is not applicable for the solar cell charge pump combination, because it is shown, that the FOC cannot be held a constant value. Meaning that the FOC method would need to follow a predefined mapping, which depends on the illumination and the output voltage. Therefore, the implementation of the maximum power point tracking algorithm (MPPTA) of this work uses a different approach which can operate continuously and ultra-low power based on the perturbation and observation (P&O) technique.

3.2 MPPT Algorithm Concept

The state-of-the-art approach for low-power harvesting chips in which the input voltage is held at a constant fraction of the open circuit voltage leads to a wrong power point for the monolithic harvester as described in section 3.1. In contrast to the monolithic implementation, an off-chip-inductor based boost converter can make use of the FOC, because it sets its output to input voltage gain in continuous conduction mode by the duty-cycle. Due to this flexibility, the overall efficiency is higher over a wider voltage gain range compared to an on-chip charge pump. As a result, the step-up converter delivers the highest output power, if the source delivers the highest input power to the converter input. Hence, approaches using this converter type can make use of the input power matching condition at which the source only needs to be characterized. Using the FOC method, which is a source only characterization method, for a monolithic harvester would additionally require a setup in which the input voltage is filtered or averaged. This filtering, done digital or analog, would also require additional power or chip area, respectively. Based on the findings from theory section 3.1 and on the disadvantages of an on-chip charge pump, basically two different approaches are derived for the monolithic harvester.

One approach would be a pre-defined or pre-calibrated lookup table for the maximum power point tracking (MPPT) controller. The lookup value, which sets the converter frequency, would need to be dependent on the solar cell short circuit current and on the output voltage. In this case the required values would need to be measured with absolute accuracy while the input voltage fraction is not of interest. Besides the measurement also a controller would be required which increases the power consumption.



(a) Conventional MPPT approach for low power harvesting systems.

(b) Proposed MPPT approach which inherently optimizes the combination of source and converter.

Figure 3.10: General concept comparison of the conventional approach and the proposed MPPTA design.

A completely different MPPT approach is to use a P&O algorithm applied on the output of the DC/DC converter. In Fig. 3.10 this difference is depicted. Instead of using a MPPT loop which is closed around the input of the converter, the loop is closed around the output. Closing the controller loop from the output of the converter back to the converter-control achieves an inherent consideration of parasitic losses. The inherent consideration can be achieved, because besides the source only, also the combination of source and converter have a monotonic output-power function of frequency until the maximum power point (MPP) is reached. Hence, even if a higher converter frequency would lead to an increase in input power

it could be just higher parasitic losses. In this case the proposed approach would not produce a wrong decision. However, to maximize the output power, the implementation can further be simplified when observing the output current only. This simplification reduces the power consumption of the algorithm, because the voltage does not need to be measured. If the current, flowing from the converter into the load has a maximum, also the power at the load has reached the MPP. The P&O algorithm enabling an ultra-low power tracking algorithm is described in the flowchart Fig.3.11, where I represents the output current, f is the converter switching frequency and f/X represents a constant fraction of the actual converter frequency which is the perturbation of the system.

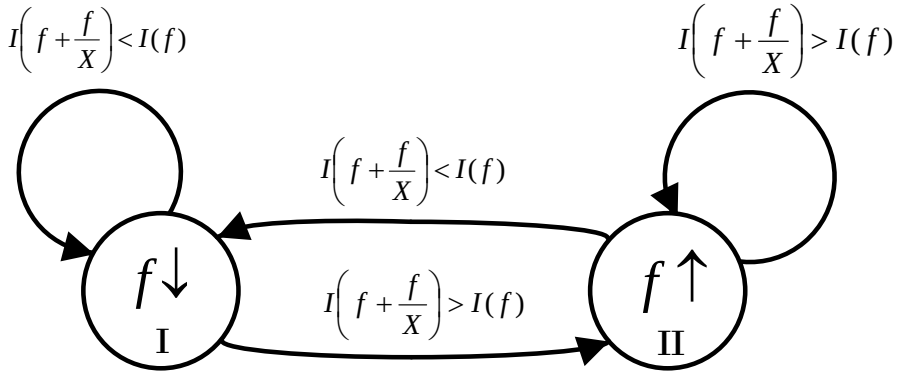


Figure 3.11: Flowchart of the output current maximization P&O algorithm. When subtracting the frequency fraction f/X from f the greater-than and less-than signs have to be changed.

The algorithm knows two different states which are I: converter frequency too high and II: converter frequency too low. By adding or subtracting a fraction of the actual converter frequency the perturbation of the system is achieved. In a next step the observation of the output current is done and compared to a previous value stored before perturbation. Based on the comparison result, the algorithm keeps staying in its state or switches to the other state. A conceptual drawing of the implemented MPPTA is depicted in Fig. 3.12.

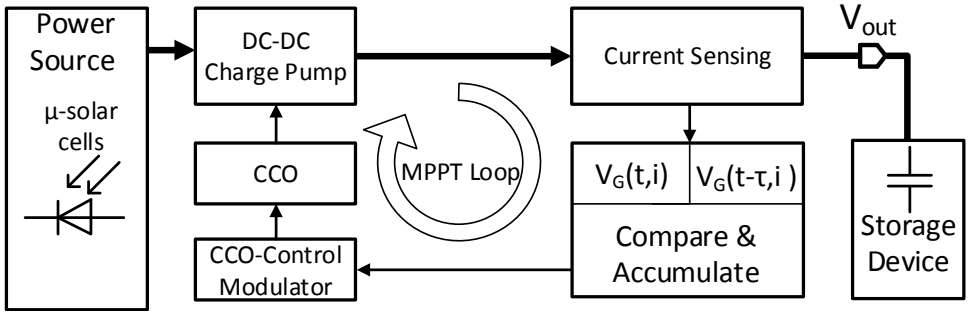


Figure 3.12: Block level implementation of the proposed ultra-low power P&O MPPTA.

The high-side current sensing block continuously senses the output current of the charge pump and delivers a voltage $V_G(t, i)$, which is related to the output current. In the next block the voltage $V_G(t, i)$ is buffered and tracked in a first track and hold (T&H) circuit. Using a perturbation clock frequency of approximately $1/\tau = 1\,\text{kHz}$ (system clock), the present representation of the output current $V_G(t, i)$ and the value from the previous clock period $V_G(t - \tau, i)$ are compared. The difference of $V_G(t, i)$ and $V_G(t - \tau, i)$ is integrated by an input-multiplexed accumulation circuit, changing its input every system clock period (τ). Accordingly, in every first clock period $V_G(t - \tau, i)$ - $V_G(t, i)$ and in every second clock period $V_G(t, i)$ - $V_G(t - \tau, i)$ is integrated. The output of the integrator is used to define the bias of the current controlled oscillator (CCO). This is done by a voltage to current conversion generating a bias current which is then related to the accumulated voltage. The CCO bias current is additionally mirrored with a 10:1 ratio into a second path. Finally, the mirrored 10 % value of the CCO bias is added to the present bias in every first system clock cycle, represented by the modulator block in Fig. 3.12. Meaning, at the beginning of every first system clock cycle the charge pump clock frequency is also approximately 10% higher than it was at the end of the previous system clock cycle. As a result, the MPPT loop reacts during every system clock cycle to the perturbation caused by the modulator. Hence, the integrator output voltage and therefore the charge pump clock increases, as a faster charge pump clock leads to a higher output current and vice versa.

Due to the multiplexed accumulator input and the modulation, the implementation can distinguish between four different cases:

- The current into the load or storage device decreases when increasing the frequency from f to f+f/x. In that case the accumulating device reduces its output and the converter frequency will be decreased.
- The current into the load or storage device increases when increasing the frequency from f to f+f/X. In that case the accumulating device increases its output and therefore the converter frequency.
- The current into the load or storage device increases when decreasing the frequency from f+f/X to f. In that case the accumulating device decreases its output and the converter frequency.
- The current into the load or storage device decreases when decreasing the frequency from f+f/X to f. In that case the accumulating device increases its output and therefore the converter frequency.

The advantages of the proposed P&O approach are its simplicity and robustness against temperature or stress related drift and measurement inaccuracies. All measured values are compared only to each other and are valid for the short time τ. Hence, no absolute value of the output current needs to be known which makes a stable reference source obsolete and relaxes the requirement of the high side current sensor. Nonlinearity of $V_G(i)$ can also be neglected, because the comparator translates the measured analog value to a digital decision which is then fed to the accumulation block. The relaxed accuracy requirements for all involved building blocks in this concept enable the ultra-low power implementation of the P&O MPPTA.

3.3 MPPT Algorithm Implementation

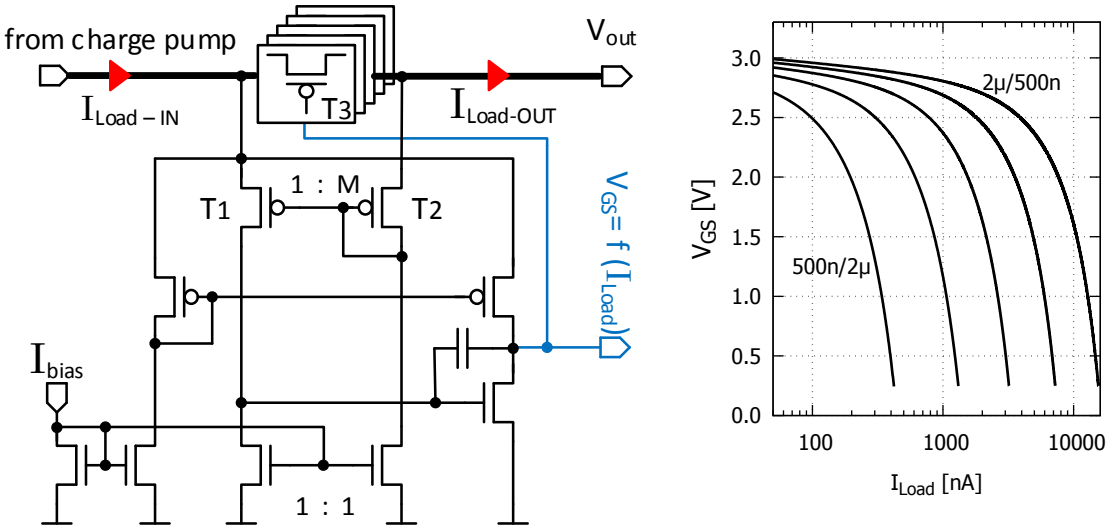
The implementation of the MPPTA is shown on transistor level for the key building blocks. During this work, two different accumulation approaches have been implemented and tested. Both approaches, one analog-only and one mixed signal, are shown, because both have been taped out and worked. However, the mixed signal approach which uses a digital counter and an current output digital to analog converter (IDAC) was identified as a more reliable and smaller solution. The first analog-only approach, which is described in detail on the following pages, showed a reproducible error occurring at high intensity illumination. When the illumination intensity inside the test chamber was increased, the algorithm seemed to reset itself at any test-chip. This behavior was also observed under natural strong sunlight conditions. As highly reasonable error source, the mechanisms that holds the information to set the clock frequency was identified. For that reason a redesign was made which holds the information in a digital counter fed to an IDAC. The mixed signal approach did not have this error and could also achieve the ultra-low power requirements. The investigations performed led to the general understanding, that the ultra-low power circuits of the MPPTA must hold any information in the analog domain as short as possible to gain reliability in this harsh environment. This is caused by the fact, that a simulation of all unwanted photocurrents is impossible and capacitor drooping as well as leakage currents become unpredictable when exposing the silicon die to sunlight.

3.3.1 High-Side Current Sensor

The first building block of the MPPTA is the high-side current sensor, depicted in Fig. 3.13, which directly connects at the charge pump output. It utilizes a scalable P-channel metal–oxide–semiconductor field-effect transistor (PMOS) sense transistor in the current path which is used to sense the current. Basically the sensor is a two stage amplifier with common gate input and built-in offset. A gate voltage is provided by the amplifier which keeps the drain-source voltage across the sense transistor T_3 constant. This constant burden voltage across T_3 is set by the mismatch of the PMOS input pair denoted by M. Considering the same current trough the input pair forced by the 1:1 N-channel metal–oxide–semiconductor field-effect transistor (NMOS) current mirror a delta V_{GS} is calculated setting both currents equal:

$$V_{SD-T_3} = \Delta V_{GS} = V_{GS-T1} - V_{GS-T2} = \frac{kT}{q} \cdot ln(M) \tag{3.3.1}$$

Due to the small bias currents, the input pair is in weak inversion causing the logarithmic relation in 3.3.1. The mismatch is layout-matched implemented with M=2 using for T_1 $3 \cdot 500\,\text{nm}/4\,\mu\text{m}$ and for T_2 $6 \cdot 500\,\text{nm}/4\,\mu\text{m}$. This amounts to a burden voltage of approximately 19 mV at room temperature causing a negligible efficiency loss in the current path. Figure 3.13a and Fig. 3.13b show the circuit implementation and the relation of the sense-gate-voltage to the load current, respectively. The bulk potential of T_3 is set by two additional PMOS devices which switch the n-well either to the charge pump side or to the



(a) High-side relative current sense amplifier and scalable sense transistor T_3. The burden voltage is independent of the current and given by design.

(b) Gate voltage V_{GS} as function of the load current. Different gate voltage traces refer to the five smallest implementaitons of T_3.

Figure 3.13: Relative current sensor using a trans-conductance concept. The bias current is 1 nA and the amplifier is supplied by the same rail in which the current is measured.

output depending which side the higher potential holds. Further it can be seen that the load current to be sensed can change over decades if T_3 is properly re-sized.

The sizing of T_3 is implemented to operate automatically, which is important to keep the sensitivity of the circuit high enough while covering the current range of interest. Meaning, that a change in gate voltage was specified to be at least 5 mV per 1 % change in load current. This specification was chosen to ensure a proper detection whether the load current has increased or decreased caused by the frequency modulation.

Due to the small V_{DS} T_3 is in the linear region. The gate-source voltage can be expressed by 3.3.2

$$V_{GS} = \frac{I_D}{\frac{W}{L} K V_{DS}} + \frac{V_{DS}}{2} + V_{Th} \quad \text{with} \quad K = \mu C_{Ox} \tag{3.3.2}$$

where C_{Ox} is the oxide capacitance, µ is the charge carrier mobility and W/L is the width to length aspect ratio of the transistor. This aspect ratio for the largest transistor is calculated by 3.3.3 to carry 500 µA.The maximum current of 500 µA was chosen to give the test chip implementation a more generic usability for other applications. This current range is not achieved by the monolithic implementation in which typically currents between 50 nA and 50µA have to be optimized.

$$\frac{W}{L} = \frac{2 \cdot I_D}{KV_{DS}\left(2V_{GS} - 2V_{Th} - V_{DS}\right)} \tag{3.3.3}$$

In a next calculation step, the ratio between two sense transistor aspect ratios is determined. Therefore the factor c is introduced further it is assumed that the length of the sense transistor is kept constant:

$$W_{n+1} = c \cdot W_n \tag{3.3.4}$$

Where W_n is the width of the n^{th} selected transistor and W_{n+1} is the next larger ratio. To express c in a first step the gate voltage difference is calculated using 3.3.2. Equal threshold voltages and a design related constant drain-source voltage are assumed which leads to 3.3.5.

$$\Delta V_{GS} = V_{GSn} - V_{GSn+1} = \frac{I_D L}{W_n K V_{DS}} - \frac{I_D L}{c \cdot W_n K V_{DS}} \tag{3.3.5}$$

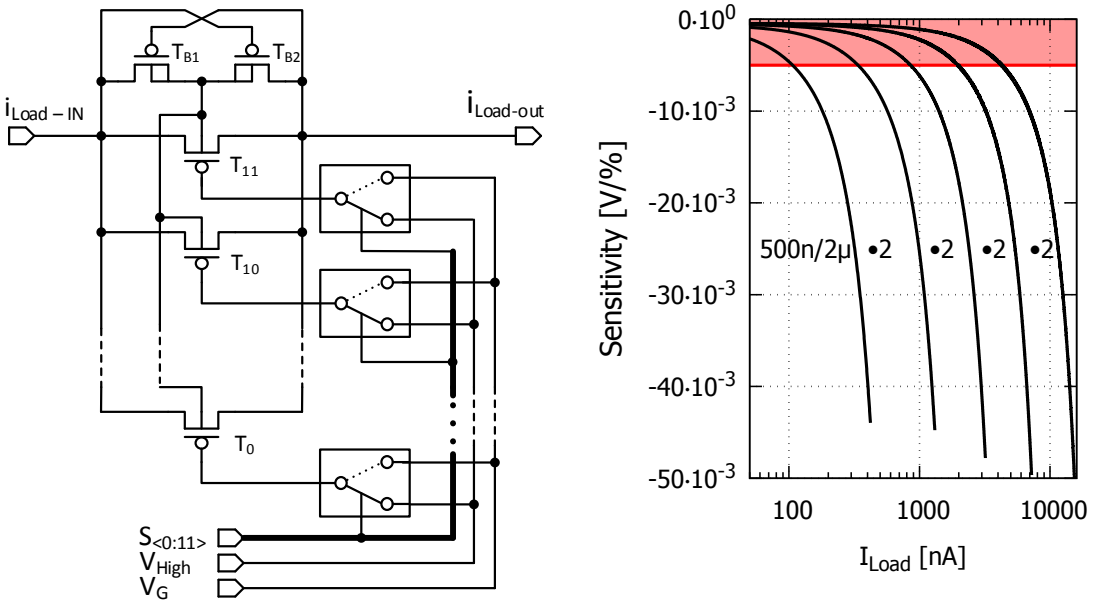
$$c = \frac{-I_D L}{K \Delta V_{GS} V_{DS} W_n - I_D L} \quad \text{where} \quad K \Delta V_{GS} V_{DS} W_n \leq I_D L \tag{3.3.6}$$

The next parameter to specify is ΔV_{GS}. The larger ΔV_{GS} is chosen, the larger c can be, which would decrease the necessary number of implemented stages. The Δvoltage is specified to be 0.6 V, because the MPPTA should start to work at supply voltages around 1.4 V. This specification allows to have an upper and lower safety margin of 0.4 V to detect whether the number of stages need to be reduced or increased. A detailed description of the stage selection is given later in this chapter. However, ΔV_{GS} of 0.6 V leads to an aspect ratio change factor of $c \approx 2$, using 3.3.6. Therefore, the number of sense transistors, denoted by S, is calculated by the binary logarithm using 3.3.7 and the current range to be covered by the implementation.

$$S = \frac{log_{10}\left(\frac{I_{max}}{I_{min}}\right)}{log_{10}\left(c\right)} \approx 12 \tag{3.3.7}$$

Basically the segmentation of the sense transistor is done to achieve a specified sensitivity as mentioned above. Generally spoken the smallest possible and largest necessary sense transistor has to be selected. Figure 3.13b shows how the gate voltage is adjusted to achieve the constant burden voltage. The sensitivity of the relative current sensor is calculated using the derivative of the V_{GS} and the load current i_{Load}. This value is further normalized to the load current and given in V/%, see 3.3.8.

$$\frac{dV}{di_{Load}} \cdot \frac{i_{Load}}{100} \qquad [V/\%] \tag{3.3.8}$$



(a) High-side PMOS sense transistor. To ensure proper sensitivity over the specified decades, binary sized transistors can be connected in parallel via signal S<0:11>. T_{B1} and T_{B2} steer the n-well potential.

(b) Sensitivity as function of load current. The sensitivity is given in volts per percent load current change, see 3.3.8. The forbidden low sensitivity area is marked red.

Figure 3.14: The sense transistor selection is done by S<0:11>. The specified minimum sensitivity of 5 mV per 1 % current change has to be reached after changing signal S. Unused gates are set to a high voltage to avoid influences.

In Fig. 3.14b the results of 3.3.8 for different sense transistor sizes are depicted. A sensitivity of 50 mV per 10% is specified because the 10% frequency modulation of the charge pump clock should be evaluated by the sensor. Consequently the area marked in red shows forbidden operating points which will be avoided by the selection logic. If the sensitivity drops towards the red area, the next smaller transistor is selected. On the other side, if the gate voltage of the sense transistor reaches a pre-defined level close to ground, the next larger transistor is switched in parallel.

Figure 3.15 shows the selection logic implementation on block-level for the sense transistor. A buffered version of the V_{GS} is compared to two reference values to meet the burden voltage and sensitivity requirements. Although the whole MPPTA is robustly designed a reliable operation is only possible if V_{GS} does not cross the reference value after the sense transistor size change. This would lead to an unwanted repetitive set and reset of the required sense transistor. The described instability is avoided by keeping ΔV_{GS} within the before described range which is specified by the segmentation of the sense transistor and the minimum startup voltage.

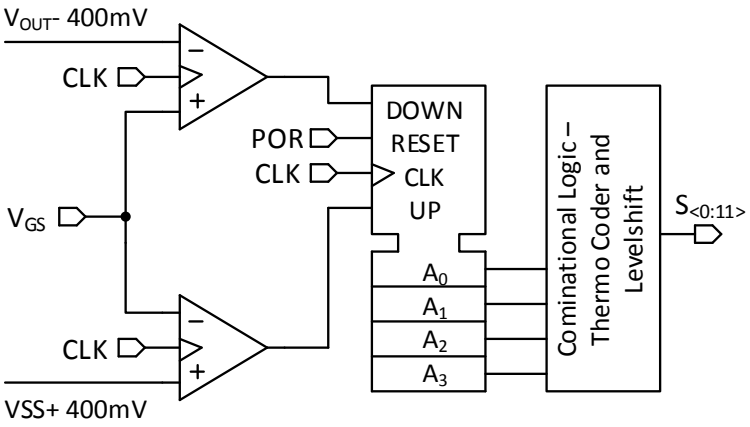


Figure 3.15: Sense transistor selection logic. The gate voltage is compared by two dynamic comparators and a synchronous bidirectional counter selects the number of necessary sense transistors.

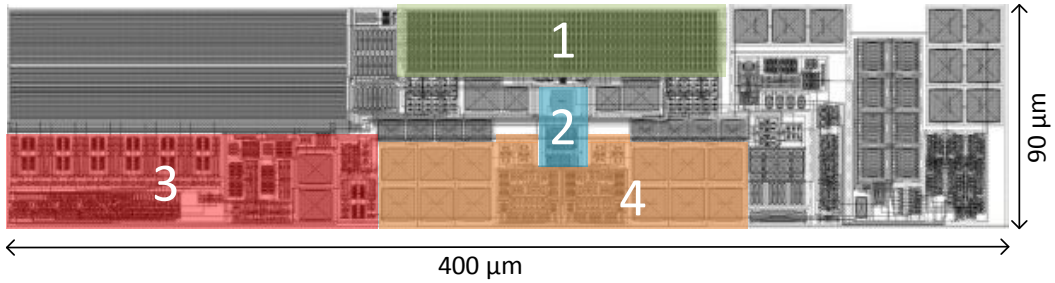


Figure 3.16: Layout of the MPPTA. 1: Sense transistor array 2: Sense amplifier 3: Sense transistor selection logic including counter, comparators, clock-preparation, thermometer coder, and level shifter 4: track and hold amplifier capacitors and switches.

3.3.2 Track and Hold Current Evaluation

The track and hold (T&H) circuit is used to evaluate the change of the gate potential from the current sensor. The T-gates are switched according to Fig. 3.17. This implementation allows keeping track of the current change using two sampled values or by comparing the old sample to the actual gate voltage. The switching frequency of the T-gates is the same that is used for the charge pump modulation which was previously defined as system clock frequency. As a result, one capacitor will always track the sense transistors gate voltage while the charge pump is operated at a higher frequency compared to the last frequency. The other capacitor will always track and hold the gate voltage while a lower charge pump clock is applied. A two cap solution can therefore be used to evaluate in every clock period of the MPPT-clock if the current has in- or decreased.

Both capacitors are referenced to V_{OUT} instead of GND. This is done because the gate

voltage V_{GS}, which is tracked, is also referenced to the output rail of the system. In the case of a constant V_{OUT} also a ground reference would be a practical solution. However, in this case the output voltage which is the source potential of the current sense transistor is at V_{OUT}. Subsequently the current representation of the sensor is also referenced to the output voltage. Considering a capacitor at the output which gets charged or discharged over time would lead to a false current reading if the tracking capacitors would have been referenced to GND.

Due to the low power demands of the whole harvester also the T&H circuit is biased with 1 nA. Therefore the dimensions of the T-gate switches are chosen to be very low-leakage also a high temperature. As a result the T-gate switches are slow long channel devices. During normal operation this slow response is not a problem, because the modulation caused gate voltage change which needs to be tracked is at maximum sensitivity, approximately 500 mV. The T&H capacitors are chosen to be small enough to track the 500 mV change which can occur at maximum sensitivity during a half clock period. However, a wrong current reading would occur after the sense transistor has changed in size due to the resetting of the gate potential. After the counter, depicted in Fig. 3.15, switches to a next larger or smaller sense transistor the new gate voltage is higher or smaller conducting the very same current, respectively. In this case the track and hold capacitors need to be charged to the new gate voltage level, before a proper evaluation can be made. To avoid this false reading during the reset phase, the MPPTA is paused for 5 clock cycles. This hold-off time gets triggered on every rising and falling edge of signal A_0 from the sense transistor logic counter. The signal is marked in Fig. 3.18.

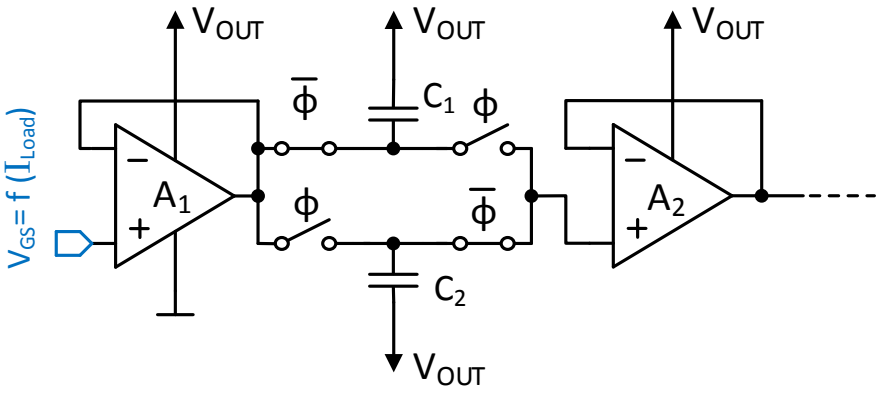


Figure 3.17: Track and hold circuit for the gate voltage of the relative current sensor. Two non-overlapping clocks are used for time interleaved current sampling. A_1 buffers the sensor signal and A_2 is used to reduce drooping. The capacitors are referenced to V_{OUT} as is V_{GS}.

Voltage of Fig. 3.18 correspond to the schematic of Fig. 3.17. The clock signal is taken from the chip pad with enabled pad level shifter and output driver to generate the 1.2 V amplitude for measurement purposes. It can be seen that the tracking capacitors alternately track and hold the gate voltage. The gate voltage from the sensor, drawn in blue, is responding to the

modulated charge pump clock due to the perturbation of the algorithm.

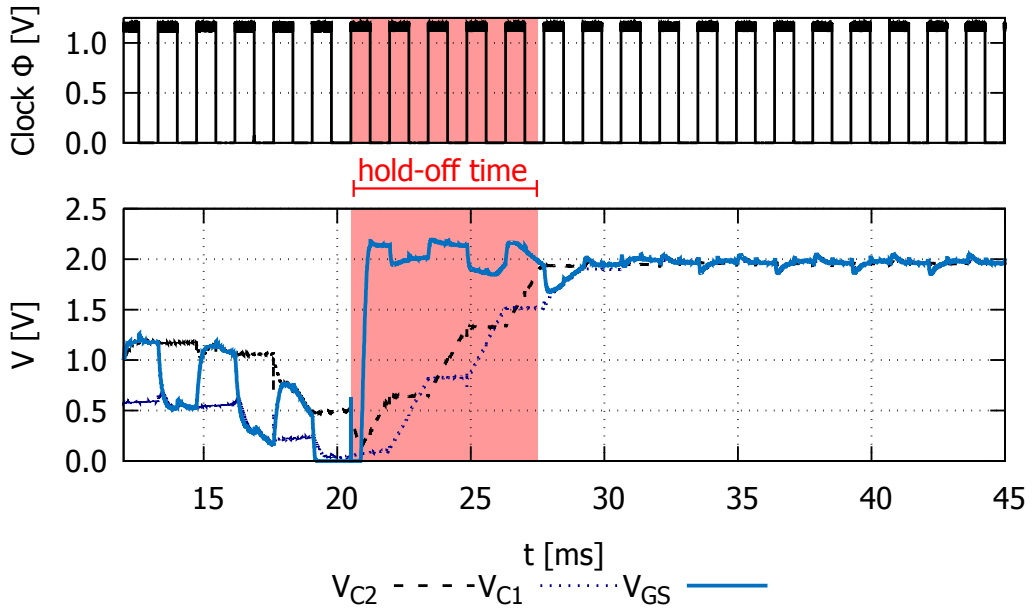


Figure 3.18: Transient voltages obtained from Fig. 3.17. Switches Φ as well as the modulator are controlled by the slow system clock above. Sensor gate voltage as well as both T&H voltages are depicted below. In this configuration example, the maximum power point is found after 30 ms.

3.3.3 Integrator versus IDAC Accumulation

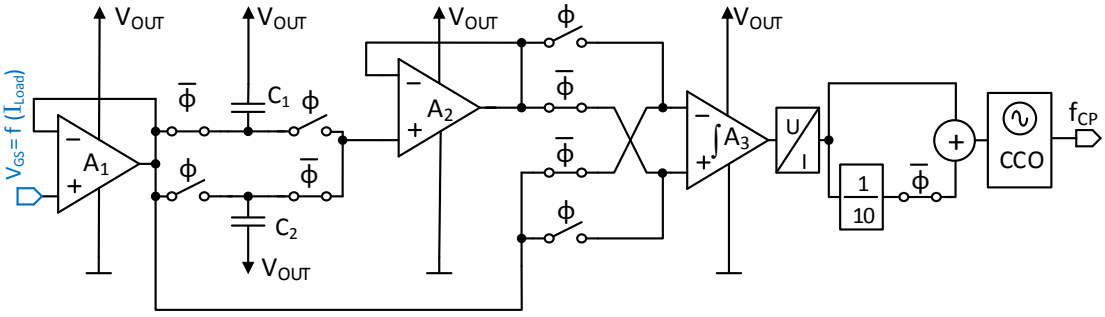


Figure 3.19: Block-level schematic of the fully analog MPPTA. Held versions of V_{GS} are compared to the actual V_{GS} and the difference is integrated in A_3.

The fully analog implemented approach of the MPPTA is depicted in Fig. 3.19. T&H amplifier A_2 buffers the held V_{GS} to avoid additional drooping by the subsequent integrator input multiplexer. The input multiplexer is used to steer the output of A_3 into the correct direction. It is synchronously switched with the T&H as is the modulator of the charge

pump clock. As a result the integrator will always integrate into the positive direction as long as a higher frequency leads to a higher output current as well as a lower frequency leads to a lower output current. In both cases the charge pump frequency is still too low. In the opposite case, in which the frequency is already too high, the integrator will always sense a negative input difference and the charge pump frequency will be corrected to lower values.

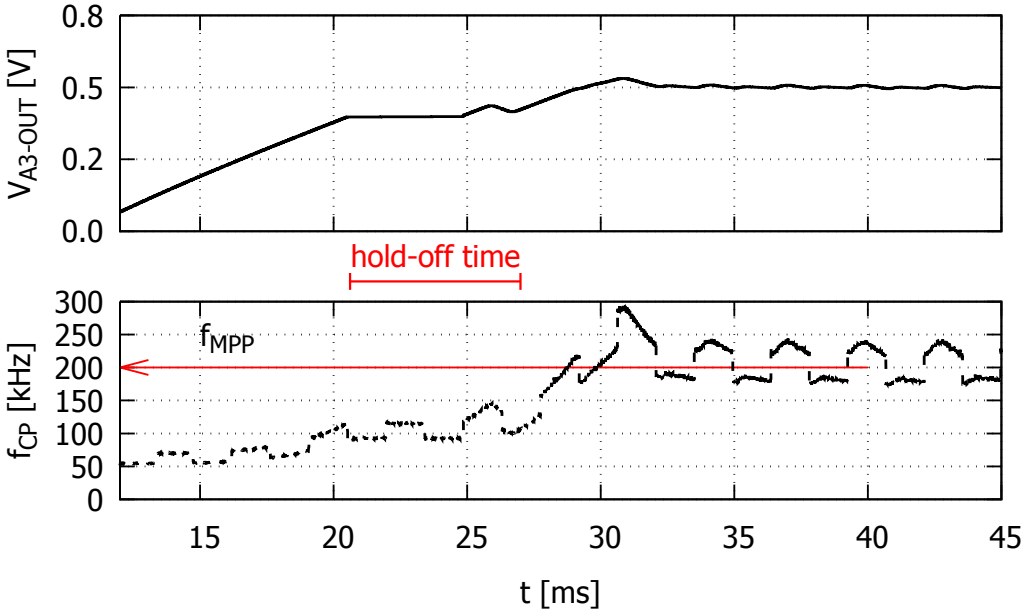


Figure 3.20: On top: transient output voltage of Integrator A_3 representing the average charge pump clock frequency. On bottom: charge pump clock frequency f_{MPP} is found after 30 ms at 200 kHz. In correspondence with signals from Fig. 3.18.

The analog implementation, in which the integrator determines the average charge pump (CP) clock operates in the laboratory test environment like in the simulation. Also under moderate natural sunlight the MPP is found and tracked correctly. However, under bright sunlight conditions a windup of the integrator and instability of the MPPTA has been observed. This behavior is most likely caused by imperfect light shielding, which generates photo current in the large junction area of the integrator capacitor. It is worth mentioning that the test chips are glued on a metal lead frame, which will reflect light into the circuit area, regardless of the metal shielding on top. In combination with the ultra-low power design which uses mostly 1 nA bias current the parasitic photo currents which are generated in every junction make a proper package mandatory. To overcome the reliability problem the large integrator capacitor and the U/I converter have been replaced by a partly digital approach, see Fig. 3.21.

This approach utilizes a dynamic zero bias comparator to compare the output of the multiplexer. It decides if f_{CP} is too low or too high by sensing the same input difference voltages as the integrator in the former implementation. The comparator output is connected to a

synchronous bidirectional 6 bit counter, see Fig. 3.21. An IDAC receives the counter value and generates the bias current for the CCO. The hold-off logic, which is still mandatory, prevents the counter from changing its value after the sense transistor has been automatically resized. A change in sense transistor size is indicated by signals $A_{0\text{-}3}$.

Figure 3.22 and Fig. 3.23 show relevant signals of the MPPTA during searching for the optimal charge pump clock frequency. In both cases the output voltage is kept constant at 3.2 V and the red light source from the solar cell characterization measurement setup is used to supply the harvester. The difference in both figures is the incoming light power which is 1 W and 2.6 W electrical input power to the red LED source, respectively.

It can be seen that the output current into the 3.2 V load responds to the frequency modulation while the charge pump clock is still too low. When the system comes closer to the MPP the response is reduced and a higher frequency would start to reduce the output current. However, in the example depicted in Fig. 3.22 the modulation does not affect the output current enough to toggle the counter value at MPP. In this particular case the optimum frequency is found at a counter value of hex 0D, which corresponds in the depicted scenario to an output current of 1.1 µA. The sense transistor size changes at 11 ms after which the IDAC holds its value constant until the T&H has readjusted.

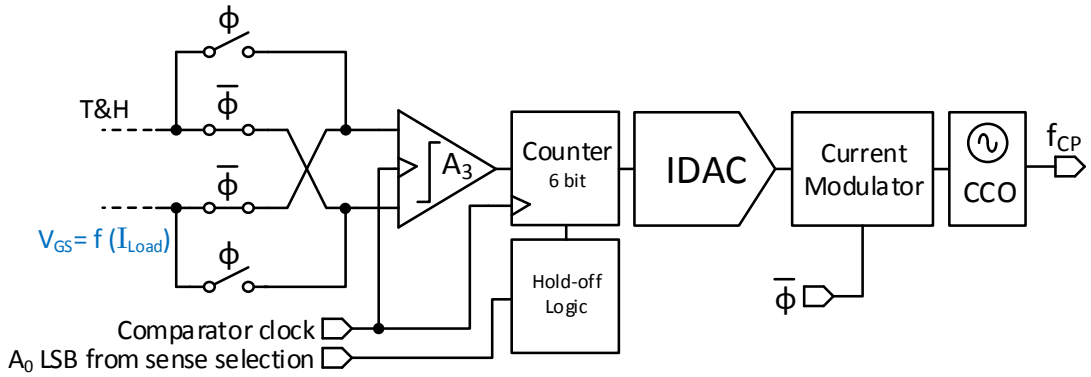


Figure 3.21: Digital approach

Figure 3.23 shows the same signals as Fig. 3.22 does, increasing the electrical light power from 1 W to 2.6 W. Due to the higher light intensity the MPP is shifted to higher clock values. In this case the MPPTA finds the optimum after 80 ms while the algorithm keeps toggling between hex 17 and 18. Also the sense transistor resizing was necessary two times, which also inserts the hold-off time twice. Figure 3.22 and Fig. 3.23 depict the output currents of the charge pump at both light intensities. In both cases the currents settle at an almost constant specific value and do not increase or decrease with clock changes, because the output power as function of charge pump frequency curve flattens around the MPP. This behavior implies that the charge pump clock in a non-ultra-low-power system can and should be chosen to be higher than minimally needed, because it does not negatively affect the performance. The monolithic self-supplied approach however will suffer from increasing parasitic losses and unnecessary higher self-supply current although the output current does not increase

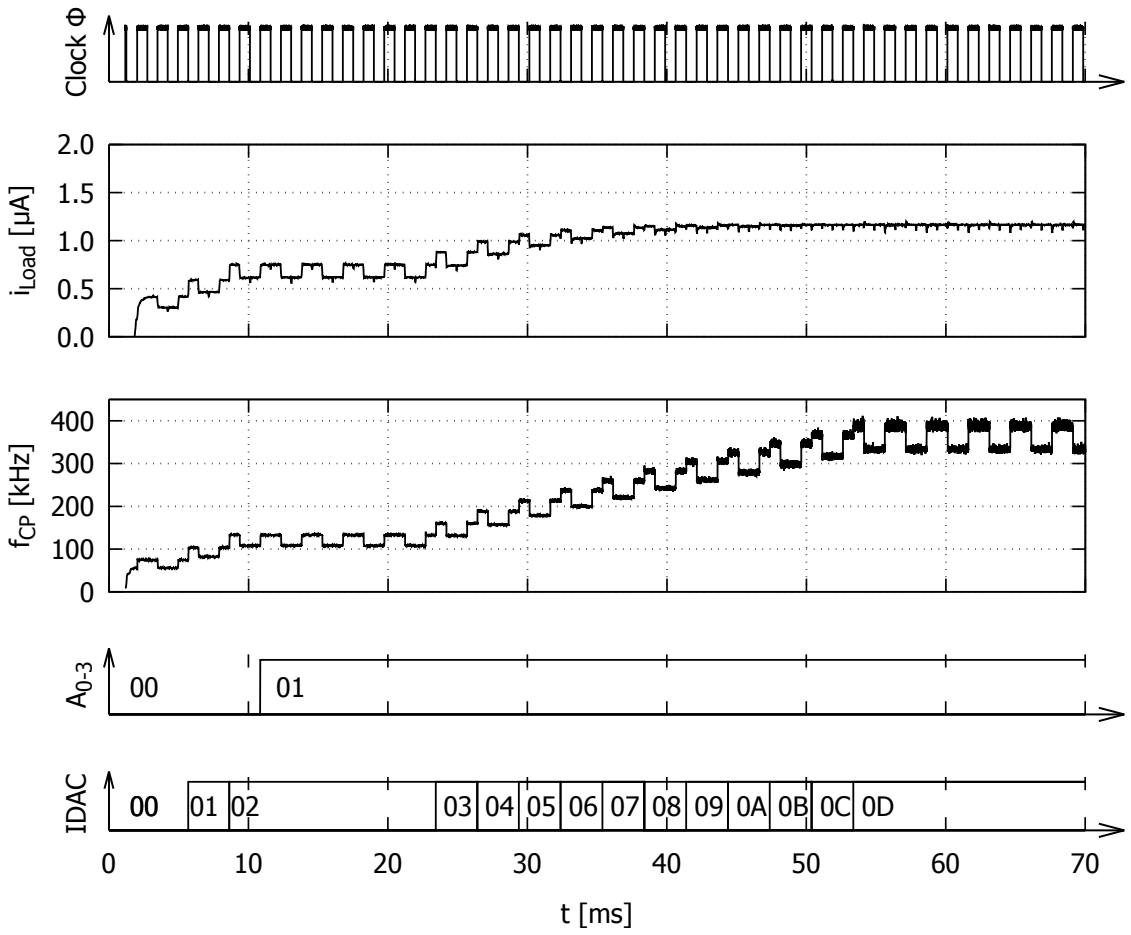


Figure 3.22: MPPTA using the IDAC approach instead of the analog integrator. The MPP is found at 55 ms after the start. Test conditions: Red light source at 1 W, constant output voltage at 3.2 V.

anymore, see section 3.1 for the theory behind. As a result the maximum power point is reached at the lowest charge pump frequency, at which i_{Load} stops to increase. This findings explain why the MPPTA finds the optimum frequency always at the lowest counter values instead of toggling between frequencies which are already too high although they would theoretically deliver the same output current.

In a next test, the response of the MPPTA to a non-constant output voltage is observed. As derived in the theory section 3.1, the optimum charge pump frequency also depends on the present output voltage of the converter. For this test a 200 nF capacitor is charged by the harvester. The charging process is depicted in Fig. 3.24a ranging from 1.5 V to 5 V. For comparison reasons, the same input source conditions as in Fig.3.23 are used. In the theory section it is shown that a rising output voltage requires an increasing collection probability (CP) clock, see Fig. 3.7a. As Fig. 3.24a depicts, the MPPTA adapts the frequency like predicted. After the initial ramp-up of the converter frequency the MPP is found after 80 ms.

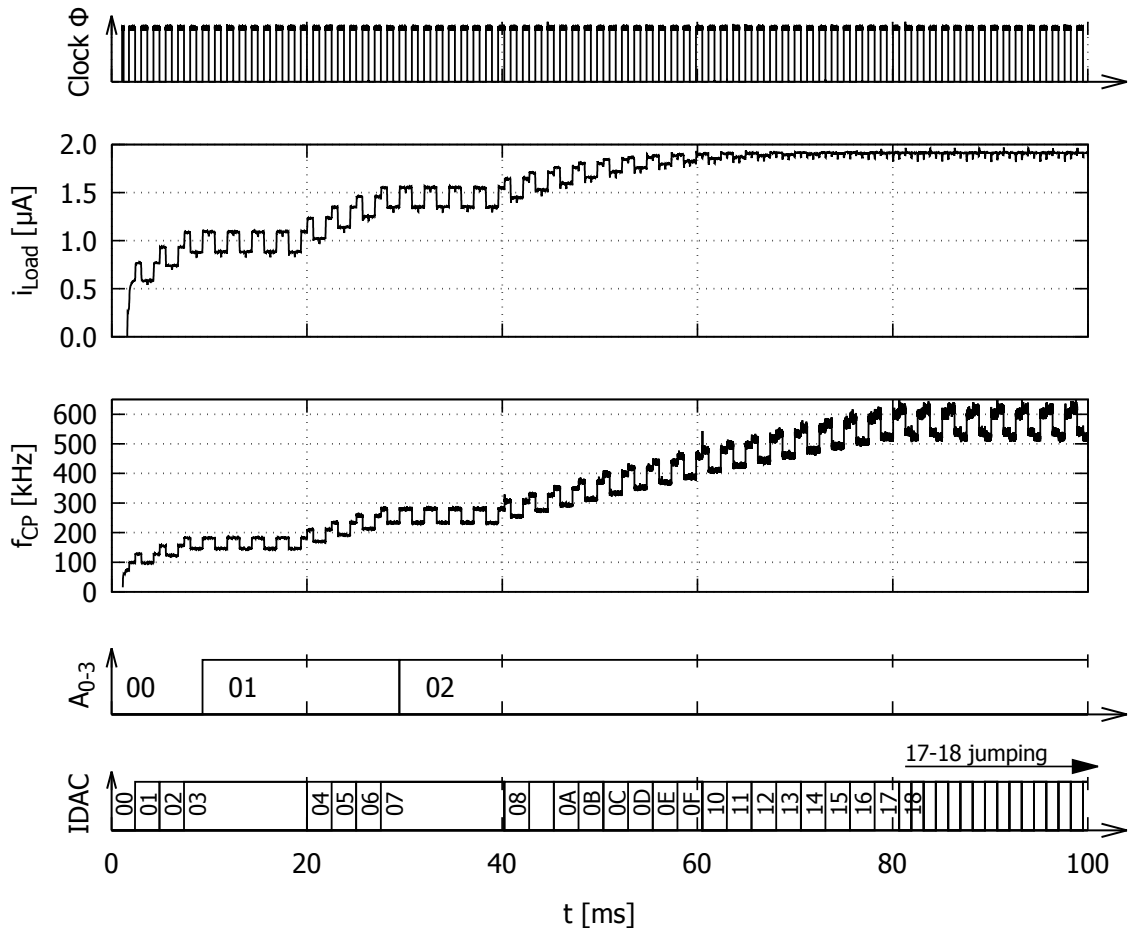
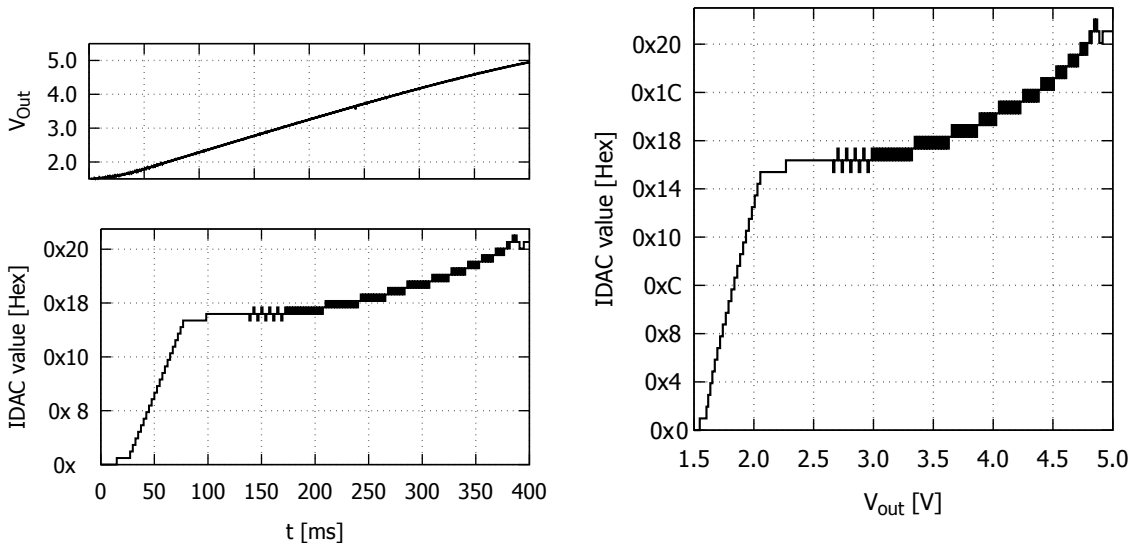


Figure 3.23: MPPTA using the IDAC approach instead of the analog integrator. The MPP is found at 80 ms after the start. Test conditions: Red light source at 2.6 W, constant output voltage at 3.2 V.

This initially found frequency is continuously adjusted during the charging process. The IDAC value correlates to the CP clock frequency.

The overall power consumption of the implemented MPPTA is $\approx 60\,nA$. This quiescent current represents a mentionable portion of the lowest possible current to be measured. As a result, the MPPTA will reduce the system efficiency for ultra-low power operation. However, without tracking algorithm this low power operation would not be serviced, because a static charge pump clock suited for this power regime would be inefficient as a whole.

The feasibility of the proposed algorithm of finding the lowest frequency at which the output current stops to increase is shown in the previous figures. Consequently, the system is working on the MPP. To quantify the efficiency of the algorithm, the relative error of the achieved output power to the highest possible output power is evaluated in the results section 3.3.6.



(a) The increasing output voltage causes the MPPTA to continuously adapt the converter frequency.

(b) After the MPP is found, the CP clock increases accordingly to the output voltage.

Figure 3.24: The IDAC value, which represents the CP clock frequency, continuously adapts to the rising output voltage of the charged 200 nF capacitor. As theory predicted, the rising output voltage requires a rising CP frequency to keep operating at MPP.

3.3.4 Current Controlled Oscillator and Modulator

The single chip solar harvester comprises two oscillators. The first one is the CCO which is the clock source for the DC/DC converters. The second one is the system oscillator for the maximum power point tracking algorithm. Both oscillators are inverter based, current starved, fife stage ring oscillators, which differ only in their operating frequency. The MPPT system clock frequency is set to be in the single digit kHz range for low power operation. Hence, the system oscillator has additional capacitors added to the gate capacitances. The CCO for the charge pump clock has no additional capacitors to keep the power consumption at high clock frequencies lower. Requirements regarding the frequency stability, jitter, and power supply sensitivity are very relaxed. Neither the DC/DC converter nor the MPPTA rely on a precise frequency. Nevertheless, the requirements on the power dissipation of the oscillators are demanding.

Fig. 3.25 shows the proposed oscillator design. This circuit includes the oscillator core (only two out of five stages are drawn), a slew rate enhancement stage, and a standard output inverter. As mentioned before, additional capacitors as drawn in Fig. 3.25 are used only for the low frequency system oscillator. T_{P1}, T_{P2} and T_{P7} as well as T_{N1}, T_{N2} and T_{N7} serve as current sources. During startup, the current of the CCO is limited to $I_{CCOstart}$ by these transistors. The CCO has no dedicated enable. Once the solar voltage V_{pos} has reached a

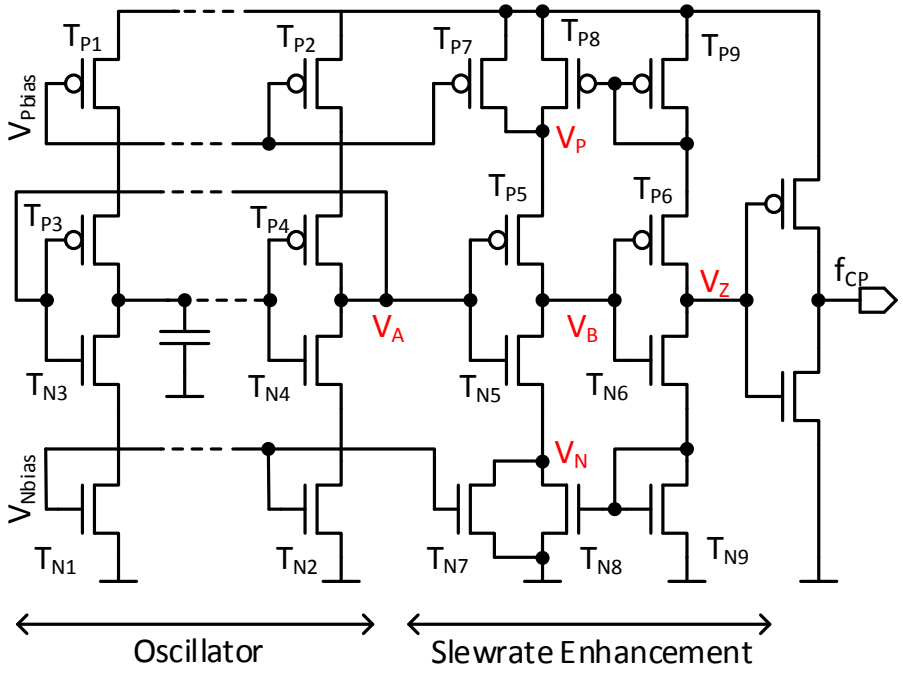


Figure 3.25: Current starved ring oscillator with self-biased slew rate enhancement. The frequency is controlled by the N- P-channel current mirrors (V_{Pbias}, V_{Nbias}). The 1 kHz system clock as well as the variable charge pump clock utilize this oscillator approach.

sufficient level, the CCO starts oscillation and therefore also the charge pumps. The system oscillator on the other side is active only when the *POWER-OK* signal is set, indicating that the necessary voltage and bias current source for the MPPT are available. Each oscillator branch is limited to a bias current of 1 nA.

When using a current starved ring design especially in combination with additional capacitors, a very low frequency and ultra-low power consumption can be achieved in the oscillators core cell. Nevertheless, when the oscillator is used as digital clock source, the power consumption substantially rises. This increase is caused by the unavoidable circuit part that does the slew rate enhancement e.g. properly scaled buffers, a Schmitt trigger, or an OTA. The implemented ultra-low power oscillator uses a different but very efficient circuit to increase the slew rate. The proposed slew rate enhancement does not need a static bias current and it can be used in a wide frequency range. The results of a transient simulation including back annotated layout parasitics are depicted in Fig.3.26.

Assuming V_A rises with a low slew rate from VSS to VDD: The first inverter stage (T_{P5} and T_{N5}) after the fed back oscillator signal (V_A) is still current starved by T_{P7} and T_{N7}. At the beginning, the channel of T_{P5} is inverted and T_{N5} is not conducting. The node voltages V_P and V_N are at VDD and VSS, respectively, as depicted in Fig. 3.26. While V_A rises further, T_{N5} changes to weak inversion, enabling a current to flow through T_{P5}, T_{N5}. While V_B is at high potential is has to be discharged by T_{N5} and T_{N7}. As T_{P7} and T_{N7} are limited to

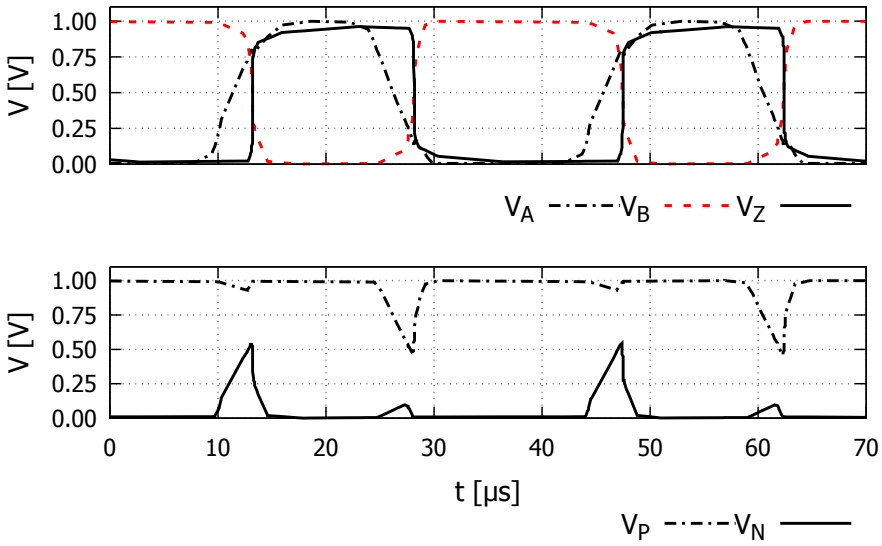


Figure 3.26: Transient simulation of slew rate enhancement node voltages according to Fig. 3.25.

same current, the potential V_N rises, because T_{N5} sinks current from V_B plus the current from T_{P5}. Therefore T_{N7} is operating as current sink while T_{P7} is not sourcing the biased current. As a result, V_P stays at a high potential. V_N follows V_A until T_{P6} and T_{N6} generate a drain current. This drain current is mirrored back to the T_{PN5} path, leading to a lowering of V_N and therefore to a higher gate-source voltage of T_{N5}. In this operating point V_A has already passed the nominal trip point, because V_N followed V_A. As V_N and V_P are building up asymmetric around the trip point, the feedback of the current mirror supports T_{P5}, T_{N5}, as well as T_{P6}, and T_{N6} to pass their trip point very fast and due to the gain of the stage almost independently of the incoming slew rate. The transition of V_A from VDD to VSS works vice versa.

Fig 3.27 shows the total power dissipation of the clock source including the oscillator and a 10/1 clock driver without load at different supplies over a given frequency range. The total power dissipation is compared to the same oscillator core using two inverters to gain the slew rate instead of the proposed slew rate enhancement. The comparative oscillator has no feedback path. Its slew rate gain is done by a long channel inverter with a higher threshold voltage process option for the first stage after the oscillator core plus one small standard inverter before the signal is fed to the 10/1 clock driver. The advantage of the proposed feedback slew rate enhancement design regarding power dissipation is given when the supply voltage rises above the transistors threshold voltage or when operating in a low frequency range. Nevertheless it is worth noting, that an inverter based ring oscillator, without advanced slew rate enhancement, is not an applicable design for an ultra-low power low frequency clock source. Thus, no comparison regarding the power dissipation below 10 kHz is made. However, the proposed design keeps scaling its power dissipation also below 10 kHz. Due to the reliable operation and the ultra-low power dissipation of the proposed oscillator

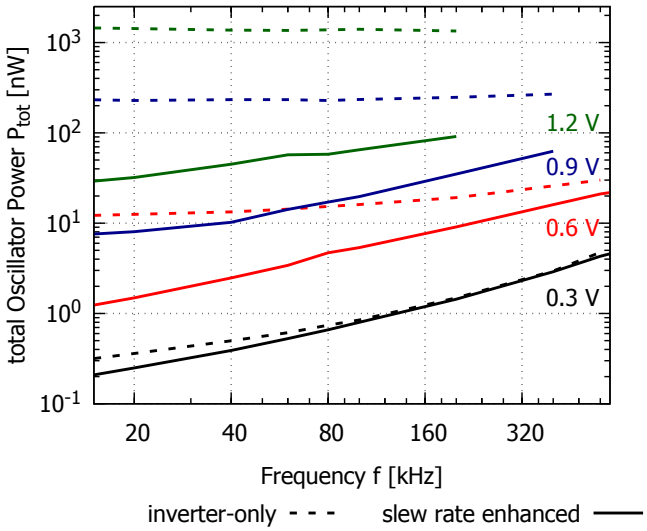


Figure 3.27: Power consumption of the oscillator with slew rate enhancement (solid line) compared to a design without feedback circuit (dotted line). The total power consumptions are compared at four different supply voltages including a 10/1 clock driver. Parasitic back annotated layout simulations. Double logarithmic scale.

besides the charge pump clock, also the MPPTA is clocked with this design, operating at 1 kHz.

3.3.5 Results - Simulation and Measurements

To determine the tracking error, in a first approach the input voltage is observed, because this voltage is bonded to a test chip pad and can also be measured. The error of the algorithm was then defined as the relative deviation from the simulated optimum input voltage to the measured voltage. Similar to the FOC method, the idea was to determine the tracking efficiency by comparing the input voltages under optimum load condition. As simulation and measurement need to be comparable a measurement-lookup-table based model of the solar cell is used to simulate the harvesting system. The input voltage of the solar cell model is then simulated in combination with the charge pump. The lookup-table contains the measured voltage and current values of the on-chip solar cell at 10 different light intensities. In-between values are linear interpolated. In the simulation, the converter frequency is then swept to find the maximum output power and the corresponding input voltage. Results are depicted in Fig. 3.28. The simulated input voltage at max. output power is named V_{Sim}.

For the measurement the harvester is operated in the solar test setup to match the simulation model. By lining up the short circuit currents of the measurement and the model the setups

can be compared. This method showed a maximum error of 3% for V_{out}=4.2 V and I_{SC}=30 µA. In addition to the simulated and measured solar cell voltage also the measured input voltage of the solar cell at maximum source power, V_{MPPT} is depicted in Fig. 3.28. This voltage would be aimed by an conventional MPPTA when using the FOC method. As can be seen, the error would be much larger, because the FOC method does not consider the charging process of the pump capacitors, the output voltage, or parasitic losses.

However, the input voltage based method of determining the tracking algorithm efficiency has some weak points. First of all the error is calculated by involving a measured and a simulated value. The simulated value is based on a model, which relies on characterization measurements that consider only voltage and current plus a static capacitance to describe the junction capacitance. A proper model of the on-chip solar cell, which allows to observe errors smaller than 3%, would need a voltage depended capacitance at least. Another error source that weakens the presented input voltage method is the simulation of the parasitic charge pump capacitors. It was shown, that the parasitics have a considerable influence on the MPP. This is why a simulation of the charge pump efficiency should not be taken as reliable result. The results from Fig. 3.28 have been achieved by the integrator based MPPTA.

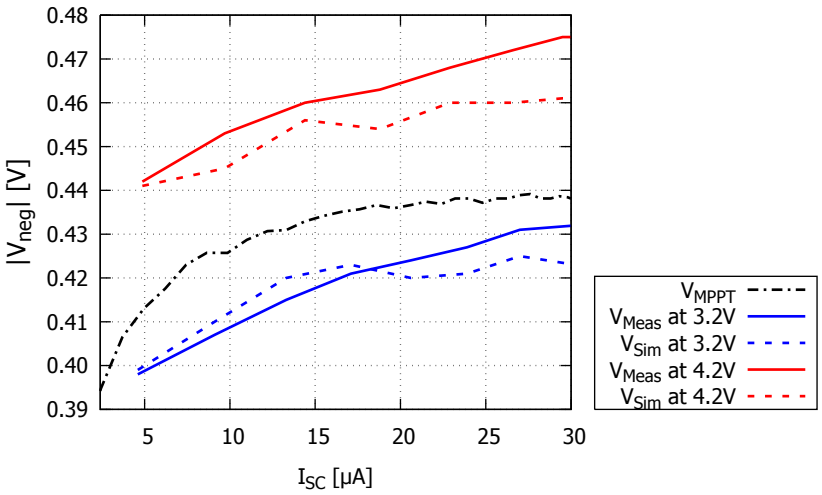


Figure 3.28: Source voltage loaded by the charge pump as function of the short circuit current (illumination). Measured source voltage in comparison to simulated optimum for two different output voltages. A FOC based algorithm would track the black dotted line creating a larger error.

The newest test chip which utilizes the more reliable IDAC accumulation approach allows to deactivate the MPPTA and to adjust the charge pump frequency from extern. After deactivation the MPPTA is detached from the comparator and the counter value which determines the oscillator frequency can be set by two external pads. To prevent a false measurement, the MPPTA is still operating in the detached mode, meaning that it still draws the required power. As a result, the tracking error can be measured without involving any

Table 3.1: MPPTA relative errors and efficiencies

	I_{SC}=10 µA			I_{SC}=20 µA			I_{SC}=30 µA		
V_{out}	e_{MPPTA}	η_{MPP}	η_{MAX}	e_{MPPTA}	η_{MPP}	η_{MAX}	e_{MPPTA}	η_{MPP}	η_{MAX}
3.2	0.19	38.98	40.22	0.05*	49.43	51.62	0.05*	49.25	51.57
4.2	1.80	39.45	39.63	0.05*	46.09	47.48	0.31	46.99	47.85

- All values are given in %.
* The error is less than the noise level of the measurement setup. It amounts to be less than 500 ppm.

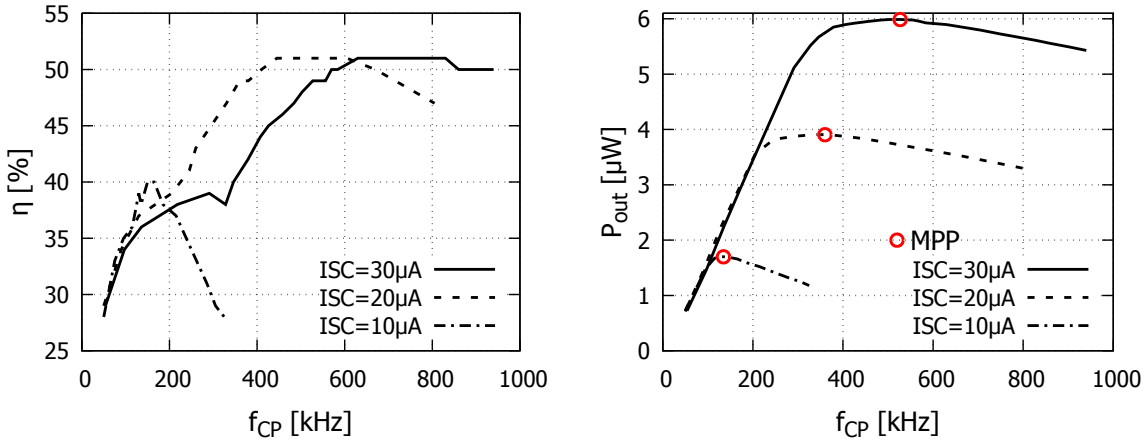
simulation or model. The error of the algorithm is defined as the relative deviation from the output power found by the algorithm to the highest possible output power, see equation 3.3.9. Measurement results are depicted in Fig. 3.29 and Fig. 3.30 for constant output voltages of 3.2 V and 4.2 V, respectively. A measurement summary of the MPPTA error, the system efficiencies at MPP, and the maximum efficiency is given in table 3.1. Values in table 3.1 are calculated using equations 3.3.9, 3.3.10, and 3.3.11. In contrast to the first attempt of defining the tracking efficiency, the new and more precise measurement method reduces uncertainness to the accuracy of the measurement setup. Reproducible results have been achieved for output currents down to ±500 pA. As table 3.1 shows, the measured worst case error, e_{MPPTA}, of the algorithm is less than 1.8 %. The average error of the implemented algorithm is 0.4% or which corresponds to an average tracking efficiency of 99.6 %.

The measured data also allows calculating the efficiency of the system, because input power was well as output power have been measured with respect to the converter frequency. Efficiencies are depicted in Fig. 3.29a and Fig. 3.30a for output voltages of 3.2 V and 4.2 V, respectively. It can be seen, that the frequency band for an efficient operation becomes narrower with decreasing input power. This is caused by the reduction of output power due to the increasing parasitic losses while the input power is slightly increasing. At higher power source conditions ($I_{SC} = 30\mu A$) measurements show a significant reduction of input power with increasing charge pump clock frequency. The reduced input power is already predicted in the theory section, see Fig. 3.4b. Due to this behavior, the efficiency of the system stays high and can even increase for charge pump clock frequencies above the ideal frequency.

$$e_{MPPTA} = \frac{100\,(P_{out-MAX} - P_{out-MPPTA})}{P_{out-MAX}} = \frac{100\,(I_{out-MAX} - I_{out-MPPTA})}{I_{out-MAX}}[\%] \quad (3.3.9)$$

$$\eta_{MPP} = \frac{100 P_{out-MPPTA}}{P_{in-MPPTA}}[\%] \quad (3.3.10)$$

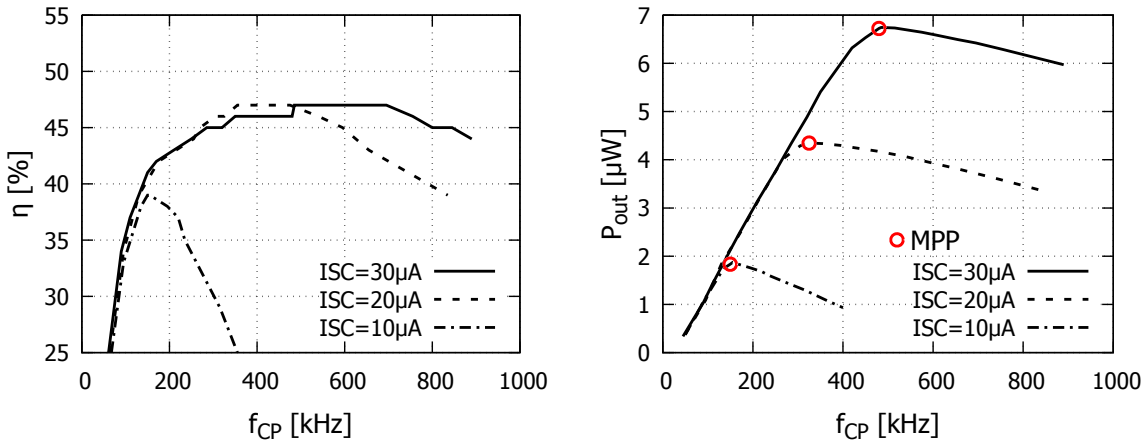
$$\max_{0<f_{CP}} \left\{ \eta_{MAX} = \frac{100 P_{out}(f_{CP})}{P_{in}(f_{CP})} \right\}[\%] \quad (3.3.11)$$



(a) Overall system efficiencies as functions of the charge pump clock frequency.

(b) Charge Pump output power at V_{out}=3.2 V. Circles indicate the operating point set by the MPPTA.

Figure 3.29: Measurement results of the efficiency and output power as functions of the converter frequency. The output voltage is kept constant at 3.2 V during measurement.



(a) SSystem efficiency plot. The correct converter frequency gains importance as the input power decreases.

(b) Charge Pump output power at V_{out}=4.2 V. Circles indicate the operating point set by the MPPTA.

Figure 3.30: Measurement results of the efficiency and output power as functions of the converter frequency. The output voltage is kept constant at 4.2 V during measurement.

3.3.6 Conclusion

A generic ultra-low power and fully autonomous MPPTA implementation that maximizes the harvester's output power is presented. The MPPTA is capable to sense currents between 50 nA and 500 µA. The implementation maximizes the output power of the DC-DC converter. Hence, it inherently considers loss mechanisms of the integrated charge pump. Utilizing the proposed approach, also the characteristic of the source is automatically considered per design. It adapts continuously to environmental changes at an update rate of 1 kHz, while consuming less than 100 nA independently of the output power. The key circuit blocks which are the high side current sensor, the oscillator, the modulator, and the analog algorithm are explained on transistor level. It is shown that the loaded input voltage follows the simulated optimum within a maximum deviation of 3 % based on simulation and measurements taken from the first test chip I designed within this work. On the newest test-chip a mixed signal implementation replaces the older fully analog algorithm gaining a higher reliability and reducing the average tracking error to be less than 0.4 %. This tracking error is based on measurements without involving any models or simulations.

The measurement results also confirm one key finding of the theory section, namely the highest input power does not necessarily lead to a maximum output power. Hence, the maximum efficiency of the system is independent from the maximum power point. Therefore state-of-the-art approaches that track input related signals cannot maximize the output power for the proposed monolithic design, even if the MPP of the source is correctly found. The proposed approach does not maximize the system efficiency in terms of output power over input power, see equation 3.3.11, but it maximizes the output power as required by a harvester.

Chapter 4

Charge Pump

This chapter introduces the monolithic DC/DC converter. A concept overview describes all necessary parts of the charge pump as well as power related considerations for ultra-low power operation. Due to the monolithic approach of the harvester a straight forward implementation of a charge pump was not possible. Within this work I therefore developed a novel flying-capacitor driver with built-in level-shifting which increases the signal swing for proper switch operation. Measures have been taken to ensure a startup of the self-supplied chip as well as handling the negative voltage of the harvesting solar cells. The converter has been taped out on three test chips without major design changes. Only the reliability of the capacitor driver has been improved from the first to the last chip.

I gave an outlook on the charge pump concept for the monolithic solar cell approach at the Solid State Device Conference in 2015 [17]. First test results of the converter have been presented at a poster session at the University Evening at the Infineon Headquarter in Munich in 2016 [41]. ■

4.1 Charge Pump Concept

The most critical issue of the charge pump concept is so keep the voltage gain of the stages greater than one at startup. To ensure this requirement, even under ultra-low power operation, the intermediate pump-stages and the output are not allowed to be loaded e.g. by oscillators or the clock generator. Therefore a dedicated power net (V_{pos}) is used to supply all peripherals necessary to operate the charge pump. This supply is created by the p-diffusion in n-well. Although this junction delivers much less power per area than the n-well to substrate it is used, because of the positive voltage with respect to ground. The voltage V_{pos} is typically in the range between 400 mV and 500 V depending on light conditions. This voltage is high enough to operate standard logic gates at low frequencies and it is slightly above the threshold voltage of a standard transistor of the process. Another reason for introducing a second solar cell array (V_{pos}) besides the harvesting solar cells (V_{neg}) is the before mentioned positive voltage with respect to ground. Due to the absence of an isolation on silicon option, the negative voltage of the harvesting cells cannot be connected to a large N-channel metal–oxide–semiconductor field-effect transistor (NMOS) source area, because this would lead to an extensive leakage current into the substrate. Figure 4.1 depicts an overview of the supply nets. It can be seen that a second smaller charge pump is implemented which

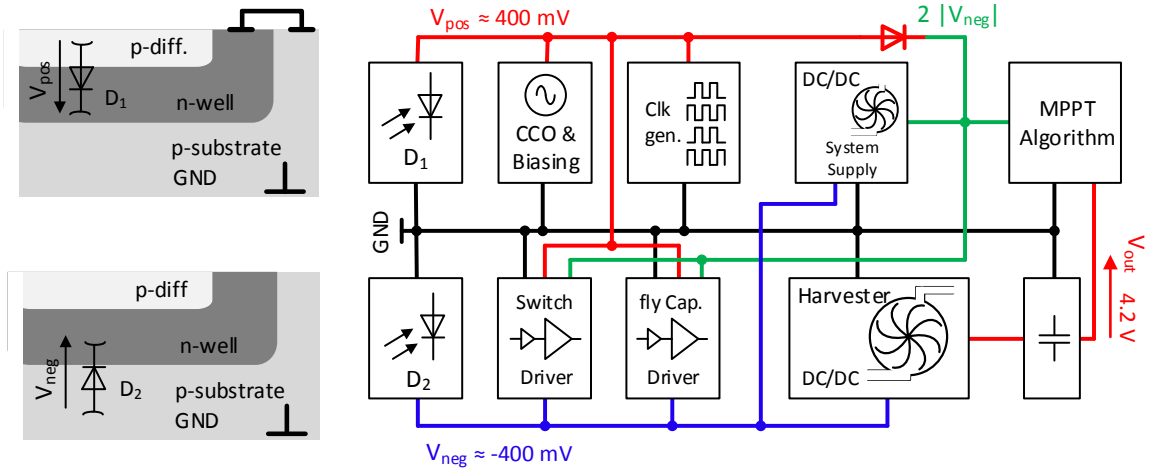


Figure 4.1: Block level implementation of the power supply nets.

produces $|2xV_{neg}|$. The complete cadence top-level schematic of this charge pump is shown in Fig. 4.4. It is worth mentioning, that the efficiency measurements of the total harvesting system given in section 3.3.5 do consider also the power used by the second two stage pump by adding it to the input power drawn from V_{neg}.

This intermediate supply is needed for the maximum power point tracking algorithm (MPPTA), because it contains several amplifiers which utilize cascodes that cannot be functional at 400 mV. The other reason for generating $|2xV_{neg}|$ is the required signal swing for the charge pump drivers. To keep the on-resistances of the charge pump switches low, a signal swing of only 400 mV is not sufficient. However, before the system has started also the output voltage of the system pump is low and therefore all on-resistances are high due to the reduced signal swing. To manage a proper and reliable startup a transistor-diode is used to support the output of the system pump. This wide transistor diode is indicated in Fig. 4.1 by the red diode symbol. A rising output voltage of the system supply decreases the on-resistances of the switches and a further rising the output is possible. Before the system supply has built up, therefore also the charge pump clock is set to a low initial frequency of 50 kHz to achieve the required voltage gain. The output voltage of the system supply is compared to a reference, setting a *POWER_OK* bit to indicate a sufficient signal swing for the switches. After the *POWER_OK* is set the MPPTA is enabled and higher charge pump clock rates are allowed respectively set by the MPPTA. These measures achieve a minimum loading of the charge pump before the on-resistances are low enough to let the system operate autonomously.

Both charge pumps use a double bootstrap approach (naming is adopted from [42]). The bootstrapping refers to the high-side switch operation and double refers to the implementation of two 180°phase shifted paths. Typically the double approach is used if the output ripple should be reduced. The necessary phase shifted clocks have to be generated regardless of

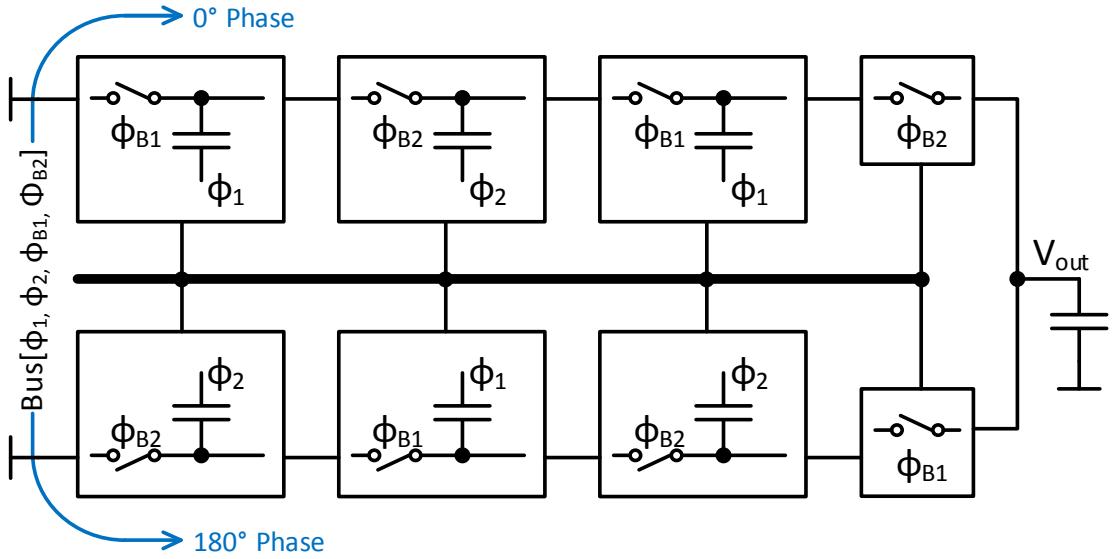
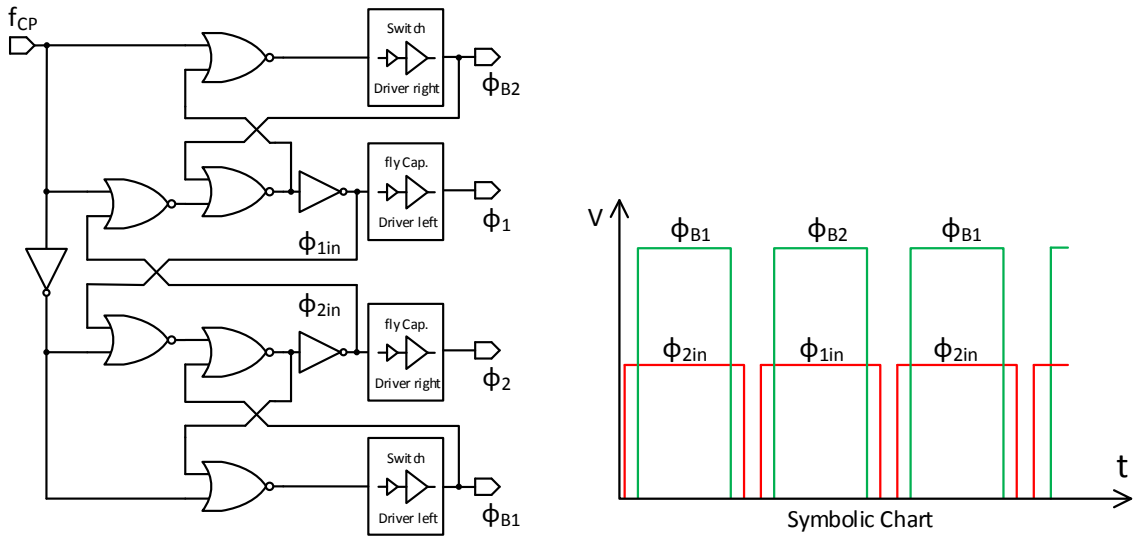


Figure 4.2: Basic block level concept of a three stage double implementation charge pump.

single or double approach, if more than one pump stage is implemented. In this work the double implementation, see Fig. 4.2, is not chosen to minimize the output voltage ripple however. When charging external energy storage a low ripple is not required. The double implementation, however, also reduces the ripple on the input voltage, in this case the ripple on the solar voltage V_{neg} and the ripple of the output current that is measured by the MPPTA. By keeping the input ripple smaller the average deviation from the ideal source loading voltage is reduced. Another advantage is the distribution of the current into two paths which relaxes the requirements of the on-resistances of the switches. The overall silicon area increase of a double implementation is negligible, because the area is mainly determined by the flying capacitors, which are half the size but implemented twice.

The operation of the bootstrapped high-side switches between subsequent flying capacitors is done by non-overlapping signals. State-of-the art approaches therefore utilize delay lines which use the propagation delay of buffers or buffers with additional capacitive loading for increased delays. This implementation was not chosen, because it would have required several extra components which all draw additional supply current. Especially if the delay line uses capacitive loading, the extra power consumption is considerably higher. Therefore the proposed and implemented clock generator utilizes the intrinsic delay of the high-side switch-drivers themselves to introduce the necessary delay as can be seen in Fig. 4.3.



(a) Non-overlapping clock generator. It ensures that subsequent high-side switches are not closed at same. It is also guaranteed that flying capacitors are operated after the switches have changed their stages. These measures are necessary to prevent backwards leakage.

(b) Symbolic drawing of the non-overlapping signals. The signals for the high-side switches have increased signal amplitudes due to the switch driver's boostrapping.

Figure 4.3: Clock generator logic gates are directly supplied by V_{pos}.The MPPT oscillator delivers f_{CP}. Additional delay is introduced by the propagation delay of the switch driver itself.

4.2 Charge Pump Implementation

4.2.1 Pump Stage with High-Side Switch

The charge pump stages are built as depicted in Fig. 4.5 that shows a single stage. For the system supply pump two stages are implemented. It is worth mentioning that the first stage always changes the negative input voltage to a positive voltage and the second stage starts to increase the magnitude. Therefore the number of implemented stages equals the multiplication of the absolute input voltage. The above half is connected to operate without phase shift and the lower half of the stage uses 180° phase shifted signals. Signals sketched above the dash-dotted line indicate the voltage swing that is applied by the drivers. During startup this voltage swing on Φ_{B1} and Φ_{B2} is less than V_{pos} which requires the low pump frequency.

Differences to a typical implementation e.g. [42] or [43] are the cross coupled implementation of T_1 and T_2, the bootstrap-top-plate diodes, and the type of capacitors. In typical applications for example when generating a write or erase voltage for a non-volatile memory, the voltage to be boosted comes from a low impedance supply voltage. Hence, when this supply is loaded by the fly-cap driver no significant ripple is expected. Further the signal swing of the fly-cap

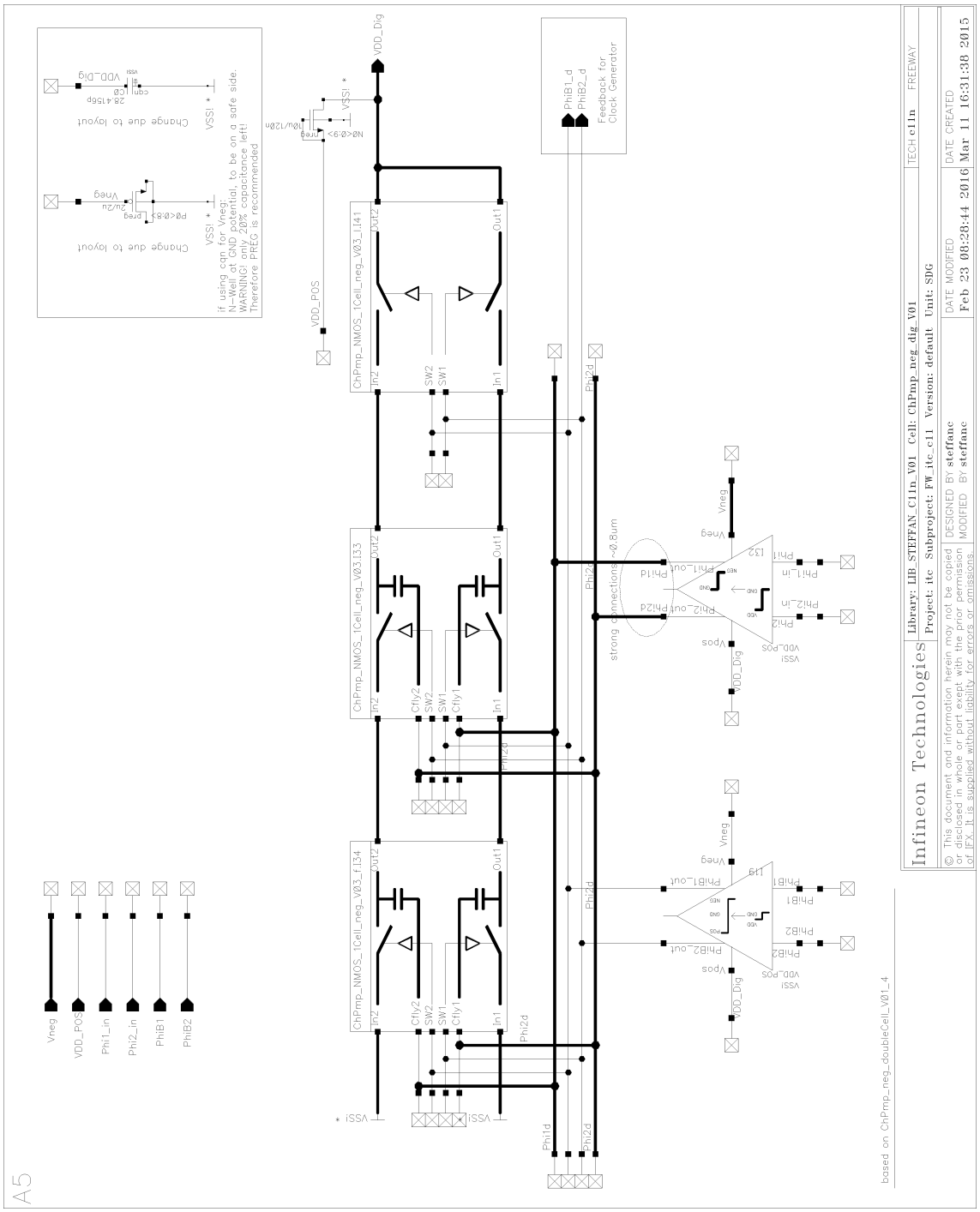


Figure 4.4: Top-level schematic of the system supply charge pump. Bus lines which carry load current are drawn thick. Circuits of the depicted block levels are discussed in detail in section 4.2.1.

driver is also high enough to properly operate a MOS switch. In these applications it is therefore sufficient to connect the gate of T_1 to the output of the pump-stage. A second bootstrapped transistor (T_2) is not necessary because the top plate of C_{FlyX} is a reliable switch signal for T_1. In this work an additional switch signal for the bootstrapping is required. The top plates of the flying capacitors do have a low signal swing (V_{neg} to GND) and no stable signal due to changing source impedance of V_{neg} with light conditions. However, the additional bootstrapping signal is already generated, because the high-side gate signal of the opposite phase can be used. To gain the reliability of the circuit, the top plates of the bootstrapping capacitors are diode connected to the output voltage of each individual pump-stage. This measure ensures that the gates of T_1 and T_2 cannot build up potentials which prevent both transistors to switch-off.

Figure 4.5 shows that all capacitors are built by the PMOS oxide capacitor. The reason is, that no other capacitor in the used process besides a metal-metal type can be charged to the negative voltage without loss in capacitance or leakage. All flying-capacitors are built using a horizontal metal-metal capacitor stack on top which is parallel connected to the oxide capacitor. This additional capacitance is built by using routing metals one to four in an interdigitated layout. The metal fingers are placed at minimum distance allowed by the design rule check. Layout back-annotation shows an approximated capacitance increase of 10 % without adding parasitic capacitance.

A better implementation in terms of efficiency would be achieved by utilizing poly-poly capacitors. They have a much smaller parasitic capacitance (αC_{Fly}) compared to the PMOS oxide. As a result the efficiency of the system could be higher. However, the poly-poly option was not available for the test-chips, therefore the overall maximum possible efficiency is lower than for a charge pump implemented in a flash process. To keep the channel of the PMOS capacitors inverted, which is mandatory to maintain the capacitance, the gates are connected to the lower potential.

4.2.2 Switch and Capacitor Drivers

Due to efficiency requirements as well as making startup of the harvester possible, a supply for the signal generation that comes directly from the input source is mandatory. Therefore the signal generation for the charge pumps is supplied by its own solar cell array delivering V_{pos}, also previously described in section 4.1. Hence, the charge pump driver must be capable to operate under supply conditions which are lower than V_{pos} during startup. It is also necessary to shift the input signal (Φ_{1in} and Φ_{2in}) levels to the required higher and lower supply rails, respectively. After the startup phase, the input signal must be shifted to $|2xV_{neg}|$ which can be twice the input signal amplitude. However, already before startup and during normal operation the input signal must be shifted to the negative supply rail (V_{neg}). In Fig. 4.6 the driver schematic is depicted. The level-shifting is done by bootstrapping the input signal as well as the inverted input signal into two cross coupled transistors pairs. Utilizing two capacitors (C_1 and C_2) and two cross coupled PMOS devices for the high side. Shifting to the negative rail is done utilizing the PMOS oxide capacitance (C_3 and C_4) and two cross coupled NOMS transistors. A simulation of the input signals plus the bootstrapped versions

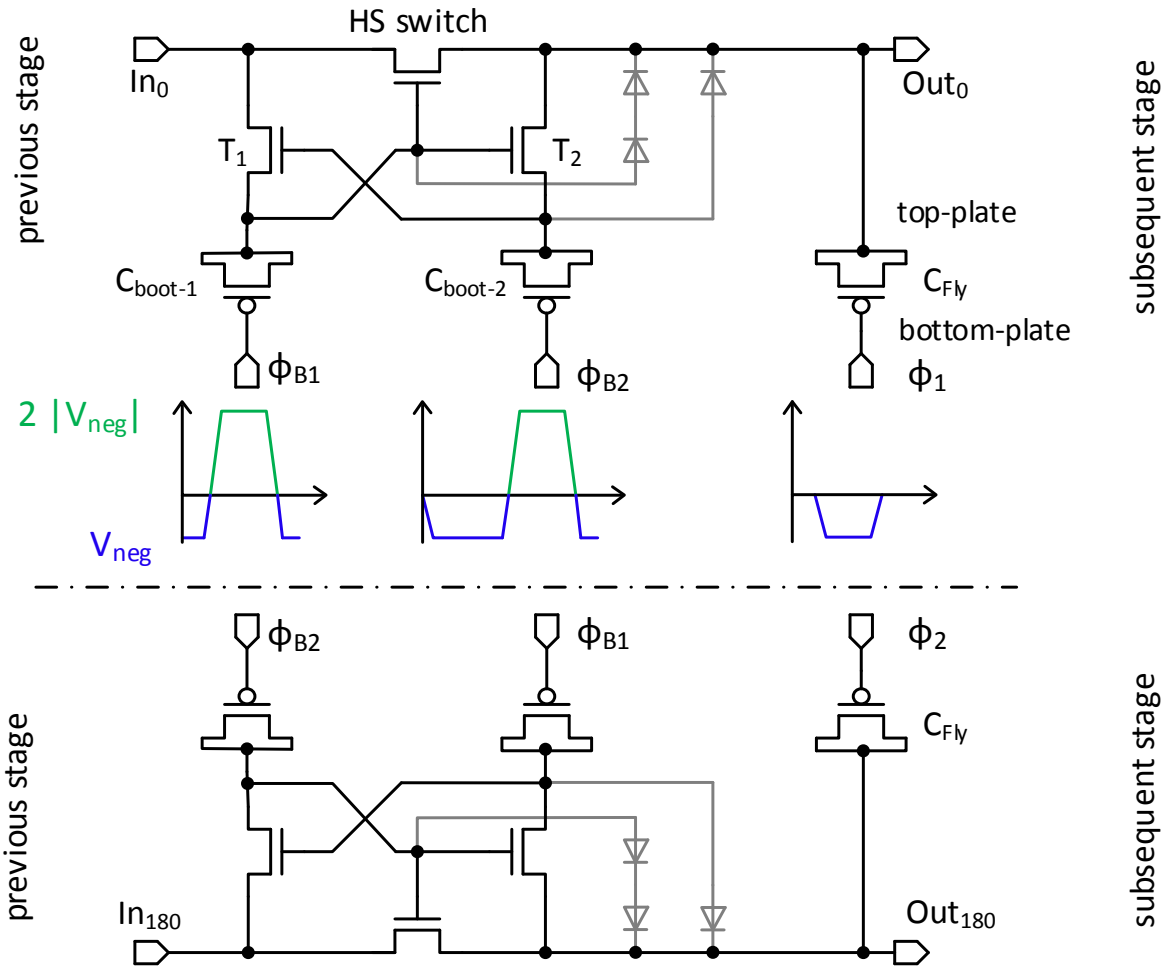


Figure 4.5: Pump stage schematic of the double implementation. PMOS gates are used as capacitors. The color coded charts indicate the voltage swing coming from the drivers.

is given in Fig. 4.7, which depicts the signal transition in the non-overlapping phase in detail. After a first gain stage, the bootstrapped signals are level shifted to signals A and B, respectively, which do have a signal swing between the system supply and V_{neg}. Therefore the output stage is built by NMOS devices.

It is worth mentioning, that the output stage uses a brake-before-make concept. Signals A and B are non-overlapping generated due to the better efficiency of the charge pump. This implementation is reused by the driver circuit. Instead of generating inverted versions of A and B for the low-side switches, the signals are used twice, inherently implementing a brake-before-make. Advantages are the absence of any current losses through the driver stage as well as the high impedance (high-Z) condition during the non-overlapping time.

Both output stages are high-Z while A and B are low. During this condition the outputs

of the driver are shorted by applying signal SC to the gate of T_{SC}. Shorting the driver outputs during the transition phase is implemented to reuse a part of the charge stored in the parasitic capacitors of C_{Fly}. This technique increases the efficiency of the pump, because the bottom plate parasitics will already hold approximately half the input voltage. Hence, after transition only half the voltage held by the bottom plate parasitic is shorted by side that switches to low, while the parasitic that needs to be charged to the input voltage already holds half of the voltage. The technique is called charge recycling and can be seen in Fig. 4.7. Charge recycling is described in [44], however the implementation in this work is different. In [44] two dedicated signals (Enable and Short) are generated to switch the driver into high-Z and shorting the outputs. This work does not need dedicated signals, because they are already generated inherently for the charge pump operation and are reused by implementing a NAND gate. The advantage of the proposed approach is a further reduction of power demand for signal generation.

The driver circuits for the flying capacitors and the high-side charge pump switches are the only circuit parts that are connected to the negative input voltage. As a result, all NMOS transistor source connections are forward biased junctions to substrate. Due to the higher doping of the NMOS source area compared to the doping concentration of the power generating n-well the built in voltage of the parasitic source junction is higher. Hence, although the junctions are forward biased, the losses are small. However the source areas of all transistors connected to V_{neg} are kept as small as possible do keep the losses low. For reliability reasons also substrate guard rings surround these devices closely. Figure 4.8 depicts the characteristic diode curves of n-well to substrate junction and the n-diffusion to substrate. The two curves compare the total size of the parasitic source to substrate junction of all implemented pump drivers to one single solar unit cell (40.7 µm x 40.7 µm). It can be seen, that the loss due to the parasitic junction is approximately 1 nA at 0.5 V. Compared to one single solar unit cell, the current loss is one order of magnitude lower within the voltage operation range and is therefore negligible.

The driver circuit for the high-side switches is shown in Fig. 4.9. It can be seen that the driver core, from the input to the bootstrapping transistors is the same as the fly-cap driver utilizes. Due to the required higher output swing, compared to the fly-cap driver, the output stage is connected to the system supply pump. In contrast to the fly-cap driver, the switch driver does not need to deliver high output currents and therefore the output stage utilizes smaller transistors. As a result, the trip point of the output stages is passed fast and no brake-before-make is implemented. However, before the system supply pump has built up its steady state output the signal swing of the driver is low and the current through the driver output stage at trip-point can lower the charge pump gain if switches are directly driven by the bootstrap stage. Therefore a long channel pair is necessary to enhance the slew-rate making the driver more efficient to enable startup.

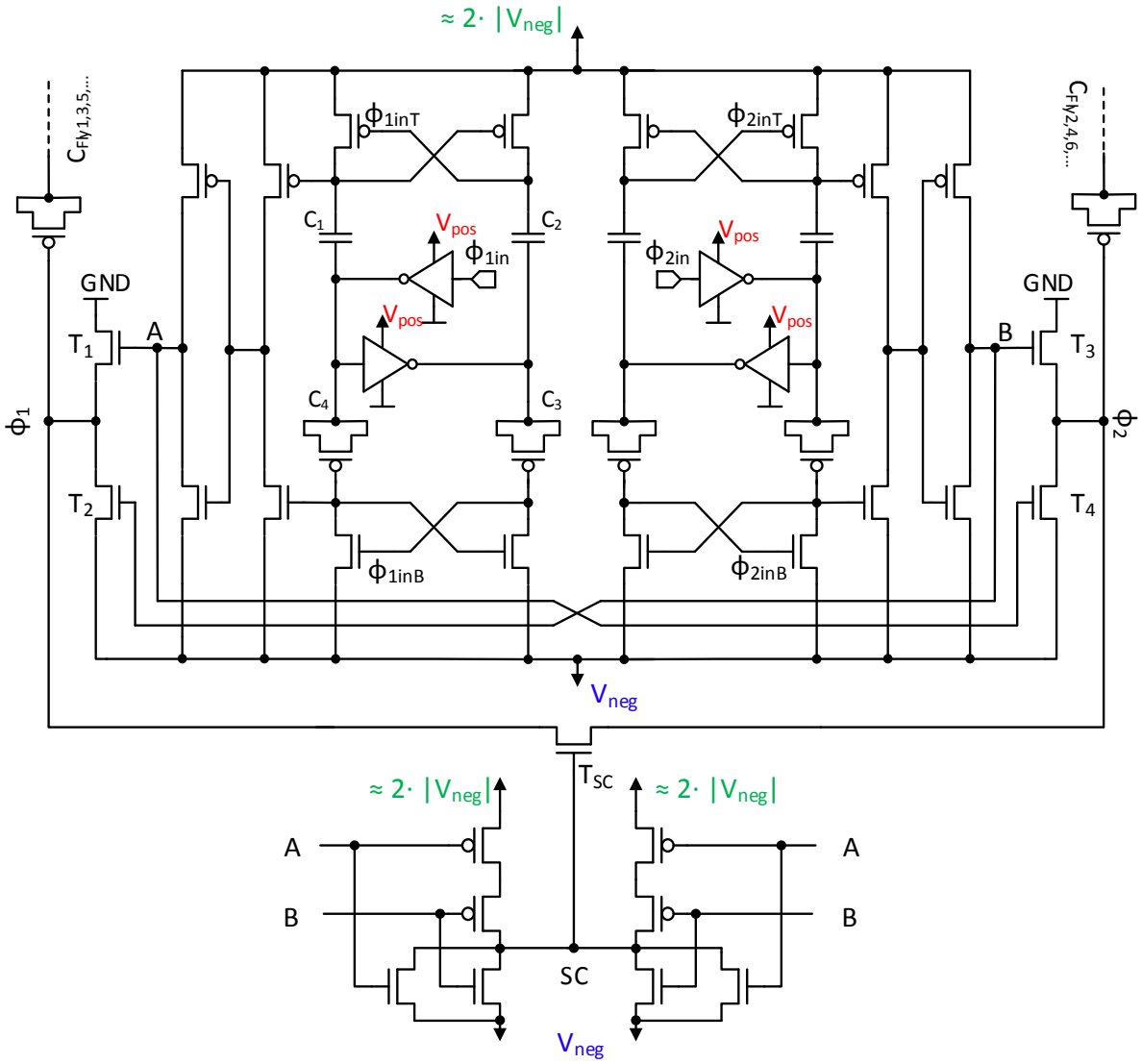


Figure 4.6: Driver circuit of the charge pump capacitors (flying capacitors). Due to symmetry also in layout, the charge recycling addition is implemented twice. The circuit does level shifting via bootstrapping and the output stage uses only NMOS transistors

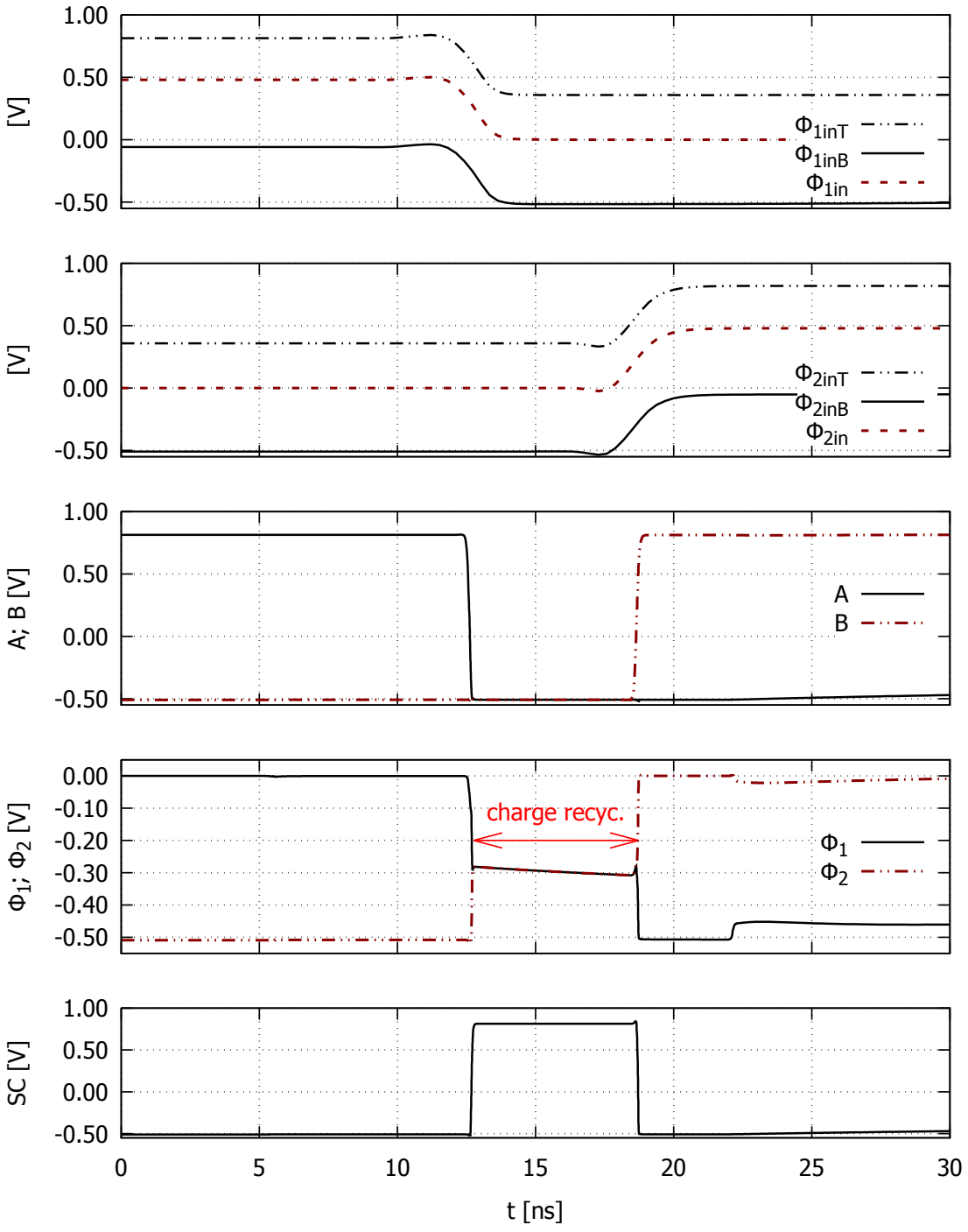


Figure 4.7: Transient simulation of the relevant driver signals. The input is bootstrapped to the higher and to the negative supply rail, respectively. The output stage utilizes only NMOS transistors.

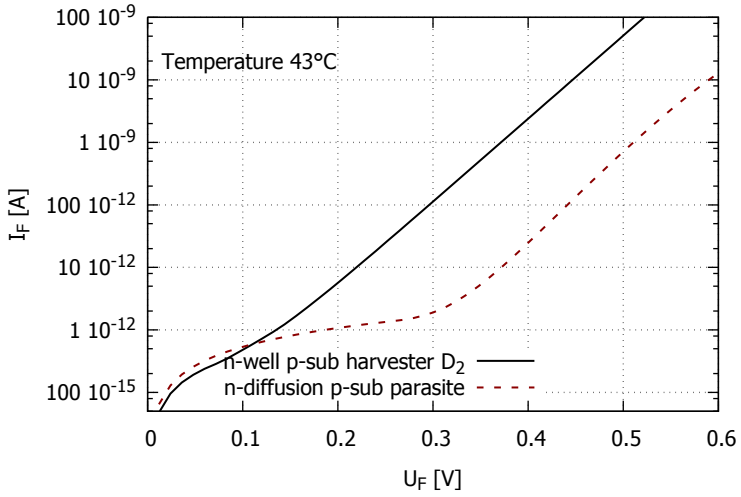


Figure 4.8: Diode characteristics of the forward biased parasitic source to substrate junction and of one single solar unit cell. The losses due to the negative voltage on the source connections are negligible.

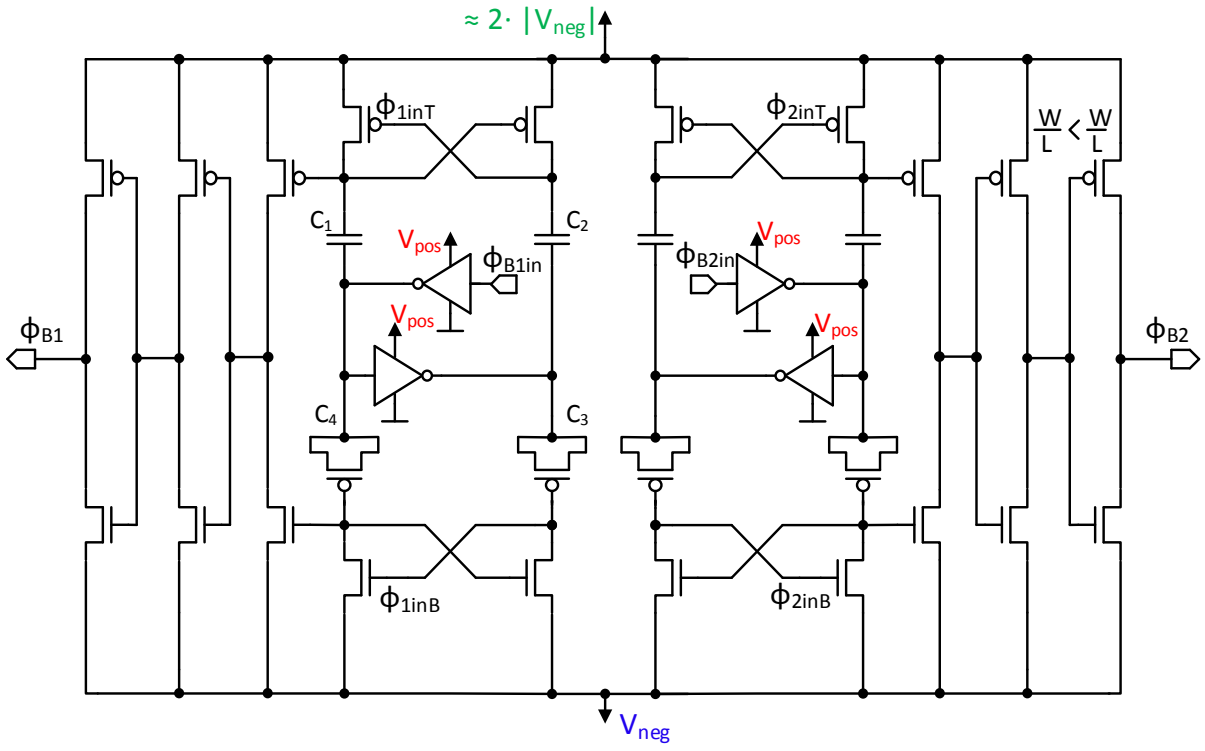


Figure 4.9: Driver circuit for the charge pump high-side switches. The first stage after the bootstrapping circuit is a long channel inverter to increase slewing.

Chapter 5

Conclusion

In the final chapter this work is compared to other recent publications on ultra-low-power energy harvesting systems as well as to low-power harvesting devices available on the market.

A research summary is given to point out the novelty of implementation and the advantages the proposed design offers. The summary also points out issues to be addressed for future work which can improve the existing design.

Achieved results are discussed and the monolithic harvester chip is depicted when operating in a demo application. ■

5.1 Comparison to Related Work

To the best of the authors knowledge, no other monolithic solar harvesting approach comprising solar cells, a DC/DC converter and a continuously working maximum power point tracking algorithm (MPPTA) was published at the time of literature study for this work. Therefore a direct system comparison to other scientific publications is not made in this chapter. However, the individual parts are compared to the most important publications on highly integrated solar harvesting approaches.

In Table 5.1 this work is compared to similar approaches regarding key features. All approaches utilize a single n-well processes. It can be seen, that both compared monolithic designs do not utilize a DC/DC converter. Their concepts are powering the circuitry directly by the low (approx. 0.5 V) solar voltage. These approaches however require special designed circuits to operate reliably at the low supply level. Power management was not included in both designs.

Guilar et al., VLSI [7], have used a two chip approach to overcome the problem of the negative voltage. A current starved oscillator was powered by a second test chip containing the on-chip solar cells. Their achieved normalized power per area outperforms all other published data. It should be mentioned here, that they have used an artificial white light source, which is not further described and which does not allow a direct comparison of the area normalized power. They have also utilized the harvesting connection scheme, which parallel connects the diffusion and the implant junction to achieve the stacked junction approach which is also used in this work. The achieved fill factor (FF) is 65 % which is lower that the FF of this work,

most likely because of the described narrow diffusion junctions inside the n-well. As observed on the solar cell test chip of this work, the placement of these junctions has a major impact on the solar performance and very narrow placement does reduce the FF.

Ayazian et al., BCAS [6], have published a monolithic system suitable to be subcutaneously implanted. The on-chip solar cells are arranged as unit cell array around the circuitry part of the sensor chip. Due to the utilized measurement principle which requires only two current starved ring oscillators, the low supply voltage is directly used. Ayazian et al. utilize the p-diffusion to n-well junction while shorting the n-well to substrate. Due to this connection scheme their achieved power is 9 $\mu W/mm^2$ which is significantly less than achieved by this work. The reported FF is 79 % which is one percent better that the FF of this work. By including the charge pump, developed in this work, having only one pump stage, the harvesting connection scheme could be applied. Meaning that the development of this work would have reduced the size of the implantable sensor from [6] to approximately 10 % of its actual size due to the higher power output.

Lee et al., SSC [4], have published a sensor platform solution built with five stacked chips that are interconnected by bond wires. On-chip solar cells are implemented, which are not further described in the publication, however also a charge pump containing maximum power point tracking (MPPT) is described. The presented MPPT method is based on the fraction of the open circuit voltage (FOC) technique. They observe the open circuit output voltage of the implemented two-, respectively three-stage charge pump to produce low power supply voltages. Recharging of the battery is not described and would not be possible with the low number of implemented stages. However, they presented a concept that allows changing the number of implemented charge pump stages which is further beneficial to increase the overall efficiency of the system. This adaption between the number of stages is used to track the maximum power point (MPP). The tracking efficiency is calculated by setting the power extracted from the source by the harvester in relation to the maximum attainable power at MPP. Calculated from office light intensities to bright sunlight they achieved an average tracking efficiency of 93.5 %. The proposed continuously working MPPTA of this work achieved an average efficiency of 99.6 %

It should be mentioned here, that the theory calculations of this work as well as the measurements have proven that the FOC method is not suitable for switched capacitor DC/DC converters with a fixed number of stages. If the number of stages is adaptive as shown by Lee et al. [4] the FOC method can be a well suited indicator whether the number of stages should be reduced or increased. To achieve a lower tracking error, however, the charge pump frequency must be configurable as shown in this work. Another issue that should be addressed in this comparison section is the equation used to calculate the efficiency of the MPPT. In this work, it is shown that tracking efficiencies for ultra-low power fully integrated harvesting devices cannot be calculated by the source characteristic only. The characteristic of the converter itself influences the result and also the power drawn by the peripherals to operate the MPPTA has to be taken into account for ultra-low power systems. The method, proposed in this work, to measure the real algorithm tracking efficiency as well as to distinguish between tracking efficiency and system efficiency of the harvester itself is mandatory for systems that harvest power in the same order of magnitude as their quiescent

power. Drawing the highest possible power from the source does not necessarily mean that the highest possible power is transported to the harvester output. Therefore the harvested output power is measured and has to be compared to the highest possible output power under perfect setup conditions to find the real tracking efficiency. As a result the tracking efficiency of the MPPTA is obtained. By comparing the input power to the output power, the system efficiency is obtained.

The energy harvesting part of the ISSCC publication from Chen et al. [8] was not described in detail. In their publication for ISSCC it was mentioned, that an integrated solar cell is used to recharge a battery. Due to the fact that a battery is used, an autonomous startup of the harvesting part was not necessary and the whole charge pump is designed for recharging the battery. In contrast to this work, no further design requirements for startup without having a supply available are needed for their sensor platform. They published an efficiency of their charge pump of 75 % achieving a battery recharge output power of 80 nW under direct sunlight with 0.07 mm^2 on-chip solar cell. The higher charge pump efficiency, compared to this work, has most likely been achieved because pump capacitors with less parasitic capacitance have been available in their process. The charge pump parasitics of this work amount to 36 % of the main capacitance still leading to 20-50 % harvesting system efficiency. It is also worth noting, that the efficiency measurement of [8] is not further described by Chen et al. In ultra-low power charge pump operation the efficiencies of the pump alone and the efficiency of the overall system when operating the converter can significantly differ. This is the case, because the power to preserve the operation of the chip and the harvested power can be in the same order of magnitude. Therefore it is important to describe the how the published efficiency data is obtained.

Table 5.1: Related work comparison on miniaturized solar energy harvesting systems

Device	Type	Process	MPPT	Solar Cell	DC/DC		FF	norm. Power	Light Source
				implementation	In [mV]	Out [V]	%	$\mu W/mm^2$	
SSC [4]	Sensor Platform	130 nm	FOC	stacked chips	520	4.1	-	20-30	Sun
BCAS [6]	Sensor Platform	180 nm	No	monolithic	500	0.5*	79	9	Solar emulator
VLSI [7]	Solar Cell	350 nm	No	two chips	550	0.55*	65	225	100 W bulb
ISSCC [8]	Sensor Platform	180 nm	No	stacked chips	450	3.6	-	1.3**	Sun
This Work	Harvester + PMU	130 nm	P&O	monolithic	400	4.2	78	80	Sun

* No DC/DC converter. Direct supply from the solar cell.
** Behind thin transparent tissue.

Energy harvesting ICs for low-power operation available on the market are all designed using step-up converters. The LTC3106 additionally allows a shared use of the inductor for buck and boost operation. Comparing the available solutions clearly points out that the application which is addressed decides which IC is best suited. First of all, the different sizes and therefore the different power levels make a direct comparison to the monolithic approach difficult. In this work the supply for an ultra-low power, monolithic and autonomous sensor platform was developed, while commercial designs need startup power ranges of at least one order of magnitude higher. On the other side, commercial harvesting solutions can handle

Table 5.2: Comparison to market available low-power harvesting ICs

Device	$V_{IN\text{-}MIN}$	$P_{IN\text{-}MIN}$	MPPT	# ext. components	η at $P_{IN\text{-}MIN}$	η_{MAX}
	[mV]	[µ W]	[-]	[-]	[%]	[%]
BQ25505	330	15	FOC	>10	10	93
LTC3106	850	12	const. V_{IN}	10	10	90
LTC3108*	20	60	-	7	35	40
This Work	380	0.65	P&O	1**	20	50

* In configuration with 1:100 ratio transformer.
** Only the energy storage is needed (capacitor or battery).

much higher power levels that the converter presented in this work. However, in terms of efficiencies and application enabling concepts, comparisons can be made. The BQ25505 for example is used by Pinuela et al. [45] because of its very low cold start input power and its MPPT capability. Compared to the cold start power of the LTC3106 the BQ25505 needs 3 µW more power, but it features the FOC MPPT, while the LTC3106 would require additional 9 µA for its MPPTA. The LTC3106 MPPTA holds the input voltage at a preset constant value. As a consequence, the MPP is not really tracked but set for one operation point. Inductor based converters clearly show, that the system efficiencies are higher than for published work on fully integrated solutions. Even if input voltages as low as 20 mV are harvested, the efficiency in combination with an external transformer is still in the range as presented in this work and other recently published integrated harvesting systems as listed in table 5.1. Only if applications demand the absence of any external component, the integrated charge pump topology should be used. Regarding the startup, one possible advantage of the integrated solution could the ultra-low power capability be. In this work the minimum input power is 0.65 µW compared to the data sheet absolute minimum input value of 12 µW achieved by the LTC3106.

The LTC3106 offers only a pseudo MPPT by keeping the input voltage at a pre-defined absolute value which is no real tracking for changing environmental conditions. The BQ25505 uses the FOC method which is well suited for highly efficient boost converters in their typical operation point. Utilizing the proposed approach of this work, which is maximizing the output power flowing into the energy storage, could increase the efficiency for operation points at minimum input power. Compared to commercial MPPTAs the proposed one is continuously operating. It tracks and maximizes the actual output power of the system while requiring several orders of magnitude less current for operation than the MPPTA of the LTC3106 does.

5.2 Research Summary

A concept, a method, an implementation, and a fully functional test chip for a monolithic integrated stand-alone photovoltaic harvester with ultra-low power MPPTA is presented. The test chip has no special treatment for the surface or the doping densities to enhance the photon absorption rate. Hence, the standard 130 nm CMOS single n-well process is used without additional mask costs.

Investigations regarding the design of CMOS on-chip solar cells and their efficiencies have been made. On a first test chip, 9 different solar cells have been taped out to observe the capability of the process to form an efficient solar cell. It was observed, that the best working solar cell structure, the n-well to substrate junction, outperforms the close surface junction of the diffusion. This observation leads to the further concept of the chip. The test chip results have been presented at the 45$^{\text{th}}$ ESSCIRC/ESSDERC in Graz in 2015. Besides the geometry study for the highest efficiency also the influence of the passivation layer was observed. It was shown, that the additional Layer can enhance the photocurrent for shorter wavelengths and does not reduce the cell efficiency. This observation added new value to the recent publications, because the influence of the passivation for CMOS integrated solar harvesters was not discussed at the time of publication. Measurement data, gathered in this work, regarding the solar output power have been cited by Pretl et al. [30]. The monolithic approach of this work was cited by Plesz et al. [46].

Further, a charge pump driver circuit capable to work with the on-chip power source is presented. Using the proposed power management and the charge pump, the well-substrate junction delivering the highest power per area can be used. The harvester chip is a proof of concept design meaning that the solar area is approximately 0.4 mm^2 chosen to proof the functionality of the implementation. A minimum startup illumination of 2.25 kLux for generating output current into a 4.2 V load is required. The charge pump capacitors are implemented with PMOS transistors for sufficient capacity per area while being capable to handle the small negative voltage produced by the solar cell. When using poly-poly or metal-metal capacitors the efficiency of the converter could be considerably increased, because the parasitic capacitors amount to 36 % of the main capacitance. A simple schematic extension to perform partly charge recycling of the parasitic capacitors within the driver circuit is also shown. While previous publications regarding charge recycling use dedicated signals for the recycling, the proposed driver circuit allows a much simpler implementation by utilizing signals that are generated to operate the charge pump itself. The advantage is the reduction of complexity and therefore a reduction of consumed power.

The implemented P&O MPPT algorithm is tested under artificial and under natural light conditions. Tracking efficiencies have been measured under reproducible well defined laboratory light conditions. It was shown that under worst case conditions the tracking error amounts to 1.8 %. The average error of the MPPTA is 0.4 % while requiring approximately 60 nA of supply current. Due to the low power consumption of the implementation, which is the lowest reported to the scientific community so far, Mr. David Newell et al. have cited this work in their publication about low-power energy harvesters in the IEEE Transactions on Power Electronics [39]. Compared to commercially available low power harvesting systems with

MPPT, the proposed design does not require a setup done by the user. Another advantage of the MPPTA of this work is that its implementation inherently considers all loss mechanisms introduced by the charge pump. Especially for fully integrated designs this MPPTA concept is therefore better suited than the state-of-the-art FOC solution. In the theory calculation section it was shown that the FOC method does not necessarily lead to the maximum power point of the system when using an integrated charge pump. Due to the novelty and potential market impact the proposed MPPTA as well as the implementation have been patented by Infineon Technologies [38].

Within this work all in all six test-chips have been taped out, where three differ only in minor bug fixes and slight modifications. Concept, design, simulation, layout, and test for all test-chips have been made by myself. Invited talks were held at the Technical University of Graz in the scope of the lecture "Selected Topics of advanced analog Circuit Design". These talks with the title "Energy Harvesting - Feasibility of Chip Integration" where held four times. Two invited talks were held at Infineon in the context of analog jour fixe meetings, containing the analog implementation in detail. Two conference presentations where held at ESSCIRC/ESSDERC and MWSCAS in Boston. A patent on the MPPTA was granted in November 2017, US9819191B1 [38], including 20 claims regarding the concept as well as the technical implementation on transistor level.

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