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# Optimization of a charge pump in a HV BCD technology, considering parasitic effects

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# Abstract

In this work, a methodology for investigating the effects of parasitic bipolar transistors will be presented. It is shown, how parasitic devices can be localized, how they can be parametrized and how they can be put into the circuit for simulation. Additionally a validation of the approach by doing comparison simulations of the circuit with and without inserted parasitics will be presented. Furthermore an overview of various charge-pump architectures and how a basic charge pump design flow can look like, is presented.

The presented methodology can be directly used in the design process by the analog designer. The designer does not have to rely on theoretic investigations. Instead he can simulate the circuit and directly see the effects of the parasitic elements.

# Acknowledgements

This chapter is dedicated to everybody who contributed to the success of this thesis. This work has been done at Infineon Technologies Austria AG in Villach during my work as a graduating student.

Especially I want to thank the following people:

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# List of variables and constants

| Symbol | Description | Unit |
|---|---|---|
| T | Temperature | K |
| W | Channel width | m |
| L | Channel length | m |
| C | Capacity | F |
| $\epsilon_r$ | Relative permittivity | K |
| A | Area | $m^2$ |
| d | Distance | m |
| V | Voltage | V |
| Q | Charge | As |
| I | Current | A |
| f | Frequency | Hz |
| R | Resistance | $\Omega$ |

## physical constants

| constant | Description | Unit |
|---|---|---|
| q | Unit charge | $1.602 \cdot 10^{-19} As$ |
| k | Boltzmann-constant | $1.38 \cdot 10^{-23} \frac{Ws}{K}$ |
| $\epsilon_0$ | Vacuum permittivity | $8.854 \cdot 10^{-12} F/m$ |

# 1 Theory

## 1.1 Capacitors

A capacitor is an electronic device, that stores electric energy. The energy is stored in form of an electric field between two electrodes. Figure 1.1 shows the basic capacitor construction with its two plates. Equation 1.1 shows,

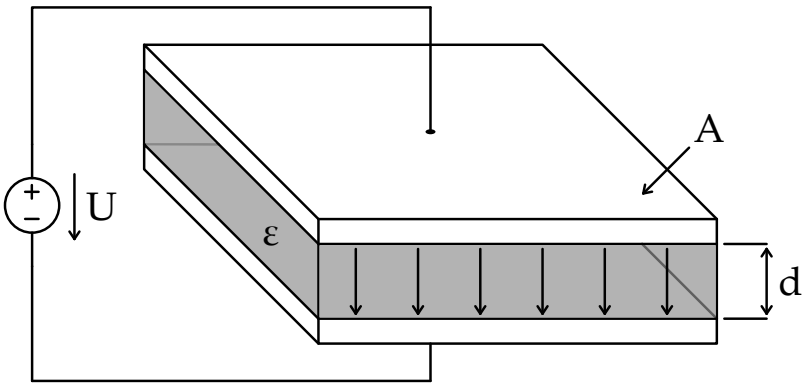


Figure 1.1: Plate capacitor principle.

that the capacitance value is dependent on the dielectric constant $\epsilon$ of the insulator between the two electrodes and the dimensions of the capacitor.

$$C = \frac{\epsilon_0 \cdot \epsilon_R \cdot A}{d} \tag{1.1}$$

## 1.2 Types of Capacitors

By using the different structures and layers a capacitor can also be implemented in CMOS technology.

### 1.2.1 Gate-oxide capacitor

One capacitor structure available in CMOS technologies is implemented with MOSFET Transistors. The two capacitor plates are formed by the gate and conducting channel [9]. The conducting channel is only generated, when a sufficient gate-bulk voltage is applied. Thus the capacitance is highly voltage dependent. Capacitance per area is at about $10fF/\mu m^2$, which is mainly defined by the oxide thickness. So it is considerably higher than other capacitor implementations.

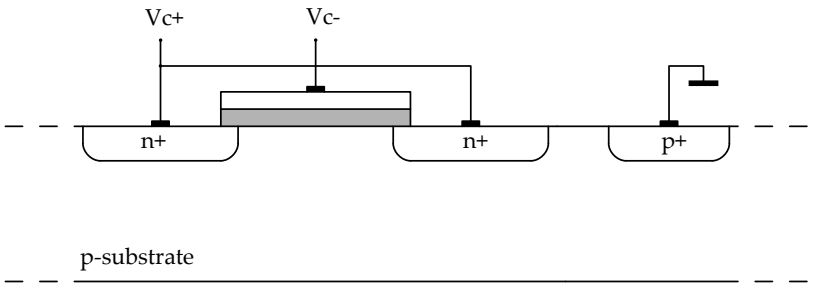


Figure 1.2: MOS capacitor.

### 1.2.2 Sandwich cap, (Metal Insulator Metal)

A common used type of capacitor in CMOS technologies is the sandwiched capacitor. It consists of lateral plates stacked vertically. These plates are made out of the available poly and metal layers. See figure 1.3.

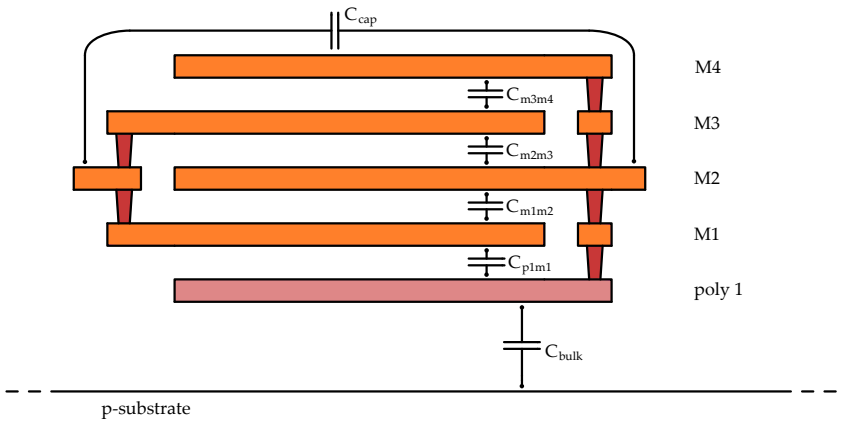


Figure 1.3: sandwich capacitor.

Care must be taken on the bottom plate capacitor. Each capacitor stack is made out of a single metal insulator metal capacitor. To get realistic results in simulation, the bottom plate cap of the poly M1 capacitor must be tied to bulk. The capacitance per area for this type of capacitor is about $0.25 fF/\mu m^2$. the main advantage of this capacitor type is the linearity.

### 1.2.3 VPP capacitor

A VPP capacitor (vertical parallel plate) consists of stripes of metal layers vertically interconnected, forming parallel plates. More than two vertical plates can be connected in parallel to construct a sandwich type of capacitor to increase the capacitance.
Figure 1.4 shows the VPP capacitor with three plates in this case. In common CMOS technologies, the vertical distance between metal layers is usually bigger than the lateral distance. Hence leading to a larger capacitance value per chip area than lateral sandwich capacitors.
By varying the lateral distance between the vertical plates, the voltage rating of the capacitor can be set to the desired needs. Something that cannot be done with lateral plate capacitors.
One disadvantage is, that VPP capacitors have a higher defect density

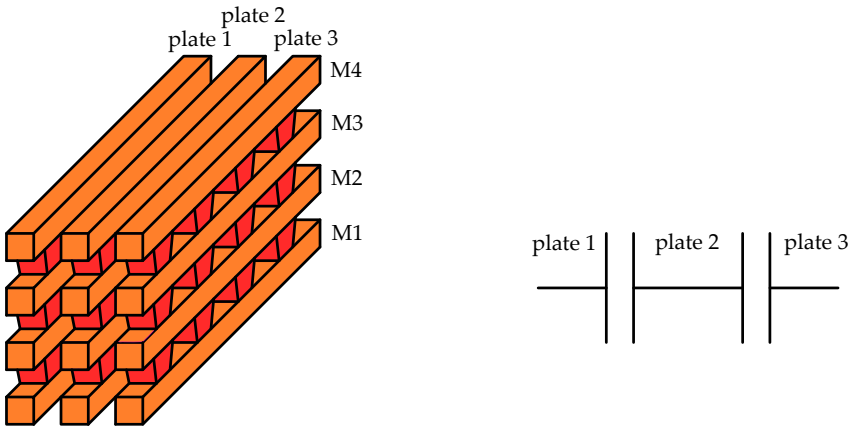


Figure 1.4: VPP capacitor.

compared to other on-chip capacitors. The probability is higher, that particles are trapped between the plates by the polishing process. This degrades the voltage rating and accuracy. According to the technology specification, the capacitance per area is about $1fF/\mu m^2$ at a voltage rating of $10V$.

## 1.3 Choosing the appropriate Capacitor

By comparing the previous listed capacitor implementations it can be summarized:
MOS capacitor: biggest capacity per area. Highly voltage dependent. Due to the high voltage swings in a charge pump, this capacitor is not suited.
VPP-capacitor: high capacity per area. Flexible voltage capability. Linear. High defect density.
Sandwich capacitor: capacity per area about 1/2 of VPP cap. Linear. High reliability.

Due to decent capacity density and very good linearity, a sandwich capacitor is considered the most suitable for the application in a charge pump.

## 1.4 Chargepumps

A charge pump is an electrical circuit, which is used to generate absolute voltage levels higher than the absolute input voltage level. This can also be implemented for negative voltages. Though this thesis is focussing on positive voltage charge pumps. One distinctive characteristic of charge pumps are the lack of magnetic devices. Only capacitors are used as energy storing devices. This is especially advantageous in integrated circuits. On-chip inductances are very area inefficient.

### 1.4.1 Switched capacitor

The working principle of charge pumps rely on switching capacitors. In every clock cycle, a specific amount of charge $\Delta Q$ is transferred into a capacitor C.

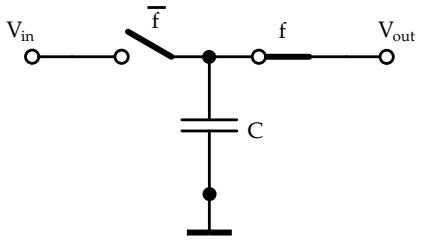


Figure 1.5: Switched capacitor.

$$\Delta Q = Q_{in} - Q_{out} = C \cdot V_{in} - C \cdot V_{out} \tag{1.2}$$

$$I = \frac{C \cdot [V_{in} - V_{out}]}{T} = \frac{V}{T} \Rightarrow R = \frac{1}{C \cdot f} \tag{1.3}$$

Equation 1.3 shows, that the above shown circuit is equivalent to a series resistor.

Various charge pump topologies have been published during the years.

### 1.4.2 First implementations and Dickson charge pump

The first voltage multiplier circuit was published by J. D. Cockcroft and E. T. Walton in 1932. These circuits where implemented with discrete components. The Cockcroft multiplier was very sensitive to stray capacitance. That was not an issue, because the coupling capacitor could be made sufficiently large. In integrated circuits however, on chip capacitors are in low picofarad range and stray capacitances are high. In 1976, J. D. Dickson improved the Cockcroft-Walton multiplier, in a way, that it can achieve high pump efficiency and low output impedance even with high stray capacitances $C_S$ [3]. This circuit, also known as the Dickson charge-pump, is shown in.

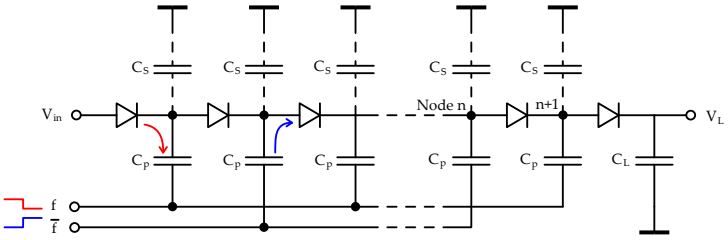


Figure 1.6: Dickson charge pump.

One dickson charge pump stage consists of a switching element (diode e.g.) and a pumping capacitor. See figure 1.6. The capacitors are in a parallel order compared to the serial order in the Cockcroft-Walton multiplier. This reduces the impact of stray Capacitors $C_S$.
Consecutive stages are clocked alternated with a clock and its inverted clock. On the falling edge of the input clock, the pump capacitor is charged with an amount of charge $Q_x$.

### 1.4.3 Bootstrap charge pump

The implementation of a dickson charge pump with MOS switches is fairly simple on the first view. But to turn on the switches, a higher gate voltage is required than what is available. A widely adopted Topology is the Bootstrap charge pump. The required gate voltage is obtained for every stage thanks to a bootstrap circuit, which uses an additional Transistor per stage. The bulk should be connected to the input voltage of the respective stage. During on clock cycle $V_2$ goes low, while $V_1$ goes high. The Bootstrap Capacitor is charged via the bootstrap Transistor. After a small timeslot $V_{B1}$ goes high to $2 \cdot V_{DD}$ and turns on the pass transistor and turns off the bootstrap transistor. Charge is pumped into the next stage [1]. This circuit has the advantage of

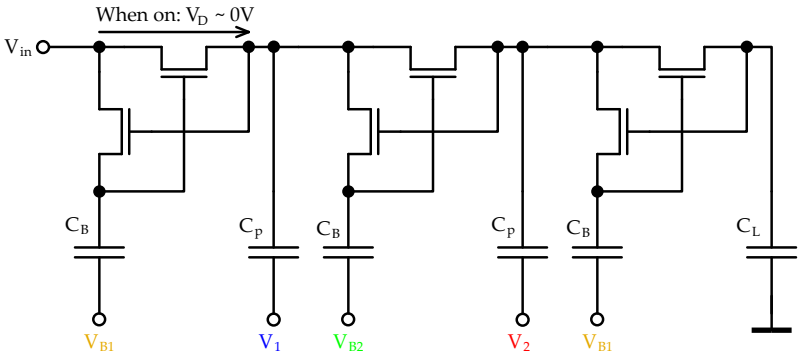


Figure 1.7: Bootstrap charge-pump.

not having a voltage loss due to a diode or threshold voltage. The price for this is a more complex clocking scheme requiring four phases going up to $2 \cdot V_{DD}$ for a single branch charge pump. Furthermore the phases have to be delay, as can be seen in 1.8.

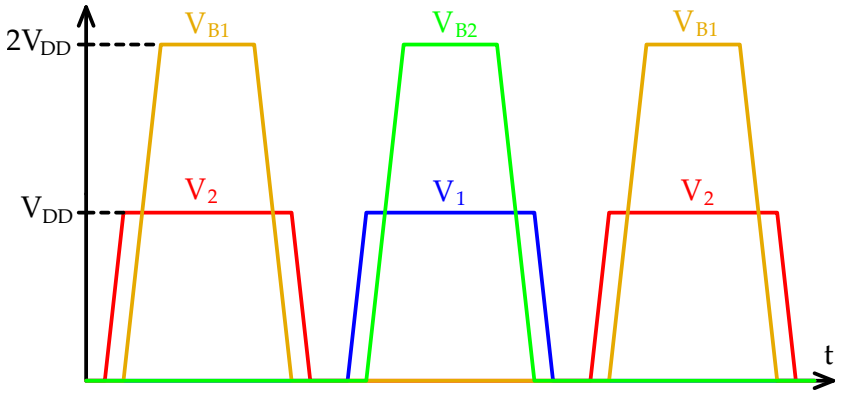


Figure 1.8: Clocking for bootstrap CP.

### 1.4.4 Cross-coupled switches

The cross-coupled charge pump has been introduced in 1998 [4]. One stage consists of four MOS switches and two pump capacitors. Figure 1.9 shows one clock cycle. When $V_{CLK}$ has its rising edge, $TN_1$ and $TP_2$ are switched off. $TP_1$ is switched on, so the charge in Capacitor $C_{P1}$ gets pumped into the output. On the same time the clock at $C_{P2}$ has its falling edge and $C_{P2}$ gets charged via $TN_2$. A cross coupled design does not need a special clocking scheme like the bootstrap charge pump described in 1.4.3. Charge-transfer and control of the switches are accomplished via the same path, resulting in less complexity.

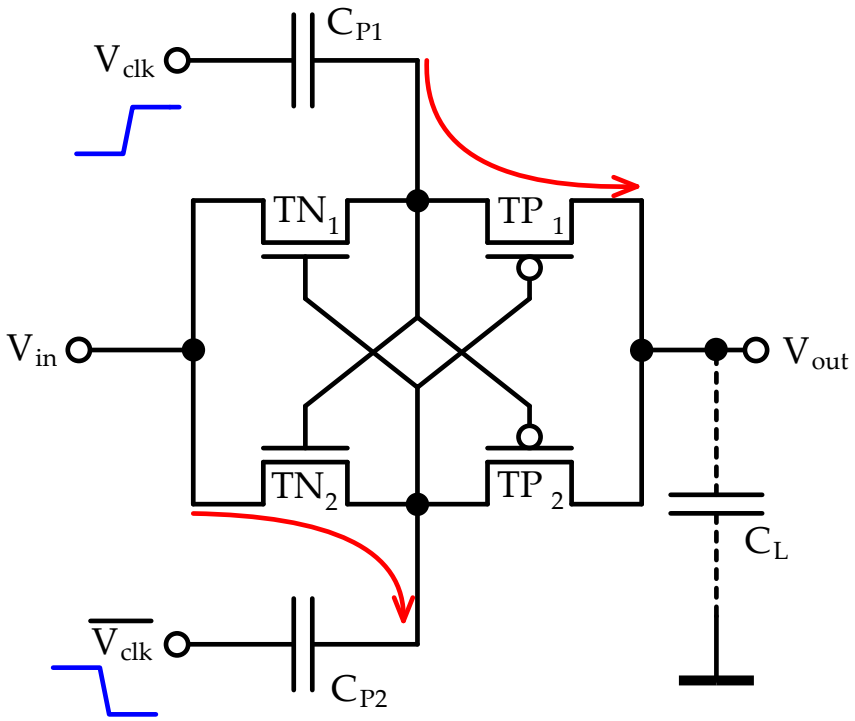


Figure 1.9: Cross-coupled CP.

### 1.4.5 Linear equivalent circuit

Charge pump design methodology is based on the procedure described in [8]. By applying the switched capacitor relation described in 1.4.1, a linear equivalent circuit for a Dickson charge pump can be obtained.
Referring to the schematic in figure 1.6, the open load voltage between each node can be expressed as in 1.4. The stray capacitance reduces the clock voltage amplitude from $V_{clk}$ to $V'_{clk}$:

$$V_{n+1} - V_n = V'_{clk} - V_D \tag{1.4}$$

$$V'_{clk} = \frac{C_P}{C_P + C_S} \cdot V_{clk} \tag{1.5}$$

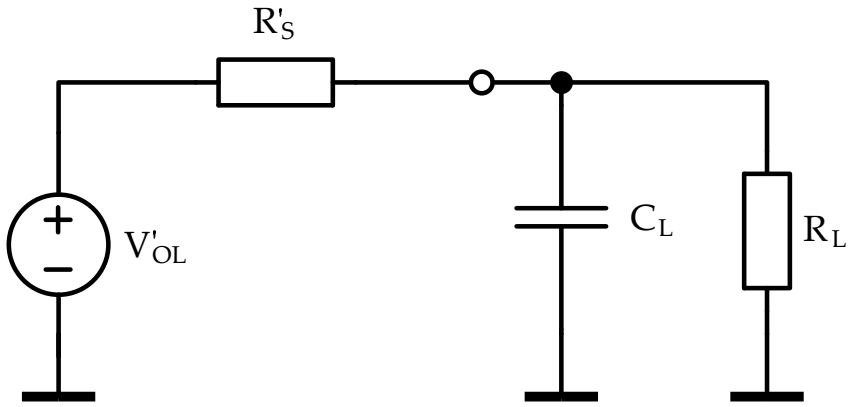


Figure 1.10: Linear equivalent circuit.

$$V_{n+1} - V_n = \left[\frac{C_P}{C_P + C_S}\right] \cdot V_{clk} - V_D \tag{1.6}$$

For N stages in series this is:

$$\begin{aligned} V_N - V_{in} &= N \cdot \left[\frac{C_P}{C_P + C_S} \cdot V_{clk} - V_D\right] \\ \Rightarrow V'_{OL} &= V_{in} - V_D + N \cdot \left[\frac{C_P}{C_P + C_S} \cdot V_{clk} - V_D\right] \end{aligned} \tag{1.7}$$

The short circuit load current for M stages in parallel can be expressed like in 1.8.

$$I'_{SC} = M \cdot \left[\frac{C_P}{C_P + C_S} \cdot V_{clk} - V_D\right] \cdot C_P \cdot f \tag{1.8}$$

$$R'_S = \frac{V'_{OL} - V_{IN}}{I'_{SC}} = \frac{1}{M \cdot C_P \cdot f} \cdot \left[N - \frac{V_D}{V_{clk} \cdot \frac{C_P}{C_P + C_S} - V_D}\right] \tag{1.9}$$

$$\frac{C_P}{C_P + C_S} = \alpha \tag{1.10}$$

By taking equation 1.7 and subtracting the voltage loss when loaded, the output-voltage depending on the output-current $I_{OUT}$ can be calculated.

$$V_{OUT}(I_{OUT}) = V_{in} - V_D + N \cdot \left[\alpha \cdot V_{clk} - V_D\right] - I_{OUT} \cdot \frac{N - \frac{V_D}{V_{CLK} \cdot \alpha - V_D}}{M \cdot C_P \cdot f} \tag{1.11}$$

### 1.4.6 Linear equivalent circuit for Cross coupled CP

One cross coupled CP stage is inherently a pair of two dickson stages in parallel. Thus the factor two in the denominator [4]. Furthermore there is no diode voltage loss due to a diode. Therefore $V_D = 0V$ can be assumed as a simplification. This results in (1.12) for the output voltage.

$$V_{OUT}(I_{OUT}) = V_{in} + N \cdot \left[\alpha \cdot V_{clk}\right] - I_{OUT} \cdot \frac{N - \frac{1}{V_{CLK} \cdot \alpha}}{2 \cdot M \cdot C_P \cdot f} \tag{1.12}$$

### 1.4.7 Clocking

When implementing more than one stage in parallel, there is the possibility to use multiphase clocks. A sample simulation with charge pumps with one and two clock pairs has been set up. Due to the higher resulting switching frequency, the output voltage ripple reduces to about 50%. This means less filtering of the output voltage is required. Furthermore the current spikes on the supply line will also be about half of the previous value, which reduces the requirements on supply architecture and filtering. See figures 1.12 and 1.13 for a sample simulation, which shows this behaviour.

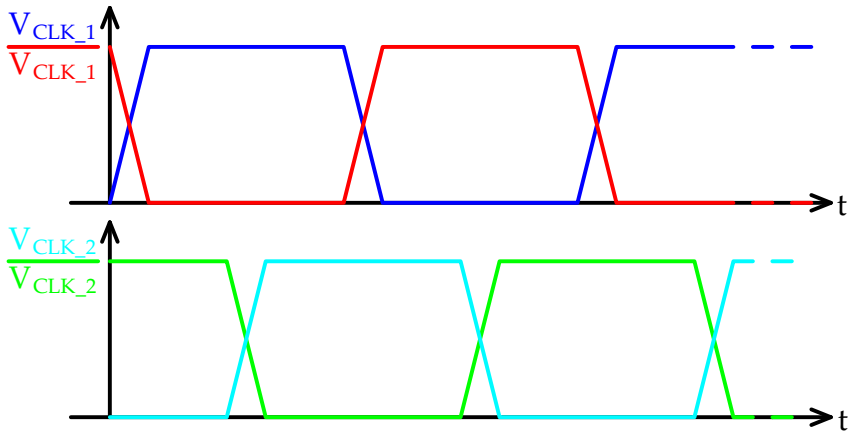


Figure 1.11: Multiphase clocks.

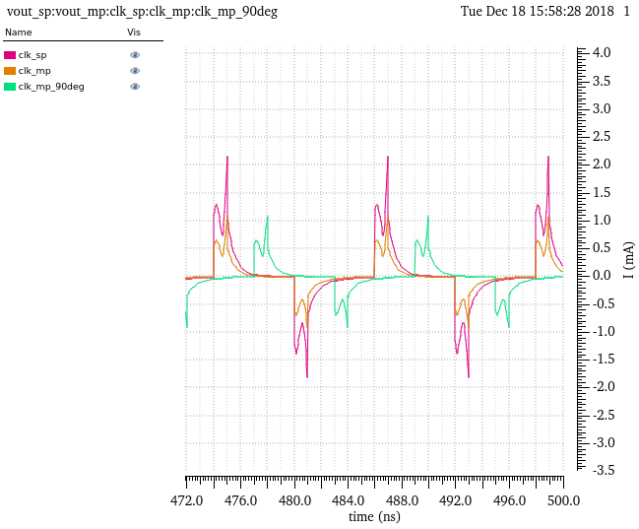


Figure 1.12: Lower voltage ripple.

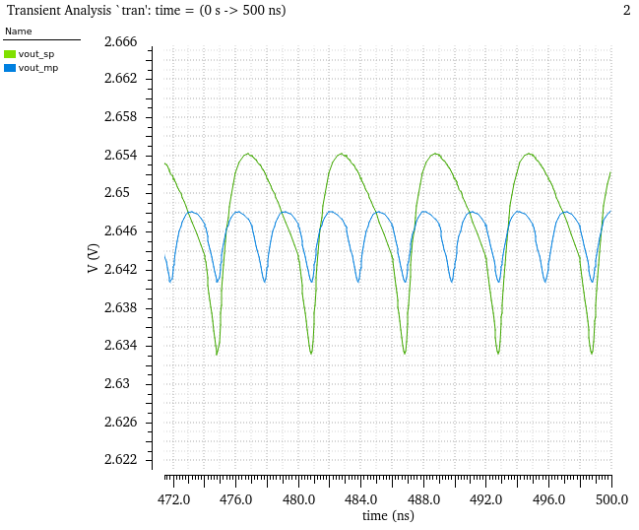


Figure 1.13: Lower Current spikes.

### 1.4.8 Clock-phase relations

The relations between clock phases is critical. All switches should switch at the same time. See figure. Figure 1.14 shows, that if both switches T1 and T2 are on at the same time, due to overlapping clock phases, current may flow from the output capacitor back to the pump capacitor and/or input

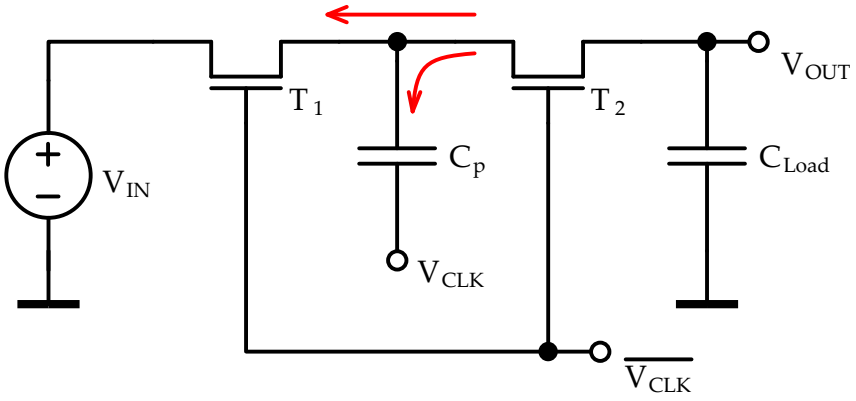


Figure 1.14: Reverse currents occur.

# 2 Design considerations

All design considerations following are based on an already existing charge pump, which has been taped out on a chip while working on this thesis. Figure 2.1 Shows the architecture of the charge pump this work is based on. For simplicity reasons only one clock phase is shown. On power-up the CP runs on a ring-oscillator. After a defined count of clock cycles, the control circuit switches from the ring-oscillator to a clock generator. This is done, because the much more stable and precise clock generator already needs the CP output voltages to start up. The voltage regulator is providing about 1.5V as a supply for the charge pump. This voltage is used to keep the output regulated to about 3.2V. The 4.2V output is unregulated.

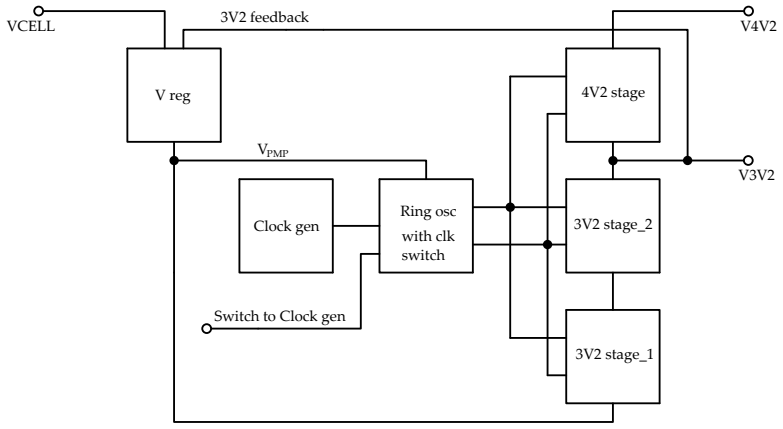


Figure 2.1: CP architecture.

## 2.1 Design specification

Before designing a circuit, design specifications are needed. Specifications are listed in table 2.1. The operating frequency is supplied by an universal clock generator on the chip and is fixed. As the charge pump is regulated there is a regulating Transistor, which needs overdrive voltage to stay in saturation. An overdrive voltage of 200mV has been considered. This results in a minimum operating voltage the CP has to perform as desired of about 1.5V.

| | | |
|---|---|---|
| VCELL | input voltage range | 1.7 to 5.5V |
| V3V2 | output voltage 3V2 | $\leq 3.2V$ |
| V4V2 | output voltage 4V2 | $\leq 4.2V$ |
| I_V3V2 | output current 3V2 | $\leq 300\mu A$ |
| I_V4V2 | output current 4V2 | $\leq 90\mu A$ |
| f_ clk | operating frequency | $84MHz$ |

Table 2.1: CP specifications.

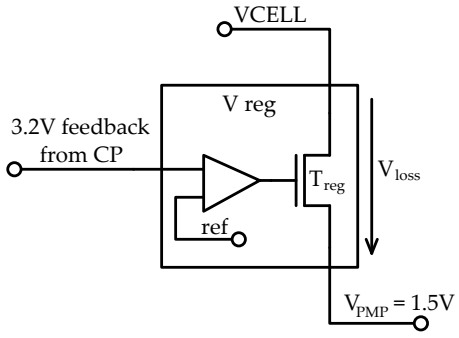


Figure 2.2: Voltage loss due to regulation.

## 2.2 Scaling rule

When rearranging Equation (1.12), a basic scaling rule can be obtained. As can be seen in 2.2.

$$C_P \cdot f \geq \frac{N - \frac{1}{\alpha \cdot V_{CLK}}}{V_{IN} - V_{OUT} + N \cdot \left[\alpha \cdot V_{CLK}\right]} \cdot \frac{I_{OUT}}{2 \cdot M} \tag{2.1}$$

$$C_P \cdot f \geq \frac{N}{V_{IN} - V_{OUT} - V_D + N \cdot \left[\frac{C_P}{C_P + C_S} \cdot V_{CLK} - V_D\right]} \cdot \frac{I_{OUT}}{M} \tag{2.2}$$

As the denominator must be positive, the minimum number of stages in series must be:

$$N > \frac{V_{OUT} - V_{IN}}{V_{CLK}} \tag{2.3}$$

## 2.3 Using the design specification

For the $3.2V$ output at the presented charge pump the number of stages in series computes to $N = 2$ stages.

$$\begin{aligned} N &> \frac{3.2 - 1.5}{1.5} = 1.133 \\ \Rightarrow N &= 2 \end{aligned} \tag{2.4}$$

The number of parallel stages to choose is basically a dependency of several factors. They include number of clock phases which have been chosen and scalability considerations. The designer has decided to use a three phase clocking system. Thus the number of parallel stages must be a multiple of $M = 3$. Because of scalability reasons, $M = 6$ parallel stages have been chosen.

$$
\begin{aligned}
C_P \cdot f &\geq \frac{2 - \frac{1}{\alpha \cdot 1.5}}{1.5 - 3.4 + 2 \cdot \left[\alpha \cdot 1.5\right]} \cdot \frac{468\mu A}{2 \cdot 6} \\
\Rightarrow C_P &\geq \frac{2 - \frac{1}{\alpha \cdot 1.5}}{1.5 - 3.4 + 2 \cdot \left[\alpha \cdot 1.5\right]} \cdot \frac{468\mu A}{2 \cdot 6 \cdot 84 \cdot 10^6} = 1,125pF
\end{aligned}
\tag{2.5}
$$

## 2.4 Scalability / Unitcell approach

To increase the output current, for example in a design change, one can resize the charge pump. This means a new verification of the circuit block. Another possibility is to take the same circuit in parallel. This opens the possibility for using multiphase clocks. Furthermore no redesign is needed.

## 2.5 Sizing switches

The type of switches have to be choosen by two main criterias: Breakdown voltage and transit frequency. As clock voltage can be 1,52V and due to possible overshoots a 1.5V device is not sufficient. 2.5V devices have to be used. The transitfrequency should be higher than the operating frequency. Sizing the switches basically means sizing the switch in terms of W and L to get a sufficiently low $R_{on}$ value. The mechanism of charge transfer in a charge pump is nothing other than charging of a capacitor, as shown in Figure 2.3. A rule of thumb for the time, after the capacitor is considered fully charged is $5 \cdot T$. The period length of the input clock is $T = \frac{1}{84MHz} = 12ns$. Full charge transfer should be accomplished in:

$$
\begin{aligned}
5T &= \frac{T_{clk}}{2} \\
\Rightarrow T &= \frac{T_{clk}}{10} = \frac{12ns}{10} = 1.2ns
\end{aligned}
\tag{2.6}
$$

$$\begin{aligned} T &= R_{on} \cdot C_{pump} \\ \Rightarrow R_{ON} &\leq \frac{T}{C_{pump}} = \frac{1.2ns}{1.125pF} = 1066\Omega \end{aligned} \tag{2.7}$$

With the estimated $R_{on}$ in hand one can calculate the needed W/L ratio. $R_{on}$ is calculated according to (2.8), which gives (2.9) by rearranging. The K' factor has been determined by a simulation run for the used transistor type. By using the minimum transistor length of $L = 400nm$ the needed transistor width computes to:

$$R_{on} = \frac{1}{K' \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH})} \tag{2.8}$$

$$\begin{aligned} \frac{W}{L} &= \frac{1}{K' \cdot R_{on}[V_{GS} - V_{TH}]} \\ \Rightarrow \frac{W}{L} &= \frac{1}{200\mu \cdot 1066 \cdot [1.5 - 0.5]} = 4.7 \\ \Rightarrow choose \frac{W}{L} &= 5 \end{aligned} \tag{2.9}$$

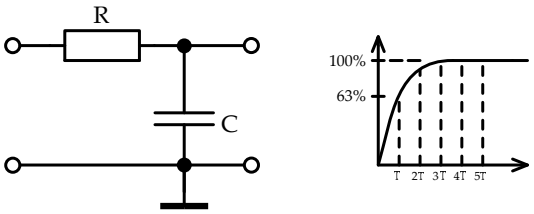


Figure 2.3: Charging of a capacitor.

$$\begin{aligned} \frac{W}{L} &= 5 \\ \Rightarrow W &= L \cdot 5 = L \cdot 400nm = 2\mu m \end{aligned} \tag{2.10}$$

The same method applied to the PMOS transistor, with a value $K = 60\mu$ computes a W/L of $\frac{W}{L} = 15.6$. A ratio of $\frac{W}{L} = 16$ has been chosen, resulting in a width W of $W = 6.4\mu$ and $L = 400n$.
The described sizing is a first-order approximation as the switch has a saturated state besides the linear (ohmic) region.

## 2.6 Additional requirements for switch sizing

The transistors in a cross coupled charge pump basically form a latch. P and NMOS have to switch possibly at the same time. Figure 2.4 illustrates this behaviour. The crossing should be at half the supply voltage. This can be achieved by sizing the PMOS Transistor about 2 to 3 times larger than the NMOS, due to the lower mobility in p-doped semiconductors. The hand calculation show, that this is requirement is met.
Another factor is robustness of the latch. This means how easy it is to flip

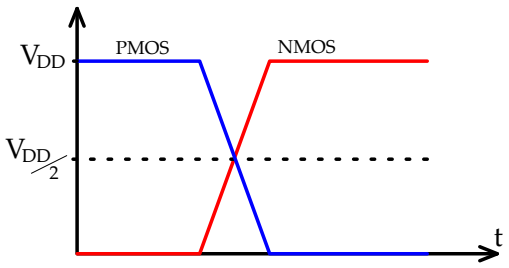


Figure 2.4: PMOS and NMOS switching at the same time.

the latch into the other state. It is basically a matter of switch size, hence gate capacitances. The bigger the switch is, the more robust is the latch. However, a trade off has to found, because more gate capacitances means more energy is needed to flip the latch, hence efficiency is decreased.

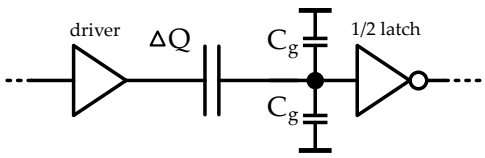


Figure 2.5: Charge $\Delta Q$ used to flip latch.

## 2.7 Clock driver sizing

Figure 2.6 shows a basic three stage driver circuit. The chain is made of inverters with exponentially increasing size to reduce EMI on the supply line [2]. The clock driver is fed by an oscillator and drives the charge pump stages. In case of requirements the driver must drive the output current in addition to the charging and discharging of the parasitic bulk capacitor shown in 1.3. The latch must be flipped sufficiently fast as well.
An analytical dimensioning of these components is basically complicated and not practical. As a rough estimation the same PMOS and NMOS dimension from the CP has been used as a basis. Each parallel string has its own driver. This means each driver has to drive two stages and the third stage, which can be counted to about $1/4$ of a main stage. Plus there is the bulk capacitance, which adds about 25% as well. With an assumed margin of 25% this would give the values computed in.

$$\begin{aligned} \frac{W}{L} &= 1.25 \cdot 1.25 \cdot 1.25 \cdot 2.25 \cdot 5 = 22 \\ \Rightarrow W &= L \cdot 5 = L \cdot 400nm = 8.8\mu m \end{aligned} \tag{2.11}$$

$$\begin{aligned} \frac{W}{L} &= 1.25 \cdot 1.25 \cdot 1.25 \cdot 2.25 \cdot 16 = 70 \\ \Rightarrow W &= L \cdot 5 = L \cdot 400nm = 28\mu m \end{aligned} \tag{2.12}$$

This applies to the last stage in the chain. In order to accommodate the exponential increase of size, the first two stages are scaled down accordingly. This scheme has been adapted a bit for fitting with the parameter optimization. See following chapters for details.

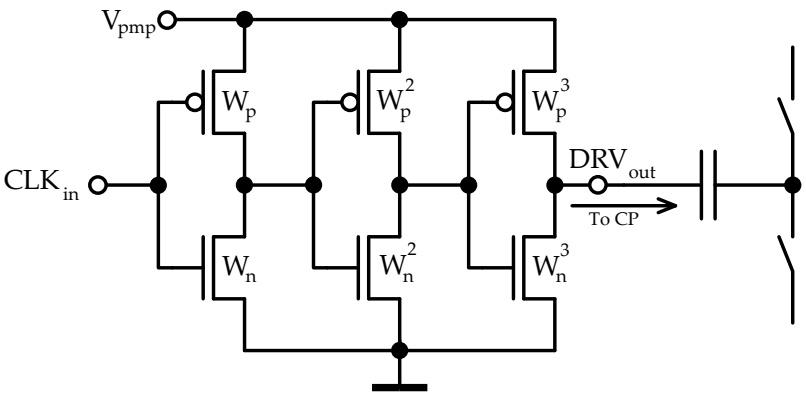


Figure 2.6: Driver.

## 2.8 Parameter optimization

To further optimize the CP design parameters and to squeeze out a possibly high performance, a optimization method is needed. Two kinds of methods can be differentiated. Algorithm which need derivatives and derivative free algorithms.
The mathematical function to be optimized is called the cost-function. If the cost-function is available in an analytical form, the derivative can be calculated. However, in case of the charge-pump optimization the cost-function is not accessible, because function values are generated by a simulation. Thus derivatives cannot be calculated. Thus a derivative free algorithm has to be chosen. The input parameters of the cost function are varied with each iteration. A score value is calculated with the output values, which is minimized with each iteration.

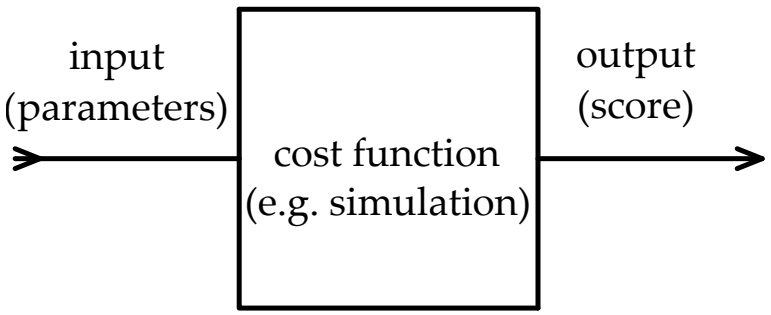


Figure 2.7: Optimization process.

### 2.8.1 Nelder-Mead-Simplex

One such algorithm has been published by J. A. Nelder and R. Mead in 1965 [7]. This iterative algorithm starts with $n+1$ starting points which form a simplex. A simplex is a structure in n-dimensional space generated by $n+1$ points that are not in the same plane. After each iteration the simplex is modified by using for simple operations. The decision, which operation is to be used is based on the values of the $n+1$ points calculated.
At first the algorithm starts by evaluating the $n+1$ starting points and sorting them from $x_b$ (best) to $x_g$ (good) to $x_w$ (worst). Then all but worst value are averaged in $x_a$.

$$x_a = \frac{1}{n} \sum_{i=1, i \neq w}^{n+1} x_i \tag{2.13}$$

It is obvious, that the line from $x_w$ to $x_a$ has a descent direction. A new point is found by reflection, given by

$$x_r = x_a + \alpha(x_a - x_w) \tag{2.14}$$

If the point found by reflection is better than the best point $x_b$, a step further can be taken with expansion,

$$x_e = x_r + \gamma(x_r - x_a) \tag{2.15}$$

However, if the reflected point is worse than the worst point, it can be assumed, that a better point exists between $x_w$ and $x_a$ and a inside contraction can be performed

$$x_c = x_a - \beta(x_a - x_w) \tag{2.16}$$

If the reflected point is not worse than the worst but still worse than the other good points, then an outside contraction can be performed

$$x_o = x_a + \beta(x_a - x_w) \tag{2.17}$$

If the new point is better than the best point, this point is accepted, otherwise the previous reflected point will be taken. If these operations all fail, the shrinking operation will be performed, where for all points but the best point a new point will be computed

$$x_i = x_b + \rho(x_i - x_b) \tag{2.18}$$

The advantage of this algorithm is its simple implementation and robust-

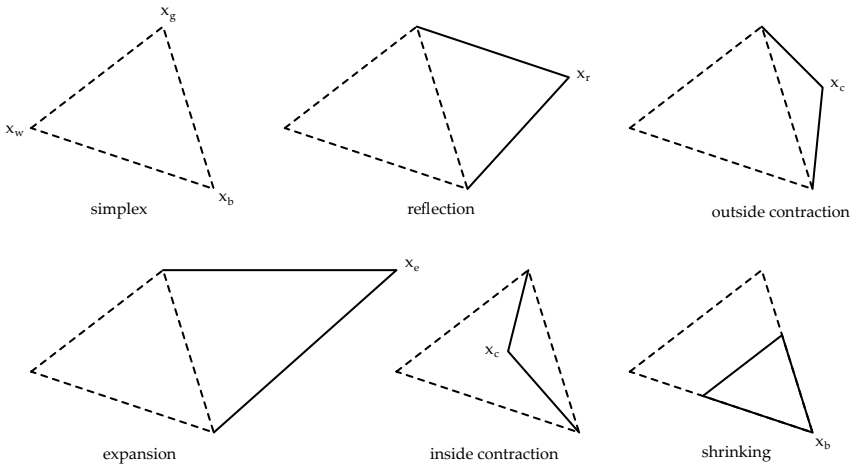


Figure 2.8: Nelder-Mead operations.

ness. However, depending on the starting points it may only find a local optimum of the cost function.

### 2.8.2 Pattern search

This optimization method was first introduced by Hooke and Jeeves [6]. The algorithm starts with an initial set of parameters $x^{(0)} \leftarrow (x_1^{(0)}, x_2^{(0)}, ..., x_n^{(0)})$ which give a function value $f_{best} \leftarrow f(x^{(0)})$. Each parameter is then varied up by a value $\delta x$. If the new function value is better than $f_{best}$ the variation will be retained and algorithm goes on with the next parameter. If the function value stays the same or gets worse for the upwards variation, the parameter will then be varied downwards by $\delta x$. The algorithm is finished, when no improvement is shown any more.

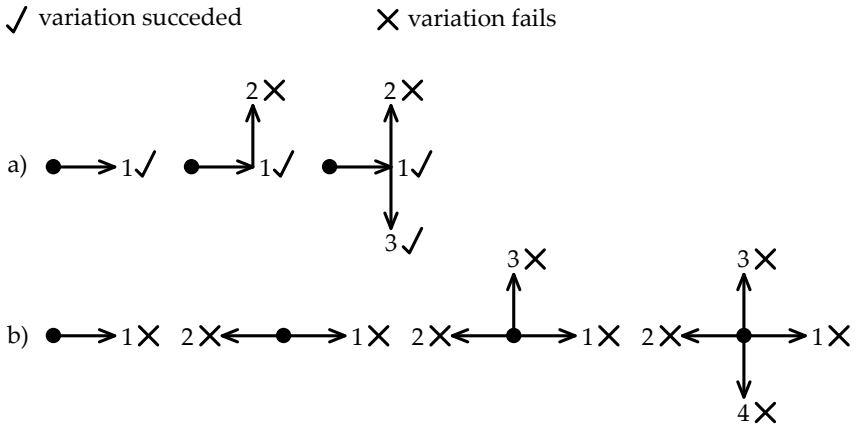


Figure 2.9: Pattern search iterations.

### 2.8.3 Applying an algorithm to the CP problem

Evaluating the cost function is expensive. In other words the simulation may take a long time to finish. Thus it is advisory to choose a fast algorithm. Numeric tests have shown [11] that the Nelder-Mead Simplex can give a good reduction in function value using a relatively small number of function evaluations. Furthermore the algorithm is easy to understand and implement.
Thus it has been decided to use the Nelder-mead algorithm for the CP

optimization problem. A program, which has already existed has been used to execute the simulation runs and do the operations of the Nelder-Mead algorithm.
As mentioned earlier, the algorithm works on a n-dimensional space, thus n parameters need to be specified. For the charge pump itself two parameters have been choosen. Width of PMOS and width of NMOS transistors. Three additional parameters have been specified for the driver circuit, which modify the width of the PMOS and NMOS transistors as well. See figure 2.10. Parameters scale, skew and ratio have been introduced. Parameter scale is the responsible parameter for exponentially increasing driver size, ratio is a multiplication factor for PMOS and division factor for NMOS. It addresses the difference in PMOS and NMOS size. Parameter skew alternatingly multiplies and divides width value for the transistors. This all is done to balance driver strength between NMOS and PMOS in order to skew the rising and falling clock edge. The algorithm uses a score value to do the

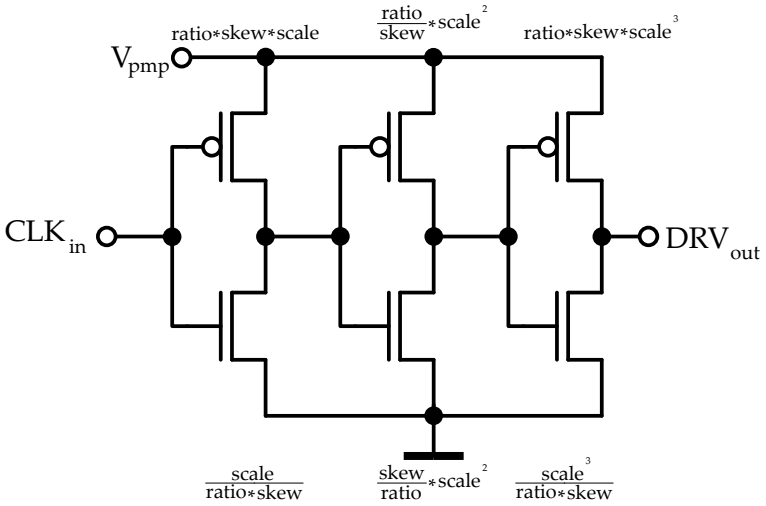


Figure 2.10: Parametrized clock driver.

optimization. In the case of the CP two parameters can be maximized, output current $i_{out}$ and efficiency $i_{out}/i_{in}$. The score is calculated as $score = neffic^2 \cdot i_{out}$, taking the square of $neffic$ to take more emphasis on the efficiency

parameter. Figure 2.11 shows an abstract of the optimizer log. Optimization is finished after 78 runs, because the improvement has been stabilized. Simulated score value has been improved from 3.4 at the beginning to 3.6 after optimization.

```
                                                                                W_P   ; W_N  ;scale; ratio  ; skew
Best so far (1):score =  3.402395 ; i_out = 312.32uA ; n_effic = 10.44% ; 6.656 ; 2.08 ; 2.7 ; 1.4768 ; 1.04
Best so far (2):score =  3.402395 ; i_out = 312.32uA ; n_effic = 10.44% ; 6.656 ; 2.08 ; 2.7 ; 1.4768 ; 1.04
Best so far (3):score =  3.402395 ; i_out = 312.32uA ; n_effic = 10.44% ; 6.656 ; 2.08 ; 2.7 ; 1.4768 ; 1.04
Best so far (4):score =  3.478013 ; i_out = 311.60uA ; n_effic = 10.56% ; 5.7897 ; 2.32928 ; 2.6472 ; 1.36752 ; 1.02064
.
.
.
Best so far (24):score =  3.569467 ; i_out = 308.95uA ; n_effic = 10.75% ; 6.08163 ; 2.86633 ; 2.48481 ; 1.22637 ; 1.07717
Best so far (25):score =  3.569467 ; i_out = 308.95uA ; n_effic = 10.75% ; 6.08163 ; 2.86633 ; 2.48481 ; 1.22637 ; 1.07717
Best so far (26):score =  3.583183 ; i_out = 313.09uA ; n_effic = 10.70% ; 6.47159 ; 3.11914 ; 2.54695 ; 1.28467 ; 1.06356
Best so far (27):score =  3.585366 ; i_out = 309.97uA ; n_effic = 10.75% ; 6.68928 ; 3.00697 ; 2.48944 ; 1.19892 ; 1.05753
.
.
.
Best so far (50):score =  3.611980 ; i_out = 309.70uA ; n_effic = 10.80% ; 7.55908 ; 3.59289 ; 2.41053 ; 1.2238 ; 1.07126
Best so far (51):score =  3.613027 ; i_out = 309.89uA ; n_effic = 10.80% ; 7.53896 ; 3.77376 ; 2.41242 ; 1.21057 ; 1.07398
Best so far (52):score =  3.613027 ; i_out = 309.89uA ; n_effic = 10.80% ; 7.53896 ; 3.77376 ; 2.41242 ; 1.21057 ; 1.07398
Best so far (53):score =  3.613027 ; i_out = 309.89uA ; n_effic = 10.80% ; 7.53896 ; 3.77376 ; 2.41242 ; 1.21057 ; 1.07398
.
.
.
Best so far (75):score =  3.613711 ; i_out = 310.34uA ; n_effic = 10.79% ; 7.69167 ; 3.84265 ; 2.41514 ; 1.22451 ; 1.06733
Best so far (76):score =  3.613716 ; i_out = 310.22uA ; n_effic = 10.79% ; 7.69438 ; 3.84384 ; 2.4129 ; 1.22293 ; 1.06733
Best so far (77):score =  3.613716 ; i_out = 310.22uA ; n_effic = 10.79% ; 7.69438 ; 3.84384 ; 2.4129 ; 1.22293 ; 1.06733
Best so far (78):score =  3.613724 ; i_out = 310.20uA ; n_effic = 10.79% ; 7.69131 ; 3.83563 ; 2.41279 ; 1.22273 ; 1.06745
```

Figure 2.11: Optimization run.

# 3 Assessing the parasitics

Due to the different layers of the CMOS technology, not only the actual MOS devices are present, also other (unwanted) devices are formed. One problem is, that these bipolar parasitic devices are not covered in the model files. The following chapter will take a look at the parasitic bipolar devices, which one are not modelled and how they can be added into the simulation.

## 3.1 Bipolar parasitics

Figure 3.1 shows the bipolar transistors present in the charge pump structure. The arrows of the BJT symbols have been left out, because depending on the biasing condition they can operate in reverse and forward mode. By inspecting the biasing conditions of these parasitic transistors it can be seen, that several bipolar parasitics are strongly reverse biased. See table 3.1 for details. According to the biasing voltages, vertical drain and source bipolar transistors need further inspection. These transistors may be critical in operation and might get conducting in certain conditions.

| parasitic | type | $V_{BE}$ | $V_{BC}$ | critical |
|---|---|---|---|---|
| $T_{pw\_pw}$ | PNP | $0V$ | $0V$ | no |
| $T_{v\_HN\_epi}$ | NPN | $-1.7V$ | $-1.5V$ | no |
| $T_{v\_pw\_lp}$ | PNP | $0V$ | $1.5V$ | no |
| $T_{v\_D\_npn}$ | NPN | $0V$ | $0V$ | yes |
| $T_{v\_S\_npn}$ | NPN | $0V$ | $0V$ | yes |
| $T_{lat\_HN\_nw}$ | NPN | $-1.5V$ | $-3.4V$ | no |
| $T_{lat\_nw\_nw}$ | NPN | $-3.4V$ | $-3.4V$ | no |
| $T_{v\_lp\_sub}$ | PNP | $1.7V$ | $1.7V$ | no |
| $T_{v\_nw\_epi}$ | NPN | $-1.7V$ | $-3.4V$ | no |
| $T_{v\_D\_pnp}$ | PNP | $0V$ | $3.4V$ | yes |
| $T_{v\_S\_pnp}$ | PNP | $0V$ | $3.4V$ | yes |

Table 3.1: Parasitic BJT biasing conditions.

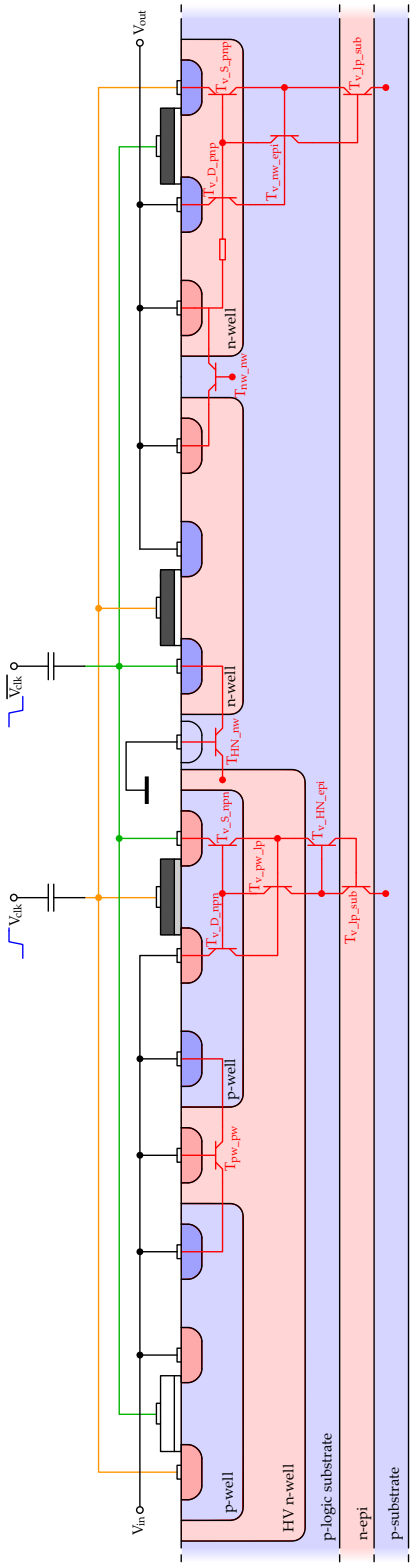


Figure 3.1: Cross section of CP.

## 3.2 Basic mechanism

Bipolar transistors are brought into conductive state, by applying forward biasing the base emitter voltage with about 0.6 to 0.7V. This can happen, when these voltages are directly applied to the corresponding pins, or when dynamic voltage drops occur. See figure 3.2. When a voltage spike hits the bulk connection, the junction capacitor between p and n-well gets charged by a current I, which results in a voltage drop at the well resistance. Depending on the well resistance this may trigger the bipolar transistor.

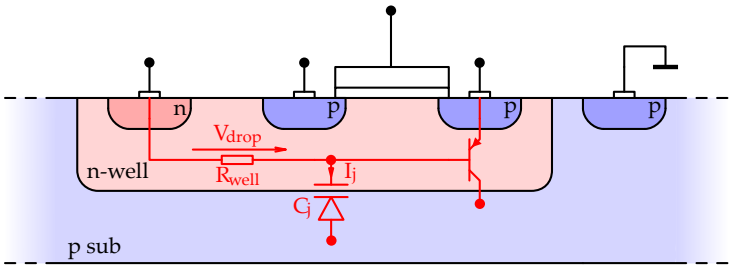


Figure 3.2: Basic mechanism of BJT getting conducting.

## 3.3 Adding BJT devices into circuit

The model files for the specific MOS devices used for simulation are lacking the parasitic devices. In order to do a simulation of the CP with the parasitic transistors, they need to be added into the circuit. For maximum reproducibility and portability it has been decided to use the analog lib NPN and PNP transistors. Section 4.1 shows the backannotated components in the circuit.

### 3.3.1 Gummel poon model

Adding just the symbols to the schematic is not enough. A proper simulation model needs to be applied and parameterized. The cadence built-in model bjt is a basic gummel poon model. Main levers of the model are transport saturation current $I_{SS}$ and forward gain $B_F$. A detailed description about the gummel-poon model and parameter extraction can be found in [10].

### 3.3.2 Hand calculation of parameters

Transport saturation current $I_{SS}$ and gain $B_F$ are basically determined by Doping concentrations and transistor dimensions. Following equations are described in [5] show the basic equations for calculating these parameters for a PNP transistor.

$$B_F = \frac{D_{pB}}{D_{nE}} \cdot \frac{N'_{AE}}{N'_{DB}} \cdot \frac{w'_E}{x_B} = 452 \tag{3.1}$$

$$I_{SS} = \frac{q \cdot A_E \cdot D_{pB} \cdot n_{iB}^2}{x_B \cdot n_B} = 6.88 \cdot 10^{-21} A \tag{3.2}$$

$$D_{pB} = \frac{k_b \cdot T \cdot \mu_p}{q} \tag{3.3}$$

$$D_{nE} = \frac{k_b \cdot T \cdot \mu_n}{q} \tag{3.4}$$

$$\mu_p = \mu_{min} + \frac{\mu_{max} - \mu_{min}}{1 + (\frac{n_B}{N_{ref}})^{\alpha}} \tag{3.5}$$

$$\mu_n = \mu_{min} + \frac{\mu_{max} - \mu_{min}}{1 + (\frac{p_E}{N_{ref}})^{\alpha}} \tag{3.6}$$

$D_{pB}$ and $D_{nE}$ are the Diffusion constants of acceptors in the base region and donators in the emitter region respectively. $\mu_p$ and $\mu_n$ are the electron and hole mobilities. For calculating these values, one needs fitting parameters, which are listed in table 3.2 [12]. Expected values for $I_{SS}$ and $B_F$ are in the range of $I_{SS} = 1 \cdot 10^{-15}$ to $1 \cdot 10^{-20}$ and $B_F < 1$. As can be seen in 3.2 and

| | Phosphorus | Boron |
|---|---|---|
| $\mu_{min}$ | 68.5 | 44.9 |
| $\mu_{min}$ | 1414 | 470.5 |
| $N_{ref}$ | $9.2 \cdot 10^{16} 1/cm^3$ | $2.23 \cdot 10^{17} 1/cm^3$ |
| $\alpha$ | 0.711 | 0.719 |

Table 3.2: Fitting parameters for mobility calculation.

3.1, the results are way off of plausible values. The reason for this might be the simplifications made on this. While layout dimensions can be measured from the layout data quite accurately, reading off doping concentration from the diagram is not that easy. So there is a unknown uncertainty in this calculation.

### 3.3.3 Determining doping concentrations from doping profile

Figure 3.3 shows a doping profile simulation of the used technology node. The doping concentration of the corresponding dopant has been obtained by taking the maximum value of the profile. Furthermore the thickness of each layer can be read out looking at the intersection with the next layer.

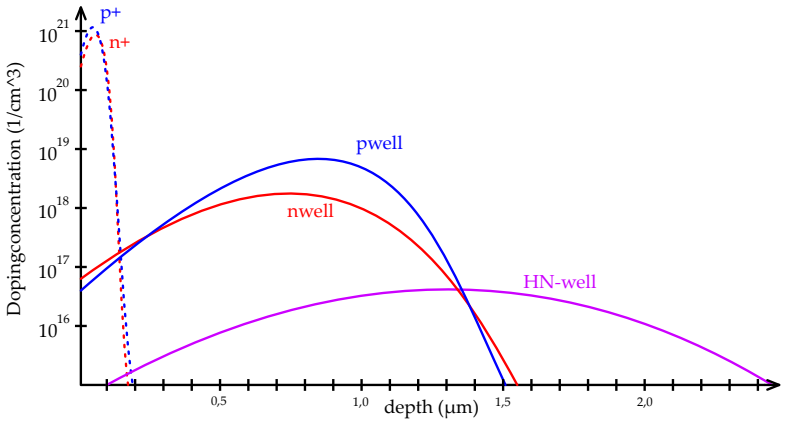


Figure 3.3: Doping profile (example).

### 3.3.4 TCAD

TCAD (Technology-CAD) is a collection of computer aided design tools, for modelling semiconductor processes. Modelling the fabrication process in particular is called a process TCAD. By simulating every process step like it would be done in reality, a semiconductor device can be built in a simulation. This sort of methodology can be used to generate SPICE models as well. This method was considered, but the effort was evaluated as to high for being used in a design flow.

### 3.3.5 Measurement of test wafer

Due to the reason, that the two methods described earlier where not giving the required accuracy for the application, a test wafer has been used to better characterize the parasitics. The test wafer contains test structures. Those where not the same as the transistors in the charge pump. However, the technology is the same. Equations 3.1 and 3.2 show, that by using the same technology, the respective parameters cancel out. For $I_{SS}$ only emitter area is left. So by measuring $I_{SS}$ of the test structures, one can scale this

value with the factor of the emitter areas. Current gain $B_F$ is approximately only dependent on technology parameters and not on layout.

### Measurement setup

For determining $I_{SS}$ and gain $B_F$ with the gummel plot, the knowledge of Base-Emitter voltage and Collector current is needed. Figures 3.4 and 3.5 show the used measurement setup for parasitic NPN and PNP transistors. To accurately measure Base and Emitter voltage, seperate probe needles have been used. This eliminates influences on the measurement results due to voltage loss at the probe needle for the current path (”Force-Sense”). See table 3.3 for details on the measurement devices.

| Device | Type | purpose |
|---|---|---|
| SM1 | Keithley K2400 | $V_B$ voltage source |
| SM2 | Keithley K2430 | $V_C / V_E$ voltage source |
| VM1 | Keithley K2000 | $V_E$ measurement |
| VM2 | Keithley K2000 | $V_B$ measurement |

Table 3.3: Overview of used devices.

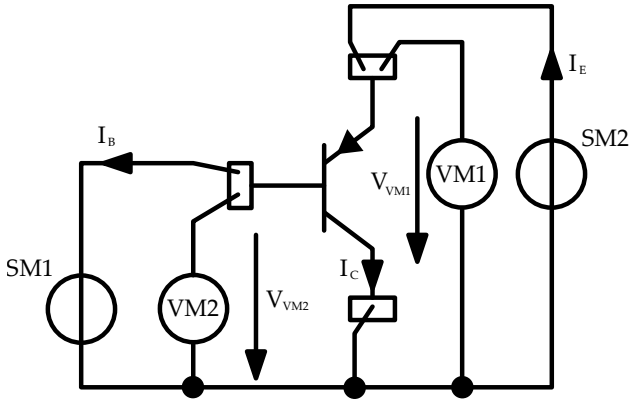


Figure 3.4: Measurement setup for parasitic PNP.

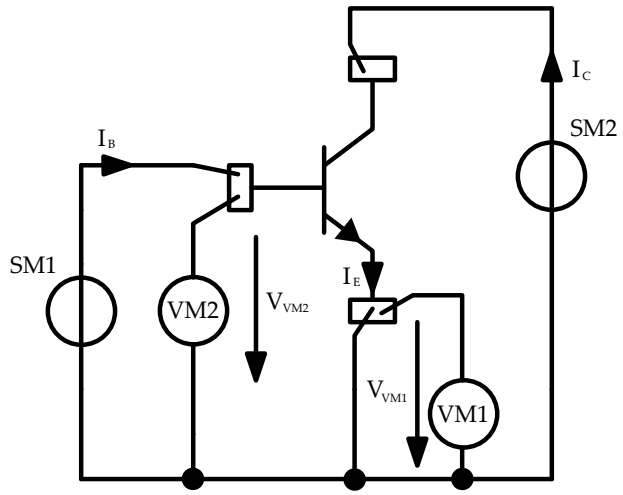


Figure 3.5: Measurement setup for parasitic NPN.

### Results - Vertical drain-source PNP

Base and collector current depending on base-emitter voltage have been plotted in a diagram. See figure 3.6. With a logarithmic scale, the characteristic gummel plot can clearly be observed. Ten pieces have been measured. Each of them showing almost the same results, saying that variation is very low. Measurement results are in the expected range.

| | |
|---|---|
| $I_{SS}$ | $8.17 \cdot 10^{-16} A$ |
| $B_F$ | 1.2 |

Table 3.4: Measurement results.

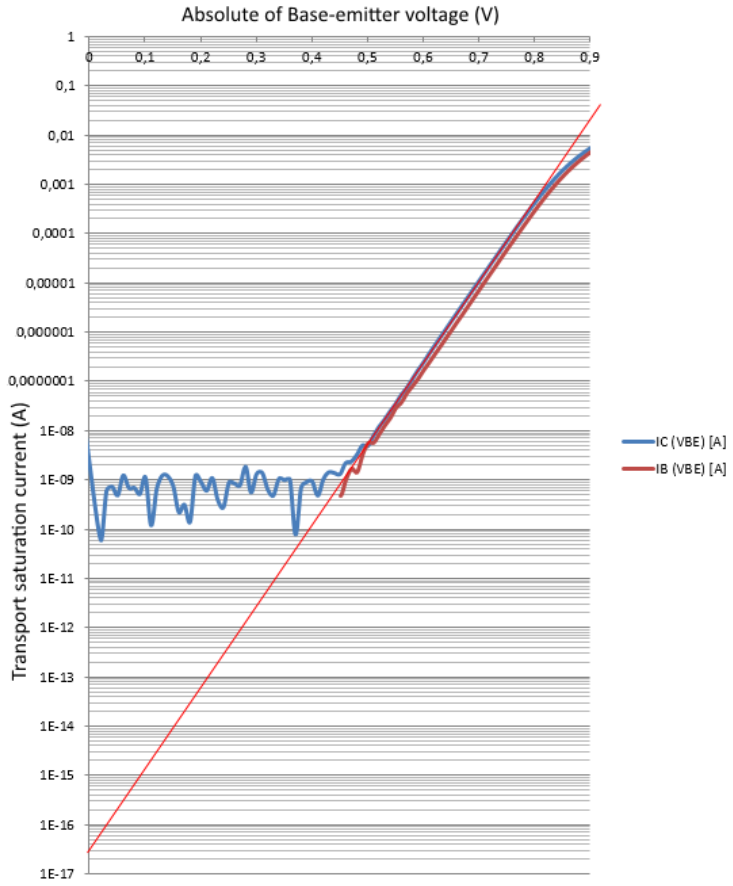


Figure 3.6: Gummel plot vertical drain-source PNP.

### 3.3.6 Parametrizing model

With the measured $I_{SS}$ and $B_F$ in hand one can use the emitter areas of the test structure and the respective transistor in the CP to scale these values to the actual value.

$$I_{SS} = I_{SSmeas} \cdot \frac{A_E}{A_{Emeas}} = 8.17 \cdot 10^{-16} \cdot \frac{8.45 \cdot 10^{-9} cm^2}{152 \cdot 10^{-9} cm^2} = 4.54 \cdot 10^{-18} A \quad (3.7)$$

```
////////////////////////////////////////////////////////
inline subckt pana_vd1_pnp (E B C S)
parameters
+ tnominal   = 22.0
+ trise      = 0.000e+00
+ mult       = 1

model pana_vd1_pnp_bip bjt
+  type     = pnp
+  is       = 4.54e-18
+  bf       = 1.2

pana_vd1_pnp (E B C S) pana_vd1_pnp_bip    area=1 m=mult

ends pana_vd1_pnp
////////////////////////////////////////////////////////
```

Figure 3.7: Parametrization of vertical drain PNP .

## 3.4 Capacitive parasitics

A PN-junction, in this case a p and a n-well, has a capacitive behaviour. The n-type and p-type doped semiconductors act like connecting leads to a capacitor, while the depletion region at the junction acts like a dielectric medium. See figure 3.9 as an illustration. The depletion region width corresponds to the distance of two capacitor plates. The width of the depletion region is dependent on the applied bias voltage and doping concentration. See Figure 3.8 for a sample simulation, which illustrates the junction capacitance in dependence of the junction area. With small junction areas there is still some non-linearity, due to the side walls of the well. If the doping concentration is higher, there will be more majority carriers carriers, which reduces the depletion region, hence larger capacitance. With a higher reverse bias voltage applied, majority carriers are getting pulled out of the depletion region, which increases it, hence the junction capacitance gets reduced. The specific capacitance value is basically a function of doping concentration, junction area and bias voltage. It can be calculated with equation 3.9. As the approximation does not hold for high doping concentrations like they are present in p+ and n+ regions, the capacitances have to be determined differently.
By using a DC simulation of generically sized PMOS and NMOS, the

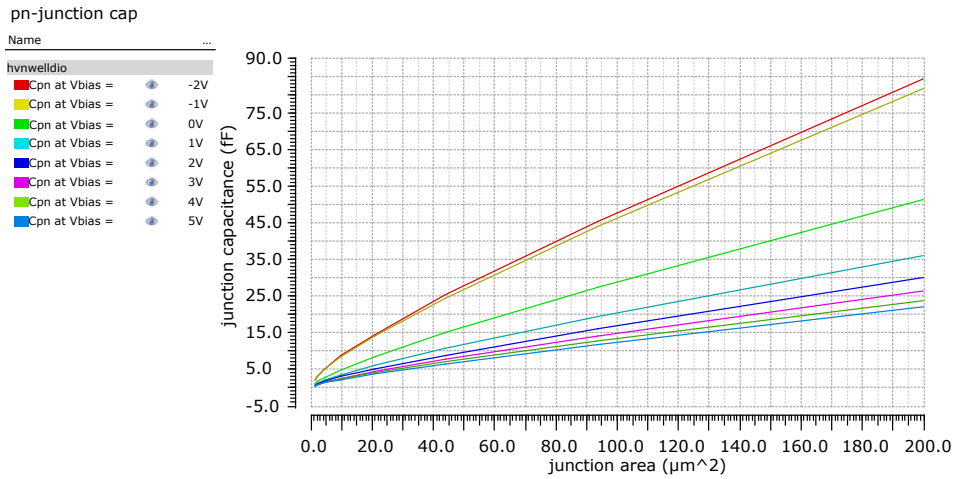


Figure 3.8: Capacitance over area and bias voltage of a pn-junction.

junction capacitances can be extracted. Table shows the extracted for a capacitances for PMOS and NMOS with a width of W=1um. The value can be scaled to a transistor with a larger width. When using multiple fingers, the values have to be divided accordingly.

$$\Phi_0 = \frac{k \cdot T}{q} \cdot ln\left(\frac{N_A \cdot N_D}{n_i^2}\right) \tag{3.8}$$

$$C_j = A_D \cdot \sqrt{\left(\frac{\epsilon_{si} \cdot q}{2} \frac{N_A N_D}{N_A + N_D}\right)(\Phi_0 - V_B)^{-1}} \tag{3.9}$$

Drain and source junction capacitors are biased with a high dynamic voltage. Junctions $C_{nw\_pl}$, $C_{HN\_pw}$ $C_{nw\_pl}$ and are constantly biased and have been neglected for this reason. They can even act as a buffer capacitor for the input and output voltage.

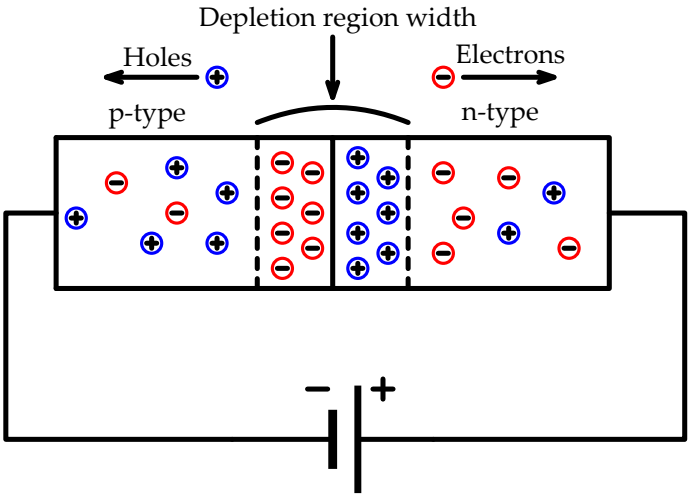


Figure 3.9: Reverse biasing a pn-junction.

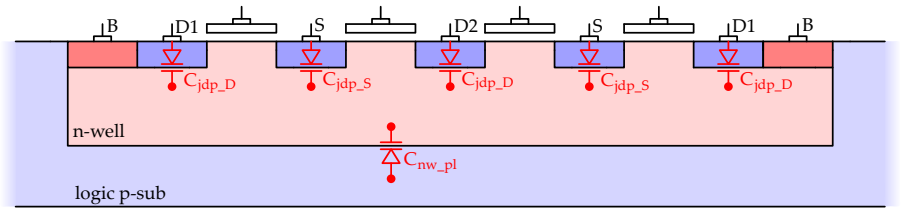


Figure 3.10: PMOS drain and source junction caps.

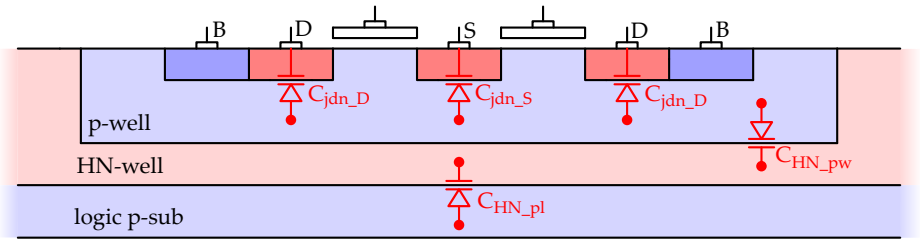


Figure 3.11: NMOS drain and source junction caps.

| Capacitor | Capacitance |
|---|---|
| $C_{jdp}$ of unit-PMOS | $600aF$ |
| $C_{jsp}$ of unit-PMOS | $600aF$ |
| $C_{jdp}$ with $W = 7.68\mu$ | $4.6fF$ |
| $C_{jsp}$ with $W = 7.68\mu$ | $4.6fF$ |
| $C_{jdp\_D}$ for each finger | $1.5fF$ |
| $C_{jsp\_S}$ for each finger | $2.3fF$ |
| $C_{jdn}$ of unit-NMOS | $1.2fF$ |
| $C_{jsn}$ of unit-NMOS | $1.2fF$ |
| $C_{jdn}$ with $W = 4.32\mu$ | $5.0fF$ |
| $C_{jsn}$ with $W = 4.32\mu$ | $5.0fF$ |
| $C_{jdn\_D}$ for each finger | $2.5fF$ |
| $C_{jsn\_S}$ for each finger | $5.0fF$ |

Table 3.5: Various capacitances.

## 3.5 Resistive parasitics (well resistances)

The mechanism described in 3.2 also considers well resistances. Well resistances are mainly determined by specific resistance and dimensions, where the specific resistance is a function of doping concentration. Figure 3.12 shows the actual layout of the pmos transistor. The transistor is built with four fingers. Every drain and source connection has its own parasitic bipolar transistor. The resistances from below the individual drain and source connections to the bulk connection have been calculated. By taking them parallel the actual base to bulk resistance can be approximated. See equations 3.10 to 3.12 for the resistance of one of the source contacts to bulk. contact resistances are $< 10\Omega$ according technology manual and have been omitted. See 3.6 for the calculated well resistances.

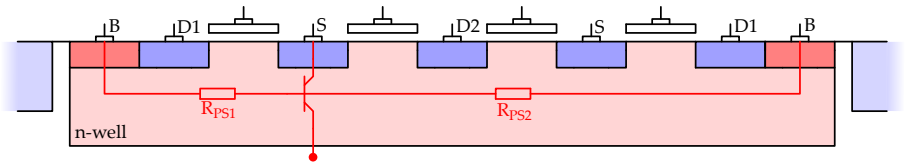


Figure 3.12: Crosssection of PMOS layout.

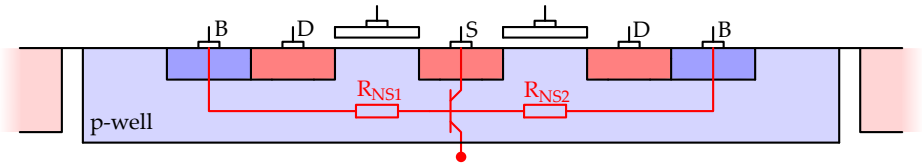


Figure 3.13: Crossection of NMOS layout.

$$\begin{aligned} R_{sq} &= \frac{\rho}{h} \\ &\Rightarrow R_{sqnw} = 180\Omega \end{aligned} \tag{3.10}$$

$$\begin{aligned} R &= R_{sq} \cdot \frac{L}{W} \\ &\Rightarrow R_{S1} = 130\Omega \\ &\Rightarrow R_{S2} = 287\Omega \end{aligned} \tag{3.11}$$

$$R_S = R_{S1} || R_{S2} = 90\Omega \tag{3.12}$$

| Resistor | Type | Resistance |
|---|---|---|
| $R_{PS}$ | PMOS | 90Ω |
| $R_{PD1}$ | PMOS | 43Ω |
| $R_{PD2}$ | PMOS | 104Ω |
| $R_{NS}$ | NMOS | 52Ω |
| $R_{ND}$ | NMOS | 32Ω |

Table 3.6: Bulk to drain/source resistances.

## 3.6 Variant with different n-well connection

A variant of the charge pump has been investigated. The HN n-well has been connected to the output voltage node. See figure 3.14. This way, a faster start-up can be achieved, because the pn junction between input and output is forward biased.

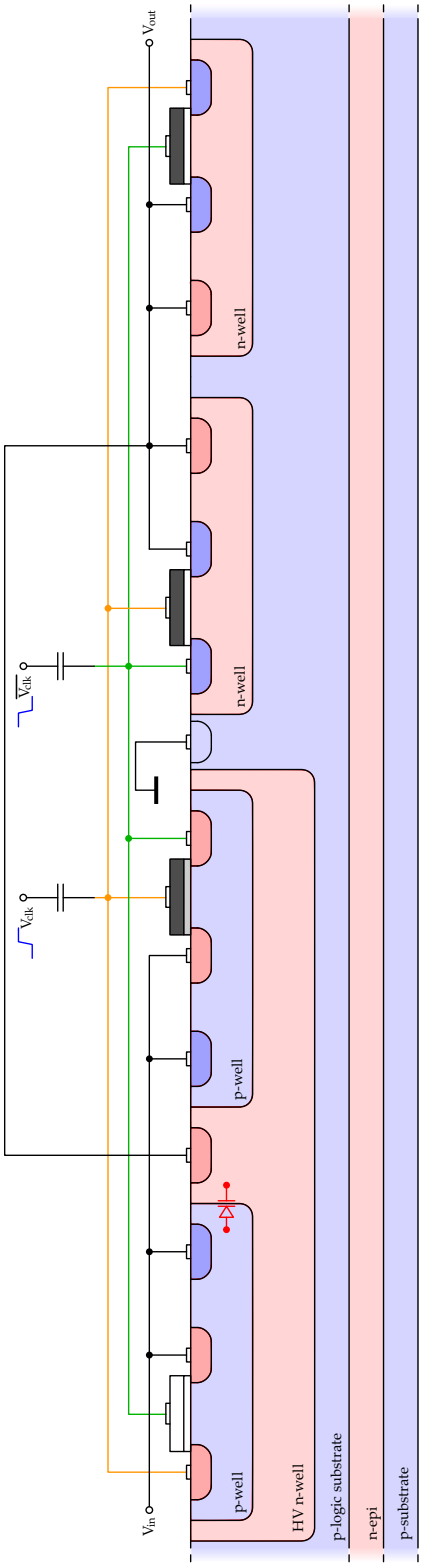


Figure 3.14: Cross section of CP with different HN n-well connection.

# 4 Comparison of simulation results

The affect of the added parasitics on the behaviour of the charge pump circuit has been investigated by doing comparing simulations. In particular the startup and settling behaviour has been observed.

## 4.1 Testbench

Figure 4.1 shows the circuit of one charge pump stage. Figures 4.2 to 4.3 show the connection of the individual parasitic bipolar transistors, resistors and capacitors, which have been determined for being possibly critical. They are connected via nets za, zb, vin, vout and BULK ot the charge pump stage. In order to consider only the transfer current of the parasitic BJTs, a voltage controlled voltage source from the analog lib has been used.

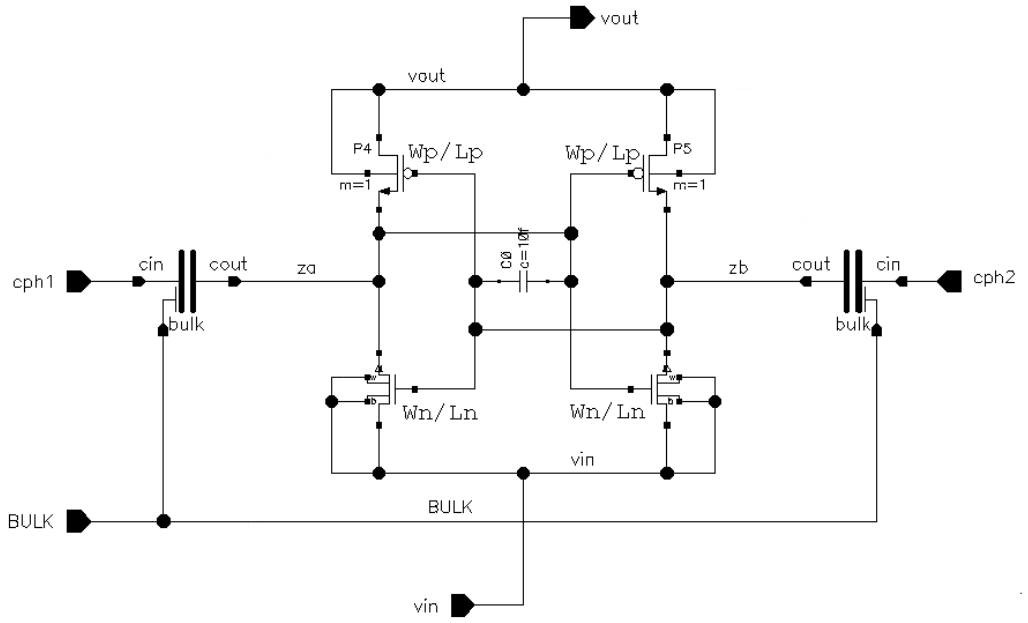


Figure 4.1: Charge pump circuit.

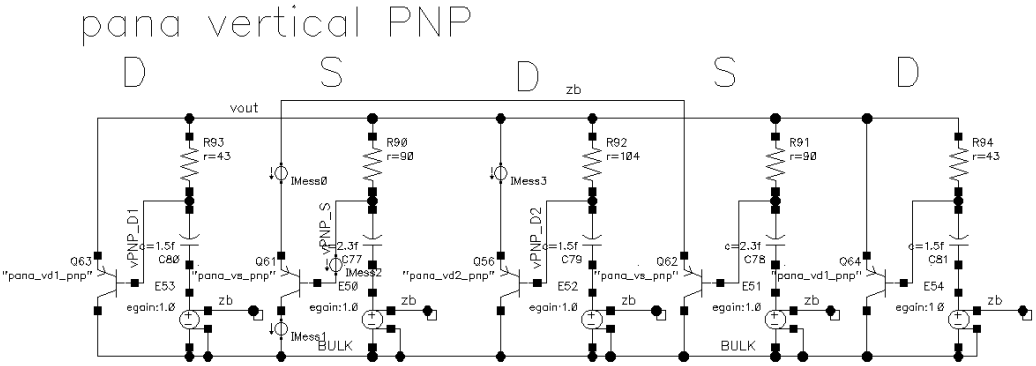


Figure 4.2: Backannotated vertical drain and source PNP.

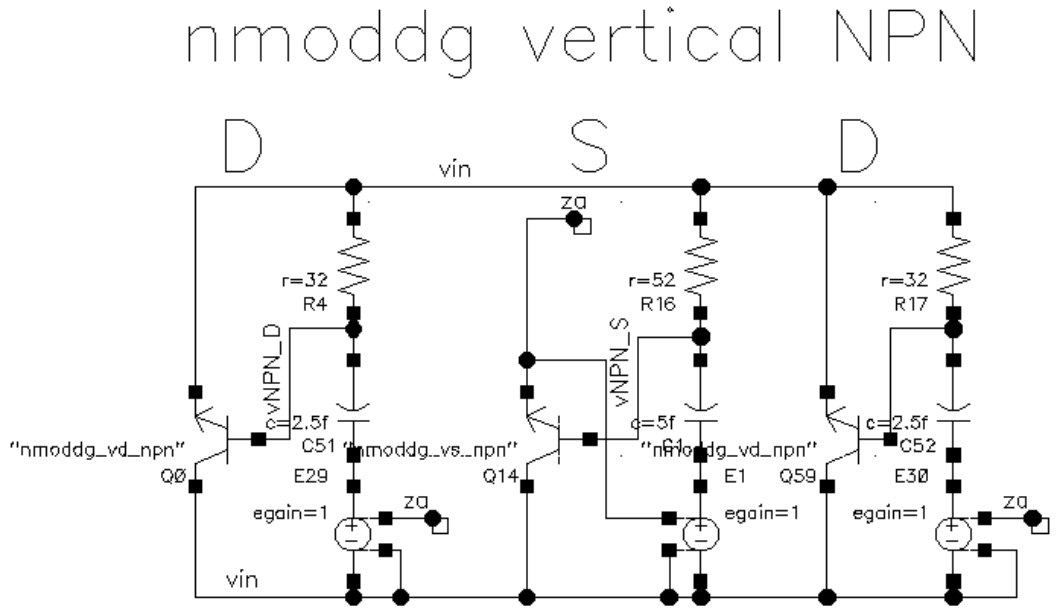


Figure 4.3: Backannotated vertical drain and source NPN.

## 4.2 Simulation results - start-up

As can be seen in the following figures, the start-up of the charge pump with added parasitics is slower than the stock charge pump. During start-up the vertical source PNP transistors of the PMOS switches get conducting and currents flow from the pumping nodes into the logic-p substrate. Figure 4.8 shows the graphs of the flowing currents.
The alternative variant with different HN n-well connection, as described in 3.6, has a slightly faster start-up behaviour. This is due to the pn junction diode which gets conducting in the start-up phase and supports charging the transfer capacitor.

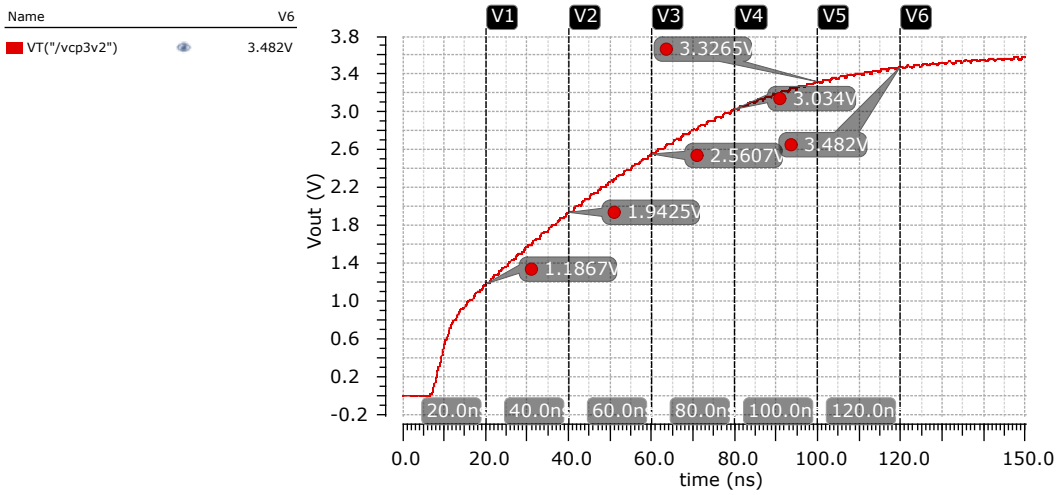


Figure 4.4: CP startup.

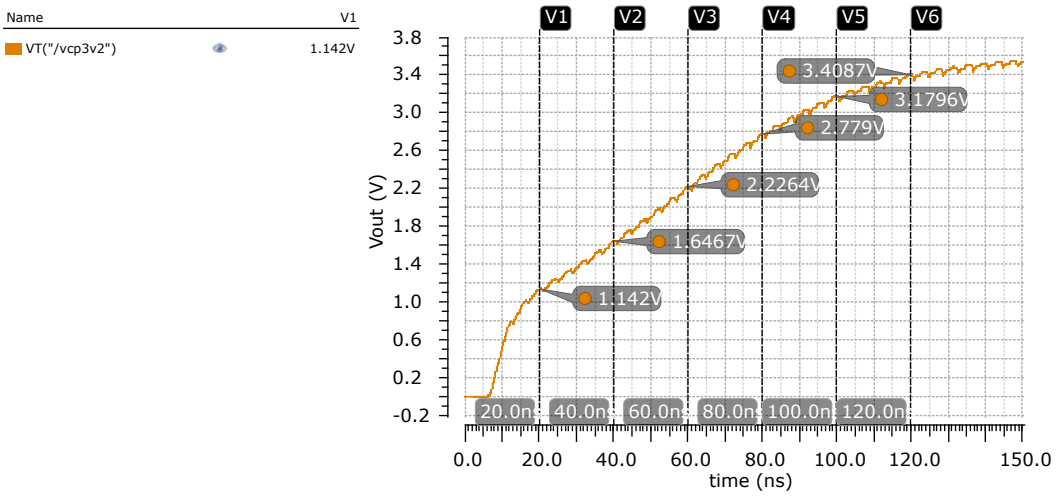


Figure 4.5: CP startup with parasitic BJT.

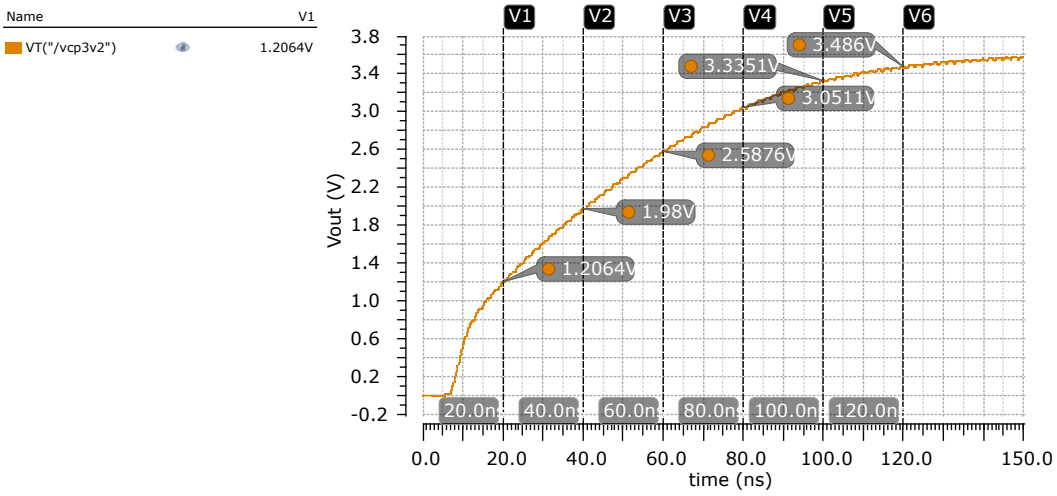


Figure 4.6: CP startup (variation).

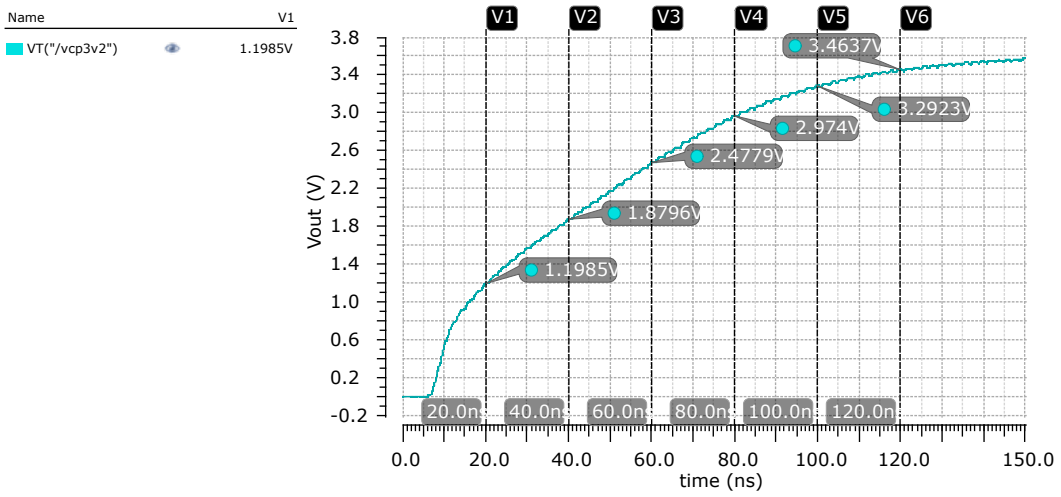


Figure 4.7: CP startup (variation) with parasitics.

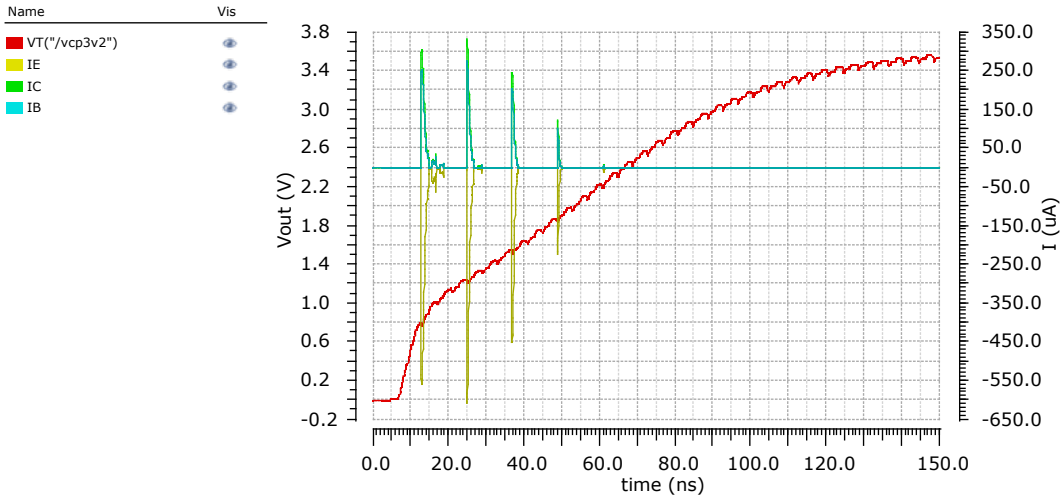


Figure 4.8: Currents of vertical source PNP during startup.

## 4.3 Settling behaviour

As can be seen in table 4.1, the backannotated bipolar transistors have almost no effect on settling behaviour. This is due to the fact, that the needed bias voltage for the transistors are not high enough to trigger the parasitics.

| simulation | value | $T = 27°C$ | $T = 85°C$ | $T = 150°C$ |
|---|---|---|---|---|
| stock | V3V2 output | $3.636V$ | $3.616V$ | $3.591V$ |
| | V4V2 output | $4.77V$ | $4.738V$ | $4.698V$ |
| | IVPMP | $3.216mA$ | $3.225mA$ | $3.236mA$ |
| | IV3V2 | $340.9\mu A$ | $339\mu A$ | $336.7\mu A$ |
| | IV4V2 | $101.5\mu A$ | $100.8\mu A$ | $99.95\mu A$ |
| | neff | $106m$ | 105.1 | 104.1 |
| | score | $30.34m$ | 30.68 | 31.1 |
| with parasitics | V3V2 output | $3.636V$ | $3.616V$ | $3.591V$ |
| | V4V2 output | 4.77 | 4.738 | 4.698 |
| | IVPMP | $3.216mA$ | $3.225mA$ | $3.236mA$ |
| | IV3V2 | $340.9\mu A$ | $339\mu A$ | $336.7\mu A$ |
| | IV4V2 | $101.5\mu A$ | $100.8\mu A$ | $99.95\mu A$ |
| | neff | $106m$ | 105.1 | 104.1 |
| | score | $30.34m$ | 30.68 | 31.1 |
| variation | V3V2 output | $3.635V$ | $3.616V$ | $3.591V$ |
| | V4V2 output | $4.69V$ | $4.738V$ | $4.698V$ |
| | IVPMP | $3.217mA$ | $3.226mA$ | $3.237mA$ |
| | IV3V2 | $340.8\mu A$ | $339\mu A$ | $336.7\mu A$ |
| | IV4V2 | $101.5\mu A$ | $100.8\mu A$ | $99.95\mu A$ |
| | neff | $106m$ | 105.1 | 104 |
| | score | $30.36m$ | 30.7 | 31.12 |

Table 4.1: Simulation results of the settled charge pump.

## 4.4 Fault injection

In order to check if the presented approach is valid, there is the possibility to do a fault injection. In this case it means manually worsen the parasitics and observe the effects in a simulation. Specifically the well resistances have been increased to $20k\Omega$ and the junction capacitors have been increased to $25fF$, to simulate a very bad design. At room temperature there is a slight decrease in output voltage. Table 4.2 shows the percentage decrease. There is more influence with higher temperatures, because of the -2mV/K temperature coefficient of the Base Emitter voltage.

| Temperature | decrease in Vout |
|---|---|
| $27°C$ | $0,6\%$ |
| $85°C$ | $1\%$ |
| $150°C$ | $1,5\%$ |

Table 4.2: Output voltage decrease with simulated bad design.

## 4.5 Measurement on Charge pump

The inspected charge pump has also been measured in the lab. Since the charge pump was part of a whole chip, it needed to be disconnected from other circuit blocks the charge-pump was supplying. This has been done with FIB (Field ion beam). This made it possible to define the load of the charge-pump externally.
Since the charge pump circuit is regulated, also the pump voltage $VPMP$ and the frequency has been measured, see figure 4.10. This information has been used to recreate the exact setup in simulation. To eliminate any influence of resistances of the probe needles, a force-sense principal has been used. Pictures 4.12 and 4.13 show the measurement setup and the ceramic sample of the chip. Figure 4.9 shows a concept drawing with the FIB cuts that have been made.
The third stage is unregulated and has been used for a comparison with the simulation. Figure 4.11 shows the percentage error of the voltage, the

last stage is adding. As can be seen, the remaining error is with $< 8\%$ in the expected range. The deviation between the two samples can be explained by statistical spread. Only two samples have been characterized. Characterizing a larger batch would have shown a statistical distribution. The simulation has been done on the RC extracted view. Bipolar parasitics have been considered as not critical in this circuit, so the remaining error can be explained with the effects of LAPO (layout polishing). In this process, the empty spaces in the metal-layers will get filled and afterwards a so called cheesing process is applied. This generates additional parasitic capacitances, which are not covered by the RC extraction flow.

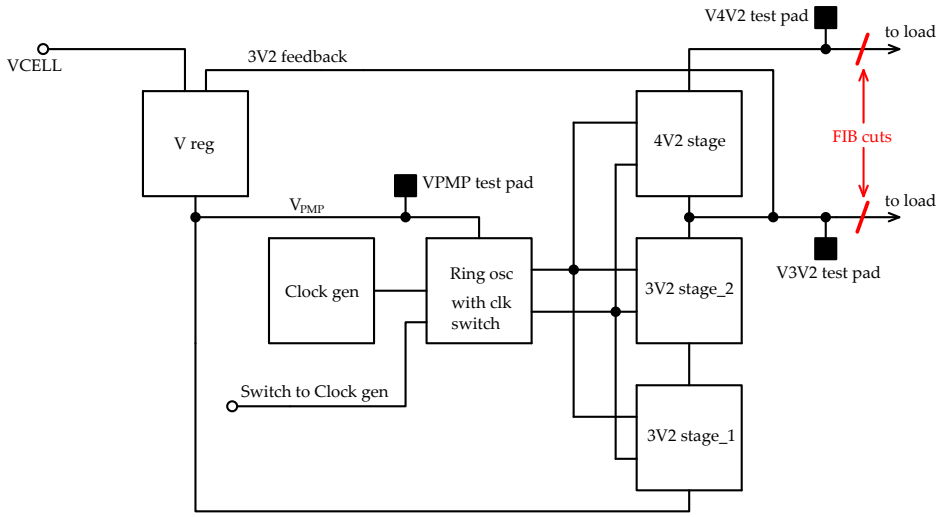


Figure 4.9: FIB cuts on charge pump circuit.

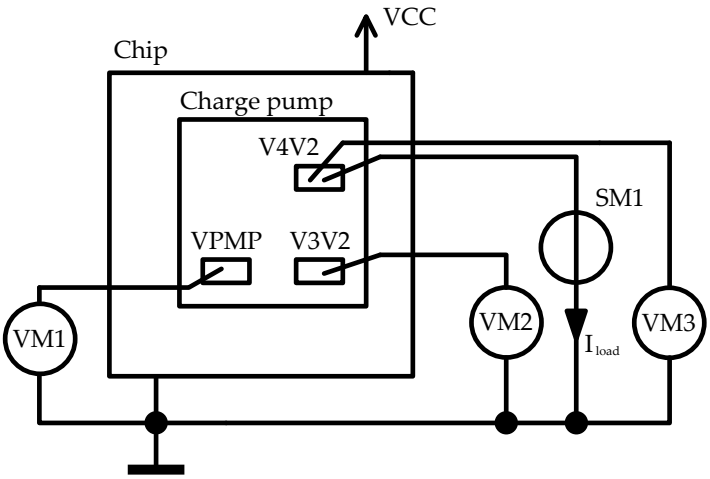


Figure 4.10: Measurement setup.

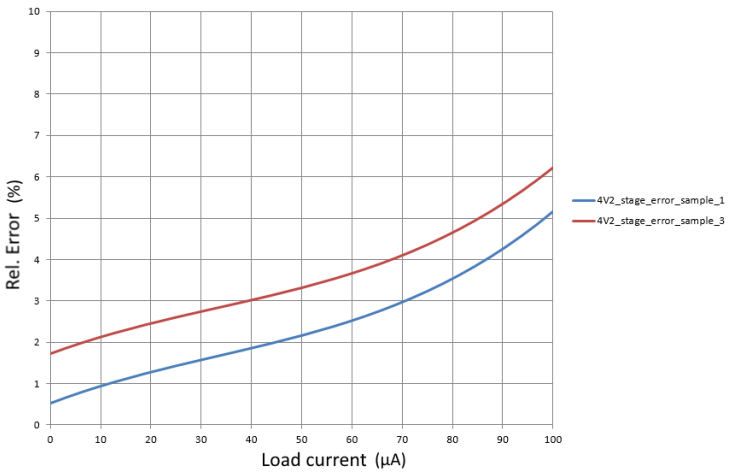


Figure 4.11: Error between measurement and simulation of last stage.

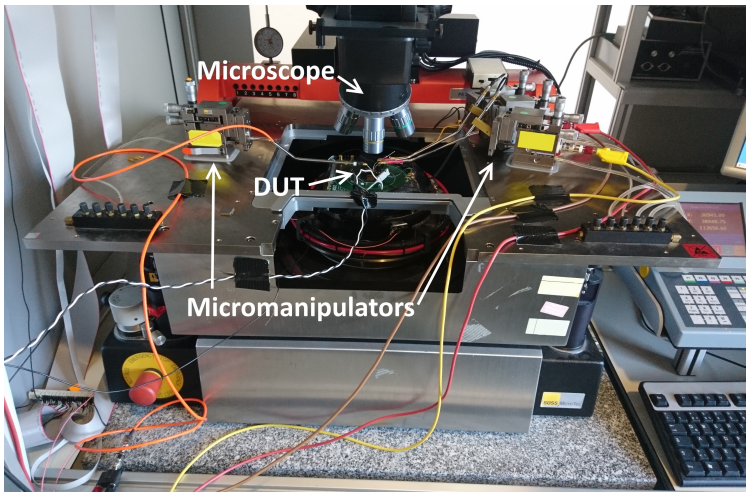


Figure 4.12: Picture of the measurement on the probestation.

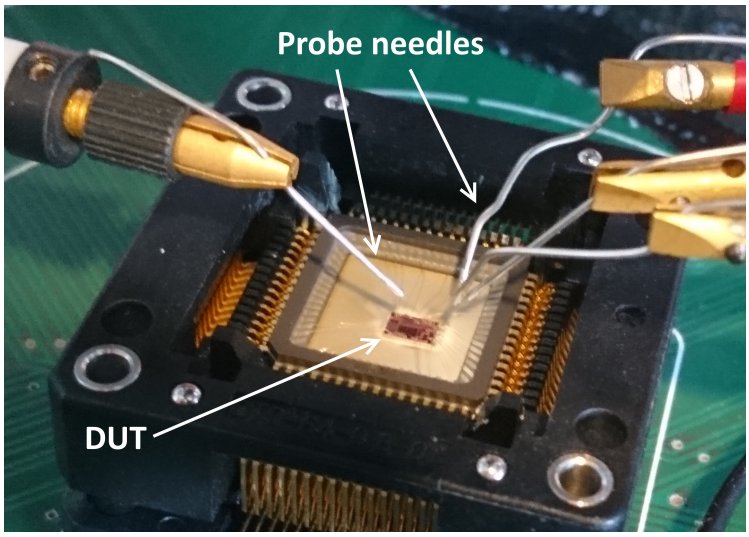


Figure 4.13: Close up of the DUT with connected probes.

# 5 Conclusion and outlook

## 5.1 Conclusion

The goal of the work was to optimize a charge pump circuit in terms of efficiency per area, by assessing the parasitic effects. The basic motivation for this work came from the fact, that the circuit designer had no possibility to do a simulation of his circuit with the parasitic elements in mind. In particular the bipolar transistors have not been considered in the MOS models. To find possible critical parasitics, the designer had do theoretically study the effects on specific circuit blocks. Of course, some parasitics may be unnoticed, by following this procedure.

These drawbacks have been addressed by manually backannotating the parasitic bipolar transistors into the circuit. To rebuild the mechanism, the well resistances and capacitances have also been backannotated. Spice models have been used to model the bipolar transistors.
Three methods for parametrizing the models have been studied. Hand calculations with layout dimensions and doping concentrations have been proven to be more than an estimation. The results are often too much off and not plausible. Main cause has been turned out to be reading off the doping concentration from the doping profile.
Determining the spice parameters from a TCAD simulations has also been considered as not feasible for a designer, because the effort is way to high. It has been shown, that measurements from a testwafer, in conjunction with layout data to get a scaling factor, gives results, that can be used for a qualitative estimation of the bipolar parasitics.

Comparing simulations of the circuit with and without the added parasitics have shown a slight impact to the start-up behaviour.

## 5.2 Outlook

In order to get a better parametrization of the bipolar transistors it would be necessary to extract more parameters out of the test structure measurement. The bipolar transistors are backannotated manually at the moment. In the long term the parasitic bipolar transistors should be characterized by the technology developers and be integrated in the MOS models.

By generating a specific test structure with a charge pump circuit (where the accessibility to all relevant nodes is guaranteed), the effects of parasitics can be better studied. Correlations with the simulation can be investigated. The developed method is not restricted to charge pump circuits only, it can be applied to any other design task.

# Appendix

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