Philipp Schmitzberger, BSc

Digitally Controlled Buck Converter for a 48V Battery Management System

Master's Thesis

to achieve the university degree of

Diplom-Ingenieur

Master's degree programme: Electrical Engineering

submitted to

Graz University of Technology

Supervisor

Ass.Prof. Dipl-Ing. Dr.techn. Gunter Winkler

Institute of Electronics
Head: Univ.-Prof. Dipl-Ing. Dr.techn. Bernd Deutschmann

Graz, May 2019

Affidavit

I declare that I have authored this thesis independently, that I have not used other than the declared sources/resources, and that I have explicitly indicated all material which has been quoted either literally or by content from the sources used. The text document uploaded to TUGRAZonline is identical to the present master's thesis.

Date

Signature

Abstract

In present 48 V mild hybrid electric vehicles (MHEVs) there is beside the main 48 V lithium-ion battery an additional 12 V battery, which is amongst other things, used to supply the battery management system (BMS) of the lithium-ion battery. To be independent of this second 12 V battery for future systems, a buck converter to step down the 48 V for the BMS is used. Instead of using a dedicated buck converter controller integrated circuit (IC), the feasibility and implementation effort of a discrete buck converter, which is digitally controlled by an already existing microcontroller unit (MCU) of the BMS, is shown. By comparison of different control schemes, voltage mode control (VMC) seems to be the most adequate control scheme for this system but still requires relative high computational effort, which is difficult to additionally implement on the existing MCU. Simulations have shown, that for this system an unregulated buck converter, where the duty cycle is calculated with the present input voltage, is possible by increasing the capacitance and choosing an appropriate sampling period to calculate the duty cycle.

Kurzfassung

In derzeitigen 48 V Mild-Hybrid Fahrzeugen (MHEV) befindet sich neben einem 48 V Lithium-Ionen-Akku noch ein zusätzlicher 12 V Akku, welcher unter anderem zur Versorgung des Batteriemanagementsystems (BMS) für den Lithium-Ionen-Akku verwendet wird. Um in zukünftigen Systemen nicht mehr an diesen zweiten 12 V Akku gebunden zu sein, wird ein Abwärtswandler verwendet um die 48 V in eine niedrigere Spannung für das BMS zu wandeln. Anstatt der Verwendung eines fertigen Abwärtswandlers mit integrierter Regelung, wird die Machbarkeit und der Implementierungsaufwand eines diskreten Abwärtswandlers, welcher von einem bereits existierenden Mikrocontroller (MCU) digital geregelt werden soll, gezeigt. Durch Gegenüberstellung verschiedener Regelungsmethoden hat sich herausgestellt, dass die Regelung über die Ausgangsspannung (VMC) am geeignetsten zu sein scheint. Durch den relativ hohen Rechenaufwand ist es jedoch schwierig diese Regelungsmethode am existierenden MCU zusätzlich zu implementieren. Simulationen haben ergeben, dass für dieses System ein ungeregelter Abwärtswandler, bei welchem das Tastverhältnis nur über die aktuelle Eingangsspannung berechnet und gestellt wird, ausreichend ist, indem die Kapazität vergrößert und eine geeignete Abtastrate gewählt wird.

Acknowledgements

In the first place I want to thank my supervisor Ass.Prof. Dr. Gunter Winkler for his assistance and the helpful discussions. Furthermore, special thanks to Prof. Dr. Bernd Deutschmann for his help and input to this thesis.

I would like to express my gratitude to Markus Pretschuh and Dr. Maximilian Hofer for their support, advices and contribution to make this thesis possible at Samsung SDI. I have received generous support from my colleagues at work which I truly appreciate.

I'm extremely grateful to my family and friends who always supported and helped me to stay motivated.

My deepest appreciation goes to my girlfriend Simone who encouraged me during writing this thesis and always believed in me.

Contents

List of Figures

1 Introduction

Digital control in DC-DC converters is increasing in popularity, due to its advantages compared to analog control. Some of these advantages are: less influence by ageing of components and component tolerances, flexibility in design and less part count for advanced compensators. Digital control also comes with some disadvantages like sampling and computational delay, limited resolution due to finite word-length and quantization of the analog-to-digital converter (ADC) and digital pulse-width modulation (DPWM) unit [1]. Furthermore, digital control of fast switching DC-DC converters require quite powerful microcontroller units (MCUs) or digital signal processors (DSPs) which are expensive. If there is an appropriate MCU already existing in the system which can additionally undertake the digital control, the advantages of digital control without increased costs or even cost savings can be realised.

1.1 System Overview

This thesis was realised in cooperation with Samsung SDI which is specialised at electrical energy storage systems for automotive applications. In present 48 V mild hybrid electric vehicle (MHEV) systems, there is beside the main 48 V battery an additional 12 V battery. Currently the battery management system (BMS) for the 48 V lithium-ion battery, at Samsung SDI, is powered by this 12 V battery. As this second 12 V battery could be removed in the future, the BMS has to be powered by its own higher voltage battery.

Figure 1.1 shows an overview of the system. The MCU for the battery management is powered by a system basis chip (SBC) which is delivering a stable supply voltage. This SBC is tailored for the MCU and has a buck converter followed by a linear regulator to minimize the losses of the linear regulator and provide a stable output voltage. The 48 V of the lithium-ion battery exceeds the upper input voltage limit of the SBC so that an additional buck converter is needed to step down the voltage. This additional buck converter would typically be realized with a dedicated buck controller integrated circuit (IC) with an analog integrated compensator.

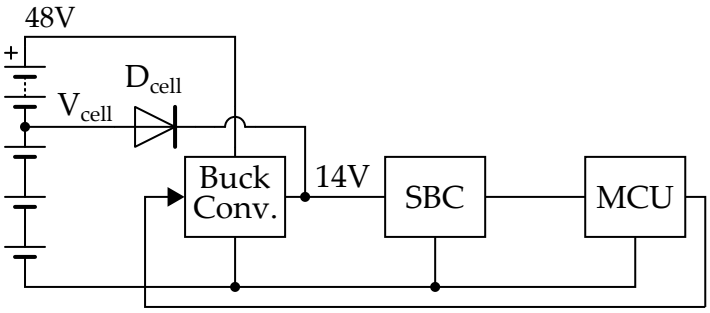


Figure 1.1: System overview

Table 1.1: Specifications

	minimum	*nominal*	*maximum*
V_{in}	25 V	48 V	75 V
V_{out}	13 V	14 V	15 V
I_{out}	50 mA		250 mA

To save costs and use the numerous advantages of digital control in power converters, the already present MCU could be used to regulate the buck converter by itself. At start-up the MCU needs an additional supply voltage to be able to start-up the buck converter. This supply voltage is provided by using the voltage V_{cell} of the first three cells of the 48 V battery in series. With this setup the MCU uses this pre-bias voltage to be able to start-up the buck converter and increases the output voltage to be above the pre-bias voltage. To prevent current flowing into the three cells a diode D_{cell} as shown in figure 1.1 is used.

1.1.1 Requirements

The specifications of the buck converter are listed in table 1.1. The input voltage range is quite high with voltages ranging from 25 V to 75 V. The output voltage of the buck converter has to be within 13 V to 15 V. The lower limit is set by the pre bias voltage $V_{cell,bias}$ of the three lithium-ion battery cells. If this lower voltage limit is undershot the current will be supplied by the three cells. This leads to an uneven discharging of the cells from the battery pack and balancing of the cells is required. With passive balancing this means that the energy provided by the three cells through this pre-bias connection has to be transferred into heat for all other cells of the battery pack. Therefore, this pre-bias connection should only be used to supply the MCU if it is in standby mode and at start-up of the buck converter.

The concept of the digitally controlled buck converter should be preferable inexpensive and energy-efficient. Furthermore, the computational effort of the MCU should be relatively small.

1.2 Thesis Organisation

In Chapter 2 the fundamentals of a buck converter and its possible modes of operation are described. Furthermore, different control schemes and their digital implementation effort are compared against each other.

Chapter 3 describes the design of a voltage mode controlled buck converter prototype. The component selection, digital controller design as well as printed circuit board (PCB) layout considerations are addressed. Besides the measurement of the designed digital controller, efficiency and the conducted electromagnetic emission (EME) were measured.

The feasibility of a buck converter without feedback to fulfil the requirements is examined in chapter 4.

2 Buck Converter Fundamentals

The buck converter, also called step-down converter, is a switched mode power supply (SMPS) topology, where the output voltage V_{out} is smaller than the input voltage V_{in}. Unlike linear regulators, which basically act like a variable resistor to reach the desired output voltage, an ideal SMPS transfers the input energy to the output without losses using energy storage elements like inductors and capacitors. Figure 2.1 shows the basic circuit of an ideal buck converter consisting of a switch S, a diode D_1 and the output filter consisting of an inductor L and a capacitor C.

By turning ON and OFF the switch S with a switching frequency f_{sw}, the desired output voltage can be adjusted by the duty cycle D. For a buck converter there are two different operating modes depending if the inductor current reaches zero: continuous conduction mode (CCM) and discontinuous conduction mode (DCM).

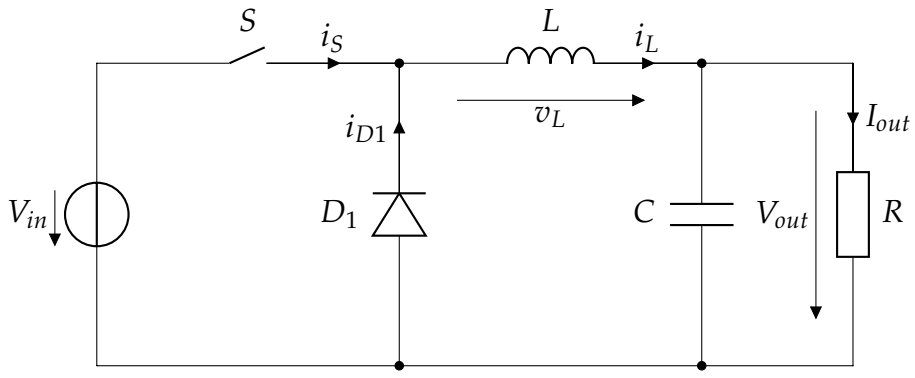


Figure 2.1: Ideal buck converter

2.1 Modes of Operation

2.1.1 Continuous Conduction Mode

In CCM , where the inductor current does not reach zero, the output-to-input voltage ratio depends only on the duty cycle D shown in equation 2.4. The operation of the buck converter in CCM can be divided into two phases: T_1: switch S is ON and T_2: switch S is OFF.

In the first phase T_1, current flows from the input voltage source through S and the inductor L to the capacitor C and load resistance R. During the time, where the switch S is ON, the current rises with the up-slope S_{up} given by equation 2.1.

After turning OFF the switch S the inductor tries to maintain the current flow due to its typical characteristics and the diode $D1$ becomes conductive. The current flows through the diode to the inductor, the capacitor and the load resistance. In this phase T_2 the inductor current declines with the down-slope S_{down} given by equation 2.2.

These two phases are repeated periodically with the switching frequency f_{sw}. In Figure 2.2, which depicts some waveforms of the buck converter, it can be seen that the inductor current waveform has a triangular shape and changes by Δi_L up and down each switching cycle. By multiplying the up-slope from equation 2.1 with the time the switch S is ON, the inductor current ripple Δi_L can be calculated with equation 2.3, which is independent from load current I_{out}. The average current through the inductor is equal to the I_{out}.

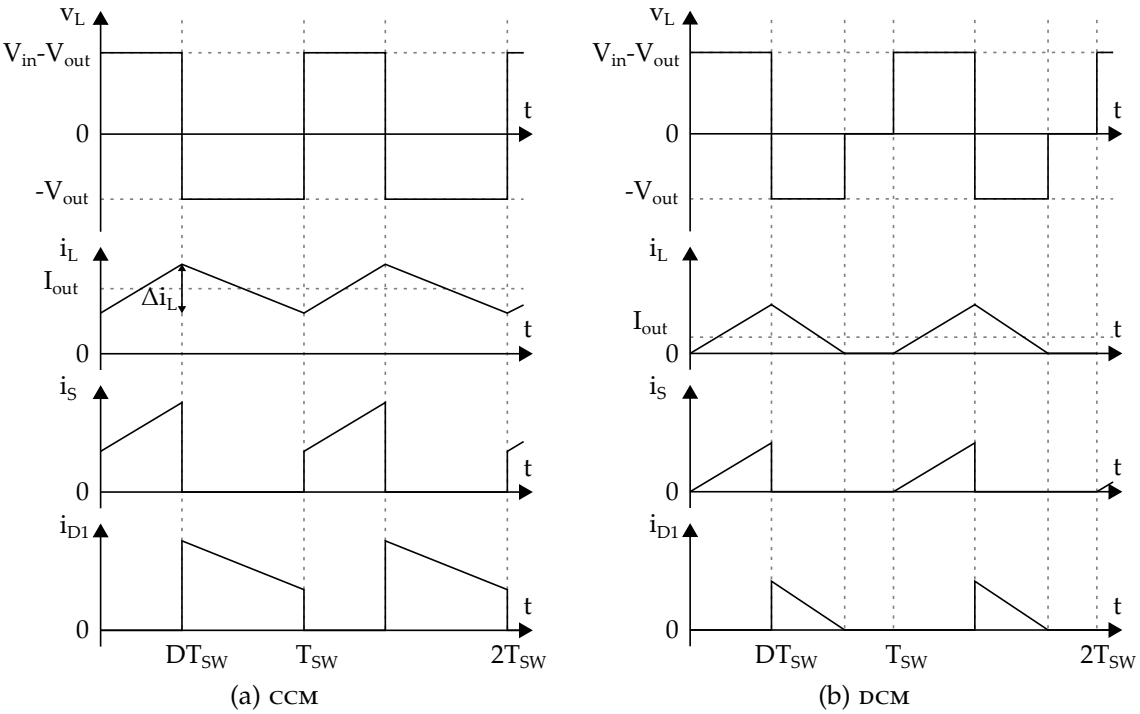
$$S_{up} = \frac{V_{in} - V_{out}}{L} \tag{2.1}$$

$$S_{down} = \frac{-V_{out}}{L} \tag{2.2}$$

$$\Delta i_L = \frac{V_{in} - V_{out}}{L} \cdot DT_{sw} \tag{2.3}$$

2.1.2 Discontinuous Conduction Mode

As the load current decreases, the average inductor current also decreases and at a certain point the inductor current reaches zero. This boundary between CCM and DCM occurs at $I_{out,crit} = {}^{\Delta i_L}/_2$. Further reduction of the load forces the inductor current to stay at zero until the beginning of the next switching cycle, as the diode only conducts current in one direction as shown in figure 2.2. In



(a) CCM (b) DCM

Figure 2.2: Waveforms buck converter in CCM (a) and DCM (b)

DCM the output-to-input voltage conversion ratio is load dependent and can be calculated with equation 2.4 for the steady state [2].

$$\frac{V_{out}}{V_{in}} = \begin{cases} D, & \text{for CCM.} \\ \frac{2}{1+\sqrt{1+\frac{4K}{D^2}}}, & \text{for DCM.} \end{cases} \qquad K = \frac{2L}{RT_{sw}} \tag{2.4}$$

2.1.3 Forced-Continuous Conduction Mode

In a synchronous buck converter the diode D_1 of figure 2.1 is replaced with a switching element that can conduct current in both directions like a metal-oxide-semiconductor field-effect transistor (MOSFET). Figure 2.3 shows a synchronous buck converter where the high-side and low-side switches are both realized with MOSFETs, which are switched complementary. This allows the inductor current to become negative and the buck converter is always operating in CCM. Therefore, this operation mode is also called forced-CCM.

Due to the finite switching speeds of MOSFETs, a dead-time, where both gate drive signals are low, has to be added to ensure that the other transistor is completely

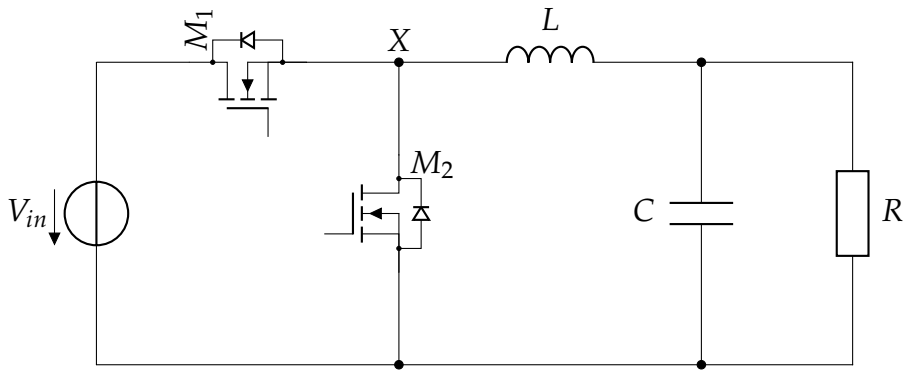


Figure 2.3: Synchronous buck converter

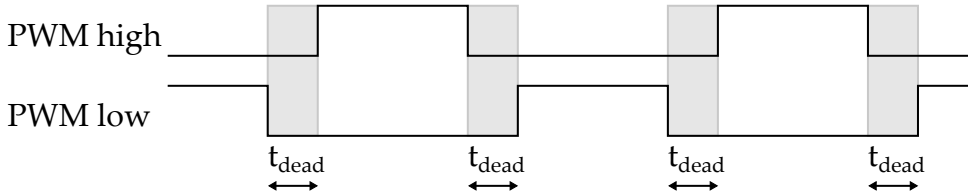


Figure 2.4: Dead-time to prevent shoot-through current

turned OFF before a transistor is turned ON. Figure 2.4 shows the timing diagram of the high-side and low-side pulse-width modulation (PWM) signal with a dead-time t_{dead}. This prevents high shoot-through current as the input voltage source would be shortened if both transistors are ON at the same time. In the period where both transistors are turned OFF the inductor current is provided through the body diode of the MOSFET.

2.2 Transfer Functions

For compensator design there are two important transfer functions of a buck converter: the control-to-output voltage transfer function $G_{vd}(s)$ and the control-to-inductor current transfer function $G_{id}(s)$.

2.2.1 Continuous Conduction Mode

There are several methods to obtain the small-signal transfer functions of a buck converter like the basic alternating current (AC) modelling approach or state space averaging [2]. In this section another method is used, where the PWM switch is

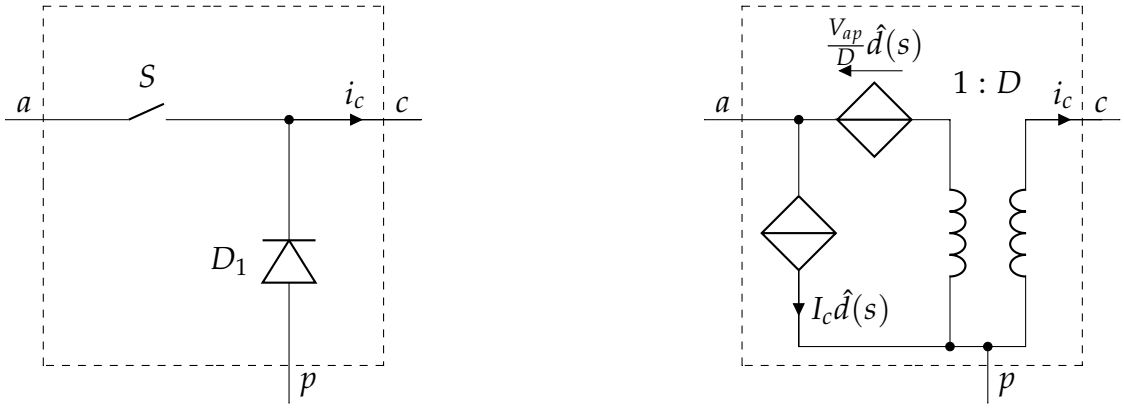


Figure 2.5: PWM switch (a) and its small- and large-signal model (b) [3]

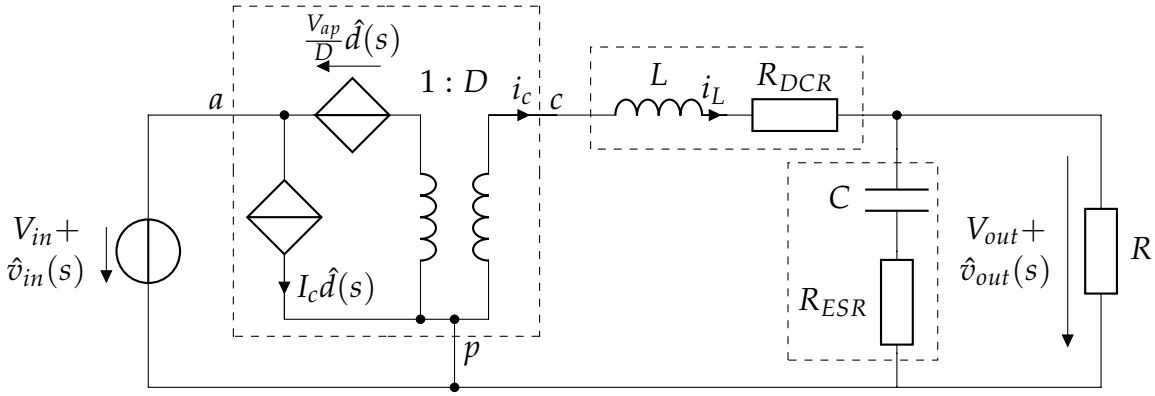


Figure 2.6: Combined small-signal and large-signal model of a non-ideal buck converter in CCM

replaced by an simplified average small- and large-signal model presented in [3]. Figure 2.5a shows a PWM switch consisting of a switch S and a diode D_1 and in figure 2.5b its small- and large-signal model with a controlled current and controlled voltage source. The ports are labelled with *a* for *active*, *c* for *common* and *p* for *passive*. By replacing the switch and diode of the buck converter with this PWM model the complete small- and large-signal model of the buck converter can be created as shown in figure 2.6. With this model all important transfer functions, like the control-to-output, line-to-output, input-impedance or output-impedance can be derived. In the following sections small AC variations are denoted with a hat, for example $\hat{d}$.

To obtain the small-signal control-to-output voltage transfer function $G_{vd,\mathrm{CCM}}(s)$ the input voltage perturbation $\hat{v}_{in}(s)$ has to be set to zero as well as the direct

Table 2.1: Component values for the control-to-output voltage function

Mode	C	R_{ESR}	L	R_{DCR}	V_{in}	R
CCM	4.7 µF	0.01 Ω	220 µH	1 Ω	48 V	140 Ω
DCM						280 Ω

current (DC) sources like V_{in}. The resulting equation, including the parasitic elements R_{DCR} and R_{ESR}, for the control-to-output voltage transfer function is given by equation 2.5. The complete derivation of $G_{vd,\text{CCM}}(s)$ is shown in the appendix section 5.

$$\begin{aligned} G_{vd,\text{CCM}}(s) &= \left.\frac{\hat{v}_{out}(s)}{\hat{d}(s)}\right|_{\hat{v}_{in}(s)=0} \\ &= V_{in}\frac{R\left(1+sCR_{ESR}\right)}{R_{DCR}+R+s\left(L+CR_{DCR}\left(R_{ESR}+R\right)+CR_{ESR}R\right)+s^2LC\left(R_{ESR}+R\right)} \end{aligned} \tag{2.5}$$

Figure 2.7 shows the bode plot of $G_{vd,\text{CCM}}(s)$ with the component values used in chapter 3 which are listed in table 2.1. The equivalent series resistor (ESR) of the capacitor produces a zero at frequency f_{ESR} given by equation 2.6. The resonant frequency of the LC filter can be calculated with equation 2.7.

$$f_{ESR} = \frac{1}{2\pi R_{C,ESR}C} \tag{2.6}$$

$$f_{LC} = \frac{1}{2\pi\sqrt{LC}} \tag{2.7}$$

For control schemes which use the inductor current to control the buck converter, the control-to-inductor current transfer function $G_{id,CCM}(s)$ has to be known. Similar to the derivation of $G_{vd,CCM}(s)$ the model shown in figure 2.6 can be used to calculate $G_{id,CCM}(s)$ which result is given in equation 2.8. The complete derivation of $G_{id,CCM}(s)$ is given in the appendix section 5.

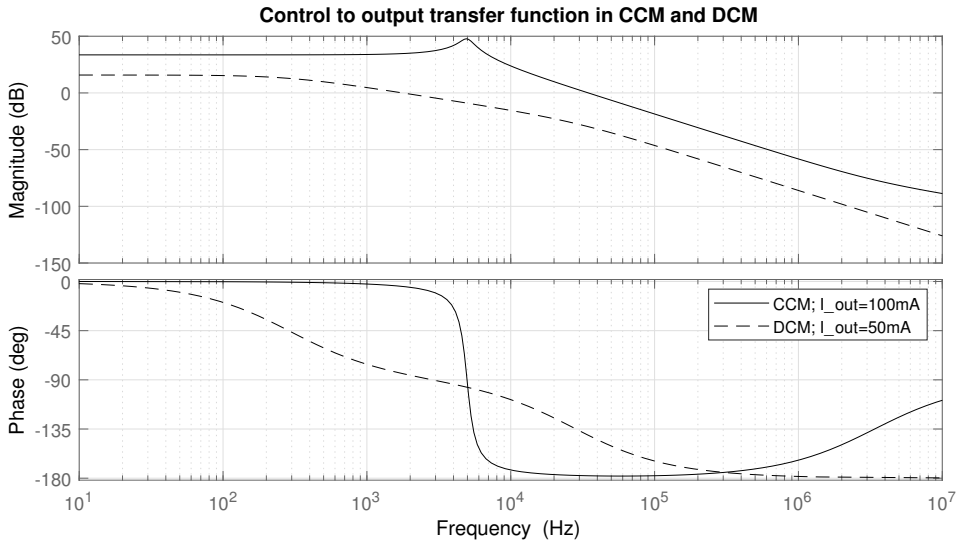


Figure 2.7: Control-to-output voltage transfer function in CCM and DCM

$$G_{id,CCM}(s) = \left.\frac{\hat{i}_L(s)}{\hat{d}(s)}\right|_{\hat{v}_{in}(s)=0}$$
$$= V_{in}\frac{1 + sC\left(R_{ESR} + R\right)}{R_{DCR} + R + s\left(L + CR_{DCR}\left(R_{ESR} + R\right) + CR_{ESR}R\right) + s^2LC\left(R_{ESR} + R\right)} \tag{2.8}$$

2.2.2 Discontinuous Conduction Mode

The control-to-output voltage transfer function of the buck converter in DCM can be calculated with equation 2.9 [2]. In DCM there are two poles. A low-frequency pole w_{p1} due to the capacitor C and a high frequency pole w_{p2} close to the switching frequency. The values for the DC gain G_{d0} and the two poles w_{p1} and w_{p2} are listed in table 2.2.

$$G_{vd,DCM}(s) = \left.\frac{\hat{v}_{out}(s)}{\hat{d}(s)}\right|_{\hat{v}_{in}(s)=0} = \frac{G_{d0}}{\left(1 + \frac{s}{w_{p1}}\right)\left(1 + \frac{s}{w_{p2}}\right)} \tag{2.9}$$

In figure 2.7 $G_{vd,DCM}(s)$ is plotted with the same component values as $G_{vd,DCM}(s)$ listed in table 2.1 expect a different R, so that the buck converter operates in DCM. Compared to $G_{vd,CCM}(s)$, the control-to-output voltage transfer function in DCM

Table 2.2: Values for the control-to-output voltage function in DCM

G_{d0}	w_{p1}	w_{p2}
$\frac{2V_{out}(1-M)}{D(2-M)}$	$\frac{2-M}{(1-M)RC}$	$\frac{2Mf_{sw}}{D(1-M)}$

varies a lot. Therefore, big attention should be paid when the compensator is designed to consider both CCM and DCM for different operating points.

2.3 Control Schemes

As the output voltage of the buck converter is only a function of the input-voltage V_{in} and the duty cycle D in CCM for steady state, the converter could be implemented without feedback just by adjusting D depending on V_{in}.

This approach has bad transient behaviour to load- and duty cycle-changes and can lead to under-damped output voltage oscillations with the LC resonant frequency dependent on the component values. Furthermore, input voltage changes get transferred to the output voltage scaled by the duty cycle D for frequencies below the cut-off frequency of the LC output filter. For most applications the output voltage limits are too tight so that a buck converter without feedback would not be feasible. Due to the special case in this system, where an additional buck converter is connected afterwards as shown in figure 1.1, the use of an unregulated buck converter is possible. Therefore, in chapter 4 the performance and design considerations using an unregulated buck converter are addressed.

To improve the performance of a buck converter, various control schemes have been developed to regulate the output voltage. Basically, there are two main fixed-frequency control schemes: voltage mode control (VMC) and current mode control (CMC). CMC can be further divided into peak current mode control (PCMC), valley current mode control (VCMC) and average current mode control (ACMC). The basic principle of VCMC and PCMC is the same, with the difference that in VCMC the inductor current is compared and limited by a lower limit reference value and in PCMC by an upper limit reverence value.

2.3.1 Voltage Mode Control

In VMC just the output voltage is used to control the buck converter by changing the duty cycle as shown in figure 2.8. Therefore, the output voltage is sensed with

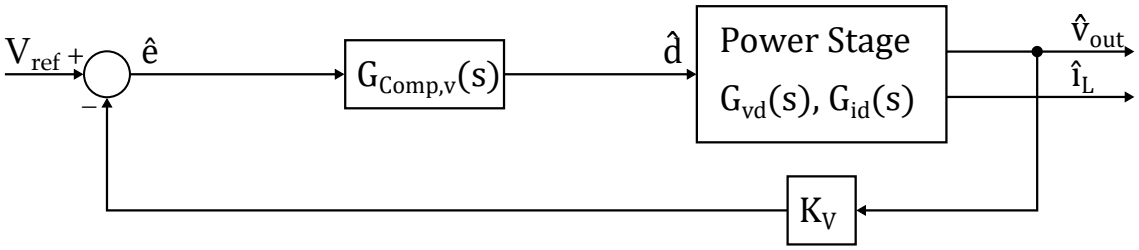


Figure 2.8: Functional diagram of VMC

the feedback gain K_V and subtracted from the reference voltage V_{ref} to form the error signal e. From this error signal the compensator $G_{Comp,v}(s)$ generates the desired duty cycle to control the buck converter. The compensator design in VMC can be difficult as the phase of the control-to-output voltage transfer function $G_{vd,CCM}(s)$ in CCM drops to $-180°$ as shown in figure 2.7. Furthermore, with a digital controller implementation, there is an additional phase decrease due to the sampling action and computational time.

As the buck converter behaves as a second order low-pass due to the LC output-filter, the dynamic response of load- or input voltage changes is slow as the controller can just react to changes in the output voltage.

2.3.2 Peak Current Mode Control

PCMC is probably the easiest current mode control and was first invented in 1978 [4], [5]. PCMC is a two loop system where the reference value V_c for the inner current loop is generated by an outer voltage loop as shown in figure 2.9. With a comparator, the driving signal for the buck converter is created by comparing the sensed inductor current with the reference current. The principle of the outer voltage loop is the same as in VMC with the only difference that instead of the duty cycle a peak current inductor reference value is generated.

Slope Compensation

For duty cycles above 0.5 sub-harmonic oscillations occur and slope compensation is required [6]. This geometric phenomena is illustrated in figure 2.10. ΔI_0 indicates a perturbation at the beginning of the switching cycle. In figure 2.10a the duty cycle is below 0.5 and Δi_L is compensated within a few switching cycles without the need of slope compensation. In the case of duty cycles above 0.5 the perturbation gets amplified as shown in figure 2.10b, which causes sub-harmonic

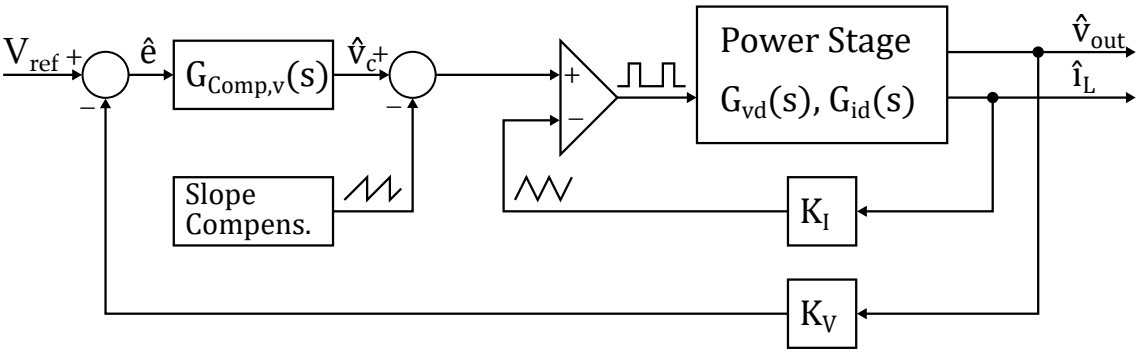


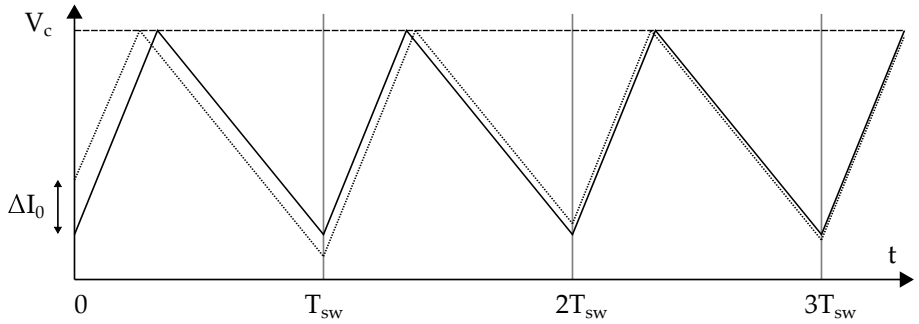
Figure 2.9: Functional diagram of PCMC

oscillations. By adding a ramp with a certain slope to the inductor current or subtracting it from the reference value this sub-harmonic oscillation can be avoided even at duty cycles above 0.5, as shown in figure 2.10c. In DCM no slope compensation is required because the inductor current starts at zero at the beginning of each switching cycle so that perturbations of previous cycles are eliminated.

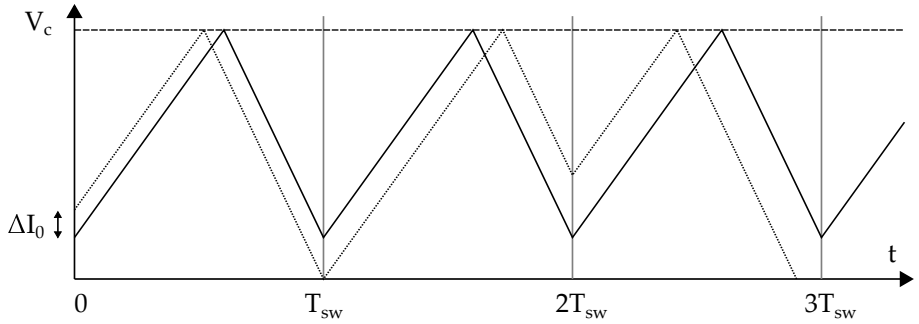
As the inductor current is limited by a reference value, PCMC offers inherent cycle by cycle current limiting. With CMC the buck converter acts like a voltage controlled current source. The design of the compensator of the outer voltage loop typically is easier compared to the one in VMC. Due to switching noise a blank time after each turn on switching has to be added, where the sensed current is not compared to the reference value.

Digital Implementation

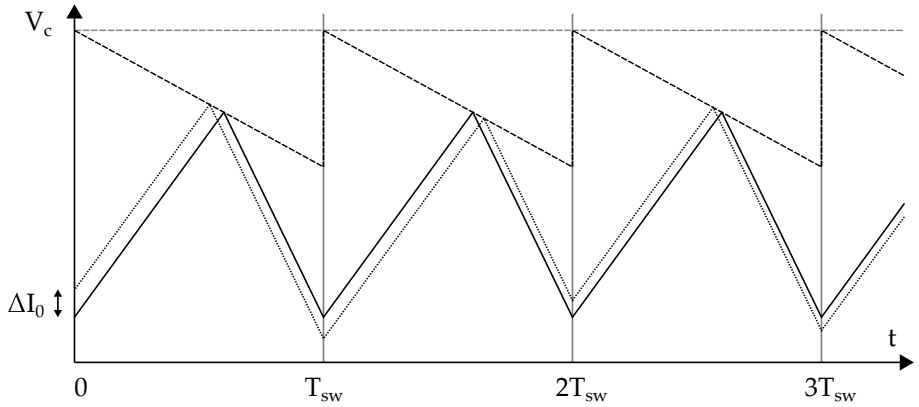
For a fully digital implementation of PCMC, the inductor current has to be sampled multiple times per switching period in order to sample or calculate the peak value. If the MCU has a digital-to-analog converter (DAC) and comparator implemented, the inner current loop could be done analog whereas the outer voltage loop could be implemented digitally as in literature [7], [8]. This approach would combine the advantages of both analog and digital control and therefore decrease the computational effort of the MCU as it just has to compute the control for the outer voltage loop. This type of controller is called a hybrid controller. Unfortunately, the target MCU has no comparators and DACs implemented and these components would have to be added external, which would increase costs, complexity and PCB area.



(a) PCMC without slope compensation and duty cycle $D < 0.5$



(b) PCMC without slope compensation and duty cycle $D > 0.5$



(c) PCMC with slope compensation and duty cycle $D > 0.5$

Figure 2.10: Effect of slope compensation at PCMC

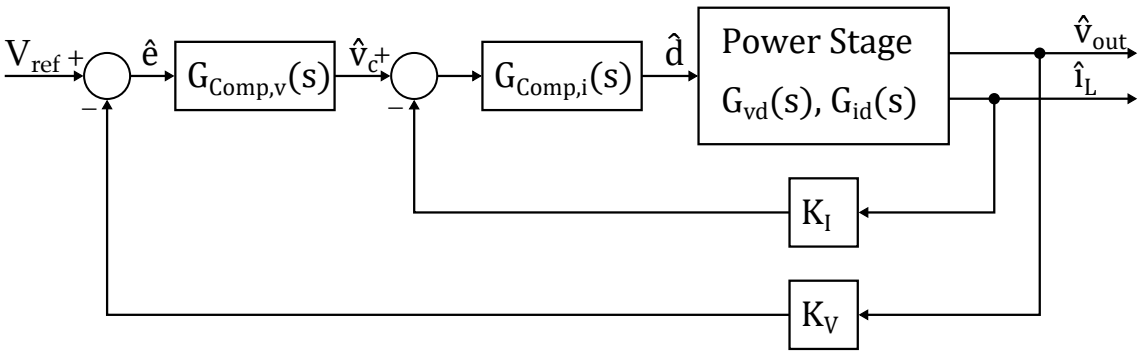


Figure 2.11: Functional diagram of ACMC

2.3.3 Average Current Mode Control

ACMC was first introduced in 1990 and is a two loop system like PCMC [9]. In ACMC there is an inner current loop controlled by a outer voltage loop as shown in figure 2.11. The principle of the outer voltage loop is like in VMC with the difference, that instead of the duty cycle a control voltage v_c as a reference for the inner current loop is generated. The current loop senses the average inductor current i_L, which is then subtracted by the control signal v_c given by the outer loop, to form the error signal e for the inner loop compensator $G_{comp,i}(s)$.

In literature [10] three different sampling techniques to obtain the average inductor current for a digital implementation of ACMC are presented: geometric, low-pass filter and slope midpoint sampling. In the geometric approach the inductor current is sampled twice per switching period and the average current is calculated from these values. With slope midpoint sampling the average inductor current is obtained by sampling the current in the middle of the slope which can be implemented relatively simple by using dual edge modulation. The advantage of ACMC compared to PCMC is that no slope compensation is required, the inner current loop can have a higher gain at low frequencies and the noise immunity is better. The drawback of ACMC is that two compensators are required and that there is no cycle by cycle current limit [9].

2.3.4 Comparison of Control Schemes

Table 2.3 summarizes the advantages and disadvantages of each control scheme, related to a digital implementation. It can be seen that there is no ideal solution and each control scheme has its own strengths.

Table 2.3: Comparison of different control schemes

Control scheme	Advantages	Disadvantages
VMC	+ one loop system + only one ADC necessary	- slower transient response - over current protection has to be implemented separately
PCMC	+ cycle by cycle current limiting + compensator design easier compared to VMC and ACMC	- bad noise immunity - slope compensation required for duty cycles > 0.5 - circuit to sense peak current necessary
ACMC	+ no slope compensation required + good noise immunity	- two digital compensator required (increased computational time) - two loop system more difficult to design - circuit to sense average current necessary

As the MCU is not only dedicated for the digital compensator and has other time critical tasks to process, computation time of the compensator as well as the frequency with which the compensator is executed is an important aspect for the selection of a proper control scheme.

VMC is chosen for the buck converter in chapter 3 because just one digital compensator has to be implemented, which results in less computational effort for the MCU. The worse transient performance compared to CMC schemes are acceptable as there is another buck converter afterwards.

2.4 Efficiency

Efficiency in power converters is an important topic, especially if the system is powered from a battery. Energy losses in the converter will be transformed into heat and can result for instance in bigger component values, the need of heat-sinks or more complex PCB layout design to get rid of the heat. The efficiency η of a converter is defined as

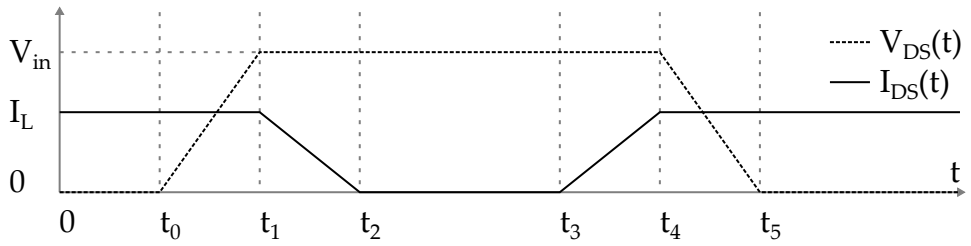


Figure 2.12: Transistor switching waveform (adapted from [2])

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}} \tag{2.10}$$

where P_{in} is the input power and P_{out} is the output power of the converter. The power loss P_{loss} which appears in the power converter is composed of the switching power loss P_{switch}, the conduction power loss P_{cond} and the fixed power loss P_{fixed} given in equation 2.11 [2].

$$P_{loss} = P_{switch} + P_{cond} + P_{fixed} \tag{2.11}$$

The following efficiency equations are given for a synchronous buck converter. Variables belonging to the high-side MOSFET are denoted with index H, whereas index L denotes the low-side MOSFET.

2.4.1 Switching Power Losses

The switching power loss P_{switch} is proportional to the switching frequency, as a certain switching energy is lost with every switching period. The major switching power losses are listed below.

Switching Clamped Inductive Load

The inductor L and body diode of the low-side MOSFET, shown in figure 2.3, act like a clamped inductive load. The typical transistor waveform for switching this type of load are shown in figure 2.12.

At t_0 the turn-OFF switching process of the high-side MOSFET starts. From t_0 to t_1 the drain-source voltage V_{DS} ramps up to V_{in} and the drain-source current I_{DS} stays constant. At time t_1 the body diode of the low-side MOSFET becomes conductive and I_{DS} declines and reaches 0 A at t_2. The turn-ON switching process

is quite similar. From t_3 to t_4 I_{DS} ramps up until the whole inductor current I_L flows through the high-side MOSFET. Afterwards V_{DS} is able to decrease to 0 V as the low-side body diode stops conducting. Power loss occurs at time intervals $t_{off} = t_2 - t_0$ and $t_{on} = t_5 - t_3$, where V_{DS} and I_{DS} are not zero. If the waveforms are assumed piecewise linear this clamped inductive switching loss $P_{UI,H}$ of the high-side MOSFET can be calculated with equation 2.12 [2].

$$P_{UI,H} = \frac{1}{2} V_{in} I_L \left(t_{off,H} + t_{on,H} \right) f_{sw} \tag{2.12}$$

If the inductor current stays positive, $P_{UI,L}$ for the low-side MOSFET can be calculated with equation 2.13, where V_D is the forward voltage drop of the body diode.

$$P_{UI,L} = \frac{1}{2} V_D I_L \left(t_{off,L} + t_{on,L} \right) f_{sw} \tag{2.13}$$

Dead-time

In the time period t_{dead}, where both transistors are completely turned OFF, the inductor current flows through the body diode and power loss occurs due to the forward voltage drop V_D of the body diode given in equation 2.14.

$$P_{dead} = 2 V_D I_L t_{dead} f_{sw} \tag{2.14}$$

When the body diode, formed by a p-n junction, changes from the forward biased to reverse biased condition the stored minority charge Q_{RR} of the diode has to be removed within the reverse recovery time t_{RR}. This process is called reverse recovery and the resulting power loss P_{RR} can be estimated with equation 2.15 [2]. Especially with high input voltages P_{RR} can be a major part of the overall power losses. To increase the efficiency an external Schottky diode with a lower forward voltage than the body diode can be added in parallel. The junction of Schottky diodes are formed by a semiconductor and metal and therefore no reverse recovery occurs.

$$P_{RR} \approx \left(V_{in} I_L t_{rr} + V_{in} Q_{RR} \right) f_{sw} \tag{2.15}$$

Output Capacitance

With every switching cycle the output capacitance $C_{OSS} = C_{DS} + C_{GD}$ of both MOSFETs has to be charged and discharged, which result in the power loss given in equation 2.16 [11].

$$P_{COSS} = \frac{1}{2} \left(C_{OSS,H} + C_{OSS,L} \right) V_{in}^2 f_{sw} \tag{2.16}$$

Gate Charge

With every switching period the input capacitance of the MOSFET has to be charged and discharged. Due to the high non-linearity of the input capacity the total gate charge Q_G is typically listed in the datasheet. With equation 2.17 the power loss P_Q of the gate drive circuit can be calculated, where V_{GS} is the applied voltage of the driver circuit [6].

$$P_Q = Q_G V_{GS} f_{sw} \tag{2.17}$$

2.4.2 Conduction Power Losses

Conduction power loss P_{cond} in power converters appears due to the forward voltage drop of the semiconductor devices, as well as conduction losses due to parasitic elements like the direct current resistor (DCR) of the inductor. The conduction power loss P_{DCR} from the DCR of the inductor can be calculated with equation 2.18.

$$P_{DCR} = I_{L,RMS}^2 R_{DCR} \approx I_{out}^2 R_{DCR} \tag{2.18}$$

The conduction power loss $P_{rds,on,H}$ for the high-side MOSFET and $P_{rds,on,L}$ for the low-side MOSFET depend on their on-resistance $r_{ds,on}$ and are given by equation 2.19 and 2.20.

$$P_{rds,on,H} = I_{L,RMS}^2 r_{ds,on,H} D \approx I_{out}^2 r_{ds,on,H} D \tag{2.19}$$

$$P_{rds,on,L} = I_{L,RMS}^2 r_{ds,on,L} (1 - D) \approx I_{out}^2 r_{ds,on,L} (1 - D) \tag{2.20}$$

2.4.3 Fixed Power Loss

The fixed loss P_{fixed} is the power loss, which is not related to the switching frequency or the output current, which could be the quiescent power needed for the MOSFET drive circuit or power dissipated by the resistor divider to scale down the voltage for the ADC. Usually, the power needed for the control circuit belongs to the fixed power losses. In this case, the MCU, which controls the buck converter, is part of the load itself.

3 Voltage Mode controlled Buck Converter

3.1 System Overview

Figure 3.1 shows an overview of the voltage mode controlled buck converter. The output voltage is scaled down by a voltage divider network, shown as gain block H_V, and fed into the ADC of the MCU. Afterwards, the error signal e is calculated by subtracting the ADC-result from the given reference voltage V_{ref}. The digital compensator, which is designed in section 3.5.4, computes the duty cycle D from the error signal. A PWM signal with the switching frequency f_{sw} is generated with the DPWM unit of the MCU which is sent to an external MOSFET driver IC to drive the MOSFETS.

As the MCU is indirectly supplied by the output voltage of the buck converter it has to be supplied from another source at initial start-up. Therefore, the output is pre-biased with three lithium-ion battery cells in series resulting in a voltage V_{cell} of 12 V using a nominal cell voltage of 4 V. To prevent current flowing into these three cells, once the output voltage is above V_{cell}, the diode D_{cell} is placed between the output voltage and the three cells.

3.2 Synchronous vs non-synchronous

In the first step of the VMC buck converter design, the decision between a synchronous or a non-synchronous buck converter has to be made. Each topology has its strengths and weaknesses, so a compromise has to be found.

High-side Driver Start-up Problem

For the high-side switch a n-channel MOSFET instead of a p-channel MOSFET is used as it has better properties like lower $r_{ds,on}$ for the same semiconductor die area

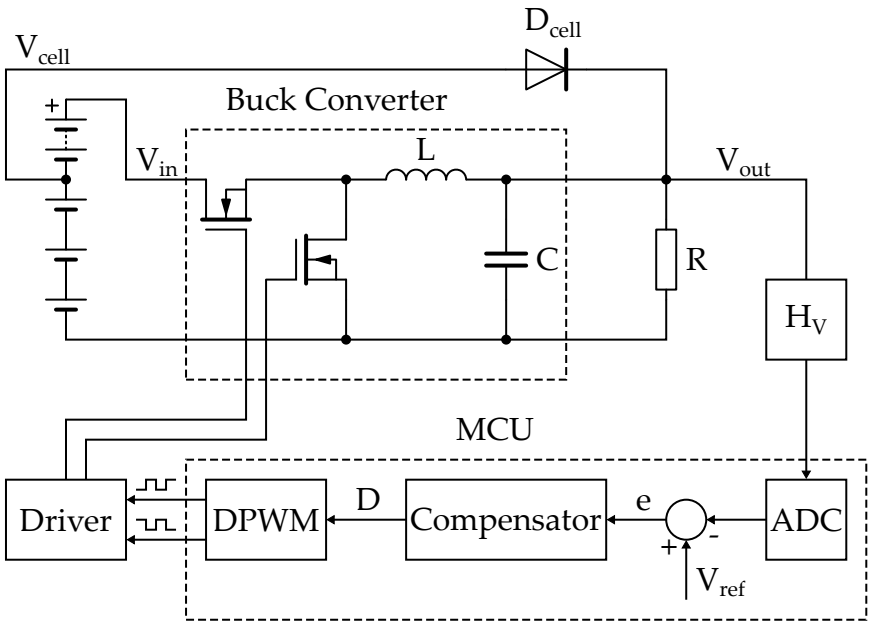


Figure 3.1: System overview

due to a better carrier mobility factor. Furthermore, the availability of n-channel MOSFET is much higher with reduced costs. To turn ON the n-channel MOSFET the gate source voltage V_{GS} has to be above the threshold voltage V_{th}. When the high-side MOSFET is fully turned ON the potential of the source is approximately the same as the input voltage V_{in}. Therefore, the potential at the gate has to be higher than the highest potential of the system and a charge pump or bootstrap driver IC is necessary. The circuit of a bootstrap driver for a pre-biased buck converter is shown in figure 3.2. A bootstrap capacitor C_{boot} is charged to approximately V_{out} when the low-side switch is ON. When the high-side switch is ON, the potential at point A of C_{boot} rises as well as the potential at point B due to the characteristic of a capacitor. In case of the non-synchronous buck converter, where the switch S is realised as a diode, at initial start-up C_{boot} can not be charged because the output is pre-biased with the first three cell voltage V_{cell}. A solution could be to use an additional switch to load C_{boot} before the first switching cycle. With a synchronous buck converter this start-up problem do not exist as the low-side MOSFET can be used to charge C_{boot}.

Comparison

Below the arguments against (–) and for (+) a synchronous topology are listed.

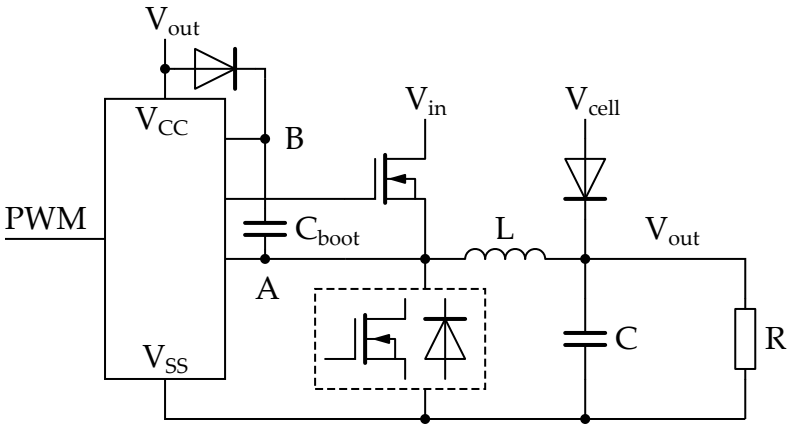


Figure 3.2: Bootstrap high-side driver circuit

- higher cost: high- and low-side driver IC, additional MOSFET is more expensive than Schottky diode
- dead-time implementation necessary to avoid shoot-through
+ no problem at start-up
+ transient performance in CCM better compared to DCM
+ compensator design is easier because buck converter always operates in CCM

The inductor and switching frequency of the non-synchronous buck converter can be selected in a way, that it also just operates in CCM and never enters DCM. Due to the start-up problem and the lack of high frequency high-side only driver ICs on the market, a synchronous buck converter topology for the prototype is used.

3.3 Dimensioning

3.3.1 Inductor

The design of a buck converter starts in most cases with choosing the inductor L according to the desired ripple current Δi_L. By reformulation of equation 2.3, the inductance value can be calculated as

$$L = \frac{V_{in} - V_{out}}{\Delta i_L} D T_{sw} \tag{3.1}$$

where the ripple current Δi_L typically is chosen between 25 % to 50 % of $i_{out,max}$.

Table 3.1: Inductor properties for different inductances and form-factors

$L \times W \times H$(mm)	L(µH)	I_{sat}(A)	I_{RMS}(A)	R_{DC}(mΩ)	f_{res}(MHz)
$5.9 \times 6.2 \times 3.3$	100	0.50	0.65	950	11
$7.3 \times 7.3 \times 4.5$	100	0.75	0.79	290	7.5
	220	0.54	0.44	920	5
	470	0.34	0.29	1600	3.2

Choosing a small inductor value results in reduced costs and a smaller PCB footprint due to the smaller form-factor of the inductor. By comparing different shielded and automotive qualified inductors of two manufacturers [1][2]there are two reasonable form-factors available for an inductance range from 100 µH to 470 µH. For both manufacturers the two form-factors are about the same size and have similar properties so that in table 3.1 inductors of just one manufacturer[2] are listed.

There are several important parameters for inductor selection to be considered. The saturation current I_{sat} is the current at which the inductance is reduced by a particular percentage. Usually this value is given for a percentage of 10 %, but this number depends on the manufacturer. A temperature rise of the inductor by a certain temperature due to the current is specified with the current value I_{RMS}. For the inductors listed in table 3.1, I_{RMS} is given for a temperature rise of 40 °C. The self resonant frequency f_{res} is formed by the inductor itself and the parasitic capacitance. Above f_{res} the inductor behaves more like a capacitor. Therefore, the switching frequency should be below f_{res}.

The biggest inductance value of the smaller form-factor is 100 µH for both manufacturers. Using equation 3.1, an inductance value of 100 µH would result in a switching frequency of 1.6 MHz for $\Delta i_L = 0.25 \cdot I_{out,max}$ or 800 kHz for $\Delta i_L = 0.5 \cdot I_{out,max}$. With higher switching frequencies electromagnetic compatibility (EMC) requirements are harder to fulfil due to fast switching of the MOSFETS. Furthermore, switching power loss P_{switch} increases proportional to f_{sw}. Therefore, the minimal cost and footprint savings of the smaller package does not justify the use of such high switching frequencies. I_{sat} and I_{RMS} of the 470 µH inductor from table 3.1 are marginal compared to $I_{out,max}$. Due to the higher current margin and better damping characteristics, which is explained in detail in chapter 4, the smaller inductance value of 220 µF is chosen. For the selected switching frequency $f_{sw} = 400$ kHz, the ripple current is $\Delta i_L = 0.45 \cdot I_{out,max}$. If a non-synchronous buck converter topology would be used, L and/or f_{sw} has to be further increased,

[1]Coilcraft MSS series
[2]Würth WE-PD series

so that $I_{out,crit} = {}^{\Delta i_L}/_2$ is above $I_{out,min}$ for all operating conditions to ensure the buck converter is always operating in CCM.

3.3.2 Output Capacitor

By rearranging equation 3.2 (adapted from [2]) the minimum output capacitor for a desired output ripple voltage Δv_{out} is calculated. Therefore, the minimum capacitor C_{min} for $\Delta v_{out} = 10\,\text{mV}$ and a typical ESR value of a multi-layer ceramic capacitor (MLCC) of $10\,\text{m}\Omega$ is

$$\begin{aligned} C_{min} &= \frac{\Delta i_L}{(\Delta v_{out} - R_{ESR}\Delta i_L)\,8 f_{sw}} = \frac{112.5\,\text{mA}}{(10\,\text{mV} - 10\,\text{m}\Omega \cdot 112.5\,\text{mA}) \cdot 8 \cdot 400\,\text{kHz}} \\ &= 3.96\,\mu\text{F} \rightarrow 4.7\,\mu\text{F}. \end{aligned}$$

$$\Delta v_{out} = \frac{\Delta i_L}{8Cfsw} + R_{ESR}\Delta i_L \tag{3.2}$$

3.3.3 Input Capacitor

The input current of a buck converter is discontinuous and results in very high ${}^{di}/_{dt}$. If this current would be supplied directly from the battery, the parasitic inductance from the path of the battery to the input of the buck converter would result in a significant voltage drop. Therefore, an input capacitor C_{in} with a low ESR is placed as close as possible to the input of the buck converter to provide the high ${}^{di}/_{dt}$. The minimum input capacitor value for a maximum voltage change ΔV_{Cin} across C_{in} can be calculated with equation 3.3 [12]. For a maximum voltage variation of $\Delta V_{Cin,max} = 0.1\,\text{V}$ and a duty cycle of $D = 0.5$ where the value is the highest, C_{in} is chosen with $2.2\,\mu\text{F}$.

$$C_{in,min} = \frac{D\,(1-D)\,I_{out,max}}{\Delta V_{Cin,max} f_{sw}} = \frac{0.5 \cdot (1-0.5) \cdot 250\,\text{mA}}{0.1\,\text{V} \cdot 400\,\text{kHz}} = 1.56\,\mu\text{F} \rightarrow 2.2\,\mu\text{F} \tag{3.3}$$

3.4 Limit Cycle Oscillations

Due to quantization in the digital controller, limit cycle oscillations (LCO) of the output voltage at the steady state can occur. The frequency and amplitude of this LCO is dependent on many parameters like control-bandwidth, open loop gain, sampling frequency or operating point of the buck converter . Conditions to avoid limit cycle oscillations in digitally controlled DC-DC converters have been presented in [13], [14]. One necessary condition to avoid LCO is given by equation 3.4, where G_{DC} is the DC control-to-output voltage gain, q_{DPWM} the DPWM resolution and q_{ADC} the ADC voltage resolution.

$$G_{DC} \cdot q_{DPWM} < q_{ADC}. \tag{3.4}$$

Therefore, the change of the voltage at the ADC input due to the change of one least significant bit (LSB) of the duty cycle should be less than one LSB of the ADC. In other words, this condition ensures that there is an ADC zero error bin for every duty cycle. Using equation 2.5 the DC control-to-output voltage gain G_{DC} is equal to V_{in} in CCM. The duty cycle resolution of the DPWM can be calculated with equation 3.5, where $n, DPWM$ is the DPWM resolution in bits.

$$q_{DPWM} = \frac{1}{2^{n,DPWM}} \tag{3.5}$$

For an up- or down-counter based DPWM unit with a PWM-clock-frequency $f_{PWM,clk}$, the bit-resolution $n, DPWM$ can be calculated with equation 3.6 for a given switching frequency f_{sw}. For an up-and-down counter based DPWM generation, which is necessary to implement the dead-time if no separate dead-time generation unit is implemented in the MCU, the bit-resolution $n, DPWM$ is reduced by one bit.

$$n, DPWM = \frac{f_{PWM,clk}}{f_{sw}} \tag{3.6}$$

Applying equations 3.5 and 3.6 the minimum ADC voltage resolution $q_{ADC,min}$ given by equation 3.4 can be calculated as follows

$$q_{ADC,min} > G_{DC} \cdot q_{DPWM} = V_{in} \frac{1}{2^{n,DPWM}} = V_{in} \frac{1}{\frac{f_{pwmclk}}{f_{sw}}}.$$

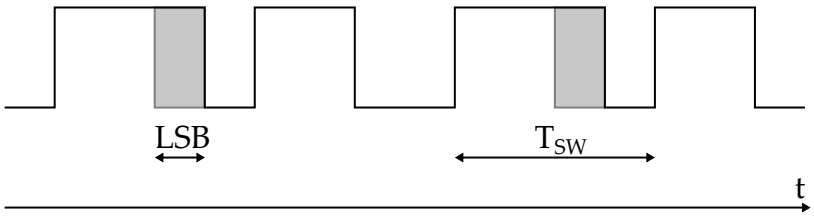


Figure 3.3: Dithering to increase resolution

Table 3.2: Minimum ADC resolution for different switching frequencies to prevent LCO

f_{sw}	100 kHz	200 kHz	400 kHz	800 kHz
$q_{ADC,min}$	75 mV	150 mV	300 mV	600 mV

Table 3.2 shows $q_{ADC,min}$ values for different switching frequencies at the maximum input voltage of 75 V and at a PWM timer frequency of 100 MHz. In case of a $f_{sw} = 400\,kHz$ a minimal ADC resolution of 300 mV is too high and leads to an inaccurate output voltage and worse performance as the controller can not react to small output changes. To minimize $q_{ADC,min}$ there are several possibilities.

- increase the PWM timer frequency f_{pwmclk}
  not possible because the maximum timer frequency of the target MCU is limited to 100 MHz
- use of an external PWM-IC with higher resolution
  unacceptable due to the increase of cost, components and PCB area
- decrease switching frequency
  unacceptable as lower switching frequencies lead to higher inductance values
- increase resolution of DPWM unit using dithering
  possible to increase the DPWM-resolution by some bits

As can seen from the list above, just the method of dithering would be an acceptable solution for this special case. The principle of dithering is to vary the LSB with a pattern over some switching cycles and to average it to increase the effective resolution. The averaging in a buck converter is done with the *LC* output filter. Therefore, the increase of resolution is limited by the *LC* output filter. Figure 3.3 shows the basic principle of dithering to increase the resolution by one bit.

In [13] a software implementation method of dithering using lookup tables is presented. A disadvantage using dithering is the additional delay, as the value of the current LSB has to be loaded with every switching cycle.

Even if the conditions to avoid limit cycle oscillations are met, these oscillations still can occur in specific operating points [15]. To ensure the amplitude and frequency of these limit cycle oscillations stay within the requirements and do not compromise the desired performance, simulations including the quantization of the ADC and DPWM unit are important.

3.5 Digital Controller Design

3.5.1 Selection of Sampling Frequency

The selection of the sampling frequency f_{samp} is a very important step in the digital controller design. Setting f_{samp} too low, would result in high phase reduction in the control loop and can cause aliasing effects in the sensed signal. On the other hand, an unnecessary high sampling frequency leads to increased computational effort, as the control algorithm is executed more frequent.

Phase Decrease of Sample and Hold

The ADC combined with the DPWM unit acts like a sample and hold circuit. The time delay due to the sample and hold can be expressed with equation 3.7 [16], where T_{samp} is the sampling period.

$$G_{SH}(s) = \frac{1 - e^{-sT_{samp}}}{s} \tag{3.7}$$

Figure 3.4 shows the bode plot of $G_{SH}(s)$ for a sampling frequency f_{samp} of 400 kHz. With frequencies close to f_{samp}, the phase starts to drop significantly. The additional phase margin reduction of the open loop transfer function at the cut-off frequency f_c can be calculated with equation 3.8 [17]. Therefore, f_{samp} should be at least 10 times higher than f_c so that the additional phase margin reduction is below 18°.

$$\Delta\varphi = -180° \frac{f_c}{f_{samp}}. \tag{3.8}$$

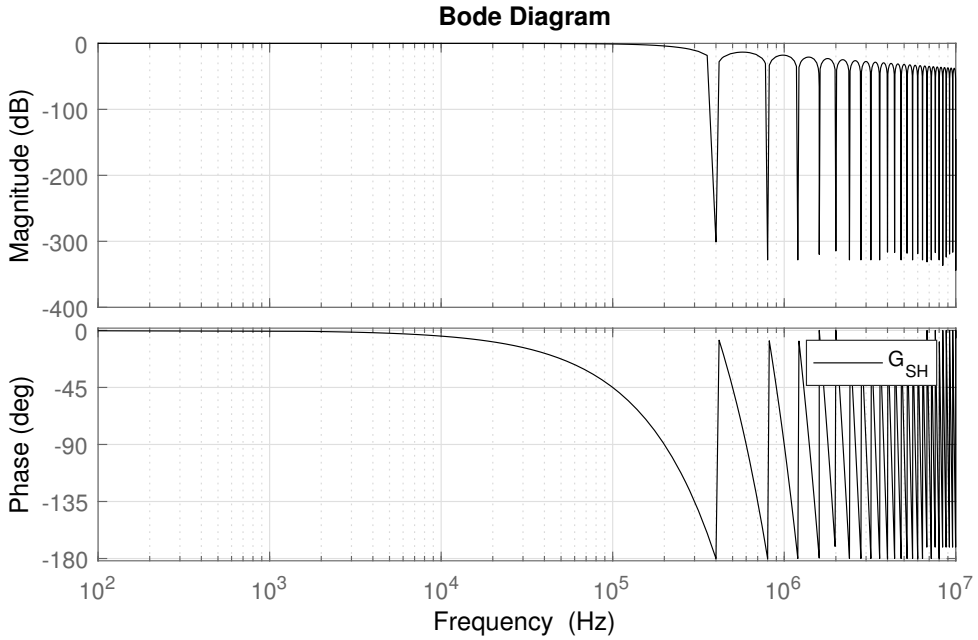


Figure 3.4: Bode diagram of sample and hold with a sampling frequency of 400 kHz

Aliasing

The Nyquist-Shannon sampling theorem implies that in order to sample a band-limited signal without loss of information it has to be sampled at least with twice the frequency of the maximum occurring frequency. In equation 3.9 f_N is the maximum occurring frequency which is also referred as the Nyquist frequency and the frequency which the sampling frequency has to exceed is called the Nyquist rate [18].

$$f_{samp} \geq 2f_N. \tag{3.9}$$

For frequencies above half the sampling frequency aliasing effects occur in the sensed output voltage signal. The high frequency switching ripple at the output would require a high sampling frequency way above the switching frequency to do not violate the Nyquist-Shannon sampling theorem. As just the main dynamic behaviour of the buck transistor is relevant for the control system, this switching ripple has to be filtered with a low-pass filter in the feedback path. To overcome this additional filtering the ADC can be synchronized with the DPWM module in order to sample the signal each time at the same time relative to the switching event. In figure 3.5 this synchronized sampling is illustrated. The

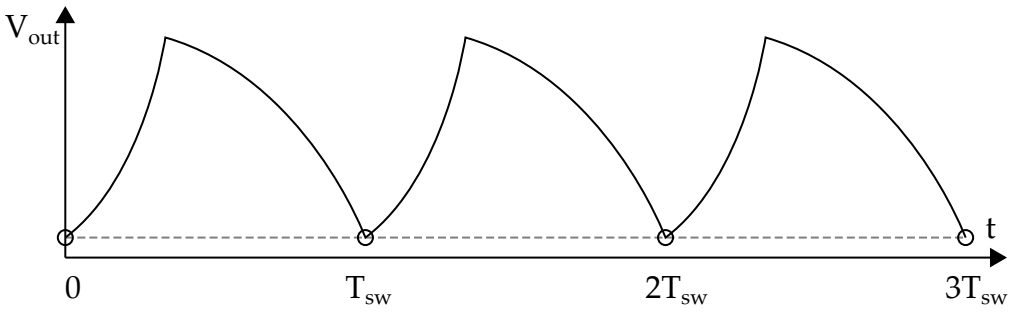


Figure 3.5: Synchronized sampling

sampling frequency should be chosen in such a way that the switching frequency f_{sw} is an integer multiple of the sampling frequency f_{samp} like in equation 3.10

$$Mf_{samp} = f_{sw} \qquad (M \in \mathbb{N} \setminus \{0\}) \tag{3.10}$$

3.5.2 Digital Design Methods

Basically there are two design methods to design a digital compensator: *digital redesign* and *direct digital design* [16].

Digital Redesign

In *digital redesign*, also called emulation method, the controller is designed in the s-domain and is then transferred into the z-domain using one of the discretization approximation methods. This has the advantage that the compensator can be designed with familiar frequency response design methods like bode plot for instance. Unfortunately, this method neglects the sample and hold action formed by the ADC and PWM as well as the time delay t_d between the start of the ADC conversion until the duty cycle update takes affect. Therefore, the additional reduction of the phase margin is not taken into account for compensator design which leads to worse performance or even an unstable system.

Direct Digital Design

With the *direct digital design* approach the plant is discretized at first. For the buck converter where the DPWM acts like a sample and hold, the zero-order hold (ZOH)

method given by equation 3.11 delivers good results, where $\mathcal{Z}$ represents the standard z-transform.

$$\mathcal{Z}\left[\frac{1-e^{-sT_{samp}}}{s}G(s)\right] \tag{3.11}$$

Afterwards the digital controller can be designed directly in the z-domain using appropriate methods available for the z-plane like root locus method. This has the advantage that poles and zeros of the compensator can directly be placed to match the discretized system and are not distorted from the desired position like in digital redesign.

In order to design the compensator with frequency response design methods in direct digital design, the discretized plant $G(z)$ has to be transferred into the w-plane using the following bilinear transformation method:

$$G(w) = G(z)\Big|_{z=\frac{2+Tw}{2-Tw}}.$$

After the compensator is designed in the w-plane with the well-known design methods, the compensator has to be transferred back into the z-plane:

$$G(z) = G(w)\Big|_{w=\frac{2}{T}\frac{z-1}{z+1}}. \tag{3.12}$$

In [8] another design method was proposed to combine digital redesign and direct digital design method with the support of computer-aided design software tools. In this method the bode plot of a discrete function is generated using $z = e^{jwT_{samp}}$. Therefore, the controller can be designed conveniently using frequency response design methods like in digital redesign with the important advantage that the sample and hold action as well as the time delay t_d is considered. In chapter 3.5.4 the use of this combined method is shown with the use of MATLAB®.

3.5.3 Stability

To determine if a linear time-invariant (LTI) system is bounded-input bounded-output (BIBO) stable, the Nyquist Criterion can be used which is a graphical method using a Nyquist plot. If the open loop transfer function $G_{open}(s)$ fulfils the properties listed below [19], the stability proof simplifies and can be determined from the bode plot of $G_{open}(s)$.

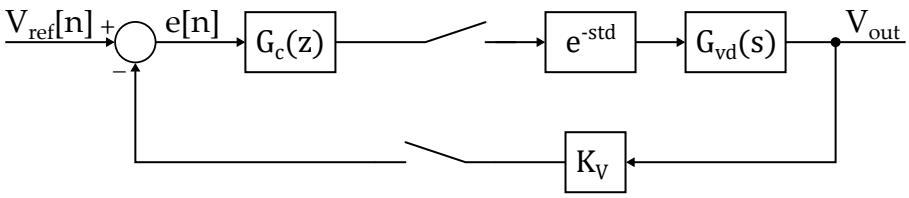


Figure 3.6: Controller block diagram

- $G_{open}(s)$ exhibits a low-pass characteristic ($\lim_{s\to\infty} G_{open}(s) = 0$)
- $G_{open}(s)$ has positive gain
- $G_{open}(s)$ has no right half plane (RHP) poles expect an eventual single pole at 0
- There is only one frequency, called the cross-over frequency w_c, where the magnitude of $G_{open}(jw)$ is equal to 1 for $w \geq 0$

In order to use this simplified method the phase margin φ_M has to be defined as the phase distance between $\angle G_{open}(jw)$ and 180° at the cross-over frequency.

$$\varphi_M = \angle G_{open}(jw_c) + 180° \tag{3.13}$$

If the four listed requirement apply to $G_{open}(s)$, the system is BIBO stable if the phase margin φ_M is positive.

3.5.4 Digital Compensator Design

For the digital compensator design the combined design method described in section 3.5.2 is applied. Figure 3.6 shows a block diagram of the control system.

$G_c(z)$ is the discrete controller which has to be designed, $G_{vd}(s)$ the control-to-output voltage transfer function from equation 2.5 of the buck converter operating in CCM and K_V the constant feedback gain. The switches should symbolize the sample and hold action from the ADC and DPWM unit.

The computational time t_{calc}, the ADC-conversion time t_{ADC} and the delay due to the DPWM can be considered by one delay block e^{-st_d}, where t_d is the time between the start of the ADC-conversion and the moment when the updated duty cycle takes effect. Depending on the organization of the sampling, calculation and duty cycle update, this time t_d can be different. Figure 3.7 shows the time table for the used digital controller with trailing edge modulation. The output voltage is sensed at the beginning of each modulation period. After the conversion time t_{ADC}, the duty cycle is calculated and updated within the computational time t_{calc}, before the next modulation period starts. Until the updated duty cycle takes

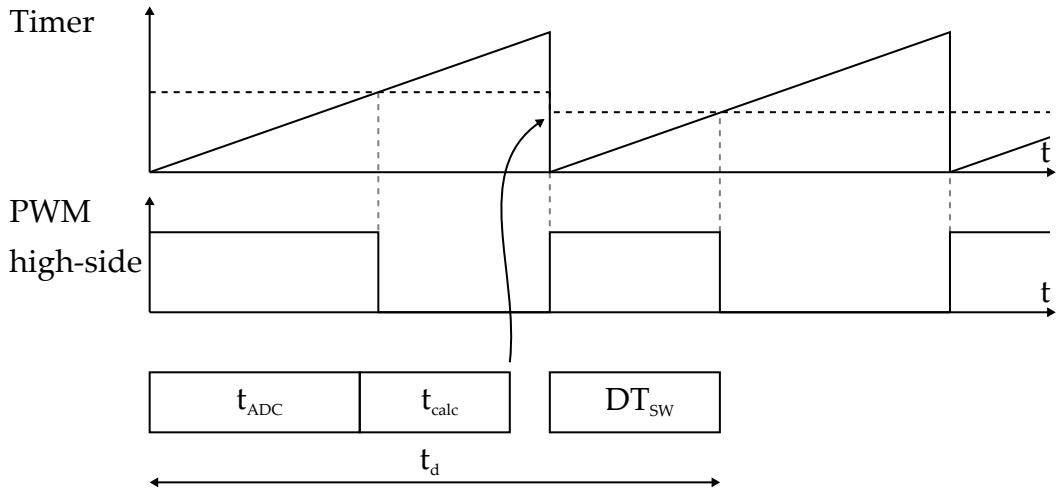


Figure 3.7: Timing diagram

effect an additional time DT_{sw} depending on the duty cycle has to be taken into account. With this timing organization the time t_d results in

$$t_d = T_{sw} + DT_{sw}. \tag{3.14}$$

At first the converter transfer function $G_{vd}(s)$ is discretized using the ZOH method (3.11) including the delay t_d to get $G_{vd}(z)$ 3.15.

$$G_{vd}(z) = \mathcal{Z}\left[\frac{1 - e^{-sT_s}}{s} G_{vd}(s) e^{-st_d}\right] \tag{3.15}$$

The MATLAB® code for a ZOH discretization method with a time delay t_d is shown in listing 3.1. Figure 3.8 shows the effect of the time delay t_d and ZOH on the phase of the control-to output voltage function of the buck converter, where $G_{vd,delay} = G_{vd}(s)e^{-st_d}$.

```
1 G_vd_delay = tf(num,den,'InputDelay',t_d);  % add delay to transfer function
2 G_vd_z = c2d(G_vd_delay, T_s, 'zoh'); % use zoh discretization method
```

Listing 3.1: MATLAB® code to discretize transfer function with an additional delay.

The open loop transfer function G_{open} is given by equation 3.16 and the closed loop transfer function G_{closed} from reference voltage to output by equation 3.17.

$$G_{open}(z) = G_c(z) K_V G_{vd}(z) \tag{3.16}$$

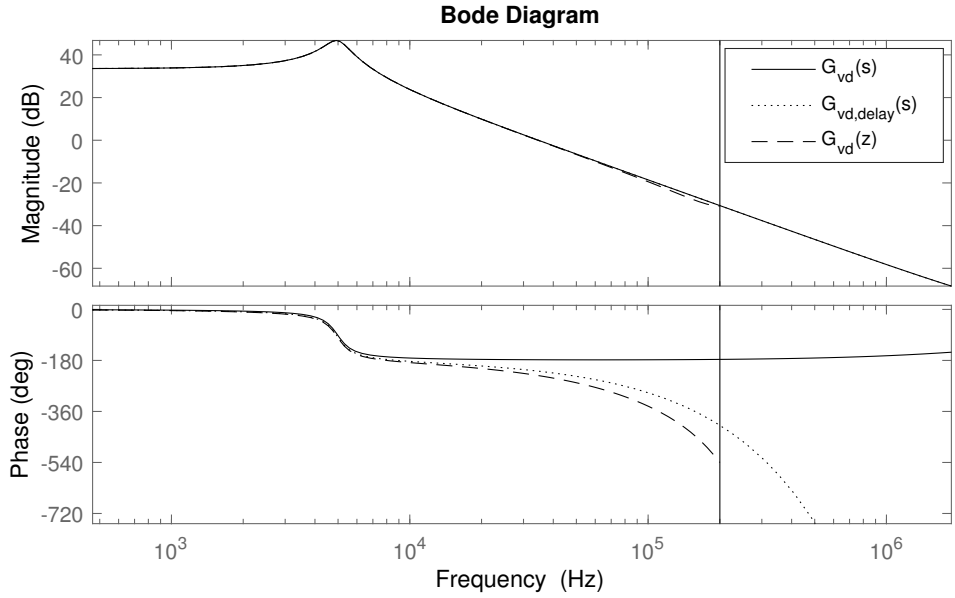


Figure 3.8: Phase reduction due to time delay and ZOH

$$G_{closed}(z) = \frac{\text{forwardpath}}{1 + \text{loop}} = \frac{G_c(z)G_{vd}(z)}{1 + G_{open}(z)} \tag{3.17}$$

In direct digital design the next step would be to either use discrete design methods like root locus method or to transform the discrete transfer function $G_{vd}(z)$ into the w-domain using bilinear transformation methods in order to use frequency response design methods. With powerful software toolboxes as the Control System Toolbox™ from MATLAB®, the discrete controller can be designed directly by visually placing zeros and poles to meet the requirements. Therefore, a bode plot of the discrete transfer function is generated by using the relationship $z = e^{jwT_{samp}}$. In the following, transfer functions mapped from time discrete transfer functions to the continuous time transfer functions using $z = e^{jwT_{samp}}$ are indicated with a prime like $G'(s) = G(z)\big|_{z=e^{jwT_{samp}}}$.

For the VMC buck converter a two-pole-two-zero (2P2Z) compensator is used. The two zeros are placed before the double pole, caused by the LC output filter, to raise the phase. One pole is placed at the origin to reduce steady state error and the second pole is placed about one decade after the cut-off frequency f_c. The bode plot of the compensated open loop transfer function $G'_{open}(jw)$ with a phase margin of $\varphi_M = 42°$ and $f_c = 14.4\,\text{kHz}$ is shown in figure 3.9. For designing $G_c(z)$ the control-to-output voltage transfer function $G_{vd}(s)$ with $V_{in,max}$ and $I_{load,min}$ is used to ensure that the phase margin for all other conditions is higher than the

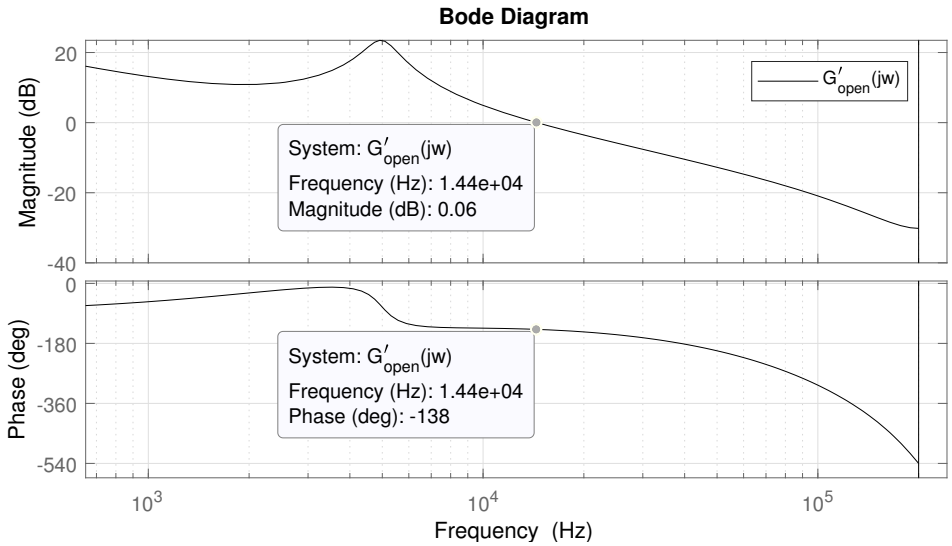


Figure 3.9: Bode plot of $G'_{open}(jw)$

designed one. All of the listed properties in section 3.5.3 are true for $G'_{open}(jw)$ and therefore the positive phase margin is sufficient to ensure BIBO stability.

3.5.5 Controller Implementation

The discrete controller transfer function $G_c(z)$, obtained in the previous section, can be written in the form 3.18, which is often normalized so that $a_0 = 1$. For this second order discrete compensator $N = M = 2$. $E(z)$ is the controller input and $U(z)$ is the controller output. The used coefficients are listed in table 3.3.

$$G_c(z) = \frac{U(z)}{E(z)} = \frac{\sum_{i=0}^{M} b_i z^{-i}}{\sum_{i=0}^{N} a_i z^{-i}} = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{a_0 + a_1 z^{-1} + a_2 z^{-2}} \tag{3.18}$$

For the time domain the discrete transfer function can be written as a difference equation as follow:

$$\frac{y(n)}{x(n)} = \frac{\sum_{i=0}^{M} b_i x\,(n-i)}{\sum_{i=0}^{N} a_i y\,(n-i)}.$$

Table 3.3: Coefficient values for digital compensator

coefficient	value	coffee	value
a_0	1	b_0	3.235
a_1	-1.112	b_1	-6.195
a_2	0.116	b_2	2.965

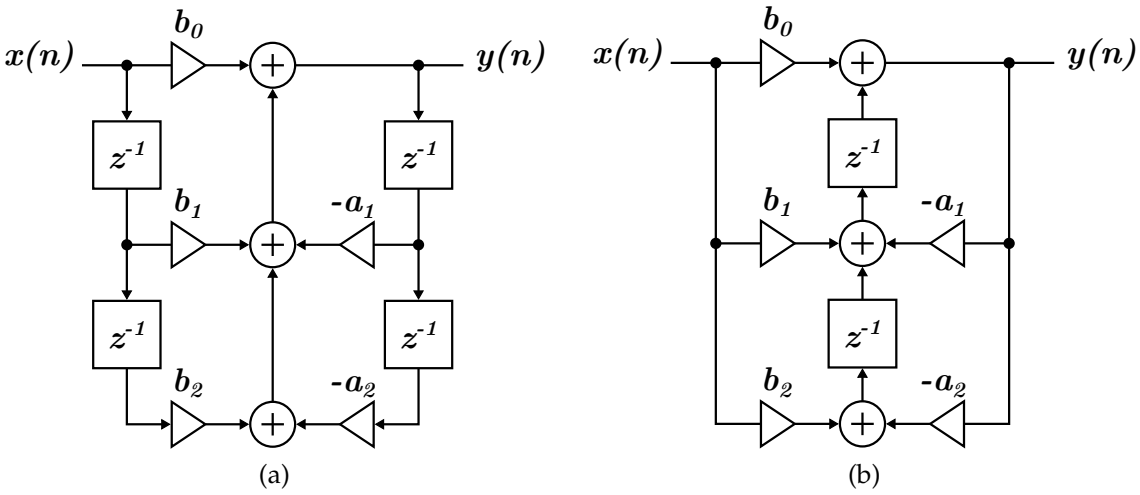


Figure 3.10: Direct form 1 (a) and direct form 2 transposed (b)

where $x(n)$ is the controller input and $y(n)$ is the controller output [18].

Theoretically there are infinite ways to implement this difference equation [18]. A common way to implement it are direct form structures. Figure 3.10 shows the block diagrams of direct form 1 (DF1) and the transposed direct form 2 (DF2). As DF2 only has half the the number of delay elements compared to DF1 and needs less computational time [20], DF2 is used.

3.5.6 Simulation of Digital Compensator

For performance simulation of the designed digital controller the Simulink® model shown in figure 3.11 is used. Figure 3.11a presents the synchronous buck converter with the pre-bias voltage V_{cell}, a variable load and the controller module. The controller subsystem is shown in figure 3.11b. As this model is also used for the unregulated buck in chapter 4 a manual switch is placed to select either the regulated or unregulated purple block. The controller subsystem consists of quantization blocks for the ADC and DPWM, saturation limits for the duty cycle

and the digital compensator. The time delay t_d is realized with a unit delay block z^{-1} and the PWM generator.

In figure 3.12 V_{out} and the duty cycle generated from the digital compensator for maximum load steps are plotted. There is a small steady state error of V_{out} which could be further reduced by a second additional pole at the origin. By simulation at various operating points the LCO addressed in section 3.4 are minimal and barely noticeable. Therefore, no dithering has to be implemented to increase the DPWM resolution.

3.6 Prototype Design

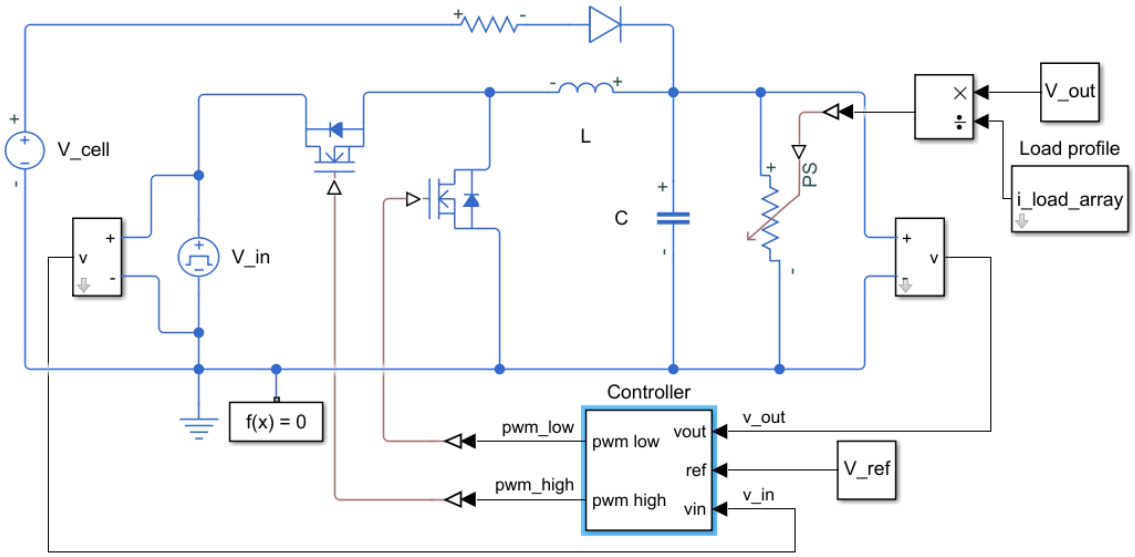
For the prototype design the TMS320F280049 MCU from Texas Instruments was selected because it has similar properties as the MCU used in the BMS. Both MCUs have a 32-bit processor, a floating point unit (FPU), 12-bit ADCs and a maximum PWM clock frequency of 100 MHz.

3.6.1 Analog-to-Digital Converter Design

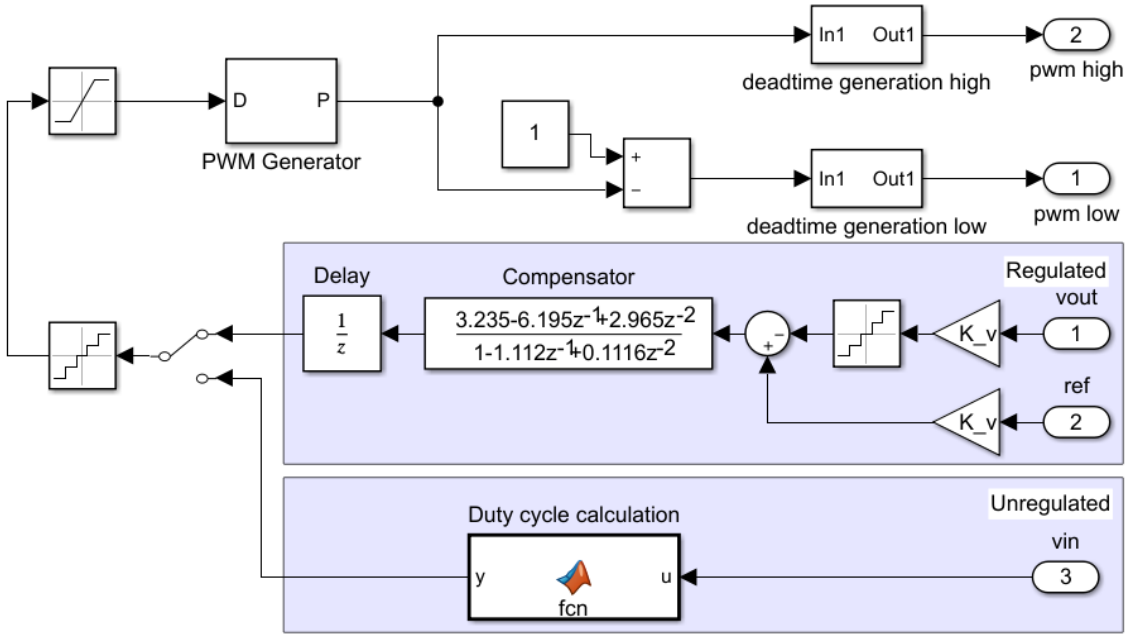
The output voltage is sampled with the sampling frequency f_{samp} to get the present output voltage for each calculation of the control effort. The used ADC is a 12-bit successive approximation-ADC and its sampling process consists of two parts. At the first part a sample and hold circuit is used to load a capacitor for the time $t_{ADC,SH}$ so that the voltage at the capacitor is within the required accuracy. Afterwards, the voltage at the capacitor is determined with the successive approximation-technique within a certain time $t_{ADC,SA}$. Without a prescaler for the ADC-clock, $t_{ADC,SA}$ is equal to 12 system clock cycles and can be calculated as

$$t_{ADC,SA} = 12 \cdot \frac{1}{f_{sys,clk}} = 12 \cdot \frac{1}{100\,\text{MHz}} = 120\,\text{ns}.$$

Therefore, the total ADC conversion time t_{ADC} is the sum of $t_{ADC,SH}$ and $t_{ADC,SA}$ and should be small to minimize the additional delay. As shown in figure 3.7 the sum of the calculation time t_{calc} and t_{ADC} should be smaller than the switching period T_{sw} so that the duty cycle can be updated at the beginning of the next switching period. According to [20] the used function to compute the second



(a) Buck converter



(b) Controller subsystem

Figure 3.11: Simulink® model for the voltage mode controlled and unregulated buck

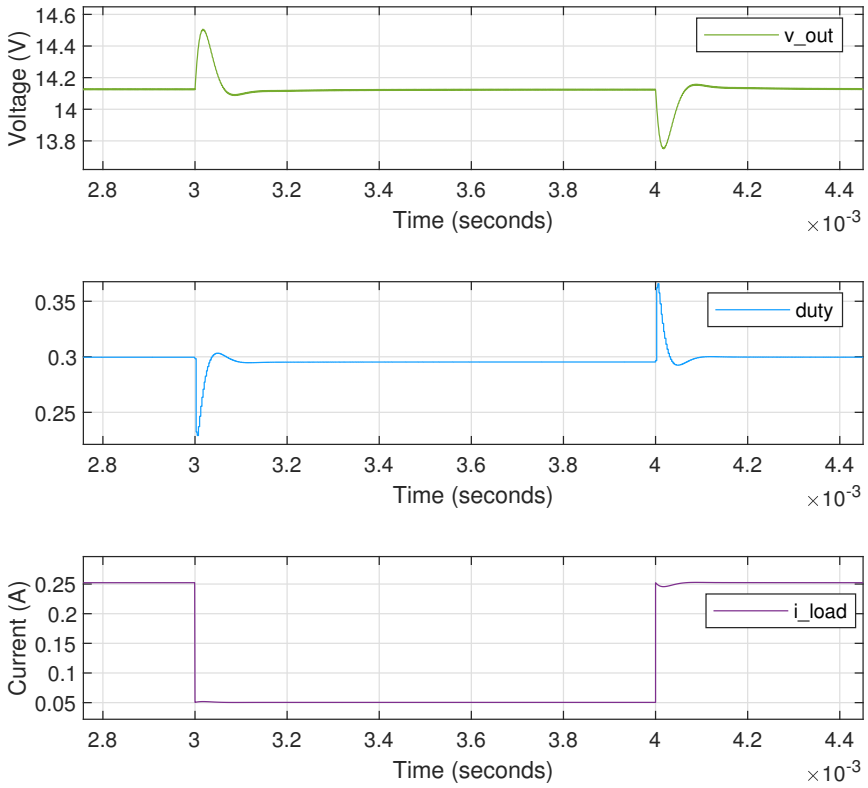


Figure 3.12: Simulation of the voltage mode controlled buck converter with maximum load steps

order control law needs 44 cycles. With a system clock of 100 MHz t_{calc} is 440 ns. Therefore the maximum time $t_{ADC,SH}$ for the sample and hold process is

$$t_{ADC,SH,max} = T_{sw} - t_{calc} - t_{ADC,SA} = 2.5\,\mu s - 440\,ns - 120\,ns = 1.94\,\mu s.$$

To add some margin $t_{ADC,SH}$ is chosen with $T_{sw}/2 = 1.25\,\mu s$.

The single ended ADC input circuit of the TMS320F280049 MCU is shown in figure 3.13. The component values of the ADC from the datasheet [21] are listed in table 3.4. The parasitic capacitance $C_{p,PCB}$ due to the trace from the voltage divider to the input of the ADC is also considered, as it is significant to the relatively small capacitance values of C_p and C_h. This parasitic capacitance can be calculated with equation 3.19.

$$\begin{aligned} C_{p,PCB} &= \epsilon_0 \epsilon_{r,FR4} \cdot \frac{l \cdot w}{d} \\ &= 8.854 \cdot 10^{-12}\,A\,s/(V\,m) \cdot 4.2 \cdot \frac{100\,mm \cdot 0.5\,mm}{0.1\,mm} \approx 20\,pF \end{aligned} \tag{3.19}$$

ϵ... vacuum permittivity
$\epsilon_{r,FR4}$... relative permittivity of FR4 used in PCBs
l... length of trace
w... width of trace
d... distance between layers on PCB

The full-scale range (FSR) of the ADC is 0 V to 3.3 V. Therefore, in order to measure the output voltage it has to be downscaled with a resistor voltage divider network as shown in figure 3.13. If the maximum output voltage $V_{out,max}$ should result to 3 V at the ADC-input, to add some margin, the resistor ratio can be calculated with equation 3.20.

$$\frac{R_2}{R_1 + R_2} = \frac{V_{ADC}}{V_{out,max}} = \frac{3\,V}{15\,V} = 0.2 \tag{3.20}$$

In order to get an accurate output voltage the resistors R_1 and R_2 have to be chosen in a way so that the capacitor C_h is charged to the voltage V_{ADC} with the desired accuracy within $t_{ADC,SH}$.

The output resistance R_{out} of the voltage divider network is $R_1||R_2$. Therefore, the time constant τ can be calculated with equation 3.21

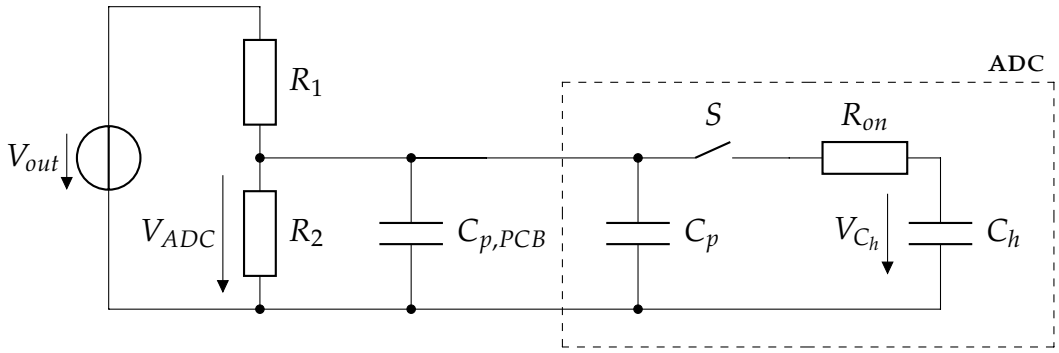


Figure 3.13: Single ended ADC channel input circuit.

Table 3.4: ADC component values

Component	Value
C_p	10 pF
C_h	10 pF
R_{on}	860 Ω

$$\tau = R_{out}\left(C_{p,PCB} + C_p\right) + \left(R_{out} + R_{on}\right) C_h. \tag{3.21}$$

By setting $t_{ADC,SH}$ equal to 5τ, the capacitor C_h is charged up to about 99 %. To add some margin $t_{ADC,SH}$ is set to be 10τ. Now the output resistance R_{out} is calculated with equation 3.22 by rearranging equation 3.21.

$$R_{out} = \frac{\frac{t_{ADC,SH}}{10} - R_{on}C_h}{C_{p,PCB} + C_p + C_h} = \frac{\frac{1.25\,\mu s}{10} - 860\,\Omega \cdot 10\,pF}{20\,pF + 10\,pF + 10\,pF} = 2910\,\Omega \tag{3.22}$$

With equations 3.20 and 3.22 R_1 and R_2 can be calculated as $R_1 = 14.5\,k\Omega$ and $R_2 = 3.6\,k\Omega$. The calculations were verified by simulation and the the end voltage is reached within $t_{ADC,SH} = 1.25\,\mu s$ with the desired accuracy.

3.6.2 Input Filter

In vehicles there are sensitive components like receivers, with the well known frequency modulation (FM) radio receiver, for instance. There are several standards available with defined limits of the EME to prevent electromagnetic interference (EMI) between these components. In order to pass the strict conducted EME limits,

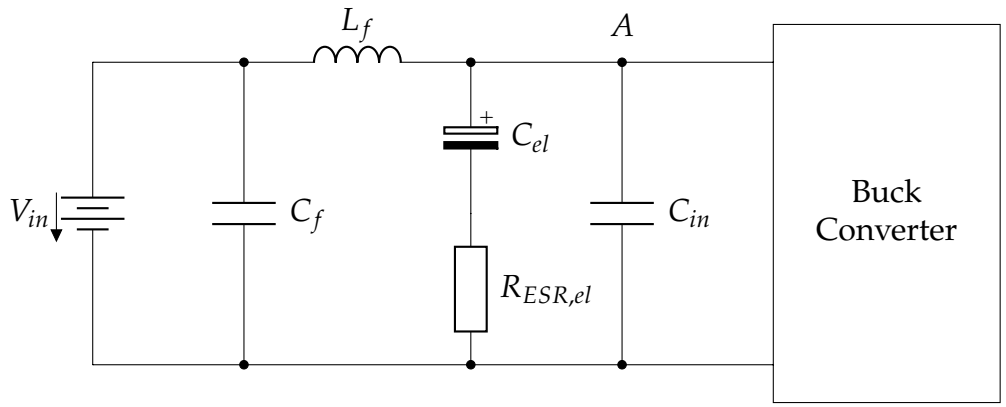


Figure 3.14: Input filter of the buck converter

a LC low-pass filter can be placed to attenuate the conducted switching noise towards the battery. Figure 3.14 shows the input filter with L_f and C_f forming the low-pass filter towards the battery. A way to design this filter is to measure the required attenuation to pass the EMC requirements. The filter components were selected with $L_f = 4.7\,\mu\text{H}$ and $C_f = 4.7\,\mu\text{F}$ so that the cut-off frequency f_c is about one decade before the switching frequency.

It is important that the filter has a low output impedance so that the transfer function of the buck converter is not affected. For AC-analysis the input voltage source can be shorted and L_f and C_{in} are in parallel. Due to the low ESR of C_{in} the quality factor of the LC circuit is high and the output impedance peak seen from point A is high. To damp this output impedance peak at the resonant frequency formed by L_f and C_{in}, an electrolytic capacitor C_{el} with an ESR $R_{ESR,el}$ can be added parallel as shown in figure 3.14 [22]. The quality factor of a parallel RLC circuit can be calculated with equation 3.23 [23].

$$Q = R\sqrt{\frac{C}{L}}. \tag{3.23}$$

Using equation 3.23 and a desired quality factor of $Q = 1$, the value of $R_{ESR,el}$ has to be $1.46\,\Omega$. Figure 3.14 shows the output impedance seen at point A towards the battery of the input filter with and without the electrolytic capacitor.

3.6.3 Printed Circuit Board Layout

Unlike linear regulators, SMPS are known to produce significant EME due to fast switching action. Therefore, the PCB layout of the converter has to be designed

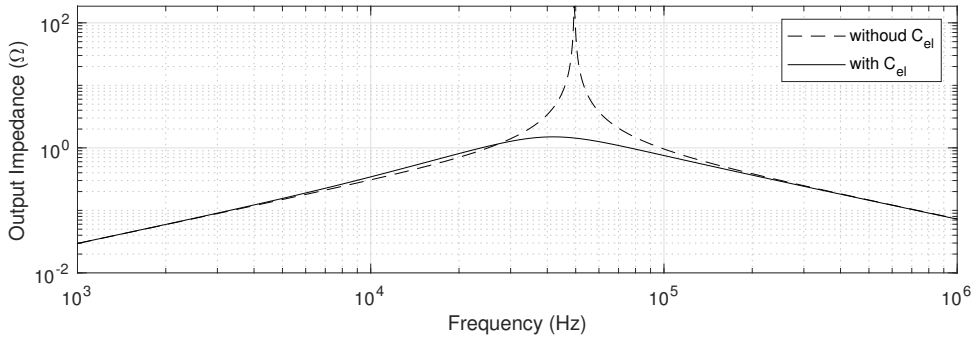


Figure 3.15: Output impedance with and without electrolytic capacitor

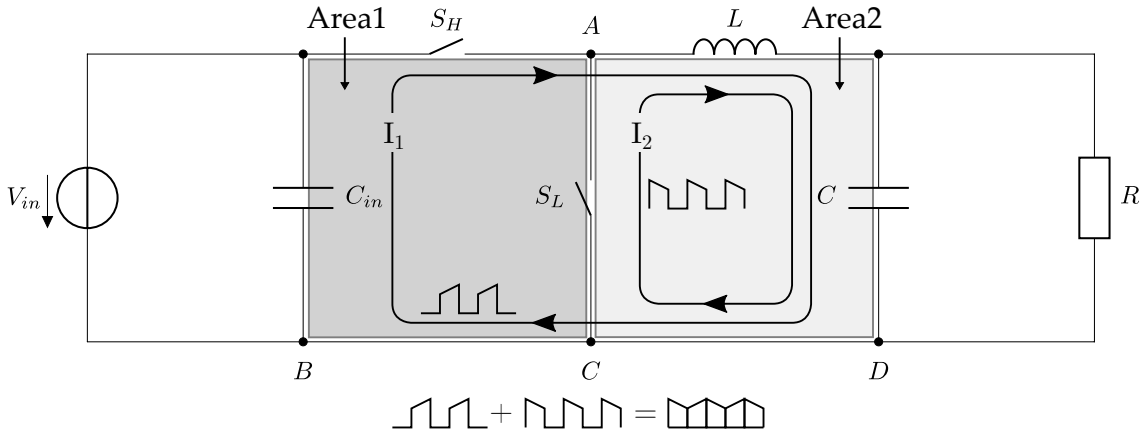


Figure 3.16: Current loops of a buck converter.

carefully to fulfil the EMC requirements. As all components as well as the traces have parasitic inductances one important design rule is to minimize the areas with high di/dt to prevent voltage changes due to $v(t) = L \cdot di/dt$. Figure 3.16 shows the two main current loops I_1 when switch S_H is closed and I_2 when switch S_L is closed of a buck converter. The current I_{in} from the input voltage source and the load current I_{out} are DC-currents due to C_{in} and C and therefore the loops formed by these currents do not have to be small.

For the current path, where the current loops I_1 and I_2 share the same path, the current is continuous but still has high di/dt due to the ripple current of the inductor. The area formed by this continuous current is denoted as $Area2$ in figure 3.16. The current path from C_{in} over S_H and S_L back to C_{in}, where the current loops I_1 and I_2 do not share the same path has *very* high di/dt as the current is discontinuous. Therefore, it is very important to place C_{in} as close as possible to minimize $Area1$ of the discontinuous current path. To prevent ground-bounce the nodes B, C and D should be placed as close as possible.

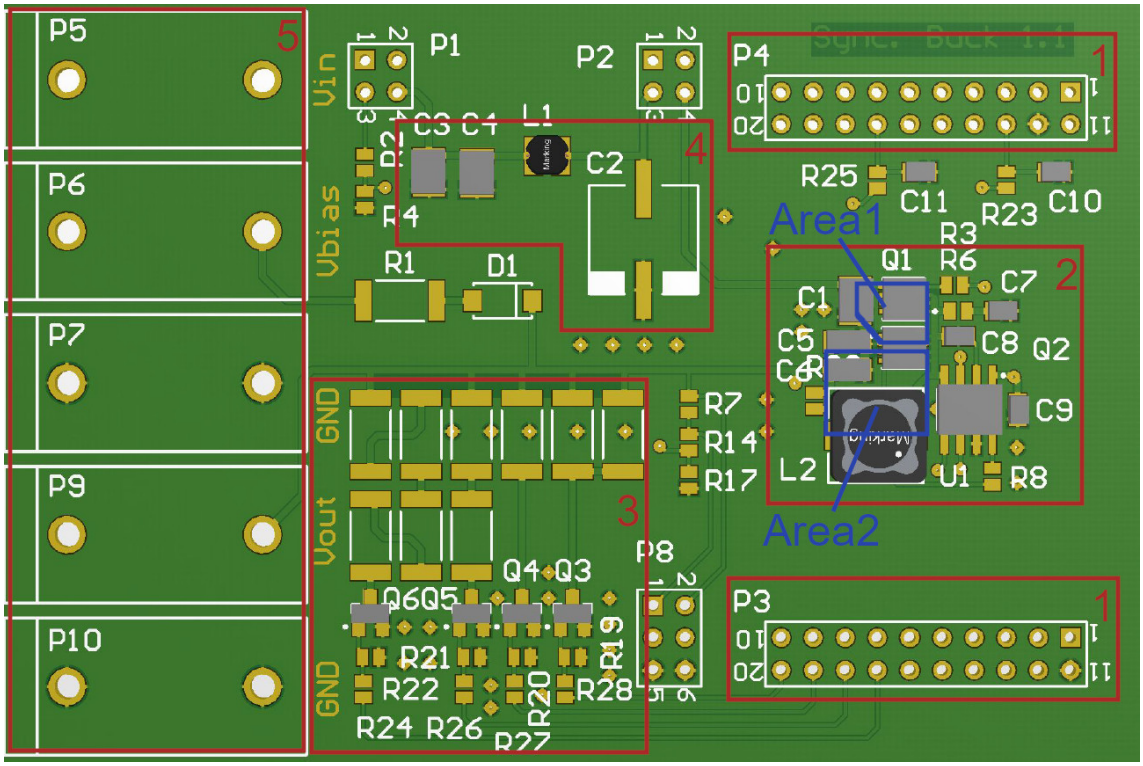


Figure 3.17: Prototype PCB layout (1: connectors to MCU; 2: buck converter with driver-IC; 3: switchable load; 4: input filter; 5: connectors for input-, output- and bias-voltage)

The PCB layout of the prototype buck converter is shown in figure 3.17. Through two pin header connectors(1) the MCU, which is located on a separate evaluation board, is connected to the prototype PCB. Between the connectors the actual buck converter, including the high- and low-side driver-IC (2) is located. The main components of the buck converter are placed so that the two blue indicated areas are minimized. In order to measure the performance of the buck converter to load changes, different output loads (3) can be switched directly by the MCU. The input filter (4) to attenuate the conducted EME is located between the input voltage connector (5) and the buck converter.

3.7 Experimental Results

3.7.1 Conducted Electromagnetic Emissions Measurement

To prove the effectiveness of the input filter, the conducted EME at the positive supply path were measured with the setup shown in figure 3.18. The device under test (DUT) (1) is located on the right with an additional lead-acid battery to provide the pre-bias voltage for start-up and a USB power bank to provide the voltage for the evaluation board and the MCU. The main 48 V supply voltage is provided from a power supply (3) through a line impedance stabilization network (LISN) (2). The LISN, which principal consists of a 5 µH inductor and a 50 Ω resistance formed by the receiver in this case, has several functionalities. It has to supply the DUT and attenuate high-frequency noise from the power supply. Furthermore, it provides a defined impedance and decouples the interference voltage produced by the DUT to the EMI-receiver (4). For this measurement setup, according to EN 55025 (identical to CISPR 25 standard), two LISNs for each supply path are used.

Before the actual measurements, test runs were performed to ensure there are no significant emissions from the environment and the internal DCDC-converter of the power bank. Figure 3.19 shows the measured conducted EME of the buck converter with and without the input filter. A significant attenuation of the conducted EME over the entire frequency range from 150 kHz to 108 MHz is achieved by adding the input filter. The peaks are located at the switching frequency $f_{sw} = 400\,\text{kHz}$ and its harmonics.

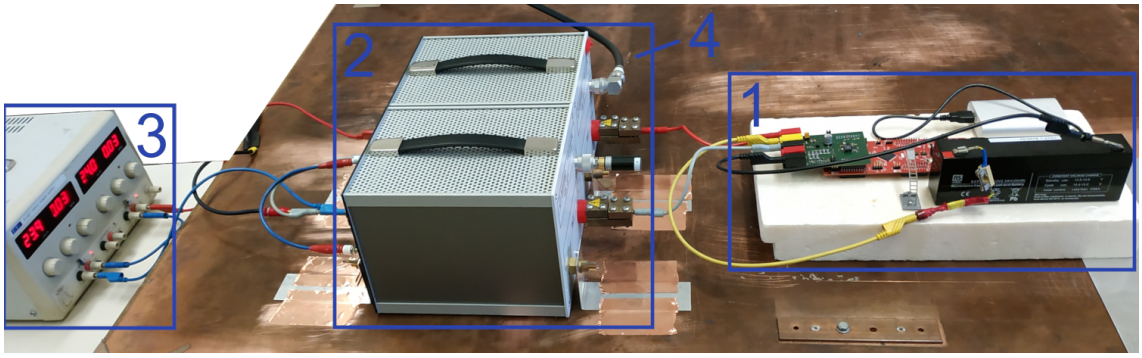


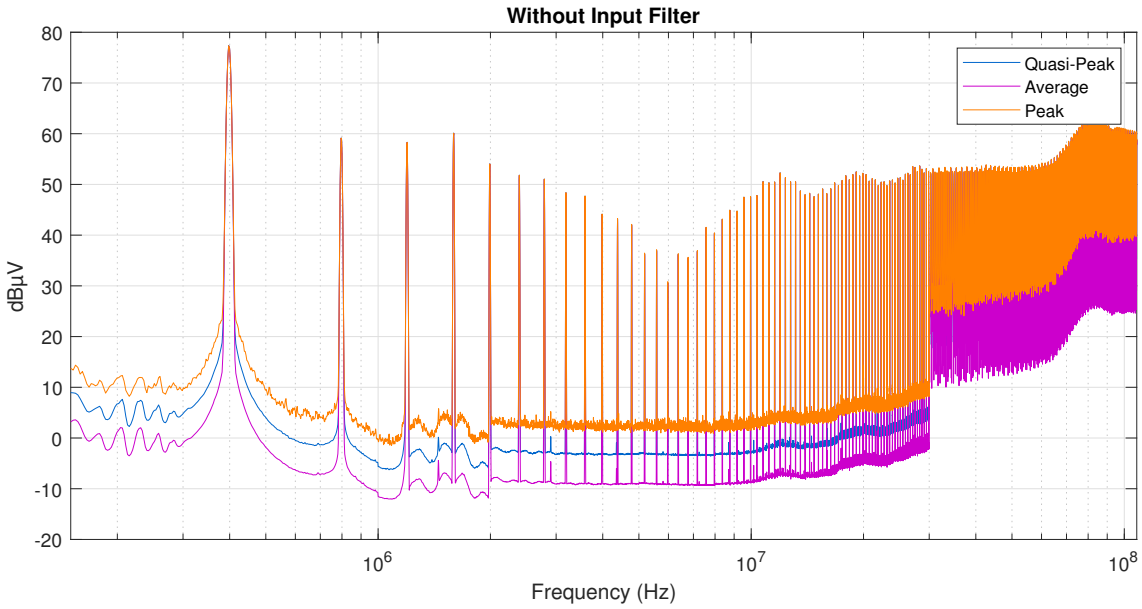
Figure 3.18: Measurement setup for conducted EME (1: DUT; 2: LISN; 3: power supply; 4: cable to EMI-receiver)

3.7.2 Efficiency Calculation and Measurement

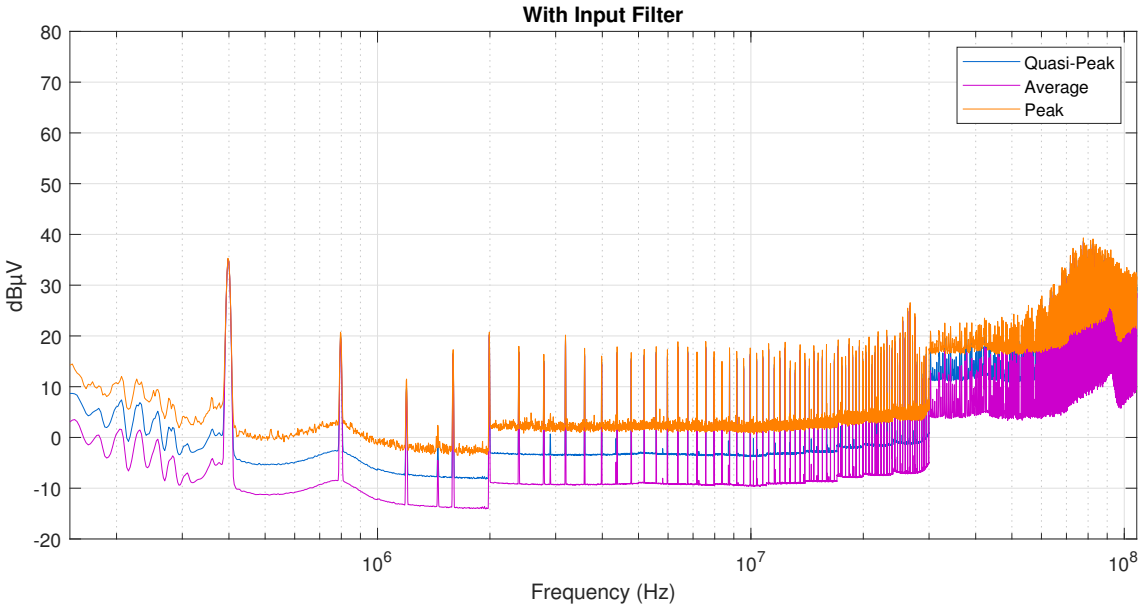
The power losses for the maximum output current $I_{out,max} = 250\,\text{mA}$ are calculated below, using the equations from section 2.4, with the values given in table 3.5. For this synchronous buck converter the same MOSFETs are used for the high- and low-side. Therefore, MOSFET-related values from this table are valid for the high- and low-side transistor. For the power loss calculations the inductor ripple current is neglected and it is assumed that $I_L \approx I_{out}$.

$$
\begin{aligned}
P_{UI,H} &= \frac{1}{2} V_{in} I_L \left(t_{off,H} + t_{on,H}\right) f_{sw} && = 528\,\text{mW} \\
P_{UI,L} &= \frac{1}{2} V_D I_L \left(t_{off,L} + t_{on,L}\right) f_{sw} && = 0.75\,\text{mW} \\
P_{dead} &= 2 V_D I_L t_{dead} f_{sw} && = 30\,\text{mW} \\
P_{RR} &= \left(V_{in} I_L t_{rr} + V_{in} Q_{RR}\right) f_{sw} && = 1380\,\text{mW} \\
P_{COSS} &= \frac{1}{2} \left(C_{OSS,H} + C_{OSS,L}\right) V_{in}^2 f_{sw} && = 80\,\text{mW} \\
P_Q &= Q_G V_{GS} f_{sw} && = 38\,\text{mW} \\
P_{DCR} &= I_{L,RMS}^2 R_{DCR} && = 62.5\,\text{mW} \\
P_{rds,on,H} &= I_{L,RMS}^2 r_{ds,on,H} D && = 0.7\,\text{mW} \\
P_{rds,on,L} &= I_{L,RMS}^2 r_{ds,on,L} (1 - D) && = 1.8\,\text{mW}
\end{aligned}
$$

The calculations above show, that the reverse recovery power loss P_{RR} is significant. In reality this loss should be smaller, as the used values from the datasheet for Q_{RR} and t_{RR} are given for a body diode forward current of 6 A, which is over 20 times more then $I_{out,max}$. Nevertheless, the power losses due to the reverse



(a)



(b)

Figure 3.19: Conducted EME measurement with (b) and without (a) input filter

Table 3.5: Values used for efficiency calculation at $I_{out,max}$.

Symbol	Description	Value
V_{in}	Input voltage	48 V
V_{out}	Output voltage	14 V
V_{GS}	Gate drive voltage of MOSFET driver-IC (datasheet)	≈14 V
D	Duty cycle V_{out}/V_{in}	0.29
R_{DCR}	DCR of inductor (measured)	1.0 Ω
f_{sw}	Switching frequency	400 kHz
t_{dead}	Dead-time to prevent high shoot-through currents	200 ns
V_D	MOSFET body diode forward voltage (datasheet)	0.75 V
C_{OSS}	MOSFET output capacitance (datasheet)	87 pF
Q_{RR}	Reverse recovery charge of MOSFET (datasheet)	61 nC
t_{RR}	Reverse recovery time of MOSFET (datasheet)	44 ns
Q_G	Gate charge of MOSFET (datasheet)	6.8 nC
$r_{ds,on}$	Drain-source ON resistance of MOSFET (datasheet)	40 mΩ
$t_{off,H}$	Turn-OFF switching time (estimated from measurement)	200 ns
$t_{on,H}$	Turn-ON switching time (estimated from measurement)	20 ns
$t_{off,L}$	Turn-OFF switching time (estimated from measurement)	10 ns
$t_{on,L}$	Turn-ON switching time (estimated from measurement)	10 ns

recovery effect can be significant, especially for the quite high input voltage. To reduce P_{RR}, a Schottky diode can be placed in parallel to the body diode of the low-side MOSFET [6]. Schottky diodes are majority carrier devices which do not exhibit the reverse recovery effect. A disadvantage of Schottky diodes is the higher leakage current. Figure 3.20 shows the measured efficiency η for output currents from $I_{out,min} = 50\,\text{mA}$ to $I_{out,max} = 250\,\text{mA}$ at $V_{in} = 48\,\text{V}$ with and without an additional Schottky diode. Using $t_{RR}/5$ and $Q_{RR}/5$ from the datasheet, the calculated efficiency is similar to the measured efficiency.

Especially for higher output currents the efficiency is increased due to the additional Schottky diode. Compared to the internal body diode, the external added Schottky diode has a significant parasitic inductance, even if it is placed directly beside the MOSFET. Therefore, the high di/dt is still provided by the body diode and the reverse recovery effect can not be avoided completely. A MOSFET with a fast integrated diode or a integrated Schottky diode could increase the efficiency as the parasitic inductance is minimized.

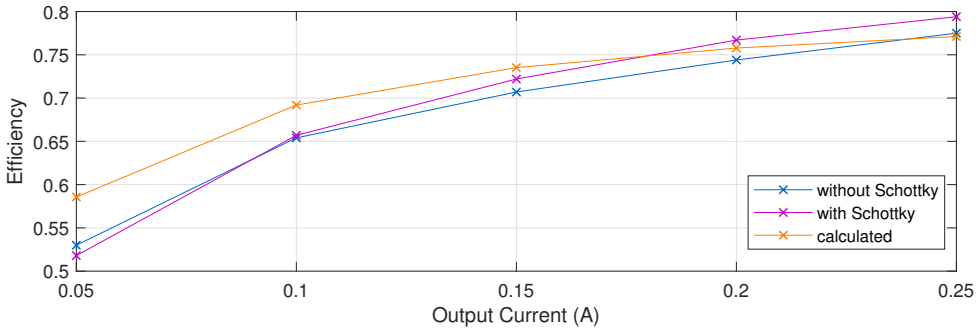


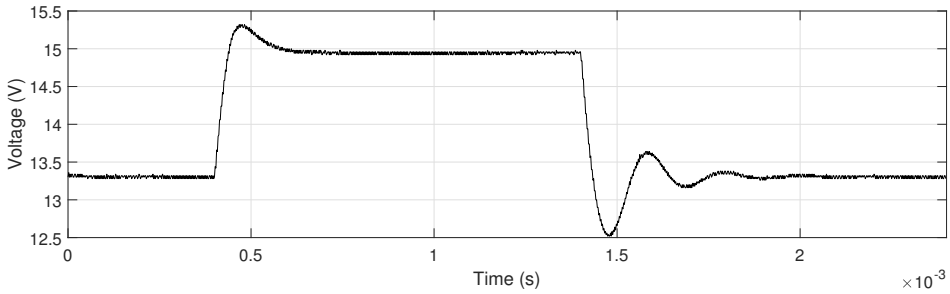
Figure 3.20: Calculated and measured efficiency for different loads with and without an external Schottky diode

3.7.3 Buck Converter Performance

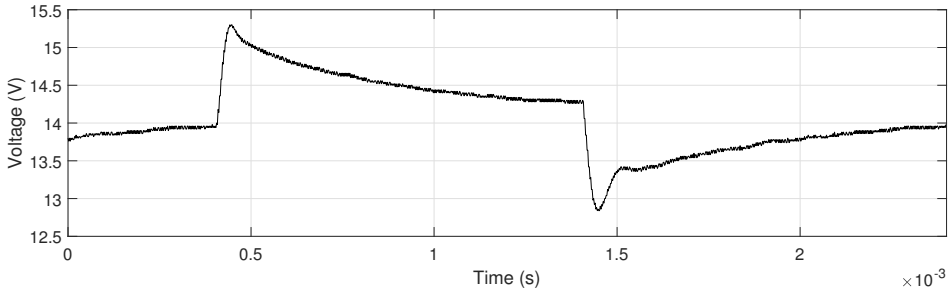
At first the output voltage was measured for the maximum load step from $I_{out,max} = 250\,\text{mA}$ to $I_{out,min} = 50\,\text{mA}$ and back again for a fixed duty cycle. From the measurement result shown in figure 3.21a the steady state output voltage is dependent on the load current and changes by approximately ΔV_{out} =1.6 V for a output current change of ΔI_{out} =200 mA. As the buck converter should be operating in forced-CCM, V_{out} at steady state is only dependent on V_{in} and D and should be load independent. This is only true for an ideal buck converter and due to parasitics like the DCR of the inductor L, I_L causes a voltage drop across L. Nevertheless, the measured DCR of the inductor is $R_{DCR} = 1\,\Omega$ and should theoretically result in just 0.2 V as shown in equation 3.24 instead of the measured 1.6 V.

$$\Delta V_{out} = R_{DCR}\Delta I_{out} = 1\,\Omega \cdot 200\,\text{mA} = 0.2\,\text{V} \tag{3.24}$$

By simulation of the buck converter with the added dead-time, the reason for this unexpected behaviour was identified. Figure 3.22 shows the simulated waveforms for a synchronous buck converter, where V_X is the voltage at the switching node X indicated in figure 2.3. When the inductor current i_L becomes negative the current is supplied by the switched ON low-side MOSFET until the low-side MOSFET is switched OFF at $t = 7\,\text{ms}$. From this moment the negative inductor current is supplied by the body diode of the high-side MOSFET and i_L starts to increase. If the inductor current reaches zero before t_{dead} ends, it stays at zero until the high-side MOSFET is turned ON. In this case the synchronous buck converter operates in a special case of DCM instead of the expected forced-CCM. It is difficult to find a proper dead-time for all operating conditions to avoid entering DCM. Therefore,



(a) fixed duty cycle



(b) regulated

Figure 3.21: Measured output voltage for a load change from 250 mA to 50 mA and vice versa for a fixed duty cycle (a) and with the compensator enabled (b)

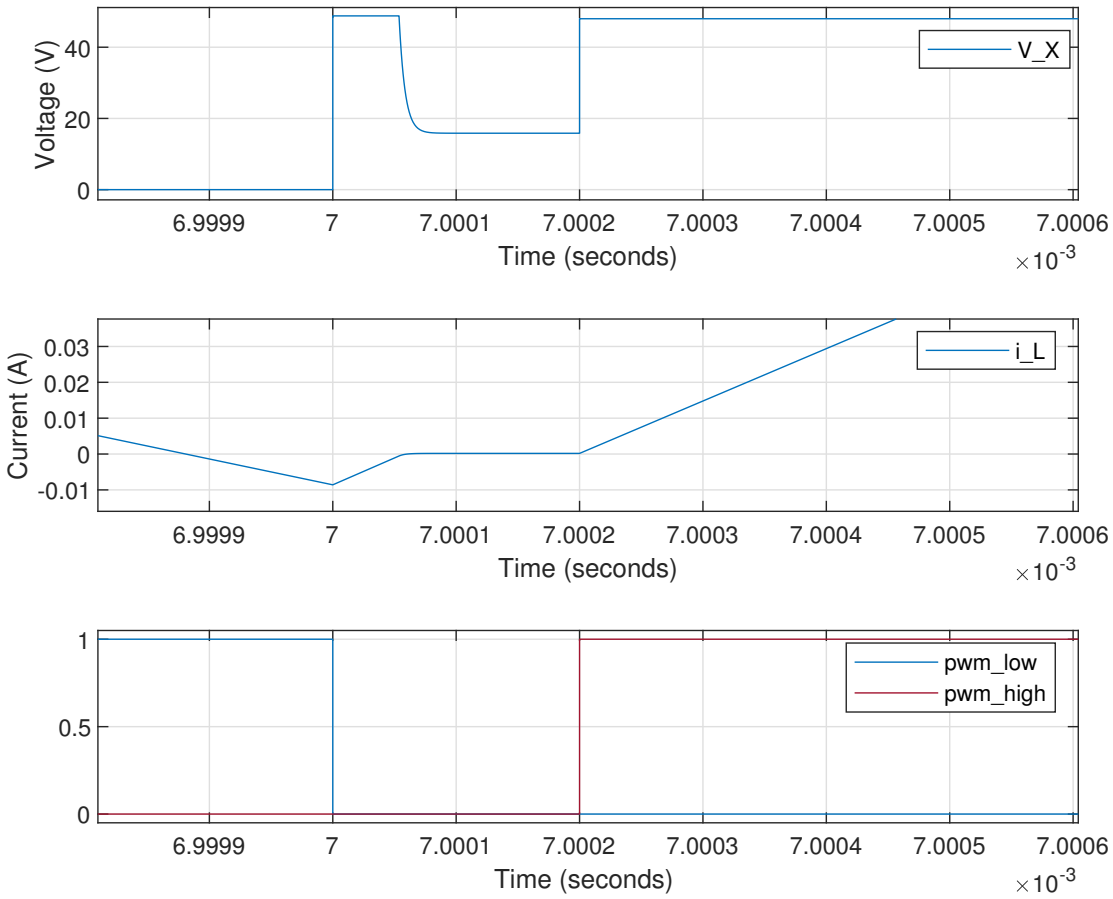


Figure 3.22: Simulation of synchronous buck converter entering DCM due to dead-time

a solution could be either a driver-IC with integrated adaptive dead-time or to design the buck converter so that i_L never becomes negative.

Nevertheless, the performance of the digital compensator was tested by applying the same load step. The measurement result with the digital compensator enabled is shown in figure 3.21b. Compared to the simulation shown in figure 3.12 the measurement differs significantly because the buck converter enters DCM.

4 Unregulated Buck Converter

The basic idea of the unregulated approach is to set the calculated duty cycle D according to the measured input voltage V_{in}, to get the desired output voltage V_{out}, without feedback of V_{out}. In DCM the output-to-input voltage conversion ratio becomes load dependent and is not longer just a function of D. As the MCU has no information about the output current, it has to be ensured that the buck converter is operating in CCM for all operating conditions.

4.1 Dimensioning

The inductor L and capacitor C of the buck converter shown in figure 2.3 have to be designed so that the maximum load change result in a voltage variation within the given specifications. The inductor L and capacitor C with their parasitic resistances R_{DCR} and R_{ESR} are forming a RLC series circuit, if the load resistance R is neglected. To minimize the voltage ripple of V_{out}, a MLCC with a low ESR is used and therefore R_{ESR} can be neglected. The damping ratio ζ of this RLC series circuit is given by equation 4.1. A relatively high ζ is preferred so that the output voltage oscillations caused by load steps or duty cycle changes decay faster. An increased ζ value can be achieved by using an inductor with a relatively high DCR or by placing an additional damping resistor in series to L.

$$\zeta = \frac{R_{DCR}}{2}\sqrt{\frac{C}{L}} \tag{4.1}$$

With a maximum load change simulation the necessary component values are determined, so that the unregulated output voltage stays within $V_{out,min} = 13\,\mathrm{V}$ and $V_{out,max} = 15\,\mathrm{V}$. For a starting point the same inductor value as in chapter 3 is used. Figure 4.1 shows V_{out} for a current load change from $I_{out,max} = 250\,\mathrm{mA}$ to $I_{out,min} = 50\,\mathrm{mA}$ and vice versa for two different setups listed in table 4.1. In order to stay within the given output voltage limits the capacitor value has to be increased to $10\,\mu\mathrm{F}$. The effect of the increased ζ due to the bigger C and R_{DCR} values are significant. The used inductor has already a relatively high DCR with $R_{DCR} = 1\,\Omega$ so that no additional damping resistor is required.

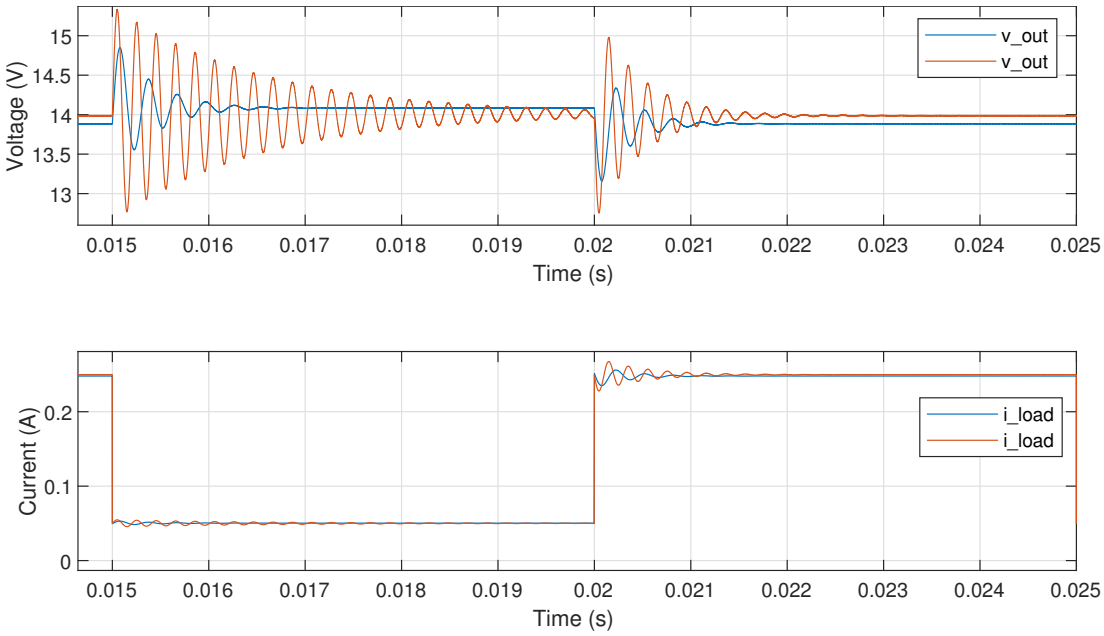


Figure 4.1: Simulation of the output voltage for maximum load steps for different component values

Table 4.1: Simulation setup for unregulated load change

Line colour	R_{DCR}	L	C
orange	0.1 Ω	220 µH	4.7 µF
blue	1 Ω	220 µH	10 µF

Due to the voltage drop above R_{DCR} the desired duty cycle D is not only dependent on V_{in} and V_{out} but also on the output current. Furthermore, the duty cycle offset, due to the added dead-time has to be considered when the duty cycle is calculated as shown in equation 4.2. Due to the low $r_{ds,on}$ of 40 mΩ the voltage drop at the MOSFET is neglected.

$$D = \frac{V_{out} + I_{out}\left(R_{DCR} + R_{damp}\right)}{V_{in}} + \frac{t_{dead}}{T_{sw}} \tag{4.2}$$

The MCU has no information about the output current I_{out} and therefore the duty cycle D is calculated with the arithmetic mean output current $I_{out} = \frac{I_{out,min} + I_{out,max}}{2}$.

4.2 Sampling Frequency

The sampling frequency f_{samp} with which the duty cycle D is calculated and updated from the measured input voltage V_{in}, is dependent on the maximum possible $\Delta V_{in}/\Delta t$. For this buck converter the fastest change of V_{in} is defined in the VDA320 standard with a transient overvoltage from 48 V to 70 V within 1 ms. Figure 4.2 shows V_{out} for the above mentioned V_{in} transient and an additional transient back to 48 V with different sampling frequencies. Furthermore, the maximum load changes are placed at the start of the V_{in} transients to simulate the worst case. For a sampling period $T_{samp} = 100\,\mu s$, the output voltage barely stays within $V_{out,min} = 13\,V$ and $V_{out,max} = 15\,V$. For this simulation the model shown in figure 3.11, with the unregulated purple block selected, was used.

4.3 Measurements

As already mentioned in section 3.7.3 due to a dead-time related issue, the synchronous buck converter of the prototype operates in DCM for small loads instead of forced-CCM. Therefore, the simulations of the maximum load step could not be verified with measurements at the prototype. Nevertheless, the impact of different sampling periods T_{samp} for the maximum input voltage transient from 48 V to 70 V within 1 ms were examined through measurements. Figure 4.3 shows the input voltage transient (red) and the output voltage (blue) for different sampling periods. For sampling periods up to 200 µs the output voltage variation stays within the specifications and significantly overshoots for a sampling period of 400 µs. The measurement results are quite similar to the simulation results

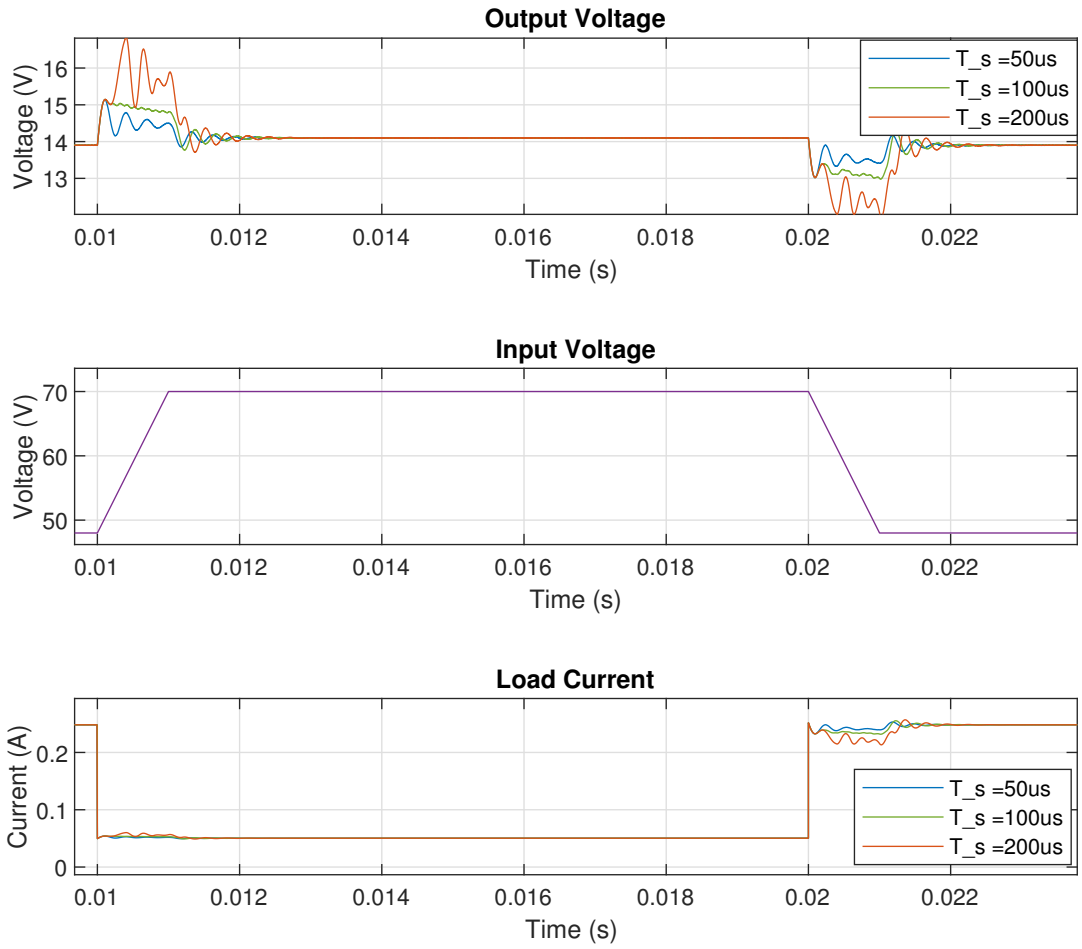
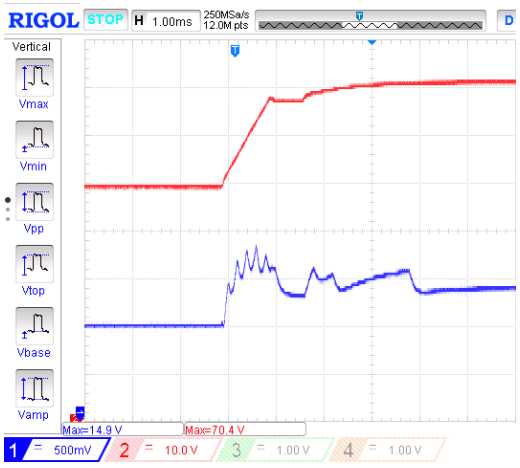


Figure 4.2: Simulation of the output voltage for a maximum input voltage transient and maximum load change for different sampling periods

shown in figure 4.2 expect that the significant output voltage over-shoot of the simulation already occurs at $T_{samp} = 200\,\mu s$.

(a) $T_{samp} = 50\,\mu s$

(b) $T_{samp} = 100\,\mu s$



(c) $T_{samp} = 200\,\mu s$

(d) $T_{samp} = 400\,\mu s$

Figure 4.3: Measured output voltage (blue) at an input voltage transient (red) from 48 V to 70 V within 1 ms for different sampling periods (time: 1 ms/div; Channel 1 (blue): 500 mV/div; Channel 2 (red): 10 V/div)

5 Conclusion

The performance and digital implementation effort of various control schemes for a buck converter have been compared. Fully digital implementations of CMC schemes require two digital compensators which results in increased computational effort for the MCU. Furthermore, a sensing circuit for either the peak or average inductor current is necessary which increases costs. VMC is a one loop control system which can be realised with a minimal count of additional components but comes with the disadvantage that a separate over current protection circuit is needed. Even though the transient performance of VMC is worse than of CMC schemes, simulations of the designed digital compensator revealed that the output voltage requirements can be fulfilled easy for the selected component values. Unfortunately, the simulations of the digital controller could not be confirmed with measurements of the prototype because the synchronous buck converter of the prototype operates in DCM for low loads due to a dead-time related issue.

Due to the relatively high allowed output voltage variations due to the additional SBC after the buck converter, the approach of the unregulated buck converter of chapter 4 turned out to be feasible. The output capacitor has to be increased until the output voltage variation for a maximum load step stay within the required limits. The simulated and measured maximum sampling period, where the duty cycle has to be calculated from the input voltage, is approximately 100 µs for the used component values, to ensure the maximum input voltage transient does not cause the output voltage to exceed the required limits. Compared to the designed VMC compensator of chapter 3 with a sampling period of $1/f_{sw} = 2.5\,\mu s$, the unregulated approach results in much less computational effort for the MCU. The sampling frequency of the VMC compensator could be chosen lower, which would increase the additional phase delay and leads to a more difficult compensator design.

If one of the two addressed approaches would be used for the control of the buck converter in the BMS, further investigation has to be done to ensure the buck converter is always operating in CCM. CCM for the unregulated approach is mandatory and for the voltage mode controlled approach preferable, due to better transient performance. Instead of a driver IC with no built in dead-time

generation, as it is used in this prototype, a driver IC with integrated adaptive dead-time should be used. This ensures that the buck converter always operates in CCM and that the MCU do not have to undertake the dead-time generation. If a bigger inductor value and/or a higher switching frequency is selected, a non-synchronous buck converter could be designed, so that the inductor current never reaches zero. With the use of a non-synchronous topology cost saving can be achieved, with the disadvantage that an additional switch has to be realized to solve the start-up problem of the high-side bootstrap driver IC. In conclusion, the use of a digitally controlled discrete buck converter instead of a dedicated buck controller IC has to be considered carefully.

Bibliography

[1] T. W. Martin and S. S. Ang, "Digital control for switching converters," in *1995 Proceedings of the IEEE International Symposium on Industrial Electronics*, vol. 2, Jul. 1995, 480–484 vol.2. DOI: 10.1109/ISIE.1995.497232 (cit. on p. 1).

[2] R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*, 2nd ed. Kluwer Academic Publishers, 2001, 883 pp., ISBN: 0-306-48048-4 (cit. on pp. 6, 7, 10, 17, 18, 25).

[3] V. Vorperian, "Simplified analysis of PWM converters using model of PWM switch. Continuous conduction mode," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 26, no. 3, pp. 490–496, May 1990. DOI: 10.1109/7.106126 (cit. on p. 8).

[4] C. W. Deisch, "Simple switching control method changes power converter into a current source," in *1978 IEEE Power Electronics Specialists Conference*, Jun. 1978, pp. 300–306. DOI: 10.1109/PESC.1978.7072368 (cit. on p. 12).

[5] A. Capel, G. Ferrante, D. O'Sullivan, and A. Weinberg, "Application of the injected current model for the dynamic analysis of switching regulators with the new concept of LC^3 modulator," in *1978 IEEE Power Electronics Specialists Conference*, Jun. 1978, pp. 135–147. DOI: 10.1109/PESC.1978.7072346 (cit. on p. 12).

[6] M. Kazimierczuk, *Pulse-width modulated DC-DC power converters*, 2nd ed. John Wiley & Sons Inc, 2015, 960 pp., ISBN: 978-1-119-00954-0 (cit. on pp. 12, 19, 48).

[7] M. Hallworth and S. A. Shirsavar, "Microcontroller-Based Peak Current Mode Control Using Digital Slope Compensation," *IEEE Transactions on Power Electronics*, vol. 27, no. 7, pp. 3340–3351, Jul. 2012. DOI: 10.1109/TPEL.2011.2182210 (cit. on p. 13).

[8] D. He, "Microcontroller-based current-mode control for power converters," PhD thesis, Auburn University, Dec. 16, 2005. [Online]. Available: https://etd.auburn.edu/bitstream/handle/10415/328/HE_DAKE_26.pdf (visited on 02/25/2019) (cit. on pp. 13, 31).

[9] L. Dixon, "Average Current Mode Control of Switching Power Supplies," *Unitrode Power Supply Design Seminar*, 1990. [Online]. Available: https://e2echina.ti.com/cfs-file/__key/telligent-evolution-components-attachments/13-112-00-00-00-00-44-35/Average-Current-Mode-Control-of-Switching-Power-Supplies.pdf (visited on 05/15/2019) (cit. on p. 15).

[10] S. He and R. M. Nelms, "Comparison of three implementations of digital average current control for dc-dc converters," in *IECON 2014 - 40th Annual Conference of the IEEE Industrial Electronics Society*, Oct. 2014, pp. 1337–1342. DOI: 10.1109/IECON.2014.7048675 (cit. on p. 15).

[11] *Efficiency of Buck Converter*, version Rev.001, ROHM Semiconductor GmbH, 2016. [Online]. Available: http://rohmfs.rohm.com/en/products/databook/applinote/ic/power/switching_regulator/buck_converter_efficiency_app-e.pdf (visited on 05/13/2019) (cit. on p. 19).

[12] M. Xie, *How to select input capacitors for a buck converter*, Texas Instruments Inc., 2016. [Online]. Available: http://www.ti.com/lit/an/slyt670/slyt670.pdf (visited on 05/13/2019) (cit. on p. 25).

[13] A. V. Peterchev and S. R. Sanders, "Quantization resolution and limit cycling in digitally controlled PWM converters," *IEEE Transactions on Power Electronics*, vol. 18, no. 1, pp. 301–308, Jan. 2003. DOI: 10.1109/TPEL.2002.807092 (cit. on pp. 26, 27).

[14] H. Peng, A. Prodic, E. Alarcon, and D. Maksimovic, "Modeling of Quantization Effects in Digitally Controlled DC-DC Converters," *IEEE Transactions on Power Electronics*, vol. 22, no. 1, pp. 208–215, Jan. 2007. DOI: 10.1109/TPEL.2006.886602 (cit. on p. 26).

[15] S. Buso and P. Mattavelli, *Digital control in power electronics*, 2nd ed. Morgan & Claypool Publishers, 2015, 229 pp., ISBN: 978-1-62705-754-7 (cit. on p. 28).

[16] Y. Duan and H. Jin, "Digital controller design for switchmode power converters," in *APEC '99. Fourteenth Annual Applied Power Electronics Conference and Exposition. 1999 Conference Proceedings (Cat. No.99CH36285)*, vol. 2, Mar. 1999, 967–973 vol.2. DOI: 10.1109/APEC.1999.750486 (cit. on pp. 28, 30).

[17] S. Choudhury, *Designing a TMS320F28ox Based Digitally Controlled DC-DC Switching Power Supply*, Texas Instruments Inc., 2005. [Online]. Available: http://www.ti.com/lit/an/spraab3/spraab3.pdf (visited on 05/19/2019) (cit. on p. 28).

[18] A. V. Oppenheim, R. W. Schafer, and J. R. Buck, *Discrete-Time Signal Processing*, 2nd ed. Prentice-Hall Inc., 1998, 870 pp., ISBN: 0-13-754920-2 (cit. on pp. 29, 36).

[19] M. Horn and N. Dourdoumas, *Regelungstechnik, Rechnerunterstützter Entwurf zeitkontinuierlicher und zeitdiskreter Regelkreise*. Pearson Studium, 2004, 457 pp., ISBN: 3-8273-7059-0 (cit. on p. 31).

[20] *C2000 Digital Control Library, User's Guide*, version 3.1, Texas Instruments Inc., Oct. 2018 (cit. on pp. 36, 37).

[21] *TMS320F28004x Piccolo Microcontrollers*, version Rev. D, Texas Instruments Inc., Oct. 2018. [Online]. Available: `http://www.ti.com/lit/ds/symlink/tms320f280049.pdf` (visited on 05/06/2019) (cit. on p. 40).

[22] A. Martin, *AN-2162 Simple Success With Conducted EMI From DCDC Converters*, Texas Instruments Inc., 2013. [Online]. Available: `http://www.ti.com/lit/an/snva489c/snva489c.pdf` (visited on 05/15/2019) (cit. on p. 42).

[23] H. Hartl, E. Krasser, W. Pribyl, P. Söser, and G. Winkler, *Elektronische Schaltungstechnik*. Pearson Studium, 2008, ISBN: 978-3-8273-7321-2 (cit. on p. 42).

Abbreviations

2P2Z two-pole-two-zero

AC alternating current
ACMC average current mode control
ADC analog-to-digital converter

BIBO bounded-input bounded-output
BMS battery management system

CCM continuous conduction mode
CMC current mode control

DAC digital-to-analog converter
DC direct current
DCM discontinuous conduction mode
DCR direct current resistor
DF1 direct form 1
DF2 direct form 2
DPWM digital pulse-width modulation
DSP digital signal processor
DUT device under test

EMC electromagnetic compatibility
EME electromagnetic emission
EMI electromagnetic interference
ESR equivalent series resistor

FM frequency modulation
FPU floating point unit
FSR full-scale range

IC integrated circuit

LCO limit cycle oscillations
LISN line impedance stabilization network
LSB least significant bit

LTI linear time-invariant

MCU microcontroller unit
MHEV mild hybrid electric vehicle
MLCC multi-layer ceramic capacitor
MOSFET metal-oxide-semiconductor field-effect transistor

PCB printed circuit board
PCMC peak current mode control
PWM pulse-width modulation

RHP right half plane

SBC system basis chip
SMPS switched mode power supply

VCMC valley current mode control
VMC voltage mode control

ZOH zero-order hold

Appendix

Transfer function derivations

The series circuit of L and R_{DCR} of figure 2.6 is summarized as Z_1 and $(C + R_{ESR}) \,||\, R$ as Z_2.

$$
\begin{aligned}
Z_1 &= sL + R_{DCR} \\
Z_2 &= \frac{\left(\frac{1}{sC} + R_{ESR}\right) R}{\frac{1}{sC} + R_{ESR} + R} = \frac{R + sRR_{ESR}C}{1 + sC\left(R_{ESR} + R\right)}
\end{aligned}
$$

The control-to-output voltage transfer function is derived in equation .1

$$
\begin{aligned}
G_{vd,CCM}(s) &= \left.\frac{\hat{v}_{out}(s)}{\hat{d}(s)}\right|_{\hat{v}_{in}(s)=0} = V_{in}\frac{Z_2}{Z_1 + Z_2} \\
&= V_{in}\frac{\frac{R+sRR_{ESR}C}{1+sC(R_{ESR}+R)}}{sL + R_{DCR} + \frac{R+sRR_{ESR}C}{1+sC(R_{ESR}+R)}} \\
&= V_{in}\frac{R\left(1 + sCR_{ESR}\right)}{R_{DCR} + R + s\left(L + CR_{DCR}\left(R_{ESR} + R\right) + CR_{ESR}R\right) + s^2LC\left(R_{ESR} + R\right)}
\end{aligned}
\tag{.1}
$$

The control-to-inductor current transfer function is derived similar in equation .2

$$
\begin{aligned}
G_{id,CCM}(s) &= \left.\frac{\hat{i}_L(s)}{\hat{d}(s)}\right|_{\hat{v}_{in}(s)=0} = V_{in}\frac{1}{Z_1 + Z_2} \\
&= V_{in}\frac{1}{sL + R_{DCR} + \frac{R+sRR_{ESR}C}{1+sC(R_{ESR}+R)}} \\
&= V_{in}\frac{1 + sC\left(R_{ESR} + R\right)}{R_{DCR} + R + s\left(L + CR_{DCR}\left(R_{ESR} + R\right) + CR_{ESR}R\right) + s^2LC\left(R_{ESR} + R\right)}
\end{aligned}
\tag{.2}
$$