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Multipurpose Electronic Control Unit for Prototyping, Testing and Verification in Automotive Industry

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Affidavit

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Abstract

Electronic Control Units (ECU) nowadays found in a modern vehicles are subject of huge interests. Development process of these units is time consuming and prone to failures. Research of this master thesis focuses on construction of multipurpose ECU which could be used for rapid prototyping, testing and verification in automotive industry. This unit also supports model based software design with MATLAB Simulink which should increase platform flexibility. Model based approach decrease time to build prototype system, make it versatile to changes and allow engineers to focus more on solution of problem rather than tools to solve it. The study covers design, implementation and verification of the unit.

Zusammenfassung

Elektronische Steuergeräte (ECUs), die heutzutage in modernen Fahrzeugen zu finden sind, sind von großem Interesse. Der Entwicklungsprozess dieser Einheiten ist zeitaufwändig und fehleranfällig. Die Forschung dieser Masterarbeit befasst sich mit dem Entwurf eines Mehrzweck-Steuergeräts, das für schnelles Prototyping, Testen und Verifizierung in der Automobilindustrie verwendet werden könnte. Dieses Gerät unterstützt auch modellbasiertes Softwaredesign mit MATLAB Simulink, wodurch die Zeit für den Aufbau eines Prototyp-Systems reduziert wird. Die Studie umfasst den Entwurf, die Implementierung und die Verifikation des Mehrzweck-Steuergeräts.

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1. Introduction

Nowadays Electronic Control Units (ECUs) in automotive industry are subject of huge interests which aims to replace a mechanical control systems. Typical ECU consists of electronic sensors, actuators and communication buses (Figure 1.2). An example of such system would be combustion engine control unit, where a combustion engine represents technical process. Feedback of a system would be a lambda sensors and fuel injectors and air intake control would be actuators (Figure 1.1). The goal of the ECU is to find optimal parameters given by set point, in this case ideal relation between fuel and air mixture. Of course this example represent simplified model of a engine control unit.

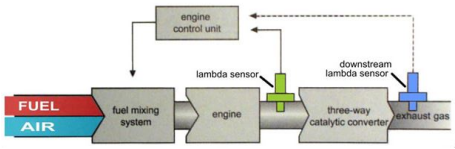


Figure 1.1.: Simplified model of engine control unit [39]

These units are under constant improvement and modifications either by hardware or software means. Secondly, constant demand of vehicle functionality requires development of new ECUs or completely reorganizing existing.

This reorganization requires also development of completely new ECUs as not only software but hardware changes are required. Development of a new ECU is usually expensive and time consuming process, which involves many development phases and it is prone to failures which may not be detected immediately and may appear in later phases of design cycles. Potential problems should be detected and resolved at early stage of development, usually at ”Requirement” or ”Design” phase of development cycle (Figure 1.4).

Having ability to build a prototype hardware at early design phase would have many benefits and some of them would be:

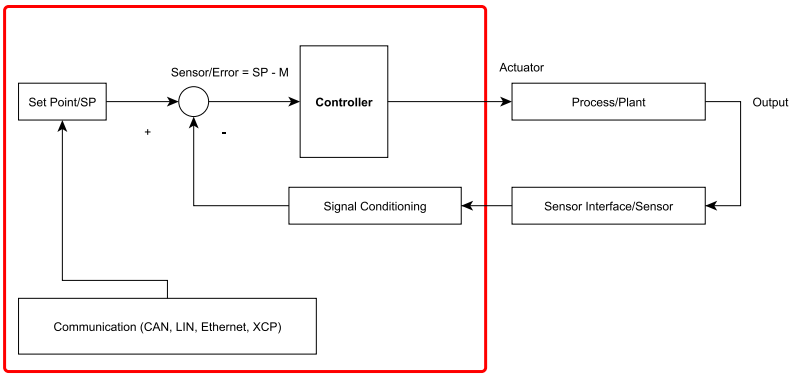


Figure 1.2.: ECU as a part of a control loop

- proof of concept
- address possible hidden design issues
- grouping and assignment of functional groups to ECUs
- early planning of bus topology and communication management

The research of this thesis focuses mainly on design and implementation of a universal ECU unit which could be used in prototyping of automotive ECUs. Beside ECU prototyping, the system proposed in this master thesis could be useful in testing phase of a newly developed ECU for example in a testing phase known as a Hardware-in-the-Loop (HIL). In this phase of a development cycle, newly constructed ECU is tested against its requirements and specifications. Usually test engineers prepare a series of automated test targeting specific requirements/specifications and evaluate them. Figure 1.3 shows typical HIL configuration where Device-Under-Test (DUT) is stimulated and the response of the system is either evaluated directly on a simulator system or sent to a PC for further processing and eventual visualisation.

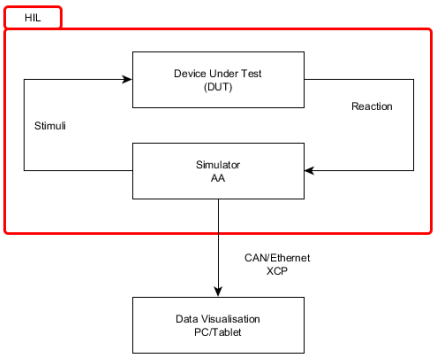


Figure 1.3.: HIL test

Of course this research will not be able to cover all requirements automotive industry could have, but main aspects will be a development of versatile unit which could cover basic requirements of a simple control systems.

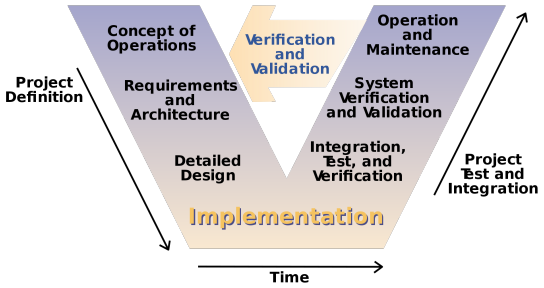


Figure 1.4.: V-Model development process [1]

1.1. Purpose

Most of prototyping and testing equipment of today require continues PC interaction for its functioning. One example of the system that works either as standalone unit or can be PC controlled is a CANextender from "Vector

Informatik". The main features of this system is that it has analog and digital inputs and outputs which are accessible over CAN interface [41]. What this system lacks is its own processing power, meaning that third party system is required to evaluate the measured parameters and to decide if potential interaction on actuators is needed. CAN-Extender is shown in Figure 1.5. Another example would be equipment from "Nation Instruments" which works with LabView and which has many derivatives targeting different problem domains. At the time of writing this master thesis NI equipment is mostly used in a Hardware-in-the-Loop and End-of-Line-Tests. Third example would so called "Beo Box" from AKKA Technologies. This system focuses mainly on automotive buses where it is used as gateway for connecting different automotive segment together. It lacks features for analog measurement, has very limited number of digital I/Os etc.

Figure 1.5.: CANextender [41]

Some of the basic requirements that unit developed in this research should fulfil are:

- flexibility: can easily fit different requirements
- connectivity:
  - common automotive real time bus systems: CAN, CAN FD, LIN
  - PC communication interfaces: USB, Ethernet for data monitoring, visualisation and ECU calibration
- model based software/firmware development for easy programming
- extensibility:

  - external digital IOs: for sensors and actuators
  - external ADC inputs: for analog sensor measurements (sensor interface should be part of sensor add-on board)
  - internal extension: Serial Peripheral Interface (SPI) and I2C for add-on boards
- Electro Magnetic Compatibility (EMC):
  - the Elector Magnetic Interference (EMI) of developed system must satisfy at least industrial standards
  - basic ESD test qualification requirements

1.2. Scope

The scope of this thesis focuses mainly on design and fulfilment of proposed requirements in the Section 1.1 which includes design,implementation and evaluation of a unit. There are many different approaches for system realization. Some of them would be either Microcontroller-Unit based MCU approach, Field Programmable Gate Array (FPGA) based or combination of both the so called System on Chip (SOC). Each of these has its advantages and disadvantages. This study focuses mainly on MCU approach. The main reason for that are availability, complexity and cost of the device. At the time of writing this thesis there are many different MCUs, addressing different problems domains. In this thesis used MCU is a one which has been developed specially for automotive applications. The electronics of a modern vehicle is complex and different units have different requirements. Human-Machine-Interface (HMI) units are less critical compared to for example Body-Units. Missing some deadline in a HMI device is not a big issue but missing a deadlines in an Airbag-Unit could have catastrophic consequences. It is obvious that construction of a single system that would cover all these different domains would be hard if not even impossible.

2. Technical Background

This chapter covers technical background required for understanding the system design, implementation and evaluation. Examples presented in this chapter are mostly parts of a system design. Knowledge presented in this chapter is a mix of the hardware and software concepts which are used in implementation of the system.

2.1. Microcontroller

A Microcontroller Unit (MCU) is single integrated circuit which contains at least Central Processing Unit (CPU), Random Access Memory (RAM), Read Only Memory (ROM) and Input/Output ports (IOs). Depending on domain of application, MCUs can have different integrated peripherals like Analog Digital Converters (ADC), interfaces like Ethernet, CAN, LIN, I2C, SPI etc. Watchdog timers, Direct Memory Access units (DMAs) etc. An example of a such a system is Renesas RH850 shown in Figure 2.1 [32].

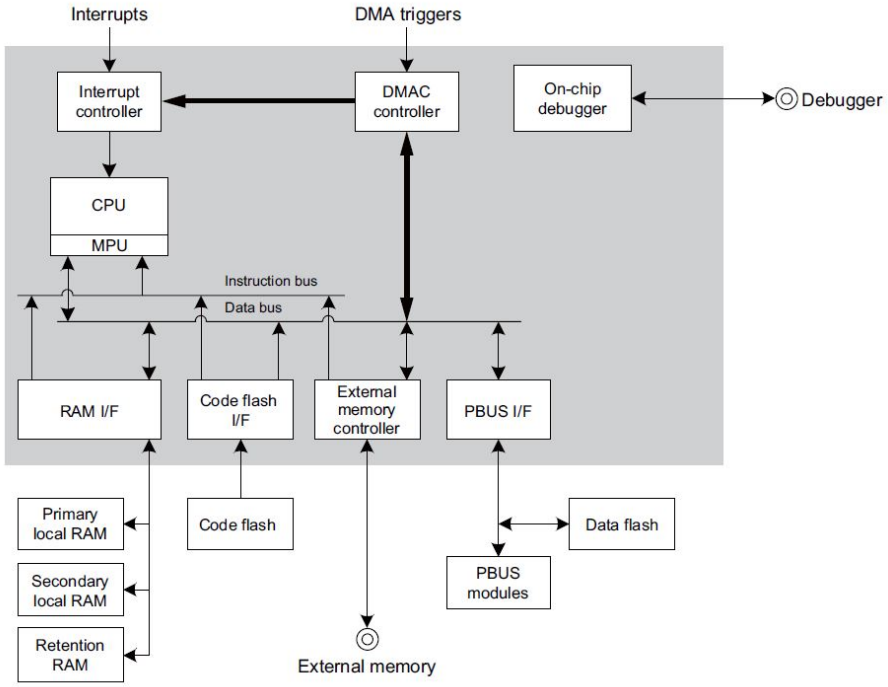


Figure 2.1.: Renesas RH850-F1L 100 [33]

Renesas RH850 F1L is a MCU designed for automotive applications. It features single 32 bit CPU, 768 Kbytes of code flash memory for executable code and 96 Kbytes of Random Access Memory (RAM). There is also so called retention RAM of 32 Kbytes, whose values are even preserved when the MCU enters sleep mode. Further MCU features I2C and SPI for peripheral extendability, OS Timer which can be used as a clock of Operating System (OS), Timer Array Units for precise and CPU independent signal generation like Pulse Width Modulation (PWM), DMAs for CPU independent copy operation, like copying ADC sampled data to buffer, CAN/LIN controllers, Joint Test Action Group (JTAG) for debugging and MCU flashing, Interrupt Controller for interrupt management, internal data flash for storing user data etc. The CPU

of RH850 has a Harvard architecture (separate data and instruction memory) and Reduced Instruction Set Computer (RISC) [13, 33].

2.1.1. Memory Organisation

Theoretical address space of this MCU is 4 GB. Table 2.1 shows a memory organisation and mapping of different peripherals into address space of the MCU.

Memory Address	Description	Size
$0x00000000 - 0x000BFFFF$	Code Flash	768 KB
$0xFF200000 - 0xFF207FFF$	Data Flash Area	32 KB
$0xFEDF0000 - 0xFEDFFFFF$	Primary Local RAM Area	64 KB
$0xFEE00000 - 0xFEE07FFF$	Retention RAM Area	32 KB
$0xFFFFAFFF - 0xFFFF8000$	DMA / INTC	12 KB
$0xFFFF7FFF - 0xFF400000$	Internal Peripheral I/O Area	11.97 MB

Table 2.1.: Renesas R7F7010243AFP memory map [13]

2.1.2. Supply Voltage

Renesas R7F7010243AFP has two different power domains, **Always-On area** (AWO) and the **Isolated area** (ISO). As the name suggests AWO area is always supplied with the voltage, where ISO area can be turned off to reduce overall power consumption [13]. For proper operation of the device following voltages are required:

- REGVCC: on-chip voltage regulators
- EVCC: for I/O port
- A0VREF: for A/D converters and the dedicated I/O ports

Tables 2.2 shows absolute voltage ratings of a each domain. Maximal current ratings of I/Os are **+/- 10 mA** in both directions (output and input direction) [13].

Symbol	Maximum Voltage [V]
REGVCC	6.5
EVCC	6.5
AoVREF	6.5
I/O	6.5
AWOVSS, ISOVSS, EVSS, AoVSS	0.5

Table 2.2.: System supply voltage (REG), port supply voltage (EVCC) and A/D-converter supply voltage (AoVREF) [33]

2.1.3. Clock

External resonator can be either crystal or ceramic with frequency range between **8** and **24** MHz [13]. It is connected to the MainOSC which generates so called clock X. High Speed Internal Oscillator (HS IntOSC) generates a clock RH with frequency of 8 MHz and Low Speed Internal Oscillator (LS IntOSC) generates a clock RL with frequency of 240 kHz. PLL circuit uses MainOSC as clock reference and generates CPLLCLK and PPLLCLK. Divided clocks are CPLLCLK2, PPLLCLK2, PPLLCLK4 [13, 33].

2.1.4. Debugger

Renesas RH850 F1L supports "Low Pin Debug Interface" called LPD (4-Pin) [13, 33]. Debugging and flash programming is performed with Renesas E1 on-chip emulator [11]. For supporting both flash programming and debugging, adequate wiring between MCU and E1 must be selected. Figure 2.2 shows required wiring for both debugging and programming support [12].

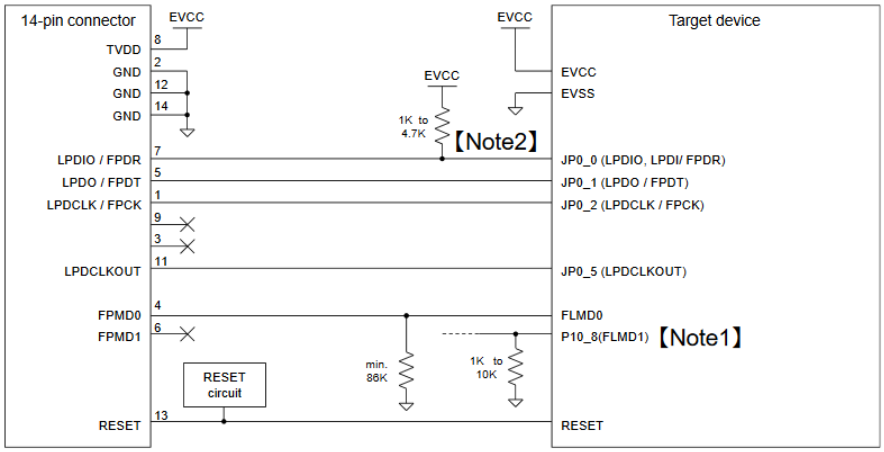


Figure 2.2.: Debugging (1-Pin or 4-Pin LPD) and programming (1-wire or 2-wire UART) [12]

Operating mode after reset is selected with pins $FLMD0$ and $FLMD1$ ($P10_8$). Possible operating modes are normal, serial programming and boundary scan. For **normal operating mode** $FLMD0$ **must be pulled low**. For **serial programming mode** $FLMD0$ **must be high and** $FLMD1$ **low**. In boundary scan mode both $FLMD0$ and $FLMD1$ must be pulled high [13].

2.2. Power Supply

Every electronic device need a power supply that provides one or more voltages. Generally DC voltage is required. Different strategies exist for generation of such voltages depending on application requirements. Some of important characteristics are output voltage and its tolerance, ripple voltage, temperature variations, maximum load current and power efficiency (Equation 2.1) [40].

$$Efficiency = \frac{Output}{Input} \cdot 100(\%) \tag{2.1}$$

2.2.1. Linear Voltage Regulator

Figure 2.3 shows an example of linear voltage regulator. A PNP transistor is connected directly to the input voltage (V_{IN}) and error amplifier regulates the V_{BE} with respect to V_{IN}.

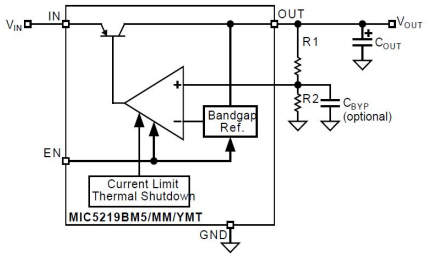


Figure 2.3.: Linear voltage regulator [27]

Analysis of voltage regulator shown in the figure 2.3 gives following Equations:

$$V_{OUT} = V_{R1} + V_{R2} = V_{R1} + V_{BandgapRef.}$$

$$V_{R1} = \frac{R_1}{R_1 + R_2} \cdot V_{OUT}$$

$$V_{OUT} = V_{BandgapRef.} + \frac{R_1}{R_1 + R_2} \cdot V_o$$

$$\boxed{V_o = (\frac{R_2}{R_1} + 1) \cdot V_{BandgapRef.}} \tag{2.2}$$

Equation (2.2) shows that output voltage depends mainly on feedback resistors and reference voltage source. Let assume reference voltage is $V_{ref} = 1.242V$ and output voltage should be fixed at 3.3V that gives that a gain factor $\frac{R_2}{R_1} + 1$

must be 2.657. Fixed voltage regulators have built in R_1/R_2 resistors and therefore predefined output voltage, where adjustable regulators require external resistor which are dimensioned according output voltage requirements. Power lost during conversion is calculated by $P_{lost} = (V_I - V_o) \cdot I_{max}$ [W] which means linear voltage regulator should be used in applications where regulated voltage (output voltage) does not differ much from the input voltage [40]. Above analysis shows that linear voltage regulator are power inefficient if used in battery powered applications where application voltage differs much from supply voltage.

2.2.2. Step-Down Converter

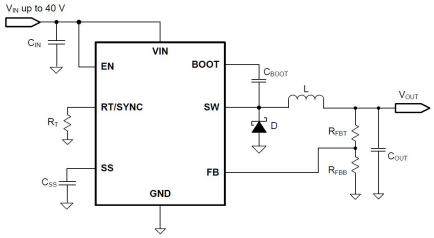


Figure 2.4.: TI LMR14020-Q1 Step-Down Converter [21]

Switched mode power supply (SMPS) are more power efficient, over 90% of power efficiency is possible [40]. Step-Down or buck DC-DC converter is used to convert high DC voltage to low DC voltage. For understanding how Step-Down converter works, the circuit shown in Figure 2.4 must be analysed. During switch off (SW) time (t_{off}) voltage across L is $(-V_{OUT}) = L \cdot \frac{\Delta I_L}{t_{off}}$ and the diode D is forward biased. Contrary during t_{on} time voltage across L is $V_{IN} - V_{OUT} = L \cdot \frac{\Delta I_L}{t_{on}}$ and the diode D is reversed biased. In steady state both currents in t_{on} and t_{off} states are the same resulting that the output voltage is:

$$\boxed{V_o = \frac{t_{on}}{t_{on} + t_{off}} \cdot V_I = \frac{t_{on}}{T} \cdot V_I} \tag{2.3}$$

Pin	Description
Boot	Bootstrap capacitor (0.1 µF)
V_{IN}	Input voltage (up to 40V)
EN	Enable pin,connect to voltage divider for under-voltage lockout
RT/SYNC	Switching frequency, connected to a resistor
FB	Output feedback, connect to the feedback divider to set V_{OUT}
SS	Soft-start, connected to a capacitor to set soft-start time
SW	Internal MOSFET

Table 2.3.: LMR14020-Q1 specification [21]

Output voltage depends mainly on factor $\frac{t_{on}}{T}$ which is called duty cycle. TI LMR14020-Q1 is configurable step down converter which accepts input voltages up to 40V and can deliver up to 2A output current. Output voltage is given by simple feedback resistor network. Further features of this regulator are integrated High-Side MOSFET, adjustable switching frequency, frequency synchronization, spread spectrum option for EMI reduction, soft-start, over- and shortvoltage protection [21]. Table 2.3 describes pins functionality of the regulator.

Setting V_{OUT} is done by feedback resistor (Figure 2.5). LMR14020 has a precise internal voltage reference of 0.75V and feedback network is calculated with Equation 2.4 [21]. Let assume V_{OUT} should be 5V and R_{FBB} 17.8kΩ which gives:

$$\boxed{R_{FBT} = \frac{V_{OUT} - 0.75V}{0.75V} \cdot R_{FBB}} \tag{2.4}$$

$$R_{FBT} = \frac{5V - 0.75V}{0.75V} \cdot 17.8k\Omega = 100k\Omega$$

Under-voltage lockout, is the voltage under which a regulator is turned off. This has a benefit in battery power application, where the device is turned off when certain voltage threshold is reached for preventing further discharging of a battery. Lockout is calculated by following Equations (Figure 2.6):

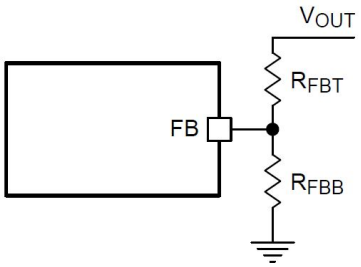


Figure 2.5.: TI LMR14020-Q1 feedback network [21]

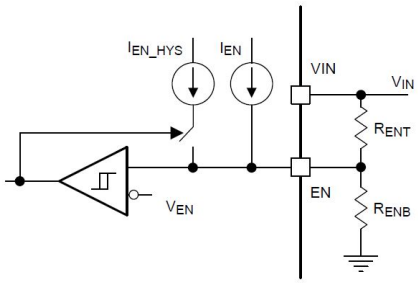


Figure 2.6.: TI LMR14020-Q1 Adjustable Under-voltage Lockout [21]

$$\boxed{R_{ENT} = \frac{V_{START} - V_{STOP}}{I_{HYS}}} \tag{2.5}$$

$$\boxed{R_{ENB} = \frac{V_{EN}}{\frac{V_{START} - V_{EN}}{R_{ENT}} + I_{EN}}} \tag{2.6}$$

Let assume $V_{start} = 5.4V$ and $V_{stop} = 5V$ are desired values of start and stop voltages. I_{HYS} current is inserted when V_{EN} terminal is above 1.2V [21]. Plugging these parameters into Equation 2.5 gives value for $R_{ENT} = 110k\Omega$. At $V_{EN} = 1.2V$ is a current $I_{EN} = 1\mu A$ [21]. Plugging all known parameters into Equation 2.6 gives $R_{ENB} = 30k\Omega$

Soft-start is a feature which prevents inrush currents when power is first applied. It generates a ramp from $0V$ to V_{REF} [21]. Desired time is calculated by Equation 2.7 where I_{SS} is a current which charges a capacitor and has a value of $3\mu A$. Let assume soft-start is approximately $1ms$ then calculated capacitance must be $C_{SS} = 4.7nF$.

$$\boxed{t_{SS}(ms) = \frac{C_{SS}(nF) \cdot V_{REF}(V)}{I_{SS}(A)}} \tag{2.7}$$

$$C_{SS} = \frac{t_{SS}(ms) \cdot I_{SS}(A)}{V_{REF}(V)} = \frac{1ms \cdot 3\mu A}{0.75V} = 4nF \approx 4.7nF$$

Switching frequency is calculated by Equation 2.8 [21]. For $1MHz$ switching frequency ($\frac{1}{t_{off}+t_{on}}$) R_T is 23.36Ω which implies standard value resistor of $23.2k\Omega$.

$$\boxed{R_T(k\Omega) = 42904 \cdot f_{SW}(kHZ)^{-1.088}} \tag{2.8}$$

Minimum inductance (L) is calculated by Equation 2.9 where K_{IND} ($\Delta i_L / I_{MAXOUT}$) is a coefficient that represents relation between maximal output current and inductor ripple current. The value for K_{IND} should be between 20% and 40%. Inductor ripple current (Δi_L) is calculated by Equation 2.10 [21]. Let assume $K_{IND} = 0.4$ then minimum inductance required is $5.5\mu H$ which results in ripple current of $\Delta i_L = 0.79A$. If inductance of $33\mu H$ is selected ripple current is $\Delta i_L = 0.13A$. Ferrite with capabilities of $2A + \Delta i_L = 2.1A$ RMA current and saturation current of $3.1A$. Suitable part would be shielded high power conductor from BOURNS SRR1208-330YL, which has inductance of $33\mu H$, RMS $2.8A$ and saturation current $3.80A$ [6].

$$\boxed{L_{MIN} = \frac{V_{INMAX} - V_{OUT}}{I_{OUT} \cdot K_{IND}} \cdot \frac{V_{OUT}}{V_{INMAX} \cdot f_{SW}}} \tag{2.9}$$

$$\boxed{\Delta i_L = \frac{V_{OUT} \cdot (V_{INMAX} - V_{OUT})}{V_{INMAX} \cdot L \cdot f_{SW}}} \tag{2.10}$$

Input voltage	5.5V to 40V
Output voltage	5V
Maximum output current	2A
Transient Response 0.1 A to 2 A	5%
Output Voltage Ripple	50mV
Input Voltage Ripple	10mV
Switching Frequency f_{SW}	1MHz
Soft-start time	1ms

Table 2.4.: LMR14020-Q1 design parameters

C_{BOOT}	$0.1\mu F; 16V; ceramic X7R or X5R$
L	$33\mu H; I_{foreward} = 2.1A; V_{breakdown} = 40V$
D	SS34 or similar
R_{FBT}	$100k\Omega$
R_{FBB}	$17.8k\Omega$
C_{OUT}	$68\mu F; 16V$
C_{IN}	$22\mu F; 50V$
R_T	$23.3k\Omega$
C_{SS}	$4.7nF$

Table 2.5.: LMR14020-Q1 calculated parameters

$$L_{MIN} = \frac{40V - 5V}{2A \cdot 0.4} \cdot \frac{5V}{40V \cdot 1MHz} = 5.5\mu H$$

Output capacitance selection is important since it affects loop stability, output voltage ripple and over/undershoot voltage during load current transients.

The diode (D) (Figure 2.4) should be a Schottky diode with breakdown voltage 25% higher than the maximum input voltage. Current rating should be equal to the maximal current (2A) [21]. Example diode would be Vishay SS34 diode which has forward current rating of $3A$ and break down voltage of $40V$ [43].

Tables 2.4 2.5 show design and calculated/recommended parameters for the LMR1420 regulator.

2.2.3. Power Supply Switch

As it has been discussed in Section 2.2.2, *LMR*1420 has enable pin which is used to enable or disable voltage regulator. Since this pin is used to set so-called "lockout voltage" it must be connected directly to the input voltage. Let suppose microcontroller or some other digital sources must be able to control enable pin, either to turn power supply on or off. For fulfilling this requirement, electrical switch must be constructed.

Let suppose electrical switch has following requirements:

- Input voltage up to 40V
- Maximal input current up to 4.6µA
- Switch controllable from CMOS 5V output
- Switch controllable from sources up to 40V

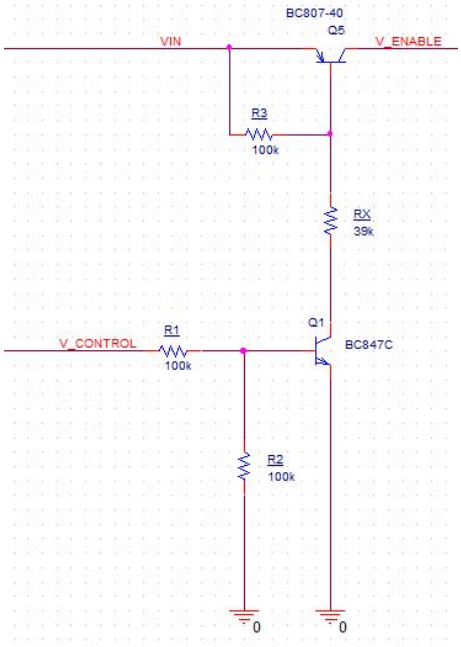


Figure 2.7.: Power Supply Switch

Parameter	Value	Unit
DC Current Gain	420	
Collector-Emitter Saturation Voltage	250	mV
Base-Emitter Saturation Voltage	700	mV

Table 2.6.: NPN BC847 [9]

Switch is implemented with two bipolar junction transistors, one PNP and one NPN. For the PNP BC807C transistor to be on, it must have approximately voltage drop V_{BE} of -0.7V otherwise the transistor is off [8]. The BC847 NPN transistor is operated in saturation mode and its purpose is to control V_{BE} voltage of PNP transistor. Resistor R_1, R_2 and R_3 are selected to have 100kΩ. NPN is in saturation region when $V_{CE,SAT} = 0.2$V and $V_{BE} = 0.7$V (Table 2.6). Resistors R_1 and R_2 set base current I_B of NPN, which is direct proportional to $I_C = h_{FE} \cdot I_B$.

Current through R_2 is given by Equation 2.11. Base current I_B of NPN transistor for $V_{CONTROL} = 40$V and $V_{CONTROL} = 5$V is given by Equations 2.12 2.13 respectively. From Equation 2.11, 2.12 and 2.13 follows that NPN transistor could potentially deliver up to 162.12mA for both cases $V_{CONTROL} = 40$V and $V_{CONTROL} = 5$V respectively (Equations 2.12 2.13). Resistor R_X makes sure that NPN transistor is in saturation region and limits the I_C current. Let assume maximal I_C current through the switch should be 1mA and from that follows that R_X must be 39kΩ (Equation 2.16). For a input voltage V_{IN} of 40V power lost on resistor is 39.1mW.

$$I_{R2} = \frac{V_{BE,NPN}}{R_2} = \frac{0.7\text{V}}{100\text{k}\Omega} = 7\mu\text{A} \tag{2.11}$$

$$I_{R1} = \frac{V_{R1}}{R_1} = \frac{V_{IN} - V_{BE,NPN}}{R_1} = \frac{40\text{V} - 0.7\text{V}}{100\text{k}\Omega} = 393\mu\text{A} \tag{2.12}$$

$$I_{R1} = \frac{V_{R1}}{R_1} = \frac{V_{IN} - V_{BE,NPN}}{R_1} = \frac{5\text{V} - 0.7\text{V}}{100\text{k}\Omega} = 50\mu\text{A} \tag{2.13}$$

$$I_C = h_{FE} \cdot I_B = h_{FE} \cdot (I_{R1} - I_{R2}) = 420 \cdot 386\mu\text{A} = 162.12\text{mA} \tag{2.14}$$

$$I_C = h_{FE} \cdot I_B = h_{FE} \cdot (I_{R1} - I_{R2}) = 420 \cdot 43\mu A = 18.06mA \tag{2.15}$$

$$R_X = \frac{V_{IN} - 0.7V - 0.2V}{1mA} = 39k\Omega \tag{2.16}$$

2.2.4. Reference Voltage-Bandgap

Main properties of reference voltage sources are precision and stability versus environmental conditions like temperature, pressure and ageing. There are many applications (voltage regulators, analog-digital converters) where stable reference voltages are required and where results of these circuits depends mainly on stability of reference voltage. Basic idea of a bandgap is to use bandgap voltage, which is a voltage that electron must overcome to go from valence to conduction band. This voltage is temperature independent [40]. Figure 2.8 shows bandgap reference with two bipolar junction transistors (BJT). Change of V_{BE} over temperature is $\frac{dV_{BE}}{dT} = \frac{-2mV}{K}$, this means that V_{BE} is Complementary To Absolute Temperature (CTAT) [40]. Combining Proportional To Absolute Temperature (PTAT) and CTAT voltage results in a constant and temperature independent voltage.

$$V_{ref} = V_{BE2} + V_{R1}$$

Following analysis of the circuit shown in Figure 2.8 should clarify possible realisation of voltage reference. Current of BJT is given by $I_C = B \cdot I_{BS} \cdot (e^{\frac{V_{BE}}{V_T}} - 1)$ [40]. Note that I_{C1} should be n times larger than I_{C2} current. ΔV_{BE} is calculated by quotient $\frac{I_{C1}}{I_{C2}}$:

$$\frac{I_{C1}}{I_{C1}} = \frac{I_{C1} = B \cdot I_{BS} \cdot (e^{\frac{V_{BE1}}{V_T}} - 1)}{I_{C2} = B \cdot I_{BS} \cdot (e^{\frac{V_{BE2}}{V_T}} - 1)}$$

Which gives:

$$V_{BE1} - V_{BE2} = ln(\frac{I_{C1}}{I_{C2}}) \cdot V_T = ln(\frac{n \cdot I_{C2}}{I_{C2}}) \cdot V_T = ln(n) \cdot V_T$$

where

$$V_T = \frac{k \cdot T}{q}$$

This voltage drop ($V_{BE1} - V_{BE2}$) is forced across R_1 and has positive temperature coefficient. Base-emitter voltage of Q2 has a negative temperature coefficient which is added to the amplified voltage ($V_{BE1} - V_{BE2}$) resulting in output voltage which is independent of temperature.

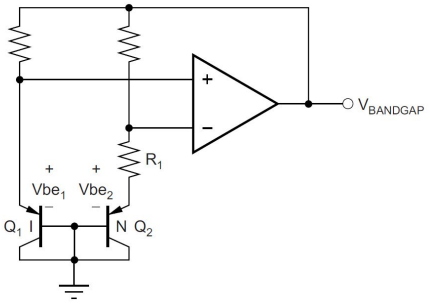


Figure 2.8.: Bandgap reference [20]

2.3. Controller Area Network - CAN/CAN FD Bus

Controller Are Network (CAN) is a serial bus system developed by Bosch in late 80's. Initially meant only for automotive communication between two or more ECU (Figure 2.9). CAN specifications has passed many revisions and the most remarkable are CAN 2.0A and 2.0B specifications which are the basis for all CAN variations until today [44]. Nowadays all automotive microcontrollers have integrated CAN controller. CAN-Controller is connected to CAN-Bus through CAN-Transceiver.

2.3.1. Physical Layer

Since different CAN specifications exist, this thesis focuses on so called High-Speed CAN which has data rate from $\geq$ 250 kbit/s up to 1Mbit/s and is

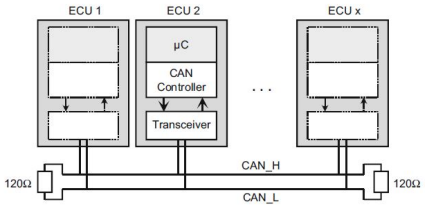


Figure 2.9.: CAN Bus [44]

defined by ISO-11898-2. Physical layer uses differential voltage which is between 0 and 2V. For collision avoidance "Carrier-Sense Multiple Access with Collision Avoidance (CSMA/CA)" is used [44].

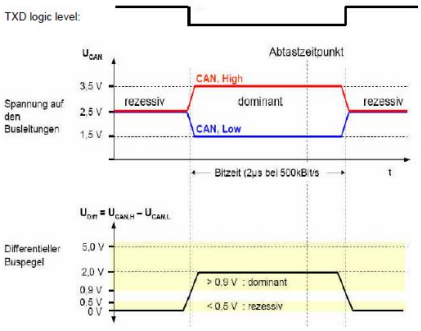


Figure 2.10.: CAN Signals [44]

The Figure 2.10 shows logical and physical representation of CAN signals. Logical low also known as dominant bit creates differential voltage which must be at least $(V_{diff} = V_{CANH} - V_{CANL}) \geq 0.9$V. Contrarily logical high known as a recessive bit creates 0V or at most $V_{diff} \leq 0.5$V.

Twisted differential cables are terminated at both ends with characteristic impedance of 120 Ω (Figure 2.9). Termination resistors prevent reflections in the cable which may increase error rate [44].

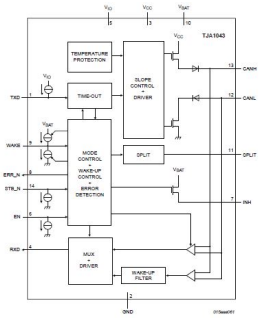


Figure 2.11.: Block diagram of NXP TJA1043 CAN-Transceiver [7]

Physical translation is realised with CAN transceiver. Simplified model consists of driver which controls two transistor (Figure 2.11). Transistors are operated as a open-drain outputs. In the dominant state both transistors are closed and in recessive state both are open. Schmitt trigger converts differential voltage to logical level, which is used to read bus but also as a feedback mechanism during writing and accessing bus for collision avoidance.

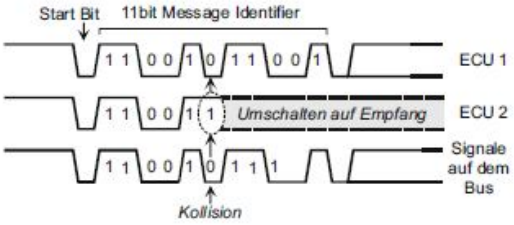


Figure 2.12.: CAN bus collision avoidance [44]

Following examples demonstrates collision avoidance. When a device writes a bit on the bus, at the same time bit is read back. If two or more devices are sending at the same time collision is detected when one of devices puts recessive bit (V_{diff} = 0V) and reads dominant bit from the bus. At that moment the device stops immediately sending. Entering into listen mode and the device who put dominant bit continues sending without event noticing that collision occurred [44]. This is the reason why a logical 0 is called dominant bit and

why in CAN arbitration phase frame with lower ID has higher priority. More about bus arbitration will be discussed in Section 2.3.2.

2.3.2. Data Link Layer

Data link layer is defined by ISO 11898–1. CAN is broadcast system meaning a message does not have source or destination address. Each frame is identified by unique ID. Logical frame consists of a start bit, header,control bits, payload, CRC, acknowledge bit and "End of Frame" part. Header contains either of 11 bits (standard ID) or 29 (extended ID). Bus arbitration is ID based, meaning that node with lower ID (more dominant bits) wins the arbitration. Control bits are set depending on frame configuration. 4 bit DLC represent payload size in bytes and can be between 0 and 8 bytes. 15 bit CRC is calculated on payload after which CRC delimiter (always recessive) follows. Acknowledge bit (dominant) must be issued by at least one node otherwise frame is resent. At the end of frame at least 7 recessive bits are sent. Receivers synchronize normally by "start bit" but sometimes frames bit are composed of long sequences of either 0 or 1. For overcoming a problem of lost synchronisation stuffing bits are added. After five consecutive bits with same value, one inverted bit is inserted. Stuffing is done on header, control bits, payload and CRC only.

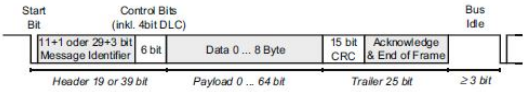


Figure 2.13.: Standard CAN frame [44]

2.3.3. CAN FD

CAN FD (Flexible Data-Rate) is further extension of CAN protocol. One of the main features that CAN-FD provide are increased data rate and the size of payload. Payload goes up to 64 bytes and bound rate overcomes 1Mbit/s limit. Note that is also reverse compatible with standard CAN specification, meaning that CAN-FD and CAN can coexist on the same network without interference [44].

2.4. LIN Bus

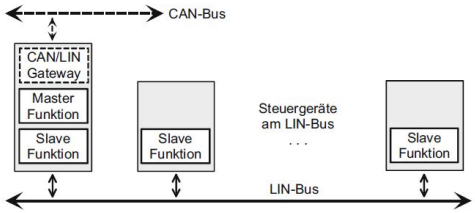


Figure 2.14.: LIN bus structure [44]

Local Interconnect Network (LIN) was developed at the late 90's by Motorola and many different motor vehicle manufacturers. The motivation for LIN was cheaper alternative for CAN-Bus and standardization protocol for connection of sensors and actuators to ECUs. LIN-Bus has single master and multiple slave bus topology where master node acts usually as CAN-LIN gateway (Figure 2.14) [44].

2.4.1. Physical Layer

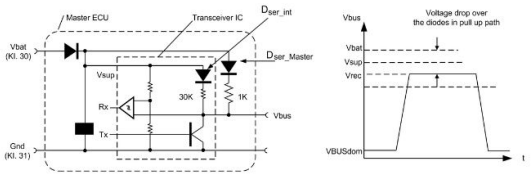


Figure 2.15.: LIN physical [42]

Commonly based on asynchronous serial communication and can be implemented with any controller that has universal asynchronous receiver-transmitter (UART). LIN-Transceiver is need to connect UART on physical bus (Figure 2.15). Bus voltage levels are derived from $V_{bat}/Clamp30$ and ground ($GND/Clamp31$) where V_{bat} represents recessive and GND dominate state (Figure 2.16) [44, 42].

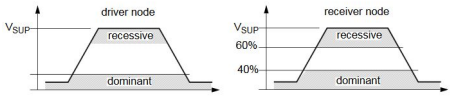


Figure 2.16.: LIN voltage levels [42]

Baud rates go from 1 kbit/s up to 20 kbits/s. LIN-Bus can have up to 16 nodes, and maximal cable length up to 40m. Bus is terminated with a pull-up resistor, 1kΩ master and 30kΩ slave node [42].

2.4.2. Data Link Layer

Data are encapsulated in LIN frame (Figure 2.17). Structure of a LIN frame contains:

- Break filed: indicates new incoming frame
- Sync field: allows the slave to synchronize to master clock
- Protected identifier: allows the slave to correctly interpret a message
- Data field: contains incoming data (maximal 8 bytes)
- Checksum: insures correct reception

Frame contains two parts header and response. The header is always generated by master where response can be either from master or slave. Master has al least one schedule table which defines the sequences of messages transmitted to the LIN-Bus Scheduling table also defines time intervals by which messages are transmitted.

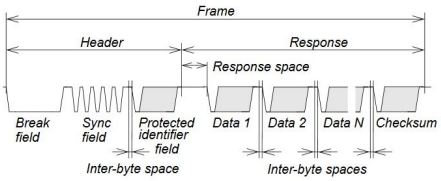


Figure 2.17.: LIN frame structure [42]

2.5. Analog-Digital Converter (ADC) - Successive Approximation (SAR)

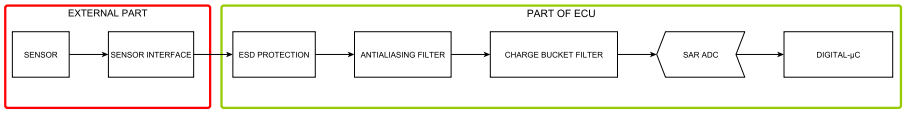


Figure 2.18.: Signal Chain

Signal chain is shown in the Figure 2.18 which is composed of two parts, external and internal part. External part represents sensor and its interface. External sensor can be any sensor of interest as long as it fits to ADC specifications and capabilities. Sensor interface is part of signal conditioning chain and must be constructed according to the ADC specifications. Internal part of a signal chain represents ECU integrated components. ESD protection circuit should protect internal components when the external interface is disconnected. Antialiasing and charge bucket filter is a part of a internal signal conditioning. Quantisation is done by Analog to Digital Converter (SAR) and digitalized values are further processed by microcontroller.

Figure 2.19 shows a structure of a typical SAR ADC. It consists of Digital to Analog Converter (DAC), comparator, N-bit register and control logic. SAR operation is broken into two phases, acquisition and conversion phase. During acquisition phase, Sample&Hold (SH) circuit is connected and the goal is to charge internal SH capacitor to the input voltage. Time taken during this phase is called acquisition time (t_{ACQ}). In the conversion phase, SH circuit is disconnected from the input and stored voltage is quantised. Depending on the resolution (N bit) of the ADC, conversion time can take up to N cycles. Voltages levels in each cycle are given by $\sum_{c=1}^{N} bit_c \cdot \frac{V_{ref}}{2^c}$ where bit_c represents bit of current conversion cycle and can be either 1 or 0. At the start of each conversion, firstly most significant bit (MSB) is set, where this bit creates $V_{ref}/2$ voltage. This is compared with in the SH circuit stored voltage. If the stored voltage is less than $V_{ref}/2$, the MSB is 1 otherwise 0.

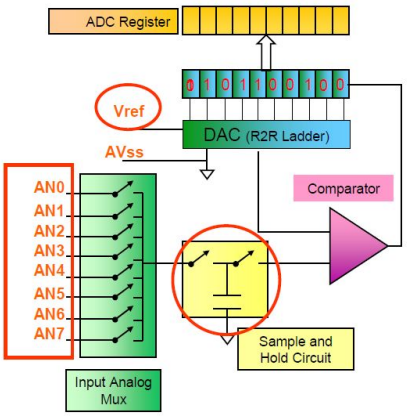


Figure 2.19.: Successive-approximation ADC [31]

A the end of conversion phase, N-bit register contains converted value of stored voltage. ADC can be either integrated directly into microcontroller or stand-alone IC which is controlled through interfaces like SPI, I2C, LVDS etc.

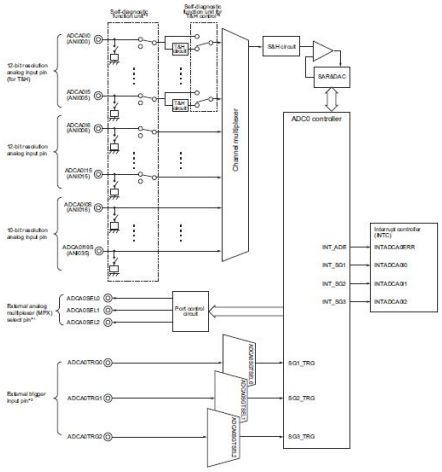


Figure 2.20.: ADCA0 of RH850 F1L Block Diagram [13]

2.5.1. Charge Bucket Filter for SAR

Usually microcontrollers have several analog input pins where single SH circuit with ADC is multiplexed using the analog multiplexer. An example is SAR-ADC integrated into RH850-F1L microcontroller which has 16 analog inputs called channels (Figure 2.20).

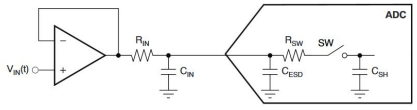


Figure 2.21.: Amplifier, charge bucket filter and ADC [19]

Voltage on capacitor C_{SH} of SH circuit during acquisition time, has to settle correctly (input voltage $V_{IN} \pm \frac{1}{2} \cdot LSB$). When input of single ADC is multiplexed and switching fast between two or more different analog inputs, which differ too much in sampled voltages and sources of these voltages have high

Name	Value	Unit
t_{ACQ}	3	µs
C_{SH}	50	pF

Table 2.7.: RH850 F1L ADC parameters

output impedances (RC time is elongated), the voltage across SH capacitor may not settle correctly within acquisition time. Wrong settled input voltage leads to incorrect sampled value. Solution to this problem is to add external capacitor $C_{IN/EXT}$ that server as a charge reservoir. Added external capacitor with impedance of the input source could further extend needed RC charge time. Adding buffer amplifier fixes the impedance problem of the voltage source that needs to be sampled, but since buffer amplifier has capacitive load on its output, it could become unstable. Stability could be fixed by adding external resistor $R_{IN/EXT}$ and selecting operational amplifier with sufficient Unity-Gain bandwidth (GBW). This circuit is known as charge bucket or front-end filter and its purpose is to make sure that the voltage across capacitor C_{SH} has settled correctly in a given t_{ACQ} time (Figure 2.21). Bandwidth (usually few hundreds kHz or less) of the antialiasing filter dominates compared to charge bucket filter (tens of MHz). Potential source of error is that a buffer amplifier with a low pass circuit on its output could cause voltage overshoot which may not stabilize to correct value during acquisition time. Crucial part of the charge bucket filter is to dimension the external resistor R_{IN}, the capacitor C_{IN} correctly as well select suitable operational amplifier with sufficient GBW. For the filter design important ADC parameters are:

- Acquisition time t_{ACQ}
- Value of Sample&Hold capacitor C_{SH}

Note that R_{SH} value shown in the table 2.7 is assumed value for internal SH circuit found in RH850 microcontroller.

Following equation can be used to dimension charge bucket filter [19]:

$$\boxed{C_{IN} = 20 \cdot C_{SH}} \tag{2.17}$$

Using Equation 2.17 and value for C_{SH} taken from Table 2.7 gives that C_{IN} is equal to 1nF.

Certain accuracy in settling for 12 bit ADC could be achieve by multiplying time constant with factor 9 [19].

$$\boxed{t_{ACQ} = 9 \cdot \tau_{FILTER}} \tag{2.18}$$

Given that $\tau_{FILTER} = R_{IN} \cdot C_{SH}$, using Equation 2.18 and knowing that $t_{ACQ} = 3\mu s$ gives that R_{IN} equals 333.333Ω (Equation 2.19) [33].

$$\boxed{R_{IN,max} = \frac{t_{ACQ}}{9 \cdot C_{IN}} = \frac{3\mu s}{9 \cdot 1\text{nF}} = 333.333\Omega} \tag{2.19}$$

GBW of the operation amplifier should be at least (optimal 4 times) [19]:

$$\boxed{GBW \geq 2 \cdot \frac{1}{2 \cdot \pi \cdot \tau_{FILTER}}} \tag{2.20}$$

Using Equation 2.20 for calculated filter elements give that selected amplifier must have at least 1.9MHz Equation 2.21.

$$\boxed{GBW = 4 \cdot \frac{1}{2 \cdot \pi \cdot R_{IN} \cdot C_{IN}} = 1.9\text{MHz}} \tag{2.21}$$

Since selected operational amplifier (TI-TLV34xx) has more GBW than needed. Using Equation 2.22 and $BMW = 2.3\text{MHz}$ of selected amplifier gives that minimal value for R_{IN} is 83.76Ω [22]. R_{IN} must be in range of $83.76\Omega \leq R_{IN} \leq 333.333\Omega$.

$$\boxed{R_{IN,min} = \frac{1}{2 \cdot \pi \cdot GBW_{OPAMP} \cdot C_{IN}} = \frac{1}{2 \cdot \pi \cdot 2.3\text{MHz} \cdot 1\text{nF}} = 83.76\Omega} \tag{2.22}$$

Name	Value	Unit
Conversion clock	40	MHz
Resolution	12	bit
Conversion time	5.75	µs
Sampling/Acquisition time	3	µs
Analog input voltage	VREF	V
Operation current	3.0	mA
Integral nonlinearity	±4	LSB
Differential nonlinearity	±3	LSB
Zero scale error	±7.5	LSB
Full scale error	±7.5	LSB
Overall error	±8.0	LSB

Table 2.8.: RH850-F1L A/D Converter Characteristics per channel [33]

2.5.2. Anti-Aliasing Filter

Acquisition time $t_{ACQ} = 3\mu s$ and conversion time of $t_{CONV} = 5.75\mu s$ give maximal sample rate of 114kHz per channel (Table 2.8).

From the Nyquist theorem $f_{SIGNAL} \leq 2 \cdot f_{SAMPLE}$ follows that maximal signal frequency allowed is $f_{signal,max} = \frac{114\text{kHz}}{2} = 57kHz$ [2]. For better results sample rate should be divided at least by 4, 8 or even more.

For preventing aliasing effect, antialiasing filter (low pass filter) should be constructed to match bandwidth of the ADC or to match signal requirements. Since in this thesis, ADC should have as much bandwidth as possible, the goal will be to have full bandwidth ADC can provide. Antialiasing filters can be either passive or active. Single pole passive low pass filter has attenuation of $-20dB$ pro decade. More bandwidth (narrow transition band) could be achieved by implementing higher order filter. Since in this system design only operational amplifier with single supply (+5V) are used, Sallen-Key (Butterworth) filter would be a good option (Figure 2.24) [34].

First step in filter design to fulfil te requirements (Table 2.9) is to calculate required filter order. Amplitude response of a Butterworth is given by equation 2.23.

Gain [dB]	Frequency [rads/s]
$G_{passband,dB} = -3dB$	$\omega = 2 \cdot \pi * 1 \cdot \text{kHz}$
$G_{stopband,dB} = -40dB$	$\omega = 2 \cdot \pi * 11.4 \cdot \text{kHz}$

Table 2.9.: Butterworth Filter Design Parameters

$$\boxed{G(\omega) = \frac{1}{\sqrt{1 + (\frac{\omega}{\omega_c})^{2 \cdot n}}}} \tag{2.23}$$

From Equation 2.23 follows that filter order is calculated by Equation 2.24. This gives filter order of 2.

$$\boxed{n = \frac{log(\frac{10^{\frac{-G_{stop,dB}}{10}} - 1}{10^{\frac{-G_{pass,dB}}{10}} - 1})}{2 \cdot log(\frac{\omega_{stop}}{\omega_{pass}})}} \tag{2.24}$$

$$\boxed{n = \frac{log(\frac{10^{\frac{40}{10}} - 1}{10^{\frac{3}{10}} - 1})}{2 \cdot log(\frac{11.4 \cdot \text{kHz}}{1 \cdot \text{kHz}})} = 1.89327 \approx 2} \tag{2.25}$$

Filter requirements can be checked by Equations 2.27 and 2.27.

$$\boxed{\omega_{cutoff} = \frac{\omega_{pass}}{(10^{\frac{-G_{pass,dB}}{10}} - 1)^{\frac{1}{2 \cdot n}}}} \tag{2.26}$$

$$\boxed{\omega_{cutoff} = \frac{\omega_{stop}}{(10^{\frac{-G_{stop,dB}}{10}} - 1)^{\frac{1}{2 \cdot n}}}} \tag{2.27}$$

From Equation 2.27 follows that ω_{cutoff} for $G_{stop,dB} = -40dB$ at ω_{stop} gives $\omega_{pass} = \frac{7163.01\ rads/s}{2\cdot\pi} = 1.14$kHz (Equation 2.28). It can be seen that filter bandwidth is slightly off required bandwidth of 1kHz. Decision must be made to either match exactly passband or stopband requirements.

$$\boxed{\omega_{cutoff} = \frac{2\cdot\pi * 11.4\cdot \text{kHz}}{(10^{\frac{40}{10}}-1)^{\frac{1}{2\cdot 4}}} = 7163.01\ rads/s} \tag{2.28}$$

From Equation 2.26 follows that to match exact passband requirements ω_{cutoff} must be 6290.65 $rads/s$ (Equation 2.29).

$$\boxed{\omega_{cutoff} = \frac{2\cdot\pi * 1\cdot \text{kHz}}{(10^{\frac{3}{10}}-1)^{\frac{1}{2\cdot 4}}} = 6290.65\ rads/s} \tag{2.29}$$

Since filter has only order of 2, single stage will be sufficient. Note that filters higher order are cascaded in more stages, where single stage has either order of 1 or 2. Poles of the filter are calculated by Equation 2.30 which gives two poles (at $s_{1,2} = -\frac{1}{\sqrt{2}} \pm j\frac{1}{\sqrt{2}}$). Normalized ($\omega_{cutoff}$ = 1) transfer function is shown in Equation 2.31 [40].

$$\boxed{S(k) = \exp^{\frac{j\pi}{2n}(2k+n-1)}} \tag{2.30}$$

$$\boxed{H(s) = \frac{1}{(s+\frac{1}{\sqrt{2}}+j\frac{1}{\sqrt{2}})(s+\frac{1}{\sqrt{2}}-j\frac{1}{\sqrt{2}})} = \frac{1}{s^2+1.41421s+1}} \tag{2.31}$$

Normalized filter function must be scaled to cut-off (ω_{cutoff}) frequency. This is done by replacing s variable in Equation 2.31 by $\frac{s}{\omega_{cutoff}}$.

$$\boxed{H(s) = \frac{1}{(\frac{s}{\omega_{cutoff}})^2+1.41421(\frac{s}{\omega_{cutoff}})+1}.} \tag{2.32}$$

Final scaled system function is calculated by Equation 2.32 where for cut-off value calculated in Equation2.29 is used. This gives following scaled system function:

$$\boxed{H(s) = \frac{1}{2.52702 \cdot 10^{-8} \cdot s^2 + 0.000225 \cdot s + 1}} \tag{2.33}$$

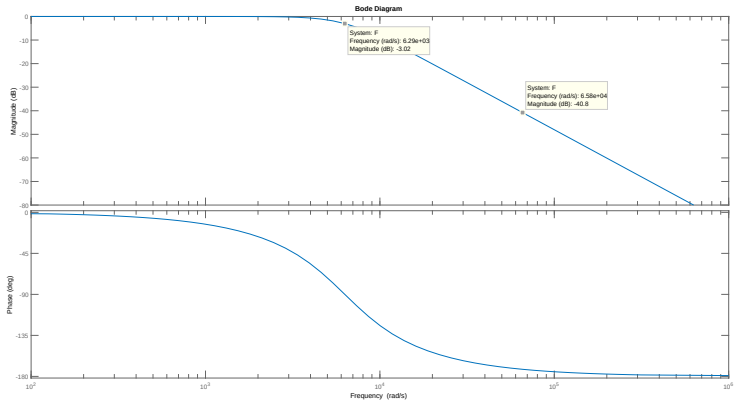


Figure 2.22.: MATLAB Bode Plot of normalized filter transfer functions

For implementation of Butterworth filter Sallen-Key circuit (Figure 2.23) is used (Figure 2.23) [40]. Transfer function of the circuit for special case where $\alpha = 1$ is given by Equation 2.34.

$$\boxed{H(s) = \frac{1}{C_1 C_2 R_1 R_2 \cdot s^2 + C_2(R_1 + R_2) \cdot s + 1}} \tag{2.34}$$

By comparing coefficients of Equations 2.33 and 2.34 follows:

$$C_1 C_2 R_1 R_2 = 2.52702 \cdot 10^{-8}$$
$$C_2(R_1 + R_2) = 0.000225$$

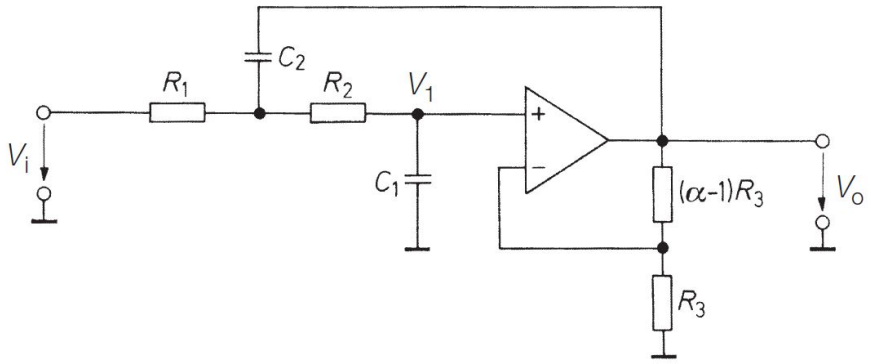


Figure 2.23.: Sallen-Key filter [40]

Element	Value	Unit
$C_{1,1}$	10	nF
$C_{1,2}$	20.5	nF
$R_{1,1}$	9.53	kΩ
$R_{1,2}$	13	kΩ
OPAMP	TI-OPAx836	

Table 2.10.: Selected Butterworth filter elements.

Q-factor for Sallen-Key filter is defined by Equation 2.35. This quantity defines amplitude magnitude of the filter at ω_{cutoff} frequency. For $Q \leq 0.5$ the filter is said to be "overdamped" and is unusable, but also filter with large Q-factor tends to be unstable [40].

$$\boxed{Q = \frac{\sqrt{R_1 R_2 C_1 C_2}}{C_1(R_1 + R_2)}} \tag{2.35}$$

Figure 2.24 shows Butterworth-Filter constructed with single Sallen-Key. The used operational amplifier is Texas Instruments OPA836.

Stage	Q-factor
First	0.707349

Table 2.11.: Calculated Q-factors for filter stages

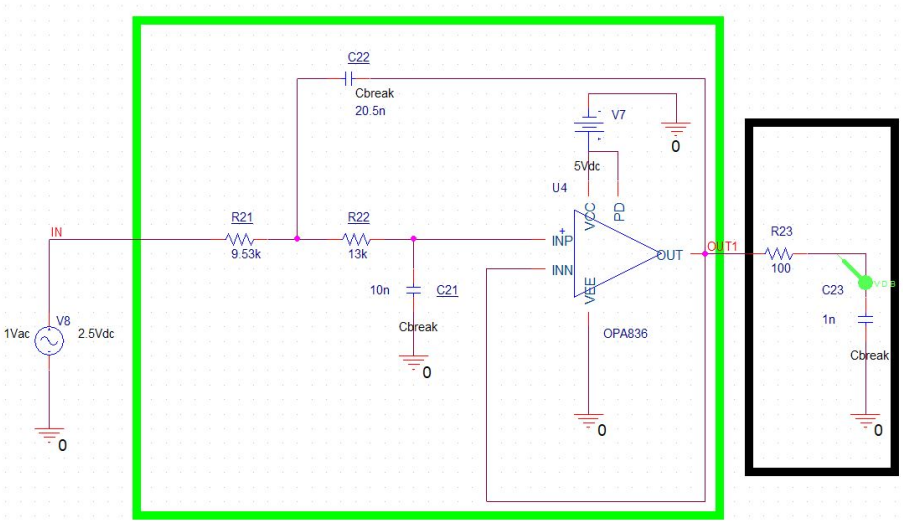


Figure 2.24.: Pspice simulation of Butterworth-Filter (green box) and ADC Front End Filter (black box) constructed with single TI-OPA836

Note that Frond End and Butterworth Filter can be constructed with single operational amplifier.

Simulation of the constructed filter using PSpice can be seen in the figure 2.25

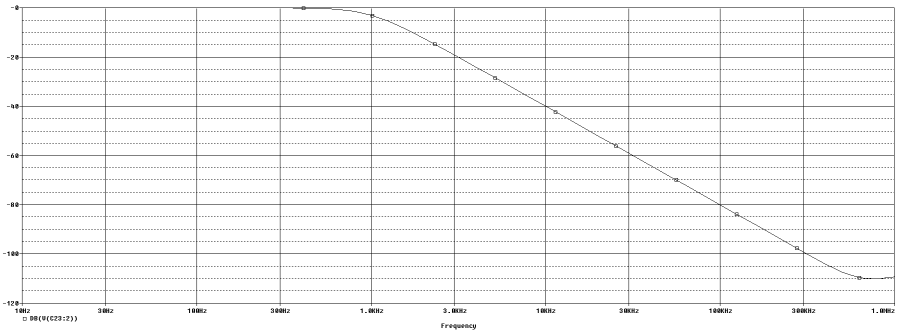


Figure 2.25.: Bode plot of constructed circuit (Figure 2.24)

2.6. SMART Switch - VN7016AJ

VN7016AJ is high-side driver for automotive applications. It is capable of driving resistive, inductive and capacitive loads. Operating voltage range is between 4V - 28V and can deliver up to 77A of current. Chip also supports so-called multi sense diagnostic feature where multiplexed analog feedback can be used to measure precisely load current, supply voltage and chip temperature. Analog feedback is controlled by 3V and 5V compatible CMOS inputs. High-side driver supports also various protection mechanisms like undervoltage shutdown, load current limitation, overtemperature protection, overpower protection etc [37].

2.6.1. Diagnostic over Multisense

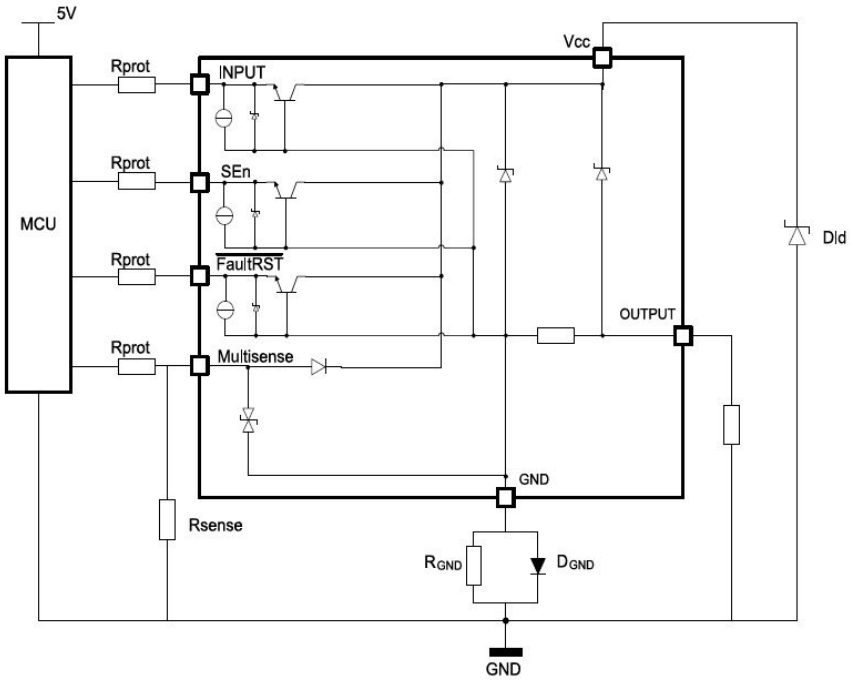


Figure 2.26.: Simplified internal structure of VN7016AJ [37]

Pins SEn, $SEL0$ and $SEL1$ control the Multisense output. SEn enables or disables diagnostic output where pins $SEL0$ and $SEL1$ are used to select measurement of interests. This multiplexed analog output gives current proportional to selected diagnostic which can be either load current, supply voltage or chip temperature [37].

SEn	$SEL0$	$SEL1$	Function
L	X	X	High Impedance
H	L	L	In normal mode (Load Current): $I_{SENSE} = \frac{1}{K} \cdot I_{OUT}$
H	L	H	In normal mode (Load Current): $I_{SENSE} = \frac{1}{K} \cdot I_{OUT}$
H	H	L	Chip Temperature $V_{SENSE} = V_{SENSE_TC}$
H	H	H	Supply Voltage $V_{SENSE} = V_{SENSE_VCC}$

Table 2.12.: Multisense output selection [37]

2.6.2. Load Current

Load current diagnostic in selected according Table 2.12 and is given by Equation 2.36 where factor K depends on output current and varies between 2500 - 5500 [37].

$$\boxed{I_{OUT}(V_{SENSE}) = K \cdot \frac{V_{SENSE}}{R_{SENSE}} = K \cdot \frac{V_{ADC}}{1\text{k}\Omega} \quad [\text{A}]} \tag{2.36}$$

2.6.3. Supply Voltage

Supply voltage diagnostic is selected according Table 2.12 and is equal to $V_{SENSE} = \frac{V_{CC}}{4}$. But V_{SENSE} voltage contains also voltage drop on protection circuit (Figure 2.26, voltage drop across parallel D_{GND} and R_{GND}) which must be subtracted from measured V_{sense} voltage [37]. This voltage drop is approximately 0.247V on development board used in this master thesis. Supply voltage si calculated by Equation 2.37

$$\boxed{V_{SUPPLY}(V_{ADC}) = \frac{V_{ADC} - V_{PROT}}{4} = \frac{V_{ADC} - 247\text{mV}}{4} \quad [\text{V}]} \tag{2.37}$$

2.6.4. Chip Temperature

Chip Temperature diagnostic is selected according Table 2.12 and is given by Equation 2.38 where $\frac{dV_{SENSE}}{dT}$ is typically -5mV for temperature range between -40°C to 150°C. For normal room temperature (25°C) T_0 is equal to 2.07V according chip specifications [37]. If these values are plugged in Equation 2.38 temperature as function of measured voltage can be calculated by Equation 2.39. Note that from measured voltage, voltage drop across protection diode must be subtracted [37].

$$\boxed{V_{SENSE}(T) = V_{SENSE}(T_0) + \frac{dV_{SENSE}}{dT} \cdot (T - T_0)} \tag{2.38}$$

$$\boxed{T_{CHIP}(V_{ADC}) = (25°\text{C} + 273.15°\text{C})K + \frac{2.07\text{V}}{5\text{mV}} - \frac{(V_{ADC} - 247\text{mV})}{5\text{mV}} \quad [\text{K}]} \tag{2.39}$$

2.7. Temperature Measurement with TC1047A

TC1047A is linear voltage sensor, whose output voltage is directly proportional to measured temperature. Sensor has temperature range of -40°C to $+125$°C. At -40°C sensor has output voltage 100mV, at 0°C 500mV, at 25°C 750mV and at 125°C 1.75V (Figure 2.27) [29].

Using linear equation $y = m \cdot x + b$ temperature function is derived. Coefficient m represent slop which is calculated by $m = \frac{125°\text{C} - (-40°\text{C})}{1.75\text{V} - 100\text{mV}}$ and gives 100. Coefficient b is calculated by setting $0 = 100 \cdot 500\text{mV} + b$ which gives -50. Temperature is calculated by Equation 2.40.

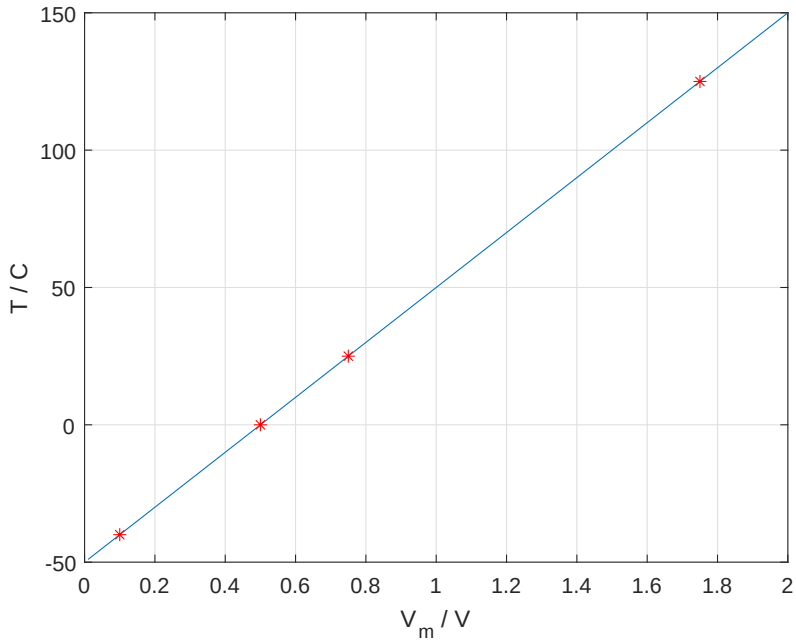


Figure 2.27.: TC1047A temperatur as a function of voltage

$$\boxed{T(V_{ADC}) = 100 \cdot V_{ADC} - 50 \ \ [°\text{C}]} \tag{2.40}$$

2.8. Serial Peripheral Interface - SPI

Serial peripheral interface (SPI) is a module that allows a full duplex synchronous, serial communication over short distance. Primarily used in embedded systems for on PCB intercommunication. SPI was developed by Motorola in the mid 1980s and was accepted by various IC integrators. Its master-slave bus topology allows single master and multiple slave devices, where master originates the frame and multiple slaves are selected trough individual slave

select lines. SPI uses four lines for data transmission: MOSI (Master Out Slave In), MISO (Master In Slave Out), SCK (Slave Clock) generated by master and SS (Slave Select) which during communication is pulled low. Because SPI lacks standard different vendors took different implementation approach [30].

2.9. I2C

Inter-Integrated Circuit (I2C) is a multi-master, multi-slave serial bus for interconnecting devices over short distance. Data transmission requires only two lines SDA and SCK [24].

2.10. Electromagnetic Compatibility - EMC

Electromagnetic compatibility is ability of a electronic device to function in electromagnetic environment within specified EMC directives. Main goal of EMC test is to make sure electronic system do not interfere with other electronic systems in terms of Electromagnetic Interference (EMI) such that other systems are unable to operate correctly. Test falls into two major categories: Electromagnetic Compatibility (EMC) and Electromagnetic Immunity. Electromagnetic Immunity is opposite of EMC, where newly developed product should stay fully operational despite Electromagnetic Interference coming from its environment. Levels of emission and immunity are defined by different directives [15].

2.10.1. EMI Coupling Mechanisms

There are different number of source from where EMI can arise. Some of potential sources are *naturally occurring EMI* (lightning and cosmic noise), *Impulse noise EMI* (Electrostatic Discharge (ESD), Switching Systems - AC inductive loads etc.). EMI sources can be classified by their bandwidth where they can have narrow band or broadband.

Electromagnetic interference from the source to the receiver is either *radiated*, *conducted* or *coupled*. Radiated coupling occurs when the source and the

receiver are far from each other and they interfere in terms of electromagnetic waves. Conducted coupling is categorized into common mode (monopole type) and differential mode (Figure 2.28). Coupled interference occur either by capacitive, inductive or common impedance coupling.

In electronic device, most of electromagnetic emission is radiated by Printed Board Circuit (PCB) and to it attached cables. Emission noise can be reduced by proper layout techniques and shielding. Solution for preventing emissions is to understand the source of emission, the coupling mechanism but also susceptibility of the victim, the level of interference it can take. EN 61000 is an example of EMC directive which specifies emission standards, testing and measurement techniques for different area of appliance [15, 5].

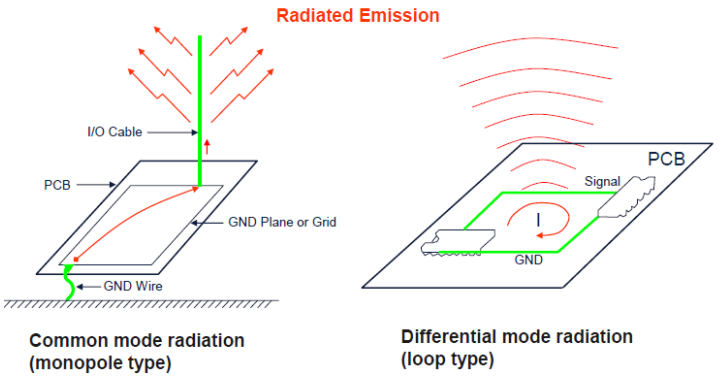


Figure 2.28.: PCB radiation types [5]

Emission preventing mechanism should be considered in early stage of device development. Following aspects are to be considered when designing new system [5]:

1. PCB Layer: having more layer can significantly decrease potential emission problems
2. Placement of Connectors: example I/O and power connectors should be on the same side of PCB
3. PCB Floor-planning: All components of particular group should be in the same zone (analog, digital zone ...)

4. Noisy parts and sensitive parts should be fare from each other
5. Big loops in power supply should be avoided (PCB without ground plane), could be prevented by routing power and ground plane simultaneously and as close as possible
6. Slots in power and ground plane should be avoided (example slots created by vias)
7. High speed signals should stay on the same layer (vias could be source of radiation)

Interference prevention elements are resistors, capacitors (bypassing capacitor, decoupling capacitors), inductors, Transient Voltage Suppressor diodes (TVS), varistor (voltage-dependent resistor), common mode chokes etc. Real capacitors are series resonant circuits and special care should be taken when selecting them. Depending on noise frequency, inductive part of them could become dominant or even start to oscillate. The same appliance for inductors. EMC immunity of metal film resistors should also be considered since under electro static discharges, these resistors could get highly resisted. TVS-diodes should be avoided in high speed signals because of high parasitic capacity that they have [15, 5].

Concerning automotive domain, here are all 12V-Power-Network characteristic impulses according DIN/ISO 40 839 are [10]:

- E1: occurs when parallel inductive loads is shut down
- E2: occurs when serial inductive loads is shut down
- E3: occurs due to parasitic capacitance and inductance in cables when switching occurs
- E4: voltage drop when engine is started
- E5: known as ”Load Dump”, occurs when the battery is disconnected from the alternator

2.11. Real Time Operating Systems - RTOS

Real time operating systems (RTOS) compared to conventional OS are special OS where real time is requirement. Given that system has n tasks with its deadlines, RTOS must be able to execute all task before deadline of each has been reached. Real time also means that if system is event trigger, it must react

in a given time otherwise some catastrophic consequences could happen. Such system have special scheduling algorithms like Earliest Deadline First (EDF), First Come First Serve (FCFS), Priority Based Scheduling etc. Beside different scheduling policies, RTOS provide Synchronisation-Management (Semaphore, Mutex, Events ...), Intertask Communication-Management(Messages Queues, Mailboxes, Pipes ...) etc. An example of RTOS is so-called Free RTOS and some of basic features that Free RTOS provides are [4]:

Priority Based Scheduling: A task with a higher priority (higher decimal number) has precedence over the task with a lower priority (lower decimal number).

Task Management: Ability to create static and dynamic tasks. Usually only static tasks are used in hard real time systems, because creation of dynamic task could lead to infeasible scheduling and break down of a system.

Task Synchronisation Mechanism: Mutex and Semaphore for resources protection (variables, thread unsafe code, SPI, I2C etc.) and task synchronisation. Beside primitive synchronisation mechanisms Free RTOS supports queues for inter-task communication and data transfer.

2.12. Model Based Software Development with SIMULINK

Model based software development in this master thesis is based on so-called Gigatronik Blockset. It is set of MATLAB scripts and custom Simulink blocks that allow generation of C code by using SIMULINK models. Some of original Blockset features are listed below [14]:

- Creation of Tasks
- Task management (priority, cycle time, stack size)
- CAN configuration (speed, interface)
- Creation of CAN signals from DBC file
- LIN configuration
- Creation of LIN signals from LDF file
- Creation of LIN scheduling table
- Build configuration

Original Blockset is tightly coupled to "Green Hills MULTI" compiler, but since compiler used in this master thesis is "IAR RH850", parts of original Blockset specially those for build configuration were completely overwritten. Beside build incompatibility issue, original Blockset was mostly based on communication buses and did not have features for ADC, Display support etc. New Blockset was not only extended to support new features but also changed behaviour of most existing features like IO management, Debug-LED etc. Please note that model based software development here generates only parts of C-code. These parts are mostly C configuration files that influence overall system behaviour, device driver initialization, hardware control code like for example I2C OLED display etc. User application C-code is generated completely from MATLAB Simulink model. Following examples shows required steps to implement custom MATLAB Simulink block. Custom block in SIMULINK can be created by *S-Function Builder*. In the graphical tool number of input and output parameters can be specified as well the name of S-function. Let suppose custom block for OLED display control is required. Assuming that it is already implemented in a system and can be directly controlled by C code. Let suppose text from custom block is given in the same format as C-printf-function uses ("Signal %d", 23). Code Listing 2.1 shows C operation required for writing some text to the defined display line. It involves text formatting, clearing selected display line (display memory) in case it already contains some text and finally writing new formatted text.

```
/*format string*/
sprintf(simulnik_model_display_temp_buff,
"SOME_TEXT",
DISPLAY_LINE);

/*clear display*/
Display_clrLine(DISPLAY_LINE);

/*write formated buffer to the display*/
Display_setStringXY(0x00u,
DISPLAY_LINE,
simulnik_model_display_temp_buff);
```

Listing 2.1: C code for display control

The goal is to have custom MATLAB Simulink block which when used in Simulink model produces exactly C code shown above which is customized in terms of parameters: TEXT and DISPLAY-LINE. Beside parameters, the generated C-code for display control must be placed in correct place (C file) in overall generated C code. Figure 2.29 shows display block.

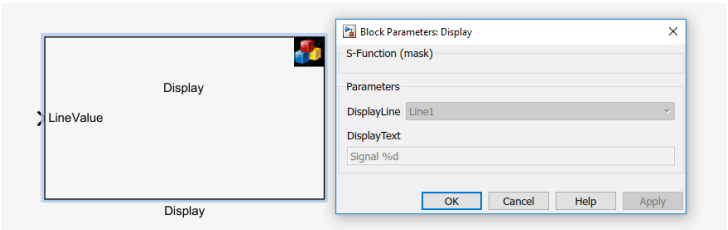


Figure 2.29.: SIMULINK custom block for display control

Listening 2.2 shows corresponding S-Function for the custom block. The most crucial part of it is *mdlRTW* method which pulls input parameters (DisplayText and DisplayLine) from custom block and stores them in Simulink Coder formerly known as Real-Time Workshop (RTW).

```
/*
file: sfc_Display.c
*/

#define S_FUNCTION_NAME  sfc_Display
#define S_FUNCTION_LEVEL 2


#define NPARAMS                 ssGetSFcnParamsCount(S)
#define SAMPLE_TIME_0           INHERITED_SAMPLE_TIME
#include "simstruc.h"


/*====================*
* S-function methods *
```

```
*====================*/
static void mdlInitializeSizes(SimStruct *S)
{


}

static void mdlInitializeSampleTimes(SimStruct *S)
{
ssSetSampleTime(S, 0, SAMPLE_TIME_0);
}


static void mdlOutputs(SimStruct *S, int_T tid)
{

}


static void mdlTerminate(SimStruct *S)
{

}


/*
*
* writes s-function parameters
to rtw file to access them later through tlc
*/
static void mdlRTW(SimStruct *S)
{
int_T  displayLine,buflen;
const char_T *displayText;

/*GET DISPLAY LINE*/
displayLine=mxGetPr(ssGetSFcnParam(S, 0))[0];
```

```
/*GET DISPLAY TEXT*/
displayText = mxMalloc(50);
mxGetString((ssGetSFcnParam(S, 1)),
displayText,50);



/***********************************/
/*writing parameters into *.rtw*/
if (
!ssWriteRTWParamSettings(
S,
2,
SSWRITE_VALUE_DTYPE_NUM,"
displayLine",&displayLine,DTINFO(SS_INT8, 0),

SSWRITE_VALUE_QSTR,"displayText",displayText
))
{

mxFree(displayText);
return;
}
mxFree(displayText);
return;
}

#endif /* MDL_RTW */
#ifdef  MATLAB_MEX_FILE
#include "simulink.c"
#else
#include "cg_sfun.h"
#endif
```

Listing 2.2: S-Function for custom display block

S-Function code must be compiled inside MATLAB before it can be used. Compiling is done by MATLAB-supported compiler. Syntax for compiling this example would be "mex sfc_Display.c". In order to generate code for compiled S-function, Target Language Compiler (TLC) file must be written which is shown in Listening 2.12. Method *Outputs* fills in predefined C template with previously stored values in RTW.

```
%implements "sfc_Display" "C"

/*GENERATE C CODE*/

%function Outputs(block, system) Output

%assign displayText=SFcnParamSettings.displayText
%assign displayLine=SFcnParamSettings.displayLine
%assign u=LibBlockInputSignal(0, "", "", 0)

sprintf(simulnik_model_display_temp_buff,
"%<displayText>",
%<u>);

Display_clrLine(0x0%<displayLine>u - 1);

Display_setStringXY(0x00u,
0x0%<displayLine>u - 1,
simulnik_model_display_temp_buff);

%endfunction
```

2.13. Ethernet

Ethernet is communication standard used for connecting local computer and other devices in so-called local area networks (LAN). Typical Ethernet

interface is composed of Medium Access Control (MAC) and Physical Layer (PHY). Both are standardised into the standard IEEE 802.3. Physical layer of modern Ethernet interface uses two pairs of twisted wires. This allows data to travel in both direction simultaneously knows as full-duplex mode. MAC layer is usually integrated into MCU where PHY is stand-alone chip. MAC and PHY are connected through standardized interface know as Media Independent Interface (MII) [44]. MCU which does not have integrated MAC controller and need Ethernet interface can use stand-alone Ethernet controller like for example Mircohip ENC424J600. Microchip ENC424J600 is IEEE 802.3 compliant Fast Ethernet Controller with integrated MAC and PHY. Connection to MCU is done either over SPI or parallel interface [17].

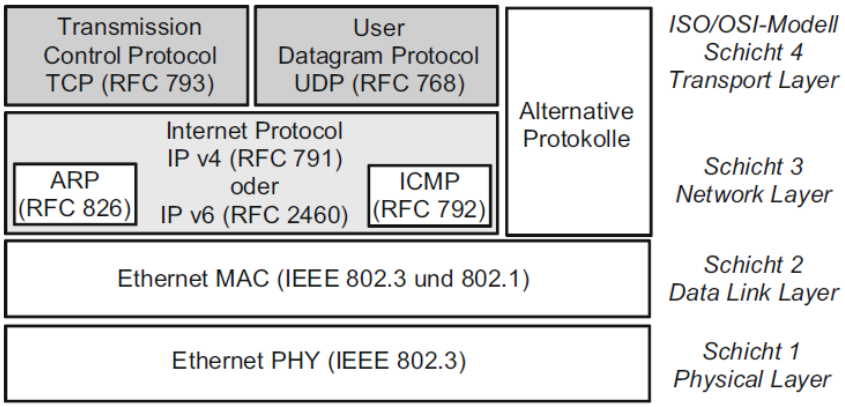


Figure 2.30.: Open Systems Interconnection - OSI

Figure 2.30 shows Open Systems Interconnection (OSI) model in which PHY and MAC are the first two layers. In embedded systems widely used open-source TCP/IP stack (OSI Network layer and up) is LightWeight IP (LwIP) stack. LwIP supports Transmission Control Protocol (TCP), User Datagram Protocol (UDP), Internet Protocol v4 and v6 (IPv4 and IPv6) etc. Three different APIs are available:

- Raw API
- Netconn API

- BSD Socket API

Raw API is native LwIP API where applications (XCP on IP, http, ftp ..) are implemented by using callbacks. Netconn API provides socket support but requires real-time operating system (RTOS). BSD Socket API is build on top of Netconn API and provides Berkeley-like sockets [35].

2.14. XCP

XCP stands for measurement and calibration protocol. It is based on CCP (CAN Calibration Protocol) which was developed in 1990s. Because CCP was limited to CAN bus systems, XCP was introduced which is more generalized version of CCP where protocol was independent from physical layer and could be used in different bus systems like XCP on Ethernet (TCP/IP and UDP/IP), XCP on SPI, XCP on I2C, XCP on CAN, XCP on CAN FD etc. Main purpose of XCP is that it allows read and write of MCU memory. Memory address locations also known as characteristic or measurement, which are described in so called A2L-file format [3]. Listing 2.3 shows an example of measurement named $WINKLER_DWork.SW_CURRENT_mA$ which is located in MCU at address $0xFEDF207A$. This measurement occupies 16 bits and should be interpreted by XCP-master as unsigned value which can store values between 0 and 65535. Another example shows characteristic named $WINKLER_DWork.SW_ENABLE$ which is 8 bits wide, located at $0xFEDF2085$ and can store value between 0 and 255 (Listing 2.4). Measurement is usually read-only where characteristics are meant to be written by XCP-master. Both examples are extracted from A2L file, which were used in system test bench setup for the control of a SMART switch. Characteristic was used to turn the switch on or off, meaning it was directly in relation to digital IO pin and measurement was used to read current through the switch, which was ADC measured value. A2L file can be generated from firmware hex image using MATLAB or Vectors Informatik CANape tool. XCP is master slave protocol, where slave have single master and master can have multiple slaves. Data (Measurement) can be either acquired by polling or synchronous data acquisition (DAQ) method. Polling is done by sending periodic requests from the XCP master to the slave. This has drawback that for each acquired data two messages (request and response) must be sent. To overcome this disadvantage

DAQ is used. In DAQ configuration phase, XCP-master lets the slave know which data need to be send. XCP-slave saves data in a buffer and sends them out. Data Transmission to XCP-slave is realized by STIM method which is very similar to DAQ but works in opposite direction [3].

```
/begin MEASUREMENT WINKLER_DWork.SW_CURRENT_mA ""
UWORD NO_COMPU_METHOD 0 0 0 65535
ECU_ADDRESS 0xFEDF207A
ECU_ADDRESS_EXTENSION 0x0
FORMAT "%.15"
/begin IF_DATA CANAPE_EXT
100
LINK_MAP "WINKLER_DWork.SW_CURRENT_mA"
0xFEDF207A 0x0 0 0x0 1 0x8F 0x0
DISPLAY 0 0 65535
/end IF_DATA
SYMBOL_LINK "WINKLER_DWork.SW_CURRENT_mA" 0
/end MEASUREMENT
```

Listing 2.3: A2L example of measurement

```
/begin CHARACTERISTIC WINKLER_DWork.SW_ENABLE ""
VALUE 0xFEDF2085 __UBYTE_S 0 NO_COMPU_METHOD 0 255
ECU_ADDRESS_EXTENSION 0x0
EXTENDED_LIMITS 0 255
FORMAT "%.15"
/begin IF_DATA CANAPE_EXT
100
LINK_MAP "WINKLER_DWork.SW_ENABLE"
0xFEDF2085 0x0 0 0x0 1 0x87 0x0
DISPLAY 0 0 255
/end IF_DATA
SYMBOL_LINK "WINKLER_DWork.SW_ENABLE" 0
/end CHARACTERISTIC
```

Listing 2.4: A2L example of characteristic

Listing 2.5 shows C code generated by MATLAB Simulink. Both A2L values shown in Listing 2.3 and 2.4 are generated from this code (SW_ENABLE and SW_CURRENT_mA). Note that A2L file is generated from code executable file and not code source file. A2L requires variable memory location which is assigned by Linker during compile process.

```
typedef struct {
boolean_T SW_ENABLE;
uint16_T SW_CURRENT_mA;
int8_T SW_TEMPERATUR_C;
uint8_T SW_VOLTAGE_V;
uint8_T SW_FRST;
boolean_T EnableADCUnit;
uint16_T ADC1;
} D_Work_WINKLER;
```

Listing 2.5: MATLAB Simulink generated C code

3. System Design

The process of device construction is divided into following phases:

Hardware Design:

1. Identification and selection of required electronic components
2. Circuit design, fulfilment of requirements and specifications
3. PCB design and fabrication
4. PCB assembly and initial hardware operation

Software Design:

1. Software Toolchain: modification of GT-Toolchain (porting to IAR RH850 compiler)
2. Integration of new modules: further development of GT-Toolchain (integration of LWIP, I2C OLED, ADC ...)

System Testing:

1. System test (Hardware and Software basic tests)
2. System integration and testing with SMART Switch
3. Data visualisation with CANape, CANoe and custom Java Application
4. EMC and EMI test.

In this master system software was considered ”beyond the scope” and is only briefly covered. This will include software architecture and hardware-software interaction. Detailed system implementation is presented in the Chapter 4. Chapter 5 covers validation and testing of the constructed system.

3.1. Hardware

For fulfilling requirements discuses in the Section 1 hardware architecture of the system was decomposed into Functional Groups (FG) (Figure 3.1). Each functional group has a scope of operation and set of functions.

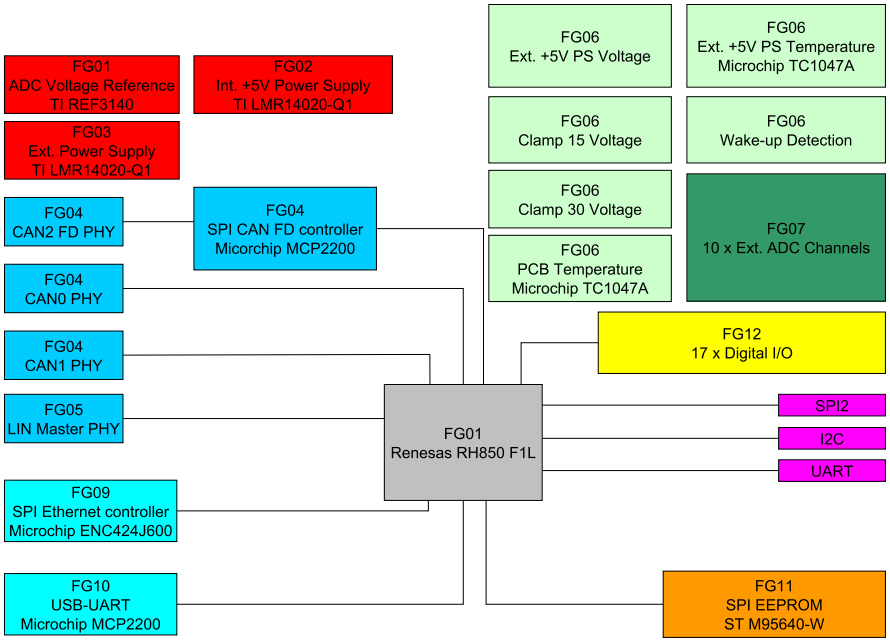


Figure 3.1.: System concept

The below listening shows all hardware functional groups:

- **FG01:** All functions/requirements related with MCU
- **FG02:** All functions/requirements related with system internal power supply (excluding ADC voltage supply)
- **FG03:** All functions/requirements related with external power supply
- **FG04:** Physical interface of all available CAN channels including external CAN FD controller

- **FG05:** Physical interface of LIN master channel
- **FG06:** All functions/requirements related to internal measurements like PCB temperature, Clamp-30/15 voltages etc.
- **FG07:** All functions/requirements related to external ADCs (Signal condition, ESD protection, Enable switch etc.)
- **FG08:** On-board connectors and expansion buses
- **FG09:** All functions related to external Ethernet controller
- **FG10:** USB to UART protocol converter
- **FG11:** EEPROM
- **FG12:** Digital I/O and ESD protection circuit
- **FG13:** External connector (D-Sub 37) and debug LED

3.1.1. FG01 - Microcontroller

Selected MCU for this system was Renesas RH850 F1L. Short summery about MCU architecture and its features can be found in Section 2.1. This group includes on-chip debugging interface which is described in Section 2.1.4. Further functions included in this group are ADC voltage reference (for detailed information about voltage reference please refer to the Section 2.2.4), CPU clock and I/O pin assignment. Detailed assignment of I/O is included in Appendix A.1. CPU clock related information and crystal requirements are discussed in Section 2.1.3. Absolute maximum ratings related to supply and ADC reference voltage are found in Section 2.1.2 and 2.2.4. ADC voltage reference was constructed with Texas Instruments REF3140. Considering that ADC is 12-bits and reference voltage is 4.096V this gives a resolution of 1mV/*bit*

3.1.2. FG02 - Internal +5V Power Supply

Input voltage of a system (Clamp-30) can vary between 6V and 40V. Considering automotive 12V power network characteristic impulses (for detailed information about impulses please refer to the Subsection 2.10.1) system should be protected against E5 impulse known as ”load dump”. Clamp-30 protection circuit combines load **dump protection** which was implemented with TDK EPCOS-B72650M0400K072 varistor, **overvoltage protection** implemented with TVS diode (breakdown voltage 44.4V to 49.1V) and **reverse**

voltage protection implemented with Vishay SS34 (maximal forward rectified current 3A)(see Section 2.10 and Section 2.10.1). Clamp-15 has similar protection circuit since it can be connected to the same source as Clamp-30. Overall internal system uses single positive $5V$ power supply. Exceptions are Ethernet interface, which uses positive $3.3V$ and CAN/LIN transceivers which beside positive $5V$ need also battery power line (VBAT). Calculated power consumptions for positive $5V$ and $3.3V$ power supplies are shown in Table 3.1. Internal $5V$ voltage regulation was constructed with Texas Instrument LMR14020-Q1 step-down converter. Main reason for having switched mode power supply is a power efficiency (see Section 2.2 for more information about power supplies). For detailed $5V$ power supply construction see Section 2.2.2. $3.3V$ power supply was constructed with linear voltage regulator and is discussed in Section 3.1.9.

IC	I_{max} [mA] @ 5V	I_{max} [mA] @ 3V3	Total [mW]
RH850 F1L EVCC	60		
RH850 F1L A0VREF	48		
RH850 F1L REGVCC	undefined		
MCP2517FD	20	-	
TC1047A	0.06	-	
REF3140	25	-	
15 x TLV34xx	15 x 0.2	-	
ENC424J600	-	300	
TXB0104	100	-	
M95640-W	5	-	
3 x TJA1043	3 x 65 + 3 x 0.5	-	
MCP2200	-	-	
TJA1021	-	-	
2 x SP0504S	-	-	
TOTAL	457.56	300	3587.8

Table 3.1.: Calculated total system power consumption [33, 28, 29, 20, 22, 17, 23, 36, 7, 18, 25, 26]

In order to fulfil desired requirement of power-save (sleep) function, positive $5V$ power supply can be turned on and off. Therefore electrical switch was constructed which enables activation of power supply by external source.

Available sources are Clamp-15, internal sources CAN/LIN transceivers and MCU. Detailed switch construction is discussed in Section 2.2.3. All wake-up sources except MCU power-hold are configurable through external jumpers. Figure 3.2 shows concept of power supply switch. Initially power supply is activated by external Clamp-15 (high) or INH signal from LIN/CAN transceivers after which MCU sets power-hold signal. This signal holds power supply activated independent if any other source is active or not. If the system decides to turn itself off (Clamp-15 must be low or deactivated) in order to save power, LIN/CAN transceiver are put into sleep mode and MCU deactivates the power supply through MCU power-hold signal. System can be woken up by any communication on LIN/CAN bus or by Clamp-15. Detection of wake-up source is described in Section 3.1.6.

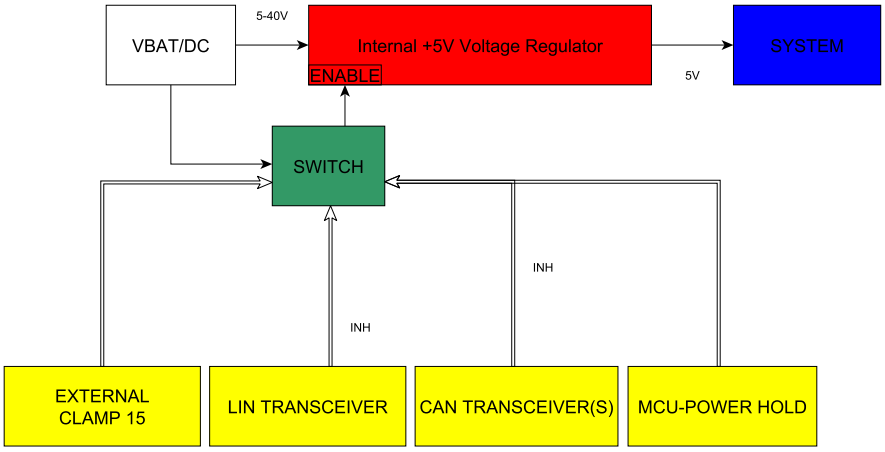


Figure 3.2.: +5V power supply switch

3.1.3. FG03 - External +5V Power Supply

System features external +5V power supply which was constructed with the identical step-down converter as the internal power supply unit (Section 3.1.2). Supply can deliver up to 10W of power and its purpose is to supply potential external add-on modules. Unlike internal supply, this PS is only controllable

(on/off) by MCU. Further features of this supply are voltage and temperature monitoring by MCU. Supply unit is also protected by ESD circuit. Temperature monitoring was constructed with TC10475 linear voltage sensor which is discussed in Section 2.7. Monitoring of a voltage was constructed with voltage divider which acts as a level shifter for ADC input of the RH850 integrated SAR ADC (Section 2.5).

3.1.4. FG04 - CAN Interfaces

High speed CAN controllers are integrated directly into RH850 MCU (See Section 2.1). Detailed information about CAN bus are found in Section 2.3. In order to provide CAN-FD bus (Section 2.3.3) and because this MCU lacks CAN-FD controller, Microchip MCP2517FD external CAN-FD controller was used. Communication between MCU and CAN-FD was implemented through SPI bus (Section 2.8). System features total three CAN channels. Two high speed and one CAN/CAN-FD channel. This enables the system to be used as gateway. Either to connect CAN nodes/networks with different baud rates together or CAN nodes/networks which may be incompatible with CAN-FD protocol. Physical layer of all three controllers was constructed with similar NXP TJA1043 CAN transceivers (Section 2.3.1). In sleep mode any of transceivers can trigger wake-up request (Section 3.1.2). Each CAN transceiver is terminated with 120Ω resistors and features ESD protection (NXP PESD1CAN). In case network does not need termination, assembly of resistors must be avoided.

3.1.5. FG05 - LIN Master Interface

RH850 has integrated LIN controllers (Section 2.1). This system has only one LIN master channel available. Detailed information about LIN bus is found in Section 2.4. Physical layer was implemented with NXP TJA1021 transceiver (Section 2.4.1). Note that selected LIN controller of RH850 can only be used as LIN master independent if LIN transceiver is terminated for slave or master use. Like CAN, LIN transceiver can also trigger wake-up request (Section 3.1.2).

3.1.6. FG06 - Internal Measurements

This functional group consists of all internal measurements. This includes Clamp-30 (VBAT), Clamp-15 voltages and PCB temperature. Both Clamp-30 and 15 voltage monitoring are constructed in the similar manner with voltage divider that acts as a level shifter and dedicated ADC channel (Section 2.5). PCB Temperature monitoring is constructed with TC10475 linear voltage sensor which is discussed in Section 2.7. Filtering is constructed with Texas Instruments TLV34xx operational amplifier.

3.1.7. FG07 - External ADC Channels

External ADC channel chain consist of ESD prtection circuit, voltage follower, second order low pass filter and charge bucket filter. Brief discussion of signal conditioning (low pass filter) as well charge bucket filter can be found in Section 2.5. All ten external ADC channels are accessible through SMA connectors. Please note that original system design was implemented with Texas Instruments TLV34xx operational amplifiers but since they do not provide sufficient bandwidth for charge bucket filters, Texas instruments OPA836 operational amplifier was used as a replacement (Section 2.5.1). All operational amplifier can be turned off by MCU to reduce power consumptions. Beside that operational amplifier can be individually turned off by external jumpers. Considering maximal input voltage, all amplifiers use single-supply (+5V) and have rail-to-rail output, but since ADC uses voltage reference of 4.096V that gives maximal input voltage of only 4.096V (Section 3.1.1).

3.1.8. FG08 - Multifunctional

The system provides following on-board connectors:

- SPI Header: which is shared between EEPROM (Section 3.1.11) but has dedicated interrupt and select lines.
- I2C Header
- UART Header
- 2 x internal +5V and GND Headers

3.1.9. FG09 - Ethernet Interface

Ethernet interface is implemented with external Microchip ENC424J600 Ethernet controller because the RH850 F1L does not any integrated. For detailed information about Ethernet see Section 2.13. Microchip ENC424J600 comes with integrated MAC and 10/100Base-T PHY in a single package. Maximal input voltage is 3.3V. Regulation of 3.3V was implemented with Microchip MIC5219 linear voltage regulator (Section 2.2.1). In order to make sure no issues related to different voltage levels between MCU and Ethernet interface occur, voltage-level translation was implemented with Texas Instruments TXB0104 voltage-level translator. Ethernet interface can be turned off by MCU to reduce power-consumptions. ESD protection circuit of Ethernet interface was constructed with Littelfuse SP0504S TVS diode array which has very low capacitance and is very suitable for high speed signal lines. Please note that ESD protection should have been placed between the RJ45 connector and the common-mode choke. Reason for not implementing ESD protection in that manner was that the used RJ45 connector has integrated common-mode chokes and physically it was only possible to access wires between the common-mode choke and the Ethernet controller. (Section 2.10).

3.1.10. FG10 - USB to UART Protocol Converter

USB-UART converter was implemented with Microchip MCP2200. Like Ethernet interface, USB input was protected with the same TVS diode array (Section 3.1.9). Beside that differential pair of USB signals are constructed with common-mode choke and corresponding capacitors that form low pass filter for suppressing high-frequency common mode currents. This design should prevent potential related issues concerning EMC/EMI of the system (Section 2.10).

3.1.11. FG11 - EEPROM

Main purpose of EEPROM is to provide non-volatile memory for user application. RH850 features integrated Data Flash Area for this purpose (Section 2.1.1) but since automotive ECU may require fault memory area for error diagnostic,

external non-volatile memory was implemented. ST M95640-W is SPI bus EEPROM which provides 64-Kbit of non-volatile memory.

3.1.12. FG12 and FG13 - Digital I/Os and External D-SUB Connector

All seventeen GPIO (FG12) are protected by ESD circuit and directly accessible through external connector (FG13). Through D-SUB PIN 37 MALE connector following functions are accessible:

- 17 GPIOs
- HS CAN 0
- HS CAN 1
- HS/CAN FD CAN 2
- +5V External Power Supply
- LIN master
- Clamp 30/Battery plus pole
- Clam 31/Battery minus pole
- Clamp 15/Battery plus or similar signal

3.1.13. Absolute Maximum Ratings

Item	Symbol	MIN	MAX	Unit
E. ADC input voltage	V_{INADC} of ADC CH[1:10]	0	4.096	V
E. ADC input current	I_{INADC} of ADC CH[1:10]		3000	pA
E. ADC Nyquist frequency	f_{INADC} of ADC CH[1:10]		57	kHz
GPIO input voltage	V_{INGPIO} of GPIO [1:17]	0	5	V
GPIO input current	I_{INGPIO} of GPIO [1:17]		10	mA
Clamp-30	V_{IN}	5.5	40	V
Clamp-31	V_{GND}		0	V
Clamp-15	V_{15}	1.2	40	V
PCB temperature sensor	T_{PCB}	-40	125	°C
E. +5V PS Voltage	V_{ext}		5	V
E. +5V PS Current	I_{ext}		2	A
Total device power rating	P_{TOTAL}		25	W
CAN 0	data rate	0.033	1	Mbit/s
CAN 1	data rate	0.033	1	Mbit/s
CAN 2*	data rate	1	2	Mbit/s
LIN Master	data rate		19200	kbit/s
Ethernet	data rate	10	100	Mbit/s

* Microchip MCP2517FD support data rate up to 8 Mbit/s but limiting factor is the NXP TJA1043 transceiver, which only supports data rate up to 2 Mbit/s.

3.2. Software Architecture

Software architecture consists of two parts ”user application” and ”basic software” (BSW). User application runs at the top of Application Abstraction Layer knows as Runtime Environment (RTE), which specifies Application Program

Interface (API) of BSW and hides its implementation details. BSW consists of hardware drivers, configuration files, hardware abstraction layer (ETH IF, CAN IF, LIN IF ...) and different services (XCP, DISPLAY ...). Figure 3.3 shows simplified software architecture model, where blocks between Microcontroller and Application Abstraction Layer describe BSW layer.

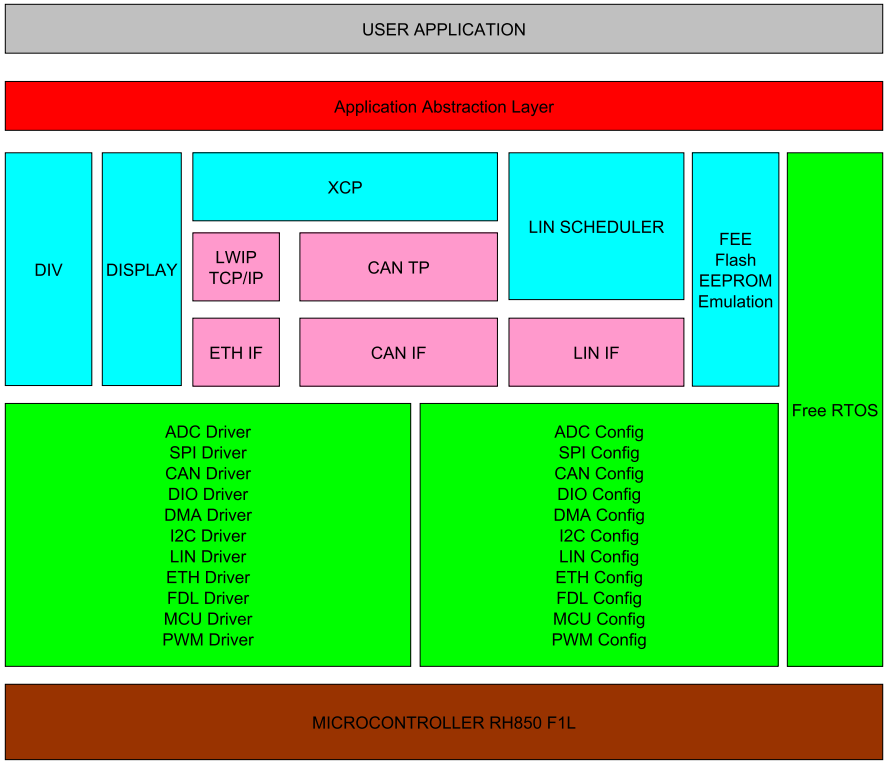


Figure 3.3.: Software architecture

3.2.1. Application Layer

Configuration files as well user application code is generated by MATLAB Simulink from user defined model. Figure 3.4 shows process steps required in building executable image. MATLAB Simulink generates C code from constructed model. This code is bundled with BSW code and compiled by IAR WORKBENCH RH850 toolchain. After successful code compilation hex image is generated which is flashed to the MCU by Renesas E1 Debugger. The tools required in build and run process are:

- MATLAB Simulink 2016b with Embedded Coder Enabled
- IAR Workbench RH850 Toolchain
- AA Toolchain (modified GT Toolchain)
- Renesas E1 Debugger

For detailed description about model based software design see Section 2.12.

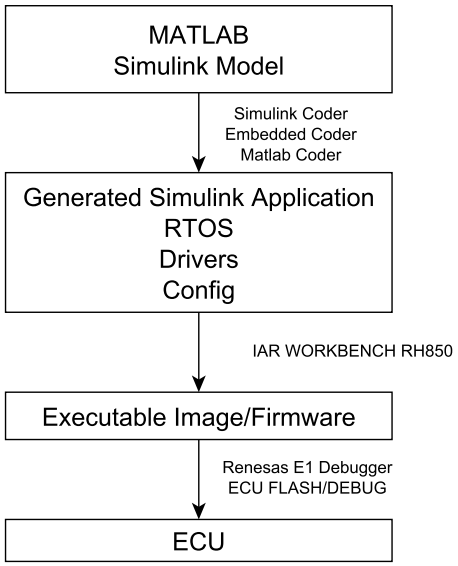


Figure 3.4.: Process of generating firmware

In the Figure 3.5 build control windows is shown. This blocks is used to build a model and flash the system.

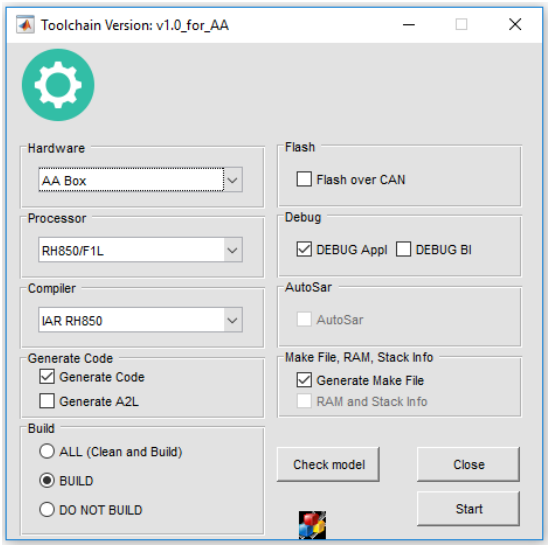


Figure 3.5.: Build tool

3.2.2. Custom SIMULINK Blocks

Task

Figure 3.6 shows task control window. Application software can have up to three threads with customizable task time, priority and stack size.

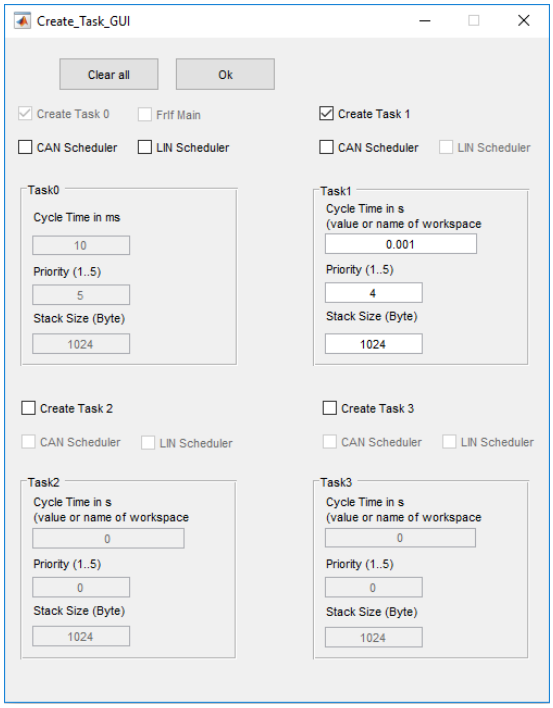


Figure 3.6.: Task control window

FG02 - Internal +5V Power Supply

Internal power supply unit can be turned of by following block:

Figure 3.7.: Sleep block

This block will put ECU in safe state, set all CAN/LIN transceivers into sleep state and at the end turn power-supply off (under assumption that Clamp-15 is low).

FG03 - External +5V Power Supply

Custom block provides functions for turning PS on/off, temperature and voltage monitoring of the PS.

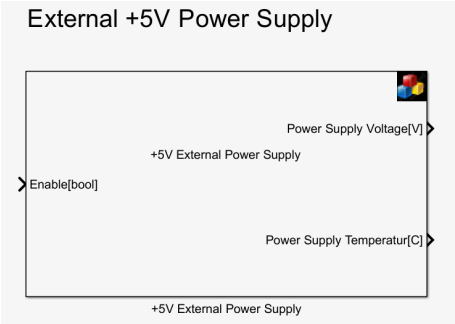


Figure 3.8.: MATLAB Simulink control block for external power supply

FG04 - CAN Bus

CAN bus contains four control blocks (Figure 3.9).

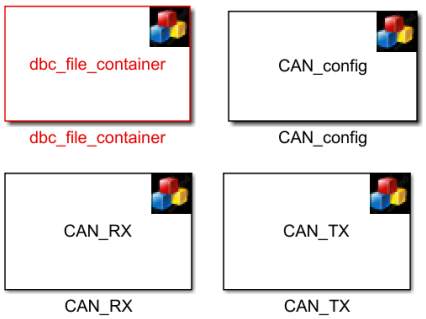


Figure 3.9.: CAN control blocks

In DBC container dbc file can be specified. DBC file holds message specifications of all CAN messages. This file is essential for CAN usage (Figure 3.10).

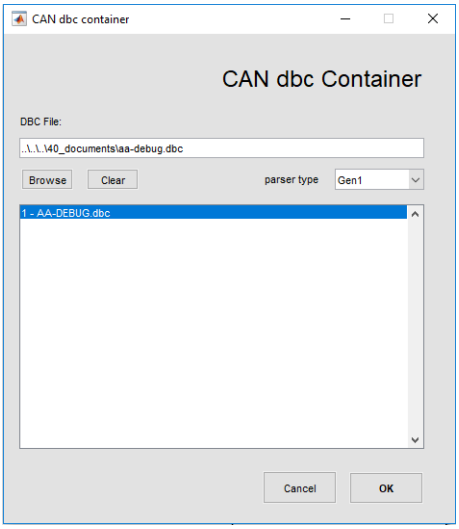


Figure 3.10.: CAN DBC block

Depending on applications requirements, CAN channel configuration windows (Figure 3.11) allows activation of specific CAN channel and specification of data rate.

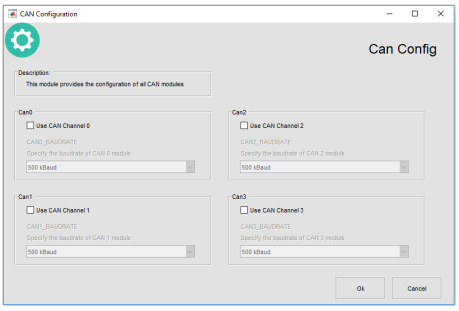


Figure 3.11.: CAN configuration block

TX and RX block are used for data reception and transition. Selectable signals in these blocks are generated from a dbc file.

Figure 3.12 shows transmission block in which beside transmit signals, cycle time and CRC algorithm (this is not CAN protocol CRC) can be specified. Similarly follows reception block seen in Figure 3.13

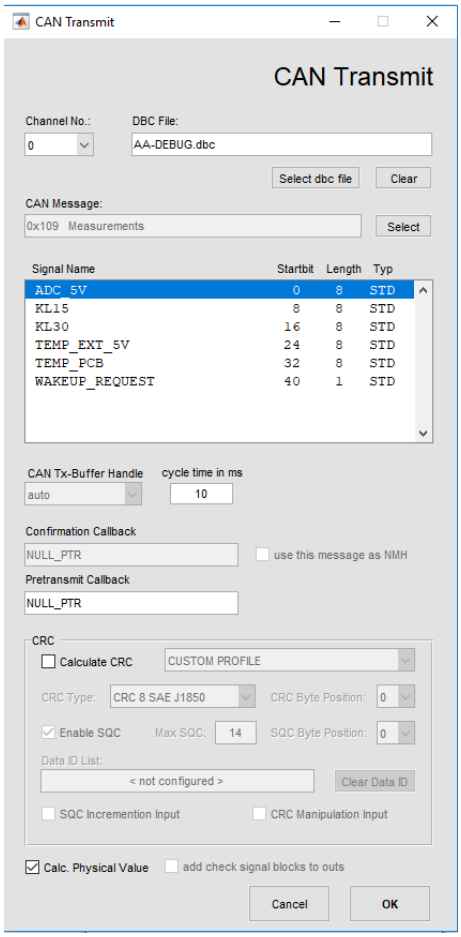


Figure 3.12.: CAN transmit block

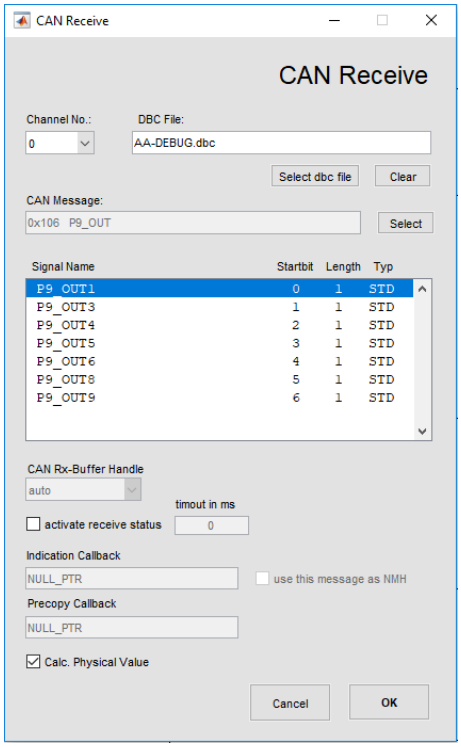


Figure 3.13.: CAN receive block

FG05 - LIN Master

Analog to CAN block, LIN contains also multiple control blocks. These are LDF container block for message description file, LIN data rate configuration block, RX/TX for data reception/transmission and LIN scheduler block.

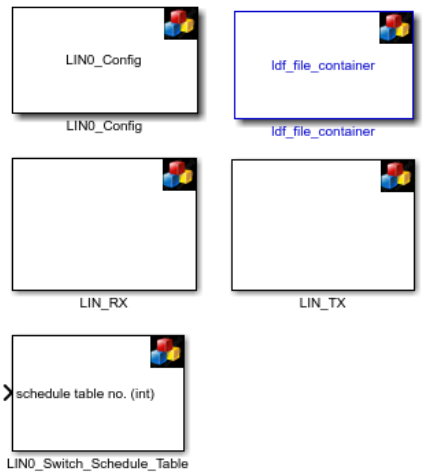


Figure 3.14.: LIN master control blocks

FG06 Internal Measurements

Wake-up request block allows application to detect if the system has been woken up by CAN/LIN transceiver wake-up request (Figure 3.15).

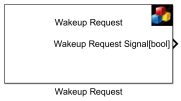


Figure 3.15.: Wake-up request read block

Figure 3.16 shows Clamp-30 voltage monitoring block. Similarly Clamp-15 monitoring exists.

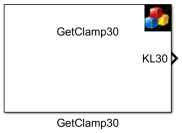


Figure 3.16.: MATLAB Simulink Clamp-15/30 voltage read block

PCB temperature monitoring block is shown in Figure 3.17

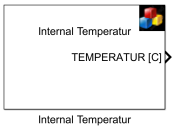


Figure 3.17.: MATLAB Simulink PCB temperature read block

FG07 External ADC channels

External ADC channels are controlled with the block shown in Figure 3.18. ADC unit must be enabled in order for ADC to deliver valid results.

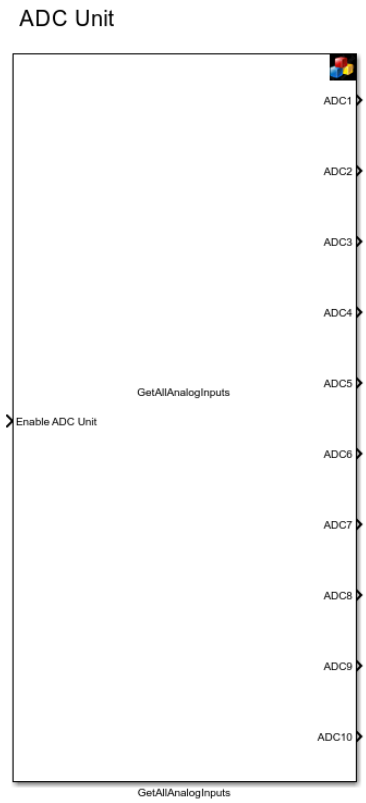


Figure 3.18.: MATLAB Simulink ADC control block

FG08 Multifunctional

For debugging OLED display and LED is available. Beside that USB-UART can be used but this interface is not accessible from MATLAB.

Display is organized into eight lines and is controlled by block shown in Figure 3.19.

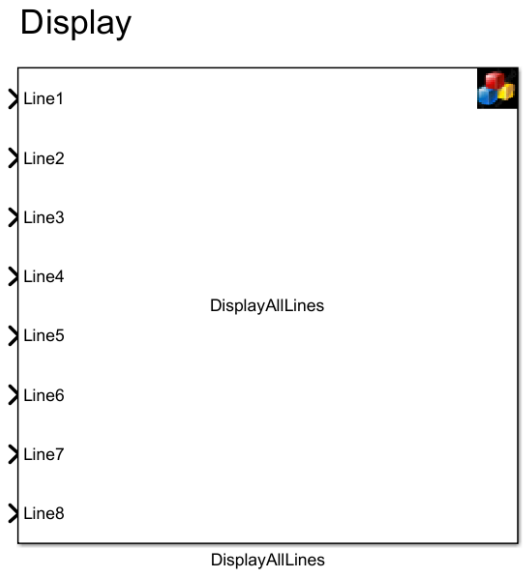


Figure 3.19.: OLED display MATLAB Simulink control block

Control block of Debug-LED is shown in Figure 3.20 where logic one turn LED on and logic zero off.

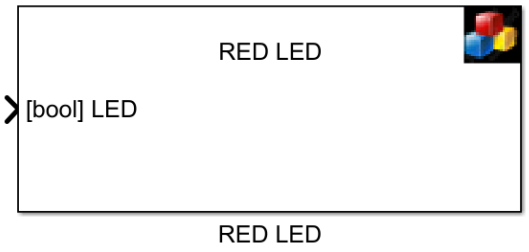


Figure 3.20.: Debug LED MATLAB Simulink control block

FG09 Ethernet Interface

Ethernet interface is configurable with blocks shown in Figure 3.21. Ethernet_Config block allows to set IP address and to create UDP and TCP sockets. Data can be transmitted or received either over TCP or UDP protocol. For more information about Ethernet see Section 2.13. Please note that IP address set here is also the IP address of XCP over TCP/IP protocol. XCP port is fixed at port 5555. For more details about XCP protocol see Section 2.14

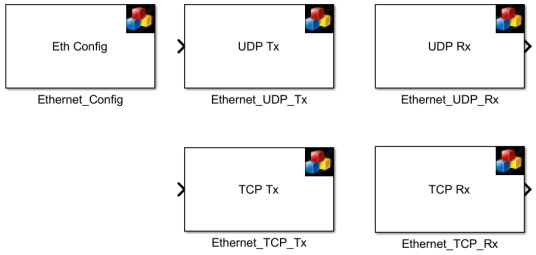


Figure 3.21.: Ethernet controller control blocks

FG11 EEPROM

Reading and writing non-volatile memory is performed with blocks shown in Figure 3.22.

Figure 3.22.: MATLAB Simulink control blocks for reading and writing of EEPROM

FG12 DIOs

Digital I/O are controlled with block shown in Figure 3.23. Please note that block must be either configured as input or output. In case of a input logic one sets I/O to 5V and logic zero to 0V.

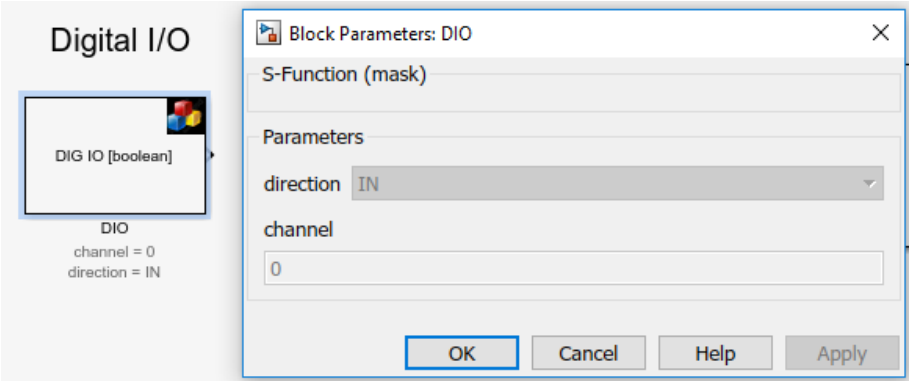


Figure 3.23.: Digital I/O control block

4. Implementation

This chapter describes detailed implementation of Printed Board Circuit (PCB). Schematics are organized into the same functional groups as it has been described in Section 3.1.

General information of the PCB:

1. Construction Tool: Autodesk Eagle Version 9 (Education)
2. Baord size: $160mmx110mm$ (fits BOPLA Alubos 1600 case)
3. Layers: 4

Board stack management:

1. Top-Signal layer
2. Ground layer
3. +5V layer
4. Bottom-Signal layer

For better schematic readability, project was imported into Altium Designer (licensed to AKKA Technologies). Figure 4.1 shows schematic components organized into functional groups.

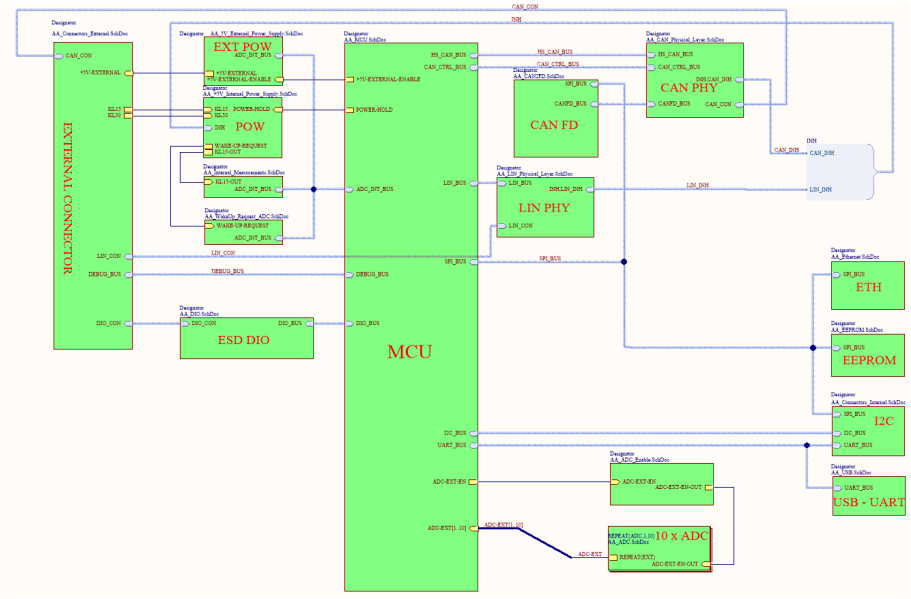


Figure 4.1.: Schematic components

4.1. FG01 Microcontroller

Functional group FG01 has four subgroups. These are debug interface related FG01 01, clock related FG01 02, ADC reference voltage FG01 03, I/O assignment FG01 04 and MCU supply FG01 05. For functional specification please refer to the Section 3.1.1.

4.1.1. FG01 01 Programming Interface

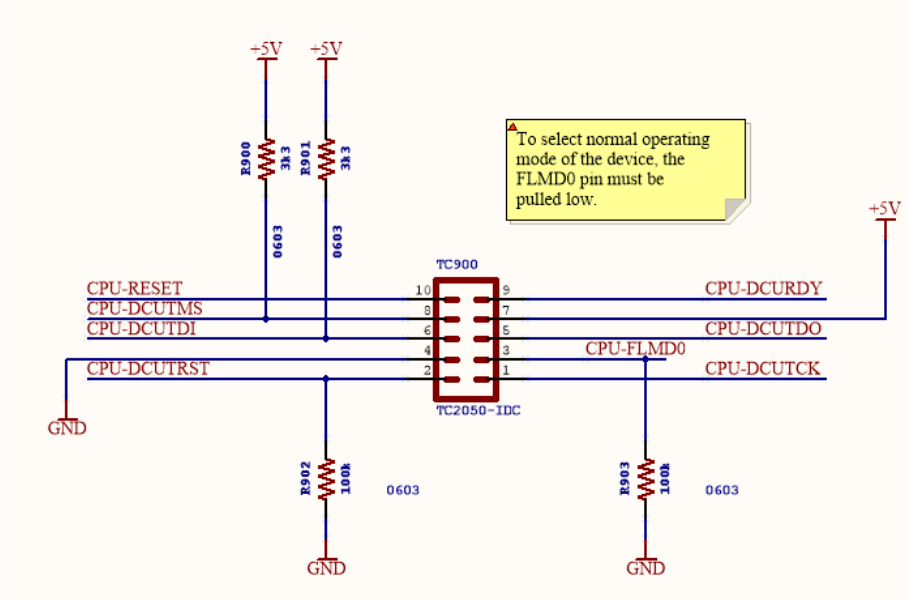


Figure 4.2.: Programming interface

Debugging connector is implemented with TC2050-IDC Tag [38]. Benefit of TC-Tag is that it does not require physical header to be soldered on the board. Instead, defined PCB test points and special Tag-Connect-Plug is used to connect Renesas E1 debugger and the board. Adapter for connecting Renesas E1 and TC2050-Tag is shown in Figure 4.3 and Figure 4.3.

Designator	Part
TC900	TC2050
R900	3.3kΩ SMD 0603
R901	3.3kΩ SMD 0603
R902	100kΩ SMD 0603
R903	100kΩ SMD 0603

Table 4.1.: Components of FG0101

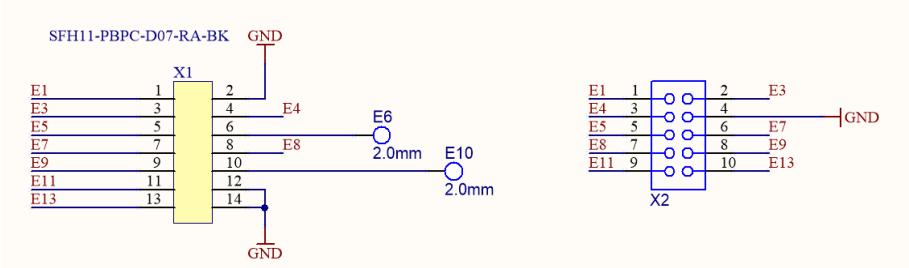


Figure 4.3.: TC2050 adapter schematic

Designator	Part
X1	CONN HDR 14POS 0.1 GOLD PCB R/A Female
X2	DEBUG 2X5 2.54MM PITCH Male

Table 4.2.: Components of TC2050 adapter

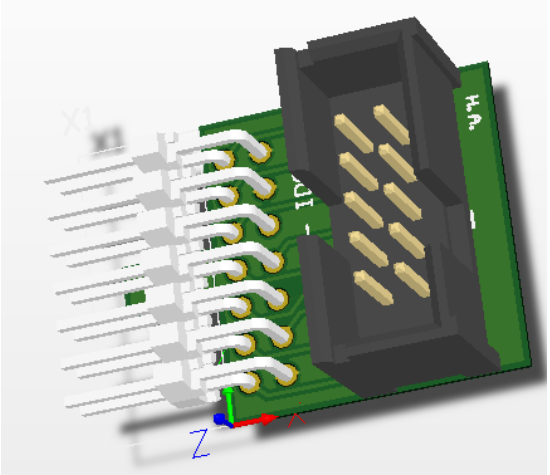


Figure 4.4.: ALTIUM 3D view of TC2050 adapter

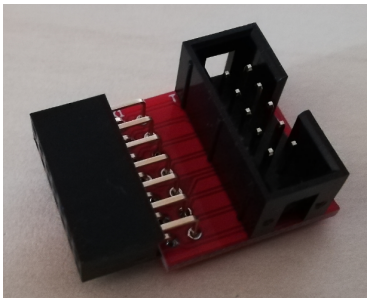


Figure 4.5.: TC2050 adapter

4.1.2. FG01 02 MCU-Clock

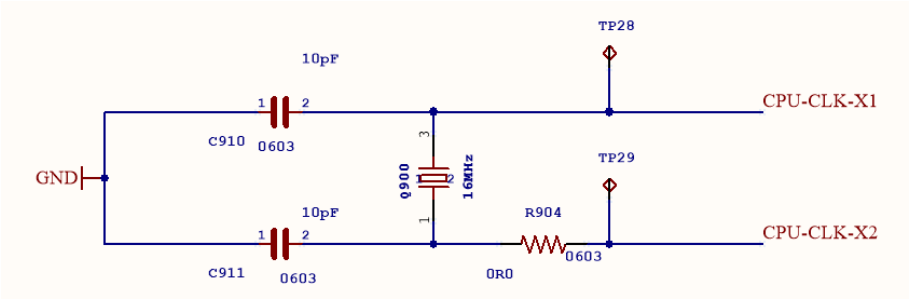


Figure 4.6.: MCU clock

Designator	Part
Q900	ABM8G-16.000MHZ-B4Y-T
C910	10pF 250V CoG/NP0 SMD 0603
C911	10pF V CoG/NP0 SMD 0603
R904	0Ω JUMPER SMD 0603

Table 4.3.: MCU clock

4.1.3. FG01 03 ADC Reference Voltage

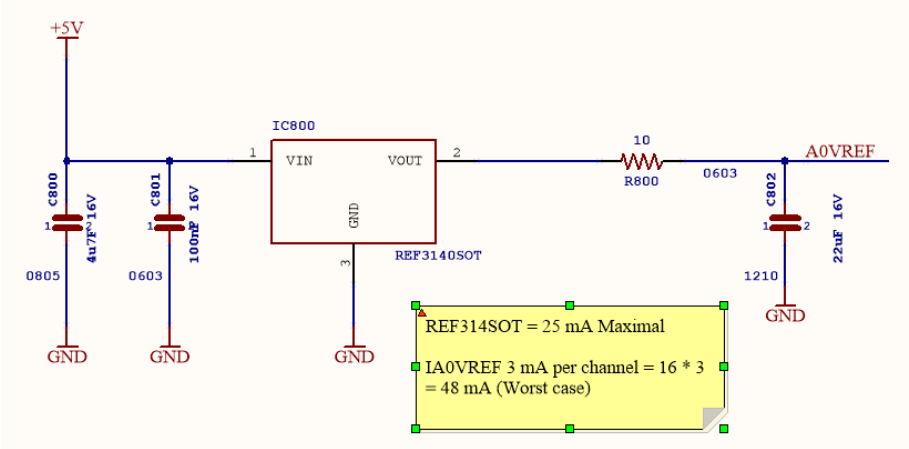


Figure 4.7.: ADC reference voltage

Designator	Part
IC800	Texas Instruments REF3140
C800	4.7µF 16V X7R SMD 0805
C801	100nF X7R 16V SMD 0603
C802	22µF X7R 16V SMD 1210
R800	10Ω SMD 0603

Table 4.4.: ADC reference voltage

4.1.4. FG01 04 MCU-I0

For detailed Pin assignment see Appendix A.1.

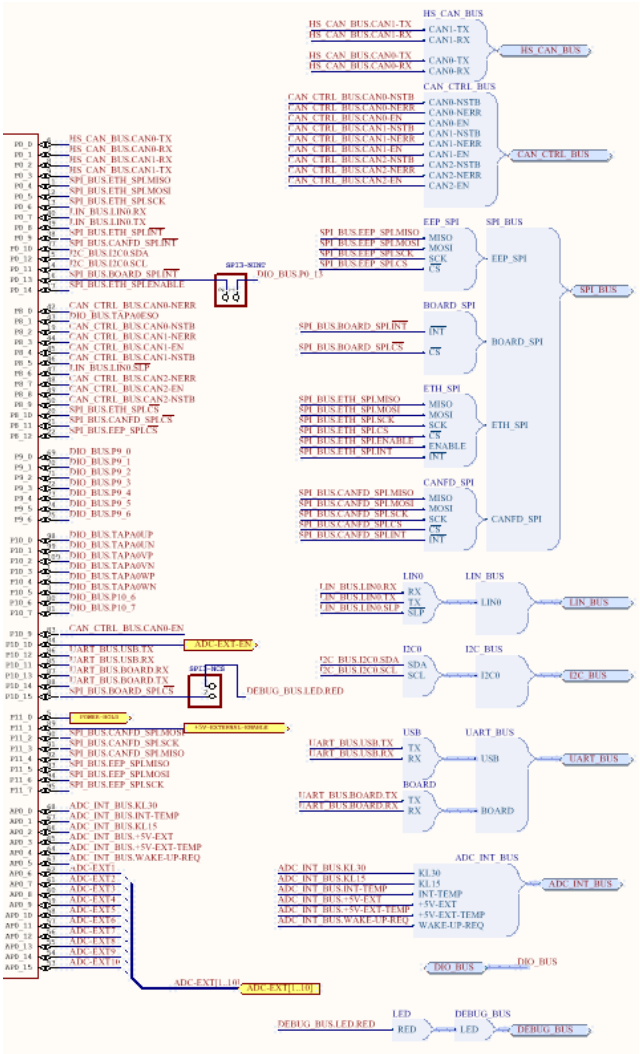


Figure 4.8.: MCU IO assignment

4.1.5. FG01 05 MCU-Voltage Supply

Both system supply voltage (REG VCC) as port supply voltage (EVCC) are powered by 5V. Alway-on (AWO) and Isolated area (ISO) capacitances (C903 and C904) are required for internal regulators. Each pin pair has own decoupling capacitor. Special care should be taken to position these capacitors when routing is performed. For avoiding EMC related issues these capacitors should be placed on the PCB as close as possible to its corresponding pins such that loops they form are as small as possible.

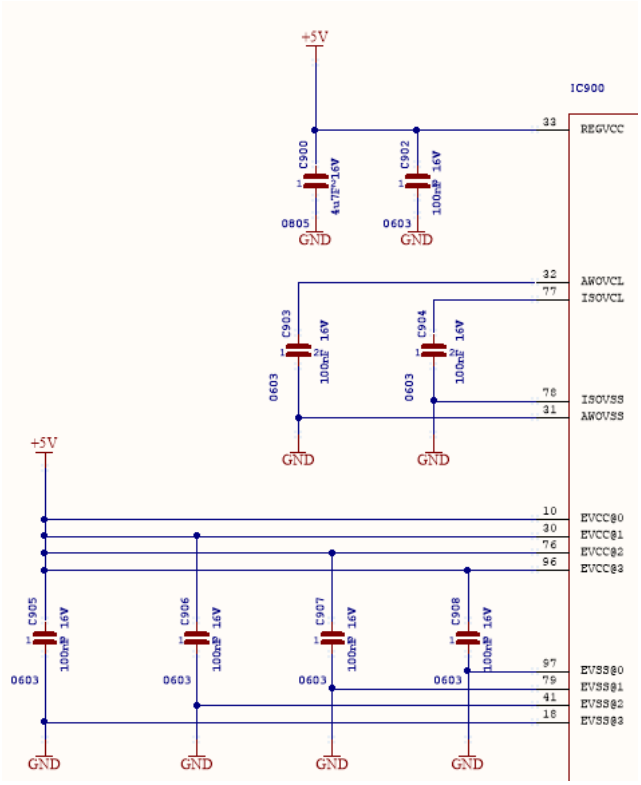


Figure 4.9.: MCU voltage supply

Designator	Part
C900	4.7µF X7R 16V SMD 0805
C901	100nF X7R 16V SMD 0603
C902	100nF X7R 16V SMD 0603
C903	100nF X7R 16V SMD 0603
C904	100nF X7R 16V SMD 0603
C905	100nF X7R 16V SMD 0603
C906	100nF X7R 16V SMD 0603
C907	100nF X7R 16V SMD 0603
C908	100nF X7R 16V SMD 0603

Table 4.5.

4.2. FG02 Internal +5V Power Supply

Functional group FG02 has four subgroups. These are Clamp-30 input stage FG02 01, voltage regulator FG02 02, PS switch FG02 03 and Clamp-15 input stage circuit. For functional specification of this group please refer to the Section 3.1.2.

4.2.1. FG02 01 KL30 Input

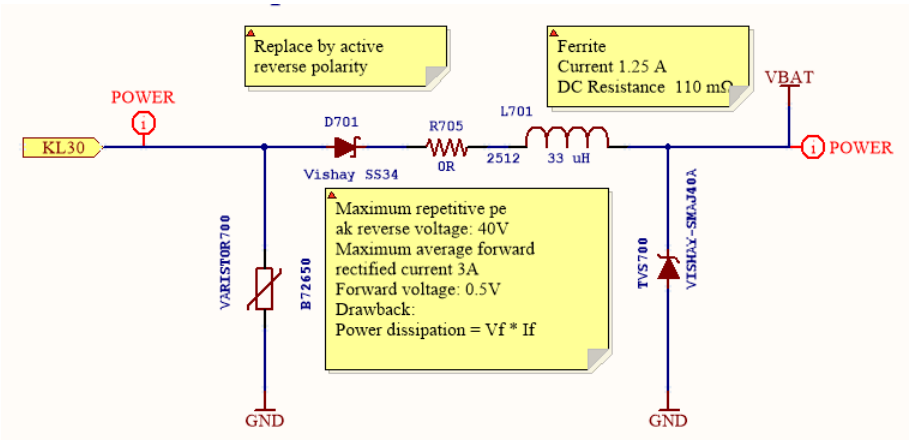


Figure 4.10.: Power supply input (clamp 30) with protection network

Designator	Part
VARISTOR700	EPCOS-B72650M0400K072
D701	Vishay SS34
R705	0Ω SMD 2512
L701	33µH SRR7045270M
TVS700	VISHAY SMAJ40A

Table 4.6.

4.2.2. FG02 02 +5V Voltage Regulator

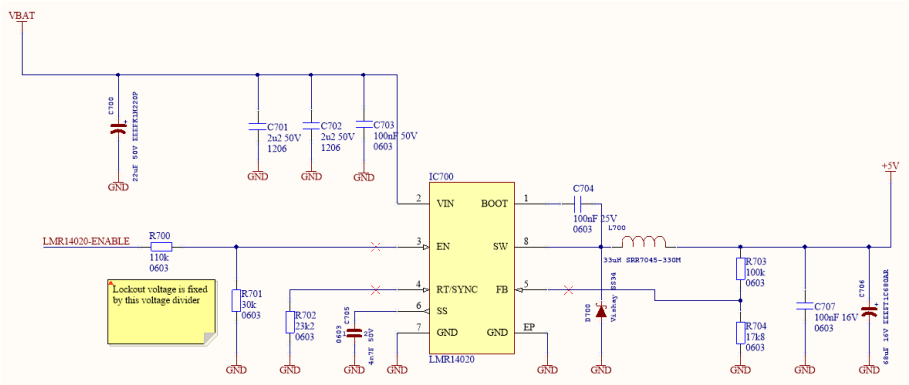


Figure 4.11.: Internal voltage supply

Designator	Part
IC 700	Texas Instruments LMR14020
C700	22µF 50V EEEFK1H220P Polarized
C701	2.2µF 50V SMD 1206
C702	2.2µF 50V SMD 1206
C703	100nF 50V SMD 0603
C704	100nF 25V SMD 0603
C705	4.7nF 50V SMD 0603
C706	68µF 16V EEEFT1C680AR Polarized
C707	100nF 16V SMD 0603
R700	110kΩ SMD 0603
R701	30kΩ SMD 0603
R702	23 2kΩ SMD 0603
R703	100kΩ SMD 0603
R704	17 8kΩ SMD 0603
D700	VISHAY SS34
L700	33µH SRR7045-330M

Table 4.7.

4.2.3. FG02 03 PS Switch

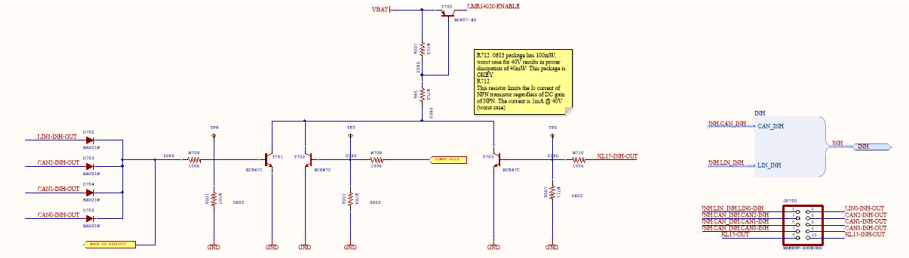


Figure 4.12.: Power supply switch

Designator	Part
T700	PNP BJT BC807 45V SMALL SIGNAL TRANSISTOR IN SOT23
T701	NPN BJT BC847C 50V SMALL SIGNAL TRANSISTOR IN SOT23
T702	100kΩ SMD 0603
T703	100kΩ SMD 0603
R706	100kΩ SMD 0603
R707	100kΩ SMD 0603
R708	100kΩ SMD 0603
R709	100kΩ SMD 0603
R710	100kΩ SMD 0603
R711	100kΩ SMD 0603
R712	39kΩ SMD 0603
R713	100kΩ SMD 0603
D702	BAW21W Small Signal Switching Diodes, High Voltage
D703	BAW21W Small Signal Switching Diodes, High Voltage
D704	BAW21W Small Signal Switching Diodes, High Voltage
D705	BAW21W Small Signal Switching Diodes, High Voltage
JP700	PINHD-2X5, Source select jumper

Table 4.8.

4.2.4. FG02 04 KL15 Input

Figure 4.13.: Clamp 15 input circuit

Designator	Part
VARISTOR701	EPCOS-B72650M0400K072
D706	Vishay SS14HE3
TVS701	VISHAY SMAJ40A

Table 4.9.

4.3. FG03 External Power Supply

External power supply is identical to +5V internal supply. For functional specification please refer to the Section 3.1.3 and 3.1.2.

4.3.1. FG03 01 +5V External Voltage Regulator

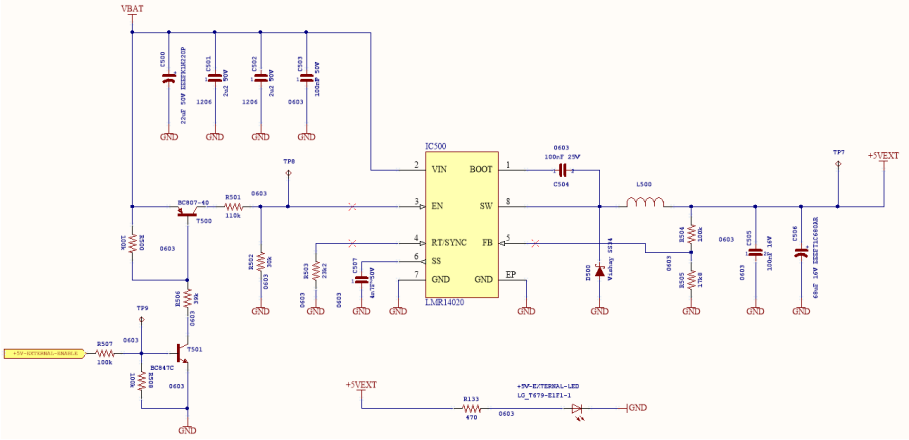


Figure 4.14.: +5V External Voltage Regulator

Designator	Part
IC 500	Texas Instruments LMR14020
C500	22µF 50V EEEFK1H220P Polarized
C501	2.2µF 50V SMD 1206
C502	2.2µF 50V SMD 1206
C503	100nF 50V SMD 0603
C504	100nF 25V SMD 0603
C505	100nF 16V SMD 0603
C506	68µF 16V EEEFT1C680AR Polarized
C507	4.7nF 50V SMD 0603
R500	110kΩ SMD 0603
R501	110kΩ SMD 0603
R502	30kΩ SMD 0603
R504	100kΩ SMD 0603
R505	17 8kΩ SMD 0603
R506	39kΩ SMD 0603
R507	100kΩ SMD 0603
R508	100kΩ SMD 0603
D500	VISHAY SS34
L500	33µH SRR7045-330M
T500	PNP BJT BC807 45V SMALL SIGNAL TRANSISTOR IN SOT23
T501	NPN BJT BC847C 50V SMALL SIGNAL TRANSISTOR IN SOT23
R133	470Ω SMD 0603
+5V-EXTERNAL-LED	Control LED

Table 4.10.

4.3.2. FG03 02 Supply Temperature

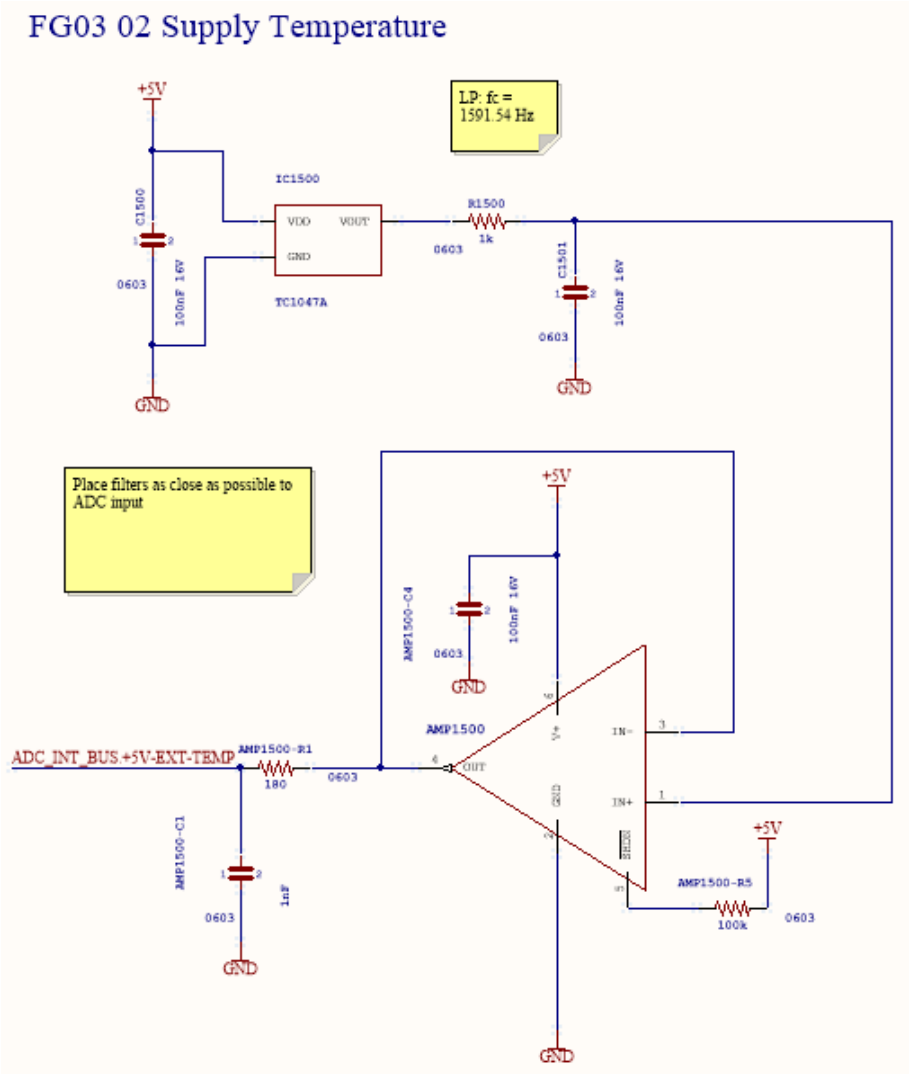


Figure 4.15.: Supply Temperature

Designator	Part
IC1500	Microchip TC1047A
C1500	100nF 16V SMD 0603
C1501	100nF 16V SMD 0603
R1500	1kΩ SMD 0603
AMP1500	Texas Instruments TLV341AIDBVR
AMP1500-C4	100nF 16V SMD 0603
AMP1500-C1	1nF 16V SMD 0603
AMP1500-R1	180Ω SMD 0603
AMP1500-R5	100kΩ SMD 0603

Table 4.11.

4.3.3. FG03 03 Output Voltage Measurement

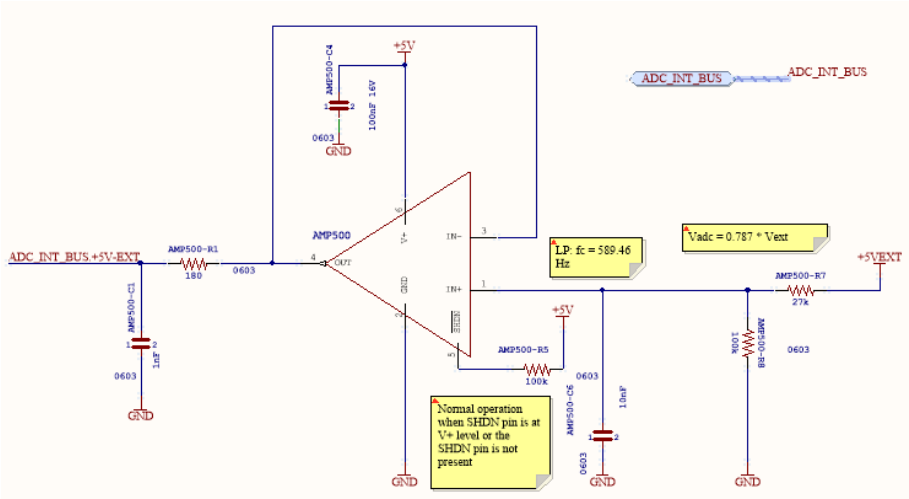


Figure 4.16.: Output Voltage Measurement

Designator	Part
AMP500	Texas Instruments TLV341AIDBVR
AMP500-C4	100nF 16V SMD 0603
AMP500-C1	1nF 16V SMD 0603
AMP500-R1	180Ω SMD 0603
AMP500-R5	100kΩ SMD 0603
AMP500-R7	27kΩ SMD 0603
AMP500-R8	100kΩ SMD 0603

Table 4.12.

4.3.4. FG03 04 ESD Protection

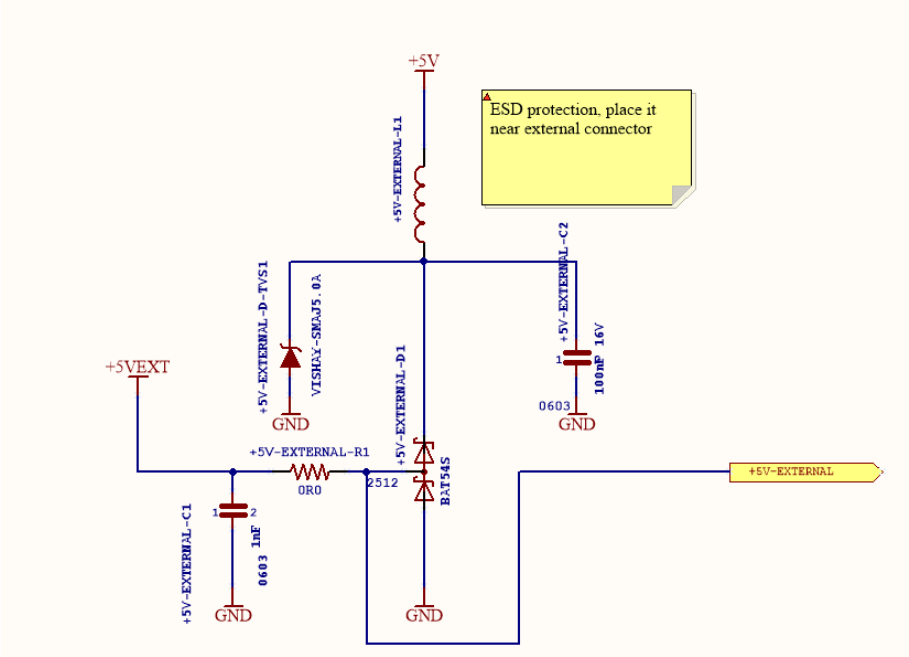


Figure 4.17.: ESD Protection

Designator	Part
+5V-EXTERNAL-D-TVS1	VISHAY SMAJ5.0A
+5V-EXTERNAL-D1	BAT54S
+5V-EXTERNAL-L1	WE-CBF SMD EMI Suppression Ferrite Bead
+5V-EXTERNAL-C1	1nF 16V SMD 0603
+5V-EXTERNAL-C2	100nF 16V SMD 0603
+5V-EXTERNAL-R1	0Ω SMD 2512

Table 4.13.

4.4. FG04 CAN

CAN physical layer is composed of three parts. CAN transceiver FG04 01, termination network FG04 02 and ESD protection circuit FG04 03. For functional specification please refer to the Section 3.1.4. This structure is repeated three times for every CAN-controller.

4.4.1. FG04 01 CAN Transceiver(s)

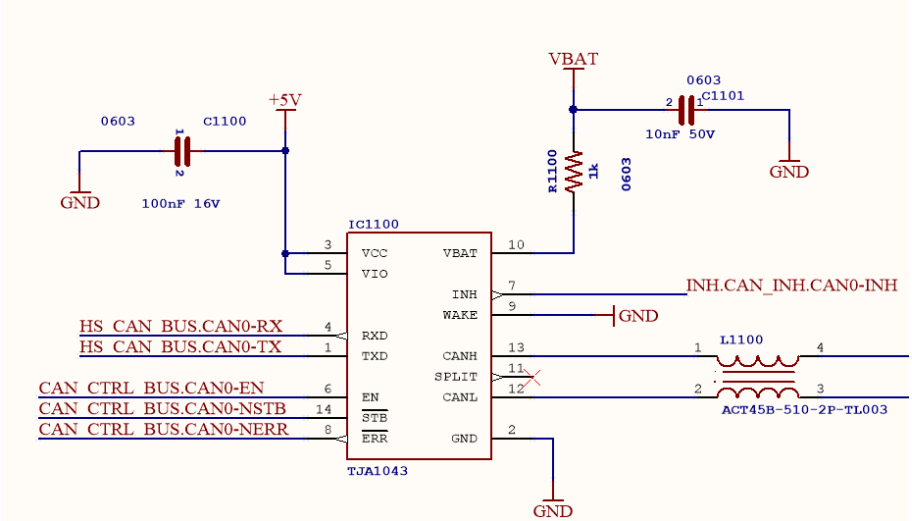


Figure 4.18.: CAN transceiver(s)

Designator	Part
IC1100	NXP TJA1043 High Speed CAN Transceiver
C1100	100nF 16V SMD 0603
C1101	10nF 50V SMD 0603
R1100	1kΩ SMD 0603
L1100	Common-mode Choke TDK ACT45B-510-2P-TL003

Table 4.14.

4.4.2. FG04 02 CAN Termination

Termination network used here is called split termination where 120Ω resistor is split into two equal resistors. Capacitor used between these two

resistors form low-pass filter. This filter should reduce common-mode noise and electromagnetic emissions.

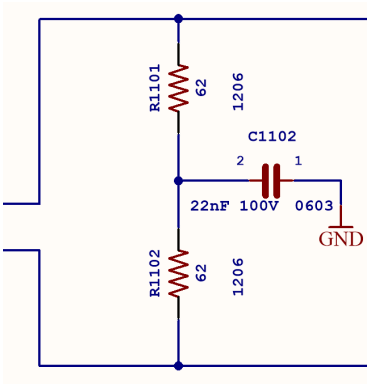


Figure 4.19.: CAN termination network

Designator	Part
R1101	62Ω SMD 1206
R1102	62Ω SMD 1206
C1102	22nF 100V SMD 0603

Table 4.15.

4.4.3. FG04 03 CAN ESD Protection

Please note that when routing the PCB protection should be placed near CAN's external connector. Second thing that needs special care when differential pairs of CAN are routed is the length, that should be matched.

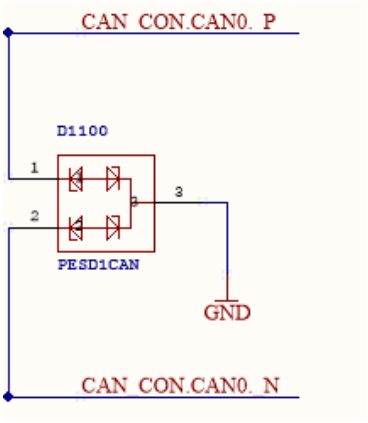


Figure 4.20.: CAN ESD protection

Designator	Part
D1100	NXP PESD1CAN CAN bus ESD protection diode

Table 4.16.

4.4.4. FG04 04 SPI CAN FD Controller

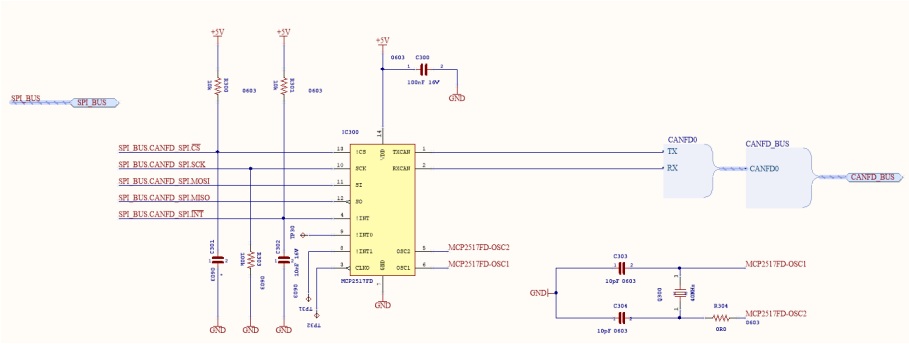


Figure 4.21.: SPI CAN FD Controller

Designator	Part
IC300	Microchip MCP2517FD External CAN FD Controller
R300	10kΩ SMD 0603
R301	10kΩ SMD 0603
R303	100kΩ SMD 0603
R304	0Ω SMD 0603
C300	100nF 16V SMD 0603
C301	*
C302	10nF 16V SMD 0603
C303	10pF SMD 0603
C304	10pF SMD 0603
Q300	ABM8G-40.000MHZ-4Y-T3

Table 4.17.

4.5. FG05 LIN Master

For functional specification please refer to the Section 3.1.5

4.5.1. FG05 01 LIN Master Transceiver

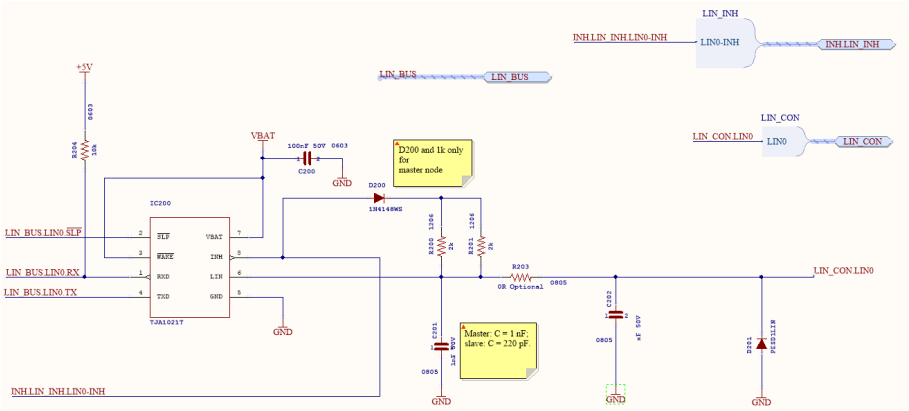


Figure 4.22.: LIN master transceiver

Designator	Part
IC200	NXP TJA1021T LIN 2.1/SAE J2602 transceiver
R200	2kΩ SMD 1206
R201	2kΩ SMD 1206
R203	0Ω SMD 0805
R204	10kΩ SMD 0603
C200	100nF 50V SMD 0603
C201	1nF 50V SMD 0603
C202	*
D200	1N4148WS
D201	LIN-bus ESD protection diode

Table 4.18.

4.6. FG06 Internal Measurements

Internal measurements consist of FG0601 PCB temperature measurement, FG0602/03 Clamp-15 and Clamp-30 voltage measurements and FG0604 wake-up request detection circuit. For functional specification please refer to the Section 3.1.6.

4.6.1. FG06 01 PCB Temperature

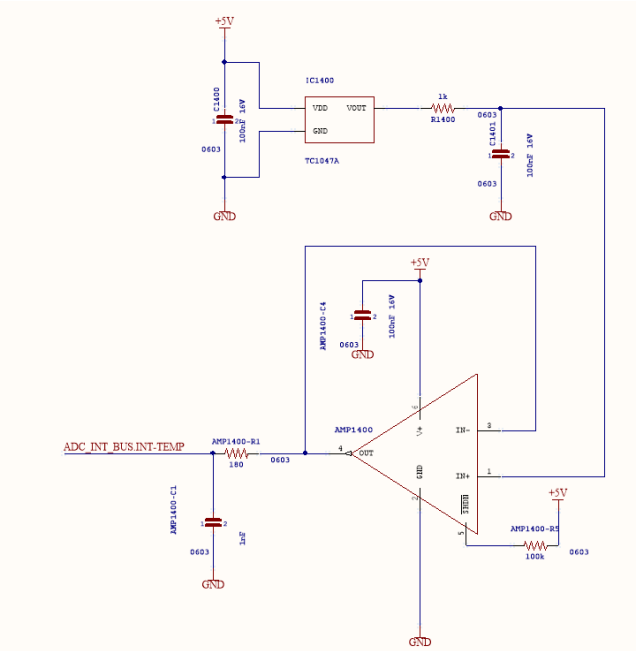


Figure 4.23.: PCB temperature

Designator	Part
IC1400	Microchip TC1047A
C1400	100nF 16V SMD 0603
C1401	100nF 16V SMD 0603
R1400	1kΩ SMD 0603
AMP1400	Texas Instruments TLV341AIDBVR
AMP1400-C4	100nF 16V SMD 0603
AMP1400-C1	1nF 16V SMD 0603
AMP1400-R1	180Ω SMD 0603
AMP1400-R5	100kΩ SMD 0603

Table 4.19.

4.6.2. FG06 02/03 Clamp 30 and 15 Voltage Measurement

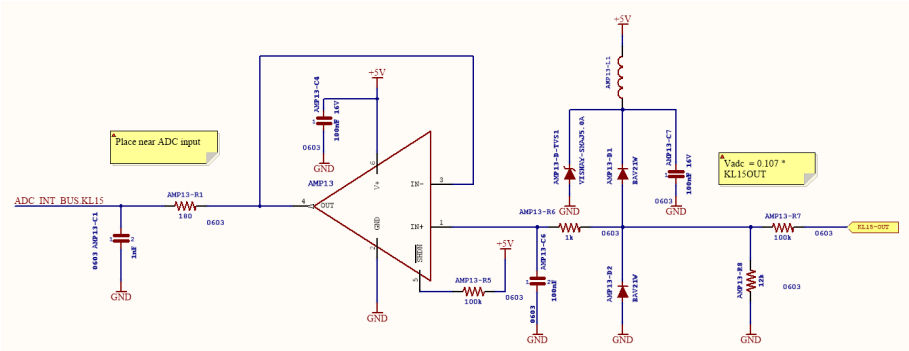


Figure 4.24.: Clamp 15 voltage measurement

Designator	Part
AMP11	Texas Instruments TLV341AIDBVR
AMP11-C4	100nF 16V SMD 0603
AMP11-C1	1nF 16V SMD 0603
AMP11-R1	180Ω SMD 0603
AMP11-R5	100kΩ SMD 0603
AMP11-R7	100kΩ SMD 0603
AMP11-R8	12kΩ SMD 0603
AMP11-L1	WE-CBF SMD EMI Suppression Ferrite Bead
AMP11-D-TVS1	VISHAY SMAJ5.0A
AMP11-D1	BAW21W
AMP11-D2	BAW21W
AMP11-C7	100nF 16V SMD 0603
AMP11-R6	1kΩ SMD 0603
AMP11-C6	100nF 16V SMD 0603

Table 4.20.

4.6.3. FG06 04 Wake-Up Request Detection

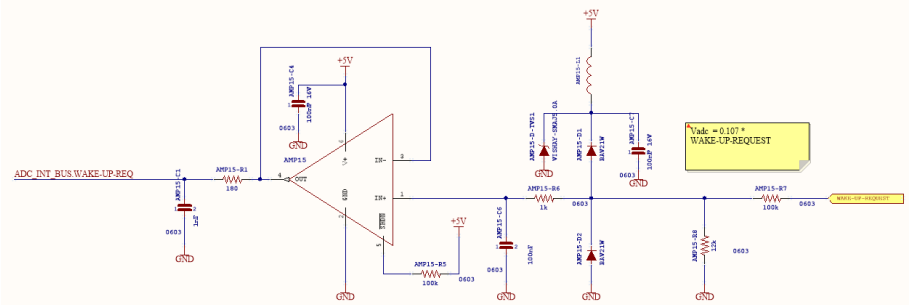


Figure 4.25.: Wake-up request detection

Designator	Part
AMP15	Texas Instruments TLV341AIDBVR
AMP15-C4	100nF 16V SMD 0603
AMP15-C1	1nF 16V SMD 0603
AMP15-R1	180Ω SMD 0603
AMP15-R5	100kΩ SMD 0603
AMP15-R7	100kΩ SMD 0603
AMP15-R8	12kΩ SMD 0603
AMP15-L1	WE-CBF SMD EMI Suppression Ferrite Bead
AMP15-D-TVS1	VISHAY SMAJ5.0A
AMP15-D1	BAW21W
AMP15-D2	BAW21W
AMP15-C7	100nF 16V SMD 0603
AMP15-R6	1kΩ SMD 0603
AMP15-C6	100nF 16V SMD 0603

Table 4.21.

4.7. FG07 External ADC channels

Total ten external ADC channels are available. Functional groups are FG0701 ADC represents signal conditioning circuit and FG0702 represents ADC on/off switch. For functional specification please refer to the Section 3.1.7.

4.7.1. FG07 01 ADC Channel

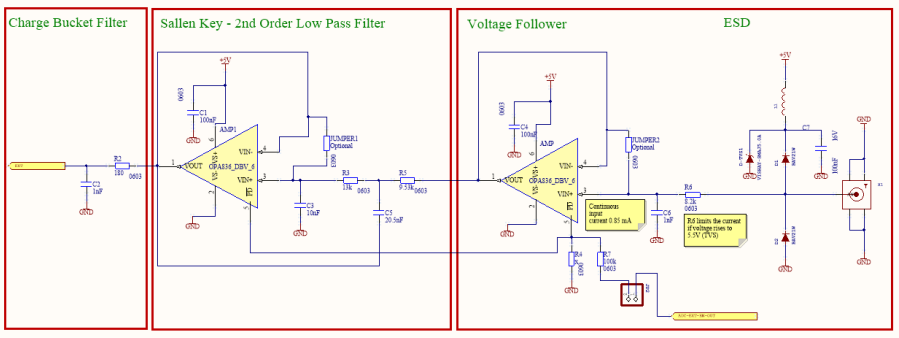


Figure 4.26.: ADC channel

Designator	Part
AMP1	Texas Instruments OP836 Rail-to-Rail
AMP2	Texas Instruments OP836 Rail-to-Rail
C1	100nF 16V SMD 0603
C2	1nF SMD 0603
C3	10nF 16V SMD 0603
C4	100nF 16V SMD 0603
C5	20.5nF 16V SMD 0603
C6	100nF 16V SMD 0603
C7	100nF 16V SMD 0603
L1	WE-CBF SMD EMI Suppression Ferrite Bead
TVS1	VISHAY SMAJ5.0A
D1	BAW21W
D2	BAW21W
R2	180Ω SMD 0603
R3	13kΩ SMD 0603
R4	*
R5	9.53kΩ SMD 0603
R6	8.2kΩ SMD 0603
R7	100kΩ SMD 0603
X1	SMA Connector

Table 4.22.

4.7.2. FG07 02 ADC Switch

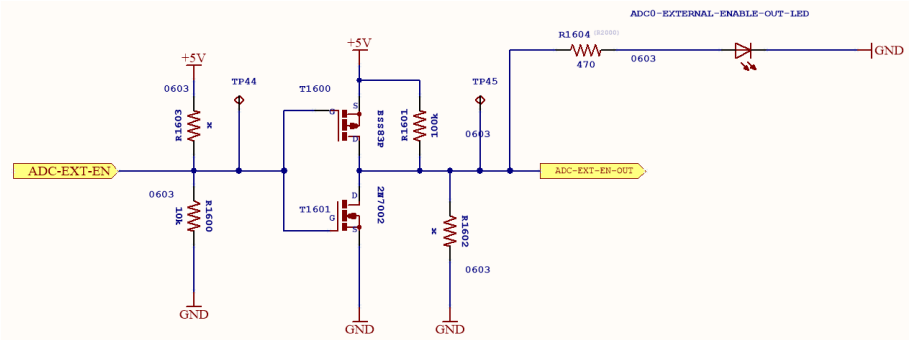


Figure 4.27.: ADC channel enable inverter

Designator	Part
T1600	BSS83P PMOS
T1601	2N7002 NMOS
R1600	10kΩ SMD 0603
R1601	100kΩ SMD 0603
R1602	*
R1603	*
R1604	470Ω SMD 0603
ADC0-EXTERNAL-ENABLE-OUT-LED	LED

Table 4.23.

4.8. FG08 Multifunctional

This functional group includes FG0802 external SPI-Connector, FG0803 I2C-Connector and FG0801 Debug-LED. For functional specification please refer to the Section 3.1.8.

- FG08 02 SPI for System Expansion

- FG08 03 I2C OLED Display

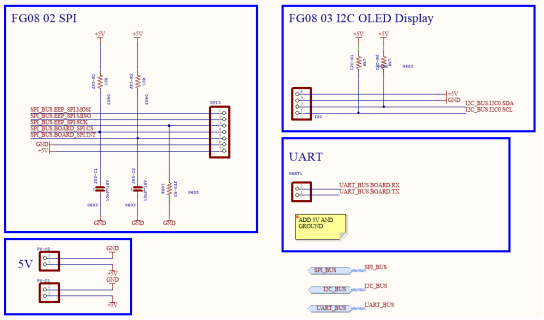


Figure 4.28.: Onboard SPI and I2C

Designator	Part
SPI3	PINHD-1X7
JP3-R1	10kΩ SMD 0603
JP3-R2	10kΩ SMD 0603
JP3-R3	100kΩ SMD 0603
JP3-C1	*
JP3-C2	*

Table 4.24.

Designator	Part
PINHD-1X4	
I2C-R1	4.7kΩ SMD 0603
I2C-R2	4.7kΩ SMD 0603

Table 4.25.

4.8.1. FG08 01 Debug LED

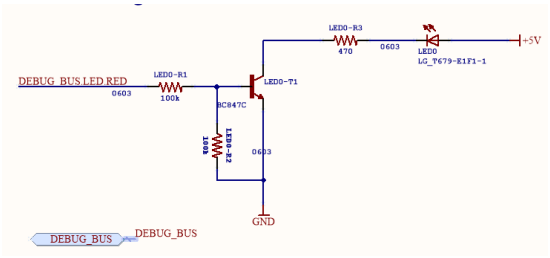


Figure 4.29.: Debug LED

Designator	Part
LED0-R1	100kΩ SMD 0603
LED0-R2	100kΩ SMD 0603
LED0-R3	470Ω SMD 0603
LED0-T1	NPN BJT BC847C 50V SMALL SIGNAL TRANSISTOR IN SOT23
LED0	LED

Table 4.26.

4.9. FG09 Ethernet Interface

Ethernet interface is composed of Ethernet controller FG0901, logic level shifter FG0902 and 3.3V linear voltage regulator. For functional specification please refer to the Section 3.1.9.

4.9.1. FG09 01 Ethernet Controller

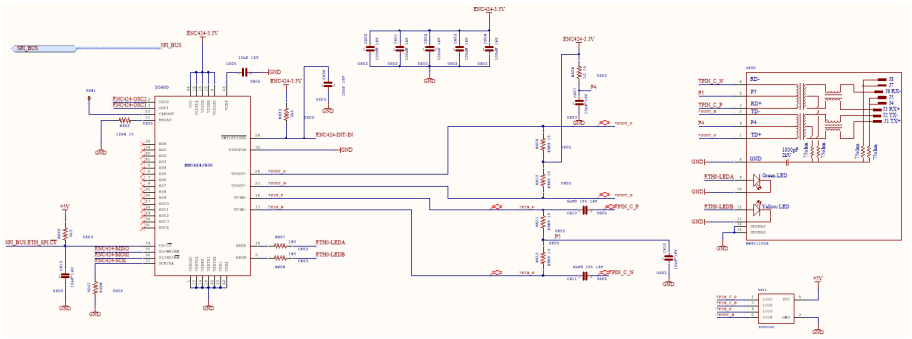


Figure 4.30.: Ethernet controller

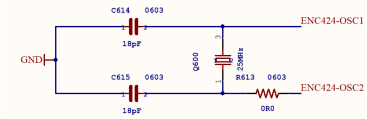


Figure 4.31.: Ethernet controller

Designator	Part
IC600	
R602	12.4kΩ 1% SMD 0603
R603	3.3kΩ SMD 0603
R604	10Ω 1% SMD 0603
R605	3.3kΩ SMD 0603
R606	100kΩ SMD 0603
R607	180Ω SMD 0603
R608	180Ω SMD 0603
R609	49.9Ω 1% SMD 0603
R610	49.9Ω 1% SMD 0603
R611	49.9Ω 1% SMD 0603
R612	49.9Ω 1% SMD 0603
R613	0Ω SMD 0603
C600	100nF 16V SMD 0603
C601	100nF 16V SMD 0603
C602	100nF 16V SMD 0603
C603	100nF 16V SMD 0603
C604	100nF 16V SMD 0603
C605	10µF 16V SMD 0805
C606	10nF 16V SMD 0603
C607	10nF 16V SMD 0603
C610	6.8nF 10% 16V SMD 0603
C611	6.8nF 10% 16V SMD 0603
C612	10nF 16V SMD 0603
C613	10nF 16V SMD 0603
C614	18pF SMD 0603
C615	18pF SMD 0603
Q600	ABM8G-25.000MHZ-B4Y-T
U601	Littelfuse SP0504S - Low Capacitance ESD Protection
J600	HR911105A RJ45 Connector

Table 4.27.

4.9.2. FG09 02 Logic Level Shifter

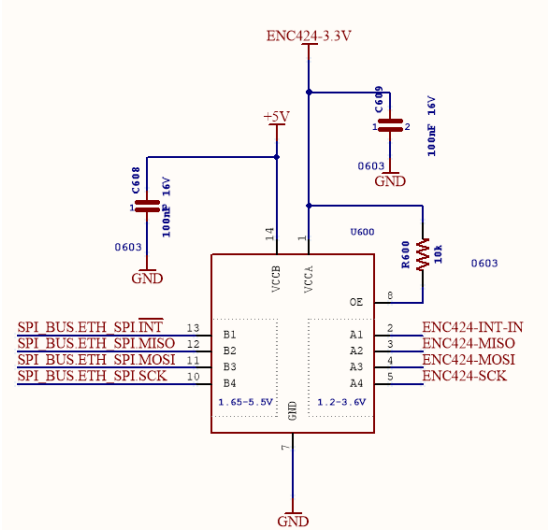


Figure 4.32.: Logic Level Shifter

Designator	Part
U600	Texas Instruments TXB0104 4-Bit Bidirectional Voltage-level Translator
R600	10kΩ SMD 0603
C608	100nF 16V SMD 0603
C609	100nF 16V SMD 0603

Table 4.28.

4.9.3. FG09 03 +3.3V LDO Regulator

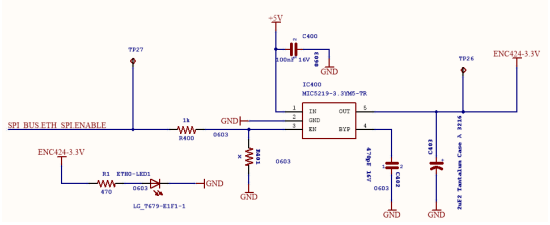


Figure 4.33.: +3.3V LDO Regulator

Designator	Part
IC400	Microchip MIC5219-3.3YM5-TR Linear Voltage Regulator
R400	1kΩ SMD 0603
R401	*
C400	100nF 16V SMD 0603
C402	470pF 16V SMD 0603
C403	2.2µF Tantalum Case A 3216
R1	470Ω SMD 0603
ETH0-LED1	LED

Table 4.29.

4.10. FG10 USB 2.0 to UART Protocol Converter

For functional specification please refer to the Section 3.1.10.

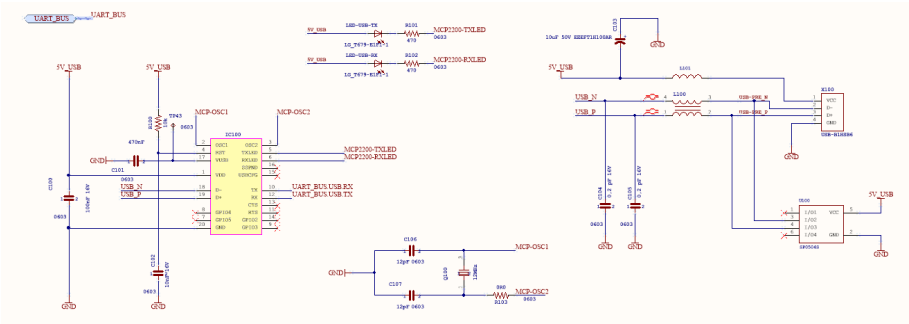


Figure 4.34.: USB 2.0 to UART protocol converter

Designator	Part
IC100	Microchip MCP2200 USB-to-UART Serial Converter
R100	10kΩ SMD 0603
R101	470Ω SMD 0603
R102	470Ω SMD 0603
R103	0Ω SMD 0603
C100	100nF 16V SMD 0603
C101	470nF 16V SMD 0603
C102	10nF 16V SMD 0603
C103	10µF 50V EEE-FT1H100AR Polarized
C104	0.2pF C0G/NP0 SMD 0603
C105	0.2pF C0G/NP0 SMD 0603
C106	12pF SMD 0603
C107	12pF SMD 0603
L100	Suppression Common Mode Choke,WE-744231091
L101	FERRITE BEAD WE-742792651, EMC Filter of USB 2.0 Port
U100	Littelfuse SP0504S - Low Capacitance ESD Protection
Q100	ABM8G-12.000MHZ-4Y-T3
X100	USB Type B Jack
LED-USB-TX	LED
LED-USB-RX	LED

Table 4.30.

4.11. FG11 EEPROM

For functional specification please refer to the Section 3.1.11.

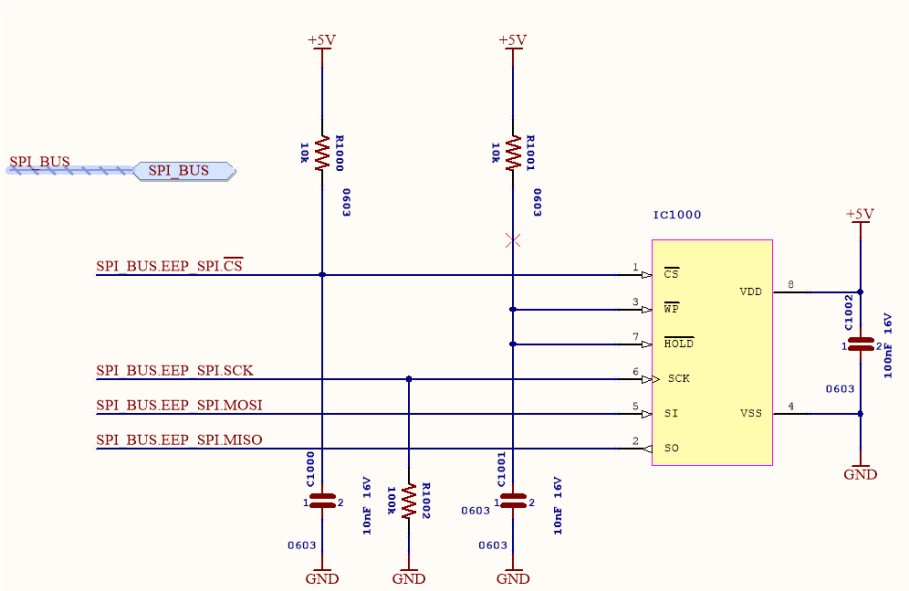


Figure 4.35.: EEPROM

Designator	Part
IC1000	ST M95640-W 64-Kbit serial SPI bus EEPROM
R1000	10kΩ SMD 0603
R1001	10kΩ SMD 0603
R1002	100kΩ SMD 0603
C1000	10nF 16V SMD 0603
C1001	10nF 16V SMD 0603
C1002	100nF 16V SMD 0603

Table 4.31.

4.12. FG12 DIOs

All available digital I/O are protected with following circuit. For functional specification please refer to the Section 3.1.12.

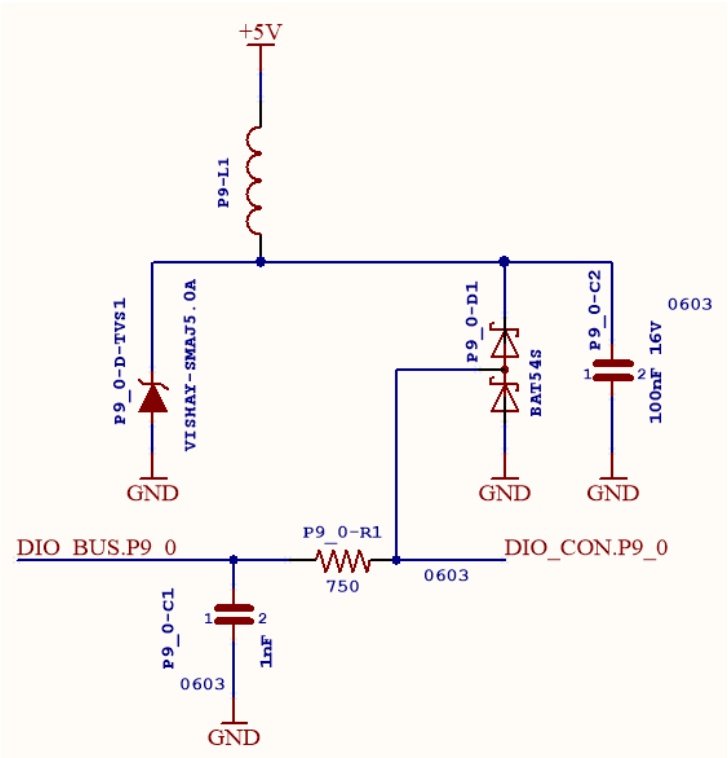


Figure 4.36.: Digital I/O with ESD protection circuit

Designator	Part
*-D-TVS1	VISHAY SMAJ5.0A
*-D1	BAT54S
*-L1	WE-CBF SMD EMI Suppression Ferrite Bead
*-C1	1nF 16V SMD 0603
*-C2	100nF 16V SMD 0603
*-R1	750Ω SMD 0603

Table 4.32.

4.13. FG13 External Connector

For available external connectivity through 37 Pin SUB-D connector see Section 3.1.12. Description of the custom cable (Figure 4.38) can be found in Table 4.34, Table 4.35, Table 4.36, Table 4.37,Table 4.38,Table 4.40 and Table 4.39.

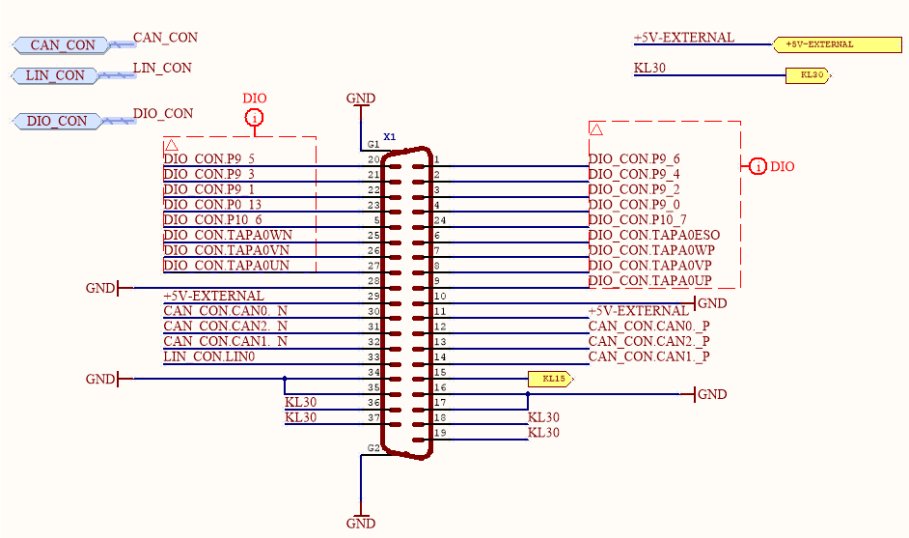


Figure 4.37.: External connector signal assignment

Designator	Part
X1	37 Pin D-SUB Connector

Table 4.33.

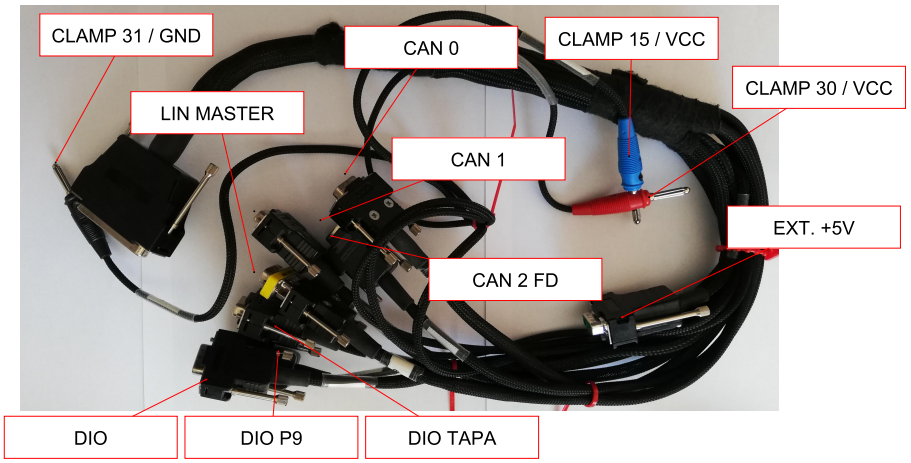


Figure 4.38.: Cable with connectors

$CAN0$		
D-Sub 9 Female Pin	**Function**	**D-Sub 37 Female Pin**
1		
2	$CAN0 - HS - LOW$	30
3	$CLAMP31/GND/Battery(-)$	$10, 16, 17, 28, 34, 35$
4		
5		
6		
7	$CAN0 - HS - HIGH$	12
8		
9		

Table 4.34.: CAN 0

$CAN1$		
D-Sub 9 Female Pin	**Function**	**D-Sub 37 Female Pin**
1		
2	$CAN1 - HS - LOW$	32
3	$CLAMP31/GND/Battery(-)$	10, 16, 17, 28, 34, 35
4		
5		
6		
7	$CAN1 - HS - HIGH$	14
8		
9		

Table 4.35.: CAN 1

$CAN2$		
D-Sub 9 Female Pin	**Function**	**D-Sub 37 Female Pin**
1		
2	$CAN2 - HS - LOW$	31
3	$CLAMP31/GND/Battery(-)$	10, 16, 17, 28, 34, 35
4		
5		
6		
7	$CAN2 - HS - HIGH$	13
8		
9		

Table 4.36.: CAN 2

LIN MASTER		
D-Sub 9 Female Pin	**Function**	**D-Sub 37 Female Pin**
1		
2		
3	$CLAMP31/GND/Battery(-)$	10, 16, 17, 28, 34, 35
4		
5		
6		
7	LIN	33
8		
9	$CLAMP30/Battery(+)$	18, 19, 36, 37

Table 4.37.: LIN Master

DIO TAPA		
D-Sub 9 Female Pin	**Function**	**D-Sub 37 Female Pin**
1	$TAPA0UP/DIO1$	9
2	$CLAMP31/GND/Battery(-)$	10, 16, 17, 28, 34, 35
3	$TAPA0VP/DIO3$	8
4	$TAPA0WP/DIO5$	7
5	$TAPA0ESO/DIO7$	6
6	$TAPA0UN/DIO2$	27
7	$5V - EXTERNAL$	11, 29
8	$TAPA0VN/DIO4$	26
9	$TAPA0WN/DIO6$	25

Table 4.38.: TAPA Connector

DIO P9		
D-Sub 9 Female Pin	**Function**	**D-Sub 37 Female Pin**
1	$P9_0/DIO8$	4
2	$CLAMP31/GND/Battery(-)$	10, 16, 17, 28, 34, 35
3	$P9_2/DIO10$	3
4	$P9_4/DIO12$	2
5	$P9_6/DIO14$	1
6	$P9_1/DIO9$	22
7	$5V - EXTERNAL$	11, 29
8	$P9_3/DIO11$	26
9	$P9_5/DIO13$	25

Table 4.39.: P9 connector

DIO		
D-Sub 9 Female Pin	**Function**	**D-Sub 37 Female Pin**
1	$P10_6/DIO15$	24
2	$CLAMP31/GND/Battery(-)$	10, 16, 17, 28, 34, 35
3	$P0_13/SPI3 - NINT - shared/DIO16$	23
4		
5		
6		
7	$5V - EXTERNAL$	11, 29
8		
9	$P10_7/DIO13$	5

Table 4.40.: DIO connector

4.14. PCB Layout

Figure 4.39, Figure 4.40 and Figure 4.41 show board geometry after routing has been completed. Fully assembled board with top and bottom functional description is shown in Figure 4.42 and Figure 4.43.

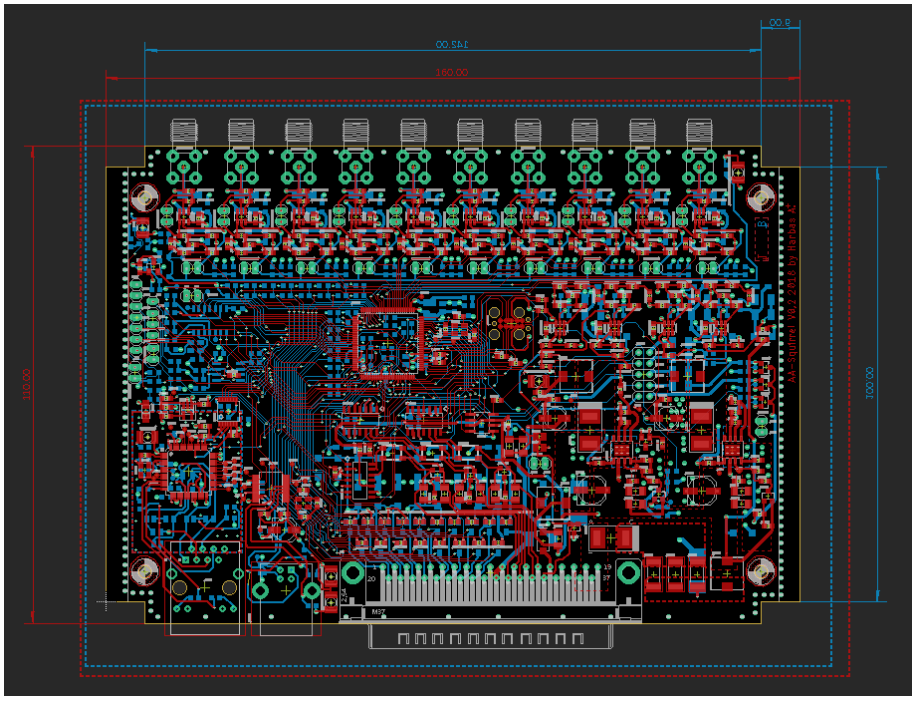


Figure 4.39.: PCB board

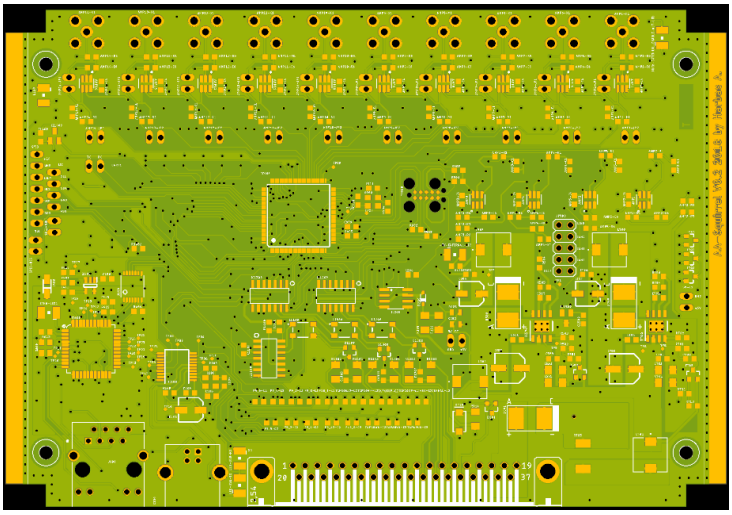


Figure 4.40.: PCB top

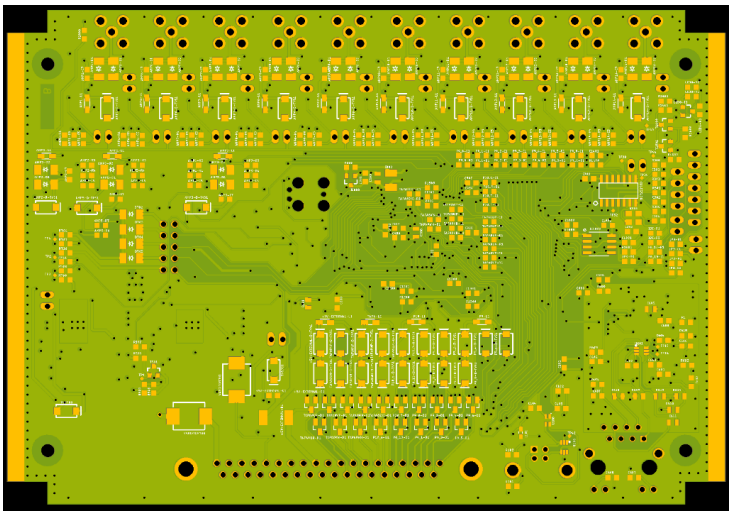


Figure 4.41.: PCB bottom

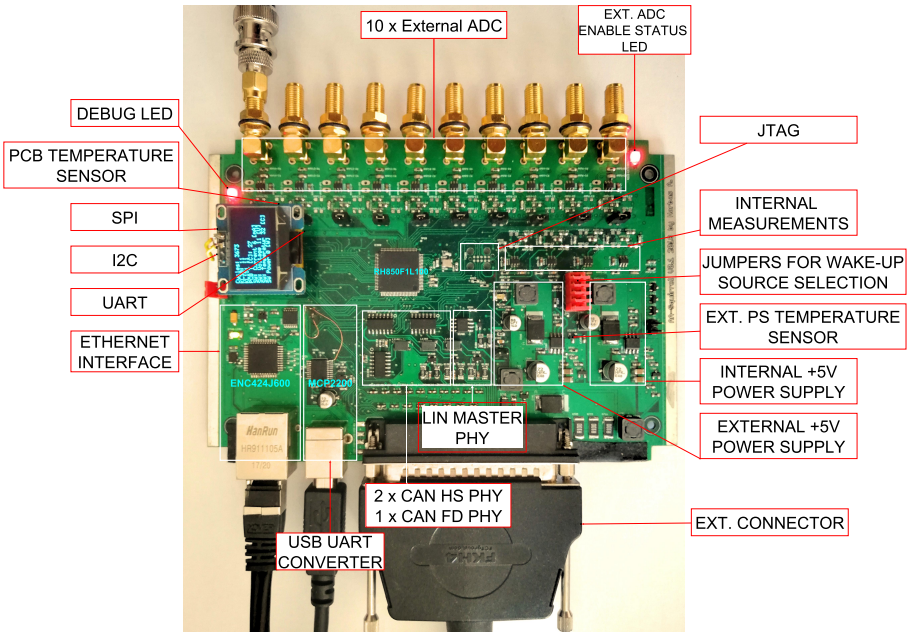


Figure 4.42.: Assembled PCB top

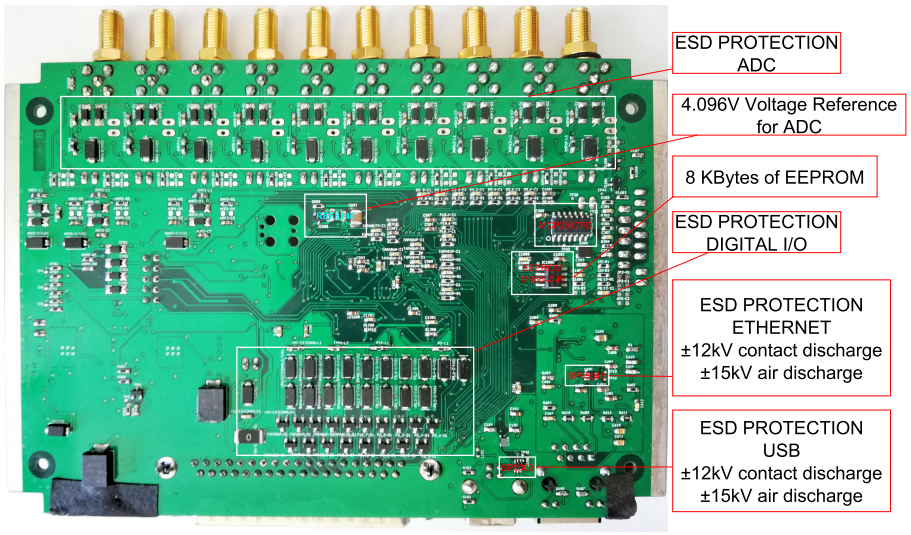


Figure 4.43.: Assembled PCB bottom

5. System Evaluation

This Chapter covers evaluation and correctness of the system. Test performed related to electromagnetic emissions and interference have been performed on Institute of Electronics (IFE) at Technical University of Graz (TUG) under supervision of Ass.Prof. Dipl.-Ing. Dr.tech. Winkler. Please note that most of the low level test were performed during commissioning of the board and will not be covered here. These were basic voltage checks, functional group checks, EEPROM read write tests, CAN - CAN FD gateway test etc. Every test consists of a hardware setup called test bench (TB) and corresponding MATLAB Simulink model. Following test have been performed:

- External ADC channel test
- EXT Power Supply load test
- I/O write test
- SMART Switch test
- LIN test
- EMI test
- ESD test

Please note that CAN and Ethernet interfaces are not tested independently but rather in combination with above listed test. All system interaction (control or/and visualisation) has been performed either by Ethernet (XCP over TCP/IP) or CAN (CANoe) interface.

5.1. External ADC Test

Purpose of the test is to verify accuracy of the external ADC channels. Test is performed on channels one, five and ten.

5.1.1. Setup

Test bench setup is shown in Figure 5.1 and used equipment in Table 5.1. As a DC voltage source Philips PM5131 signal generator is used, where RIGOL DS1054Z acts as a golden device for voltage measurement. Simulink model is shown in Figure 5.2 which actually sends out all external ADC readings over CAN interface. OLED-Display in the model shows basic system information like Clamp-30 voltage, PCB-Temperature, Clamp-15 voltage and ADC channel 1 measurement. Data visualization is performed with Vector CANcaseXL and CANoe control/debug panel shown in Figure 5.3. Voltage is varied over full scale range of ADC ($0V$ - 4.096V).

Hardware

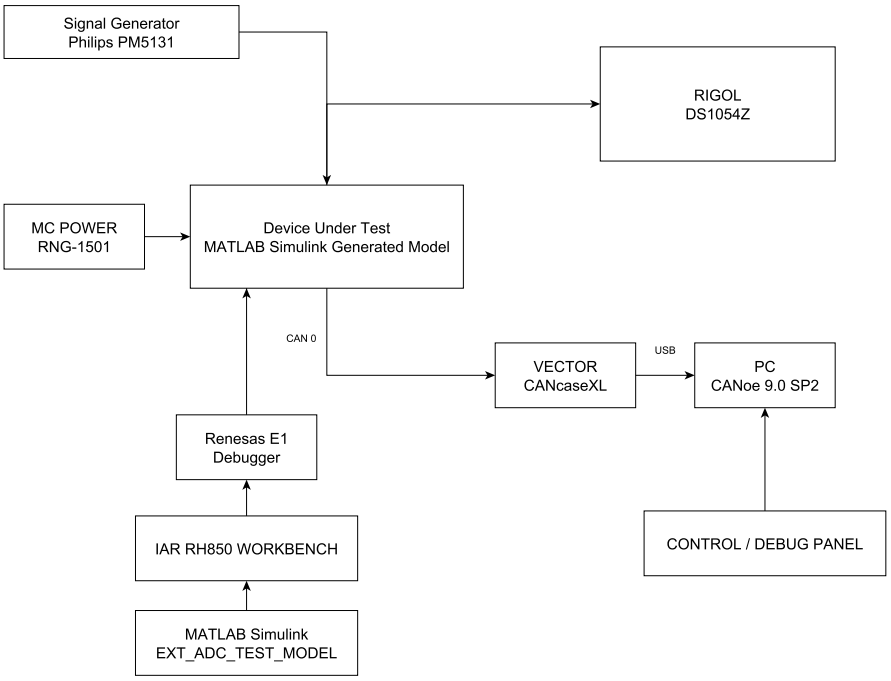


Figure 5.1.: external ADC Test bench setup

Tool Name	Description
RIGOL DS1054	Input voltage measurement
PHILIPS PM5131	Variable DC voltage source
VECTOR CANcaseXL	CAN-Bus to PC
MC POWER RNG-1501	Power supply for Device Under Test
Renesas E1	JTAG Debugger

Table 5.1.: Test bench equipment

Software

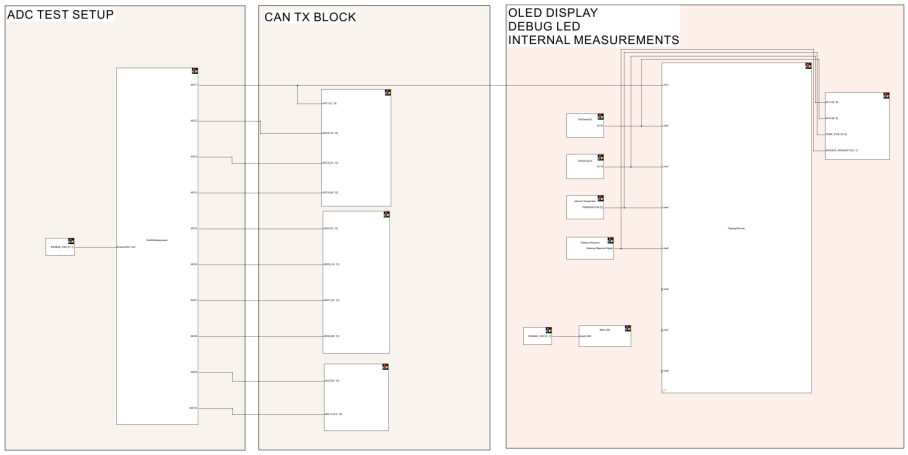


Figure 5.2.: MATLAB Simulink test bench model

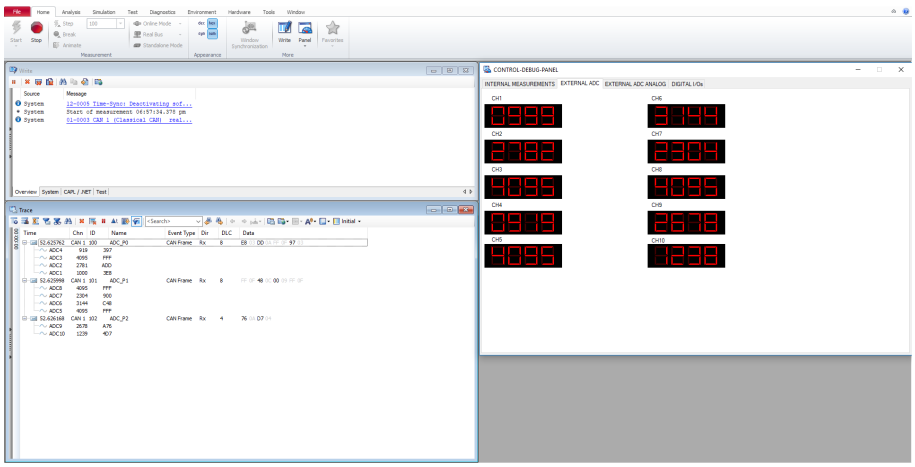


Figure 5.3.: Test bench control/debug panel

5.1.2. Results

Step	V_{IN} adjusted/measured [mV] RIGOL DS1054	CH1 [mV] CANoe Control Panel	CH5 [mV] CANoe Control Panel	CH10 [mV] CANoe Control Panel
1	1	1	1	
2	400	398	396	398
3	800	801	791	799
4	1200	1199	1201	1196
5	1600	1598	1601	1601
6	2000	2000	2009	2004
7	2400	2401	2397	2410
8	2800	2800	2757	2809
9	3200	3168	3155	3168
10	3600	3556	3566	3562
12	4000	3978	3984	3977
13	4080	4048	4061	4051
14	4180	4095	4095	4095

Table 5.2.: Results of ADC CH1,CH5 and CH10 voltage measurement over full scale range

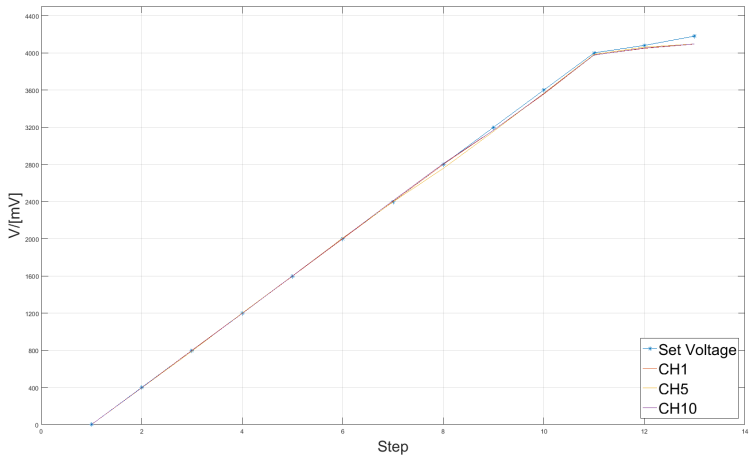


Figure 5.4.: Plot of measured results

5.1.3. Conclusion and Discussion

Obtained results are shown in Figure 5.2 and corresponding plot in Figure 5.4. Voltage is measured in 400mV steps. Results are very close to RIGOL measurements with slightly exception is some ranges which could be related to RIGOL setup of volt/div resolution. Above 4.096V (Step 12) shows ADC saturation where full scale range has been reached.

5.2. EXT Power Supply

Purpose of this test is to examine the behaviour of a power supply under load. Test was performed for 30 minutes, during that time, PS output voltage, PS temperature, output current and ripple voltage were monitored.

5.2.1. Setup

Test bench is shown in Figure 5.5. Total load of 3.916Ω is constructed with twelve in parallel connected 47Ω resistors. Current is measured with Voltcraft VC820 amperemeter and ripple voltage with RIGOL DS1054Z. Simulink model Figure 5.7 is constructed such that PS can be enabled or disabled over CAN bus. Beside that PS temperature and internally measured voltage are sent over CAN bus. Data visualisation and model control are performed using Vector CANcaseXL and CANoe tool.

Hardware

Figure 5.6 shows test bench setup. Equipment used in the test bench is shown in Table 5.3.

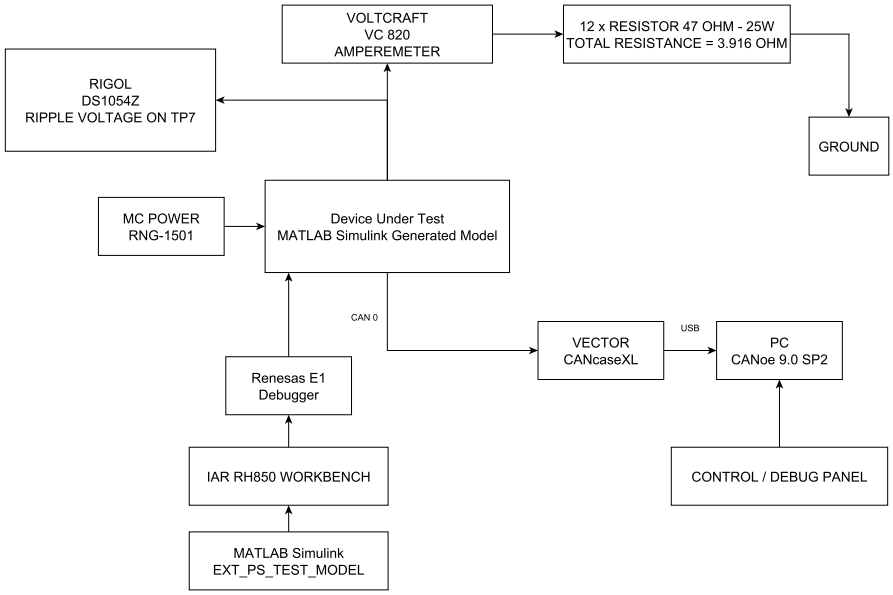


Figure 5.5.: EXT PS test bench setup

Tool Name	Description
RIGOL DS1054	Ripple voltage measurement
VOLTCRAFT VC 820	Amperemeter
VECTOR CANcaseXL	CAN-Bus to PC
MC POWER RNG-1501	Power supply of Device Under Test
Renesas E1	JTAG Debugger
12 x High Power Resistors 47Ω 1%	Load

Table 5.3.: Test bench equipment

Figure 5.6.: EXT PS test bench

Software

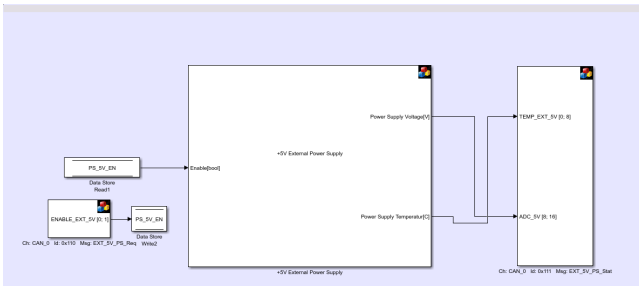


Figure 5.7.: MATLAB Simulink test bench model

Figure 5.8.: Test bench control/debug panel

5.2.2. Results

R_{LOAD} [Ω]	$I_{measured}$ [A]	$I_{calculated}$ [A]	V_{OUT} [mV]	T [°C]	V_{ripple} [mV]
3.916	1.144	1.2768	4979	34	89.20

Table 5.4.: EXT PS test bench results

5.2.3. Conclusion and Discussion

Result obtained are shown in Figure 5.4. Temperature sensor of power supply reported 34°C during test time. Output voltage measured by internal circuit is 4979mV. Ripple voltage measured is 89.20mV which is slightly higher compared to the design parameters (Table 2.4).

5.3. I/O Test

This test verifies functionality of external digital I/Os and cable wiring.

5.3.1. Setup

Test bench setup is shown in Figure 5.9. I/Os are evaluated with logic analyser. Simulink model for all three digital connectors is shown in Figure 5.11, Figure 5.14 and Figure 5.12 which implements seting I/Os either to ”HIGH” or ”LOW” through CAN interface. Control is implemented with CANoe's panel shown in Figure 5.14 which periodically pulse (Period 2s) all digital I/Os of selected connector.

Hardware

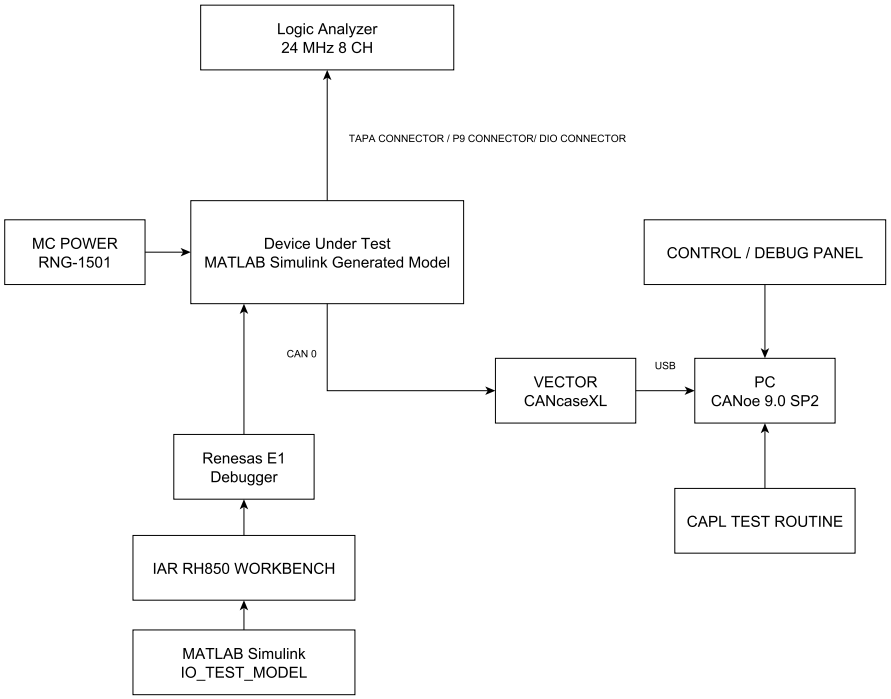


Figure 5.9.: I/O test bench setup

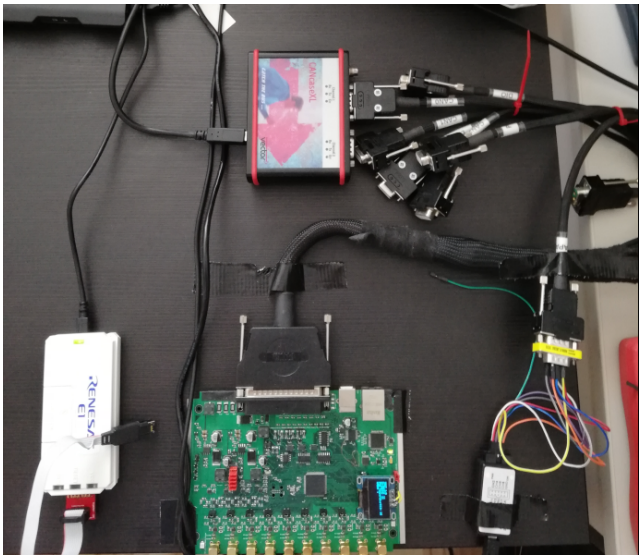


Figure 5.10.: I/O test bench

Tool Name	Description
VECTOR CANcaseXL	CAN-Bus to PC
MC POWER RNG-1501	Power supply for Device Under Test
Renesas E1	JTAG Debugger
8 Channel 24 MHz logic analyser	Test of all connector pins at once

Table 5.5.: Test bench equipment

Software

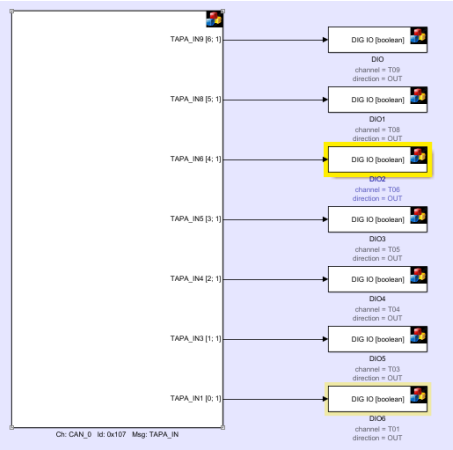


Figure 5.11.: MATLAB Simulink test bench model

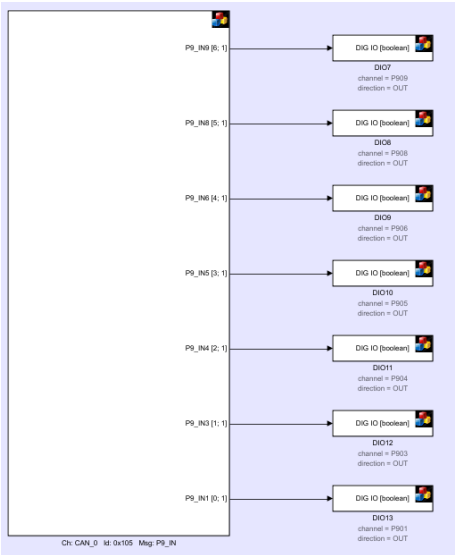


Figure 5.12.: MATLAB Simulink test bench model

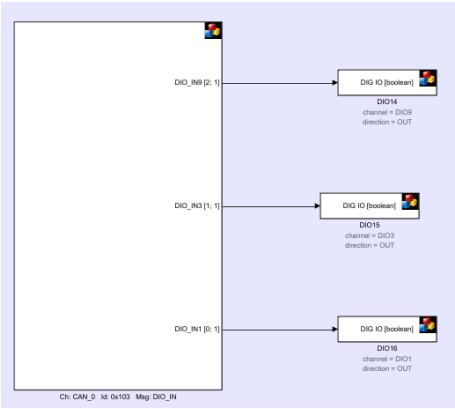


Figure 5.13.: MATLAB Simulink test bench model

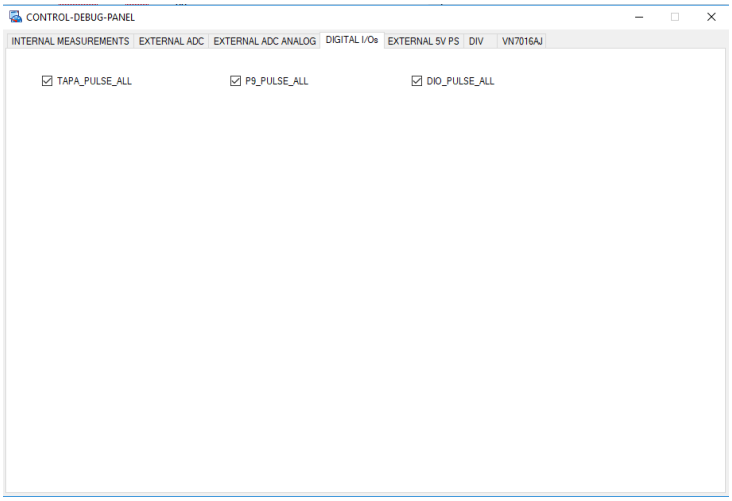


Figure 5.14.: Test bench control/debug panel

5.3.2. Results

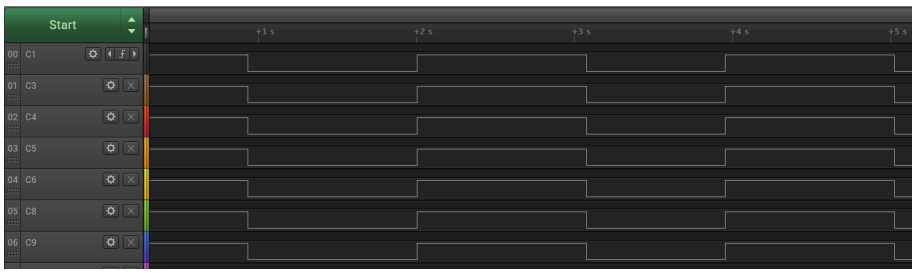


Figure 5.15.: Logic analyser results of P9 connector 1s pulse(all seven pins, see Table 4.39 for pin mapping)

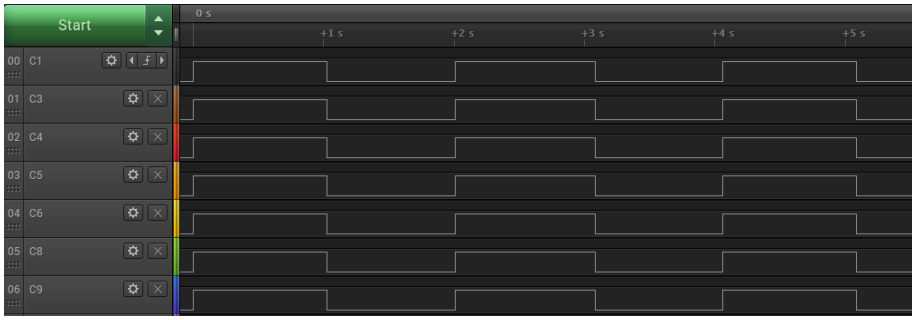


Figure 5.16.: Logic analyser results of TAPA connector 1s pulse (all seven pins, see Table 4.38 for pin mapping)

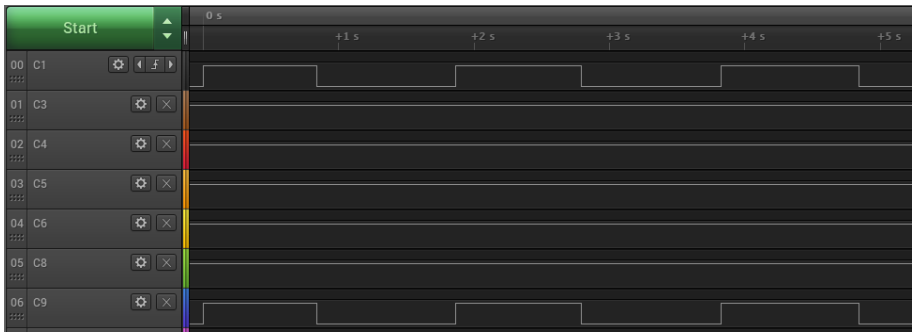


Figure 5.17.: Logic analyser results of DIO connector 1s pulse (all three pins, see Table 4.38 for pin mapping)

5.3.3. Conclusion and Discussion

Logic analyser results are shown in Figure 5.15 for all seven I/Os of P9 connector, Figure 5.16 of TAPA connector and Figure 5.17 for three I/Os of DIO connector. Please not that *P*013 of DIO connector (C3) is shared with SPI3 and is not connected. It can be seen that all I/Os performed correctly.

5.4. SMART Switch

In this test high side switch known as SMART-Switch represents test object which is controlled by device under test (DUT). Detailed information about SMART-Switch can be found in Section 2.6. Purpose of this test is to demonstrate and evaluate capability of DUT to act as controller in a control process loop (Figure 5.18). Test involves control of digital I/Os, EXT ADC channel measurement, implementation of MATLAB Simulink algorithm for diagnosis (Multisense) and XCP for user interaction and data visualisation.

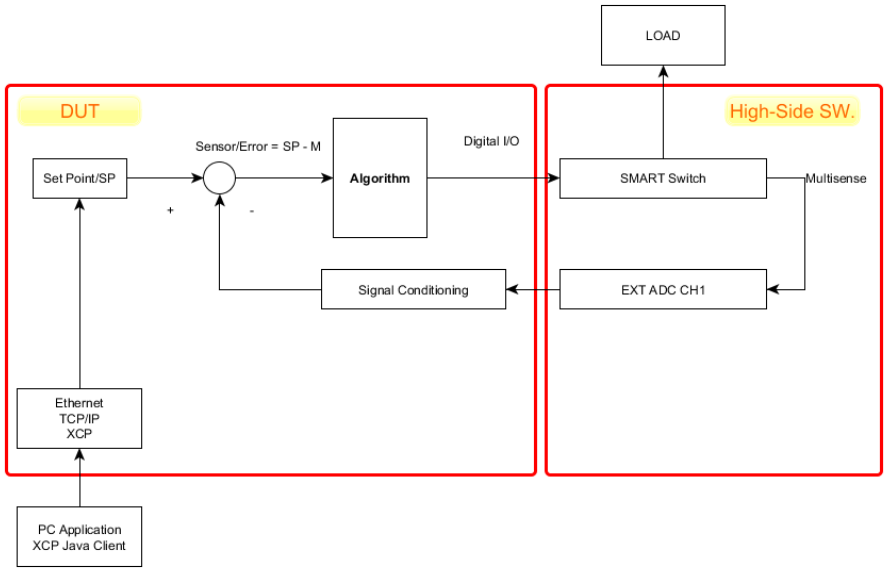


Figure 5.18.: DUT in control loop

5.4.1. Setup

Test bench setup is shown in Figure 5.19. High-Side switch is powered by the same voltage source as DUT. Current through test object is measured by Voltcraft VC820 and a voltage drop across load by RIGOL DS1054Z. Multisense

output of a High-Switch board is connected to external ADC channel-1 of the DUT. Control algorithm is shown in Figure 5.22 which is constructed as a state machine with three different states. In current state, I/O are set such that Multisense give current measurement on multisense output. Similarly the same happens for voltage and temperature sensing. Since current factor K depends on load current, in this test K is selected to be 3800 (See Section 2.6). MATLAB Simulink implementation of a proposed algorithm is shown in Figure 5.23. State machine is implemented in a MATLAB function and I/O control and ADC measurement in Simulink blocks. Custom PC application (Java, XCP-Client library) is shown in Figure 5.24, which gives ability to turn High-Side switch on/off. Beside that application shows all three multisense diagnostic values and calculated power consumption of the load. These values are graphed also in corresponding plots as a function of time.

Hardware

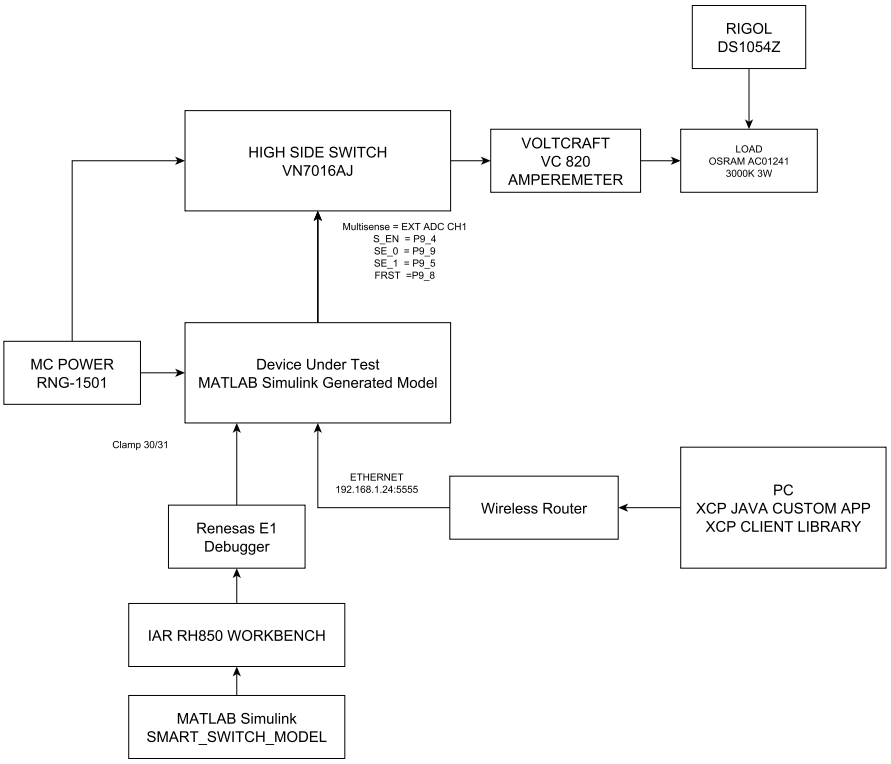


Figure 5.19.: SMART Switch test bench setup

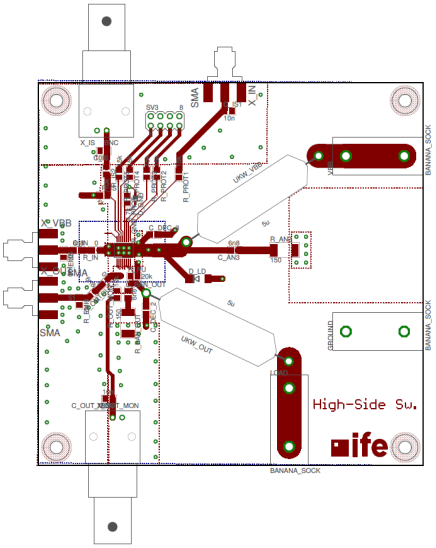


Figure 5.20.: VN7016AJ high side switch board (property of IFE TU GRAZ)

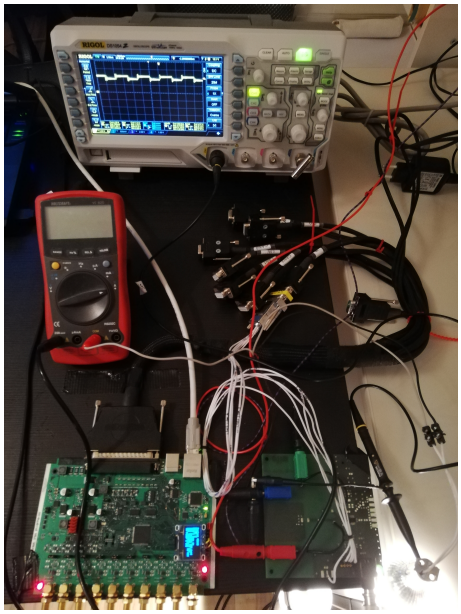


Figure 5.21.: Test bench

Tool Name	Description
RIGOL DS1054	Voltage measurement on load
VOLTCRAFT VC 820	Current through load
MC POWER RNG-1501	Power supply of Device Under Test
Renesas E1	JTAG Debugger
OSRAM AC01241 3000K 3W	Load
High-Side Sw. Board (IFE TU Graz)	Test object

Table 5.6.: Test bench equipment

Software

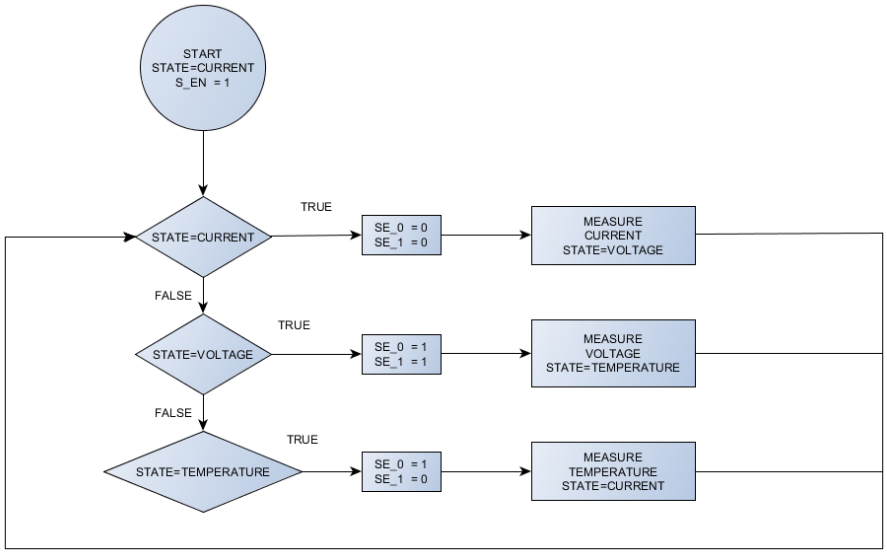


Figure 5.22.: SMART switch multisense algorithm

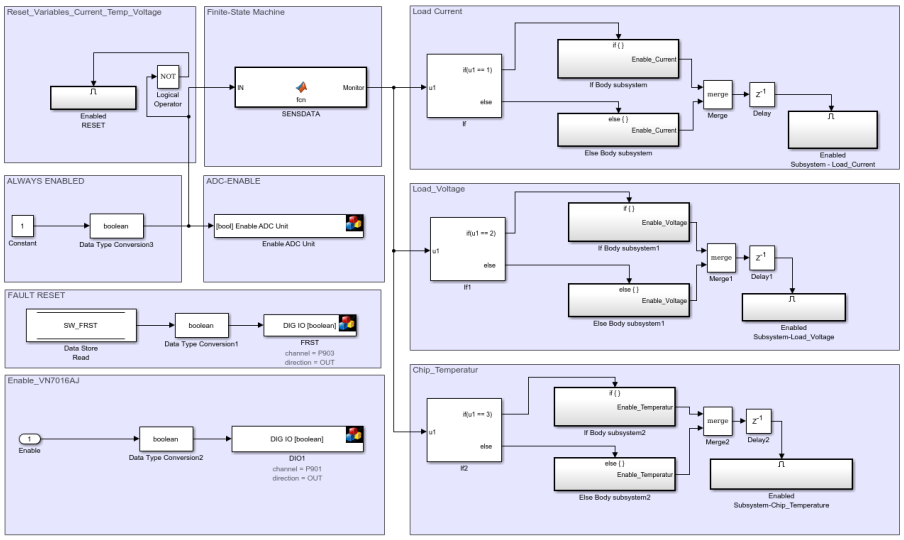


Figure 5.23.: SMART switch multisense algorithm implemented into SIMULINK model

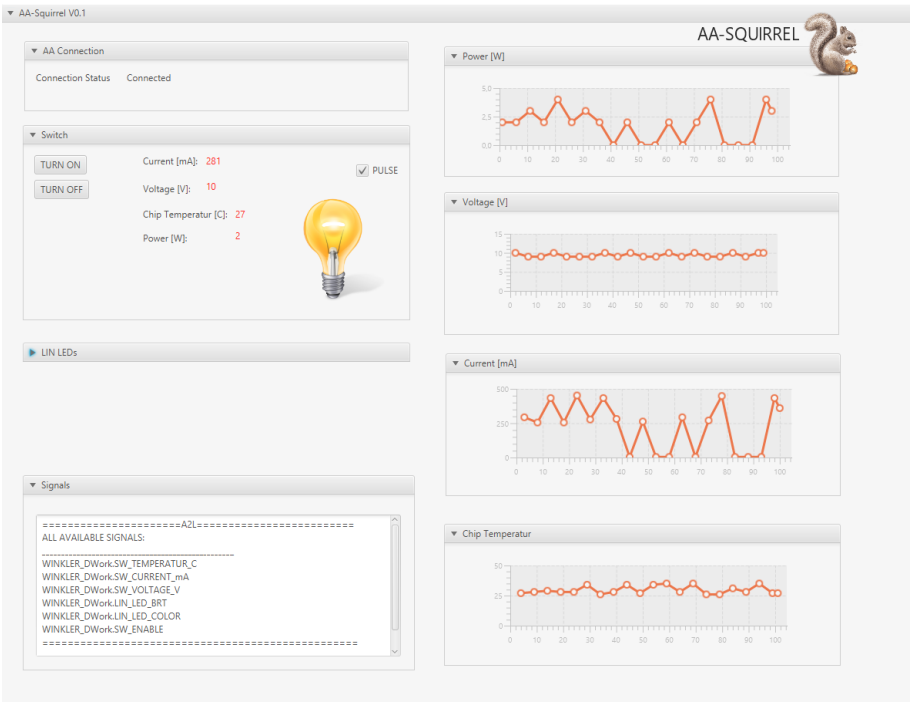


Figure 5.24.: XCP SMART switch java application

5.4.2. Results

V_set [V]	**I_VC820** [mA]	**I_multi** [mA]	**V_multi** [V]	**T_multi** [°C]
7	430	420	7	29
10	296	281	10	28
15	223	219	15	30

5.4.3. Conclusion and Discussion

Multisense measurement were taken by three different input voltages (7,10 and 15V). For all three set voltages (V_{set}), mutisense reported correct values

(see V_{multi}). The reason for deviation of measured current (I_{multi}) compared to excepted I_{VC820} is probably due to factor K, which has been used in Simulink model. This factor K is not constant and varies with a load current. For detailed information about K-factor see Section 2.6.

5.5. LIN

Purpose of this test is to evaluate correctness of LIN-Master interface. Test object used in this test is proprietary hardware (four LIN slave LEDs used as ambient light in the cockpit of a vehicle) without any detailed technical informations available. Only information known are LIN signals for selection of LED colour and brightness given in a LIN Description File (LDF) and the LIN bitrate. In normal use, these LIN slave LEDs have dedicated ECU. This ECU connects to some HMI (over CAN bus) and gives a customer possibility to select desired colour and brightness. Beside LIN correctness, this test demonstrates how easy it is to build prototype ECU and even offer HMI over PC.

5.5.1. Setup

Test bench setup is shown in Figure 5.25. Basically LIN slaves are connected to LIN master of DUT. LIN LEDs are powered by Clamps-30 and 31 trough LIN connector (See Table 4.37). Simulink model is shown in Figure 5.26 implements colour and brightness control of LIN signals through XCP. Corresponding "A2L" file for XCP is shown in Listening 5.1 which specifies "COLOUR" and "BRIGHTNESS" parameters needed by XCP protocol (ECU memory location, size of variable, default variable value etc...). Parameters (colour and brightness) are set from custom PC-Application shown in Figure 5.27.

Hardware

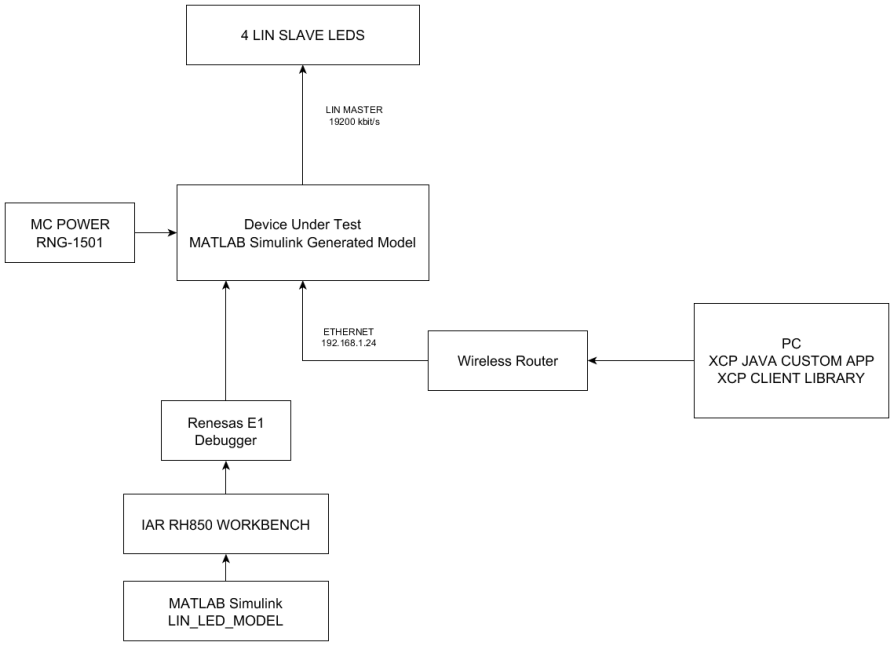


Figure 5.25.: LIN test bench setup

Tool Name	Description
MC POWER RNG-1501	Power supply of Device Under Test
Renesas E1	JTAG Debugger
4 x LIN LED slave	Test object

Table 5.7.: Test bench equipment

Software

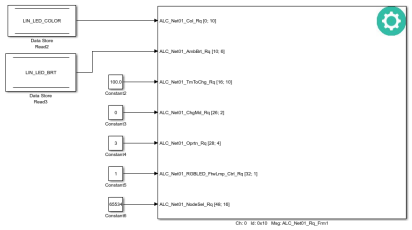


Figure 5.26.: MATLAB Simulink test bench model

```
/begin CHARACTERISTIC AA_TOP_MODEL_DWork.LIN_LED_BRT
VALUE 0xFEDF0AA9 __UBYTE_S 0 NO_COMPU_METHOD 0 255
ECU_ADDRESS_EXTENSION 0x0
EXTENDED_LIMITS 0 255
FORMAT "%.15"
/begin IF_DATA CANAPE_EXT
100
LINK_MAP "AA_TOP_MODEL_DWork.LIN_LED_BRT"
0xFEDF0AA9 0x0 0 0x0 1 0x87 0x0
DISPLAY 0 0 255
/end IF_DATA
SYMBOL_LINK "AA_TOP_MODEL_DWork.LIN_LED_BRT" 0
/end CHARACTERISTIC

/begin CHARACTERISTIC AA_TOP_MODEL_DWork.LIN_LED_COLOR
VALUE 0xFEDF0AA8 __UBYTE_S 0 NO_COMPU_METHOD 0 255
ECU_ADDRESS_EXTENSION 0x0
EXTENDED_LIMITS 0 255
FORMAT "%.15"
/begin IF_DATA CANAPE_EXT
100
LINK_MAP "AA_TOP_MODEL_DWork.LIN_LED_COLOR"
```

```
0xFEDF0AA8 0x0 0 0x0 1 0x87 0x0
DISPLAY 0 0 255
/end IF_DATA
SYMBOL_LINK "AA_TOP_MODEL_DWork.LIN_LED_COLOR" 0
/end CHARACTERISTIC
```

Listing 5.1: A2L file for control of LIN LEDS signals

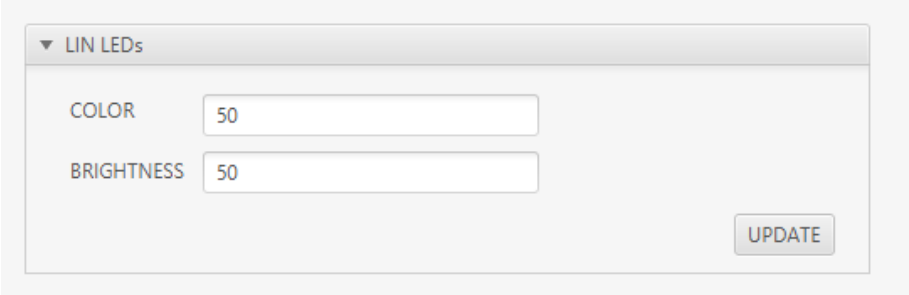


Figure 5.27.: XCP java control application

5.5.2. Results

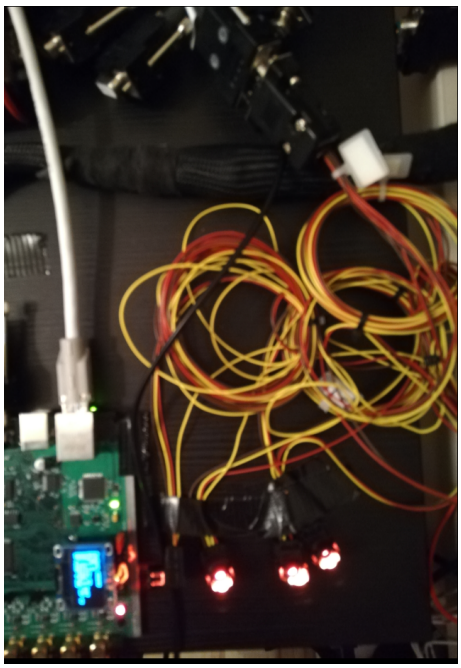


Figure 5.28.: LIN slaves

5.5.3. Conclusion and Discussion

This test does not involve any testing metric but rather visual inspection shown in Figure 5.28. It can be reported that LEDs responded each time different combinations of ”COLOUR” and BRIGHTNESSES” were set.

5.6. Electromagnetic Emissions

In order to make sure overall radiated emissions of a constructed system are within tolerable levels, EMI tests under different conditions have been performed. Please not that test setup performed were not exactly matched to the EN55022 regulations. Nevertheless results obtained give good indication if the system is capable of passing EMC tests.

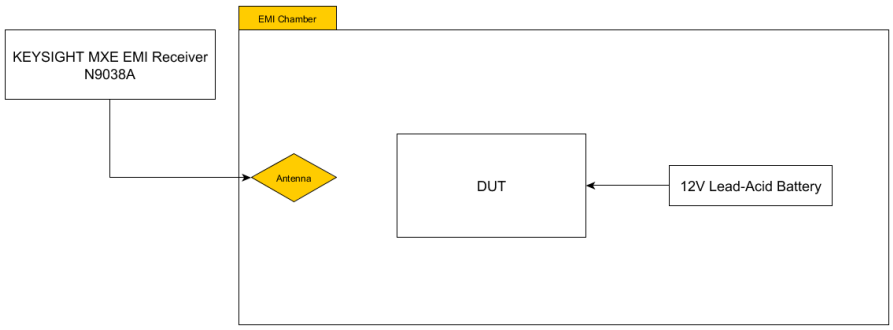
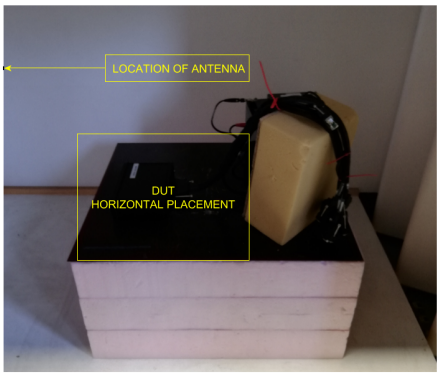
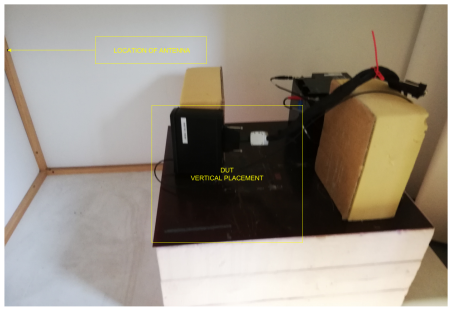


Figure 5.29.: EMI test setup



(a) Horizontally placed DUT in a chamber



(b) Vertically placed DUT in a chamber

All EMI test have been performed with the same setup as shown in Figure 5.29. Horizontal and vertical placement of a DUT (Figures 5.30a and 5.30b) should maximize reception of potential emissions in a direction of the antenna.

Figure 5.31.: Spectrum

Figure 5.31 shows an example of measured field strength (Start Frequency: 30MHz, Stop Frequency: 1GHz) by EMI receiver. Yellow line represents envelop under which measured interference is within limits. Limits are set according EN 55022 standard for radiated emissions and correspond to the Class B (residential environment) emissions limits [16]. Electric field strength for radiated emissions is measured in decibel-microvolts per meter (dBµV/m).

EMI-Receiver setup is shown in Table 5.8. Two antennas are used to cover full spectrum. One antenna covers spectrum from 30MHz to 119MHz, and the

other from 119MHz to 1GHz.

Characteristic	Description
Start Frequency	30MHz
Stop Frequency	1GHz
Detector	Quasi-Peak Detector
Measurement Time (dwell)	1s
RBW	120kHz (6 dB)
Limits	EN 55022, Radiated, Class B, 30 MHz to 1 GHz (10m)

Table 5.8.: EMI receiver setup

5.6.1. Radiated EMI - Test 1

Setup

Device is placed horizontally. Active parts of the system are CAN and LIN.
No ferrite bead has been placed around cable yet.

Result

Figure 5.32.: Spectrum

5.6.2. Radiated EMI - Test 2

Setup

The same test configuration as in a Test 5.6.1 with the exception that ferrite bead has been placed around cable.

Result

Figure 5.33.: Spectrum

5.6.3. Radiated EMI - Test 3

Setup

The same configuration as in a Test 5.6.2 but vertically placed DUT.

Result

Figure 5.34.: Spectrum

5.6.4. Radiated EMI - Test 4

Setup

The same configuration as in a Test 5.6.3 plus 50cm coaxial cable connected to SMA connector of a external ADC channel 1.

Result

Figure 5.35.: Spectrum

5.6.5. Radiated EMI - Test 5

Setup

The same configuration as in a Test 5.6.4 with enabled external 5V power supply and without ferrite bead around cable.

Result

Figure 5.36.: Spectrum

5.6.6. Radiated EMI - Test 6

Setup

The same configuration as in a Test 5.6.5 but now with ferrite bead around cable.

Result

Figure 5.37.: Spectrum

5.6.7. Conclusion

First EMI test Subsection 5.6.1 shows emission violation of specified limits at following frequency:

- 115.26MHz - 4.698dB
- 149.96MHz - 0.146dB
- 157.04MHz - 2.094dB

After applying ferrite bead around cable (reduces cable radiation by introducing impedance mismatch between source and cable and by making cable

behave like a bad antenna)). Test in Subsection 5.6.2 which is identical to the first test with exception that ferrite was added shows far more better results where only component left that violates limits was at 156.02MHz and was 1.957dB over the limit. The same test was repeated by placing the device in vertical position. Test in Subsection 5.6.3 shows that this change did not have much impact, still single violation slightly shifted to 160.04MHz and 1.611dB over the limit envelope. Test in Subsection 5.6.4 where coaxial cable was attached to external ADC shows that some spectral components increased but no new violation occurred except the one that happened in previous test. Test in Subsection 5.6.5 shows the results of a device where almost everything was turned on (all device subsystems were active) and ferrite bead from the cable is removed again. Again three violations occurred with very similar values and frequencies that occurred in the first test. It is obvious that this emissions are coming from the cable. After applying the ferrite bead to the same configuration, emissions reduced significantly leaving the two violations around 150MHz. No further research was made in order to find possible reasons for these violation. Also violations found do not necessarily mean that the units failed EMI testing, since the test setup was not normed.

5.7. Electrostatic Discharge Immunity Test - IEC 61000-4-2

IEC 61000-4-2 is a international immunity test that proves ability of electronic equipment to withstand ESD generated from human body or metal objects with a built up static charge. The current waveform generated from ESD-Gun corresponds the wave form generated in a condition where electrified human body is discharged. For more information see Section 2.10.

5.7.1. Setup

Test setup is shown in Figure 5.38. Please note that test setup is not strictly carried out according the standards defined by IEC 61000-4-2. ESD discharge impulses (see Table 5.10) were applied to the following parts of the system:

- Digital P9_01 pin

- External ADC channel 1
- Different parts of DUT enclosure
- Shielding of D-Sub 37 connector

During ESD stressors, DUT was operational and in a exactly the same setup as it was presented in High-Side-Test-Bench in Section 5.4.

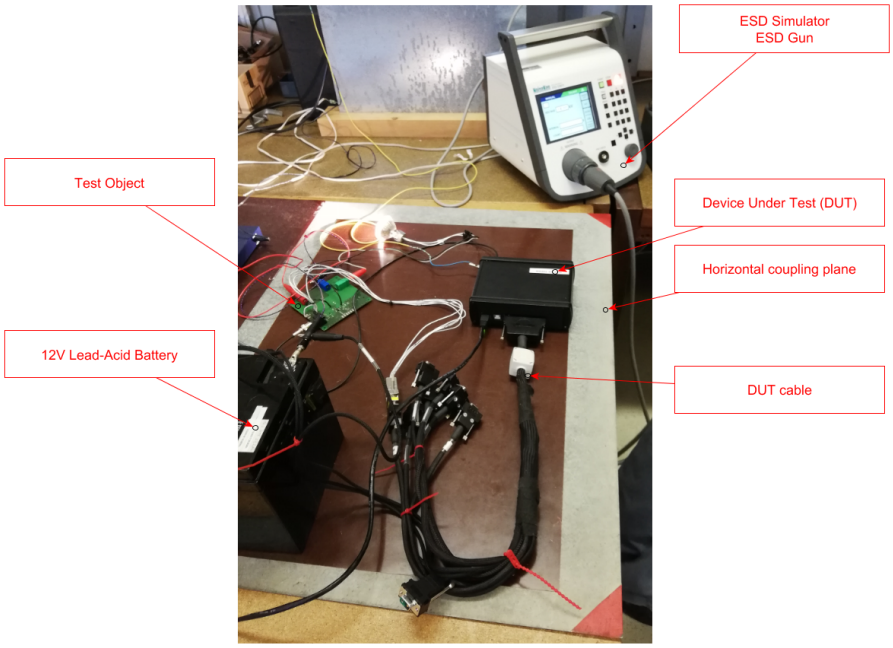


Figure 5.38.: ESD test setup

Tool Name	Description
NoiseKen ESP-S3011	ESD Simulator-Gun
12V Lead-Acid Battery	DUT power source

Table 5.9.: ESD test equipment

Characteristic	Description
Output Voltage	4kV
Polarity	Positive and Negative
Discharge Interval	1 s
Number of Discharges	5

Table 5.10.: ESD impulse characteristics

5.7.2. Results and Discussion

This test does not provide any quantitative results but rather observations. During and after all ESD stressors performed on it, the DUT was correctly operational. Parts like external ADC channel-1 and digital P9_01 on which ESD-Tests have been performed are directly involved in control of a test object and any malfunction of these parts should directly impact correctness of a test object operation. No faults could be determined on the unit.

6. Discussion

Verification test carried out in the Chapter 5 shows that the achievements of system are very acceptable. Nevertheless some improvements would be necessary. Initial input stage of external ADC channels was constructed with cascaded anti-aliasing low pass filters. This approach creates high input impedance to the SH circuit of a SAR ADC which leads a sample voltage to settle incorrectly on the SH capacitor. Operational amplifier TI-TLV34xx used for filtering has a slew rate of 0.9V/µs. Assuming applied input voltage is 4.096V (maximal input voltage). The TLV34 operational amplifier needs 4.511µs to settle its output (forward settle) to the input voltage (see Equation 6.1). ADC acquisition time is 3µs which shows that the slew rate of a used operational amplifier is insufficient and the voltage sampled may be incorrect.

$$t_{settle} = \frac{4.096V}{0.9}\mu s = 4.511\mu s \tag{6.1}$$

Solution to this problem would be to use operational amplifier with higher slew rate, as for example TI OPA 836 which has a slew rate of 560V/µs. The settle time with this amplifier would be only 0.0073µs.

During integration of a LWIP TCP/IP, the size of RAM in a microcontroller became a problem. RAM size of $64KB$ may become insufficient specially when SIMULINK models are large. This problem has been solved by placing all LWIP buffers into so called "Retention RAM Area" which has a size of $32KB$. Speed of Ethernet may become an issue specially when to much signals in XCP communication are involved. This issue is directly related to the memory limitation of the MCU. Solution two this problem would be to use a MCU with more RAM. Like for example Renesas RH850 R7F701649, which is very similar to RH850 F1L used in this research. Alternative solution would be to make a modular system with two units. First unit could have at least a Ethernet and CAN interface and act as XCP-CAN gateway. The second system

would be identical to the unit constructed in this master thesis. This approach would increase overall system performance and make it more predictable, since Ethernet services are very CPU intensive tasks and may affect overall real-time capability of a system.

ADC (AVREF) is supplied with a voltage reference which can deliver maximal current of 25mA. According to the RH850 specifications ADC can draw up to 48mA of current. It is obvious that the used reference may not deliver sufficient current to all ADC channels.The solution to this problem would be to use a buffer circuit between voltage reference and ADC supply pin which can deliver required current but keep the voltage reference stable.

Internal measurements like the one for Clamp-15 and 30 voltage measurements, use simple voltage dividers for adjusting a voltage level to the ADC inputs. This approach creates a constant power dissipations. Improvements could be made by making voltage divider switchable (e.g. NMOS transistor). This would require at least one IO of the MCU to turn divider(s) on when measuring and off when they are not used.

Great caution must be taken when implemented algorithm in Simulink depends on execution order. Execution order of a generated code does not follow strictly Simulink model unless it has been specified. The priority found in ”Block Properties” specifies the order of a code generation. Block with lower priority has precedence over a block with a higher priority. Assuming Simulink model has two CAN blocks. One transmit and one receive block. In order to make sure the CAN signals are firstly receiver and then transmitted, the receive block must have lower priority than the transmit block. This would force a Simulink to generate code in a right order.

Some drawbacks of a XCP protocol are that if a firmware of ECU changes (meaning addresses of a signals have changed), new A2L must be generated and reloaded in all custom application where it was used. An example would be a test case with the SMART-Switch. If the Simulink model of this example is to change, the application which uses A2L for XCP communication, must update new A2L in order to work correctly. One possible issue of a XCP that could be seen as a limitation is that it supports only single master. A slave device can only have one master, but a master can have multiple slaves.

7. Conclusion

This master thesis covers almost all aspects of electronic unit construction, from the idea to fully functional unit. In introduction part comparison of existing similar control units and different aspects of implementation have been discussed. Technical background of the thesis covers most of the relevant knowledge a reader should get in order to understand the concept and technologies used in this thesis. System design focuses mainly on the problem of a system decomposition into a functional groups and their structural organisation. Also correlation of these groups are discussed and how they sum up in order to fulfil requested requirements. Beside that, the system design covers the technical details and the component identification required for implementation. Both hardware and software architectures are discussed here. Implementation part of thesis focuses mainly on hardware realisation of the unit. This includes schematics of the device, mechanical parts, PCB, packaging etc. Evaluation parts tries to verify correctness of the unit by comparing the acceptance criteria extracted from the initial requirements. Detailed verification of all system components and specification would be beyond the scope of this thesis and could be a subject of other project. All relevant findings, issues and potential solutions are presented in final discussion. At the time of doing this research one interesting System-on-Chip (SOC) has been discovered. It is Xilinx Zynq 7000 SOC, which would improve this concept in term of performance and flexibility significantly. Theoretical this SOC could offer not only software Simulink function-blocks, but hardware too. Depending on application requirements one could select between hardware and software algorithm implementation. Most of the automotive interfaces could be implemented as a IP-Cores which would make them very versatile to standard changes. The drawback of such unit would be implementation complexity and the price. This approach gives a huge flexibility by following the same idea and could be a subject of future work.

Appendix

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Appendix A.

Pin Mappings

A.1. CPU Pin Mapping

PORT	SYMBOL	TYPE	NAME
JTAG port 0	JP0_0	Debug/Prog	DCUTDI
	JP0_1	Debug/Prog	DCUTDO
	JP0_2	Debug/Prog	DCUTDCK
	JP0_3	Debug/Prog	DCUTDMS
	JP0_4	Debug/Prog	DCUTDRST
	JP0_5	Debug/Prog	DCUTDRDY

PORT	SYMBOL	TYPE	NAME
Port 0	P0_0	CAN0-TX	CAN0-TX
	P0_1	CAN0-RX	CAN0-RX
	P0_2	CAN1-RX	CAN1-RX
	P0_3	CAN1-TX	CAN1-TX
	P0_4	CSIH1SI	ETH0-SDO
	P0_5	CSIH1SO	ETH0-SDI
	P0_6	CSIH1SC	ETH0-SCK
	P0_7	RLIN21RX	LIN0-RX (Pullup is very important!)
	P0_8	RLIN21TX	LIN0-TX
	P0_9	INTP12	ETH0-NINT
	P0_10	INTP3	CAN2-NINT
	P0_11	RIIC0SDA	I2C-SDA
	P0_12	RIIC0SCL	I2C-SCL
	P0_13	INTP12	SPI3-NINT
	P0_14	Normal Port	ETH0-ENABLE
Port 8	P8_0	Normal Port	CAN0-NERR
	P8_1	TAPA0ESO	TAPA0ES0
	P8_2	Normal Port	CAN0-NSTB
	P8_3	Normal Port	CAN1-NERR
	P8_4	Normal Port	CAN1-EN
	P8_5	Normal Port	CAN1-NSTB
	P8_6	Normal Port	LIN0-NSLP
	P8_7	Normal Port	CAN2-NERR
	P8_8	Normal Port	CAN2-EN
	P8_9	Normal Port	CAN2-NSTB
	P8_10	Normal Port	ETH0-NCS
	P8_11	Normal Port	CAN2-NCS
	P8_12	Normal Port	EEP-NCS
Port 9	P9_0	Normal Port	P9_0
	P9_1	Normal Port	P9_1
	P9_2	Normal Port	P9_2
	P9_3	Normal Port	P9_3
	P9_4	Normal Port	P9_4
	P9_5	Normal Port	P9_5
	P9_6	Normal Port	P9_6

PORT	SYMBOL	TYPE	NAME
Port 10	P10_0	TAPA0UP	TAPA0UP
	P10_1	TAPA0UN	TAPA0UN
	P10_2	TAPA0VP	TAPA0VP
	P10_3	TAPA0VN	TAPA0VN
	P10_4	TAPA0WP	TAPA0WP
	P10_5	TAPA0WN	TAPA0WN
	P10_6	Normal Port	P10_6
	P10_7	Normal Port	P10_7
	P10_9	Normal Port	CAN0-EN
	P10_10	Normal Port	ADC0-EXTERNAL-ENABLE
	P10_11	RLIN31RX	UART-RX-USB
	P10_12	RLIN31TX	UART-TX-USB
	P10_13	RLIN32RX	UART1-RX
	P10_14	RLIN32TX	UART1-TX
	P10_15	Normal Port	SPI3-NCS/P10_15-LED
Port 11	P11_0	Normal Port	POW-HOLD
	P11_1	Normal Port	5V-EXTERNAL-ENABLE
	P11_2	CSIH2SO	CAN2-SDI
	P11_3	CSIH2SC	CAN2-SCK
	P11_4	CSIH2SI	CAN2-SDO
	P11_5	CSIH3SI	EEP-SDO
	P11_6	CSIH3SO	EEP-SDI
	P11_7	CSIH3SC	EEP-SCK

PORT	SYMBOL	TYPE	NAME
Analog Port 0	AP0_0	Normal Port	KL30-ADC
	AP0_1	Normal Port	INT-TEMP-ADC
	AP0_2	Normal Port	KL15-ADC
	AP0_3	Normal Port	5V-EXT-ADC
	AP0_4	Normal Port	5V-EXT-TEMP-ADC
	AP0_5	Normal Port	WAKE-UP-REQUEST-ADC
	AP0_6	Normal Port	ADC-EXTERNAL-1
	AP0_7	Normal Port	ADC-EXTERNAL-2
	AP0_8	Normal Port	ADC-EXTERNAL-3
	AP0_9	Normal Port	ADC-EXTERNAL-4
	AP0_10	Normal Port	ADC-EXTERNAL-5
	AP0_11	Normal Port	ADC-EXTERNAL-6
	AP0_12	Normal Port	ADC-EXTERNAL-7
	AP0_13	Normal Port	ADC-EXTERNAL-8
	AP0_14	Normal Port	ADC-EXTERNAL-9
	AP0_15	Normal Port	ADC-EXTERNAL-10