Zlatko Bosnjic

Half bridge based on Silicon carbide MOSFETs- Design and Evaluation

MASTER'S THESIS

to achieve the university degree

Diplom-Ingenieur

Master's degree programme: Electrical Engineering

submitted to

Graz University of Technology

Supervisor:

Krischan Klaus, Ass.Prof. Dipl.-Ing. Dr.techn.

Electric Drives and Machines Institute

Graz University of Technology

Graz, June, 2021

EIDESSTATTLICHE ERKLÄRUNG

AFFIDAVIT

Ich erkläre an Eides statt, dass ich die vorliegende Arbeit selbstständig verfasst, andere als die angegebenen Quellen/Hilfsmittel nicht benutzt, und die den benutzten Quellen wörtlich und inhaltlich entnommenen Stellen als solche kenntlich gemacht habe. Das in TUGRAZonline hochgeladene Textdokument ist mit der vorliegenden Masterarbeit identisch.

I declare that I have authored this thesis independently, that I have not used other than the declared sources/resources, and that I have explicitly indicated all material which has been quoted either literally or by content from the sources used. The text document uploaded to TUGRAZonline is identical to the present master's thesis.

_____ _____

Datum / Date Unterschrift / Signature

Kurzfassung

Der Umfang dieser Arbeit ist das Design, die Entwicklung und das Testen einer Halbbrücke basierend auf Siliziumkarbid-Leistungs-MOSFETs zum Einsatz im Bereich elektrischer Antriebe. Der Wirkungsgrad der Halbbrücke bei erhöhter Schaltfrequenz war der Mittelpunkt des Designs. Für diese Anwendung wurde eine Platine entwickelt und hergestellt. Das Schaltverhalten wurde mittels Doppelpuls Test (DPT) als Charakterisierunsmethode für unterschiedliche Betriebsbedingungen, wie z.B variierende Zwischenkreisspannung und unterschiedliche Lasten, getestet. Überstromschutz wurde ausführlich überprüft.

Abstract

The scope of this thesis is the design, development and testing of a half bridge based on silicon-carbide power MOSFETs for application in electric drives. Half bridge efficiency at elevated switching frequencies was the focus point of the design. A dedicated printed circuit board was designed and manufactured for this application. Switching behavior of the device was tested using the Double Pulse Test (DPT) as a characterization method for different operating conditions, such as varying DC-Link voltage and different load currents. Over-current and protection was tested extensively as well.

Contents

1 Introduction

Electrical power conversion allows for processing and control of the flow of electric energy. The end-user load is supplied with voltages and currents best suited for the intended application [1]. Devices that convert electrical energy from one form to another are called power converters. They are usually subdivided into four categories:

- DC to DC converters
- DC to AC converters
- AC to DC converters
- AC to AC converters

The half bridge topology that is developed and discussed in this paper can be used as a bidirectional DC to DC converter as well as a phase leg of a DC to AC inverter. This thesis focuses on DC to AC conversion of electrical energy.

The demand for higher power density, as well as higher efficiency power converters is steadily increasing. Wide bandgap materials, such as silicon-carbide (SiC) and gallium-nitride (GaN) are emerging as viable alternatives for standard silicon (Si) switching devices. Advantages of wide bandgap semiconductors are increased operating voltage limits, higher switching speeds and lower specific on-state resistance when compared to silicon devices [2]. These properties of silicon-carbide allow for a reduction in power converter size as well as output filter size and weight, while also decreasing the power loss due to switching and on-state conduction. Although the design of electric power converters based on wide bandgap materials is similar to the design of silicon-based devices, extra caution must be taken to limit voltage and current ringing, as well as electromagnetic interference (EMI) [3] caused by significantly higher switching speeds, lower voltage rise times and lower current rise times when compared to silicon devices.

2 Comparison of Si and SiC power MOSFETs

Due to the inherent material properties of silicon-carbide when compared to the properties of silicon, its use is well suited for switching devices, especially for medium-voltage and high-power applications such as electric drives. Table 1 shows an overview of material properties of interest for both silicon and silicon-carbide.

In the 600 V range, the SiC power Metal Oxide Semiconductor Field Effect Transistor (MOSFET) has strong competitors - the superjunction Si MOSFET and Si IGBT. However, for higher blocking voltages, e.g. 1.2 kV and 1.7 kV, the SiC power MOSFET shows a clear advantage when on-state conduction losses are compared [4]. An additional benefit of SiC MOSFETs when compared to Si IGBT is the ability to operate in the third quadrant, reducing the conduction losses and eliminating the need for an anti-parallel diode [5].

Material	E_g	E_C	ϵ_r	λ	T_{MAX}
-	eV	V/cm	-	W/(cm*K)	°C
Si	1.1	$3 \cdot 10^5$	11.7	1.5	200
4H-SiC	3.2	$3 \cdot 10^6$	10	5	600

Table 1: Comparison of Si and SiC material properties [6]

As shown in Table 1, a ten-fold increase in the breakdown electric field strength E_C allows for a reduction in semiconductor thickness compared to silicon, while keeping the same blocking voltage. This reduces the on-state conduction losses of the power switch. Higher band-gap energy E_g, thermal conductivity λ and maximum operating temperature T_{MAX} result in an increase of switching device power density and allow for application in harsher environments with higher ambient temperatures [7].

Some drawbacks and limitations of SiC power MOSFETs are production difficulties [7], gate-oxide reliability [8], and lower maximum short-circuit times in comparison with Si power MOSFETs. A detailed analysis of the mentioned problems can be found in [4]. Wafer production and gate-oxide reliability are outside of the scope of this thesis and will not be discussed further.

3 Half bridge design

The goal of the thesis was to design, develop and test a two-level half bridge converter based on SiC semiconductor power MOSFETs. Figure 1 shows the circuit diagram of such a half bridge. The circuit was implemented on a printed circuit board (PCB), which was designed specifically for this application.

In Table 2, the nameplate data of two induction machines (IMs) used in the laboratory of the Electric Drives and Machines Institute is shown. These nameplate values served as reference values for the dimensioning and the design of the half bridge, as they are the intended load for the converter.

-	Machine 1	Machine 2
Nominal Voltage	124 V	400 V
Nominal Current	21.4 A	10.5 A
Nominal Power	3.3 kW	5.5 kW
Frequency	150 Hz	50 Hz
Speed	4265 rpm	2900 rpm

Table 2: Nameplate data of the induction machines

With an overload factor of 2 for Machine 1, the maximum RMS current of the half bridge is set to 42.8 A. Additionally, the blocking voltage of the power MOSFETs was chosen to allow for a safe margin of operation in case of voltage overshoot when supplying Machine 2.

Functional logic operation of the half bridge is presented in Table 3. It is important to note that care must be taken not to have both switches turned-on at the same time, as this will lead to short-circuit of the DC voltage source. This results in destruction of the power switches in an order of a few microseconds according to manufacturer datasheets found in: [9], [10], [11] and [12].

T_1	T_2	V_{OUT}
OFF	OFF	Load Defined[1]
ON	OFF	V_{DC}
OFF	ON	0 V
ON	ON	Short-Circuit

Table 3: Output voltage as a function of switch states

[1]With positive output current the output voltage is 0 V. At negative output current the voltage is V_{DC}. At zero current the load defines the voltage.

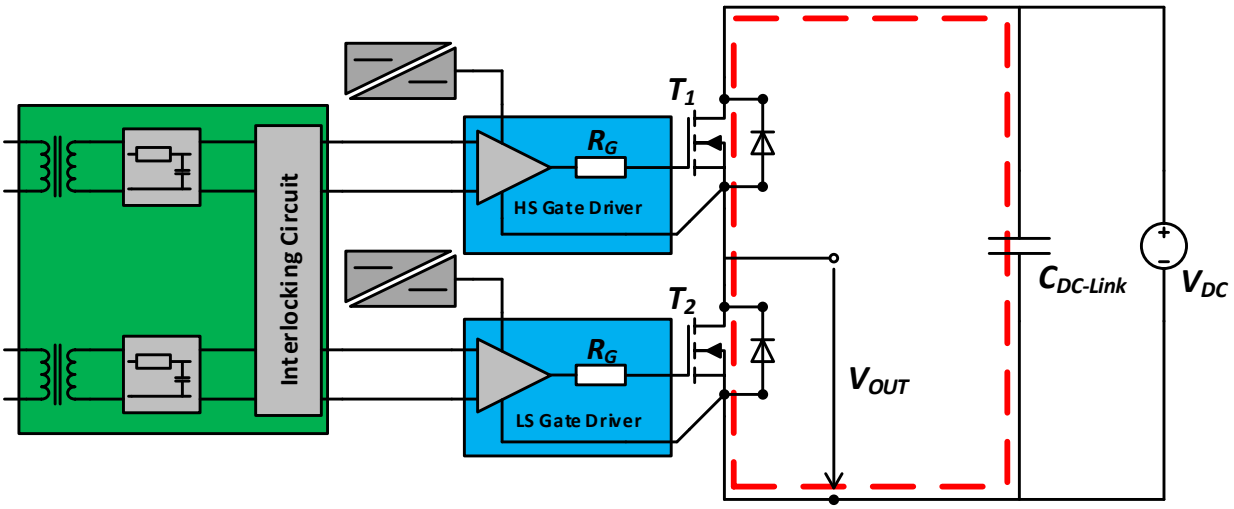

Figure 1: Half bridge circuit diagram with indicated functional blocks

In Table 4, a summary of the design goals for the half bridge is presented. As already mentioned, the design focuses on minimizing the losses of the converter, as well as maximizing the switching frequency f_{SW}, in order to reduce output harmonic content. This reduction in voltage and current harmonics at the half bridge output results in the reduction of the size and weight of the output filter needed for sinusoidal operation.

-	Value
DC-Link Voltage	566 V
Output RMS Current	50 A
Switching Frequency	50 kHz
Total Conversion Efficiency	98 %

Table 4: Design goals for the half bridge

The design process can be split into two parts: component selection and PCB design. A subdivision of the functional parts of the half bridge circuit can be made as follows:

- Signal isolation, filtering, and interlocking circuit (marked in green in Figure 1)
- Gate driver circuit (marked in blue in Figure 1)
- Power/commutation loop (red loop in Figure 1)

In order to prevent the occurrence of high voltages at the signal input of the board, in case of a failure of the circuit or part of the circuit, a signal isolator was used at board input. The signal isolator was chosen with low propagation delay in mind while also being able to provide isolation for four input, and two output channels. A low pass filter was applied to the outputs of the signal isolator. The filtered control

signals were passed through a dedicated interlocking circuit in order to prevent both power switches from being turned on at the same time.

As seen in Table 3, if both power switches are in the ON-state at the same time, a low resistance path from the DC voltage source to ground is present and the switches will be destroyed quickly.

The gate driver circuit consists of the gate driver integrated circuit (IC), with additional passive components, such as current limiting gate resistors and the desaturation circuit which will be discussed in more detail in Paragraphs 3.2 and 4.1.

3.1 Component selection

Selection of the components needed for the implementation of the proposed half bridge is centered around the power MOSFETs and the gate driver integrated circuit (IC). In Table 5, an overview of some commercially available SiC MOSFETs suitable for the proposed application is shown. The electrical device characteristics that are of interest (breakdown voltage V_{DS}, maximum continuous drain current I_D, on-state resistance $R_{DS(ON)}$…) are also presented in the table, along with color coding for an overview of advantages of a specific device model. Parameters are extracted from the manufacturer datasheets: [9], [10], [11] and [12]. After selecting the power MOSFETs suitable for design, a comparison of power losses for the intended application has been made.

When selecting the power MOSFETs for the design, the starting point is the blocking voltage $V_{DS,Max}$ of the MOSFET. The maximum allowable drain current I_D is the second value of interest. These values are dictated by the intended application load of the half bridge. As already stated, a 1200 V blocking voltage was chosen for this application. Maximum drain current is a function of MOSFET case temperature T_C. At 25 °C, the MOSFET from CREE shows an advantage over the other devices. However, at 100 °C both the CREE C3M0016120K and the On Semiconductor NTH4L020N120SC1 show similar results as seen in Table 5. Assuming adequate cooling, both devices are suitable for the design with some safety margin regarding the drain current at a case temperature of 100 °C.

MODEL / PARAMETERS	CREE C3M0016120K		Microsemi MSC025SMA120B		Rohm SCT3022KL		On Semiconductor NTH4L020N120SC1		Unit
	Value	Condition(s)	Value	Condition(s)	Value	Condition(s)	Value	Condition(s)	
-	**Absolute Maximum Ratings**								-
Breakdown Voltage $V_{DS,Max}$	**1200**	V_{GS} = 0 V I_D = 100 µA	**1200**	V_{GS} = 0 V I_D = 100 µA	**1200**	V_{GS} = 0 V I_D = 1 mA	**1200**	T_J = 25°C	V
Continuous Drain Current I_D	**115**	V_{GS} = 15 V, T_C = 25˚C	**103**	T_C = 25˚C	**95**	T_C = 25˚C	**102**	T_C = 25˚C	A
	85	V_{GS} = 15 V, T_C = 100˚C	**73**	T_C = 100˚C	**67**	T_C = 100˚C	**84**	T_C = 100˚C	
Gate-Source Voltage V_{GS}	**-8 / 19**	f > 1 Hz	**-10 / 23**	-	**-4 / 22**	-	**-15 / 25**	T_J = 25°C	V
-	**Electrical Characteristics at Operating Point**								
Drain-Source On-State Resistance $R_{DS(ON)}$	**17**	V_{GS} = 15 V, I_D = 75 A, T_J = 25˚C	**25**	V_{GS} = 15 V, I_D = 40 A, T_J = 25˚C	**24**	V_{GS} = 18 V, I_D = 63 A, T_J = 25°C	**29**	V_{GS} = 20 V, I_D = 60 A, T_J = 25°C	mΩ
	32	V_{GS} = 15 V, I_D = 75 A, T_J = 175˚C	**36**	V_{GS} = 15 V, I_D = 75 A, T_J = 175˚C	**42**	V_{GS} = 18 V, I_D = 63 A, T_J = 175°C	**40**	V_{GS} = 20 V, I_D = 60 A, T_J = 175°C	
Gate Threshold Voltage $V_{GS(th)}$	**3**	V_{DS} = V_{GS}, I_D = 23 mA	**2.8**	V_{DS} = V_{GS}, I_D = 3 mA	**2.7-5.6**	V_{DS} = 10 V, I_D = 18.2 mA	**2.7**	V_{DS} = V_{GS}, I_D = 20 mA	V
	2	V_{DS} = V, I_D = 23 mA, T_J = 175˚C		V_{DS} = V_{GS}, I_D = 3 mA		V_{DS} = 10 V, I_D = 18.2 mA		V_{DS} = V_{GS}, I_D = 20 mA	
Input Capacitance C_{ISS}	**6100**	V_{GS} = 0 V, V_{DS} = 1000 V, f = 1 MHz, V_{AC} = 25 mV	**3200**	V_{GS} = 0 V, V_{DD} = 1000 V, f = 1 MHz, V_{AC} = 25 mV	**3000**	V_{GS} = 0 V, V_{DS} = 800 V, f = 1 MHz	**2900**	V_{GS} = 0 V, V_{DS} = 800 V, f = 1 MHz	pF
Output Capacitance C_{OSS}	**350**		**400**		**200**		**350**		
Total Gate Charge Q_g	**211**	V_{DS} = 800 V, I_D = 75 A	**232**	V_{DD} = 800 V, I_D = 40 A	**178**	V_{DD} = 600 V, I_D = 36 A	**220**	V_{DS} = 600 V, I_D = 80 A	nC
Turn-On Switching Energy E_{ON}	**1.15**	**V_{DS}=600V,V_{GS}=-4V/+15V, I_D=75A,$R_{G(ext)}$ = 2.5Ω, L= 65.7 µH, T_J=175˚C (Body Diode as freewheeling Diode)**	**-**	-	**2.10**	**V_{DD}=600 V, V_{GS}=18V/0V, T_A = 25˚C, R_G=0Ω, L=250 mH**	**-**	-	mJ
Turn-Off Switching Energy E_{OFF}	**0.38**		**-**		**0.95**		**-**		mJ
Package Type	TO-247-4		TO-247		TO-247		TO-247-4		-

Table 5: Comparison of significant electrical parameters for SiC power MOSFETs of interest

Keeping the blocking voltage and allowable drain current values in mind, the next step of MOSFET selection is to optimize the design for higher switching frequencies or to choose a specific switching frequency f_{SW} for which the device power losses should be minimized. This thesis presents the design process for a fixed switching frequency of 50 kHz. Conversion efficiency at a given frequency can be derived from the load power and total switching device losses. Power MOSFET losses can be obtained as a sum of conduction and switching losses as shown in Equation (1). The application note [13] from Infineon provides a detailed overview of MOSFET power loss calculation using MOSFET datasheet parameters.

$$P_{Loss} = P_{Cond} + P_{SW} \tag{1}$$

Estimation of conduction losses P_{Cond} is relatively straightforward. At a given drain current I_D and junction temperature T_J, conduction losses can be calculated as in Equation (2). D represents the duty cycle.

$$P_{Cond} = E_{Cond} \cdot f_{SW} = \int_0^{t_{ON}} i_D^2(t) \cdot R_{DS(ON)}(T_J)\, dt \cdot f_{SW} = I_D^2 \cdot R_{DS(ON)} \cdot D \tag{2}$$

Switching losses on the other hand are more challenging to estimate from the device datasheet. It is also much more difficult to measure the switching losses experimentally due to fast rise and fall times of drain current and drain source voltage. Equation (3) gives an approximate formulation for the upper bound of switching losses for a power MOSFET, when the body diode losses are disregarded.

$$P_{SW} = (E_{ON} + E_{OFF}) \cdot f_{SW} \tag{3}$$

E_{ON} and E_{OFF} are defined as follows (Equation (4) and Equation (5) respectively):

$$E_{ON} = \int_0^{t_{ri}+t_{fu}} v_{DS}(t) \cdot i_D(t)\, dt = V_{DC} \cdot I_D \cdot \frac{t_{ri} + t_{fu}}{2} + Q_{rr} \cdot V_{DC} \tag{4}$$

$$E_{OFF} = \int_0^{t_{ru}+t_{fi}} v_{DS}(t) \cdot i_D(t)\, dt = V_{DC} \cdot I_D \cdot \frac{(t_{ru} + t_{fi})}{2} \tag{5}$$

Reverse recovery charge Q_{rr}, current rise time t_{ri} and current fall time t_{fi} can be found in the datasheets of the power MOSFETs. Voltage rise and fall times t_{ru} and t_{fu} can be approximated from

the gate-drain capacitance C_{GD}charging times. As already stated, the power MOSFET capacitances exhibit nonlinearity as they are voltage depended. However, a two-point approximation is still useful as a first approximation. An overview of the full loss estimation procedure can be found in [13].

Under the assumption of a 50% duty cycle and DC-Link voltage equal to the peak value of machine nameplate line to line voltage at a fixed switching frequency of 50 kHz and for varying drain current $I_D \in [0.5,\ 2.0] \cdot \sqrt{2} \cdot I_N$, the switching losses for the four MOSFETs from Table 5 can be calculated using Equations (1) – (5). I_N represents the induction machine nameplate RMS current. For calculation of the losses, the recommended static gate-source voltage was used for each MOSFET. These values can be found in the device datasheets. The junction temperature T_J was assumed to be 25 °C.

The following figures represent an upper bound estimation of MOSFET losses calculated in MATLAB.

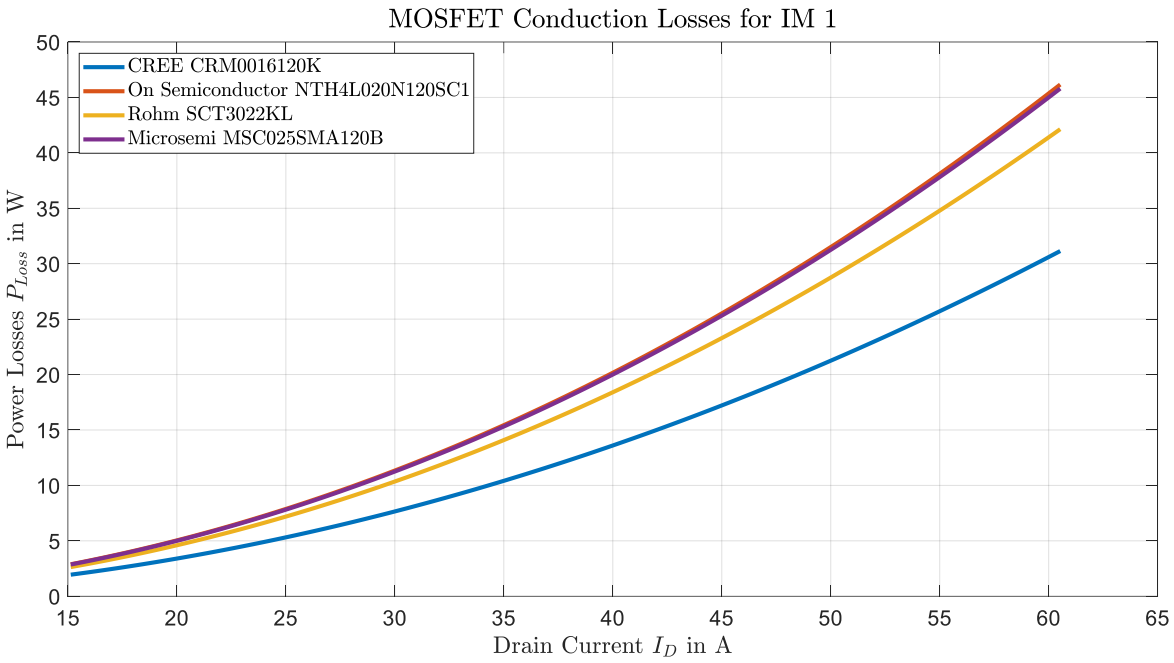

Figure 2: Calculated MOSFET conduction losses for IM 1 (Table 2)

Figure 2 shows the comparison of conduction losses for MOSFETs in Table 7. Nameplate current of Induction Machine 1 from Table 2 was taken as reference. As is expected, the losses rise with the square of the drain current. Low on-state resistance of the CREE C3M0016120K results in lower conduction losses when compared with other MOSFETs.

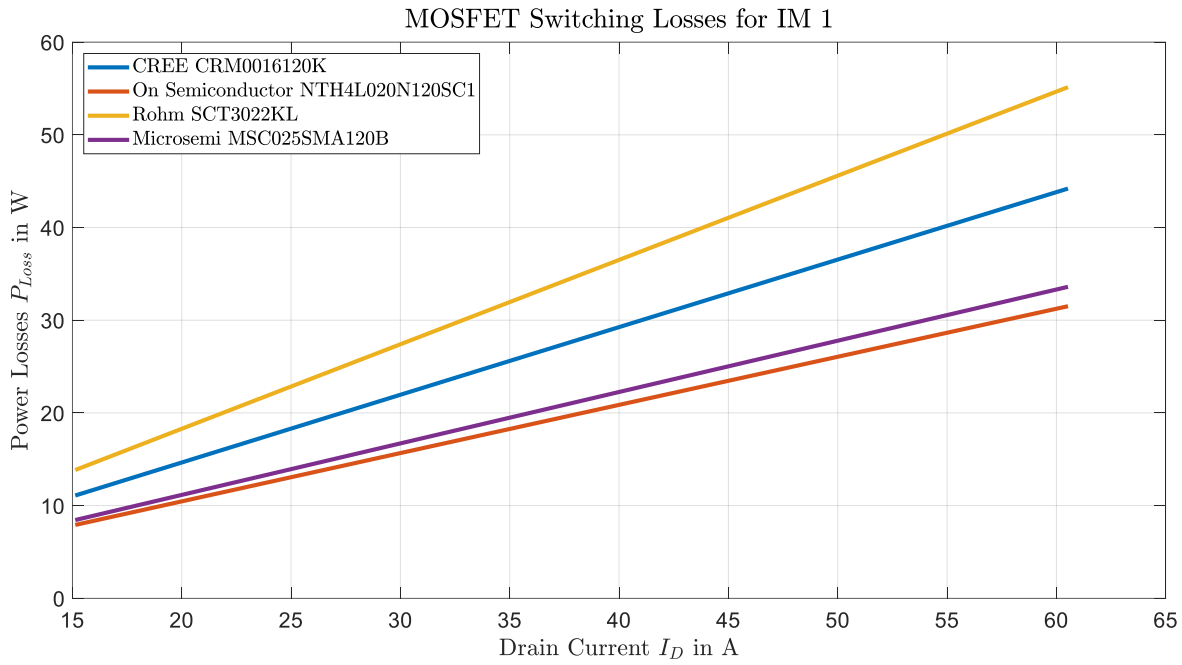

Figure 3: Calculated MOSFET switching losses for IM 1 (Table 2)

Comparison of MOSFET switching losses is shown in Figure 3. A linear rise in switching losses can be observed with the rise in drain current. High values of gate-drain capacitance C_{GD}, result in higher switching losses which can be seen for the CREE and Rohm MOSFETs.

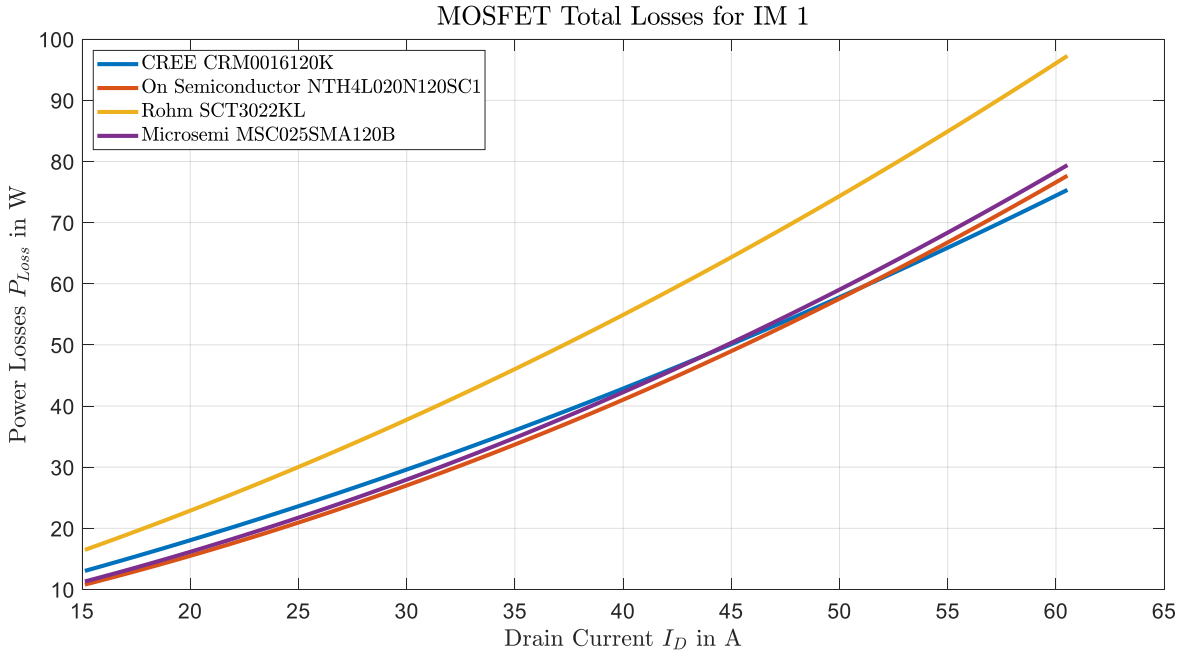

Figure 4: Calculated total MOSFET losses for IM 1 (Table 2)

In Figure 4, the sum of conduction and switching losses for IM 1 is shown. Although the results are similar for all four MOSFETs, the Rohm SCT3022KL exhibits significantly higher losses, especially noticeable at higher drain currents.

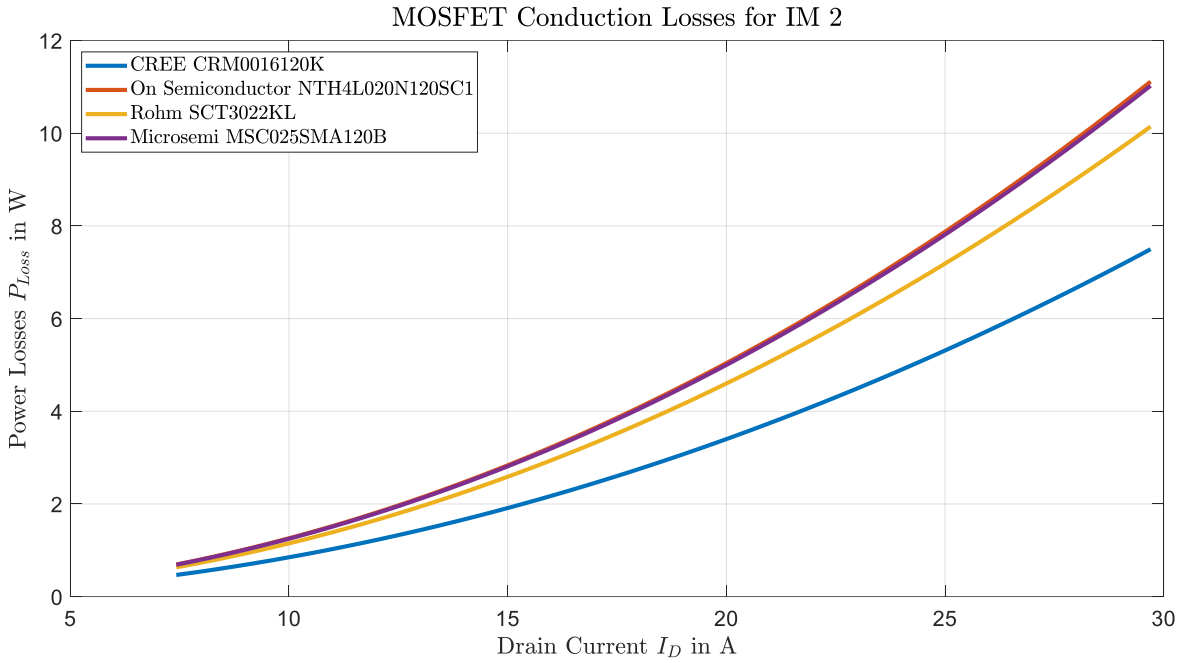

Figure 5: Calculated MOSFET conduction losses for IM 2 (Table 2)

For Induction Machine 2 (Table 2), the conduction losses as a function of drain current are shown in Figure 5. As for Induction Machine 1, the CREE power MOSFET shows a clear advantage due to its lower on-state resistance. It is also important to note that the datasheet values for drain-source on-state resistance of MOSFETs show a mean value across multiple production samples. Keeping that in mind, the actual resistance values, and in turn power losses might differ for different device samples.

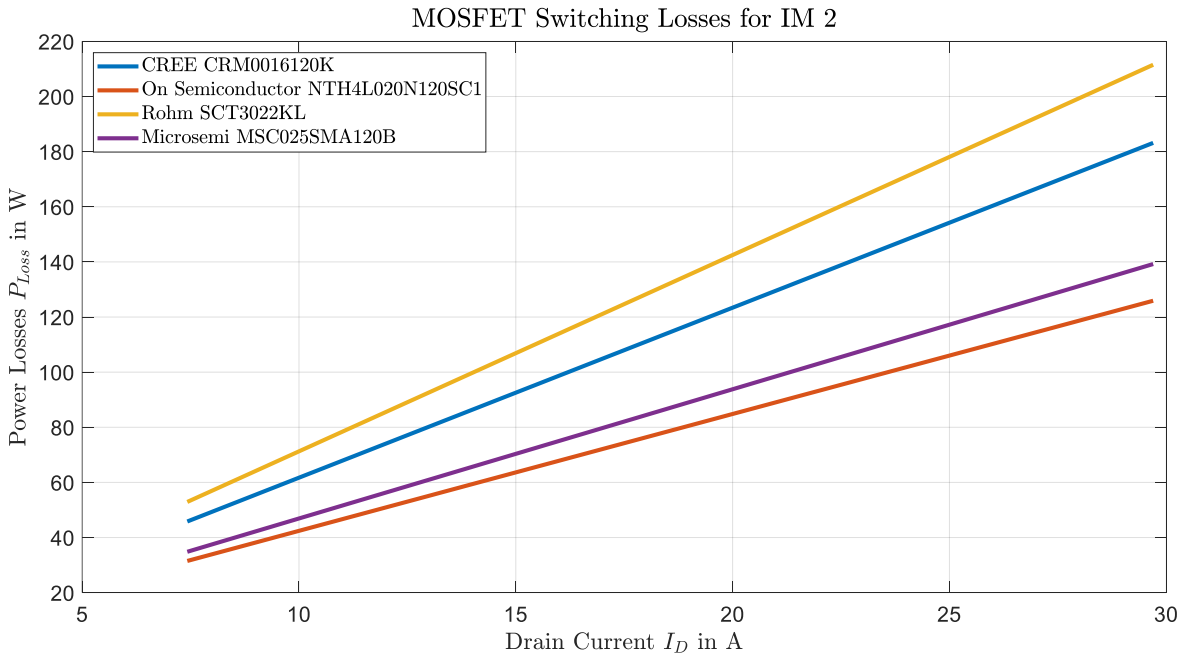

Figure 6: Calculated MOSFET switching losses for IM 2 (Table 2)

Figure 6 shows the switching losses for currents expected when supplying Induction Machine 2. Again, the results are comparable to results for Induction Machine 1.

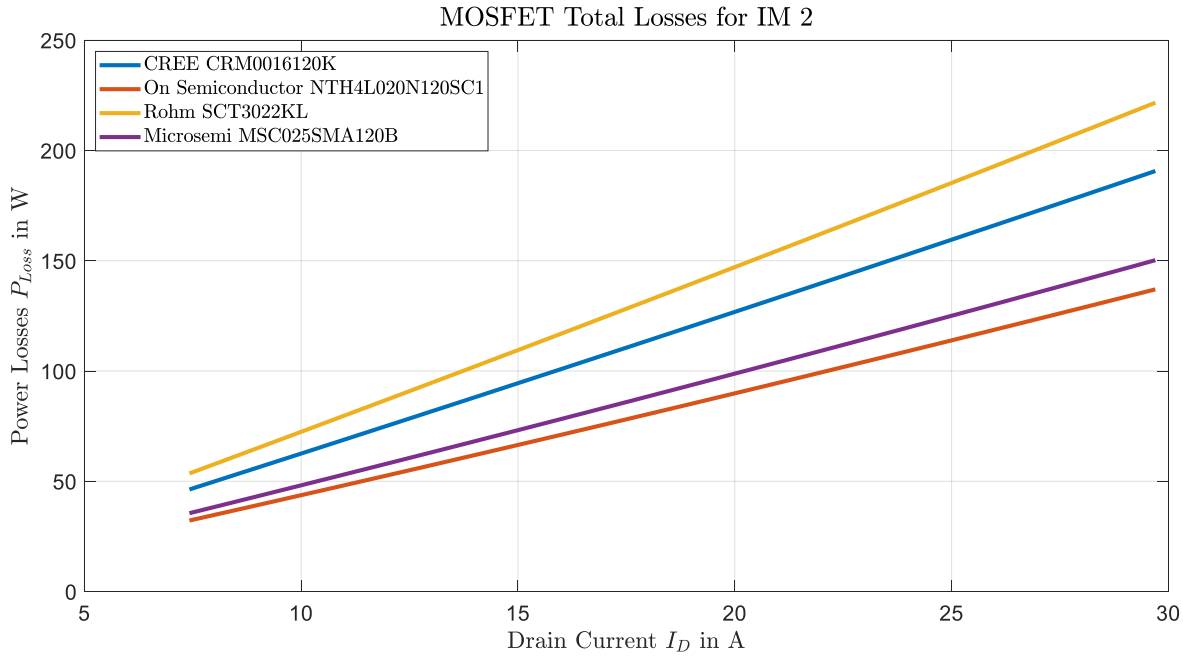

Figure 7: Calculated total MOSFET losses for IM 2 (Table 2)

Figure 7 shows the calculated total losses for varying drain current when Induction Machine 2 is taken as a reference. It can be seen that at drain currents over 25 A the power dissipation of the Rohm and CREE MOSFETs is close to the allowable power dissipation of the device. A drain current of 25 A corresponds to an overload factor of 1.7 for IM 2.

The results in previous figures show a rough upper bound estimate of total MOSFET losses with varying drain current at a fixed switching frequency. Although the results show similar behavior for all four devices, a clear distinction between conduction and switching losses can be made. It is also important to note that, at low voltages, the high gate-drain capacitance C_{GD} results in an increase of the switching power losses.

Based on the presented results in this chapter and the availability at time of ordering, the On Semiconductor NTH4L020N120SC1 was chosen. It is also important to note that the T0-247-4 package provides an additional source pin which reduces gate loop inductance and allows for faster switching.

The next step of the design process was the selection of the appropriate gate driver IC for the intended application, and the previously chosen power MOSFET. The electrical characteristics of the gate driver ICs that were considered for the half bridge are shown in Table 8. Necessary prerequisites for the design were the ability to provide negative voltage for SiC MOSFET turn-off, high isolation voltage, low propagation delay and high common mode transient immunity (CMT).

MODEL / PARAMETER	Analog Devices ADuM4135	Texas Instruments UCC5870-Q1	Infineon 1ED3124MC12H	Unit
-	Electrical Characteristics			-
Power Supply Output - High Side V_{CC2}	30	30	35	V
Power Supply Output – Low Side V_{EE2}	-15	-12	0	V
Peak Output Source Current $I_{OUT,MAX}$	4.61	15	13.5	A
Peak Output Sink Current $I_{IN,MAX}$	5	15	14	A
Dielectric Insulation Voltage	5000	3750	5700	V
Propagation delay, typical	55	150	270	ns
Common Mode Transient Immunity $\|CM\|$	100	100	200	kV/µs
DESAT Overcurrent Protection	YES	YES	NO	-

Table 6: Comparison of significant electrical parameters for gate driver ICs of interest

Based on the data provided in Table 6, selection of the gate driver IC could be made. Firstly, maximum and minimum voltage levels were compared to the recommended gate turn-on and turn-off voltages of the selected power MOSFET. The Infineon 1ED3124MC12H does not support negative supply voltages and so additional external circuitry would be needed in order to utilize the potential of the power MOSFET. Next, the maximum sink and source currents of the gate driver ICs were compared. Although the ADuM4135 gate driver IC from Analog Devices has significantly lower current limits, the additional gate resistor R_G that would be used to limit gate current mitigates any potential advantages that higher gate currents might provide. Common mode transient immunity (CMTI) was compared to the expected drain-source voltage rates $\frac{dv_{DS}}{dt}$. As the expected rate of change for the drain-source voltage was in the order of 20 kV/µs to 30 kV/µs, all three gate drivers could be considered. The dielectric insulation strength, expressed as the dielectric insulation voltage in Table 6 was also well over any voltage expected at the power side of the board during operation. Finally, the built-in desaturation protection and lowest propagation delay of the ADuM4135 made it the most viable choice for the half bridge design.

As already stated, the design focuses on reducing the inductance of the power loop by reducing the loop area. However, this area constraint reduces the amount of DC-Link capacitance that can be fitted on the PCB. The tradeoff influences the stability of the DC-Link voltage – excessive voltage sag and voltage oscillation might occur during switching. A combination of electrolytic and ceramic capacitors was used for the proposed half bridge configuration to reduce DC-Link voltage ripple. A detailed overview of capacitor electrical properties is shown in Table 7.

During initial testing, the influence of the ceramic DC-Link capacitors on device switching behavior was assessed. No significant improvement of DC-Link voltage stability was noticed when comparing measurement results with one and two CeraLink ceramic capacitors. Therefore, instead of the proposed four parallel capacitors, only two CeraLink B58035U7155M062 ceramic capacitors were placed in parallel at the half bridge DC-Link as close as possible to the switching devices. This was done in order to minimize switching loop inductance. Two electrolytic Nichicon UCP2W101MHD capacitors in series were also added in parallel to the ceramic capacitors. At an operating voltage of 600 V, the total DC-Link capacitance is 53 µF.

MODEL / PARAMETER	TDK CeraLink B58035U7155M062		Nichicon UCP2W101MHD		Unit
-	Value	Condition(s)	Value	Condition(s)	-
Type	**Ceramic**	-	**Electrolytic**	-	-
Rated Voltage V_R	**700**		**400-450**	-	V
Nominal Capacitance C_{nom}	**1.5**	V = 600 V	**100**	-	µF
Maximal Dissipation Factor $\tan(\delta)$	**0.02**	-	**0.24**	f = 120 Hz	-
Equivalent Series Resistance ESR	**2**	T = 75°C, V = 200 V, f = 50 kHz	**3.18**[2]	f = 120 Hz-	Ω

Table 7: Electrical properties of DC-Link capacitors

In Table 8 the most significant additional components are shown. The signal isolator has four input channels for differential gate driver control signals and two output channels used for status and fault reporting. Low typical propagation delay of 7.2 ns was the determining factor in device selection [14].

Application	Manufacturer	Component
Signal isolator	Analog Devices	ADuM262N
Single-output Isolated DC-DC power supply	Murata	MEJ20505SC
Dual-output isolated DC-DC power supply	RECOM	R05P22005D

Table 8: List of additional significant components

The isolated DC-DC converters were used in order to provide stable DC supply voltage to isolated parts of the board. RECOM R05P22005D was the only power supply that provided 20 V / -5 V dual rail output at 2 Watts of maximum output power.

[2] Not available in device datasheet, extracted from $\tan(\delta)$

3.2 Printed Circuit Board design

The printed circuit board (PCB) was designed using KiCad 5.1.6.Based on considerations from previous chapters, the KiCad schematic in Figure 8 was developed. From left to right the following subcircuits are included:

- Signal isolation and filtering
- Power supply
- Interlocking circuit
- Low side and high side gate driver circuit

Inputs to the board are four control signals for the low side and high side gate control. In the schematic they are labeled as “VI+_HS_IN”, “VI-_HS_IN”, “VI+_LS_IN” and “VI-_LS_IN”. Status and fault reporting is done over “RDY_IN” and “FLT_IN” signals respectively. Additionally, the board is supplied with 5 Volts via a standard 2 pin terminal labeled as “J1” in the schematic.

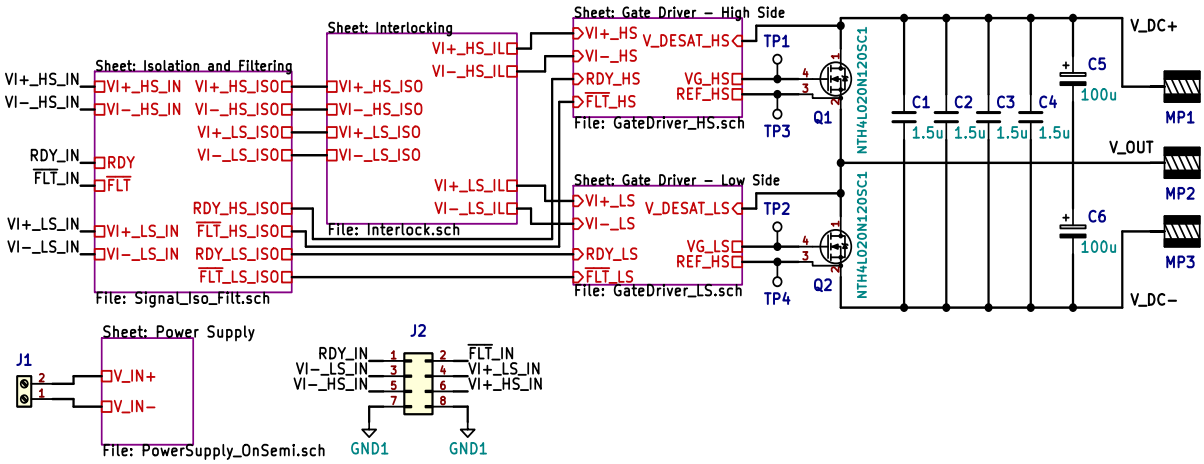

Figure 8: Full KiCad schematic with labeled subcircuits

Figure 9 shows the control signal isolation circuit. 5 kΩ pull-up resistors are used for the “RDY_HS_ISO”, “RDY_LS_ISO”, “FLT_HS_ISO” and “FLT_LS_ISO” signals to improve reliability. Also, status LEDs are available for indication of the gate driver ready and gate driver fault state. The gate driver status signals are combined into one signal before the signal isolator. This was done in order to reduce the number of isolation channels needed.

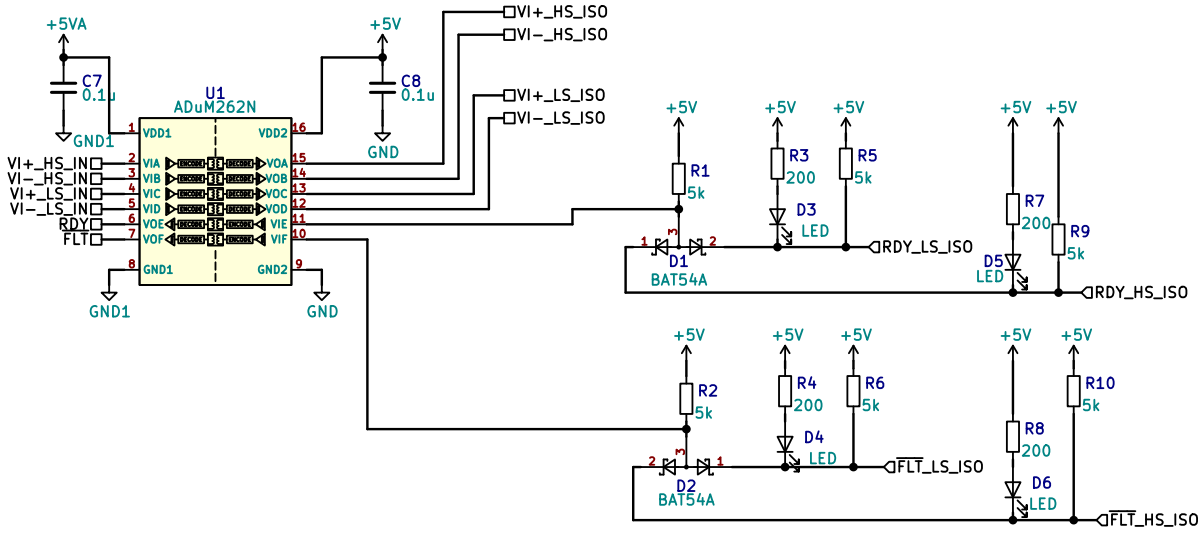

Figure 9: Signal isolation KiCad subcircuit with status LEDs

Shown in Figure 10, is the interlocking circuit with a low-pass RC filter at the input. The idea behind the interlocking circuit is to prevent a control state, where both the high side and low side gate drivers have an on-state command at the same time. This is achieved by delaying the turn-on signal of both the upper and lower gate driver and by forcing the active-low signal to the low state as soon as an active-high signal is present at the opposite gate driver signal.

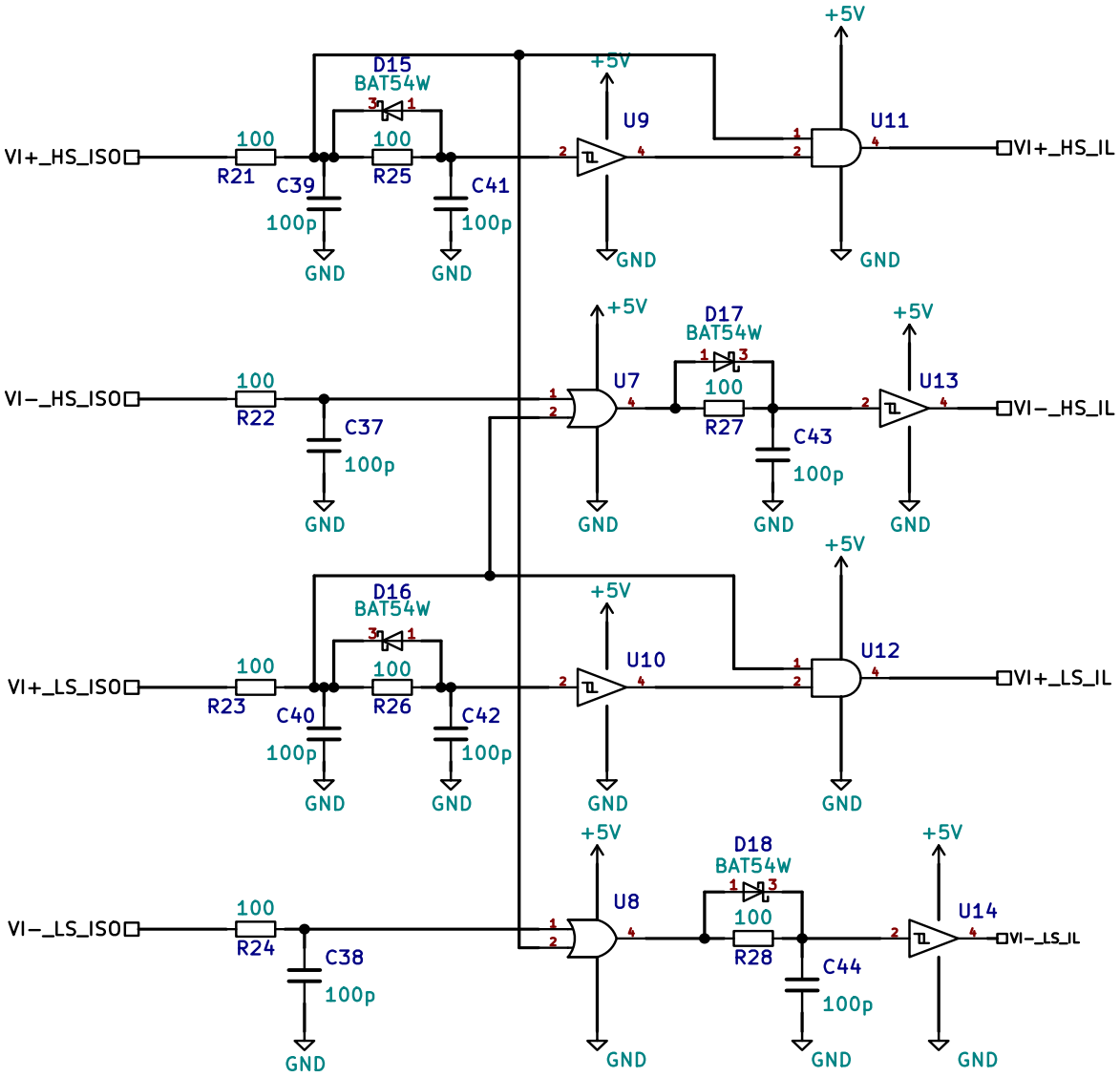

Figure 10: Signal filtering and interlocking KiCad schematic

In Figure 11, the high side gate driver circuit is shown. The low side gate driver circuit is equivalent, and the circuit schematic is omitted from this thesis.

The gate circuit provides separate sink and source paths for charging and discharging MOSFET input capacitance C_{ISS}. Both the charge path and the discharge path have a current limiting resistor of 10 Ω. A gate sense pin together with a miller clamp is also available for robustness. This provides a low impedance path to the gate pin of the MOSFET and in turn prevents self-turn on during switching operations. Built in desaturation protection is also available on the ADuM4135 gate driver utilized in the circuit according to datasheet recommendations.

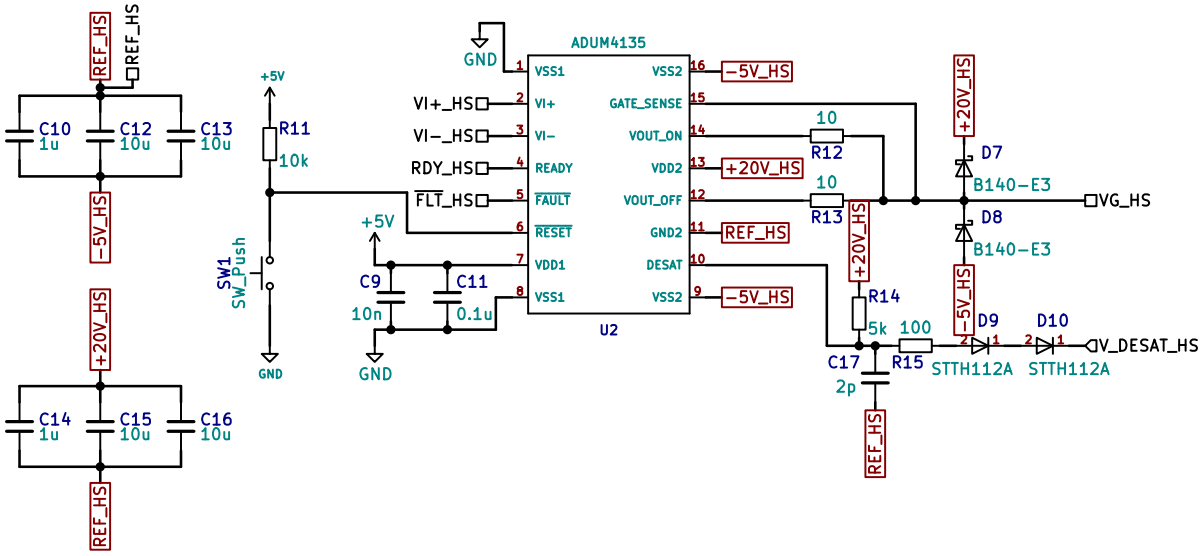

Figure 11: High side gate driver KiCad schematic

During testing, failure of the desaturation protection circuit was observed although the circuit was based on the device datasheet [14] recommendations. Additional information on DESAT circuit design could be found in the application note of the manufacturer [15]. The exact failure mechanism could not be determined or reproduced. However, the problem was mitigated using additional components as shown in Figure 12 and in Table 9 in red. The idea behind the Extended structure shown in Figure 12 was found in [15].

Component	Basic structure	Extended structure
R_{PU}	5 kΩ	15 kΩ
C_{BLK}	12 pF	18 pF
R_{DESAT}	24 kΩ	8.2 kΩ
D_1	STTH112A	STTH112A
D_2	STTH112A	STTH112A
R_{PD}	-	24 kΩ
D_3	-	BAS170
D_4	-	BAS170

Table 9: Desaturation circuit passive components

The DESAT pin of the gate driver monitors the MOSFET drain-source voltage v_{DS} during the on state. As soon as the voltage at the DESAT pin V_{DESAT} of the gate driver reaches a set value of 9 V, soft shutdown is initiated.

$$V_{DESAT} = I_{DESAT} \cdot R_{DESAT} + V_{D1}(I_{DESAT}) + V_{D2}(I_{DESAT}) + V_{DS}(I_D, T_J) \tag{6}$$

$$I_{DESAT} = I_{CHG} + \frac{V_{DD2} - V_{DESAT}}{R_{PU}} - \frac{V_{DESAT}}{R_{PD}} \tag{7}$$

Rearranging Equation (6) and Equation (7) under the assumption that the MOSFET junction temperature is constant, and that voltage drop across diodes $D_3$and D_4 is equal we arrive at:

$$V_{DESAT} = \frac{R_{DESAT} \cdot \left(I_{CHG} + \frac{V_{DD2}}{R_{PU}}\right) + 2 \cdot V_D(I_{DESAT}) + I_D \cdot R_{DS(ON)}(T_J)}{R_{DESAT} \cdot \frac{R_{PD} + R_{PU}}{R_{PD} \cdot R_{PU}} + 1} \tag{8}$$

I_{CHG} is the current supplied by the gate driver IC and can be found in the driver datasheet. $V_D(I_{DESAT})$ is the voltage drop across the blocking diodes and is assumed to be 0.3 V for this application. Circuit component values R_{DESAT}, R_{PD}, R_{PU} from Equation (8) can be found in Table 9.

For testing, we can assume that the junction temperature of the MOSFET is approximately equal to the room temperature. Therefore, we can assume that the drain source resistance is 28 mΩ, as per manufacturer datasheet. Evaluating Equation (8) with all the known parameters, we arrive at a

maximum allowable drain current of approximately 60 A. This value is suitable for supplying the Induction Machines from Table 2 under overload conditions (up to a factor of two for IM 1).

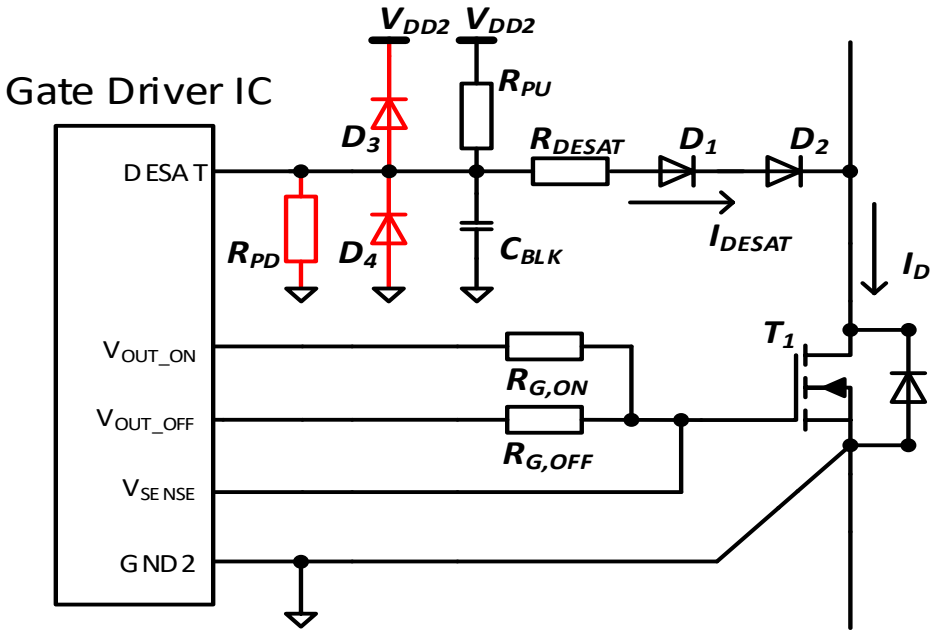

Figure 12: Gate driver circuit with additional passive components marked in red (based on [15])

It is also important to estimate the total blanking time t_{BLK} provided by the internal gate driver delay $t_{BLK,INT}$ and the blanking time caused by blanking capacitor C_{BLK} charging. This blanking time prevents the operation of the desaturation circuit from triggering a device shutdown during transitions from the off-state to the on-state. An approximation of the total blanking time is shown in Equation (9).

$$t_{BLK} = t_{BLK,INT} + t_{BLK,CAP} = t_{BLK,INT} + \frac{V_{DESAT} \cdot C_{BLK}}{I_{CHG} + \frac{V_{TH} - V_{DESAT}}{R_{TH}}} = 485\ ns \tag{9}$$

V_{TH} and R_{TH} are the parameters of the equivalent voltage source formed by the pull-up R_{PU} and pull-down R_{PD} resistance. They are defined as follows:

$$V_{TH} = V_{DD2} \cdot \frac{R_{PD}}{R_{PU} + R_{PD}} \tag{10}$$

$$R_{TH} = \frac{R_{PU} \cdot R_{PD}}{R_{PU} + R_{PD}} \tag{11}$$

After calculating the necessary component values and the circuit schematic is finished, a printed circuit board was designed. Some values of interest for the PCB chosen for this design can be found in Table 10.

Length	150 mm
Width	65 mm
Copper Thickness	35 µm
Number of Layers	4
Isolation Thickness	2x78 µm[3]
Electric Strength	48 kV/mm
Isolation Material	FR4

Table 10: PCB dimensions and properties

In Figure 13, Figure 15, Figure 14 and Figure 16 PCB copper layers are shown. Standard practice was applied, in which the signal layers are on top and bottom of the board, respectively. Power and ground traces and copper pours are the two inside layers. This has proven to be helpful when trying to mitigate EMI and cross talk on the board.

This layer scheme was not applied for the power loop in order to reduce trance length and double the conduction layers where possible. The benefits of having multiple layers available for power traces are lower resistance, inductance and in turn lower power losses.

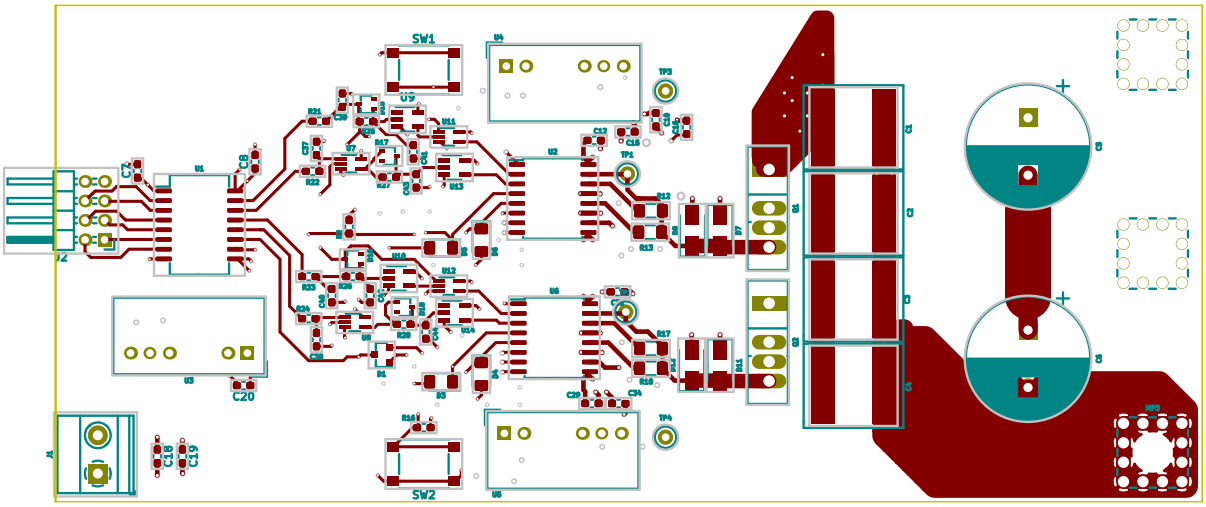

Figure 13: PCB top layer with component outlines

[3] Manufacturer claim for isolation between the external and internal layers.

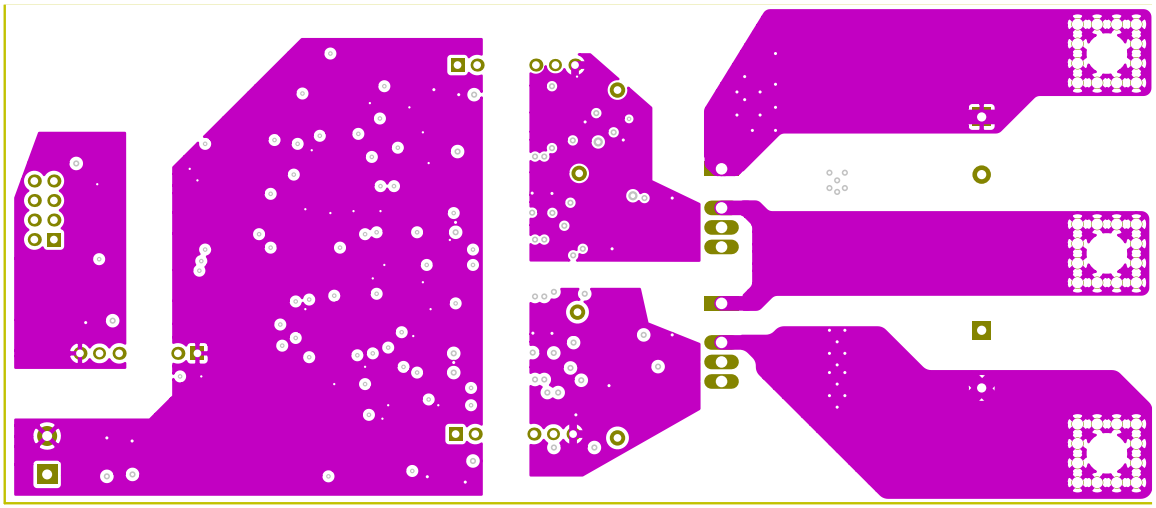

Figure 15: PCB power layer

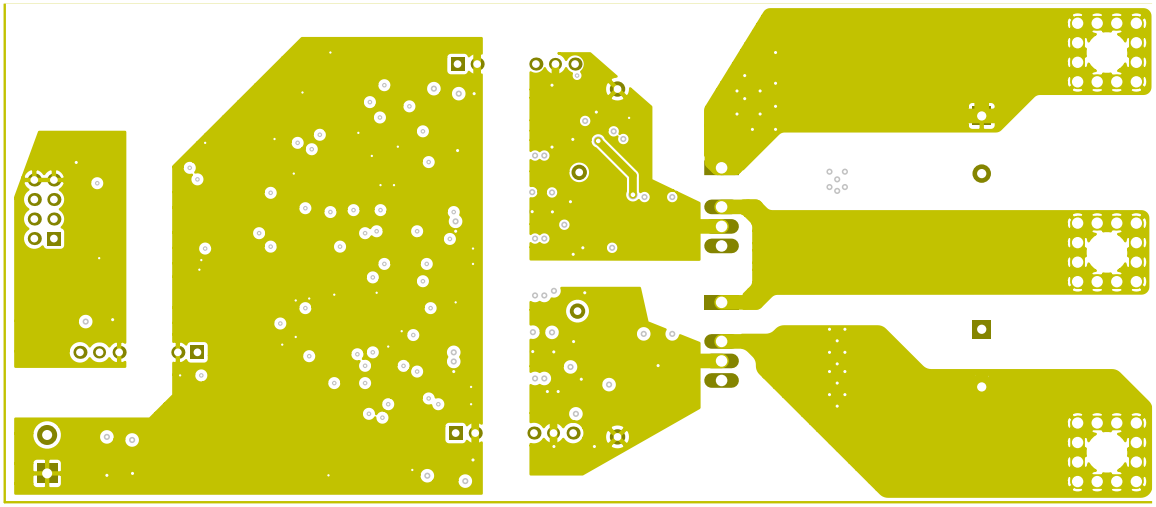

Figure 14: PCB ground layer

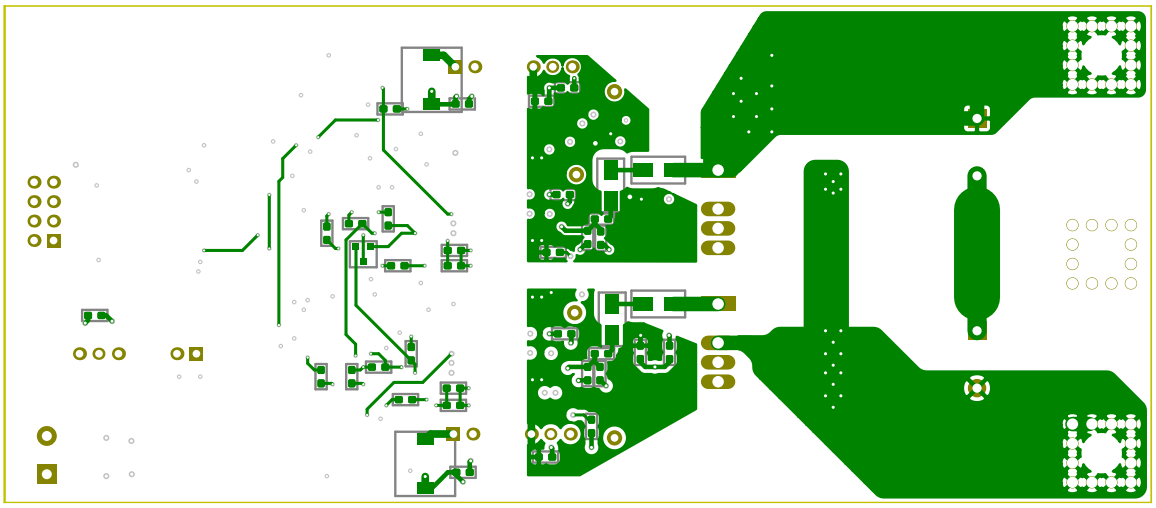

Figure 16: PCB bottom layer

3.3 PCB and component parasitics

The power loop of the half bridge consists of the power MOSFETs and the DC-Link capacitors. This is the most crucial part of the design for high switching frequencies and fast switching. Minimizing the power loop inductance reduces the drain-source voltage V_{DS} overshoot, as well as the ringing of the drain-source voltage V_{DS} and the drain current I_D [16]. Reduction of the power loop inductance also decreases the switching losses of the half bridge due to the lower energy that needs to be dissipated in the MOSFET during turn-off.

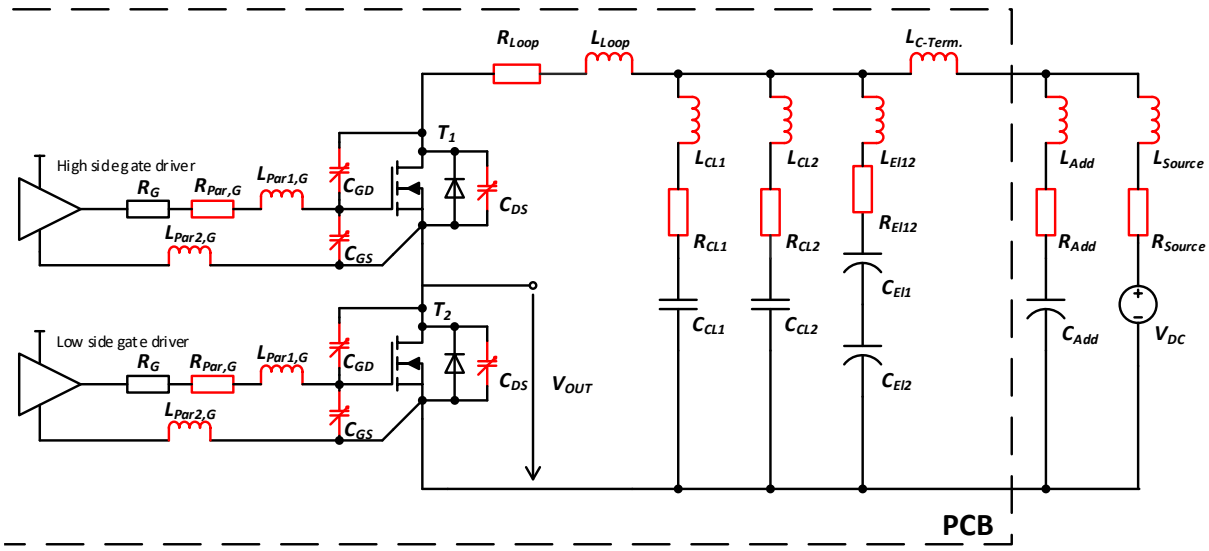

Figure 17: Power loop and gate driver loops with board and component parasitics marked in red

Figure 17 shows the power loop of the half bridge, along with the gate drive circuits. Parasitic resistances and inductances are shown in red. $R_{Par,G}$ represents the sum of the output resistance of the gate driver, copper-trace resistance, and the internal gate resistance of the power MOSFET. $L_{Par1,G}$ represents the parasitic inductance of the copper trace between the gate driver and the gate pin of the MOSFET. $L_{Par2,G}$ represents the inductance of the return path of this signal, along with the inherent inductances of the MOSFET. These values can be partially determined from device datasheets and measurements.

R_{Loop} and L_{Loop} are the PCB trace resistance and inductance, respectively. The value of L_{Loop} contributes significantly to the switching behavior, overvoltage and ringing. The PCB design focused on reducing the commutation loop area in order to reduce the parasitic inductance. In Equation (10) the power loop voltage equation is shown, assuming the CeraLink capacitors C_{CL1} and C_{CL2} are at DC-Link voltage and can provide enough charge for the switching transient.

$$(\sum L) \cdot \frac{di_L}{dt} = \left(L_{Loop} + L_{CL}\right) \cdot \frac{di_L}{dt} = v_{DC}(t) - v_{DS}(t) \tag{12}$$

It can be seen that the only parameter which can be influenced by the PCB design is L_{Loop}. This equation also allows for approximation of power loop inductance with the help of MOSFET drain current measurement, MOSFET drain-source voltage measurement and DC-Link voltage measurement during turn-off. This is also shown in Equation (11).

$$L_{Loop} \approx \frac{v_{DC}(t) - v_{DS}(t)}{\frac{\Delta i_L}{\Delta t}} - L_{CL} \tag{13}$$

C_{DS}, C_{GS} and C_{GD} are the internal power MOSFET capacitances. In Figure 17 they are represented as variable capacitances, as their value depends on the applied voltage. MOSFET capacitances cannot be influenced by a change in topology or PCB design. They are inherent properties of the geometry and materials of the power switch. The values can be found in MOSFET datasheets.

The DC-Link capacitors labeled as C_{CLi} and C_{Eli} also have internal parasitic resistances and inductances. They are labeled as R_{CLi}, L_{CLi}, R_{El12} and L_{El12}.

4 Testing and measurement results

The testing was done at the Power Electronics Laboratory at the Electric Drives and Machines Institute, Graz University of Technology. Testing can be split into functional testing of the control signals and power testing using the Double Pulse Test (DPT) to characterize MOSFET switching behavior.

An overview of the measurement equipment can be found in Table 11. Post-processing and data visualization was done in MATLAB.

Device	Manufacturer	Model	Description
Oscilloscope 1	LeCroy	WaveRunner 8000HD	2 GHz, 2 GS/s
Oscilloscope 2	LeCroy	WaveRunner 625Zi	2 GHz, 2 GS/s
Passive Voltage Probe	LeCroy	PP005	500 MHz-
Isolated Voltage Probe	LeCroy	HVF0108	150 MHz
HV Differential Voltage Probe	LeCroy	HVD3106A	1 kV, 120 MHz
Current Probe	LeCroy	CP031A	30 A, 100 MHz
Current Probe	LeCroy	CP150	150A, 20 MHz
Rogowski Coil with Amplification	EAM	-	-

Table 11: Measurement equipment used during testing

4.1 Functional testing of isolation, interlocking and desaturation protection

The first step of testing was to validate the signal isolation and interlocking of the device. Propagation delay was also measured and compared to the datasheet claims. The signals are labeled with “HS+”, for the positive signal of the high side gate driver, “HS-“ for the negative signal of the high side gate driver, “LS+” for the positive signal of the low side gate driver and “LS-“ for the negative side gate driver.

Figure 18 shows the measured voltages of the positive signal for the high side gate driver during the turn on transient. The measured delay between the 50% signal values is about 17 ns which corresponds to the upper limit of the claimed datasheet values. For this application, the result is more than suitable.

Equivalently, Figure 19 shows the measured voltage of the negative signal for the high side gate driver. Propagation delay is equivalent to the value for the positive signal. The signals were measured using the passive probe and Oscilloscope 2 from Table 11.

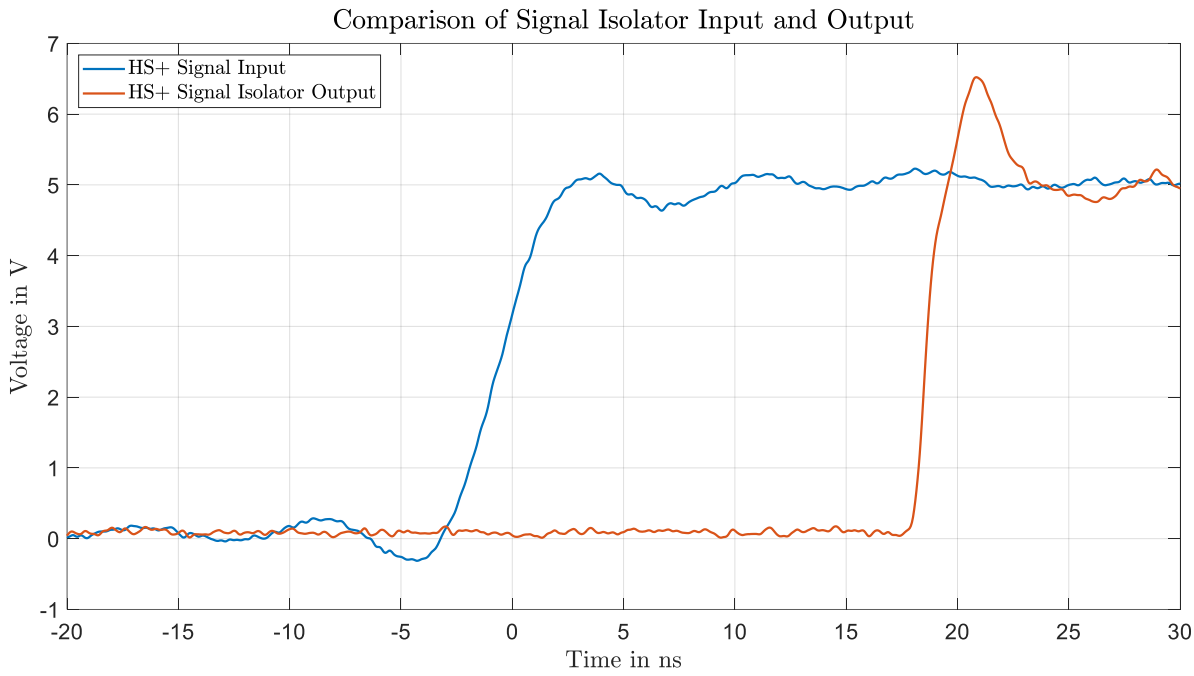

Figure 18: Signal Isolator propagation delay for positive high side channel

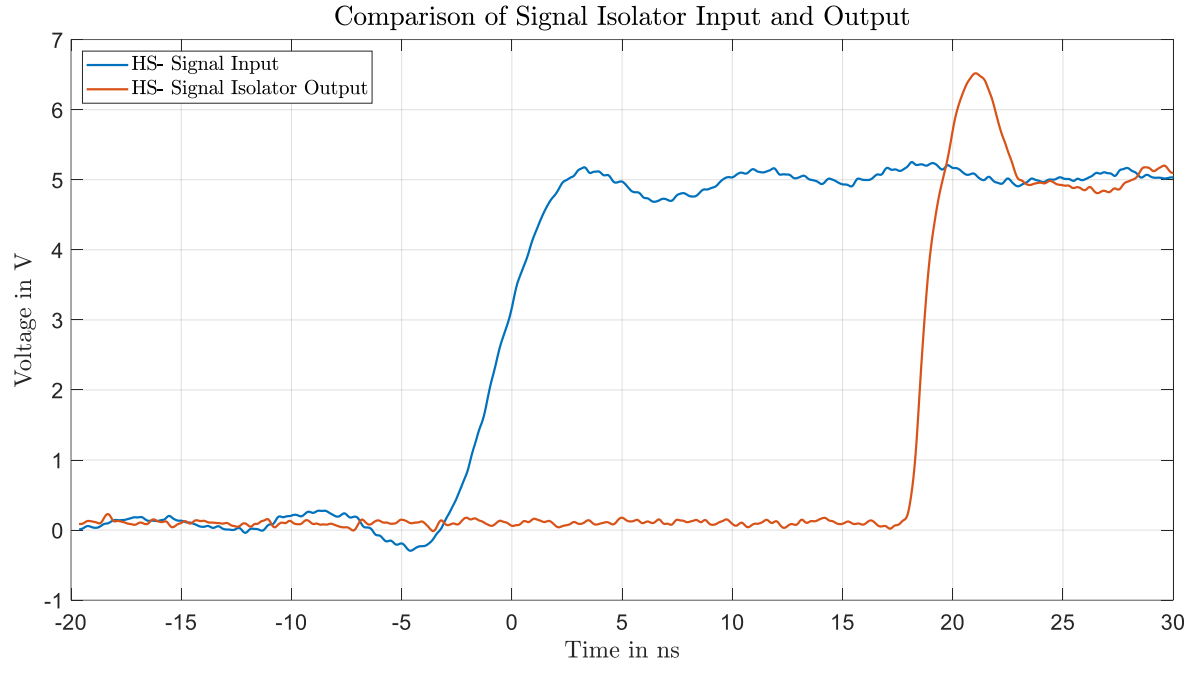

Figure 19: Signal Isolator propagation delay for negative high side channel

Figure 20 shows a comparison between input signal control states and gate source voltages, both at the high side MOSFET, as well as the low side MOSFET. This measurement was done without the MOSFETs soldered to the board. Applying control signals with double the frequency at every input of the board, we can observe all possible input states at a given frequency. This test verifies the functionality of the interlocking circuit. “HS+”, “HS-“, “LS+” and “LS-“ signals were measured at the PCB input with Oscilloscope 1 using digital probes. Gate voltage signals were measured using passive probes.

Figure 21 shows the DESAT voltage waveform, drain source voltage waveform and gate source voltage waveform when a voltage ramp is applied between MOSFET drain and source. This measurement was also done without power MOSFETs present. As can be seen, when the drain source voltage reaches the required values at which the voltage of the DESAT pin crosses 9 V, the overcurrent protection triggers, and positive gate-source voltages are no longer present.

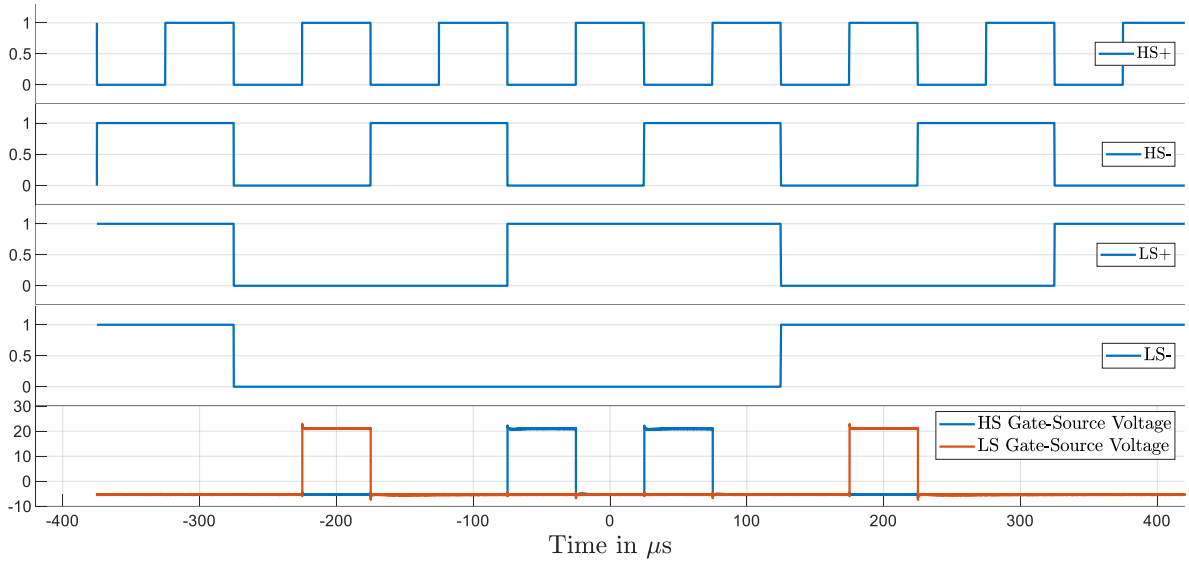

Figure 20: Comparison of input control signals with gate driver output voltage

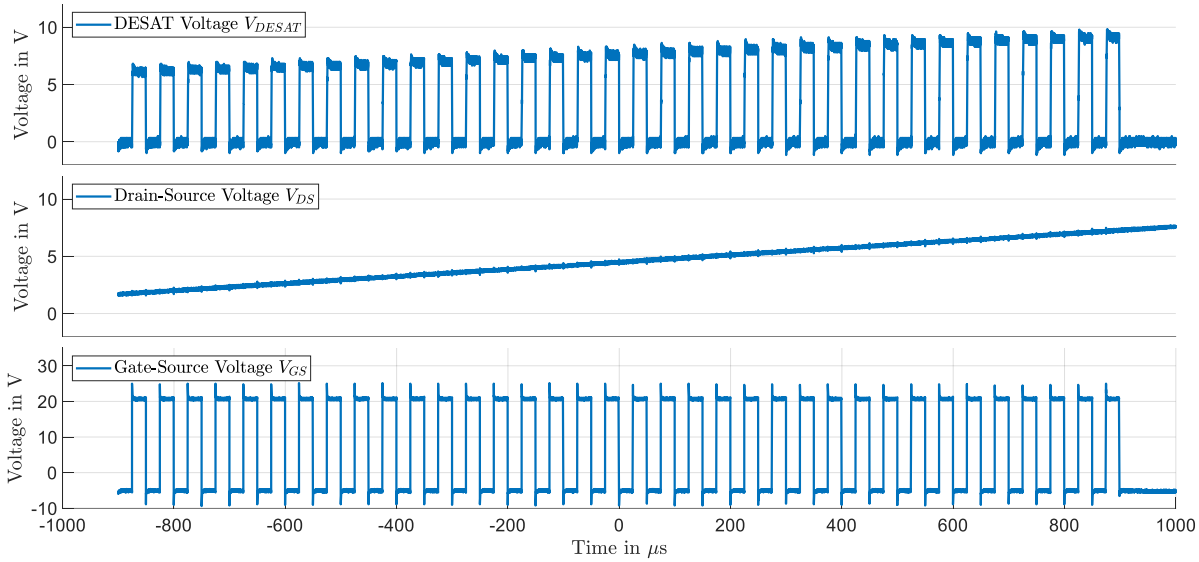

Figure 21: DESAT voltage compared with voltage ramp applied to MOSFET drain pin

The measurement results shown in this chapter provide the confirmation of proper operation of the functional logic part of the PCB. Signal isolation was tested and verified, as well as the interlocking circuit and DESAT protection.

4.2 Double Pulse Test (DPT)

This chapter covers the power testing of the half bridge. The standard categorization method for half bridge switching performance is the Double Pulse Test. Briefly described, two subsequent voltage pulses are applied at the gate of one of the power MOSFETs. Across the second MOSFET an inductive load is present. The first pulse allows for current to build up through the inductor. The MOSFET is then turned off. Current keeps flowing through the inductor and the anti-parallel diode of the second switch. A second pulse is applied after some time. This procedure categorizes the turn on and turn off transients. It is discussed in more detail in [17].

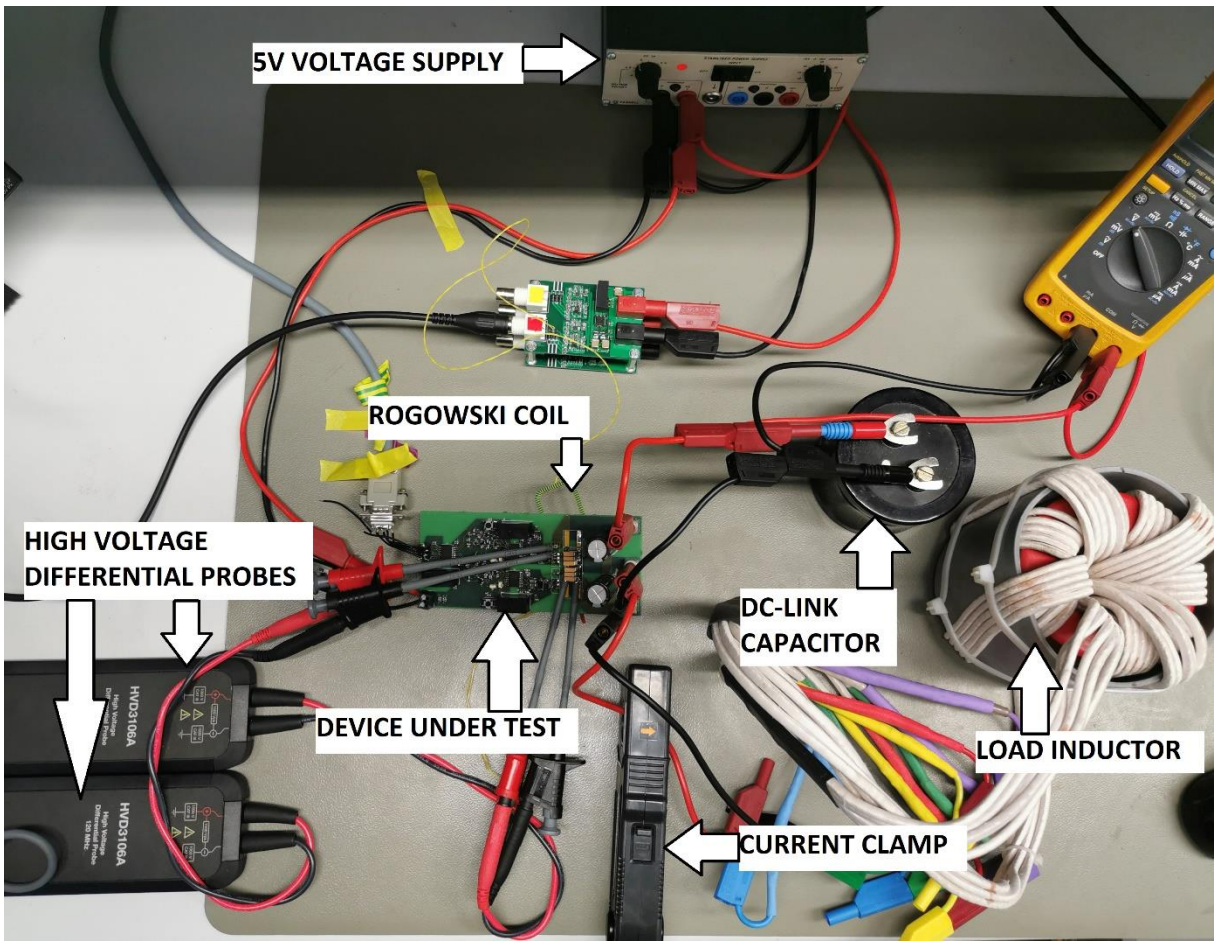

Figure 22: Measurement test setup for double pulse testing

Following figures show the measurement results from Double Pulse Tests at different DC-Link voltages. Testing was done in 100 V increments, starting at a DC-Link voltage of 50 V up to 550 V. In Figure 23, Figure 24, Figure 25, Figure 26, Figure 27 and Figure 28 measurements of drain-source voltage V_{DS}, DC-Link voltage V_{DC}, drain current I_D and load current I_L are shown for different DC voltage levels. Drain-source voltage and DC-Link voltage were measured with high voltage differential probes. The load current was measured with a current clamp. Drain current was measured with a custom made Rogowski coil due to size constraints of the MOSFET drain pin. The gain and offset of the drain current measurement were calculated in post-processing and adjusted to fit with the load current measurement during low frequency periods. During switching transients, the drain current measurement shows strong oscillations. It could not be verified if this is a result of the device under test (DUT), or the measurement coil itself. Comparison of drain current is therefore omitted in this thesis.

It is also important to note that some voltage oscillation and voltage sag is present at the DC-Link during switching. This can be attributed to the lack of DC-Link capacitance on the board. For voltage testing up to 450 V a 2200 µF capacitor (C_{ADD} in Figure 17, also labeled in Figure 22) was added close to the DC-Link terminals of the board improved DC-Link voltage stability. For higher voltages a series connection of two of those capacitors was present at the DC-Link input of the PCB. For better comparison, the measurements presented in Paragraph 4 are caried out with two of those capacitors in series.

In order to achieve equal load current at first turn off for different voltage levels, the duration of the first voltage pulse had to be varied. With known load inductance ($L_{LOAD} = 68\ \mu H$) and DC-Link voltage, the load current at the end of the first pulse τ_1 can be calculated as follows:

$$i_L(t = \tau_1) = \frac{V_{DC}}{L_{LOAD}} \cdot \tau_1 \tag{14}$$

Rearranging to solve for pulse duration we arrive at:

$$\tau_1 = \frac{I_L \cdot L_{LOAD}}{V_{DC}} \tag{15}$$

A representative value of 35 A for the load current was chosen and using Equation (13) pulse durations were calculated (Table 12).

DC-Link Voltage V_{DC}	**Pulse duration τ_1**
V	**µs**
50	47.6
150	15.9
250	9.5
350	6.8
450	5.3
550	4.3

Table 12: Calculated pulse duration τ_1 as a function of DC-Link voltage

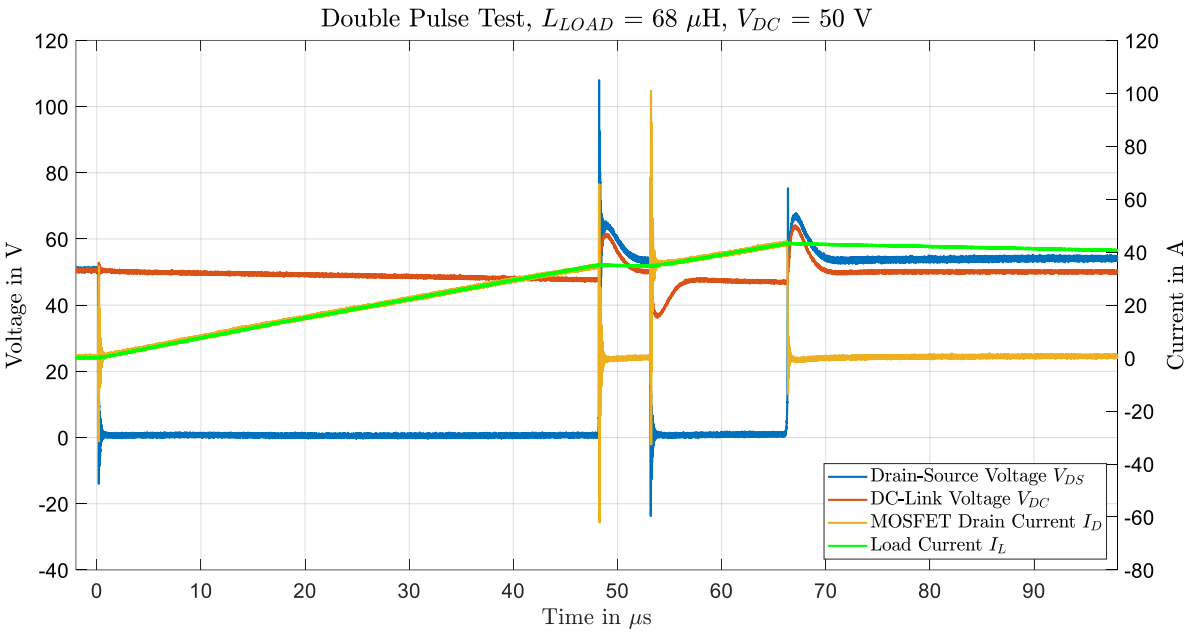

Figure 23: Double Pulse Test at 50 VDC with 68 µH inductive load

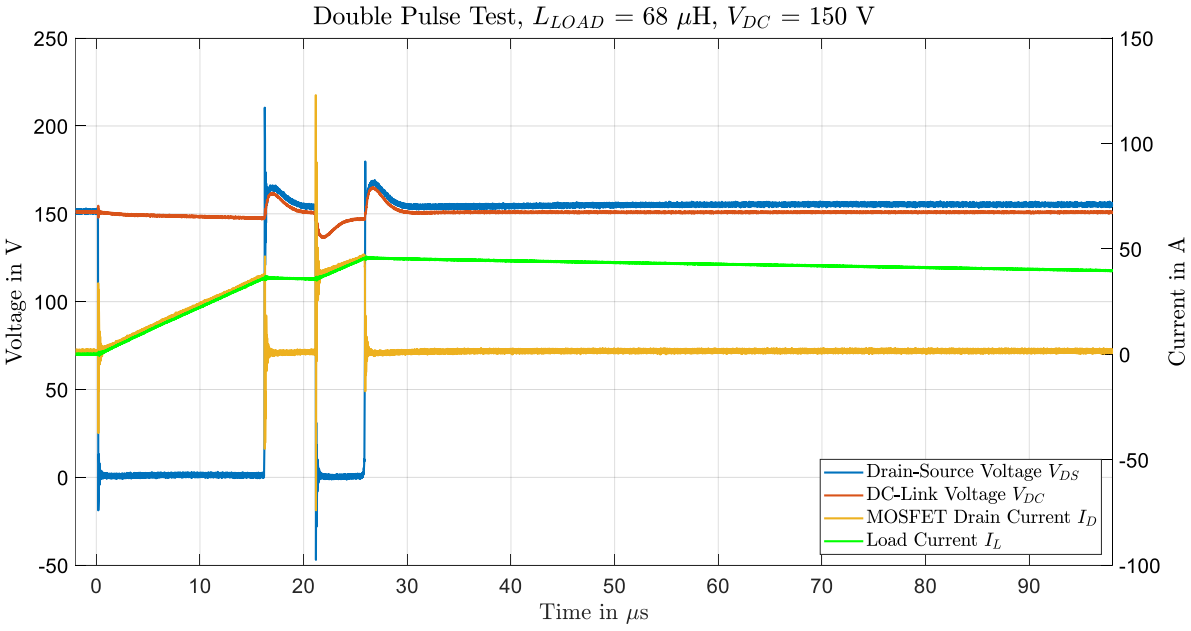

Figure 24: Double Pulse Test at 150 VDC with 68 µH inductive load

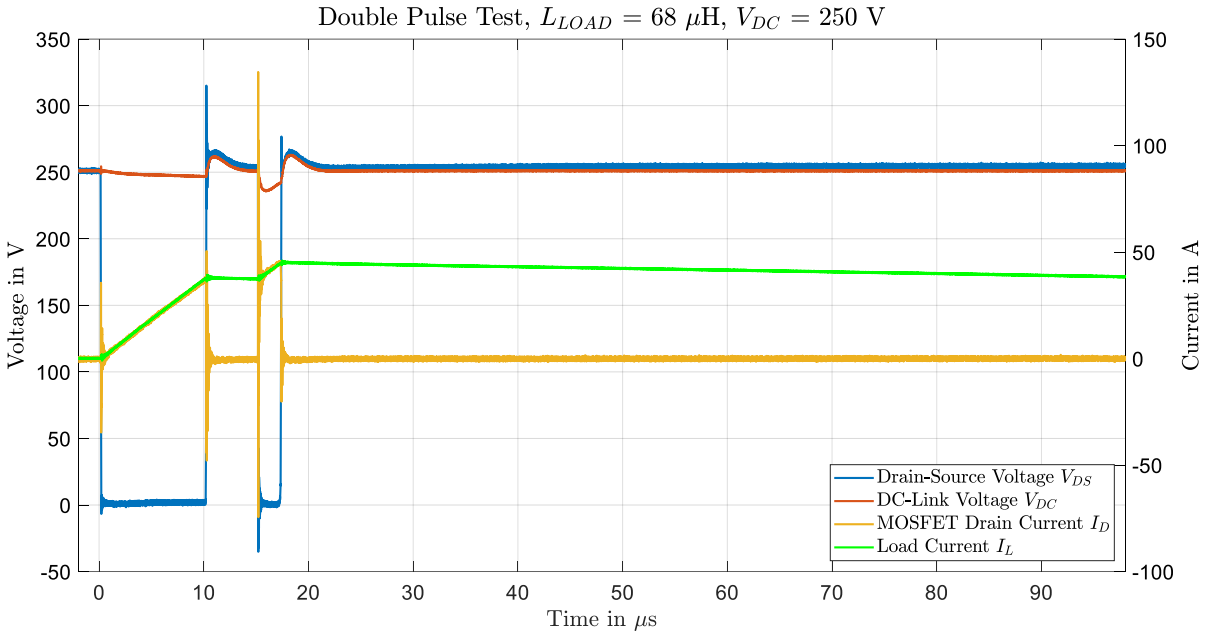

Figure 25: Double Pulse Test at 250 VDC with 68 µH inductive load

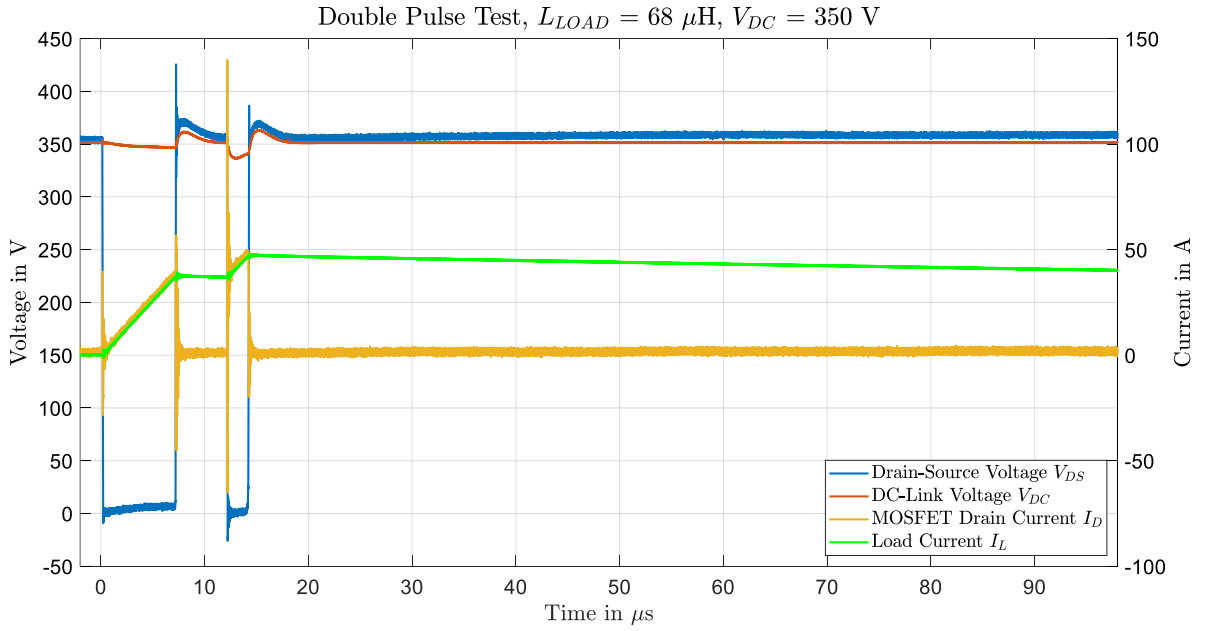

Figure 26: Double Pulse Test at 350 VDC with 68 µH inductive load

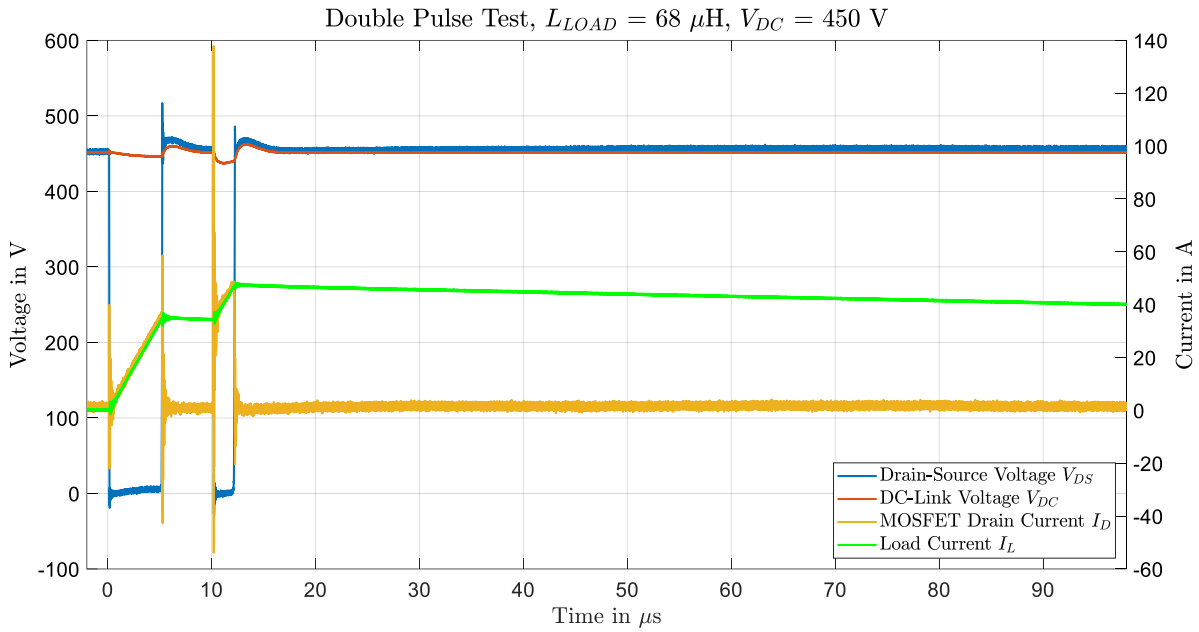

Figure 27: Double Pulse Test at 450 VDC with 68 µH inductive load

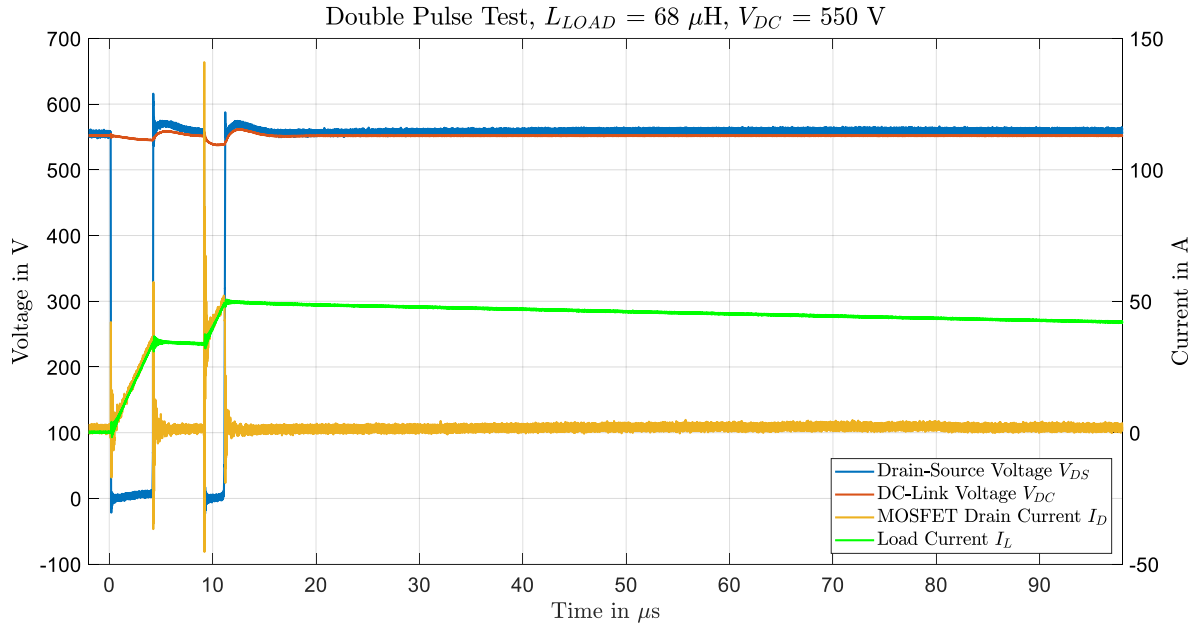

Figure 28: Double Pulse Test at 550 VDC with 68 µH inductive load

In Figure 29 a comparison of Drain-source voltage for all tested DC-Link voltage levels is shown. Figure 30 shows the comparison of the load current. A slight voltage overshoot is noticeable during turn off. Also, voltage undershoot is present during turn-on. The value of the overshoot is 60 V and does not dependent on the DC-Link voltage. This is visible more clearly in Figure 31.

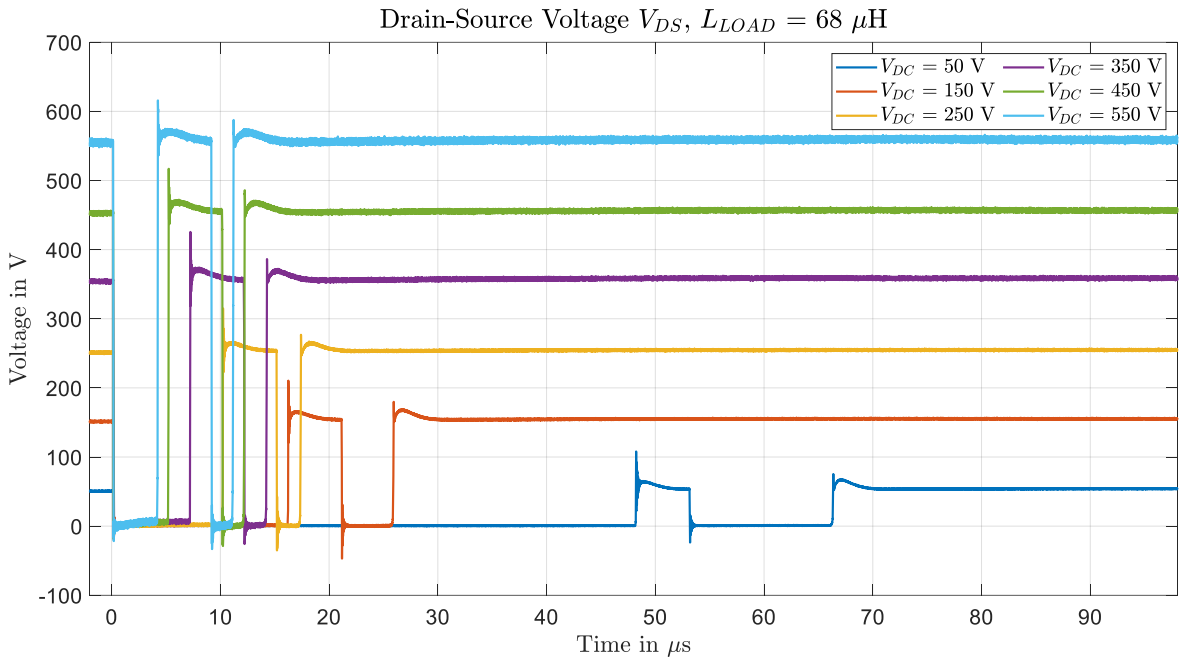

Figure 29: Comparison of Drain-source voltage measurements from DPT

An overview of the load current for varying DC-Link voltage and pulse duration can be seen in Figure 30. As already stated, the duration of the first pulse is varied in order to keep the load current at approximately 35 A for each voltage level. This is clearly visible in the figure. What is also important to note, is the current amplitude at the second turn-off. This turn-off event is initiated by the desaturation protection of the circuit. Although the triggering limit of 60 A was implemented using the external circuitry discussed in Paragraph 3.2, the actual current value at which the desaturation circuit triggers varied slightly for different DC-Link voltages. This might be attributed to the change in on-state drain-source resistance $R_{DS(ON)}$ with changing junction temperature T_J. Another possibility is the influence of the steepness of the current.

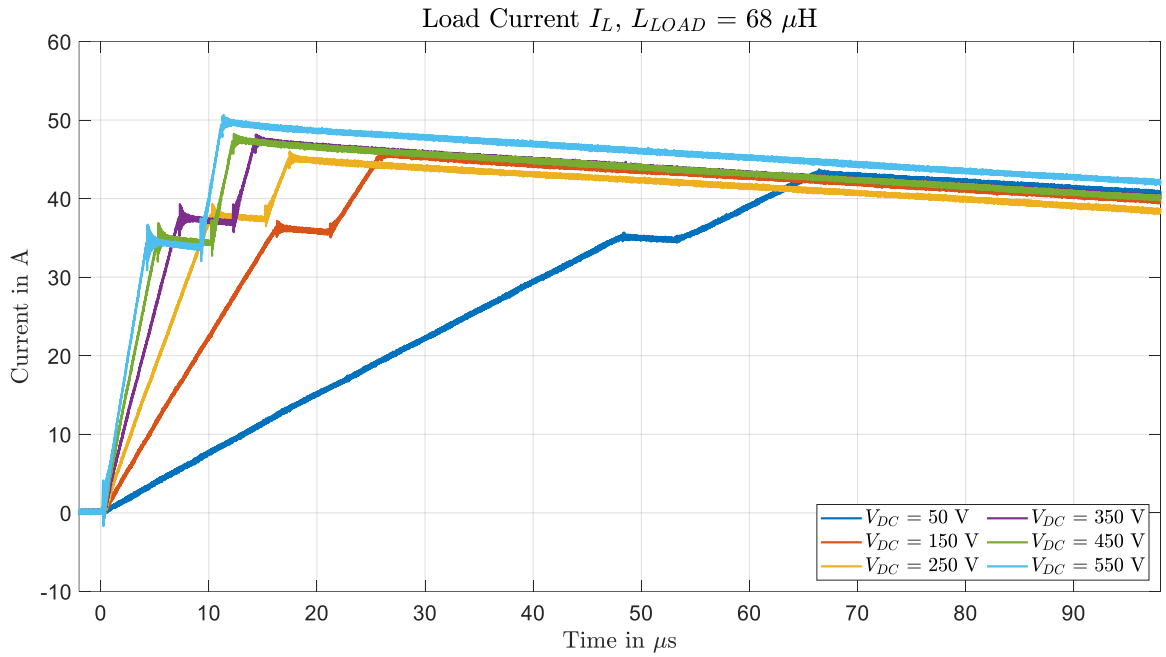

Figure 30: Comparison of Load current measurements from DPT

Figure 31 shows the drain-source voltage waveforms during turn-off of the first pulse. Waveforms were aligned in post-processing.

The rate of change appears to be similar for all voltage levels and is approximately equal to 17 kV/µs. An increase in ringing frequency can be observed with the rise in voltage. This is due to the reduction in MOSFET drain-source capacitance C_{DS} with increasing voltage.

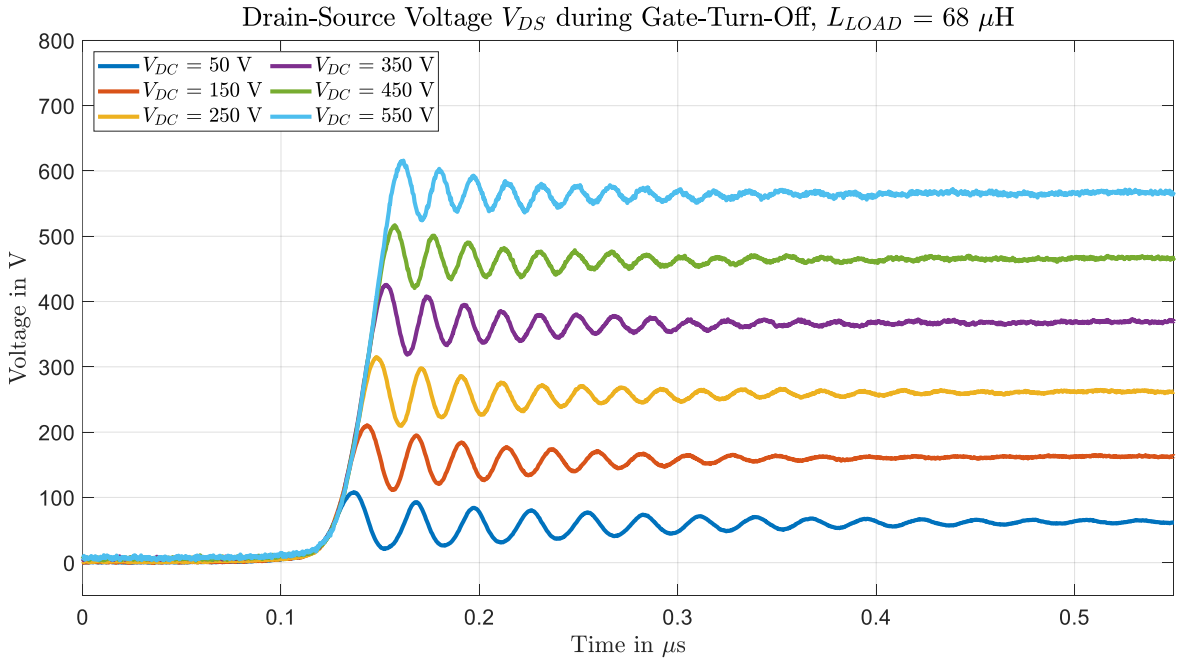

Figure 31: Comparison of Drain-source voltage measurement during Gate-Turn-Off

Figure 32 shows the drain source voltage during turn off as well. However, compared to Figure 31, this turn off even was initiated by the gate driver DESAT protection, as the drain current reached overcurrent condition. Equivalent to formatting in Figure 31, the waveforms were aligned in post-processing. This type of shutdown is a soft shutdown realized by a second (weaker) MOSFET inside the driver, and the rate of change of both voltage and current is lower when compared to forced turn-off. The rate of change for the drain-source voltage is approximately 6 kV/µs for this case.

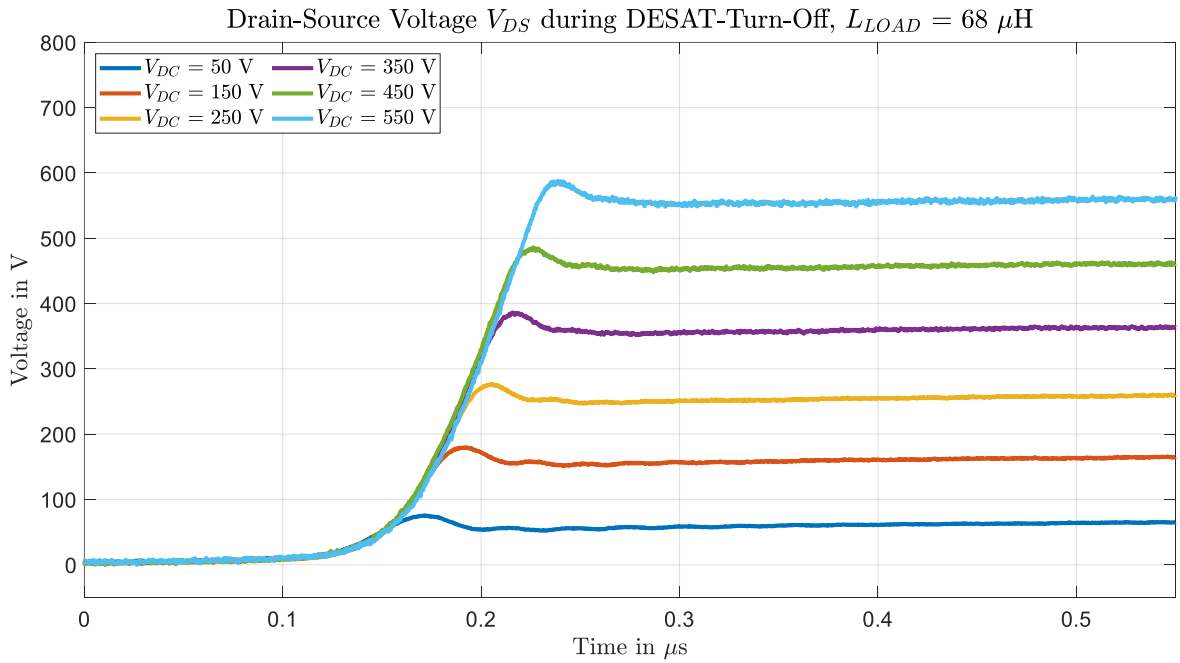

Figure 32: Comparison of Drain-source voltage measurement during DESAT Turn-Off

4.3 Commutation loop inductance

Measuring the drain current I_D of the half bridge MOSFETs proved to be challenging, firstly due to size constraints on the PCB, and secondly due to high current values present during normal operation. Also, during switching, high rates of change in current could be observed.

Preliminary testing was carried out with the commercially available current probe LeCroy CP031A, described in Table 11. Although the measurement range of the probe was suitable when considering bandwidth and maximum current values, the size of the probe required an additional wire loop at the drain pin of the MOSFET under test.

In order to reduce the loop inductance, which was also an aspect of the design presented in this thesis, the current clamp current measurement was substituted with a dedicated Rogowski coil placed around the pin of the high-side MOSFET. This had eliminated the need for a dedicated wire loop for current

measurement. However, during further testing, the measurement results of the Rogowski coil showed significant oscillation, measurement time delay and incorrect rise and fall times of the drain current.

Keeping this in mind, the approximation of power loop inductance L_{Loop} proved to be quite challenging. For tests conducted without reliable drain current measurements, the period of drain-source voltage was examined. As seen in Figure 31, the drain source-voltage oscillates with increasing frequency for higher DC-Link voltages.

In order to estimate the inductance, the-resonance of the loop inductance and the drain-source MOSFET capacitance C_{DS} could be expressed from Equation (16).

$$\omega = \frac{1}{\sqrt{L_{Loop} \cdot C_{DS}}} \tag{16}$$

It follows obviously:

$$L_{Loop} = \frac{1}{\omega^2 \cdot C_{DS}} \tag{17}$$

The drain-source capacitance of the MOSFET can be found in the datasheet of the device. The angular frequency ω can be approximated from the period of oscillation in Figure 31. The drain-source capacitance is however voltage dependent as already stated in this thesis. In Table 13 and in Figure 33, the calculation results are presented.

DC-Link Voltage V_{DC}	**Drain-Source Capacitance C_{DS}**	**Angular Frequency ω**	**Calculated Loop Inductance L_{Loop}**
V	pF	Rad/s	nH
50	845	211.8	26.4
150	445	269.2	31.0
250	370	299.2	30.2
350	322	330.7	28.4
450	277	342.7	30.7
550	258	355.6	30.6

Table 13: Loop inductance estimation from drain-source voltage oscillation

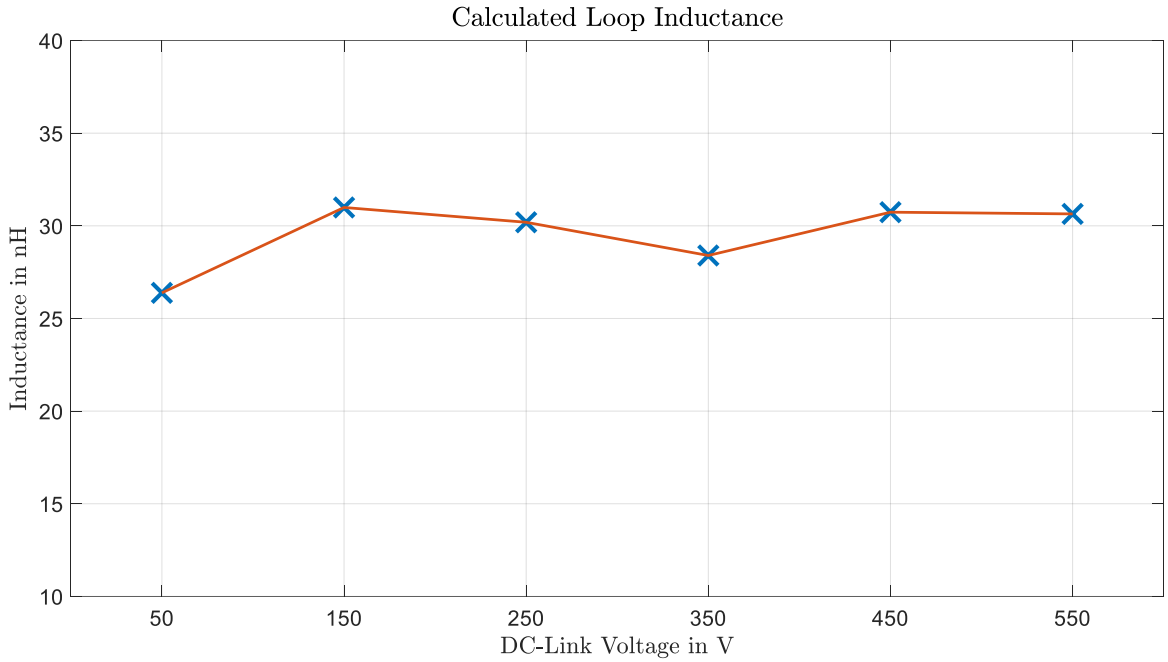

Figure 33: Calculated loop inductance as a function of DC-Link voltage

As an example for loop inductance estimation from the rate of change of drain current $\frac{di}{dt}$, a measurement from preliminary testing was examined. Applying the following equation (already stated in Paragraph 3.3):

$$L_{Loop} \approx \frac{v_{DC} - v_{DS}}{\frac{\Delta i_L}{\Delta t}} - L_{CL} \tag{18}$$

to current and voltage waveforms in Figure 34, we arrive at a value for loop inductance of 50.3 nH.

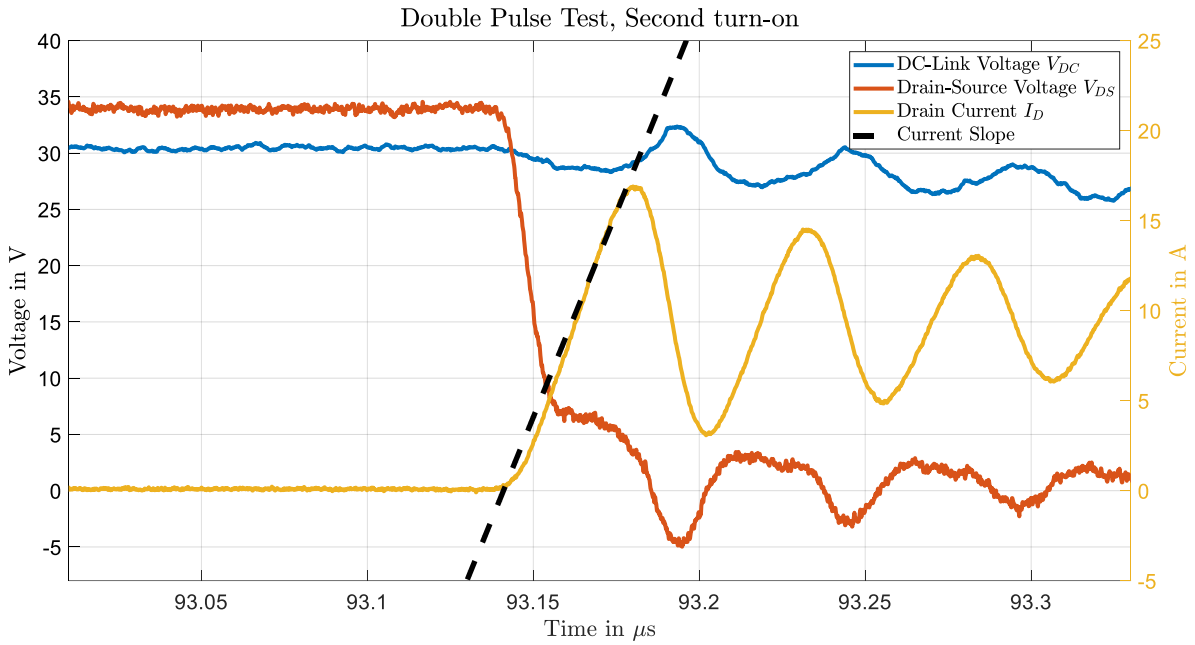

Figure 34:Turn on event at 30 VDC with added loop inductance for current measurement

The black dotted line represents the rate of change of current.

When comparing the results of the inductance approximation from the drain-source voltage oscillation and the inductance calculated from current rate of change, we can conclude that the additional loop used for current measurement had an inductance of 20-25 nH. This agrees with the calculation results for the wire geometry used.

5 Conclusion and further work

The work presented in this thesis encompassed the design and testing process of a half bridge with special focus on design and testing challenges for silicon carbide devices. When compared to silicon-based half bridge design, additional precaution must be taken when designing the power loop of the circuit. Short circuit protection proved to be challenging as well. For testing, it is important to have high bandwidth equipment available.

In Paragraph 4, testing and evaluation of the device is presented. Switching performance of the half bridge was evaluated for the intended DC-Link voltage range: 50 V to 550 V. The measurement results show acceptable half bridge performance. Voltage overshoot is approximated to be 50-60 V at the peak of nominal current for IM 1 and is well below the maximum drain-source voltage of the MOSFETs even at 550 V DC-Link voltage. Also, the functionality of the desaturation overcurrent protection was confirmed for all voltage levels.

Some possible ideas for future work include:

- Loss evaluation at different voltages and frequencies
- Influence of gate resistance on switching behavior
- Influence of additional DC-Link capacitance
- Improvement of current measurement
- Short-circuit testing
- Modular three-phase inverter based on this half bridge design

A good starting point for further testing would be the estimation of device power losses at higher voltages, as well as at different frequencies. A reasonable continuation for testing might be the comparison of switching losses to output filter weight with varying frequency.

Another tradeoff might be investigated when considering a variation in the gate resistance R_G. With the increase of the gate resistance lower voltage overshoot is possible. However, this increases the switching losses.

If higher DC-Link voltage stability is needed, a redesign of the PCB power side could prove to be a viable solution by increasing the DC-Link capacitance.

The current measurement setup should be examined in order to determine the cause of oscillation in the measurement signals. Some possible solutions for more robust current measurement are dedicated current sense resistors on the PCB and Rogowski coils designed with signal integrity in mind.

Additionally, short-circuit protection might be evaluated for two possible cases: MOSFET turn-on while the half bridge output is shorted and short-circuit event during the on-state of the high-side MOSFET.

Finally, the design presented here could be incorporated into a modular three-phase voltage source inverter as one of the phase legs.

6 References

[1] N. Mohan, T. M. Undeland and W. P. Robbins, Power Electronics, 2nd ed., John Wiley & Sons, 1995.

[2] J. Biela, M. Schweizer, S. Waffler and J. W. Kolar, "SiC versus Si—Evaluation of Potentials for Performance Improvement of Inverter and DC–DC Converter Systems by SiC Power Semiconductors," *EEE Transactions on Industrial Electronics,* vol. 58, pp. 2872-2882, July 2011.

[3] S. Yin, K. J. Tseng, R. Simanjorang, Y. Liu and . J. Pou, "A 50-kW High-Frequency and High-Efficiency SiC Voltage Source Inverter for More Electric Aircraft," *EEE Transactions on Industrial Electronics,* vol. 64, pp. 9124-9134, November 2017.

[4] J. Millán, P. Godignon, X. Perpina, . A. Perez-Tomas and J. Rebollo, "A Survey of Wide Bandgap Power Semiconductor Devices," *IEEE Transactions on Power Electronics,* vol. 29, pp. 2155-2163, May 2014.

[5] X. She, A. . Q. Huang, Ó. Lucía and B. Ozpineci, "Review of Silicon Carbide Power Devices and Their Applications," *IEEE Transactions on Industrial Electronics,* vol. 64, pp. 8193-8205, October 2017.

[6] A. K. Morya, M. C. Gardner, B. Anvari, L. Liu, A. G. Yepes, J. Doval-Gandoy and H. A. Toliyat, "Wide Bandgap Devices in AC Electric Drives: Opportunities and Challenges," *IEEE Transactions on Transportation Electrification,* vol. 5, pp. 3-20, March 2019.

[7] J. Millán, "A REVIEW OF WBG POWER SEMICONDUCTOR DEVICES," in *(CAS) International Semiconductor Conference*, pp. 57-66, 2012.

[8] K. P. Cheung, "SiC Power MOSFET Gate Oxide Breakdown Reliability – Current Status," in *IEEE International Reliability Physics Symposium*, pp. 2B.3-1-2B.3-5, 2018.

[9] "CREE C3M00162120K Datasheet," April 2019. [Online]. Available: https://www.wolfspeed.com/downloads/dl/file/id/1483/product/643/c3m0016120k.pdf. [Accessed June 2021].

[10] "Microsemi MSC025SMA120B Datasheet," October 2019. [Online]. Available: https://www.microsemi.com/document-portal/doc_download/1243495-msc025sma120b-datasheet. [Accessed June 2021].

[11] "OnSemicondutor NTH4L020N120SC1 Datasheet," April 2021. [Online]. Available: https://www.onsemi.com/pdf/datasheet/nth4l020n120sc1-d.pdf. [Accessed June 2021].

[12] "Rohm SCT3022KL Datasheet," June 2018. [Online]. Available: https://fscdn.rohm.com/en/products/databook/datasheet/discrete/sic/mosfet/sct3022kl-e.pdf. [Accessed June 2021].

[13] D. Graovac, M. Pürschel and A. Kiep, "MOSFET Power Losses Calculation Using the DataSheet Parameters," 2006. [Online]. Available: https://application-notes.digchip.com/070/70-41484.pdf. [Accessed June 2021].

[14] "Analog Devices ADuM262N Datasheet," [Online]. Available: https://www.analog.com/media/en/technical-documentation/data-sheets/ADuM260N-261N-262N-263N.pdf. [Accessed May 2021].

[15] “Using the ADuM4135 Gate Driver with the Microsemi APTGT75A120T1G 1200 V,” May 2019. [Online]. Available: https://www.analog.com/media/en/technical-documentation/application-notes/AN-1602.pdf. [Accessed June 2021].

[16] L. Zhang, P. Liu, A. Q. Huang, S. Guo and R. Yu, “An Improved SiC MOSFET-Gate Driver Integrated Power Module with Ultra Low Stray Inductances,” in *IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, pp. 342-345, 2017.

[17] S. S. Ahmad and G. Narayanan, "Double pulse test based switching characterization of SiC MOSFET," in *2017 National Power Electronics Conference (NPEC)*, pp. 319-324, 2017.