Hanka Alagić, BSc

Development of an Area Optimized, EMC Robust Power Management for Automotive Impedance Monitoring

MASTER'S THESIS

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Supervisor

Ass. Prof. Dipl. Ing. Dr. techn. Peter Söser
Institute of Electronics

Dipl. Ing. Günter Hofer
Infineon Technologies Austria AG

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Affidavit

I hereby declare that the present master's thesis was composed by myself and that I have only used the declared resources. All formulations and concepts taken verbatim or in substance from printed or non-printed material or from the Internet have been cited according to the rules of good scientific practice.

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Abstract

This thesis discusses alternative power supply concepts for the impedance-measurement IC with high-performance requirements. The analysis is concentrated on the linear voltage regulators. There are various concepts of how an application-specific linear voltage regulator can be realized. Based on the given specifications, different topologies have been analyzed, starting with the most simple ones and extending to the more complicated architectures. The design is done using $130\,nm$ technology and it has been tested for various load and line disturbance profiles. The analysis is based on simulations over all process corners and wide temperature range, taking into account the mismatch of the devices and process variations. Firstly, the characteristic differences of linear voltage regulators with NMOS or PMOS pass device have been compared. The performances of the linear voltage regulator with an NMOS pass device without the charge pump circuit have been evaluated. Advantages of using low or medium voltage devices regarding the area reduction versus exceeding the breakdown voltage of the particular devices have been discussed. That leads to the design of the stacked architecture with a pre-regulator and three main voltage regulators using low voltage NMOS pass devices, together with the internal bias and bandgap voltage reference, charge pump and clock generation circuit. No external components, such as buffer capacitors have been used. The three main regulators are able to regulate a dynamic battery cell voltage from $2\,V$ to $5\,V$ to a nominal $1.5\,V$ output voltage at a maximum load current of $10\,mA$ each. Output voltage variation for different line and load transient profiles doesn't exceed the $\pm 10\%$ of the nominal output voltage.

Keywords: power supply concepts, linear voltage regulators, analog integrated circuits, NMOS/PMOS pass device, impedance measurement

Kurzfassung

In dieser Arbeit werden alternative Spannugsversorgungskonzepte für den Impedanzmess-IC mit hohen Leistungsanforderungen diskutiert. Die Analyse konzentriert sich dabei auf die linearen Spannungsregler. Es gibt verschiedene Konzepte, wie ein anwendungsspezifischer linearer Spannungsregler realisiert werden kann. Basierend auf den gegebenen Spezifikationen wurden verschiedene Topologien analysiert, angefangen bei den einfachsten bis hin zu den komplizierteren Architekturen. Der Schaltungsentwurf wurde in 130 nm-Technologie durchgeführt und für verschiedene Last- und Netzstörungsprofile getestet. Die Analyse basiert sich auf Simulationen über alle Prozessecken (Process Corners) und einen weiten Temperaturbereich, wobei auch zufällige Bauteilmismatch und Prozessvariationen berücksichtigt werden. Zunächst wurden die charakteristischen Unterschiede von linearen Spannungsreglern mit NMOS- oder PMOS-Durchlassbauelement verglichen. Die Leistungen des linearen Spannungsreglers mit einem NMOS-Durchlassbauelement ohne Ladungspumpe wurden ausgewertet. Die Vorteile der Verwendung von Nieder- oder Mittelspannungsbauelementen hinsichtlich der Flächenreduzierung gegenüber dem Überschreiten der Durchbruchspannung der jeweiligen Bauelemente wurden diskutiert. Dies führte zum Entwurf einer gestapelten Architektur mit einem Vorregler und drei Hauptspannungsreglern unter Verwendung von Niederspannungs-NMOS-Durchlasstransistoren, zusammen mit der internen Bias- und Bandgap-Spannungsreferenz, der Ladungspumpe und der Takterzeugungsschaltung. Es wurden keine externen Komponenten, wie z.B. externen Kondensatoren, verwendet. Die drei Hauptregler sind in der Lage, eine dynamische Batteriezellenspannung von 2 V bis 5 V auf eine nominale Ausgangsspannung von 1.5 V bei einem maximalen Laststrom von jeweils 10 mA zu regeln. Die Ausgangsspannungsvariation für verschiedene transiente Netz- und Lastprofile überschreitet nicht die $\pm 10\%$ der nominalen Ausgangsspannung.

Schlagwörter: Spannungsversorgungskonzepte, lineare Spannungsregler, analoge integrierte Schaltungen, NMOS/PMOS-Durchlassbauelement, Impedanzmessung

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1 Motivation

Li-ion batteries have a wide field of applications such as portable electronics, electric household items, medical health instruments and as well as electric vehicles. Therefore multipack batteries as well as single cells have to be under constant monitoring to ensure that the function and the safety of the vehicle occupants is guaranteed. In addition to permanent voltage and temperature measurement, electrochemical impedance spectroscopy (EIS) is used.
A complete state determination of the Li-ion cells can be made from the internal impedance curves in the frequency range from mHz to a few kHz. The impedance range varies from a few $m\Omega$ to a few $100\mu\Omega$ depending on the cell chemistry and size of the battery cells. To be able to determine imprinted AC voltage changes down to a few $10\,\mu V$, in an environment that is very noisy due to the switching of the power transistors, the requirements for the supply voltage for the measurement hardware are enormous. In this context, the power supply concept has to meet high performances such as high power supply rejection ratio with maximum $200\,mV$ noise per cell.

2 Electrochemical Impedance Spectroscopy

A cell is the basic part of the battery. Li-ion rechargeable cells have become more and more popular due to their high energy and power density, low self-discharge rate and long lifetime, but have to be constantly monitored due to reduced lifetime of the cells operated outside their safe operating area. Li-ion cell capacity decreases linearly with the number of charge and discharge cycles. All that changes can be associated with the variations in the internal impedance of the battery itself. The resistance of a typical Li-ion cell is in the order from 500 $\mu\Omega$ to 800 $\mu\Omega$. [1]

Electrochemical Impedance Spectroscopy (EIS) is a technique used for the determination of a battery cell impedance in order to estimate and accurately predict the State of Charge (SoC) and State of Health (SoH) of the battery and define its operational boundaries. [2]

SoC refers to the actual available charge compared to the total charge of the battery when fully charged, while SoH refers to the actual condition of the battery compared to the nominal state. [1]

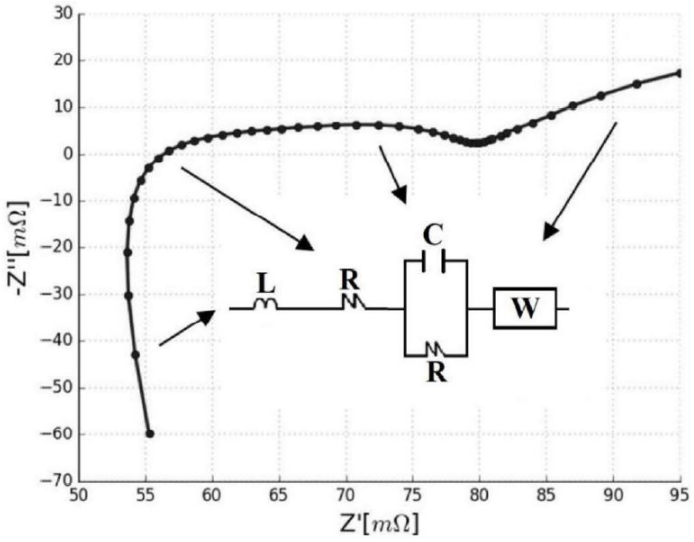


Figure 2: Typical Li-ion battery impedance measurement - Nyquist plot with an equivalent electrical model [17]

EIS measurements consist of applying an AC signal at the battery terminals and repeatedly measuring the impedance at different frequencies (typically kHz to mHz range) which is then used to determine the battery performance under different operating conditions and

temperatures, since the impedance values also vary with the temperature. These data are relevant for battery management and can improve range prediction accuracy. [2]
The impedance values can be visualised in the Nyquist plot, which is used to present the real and the imaginary impedance components, as shown in the figure 2, where the frequency decreases from left to right, or in the Bode plot as a separate representation of the impedance magnitude and phase over the frequency range. [3]
The impedance curve can then be compared to the characteristic shape of impedance graphs of basic electrical elements and the equivalent electrical circuit can be modeled and used to predict the dynamic changes during the battery life. For example, high frequency response near the origin of the plot can be modeled by an inductor and an ohmic resistor due to the metal elements of the cell and cables, the middle part by an RC-parallel branch dependent on the electrode potential. [17]
Low frequencies on the right side are represented by the Warburg impedance W associated with the diffusion process of Li-ion in the electrode material. [19]
EIS of Li-ion batteries has been limited to the laboratory measurements and it requires a well-defined measurement setup, a proper measurement hardware and a deep understanding of the chemical and dynamic processes happening inside the battery in order to correctly evaluate the measured impedance data.
Long lasting batteries, such as the ones used in electric vehicles have to be monitored onboard during the operation in order to measure the temperature of the cell cores and establish their SoC and SoH. The data is then used for safety measures and improvements in the battery management systems (BMS). [3]
This usually involves a complex implementation and high costs.

3 Introduction to Linear Voltage Regulator Topologies

A voltage regulator produces a constant output voltage from a poorly specified DC input voltage. It consists of an internal reference voltage, an error amplifier, a resistive feedback voltage divider and a pass device. The error amplifier compares the reference voltage with the feedback and delivers the voltage that controls the gate of the pass device responsible for sourcing the output current. If the output voltage falls below the desired value, decreasing also the difference between the feedback and reference voltage, the error amplifier increases the gate voltage and with that the gate-source voltage of the pass device is increased, thus more current can flow through the pass device, increasing in turn the output voltage. Therefore the pass transistor in the linear voltage regulator acts as a variable resistor regulated by the feedback loop and can be realized as a bipolar junction transistor (BJT) as well as a metal–oxide–semiconductor field-effect transistor (MOSFET).

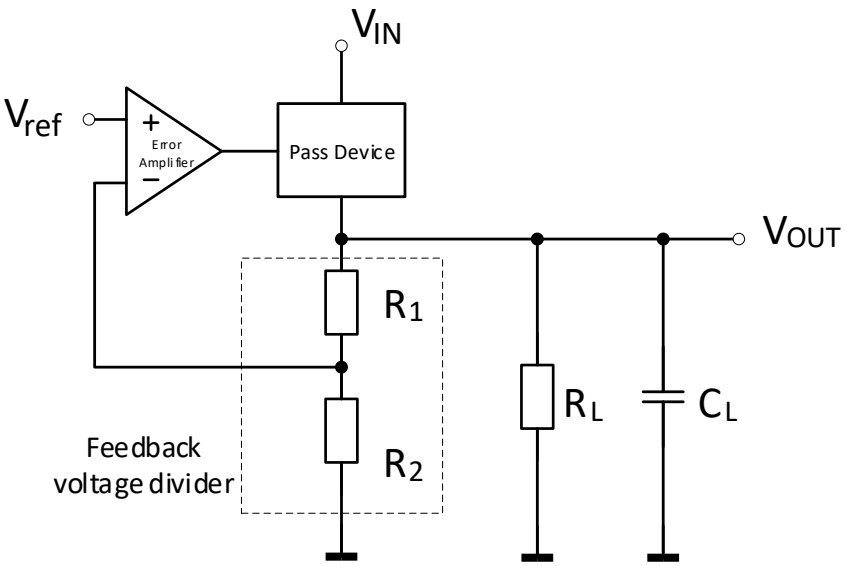


Figure 3: Linear voltage regulator - block diagram

Fixed reference voltage is usually provided by the bandgap circuit. The resistive feedback network determines the mathematical relationship between the reference and the output voltage as:

$$V_{OUT} = \frac{R_1 + R_2}{R_2} V_{ref} \tag{1}$$

There are three main types of voltage regulators [21]:

- linear voltage regulators
- switching mode voltage regulators
- shunt voltage regulators

In this work the main focus is set to linear voltage regulator with a pass device connected in series with the unregulated supply and the load. Shunt regulators are the linear voltage regulators with the pass device connected in parallel with the load. [21]

3.1 Characteristics of Linear Voltage Regulators

In this section some of the main characteristics of the linear voltage regulators (LVR) are explained.

3.1.1 Drop-out Voltage

Drop-out voltage is defined as the minimum voltage difference between the input and the output at which the output voltage regulation can be maintained [8]. If this voltage difference drops below the minimum drop-out voltage, the pass device of the regulator acts as a variable resistor and operates in a linear region where the output follows the input voltage. To be able to regulate the output voltage to a desired value, the linear voltage regulator normally operates in a saturation region, where its pass device acts as a voltage controlled current source. An LVR can be referred to as a low drop-out (LDO) regulator if it can operate in low drop-out voltage regulation.

3.1.2 Load Regulation

The dependence of the output voltage V_{OUT} on the load current I_{OUT} is defined as the load regulation. It is similar to load transient response. The only difference is that the transient response refers to dynamic variation of the load, while load regulation to the static variation. The ideal behaviour would be that the output voltage is not influenced by the change in the

load current, but due to the finite open loop gain, a change in the output current causes a change in the output voltage.

$$Load\ Regulation = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} \approx \frac{-1}{g_m A \frac{R_2}{R_1+R_2}} \tag{2}$$

Equation 2 applies for both NMOS and PMOS pass device, and it shows that load regulation depends on the open loop gain of the amplifier A, the transconductance of the pass transistor g_m and the resistive divider with R_1 and R_2. [9]
Load transient response is affected by the load capacitor and the overall phase margin of the system. A higher value of the output capacitance reduces the over-/undershoots of the output voltage during the load transients, but it also increases the settling time, which is the time needed for the regulator to stabilize the output voltage back to its nominal value.

3.1.3 Line Regulation

The line regulation defines the variation of the output voltage with the change of the input voltage. It is related to line transient response which refers to dynamic variation in the input voltage, and line regulation to the static variation.

$$Line\ Regulation = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \tag{3}$$

PMOS line regulation can be defined as [9]:

$$\frac{\Delta V_{OUT}}{\Delta V_{IN}} \approx \frac{1}{A \frac{R_2}{R_1+R_2}} \tag{4}$$

Equation 5 describes the line regulation for the NMOS pass device, introducing the intrinsic gain of the pass device $g_m \cdot r_o$ as an additional parameter. [9]

$$\frac{\Delta V_{OUT}}{\Delta V_{IN}} \approx \frac{1}{g_m r_o A \frac{R_2}{R_1+R_2}} \tag{5}$$

Increasing open loop gain improves both load and line regulation.

3.1.4 Stability

The LVR can easily become unstable due to its negative feedback loop and a connection of at least 2 gain stages. A thorough stability analysis of the system has to be done in order to check its stability. This is usually done by AC analysis using Bode plots and calculating the phase margin of the system to assess the stability of the control loop.
Stability can be determined by analyzing the approximate location of the poles and zeros. Each of them has an impact on the gain and phase of the feedback loop. Poles contribute with $-90°$ and zeros with $+90°$ in phase shift. The impact on the gain is $\pm 20dB$ per decade, respectively for zeros and poles. So basically, the phase of the system can be inverted with two poles. The phase shift can be compensated with a zero. Different compensation techniques are possible, depending on the architecture of the regulator.

3.1.5 Power Supply Rejection - PSR

Power supply rejection describes the ability of a regulator to suppress power supply noise from its output over a wide frequency range.

$$PSR(f) = \frac{\Delta V_{OUT}(f)}{\Delta V_{IN}(f)} \tag{6}$$

The power supply rejection ratio (PSRR) is measured in decibel and defined as:

$$PSRR = 20log\, PSR \tag{7}$$

PSR of an LDO is mostly determined by the open loop gain of the error amplifier. There are three regions that characterize the PSRR of an LDO. The first one is in the low frequency region and it refers to the bandgap reference PSRR, second region is the open loop gain region of the error amplifiers gain bandwidth up to the unity gain frequency, and the third region is above unity gain frequency where the output capacitor dominates along with any parasitics between the input and output voltage. [18]

4 Design Specifications and Requirements

The linear voltage regulator is implemented in 130 nm technology and it is assumed to be a part of an impedance measurement IC of a single cell Li-ion battery.

For the dynamic input voltage range from 2 V - 5 V the LVR should generate a stable, nominal output voltage of 1.5 V with a maximum error of $\pm 10\%$ of the nominal value, which equals to the minimum of 1.35 V and the maximum of 1.65 V. This error budget is defined by the safety limitation of the digital library devices.

Application specific design includes various high performance requirements. The voltage regulator needs to react fast in case of a quick load change or a change in the supply voltage in order to keep the output voltage stable. Therefore minimizing the regulator's transient response and increasing its power supply rejection ratio (PSRR) are important tasks. The main design specifications listed in the Table 1 dictate the architecture of the circuit, as well as the choice of the pass device.

Process technology	130 nm
Operating input voltage range	2 V to 5 V
Nominal output voltage V_{OUT}	1.5 V
Maximum output voltage error	$\pm 10\%$ V_{OUT}
Temperature region	$-40°C$ to $120°C$

Table 1: Main design specifications

5 Pass Device Comparison

The selection of the pass device needs to satisfy the design specifications, such as defined input and output voltage range. Despite the fact that the MOS as well as BJT transistors can be used as pass device, the focus will be set on MOS devices, as on the comparison between the NMOS and PMOS transistors. Keeping up with the technology trends and using lower supply voltages leads in favour of using the PMOS pass device because there is no need for the higher gate voltage to achieve the low dropout voltage. Using low voltage devices is preferable due to better power efficiency, smaller chip area and low costs, but also introduces the problem of the low device breakdown voltage.

5.1 Pass Device Characterization

Figure 4 shows the testbench used to check the dynamic behaviour of the non-regulated pass device by applying a step to the input voltage or load current. The simulations are done in order to roughly characterize and choose the pass device. For this purpose medium voltage devices are chosen, which can tolerate higher input supply voltages according to the design specification.

Simulations are done separately for both PMOS and NMOS pass device. An ideal voltage source is used at the gate of the pass device, which voltage has been determined for the nominal output voltage of $1.5\,V$ at the load current of $1\,mA$. Supply voltage is set to $5\,V$. In the figure 5 the applied step in the output current is depicted. Figures 6a and 6b show the applied change in the supply voltage.

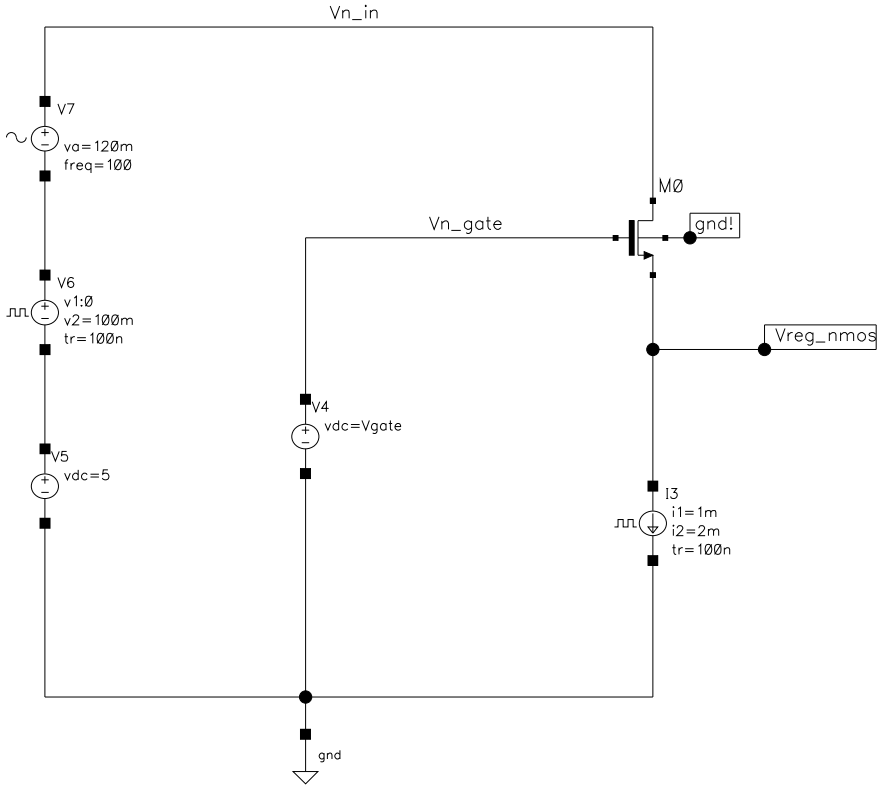


Figure 4: Testbench - dynamic behaviour of the pass device

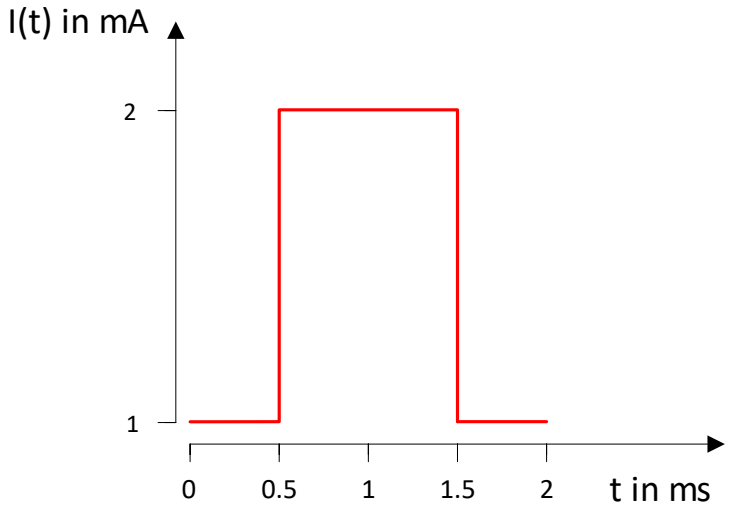
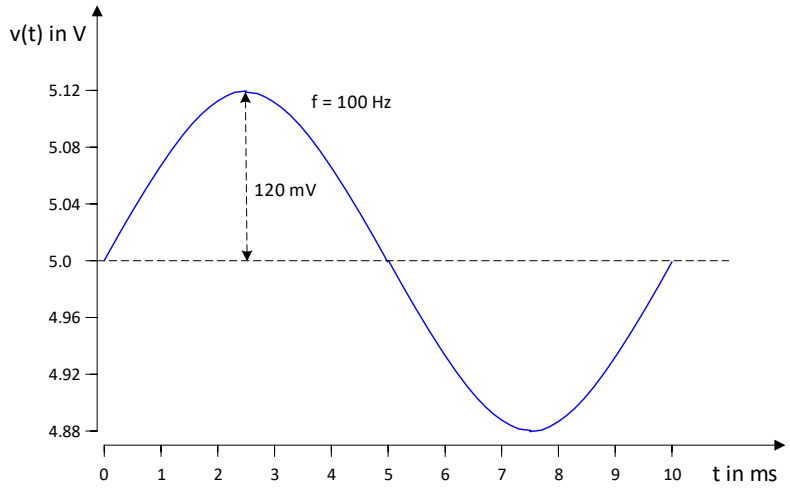
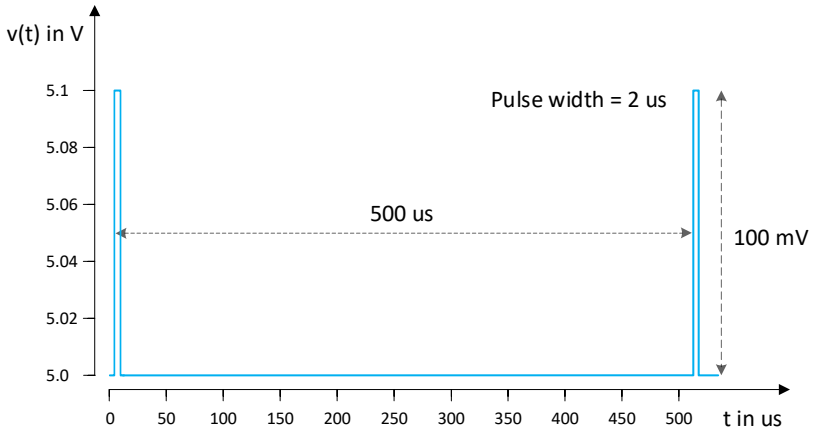


Figure 5: Load current pulse with a rise/fall time of 100 ns



(a) Sine wave



(b) Pulse signal

Figure 6: Change of the input voltage

Disturbance profile	NMOS	PMOS
Load current pulse	$\Delta V_{OUT} = 67\,mV$	$\Delta V_{OUT} = 3.5\,V$
Input voltage change-100 mV pulse	$\Delta V_{OUT} = 4.38\,mV$	$\Delta V_{OUT} = 2.76\,V$
Input voltage change-sine wave	$\Delta V_{OUT} = 5.25\,mV$	$\Delta V_{OUT} = 3.09\,V$

Table 2: Summary PMOS vs. NMOS pass device - Output voltage step response

Table 2 shows the summary of the differences in the output voltage ΔV_{OUT} from the nominal output value, as response to the presented disturbance profiles. It can be seen that the

NMOS pass device shows much better step response to the change in the input voltage or output current. The values of the change in the output voltage stay in the mV-range for the NMOS, while the PMOS pass device exceeds its maximum drain-source breakdown voltage. Therefore it can be concluded that the NMOS pass device is basically self-regulating and less sensitive to noise on its source or drain node. To avoid changes in the output voltage due to the load or line variations, a negative feedback is required. This is realized by adding an error amplifier to the feedback loop which controls the gate voltage of the pass device and adjusts the gate-source voltage depending on the change in the load or supply voltage.

5.2 NMOS as Pass Device

An NMOS pass device requires a positive drive voltage from its gate with respect to the output voltage. It operates as a source follower with a gain of approximately one and a non inverting behaviour [14]. This improves the stability of the feedback loop because no additional phase shift is introduced and the gain doesn't change with the load current. As shown in the testbench from the section 5.1, an NMOS pass device has much better behaviour regarding the noise suppression. In the case of increase of the load current, the gate-source voltage increases accordingly, thus regulating the constant voltage at the source node. The same procedure happens in case of the ripple at the power supply line, where the gate voltage follows the change in the supply voltage keeping the output voltage constant. Considering the chip area, NMOS pass device requires a smaller area than a PMOS to be able to source the same load current. This is due to the fact that majority carriers-electrons in the NMOS transistor have higher mobility than the holes in the PMOS transistor [14]. Smaller transistor size implies smaller gate-source capacitance and reduces the necessary chip area.

Main drawback of an NMOS pass device is the need for the charge pump circuit to keep its gate-source voltage higher than the threshold voltage of the pass device. This means that the supply voltage cannot fall below the desired output voltage plus the gate-source voltage of the pass device, since the error amplifier feeding the gate of the pass device is limited to this supply and can't pull the gate voltage above it. The solution for this is in the use of a charge pump, which is necessary to achieve low drop-out voltage.

However, the charge pump also comes with significant disadvantages such as additional current consumption, line noise, electromagnetic interference and increase in the chip area.

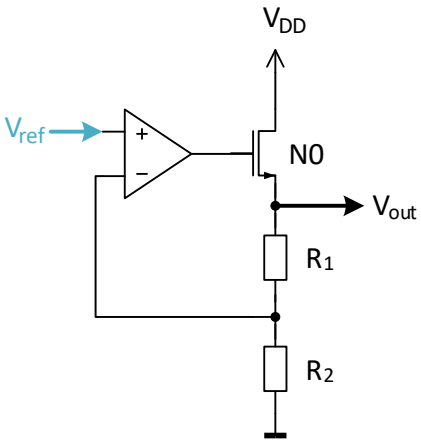


Figure 7: LVR with NMOS pass device

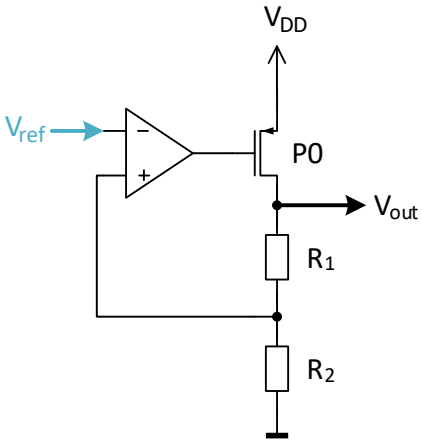


Figure 8: LVR with PMOS pass device

5.3 PMOS as Pass Device

A PMOS pass device requires a negative drive voltage from its gate with respect to the battery cell voltage. In its common source configuration it has more than a unity gain and phase shift, thus any ripple on its drain terminal gets amplified at the source. The noise at the power supply line is sensed directly at the source of the PMOS transistor.

PMOS pass device introduces another gain stage which depends on the output current. Stability is also harder to achieve due to its inverting behaviour. If the low dropout voltage is necessary then the use of the PMOS transistor as pass device is recommended, due to the fact that the input voltage can be as low as output voltage plus the saturation voltage of the pass device. There is no need for the charge pump circuit like for the NMOS pass device.

6 Load and Line Disturbance Profiles

The defined line and load disturbance profiles are related to the dynamic variation of the load current and supply voltage. The profiles have been determined empirically, according to the known disturbances or noises that can occur when the battery is in use.

6.1 Load Current Profiles

One of the main specification for the design of an LVR is a capability of driving a high current load. Every change in the load current will cause a change in the gate-source voltage of the pass transistor, thus invoking the change in the output voltage.
As described in the section 3.1.2, the reaction of the regulator to the change in the load current is defined as the load regulation or load transient response, depending on if it's a static or dynamic change. The rise time of the load current change has the biggest impact on the variation in the output voltage. With the increase in the slew rate and the current, higher peaks appear on the output voltage.
The analysis and simulation of the different LVR topologies is done for several load profiles with different slew rates, described in the figures below. The values of the maximum rise and fall time of the load and line transients, that the control loop of the regulator can follow without exceeding the error margin of the output voltage, differ among the analyzed topologies.

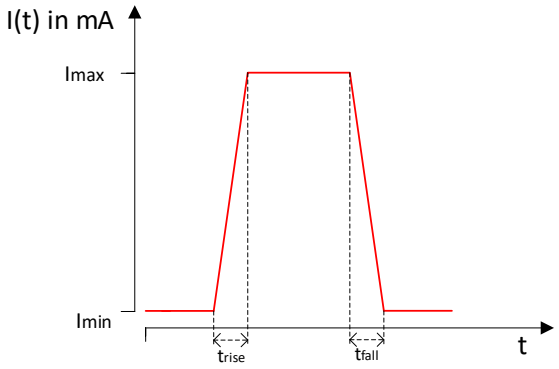


Figure 9: Load current profile - transient jump from minimum to maximum value with undefined rise and fall time

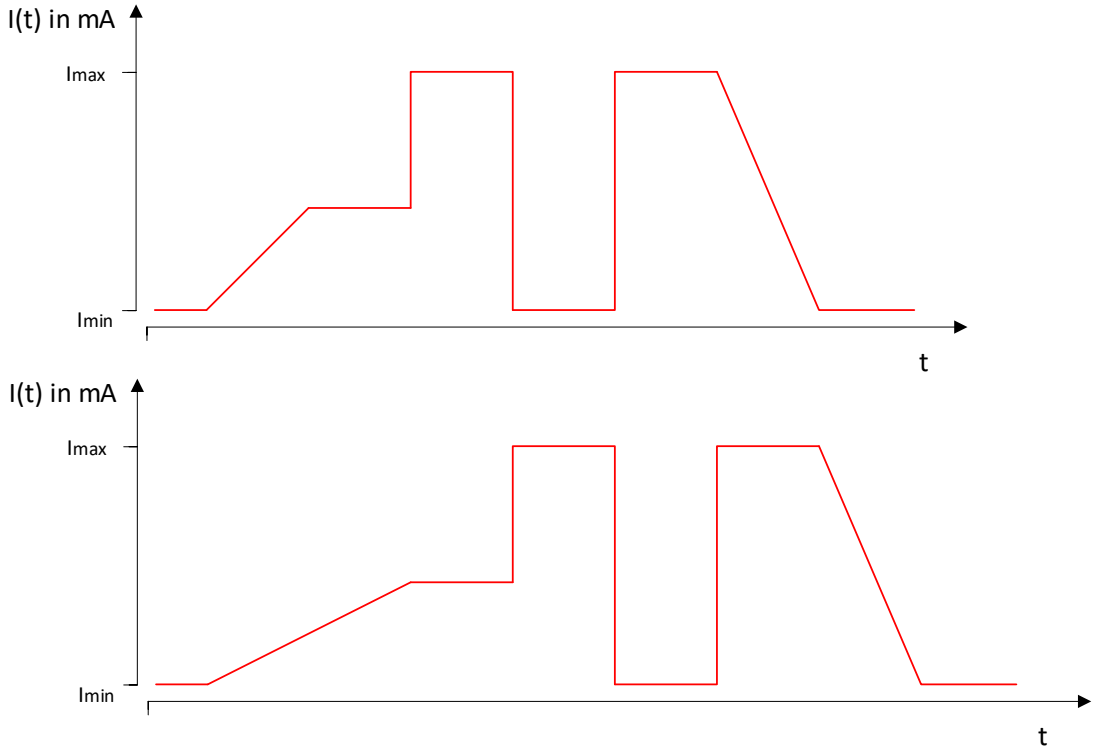


Figure 10: Opposite load current profiles applied to 2 different LVRs with the same supply voltage to investigate the influence among each other

6.2 Digital Load Current Profile

The LVR produces a stable supply voltage for the digital core which operates in the high frequency region. A digital load usually creates large current spikes, which have a lot of impact on the regulator output voltage. For example, if a clock frequency of the digital controller is increased, the large current peaks cause the increase of the average load current producing undershoots in the output voltage, which depend on the output capacitance and the frequency. From the equation 8, it can be seen that the values of such undershoots increase with the average current of the clock tree $I_{avg,clk}$ and decrease with a bigger output capacitor C. On-chip capacitors are usually limited by the chip area. A buffer capacitor which is big enough to minimize the output voltage peaks caused by high digital load transients has to be placed off-chip. Such external capacitor requires one extra pin on the chip and in turn also increases the area and total costs of the chip production.

$$\Delta V_{OUT} = \frac{I_{avg,clk}}{C \cdot f_{clk}} \tag{8}$$

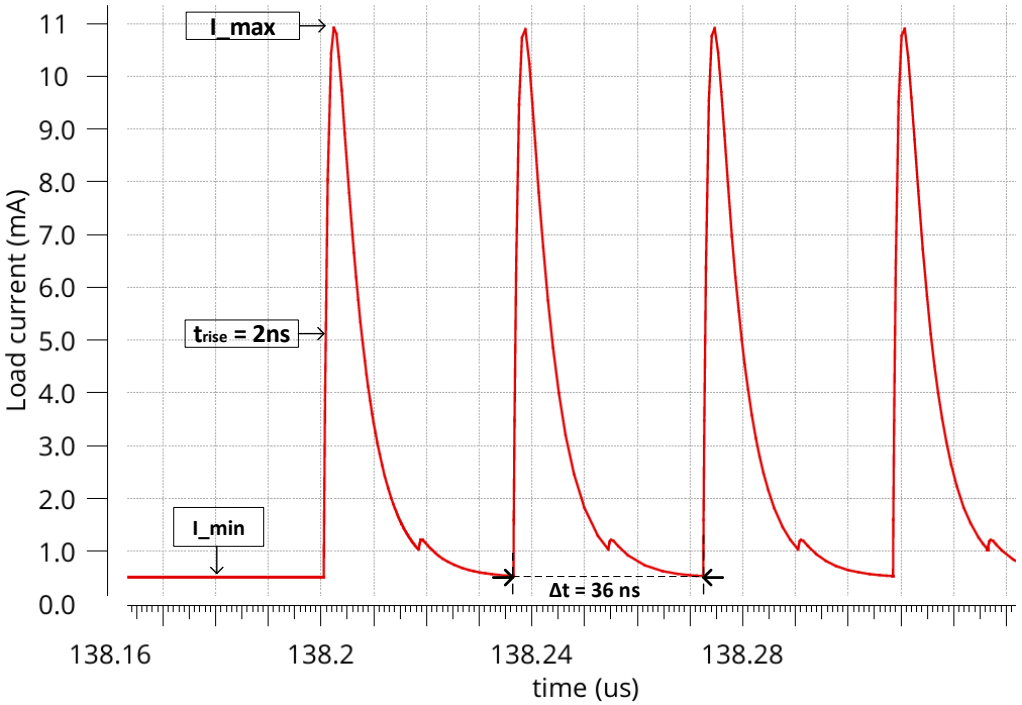


Figure 11: Digital load current profile generated from a clock tree simulation

In order to characterize such a current profile to be able to include it in the simulation with the voltage regulator, another simulation of a particular clock tree is done.
The testbench of the clock tree is built out of a $28\,MHz$ ideal clock pulse and a numerous amount of CMOS buffers supplied by the regulator output voltage. A $100\,\Omega$ resistor and a $500\,pF$ parasitic capacitor are used for the ideal supply voltage decoupling. Generated current profile is analyzed and integrated in the testbench of the regulator using the ideal current source with exponential rise time. This current source was added on the top of the constant DC load current.
The generated current measured at the supply pin showed high peaks during switching and the regulator was tested for the maximum current peak at which the output voltage stays inside the allowed region of $\pm 10\%$ of the nominal value.

6.3 Line Transient Profile

Line transients mostly involve sharp rising pulses or peaks on top of the cell voltage which cause the typical undershoots or overshoots in the output voltage, measured at a constant load. Following figures show the line profiles used for the line transient response analysis. For

example, figure 13 illustrates a possible disturbance profile during the switching of the power transistors with the frequency of $20\,kHz$ when the high current flows through the internal inductance of the battery cell.

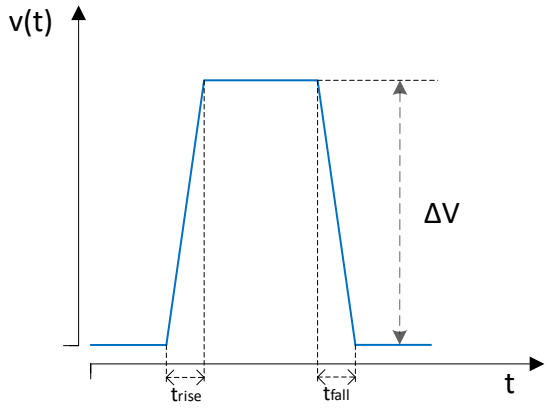


Figure 12: Line transient pulse

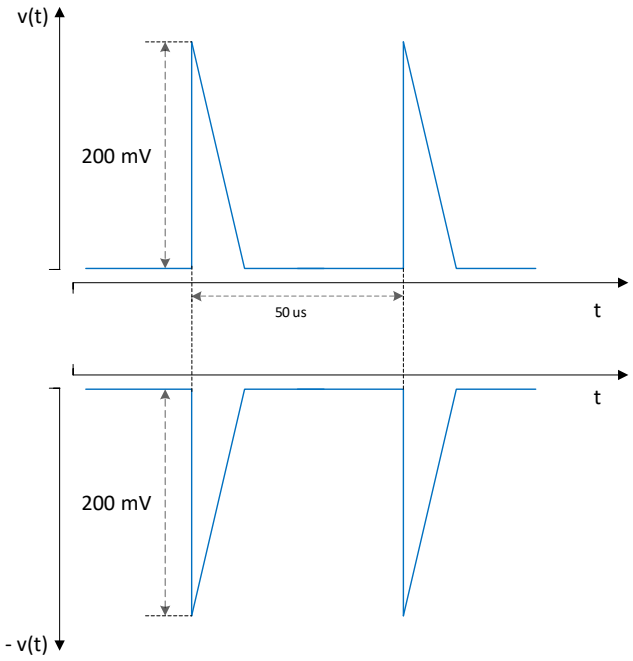


Figure 13: Line transient peaks

7 Analysis of the Different Regulator Topologies

In this chapter different linear voltage regulator topologies are analyzed and compared in order to find the optimum concept which can satisfy the specification and also reduce the area and production costs. The presented designs have been verified for a typical mean point of the process corners through DC, AC and transient simulation at a nominal room temperature of $27°C$, as well as corner analysis for all the process corner models of the resistors, capacitors and transistors (fast-fast (FF), slow-slow (SS), fast-slow (FS), and slow-fast (SF)) for worst case temperatures of minimum $-40°C$ and maximum $120°C$. Random mismatch and process variations have been verified through Monte Carlo simulations for 3 standard deviations away from the mean value (3 sigma).

7.1 LVR with a Medium Voltage (MV) PMOS Pass Device

First supply concept that was analyzed is the typical linear voltage regulator with a PMOS pass device. This topology doesn't require a charge pump and an oscillator which keeps the design process simple. The circuit has been implemented with a medium voltage device which can tolerate drain-source and gate-source voltages higher than the specified input range. In case the load is switched off and the output voltage goes to $0\,V$, the pass device can tolerate the full supply voltage across its drain-source terminals.

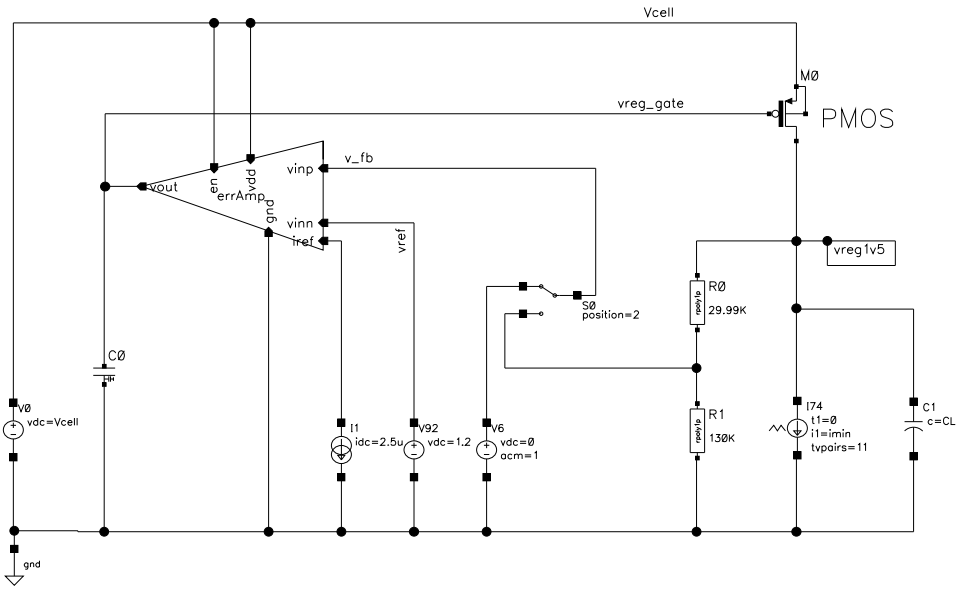


Figure 14: Linear voltage regulator with a medium voltage PMOS pass device

Figure 14 presents the testbench used to characterize the behaviour of this regulator topology. The circuit consists of an error amplifier, PMOS pass device and the resistive feedback dividers. Bias current and reference voltage are derived from ideal voltage and current sources.

A simple symmetrical current mirror operational transconductance amplifier (OTA) from figure 15 is used as an error amplifier. It consists of differential input pair N_1 and N_2 and this differential input is converted to a single ended output via current mirrors. Cascoded form is used in order to increase the gain of the OTA. PMOS pass device in common source configuration is a gain stage itself and it creates an additional pole at lower frequencies.

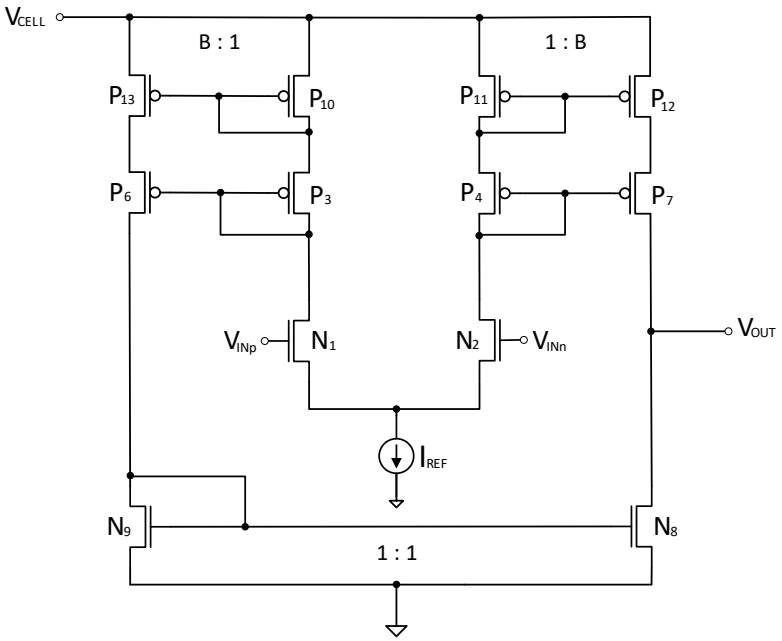


Figure 15: Symmetrical current mirror OTA

The gain of the first stage - OTA is defined as the product of the transconductance of the input stage G_m and the output resistance R_{OUT}:

$$A_{OTA} = G_m \cdot R_{OUT} \tag{9}$$

where $G_m = g_{m1} \cdot B$ and $R_{OUT} = r_{ds8}||(r_{ds12}r_{ds7}g_{m7})$ (the index of the transconductance g_m and drain-source resistance r_{ds} refer to the respective transistor index from the figure 15). $B = 2$ is the current ratio of the input and output branch.

The DC gain of the PMOS pass device can be calculated as:

$$A_{PD} = -g_{m_{PD}} \cdot R_L \tag{10}$$

The overall gain of the system is defined as the product of the gains of the two stages:

$$A_{PD} = -G_m R_{OUT} \cdot g_{m_{PD}} R_L \tag{11}$$

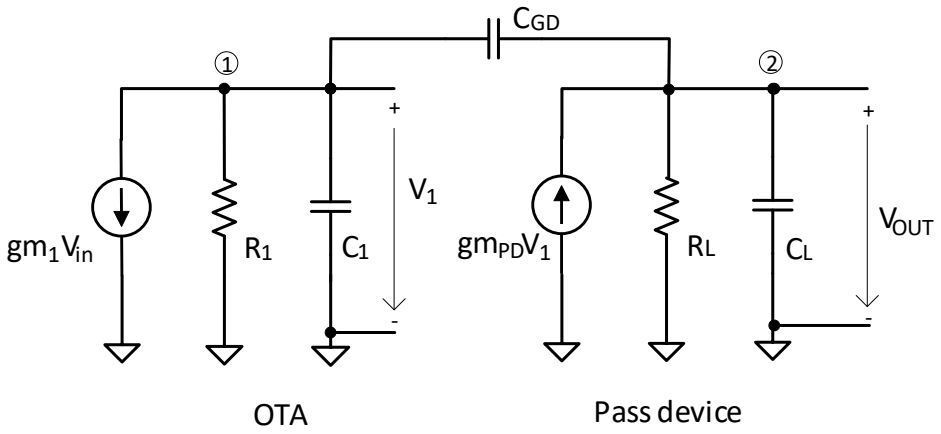


Figure 16: Small signal model of the OTA and the PMOS pass device

From the small signal analysis of the model from figure 16 the dominant pole can be approximated to [13]:

$$p_d = -\frac{1}{C_1 R_1 + C_L R_L + g_{m_{PD}} C_{GD} R_1 R_L} \tag{12}$$

where index numbers of the resistances refer to the overall resistance at the respective nodes. C_1 includes the output capacitance of the OTA and gate-source capacitance of the pass device, $R_1 = R_{OUT}$ is the output resistance of the OTA, R_L is the output resistance of the pass device, and C_L is the load capacitance at the output node of the regulator.
Non-dominant pole from the equation 13 is also approximated according to [13].

$$p_{nd} = -\frac{C_1 R_1 + C_L R_L + g_{m_{PD}} C_{GD} R_1 R_L}{C_L C_{GD} R_1 R_L + C_1 C_L R_1 R_L} \tag{13}$$

Gate-drain capacitance C_{GD} of the pass device creates a right half plane zero $z_{RHP} = \frac{g_{m_{PD}}}{C_{GD}}$.

7.1.1 Simulation Results

To analyze the performances of this design topology and to get the rough estimate of this PMOS pass device for these design specifications, simulations have been performed which showed following results as described below.

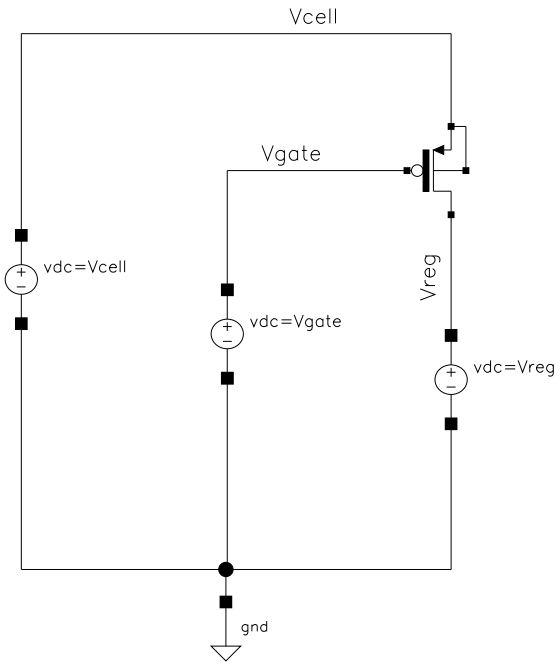


Figure 17: Testbench for the determination of the current capability of the mid-voltage PMOS pass device

For high load currents the pass device has to be large. Varying the width of the pass device over the minimum length, different gate areas can be obtained. Table 3 shows current capability of this PMOS pass device for the testbench from the figure 17. The drain-source current flowing through the pass device can be determined by applying the constant voltages on all terminals of the pass device. Therefore the drain voltage is set to the minimum input voltage $V_{CELL} = 2\,V$, the source is set to the desired output voltage of $V_{REG} = 1.5\,V$, and the gate voltage to $300\,mV$, which represents the minimum saturation voltage of the NMOS transistor N_8 at the output of the OTA from the figure 15. Simulation results over all the process corners show the nominal, minimal and maximal current that this mid-voltage PMOS transistor can deliver for the given conditions. The minimal current I_{min} is measured for slow process corners at the highest temperature of $120°C$, the nominal current I_{nom} for

the typical process corner at $27°C$ and the maximal current I_{max} for the fast corners at the lowest temperature of $-40°C$.

Pass device area	I_{min}	I_{nom}	I_{max}
A_{min}	$3.7\,mA$	$6.5\,mA$	$9.4\,mA$
$1.6A_{min}$	$6.0\,mA$	$10.4\,mA$	$15.0\,mA$
$2A_{min}$	$7.5\,mA$	$13.0\,mA$	$18.8\,mA$
$2.7A_{min}$	$10.2\,mA$	$17.6\,mA$	$25.3\,mA$
$10A_{min}$	$37.7\,mA$	$65.0\,mA$	$93.9\,mA$

Table 3: Current capability of the PMOS pass device over different gate dimensions; A_{min} refers to the gate area obtained for the minimum gate dimensions needed to source a nominal load current larger than $5\,mA$

The chosen area for further analysis of this pass device is $2.7A_{min}$ in order to be able to source load current of minimum $10\,mA$.

AC Simulation Results

The open loop AC analysis is performed to check the stability of the system. The loop is opened at the feedback node and the nominal results at minimum and maximum load current and supply voltage are shown in the figure 18.

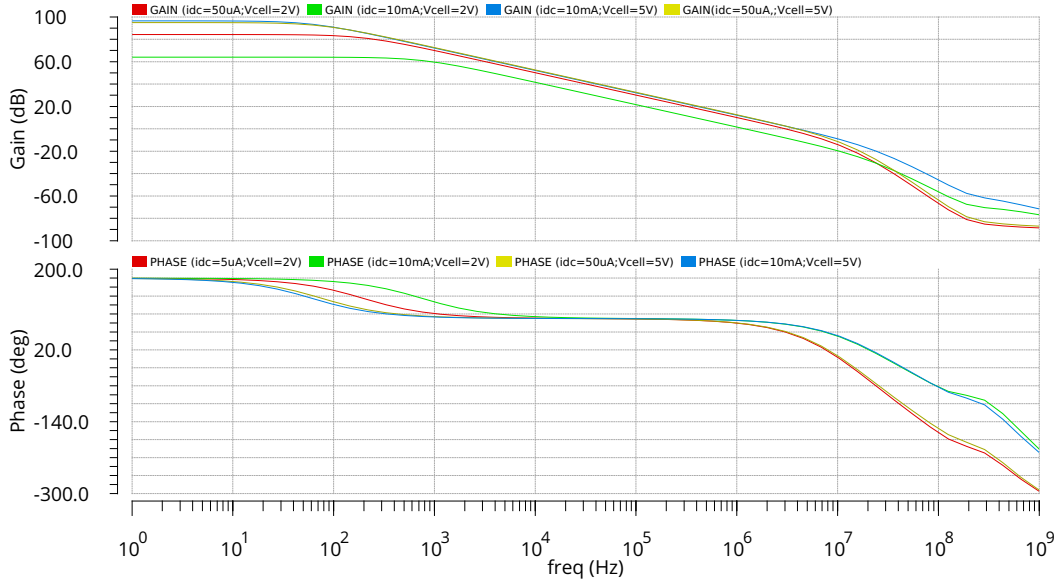


Figure 18: Gain and phase for load current of $50\,\mu A$ and $10\,mA$ at supply voltage $V_{CELL} = 2\,V$ and $V_{CELL} = 5\,V$; nominal run at $\vartheta = 27°C$

After simulation over all process corners with worst case temperatures of $-40°C$ and $120°C$, along with 100 Monte Carlo runs for 3 sigma taking both process and mismatch variations into account, the results have been summarized in the table below. Minimum and maximum values of the AC analysis parameters have been determined for load current of $50\,\mu A$ and $10\,mA$ over the whole supply voltage range. Nominal values in the table 4 refer to two different supply voltages $V_{CELL} = 2\,V$ and $V_{CELL} = 5\,V$.

The open loop gain from the equation 11 depends on transconductance of the pass device and the output resistance. With higher supply voltage, open loop gain increases because of the increase of the drain-source resistance of the pass device. If the load current increases, it causes two effects: increase of the transconductance and decrease of the output resistance, thus for higher supply voltages there is no significant change of the open loop gain. Sourcing the high load current at lower supply voltages causes the pass device to operate near the linear region reducing the gain of the system. On the other hand for lower load current, output resistance increases and moves poles to lower frequencies causing phase margin reduction and instability. For load current lower than $50\,\mu A$, the phase margin is significantly reduced and the system is considered to be unstable.

	Nom @$V_{CELL} = 2\,V$	Nom @$V_{CELL} = 5\,V$	Min	Max	Unit
Gain	84.33	95.00	70.93	97.36	dB
UGF	3.07	4.08	2.72	4.28	MHz
Bandwidth	197.60	77.32	61.04	1.01k	Hz
Phase Margin	59.79	53.49	48.69	65.84	°

(a) Results for minimum load current $I_{LOAD} = 50\,\mu A$

	Nom @$V_{CELL} = 2\,V$	Nom @$V_{CELL} = 5\,V$	Min	Max	Unit
Gain	64.10	96.54	43.09	97.98	dB
UGF	1.24	4.14	1.08	4.36	MHz
Bandwidth	754.40	61.01	54.24	6.53k	Hz
Phase Margin	85.01	74.12	57.07	87.39	°

(b) Results for maximum load current $I_{LOAD} = 10\,mA$

Table 4: Nominal and worst case AC analysis parameters for minimum and maximum load current over the whole supply region

Load Regulation

Static load regulation from zero to maximum load current resulted in the worst case of $\frac{3.1\,mV}{10\,mA}$ change in the output voltage over all process corners and worst case temperatures at the supply voltage of $V_{CELL} = 2V$. The results are presented in the figure 19.

A PMOS pass device has generally worse dynamic load regulation than an NMOS, as described in the section 5.1. Output voltage response to the current profile from figure 20 with rise time of $10\,\mu s$ from $500\,\mu A - 10\,mA$ resulted in peaks smaller than $\pm 10\%$ of the nominal output value. For shorter rise and fall times or smaller minimum current, the peaks exceed the allowed region, due to the slow loop response of the regulator. The worst case over- and undershoots are noted for slow process corners at the $120°C$ temperature, which stay in the region of $\pm 10\%$ of the nominal output voltage.

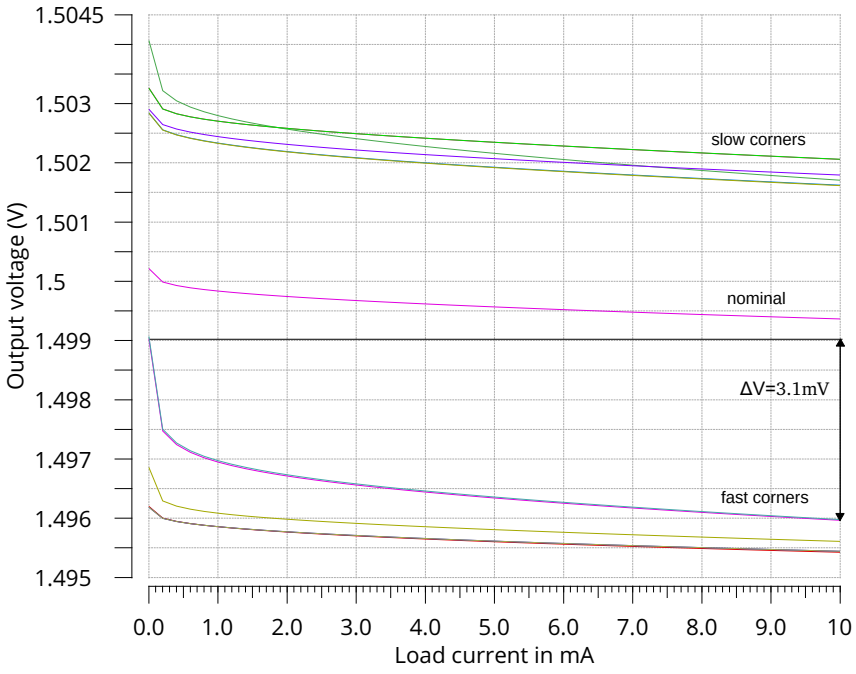


Figure 19: Static load current regulation of PMOS LVR for $V_{CELL} = 2\,V$; typical and all process corners, $\vartheta = -40°C; 27°C; 120°C$

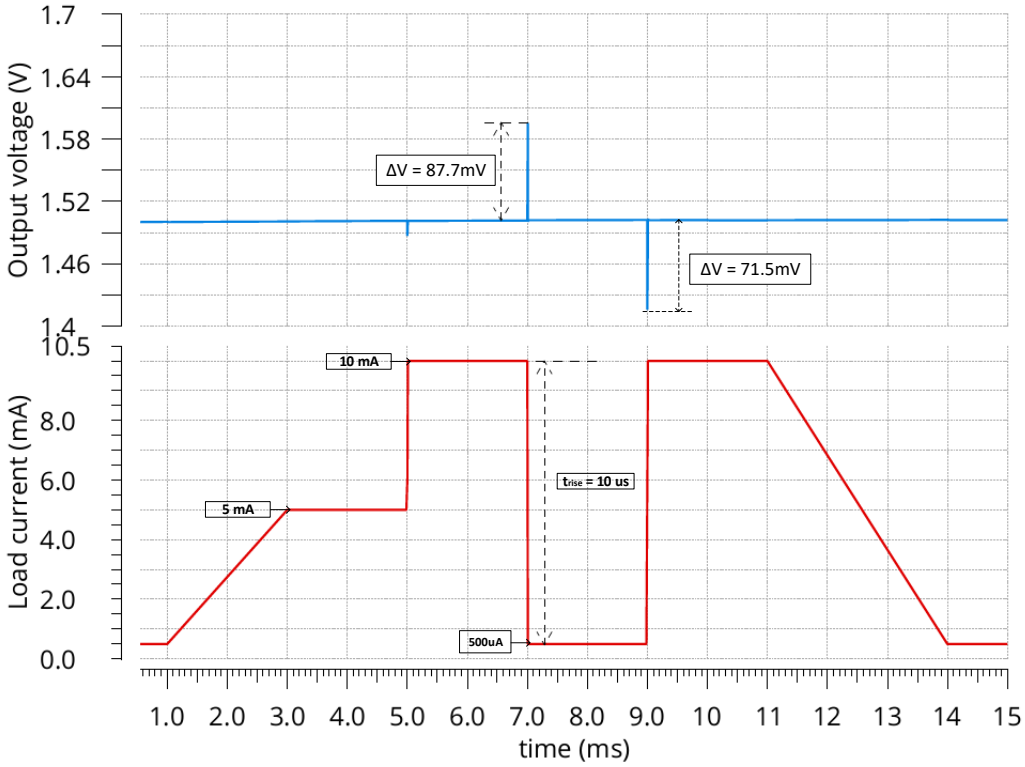


Figure 20: Dynamic load regulation of PMOS LVR for $V_{CELL} = 2\,V$; typical process corners

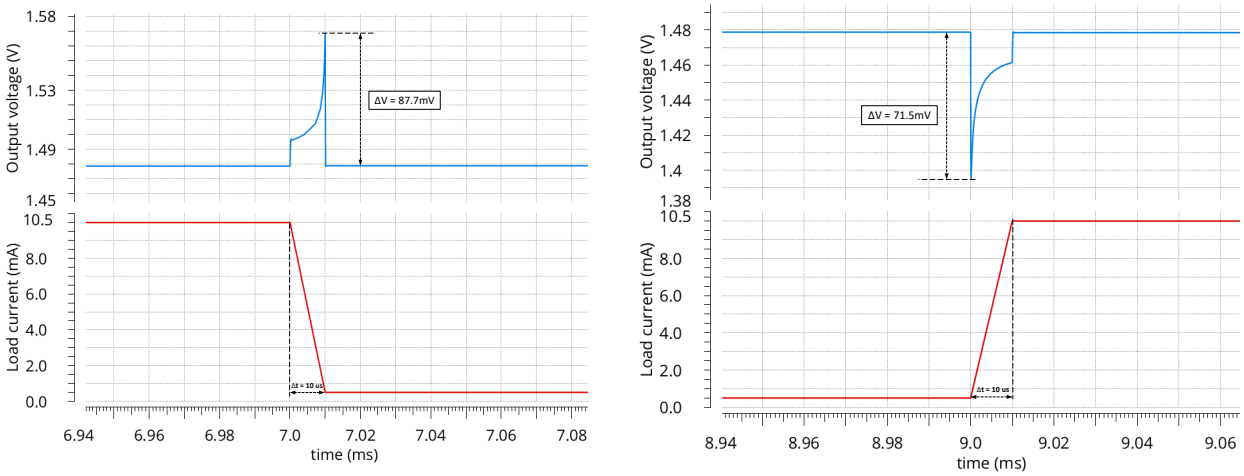


Figure 21: Zoomed peaks of the output voltage at the falling and rising edge of the load current profile from figure 20

Line Regulation

Static line regulation for $V_{CELL} = 2V - 5V$ at the load current of $1\,mA$ show maximum $\frac{4.6\,mV}{3\,V}$ for worst case process corner. The results are presented in the figure 22. For a typical corner at higher supply voltage the line regulation is improved to $740\frac{\mu V}{V}$.

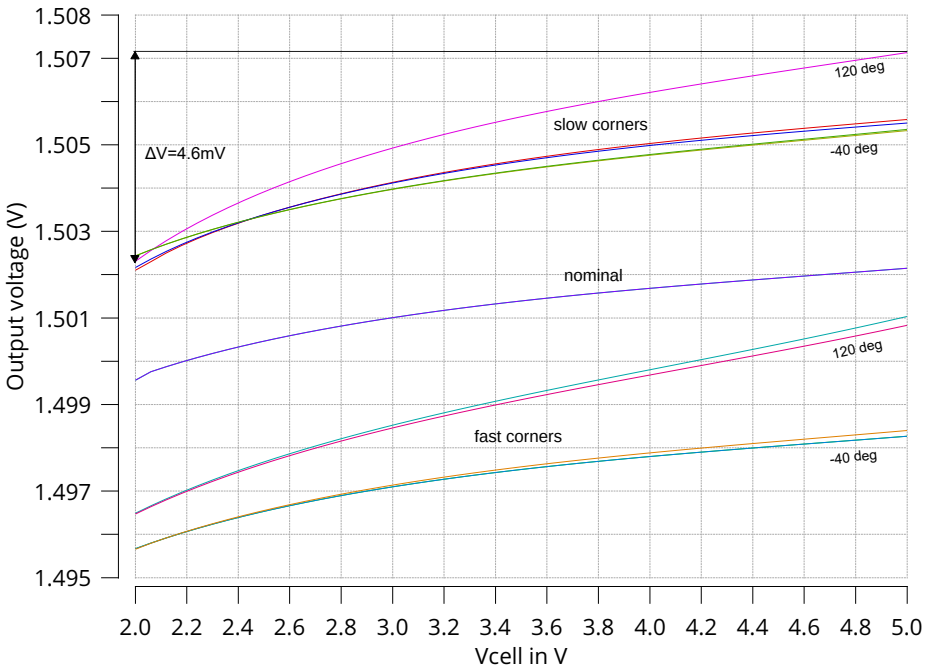


Figure 22: Static line regulation of PMOS LVR for $V_{CELL} = 2\,V$; typical and all process corners, $\vartheta = -40°C, 27°C, 120°C$

Dynamic line regulation for $\Delta V_{CELL} = 200\,mV$ in $2\,\mu s$ for all process corners is plotted in the figure 23. The highest over- and undershoot occurs during slow process corner at $-40°C$. Due to the instability of the analyzed linear voltage regulator with the PMOS pass device for lower load current, the further analysis is concentrated on the NMOS pass device.

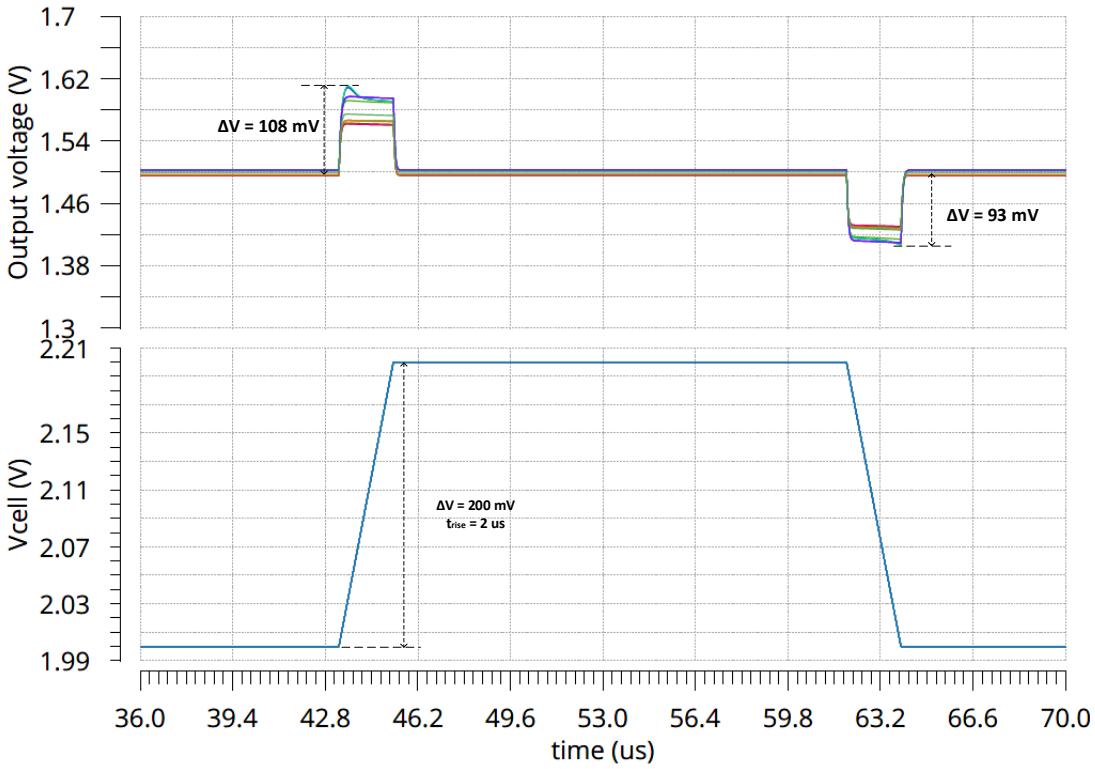


Figure 23: Dynamic line regulation of PMOS LVR for $\Delta V_{CELL} = 200\,mV$ in $2\,\mu s$; typical and all process corners, $\vartheta = -40°C; 27°C; 120°C$

7.2 Cascoded Topology - Introduction of the Pre-regulator Circuit

In this section a low voltage triple well NMOS pass device is analyzed and its boundary conditions and performances that can be achieved without the charge pump circuitry for the given specifications. Triple well process uses deep n-well to isolate p-well from p-substrate, which benefits in reduced substrate noise coupling. Body and deep n-well can therefore be biased separately, which also reduces the body effect and the increase in the threshold voltage of the pass device. [15]

7.2.1 Circuit Description

A schematic of this regulator topology is depicted in Figure 24 and it consists of two regulation loops stacked on top of each other.

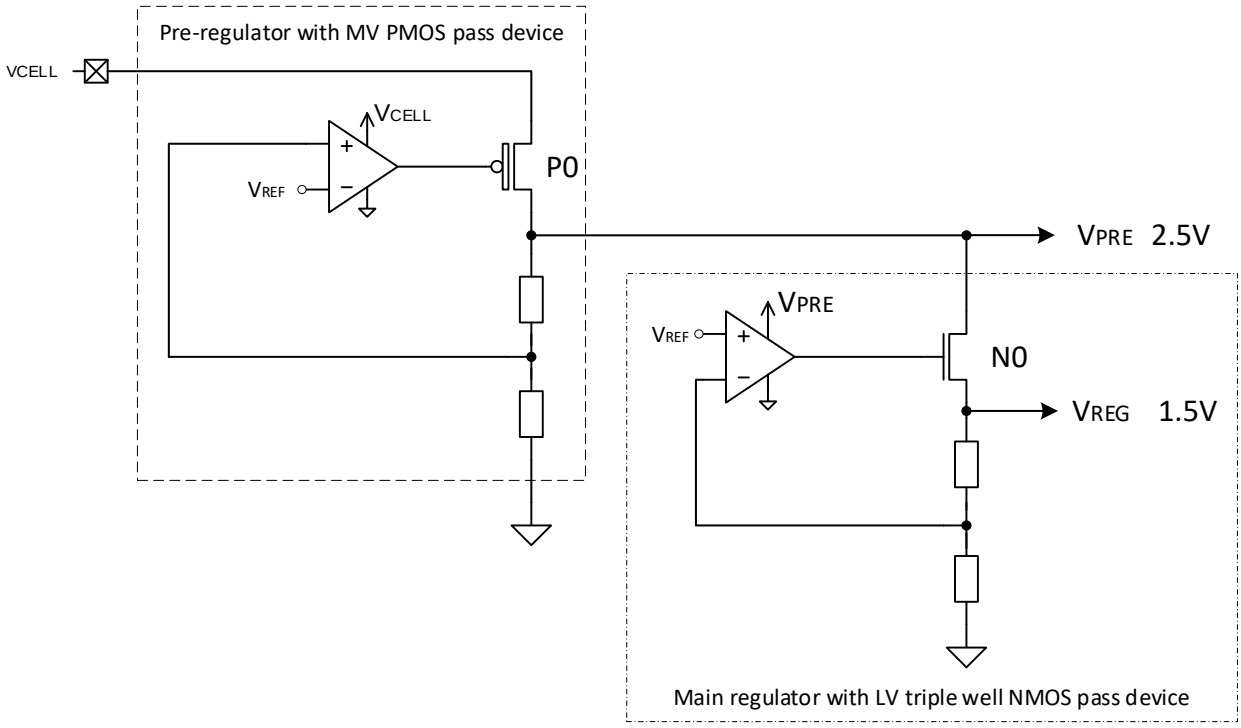


Figure 24: Stacked architecture of LVRs

Due to the dynamic supply voltage, the breakdown range of the low voltage (LV) NMOS pass device is exceeded, so a stacked architecture employing a pre-regulator is used. The main regulator uses low voltage triple well NMOS pass device. The voltage regulator with a mid-voltage (MV) PMOS pass device analyzed in the chapter 7.1 is used as a pre-regulator. It regulates the battery cell voltage V_{CELL} to a stable voltage with the nominal value of $V_{PRE} = 2.5\,V$.
This way the main regulator sees less variations on its drain terminal. For further improvement of the power supply rejection, the error amplifier of the main regulator is also supplied by the pre-regulator output voltage.

7.2.2 Pre-regulator with MV PMOS Pass Device

The testbench from the figure 17 and the results presented in the table 3 show that this pass device has to be large in order to source the high load current. Considering a low input voltage of $V_{CELL} = 2\,V$, there is not enough voltage headroom available for this device to operate in saturation region, thus it acts as a switch, passing the cell voltage onto the drain of the main regulator's pass transistor. For the purpose of analyzing the performances of this regulator topology, a big PMOS pass device with $10A_{min}$ is chosen.
Dropout voltage simulation over current load range from $0 - 15\,mA$ showed worst case result of maximum $84\,mV$ for slow corners at $-40°C$ and $V_{CELL} = 2\,V$. This means that the regulated voltage V_{PRE} can drop to min $1.916\,V$ in the worst case corner.

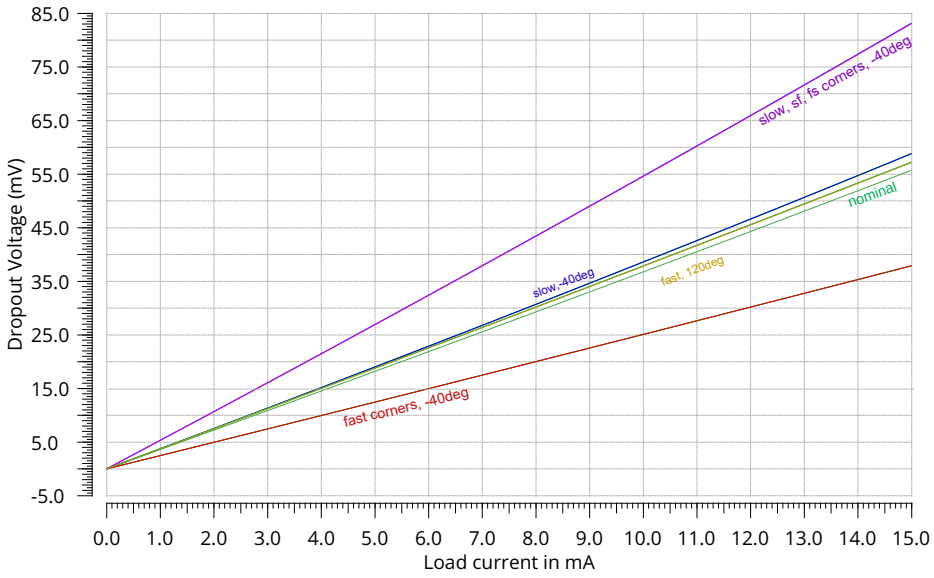


Figure 25: Dropout voltage of the pre-regulator over load current, nominal and all process corners, $\vartheta = -40°C; 27°C; 120°C$

7.2.3 Main Regulator with LV Triple Well NMOS Pass Device

The testbench from figure 26 is taken for the analysis of the main regulator. The ideal voltage controlled voltage source with high gain is used as an error amplifier and the supply voltage is set according to the output voltage of the pre-regulator V_{PRE}. If the maximum dropout voltage of $84\,mV$ for the pre-regulator is taken into account and the maximum voltage at the gate of the NMOS is limited to approximately one saturation voltage below the $V_{PRE} = 1.916\,V$, the following results are obtained.

From the figure 27 it can be seen that the main regulator output voltage V_{REG} is significantly reduced for the slow corners at low temperatures, due to the increase in the threshold voltage of the pass device.

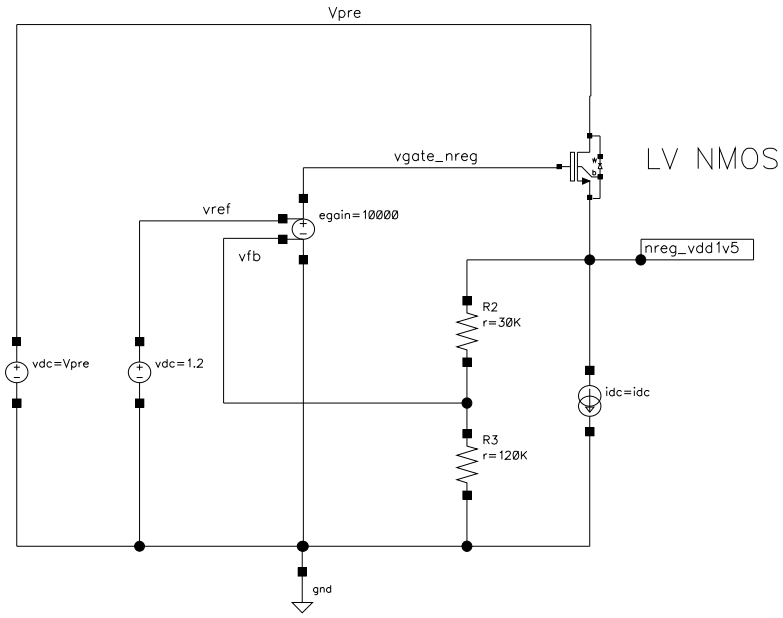


Figure 26: Testbench for the simulation analysis of the main regulator

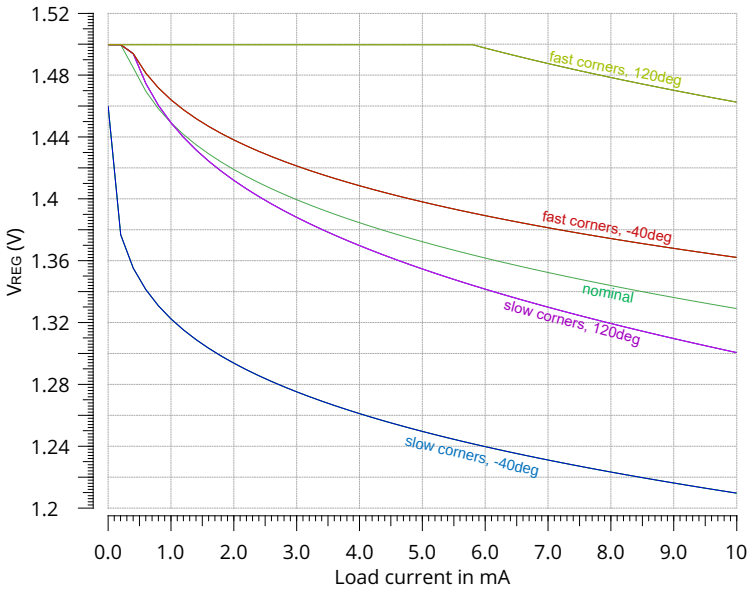


Figure 27: Main regulator output voltage over load current at $V_{CELL} = 2\,V$, nominal and all process corners, $\vartheta = -40°C; 27°C; 120°C$

This clearly shows that for this boundary conditions there is not enough voltage headroom for the proper output voltage regulation. Therefore further analysis was done by using a charge pump to increase the gate voltage of the NMOS pass device.

7.3 Cascoded Topology using Low-Voltage Devices

This concept is designed by stacking three low-voltage transistors on top of each other, where the first one acts as a PMOS switch, the second one as an NMOS pass device of the main regulator and the third one as an NMOS pass device of the pre-regulator. The previous analysis showed that the charge pump is necessary for this structure, so the design optimization in this case can be concentrated on area reduction in the form of using low voltage devices with smaller gate-oxide thickness, which is preferable due to the lower costs, but it also implies taking precautionary measures not to exceed the breakdown voltage of every single device. Therefore the battery cell voltage needs to be adapted to a voltage level which can then be used as a supply for blocks used in the circuit. The differences to the pre-regulator topology from the chapter 7.2 is that the PMOS pass device is replaced by another triple well low voltage NMOS pass-device.

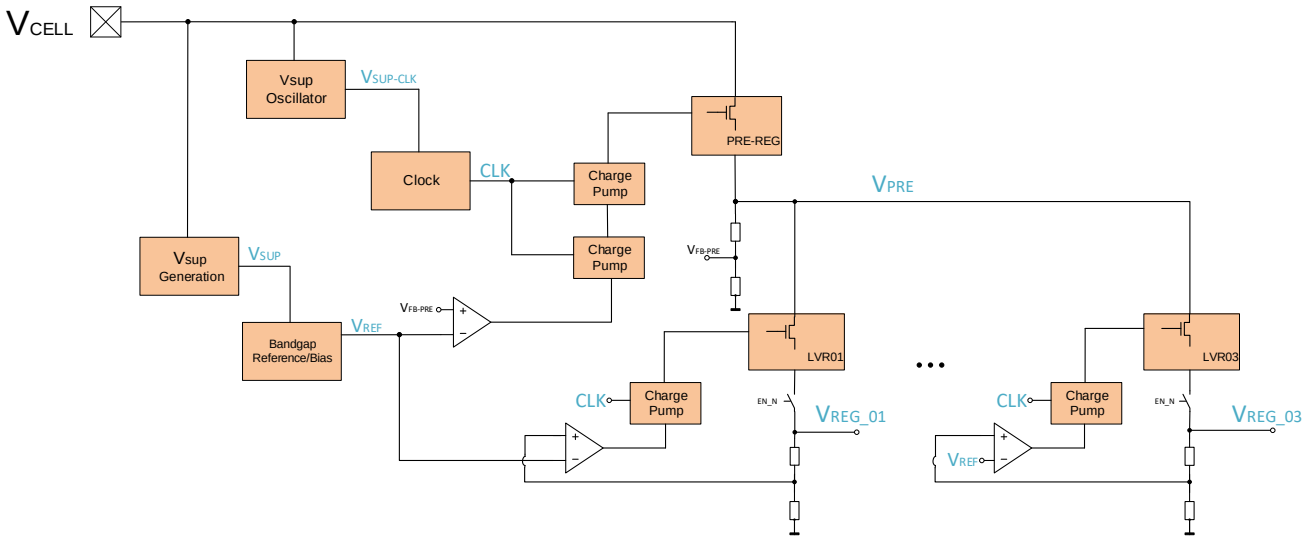


Figure 28: Block diagram of the new concept. Error amplifiers are supplied by the voltage V_{SUP}. Three main regulators LVR01-LVR03 are supplied by the pre-regulator output V_{PRE}.

7.3.1 Circuit Description

This initial design topology used only the main regulator with the NMOS pass device and a PMOS switch in series, where the switch is used to prevent the drain-source voltage of the pass device from exceeding the breakdown voltage. If the load is switched off, then the battery cell voltage is divided between the pass device and the switch. Simulation results of

such a concept showed high peaks at the drain-source voltage of the main pass device while load is switching on and off.

To insure that the voltages stay inside the safe operating range, another pre-regulator is added to the circuit, using low-voltage NMOS pass device which keeps the drain voltage of the main regulator stable.

The design specifications listed in the table 1 are also valid for this concept.

Figure 28 shows a block diagram of this voltage regulator topology. It includes a block for the supply voltage generation V_{SUP} of the internal bandgap reference voltage V_{REF}, another block used as the supply for the clock circuitry $V_{SUP-CLK}$, one pre-regulator with the output voltage V_{PRE}, three main voltage regulators with output voltages V_{REG_01-03}, charge pumps and the clock generation circuitry.

The schematic of the bias generation blocks V_{SUP}, V_{REF} and I_{REF} is included in the appendix C.

7.3.2 Supply Voltage Generation - V_{SUP}

To generate an internal supply voltage from the battery cell voltage V_{CELL}, suitable for supplying bandgap circuit, error amplifiers and other supporting blocks built with low-voltage devices, a circuit depicted on the figure 29 is designed.

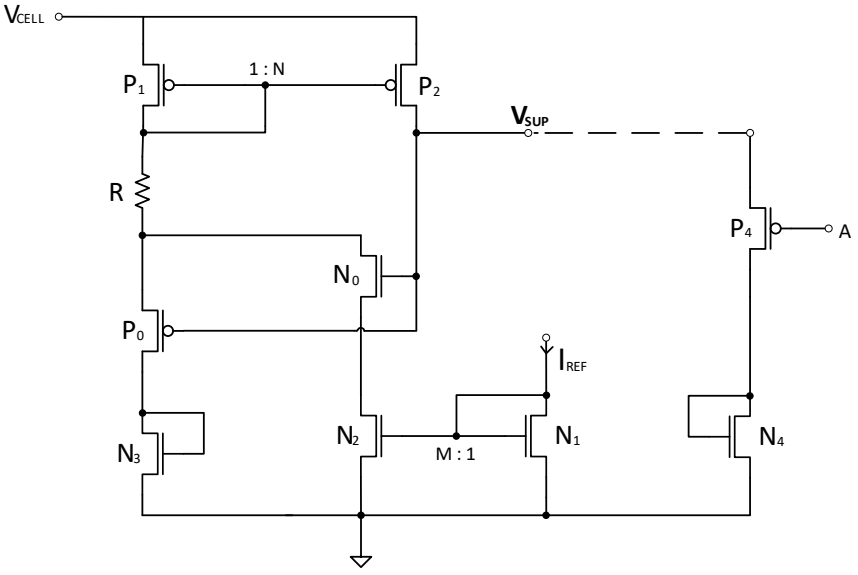


Figure 29: V_{SUP} voltage generation circuit

The circuit consists of a PMOS current mirror P_1 and P_2, one PMOS P_0 and one NMOS transistor N_0 that control the current which is being copied, and a resistor R for the current limitation. The feedback path is taken from the output of the amplifier of the bandgap circuit. That output node A is connected to the gate of the PMOS transistor P_4 with diode connected load N_4. The NMOS current mirror at the source of N_0 mirrors the constant $PTAT$ current generated in the bandgap block. Different mirroring ratio M sets the maximum current flowing through N_0 and limits the value of the generated voltage V_{SUP} which is connected to the gates of the two controlling transistors N_0 and P_0. If the voltage V_{SUP} increases for higher cell voltage, the transistor N_0 takes over the current control through the PMOS current mirror, keeping the constant V_{SUP}. In the other case that V_{SUP} decreases for lower cell voltage, the transistor P_0 conducts and adds more current to the PMOS current mirror, thus in turn increasing the voltage V_{SUP}.

The most significant disadvantage of this approach is low efficiency due to the fact that the current through the resistor R is increasing the overall current consumption. Therefore the resistor should be high-ohmic and in this case the value was set to $10\,M\Omega$.

Figure 30 presents V_{SUP} as a function of the battery voltage V_{CELL} for a nominal simulation at a temperature of $27°C$ including all the process corners for worst case temperatures. The worst case values are summarized in the table 6.

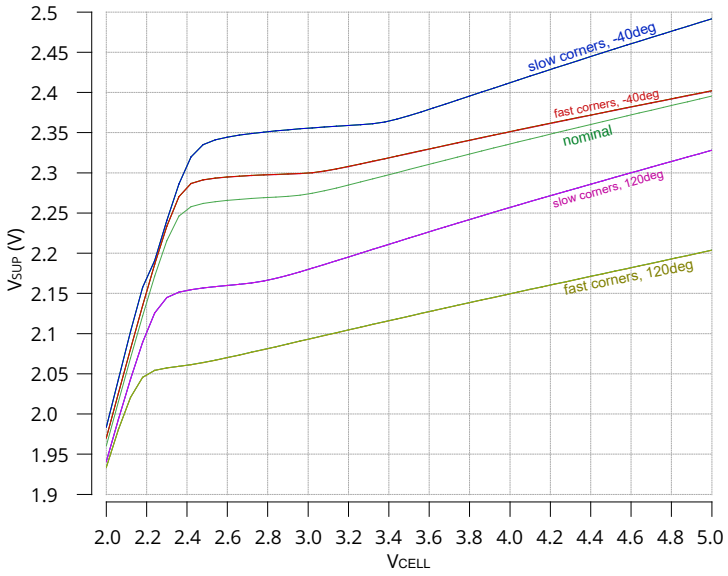


Figure 30: V_{SUP} as function of the battery voltage, nominal result at $\vartheta = 27°C$ and all process corners, $\vartheta = -40°C, 120°C$

7.3.3 Bandgap Voltage Reference - V_{REF}

One of the main blocks of a linear voltage regulator is the bandgap voltage reference. The output of this block is a stable, temperature- and supply voltage independent voltage reference of approximately $1.2\,V$ which is close to the silicon energy gap voltage at a temperature of $0°K(1.22\,eV)$. [20]

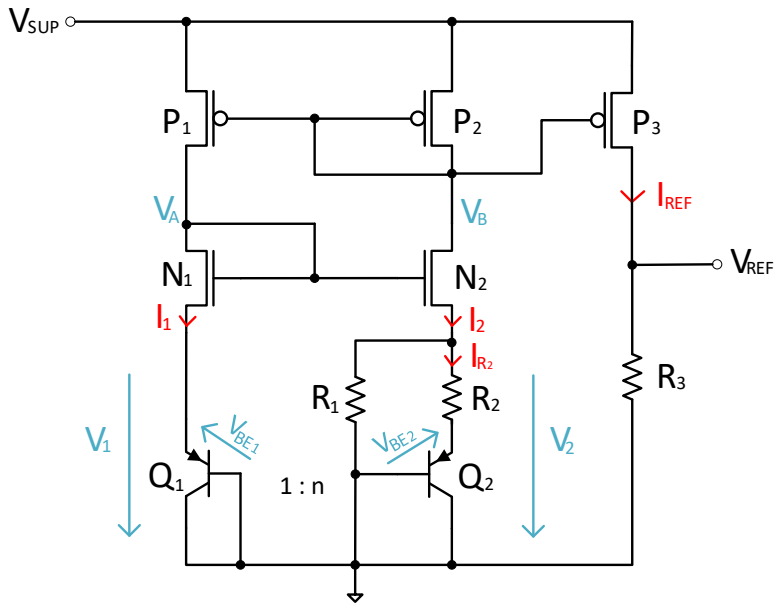


Figure 31: Bandgap core circuit

The bandgap core circuit depicted in figure 31 is designed analog to [6] and its main parts are the two diode connected bipolar junction transistors Q_1 and Q_2 with different emitter area ratios n. Theoretically the base-emitter voltage V_{BE} of the pn-junction is temperature dependent with a temperature coefficient of approximately $-2.2\frac{mV}{K}$ at room temperature and it is therefore called $CTAT$ (complementary to absolute temperature), due to the fact that the voltage decreases with increasing temperature. Summing the $CTAT$ voltage with the thermal voltage V_T (equation 15) which is proportional to absolute temperature ($PTAT$) mulitplied by the constant coefficient produces an output voltage that is independent of the temperature and power supply changes. [12]
This voltage V_{REF} is used as a precision voltage reference to feed the error amplifier of the voltage regulator and also for some biasing of the supporting circuitry.

$$V_{REF} = V_{BE} + K \cdot V_T \tag{14}$$

K is the gain coefficient, which the designer can choose in order to achieve zero temperature coefficient and it can be adjusted with the values of the resistors and the emitter area ratios of Q_1 and Q_2.

$$V_T = \frac{kT}{q} \tag{15}$$

T is the absolute temperature, k is the Boltzmann's constant($1.38 \cdot 10^{-23} J/^\circ K$) and q is a magnitude of electron charge. [6]
Assuming that the voltages V_1 and V_2, as well as the currents I_1 and I_2 are equal (under consideration that the N_1 and N_2 are equal and have the same gate-source voltages), we can define the following equations [6]:

$$\begin{aligned} V_1 &= -V_{BE_1} \\ V_2 &= I_{R_2} \cdot R_2 - V_{BE_2} \end{aligned} \tag{16}$$

Since $V_1 = V_2$ then the voltage across the resistor R_2 is defined as:

$$I_{R2} \cdot R_2 = V_{BE_2} - V_{BE_1} = \Delta V_{BE} \tag{17}$$

This voltage ΔV_{BE} presents the difference between two pn-junctions voltages and is defined in equation 18, where n is the ratio of the emitter areas of the two bipolar junction transistors (the popular designer's choice is $n = 8$). [6]

$$\Delta V_{BE} = V_t \cdot ln(\frac{n \cdot I_1}{I_{R2}}) \tag{18}$$

According to this we can assume that the ΔV_{BE} is also a $PTAT$ voltage because it is proportional to the thermal voltage V_T, and a current through R_2 is a $PTAT$ current:

$$I_{R_2} = I_{PTAT} = \frac{V_t}{R_2} ln(\frac{n \cdot I_1}{I_{R_2}}) \tag{19}$$

The voltage across the resistor R_1 is equal to $\mid V_{BE_1} \mid$ and therefore the current through R_1

is a $CTAT$ current.

$$I_{R_1} = \frac{V_{BE_1}}{R_1} \tag{20}$$

Using the right gain factor K and summing the $PTAT$ and $CTAT$ currents results in a temperature independent current reference I_{REF} which is then mirrored by the current mirror P_2-P_3 to the output stage producing a stable voltage reference V_{REF} across the resistor R_3 [6]. This voltage is used as an input for the error amplifier and compared to the feedback voltage of the regulator.

$$V_{REF} = (I_{PTAT} + I_{R_1})R_3 = [\frac{V_t}{R_2} ln(\frac{n \cdot I_1}{I_{R_2}}) + \frac{V_{BE_1}}{R_1}]R_3 \tag{21}$$

Another advantage of this circuit is that the reference current I_{REF} can be used for further biasing.

The whole bandgap reference block together with the amplifier and the startup circuit is depicted in the figure 32.

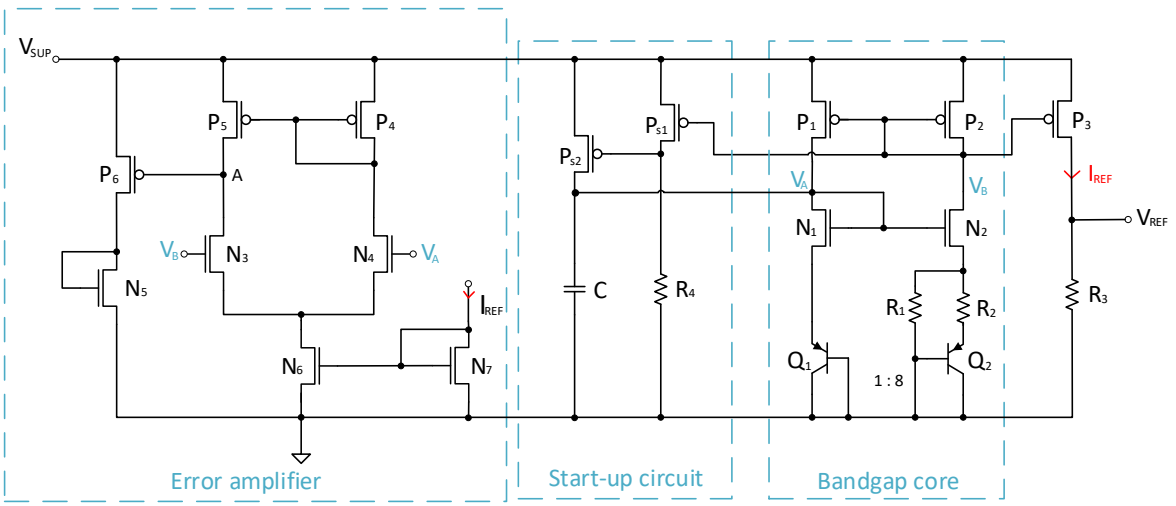


Figure 32: Bandgap voltage reference block

Next part of the bandgap block is the *start-up circuit* with an operational amplifier based on the similar topology presented in [7].

Transistors P_{s_1} and P_{s_2} together with a resistor R_4 we can see on Figure 32 are building the start-up block for the bandgap core. The capacitors are added for the voltage stabilisation. If the voltage V_B is at high level and the gate-source voltage of P_{s_1} is lower than the thresh-

old voltage, then the gate voltage of P_{s_2} is low enough to turn the transistor on and charge the capacitor C increasing the voltage V_A. At the low level of the voltage V_B, the gate of the transistor P_{s_1} is pulled down until the transistor starts conducting, increasing the gate voltage of P_{s_2}, which in turn decreases the voltage V_A, ensuring that V_A equals V_B.

Simulation Results of the Bandgap Circuit

Table 5 shows the values of components used in the bandgap core circuit, determined by a nominal DC sweep for an output reference voltage $V_{REF} = 1.2\,V$ at an input voltage of $2\,V$ and a temperature of $27\,°C$.

Components	Values	Unit
n	8	
R_1	1	$M\Omega$
R_2	112	$k\Omega$
R_3	880	$k\Omega$
R_4	10	$M\Omega$
C	400	fF

Table 5: Components values of the bandgap circuit

Cell voltage variations inside the specified range from $2\,V$ to $5\,V$ from figure 33 show nominal (for $27\,°C$) and worst case values of the variation of the reference voltage for all process corners and worst case temperatures.

Temperature sweep from $-40\,°C$ to $120\,°C$ for the supply voltage of $V_{CELL} = 2\,V$ depicted in figure 34 shows worst case variation of the reference voltage of approximately $5.65\,mV$ over all process corners. These variations can be explained by the influence of the current gain between the base and collector current, the base resistance of the bipolar junction transistors, resistor spread and offset of the amplifier. [5]

The generated reference current I_{REF} shows minimum variations due to change in the supply voltage. The biggest deviations occur among the slow and fast process corners, due to the change in the carrier mobility.

Mean, minimum and maximum values of the internal supply voltage V_{SUP}, bandgap voltage and current reference V_{REF} and I_{REF} for the Monte Carlo simulation for 3 sigma over 200 runs for all variations including corner simulation are summarized in the table 6.

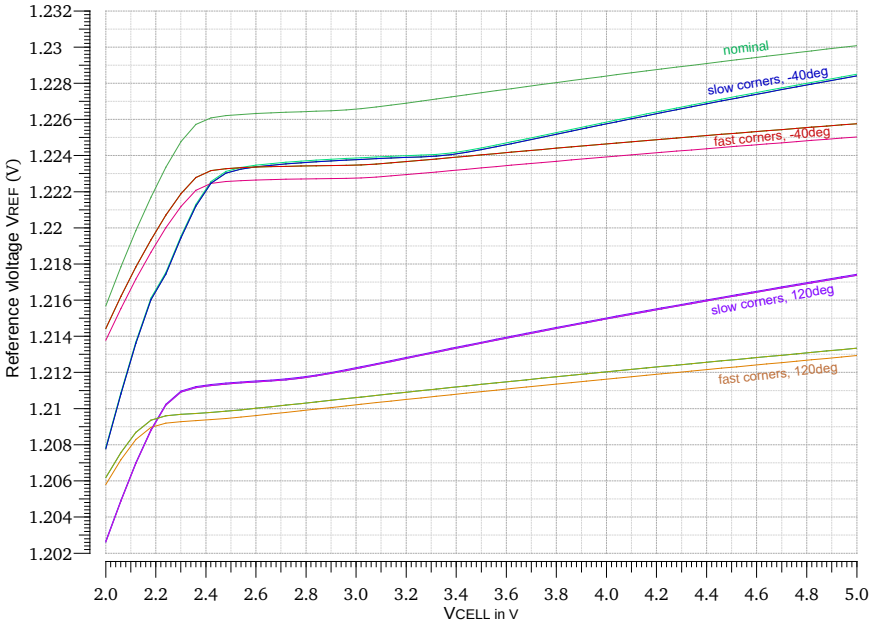


Figure 33: Reference voltage as function of supply voltage for nominal and all process corners, $\vartheta = -40°C, 120°C$

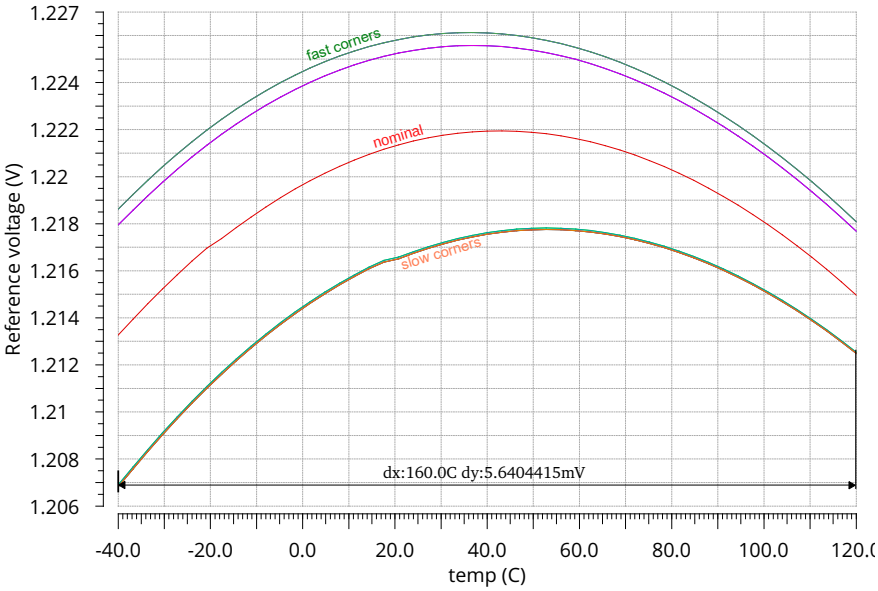


Figure 34: Temperature sweep of the bandgap reference voltage

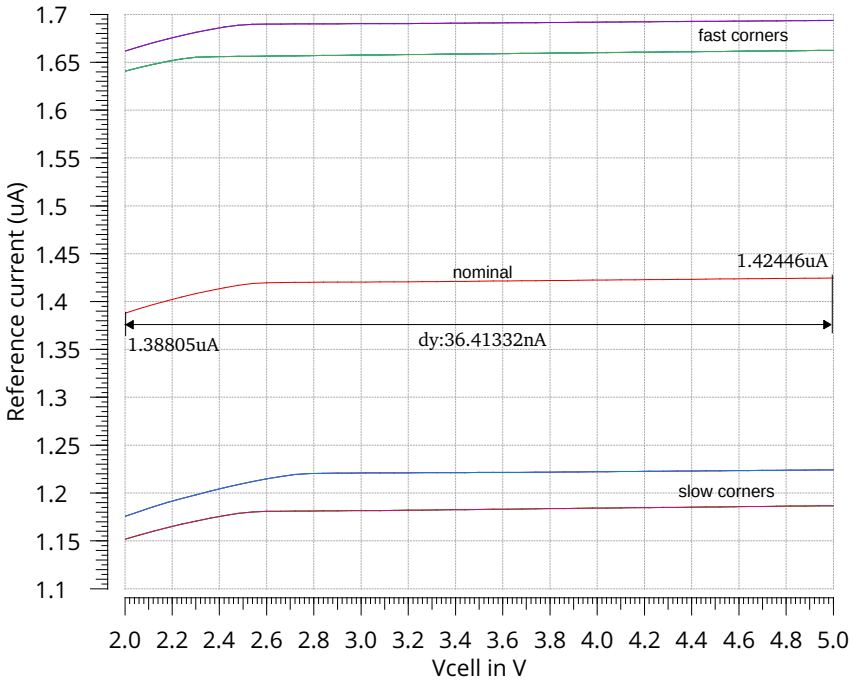


Figure 35: Reference current as a function of the supply voltage

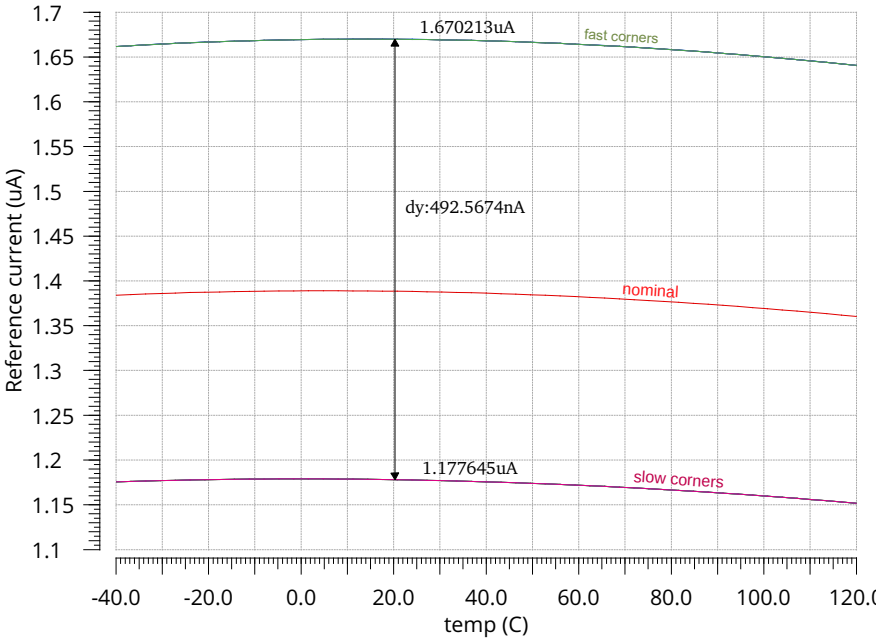


Figure 36: Reference current as a function of the temperature

	Min	Nom	Max
V_{SUP} @$V_{CELL} = 2\,V$	$1.934\,V$	$1.961\,V$	$1.984\,V$
V_{SUP} @$V_{CELL} = 5\,V$	$2.204\,V$	$2.369\,V$	$2.492\,V$
V_{REF} @$V_{CELL} = 2\,V$	$1.203\,V$	$1.216\,V$	$1.216\,V$
V_{REF} @$V_{CELL} = 5\,V$	$1.213\,V$	$1.230\,V$	$1.230\,V$
I_{REF} @$V_{CELL} = 2\,V$	$1.143\,\mu A$	$1.381\,\mu A$	$1.656\,\mu A$
I_{REF} @$V_{CELL} = 5\,V$	$1.157\,\mu A$	$1.398\,\mu A$	$1.672\,\mu A$

(a) Corner simulation results including worst case temperatures

	Min	Mean	Max	Std Dev
V_{SUP} @$V_{CELL} = 2\,V$	$1.952\,V$	$1.960\,V$	$1.968\,V$	$3.495\,mV$
V_{SUP} @$V_{CELL} = 5\,V$	$2.295\,V$	$2.393\,V$	$2.553\,V$	$48.49\,mV$
V_{REF} @$V_{CELL} = 2\,V$	$1.147\,V$	$1.216\,V$	$1.308\,V$	$30.71\,mV$
V_{REF} @$V_{CELL} = 5\,V$	$1.158\,V$	$1.230\,V$	$1.327\,V$	$31.80\,mV$
I_{REF} @$V_{CELL} = 2\,V$	$1.254\,\mu A$	$1.382\,\mu A$	$1.529\,\mu A$	$61.06\,nA$
I_{REF} @$V_{CELL} = 5\,V$	$1.266\,\mu A$	$1.399\,\mu A$	$1.551\,\mu A$	$62.90\,nA$

(b) Monte Carlo mismatch and process variations

Table 6: Summary of the mean and worst case values for V_{SUP}, V_{REF} and I_{REF} for $V_{CELL} = 2\,V; 5\,V$ - Monte Carlo and corner simulation results

The values from the table 6 show that the bandgap reference voltage has less deviation for the process corner and temperature variations, while on the contrary, local device mismatch and global process tolerances have more influence on it. The internal supply voltage V_{SUP} depends mostly on the supply voltage V_{CELL}, while the process, temperature and mismatch deviations are in this case negligible. The important case is that the V_{SUP} is still high enough to be able to supply the rest of the circuit blocks at low battery cell voltage, and that it doesn't exceed the voltage breakdown of the devices at the high cell voltage. The reference current I_{REF} is more sensitive to process corner and temperature variations than to the local device mismatch, because here the dimensions of the devices are increased keeping the same W/L ratio in order to reduce the mismatch according to the Pelgrom's law, which claims that the mismatch is inversely proportional to the gate area [11]. So for example, the standard deviation of MOS threshold voltage V_T is defined as:

$$\sigma^2_{\mathrm{VT}} = \frac{A^2_{\mathrm{VT}}}{2WL} \tag{22}$$

where A_{VT} is a process dependent constant.

7.3.4 Error Amplifier of the LVR

An operational amplifier with $PMOS$ input differential pair depicted in the figure 37 is used as an error amplifier for the voltage regulator. It is supplied by the output voltage of the shunt regulator V_{SUP} described in 7.3.2 and biased by the reference current I_{REF}. It consists of two stages and a split-length differential pair for frequency compensation presented in [16].

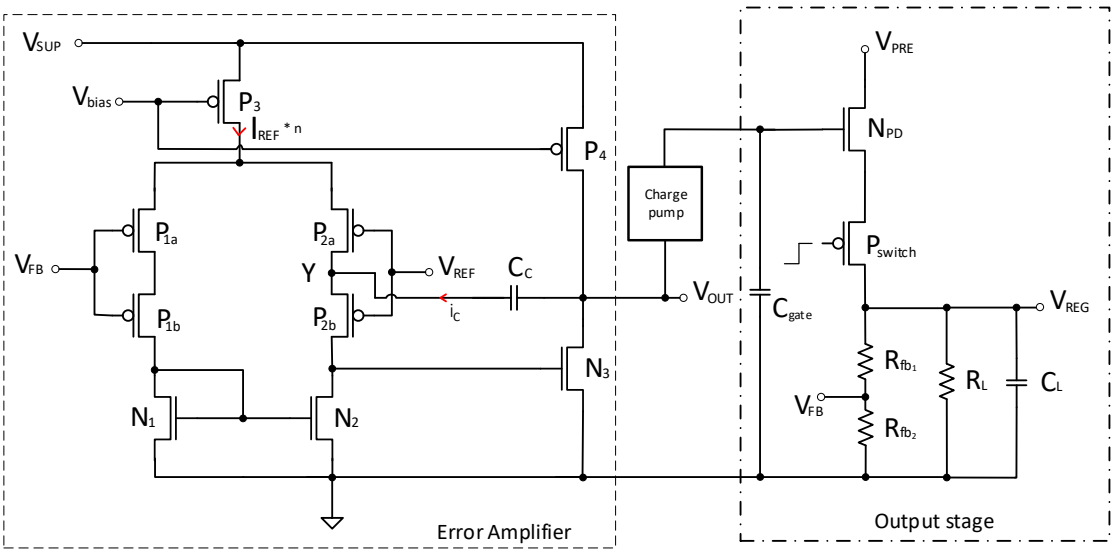


Figure 37: Error amplifier and the output stage of the main regulator

Feedback voltage V_{FB} of the regulator is applied to the positive input and the reference voltage V_{REF} to the negative input of the error amplifier, because of the inverting second stage of the amplifier. The differential input is converted to single-ended output V_{OUT} by the current mirror $N_1 - N_2$. As soon as the feedback voltage decreases, more current flows through the left signal path - transistors P_{1a} and P_{1b} and therefore less current flows through the right side P_{2a} and P_{2b}, due to the constant reference current. The gate voltage of N_3 decreases and since the second stage is also inverting, the output voltage V_{OUT} therefore increases. With an increase in the feedback voltage, output voltage decreases accordingly.

The goal for this concept was area optimization in the sense of using low voltage n-channel pass devices with smaller gate-oxide thickness and minimum gate length and also by avoiding the use of a charge pump, since it increases the area consumption. The results of the previous voltage regulator from the chapter 7.2 showed that such concept has limited performance and

it is not suitable for higher load. The gate of the NMOS regulator needs to be driven above the lowest supply rail, so an integrated charge pump was used to boost up the gate voltage of the NMOS pass device above the supply level when the input battery voltage is in the lower range.
The operational amplifier was designed following the specifications for a high gain. That is achieved by making the transconductance of the input differential pair and the output resistance big, as defined for the DC voltage gain of the amplifier:

$$A_{DC} = G_m \cdot R_{OUT} \tag{23}$$

The transconductance of the first stage g_{m_1} and the output resistance R_{out_1} are defined in the following equations, where $r_{ds_{N2}}$ and $r_{ds_{P2b}}$ represent the drain-source resistances of the transistors N_2 and P_{2b} respectively and g_{m_1} is the transconductance of the $PMOS$ split-length differential pair.

$$G_{m_1} = g_{m_1} \tag{24}$$

$$R_{out_1} = r_{ds_{N2}} \,||\, (g_{mp_{2b}} \cdot r_{ds_{P2b}} \cdot \frac{1}{g_{mp_{2a}}}) \tag{25}$$

So the gain of the first stage is:

$$A_1 = -G_{m_1} \cdot R_{out_1} \tag{26}$$

Second stage is an inverting common source stage formed by the transistor N_3 whose gate is driven from the drains of N_2 and P_{2b} with a $PMOS$ active load P_4. The gain of the second stage A_2 adds up to the overall gain of the regulator, but since another stage is introduced, the bandwidth decreases by the square root of the stage numbers.

$$A_2 = -g_{m_2} \cdot (r_{ds_{N3}} || r_{ds_{P4}}) \tag{27}$$

where $r_{ds_{N3}}$ and $r_{ds_{P4}}$ are drain-source resistances of transistors N_3 and P_4, respectively, and g_{m_2} is the transconductance of the transistor N_3.

Output stage from the figure 37 is non-inverting and it consists of the low voltage $NMOS$

pass device N_{PD} in common drain (source follower) configuration. Its drain is connected to the pre-regulator output voltage V_{PRE} voltage and at its source terminal there is a low voltage $PMOS$ transistor P_{switch} that acts as a switch for the load. The gate of the $NMOS$ pass device is driven by the integrated charge pump, described in the section 7.3.6, to insure low dropout voltage. Capacitor C_{gate} is connected between the gate of the pass device and the ground to decrease the influence of the charge pump ripple.

$$A_{PD} \approx \frac{g_{m_{PD}} R_L}{1 + g_{m_{PD}} R_L} \tag{28}$$

Under assumption that load resistance R_L is much lower than the sum of the feedback resistors R_{fb1} and R_{fb2} and considering a high $g_{m_{PD}} R_L$, the gain of the NMOS source follower A_{PD} is approximately equal to 1.
The overall gain A_{OUT} is simply the product of the voltage gains of the individual stages:

$$A_{OUT} = A_1 \cdot A_2 \cdot A_{PD} \tag{29}$$

7.3.5 Stability Analysis and Compensation Technique

This design requires a special stability compensation because multiple gain stages create multiple poles and can therefore make the system unstable. Indirect compensation using split length differential pair is used, which is based on the splitting the lengths of the differential pair transistors in order to create a low impedance node to feed back the compensation current i_c to the output of the first stage. By splitting the differential pair $PMOS$ from the figure 37 we get a low impedance node Y from the upper device P_{2a} that is in triode or in cut-off region. The transconductance of each split length device can be calculated as $g_{m_p} = \sqrt{2} \cdot g_{m_1}$, where g_{m_1} is the equivalent transconductance of the differential pair input stage. [16]
A simplified small signal model of the circuit from the figure 37 is depicted in the figure 38 and it shows the three main stages, simplified input differential pair stage, second gain stage and the output pass device with the load resistance R_L and the load capacitance C_L, where the feedback resistors are neglected. The current $i_c \approx \frac{V_2}{\frac{1}{sC_c} + \frac{1}{g_{m_p}}}$ is the feedback current that flows through the compensation capacitor C_c and R_i and C_i represent the resistances and the capacitances connected to corresponding nodes i.

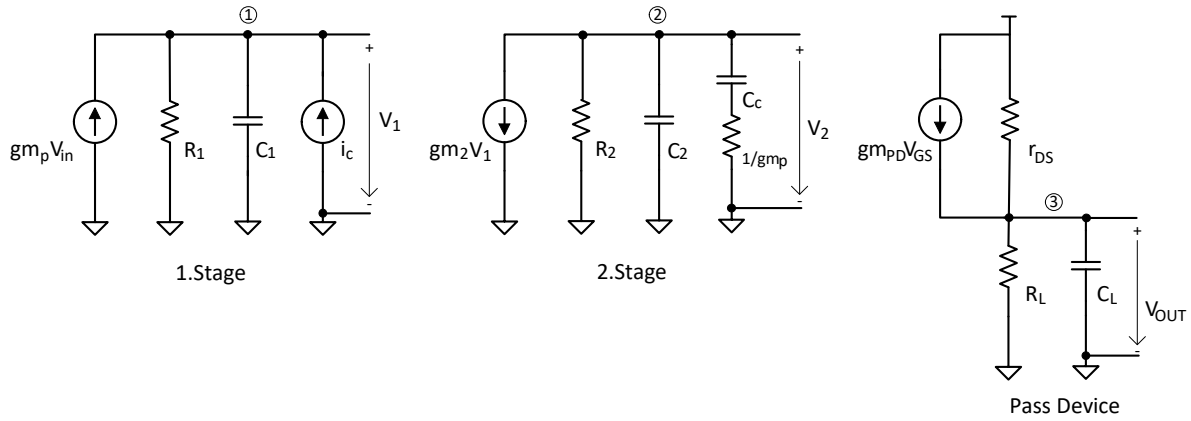


Figure 38: Simplified small signal model

Applying the nodal analysis, we get the following equations:

$$1. \ -g_{m_p}V_{in} + \frac{V_1}{R_1} + sC_1V_1 - i_c = 0$$
$$2. \ g_{m_2}V_1 + \frac{V_2}{R_2} + sC_2V_2 + \frac{V_2}{\frac{1}{sC_c} + \frac{1}{g_{m_p}}} = 0$$
$$3. \ g_{m_{PD}}(V_2 - V_{OUT}) + \frac{V_{OUT}}{r_{DS}} + \frac{V_{OUT}}{R_L} + sC_LV_{OUT} = 0$$

The solution of this system of equations, neglecting the gain of the source follower stage, results in the the transfer function $T(s)$:

$$T(s) \approx \frac{g_{m_p}^2 R_1 g_{m_2} R_2 (1 + \frac{C_c}{g_{m_p}} s)}{a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0} \tag{30}$$

The coefficients of the denominator can be approximated to:

$$
\begin{aligned}
a_0 &\approx g_{m_p} \\
a_1 &\approx g_{m_p} g_{m_2} R_1 R_2 C_c \\
a_2 &\approx g_{m_p} g_{m_2} R_1 R_2 R_L C_L C_c \\
a_3 &\approx g_{m_p} R_1 R_2 R_L C_1 C_L (C_2 + C_c) \\
a_4 &\approx R_1 R_2 R_L C_1 C_2 C_L C_c
\end{aligned}
$$

From the numerator expression the open loop gain can be defined as:

$$A_{OL} = g_{m_p}^2 R_1 g_{m_2} R_2 \tag{31}$$

The compensation capacitor C_c creates one left half plane (LHP) zero located at:

$$z_{LHP} = -\frac{g_{m_p}}{C_c} \tag{32}$$

The LHP zero increases the phase margin and the overall stability of the system. Assuming that the dominant pole is located at much lower frequencies than the other poles, it can be estimated as:

$$p_1 \approx -\frac{a_0}{a_1} = -\frac{1}{g_{m_2} R_1 R_2 C_c} \tag{33}$$

From the equation 33 it can be seen that the dominant pole mainly depends on gain of the second stage, the output resistance of the first stage and the compensation capacitance.
The gain-bandwidth GBW of the system can be determined as:

$$GBW = A_{OL}\, p_1 = \frac{g_{m_p}^2}{C_c} \tag{34}$$

The non-dominant poles are approximated to:

$$p_2 \approx -\frac{a_1}{a_2} = -\frac{1}{R_L C_L} \tag{35}$$

$$p_3 \approx -\frac{a_2}{a_3} = -\frac{g_{m_2} C_c}{C_1 (C_2 + C_c)} \tag{36}$$

The table 7 shows the values of the components from the figure 37. The multiplication factor n refers to bias current of the error amplifier I_{REF} coming from the bandgap block. Gate capacitance C_{gate} decreases the charge pump ripple at the gate of the pass device, and the load capacitance C_L improves the load transient regulation. The values for the resistive feedback divider R_{fb_1} and R_{fb_2} are determined by the voltage division between the feedback voltage V_{FB} and the regulator output voltage V_{REG} according to the equation 1.

Components	*Values*
n	2
R_{fb_1}	$30\,k\Omega$
R_{fb_2}	$120\,k\Omega$
C_{gate}	$12\,pF$
C_c	$2\,pF$
C_L	$100\,pF$

Table 7: Component values of the error amplifier and the output stage of the main regulator

7.3.6 Charge Pump

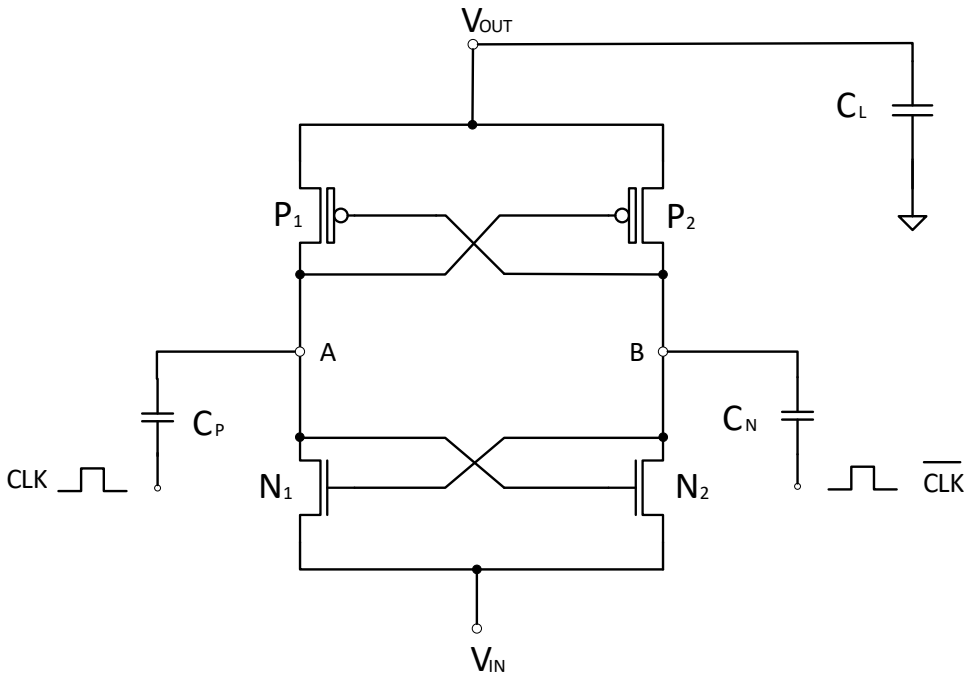


Figure 39: Cross-coupled charge pump

The charge pump from Figure 39 contains the pumping capacitors C_P, C_N and cross-coupled MOS switches. A cross-coupled pair works as a positive feedback, where the change on the one side gets amplified by the other side.

The basic functionality of the cross-coupled charge pump can be described as followed:

At the beginning the input capacitors C_P and C_N are discharged. The cross coupled NMOS transistors are driven by the two complementary clock signals CLK and $\overline{CLK}$ supplied by the voltage V_{DD}. Assuming the voltages on the nodes A and B are $0\,V$ and $CLK = V_{DD}$, charge gets injected into the capacitor C_P raising the node A to approximately V_{DD}. When $\overline{CLK}$ changes from $0\,V$ to V_{DD}, charge is injected into the capacitor C_N and voltage at the node B raises to V_{DD}. Another CLK transition to V_{DD} changes the potential on the node A to approximately $2V_{DD}$, while in turn the same described procedure happens in the right branch, so basically the two node voltages A and B alternate between V_{DD} and $2V_{DD}$, turning the cross-coupled PMOS switches on with whichever node has a smaller voltage, and passing the higher voltage to the output.

The charge pump output is connected directly to the gate of the pass device, and therefore

it is not loaded and no extra current is drawn from the charge pump. The advantage of such a structure is that smaller pumping capacitors can be used, keeping the area of the charge pump small. The disadvantage is that the charge pump ripple is directly seen on the gate of the pass device, passing the ripple onto the regulator output voltage. The maximum difference between input and output voltage is limited to approximately $1.5\,V$, and the settling time depends on the load capacitance at the output of the charge pump. Smaller load capacitance implies shorter settling time, but also bigger ripple at the output voltage due to switching. Output ripple can be reduced by increasing the clock frequency and the area of the output capacitor.

An internal CTS (Comprehensive Transponder Systems) relaxation oscillator independent of the supply voltage and bias current variations as described in [10] is used for the clock circuitry. The supply voltage for the oscillator is created using an additional supply voltage generation circuit as described in the chapter 7.3.2 in order to avoid switching noise in other blocks. Reference current from the bandgap block is used for the bias current. The single output clock is then sent to a non-overlapping two-phase clock generator using NAND gates to avoid charge sharing of the pumping capacitors in the charge pump as depicted in the figure 40.

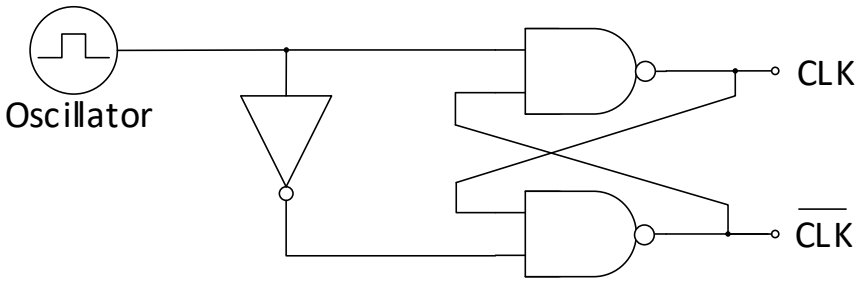


Figure 40: Non-overlapping clock generation

Charge pump is implemented in the circuit once for the main regulator, and once more as two single charge pumps connected in series at the gate of the pre-regulator pass device. The values of the components for the charge pump circuit are shown in the table 8. The simulation of the nominal corner for $5\,V$ supply voltage and $1\,mA$ load current at the temperature of $27°C$, $3.5\,MHz$ frequency resulted in approximately $1\,mV$ output ripple, as shown in the

figure 41.

Component	Value	Unit
C_P	40	fF
C_N	40	fF
C_L	12	pF

Table 8: Component values of the charge pump circuit from the figure 39

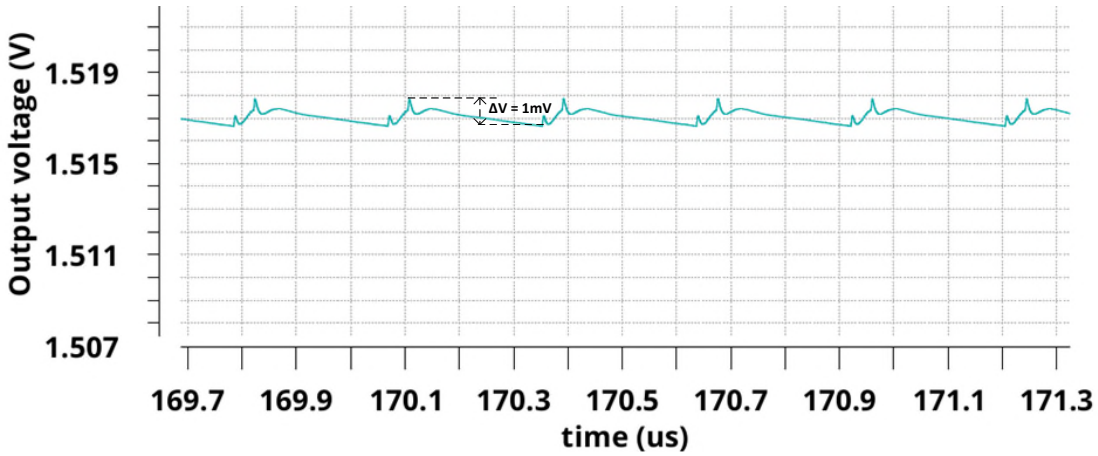


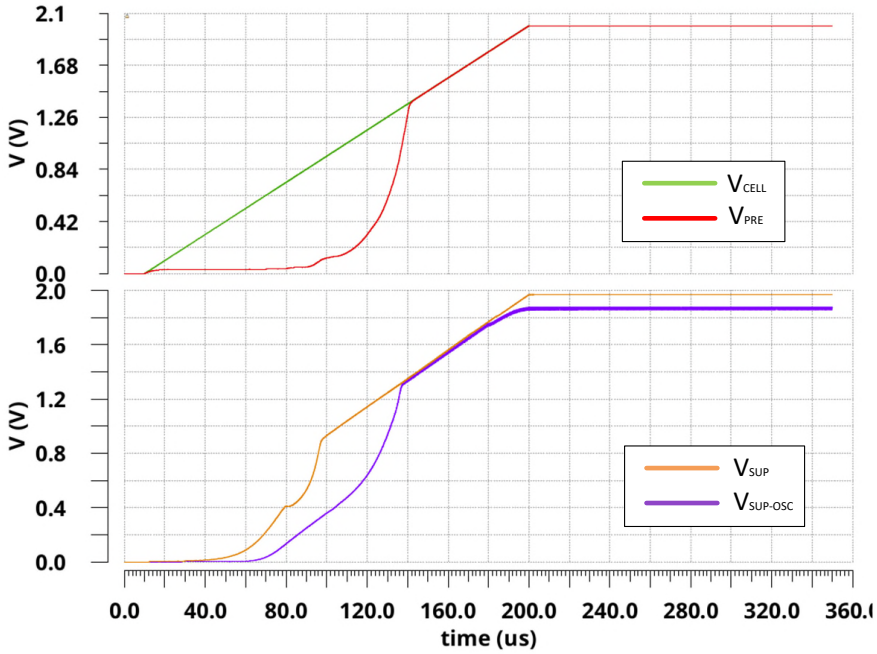
Figure 41: Output ripple due to charge pump switching

7.3.7 Simulation Results

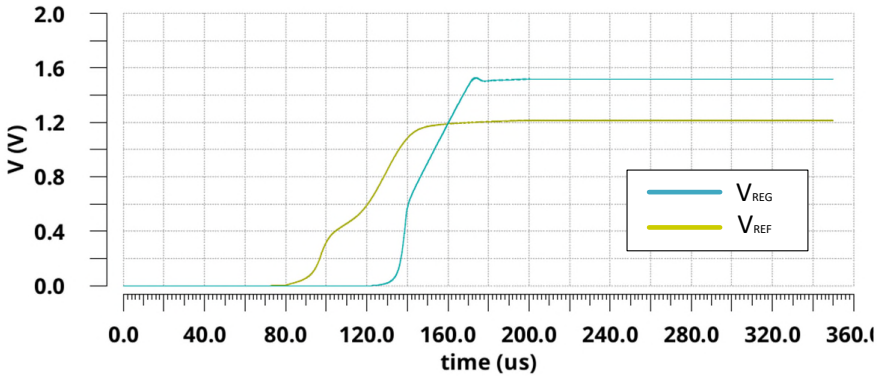
The testbench of this LVR is added in the Appendix A. The simulations have been performed for a single, as well as for 3 main linear voltage regulators.

Start-up Behaviour

Fig. 42a and 42b show the nominal start-up behaviour of the different voltages for the supply voltage change from $0\,V$ to $2\,V$ in $190\,\mu s$ for a load current of $1\,mA$. It can be seen from the plots that as soon as the supply voltage V_{CELL} reaches $2\,V_{TH} + 3\,V_{DSAT}$, which are the threshold and saturation voltages of the transistors P_0, P_1 and N_3 from the figure 29, the voltage V_{SUP} increases and follows in this case $V_{CELL} - V_{DSAT_{P2}}$, while the bandgap circuit generates the reference voltage V_{REF}. Similarly to V_{SUP}, the supply voltage for the oscillator circuit $V_{SUP-OSC}$ increases and the charge pump is activated, raising the gate voltage of the pre-regulator pass-device, which produces the output voltage V_{PRE} used as a supply voltage at the drain of the main regulator pass device. The regulated output voltage V_{REG} is stabilized at $1.5\,V$ for the above mentioned current load when the V_{CELL} reaches approximately $1.8\,V$.



(a)



(b)

Figure 42: Start-up behaviour for cell voltage change from $0\,V$ to $2\,V$ in $190\,\mu s$; load current $1\,mA$; typical process corner, $\vartheta = 27°C$. (a) Supply voltage for the bandgap and error amplifiers V_{SUP}; oscillator supply voltage $V_{SUP-OSC}$; pre-regulator output voltage V_{PRE}. (b) Bandgap reference voltage V_{REF}; main regulator output voltage V_{REG}

AC Analysis

The open loop AC analysis is done for the testbench added in the appendix B. The loop is opened at the feedback node V_{FB} where an inverted AC-source with $1\,V$ AC magnitude is connected. For this purpose, it is assumed that the charge pump voltages at the gates of the pre-regulators are settled. Figure 43 shows the frequency response of the regulator at the supply voltage of $2\,V$ for the load current of both $50\,\mu A$ and $15\,mA$ and the results for the supply voltage of $5\,V$ are presented in the figure 44.

The comparison of the simulated results are given in the table 9. The DC gain of the system stays approximately the same for the minimum and maximum load current and doesn't vary a lot with the supply voltage which is characteristic for the voltage regulators with the $NMOS$ pass device. The same is valid for the bandwidth of the regulator due to the fact that the dominant pole is generated at the output of the error amplifier, and doesn't vary with the load current. Since the non-dominant pole p_2 from the equation 36 depends on the output resistance, the increase in the load current reduces the output resistance and moves this pole to the higher frequencies which causes the increase in the phase margin and unity gain frequency.

Supply voltage	$2\,V$		$5\,V$	
Load current	$50\,\mu A$	$15\,mA$	$50\,\mu A$	$15\,mA$
Gain	$89.7\,dB$	$90.8\,dB$	$90.5\,dB$	$93.7\,dB$
UGF	$2.7\,MHz$	$4.6\,MHz$	$3.1\,MHz$	$8.1\,MHz$
Bandwidth	$105.9\,Hz$	$89.2\,Hz$	$105.3\,Hz$	$74.2\,Hz$
Phase Margin	$56.1°$	$98.1°$	$56.6°$	$81.4°$

Table 9: Nominal simulation results of the AC Analysis

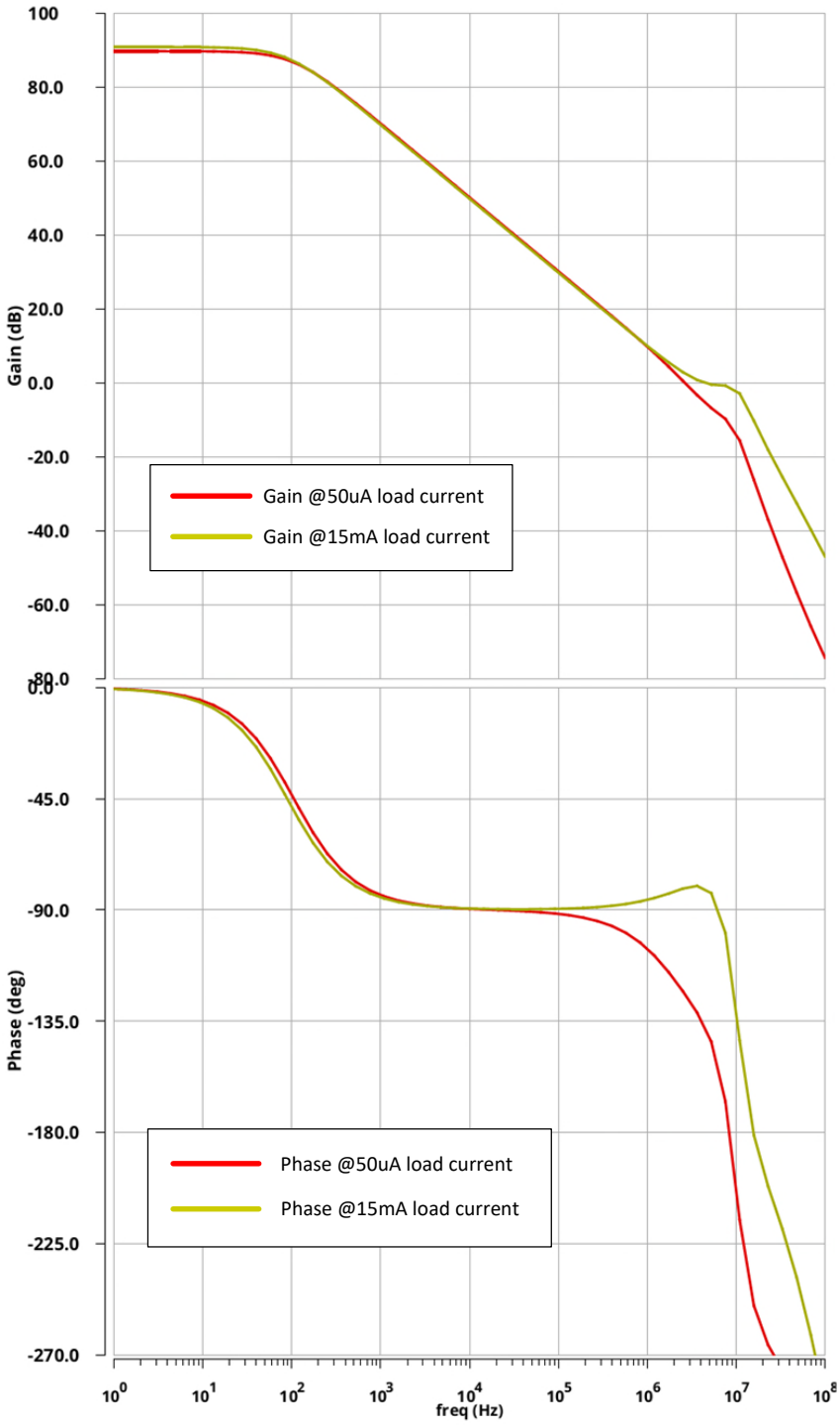


Figure 43: Frequency response of the regulator at $2\,V$ supply voltage for load currents of $50\,\mu A$ and $15\,mA$, typical process corner, $\vartheta = 27\,°C$

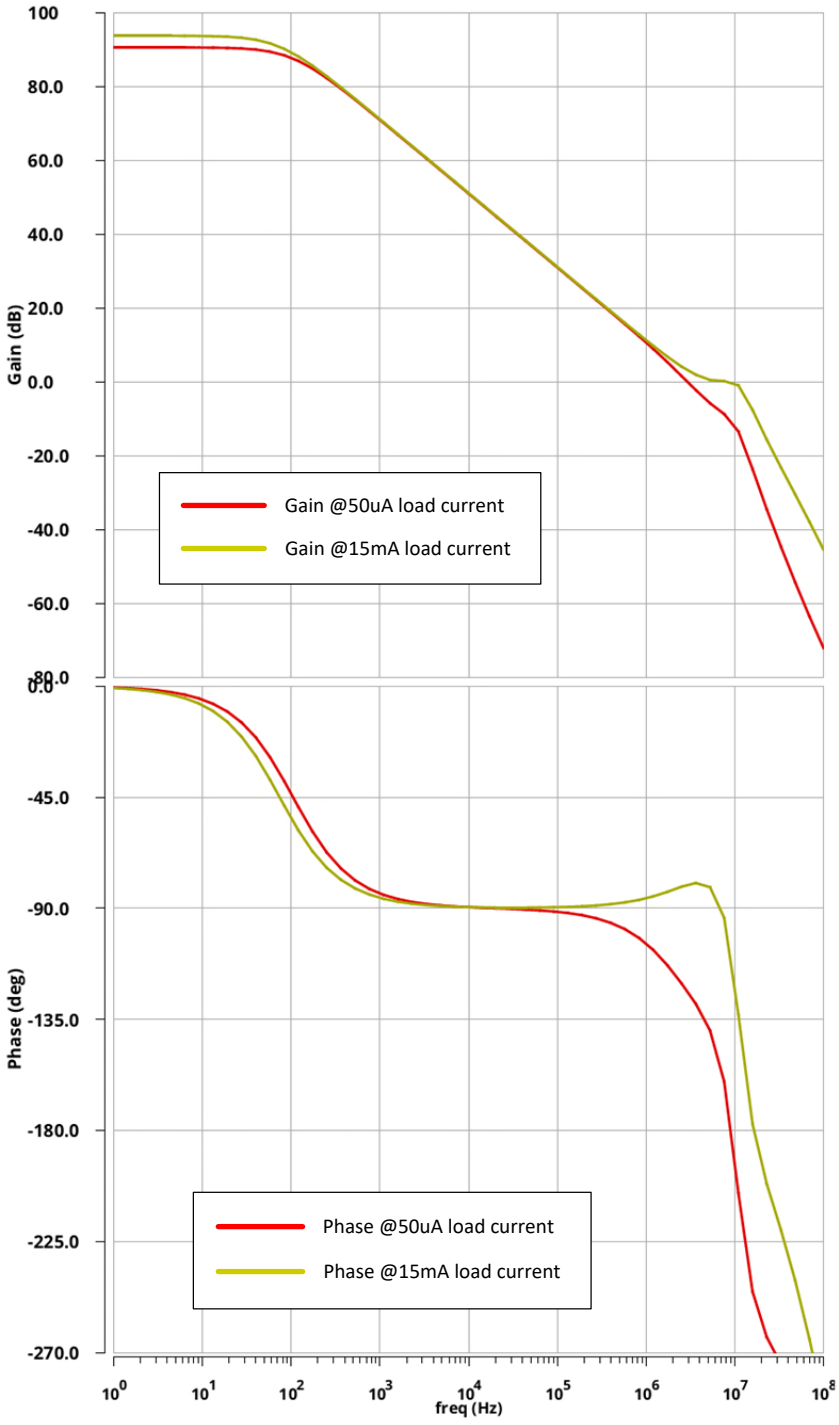


Figure 44: Frequency response of the regulator at $5\,V$ supply voltage for load currents of $50\,\mu A$ and $15\,mA$, typical process corner, $\vartheta = 27\,°C$

The corner analysis for all process corners at minimum and maximum battery voltage, as well for the minimum and maximum load current for temperature values of $-40°C$ and $120°C$ resulted in the worst case AC analysis parameters given in the table 10, inclusive the summary of the Monte Carlo simulation for 3 sigma with 200 runs taking both process and mismatch variations into account.

	Min	Mean	Max	Unit
Gain	73.549	77.23	99.38	dB
UGF	792.8k	1.73	13.44	MHz
Bandwidth	52.72	227.3	362.6	Hz
Phase Margin	51.88	89.94	99.38	°

Table 10: The worst case AC analysis parameters for: $V_{CELL} = 2\,V; 5\,V$, $I_{LOAD} = 50\,\mu A; 50\,mA$, all process corners and 200 MC runs, $\vartheta = -40°C; 120°C$

Power Supply Ripple Rejection - PSR

Power supply ripple rejection ratio ($PSRR$) at the output of the main regulator is determined in a closed loop AC simulation by applying a $1\,V$ AC-source to the supply voltage V_{CELL}.

At lower frequencies, the $PSRR$ results in higher absolute values, and it is mainly defined by the open loop gain and the $PSRR$ of the bandgap reference [18]. As the frequency increases, the absolute value of the $PSRR$ drops. The open loop gain of the regulator decreases, until it comes to the unity gain frequency (UGF), where the $PSRR$ is the worst. Figure 46 shows that the $PSRR$ of the NMOS pass device regulator doesn't change with the varying load current at lower frequencies, since the change in load current doesn't affect the gain of the regulator. Above the UGF, with the load current variations, the output resistance also changes and the influence of the load capacitor on the $PSRR$ can be observed.

Figure 45 shows that the worst $PSRR$ occurs in the range near the unity gain frequency at lowest supply voltage $V_{CELL} = 2\,V$. This is due to lack of the voltage headroom for the pre-regulator at lower supply voltage. In this case the pass device of the pre-regulator acts as a switch and cannot suppress the noise coming from the power supply line anymore.

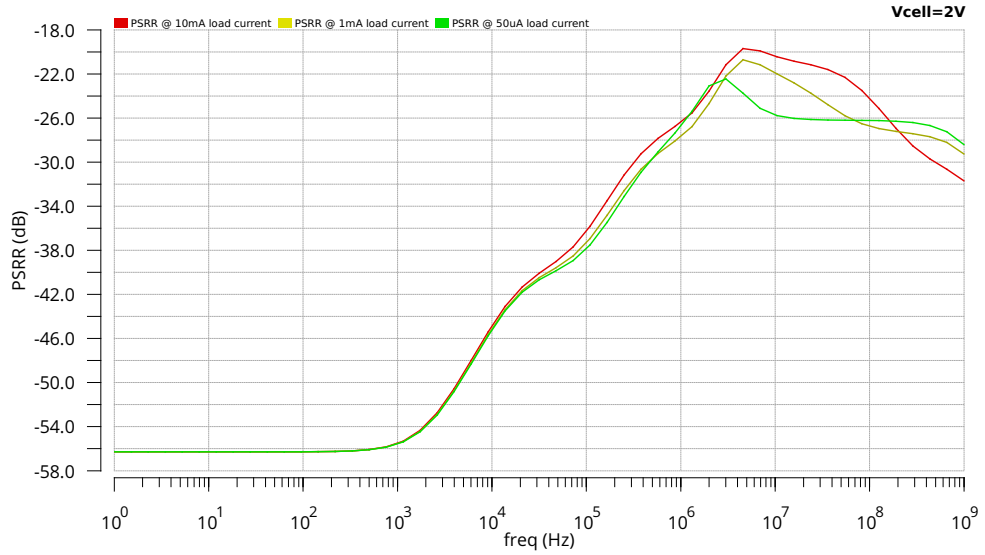


Figure 45: PSRR for $V_{CELL} = 2\,V$ at varying load current $I_{LOAD} = 50\,\mu A; 1\,mA; 10\,mA$

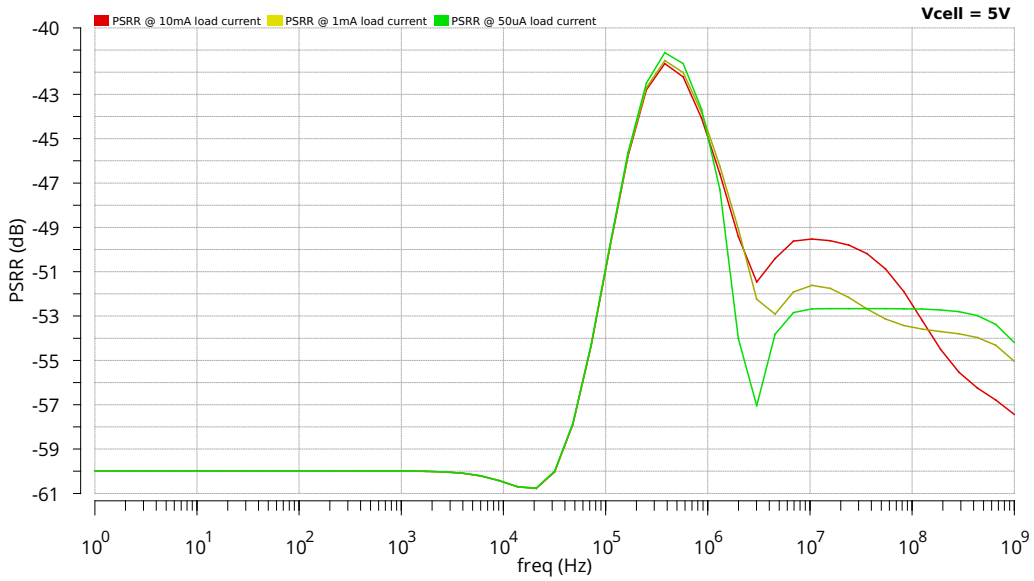


Figure 46: PSRR for $V_{CELL} = 5\,V$ at varying load current $I_{LOAD} = 50\,\mu A; 1\,mA; 10\,mA$

Line Transient Response

Regulator output voltage response for a change in the supply voltage at different load current shows the minimum supply voltage which is needed for a low drop-out regulation. As it can be seen from the figure 47, at lower current load approximately $V_{CELL} \geq 1.56\,V$ is needed for a stable output voltage regulation, and $V_{CELL} \geq 1.75\,V$ for a maximum output current of $10\,mA$. Small drop-out voltage for an $NMOS$ pass device is achievable when the charge pump is used to make the gate voltage higher than the supply.

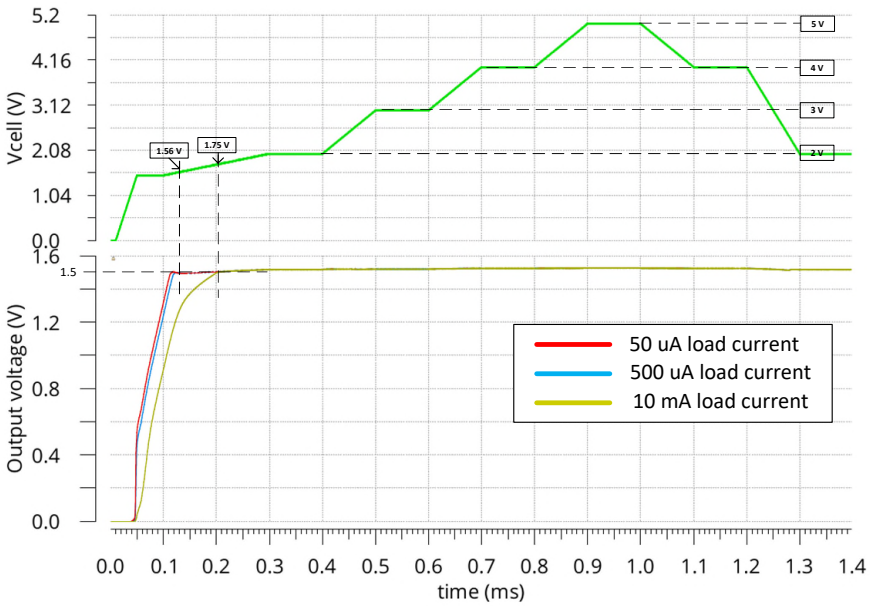


Figure 47: Regulator output voltage response to a gradual change in the supply voltage V_{CELL}; typical process corner, $\vartheta = 27°C$

Line transient profiles described in the chapter 6.3 are used to test the regulator for the change in the supply line, which influences the output voltage through several different paths, such as the path to the block for V_{SUP} voltage generation, which is used as a supply voltage for the bandgap circuit and the error amplifiers, or through the pre-regulator output voltage. Figure 48 shows the output voltage response to the supply voltage variation of $1\,V$ with rise and fall time of $4\,\mu s$. On the figures 49a and 49b output voltage response to the $\pm 200\,mV$ peaks in the supply voltage is presented. The changes in the output voltage stay inside the range of $\pm 10\%$ of the nominal output voltage.

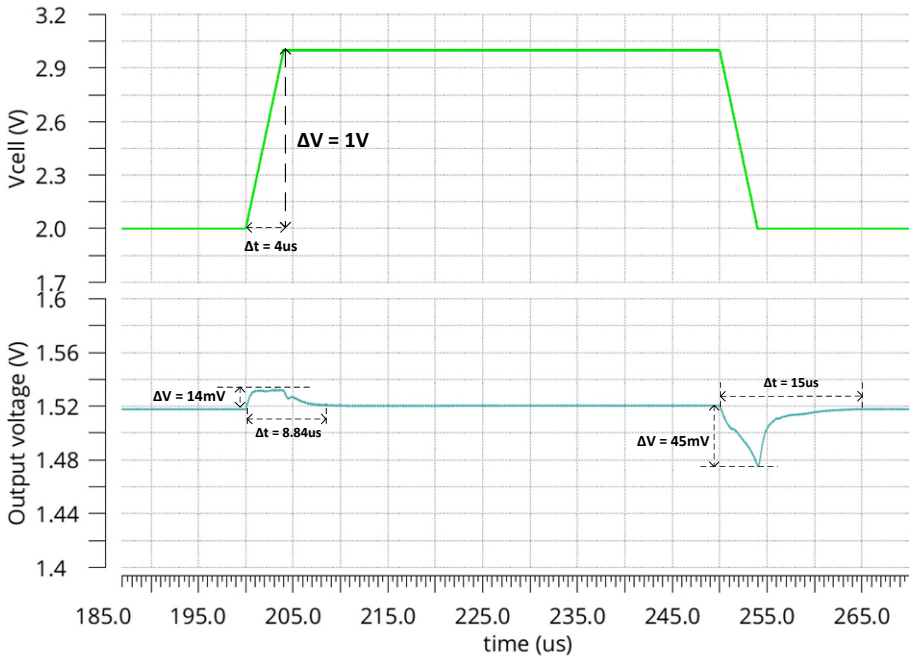
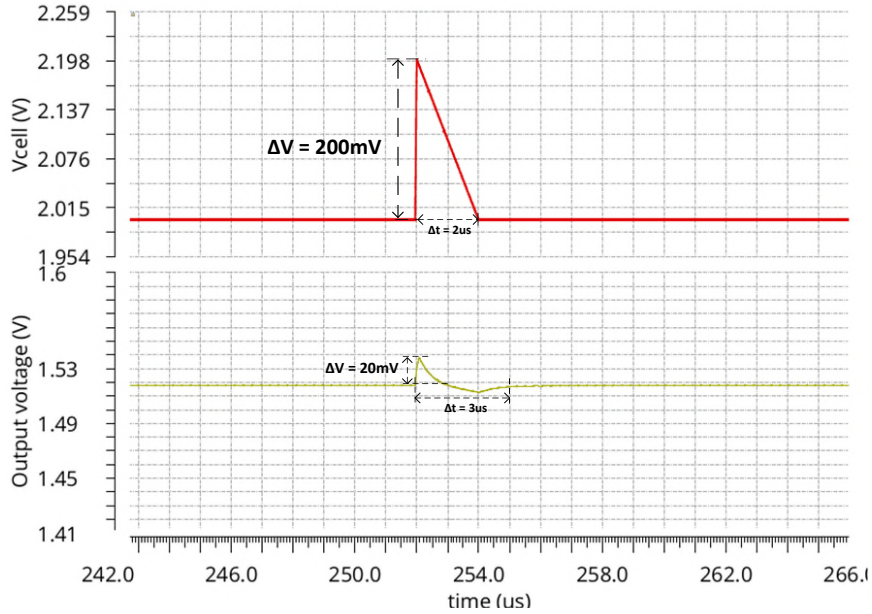


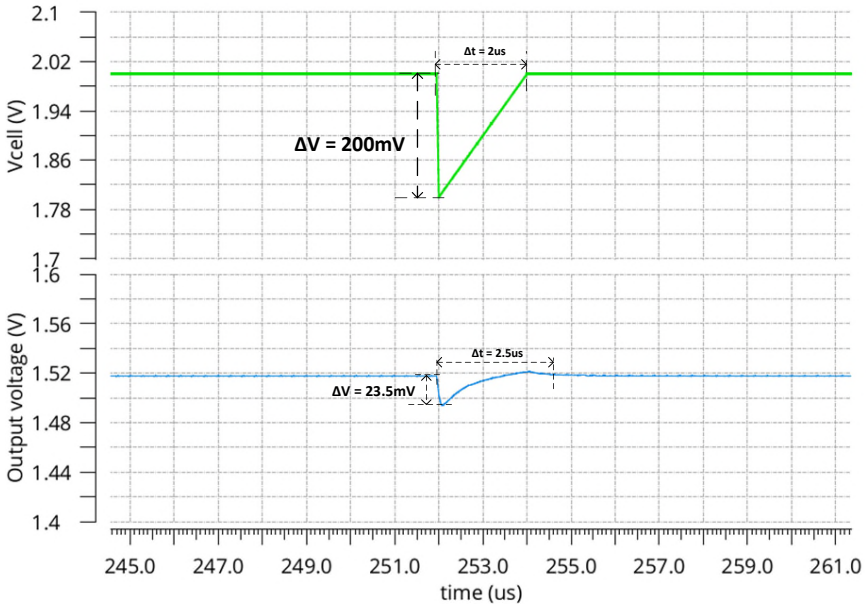
Figure 48: Line transient response for $\Delta V_{CELL} = 1\,V$ at $1\,mA$ load current for a nominal simulation at $27°C$

The corner simulations through all the process corners and temperatures of $-40°C$ and $120°C$ for the positive and negative peaks at $V_{CELL} = 2\,V$ presented on figures 50a and 50b show that all the over- and undershoots for the regulator output voltage are in the range of $\pm 10\%$ of the nominal output voltage.

Positive peaks at $V_{CELL} = 5\,V$ don't cause any major changes on the significant signals or any overvoltage conditions, as it can be seen from the simulation result on the figure 51.

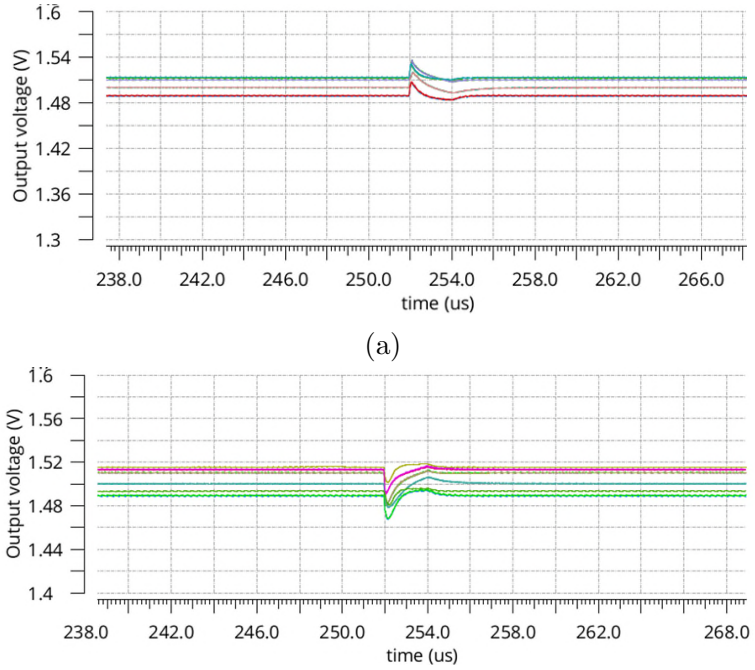


(a)



(b)

Figure 49: Line transient response to fast rising peaks in the supply voltage (typical process corner, $\vartheta = 27°C$. (a) Positive 200 mV peaks at $V_{CELL} = 2\,V$ (b) Negative 200 mV peaks at $V_{CELL} = 2\,V$.



(a)

(b)

Figure 50: Line transient response to fast rising peaks in the supply voltage (corner simulation for all process corners, $\vartheta = -40°C; 120°C$. (a) Output response to $200\,mV$ peaks at $V_{CELL} = 2\,V$. (b) Output response to $-200\,mV$ peaks at $V_{CELL} = 2\,V$.

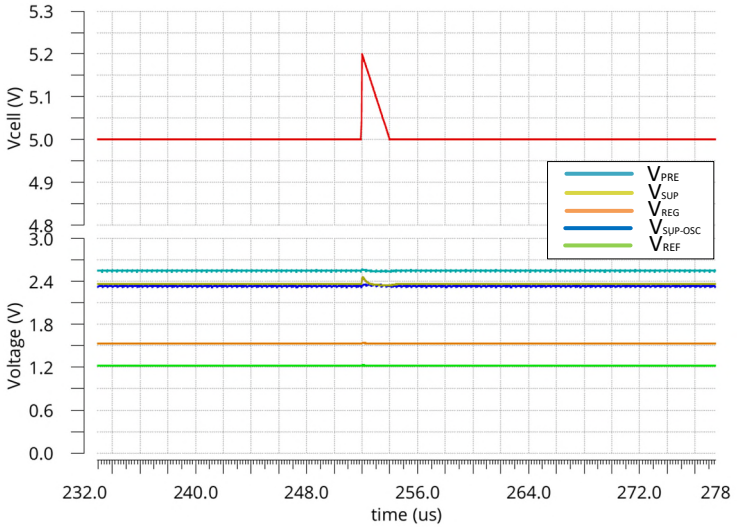


Figure 51: Line transient response of the internal supply and reference voltages for $\Delta V_{CELL} = 200\,mV$

Load Transient Response

Transient response to a load current step from $20\,\mu A$ to $10\,mA$ in $5\,\mu s$ for a typical nominal simulation as it can be seen from the figure 52, which shows that the under- and overshoots at the output voltage also stay in the range of $\pm 10\%$ of the nominal output voltage. Worst case results over all process corners with highest voltage over- and undershoots and longest recovery time are obtained for fast corners at $120°C$ temperature.

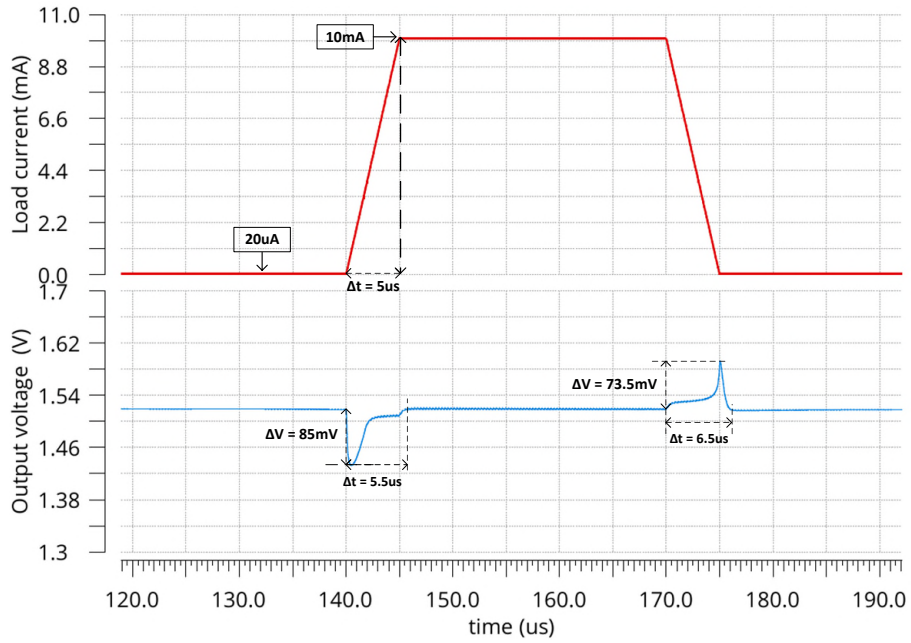


Figure 52: Load transient response for the applied step in the load current from $20\,\mu A$ to $10\,mA$ in $5\,\mu s$ at $V_{CELL} = 2\,V$; typical process corner, $\vartheta = 27°C$

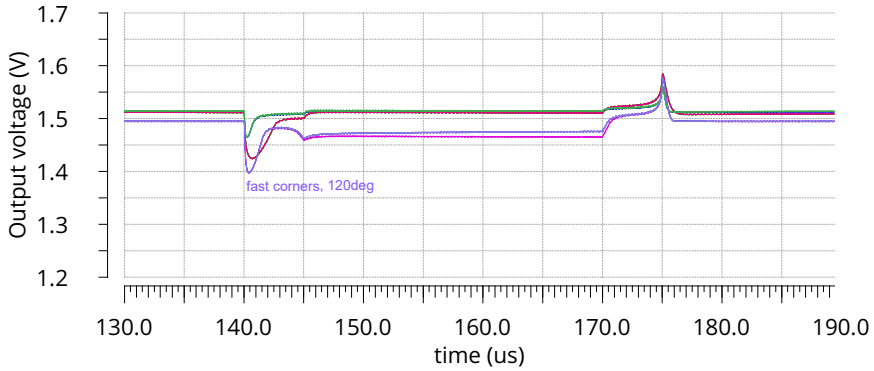


Figure 53: Load transient response for the change in the load current from $20\,\mu A$ to $10\,mA$ in $5\,\mu s$ at $V_{CELL} = 2\,V$; all process corners; $\vartheta = -40°C; 120°C$

Two opposite load profiles as shown in the figure 54, which are applied on two separate regulators don't impact each other's output voltage, even though they share the same bandgap reference and the same drain voltage.

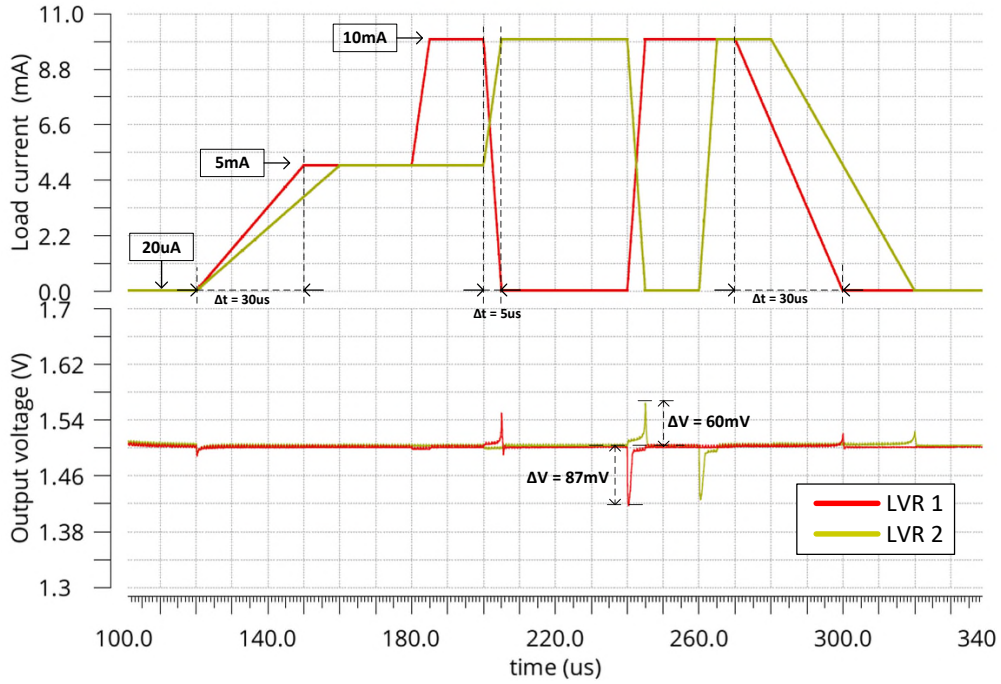


Figure 54: Load transient response for two opposite load transient profiles at two separate linear voltage regulators LVR 1 and LVR 2 for $V_{CELL} = 2\,V$; typical process corner, $\vartheta = 27°C$

The worst load transient response is expected for the digital load current profile described in the section 6.2. High fast rising current peaks from $500\,\mu A$ to $7.2\,mA$ in $2\,ns$ rise time with a period of $36\,ns$ as depicted in the figure 55 cause the biggest undershoot of the output voltage at $1.36\,V$.

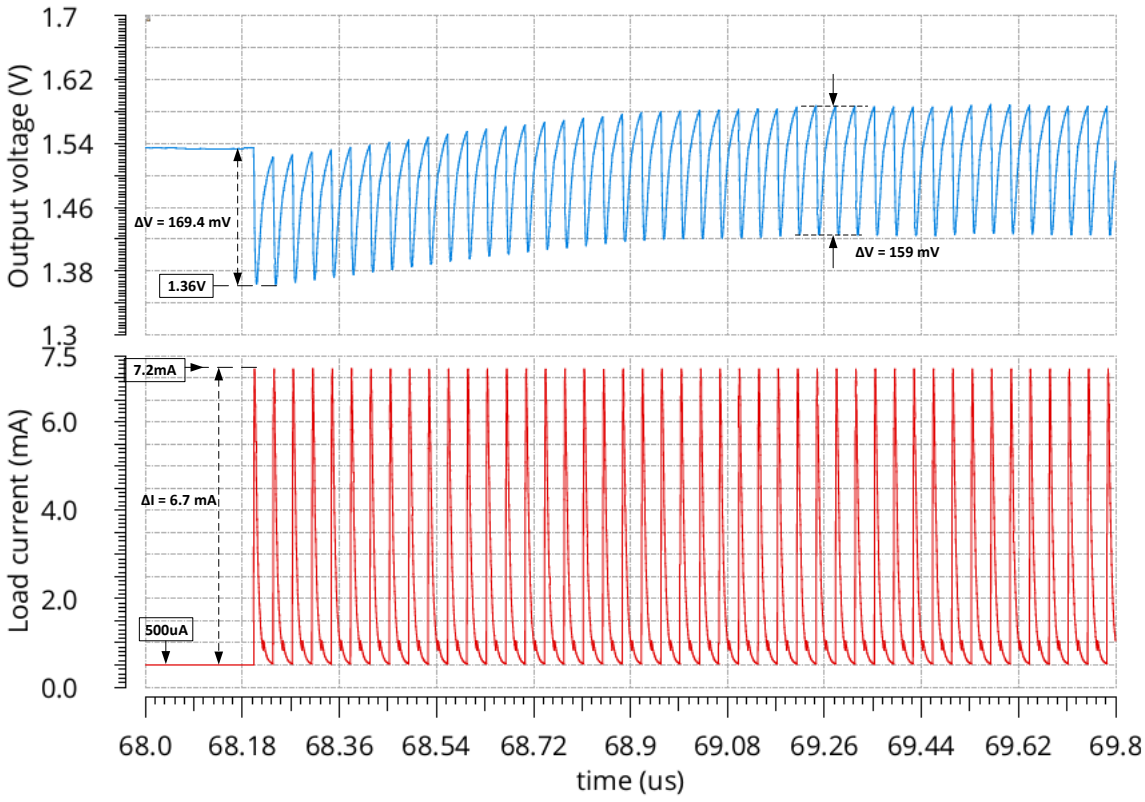


Figure 55: Load transient response to digital current load profile; $V_{CELL} = 2\,V$; typical process corner $\vartheta = 27°C$.

8 Conclusion and Outlook

This thesis presents the analysis of different linear voltage regulator topologies, such as:

- linear voltage regulator with a medium voltage PMOS pass device,
- cascoded structure of the voltage regulator using medium voltage PMOS pass device as a pre-regulator and a low voltage NMOS pass device without the charge pump circuit,
- cascoded structure using only low voltage NMOS pass devices and cross-coupled micro charge pumps.

The characteristic differences between the linear voltage regulators with NMOS or PMOS pass device are analyzed. The possible advantages or disadvantages of using medium or low voltage pass devices in terms of area optimization versus exceeding the safe operation region of the devices have been discussed. Therefore, the cascaded structure using pre-regulator is introduced, which regulates the high supply voltage to a voltage level suitable for supplying a block with low voltage devices with smaller gate area.

The LVR with a medium voltage PMOS pass device manifests its advantages in the simplicity of the design with no additional circuit components, such as pre-regulator or charge pump. The current capability of PMOS is much lower than the one of the NMOS pass device, due to the low mobility of the charge carriers. This LVR can operate in low dropout region, but has degraded load regulation and dynamic load response. It requires complex stabilisation due to the pole at lower frequencies. Open loop AC simulations of this LVR showed a significant reduction of the phase margin for low load current.

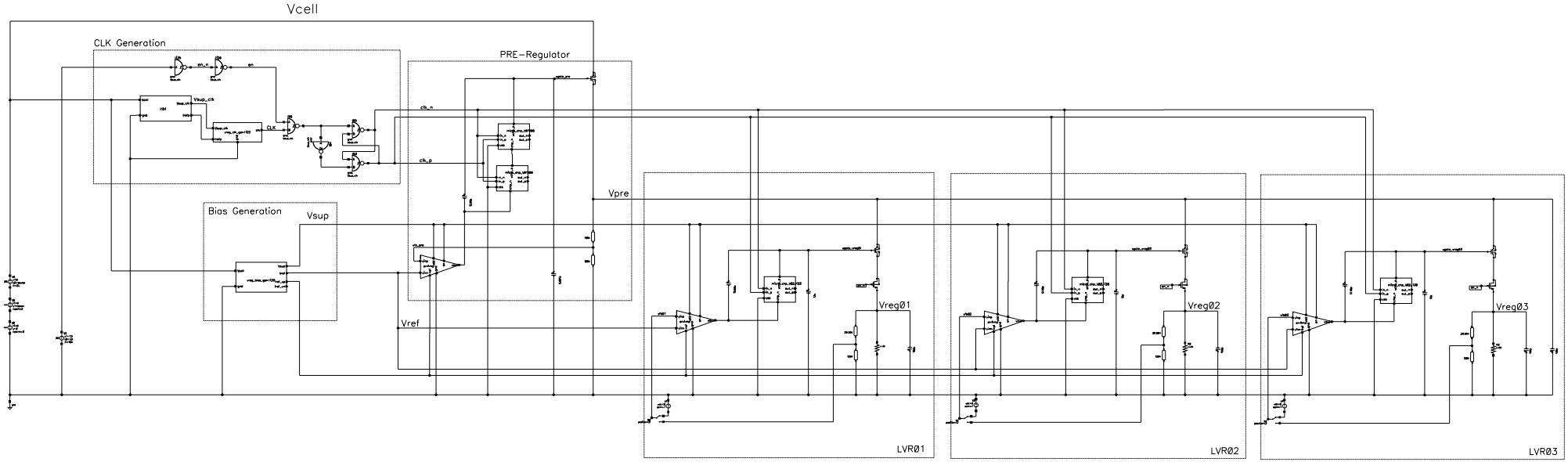
Cascoded topology using low voltage NMOS pass device without the charge pump can regulate the output voltage only for typical process corners, and its performance degrades significantly for slow corners and low temperatures, due to the increase in the threshold voltage of the pass device.

Therefore in the third concept the cross-coupled micro charge pump is employed which has the advantage of using small pumping capacitors, but since its output is directly connected at the gate of the pass device, the charge pump ripple is directly transferred to the output

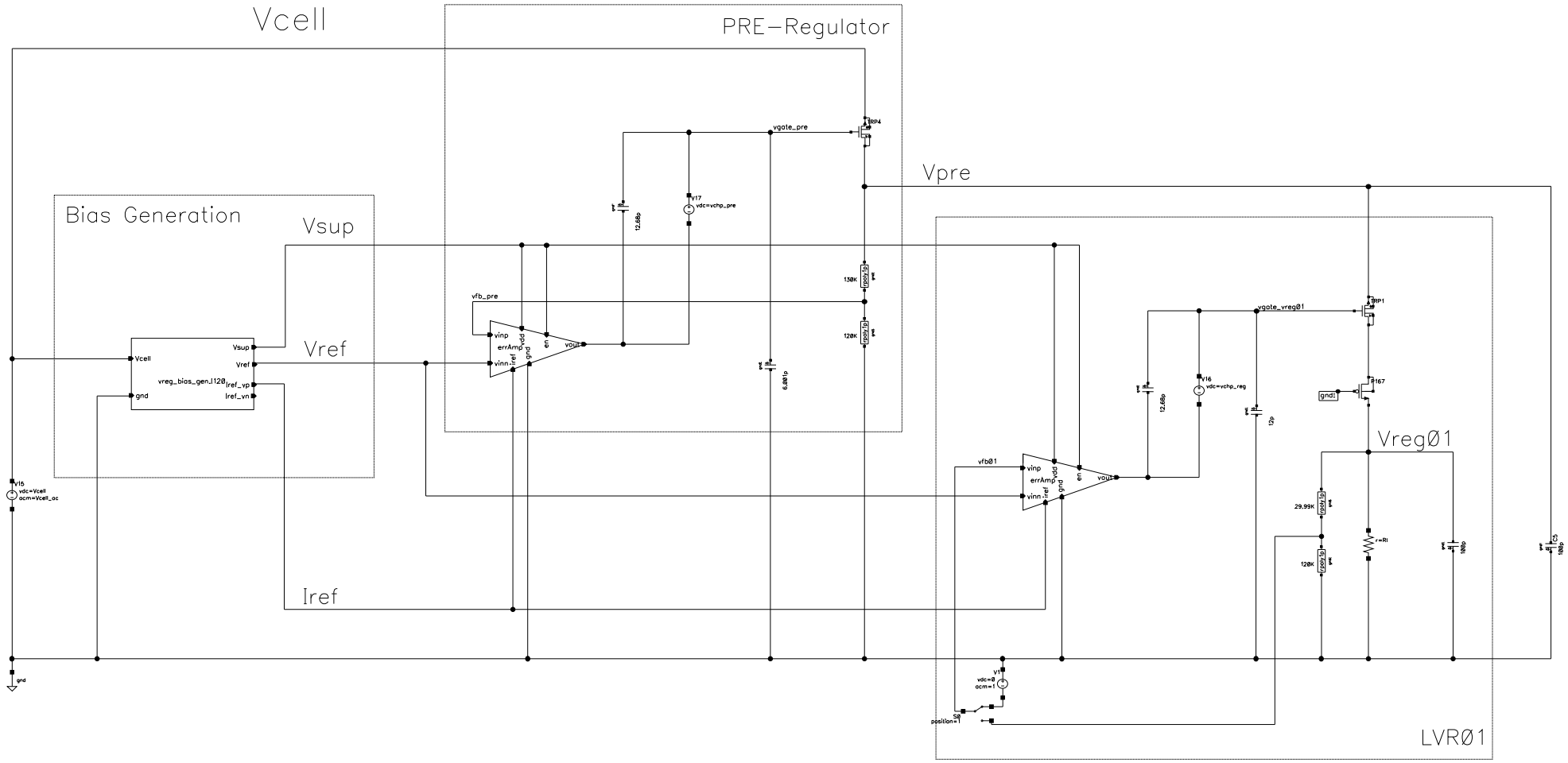
voltage and every pass device requires an additional charge pump at the gate. High input impedance of the NMOS source follower structure is not seen as an additional load for the charge pump output voltage. To reduce the overall chip area this concept is designed using low voltage MOS devices only. In order not to exceed the breakdown voltage region of any of the low voltage devices, an internal supply voltage is generated which was used as a supply voltage for the bandgap reference voltage and the two stage error amplifiers. Clock generation circuitry was supplied by an extra supply voltage generation circuit in order to avoid noise coupling in the other blocks. This design showed an acceptable load and line regulation with a fast transient response time over all process corners and temperature range from $-40°C$ - $120°C$.

The future work can be concentrated on reducing the output ripple caused by the charge pump. For example, it can be reduced by using a regulated cascode current mirror at the gate of the pass device, as presented in [4], but this additionally loads the charge pump and increases in turn the size of the pumping capacitors, and therefore the overall chip area. Additional supply voltage generation needed for the clock circuit increases the overall current consumption, so future work can also be concentrated on solving this problem too.

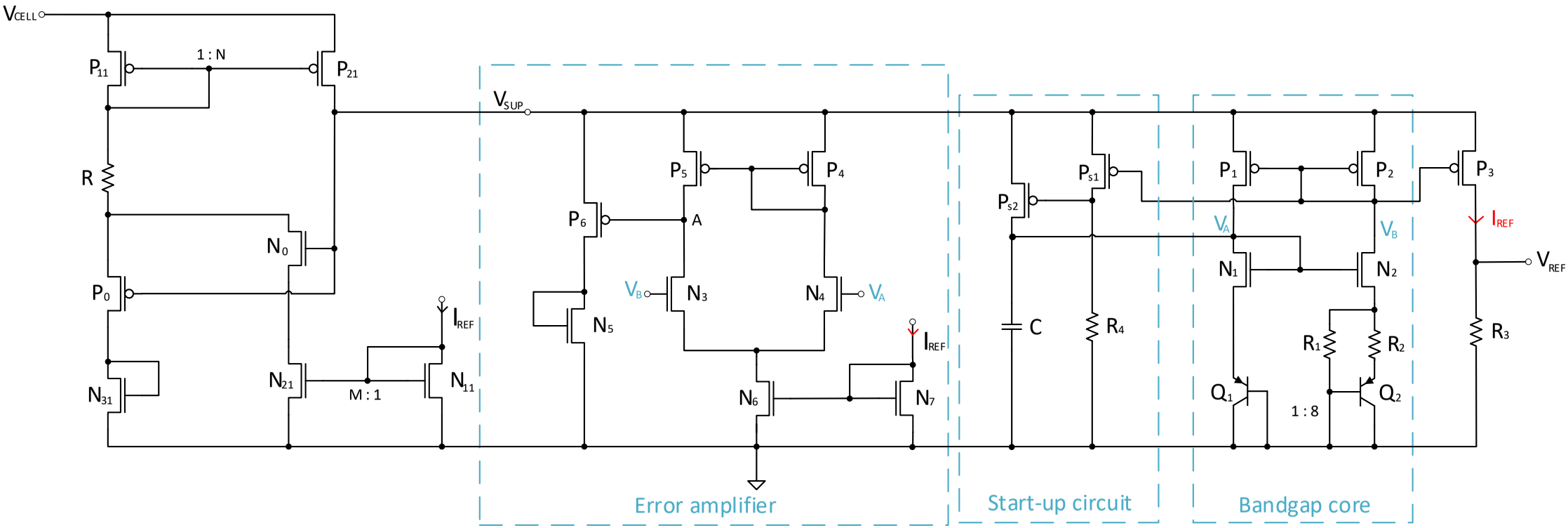
A Testbench - Cascoded Topology Using Low-Voltage Devices


Vcell
CLK Generation
PRE-Regulator
Bias Generation
Vsup
Vpre
Vref
Vreg01
Vreg02
Vreg03
LVR01
LVR02
LVR03

B AC Simulation Testbench - Cascoded Topology Using Low-Voltage Devices


Vcell
PRE−Regulator
Bias Generation
Vsup
Vref
Iref
Vpre
vgate_pre
vfb_pre
vinp
vinn
errAmp
vout
vgate_vregØ1
vfbØ1
VregØ1
LVRØ1
gnd!
gnd
Vcell
vreg_bias_gen_1120
Iref_vp
Iref_vn
vdc=vchp_pre
vdc=vchp_reg
vdc=Vcell
acm=Vcell_ac
vdc=0
acm=1
position=1
130K
120K
29.99K
12.68p
6.801p
12p
100p

C Schematic of the Bias Generation: V_{SUP}, V_{REF} and I_{REF}


VCELL
P11
1 : N
P21
R
N0
P0
N31
N21
M : 1
N11
IREF
VSUP
P5
P4
P6
A
VB
N3
N4
VA
N5
N6
N7
IREF
Error amplifier
Ps1
Ps2
C
R4
Start-up circuit
P1
P2
P3
VA
VB
IREF
VREF
N1
N2
R1
R2
R3
Q1
Q2
1 : 8
Bandgap core

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