Johannes Sebastian Lindmoser, BSc

Analysis of a Quasi-Resonant Converter with High Power Density

Thesis

to the acquisition of the academic degree of
Diplom-Ingenieur

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(in cooperation with Infineon Technologies Austria AG)

Ass. Prof. Dipl.-Ing. Dr. techn. Klaus Krischan
Electric Drives and Machines Institute
Graz University of Technology

2021

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Contents

Abstract

In this thesis, a galvanically isolated quasi-resonant topology is investigated for its potential applications.

The aim of this investigation is to determine whether this topology satisfies a number of essential requirements. These include a specified input voltage range as well as output power range.

The topology discussed in this thesis has evolved from a non-isolated resonant converter.

An advantage of the converter topology described here is galvanic isolation but also a soft-switching behavior of the semiconductor switches (MOSFET) in certain operating cases. This is advantageous at high switching frequencies as it reduces switching losses. Therefore, this topology is hoped to enable high power densities.

In this academic work, the topology is modeled using a mathematical description and its behavior is investigated.

From the resulting design rules, some designs are presented at the end of the thesis, which show that this topology is not ideal for the desired application.

The loss models created should give a short overview of the possible losses of this topology for the chosen design and application area.

Zusammenfassung

In dieser Arbeit wird eine galvanisch getrennte, quasi resonante Topologie auf ihre Einsatzmöglichkeiten untersucht.

Das Ziel dieser Untersuchung ist es festzustellen, ob diese Topologie eine Reihe von wesentlichen Anforderungen erfüllt. Dazu gehören ein vorgegebener Eingangsspannungsbereich sowie Ausgangsleistungsbereich.

Die in dieser Arbeit behandelte Topologie hat sich aus einem nicht isolierenden Resonanzwandler entwickelt.

Die hier beschriebene Wandlertopologie weist als Vorteil eine galvanische Trennung auf und hat außerdem in bestimmten Betriebszuständen das Soft-Switching Verhalten der Halbleiterschalter (MOSFET). Dies ist bei hohen Schaltfrequenzen von Vorteil, da dadurch Schaltverluste reduziert werden. Daher erhofft man sich, dass diese Topologie hohe Leistungsdichten ermöglicht.

In dieser Arbeit wird die Topologie mit Hilfe einer mathematischen Beschreibung modelliert und auf ihr Verhalten hin untersucht.

Aus den daraus resultierenden Entwurfsregeln werden am Ende der Arbeit einige Entwürfe präsentiert, die zeigen, dass diese Topologie für die gewünschte Anwendung nicht ideal ist.

Die erstellten Verlustmodelle sollen einen schnellen Überblick über die möglichen Verluste dieser Topologie für das gewählte Design und den Anwendungsbereich geben.

Acknowledgements

I would especially like to thank Ass. Prof. Dipl.-Ing. Dr. techn. Klaus Krischan whose patience and assistance has made the completion of this work possible.

Many thanks go to my family for always being there to support me.

Thanks to all of you.

Motivation

The desire and demand for smaller and more compact devices has always been present and is progressing. Therefore, there is an interest in reducing the size of converters while increasing the amount of power they can convert. This inevitably means that the energy density of converters is increasing. With improved and enhanced semiconductor components and improved manufacturing methods, the current task is to look for potential candidates of converter topologies that are suitable for high power densities.

In this thesis, a quasi-resonant converter is presented, which is inspired by the concepts of Cuk. The main goal is to find out whether such topologies are suitable for high power density designs.

Structure of this Thesis

The main aim of this thesis is the analysis of a topology and whether it meets certain key requirements.

The following topics are covered:

- Brief explanation of the topology
- State space description
- Analytical description of its behaviour
- Design rules
- Design attempts
- Conclusion

Key requirements

The converter that is the subject of this work must meet the following main requirements for applications in telecommunication.

- Power
  - 600 W at wide input range: 36 V to 75 V
  - 800 W at narrow input range: 40 V to 56 V
- Output voltage: 12 V (±2% ≡ ±240 mV)
- Single phase system
- Isolation requirements: 2.5 kV, galvanic
- Efficiency at $V_{in,nominal}$ = 54.5 V:
  - > 97% at 75% of Load (450 W)
  - > 96% at 100% of Load (600 W)
- Power density: 22 W cm^{-3}
- Switching frequencies above 500 kHz

Chapter 1

Introduction

The circuit shown in figure 1.1 has been presented by Slobodan Cuk. In his remarks, he points out that the transformer used is called a hybrid transformer due to its operating characteristics. Figure 1.2 shows how the currents are composed in this circuit. To convert from high input voltages to relatively low output voltages, Slobodan Cuk indicates that most converter topologies require cascaded converters, whereas this topology has the potential to accomplish this hurdle in one converter stage.

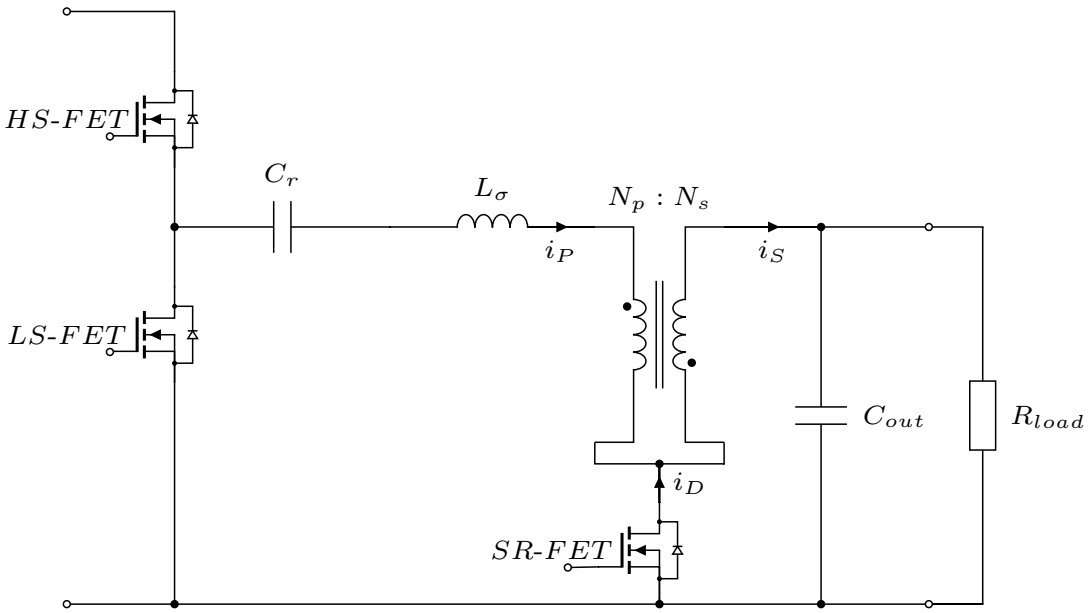

Figure 1.1: Basic hybrid switching converter [1–3]

Another benefit is constituted by the synchronous rectifier, as it can be switched on and off without current, which is referred to as currentless switching. This is very advantageous due to the elimination of switching losses. [1–3]

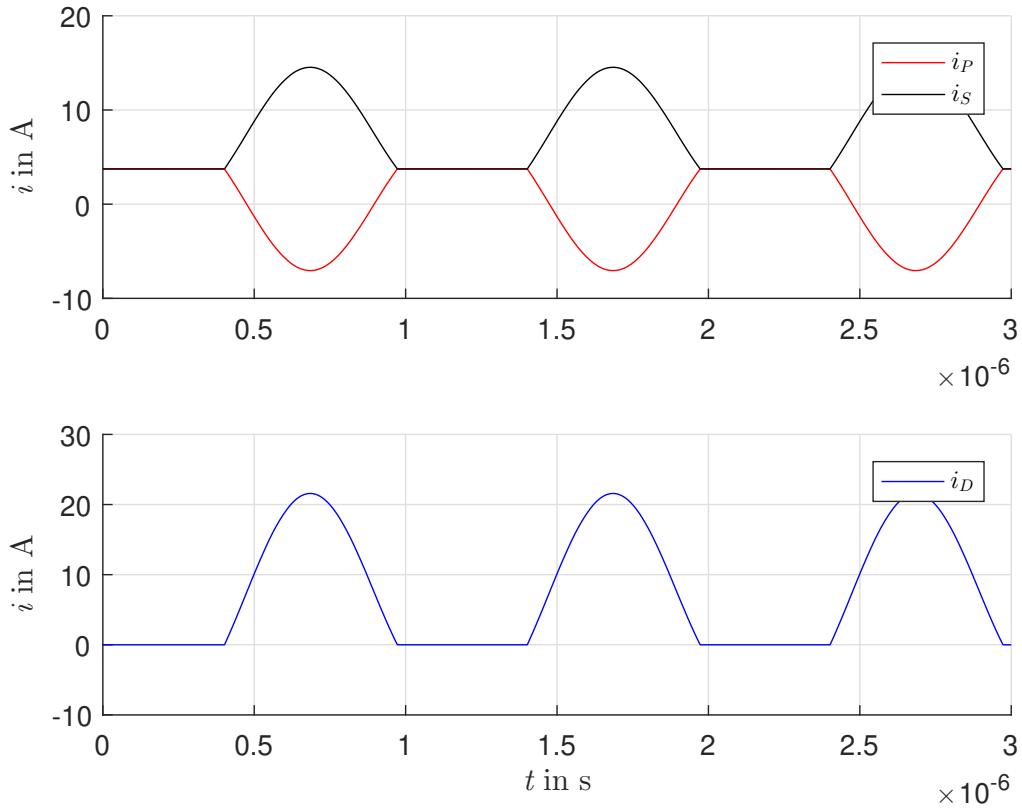

Figure 1.2: Hybrid transformer currents

At Infineon, the question arose whether this circuit could be redesigned to become a converter providing galvanic isolation. As a result, the following circuit 1.3 has been proposed. Since a crucial part of the circuit was set up in a different way, question to ask is what properties this topology must have, which marks the start of this thesis.
Naturally, the behaviour was expected to be different from that of the non-insulated variant, but it was hoped that some of the supposed advantages would also be found here.

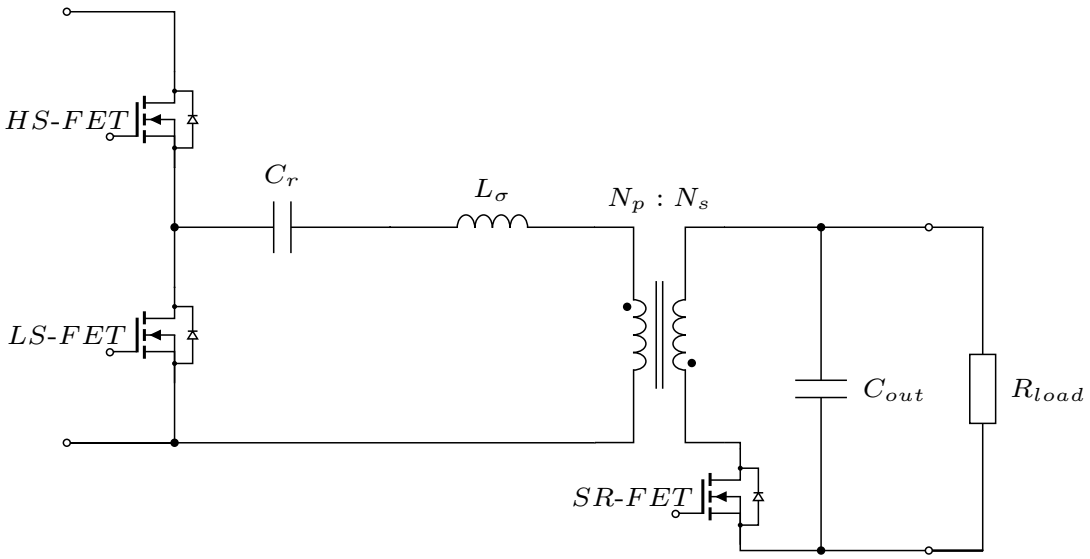

Figure 1.3: Proposal for an isolating converter based on figure 1.1

After initial simulations, it was decided to split the transformer into a transformer with a coupling factor close to 1 and a storage choke.
This results in a separation of the tasks in the converter.
Therefore the transformer has to be designed in such a way that it can only be used to transmit power as no energy should be stored in it.
This task is performed by the storage choke, which is now referred to as external magnetizing inductance.

The decision to separate these components contradicts the demand for the highest possible power density. Nevertheless, it was decided to do so based on the assumption that it would make it easier to set the individual parameters of the circuit, which in the long run would simplify the design process.

Figure 1.4 shows this modified circuit.

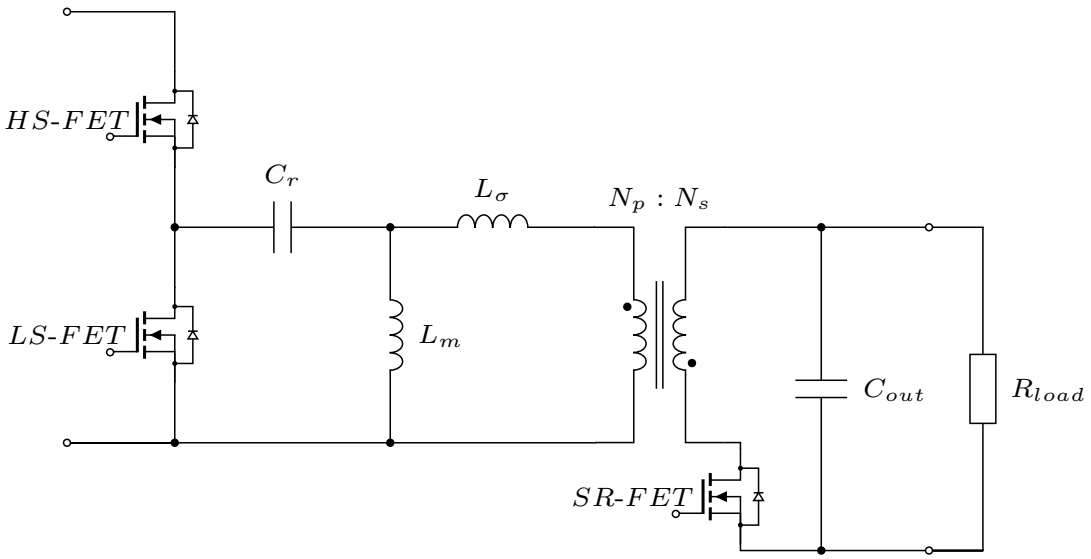

Figure 1.4: Proposal for an isolating converter with external magnetizing inductance

This converter consists of a half bridge at the input, followed by a capacitor C_r and an inductor L_m, which have the task to store energy for the conversion process.
This inductance is the external magnetisation inductance L_m.
The leakage inductance L_σ of the transformer is of crucial importance for the conversion process and therefore taken into account.
The transformer has the function of transferring energy from the primary to the secondary side and is in no way used as energy storage.
The circuit viewed in a simplified way, the switch on the secondary side can be treated like a diode, which is why it is also called synchronous rectifier.
The output then only consists of a capacitor as an output filter.
The total count of switches in this topology is therefore three which are referred to as:

- high-side switch (HS)
- low-side switch (LS)
- synchronous-rectifier (SR)

Chapter 2

Principle of Operation

This converter has two intervals determined by the on and off intervals of the two active switches of the half bridge.Which are called t_{on} and t_{off} interval. In figure 2.1 below, the currents of these two intervals are marked with red and green arrows.

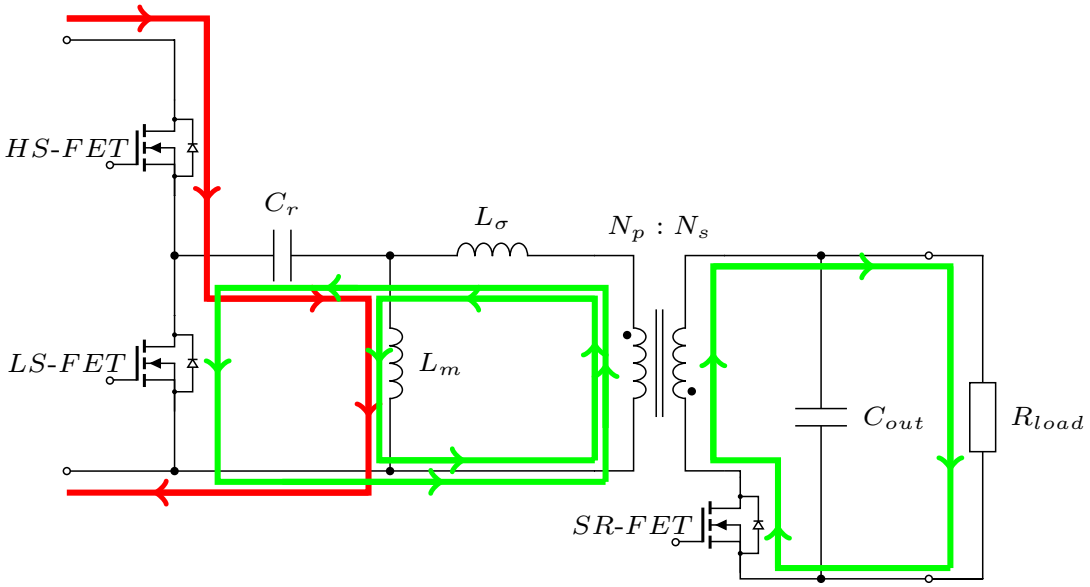

Figure 2.1: Principle of operation of topology

t_{on}-*Mode* **(HS on)**

In this operation mode, the high side switch of the half bridge is turned on. The current flow described that occurs in the t_{on}-*Mode* is shown in red:

- The current flows from the input potential via the active HS switch, through the resonance capacitor C_r and the external magnetising inductance L_m.
- C_r is charged, L_m is energized.
- The current should start slightly negative and rise steadily until a certain level is reached. The peak current at the end of this operation mode defines the energy stored in the converter and thus the output power.
- At the end of the t_{on}-*Mode* the HS switch is turned off and the output capacitor of the HS MOSFET is charged because of the current while the output capacitor of the LS MOSFET is discharged. Therefore it is possible to perform zero-voltage-switching of the half bridge ($ZVS_{HB}@HS \rightarrow LS$).
- In theory, the output capacitance of the SR is also discharged and can be switched on under a zero voltage condition ($ZVS_{SR}@turnOn$).

t_{off}-*Mode* (LS and SR on)

In this operation mode, the HS switch is switched off but the LS switch and SR are switched on. The current flow described that occurs in the t_{off}-*Mode* is shown in green in figure 2.1.

This t_{off}-*Mode* consists of three sub operation modes performed by C_r and L_m.

- Sub-mode 1: At the beginning of the t_{off}-*Mode*
  - Due to the changed half bridge voltage, a current begins to flow through the transformer, which consequently charges the output capacitor. The leakage inductance L_σ of the transformer prevents a sudden increase in the current.
  - The current through L_m drops constantly.
  - The current through C_r falls but starts to deviate from the current passing through L_m; this difference is caused by the current which flows through the primary winding of the transformer.
- Sub mode 2: This operation mode starts when the current through C_r becomes negative
  - In this situation the currents through C_r and L_m add up and thus both contribute to a higher energy transfer via the transformer.
  - C_r and L_σ are parts of a resonance oscillator, so the current through these components rises and falls in a sinusoidal shape.
- Sub mode 3: This operation mode starts when the current through L_m becomes negative
  - C_r is currently the only energy source that still has energy left.
  - As C_r starts energising L_m with current in reverse direction, the current through the transformer continues to decrease.
  - t_{off}-*Mode* ends when the currents from C_r and L_m are equal. This means that the current across the transformer becomes zero which is when the SR switches off ($ZCS_{SR}@TurnOff$).
  - At the end of this mode the LS switch is turned off and the negative current through C_r charges the output capacitor of the LS and discharges

the HS switch which makes it possible to switch again under a zero voltage condition (ZVS_{HB}@$LS \rightarrow HS$).

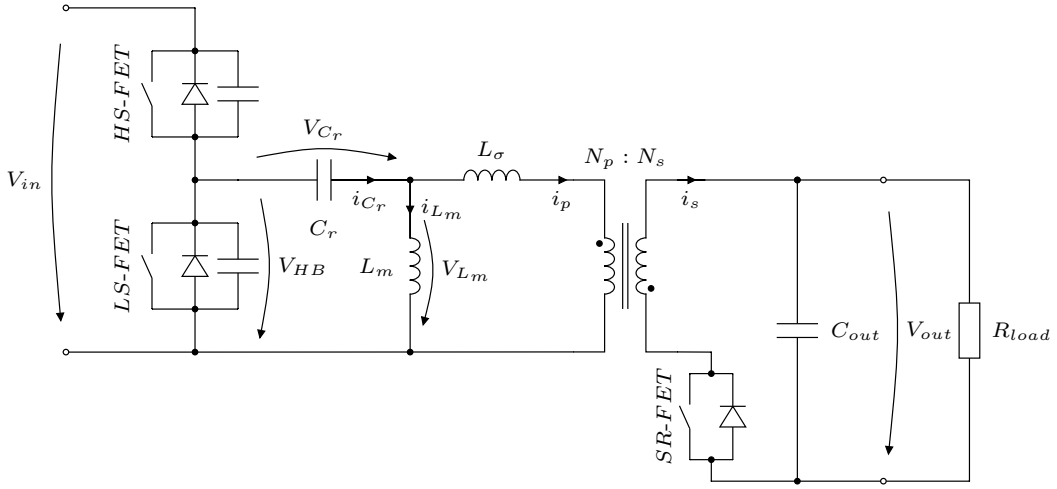

Figure 2.2: Equivalent circuit of this topology

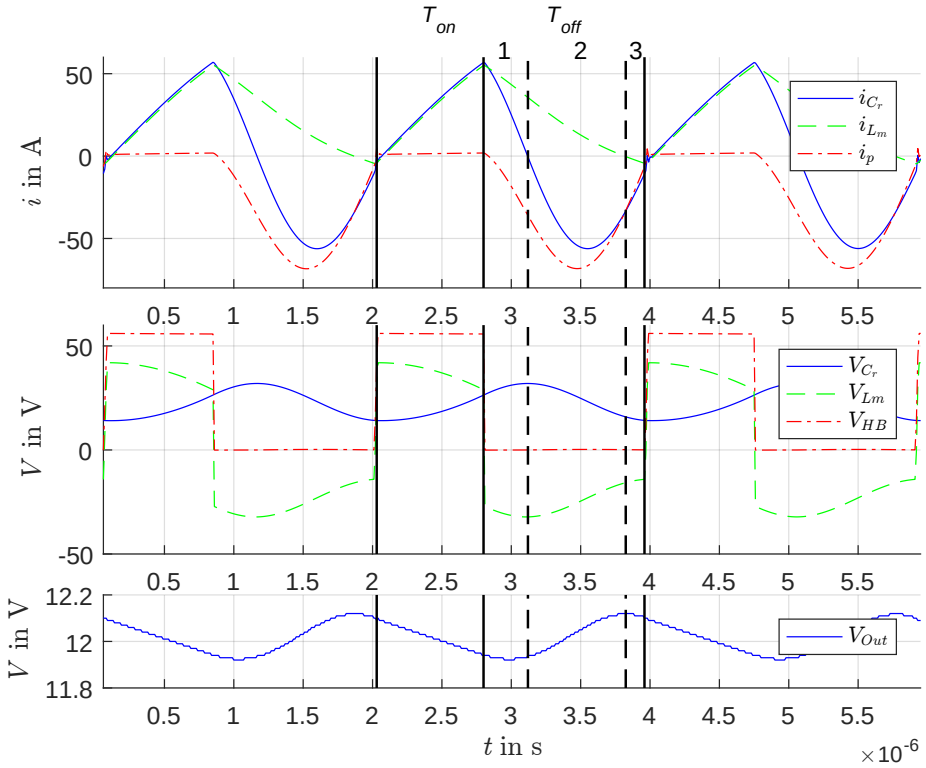

Figure 2.3: Typical voltage and current curves of this topology

Chapter 3

State Space Model

A state space model is created to describe the general behaviour of the converter and its relationships. Which will then be used for further analysis.
To describe its general behaviour, the complexity of the model is reduced to its minimum.
Therefore the model is initially assumed to be lossless, lossy components such as resistance and iron core loss are neglected until further notice.
The equivalent circuit diagrams of the semiconductor switches are also reduced to simple switches. Consequently, output capacitors of the Mosfets are not taken into account. As a result, the switching behaviour of the half bridge cannot be considered here, which will be later explored explicitly.

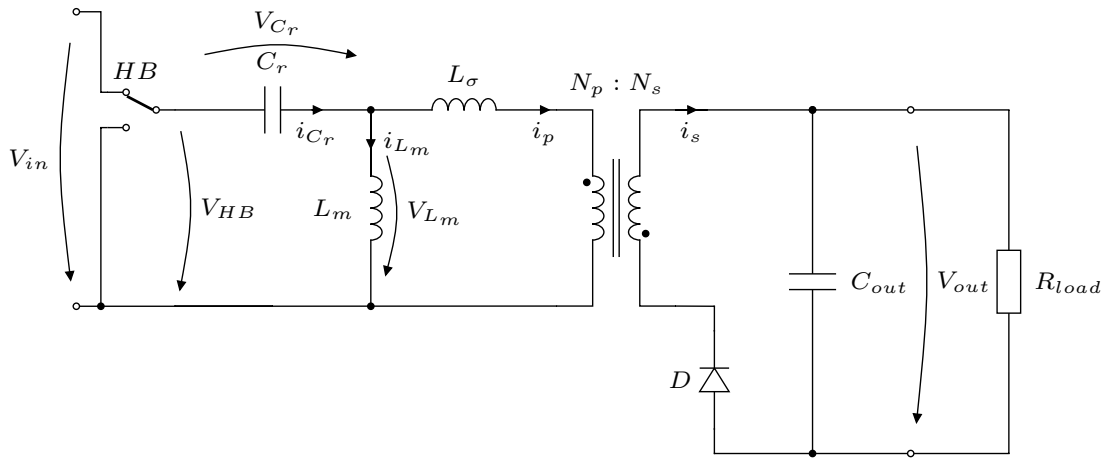

Figure 3.1: Simplified equivalent circuit

The half bridge is modeled with an ideal alternating switch and the synchronous rectifier with an ideal diode. To further reduce the complexity of the analysis, the magnetizing inductance of the transformer is assumed to be infinite. The resulting simplified equivalent circuit is shown in Figure 3.1.

A linear, time-invariant system serves as the model for this circuit. The resulting state space model is described by the following equation 3.1, in which $\mathbf{x}$ is the state vector, $\mathbf{A}$ is the system matrix, and $\mathbf{b}$ is the input vector.

$$\frac{d\mathbf{x}}{dt} = \mathbf{A}_i\mathbf{x} + \mathbf{b}_i u \tag{3.1}$$

For each switch position of the half bridge a separate state space model is needed. In the equation 3.1 the model parameters are indexed to indicate this fact.

3.1 State Space Model - t_{on}-*Mode* (HS on)

The equivalent circuit for the first switch position is quite simple. It essentially consists of two separate circuits. The simplified equivalent circuit for the T_{on} *mode* is shown in Figure 3.2. At the input, the supply voltage acts on a series connection of capacitor and inductance. At the output, the load resistance is supplied by the loaded output capacity.

Due to the fact that the synchronous rectifier is open, no energy can be transmitted via the transformer. Nevertheless, a current can flow through the primary side of the transformer and the associated leakage inductance. Since an external magnetizing inductance is proposed for this topology, it is further assumed that the main current path runs via the external magnetizing inductance and not via the primary side of the transformer. There will always be a small current energizing the core of the transfer transformer, but it should be negligible.

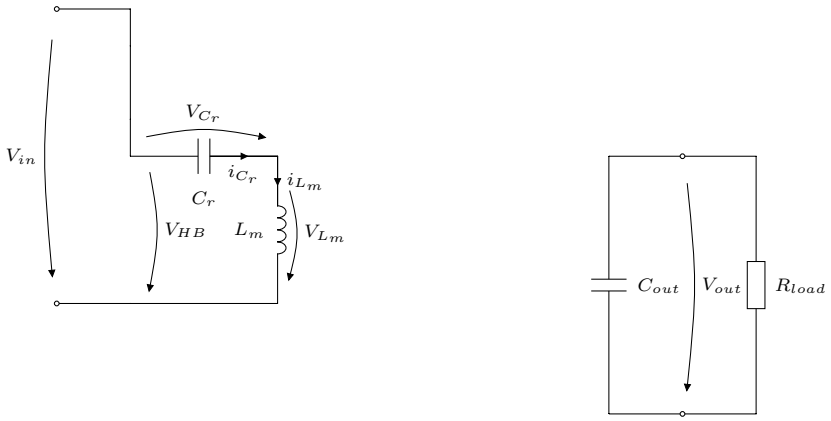

Figure 3.2: Simplified equivalent circuit, t_{on}-*Mode* (HS on)

Equation 3.2 is the mathematical expression of this state space model.

$$\begin{bmatrix} \dot{v_{C_r}} \\ \dot{i_{L_m}} \\ \dot{i_p} \\ \dot{v_{C_{out}}} \end{bmatrix} = \begin{bmatrix} 0 & C_r^{-1} & 0 & 0 \\ -L_m^{-1} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -(R_{load} \cdot C_{out})^{-1} \end{bmatrix} \cdot \begin{bmatrix} v_{C_r} \\ i_{L_m} \\ i_p \\ v_{C_{out}} \end{bmatrix} + \begin{bmatrix} 0 \\ L_m^{-1} \\ 0 \\ 0 \end{bmatrix} \cdot V_{in} \tag{3.2}$$

3.2 State Space Model - t_{off}-*Mode* (LS and SR on)

The equivalent circuit for the second switch position is shown in Figure 3.3.

The current through the leakage inductance and the primary side of the transformer is assumed to be 0 A at the beginning of this t_{off}-*Mode*. Initially the current begins to rise quasi-sinusoidally and energy is transferred to the other side. Due this sinusoidal current swing, after a while the current crosses the 0 A line and marks the end of this operation mode.

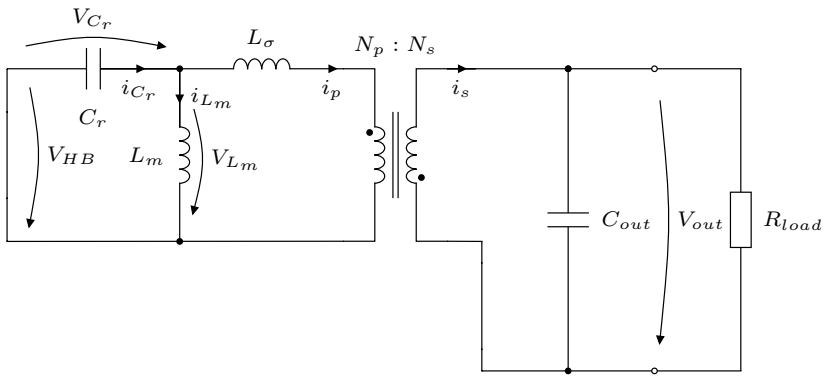

Figure 3.3: Simplified equivalent circuit, t_{off}-*Mode* (LS and SR on)

Equation 3.3 is the mathematical expression of this state space model.

$$\begin{bmatrix} \dot{v_{C_r}} \\ \dot{i_{L_m}} \\ \dot{i_p} \\ \dot{v_{C_{out}}} \end{bmatrix} = \begin{bmatrix} 0 & C_r^{-1} & C_r^{-1} & 0 \\ -L_m^{-1} & 0 & 0 & 0 \\ -L_\sigma^{-1} & 0 & 0 & \frac{N_P}{N_S} \cdot L_\sigma^{-1} \\ 0 & 0 & -\frac{N_P}{N_S} \cdot C_{out}^{-1} & -(R_{load} \cdot C_{out})^{-1} \end{bmatrix} \cdot \begin{bmatrix} v_{C_r} \\ i_{L_m} \\ i_p \\ v_{C_{out}} \end{bmatrix} \tag{3.3}$$

3.3 State Space Simulation

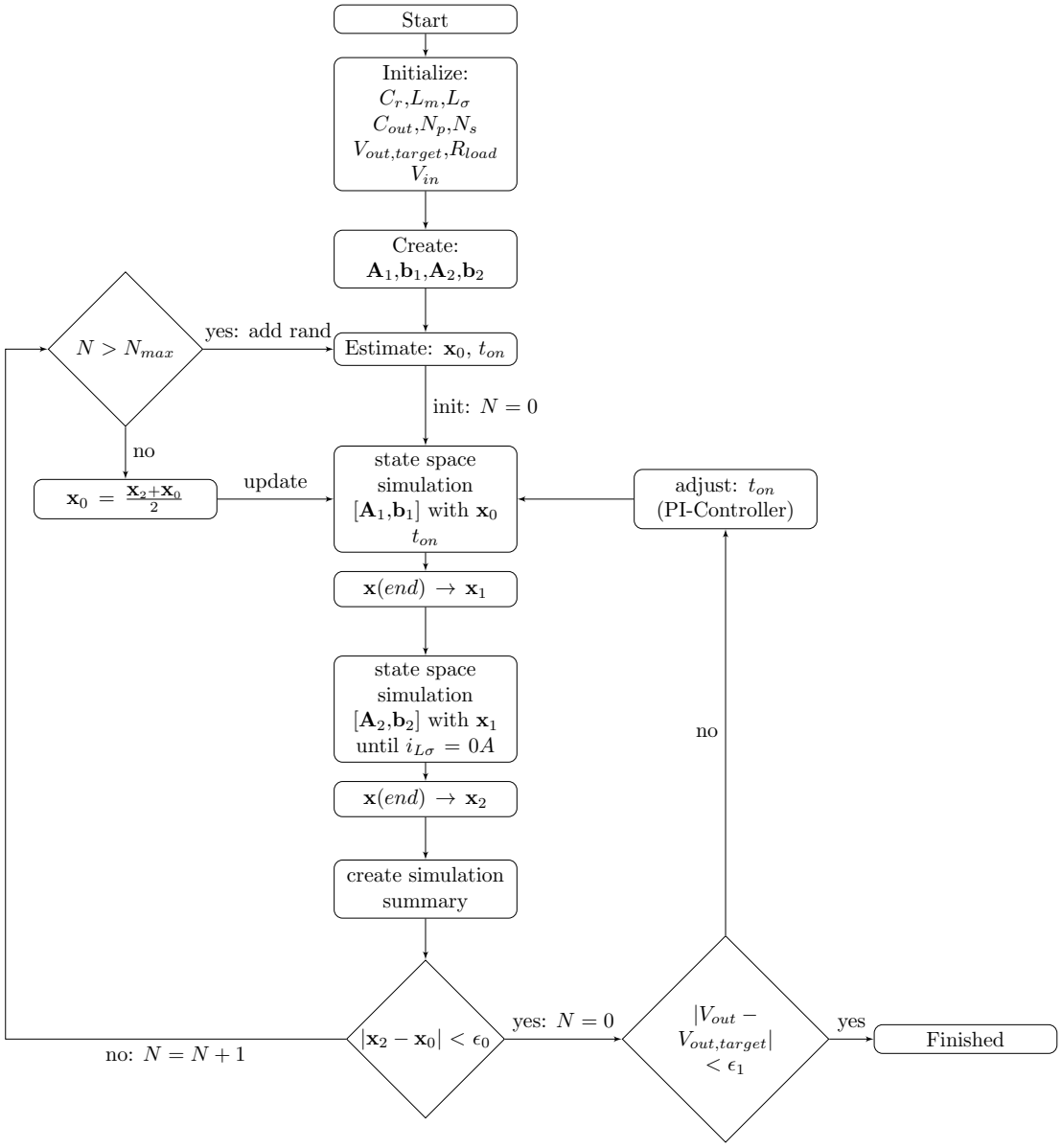

Figure 3.4: Matlab: State space simulator / steady state finder

The goal of the state space simulation is to get the waveforms of the converter's currents and voltages, mainly for analysis and later for design purposes as well as to find proper timing values for t_{on} and t_{off}.

It is particularly hard to find an analytical description for the t_{off} duration.

However through simulation this value can be found quite simply.
To make this work the values of the parts (C_r, L_σ, L_m, $\frac{N_p}{N_s}$, C_{out}) have to be given, as well as the supply voltage V_{in}. A target has to be defined, for instance the output voltage $V_{out,target}$. In combination with the right choice of the output load R_{load} the output power is indirectly defined by that as well.
The flowchart 3.4 is a brief explanation of how to find a steady-state solution that achieves the target output voltage.

The state space simulation is enirely done in Matlab via the built in linear simulation tool *lsim()*.
After creating the needed Matrices and Vectors A, b for the first and second mode of the converter the initial conditions x_0 have to be estimated. The proper selection of the initial conditions increases the chance of faster reaching a steady state operation.

$$\mathbf{x}_0 = \begin{bmatrix} v_{C_r,0} \\ i_{L_m,0} \\ i_{L_{p,0}} \\ v_{C_{out,0}} \end{bmatrix} = \begin{bmatrix} V_{out,target} \cdot \frac{N_S}{N_P} \\ V_{out,target} \cdot \frac{1}{R_{load}} \cdot \frac{N_P}{N_S} \\ 0 \\ V_{out,target} \end{bmatrix} \tag{3.4}$$

The very first state space simulation begins with the default initial condition values 3.4. The t_{on} duration for this first part of the period has to be estimated as well. How those estimations are derived will be shown in the next chapter.

After the initial steps the first simulation run is be performed. First, the state space simulation of the t_{on}-*Mode* is executed. Its last value of the time series $x(end)$ is then used as the initial condition for the second state space simulation the t_{off}-*Mode*. As shown in the flow chart, the state variable of the second simulation is then used for comparison. In the steady state of a converter operation the start condition must match the end condition.

$$|\mathbf{x}_2 - \mathbf{x}_0| < \epsilon_0 \tag{3.5}$$

If those state variables are too far apart, their averages will become the new initial condition for the next simulation round. This has been proven to be quite an efficient method of speeding up the steady state finding problem.

$$\mathbf{x}_0^{new} = \frac{\mathbf{x}_2 + \mathbf{x}_0}{2} \tag{3.6}$$

If the steady state does not appear after a certain number of runs, new randomly chosen initial conditions have to be used instead.

In case that the steady state has been reached, the output voltage is averaged over one full period and compared to the target output voltage. If it deviates too much, this value is fed into a PI-Controller as an error and the t_{on} duration is adjusted for the next steady state finding cycle.

This double loop structure, while not time efficient, almost always finds the correct t_{on} values for the given set of component values and target output voltage.

Chapter 4

Analytical Description of the Circuit

4.1 Approximation of the Duration of t_{off}-*Mode*

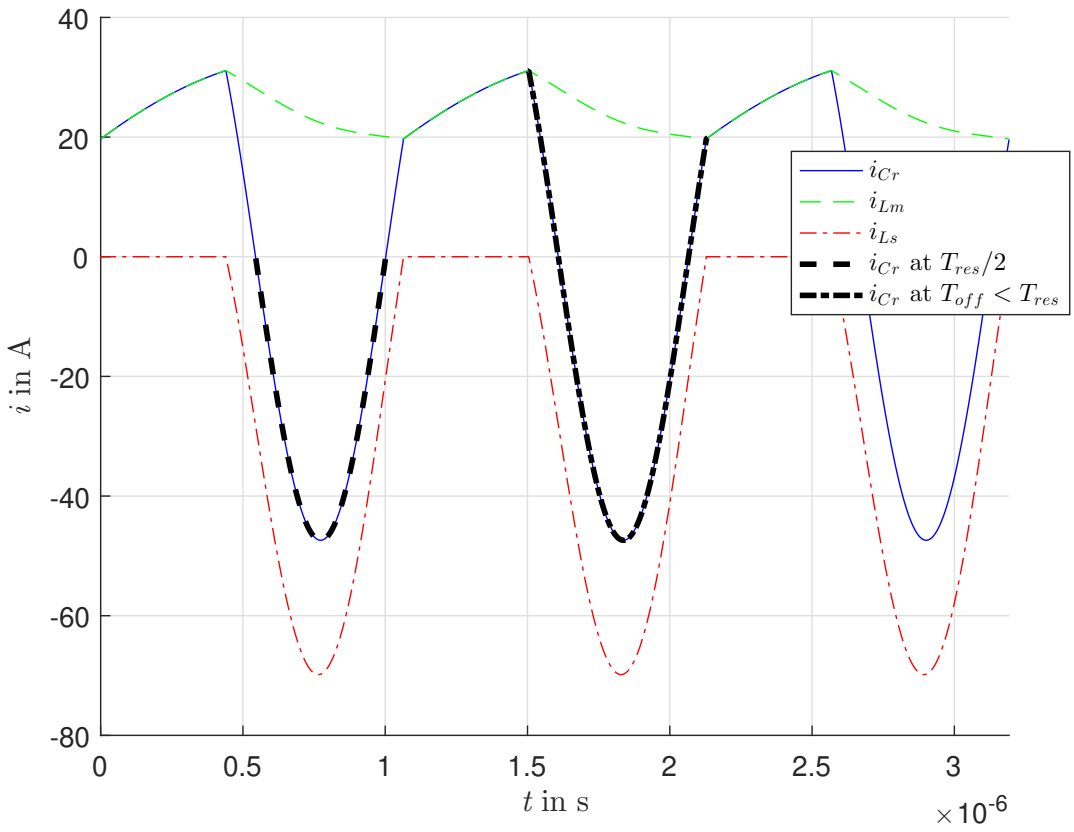

Figure 4.1: Typical current waveform in the linear model

Since an oscillation process between inductors and capacitors occurs during the t_{off}-*Mode*, this mode is also referred to as the resonance mode. The duration of this oscillation process, is kept in a fixed range and can be calculated quite well. However, due to the non-linear behaviour of inductors with an iron core and air gap, this time span can only be calculated approximately. The duration of the t_{off}-*Mode* depends on the initial conditions of the mode and the component elements of the circuit.

As shown in black dashed lines in Figure 4.1, the current flowing through the resonance capacitor C_r executes a sinusoidal swing whose frequency can be computed and thus the limits of this period can be estimated.

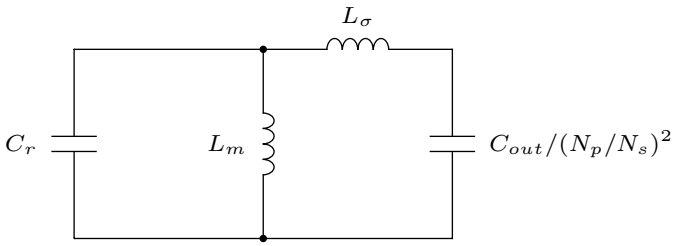

Figure 4.2: Reduced linear model for resonant frequency calculation

This model 4.2 is used to calculate the impedance, from which the resonance frequency can then be calculated.

$$\omega^4 \cdot C_r L_m L_\sigma C_{out} \frac{N_s^2}{N_p^2} + \omega^2 \cdot (-L_\sigma C_{out} \frac{N_s^2}{N_p^2} - C_r L_m - L_m C_{out} \frac{N_s^2}{N_p^2}) + 1 = 0 \tag{4.1}$$

The solution of the angular frequency from equation 4.1 is solved as follows.

$$k_1 = -L_\sigma C_{out} \frac{N_s^2}{N_p^2} - C_r L_m - L_m C_{out} \frac{N_s^2}{N_p^2} \tag{4.2}$$

$$k_2 = C_r L_m L_\sigma C_{out} \frac{N_s^2}{N_p^2} \tag{4.3}$$

$$\omega_{res} = \sqrt{\frac{\pm\sqrt{k_1^2 - 4k_2} - k_1}{2k_2}} \tag{4.4}$$

$$f_{res} = \frac{\omega_{res}}{2\pi} \tag{4.5}$$

$$T_{res} = \frac{1}{f_{res}} = 2\pi\sqrt{\frac{2k_2}{\pm\sqrt{k_1^2 - 4k_2} - k_1}} \tag{4.6}$$

Figure 4.1 shows that the duration of the t_{off}-*Mode* can only be between $T_{res}/2$ and T_{res}.

$$\frac{T_{res}}{2} < t_{off} < T_{res} \tag{4.7}$$

4.2 Zero-voltage Switching Capability of the Half Bridge

Zero-voltage switching (ZVS) from the HS to the LS of the half bridge can always be achieved, whereas switching from the LS to the HS depends on the design of the circuit. It is obvious that ZVS is desired whenever possible, especially for high frequency converters, and therefore care must be taken during the design phase to accomplish this behaviour.

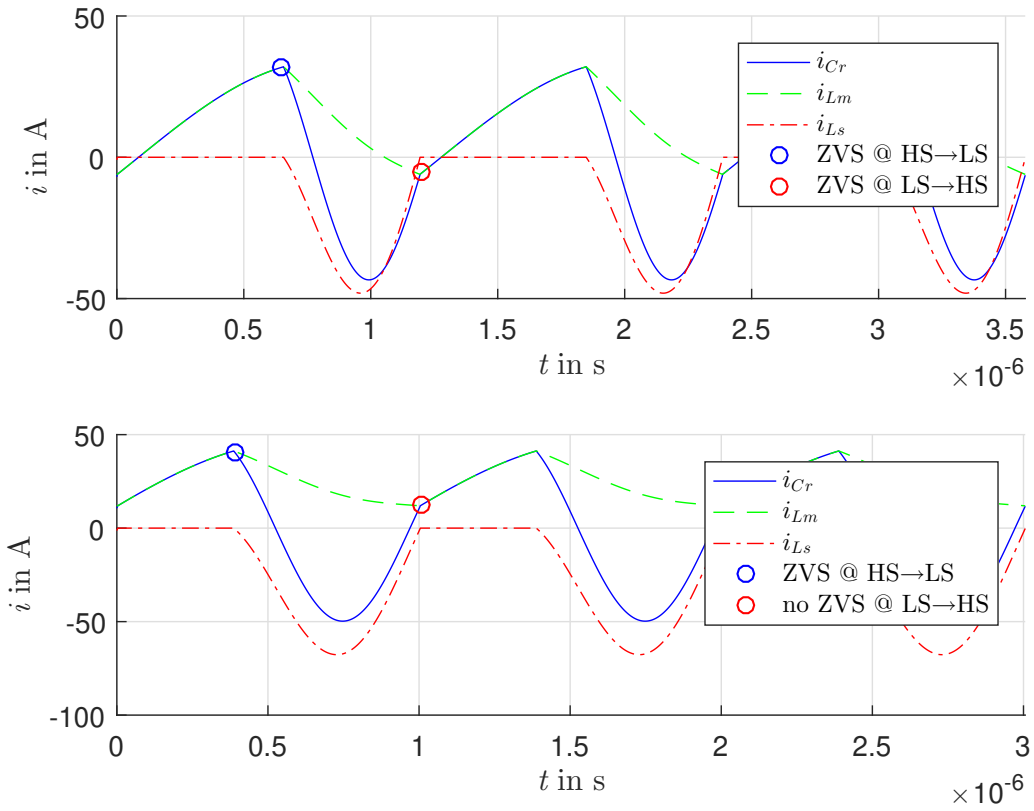

Figure 4.3: typical current curve with and without ZVS

In figure 4.3 the switching instants are indicated with circles. The current curve i_{Cr} of the first subplot shows that the current curve can always be used to charge the drain source capacitors of the MOSFETS of the half bridge. The second subplot shows that only the switch from HS to LS works under the ZVS condition.

At the end of the second operation mode (t_{off}-*Mode*) the current through L_m should get slightly negative, just enough to achieve ZVS from LS to HS.

The sum of all power MOSFET output capacitances are used to create a design constraint for the ZVS behaviour for LS to HS and for the calculation of the minimum current needed in the magnetising inductor.

$$\frac{L_m \cdot I_{L_m}^2}{2} = E_{L_m} > E_{C_{oss}} = \frac{C_{oss,\Sigma} \cdot V_{in}^2}{2} \tag{4.8}$$

$$|I_{L_m}| > V_{in} \cdot \sqrt{\frac{C_{oss,\Sigma}}{L_m}} \tag{4.9}$$

$$I_{L_m} < -V_{in} \cdot \sqrt{\frac{C_{oss,\Sigma}}{L_m}} \tag{4.10}$$

The minimum amount of negative current i_{L_m} needed to reach ZVS can be seen in equation 4.10.

The output capacitance of the MOSFET is a function of the drain-source voltage. Hence, this must be taken into account accordingly in the above-mentioned calculation.

$$C_{oss,\Sigma} = C_{oss,HS}(V_{IN}) + C_{oss,LS}(0V) \tag{4.11}$$

4.3 Optimal Duty Cycle

Due to the fact that energy is only transferred to the output in the t_{off}-*Mode* the transformer current looks similar to the one shown in figure 4.4. The shape of the current of the primary and secondary windings of the transformer are similar, which is why only the primary current is considered here. The shape of the current is not perfectly sinusoidal, but is assumed to be so for simplicity. As already mentioned, due to the topology, energy is only transmitted in the second mode, which leads to the chopped-off semisine-shaped current profile through the transformer.

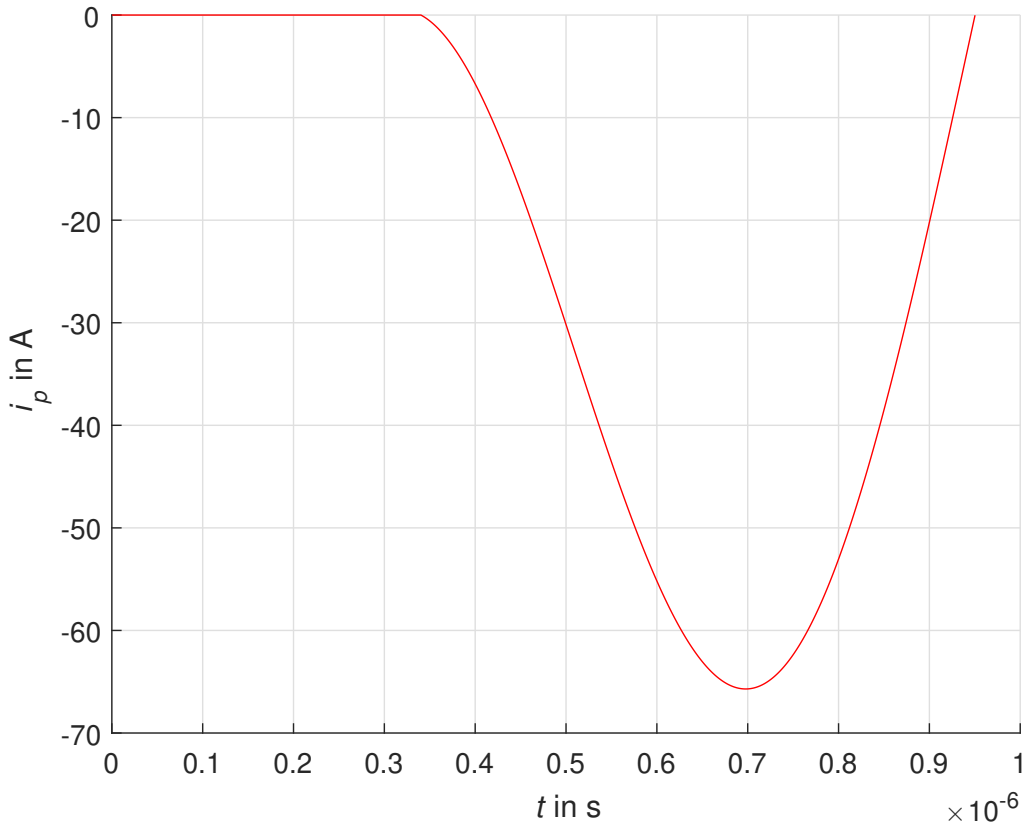

Figure 4.4: Transformer current

The idea is that because of the i^2R losses, it is desirable to flatten this shape as much as possible to aim for the lowest possible current peak.

In other words, the root mean square value of the current, viewed over the converter period, should be as small as possible.

The duty cycle is defined as:

$$d = \frac{t_{on}}{t_{on} + t_{off}} \tag{4.12}$$

As for the root mean square value of the current the following holds true:

$$I_{RMS} = \sqrt{\frac{1}{T}\int_{t_{on}}^{T}\left[-I_{peak}\cdot\sin\left(\frac{\pi}{t_{off}}\cdot(t-t_{on})\right)\right]^2 dt} = I_{peak}\cdot\sqrt{\frac{1-d}{2}} \tag{4.13}$$

The mean value can be given as follows:

$$I_{mean} = \frac{1}{T}\int_{t_{on}}^{T} -I_{peak}\cdot\sin\left(\frac{\pi}{t_{off}}\cdot(t-t_{on})\right)dt = -I_{peak}\cdot(1-d)\cdot\frac{2}{\pi} \tag{4.14}$$

In view of comparing this calculation under the premise of the same output power, the formulae set out above are now combined.

$$\begin{aligned} P_{out} = V_{out}\cdot I_{out} &= V_{out}\cdot I_{mean} \\ &= V_{out}\cdot I_{peak}\cdot(1-d)\cdot\frac{2}{\pi} \\ &= V_{out}\cdot I_{RMS}\cdot(1-d)\cdot\frac{2}{\pi}\cdot\sqrt{\frac{2}{1-d}} \end{aligned} \tag{4.15}$$

After rearranging, the RMS value is as follows:

$$I_{RMS} = \frac{P_{out}}{V_{out}}\cdot\frac{\pi}{\sqrt{8\cdot(1-d)}} \tag{4.16}$$

$$\frac{I_{RMS}}{I_{mean}} = \frac{\pi}{\sqrt{8\cdot(1-d)}} \tag{4.17}$$

According to (4.17), the I_{RMS} is small for small duty cycle values of d. In other words, the longer the t_{off}-*Mode* takes, the lower I_{peak} becomes and therefore the $i^2\cdot R$ losses decrease.

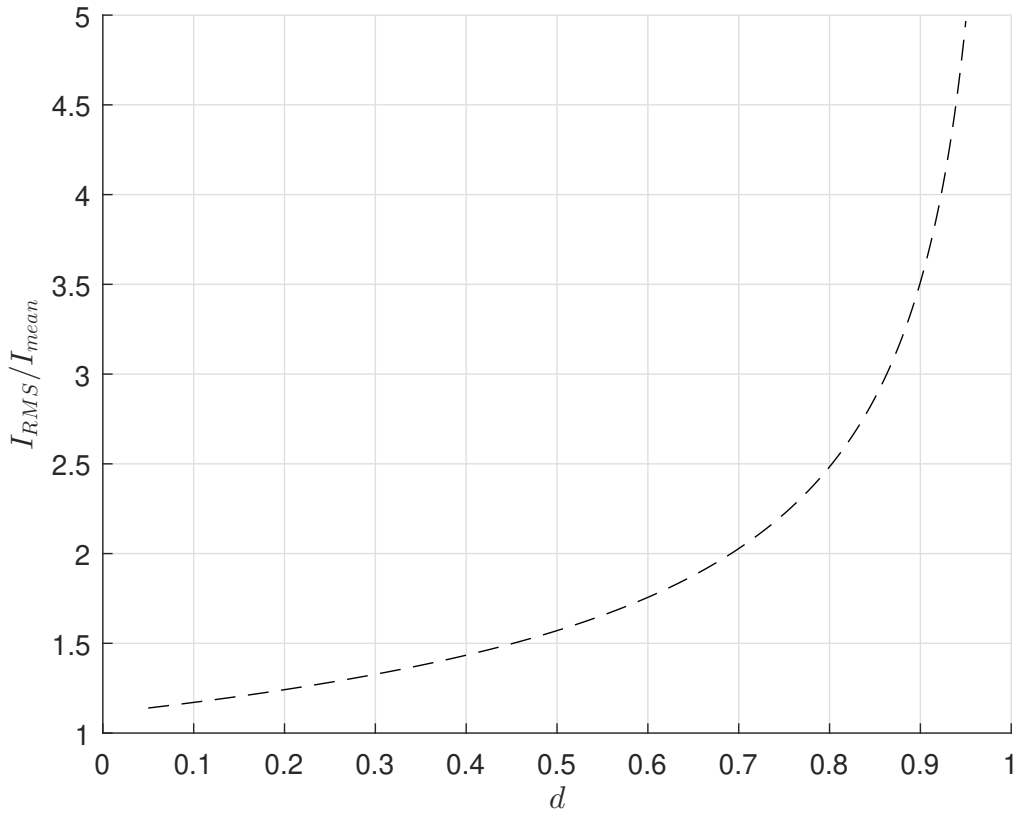

Figure 4.5: $\frac{I_{RMS}}{I_{mean}}$ vs duty cycle

4.4 Input-output Voltage Relationship

Now the relationship between input voltage and output voltage will be derived.

To conduct this calculation, it is assumed that the converter is in a steady state. This means that all considered currents and voltages at the beginning of a conversion cycle and at the end of the conversion cycle are of the same value.

$$\mathbf{x}(0) = \mathbf{x}(T) \tag{4.18}$$

This is of particular interest for the currents through the inductors L_m and L_σ. Since the same is valid for all inductances, L is used as a placeholder in the following description.

Due to the steady state, the following relation 4.19 holds.

$$i_L(0) = i_L(T) \tag{4.19}$$

The differential equation given in 4.20 describes the relationship between the voltage v_L and the current i_L of the inductance.

$$\frac{di_L}{dt} = \frac{1}{L} \cdot v_L \tag{4.20}$$

If equation 4.20 is converted and integrated over the period of an entire conversion cycle T, it must be concluded that the mean voltage across an inductance in the steady state must be 0V, otherwise the previously assumed assumption about the steady state would not be true.

$$\int_0^T di_L = \frac{1}{L} \int_0^T v_L \cdot dt \tag{4.21}$$

$$i_L(T) - i_L(0) = \frac{1}{L} \int_0^T v_L \cdot dt = 0 \tag{4.22}$$

$$\frac{1}{L} \int_0^T v_L \cdot dt = 0 \rightarrow \overline{v_L} = 0 \tag{4.23}$$

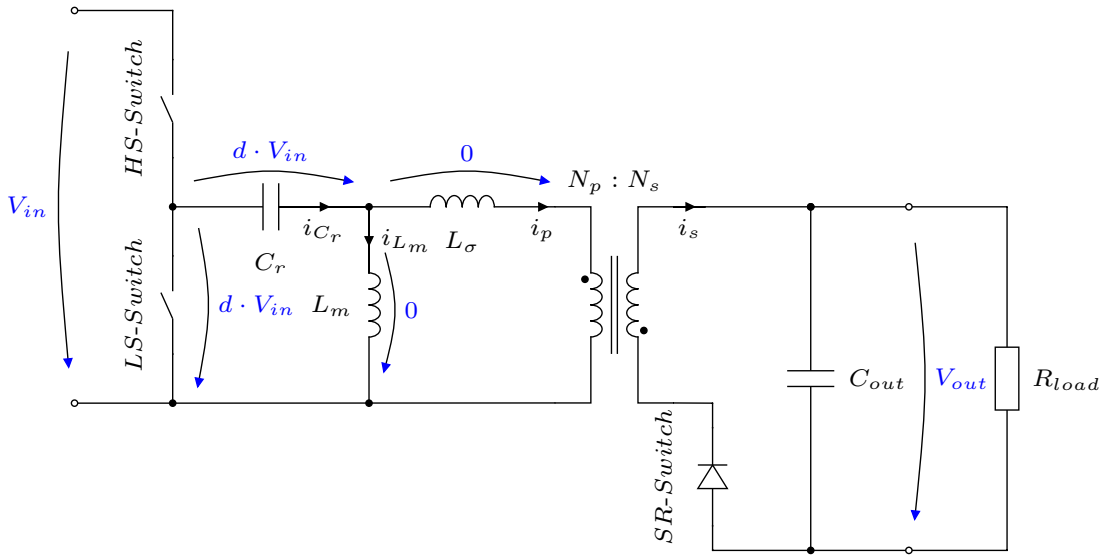

Figure 4.6: Average voltages

Therefore, the mean voltages $\overline{v_{L_m}}$ and $\overline{v_{L_\sigma}}$ of the inductors are 0V.

$$\overline{v_{L_m}} = 0 \tag{4.24}$$

$$\overline{v_{L_\sigma}} = 0 \tag{4.25}$$

In figure 4.6 the mean voltages of the components are shown in blue. The average voltage at the output of the half bridge can be written as shown in equation 4.26.

$$\overline{v_{in}} = d \cdot V_{in} \tag{4.26}$$

According to the *2nd* Kirchhoff's law, the following loop applies.

$$\overline{v_{in}} = \overline{v_{C_r}} + \overline{v_{L_m}} \tag{4.27}$$

As a result, the average voltage of the capacitor C_r can be expressed as follows.

$$\overline{v_{C_r}} = d \cdot V_{in} \tag{4.28}$$

Next, the t_{off}-*Mode*, in which energy is transmitted to the output, is considered. Due to the switching position of the half bridge, the capacitor C_r is connected in parallel to the inductor L_m, causing it to have the voltage of the resonant capacitor v_{C_r}.
Because of the blocked diode, no current can flow through the leakage inductance, which means that its voltage is 0V. In the second mode, current begins to flow across the leakage inductance. Since the average voltage of an inductance must be 0 V, the average voltage $\overline{v_{L\sigma}}$ in this second phase must be 0 V.
It can be shown that the voltage on the primary side of the transformer corresponds to $V_{Cr} = d \cdot V_{in}$ while voltage on the secondary side is equivalent to V_{out}. The implication is as follows:

$$\overline{v_{C_r}} = \frac{N_P}{N_S} \cdot \overline{v_{out}} \tag{4.29}$$

Equation 4.29 and 4.28 can be equated, resulting in the input-output relationship equation viewed in 4.30.

$$\overline{v_{out}} = \frac{d}{\frac{N_P}{N_S}} \cdot V_{in} \tag{4.30}$$

Consequently, the output voltage of the converter is a function of the turns ratio, the duty cycle and the input voltage.

$$V_{out} = \frac{d}{\frac{N_P}{N_S}} \cdot V_{in} \tag{4.31}$$

Chapter 5

Design Considerations

This section describes and explains the design steps performed. It is most important to reach the targets and stick to them as much as possible.

5.1 Target Specifications

The targets are listed in the chapter Motivation, Key Requirements on page XV.

The following key requirements are of interest in this section.

- Power
  - $600W$ at wide input range: $36V$ to $75V$
- Output voltage: $12V$ ($\pm 2\% \equiv \pm 240mV$)
- Efficiency at $V_{in,nominal} = 54.5V$:
  - $> 97\%$ at 75% of Load (450W)
  - $> 96\%$ at 100% of Load (600W)

The following design process tries to meet these key requirements.

5.2 Transformer

5.2.1 Turns Ratio $a = \frac{N_p}{N_s}$

This section deals with the question, which turns ratio is optimal considering the wide input voltage range, and tries to keep the best possible duty cycle values at the same time.

$$a = \frac{N_p}{N_s} \tag{5.1}$$

$$V_{out} = \frac{d}{a} \cdot V_{in} \rightarrow a(V_{in}, d) = \frac{V_{in}}{V_{out}} \cdot d \tag{5.2}$$

The function $a(V_{in}, d)$ shown in (5.2) is used to show which relationships are possible between input voltage, duty cycle and turns ratio.

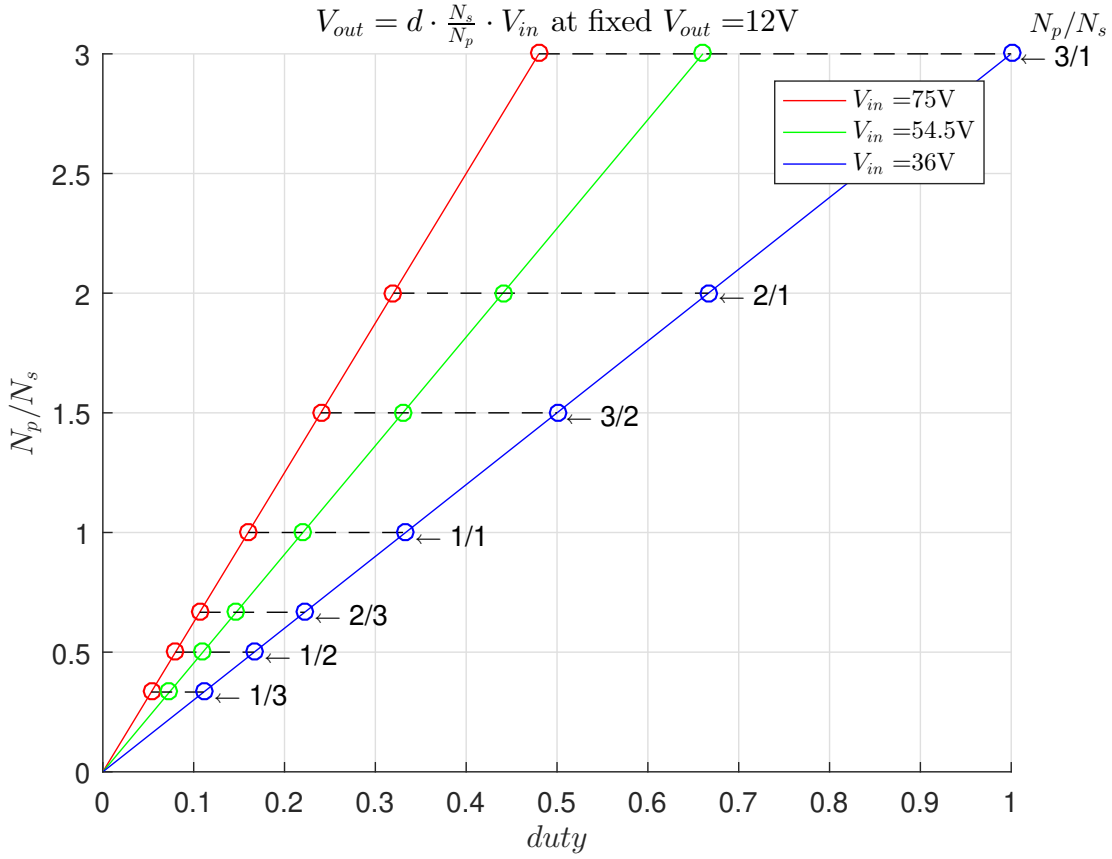

Figure 5.1: Turns ratio

The relationship described by equation 5.2 is shown in Figure 5.1. From chapter 4.3 it is known that it makes sense to aim for the smallest possible duty cycle due to the potentially smaller RMS currents. Accordingly, all those options that appear further left are to be preferred.
Although lower duty cycles are preferable in terms of lower RMS currents, the effective duty cycle range narrows down significantly, thus making it hard to

control the converter due to the timing differences of the t_{on}-*Mode* becoming too small. It can be concluded that a different approach must be found for the selection of a suitable duty cycle.

By looking at figure 5.1, it is simply deduced that the turns ratio $N_p/N_s = 3/1$ cannot be used with these requirements, since it would require a duty cycle d of 1 at an input voltage V_{in} of $36V$, which is not possible. However, what can be deduced is that only winding ratios below 3/1 work.

In the following sections an attempt is made to deduce the optimal turns ratio in order to minimize the copper and the core losses of the transformer. Figure 5.2 shows the relationship between copper and core losses versus peak AC flux density [4, p.568]. In addition to the optimal turns ratio, other parameters of the transformer must also be taken into account. This means the goal is to find a design of winding ratio and PCB design that has the potential to cause the most optimal, so to say, the lowest losses in the transformer. The windings of the planar transformer are realized with a printed circuit board.

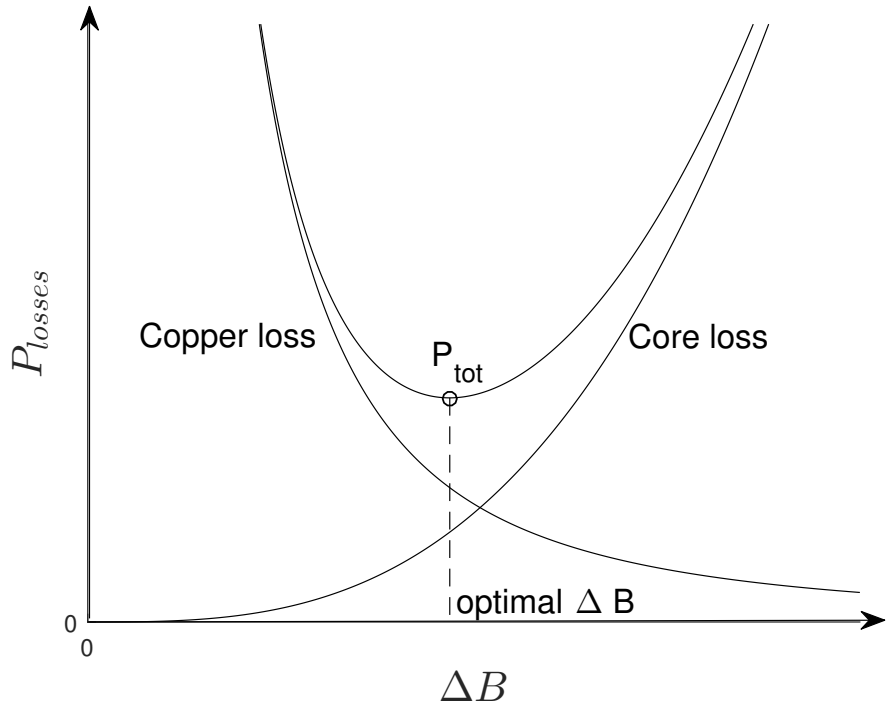

Figure 5.2: Core losses, copper losses in dependence of peak ac flux density (according to [4, p.568])

5.2.2 Winding Losses

For direct current or under low frequency conditions the copper losses can be easily written as stated in equation 5.3.

$$P_{CU} = I_{RMS}^2 \cdot R_{DC} \tag{5.3}$$

R_{DC} refers to the resistance measured under direct current conditions. The length l and the cross-section A of the wire or PCB trace as well as the specific conductivity are needed.

$$R_{DC} = \frac{\rho \cdot l}{A} \tag{5.4}$$

As the power converter operates at high frequencies skin and proximity effects are prevalent. This redistributes the current density, resulting in an increase of the effective resistance of the windings as well as significant copper losses [5].

There is a way of modelling winding losses in high frequency planar power transformers given by the paper [5]. This method is used to model the losses occurring in the windings of the transformer.

Skin Effect

The current flowing through the conductor induces a magnetic flux that surrounds the source current. Described by Lenz's law, the alternating flux induces eddy currents in the conductor, which leads to a shift of the current density outwards. By solving the Maxwell's equation it is possible to describe the current density. Consequently, the current density is highest at the surface and decays exponentially going deeper into the conductor. A *penetration depth* or *skin depth* can be stated for sinusoidal currents of frequency f in the conductive material. [4, p. 508]

$$\delta = \sqrt{\frac{1}{\pi \mu \sigma f}} \tag{5.5}$$

The permeability μ is equal to μ_0 for a copper conductor. [4, p. 509] The skin effect describes why the copper losses increase at higher frequencies. The graph 5.3 shows that at higher frequencies the utilised cross-section of the conductor is reduced and therefore not the full wire is used. [4, p. 510]

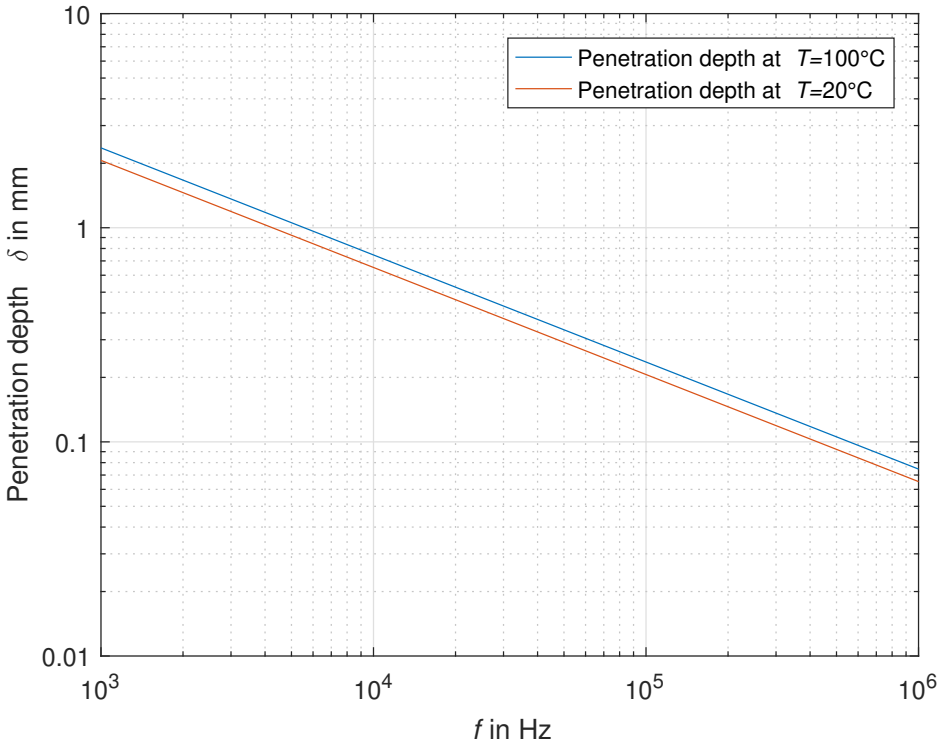

Figure 5.3: Penetration depth of a copper conductor vs frequency

Proximity Effect

The proximity effect is predominant at closely packed neighbouring windings and induces copper loss in adjacent conductors. The magneto motive force (MMF) can be used as a measure for the proximity losses. In order to reduce copper losses induced by the proximity effect, primary and secondary windings ought to be interleaved.

Model

To describe these losses clearly, the geometry of the transformer is necessary. Figure 5.4 shows a cross section of an exemplary planar transformer consisting of

three primary layers and two secondary layers, according to the explanations in [5]. The windings are spirally etched into the circuit board, and their simplification to circles in the model does not reduce the accuracy of the calculation by much. Through the interleaving of the windings the MMF is kept as small as possible.

The radii r_o and r_i are constraints mainly defined by the core used. Consequently, they define the maximum width w of the winding window. The same applies to the winding window height, which limits the maximum number of PCB layers. The parameter h is used to describe the height of the conductive material, whereas w_s is used to qualify the width of a single turn.

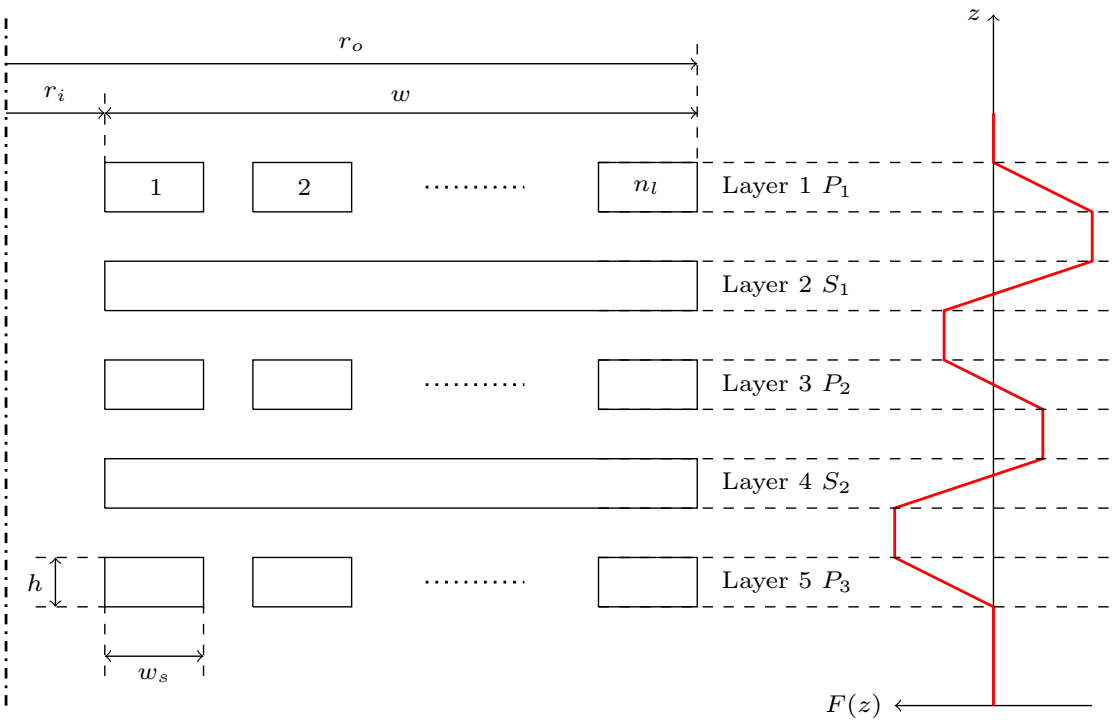

Figure 5.4: Cross-section of a Planar Transformer (according to [5])

With these parameters the porosity factor can be defined for each layer i, which is the ratio of used copper width versus available window width with n_l being the number of turns per layer. [5]

$$\eta_i = \frac{n_l \cdot w_s}{w} \tag{5.6}$$

Using this formula, each layer i can now be described as a uniform foil winding with its equivalent conductivity. [5]

$$\sigma_{e,i} = \eta_i \cdot \sigma \tag{5.7}$$

The formula for skin depth can next be extended by the porosity factor. [5]

$$\delta_{e,i} = \frac{\delta}{\sqrt{\eta_i}} = \sqrt{\frac{1}{\pi \mu_0 \eta_i \sigma f}} \tag{5.8}$$

The factor φ is the ratio between the conductor height h and the skin depth δ_e. [5]

$$\varphi_i = \frac{h}{\delta_{e,i}} \tag{5.9}$$

With this relation the DC resistance of a layer R_{DC} can then be modified to accompany the skin effect. [5]

$$R_{AC,i} = R_{DC,i} \cdot \varphi_i = \frac{\rho \cdot l}{h \cdot w_s} \cdot \frac{h}{\delta_{e,i}} = \frac{\rho \cdot l}{\delta_{e,i} \cdot w_s} \tag{5.10}$$

The following equations and functions are used to determine the loss caused by skin and proximity effects. Here $F(h)$ is the MMF. In order to obtain an analytical solution for the proximity losses, it is assumed that the course is described with straight line sections, as seen in figure 5.4 on the right. This means that once a layer structure of the transformer has been selected and the current through each layer is known, an approximation of the MMF is possible. I stands for the root mean square of the current, which flows through the winding of this layer i. The value of m is the ratio between MMF and the ampere turns prevailing in the layer. [4, p. 516]

$$m = \frac{F(h)}{n_l \cdot I} \tag{5.11}$$

$$G_1(\varphi) = \frac{sinh(2\varphi) + sin(2\varphi)}{cosh(2\varphi) - cos(2\varphi)} \tag{5.12}$$

$$G_2(\varphi) = \frac{sinh(\varphi) \cdot cos(\varphi) + cosh(\varphi) \cdot sin(\varphi)}{cosh(2\varphi) - cos(2\varphi)} \tag{5.13}$$

$$Q(\varphi, m) = (2m^2 - 2m + 1) \cdot G_1(\varphi) - 4m \cdot (m - 1) \cdot G_2(\varphi) \tag{5.14}$$

The calculation of the power dissipation of each layer i is made possible in this way. [4, p. 516] [5]

$$P_i = I^2 \cdot R_{DC,i} \cdot \varphi_i \cdot Q(\varphi_i, m) \tag{5.15}$$

$$P_{cu} = \sum_{j=0}^{inf} \sum_{i=1}^{M} P_i(I_j, f_j) \tag{5.16}$$

Equation 5.16 finally sums the occurring proximity losses over all M-layers and from these the j-sum over the harmonics is calculated.

The simulation of the state space model in chapter 3 allows to extract the primary and secondary current waveforms of the transformer. These are then Fourier-transformed (fft) into a list of RMS values $I_{eff,j}$ and frequencies f_j and then fed into this model to calculate the losses. Repeating this process with different designs and loads offers the possibility to compare the losses.

According to [5], the least possible proximity losses can be achieved by interleaving the windings so that the primary and secondary currents are in phase. Furthermore, it is assumed that the planar transformer will use this optimized interleaved winding design in order to reduce losses. However, this situation might also reduce the leakage inductance and increase the coupling capacitance. [see chapter 5.3]

5.2.3 Core Losses

The following section considers the losses occurring in the magnetic material of the transformer.

As described in literature [5] core losses in magnetic materials consist mainly of three parts:

- eddy current losses
- hysteresis losses

- excess eddy current losses

Referring to [5], the magnetic domain wall motion existing inside magnetic material is considered to be the origin of excess eddy current losses.
According to [6] there are two different approaches to the calculation of core losses.

The first approach is based on a mathematical representation of the hysteresis loop, which is then used to determine the energy loss in the core during a switching cycle. Several different improvements are made to further increase its accuracy. Nevertheless, it comes along with big disadvantages.

- Due to the need to calculate the hysteresis loops, an additional step is required to integrate the area of the B-H loop to obtain information about core loss.
- The suppliers often do not provide the necessary parameters of the used magnetic materials.
- The influence of the temperature on the hysteresis loop is not taken into account.

The second approach is based on an empirical method using Steinmetz equations. Those can be applied to directly calculate core losses, so there is no need for any hysteresis loop model. This approach is beneficial because suppliers of magnetic cores do publish their core loss data, which changes with frequency, excitation level and temperature. In order to be practical, these are measured with sinusoidal excitation of the core. This sinusoidal approach of measuring might be enough for loss calculations of conventional transformers. However, for switched mode power converters or alike which have no sinusoidal magnetizing currents there is a need to adapt the Steinmetz equation. [6]

The equation 5.17 is a modified version of the Steinmetz equation and calculates the specific power density P_v in $\mathrm{W/m^3}$. [7]

$$P_v = C_m \cdot f^x \cdot B^y \cdot (c_{t2} \cdot \tau^2 - c_{t1} \cdot \tau + c_{t0}) \tag{5.17}$$

The parameters C_m, x, y, c_{t2}, c_{t1} and c_{t0} are those needed to describe the loss properties of the material, which are ideally measured by the manufacturer. In this

Name	f_{min} kHz	f_{max} kHz	x	y	C_m	c_{t0}	c_{t1}	c_{t2}
3F98	300	600	2.1	2.3	0.000195	2.5	0.03	0.00015
3C30	20	100	1.42	3.02	0.00713	4	0.0665	0.000365
	100	200	1.24	3.02	0.00713	3.8	0.068	0.0004
3F3	100	300	1.63	2.45	0.00025	1.26	0.0105	7.9e-05
	300	500	1.8	2.5	2e-05	1.28	0.0105	7.7e-05
	500	1000	2.4	2.25	3.6e-09	1.14	0.0081	6.7e-05
3F4	500	1000	1.78	2.9	0.0012	1.15	0.011	9.5e-05
	1000	3000	2.8	2.4	1.1e-11	0.67	0.0001	3.4e-05
4F1	3000	5000	1.37	2.425	19.525	1.43617	0.0133734	9.01169e-05
	5000	7500	1.37	2.425	19.5626	2.20993	0.027	0.000149007
	7500	10000	1.37	2.425	21.3125	1.72273	0.0310014	0.000237741

Table 5.1: Material specific parameters for the determination of magnetic losses (adopted from [7])

project Ferroxcube materials are used not only because these parameters are available but also due to the fact that the core materials are suitable for high frequencies. [7]

For sinusoidal excitations equation 5.17 is used, in which f represents the frequency in Hz, τ the temperature in °C and B the peak magentic flux density in T. To enable its use for non sinusoidal magnetizing currents the equivalent frequency $f_{sin,eq}$ has to be calculated. The time-discrete waveform of the magnetic flux density is described by B_k. Here B_{max} is the largest and B_{min} the smallest occurring value. [5] [6]

$$f_{sin,eq} = \frac{2}{\pi^2} \sum_{k=2}^{K} \left[\frac{B_k - B_{k-1}}{B_{max} - B_{min}} \right]^2 \cdot \frac{1}{t_k - t_{k-1}} \tag{5.18}$$

To perform such a calculation, the magnetic flux density B must be determined over one switching cycle. Due to the linear simulation model created in the previous chapter the voltage across the primary winding is known and therefore the magnetic flux can be calculated.

$$\frac{d\phi_P}{dt} = \frac{U_P}{N_P} \rightarrow \phi(\zeta) = \int_0^{\zeta} \frac{U_P}{N_P} dt + \phi_0 \tag{5.19}$$

With the core geometry parameter A_e, which is the effective magnetic area, given the magnetic flux density B is deduced. From this, the peak magnetic flux density can be determined for the equation 5.21.

$$B(\zeta) = \frac{\phi(\zeta)}{A_e} \tag{5.20}$$

Due to the discrete nature of the state space simulator a discrete time series of the magnetic flux density B_k can be created without any extra steps. The time difference $t_k - t_{k-1}$ in equation 5.18 is the fixed simulation step size dt. Putting all this together the equivalent frequency $f_{sin,eq}$ can now be inserted into the equation 5.21 to finally calculate at least an estimation of the magnetic core losses P_{core} of the planar transformer.

$$P_v = C_m \cdot f_{sin,eq}^{x-1} \cdot B^y \cdot f \cdot (c_{t2} \cdot \tau^2 - c_{t1} \cdot \tau + c_t) \tag{5.21}$$

$$P_{core} = P_v \cdot V_e \tag{5.22}$$

5.2.4 Automated Design Script

As it is not yet known which turns ratio is the most promising and since apart from that there are a number of different possibilities of design and construction of the transformer, an automated design process is advantageous.

The script is based on the premise of finding a set of considerations for the transformer that promise the lowest losses. To find those in an algorithmic way the following steps are performed.

First of all, a range of different promising turns ratios have to be defined.
This is done by considering the input voltage range and target output voltage.
The formula 5.2 connects those input voltages with the turns ratio and duty cycle.
A series of different turns ratios will be created and then put into the state space model to be simulated. Those simulation results are needed to calculate the losses properly. There is one crucial aspect to point out here; the state space model also needs values for the other parts of the circuit, which are not known yet. So default values will be put in place for L_m, L_σ, C_r and C_{out}. Due to the properties of this script, it might be adapted in a later project in order to perform an automatic optimization.

Apart from the pre-simulation step the core geometry has to be defined. Currently this script only allows the use of one core shape. Which is fixed, namely the following parameters: volume V_e, magnetic area A_e, inner radius r_i, outer radius r_o and window height h_{window}.

The geometry of the PCB is defined by the thickness of the PCB itself h_{PCB} and the thickness of the conductor material $h_{conductor}$. Whether these are several individual PCBs which are layered or a multilayer PCB is open. The designation h_{PCB} only stands for the distance between two conductive layers.

The total count of layers M fitting into the core window can be defined as:

$$M = floor\left(\frac{h_{window}}{h_{PCB} + h_{Conductor}}\right) \tag{5.23}$$

The dielectric strength of the PCB must be high enough to satisfy the required galvanic isolation of $2.5kV$.

$$\text{dielectric strength} > \frac{2.5kV}{h_{PCB}} \tag{5.24}$$

Granted that all the state space simulations are done, the geometries are defined and the dielectric strength is high enough, the next step is to list all promising core materials for the magnetic loss calculations.

After that initialization phase the script starts its main loop in which the layers M get assigned a side.

Step by step, all possible combinations of the winding assignment per winding layer are tried out and it is checked whether a functioning transformer could result from it.

The key query is whether the target winding ratio is reached or not.

This is a brute force approach which will certainly try all possible combinations of how to build up a transformer.

If it eventually finds a layer structure satisfying the target turns ratio, it will calculate the copper losses according to the description in chapter 5.2.2.

Apart from that it will initialize a second loop in which it will calculate the magnetic losses of the core for different core materials.

After the best material is selected the losses are summed up and stored.

Having run through all the different transformer setups, this script provides the best layer structure of the primary and secondary side assignment, as well as the core material to be used and the expected losses.

Figure 5.5 is a graphic depiction of this script.

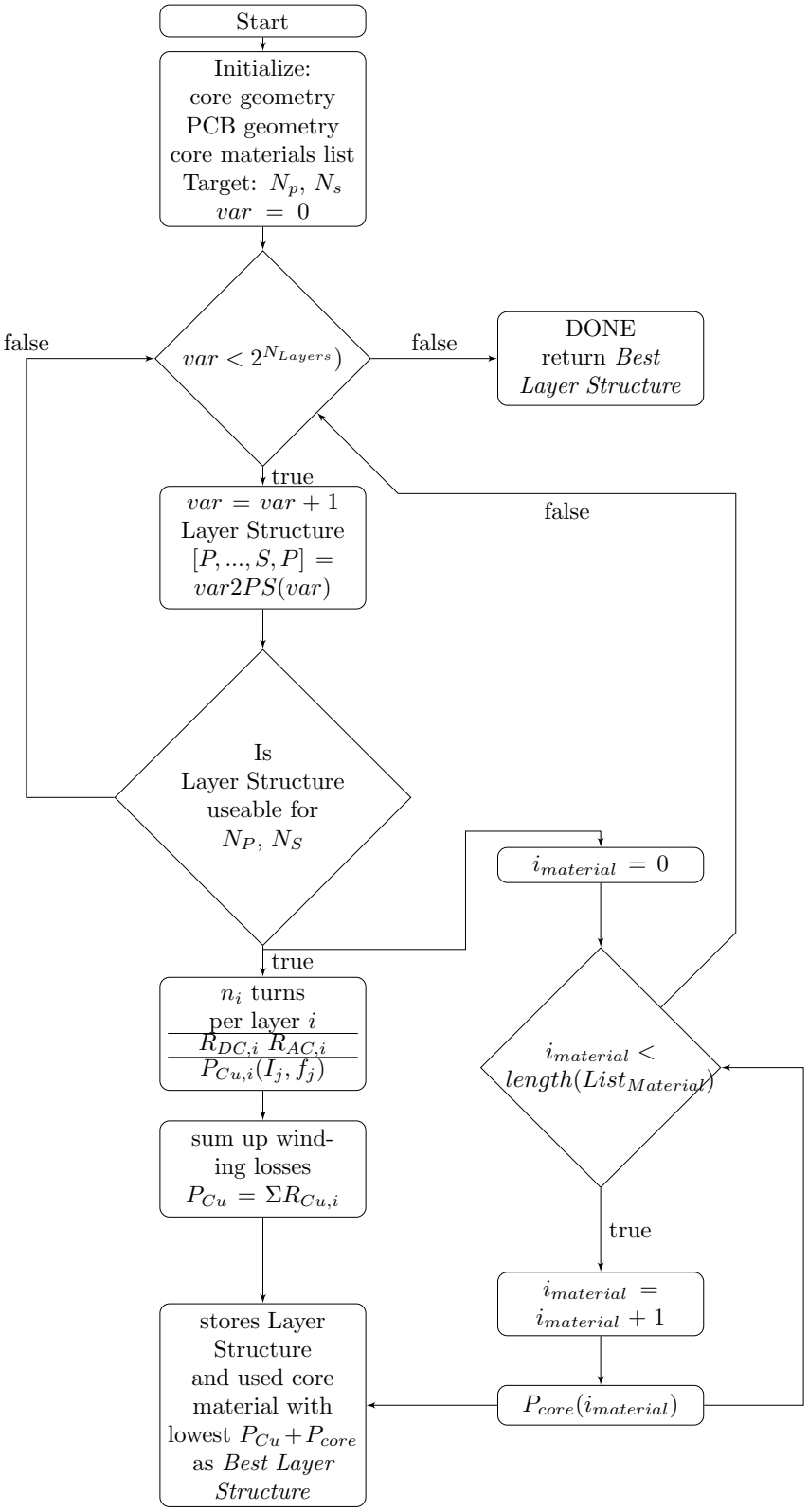

Figure 5.5: Flow chart of planar transformer loss calculation

5.3 Leakage Inductance L_σ

Since the design of the transformer was discussed in the previous chapter, it makes sense to investigate and find out the effective leakage inductance of this transformer. In scientific sources there are different methods how to calculate the leakage inductance of a transformer, especially a planar transformer.

The authors in [8] state that the energy of the leakage inductance can be written as follows.

$$E = \frac{\mu_0 l_w b_w}{2}\left[\int_0^{h_1}\left(\frac{N_1 I_1 x}{b_w h_1}\right)^2 dx + \int_0^{h_2}\left(\frac{N_2 I_2 x}{b_w h_2}\right)^2 dx + \left(\frac{N_1 I_1}{b_w}\right)^2 h_\Delta\right] \tag{5.25}$$

The following variables have the following meaning:

- l_w mean length of traces ($\approx (r_o + r_i) \cdot \pi$ in figure 5.4)
- b_w width or breadth of winding window (w in figure 5.4)
- h_1 total height of primary side (conductor) (h in figure 5.4)
- h_2 total height of secondary side (conductor)
- h_Δ total height of insulator

The first term in 5.25 is the energy of the leakage inductance of the primary side $L_{\sigma,P}$, whereas the second term represents the energy of the secondary side leakage inductance $L_{\sigma,S}$.

$$E = \frac{L_\sigma \cdot I^2}{2} \tag{5.26}$$

The energy can also be stated by means of the inductance itself 5.26 and thus a formula for the leakage inductance can be written for the non-interleaved structure 5.27. [8]

$$L_\sigma = \frac{2W}{I_p^2} = \mu_0 N_1^2 \frac{l_w}{b_w}\left(\frac{h_1 + h_2}{3} + h_\Delta\right) \tag{5.27}$$

This is one of the methods used in this design process to estimate the value of the leakage inductance. According to [8] the internal leakage inductance is mainly influenced by whether the layers of the transformer are interleaved or not. The created modified formula 5.28 takes the nested structure of the windings into account by using an interleaving factor M. This new parameter M stands for the number of interleaved multiples of repeating primary-secondary windings in the layer stack. This obviously reduces leakage inductance significantly.

$$L_\sigma = \mu_0 \frac{N_1^2 \cdot l_w}{M^2 \cdot b_w} \left(\frac{\sum h_i}{3} + \sum h_\Delta \right) \tag{5.28}$$

Although this formula is simple to use and might also give a better estimation of the leakage inductance L_σ there is an even more precise method.

The authors in [9] state that the method uses the magnetic field strength occurring in the winding window to deduce the energy stored within it. It is worth mentioning that the previously presented script for transformer calculations can of course provide the magneto motive force (MMF) of the layer stack in the respective transformer. Therefore, this method is more promising to make more appropriate estimates for leakage inductance.

The MMF is shown in figure 5.4 as $F(x)$. In each conductive part of the layer stack the magneto motive force adds up to the local Ampere-Turn-Value. Between two conductive layers the MMF stays at the same level.

$$F(x) = n(x) \cdot I(x) \tag{5.29}$$

The magnetic field strength $H(x)$ in the winding window can be derived by dividing the MMF $F(x)$ by the average length of the field line, which is due to its location in the air basically the width or breadth b_w of the winding window.

$$H(x) = \frac{F(x)}{b_w} \tag{5.30}$$

The energy stored in the leakage magnetic field of the winding window can be stated as follows. [9]

$$E = \frac{\mu_0 b_w l_w}{2} \int_0^h H^2(x) dx \tag{5.31}$$

Using the relation 5.26 again the leakage inductance L_σ can then be calculated.

Above a certain degree of interleaving, these values for L_σ tend to become very small. Therefore, the trace on the board connecting the external magnetising inductance L_m and the transformer must be taken into account.

5.4 External Magnetizing Inductance L_m

The purpose of the external magnetization inductance is to store intermittent energy for the conversion cycle and if possible to support the ZVS of the half bridge from the low to the high side.

Presumed that a suitable value for L_m has been found for the converter, the following steps should be considered for the design process. Similar to the previous chapter, it is assumed that the geometry of the core has already been defined. (A_e, l_e)

$$U_{Lm} = N \cdot \frac{d\phi}{dt} = N \cdot \frac{A_e \cdot dB}{dt} \rightarrow \bar{U}_{Lm} = N \cdot \frac{A_e \cdot \Delta B}{\Delta t} \tag{5.32}$$

In the steady state condition of the converter the magnetic flux density B rises in the t_{on}-*Mode* and falls back to where it started in the t_{off}-*Mode*. This change of the magnetic flux density is called ΔB, correlates to the losses in the core and should be limited by design. This value ΔB_{max} has to be defined previous to the design steps.

$$\Delta B < \Delta B_{max} \tag{5.33}$$

The voltage U_{L_m} is known as a result of the state space simulation done in chapter 3. Only one time frame of the conversion cycle is needed for the calculation, so the t_{on} time is used as dt. The voltage across the inductor for this time frame will be averaged $\bar{U}_{L_m}$ accordingly.

$$\bar{U}_{Lm} = \frac{1}{t_{on}} \int_0^{t_{on}} U_{L_m}(t)dt \tag{5.34}$$

This allows the number of turns N to be calculated.

$$N = \frac{\bar{U}_{Lm} \cdot t_{on}}{A_e \cdot \Delta B_{max}} \tag{5.35}$$

Therefore the inductance factor A_L can be determined and consequently the new effective permeability $\mu_{eff,new}$.

$$A_L = \frac{L_m}{N^2} \tag{5.36}$$

$$\mu_{eff,new} = \frac{A_L \cdot l_e}{\mu_0 \cdot A_e} \tag{5.37}$$

The core material for testing is selected in accordance with μ_{eff}.The air gap l_{gap} is calculated and the losses corresponding to the core material and geometry are calculated and compared with other core materials.

The needed air gap l_{gap} can than be derived from the following equation.

$$l_{gap} = \left(\frac{\mu_{eff}}{\mu_{eff,new}} - 1 \right) \cdot \frac{l_e}{\mu_{eff}} \tag{5.38}$$

If the selected core-material combination leads to an inductor setup where the air gap l_{gap} might be too large, this gap is limited and the resulting external magnetization inductance L_m is returned. Since a larger air gap leads to an increased fringing flux, it has a negative effect on the windings. The winding sections located near the air gap have additional eddy current losses, too. Therefore, the air gap should be as small as possible. If this results in a non-functioning converter, the core-material combination must be changed.

5.4.1 Losses

The analysis of the losses for the external magnetizing inductance is similar to the analysis done for transformer losses. In the same way as with the transformer, the winding layout of the inductor is determined, from which the dc resistance is calculated. Based on the known current waveform through external inductance, the AC resistance is estimated. The winding loss P_{cu} (5.2.2) is then determined while at the same time the magnetic losses P_{core} are calculated (similar to 5.2.3).

5.5 Resonance Capacitance C_r

This circuit requires several design considerations and the degree of freedom is limited. Considering the premise of reaching high power density and high efficiency the transformer and the external magnetization inductor must be designed in a way to fulfill this request. The leakage inductor is then a result of the transformer design and cannot be chosen freely. The only part left which has an influence on the behaviour of the converter is the resonant capacitor C_r, which has a huge impact on the resonant frequency f_{res} (Chapter 4.1). With those equations, it is possible to estimate which values for C_r might be fitting, using all components in the circuit.

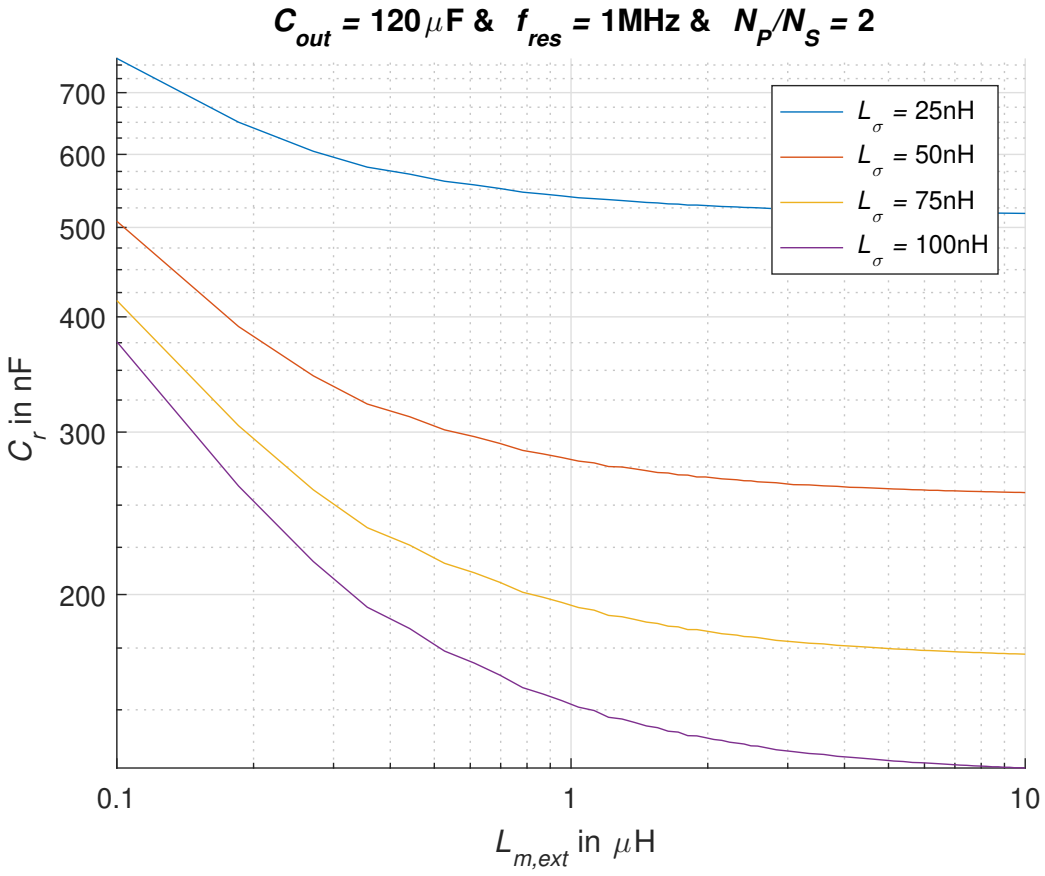

Figure 5.6: Resonant capacitor as a function of L_σ, L_m, N_P/N_S, C_{out}, f_{res}

Figure 5.6 shows the relation between resonance capacitor C_r, external magnetizing inductance L_m and leakage inductance L_σ with the fixed output capacitance C_{out}, resonance frequency f_{res} and turns ratio N_p/N_s.

5.5.1 Losses

The equivalent series circuit of a capacitor (figure 5.7) is used for loss calculation. The equivalent series resistance *ESR* is the major contributor to the losses occurring in the capacitor.

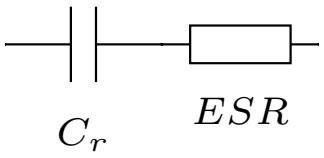

Figure 5.7: Equivalent series circuit diagram of a capacitor

$$P_{C_r} = I^2_{C_r,eff} \cdot ESR \tag{5.39}$$

5.6 Output Capacitance C_{out}

The task of the output capacitor C_{out} is to be a low pass filter and to provide DC voltage to the load. To obtain an estimate of the required capacitance value, which also takes into account the equivalent series resistance (ESR) of the capacitance, the following equivalent circuit 5.8 is considered.

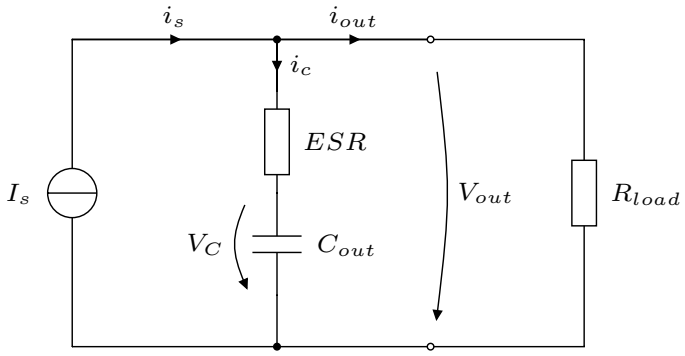

Figure 5.8: Simplified equivalent circuit of the output filter

The current source I_s substitutes the transformer secondary. For the current waveform of the secondary side of the transformer, it is known that the current in t_{off}-*Mode* approximates a sine wave, while in t_{on}-*Mode* it is 0A. Equation 5.40 describes the simplified secondary-side current i_s for the t_{off}-*Mode*.

$$i_s(t) = I_{s,peak} \cdot sin\left(\frac{\pi}{(1-d)} \cdot \frac{t}{T}\right) \tag{5.40}$$

To determine the required peak current on the secondary side $I_{s,peak}$, 4.14 is used. For the average current I_{mean}, the target output power $P_{out,target}$ and the target output voltage $V_{out,target}$ are used to determine its value.

$$I_{s,peak} = \frac{P_{out,target}}{V_{out,target}} \cdot \frac{\pi}{2 \cdot (1-d)} \tag{5.41}$$

With equation 5.41, the secondary peak current $I_{s,peak}$ depends not only on the output reference voltage and output reference power, but also on the duty cycle d.

This makes it possible to calculate the voltage of the output filter capacitance at any point in time.

For the time duration $0 < t < t_{on}$ of the t_{on}-*Mode* the following equations 5.42 represent the voltage across the output capacitance.

$$V_c(t) = V_c(0) \cdot e^{-\frac{t}{(ESR+R_{load})\cdot C)}} \tag{5.42}$$

For the time duration $0 < t < t_{off}$ of the t_{off}-*Mode* this equation 5.43 approximates the output capacitance voltage.

$$V_c(t) = V_c(t_{on}) \cdot e^{-\frac{t}{(ESR+R_{load})\cdot C}} + \frac{P_{out,target}}{V_{out,target}} \cdot \frac{T}{2} \cdot \frac{R_{load}}{(ESR + R_{load}) \cdot C} \cdot \left[1 - cos\left(\frac{\pi}{(1-d)} \cdot \frac{t}{T}\right)\right] \tag{5.43}$$

Using 5.42, 5.43 and 5.40, the output voltage $V_{out}(t)$ can be calculated. The output capacitance C_{out}, its equivalent series resistance ESR, the target output power $P_{out,target}$, the duty cycle d and the converter period duration T define the waveform of this output voltage.

$$V_{out}(t) = V_c(t) \cdot \frac{R_{load}}{ESR + R_{load}} + i_s(t) \cdot \frac{ESR \cdot R_{load}}{ESR + R_{load}} \tag{5.44}$$

The output voltage ripple according to the specifications is $\pm 240mV$, which is the sum of the capacitive part and the equivalent series resistance (ESR) voltage drop.

$$\Delta u = 2 \cdot 240\,\text{mV} = 480\,\text{mV} \tag{5.45}$$

The output voltage $V_{out}(t)$ must satisfy this constraint. Figure 5.9 is intended to show the voltage curve as an example.

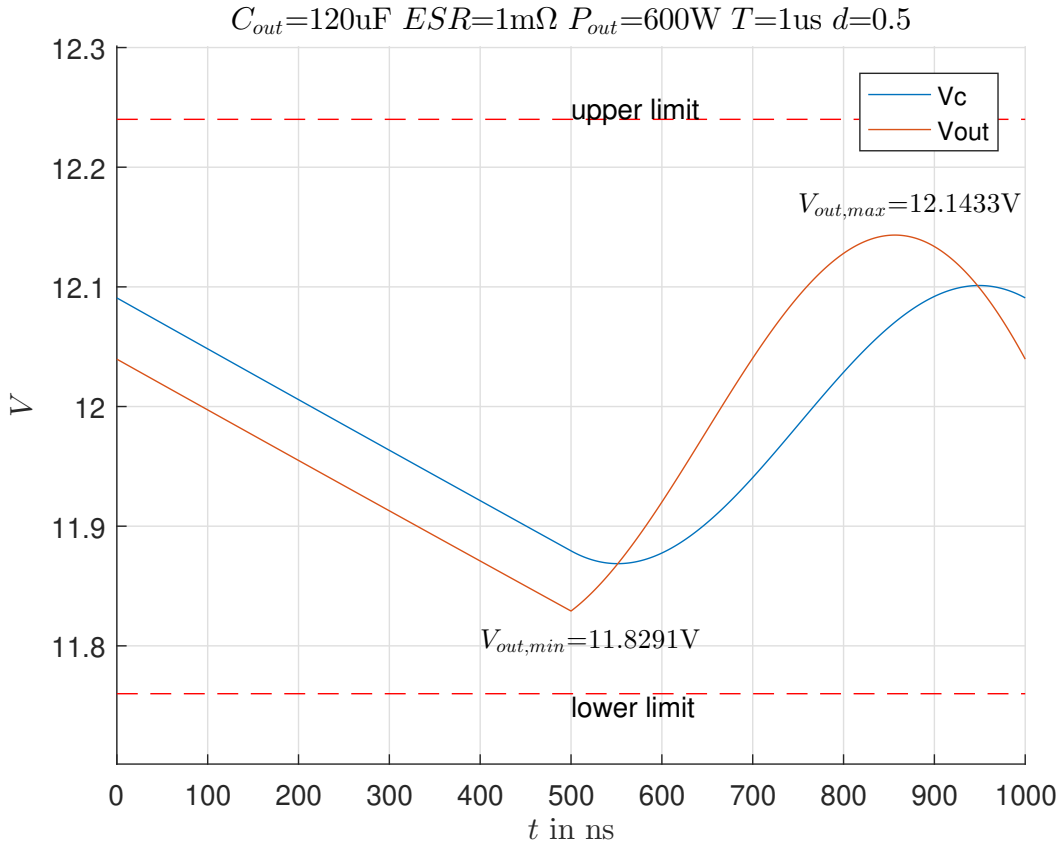

Figure 5.9: $V_{out}(C, ESR, P_{out}, T, d, t)$

Using this relationship, another figure 5.10 can be drawn showing the maximum and minimum output voltages as a function of duty cycle d at various ESR and C_{out} selections.

It can be seen that the possible operating range of the duty cycle is limited as the resistance of the ESR increases.

As ESR values increase, the capacitance value C_{out} must increase even further to fall below the target output voltage ripple.

The duty cycle in Figure 5.10 was limited to that required in a circuit design with a transformer turns ratio N_p/N_s of 2/1.

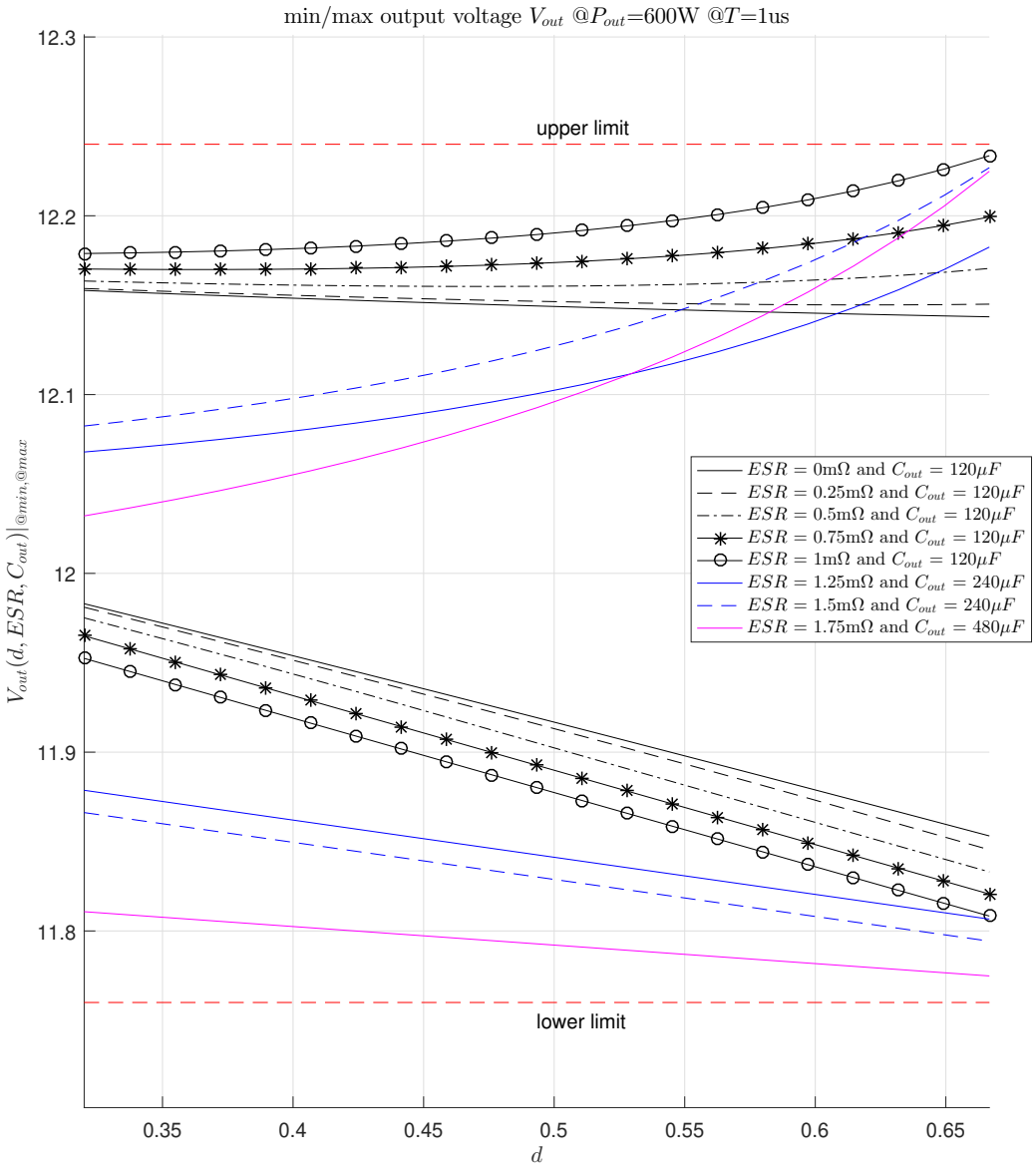

Figure 5.10: $V_{out}|_{max/min}(C, ESR, P_{out}, T, d)$

5.7 Half Bridge and Synchronous Rectifier

According to figure 1.4 there are three semiconductor switches. The half bridge contains the High Side Mosfet (HS-FET) and the Low Side Mosfet (LS-FET). On the secondary side of the transformer there is a synchronous rectifier (SR-FET).

5.7.1 MOSFETs

Figure 5.11 shows the equivalent circuit of a typical MOSFET with its body diode and terminal capacitances.

In terms of operating modes of the MOSFET, there are two main operating areas. There is the ohmic region and there is the saturation region. In the ohmic region, the relationship between drain-source voltage and drain current follows almost Ohm's law. In the saturation region, the drain current is almost independent of the drain-soruce voltage and is therefore also called linear mode operation.
Using the MOSFET as a switch, the device will go through the linear operation mode from the moment V_{GS} exceeds the gate-source threshold voltage. As soon as the drain-source voltage drops close to 0 V it is in ohmic operation mode.
This means that the switch is in the linear operating mode during the process of switching. This transition takes only a few nano seconds (less than 10 ns). [10]

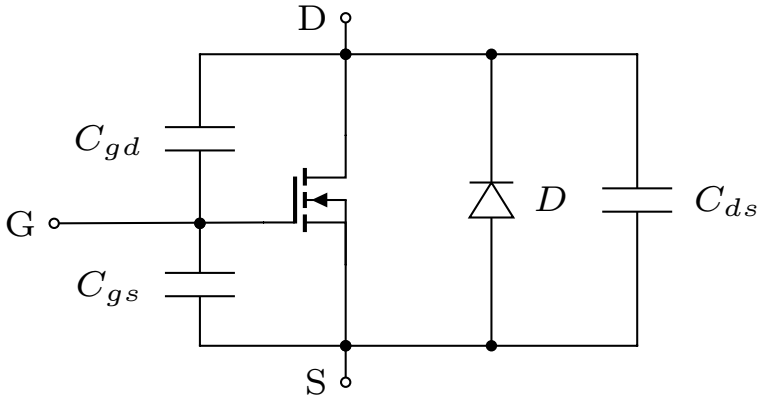

Figure 5.11: Equivalent circuit of MOSFET featuring the bodydiode and its terminal capacitors

The body diode of the MOSFET allows only one direction of current to be blocked. In the topology described here, this does not pose a problem, since all switching operations ideally only need to block the current in one direction.

A major influence on the behaviour of a MOSFET are the parasitic capacitances. They have a nonlinear voltage dependence and represent an influence on the switching characteristics as well as the occurring losses. [4, p.80]

5.7.2 Losses

It is assumed that for some switches in this topology it might be necessary to take several of them in parallel to be able to carry the current.

5.7.2.1 Conduction Losses

When current flows through the MOSFET, conduction losses can be described by equation 5.46 where R_{DSon} is the drain-source resistance at on-state, n is the number of switches in parallel, f_{PWM} is the switching frequency, $T_{SW(on)}$ is the duration of the on-state of the mosefet and i_D is its drain current. To further decrease the conduction losses larger chip areas for the MOSFETs are beneficial. [11]

$$P_{cond} = n \cdot f_{PWM} \int_0^{T_{SW(on)}} R_{DSon} \cdot \left(\frac{i_D}{n}\right)^2 dt = \frac{1}{n}\left[f_{PWM} \int_0^{T_{SW(on)}} R_{DSon} \cdot i_D^2 dt\right] \tag{5.46}$$

5.7.2.2 Gate Driving Losses

The gate capacitance must be charged and discharged in one full cycle of the switching period. The energy required to move this charge is lost and accounts for losses, which can be calculated using equation 5.47. Since the value for the input capacitance C_{iss} changes with V_{DS}, it is more appropriate to use the gate charge Q_g specified by the manufacturer. Larger chip areas for the MOSFET result in larger capacitances and thus lead to higher gate driving losses. [11]

$$P_{drive} = n \cdot f_{PWM} \cdot Q_g \cdot V_{GS} \tag{5.47}$$

5.7.2.3 Switching Losses

The switching losses occur as the name implies at the moment of switching. The switch is turned on under voltage and turned off under current, which is called a hard switching topology. This type of operation results in additional losses in the switches and causes high stress. Because those losses occur periodically they increase in case of higher frequencies in a linear manner. The topology and the mode of operation defines those losses greatly.

Figure 5.12 shows the switching losses of a hard switching topology.

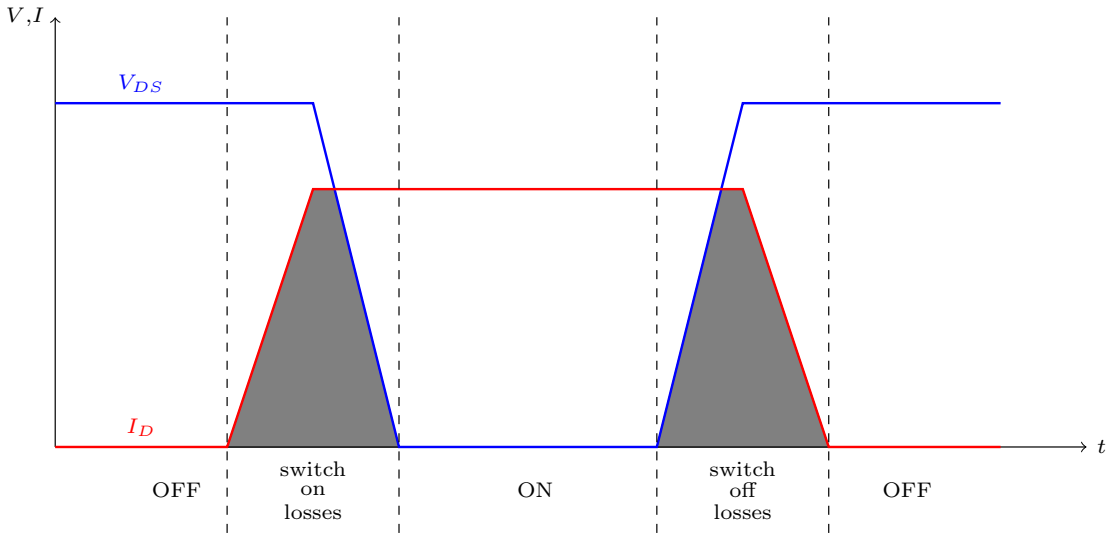

Figure 5.12: Hard switching losses scheme

In a soft-switching topology, the drain-source capacitance C_{DS} is discharged so that the voltage across it approaches zero and then the MOSFET is turned on. This is called *Zero Voltage Switching* (ZVS). In the case of *Zero Current Switching* (ZCS) the drain current I_D gets close to zero Amperes and the turn off occurs afterwards.

Due to the potential of greatly decreased losses and thus increased efficiency those soft switching topologies are most promising for achieving the highest power density. [4] [12] [13]

Those soft switching events can be seen in figure 5.13.

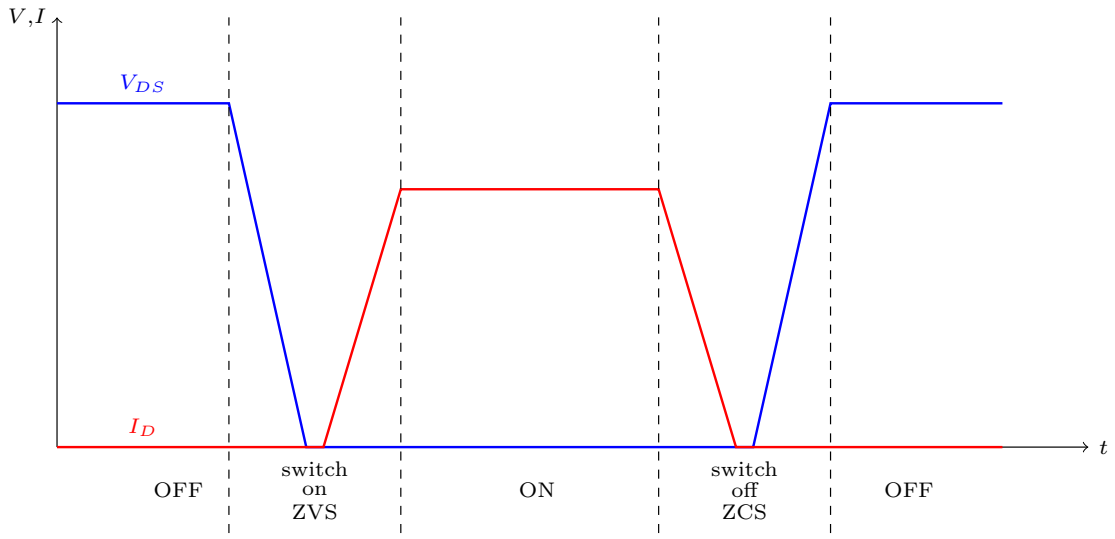

Figure 5.13: Soft switching losses scheme

5.7.2.3.1 Soft Switching of the Half Bridge

Looking at the half bridge of this converter two situations can arise to enable soft switching.

Switching from $HS \rightarrow LS$

Before the HS switch is turned off and the LS is turned on, a current with positive direction flows out of the half bridge. When the currently closed HS switch is opened, the current must flow through its terminal capacitance C_{OSS}, charging it in the process. In the same way, the LS located C_{OSS} starts to discharge and the half bridge voltage swings from V_{in} to $0V$. Until the LS body diode starts conducting, the LS switch can be turned on with virtually no losses.

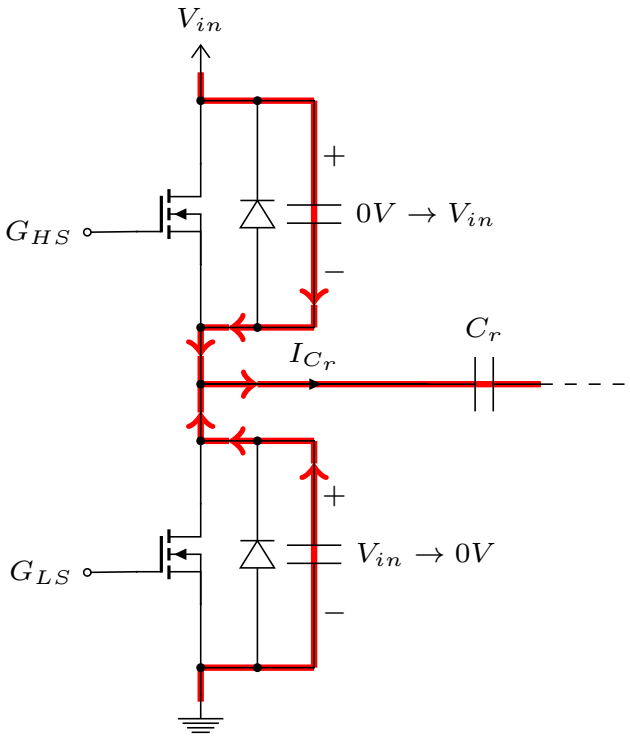

Figure 5.14: ZVS behaviour at Switch between $HS \rightarrow LS$

Switching from $LS \rightarrow HS$

Before the LS switch is turned off and the HS switch is turned on, a current flows into the half bridge. As soon as the currently closed LS switch is opened, the current must flow through its terminal capacitance C_{OSS}, charging it in the process. In the same way, the HS located C_{OSS} starts to discharge and the half bridge voltage swings from $0V$ to V_{in}. Until the HS body diode starts conducting, the HS switch can be turned on with virtually no losses.

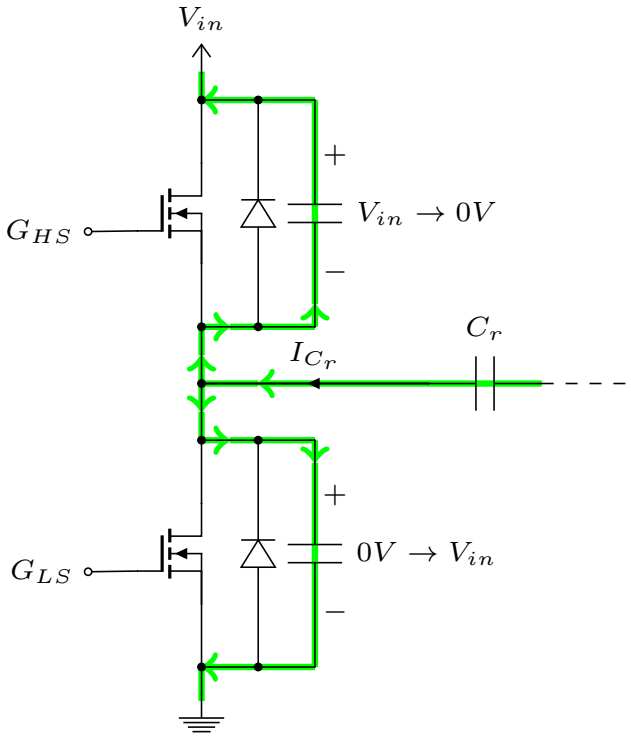

Figure 5.15: ZVS behaviour at Switch between $LS \rightarrow HS$

This situation however is load dependent and cannot always be achieved. This is a major drawback of this topology, which can be seen in the figure 4.1.

5.7.2.3.2 Soft switching of the Synchronous Rectifier

Due to its location at the secondary side of the transformer, the synchronous rectifier can be switched on naturally under a zero voltage condition.

After the transfer of energy is completed, the current through the transformer drops back to zero and the SR can switch off at a zero current situation.
This should be similar to the soft switching scheme viewed in figure 5.13.

Chapter 6

Example Designs

6.1 First Design

To further investigate the behaviour of the converter, a first design is necessary.

6.1.1 Turns Ratio: 1/1

First of all, the turns ratio $\frac{N_P}{N_S}$ is selected. In figure 5.1 in chapter 5.2.1 the span of feasible turns ratios is shown.
To provide suitable output voltage regulation at dynamic loads, a wide range of the controllable duty ratio d is required.
In addition, it is useful to keep the total number of turns $(N_p + N_s)$ as low as possible. Aiming at the broadest possible duty ratio range and a small total number of turns $(N_p + N_s)$, the following turns ratios are suitable for a start:

- $\frac{N_P}{N_S} = \frac{1}{1}$ (selected for further design)
- $\frac{N_P}{N_S} = \frac{2}{1}$

6.1.2 CORE: ER 32/6/25

Several things must be considered when selecting the core geometry. Given the nature of this investigation, where the goal is to find a possible design with high power density, the smallest core available might be favorable. But considering also the lowest possible losses, the selection may well favor a larger magnet core geometry.

The selection of core dimensions must be such that the desired target power density of the entire transducer is at least 22 W cm^{-3}.
In equation 6.1, V is the available volume of the entire converter.

$$V = \frac{600\,\mathrm{W}}{22\,\mathrm{W\,cm^{-3}}} = 27\,272.7\,\mathrm{mm^3} = (30.1\,\mathrm{mm})^3 \tag{6.1}$$

Since the magnetic components in a circuit can take up a lot of space, it is necessary to reserve enough room for the forward transformer.
Table 6.1 lists the core shapes that are available for this project.

Name	Volume	% of V
ER 11	330.0 mm^3	1.2 %
ER 14.5	573.2 mm^3	2.1 %
ER 18	1100.0 mm^3	4.0 %
ER 23	2958.0 mm^3	10.8 %
ER 32	9784.1 mm^3	35.9 %
ER 41	19 767.3 mm^3	72.5 %

Table 6.1: List of available core options

As the other components must not be forgotten either, the choice for the transformer core falls on **ER 32/6/25**.
ER 41 is eliminated because it would take up almost three quarters of the available space.

V_e	5400 mm^3
l_e	38.2 mm
A_e	141.0 mm^2
h	5.8 mm
d_i	12.40 mm
d_o	27.2 mm

Table 6.2: Geometric properties: **ER 32/6/25**

6.1.3 PCB

The design guide [7] recommends FR2 or FR4 PCB material for power converters. The dielectric strength of this material is around 39 kV mm^{-1}. To ensure galvanic isolation of at least 2.5 kV the PCB core thickness h_{PCB} must not be less then 65 µm.

The thickness of the used PCBs can be specified between 0.4 mm and 3.2 mm.
The thickness of the copper layer is selectable between 35 µm and 210 µm.
It is assumed that the height of the core h_{PCB} is 400 µm and the one of the copper $h_{Conductor}$ is 210 µm.

In accordance with this specification, the number of winding layers M in the transformer (5.23) is as follows.

$$M = floor\left(\frac{h_{window}}{h_{PCB} + h_{Conductor}}\right) = floor\left(\frac{5.8mm}{400\mu m + 210\mu m}\right) = 9Layers \tag{6.2}$$

Since only one copper side remains exposed in a multilayer PCB of 9 copper layers, this side must still be insulated against the magnetic core. For this purpose, there is just a space of 310 µm left to apply an insulation with coating.

The previously mentioned script (5.2.4), which automates the transformer design step, outputs the following result for the layer structure.

Primary side	$N_{P,target} = 1$	5 Layers in parallel	$R_{DC} = 0.16m\Omega$
Secondary side	$N_{S,target} = 1$	4 Layers in parallel	$R_{DC} = 0.20m\Omega$

Table 6.3: Planar transformer setup

Layer Nr.	Side	Turns	R_{DC} mΩ	*dMMF* A	*MMF* A
1	P	1	0.819	0.2	0.2
2	S	1	0.819	-0.25	-0.05
3	P	1	0.819	0.2	0.15
4	S	1	0.819	-0.25	-0.1
5	P	1	0.819	0.2	0.1
6	S	1	0.819	-0.25	-0.15
7	P	1	0.819	0.2	0.05
8	S	1	0.819	-0.25	-0.2
9	P	1	0.819	0.2	0

Table 6.4: Layer structure of planar transformer

These calculations are based on the ideal current distribution of parallel connected layers. Since this is not guaranteed, the results are to be considered as the best case scenario.

The switching frequency f_{PWM} is specified as 1MHz, which is why **3F3** is used as the magnetic core material, as it was designed for higher frequencies.

The determination of the losses of the magnetic core and the leakage losses will only be possible later, when a transient simulation has taken place.

6.1.4 Stray Inductance L_σ

The previously used script can use the geometry data of the planar transformer and its layer structure to calculate its leakage inductance. The procedure has already been described in chapter 5.3.

Method	Equation	L_σ	k	$(1-k)$
1	5.27	36.31 nH	99.1302 %	0.8698 %
2	5.28	3.39 nH	99.9187 %	0.0813 %
3	5.31	0.97 nH	99.9767 %	0.0233 %

Table 6.5: Results of leakage inductance

The first method takes the thickness of the primary and secondary sides but also the insulation material in the winding window into account. (5.27)
The second method evolves from the first one and is supplemented by the fact that the various layers are interleaved. In this case, the number of interleaved multiples M is set to 4. (5.28)
The third method uses the MMF values from table 6.4 to calculate the energy stored in the transformer winding area and thus estimates the leakage inductance. (5.31)

Since the magnetic leakage field inside the planar transformer is taken into account, deviations may occur.

The results in table 6.5 provide various estimates for the leakage inductance. Considering that method three allows a much more precise modeling of the leakage inductance than the other two methods, this estimate is probably the most accurate approximation that does not require a finite element method simulation.

Once the leakage inductance is known, the coupling factor (6.4) of the planar transformer is to be calculated from the mutual inductance (6.3). For each of these three methods, the coupling factor is shown in the table 6.5.

$$L_M = \mu_0 \cdot \mu_r \cdot N_P \cdot N_S \cdot \frac{A_e}{l_e} = 4\pi \cdot 10^{-7} \cdot 900 \cdot 1 \cdot 1 \cdot \frac{141 \cdot 10^{-6}}{38.2 \cdot 10^{-3}} = 4.17\,\mu\text{H} \tag{6.3}$$

$$k = 1 - \frac{L_\sigma}{L_M} \tag{6.4}$$

It should be noted that the possible conductor loops on the PCB, which also play their part in increasing the effective inductance, have not even been considered. In [14] a formula is presented, which can provide the inductance of the printed circuit board L_{PCB}.

$$L_{PCB} = \mu_0 \cdot \frac{e}{w} \cdot l \cdot \left(\frac{1}{1 + \frac{e}{w}} + 0.024 \right) \tag{6.5}$$

In equation 6.5, w represents the width of the line, e represents the distance between the copper planes, and l represents the length of the line.

Since the component positions on the PCB and the dimensions of the components themselves are still unknown, it only makes sense to determine this resulting line inductance once these have been determined.

However, to obtain at least an estimate of the range of magnitudes in which this line inductance acts, a conductor semicircle on the primary and a conductor semicircle on the secondary are assumed to contribute to the total effective leakage inductance. Therefore, to make this very simple approximation, the lines to and from the **ER 32/6/25** core are assumed to form a circle as a whole.

From the manufacturer's data sheet [15], the dimensions of the magnetic core **ER 32/6/25** can be used to estimate the diameter of the loop.

$$l = d \cdot \pi = \frac{d_o + d_i}{2} \cdot \pi = \frac{27.2\,\text{mm} + 12.4\,\text{mm}}{2} \cdot \pi = 62.2\,\text{mm} \tag{6.6}$$

For width w of the line the window width of the core is assumed.

$$w = \frac{d_o - d_i}{2} = \frac{27.2\,\text{mm} - 12.4\,\text{mm}}{2} = 7.4\,\text{mm} \tag{6.7}$$

$$L_{PCB} = \mu_0 \cdot \frac{400\,\mu\text{m}}{7.4\,\text{mm}} \cdot 62.2\,\text{mm} \cdot \left(\frac{1}{1 + \frac{400\,\mu\text{m}}{7.4\,\text{mm}}} + 0.024 \right) = 4.11\,\text{nH} \tag{6.8}$$

In addition to the leakage inductance of the transformer, there is a series inductance of the line L_{PCB} of 4.11 nH.

Considering this line inductance as well, it is reasonable to set the total leakage inductance in this case to about 5 nH in total.

If this topology were ever to be built, it would anyway be necessary to carry out a detailed FEM simulation beforehand in order to obtain the best possible estimates for the leakage inductance.

6.1.5 Magnetizing Inductance L_m vs Resonance Capacitance C_r

As described in chapter 5.5, the relationship between resonance capacitance C_r and magnetisation inductance L_m is established under the assumption of a desired resonance frequency f_{res} taking into account the already known component values of the circuit.

The following calculation is the derivation of an equation that can be used to estimate the resonant frequency.

Equation 4.7 is applied to obtain an estimate for the resonant frequency of the circuit. This results in the C_r-L_m combinations which are considered for the circuit design.

$$t_{off} = T_{PWM} \cdot (1 - d) \tag{6.9}$$

The representation of the off-time t_{off} in 6.9 is substituted by 4.7 to obtain the new equation 6.10.

$$\frac{f_{PWM}}{2 \cdot (1 - d)} < f_{res} < \frac{f_{PWM}}{(1 - d)} \tag{6.10}$$

On the basis that the input-output relationship of the voltage can be described by 4.30, the following equation is formulated.

$$\frac{f_{PWM}}{2 \cdot (1 - \frac{V_{out}}{V_{in}} \cdot \frac{N_P}{N_S})} < f_{res} < \frac{f_{PWM}}{(1 - \frac{V_{out}}{V_{in}} \cdot \frac{N_P}{N_S})} \tag{6.11}$$

This allows to calculate an upper and a lower bound for the resonance frequency depending on the given input voltage.

In figure 6.1 the resonance capacitance C_r is plotted as a function of the magnetizing inductance L_m and resonance frequency at its respective input voltage.

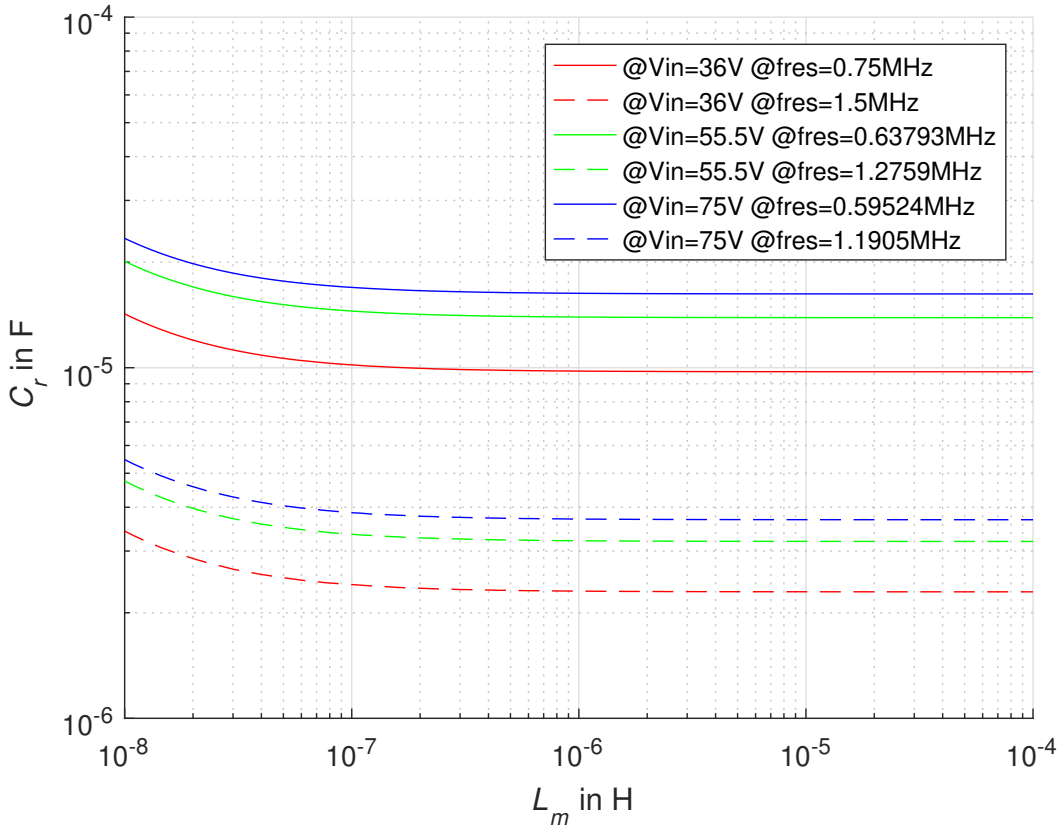

Figure 6.1: C_r vs L_m at f_{PWM}=1MHz and at different input voltages V_{in}

Only the value pairs C_r-L_m, which occur between the red solid line and the blue dashed line, are considered for the circuit design. This section is suitable for all planned input voltages.

In order to make a further restriction in the design, the occurring currents and voltages of these components are investigated.

Based on the earlier assumption of the relation between input and output voltage 4.30, the necessary duty cycle is calculated. With this in turn, the on-time t_{on} is computed.

Figure 6.2 shows those maximum and minimum expected currents i_{Lm} and voltages u_{Cr} in the converter on mode at different C_r-L_m pairings.

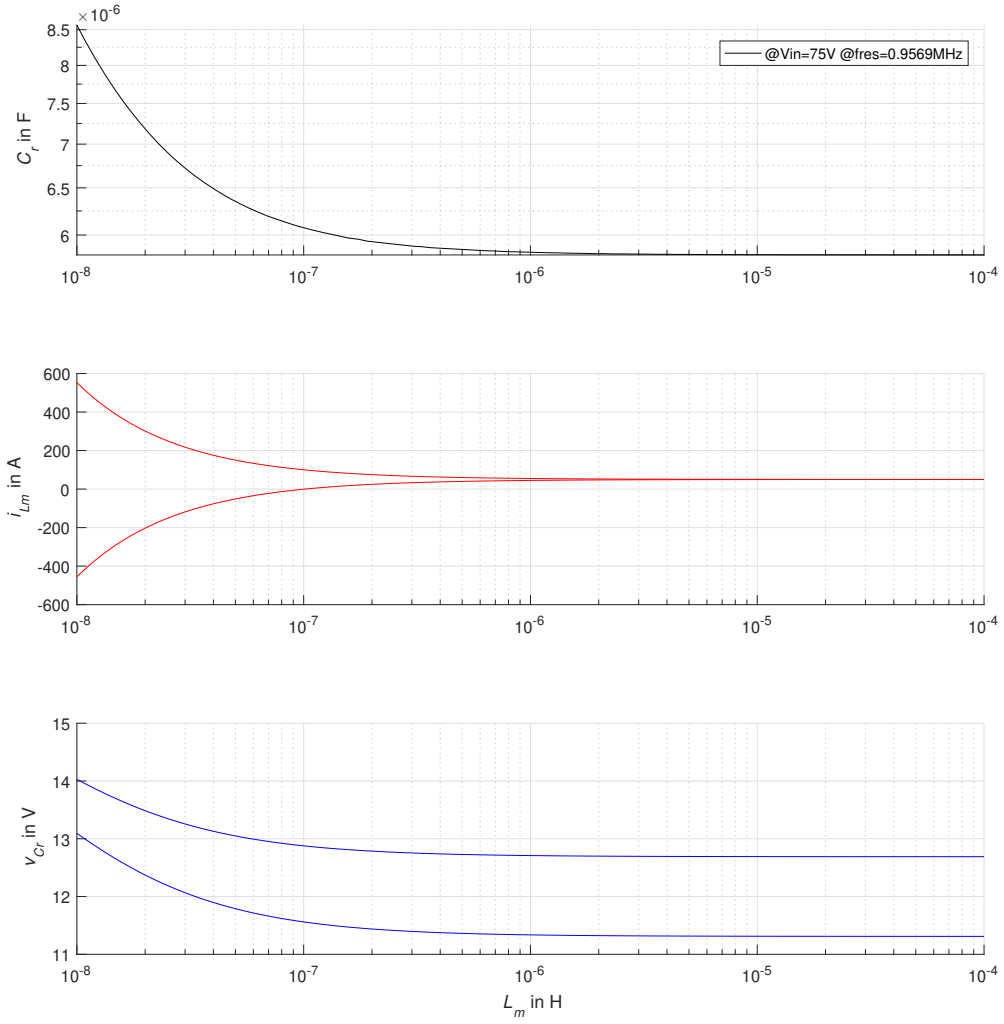

Figure 6.2: C_r vs L_m and assumed i_{Lm} and v_{Cr} at on mode, $V_{in} = 75V$, $P_{out} = 600W$. (worst case)

In this situation the supply voltage is connected to a capacitor in series with an inductor, while a series resonant circuit is present here.
As shown in the figure above, it can be expected that the current increases as the inductance decreases.

To keep the i^2R losses small, a magnetization inductance L_m of 1µH has been chosen. From the abundance of possible resonance capacitances C_r, 6 µF has been selected, since it is relatively centrally located between the shell curves in figure 6.1.

6.1.6 State Space Simulation

The first design step being done, the state space simulation for different input voltages as well as for different output powers is carried out with the help of a Matlab programme.

Figure 6.3 shows the current circuit with the selected component values.

The simulation script automatically regulates the output voltage to the desired value of 12V. In order to define the amount of power to be transmitted, only the load resistance on the output side must be set accordingly.

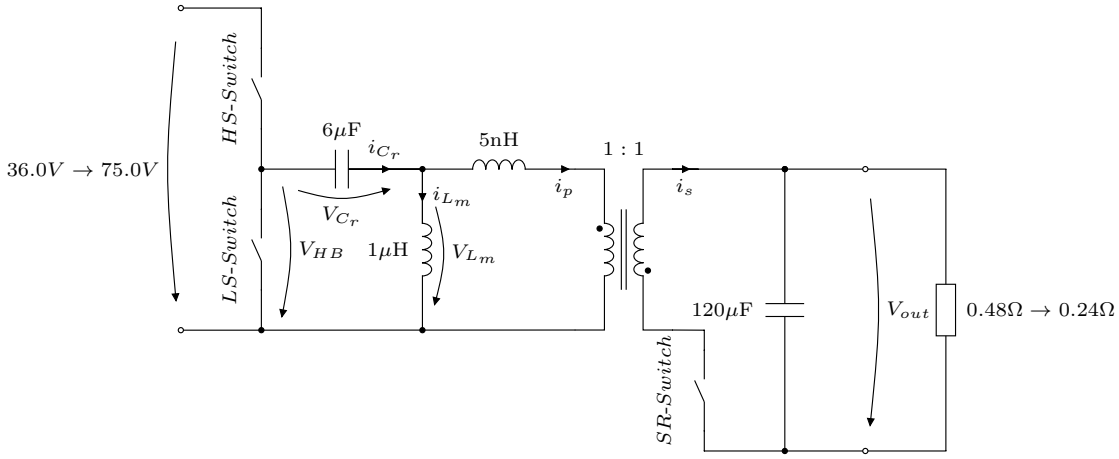

Figure 6.3: Circuit of first design iteration

The situation with the nominal input voltage V_{in}=55.5V and the nominal output power P_{out}=450W is examined.

The two conversion modes can be easily distinguished in figure 6.4 by the current flow of the leakage inductance i_P. If it is 0 A, the circuit is in the first operation mode, the charging mode. If the current is not 0, the circuit is in the second operation mode, the transmission mode.

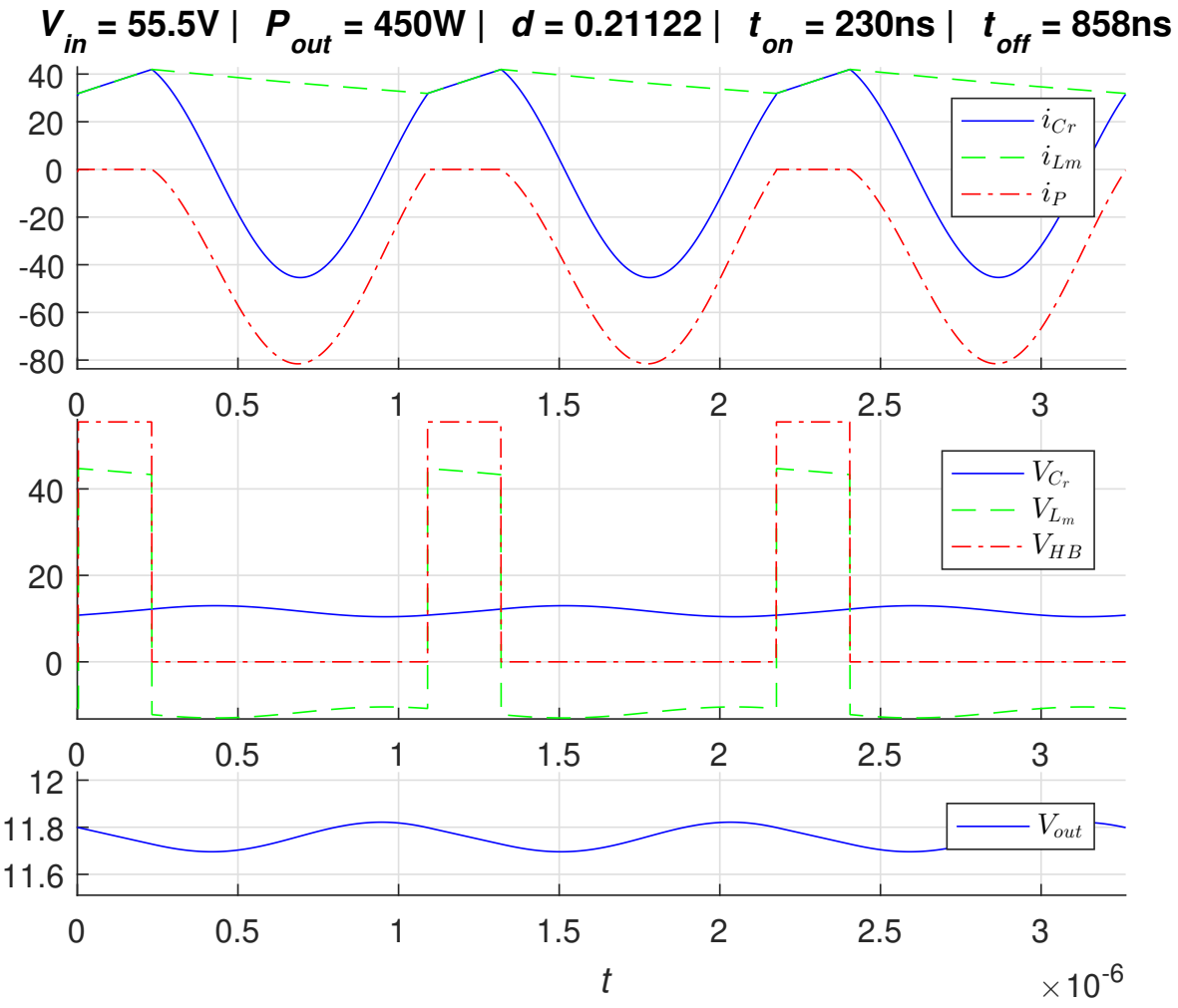

Figure 6.4: Simulation result of first design @V_{in} = 55.5V and P_{out} = 450W

It is noticeable that the current through the magnetising inductance i_{Lm} is always positive and remains that way. As described in chapter 5.7.2.3.1, a negative current at the end of the second mode is desirable, as it enables a ZVS of the half bridge. Since this is not the case here, it must be assumed that the switching losses have to be taken into consideration.

Apart from that, the desired output voltage is successfully achieved at a switching frequency of 0.919MHz, at nominal input voltage and nominal output power.

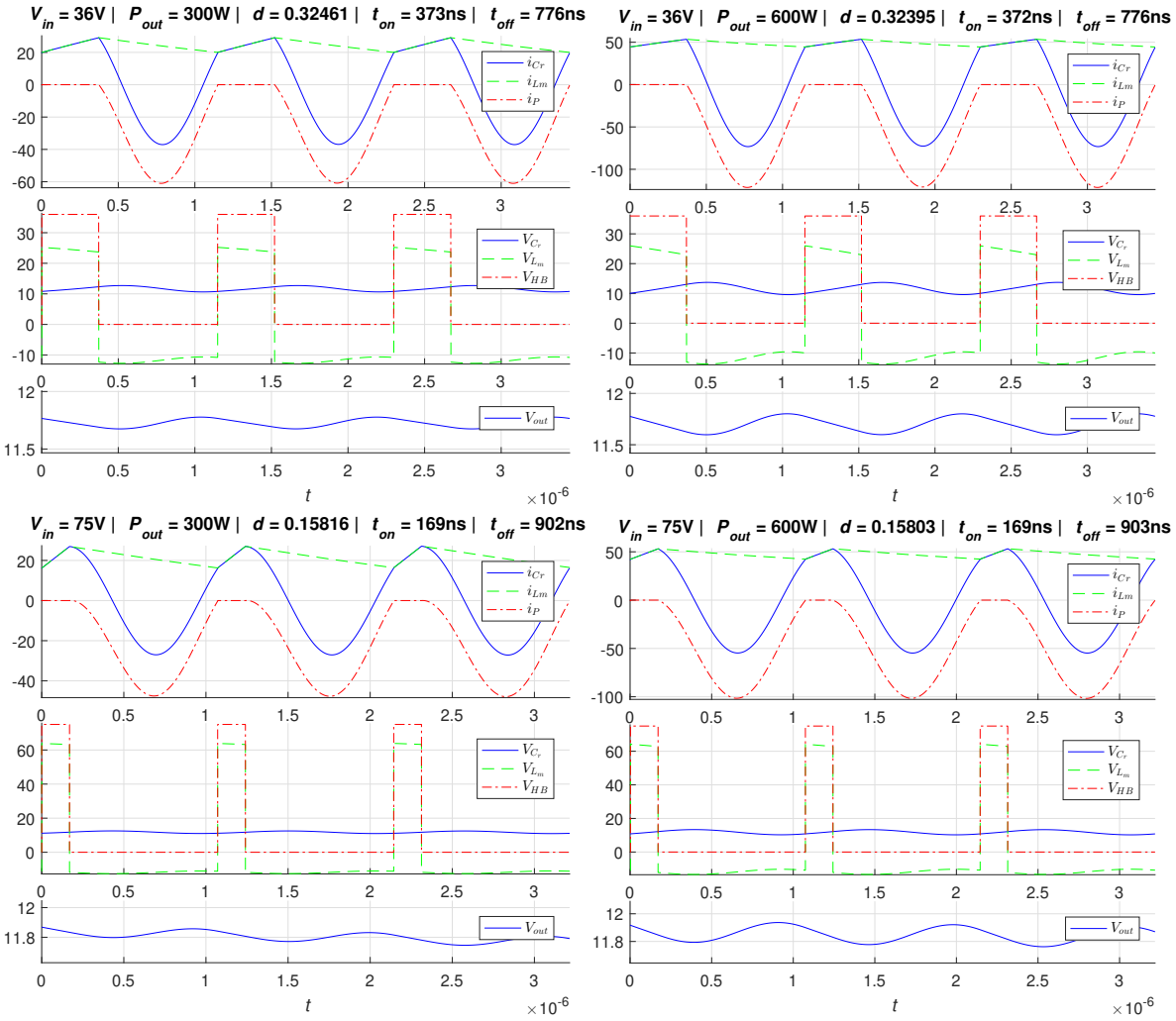

Figure 6.5: Simulation result of first design

The general behaviour of this converter remains similar over the entire input voltage range and load range. This means that the desired ZVS behaviour of the half bridge, when switching from the second to the first mode, is completely absent.

The only way to achieve the ZVS would now be to further reduce the magnetising inductance L_m (Second design 6.2).

V_{in}	P_{out}	V_{out}	ZVS@LS2HS
36 V	300 W	✓	
36 V	600 W	✓	
75 V	300 W	✓	
75 V	600 W	✓	
55.5 V	450 W	✓	

Table 6.6: Summary: C_r=6 µF, L_m=1 µH, L_σ=5 nH, C_{out}=120 µF, $\frac{N_P}{N_S} = 1$

6.2 Second Design

This design iteration is identical to the previous one, except that the component value of the magnetising inductance L_m has been selected to be 100 nH.

6.2.1 State Space Simulation

Figure 6.6 shows the current circuit with the selected component values.

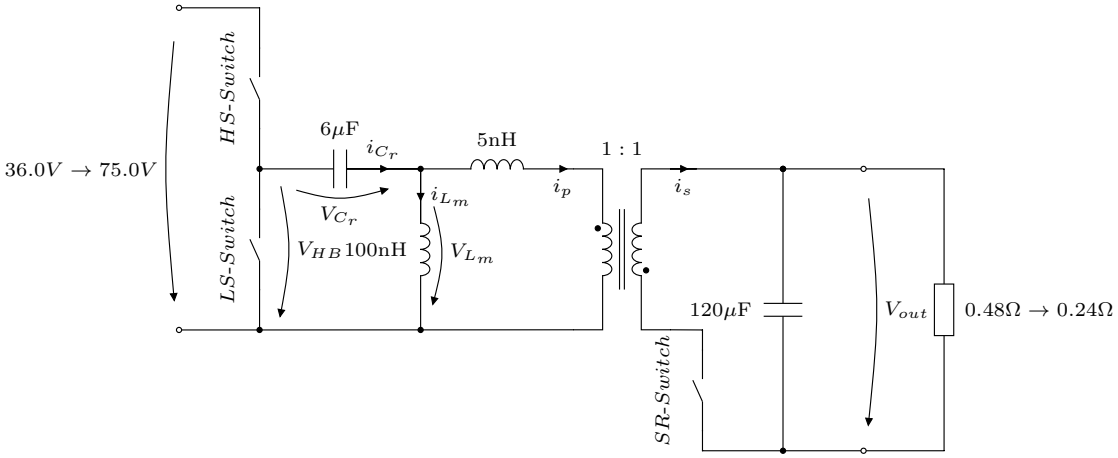

Figure 6.6: Circuit of second design iteration

The simulation result for the nominal input voltage V_{in}=55.5 V and the nominal output power P_{out} = 450 W is shown in 6.7.

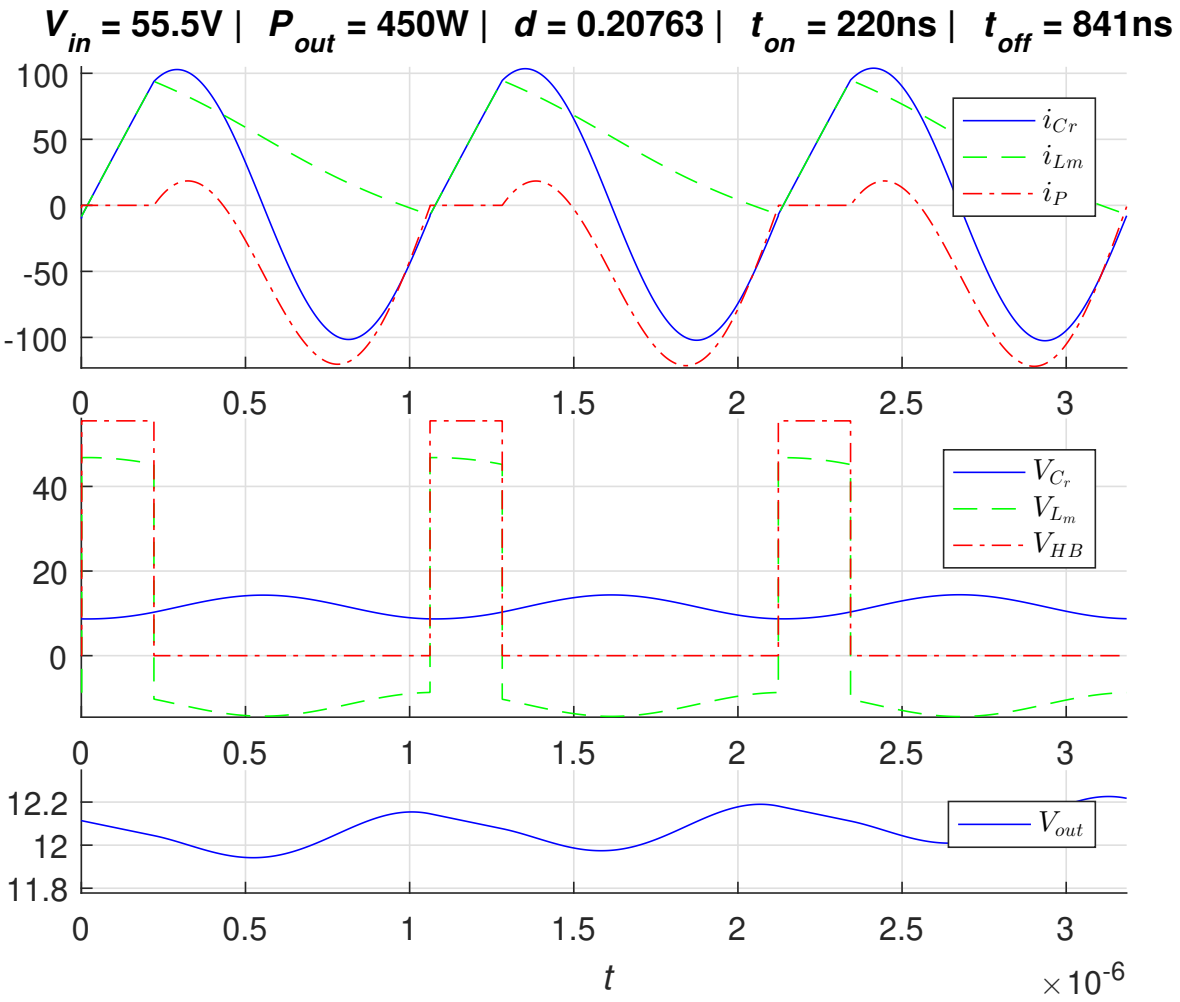

Figure 6.7: Simulation result of second design @V_{in} = 55.5V and P_{out} = 450W

It can be seen that now the current through the magnetizing inductor i_{Lm} is negative at the end of the second mode, implying that the desired ZVS behaviour of the half bridge is now possible.

Now there is also a new behaviour that has not been considered before.
In this topology, it has been assumed so far that the transformer only serves to transfer energy from the primary to the secondary side. Which in this circuit (figure 6.6) would mean that the current i_P would always have to be negative.
In figure 6.7 this is not the case.

This behaviour is made possible by the fact that the synchronous rectifier, which is a controllable switch, not only conducts the forward current, but can also conduct a

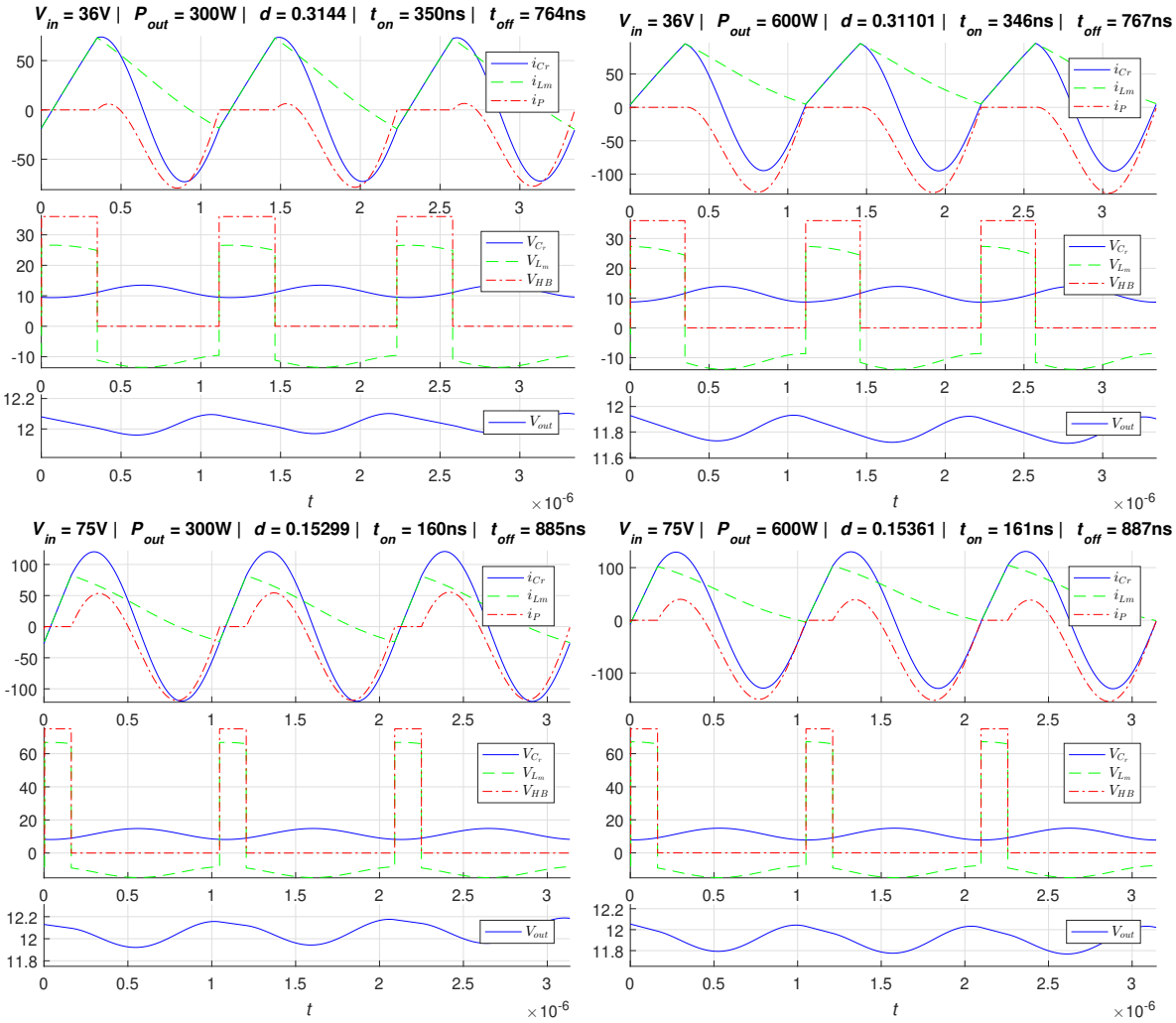

Figure 6.8: Simulation result of second design

reverse current if required. This is intentional, because otherwise this circuit is not able to achieve the desired output voltage.
At the expense of additional reactive power in the converter, the output voltage can be reached.

As can be seen in Figure 6.8, the ZVS behaviour is not obtained in all operating points.
To have ZVS at all operating points, the magnetizing inductance L_m is further reduced (third design 6.3).

V_{in}	P_{out}	V_{out}	ZVS@LS2HS	reactive power
36 V	300 W	✓	✓	✓
36 V	600 W	✓		
75 V	300 W	✓	✓	✓
75 V	600 W	✓		✓
55.5 V	450 W	✓	✓	✓

Table 6.7: Summary: C_r=6 µF, L_m=100 nH, L_σ=5 nH, C_{out}=120 µF, $\frac{N_P}{N_S} = 1$

6.3 Third Design

This design iteration is identical to the previous one, except that the component value of the magnetising inductance L_m has been selected to be 75 nH.

6.3.1 State Space Simulation

Figure 6.9 shows the current circuit with the selected component values.

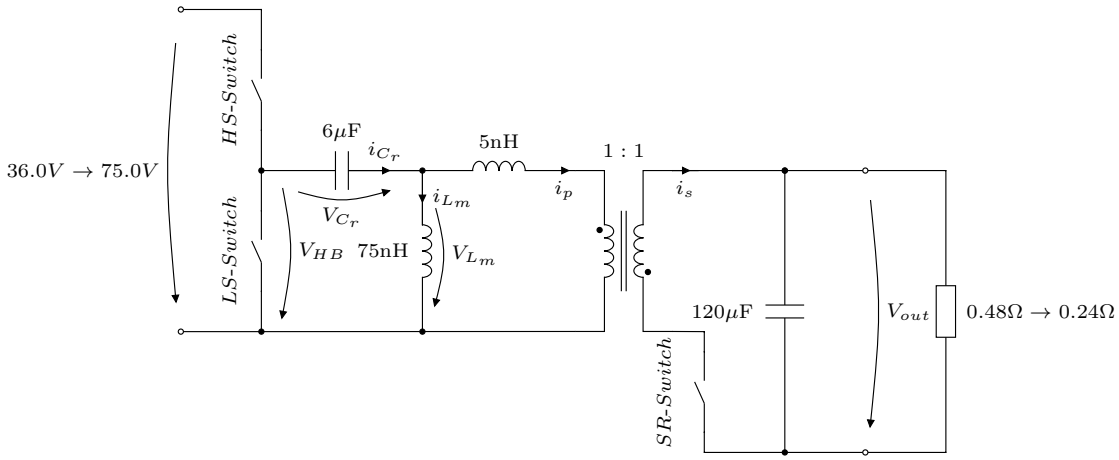

Figure 6.9: Circuit of third design iteration

The simulation result for the nominal input voltage V_{in}=55.5 V and the nominal output power P_{out} = 450 W is shown in 6.10.

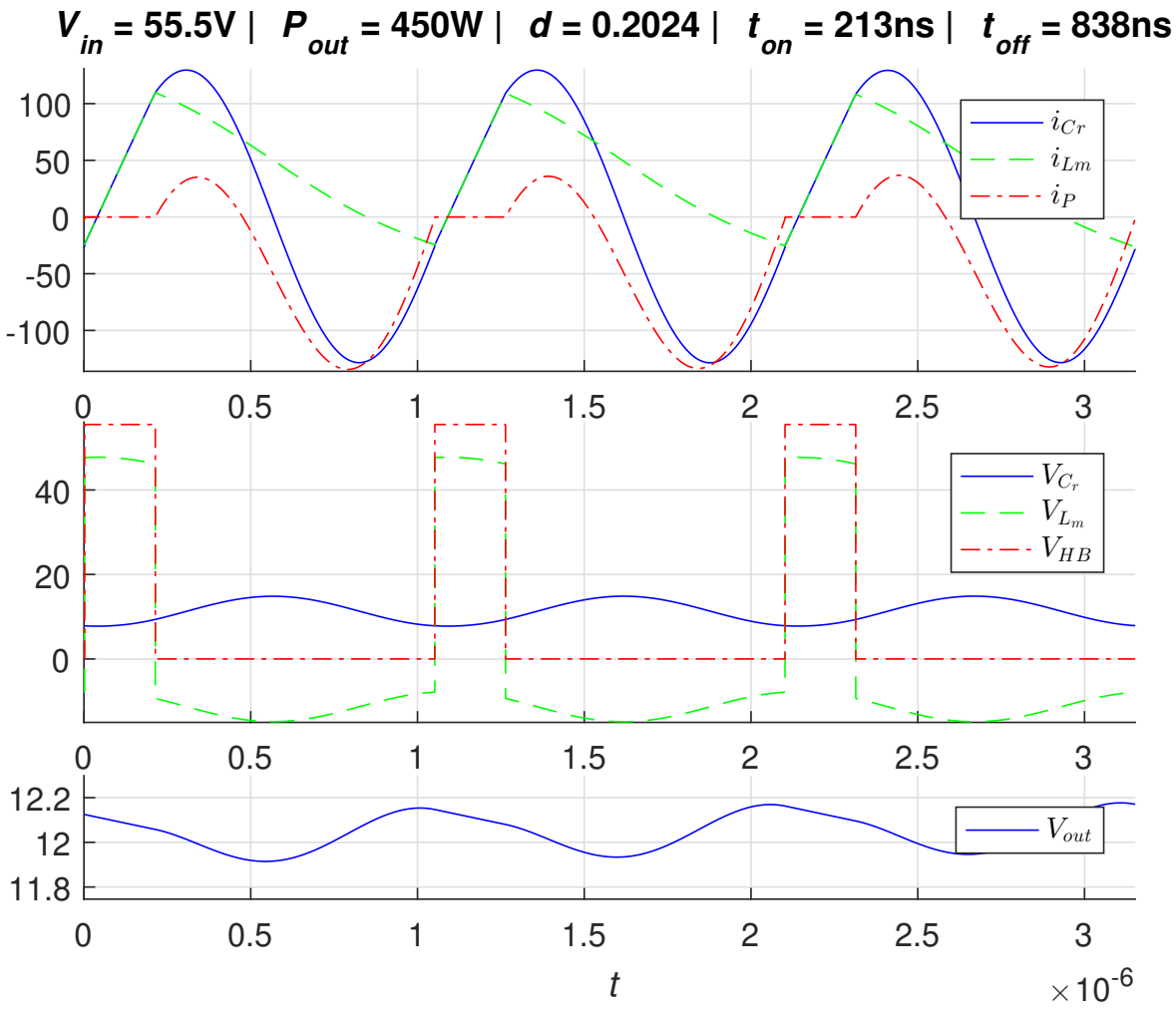

Figure 6.10: Simulation result of third design @V_{in} = 55.5V and P_{out} = 450W

Like the previous design, the ZVS behavior is prevalent.

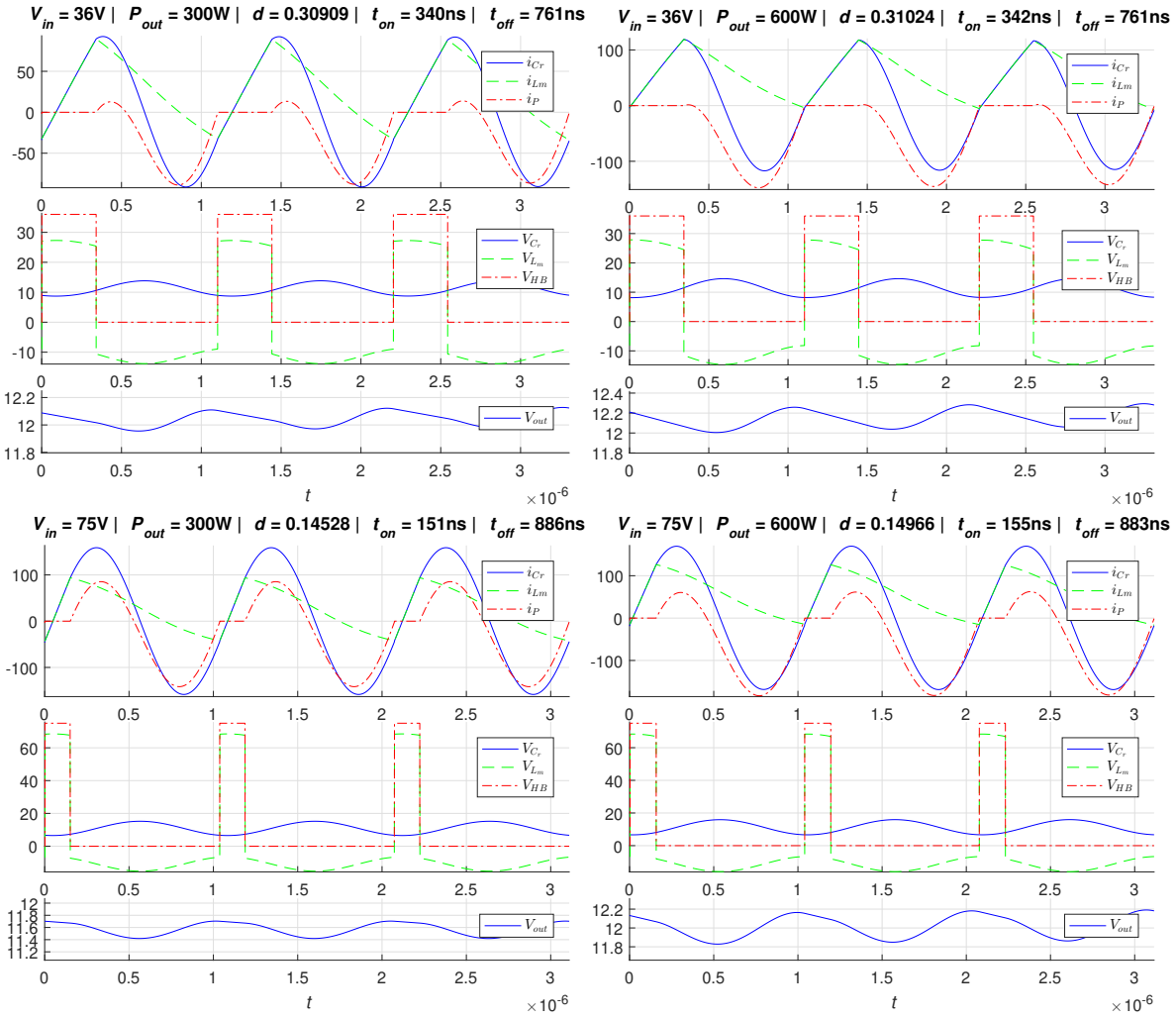

Figure 6.11: Simulation result of third design

As can be seen in Figure 6.11, the ZVS behaviour is achieved at all operating points.

V_{in}	P_{out}	V_{out}	ZVS@LS2HS	reactive power
36 V	300 W	✓	✓	✓
36 V	600 W	✓	✓	
75 V	300 W	✓	✓	✓
75 V	600 W	✓	✓	✓
55.5 V	450 W	✓	✓	✓

Table 6.8: Summary: C_r=6 µF, L_m=75 nH, L_σ=5 nH, C_{out}=120 µF, $\frac{N_P}{N_S} = 1$

Chapter 7

Loss Performance Survey

The third design satisfies the required key parameters and exhibits ZVS behavior for the half-bridge.
Next, the power dissipation of the components of this topology is investigated here. The current and voltage curves at nominal input voltage ($55.5V$) and nominal output power ($450W$) of the third design are selected for this loss analysis.

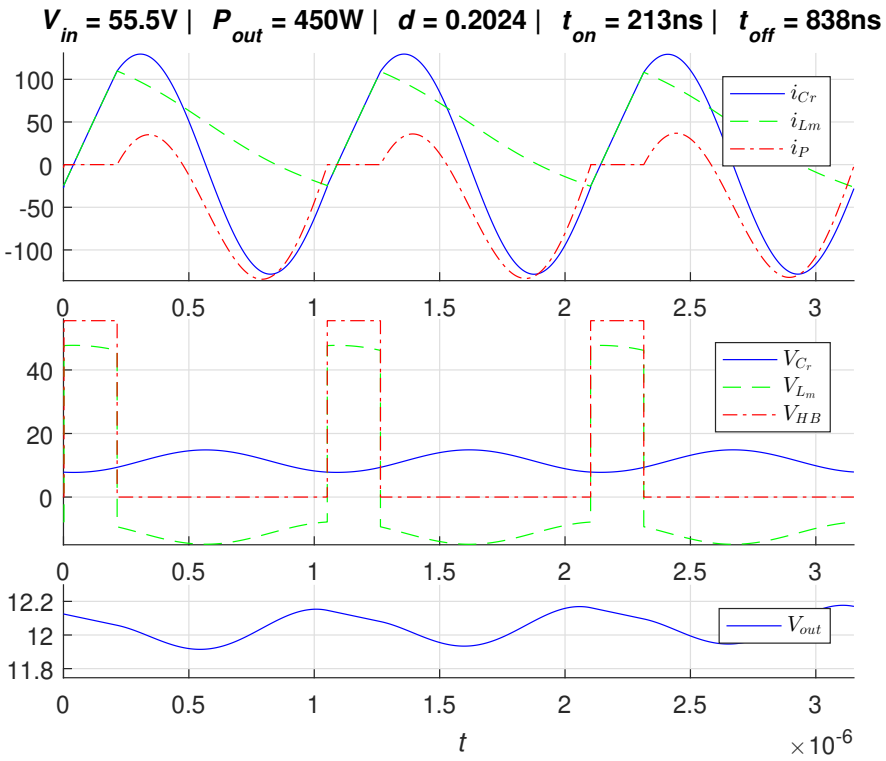

Figure 7.1: Simulation result of third design (6.3) @V_{in} = $55.5V$ and P_{out} = $450W$

7.1 Transformer: conductor losses

The additional losses in the conductive material caused by the skin effect and proximity effect can be calculated as explained in chapter 5.2.2.

From the current spectrum, 500 frequencies were used to calculate the losses.

Layer Nr.	Side	Turns	R_{DC} mΩ	$dMMF$ A	MMF A	$P_{Cu,AC}$ W
1	P	1	0.819	0.2	0.2	0.265
2	S	1	0.819	-0.25	-0.05	0.414
3	P	1	0.819	0.2	0.15	0.265
4	S	1	0.819	-0.25	-0.1	0.414
5	P	1	0.819	0.2	0.1	0.265
6	S	1	0.819	-0.25	-0.15	0.414
7	P	1	0.819	0.2	0.05	0.265
8	S	1	0.819	-0.25	-0.2	0.414
9	P	1	0.819	0.2	0	0.265

Table 7.1: Planar transformer layer structure and conductor losses per layer

Table 7.1 assigns the corresponding losses to each layer of the multilayer board.

$$\begin{aligned} \text{Conductor primary side losses} \quad & P_{Cu,AC,P} = 1.326\,\text{W} \\ \text{Conductor secondary side losses} \quad & P_{Cu,AC,S} = 1.657\,\text{W} \end{aligned}$$

Since a uniform current sharing is assumed in the parallel layers, these results are considered as the minimum expected losses.

7.2 Transformer: magnetic losses

Section 5.2.3 describes the procedure for calculating the magnetic losses.

The switching frequency f_{sw} of the converter determined by the simulation is 951.5 kHz.
Therefore, the core material designed for such high frequencies is **3F3**.
In order to be able to apply the Steinmetz equation, the equivalent frequency $f_{sin,eq}$ must first be determined, see equation 5.18.

$$f_{sin,eq} = 1180.9\,\text{kHz} \tag{7.1}$$

$$P_{core}/V = 542.2\,\text{mW/cm}^3 \tag{7.2}$$

$$\text{Magnetic losses} \quad P_{Mag} = 2.928\,\text{W}$$

7.3 Magnetizing Inductance

The magnetization inductance has to be included in the loss calculation of the circuit.

For the external magnetization inductance, another magnetic core of the same type **ER 18/3.2/10** and the same material as for the transformer is used.
To obtain the desired inductance, 2 turns must be placed in the winding space and an air gap of 2 mm in total is necessary.
If this were to be constructed with a multilayer board with 9 layers, the following losses would occur.

$$\text{Conductor losses} \quad P_{Cu,AC,L_m} = 1.802\,\text{W}$$
$$\text{Magnetic losses} \quad P_{Mag,AC,L_m} = 2.460\,\text{W}$$

7.4 I^2R- losses

The corresponding current characteristics were taken from the state space simulation in order to determine the resistance losses.

7.4.1 MOSFET: I^2R- losses

In order to allow an approximate loss calculation, a choice for the semiconductor switches has to be made. For this reason, the **IPT026N10N5** [16] a product from Infineon was selected. This has a $R_{DS,on}$ value of 2.6 mΩ.

$$\begin{aligned} I^2R\text{- losses of half bridge} \quad P_{HB} &= 90.2914\,\mathrm{A}^2 \cdot R_{DS,on} \\ &= 90.2914\,\mathrm{A}^2 \cdot 2.6\,\mathrm{m\Omega} = 0.235\,\mathrm{W} \\ I^2R\text{- losses of synchronous rectifier} \quad P_{SR} &= 69.2207\,\mathrm{A}^2 \cdot R_{DS,on} \\ &= 69.2207\,\mathrm{A}^2 \cdot 2.6\,\mathrm{m\Omega} = 0.180\,\mathrm{W} \end{aligned}$$

7.4.2 Capacitors: I^2ESR- losses

A product of muRata was chosen for the resonant capacitor C_r, **GRM219R7YA105MA12** [17]. The resonant capacitor exhibits a DC voltage of about 10 V during operation, thus the capacitance changes from 1 µF to 0.755 µF according to the manufacturer's data sheet. This results in the need to connect 8 of these components in parallel. At the switching frequency that occurs, such a capacitor has an ESR of 6 mΩ.

$$\begin{aligned} I^2R\text{- losses of } C_r \quad P_{C_r} &= 90.2914\,\mathrm{A}^2 \cdot \frac{ESR_{C_r}}{n} \\ &= 90.2914\,\mathrm{A}^2 \cdot \frac{6\,\mathrm{m\Omega}}{8} = 0.068\,\mathrm{W} \end{aligned}$$

For the output capacitor C_{out}, **GRM43ER61C226ME01** [18] a product of muRata was chosen. The output capacitor exhibits a DC voltage of about 12 V during operation. This means that the capacitance drops from 22 µF at this DC voltage to

16 μF according to the manufacturer's data sheet. This results in the need to connect 8 of these components in parallel. At the switching frequency that occurs, the ESR of one capacitor has 3 mΩ.

$$\begin{aligned} I^2R\text{- loss of } C_{out} \quad P_{C_{out}} &= 57.5096\,\mathrm{A}^2 \cdot \frac{ESR_{C_{out}}}{n} \\ &= 57.5096\,\mathrm{A}^2 \cdot \frac{3\,\mathrm{m\Omega}}{8} = 0.021\,\mathrm{W} \end{aligned}$$

7.5 MOSFET: Gate Driving Losses

From the datasheet [16] of the selected MOSFET the gate charge Q_g (96 nC) and the gate-source voltage V_{GS} (10 V) are taken, which are used for the approximate calculation of the gate driving losses.

$$\begin{aligned} \text{Gate driving losses} \quad P_{drive,HB+SR} &= n \cdot f_{SW} \cdot Q_g \cdot V_{GS} \\ &= 3 \cdot 951.5\,\mathrm{kHz} \cdot 96\,\mathrm{nC} \cdot 10\,\mathrm{V} = 2.740\,\mathrm{W} \end{aligned}$$

7.6 Loss Overview at Nominal Operating Point

Conductor primary side losses	$P_{Cu,AC,P}$	1.326 W
Conductor secondary side losses	$P_{Cu,AC,S}$	1.657 W
Transformer magnetic losses	P_{Mag}	2.928 W
L_m conductor losses	P_{Cu,AC,L_m}	1.802 W
L_m magnetic losses	P_{Mag,AC,L_m}	2.460 W
I^2R- losses of half bridge	P_{HB}	0.235 W
I^2R- losses of synchronous rectifier	P_{SR}	0.180 W
Gate driving losses	$P_{drive,HB+SR}$	2.740 W
I^2R- losses of C_r	P_{C_r}	0.068 W
I^2R- loss of C_{out}	$P_{C_{out}}$	0.021 W
Total losses	P_{losses}	13.418 W

Table 7.2: Summary of loss performance survey @V_{in} = 55.5 V and @P_{out} = 450W

The efficiency for this operating point can now be calculated from this table.

$$\eta = \frac{P_{out}}{P_{out} + P_{losses}} = \frac{450\,\text{W}}{450W + 13.418\,\text{W}} = 97.1\,\% \tag{7.3}$$

7.7 Loss Summary

In the table 7.3 all losses considered so far are now also shown for the other operating points.
The efficiency for these operating points is also given.
Figure 7.2 shows the efficiency as a function of the output power.
In the appendix A an example of such a loss report of the made Python program is shown.

V_{in}	36.0V	55.5V	75.0V	36.0V	55.5V	75.0V	36.0V	55.5V	75.0V
P_{out}	300W	300W	300W	450W	450W	450W	600W	600W	600W
$P_{Cu,AC,P}$	0.501W	0.989W	1.964W	0.857W	1.326W	2.263W	1.417W	1.954W	2.704W
$P_{Cu,AC,s}$	0.627W	1.236W	2.455W	1.072W	1.657W	2.828W	1.772W	2.443W	3.380W
P_{Mag}	1.426W	2.889W	4.567W	1.429W	2.928W	4.621W	1.430W	2.957W	4.629W
P_{Cu,AC,L_m}	1.195W	1.414W	1.584W	1.518W	1.802W	1.939W	2.008W	2.446W	2.429W
P_{Mag,AC,L_m}	1.195W	2.424W	3.844W	1.200W	2.460W	3.892W	1.206W	2.489W	3.903W
P_{HB}	0.162W	0.223W	0.291W	0.178W	0.235W	0.300W	0.202W	0.253W	0.311W
P_{SR}	0.112W	0.150W	0.206W	0.150W	0.180W	0.227W	0.196W	0.226W	0.254W
$P_{drive,HB+SR}$	2.623W	2.751W	2.785W	2.621W	2.748W	2.783W	2.618W	2.745W	2.783W
P_{C_r}	0.047W	0.064W	0.084W	0.051W	0.068W	0.087W	0.058W	0.073W	0.090W
$P_{C_{out}}$	0.013W	0.020W	0.028W	0.016W	0.022W	0.030W	0.020W	0.025W	0.031W
P_{losses}	7.901W	12.159W	17.809W	9.092W	13.425W	18.969W	10.927W	15.611W	20.515W
η	97.43 %	96.10 %	94.40 %	98.02 %	97.10 %	95.96 %	98.21 %	97.46 %	96.69 %

Table 7.3: Summary of loss performance survey

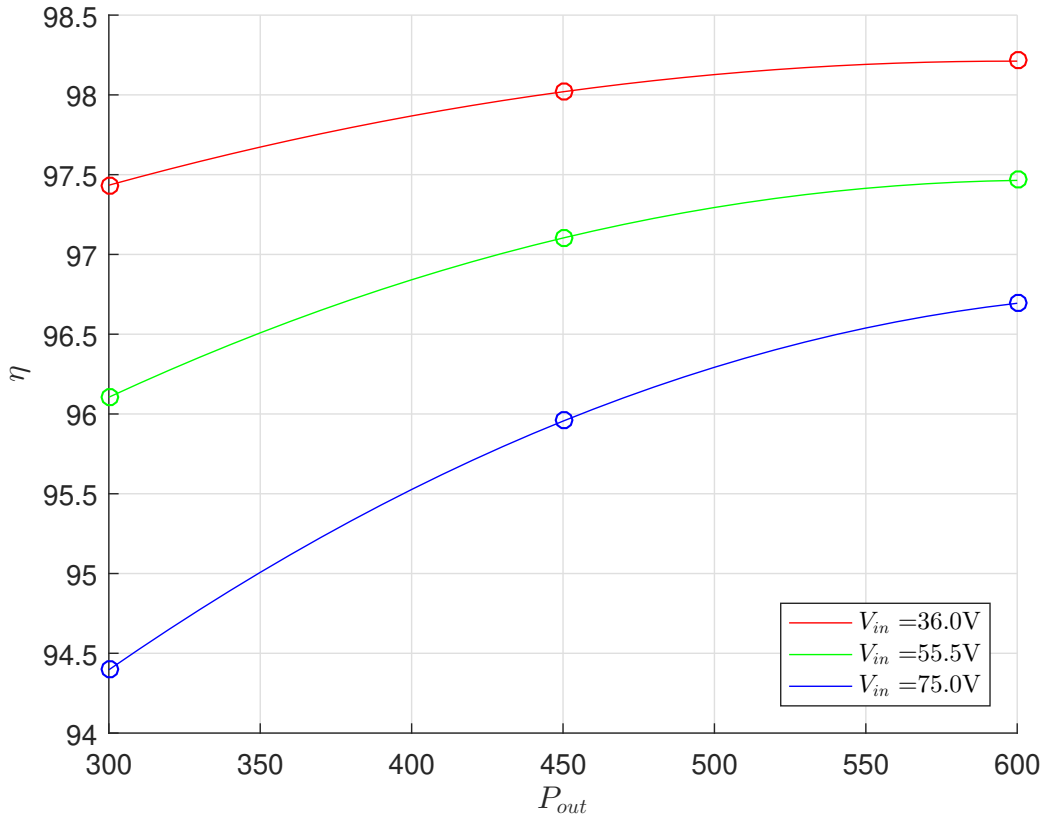

Figure 7.2: Efficiency at different operating points

Chapter 8

Example designs with added constraints

There was interest within the company to see if this topology would also work with an increased leakage inductance value.
If this topology were ever to be built, it would anyway be necessary to carry out a detailed FEM simulation beforehand in order to obtain the best possible estimates for the leakage inductance.
The value for leakage inductance L_σ was specified by the company to be $100nH$.

In addition, it was required to verify that the converter can be operated with a minimum reactive component. Meaning that the synchronous rectifier should only conduct current in its forward direction.

From the design point of view, for now, all the selections made for the component values can be taken from the chapter 6 with the exception of the leakage inductance, which has now been given.

8.1 Fourth Design

8.1.1 Magnetizing Inductance L_m vs Resonance Capacitance C_r

Similar to the chapter 6.1.5, all C_r-L_m combinations at different input voltages and resonant frequencies are now calculated.

Only the value pairs C_r-L_m in figure 8.1, which occur between the red full line and the blue dashed line, are considered for the circuit design. This section is suitable for all planned input voltages.

As with the first design, the currents and voltages occurring in these components are now examined in order to make a further restriction in the design.

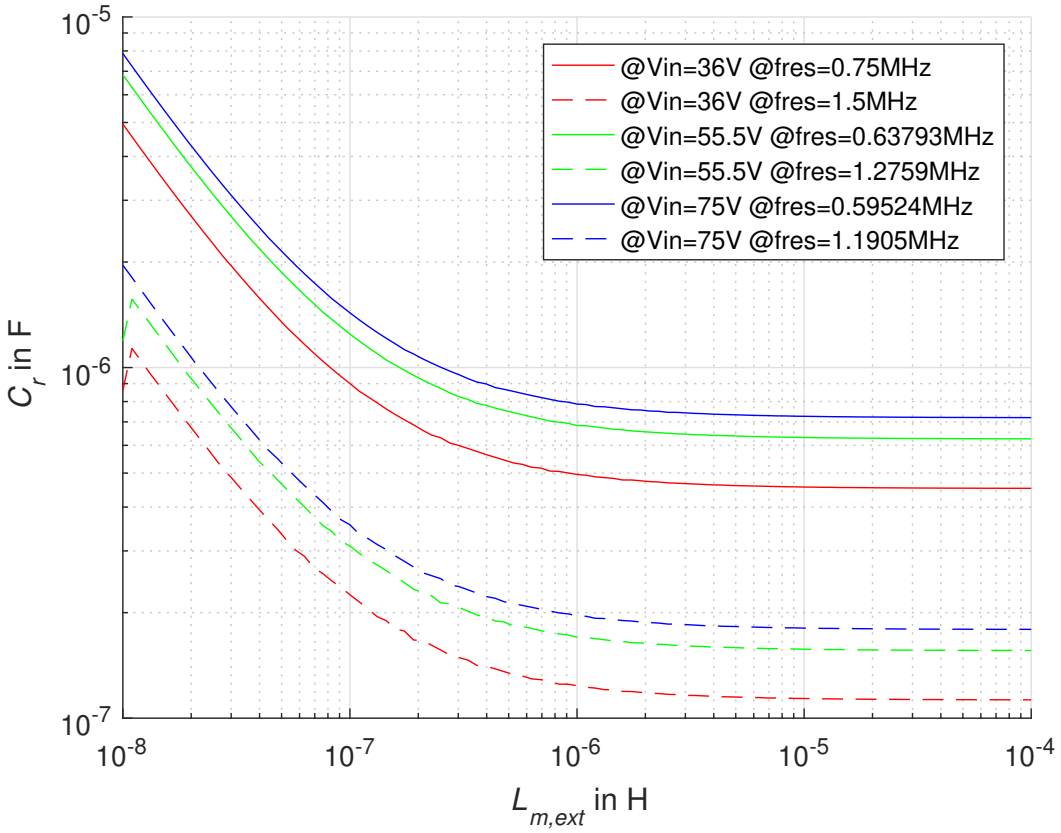

Figure 8.1: C_r vs L_m at f_{PWM}=1MHz and at different input voltages V_{in}

Figure 8.2 shows those maximum and minimum expected currents i_{Lm} and voltages v_{Cr} in the converter on mode.

To keep the i^2R losses small, a magnetization inductance L_m of 1µH has been chosen. From the abundance of possible resonance capacitances C_r, 300 nF has been selected, since it is relatively centrally located between the shell curves.

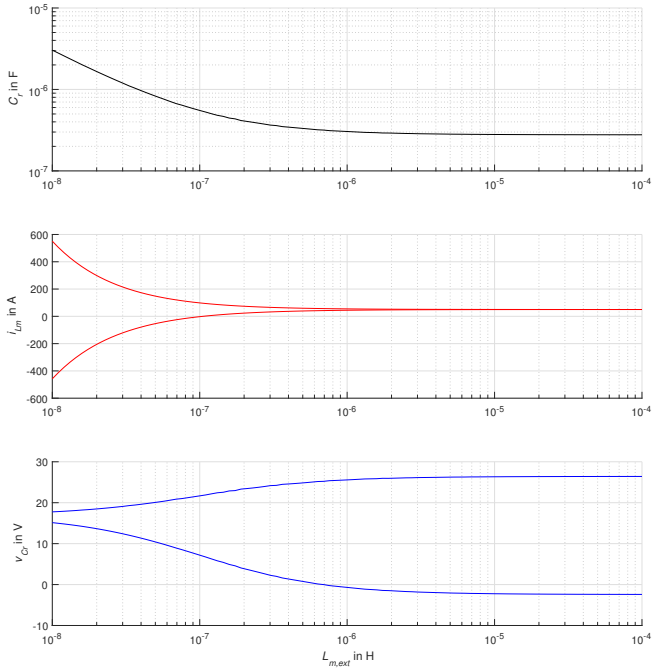

Figure 8.2: C_r vs L_m and assumed i_{Lm} and v_{Cr} at on mode, $V_{in} = 75V$, $P_{out} = 600W$. (worst case)

8.1.2 State Space Simulation

Figure 8.3 shows the current circuit with the selected component values.

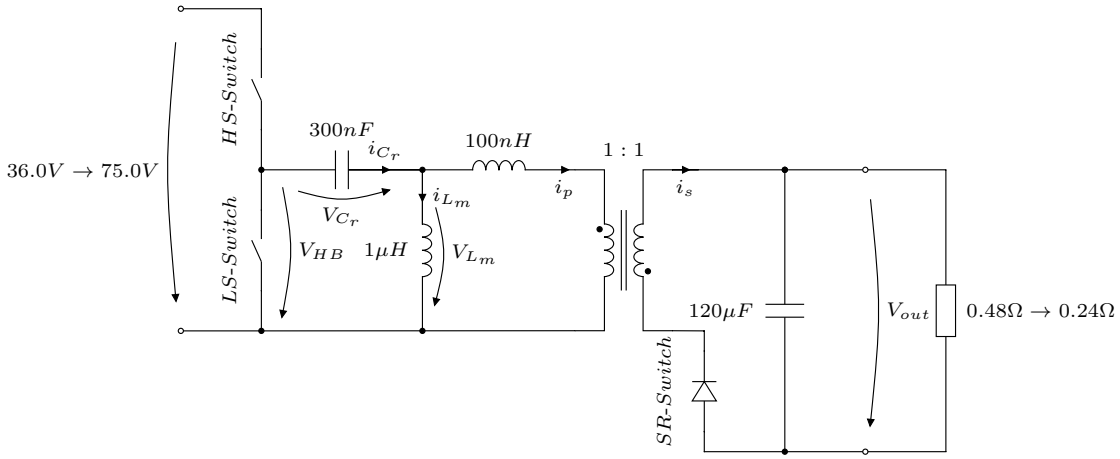

Figure 8.3: Circuit of fourth design iteration

The situation with the nominal input voltage V_{in}=55.5V and the nominal output power P_{out}=450W is examined.

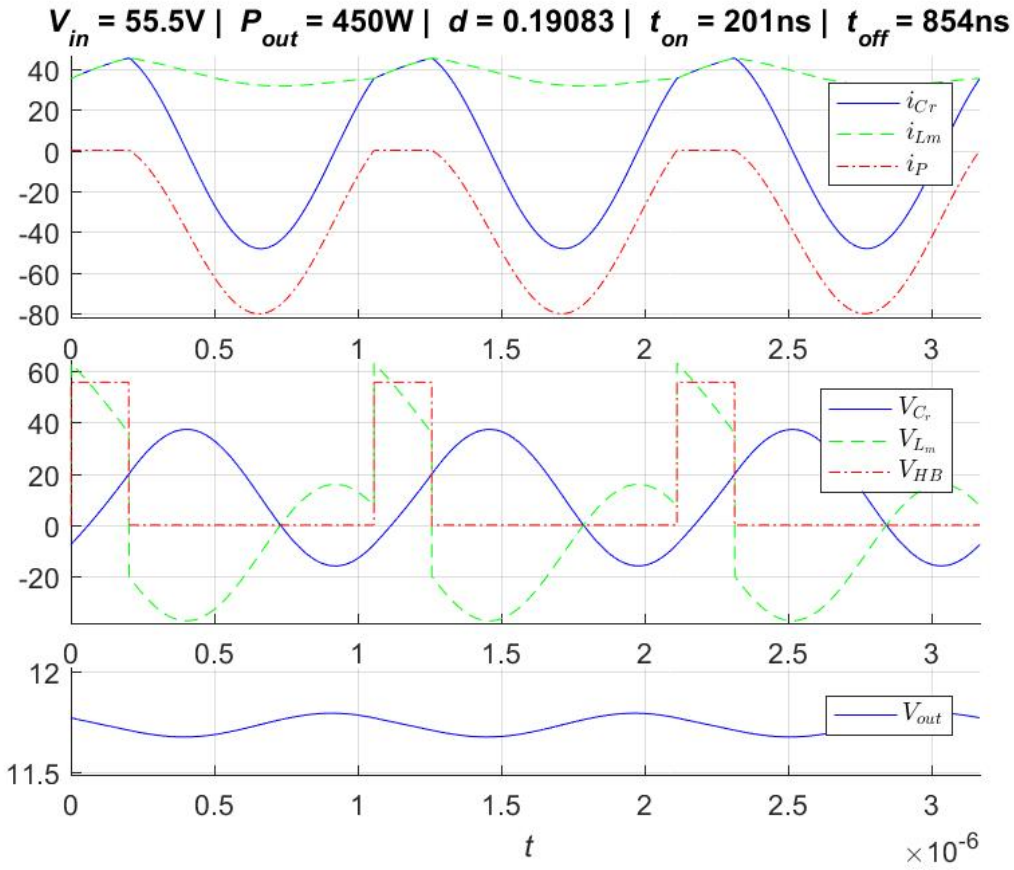

Figure 8.4: Simulation result of fourth design @V_{in} = 55.5V and P_{out} = 450W

At first glance, it can be seen that this is a similar operating case to the first design. Here, too, the current which flows through the magnetizing inductance remains positive and thus a ZVS behavior is not achieved.

The general behaviour of this converter remains similar over the entire input voltage range and load range. This means that the desired ZVS behaviour of the half bridge, when switching from the second to the first mode, is completely absent.

The only way to achieve the ZVS would now be to further reduce the magnetising inductance. However, this would make it more difficult to regulate the desired output voltage. Since the output voltage has not been reached at maximum input voltage and minimum output power, this is not an option. This can be seen in the

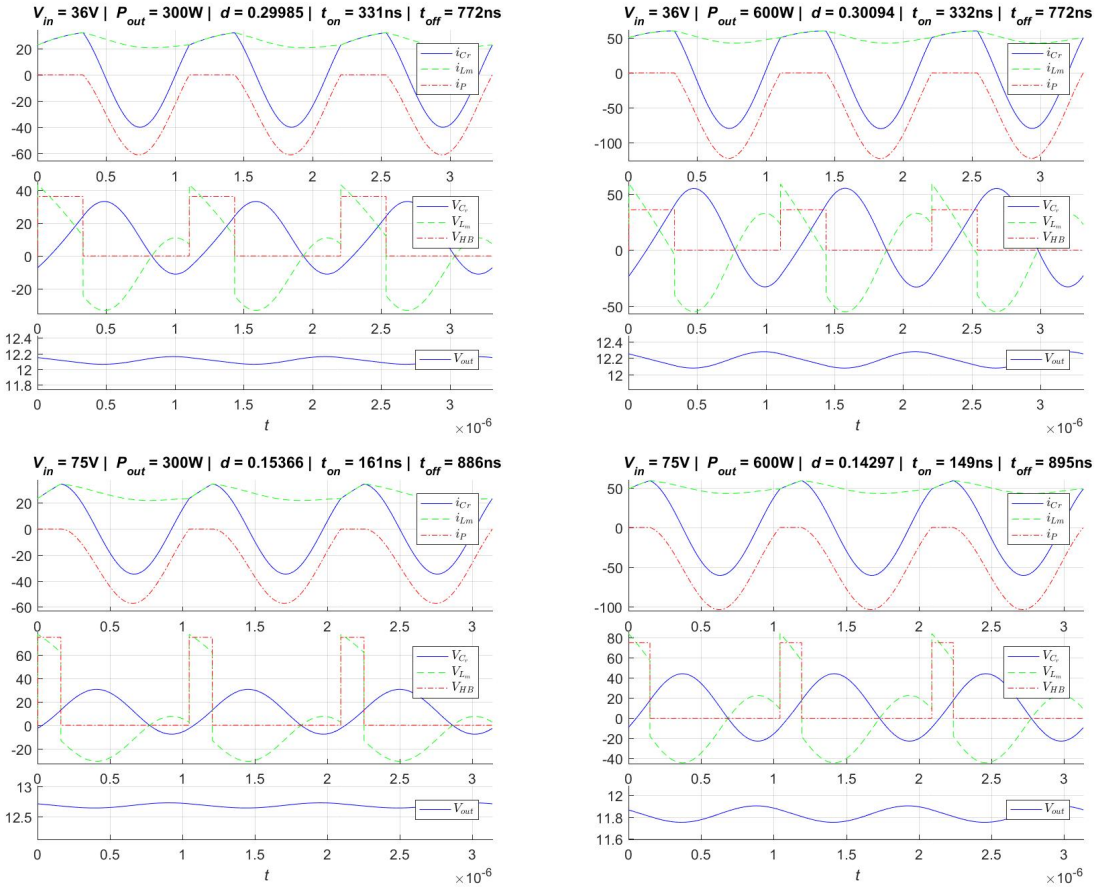

Figure 8.5: Simulation result of fourth design

simulation result at the bottom left of the figures 8.5. This inability to reach the output voltage is due to the fact that no reverse current is allowed through the synchronous rectifier.

At this stage, two possible design changes are possible.
The first one is to make a different selection in the possible range of values for the resonant capacitor C_r (Fifth design 8.2).
If this does not change much, a new design with the transformer winding ratio set to 2:1 has to be drafted (Sixth design 8.3).

V_{in}	P_{out}	controlability of V_{out}	ZVS@LS2HS
36 V	300 W	✓	
36 V	600 W	✓	
75 V	300 W		
75 V	600 W	✓	
55.5 V	450 W	✓	

Table 8.1: Summary: C_r=300 nF, L_m=1 µH, L_σ=100 nH, C_{out}=120 µF, $\frac{N_P}{N_S} = 1$

8.2 Fifth Design

This design iteration is identical to the previous one, except that the component value of the resonant capacitor C_r has been selected to be 200 nF.

8.2.1 State Space Simulation

Figure 8.6 shows the current circuit with the selected component values.

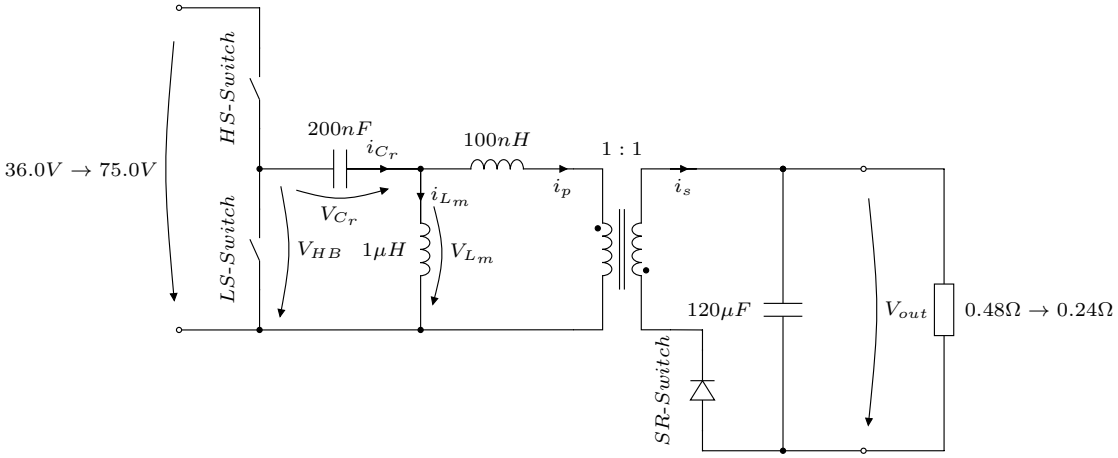

Figure 8.6: Circuit of fifth design iteration

The simulation result for the nominal input voltage V_{in}=55.5 V and the nominal output power P_{out} = 450 W is shown in 8.7.

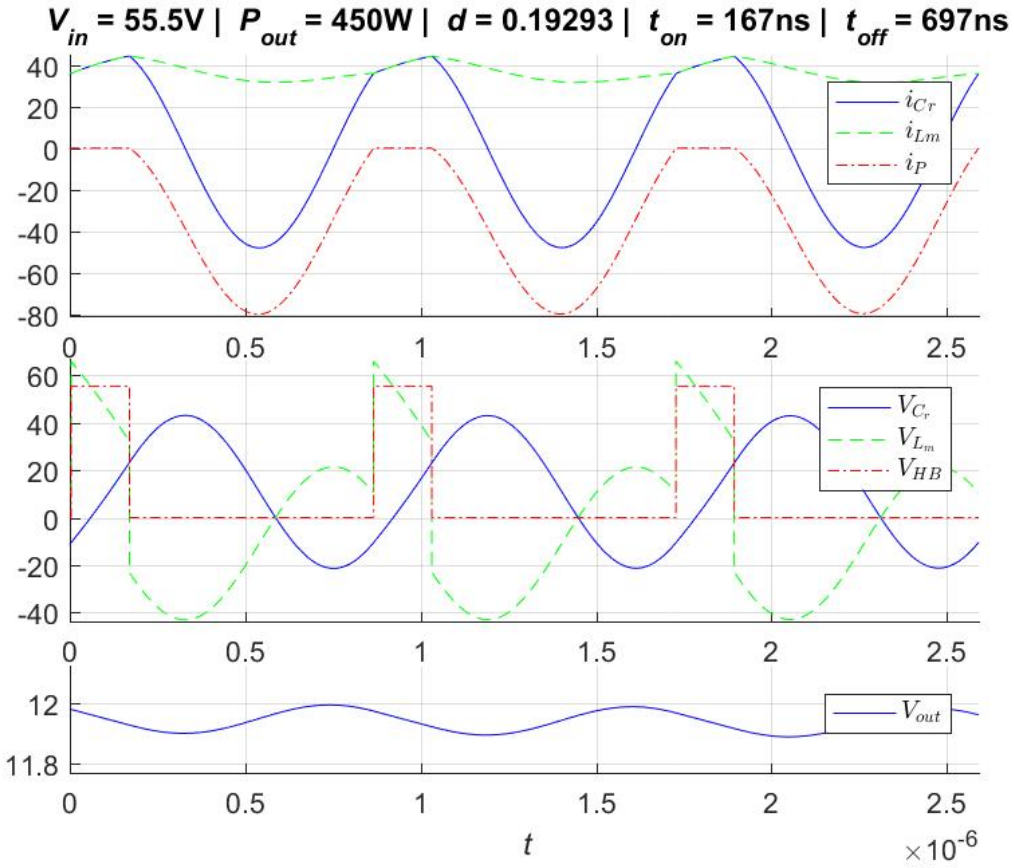

Figure 8.7: Simulation result of fifth design @V_{in} = 55.5V and P_{out} = 450W

As in the previous design, no ZVS behavior is seen. However, the required output voltage can be achieved at all specified operating points.

V_{in}	P_{out}	controlability of V_{out}	ZVS@LS2HS
36 V	300 W	✓	
36 V	600 W	✓	
75 V	300 W	✓	
75 V	600 W	✓	
55.5 V	450 W	✓	

Table 8.2: Summary: C_r=200 nF, L_m=1 µH, L_σ=100 nH, C_{out}=120 µF, $\frac{N_P}{N_S} = 1$

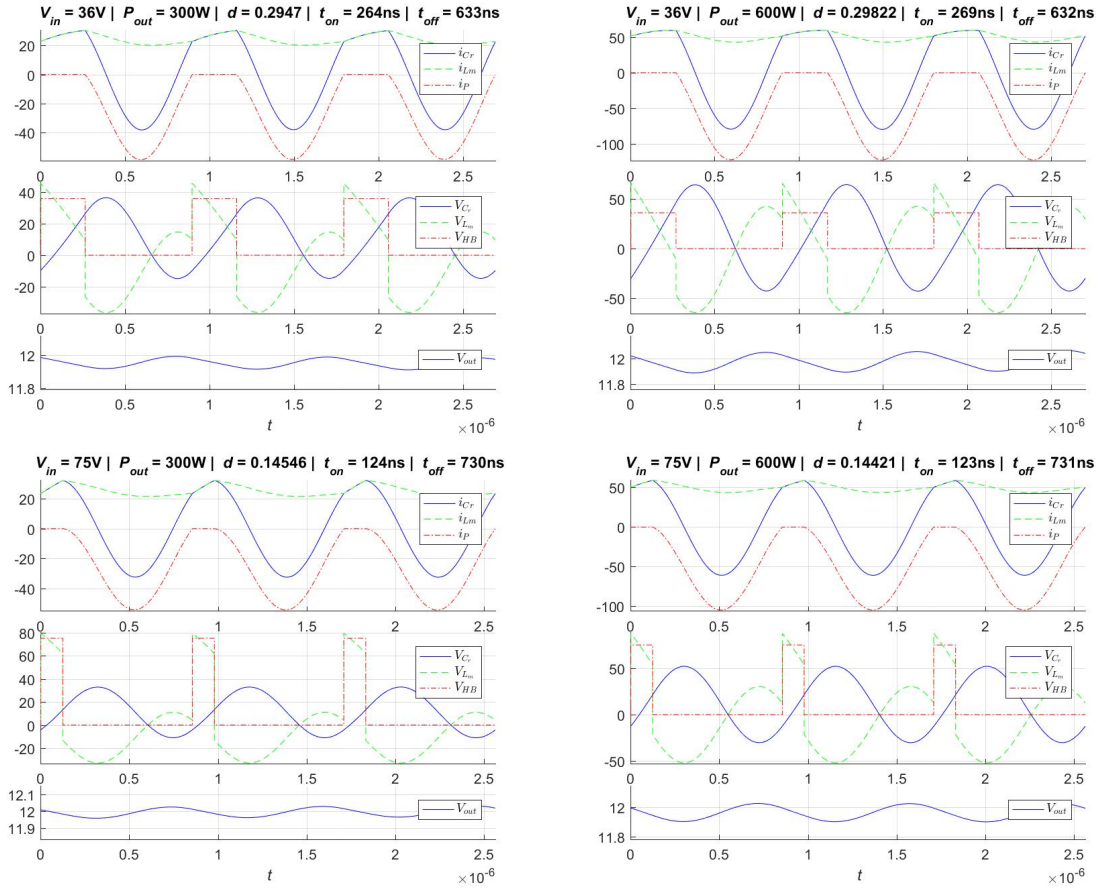

Figure 8.8: Simulation result of fifth design

8.3 Sixth Design

The construction steps are identical to the previous ones, but now a different winding ratio of 2:1 is assumed.

8.3.1 Turns Ratio: 2/1

Since the first choice for the turns ratio (6.1.1) did not work, this option is selected.

- $\frac{N_P}{N_S} = \frac{2}{1}$ (selected for further design)

8.3.2 CORE, PCB and Stray Inductance

The same magnetic core (**ER 32/6/25**) as well as the same dimensions of the multilayer PCB are used.

Primary side	$N_{P,target} = 2$	(2 Layers in series) x 2 in parallel	$R_{DC} = 0.82m\Omega$
Secondary side	$N_{S,target} = 1$	5 Layers in parallel	$R_{DC} = 0.16m\Omega$

Table 8.3: Planar transformer setup

Table 6.4 lists the structure of the planar transformer given a winding ratio of 2:1.

Layer Nr.	Side	Turns	R_{DC} mΩ	$dMMF$ A	MMF A
1	S	1	0.819	-0.4	-0.4
2	P	1	0.819	0.5	0.1
3	S	1	0.819	-0.4	-0.3
4	P	1	0.819	0.5	0.2
5	S	1	0.819	-0.4	-0.2
6	P	1	0.819	0.5	0.3
7	S	1	0.819	-0.4	-0.1
8	P	1	0.819	0.5	0.4
9	S	1	0.819	-0.4	0

Table 8.4: Planar transformer layer structure

8.3.3 Magnetizing Inductance L_m vs Resonance Capacitance C_r

The approach taken here is to calculate all possible C_r-L_m combinations based on the selected switching frequency f_{PWM} at the different input voltages V_{in} and already known part values.
It is evident from figure 8.9 that there are very small overlapping areas. This means that if a C_r-L_m selection is made, the switching frequency will vary more than before at different input voltages.
The choice of magnetization inductance is 1 µH. If no ZCV behavior is apparent, a smaller choice should be used.
The value for the resonant capacitor C_r is chosen in such a way that its position is as central as possible between the curves shown in 8.9 resulting in 60 nF.

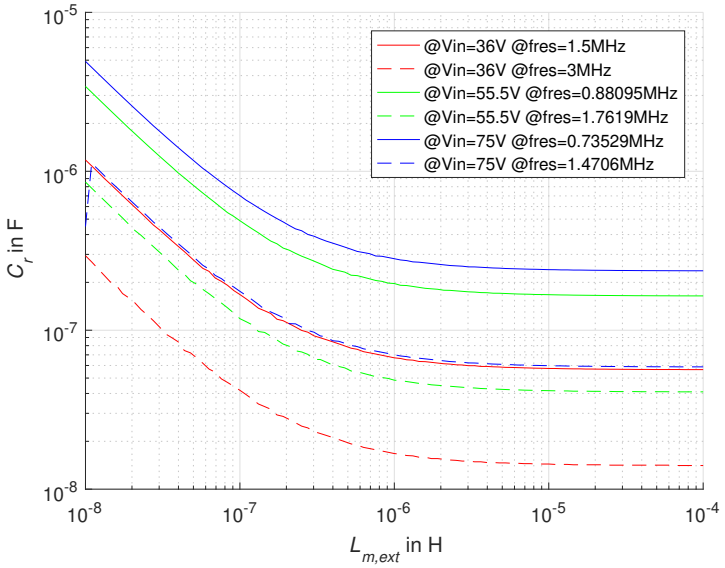

Figure 8.9: C_r vs L_m

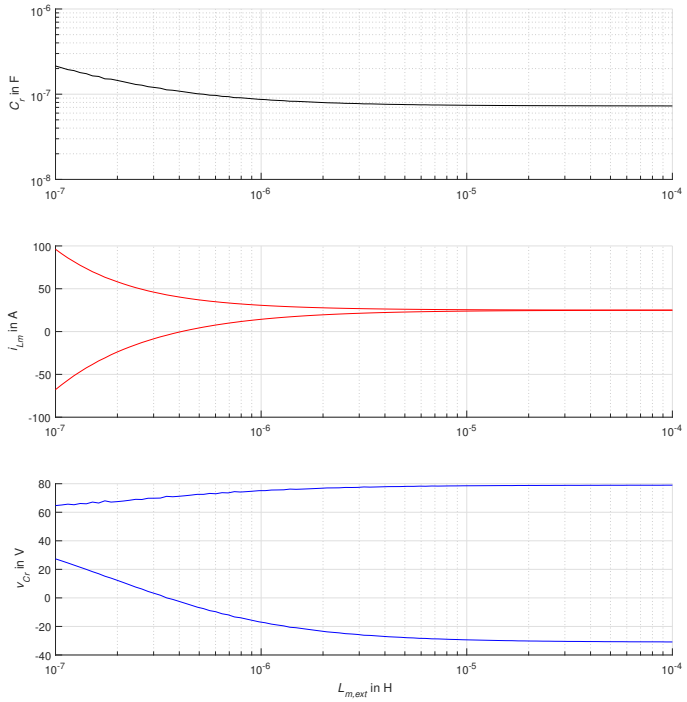

Figure 8.10: C_r vs L_m and assumed i_{Lm} and v_{Cr} at on mode, V_{in}=75V, P_{out}=600W. (worst case)

8.3.4 State Space Simulation

Figure 8.11 shows the current circuit with the selected component values.

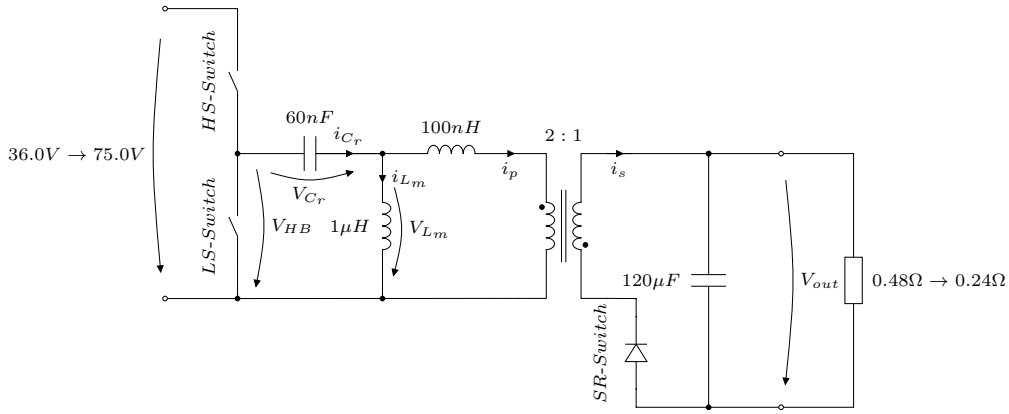

Figure 8.11: Circuit of sixth design iteration

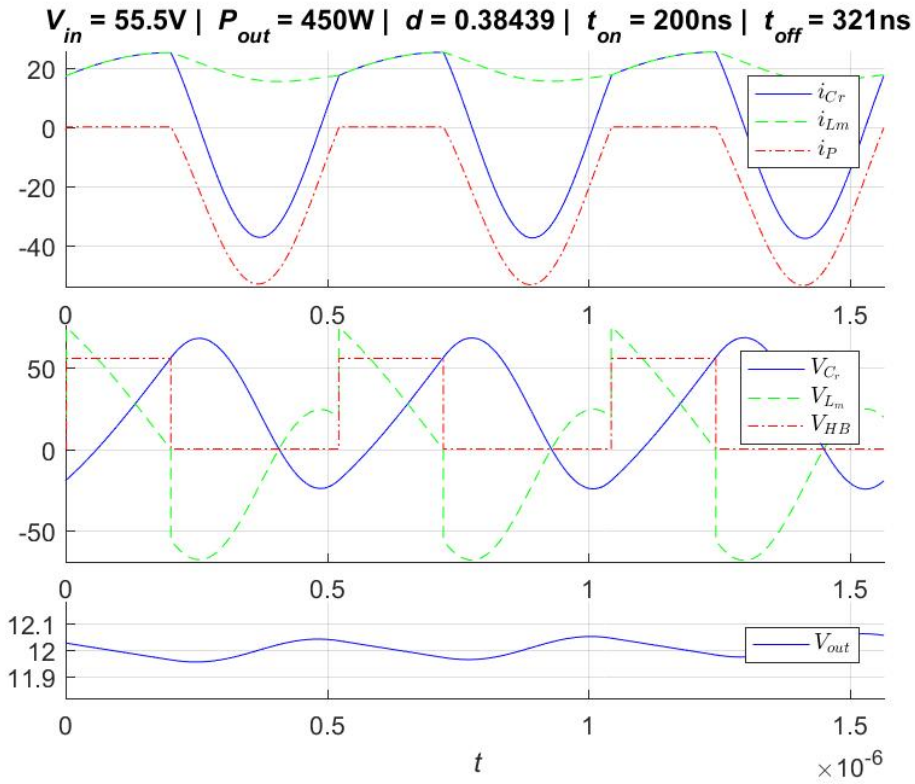

Figure 8.12: Simulation result of sixth design @V_{in} = 55.5V and P_{out} = 450W

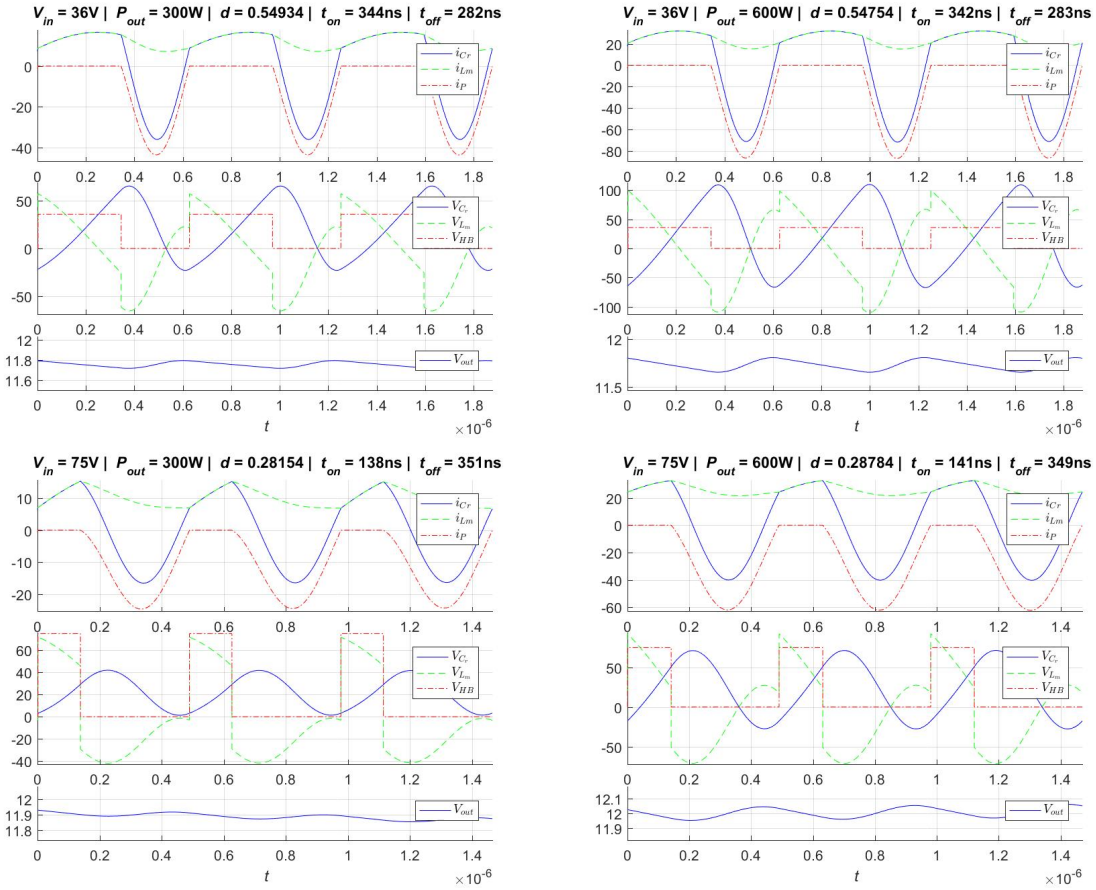

Figure 8.13: Simulation result of sixth design

V_{in}	P_{out}	controlability of V_{out}	ZVS@LS2HS
36 V	300 W	✓	
36 V	600 W	✓	
75 V	300 W	✓	
75 V	600 W	✓	
55.5 V	450 W	✓	

Table 8.5: Summary: C_r=60 nF, L_m=1 µH, L_σ=100 nH, C_{out}=120 µF, $\frac{N_P}{N_S} = 2$

Figure 8.12 is the state space simulation at nominal input voltage and nominal output power.

Figure 8.13 shows the four simulation results for the four special operations points.

As can be seen from table 8.5, the output voltages can be successfully regulated to 12 V, but even in this situation the desired ZVS behavior is missing.

8.4 Seventh Design

The seventh design is an iteration of the sixth design, trying a different C_r-L_m combination.

It is proposed to introduce a larger current change in the inductor, to achieve a ZVS. To accomplish this, the inductance L_m must be reduced, so 0.3 µH is chosen for it and for the resonant capacitance C_r a value of 100 nF is suggested.

8.4.1 State Space Simulation

Figure 8.14 shows the current design and 8.15 and 8.16 are the simulation results.

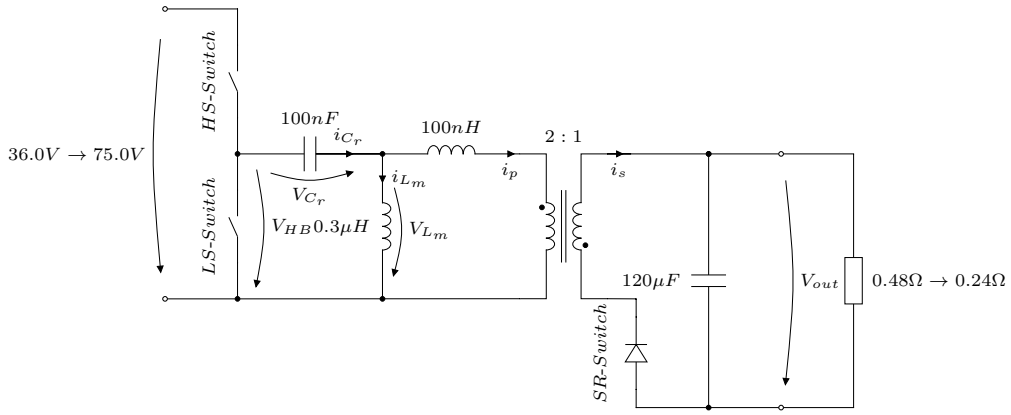

Figure 8.14: Circuit of seventh design iteration

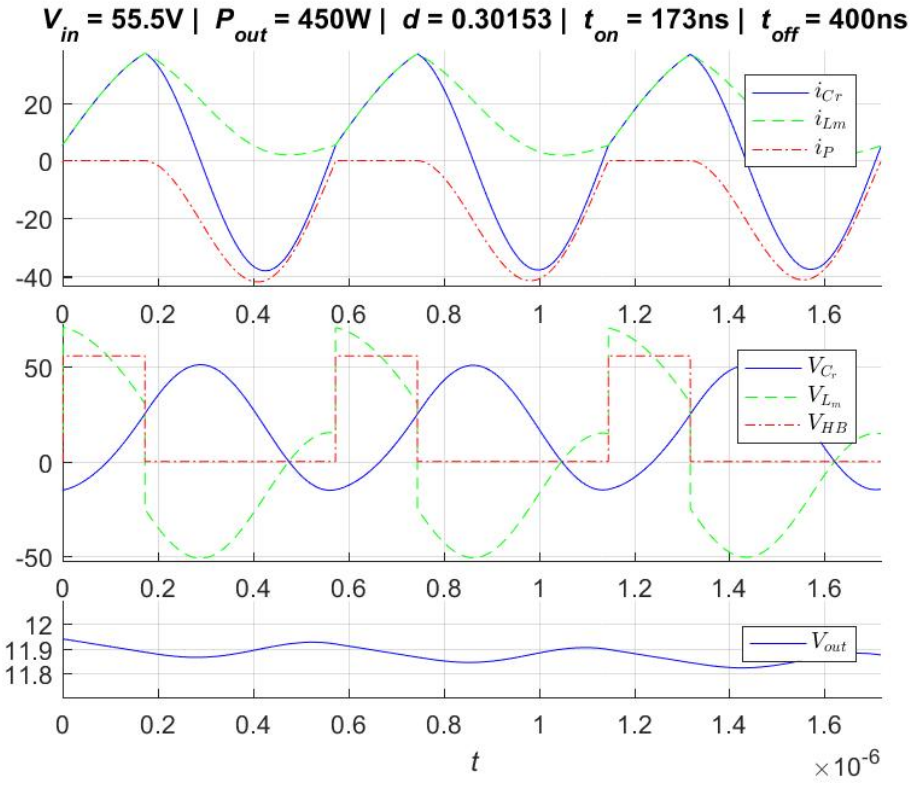

Figure 8.15: Simulation result of seventh design @V_{in} = 55.5V and P_{out} = 450W

V_{in}	P_{out}	controlability of V_{out}	ZVS@LS2HS
36 V	300 W	✓	(close)
36 V	600 W	✓	
75 V	300 W		(close)
75 V	600 W		
55.5 V	450 W	✓	

Table 8.6: Summary: C_r=100 nF, L_m=0.3 µH, L_σ=100 nH, C_{out}=120 µF, $\frac{N_P}{N_S} = 2$

Table 8.6 provides the summary of this analysis. It can be seen that the controllability of the output voltage has deteriorated whereas the ZVS operation is coming closer to the desired behavior.

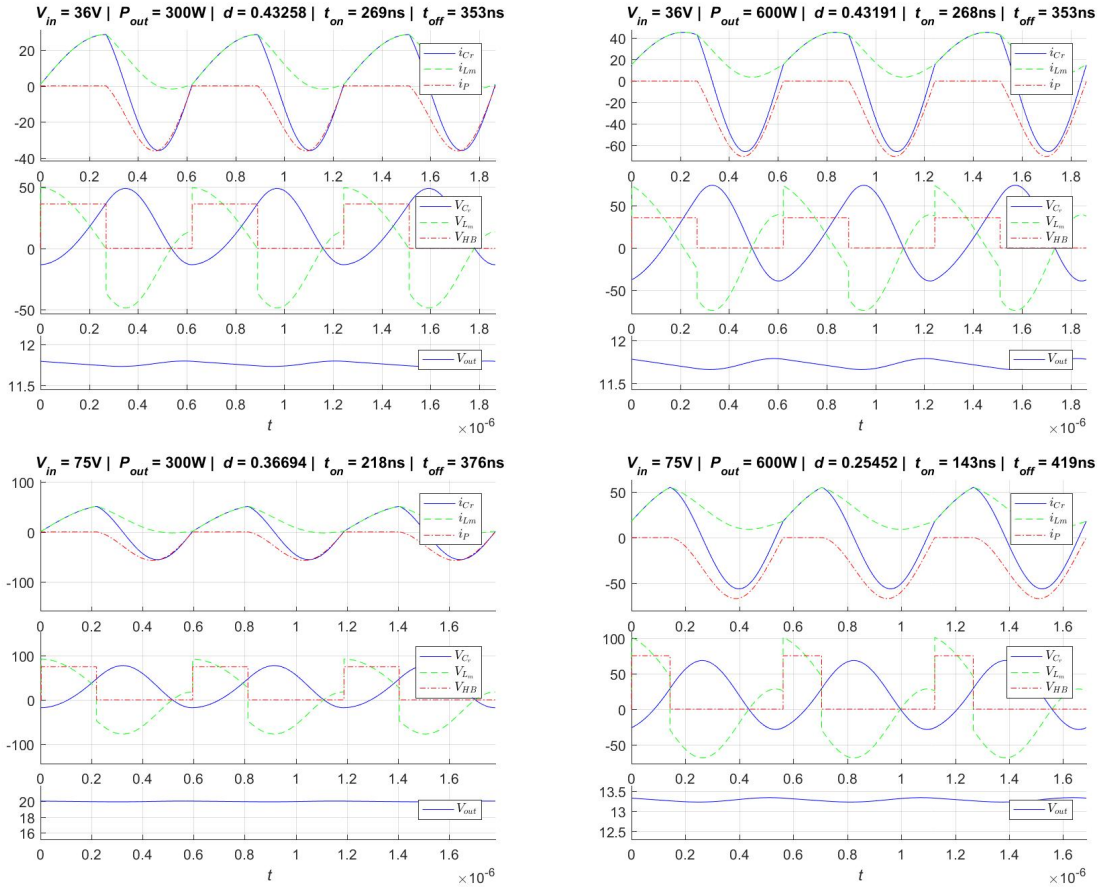

Figure 8.16: Simulation result of seventh design

8.5 Eighth Design

In order to regain the controllability of the output voltage, it might be useful to reduce the capacitance value of C_r. This setup is identical to the previous one, except that for the resonant capacitance C_r, 50 nF has been selected.

8.5.1 State Space Simulation

Figure 8.17 shows the current design while 8.18 and 8.19 are the simulation results.

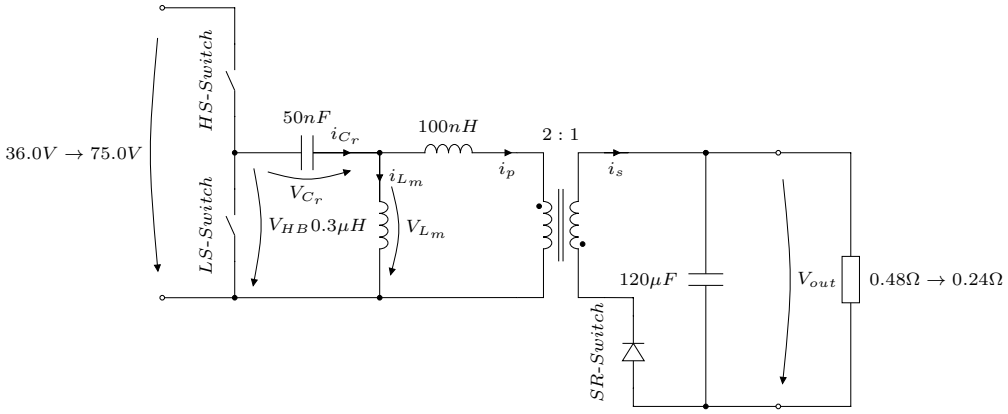

Figure 8.17: Circuit of eighth design iteration

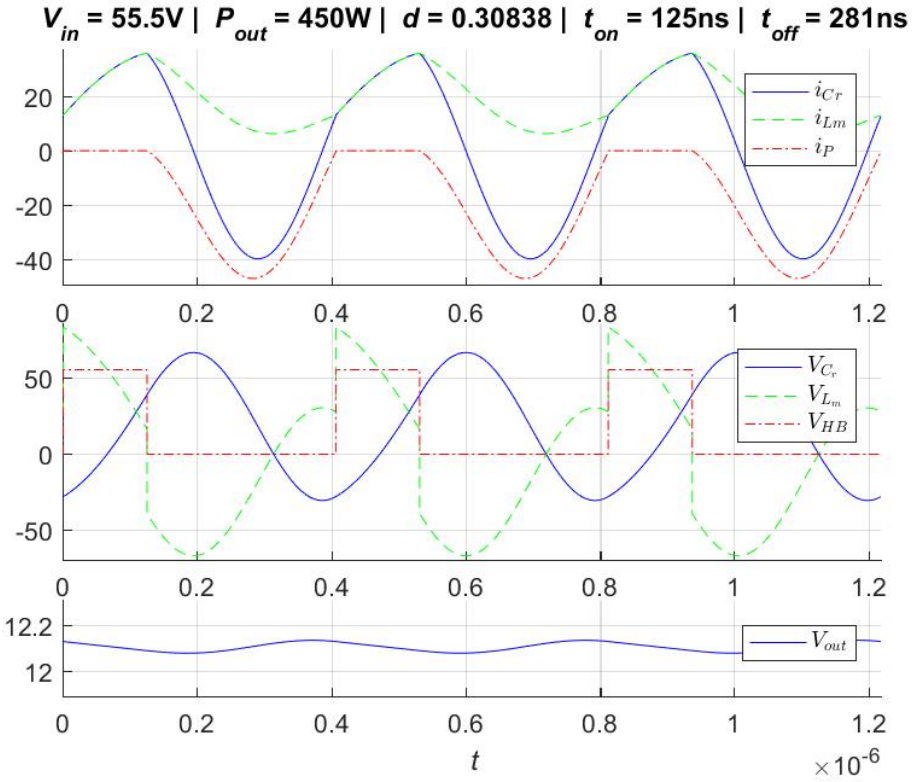

Figure 8.18: Simulation result of eighth design @V_{in} = 55.5V and P_{out} = 450W

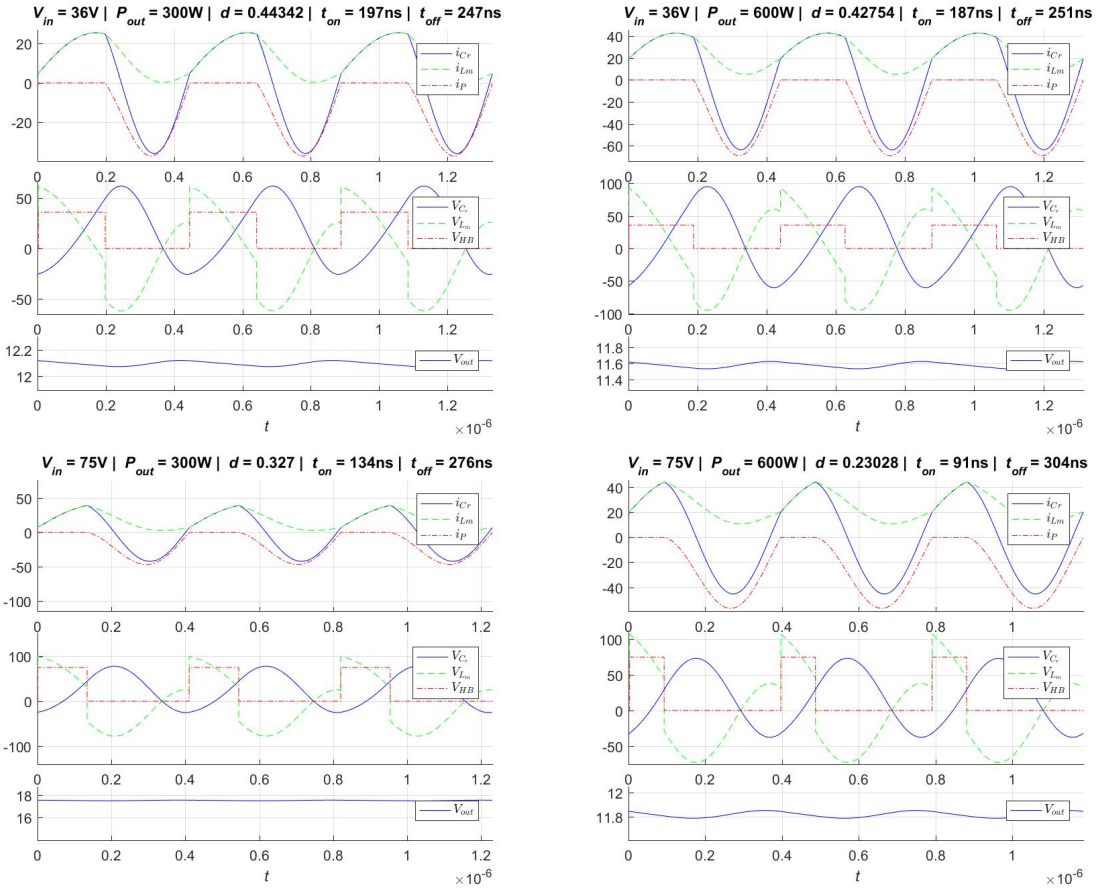

Figure 8.19: Simulation result of eighth design

V_{in}	P_{out}	controlability of V_{out}	ZVS@LS2HS
36 V	300 W	✓	
36 V	600 W	✓	
75 V	300 W		
75 V	600 W	✓	
55.5 V	450 W	✓	

Table 8.7: Summary: C_r=50 nF, L_m=0.3 µH, L_σ=100 nH, C_{out}=120 µF, $\frac{N_P}{N_S} = 2$

The table 8.7 summarizes the result of the eighth design.

The controllability of the output voltage has again not been achieved in all operating points, nevertheless the range has increased.

However, the desired ZVS behavior has not been found.

8.6 Ninth Design

Considering the already prevalent problem of not being able to control the output voltage with the current design, a further reduction of the resonant capacitance definitely does not lead to the desired ZVS behavior.

Although increasing the capacitance will definitely degrade the controllability of the output voltage, the ZVS behavior could be established.

As a test, a larger value for the capacitor C_r = 270 nF was chosen .

8.6.1 State Space Simulation

Figure 8.20 shows the current design, figures 8.21 and 8.22 are the simulation results.

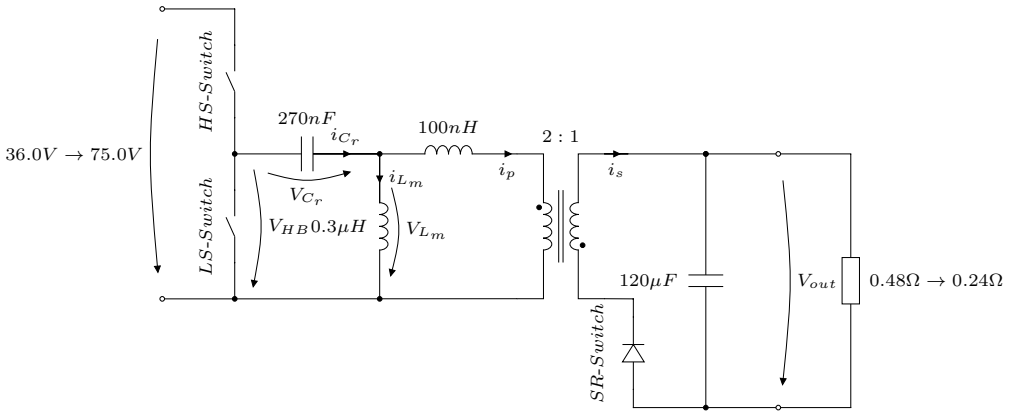

Figure 8.20: Circuit of ninth design iteration

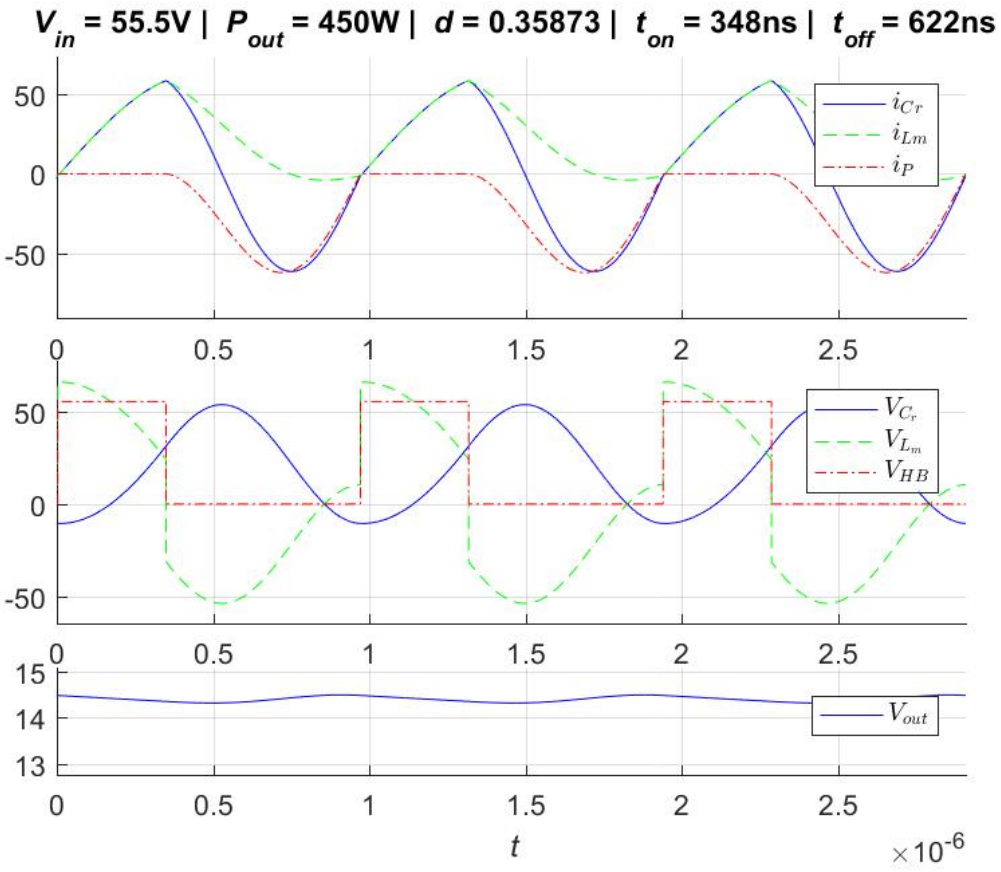

Figure 8.21: Simulation result of ninth design @V_{in} = 55.5V and P_{out} = 450W

V_{in}	P_{out}	controlability of V_{out}	ZVS@LS2HS
36 V	300 W	✓	✓
36 V	600 W	✓	
75 V	300 W		✓
75 V	600 W		
55.5 V	450 W		✓

Table 8.8: Summary: C_r=270 nF, L_m=0.3 µH, L_σ=100 nH, C_{out}=120 µF, $\frac{N_P}{N_S} = 2$

As predicted, the controllability was greatly reduced, but in return, the ZVS behavior was finally achieved. This can be seen in table 8.8.

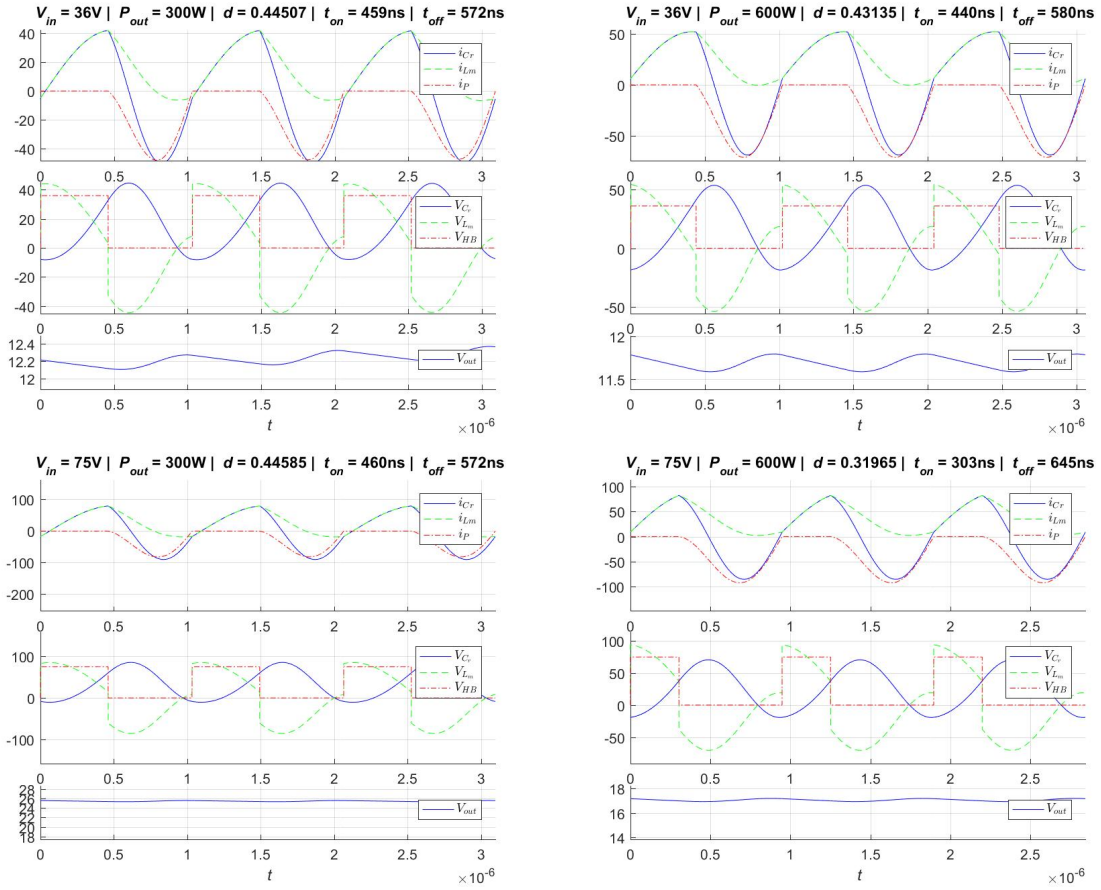

Figure 8.22: Simulation result of ninth design

The case where the required output voltage has been reached and ZVS from the low-side switch to the high-side switch would also be possible is prevalent at 36 V input voltage and 300 W output power.(Figure 8.23)

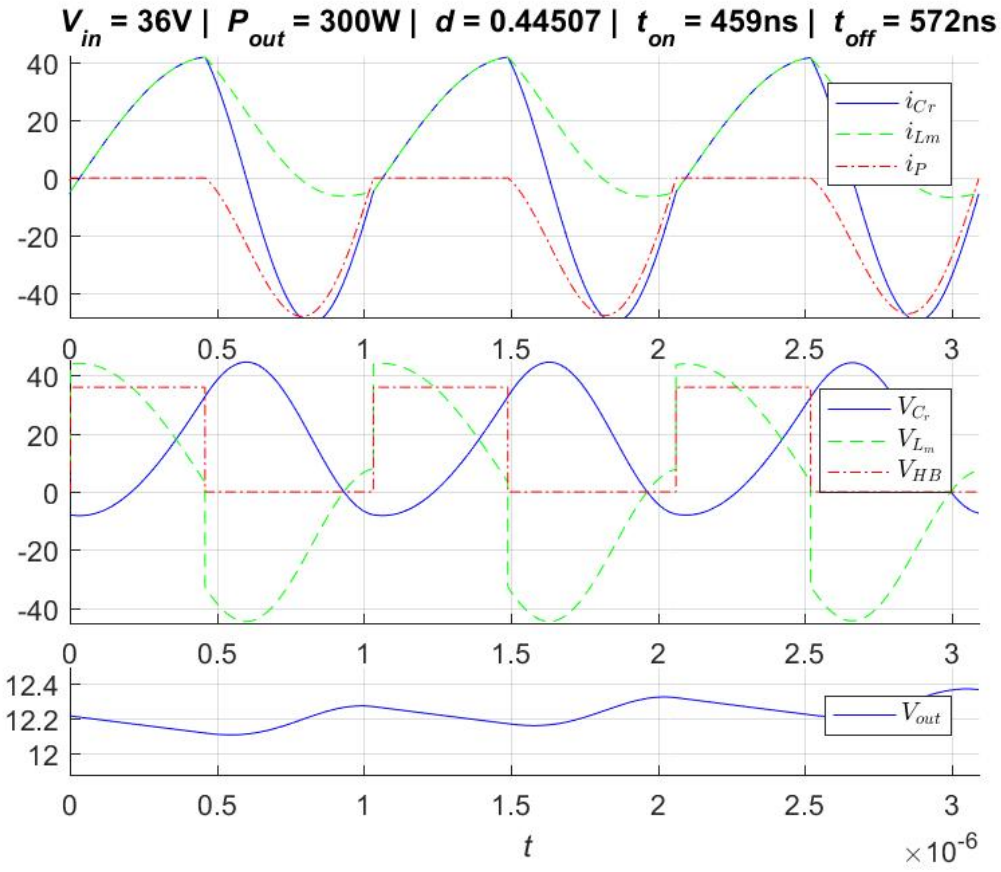

Figure 8.23: Simulation result of ninth design @V_{in} = 36.0V and P_{out} = 300W

As can be seen clearly, the course of the magnetising current i_{Lm} is favourable for the ZVS behaviour of the half bridge, which means that switching losses are greatly reduced.

However, this behaviour does not extend over the entire input voltage range or output power range.

Looking at the various simulation results in the figures of 8.22, it is evident that not only the ZVS has not always been achieved, and if so, only approximately, but also that the output voltage cannot be regulated everywhere.

It seems that in this design the ZVS behaviour of the half bridge is lost at higher output power, whereas the controllability of the output voltage is lost at higher input voltages.

There have been several other design attempts in the course of this study, all with the same result, namely that the ZVS behaviour is only reached for a limited output power range.
However, if the desired ZVS is achieved in a design, it is to be expected that the output voltage cannot be regulated correctly at higher input voltages.
In other words, this topology is not suitable for the key requirements imposed and the constraints that apply to this design attempt.

Chapter 9

SPICE Model

A simulation model has also been created in spice software.
It was primarily intended to be employed to supplement the loss calculation of this circuit. However, due to the difficulties associated with this topology and not obtaining adequate results, this model was not used.
The SPICE software applied in this work is the program called **Micro-Cap 12**.
Figure 9.1 shows the circuit, whose components values were taken from the ninth design.
The controller built into the simulation to obtain the desired output voltage is shown in figure 9.2.

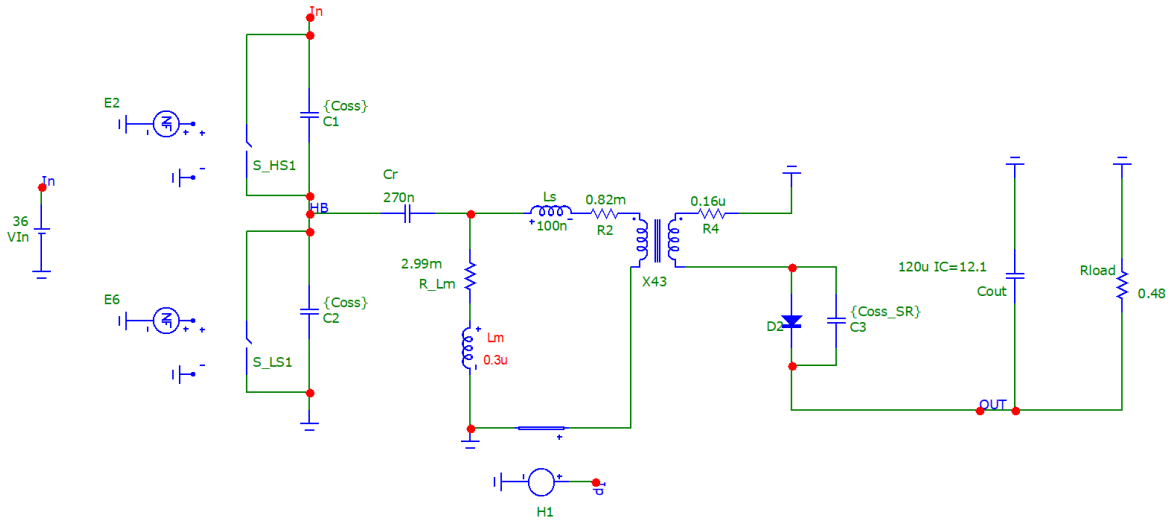

Figure 9.1: Circuit in Micro-Cap 12 of the ninth design

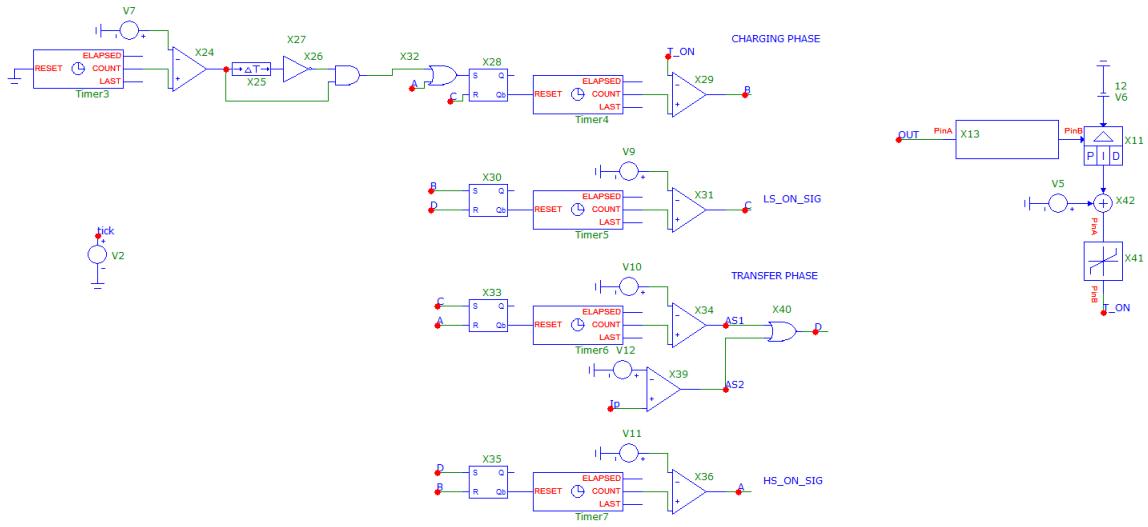

Figure 9.2: Controller of the circuit

Figure 9.2 shows the circuitry required for this simulation to generate the control signals for the semiconductor switches.
The t_{on} time duration is adjusted by a PI controller.
The sequence logic allows the setting of dead times and switches automatically to the charging mode at a zero crossing of the primary current. Therefore no t_{off} duration has to be set.

Chapter 10

Conclusion

In order to build the most compact, power-dense converter possible, the switching frequency is increased. This leads to smaller component dimensions but also to greater switching losses, which rise linearly to its frequency. To avoid these switching losses completely or at least partially, a soft-switching topology is desired to mitigate these losses.

In the process of developing the converter, programs were written in Python and in Matlab.
The simulation of the converter was done in Matlab. The component values of the converter are given and the Matlab script attempts to meet the desired output voltage by readjusting the t_{on} time. The t_{off} time is a consequence of the resonant oscillation.
As soon as a steady state is reached or a maximum simulation time is exceeded, the script stops and stores the information of the last few periods of the converter.
This data is then taken over by the next program written in Python, which is able to calculate the losses of the magnetic components of the converter. This script is provided with the dimensions of the core, material and its properties, as well as information about what kind of multilayer boards are available.
From this information, the script then creates a layer structure that is optimal in terms of minimal losses.

The result of simulating this circuit in SPICE (Simetrix, LTSpice, MicroCap), is that the converter continues to function if it is not controlled exactly, but then situations arise in which energy is not transferred and thus the reactive power in the converter is increased.

A successive readjustment is possible, but requires an extra winding in the transformer to measure the transferred current, triggering the end of the second mode at the moment the current drops to zero amperes. This is feasible, but again increases the control effort.
Should this topology ever be used, the question arises as to how it can be controlled in a practicable way.

Another component of the written program was the evaluation based on the losses. The final feedback by means of an optimiser was cancelled in the end, as there was no interest in it on the part of the company.

Based on the assumptions mentioned in this work, a simplified model of a quasi-resonant transducer with the goal of the highest possible power density was created.
With the help of the relationships found and simulations carried out, an approximate loss calculation and thus an estimate of the efficiency at various operating points has become possible. For this, see the figure 7.2.

In conclusion, the following can be said: This topology has the potential of promoting ZVS behaviour of the half bridge under certain circumstances. This is only achieved to a limited extent, taking into account the desired input voltage range and output power range.

A design could be found in which the ZVS behavior is recognizable, but mostly at the expense of a higher reactive power.

Added to the above requirements is the requirement for minimum reactive power, and it becomes even more difficult to find a design that works.
According to the existing state of knowledge, the required specifications cannot be met with this topology.

Another way of achieving this would be to reduce the switching frequency, but this would entail an increase in the component values and ultimately the power density would suffer.

In an application where the input voltage range is relatively narrow, a design could definitely be found in which the ZVS behavior is apparent.

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Appendix A

Loss Report

What follows is an excerpt from the report of the python program to calculate the losses.

```
********************************************************************************
o-read: RESULT_2_STEADY_STATE_Ls_5e-09_Lm_7p5e-08_Cr_6e-06_Cout_0p00012_Rload_0p32_a_1_Vin_55p5_Vouttarget_12.mat
|
+-----> Loading: result files from Steady State Simulation
|
+-----> Cr = 6uF
+-----> Ls = 0.005uH
+-----> Lm = 0.075uH
+-----> Co = 120uF
|
+-----> Np/Ns = 1/1
|
+-----> Pout = 450.00W
|
+-----> Vout = 12.0258V (simulation result from B_TurnRatioFinder_SteadyStateFinder.m)

------------------------------------------- I^2 x R - Losses -------------------------------------------

 I2R_HB : 90.2914A^2 x R_DS_on
 I2R_SR : 69.2207A^2 x R_DS_on
 I2R_CR : 90.2914A^2 x ESR_Cr
 I2R_Co : 57.5096A^2 x ESR_Cout

------------------------------------------- Calculation of LM -------------------------------------------

                    target Lm: 0.075ÃH
                         Core: ER 18   / 3.2 / 10
                           Ve: 667mm^3
                           le: 22.1mm
                           Ae: 30.2mm^2
                            h: 3.2mm
                           ri: 3.1mm
                           ro: 7.8mm
                    Material : 3F36 --> AL : 1.7e-06 nH/turns^2
                    Material : 3F46 --> AL : 1.1e-06 nH/turns^2

          Calculated N count : 2   (2.19705)
                          AL : 18.75nH/N^2
Layer Structure.....................
 Layer Count                M : 10
 Total Windings             N : 2

                 R_DC_TOTAL : 5.89133mOhm

                    Pcu_sum : 1.80196W
                    Pv(mag.): 2.45987
```

```
------------------------------------------- Calculation of T -------------------------------------------

TRANSFORMER SETUP

TARGET:        Np ..................................... 1
               Ns ..................................... 1

CORE GEOMETRY: inner radius of window ................. 7.2 mm
               outer radius of window ................. 13.6 mm
               height of winding window ............... 5.8 mm
               height of PCB Layer .................... 0.4 mm
               height of CONDUCTOR .................... 0.21 mm
               width of CONDUCTOR clearance on PCB ... 0.01 mm
               conductivity ........................... 1.68e-08 Ohm m
               Ã_0 bzw. permeability0 ................. 1.25664e-06 H/m

               width of window ........................ 6.4 mm
               Area_of_window ......................... 0.03712 mm
               median radius of circumference ........ 10.4 mm
               median circumference ................... 65.3451 mm
               height of PCB and CONDUCTOR ........... 0.61 mm
               QUANTITY of LAYERS ..................... 9

=========================> COPPER LOSSES <==========================
               Primary ................................ 5Parallel
               Secondary .............................. 4Parallel

               RDC_p .................................. 0.16mOhm  (0.79W DC)
               RDC_s .................................. 0.20mOhm  (0.98W DC)

               maxMMF ................................. 0.200000A

Layer Side  Turns RDC [mOhm]  dMMF [A]  MMF[A] porosityF eq.Conductivity Pcu_ac
1     P     1     0.819       0.2       0.2     1         5.95e+07        0.265W
2     S     1     0.819       -0.25     -0.05   1         5.95e+07        0.414W
3     P     1     0.819       0.2       0.15    1         5.95e+07        0.265W
4     S     1     0.819       -0.25     -0.1    1         5.95e+07        0.414W
5     P     1     0.819       0.2       0.1     1         5.95e+07        0.265W
6     S     1     0.819       -0.25     -0.15   1         5.95e+07        0.414W
7     P     1     0.819       0.2       0.05    1         5.95e+07        0.265W
8     S     1     0.819       -0.25     -0.2    1         5.95e+07        0.414W
9     P     1     0.819       0.2       0       1         5.95e+07        0.265W

 Total Primary Losses ................................ 1.325945W
 Total Secondary Losses .............................. 1.657432W

0:  951474.785918Hz ... 0.549637W
1:  1902949.571836Hz ... 2.367816W
2:  2854424.357755Hz ... 0.057830W
3:  3805899.143673Hz ... 0.003858W
4:  4757373.929591Hz ... 0.001928W
and more ...

=========================> MAGNETIC LOSSES <==========================
  Material: 3F3  Bmax / Bmin = 0.071mT / -0.001mT
  f_switching = 954198.473283Hz
  f_sin,eq    = 1180871.854481Hz
  P_core      = 0.542235W/cm^3

  Magnetic Losses ..................................... 2.928067W

============================> TOTAL LOSSES <============================
  Pout ................................................ 450.000000W
  Pv,total ............................................ 5.911444W   (1.314%)

=========================> Magentic Characteristic <=========================
  target Np ............... 1
  target Ns ............... 1

  magnetic Area ........... 141.000000mm^2
  magnetic length ......... 38.200000m
```

```
  Lp ..................... 9.28ÃF
  Ls ..................... 9.28ÃF
  Lm ..................... 9.28uF

  Method 1 (calculated coupling factor k1 = 0.996086 , 99.6086%, 0.3914%)
  stray Llk ............... 36.31nF


  Method 2 (calculated coupling factor k2 = 0.999634, 99.9634%, 0.0366%)
  stray Llk ............... 3.39nF
  M interleaving factor ... 4.00

  Method 3 (calculated coupling factor k3 = 0.999895, 99.9895%, 0.0105%)
  stray L ................. 0.97nF

*******************************************************************************
```