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An Ultra-Low Power Resistance/Capacitance Sensing Circuit for RFID Transponder ICs in a 40nm CMOS Technology

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Kurzfassung

Radiofrequenz-Identifikations-Technologie (RFID) ermöglicht die Kommunikation mit RFID-Transpondern (Tags). Die RFID-Tags werden z.B. auf Verpackungen als Manipulationsschutz verwendet. Um festzustellen ob eine Verpackung geöffnet wurde, wird der Wert eines externen Widerstands bzw. Kondensators mit einer Tag Tamper Schaltung gemessen. Die passiven Tags werden mit der Energie aus dem Elektromagnetischen Feld des RFID-Lesers versorgt, deshalb ist der Leistungsverbrauch limitiert auf bis zu wenige µW. Der Stromverbrauch der Tag Tamper Schaltung ist begrenzt mit 3 µA.

Diese Arbeit untersucht verschiedene Messmethoden für einen Tag Tamper Block. Die Messmethoden werden bezüglich Fläche, Stromverbrauch, Messzeit, Messbereich, Genauigkeit und Temperaturverhalten miteinander verglichen. Der Tag Tamper soll eine Kapazität zwischen 2 pF und 5 pF messen mit einer Genauigkeit von 250 fF. Weiters, soll die Genauigkeit die Prozess-und Mismatch-Variationen aushalten und die Messzeit soll nicht größer als 220 µs sein.

Zwei Messmethoden werden in einer 40nm Technologie umgesetzt. Außerdem wird für eine Messmethode, Iterative Delay Chain Discharge, das Layout, mit einer Fläche von 9681 µm^2, umgesetzt und die Netzliste mit parasitären Kapazitäten wird extrahiert und simuliert. Die Simulationsergebnisse werden bezüglich der definierten Spezifikationen verglichen.

Schlagwörter: ultra-low Power, Tag Tamper, Kapazitätsmessung, Widerstandsmessung, CMOS integrierte Schaltungen

Abstract

Radio-frequency identification (RFID) technology enables the communication with RFID transponders (tags). The RFID tags can be used on packages as a tamper protection. Tag tamper measures an external resistance or capacitance in order to determine if a package was opened. The passive tags use the energy of the electromagnetic field generated by the RFID reader. Therefore, the power consumption is limited to a few µW. The current consumption of the tag tamper block is limited to 3 µA.

In this thesis, several different sensing methods for a tag tamper block are discussed. The methods are compared with respect to area, current consumption, measurement time, measurement range, accuracy and temperature behaviour. The tag tamper should be able to measure a capacitance between 2 pF and 5 pF with an accuracy of 250 fF. The accuracy has to withstand process and mismatch variations and the measurement time should not exceed 220 µs.

Two sensing methods are implemented in a 40nm CMOS technology. Furthermore, the layout of the iterative delay chain discharge, with an area of 9681 μm^2, is implemented and the netlist with parasitic capacitances extracted and simulated. The simulation results of the two methods are compared with respect to the requirements.

Keywords: ultra-low power, tag tamper, capacitance sensing, resistance sensing, CMOS integrated circuits

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Ricardo Oliveira for doing the initial layout of the block and Jingnan Xu for his support on layout changes.

Glossary

ASK Amplitude-Shift Keying
CBCM Charge Based Capacitance Measurement
CCO Capacitive Controlled Oscillator
CDC Capacitance-to-Digital Converter
CLK Clock
CNT Counter
CTT Capacitive Tag Tamper
DP Detection Pin
DUT Device Under Test
ESD ElectroStatic Discharge
GO1 Transistor with thin gate oxide
GO2 Transistor with thick gate oxide
GPIO General Purpose Input Output
IC Integrated Circuit
NFC Near-Field Communication
PWM Pulse-Width Modulation
RFID Radio-Frequency IDentification
RTT Resistive Tag Tamper
SC Switched Capacitor
TDC Time-to-Digital Converter

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Chapter 1

Introduction

1.1 Motivation

Manufacturers want to protect their products against tampering. One way to assure the authenticity of a product is to integrate RFID tags into the products. RFID tags give the whole supply chain and the end customer the possibility to check the authenticity of a product by simply reading the labels with an RFID reader. This solution is sufficient for products where the tag can be integrated in the product (e.g. clothing, electronic products). However, some products require additional protection.

Imagine you have a high quality product like a bottle of wine or a perfume. In order to protect that product against manipulation, it is not enough to put a tag on the package or on the bottle. There is always the risk of someone reusing that bottle by refilling it with a low-quality product and selling it again. This fraud can have a significant impact on your business.

Therefore, a more secure solution is needed. With tag tamper it can be detected if a packaging was opened. This tag has an external resistor or capacitor which value depends on the condition of the packaging. By reading the tag, the resistance and capacitance are measured. According to these values, it can be determined if the package was opened or not. Tag tamper can be used as protection against refill and manipulation of medication, bottles (wine, perfume etc.), cosmetics, logistics packaging and many more.

1.2 Scope

Tag tamper circuits are resistance and capacitance sensing circuits that are used in RFID transponders for additional security against tampering. This thesis considers several different sensing circuits to be implemented in 40nm CMOS technology. The supply voltage is 1.1 V and the sensing circuits should meet the required accuracy over a temperature range from $-40\,^{\circ}\mathrm{C}$ to $125\,^{\circ}\mathrm{C}$.

The operating principles of all the considered sensing circuits are described. Their advan-

tages and disadvantages regarding measurement time, accuracy, current consumption, area and temperature behaviour are discussed.

Two capacitive sensing circuits (CTTs), the iterative delay chain discharge and the linear slope charging were chosen to be designed in 40nm CMOS technology. The iterative delay chain discharge was published in [9]. The linear slope charging is based on an existing circuit which is part of a tag tamper block designed by Rainer Stadlmair in 140nm CMOS technology. The implemented measurement methods are explained by describing each block of the implemented CTTs.

The implemented CTTs are investigated regarding accuracy, current consumption, temperature dependence and influence of disturbance. The iterative delay chain discharge has also been implemented in layout by Ricardo Oliveira and is verified by simulating the netlist with parasitic capacitances extracted from layout.

The specifications for the tag tamper block are listed in Table 1.1.

Specifications	Unit	Min.	Nom.	Max.
f_{clk}	MHz	-	1.695	-
C_{range}	pF	2.0	-	5.0
$C_{accuracy}$	pF	-	0.25	-
C_{range_dbl}	pF	4.0	-	10.0
Measurement time	µs	-	-	220
Temperature	°C	-40	27	125
Current consumption	µA	-	-	3
Area	μm^2	-	-	34000

Table 1.1: Specifications.

1.3 Outline

Chapter 2 introduces radio-frequency identification and NFC systems. The operating principles are explained, as well as their applications. Furthermore, tag tamper block is introduced. Examples of possible implementations and applications are described. Finally, the disturbances that can occur at the tag tamper block are discussed.

Various methods for measuring capacitance or resistance were considered for this thesis. Chapter 3 gives an insight into these methods. The working principle of each method is described, as well as their advantages and disadvantages.

Chapter 4 describes the implementation of the two chosen methods. Each sub-block of the designed tag tamper is described in detail and simulated separately. Furthermore, the

layout of the iterative delay chain discharge CTT is presented.

In Chapter 5, the simulation results of the two implemented CTTs, as well as the extracted layout simulation of iterative delay chain discharge CTT, are compared. The results include accuracy, current consumption, temperature behaviour, influence of disturbance, process variations and mismatch.

Chapter 2

Background

RFID (Radio-Frequency IDentification) is an identification method which uses radio-frequency to transmit data between a reader and a transponder (often referred to as a tag or a label). Both the reader and the tag consist of an IC and an antenna for communication through electromagnetic fields. Together, they form an RFID system as illustrated in Figure 2.1.

Tags can be passive, semi-passive or active regarding the power source. Active and semi-passive tags have an on-board power source. Active tags use the on-board power source for communication with a reader while the semi-passive use its power source to supply on-board electronics. Passive tags are most commonly used. They need to harvest the energy from the electromagnetic fields generated by the reader. Therefore, passive tags cannot reach reading distances that can be achieved with active tags. [11], [12], [10].

RFID systems use different frequency ranges (Table 2.1) which determine their performance and cost. Systems operating at lower frequencies have slower data rates and are generally larger, due to larger antennae, compared to the systems operating at higher frequencies. However, they show better performance near metals and liquids. [10], [12]

The reading range of a passive tag is closely related to the chosen frequency. Typical range for LF is 50 cm, 10 cm for HF, while UHF or Microwaves can reach up to 10 m. The reading range is also limited by the output power, which is usually regulated for higher frequencies, to avoid health concerns to humans and interference with other electronic circuits. [12], [13].

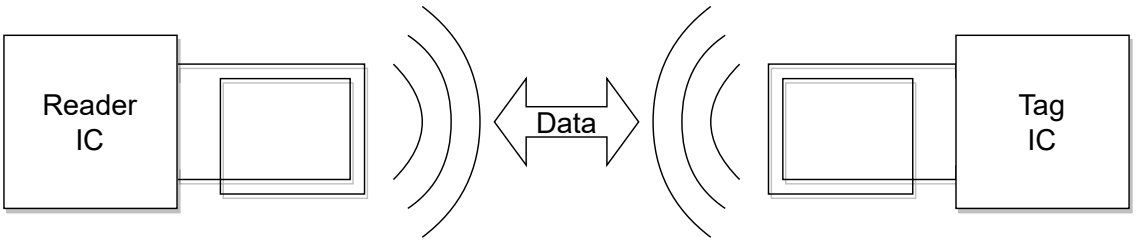

Figure 2.1: RFID System.

Frequency Band	Frequency Range	Typical Frequencies used in RFID Systems
Low Frequency (LF)	100 kHz - 500 kHz	125 kHz 134.2 kHz
High Frequency (HF)	10 MHz - 15 MHz	13.56 MHz
Ultra High Frequency (UHF)	400 MHz - 950 MHz	866 MHz Europe 915 MHz United States
Microwaves	2.4 GHz - 6.8 GHz	2.45 GHz 3.0 GHz

Table 2.1: Commonly used frequency bands for RFID systems (Modified from source: [10]).

Some of the RFID applications are illustrated in Figure 2.2. RFID system is often compared with barcode system. The barcode is also used for automatic identification, but the drawback is that the reader must be in close range and have a line of sight. Although this is acceptable in retail, RFID improves identification in warehouses. Tracking packages in transportation is made easier.
Additional to retail and logistics, use of contactless smart cards is widely spread. Many big cities in the world use smart cards in public transportation. Contactless payment in retail is part of everyday life. Smart cards are also used to check access authorisation to buildings, rooms etc. Similar to smart cards, a huge market are electronic passports which are used by many countries worldwide.
There is also an increase use of RFID systems in industry and agriculture. In industry, more processes can be automatized when identification of tools and components is made possible. Furthermore, manufacturers can put a unique ID on their products so the end customer can check the authenticity of the product.
Animal identification is commonly used for disease control and to ensure quality. RFID systems with integrated sensors are also becoming more popular. A possible use is a humidity sensor that is used to check the soil humidity. [14], [2].

2.1 Near-Field Communication (NFC)

NFC is an interface and a communication protocol built on top of RFID. It is used in a peer-to-peer or reader-tag network. A transmitter and a receiver are alternately connected to the antenna, which is usually a surface coil or a conductor loop. Data is carried by the alternating magnetic field with a frequency of 13.56 MHz. The magnetic field is modulated with ASK modulation. The distance between two NFC devices can reach up to 20 cm. NFC has two different operating modes which contribute to power saving [2], [15].

The communication starts when the first NFC interface activates its transmitter and thus works as the NFC initiator. The other NFC interface detects the magnetic field and automatically becomes the NFC target.
In active mode, both NFC interfaces generate magnetic fields. Data is always transmitted

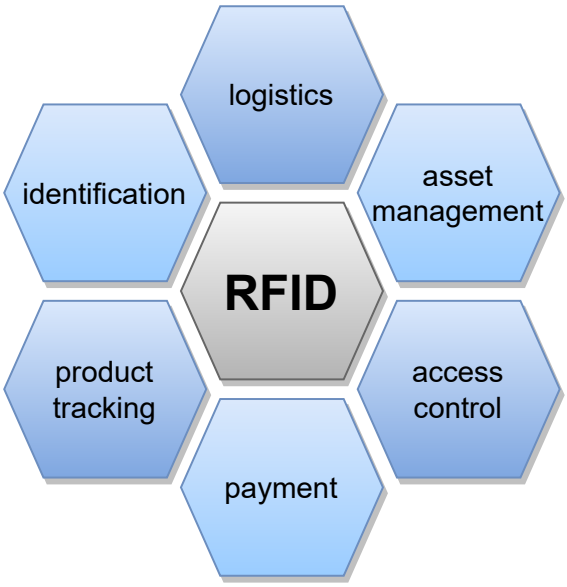

Figure 2.2: RFID applications (Modified from source: [1]).

from transmitter to receiver. When transmitting data from NFC target to NFC initiator, the target activates the transmitter and the initiator switches to receiving mode.
In passive mode, the NFC initiator does not turn off the magnetic field after transmitting to the NFC target. The target transmits data to the initiator by load modulation of the magnetic field generated by the initiator. This allows the NFC target to minimize the power consumption. The NFC interface can behave similar to an RFID reader in "reader-emulation mode" or an contactless smart card in "card-emulation mode". The different modes are illustrated in Figure 2.3. [2].

NFC is widely used in smartphones. The smartphone can act as a smart card which can be used for contactless payment, getting access for buildings or events and much more.
When used as a reader, a NFC-equipped smartphone can read NFC tags which can then open a link in your web browser or an app can use the data from the NFC tag to improve user experience.
Besides smartphones, smart watches and bracelets with NFC are also used for contactless payment or identification. Some NFC applications are illustrated in Figure 2.4.

2.2 Tag Tamper

Since RFID tags are widely used to track and identify products and logistic packages, it is also of great interest for the manufacturers and the end customers to detect if the package was damaged or already opened. An RFID tag can be equipped with a protection against tampering. This is referred to as "Tag Tamper". Tag tamper detects unauthorized opening of a package by measuring an external resistance or capacitance at the startup of the IC. The status can be updated only if the tag is active. In case of detecting an open package after the tag is powered by an RF field, the event will be permanently stored in the IC [4]. Depending on the measurand, we differentiate between Resistive Tag Tamper (RTT) and

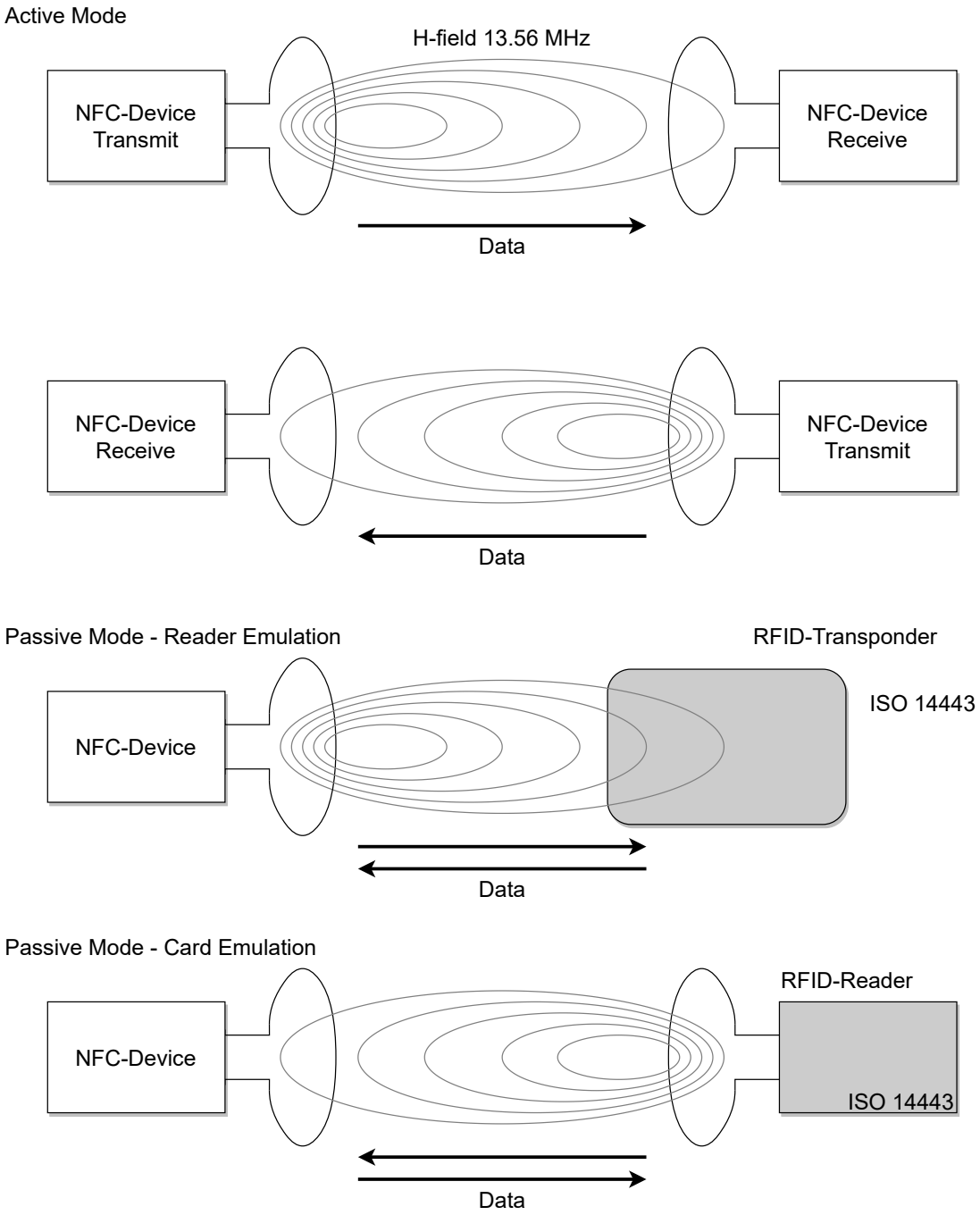

Figure 2.3: NFC modes (Modified from source: [2]).

Capacitive Tag Tamper (CTT). The resistive and capacitive tag tamper ICs are illustrated in Figure 2.5 and Figure 2.6.

RTT measures the resistance of an external wire loop connected to the IC pins. The resistance increases when the wire is damaged or broken. When the resistance crosses a

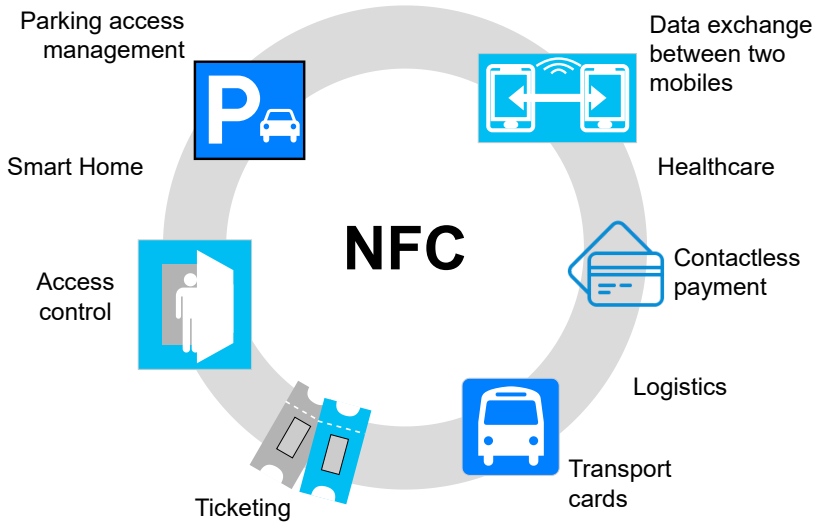

Figure 2.4: NFC applications (Modified from source: [3]).

defined threshold, the package is considered open.

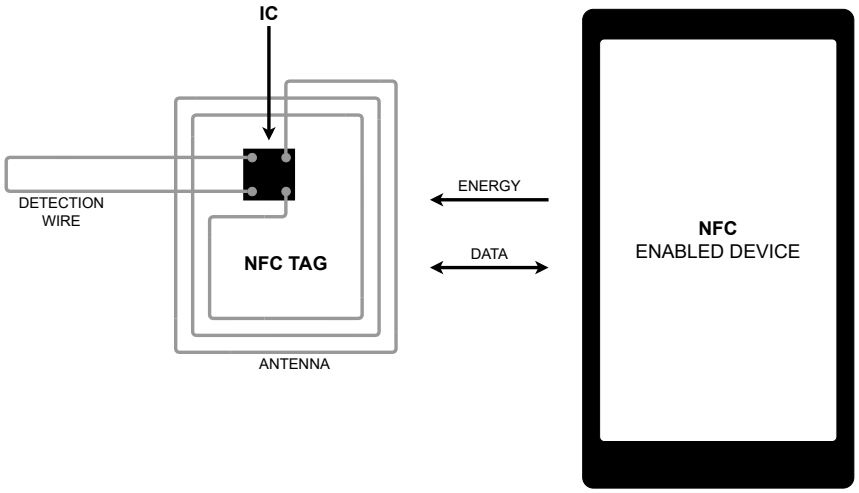

Figure 2.5: Resistive Tag Tamper (Modified from source: [4]).

CTT measures the value of an external capacitance. The capacitor to measure is usually constructed with two parallel conducting plates. Changing the overlap area or the distance between the plates, changes the capacitance value. The capacitance can also be changed by moving or changing the dielectric between the plates. When the capacitance exceeds the defined range, the package is considered open.

Generally, CTTs are more secure because it is harder to manipulate them. The broken external wire of the RTT could be reconnected while it's harder to restore the initial arrangement of the external capacitor on CTT.

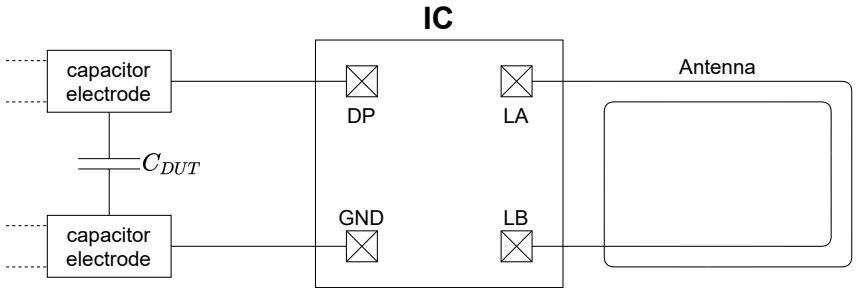

Figure 2.6: Capacitive Tag Tamper.

2.2.1 Disturbance

Disturbances can be generated by the NFC reader or by the tag loop antenna. The signals can couple into the tag tamper detection pin (DP) and cause measurements to fail or alter the results. The voltages at the NFC tag antenna are low compared to the voltages on the NFC reader. Therefore, only the disturbance induced by the reader was considered in this project.

Depending on the coupling path, on which the electromagnetic energy is transferred from the source to the receptor we can differentiate between several coupling modes [16]. The most important regarding the RFID system and tag tamper are the inductive and capacitive coupling.

Inductive coupling occurs between two or more wire loops. A noise current flowing in a closed loop circuit produces a magnetic flux, which induces a noise voltage in another closed loop placed in a small distance. To reduce this coupling effect, the wire loop area should be minimized as well as the overlap area of the NFC antenna and the RTT wire loop of the detection wire.
Because this coupling mode involves closed wire loops, it would have more impact on RTT than on CTT. Since the main focus of this thesis isn't RTT, inductive coupling was not considered while designing the tag tamper.

Capacitive coupling can occur between two wires with different potentials. The high frequent voltage couples through a stray capacitance from one conductor to another. To reduce the disturbance, caused by capacitive coupling, the source of the disturbance and the receptor should be as far as possible. Shielding also reduces the disturbance. None of these techniques are very useful since distance between the reader and the tag IC cannot be significantly increased and shielding is expensive and often not possible. A useful method would be to arrange the capacitor plates perpendicular to the tag antenna. However, for the case that the geometrical measures are not enough, a low-pass filter, described in chapter 4, is used to filter the disturbance.

The capacitive coupling from the reader to the test pin of the C_{DUT} is modelled with the circuit in Figure 2.7.

The model with the values in Table 2.2 was provided by the company and is the result of lab measurements. The parameters u and v represent the asymmetry between the coupling capacitances. A disturbance voltage $V_{disturb}$ is obtained at the capacitor C_{DUT} only if there

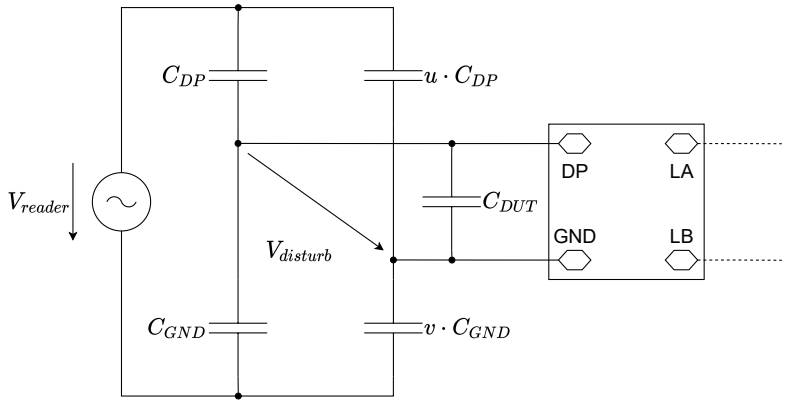

Figure 2.7: Schematic of the capacitive coupling model.

is an asymmetry $u \neq v$.

V_{reader}	C_{DP}	C_{GND}	u	v
V	fF	fF	-	-
50	100	100	0.1	1

Table 2.2: Capacitive coupling model parameters.

To calculate the voltage on the capacitor C_{DUT} first a delta to star conversion is done. The equations (2.1), (2.2) and (2.3) are used to calculate the capacitances in the star connection.

$$c_1 = \frac{C_2 \cdot C_3 + C_3 \cdot C_1 + C_1 \cdot C_2}{C_1} \tag{2.1}$$

$$c_2 = \frac{C_2 \cdot C_3 + C_3 \cdot C_1 + C_1 \cdot C_2}{C_2} \tag{2.2}$$

$$c_3 = \frac{C_2 \cdot C_3 + C_3 \cdot C_1 + C_1 \cdot C_2}{C_3} \tag{2.3}$$

If we apply the delta to star transformation to the capacitive coupling model, we get the schematic depicted in Figure 2.8 (down right). The capacitances c_a, c_b and c_c are calculated with following equations:

$$c_a = \frac{C_{GND} \cdot C_{DUT} + C_{DUT} \cdot v \cdot C_{GND} + v \cdot C_{GND} \cdot C_{GND}}{v \cdot C_{GND}}, \tag{2.4}$$

$$c_b = \frac{C_{GND} \cdot C_{DUT} + C_{DUT} \cdot v \cdot C_{GND} + v \cdot C_{GND} \cdot C_{GND}}{C_{GND}}, \tag{2.5}$$

$$c_c = \frac{C_{GND} \cdot C_{DUT} + C_{DUT} \cdot v \cdot C_{GND} + v \cdot C_{GND} \cdot C_{GND}}{C_{DUT}}. \tag{2.6}$$

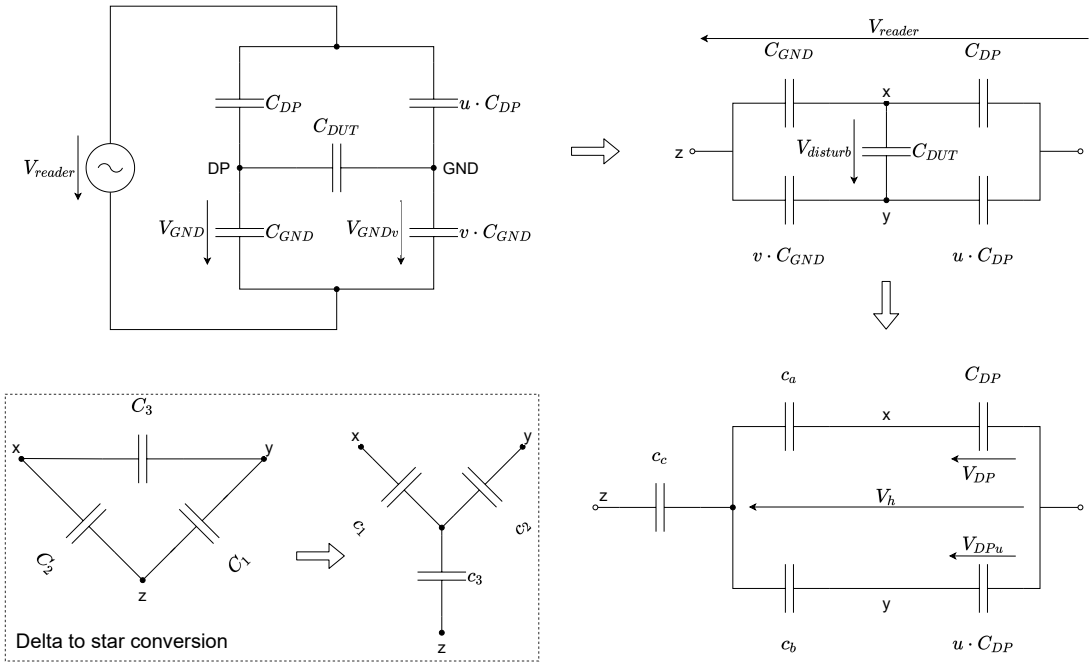

Figure 2.8: Capacitive coupling model transformation for easier calculation.

To calculate the voltage V_h, first the capacitance C_h is calculated. C_h consists of c_a, C_{DP}, c_b and $u \cdot C_{DP}$.

$$C_h = \frac{c_a \cdot C_{DP}}{c_a + C_{DP}} + \frac{c_b \cdot u \cdot C_{DP}}{c_b + u \cdot C_{DP}} \tag{2.7}$$

Now the voltage V_h can be calculated with the following equation.

$$V_h = V_{reader} \cdot \frac{c_c}{c_c + C_h} \tag{2.8}$$

The voltages over the capacitances C_{DP} and C_{DPu} can be calculated.

$$V_{DP} = V_h \cdot \frac{c_a}{c_a + C_{DP}} \tag{2.9}$$

$$V_{DPu} = V_h \cdot \frac{c_b}{c_b + u \cdot C_{DP}} \tag{2.10}$$

The disturbance voltage $V_{disturb}$ over the capacitor C_{DUT} is then calculated:

$$V_{disturb} = V_{GND} - V_{GNDv} = (V_{reader} - V_{DP}) - (V_{reader} - V_{DPu}) = V_{DPu} - V_{DP}. \tag{2.11}$$

If we insert the model parameters from Table 2.2, we can calculate the amplitude of the disturbance voltages for given capacitances C_{DUT}. The Table 2.3 holds the amplitude values of $V_{disturb}$, for the maximum and minimum C_{DUT}, defined in Table 1.1 (C_{range}). The measures to reduce the impact of the disturbance are described for each method in chapter 4.

C_{DUT}	$V_{disturb}$
pF	V
2	0.7
5	0.286

Table 2.3: Amplitude of the disturbance voltage calculated for given capacitances.

2.2.2 Applications

As already mentioned at the beginning of this section, tag tamper circuits are used to detect if a package was opened. This information can be used as a protection against unauthorized opening, or it can be used for loyalty programs. For example, by scanning the tag, the customer can get access to a web page only if the package was opened. Figure 2.9 illustrates possible RTT and CTT realizations.

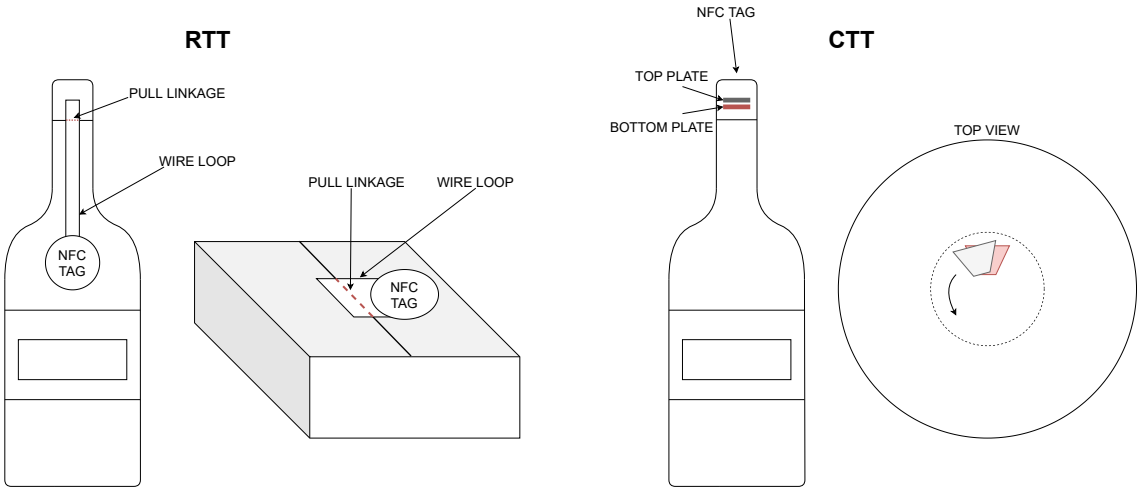

Figure 2.9: Possible realizations of resistive (left) and capacitive (right) tag tamper.

Chapter 3

Sensing methods

The previous chapter gave insight of the RFID and NFC technology and their applications. Furthermore, the tag tamper was introduced with resistance and capacitance sensing methods. The possible applications as well as the occurrence of disturbances was also discussed.

This chapter presents various possible capacitive and resistive measurement methods for implementations of CTT and RTT. The methods are compared regarding measurement time, area, current consumption, temperature behaviour, etc. Some of them contain simulation results to demonstrate the working principle or to point out the disadvantages.

3.1 Capacitive Tag Tamper (CTT)

This section briefly describes the considered measurement methods. Methods that use two pins (none of them is the ground pin) for measuring a capacitance, were not considered and are not mentioned here, because for this thesis, only one GND pin and one GPIO pin are available. Furthermore, the measurements that are able to measure only the relative change of the capacitance are also not included in this thesis.

3.1.1 Charge Based Capacitance Measurement

Figure 3.1 depicts the schematic for the CBCM method. When both V_p and V_n are LOW, the unknown capacitance C_{DUT} is charged. When V_p and V_n are $HIGH$, the charge is transferred to the C_{charge} capacitance. With every clock cycle the voltage V_c rises for one step as shown in Figure 3.2 (upper plot). The step size depends on the ratio between C_{DUT} and C_{charge}, where C_{charge} has to be greater than C_{DUT}. The voltage V_c is rising until it reaches the reference voltage V_{ref}. After crossing the reference voltage, V_{out} transitions to $HIGH$ and, after the defined delay, V_{ctrl} also transitions to $HIGH$ discharging the capacitor C_{charge} over transistors MN_4 and MN_5. The delay should be long enough to fully discharge the capacitor. The frequency of the V_{out} pulses is then the output [5].
Regarding the measurement specifications, defined in Table 1.1, C_{charge} would have to be quite big ($> 20\,\text{pF}$) to reduce the step size and therefore, achieve the required accuracy within $220\,\mu\text{s}$ measurement time.
The size of C_{charge} could be decreased by switching the positions of the two capacitors.

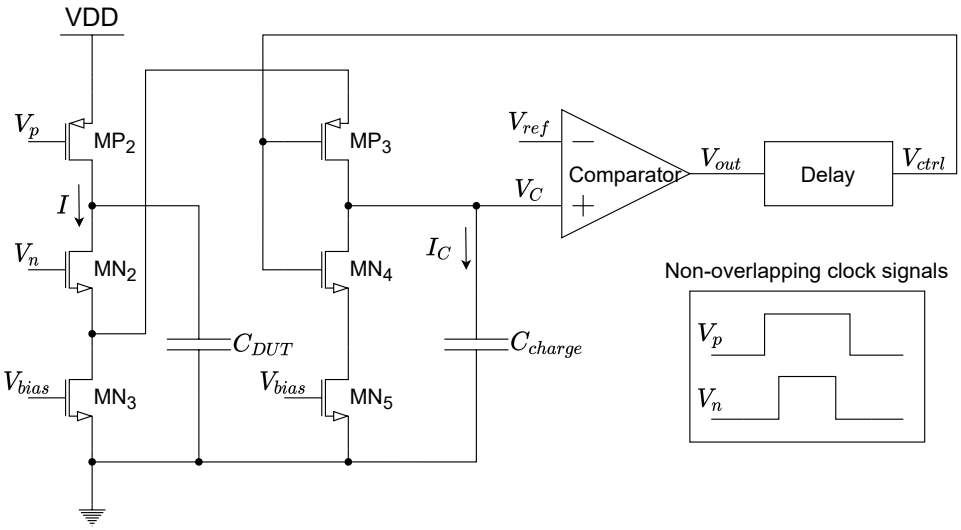

Figure 3.1: CBCM circuit (Modified from sources: [5], [6]).

Now, the capacitor C_{DUT} is charged with the charge transferred from C_{charge}, and therefore C_{DUT} has to be greater than C_{charge}. For given specifications, it is also more convenient to count the pulses during measurement than measure the time between two pulses.
However, including these changes, the required accuracy was not achieved in the specified measurement time.

3.1.2 Capacitive Controlled Oscillator

This method uses an oscillator with capacitors after each inverter to increase the delay as shown in Figure 3.3. The capacitors C_i have a known, fixed value and C_{DUT} is the unknown capacitor. The frequency of the oscillator depends on the value of the C_{DUT} capacitor. Similarly to the CBCM method, the output is the number of pulses in the given measurement time [17], [18], [7].
The delay of the oscillator increases by increasing the C_{DUT}, and therefore the number of pulses decreases. Less pulses means that the capacitances have been charged fewer times which leads to lower current consumption. With larger capacitances, more current is needed to charge them, so the current consumption is higher. These two effects can cancel each other out. The advantage of this method is that the current consumption stays approximately the same over the whole measurement range.
This oscillator method has a strong temperature and supply voltage dependence. Another disadvantage is that the number of pulses is not linearly dependent on the C_{DUT} capacitance as shown in Figure 3.4.

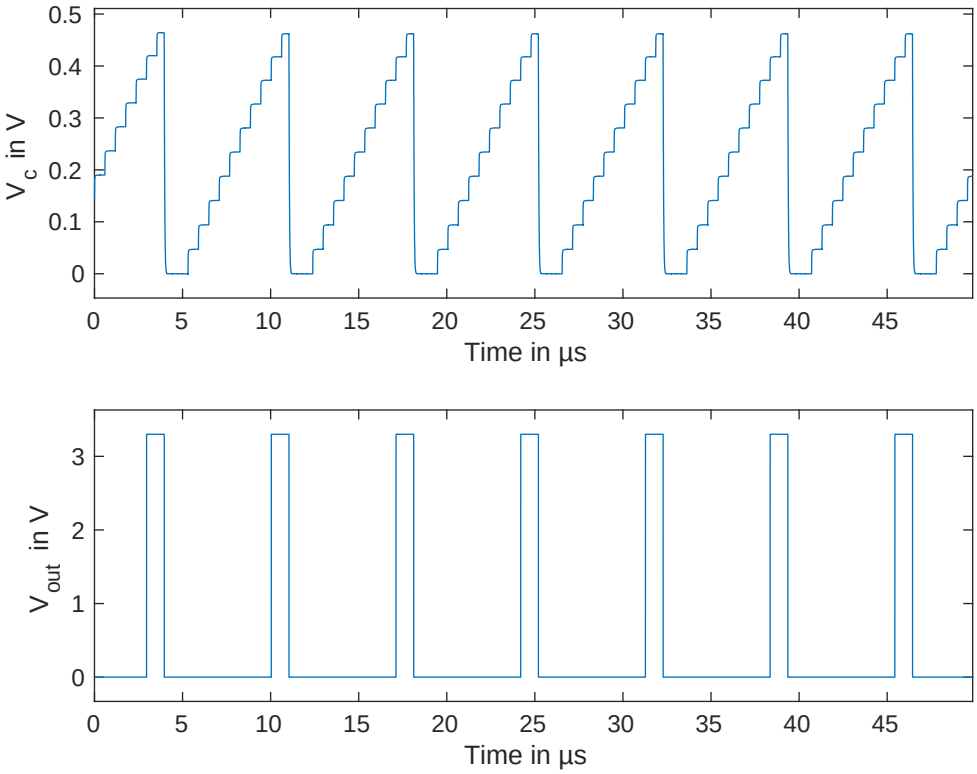

Figure 3.2: CBCM simulation - V_c (upper) and V_{out} (lower).

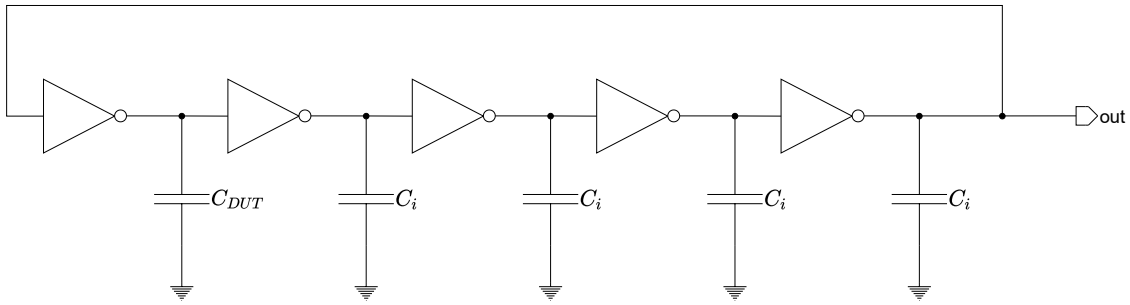

Figure 3.3: Capacitive Controlled Oscillator (Modified from source: [7]).

3.1.3 Delta-Sigma Capacitance-to-Digital Converter

The simple delta-sigma capacitance-to-digital converter, depicted in Figure 3.5, consists of an inverted SC (switched capacitor) integrator, a comparator and a D-latch. The constant voltage $V_{ref1} - V_{ref2}$ is integrated. The integrator starts at a positive voltage, defined by C_{FB} and V_{ref1}, and gets closer to 0 V with each clock cycle. The step size depends on the ratio between the capacitances C_{DUT} and C_i as well as on the difference between the two reference voltages V_{ref1} and V_{ref2}. When the output of the integrator reaches 0 V, the

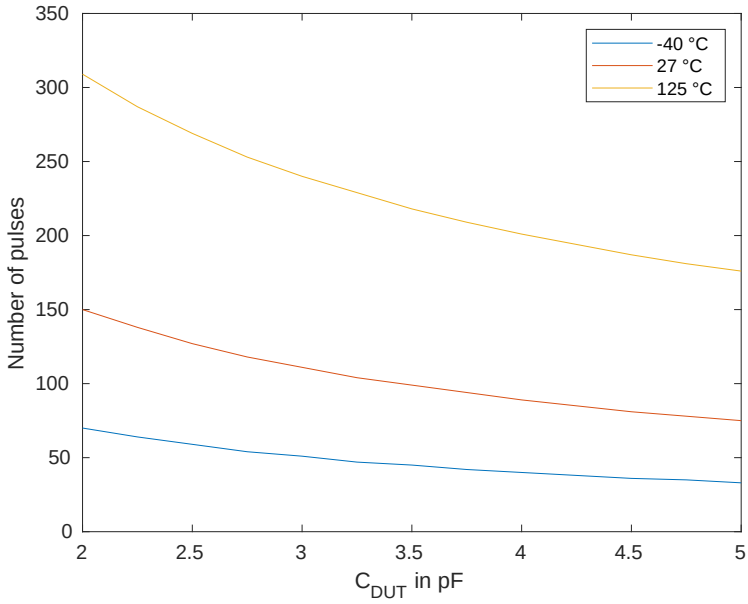

Figure 3.4: Capacitive controlled oscillator simulation - Number of pulses at the output for different temperatures and C_{DUT} capacitance values.

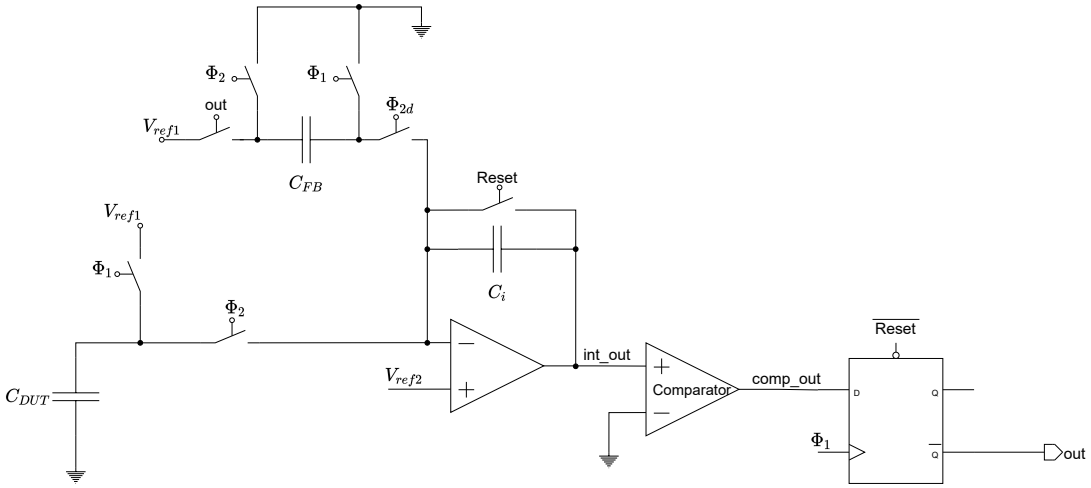

Figure 3.5: Delta-Sigma CDC (Modified from source: [8]).

comparator transitions to *LOW* and the output of the D-latch transitions to *HIGH*. D-latch output keeps the capacitor C_{FB} connected to V_{ref1} until the integrator output jumps to initial positive voltage and the comparator output transitions to *HIGH*. The integration starts again, and for each integration there is a pulse at the output of the D-latch as shown in Figure 3.6. The frequency of these pulses is proportional to the measured capacitance C_{DUT} [8].

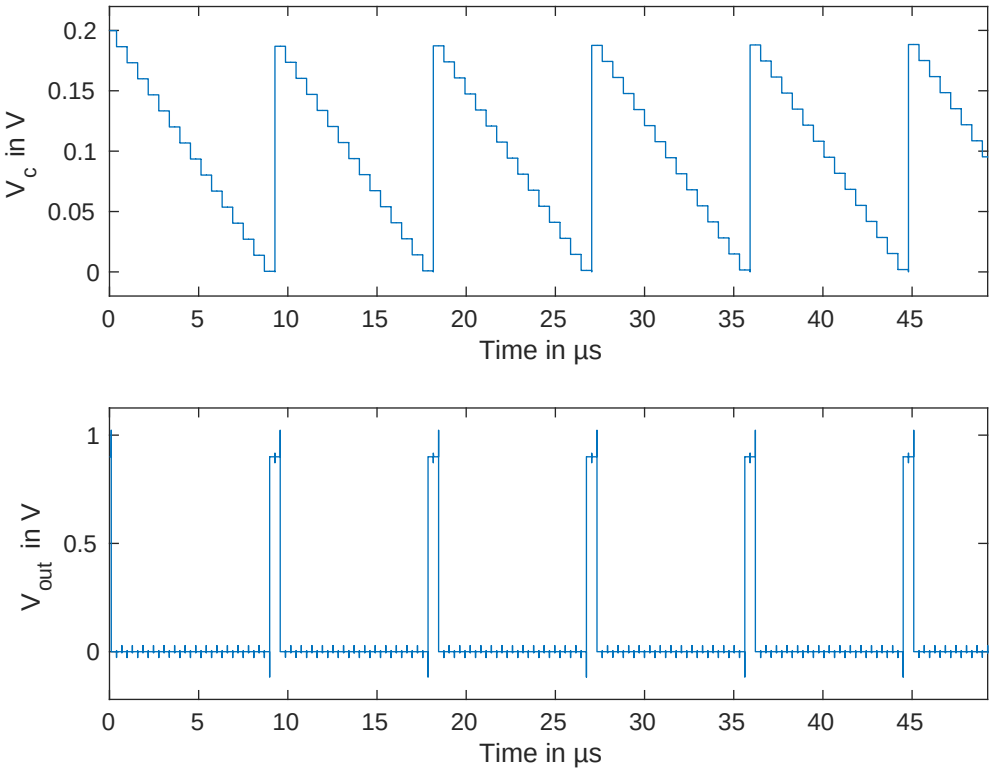

Figure 3.6: Delta-Sigma CDC simulation - Voltage at the inverted integrator output V_{int_out} and output voltage V_{out}.

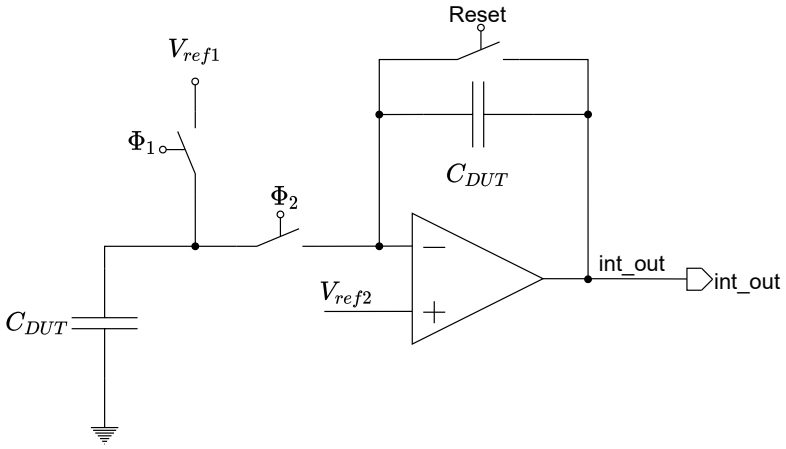

Figure 3.7: SC integrator.

SC Integrator

Figure 3.7 depicts an SC integrator, which is the most important block of the delta-sigma CDC. The output voltage and the clock signals are shown in Figure 3.8. With the equation

(3.1) the voltage at the output of the integrator can be calculated [8]. Offset and error voltage were neglected.

$$V_{int\_out}(n) = V_{int\_out}(n-1) - \frac{C_{DUT}}{C_i} \cdot (V_{ref1} - V_{ref2}) \tag{3.1}$$

Reshaping the previous equation, the voltage step ΔV_{int_out} at the integrator output can be calculated:

$$\Delta V_{int\_out} = V_{int\_out}(n-1) - V_{int\_out}(n) = \frac{C_{DUT}}{C_i} \cdot (V_{ref1} - V_{ref2}). \tag{3.2}$$

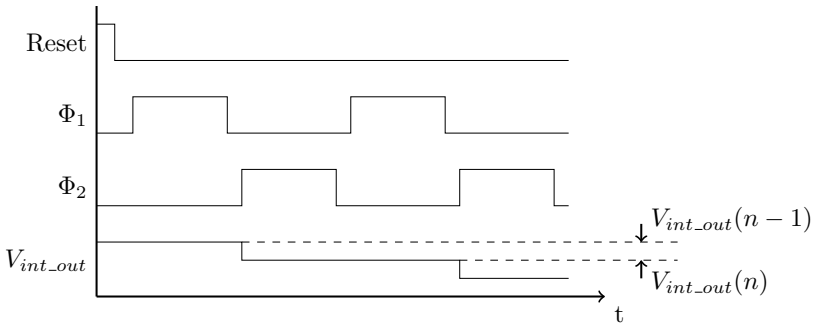

Figure 3.8: SC integrator signals (Modified from source: [8]).

According to the equation (3.2), the voltage step ΔV_{int_out} can be changed by the reference voltages and the capacitance ratio C_{DUT}/C_i. The reference voltages are usually provided and sometimes they cannot be freely chosen. Therefore, for the given capacitance C_{DUT}, the typical way to change the voltage step would be by changing the internal on-chip capacitance C_i. The internal capacitance has to be bigger than the unkown capacitance C_{DUT} or the circuit won't work. Depending on the reference voltages, C_i can be relative big.
To reach the accuracy requirement, a voltage step and a starting voltage have to be chosen with which the number of clock cycles, required to reach 0 V, is different for every 250 fF. This way, the time between two pulses (the frequency) will be different for every 250 fF. However, increasing the accuracy with more steps leads to less pulses in the defined measurement time. The accuracy of $C_{accuracy} = 250\,\text{fF}$ cannot be reached with this specifications. Either a longer measurement time must be specified or a faster clock should be provided, which would lead to higher current consumption.

Considering the discussed accuracy issues, the relative big internal capacitance and the generation of two non-overlapping clocks, it was decided to exclude this method from further investigations.

3.1.4 Linear Slope Charging

Figure 3.9 depicts the block diagram of the linear slope charging CTT. This sensing method is charging the unknown external capacitor C_{DUT} with a constant charging current and comparing the voltage at the capacitor with a reference voltage. The clock pulses are

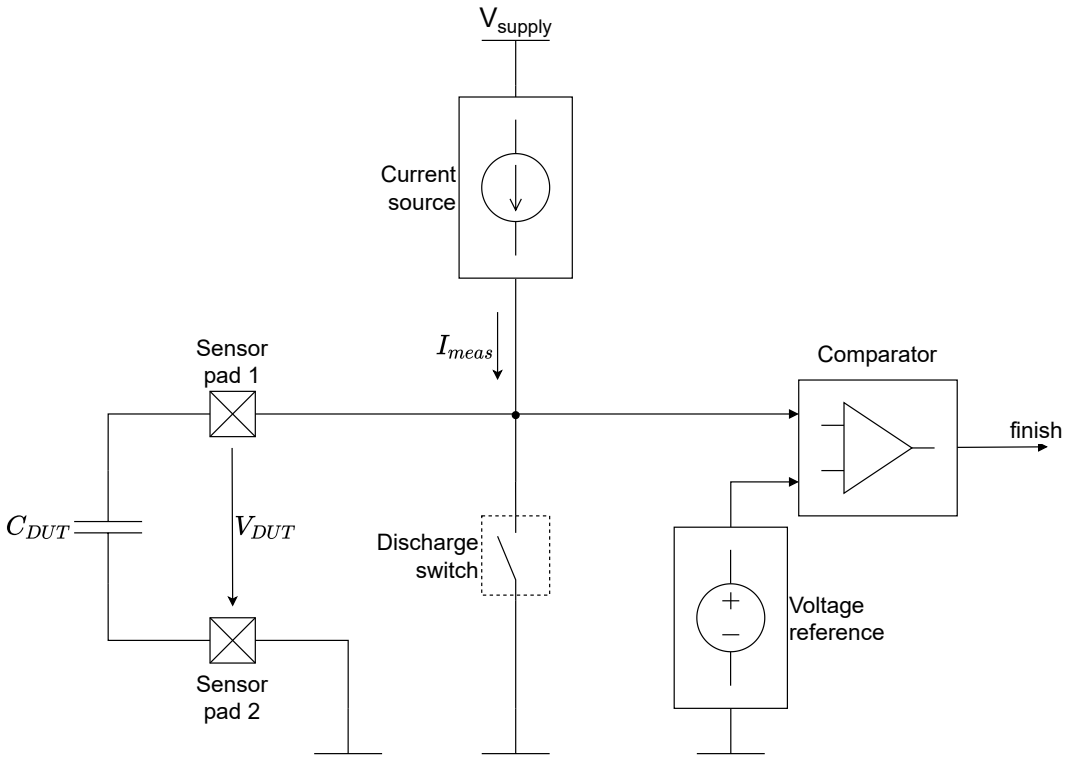

Figure 3.9: Linear slope charging CTT.

counted until the voltage at the capacitor crosses the reference voltage as illustrated in Figure 3.10.

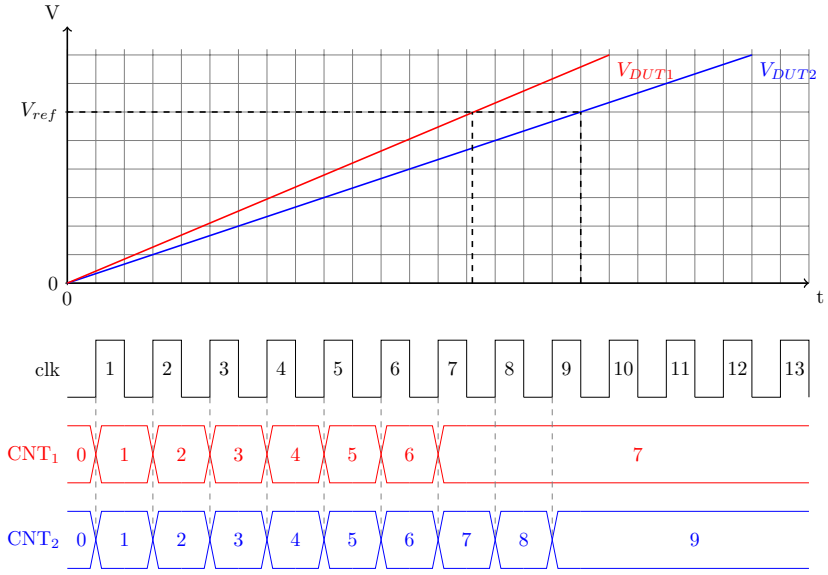

Figure 3.10: Linear slope charging measurement for $C_{DUT1} < C_{DUT2}$.

Out of the equation for capacitance, the unknown capacitance C_{DUT} can be calculated as follows:

$$C_{DUT} = \frac{Q}{V_{ref}} = \frac{I_{meas} \cdot t}{V_{ref}}, \tag{3.3}$$

where I_{meas} is the constant charging current, V_{ref} the reference voltage and t the time needed to charge the capacitance C_{DUT} from 0 V to V_{ref}.

3.1.5 Iterative Delay-Chain Discharge

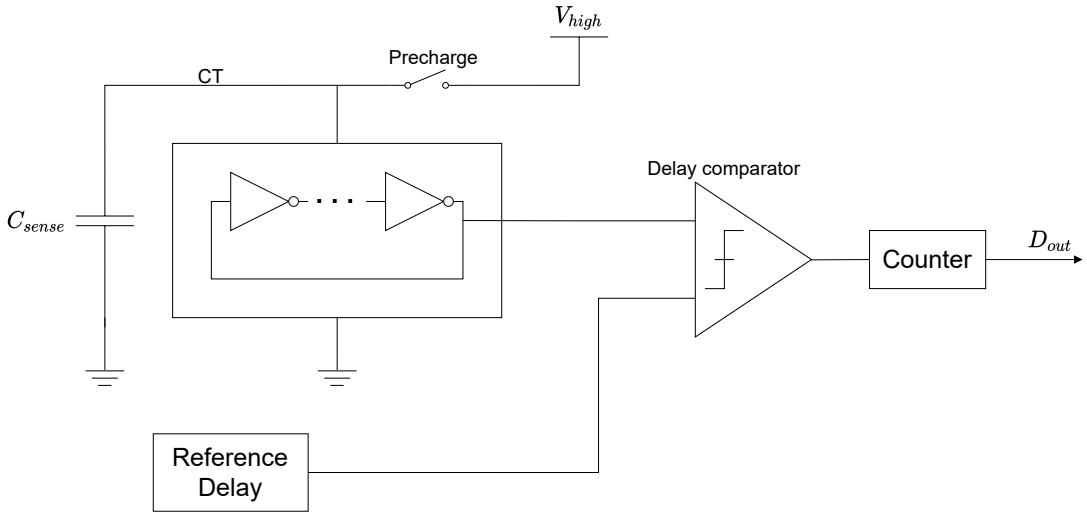

Figure 3.11: Iterative delay chain discharge (Modified from source: [9]).

Figure 3.11 depicts the iterative delay chain discharge. This method uses an oscillator that is supplied with the voltage stored in the capacitor C_{sense}. With each pulse, the oscillator draws charge from the capacitor and therefore the voltage V_{CT} on the capacitor decreases. The voltage decrease increases the delay of the oscillator. The output of the oscillator is connected to a delay comparator which compares the falling edge of the oscillator output and the reference delay. The reference delay can be implemented using the same oscillator, but with a lower supply voltage. The pulses are counted until the delay of the oscillator is larger than the reference delay [9].
The voltage drop at the capacitor depends on the capacitance value of C_{sense}. In a larger capacitor, more charge Q_C is stored at the same voltage (3.4) which means that for each pulse the voltage step V_{CT} will be lower than with a smaller capacitor.

$$Q_C = C_{sense} \cdot V_{high} \tag{3.4}$$

Figure 3.12 depicts voltage V_{CT} for two different capacitances. The capacitor C_{sense} is charged to V_{high} and it is discharged until the voltage V_{CT} reaches the supply voltage V_{low} of the oscillator used as a reference delay. The number of pulses at the output depends on the capacitor C_{sense}. The ratio of two different capacitors will be the same as the ratio of the resulting pulses at the output.

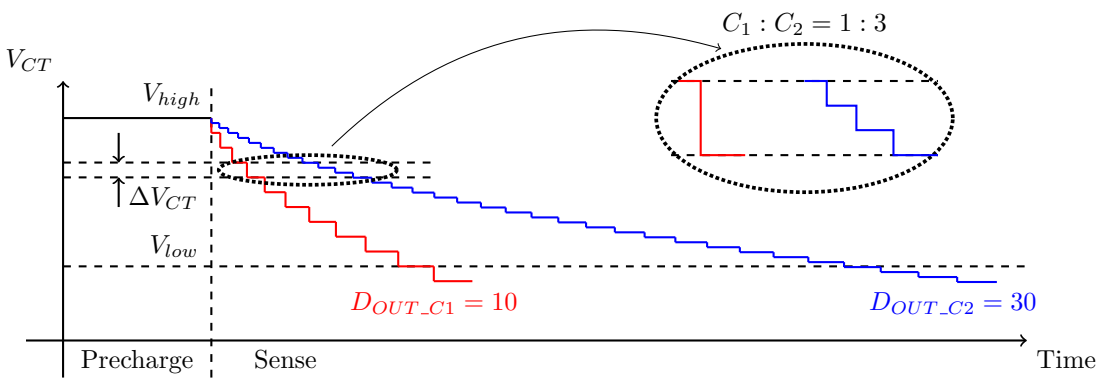

Figure 3.12: Iterative delay chain discharge voltages (Modified from source: [9]).

The voltage step V_{CT} can be calculated as follows:

$$\Delta V_{CT} = \frac{\Delta Q_{osc}}{C_{sense}}, \tag{3.5}$$

where ΔQ_{osc} is the charge that the oscillator consumes when a rise or a falling edge passes through all of the inverters of the oscillator.

The advantages of this method are that it does not require current sources and clock signals. The measurement time of this method is much faster compared to the other methods introduced. It depends on the conversion time of the delay comparator and on the delay of the delay chain.

Reference Delay

The reference delay is generated with a second (reference) oscillator which is supplied with a lower voltage V_{low}. The two oscillators are identical.

Delay Comparator

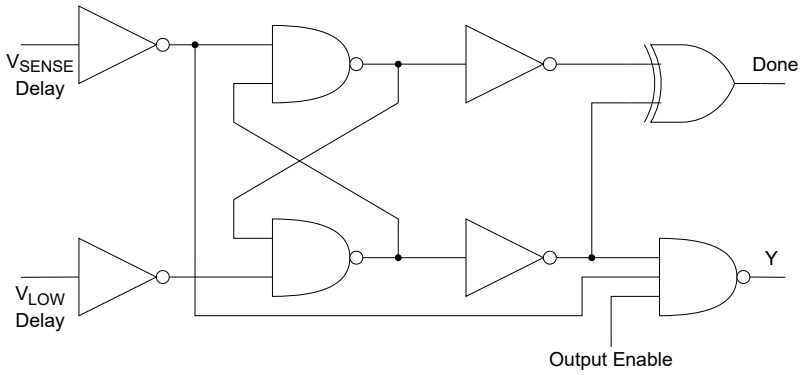

Figure 3.13: Delay Comparator (Modified from source: [9]).

The delay comparator is depicted in Figure 3.13. It is based on SR latch and it compares only the falling edges. The output (Y) is *HIGH* as long as the falling edge of the sense oscillator is faster than the reference oscillator. There is also a *Done* signal that indicates when the comparison finished and the next edge can be generated. The asynchronous counter is counting the Done pulses until the transition of the comparator output from *HIGH* to *LOW*.

3.1.6 Other methods

Besides the described methods, there were also some methods that were considered, but discarded because they did not meet the specifications or the working principle was very similar to other methods already described earlier in this chapter.

Relative Phase Delay

The output signal of this method is a PWM (Pulse Width Modulation) where the duty cycle is proportional to the measured capacitance [19]. The pulse at the input goes through two different paths. One path is delayed with a resistor and the unknown capacitor while the one does not have any resistor nor capacitor. The two pulses are then compared at the output. The difference between these two pulses is then measured.
The specified clock frequency f_{clk} (Table 1.1) is too low to measure the pulse width at the output with the accuracy required. Another possibility would be to use an enormous resistor or increase the pulse width at the input.

Relaxation Oscillator

The output frequency of the relaxation oscillator depends on the time constant $\tau = R \cdot C$. With larger capacitances, the frequency is lower. The capacitance can be determined by counting the pulses at the output in a given time [20].
To be able to count the pulses (for e.g. with asynchronous counters) the frequency of the relaxation oscillator has to be reduced by using a large resistor R. Another disadvantage of this method is the large current consumption.

Time Based CDC using Current Starved Inverters

Similar to relative phase delay, this method also uses two different paths for a pulse of which one is delayed with the unknown capacitance [21]. The output is also a PWM.
To reach the required accuracy ($C_{accuracy}$ in Table 1.1), a TDC (Time-to-Digital Converter) with a reference clock $f_{clk} = 1\,\text{GHz}$ is needed. There is no reference clock available, in this project, to measure the pulse width accurately enough.

Ballistic Techniques

This method measures the charging time of the unknown capacitance [22].
The charging time needs to be decreased to be able to measure it with the available clock frequency. The only way to decrease the charging time is to use a large resistor, which is often unwanted. Furthermore, this method does not have any advantages, compared to

the other methods based on measuring charging time of a capacitance, so it was excluded from additional simulations.

3.2 Resistive Tag Tamper (RTT)

RTT is not the main focus of this thesis and not a lot of research was done regarding external resistance measurement, given the fact that the measurement accuracy is low and it is used only to detect if a wire loop is open or closed (if $R_{DUT} < 50\,\Omega$ or $R_{DUT} > 1\,\mathrm{M}\Omega$). Only one method was considered, but not implemented. The working principle of this RTT is described here. In chapter 4 it is described how to implement the RTT into the existing CTT designs.

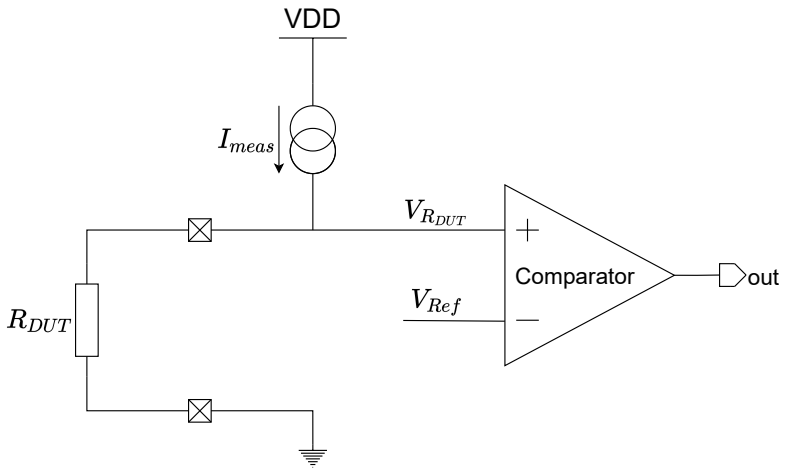

Figure 3.14: Proposed RTT.

The RTT depicted in Figure 3.14 drives a constant current through the unknown resistor R_{DUT}. The current I_{meas} causes a voltage drop $V_{R_{DUT}}$ over the resistor R_{DUT}. The voltage $V_{R_{DUT}}$ is then calculated as follows:

$$V_{R_{DUT}} = I_{meas} \cdot R_{DUT}. \tag{3.6}$$

$V_{R_{DUT}}$ is then compared with a reference voltage V_{Ref}. The RTT is considered open if the comparator output is *HIGH*, and closed otherwise.

Chapter 4

Circuit implementation

In the previous chapter several different measurement methods were introduced as well as their advantages and disadvantages.

This chapter describes the implementation of the linear slope charging CTT and iterative delay chain discharge CTT in a 40 nm CMOS technology. Each block of the two designs is described separately. The important block simulation results are also demonstrated in this chapter.

In addition to the implementation of the CTTs, the possible implementation of resistance measurement for the RTT is discussed.

4.1 Linear slope charging

The working principle of this method is described in section 3.1.4. A supply voltage of $VDD = 1.1\,\mathrm{V}$ was used and an additional clock signal (for digital part) was provided with frequency $f_{clk\_dig} = 3.39\,\mathrm{MHz}$. This faster clock signal is used to measure the charging time with increased accuracy.
To decrease the temperature and voltage variation effects, the same circuit was implemented twice, as shown in Figure 4.1. Two measurements are performed at the same time, with same voltage references for the comparators and the same supply voltage. This way, all long-term variations are cancelled out. The capacitor C_{DUT} and the internal reference capacitor C_{int} are measured. The charging current of the internal capacitor *ioutint* is fixed while the charging current of the external capacitor *ioutext* can be configured depending on the C_{DUT}. The selected current should minimize the difference of the slopes between the external and internal capacitor voltages and therefore, minimize the difference between the two counter values. Furthermore, three different reference voltages are used. At the lowest, the counter starts counting and it stops at the highest reference voltage. The reference voltage in the middle is used for the linearity check.
All the input and output pins are listed in Table 4.3. An example of the signals during the measurement is illustrated in Figure 4.2.

Calibration

Several measurements are done with different values for the charging current *ioutext*. The current which results in the smallest difference in counter values (external CNT_{2ext} and internal CNT_{2int}) is then chosen as the measurement current, and the counter difference is stored as the calibration value:

$$CALIB = CNT_{2ext} - CNT_{2int}. \tag{4.1}$$

Measurement

The measurement is performed with the same charging current that was selected during calibration. After the measurement, the difference between the two counter values CNT_{2ext} and CNT_{2int} (and the calibration value) is compared with *TAMPER THRESHOLD*. If the calculated value exceeds the tamper threshold, the tag is considered tampered. Table 4.1 contains examples for both cases.

CNT_{2ext}	CNT_{2int}	$CALIB$	CNT_{2ext} $-CNT_{2int}$ $-CALIB$	TAMPER THRESHOLD	STATUS
500	480	10	10	30	NOT TAMPERED
550	480	10	60	30	TAMPERED

Table 4.1: Linear slope charging measurement.

Figure 4.3 shows the voltages at the positive input and the output of the comparator for the internal and the external measurement. At the beginning of the measurement, the capacitors are discharged and the charging starts. The counter starts counting at the first transition of the comparator output from *LOW* to *HIGH*. At the second transition the counter value CNT_1 is stored. The final counter value CNT_2 is stored at the third transition and the measurement is finished.

Linearity check

To detect the disturbances, discussed in section 2.2, which would lead to non-linear charging slopes, a linearity check is carried out after the measurement. Three reference voltages are used: $V_{ref0} < V_{ref1} < V_{ref2}$ as illustrated in Figure 4.4. At V_{ref0} the counter starts counting the clock pulses and it stops at V_{ref2}. The counter value at V_{ref1} is also stored to perform the linearity check after the measurement. The slope of the voltage between V_{ref0} and V_{ref1} should be the same ($\pm$threshold) as the slope between V_{ref1} and V_{ref2}.

The chosen reference voltages are: $V_{ref0} = 300\,\text{mV}$, $V_{ref1} = 600\,\text{mV}$, $V_{ref2} = 900\,\text{mV}$.
An exampled is demonstrated in Table 4.2 with $LIMIT = 30$.

CNT_2	CNT_1	$CNT_2 - 2 \cdot CNT_1$	LIMIT	Measurement Error
500	240	20	30	NO ERROR
550	240	70	30	ERROR

Table 4.2: Linearity check example.

Pin	**Use**
VDD	Supply
VSS	Ground
ctt_clk_i	Clock signal
tt_en_i	Enable / disable the CTT measurement
tt_test_en_i	Connect / disconnect the CTT block during test
tt_double_imeas_i	Select / deselect double range measurement
tt_imeas_ctt_ctr_n_i<4:0>	Select the measurement current *ioutext*
tt_cfilt<1:0>	Select the filter capacitance
tt_pulldn_int_cap_i	Discharge capacitors used for internal measurement
tt_pulldn_ext_cap_i	Discharge capacitors used for external measurement
tt_ref_int_sel_i<2:0>	Select reference voltage for internal measurement
tt_ref_ext_sel_i<2:0>	Select reference voltage for external measurement
vref<2:0>	Reference voltages
tt_int_comp_a_o	Indicates when the internal measurement is done
tt_ext_comp_a_o	Indicates when the external measurement is done

Table 4.3: Pins of the linear slope charging CTT.

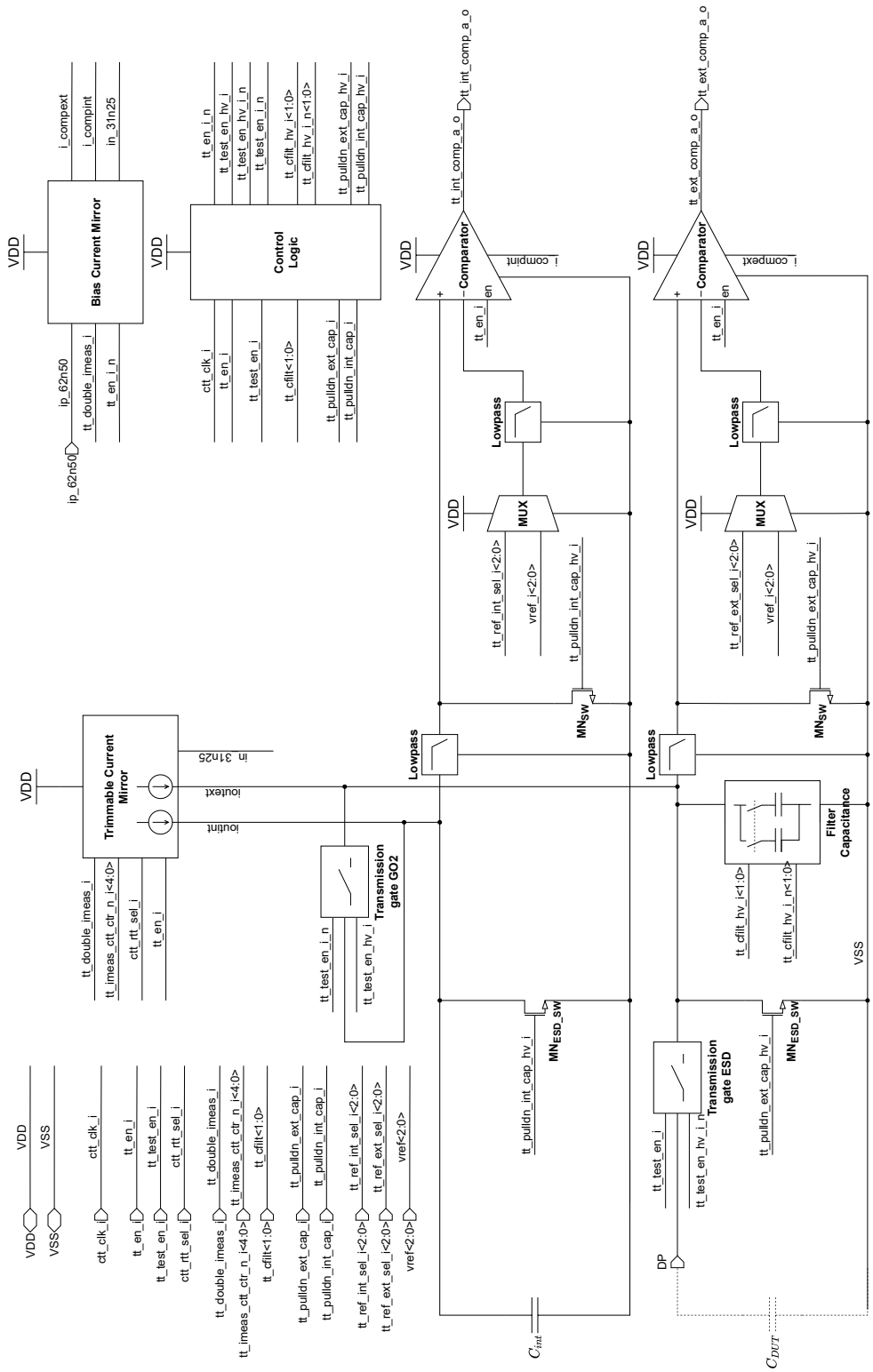

Figure 4.1: Linear slope charging CTT implementation.

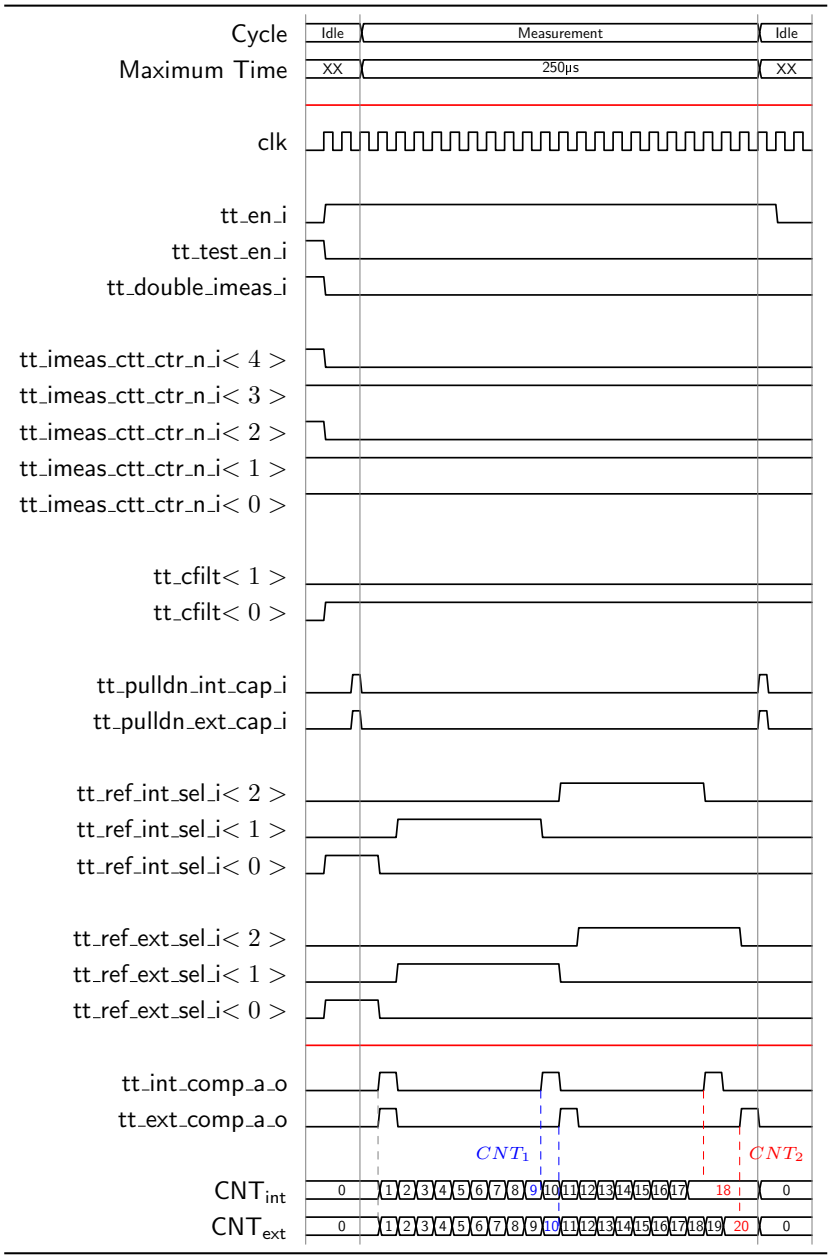

Figure 4.2: Input and output signals of the linear slope charging CTT.

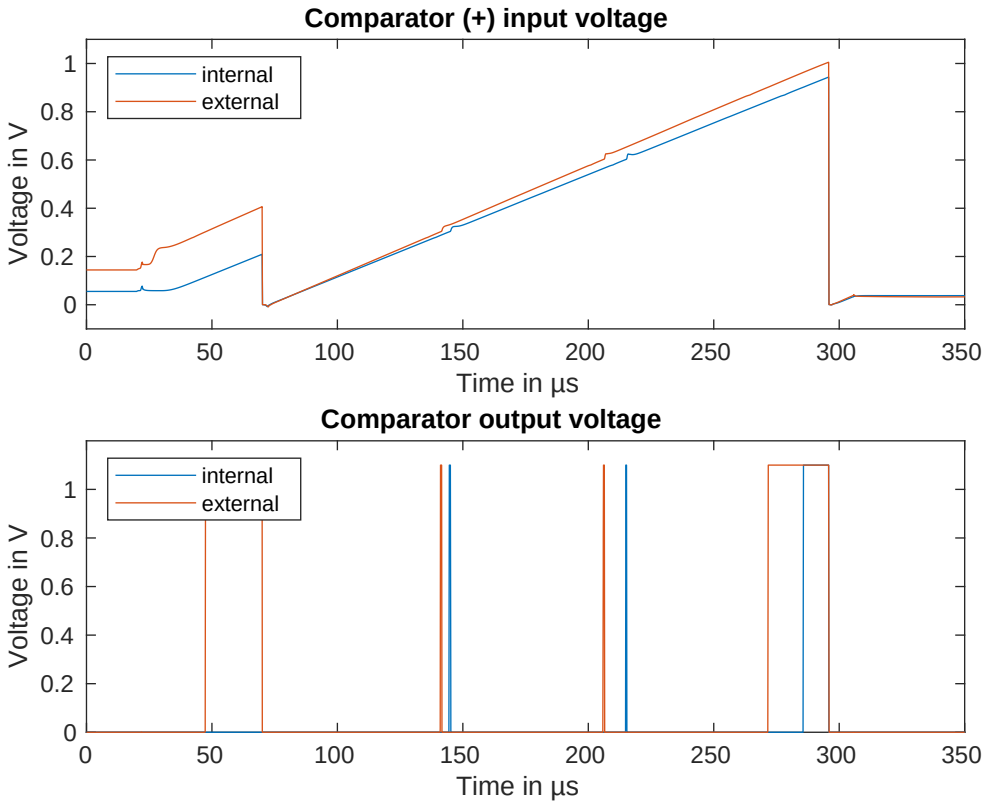

Figure 4.3: Linear slope charging measurement.

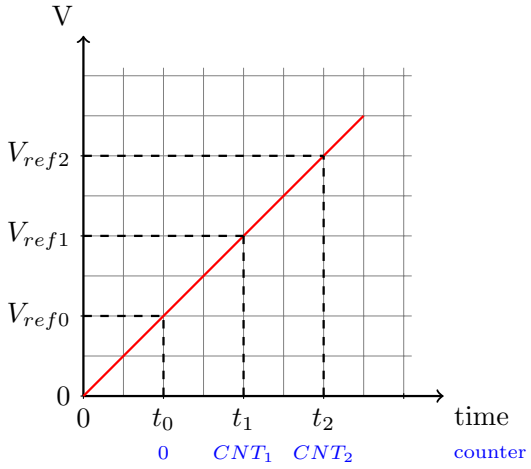

Figure 4.4: Linearity check.

4.1.1 Comparator

The schematic of the comparator is depicted in Figure 4.5. It is designed as an OTA, with transistors MP_{1-7} and MN_{1-7}, and an additional inverter at the output, made out of transistors MP_8 and MN_8. The comparator has a PMOS and an NMOS input differential pair to function properly in the required input voltage range $V = 300\,\text{mV}...\,900\,\text{mV}$.
Transistors MP_{11} and MP_{12} are used to generate the bias voltage *Vbp* for MP_6 and MP_7. The transistor MP_{11} has the same dimensions as transistors MP_4 and MP_5, while the transistor MP_{12} are equal to transistors MP_6 and MP_7.
Similarly to *Vbnp*, the bias voltage *Vbn* for the transistors MN_6 and MN_7 is generated by cascoding the transistors MP_{11} and MN_{12}.
The dummy transistors should be placed at the beginning and the end of the current mirror structures, so that every branch sees the same surrounding and mirrors the current more accurately. Therefore, each dummy transistor has a multiplier of $m = 2$.
The input *en* and its inverse *en_n* generated by the MP_{13} and MN_{13} transistors are used to enable or disable the comparator. This is realized by switching the transistors MP_{en1-3} and MN_{en1-3}.
The offset voltage V_{offset} of the comparator was simulated for different temperatures and input common mode voltage V_{incm}. The simulation results obtained by the Monte Carlo simulation (200 samples) are listed in Table 4.4. The histogram of the offset for local mismatch and $V_{incm} = 600\,\text{mV}$ at 27 °C is shown in Figure 4.6.
The delay t_{delay} of the comparator was simulated by sweeping the voltage at the positive input with a slope of $4\,\text{mV}/\mu\text{s}$, which is in the range of the slopes used in capacitance measurements. The voltage at the negative V_{inn} input was set to a constant value corresponding to the reference voltages. The simulation results are listed in Table 4.5. The histogram of the delay of the comparator with the same parameters is depicted in Figure 4.7.

mismatch	Temperature	$V_{incm} = 300\,\text{mV}$		$V_{incm} = 600\,\text{mV}$		$V_{incm} = 900\,\text{mV}$	
		Mean	Std Dev	Mean	Std Dev	Mean	Std Dev
	°C	µV	mV	µV	mV	µV	mV
global and local	−40	−76.01	1.575	−70.58	1.554	−77.35	1.559
	27	−90.07	1.575	−88.81	1.567	−87.79	1.565
	125	−103.9	1.627	−98.88	1.621	−95.97	1.618
local only	−40	−4.461	1.651	−4.002	1.635	−7.814	1.667
	27	−13.77	1.655	−13.39	1.648	−12.5	1.651
	125	−7.883	1.705	−5.683	1.702	−5.81	1.7

Table 4.4: Monte Carlo simulation results of the comparator offset V_{offset}.

mismatch	Temperature	$V_{inn} = 300\,\text{mV}$		$V_{inn} = 600\,\text{mV}$		$V_{inn} = 900\,\text{mV}$	
		Mean	Std Dev	Mean	Std Dev	Mean	Std Dev
	°C	ns	ns	ns	ns	ns	ns
global	−40	300	393.8	303.7	388.5	341.5	389.9
and	27	322.9	393.5	326.5	391.4	340	390.7
local	125	353.1	405.8	359.2	404.3	373.8	403.6
local	−40	316.7	414.2	319	410.2	356.4	419.6
	27	341.1	414.9	344.2	413.3	357	414.4
only	125	376.1	427.5	381.4	426.6	395.4	426.9

Table 4.5: Monte Carlo simulation results of the comparator delay t_{delay}.

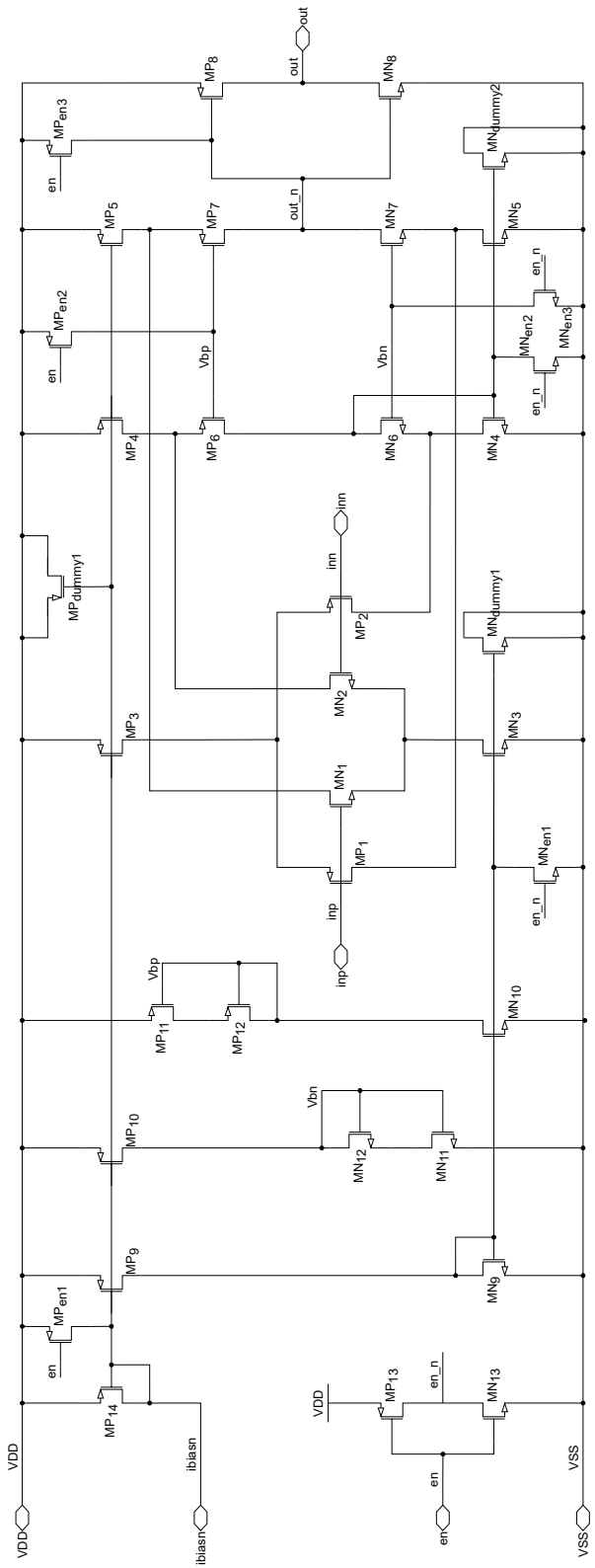

Figure 4.5: Schematic of the comparator.

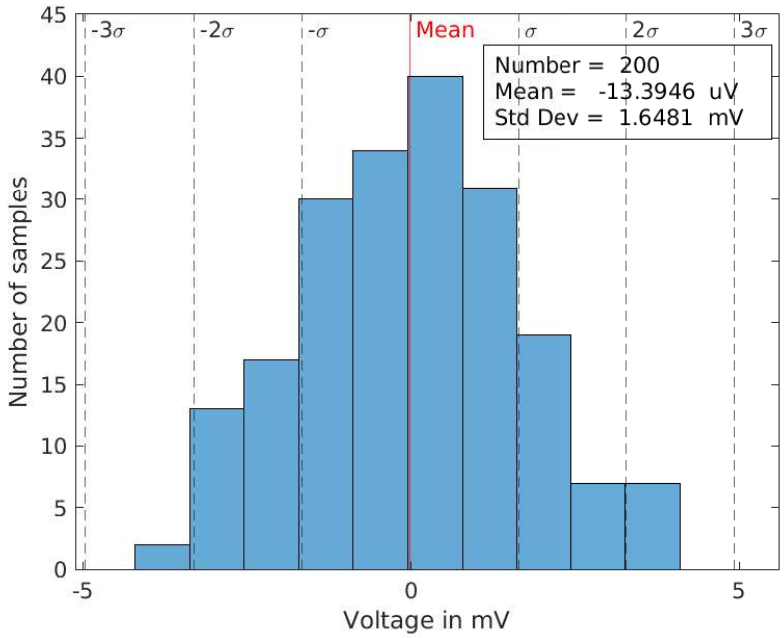

Figure 4.6: Monte Carlo simulation of the comparator offset for local mismatch $V_{incm} = 600\,\text{mV}$ at $27\,^{\circ}\text{C}$.

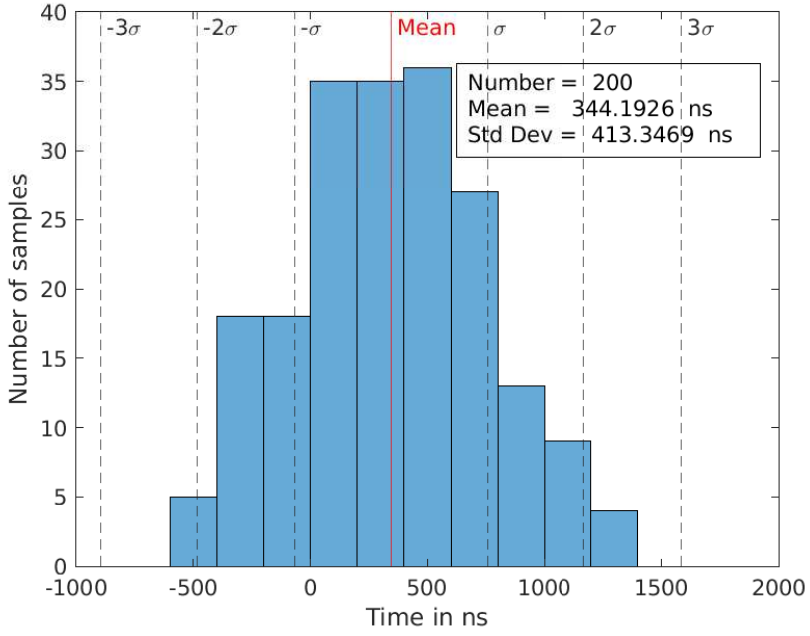

Figure 4.7: Monte Carlo simulation of the delay of the comparator during rising edge for local mismatch $V_{inn} = 600\,\text{mV}$ at $27\,^{\circ}\text{C}$.

4.1.2 Control logic

The control logic block consists of one charge pump and four level shifters. It is used for signal conditioning. The NMOS switches and the transmission gates need controlling voltages higher than the supply voltage *VDD* at the gates of the NMOS transistors to decrease their on resistance R_{on} as described in section 4.1.8. This block creates the inverse of the input controlling signals and increases their *HIGH* level.

Charge pump

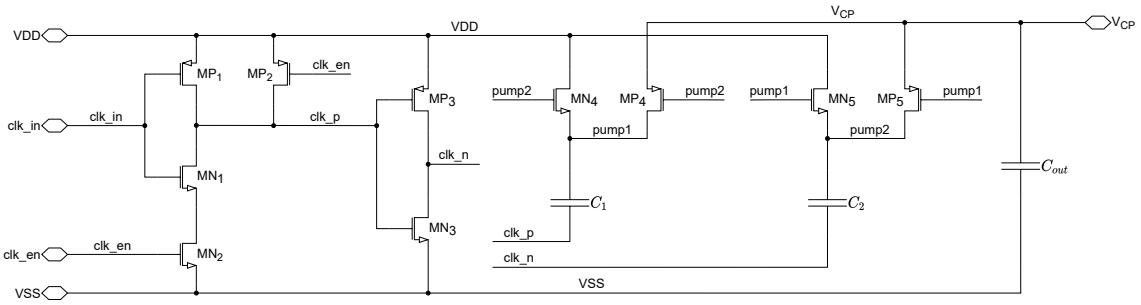

Figure 4.8: Schematic of the charge pump.

The schematic of the charge pump used in this control logic is depicted in Figure 4.8. Charge pump generates a voltage $V_{CP} \approx 2.15\,\mathrm{V}$, which is almost the double of the supply voltage $VDD = 1.1\,\mathrm{V}$.
The settling time $t_{settling}$ is the required time for the voltage V_{CP} to reach it's stable value. This is the minimum time that the charge pump should be running prior to enabling the CTT block, to ensure a proper functionality of the transmission gates and the NMOS switches during measurement. Table 4.6 holds the minimum, maximum and nominal values of the settling time $t_{settling}$ for different temperatures. The simulation was performed over various process corners with $VDD = 1.1\,\mathrm{V}$ and $f_{clk} = 1.695\,\mathrm{MHz}$.
The plot of the output voltage V_{CP}, for nominal corner at 27 °C, is shown in Figure 4.9. The charge pump is enabled by setting the *clk_ en* to *HIGH* at 5 µs.

Temperature	Minimum	Nominal	Maximum
°C	µs	µs	µs
−40	42.79	46.33	51.05
27	41.02	43.67	47.51
125	39.25	41.02	43.97

Table 4.6: Settling time $t_{settling}$ of the charge pump.

Level shifter

The level shifter depicted in Figure 4.10 is used to change the *HIGH* level of the input *in* from the voltage V_{supply_low} to the voltage V_{supply_high}. The input signal *in* is inverted by the CMOS inverter made out of MP_1 and MN_1 to get the inverted input *in_ n* which is the only output of this block that has a *HIGH* level at V_{supply_low}.

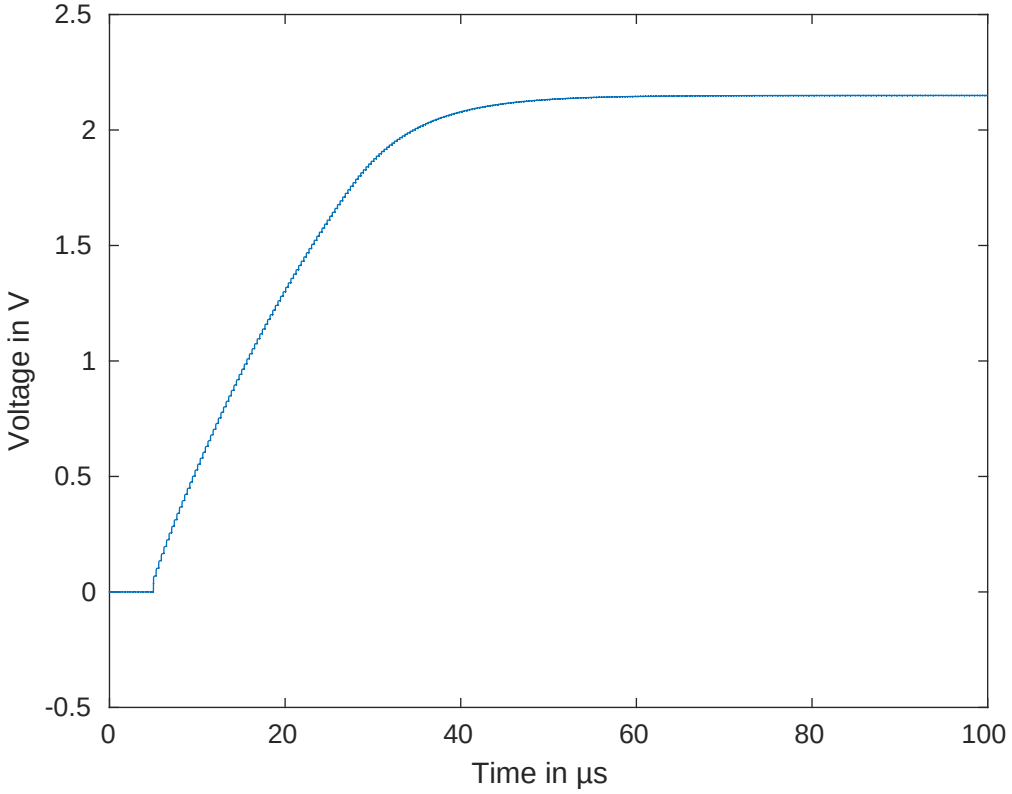

Figure 4.9: Output of the charge pump.

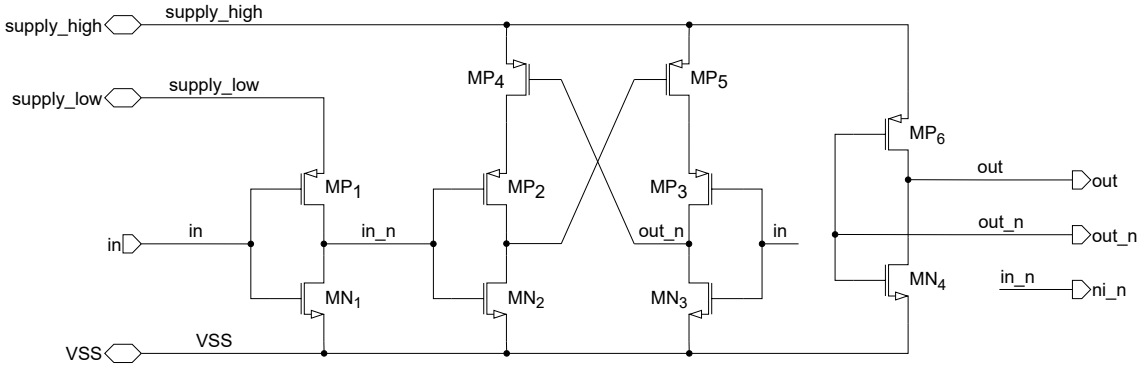

Figure 4.10: Schematic of the level shifter.

When the input in is $HIGH$, the inverted input in_n is LOW and out_n is also LOW due to MP_3 and MN_3 inverter. The inverter consisting of MP_6 and MN_4 inverts the out_n to out which is $HIGH$ with $V_{out} = V_{supply\_high}$.
When the input transitions to LOW, first in_n transitions to $HIGH$ and turns on the transistor MN_2 which pulls the gate of the transistor MP_5 to VSS. The transistor MP_5 is now conducting as well as MP_3 due to $V_{in} = V_{LOW}$. Therefore, $V_{out\_n} = V_{supply\_high}$, and

the output *out* is *LOW*.

The voltage range of this topology is limited by transistor parameters ($V_{ds_{max}}$, V_{th}). However, in order to operate properly, the *HIGH* level of the input *in*, as well as the voltage V_{supply_low}, should be higher than the threshold level of the inverters consisted of MP_2 & MN_2 and MP_3 & MN_3. This requirement is fulfilled when the following is true:

$$V_{supply\_low} > \frac{1}{2} \cdot V_{supply\_high} \tag{4.2}$$

The delay of the three outputs with different voltages and corners was simulated. The values reach up to a few nanoseconds. However, the delay of the level shifter is not of big importance because it is used only to shift the level voltages of the controlling signals for switches and transmission gates. These stay the same during the measurement, so that their delay has no impact on the measurement. Therefore, the simulation results of the level shifter are not presented in this thesis.

4.1.3 Bias current mirror

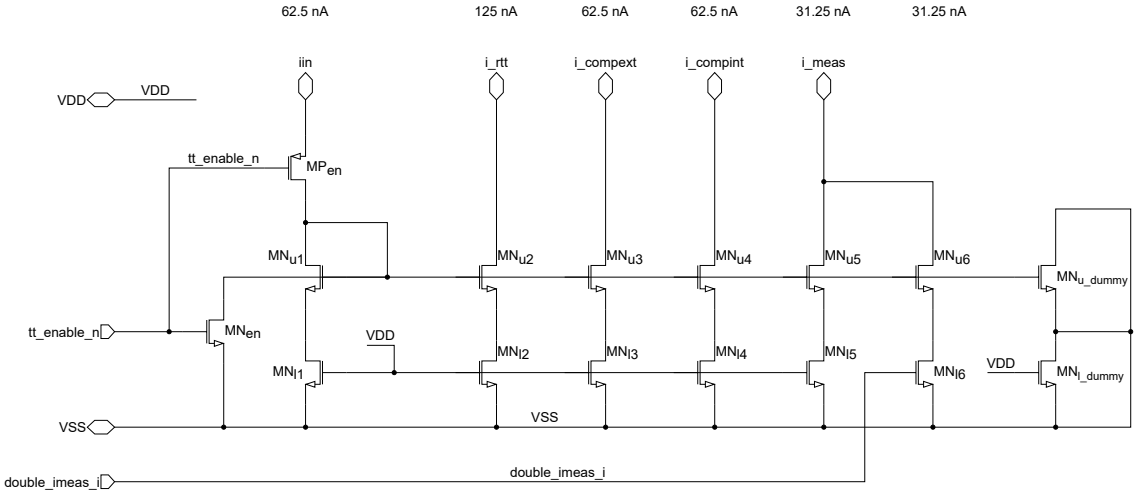

Figure 4.11: Schematic of the bias current mirror block.

The bias current mirror block is used to generate bias currents for the comparators $I_{i\_compext}$ and $I_{i\_compint}$ as well as the measurement currents I_{i_meas} and I_{i_rtt} used by CTT and RTT. This is achieved by current mirrors that mirror the input current I_{iin} as shown in Figure 4.11.

The input *tt_enable_n* is used to enable this block. To enable it, this input has to be *LOW* to turn on MP_{en} and enable the flow of the input current I_{inn}. When set to *HIGH*, MP_{en} is of and the gates of the upper NMOS transistors MNu are pulled to *VSS* with MNen, disabling any current flow.

When using the double range C_{double_range} denfined in Table 1.1, the input *double_imeas_i* should be *HIGH* to enable the NMOS MN$l6$ which doubles the CTT measurement current I_{i_meas}.

The upper transistors MN_{u1} to MN_{u6} are used to mirror the current while the lower transistors MN_{l1} to MN_{l6} are used to enable the individual branches. Only MN_{l6} is needed to enable double range, the other lower transistors are just there for symmetry and are always enabled through the gate connection to *VDD*.

All the upper transistors, including the dummy transistor MN_{u_dummy}, have the same width W_{Nu} and length L_{Nu}. The lower transistors, with the dummy transistor MN_{l_dummy}, have the width W_{Nl} and the length L_{Nl}. However, the number of transistors connected in parallel, represented by the multiplier m, is different. Table 4.7 shows the different multiplier values for each branch. The upper MN_u and the lower MN_l transistors from the same branch have the same multiplier.
The dummy transistors should be placed at the beginning and at the end of the current mirror structure during layout. Therefore, the multiplier $m = 2$ for the dummy transistors. The transistors MP_{en} and MN_{en} are not listed in the table, because they are used as switches to enable and disable this bias current mirror block and their dimensions don't have a significant impact on the performance of the current mirror structure.

Transistor	m
MN_1	2
MN_2	4
MN_3	2
MN_4	2
MN_5	1
MN_6	1
MN_{dummy}	2

Table 4.7: Bias current mirror transistor multipliers.

4.1.4 Trimmable current mirror

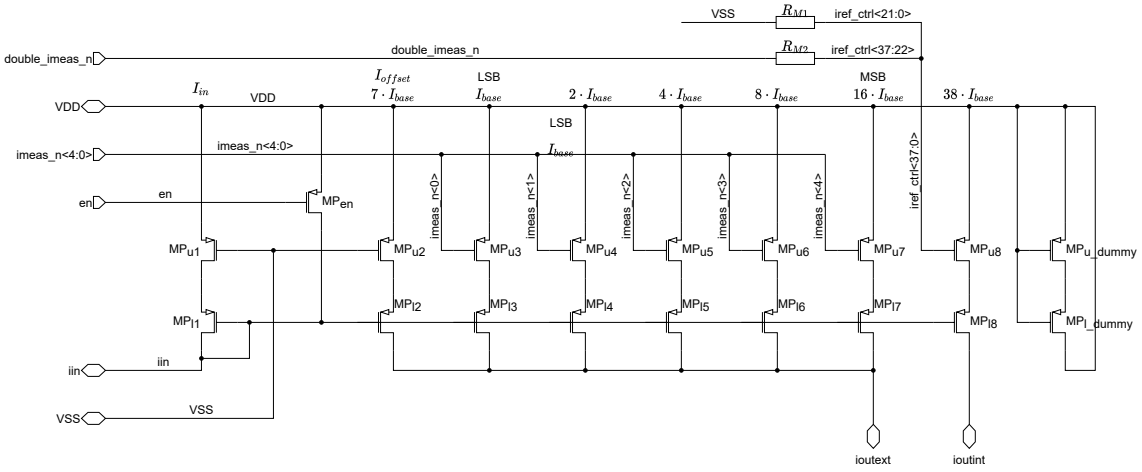

Figure 4.12: Schematic of the trimmable current mirror block.

Trimmable curent mirror defines the currents for charging the unknown external C_{ext} and

the internal reference capacitor C_{int} out of the input current I_{in} at the *iin* pin. The schematic of this block is depicted in Figure 4.12.
The current for the internal measurement $I_{ioutint}$ is fixed with the dimension of the MP_{l7} transistor. It is changed only when the input current I_{iin} is doubled due to double range setting. In this mode the input *double_ imeas_ n* is *HIGH*, which turns off transistors 22-to-37 and therefore, decreases the output current $I_{ioutint}$.
The current $I_{ioutext}$ is used to charge the external capacitor. Its value can be trimmed with the *imeas_ n*<4 : 0> input signals.

The input *imeas_ n*<4 : 0> enables/disables the individual branches of the current mirror structure, by switching the transistors MP_{u3} to MP_{u7}. Similar to the bias current mirror block described in the previous section, the dimensions of one transistor unit for the upper and the lower transistors is defined. The transistors are then connected in parallel. The number of transistors is represented by the multiplier m, which is listed in Table 4.8, together with the current flowing through each branch.

Transistor	m	Current
-	-	nA
MP_1	32	31.25
MP_2	7	6.836
MP_3	1	0.977
MP_4	2	1.953
MP_5	4	3.906
MP_6	8	7.813
MP_7	16	15.625
MP_8	38	37.109
MP_{dummy}	2	0

Table 4.8: Trimmable current mirror transistor multipliers.

The output current I_{outext} can be calculated with the following equation:

$$I_{outext} = (31 - imeas\_n_{dec}) \cdot I_{base} + I_{offset} = (31 - imeas\_n_{dec}) \cdot \frac{I_{in}}{32} + 7 \cdot \frac{I_{in}}{32}, \quad (4.3)$$

where $imeas\_n_{dec}$ is a decimal number converted from the 5-bit input controlling signal *imeas_ n*<4 : 0>. The base current I_{base} is the current flowing through one transistor:

$$I_{base} = \frac{I_{in}}{32}. \quad (4.4)$$

The offset current I_{offset} is chosen to be seven times the base current I_{base}. By inserting the calculations for the offset and the base current in the equation (4.3), the following equation is obtained:

$$I_{outext} = (31 - imeas\_n_{dec}) \cdot \frac{I_{in}}{32} + 7 \cdot \frac{I_{in}}{32}. \quad (4.5)$$

The values of the input current I_{in} depending on the *double_ imeas_ n* input, as well as the values for the output current I_{outint} for the measurement of the internal capacitance, are shown in Table 4.9.

double_imeas_n	I_{in}	$I_{ioutint}$
-	nA	nA
HIGH	31.25	37.109
LOW	62.5	42.969

Table 4.9: Trimmable current mirror input I_{in} and output current $I_{ioutint}$.

The transistor MP_{en} is used to enable the block by setting input *en* to *HIGH*.
The resistors R_{M1} and R_{M2} are metal connections which allow connecting the single input nodes to multiple nodes.

4.1.5 Multiplexer

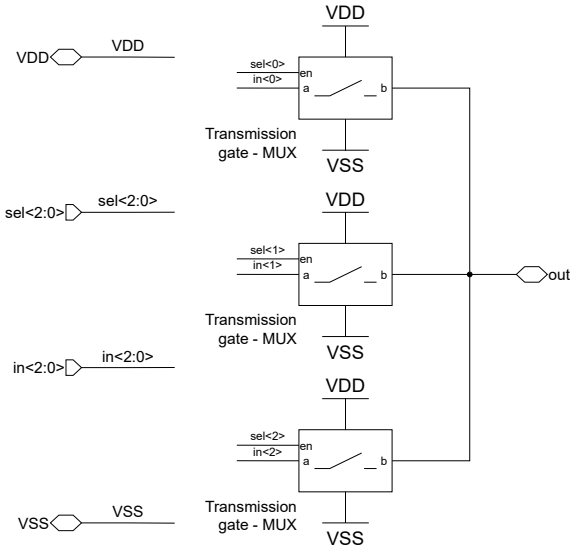

Figure 4.13: Multiplexer.

The multiplexer is used to select between three different reference voltages. The schematic of the multiplexer is depicted in Figure 4.13. It consists out of three identical transmission gates which are described in section 4.1.8. The reference voltages are connected on the *in<2:0>* pins and they are individually selected by switching the transmission gates with *sel<2:0>*. There shouldn't be more than one *sel* pin *HIGH* at once in order to get the correct reference voltage at the output *out* of the multiplexer.

4.1.6 Low-pass filter

The low-pass filter used in this implementation has two main tasks. The first is to filter the disturbance that can be induced by the reader on the detection pin (DP). The disturbance frequency is also the reader frequency $f_{disturb} = 13.56\,\mathrm{MHz}$. An RC low-pass filter, as shown in Figure 4.14, was designed to filter this disturbance. The chosen resistance and capacitance were $R = 1\,\mathrm{M\Omega}$ and $C = 1\,\mathrm{pF}$, which defines the corner frequency of the filter as follows:

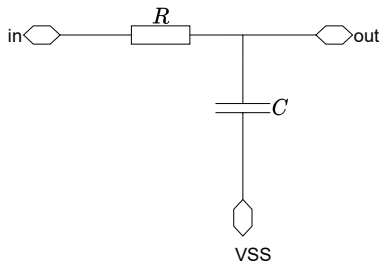

Figure 4.14: RC low-pass.

$$f_c = \frac{1}{2 \cdot \pi \cdot R \cdot C} = \frac{1}{2\pi \cdot 1\,\mathrm{M\Omega} \cdot 1\,\mathrm{pF}} = 159.155\,\mathrm{kHz}. \tag{4.6}$$

The values obtained by the AC simulation are in Table 4.10. The corner frequency f_c is not exactly the same as the calculated value in (4.6) because the resistor and capacitor values are set by their dimensions, and are not exactly the same as the values used in the calculation. Attenuation a and attenuation in dB a_{dB} at $f = 13.56\,\mathrm{MHz}$ were also determined by the AC simulation as shown in Figure 4.15.

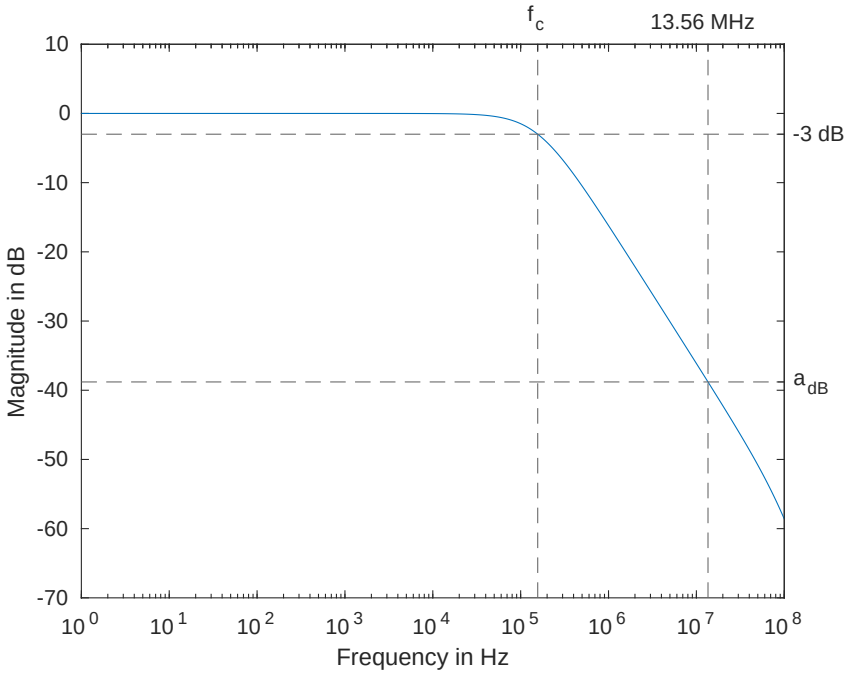

Figure 4.15: RC low-pass - AC simulation.

For the given attenuation a and the input voltage $V_{in} = V_{disturb}$, the output voltage of the RC low-pass filter for the disturbance can be calculated. The frequency is known since it is the frequency of the NFC reader $f_{reader} = 13.56\,\mathrm{MHz}$. The amplitude depends on the C_{DUT} as discussed in section 2.2.1. For the calculation, the worst-case disturbance influence is chosen with smallest capacitance $C_{DUT} = 2\,\mathrm{pF}$. According to Table 2.3, the

f_c	a_{dB}	a
kHz	dB	-
156.4	-38.8	$11.48 \cdot 10^{-3}$

Table 4.10: RC low-pass values obtained by AC simulation.

amplitude of the disturbance voltage, which is also the voltage at the input of the filter, is $V_{disturb} = 0.7\,\mathrm{V}$.

$$V_{out} = V_{disturb} \cdot a = 0.7\,\mathrm{V} \cdot 11.48 \cdot 10^{-3} = 8.036\,\mathrm{mV} \tag{4.7}$$

The V_{out} calculated in (4.7) is the maximum possible amplitude of the voltage, induced by disturbance, that can occur at the filter output.

The second task of the RC low-passs filter is to filter the output of the multiplexer MUX, to avoid voltage ripples when the multiplexer is switching between different reference voltages. A voltage ripple at the negative comparator input could cause the comparator to trigger to early which would result to wrong counter values. The same RC filter, as for filtering the disturbance, was used in this case.

4.1.7 Filter capacitance

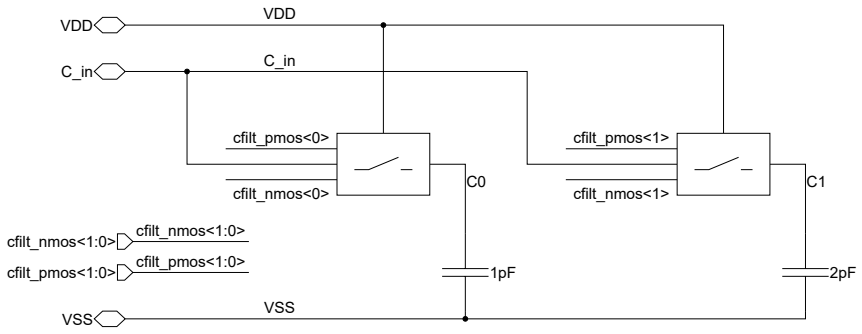

Figure 4.16: Selectable filter capacitance.

With the filter capacitance block, depicted in Figure 4.16, the user can add additional capacitors to the external measurement path. This filter capacitance C_{filt} is required depending on the expected disturbance induced by the NFC reader. Increasing the filter capacitance, increases the overall capacitance to charge during measurement. Therefore, the charging current *ioutext* should also be increased accordingly,
The capacitance can be changed by switching the GO2 transmission gates, described in section 4.1.8, with *cfilt_ pmos<1:0>* and *cfilt_ pmos<1:0>* inputs. The input PMOS signal *cfilt_ pmos<1:0>* is always the inverse of the NMOS controlling signal *cfilt_ nmos<1:0>*. The possible settings for the filter capacitance are listed in Table 4.11.

cfilt_nmos<1>	cfilt_nmos<0>	C_{filt}
-	-	pF
LOW	LOW	0
LOW	HIGH	1
HIGH	LOW	2
HIGH	HIGH	3

Table 4.11: Possible settings for the filter capacitance C_{filt}.

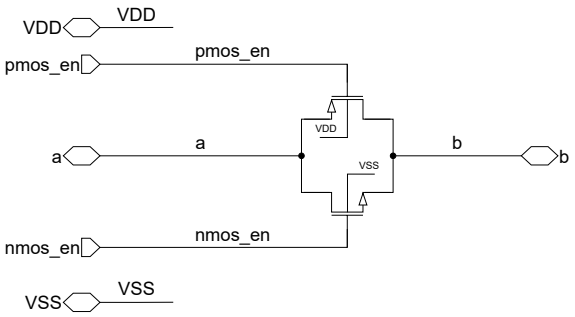

Figure 4.17: Transmission gate ESD.

4.1.8 Transmission-gate

ESD

The ESD transmission gate is used to enable or disable the CTT block. It is positioned directly at the detection pin of the IC and therefore, ESD transistors are used. This transmission-gate is made up of one PMOS and one NMOS as depicted in Figure 4.17. The substrate terminals (bulks) of the transistors are connected to the supply VDD or to ground VSS. Each transistor has its own controlling input signal $pmos\_en$ and $nmos\_en$. When the voltage at the NMOS gate ($nmos\_en$) is $HIGH$ ($pmos\_en$) and the voltage on the PMOS gate is LOW, the switch is on an there is a conducting path between a and b with a resistance R_{on}. To turn off the switch the voltage at $nmos\_en$ has to be LOW and $HIGH$ on $pmos\_in$ pin. This results to a resistance R_{off}.

The on resistance of this block depends on the input voltage V_a, as illustrated in Figure 4.18. The source of the NMOS is connected to the output b. As the input and output increase, the threshold voltage of the NMOS V_{T_n} increases because of the source-bulk voltage increase. If the gate voltage is too low, the transistor goes to subthreshold region and the on resistance R_{on} increases as shown in Figure 4.18 (blue line). The resistance is decreased again when the PMOS goes to linear region.
By increasing the gate voltage V_{nmos_en}, the NMOS stays in linear region for higher voltages (orange). Therefore, a voltage higher than VDD is needed to minimize the nonlinearities introduced by the transmission gate.

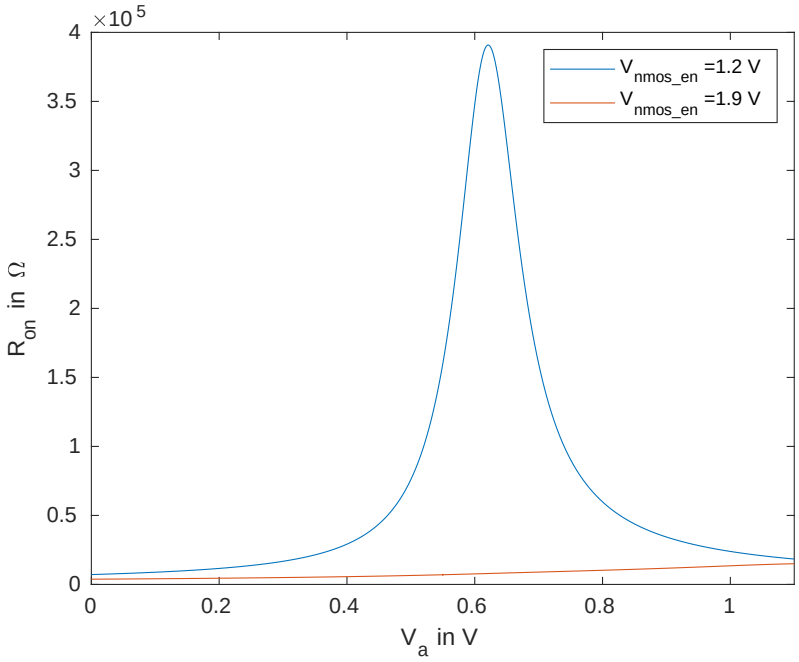

Figure 4.18: The transmission gate *on* resistance R_{on} over the input voltage V_a for different NMOS gate voltages V_{nmos_en}.

GO2

The GO2 transmission gate is used to short the outputs of the trimmable current mirror during test to prevent possible damages to the the current mirror transistors with thinner gate oxide (GO1).

The same topology and controlling signals are used in this transmission gate as in ESD. The only difference is the transistors that are used. Instead of the large ESD transistors, the GO2 transistors are used, which have a thicker gate oxide and can withstand higher voltages than the GO1 transistors in MUX transmission gates.

MUX

The schematic of the MUX transmission gate is depicted in Figure 4.19. This transmission gate has one controlling input *en* for the NMOS transistors and generates the inverted and slightly delayed signal *en_ n* for the PMOS transistors with the inverter made out of MP_1 MN_1. Transistors MN_2 and MP_2 are used to delay the *en* signal so that the dummy transistors switch at the same time as the transistors MN_3 and MP_3.
This transmission gate is used in the multiplexer which chooses the reference voltage for the comparator. To avoid any variations in reference voltage, due to switching transistors, the dummy transistors were added. These are necessary to reduce the charge injection from the switching transistors.

Because of the constant reference voltage at the input of the transmission gates, the on resistance R_{on} has no significant impact on the output voltage. Therefore, controlling

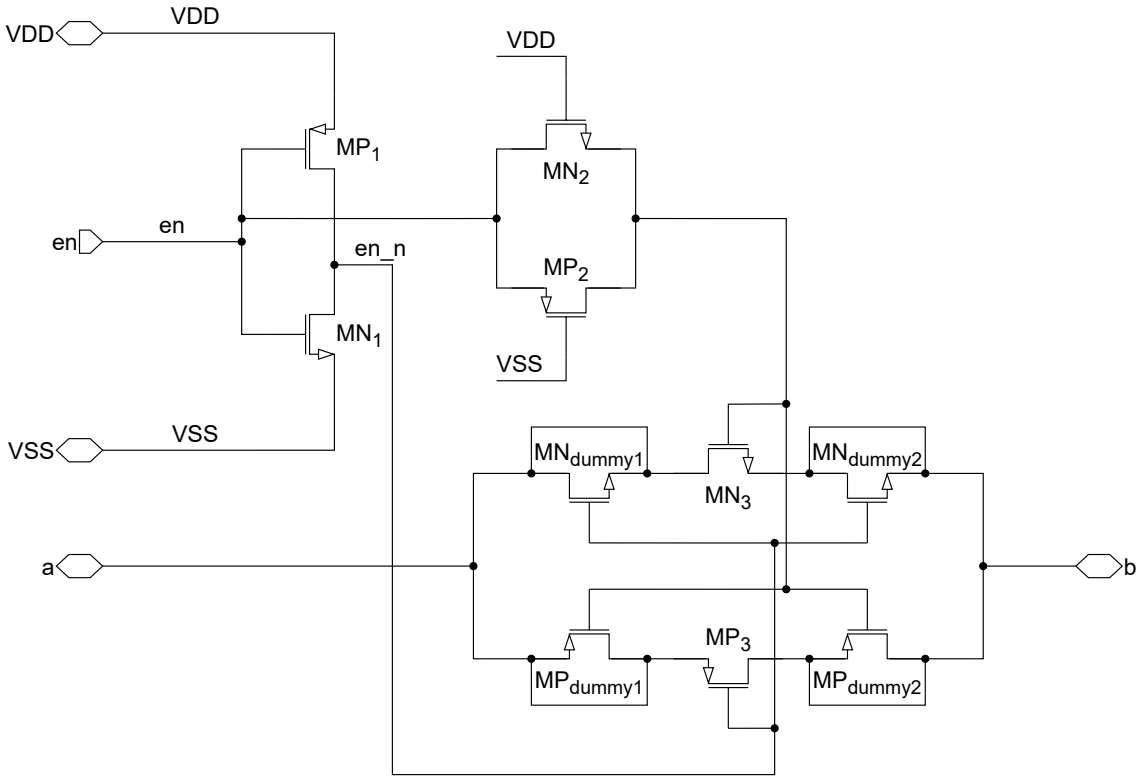

Figure 4.19: Transmission gate MUX.

voltages with *HIGH* level higher than *VDD* are not necessary.

4.1.9 NMOS switches MN_{SW} and MN_{ESD_SW}

The NMOS switches are used in the internal and external measurement path. They discharge the capacitors before and after the measurement.

MN_{ESD_SW} is an ESD NMOS transistor to be able to withstand higher voltages at the detection pin. It is used to discharge the external C_{DUT} as well as the filter capacitance C_{filt}. This transistor needs to discharge the maximum capacitance $C_{DUT\_max} + C_{filt} = 10\,\mathrm{pF} + 3\,\mathrm{pF} = 13\,\mathrm{pF}$ charged to $VDD = 1.1\,\mathrm{V}$ in less than 600 ns.
The same transistor is used for the internal measurement to discharge the internal reference capacitor C_{int}.

MN_{SW} is used to discharge the capacitor in the low-pass filter. This transistor is much smaller because it does not have to withstand voltages higher than *VDD* and it has to discharge only a capacitance of 1 pF.

4.1.10 Double range

Linear charging slope CTT has the double range feature implemented, which enables the extending the measurement range from $C_{range} = 2...5\,\mathrm{pF}$ to $C_{range\_dbl} = 4...10\,\mathrm{pF}$. By

increasing the range, the accuracy is decreased to $C_{accuarcy\_dbl} = 500\,\text{fF}$.
The double range is activated by setting the *tt_double_imeas* pin to *HIGH*. This setting doubles the measurement current I_{i_meas} in the bias current mirror block, as described in section 4.1.3. The charging currents I_{outint} and $I_{ioutext}$ are then generated in the trimmable current mirror block described in section 4.1.4.

4.1.11 RTT implementation

The RTT, described in section 3.2, can easily be implemented additionally to the CTT described in this section. The reference voltages and the comparator at the external measurement path can be reused. A dedicated RTT current source can be implemented and connected to the *ioutext*. The measurement current should be chosen depending on the requirements.
If the wire loop resistance $R_{DUT} > 1\,\text{M}\Omega$ is considered as tampered, and the voltage reference is $V_{ref1} = 600\,\text{mV}$, the current I_{meas}, needed for the RTT measurement, can then be calculated as follows:

$$I_{meas} = \frac{V_{ref1}}{R_{DUT}} = \frac{600\,\text{mV}}{1\,\text{M}\Omega} = 600\,\text{nA} \tag{4.8}$$

The reuse of the comparator minimizes the area increase which is determined by the additional current source block. The size of this block depends on the value and accuracy of the measurement current I_{meas}.

4.2 Iterative delay chain discharge

This CTT was implemented slightly different than the method described in section 3.1.5. Several improvements, regarding the requirements, were made, as shown in Figure 4.21. However, the working principle stays the same. All the input and output pins are listed in Table 4.12. An example of the controlling signals during the measurement is illustrated in Figure 4.22. The voltages used in this implementation are: $V_{high} = 1.1\,\text{V}$, $V_{low} = 0.75\,\text{V}$ and $V_{tgate} = 2.1\,\text{V}$.
The biggest change is that the same circuit is implemented twice. Two measurements are performed in parallel at the same time, once with the unknown capacitance C_{DUT}, and once with the internal reference capacitance C_{int}. The difference of the counter values for the external and the internal capacitance are then subtracted. With this approach, the errors, induced by reference voltage variation as well as temperature influences, are minimized. The value for the internal reference capacitance C_{int} should be set during calibration and its value should result to a minimal value for $CALIB$.

$$CALIB = CNT_{ext} - CNTint. \tag{4.9}$$

There are two delay chains. The reference delay chain **ref** is supplied with a constant voltage, while the **sense** delay chain is supplied with the voltage stored in the unknown capacitor C_{DUT}. The voltage at the capacitor decreases with every edge passing through the **sense** delay chain, causing the delay of the delay chain to increase. The delays of the two delay chains are then compared in the delay comparator. The clock pulses *clk*

are counted while the *finish* output of the delay comparator is *HIGH*. The counter values for the external CNT_{ext} and the internal CNT_{int} measurement are then subtracted and corrected with the calibration value $CALIB$.

$$\text{Result} = CNT_{ext} - CNT_{int} - CALIB \tag{4.10}$$

Figure 4.20 depicts the voltages at the supply of the sense delay chain and at the output of the delay comparators, as well as the corresponding counter values for capacitance measurements $C_{DUT} = 2\,\text{pF}$ and $C_{DUT} = 5\,\text{pF}$.

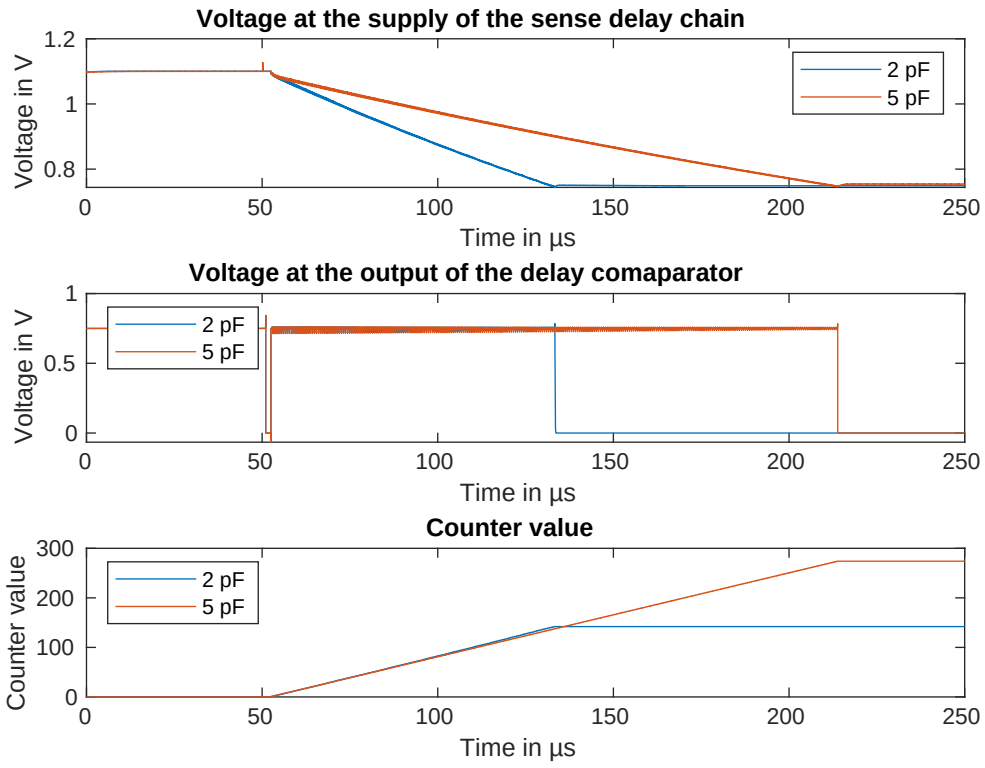

Figure 4.20: The voltages at the sense delay-chain supply for $C_{DUT} = 2\,\text{pF}$ and $C_{DUT} = 5\,\text{pF}$, as well as the voltages at the output of the delay comparator and the corresponding counter values.

The PMOS **MP_charge** is used to charge the capacitor when the *charge_en_n* is *LOW*.

The transmission gate is added to have the ability to disable the CTT block when it is not in use. For the transmission gate to work properly, a level shifter was needed, and a higher voltage *vtgate*. The level shifter used in this CTT is the same as in the linear slope charging CTT in section 4.1.2. It is assumed that a higher voltage will be available, however, if that's not the case, the charge pump, as described in section 4.1.2, can be implemented.

An RC low-pass filter was added to filter the disturbances induced by the NFC reader. This

low-pass filter limits the pulse frequency at the delay chain input *edge_ext*. The **sense** delay chain is consuming charge from the capacitor of the RC filter for each edge. The time between two edges has to be long enough for the charge to transfer from the external capacitor C_{DUT} to the capacitor in the RC low-pass filter. Otherwise, the delay chain would just draw charge from the low-pass capacitor and the measurement result would not be dependent on the C_{DUT} capacitor.
Furthermore, the charging time needed to charge the capacitors under measure was also increased by adding the additional filter capacitor and the large filter resistance.

The initial design used the *Done* signal from the delay oscillator to generate the next edge for the delay chains. However, by limiting the pulse width with the RC filter, the next edge would be generated to early. Therefore, the *clk* signal $f_{clk} = 1.695\,\text{MHz}$ is used to generate pulses. AND gates were added to control the pulse generation.

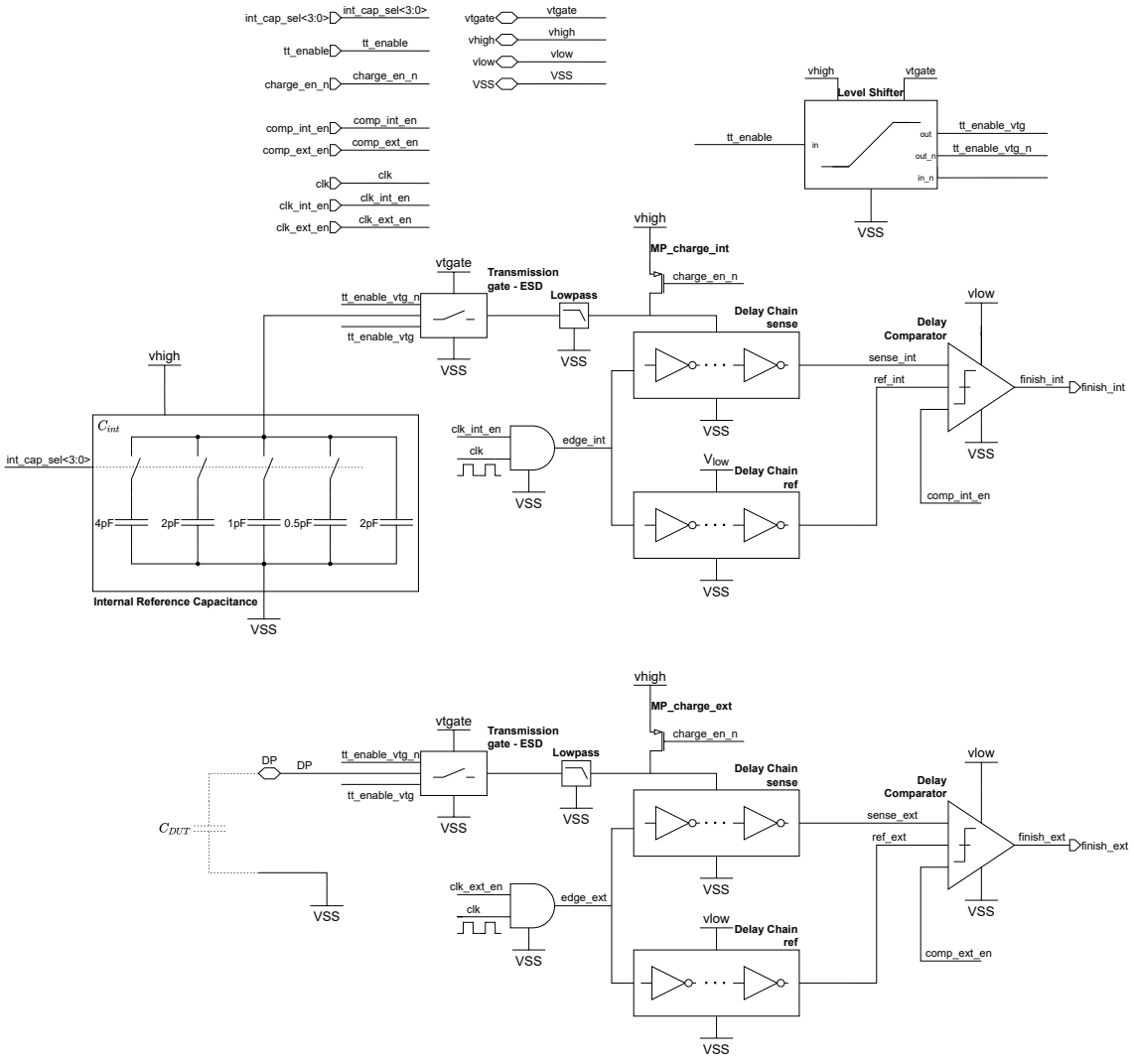

Figure 4.21: Iterative delay chain discharge CTT.

Pin	Use
DP	Detection Pin
VSS	Ground
vlow	Supply voltage for the reference delay-chains, the delay-comparators and the logic AND gate
vhigh	Charging voltage, C_{int} supply voltage and voltage level for all the signals (controlling signals, clock, etc.)
vtgate	Supply voltage for the transmission gates and the higher voltage for the level shifter
int_cap_sel<3 : 0>	Selecting the value of the internal reference Capacitance C_{int}
tt_enable	Enable/disable Tag Tamper -> switch on/off ESD transmission gate
charge_en_n	Enable/disable charging of external and internal Capacitor
comp_int_en	Enable/disable the comparator (internal measurement)
comp_ext_en	Enable / disable the comparator (external measurement)
clk	Clock signal $f_{clk} = 1.695\,\text{MHz}$
clk_int_en	Enable / disable the *clk* signal(internal measurement)
clk_ext_en	Enable / disable the *clk* signal(external measurement)
finish_int	Indicates when the internal measurement is done
finish_ext	Indicates when the external measurement is done

Table 4.12: Pins of the iterative delay chain discharge CTT.

4.2.1 Delay chain

The delay chain is made of eight CMOS inverters. The current consumption of the delay chain, or the charge needed for a rising or a falling edge to pass the delay chain, determines the voltage step at the capacitors C_{DUT} and C_{int}. The current consumption can be increased or reduced by increasing or decreasing the number of inverters in the delay chain. Another way to manipulate the current consumption are the transistor dimensions. The delay is voltage dependent, as shown in Figure 4.23, which makes this measurement possible. However, with the change of the supply voltage, the current consumption also slightly changes which leads to non-constant voltage steps when the voltage on the capacitor decreases from V_{high} to V_{low}. For the requirements of this thesis, there are no additional errors introduced because of these effects, but they should be considered when using this method for different measurements.
The delay chain has also a strong temperature dependence, but in this measurement method, the temperature variation has almost no impact as long as the temperature is the same for each delay chain, which is usually the case. The same is true for process parameters (corners) listed in Table 4.13. The letter "a" at the end of the corner name, in Figure 4.23, indicates that these are alternate corners, which are used to simulate process-only variations. In addition to the alternate corners, functional corners, indicated by the letter "f" at the end of the corner name, were used in section 5.9. Functional corners are aligned with process limits and they include process and mismatch variations. While alternate corners are used to analyze the performance, the functional corners are mainly

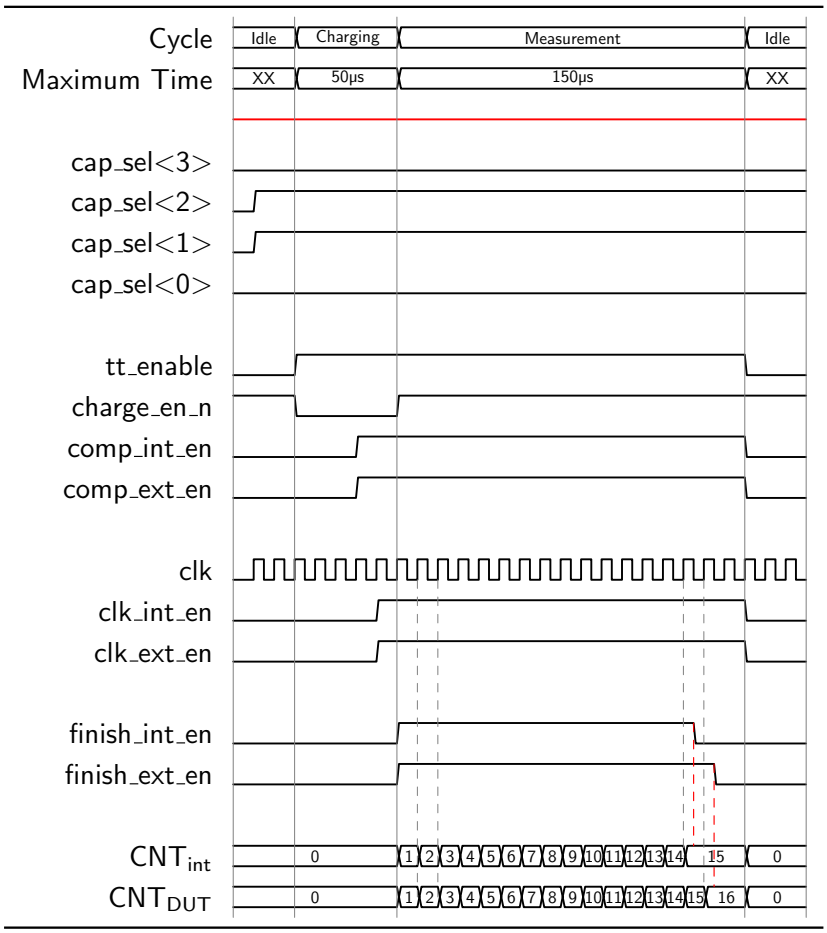

Figure 4.22: Input and output signals of the iterative delay chain discharge CTT.

used to check the robustness of a circuit.
Mismatch could cause variations in measurement, however, this was eliminated by calibration which is realised with the measurement of the internal reference capacitor C_{int}.

Corner	Definition
nom	nominal
fast	fast NMOS, fast PMOS fast passive components (small capacitance and resistance)
ff	fast NMOS, fast PMOS
fs	fast NMOS, slow PMOS
sf	slow NMOS, fast PMOS
ss	slow NMOS, slow PMOS
slow	slow NMOS, slow PMOS, slow passive components (large capacitance and resistance)

Table 4.13: Definition of process corners.

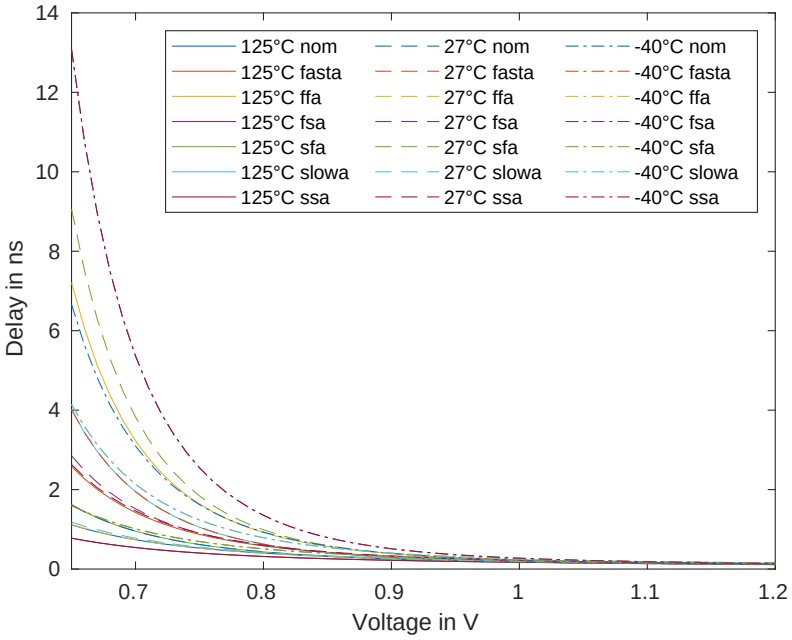

Figure 4.23: Delay of the falling edge over the supply voltage for different temperatures and corners.

4.2.2 Delay comparator

The working principle of this block is described in section 3.1.5. The same schematic as in Figure 3.13 was used, however, the *Done* output was not used for measurement. The pulses are created with the clock signal $f_{clk} = 1.695\,\text{MHz}$ which is much slower than the time needed for the comparator to finish comparing. Therefore, there is no check if the delay comparator is done comparing the signals from the delay chains, before the next edge is generated.

Start-up

The *finish* signal (Y in Figure 3.13) should be *HIGH* at the beginning of the measurement and transition to *LOW* only when the *SENSE* input is slower than the *reference*. Since the delay comparator consists of several logic gates, the values, which the internal nodes adopt during start-up, are not defined. The values depend on temperature and process parameters.
After powering up this block and enabling it by setting *OE* to *HIGH*, the output could be either *HIGH* or *LOW*. In both cases, the output stays *HIGH* or transitions to *HIGH* when the measurement starts and the edges start arriving at the comparator inputs. It is important to detect the $HIGH \rightarrow LOW$ transition of the output only after the measurement has started.

Offset

While determining the offset of the voltage comparator as the one described in section 4.1.1 is straightforward, the offset of the delay comparator must be determined with a transient simulation. The time of the LOW input falling edge t_{LOW} is constant and the time of the *SENSE* falling edge t_{SENSE} is swept. For each t_{SENSE} a transient simulation is done. The minimum falling time $t_{SENSE_{min}}$ at which the output Y transitions from *HIGH* to LOW is then used to calculate the offset in seconds:

$$t_{offset} = t_{SENSE_{min}} - t_{LOW}. \tag{4.11}$$

The delay t_d of the delay comparator can then be calculated in the same simulation with the following equation:

$$t_d = t_{Y_{min}} - t_{SENSE_{min}}. \tag{4.12}$$

Figure 4.24 illustrates the simulation of the delay comparator offset. The t_{SENSE} sweep was done in 10 ps steps. The result of the Monte Carlo simulation for the offset t_{offset}, with global and local mismatch at 27 °C, is depicted in Figure 4.25. Table 4.14 contains the Monte Carlo simulation results of the delay comparator offset t_{offset}. The simulation was performed for 200 points. The offset of the delay comparator can vary a few hundred picoseconds. This variation has no significant impact on measurement results, because it is much smaller compared to the delay variation of the delay chain described in previous section.

mismatch	Temperature	Mean	Std Dev
	°C	ps	ps
global and local	−40	39.85	107.8
	27	39.65	43.36
	125	36.6	21.86
local only	−40	38.1	100.4
	27	38.5	41.86
	125	35.95	21.99

Table 4.14: Monte Carlo simulation results of the delay comparator offset t_{offset}.

4.2.3 Internal reference capacitor C_{int}

The internal reference capacitance consists of five capacitors and four transmission gates as shown in Figure 4.26. The capacitance value can be selected by connecting the capacitors in parallel. The *cap_sel<3:0>* pins are used to enable the transmission gates which connect the capacitors to the *cap* pin.
Table 4.15 contains the possible configurations for this block. A C_{int}, which is the closest to the external capacitor value C_{DUT}, or which results to minimum counter difference $|CNT_{int} - CNT_{DUT}|$, should be chosen to minimize the measurement errors due voltage and temperature variations.

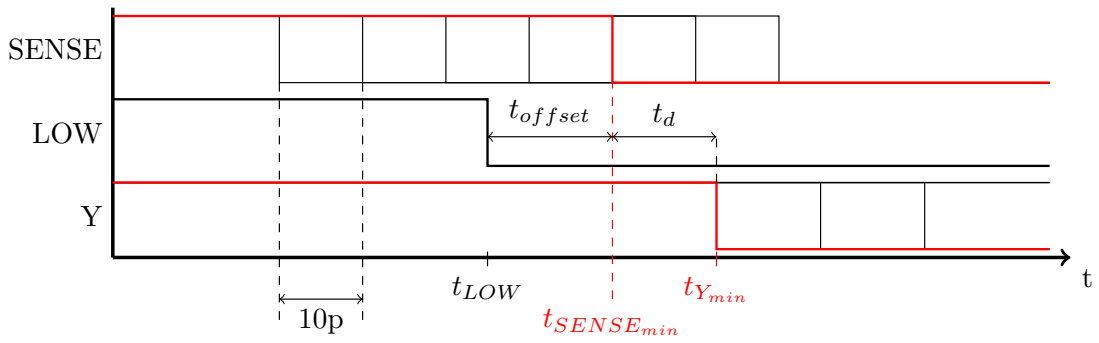

Figure 4.24: Offset simulation of the delay comparator.

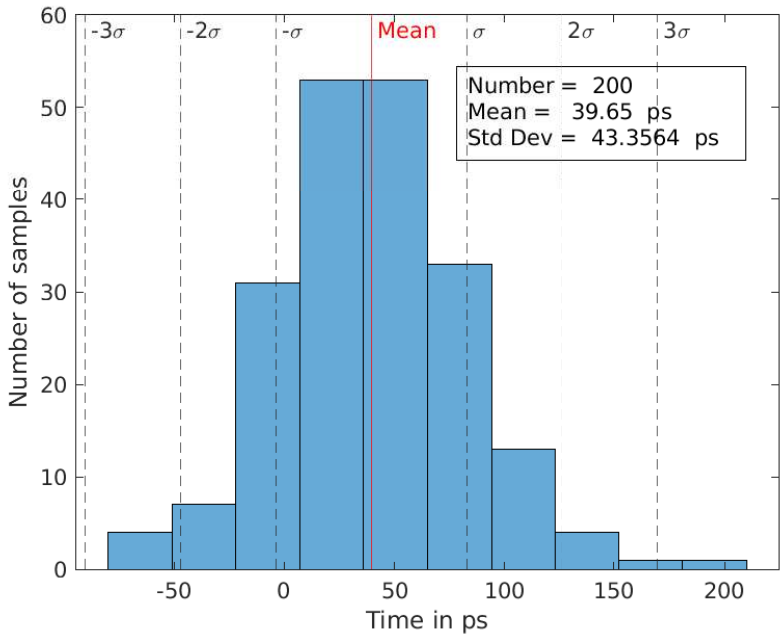

Figure 4.25: Monte Carlo simulation of the delay comparator offset t_{offset} for global and local mismatch at 27 °C.

4.2.4 Low-pass filter

The requirements for the low-pass filter are the same as for the linear slope charging CTT. Therefore, the filter described in section 4.1.6 can be used, with the values in Table 4.16

For the iterative delay chain discharge CTT, a SC low-pass filter was also considered. The idea was to reduce the area by replacing the huge 1 MΩ resistor with a smaller capacitor and two switches as illustrated in Figure 4.27. The resistance of the switched capacitor circuit is defined with the following equation:

$$R = \frac{1}{f_{clk} \cdot C_{SC}} \tag{4.13}$$

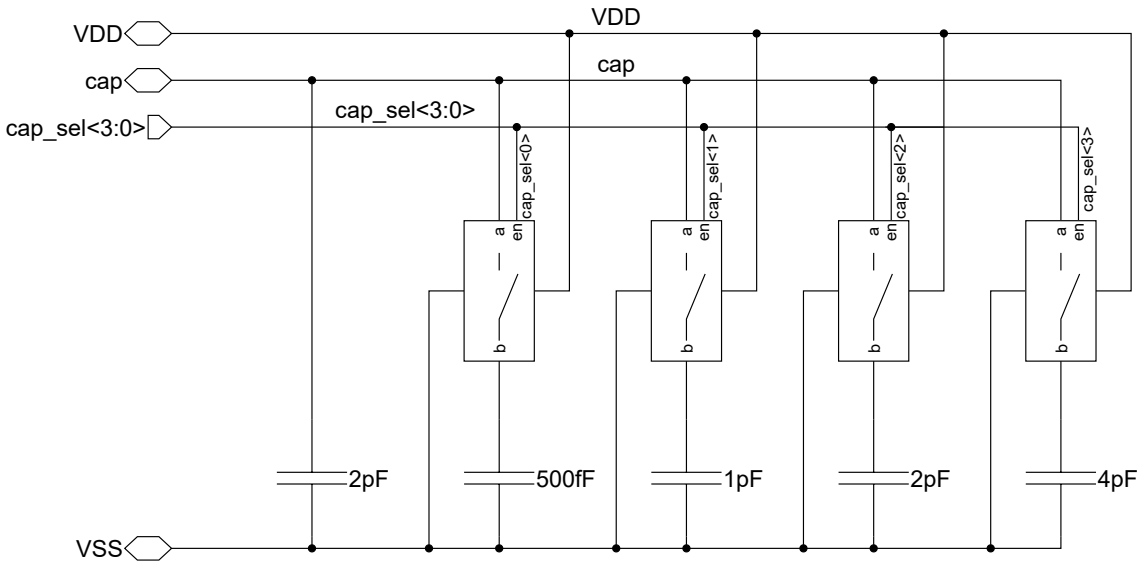

Figure 4.26: Schematic of the variable internal reference capacitor C_{int}.

Nr.	*cap_sel*				C_{int}
	<3>	<2>	<1>	<0>	
	level	level	level	level	pF
1	LOW	LOW	LOW	LOW	2
2	LOW	LOW	LOW	HIGH	2.5
3	LOW	LOW	HIGH	LOW	3
4	LOW	LOW	HIGH	HIGH	3.5
5	LOW	HIGH	LOW	LOW	4
6	LOW	HIGH	LOW	HIGH	4.5
7	LOW	HIGH	HIGH	LOW	5
8	LOW	HIGH	HIGH	HIGH	5.5
9	HIGH	LOW	LOW	LOW	6
10	HIGH	LOW	LOW	HIGH	6.5
11	HIGH	LOW	HIGH	LOW	7
12	HIGH	LOW	HIGH	HIGH	7.5
13	HIGH	HIGH	LOW	LOW	8
14	HIGH	HIGH	LOW	HIGH	8.5
15	HIGH	HIGH	HIGH	LOW	9
16	HIGH	HIGH	HIGH	HIGH	9.5

Table 4.15: Internal reference capacitance C_{int} selection.

Given that the clock frequency is $f_{clk} = 1.695\,\text{MHz}$, by rearranging the previous equation (4.13), the needed capacitance can be calculated:

$$C_{SC} = \frac{1}{f_{clk} \cdot R} = \frac{1}{1.695\,\text{MHz} \cdot 1\,\text{M}\Omega} = 589.97\,\text{fF}. \tag{4.14}$$

R	C	f_c
MΩ	pF	kHz
1	1	159.155

Table 4.16: Selected RC low-pass values.

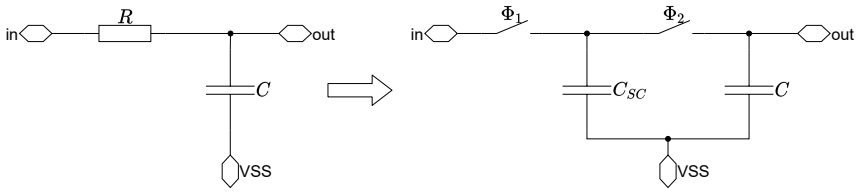

Figure 4.27: RC low-pass filter to SC low-pass filter.

The SC filter has now the same corner frequency as the RC low-pass. But there is also another requirement when using SC filters. The switching frequency f_{clk} should be several times higher than the corner frequency of the signal to avoid aliasing. Since the main disturbance source is the RFID reader with frequency $f_{reader} = 13.56\,\text{MHz}$, which is 8 times higher than the clock frequency, aliasing would not be important because the filter would always sample at exactly the same point after eight periods of the disturbance signal. This theory works but a DC offset is introduced because of the phase delay between the disturbance and the clock signal. This DC offset, introduced by the disturbance and the SC filter, at the supply of the delay chain leads to an error of the counter values. A possible solution to this problem would be to use a very accuracy phase shift of the clock signal. This solution was not suitable for this project.

Regarding the problems that come with the use of an SC filter, it was decided that a conventional RC filter, as described in linear slope charging CTT, is the better option despite the area.

4.2.5 Transmission gates

The transmission gate ESD used in this CTT is the same as the the one described in section 4.1.8. It's purpose is to be able to disconnect the CTT block from the detection pin (DP). Another transmission gate ESD was added to the internal measurement path for symmetry.

Another transmission gate is used in the C_{int} block. The circuit is the same as for the transmission gate ESD with additional inverter to generate the negative controlling signal for PMOS. Furthermore, the transistors used in this transmission gate are not ESD, but GO2 devices.

4.2.6 Layout

The layout of the iterative delay chain discharge CTT is depicted in Figure 4.28. It is clearly visible that the capacitors of the trimmable internal reference capacitance block C_{int}, cover a large portion of the CTT area. A dummy capacitor was added in the upper

left corner to fill the empty space in the rectangle constructed of capacitors from the C_{int} block.

The size of this CTT block is x x y = 94.05 µm x 102.93 µm, which results to an area A:

$$A = x \cdot y = 94.05\,\mu m \cdot 102.93\,\mu m = 9681\,\mu m^2 = 0.009681\,mm^2 \tag{4.15}$$

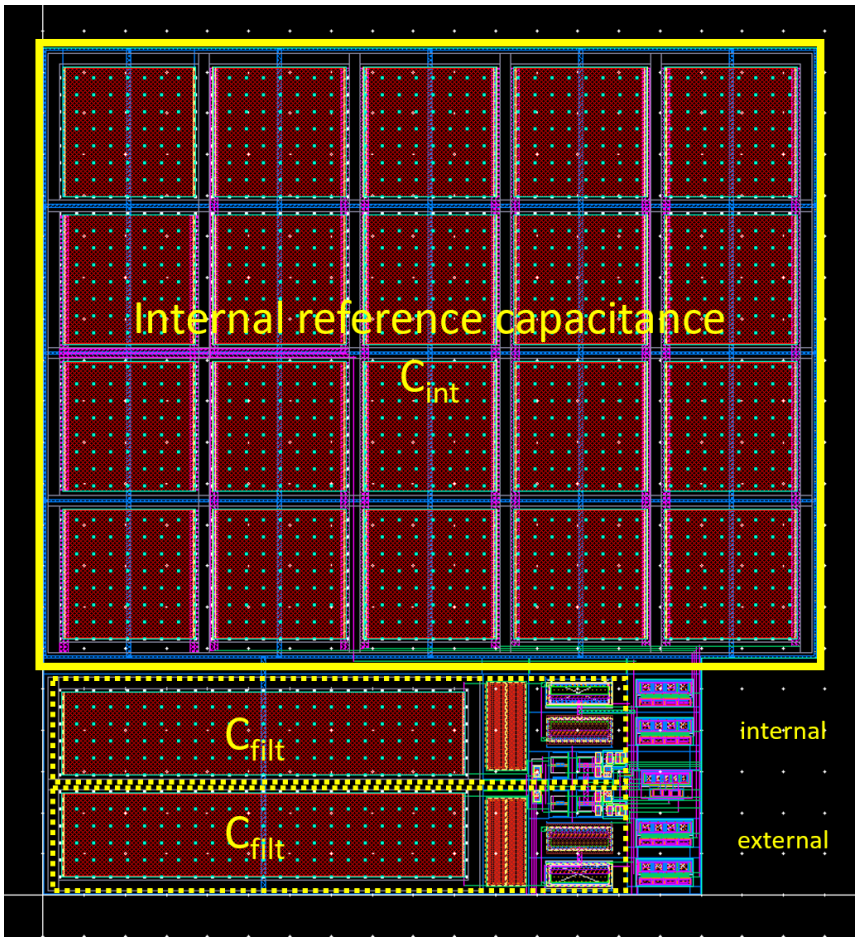

Figure 4.28: Layout of the iterative delay chain discharge CTT.

The components of the external and internal measurement path are shown in Figure 4.29. The labels in the figure are explained in Table 4.17.

4.2.7 Double range

In this iterative delay chain discharge CTT, the possibility to switch between normal measurement range and the double range (Table 1.1) was not implemented.
This feature can be realized by adding an additional input pin that would enable the double range, similar to linear slope charging CTT in section 4.1. The possibility to expand the measurement range, while the measurement time stays the same, can be implemented by modifying the delay chain and therefore, increasing its current (charge) consumption.

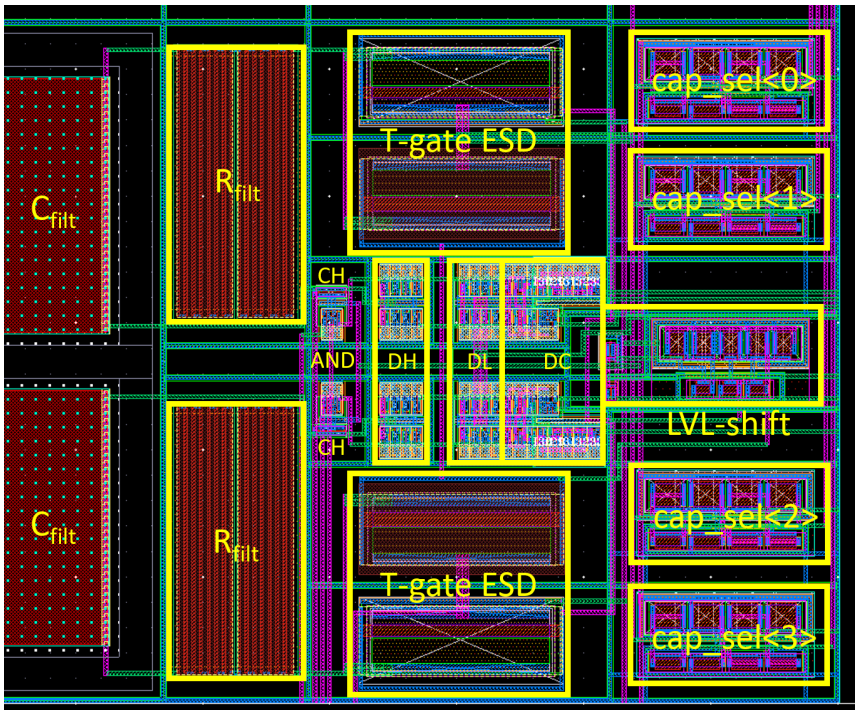

Figure 4.29: Layout of the internal and external measurement path of the iterative delay chain discharge CTT.

Label	Component
C_{int}	Internal reference capacitance C_{int}
C_{filt}	Capacitor of the RC low-pass filter
R_{filt}	Resistor of the RC low-pass filter
T-gate ESD	Transmission gate - ESD
cap_sel$< 3:0 >$	Transmission gates of the C_{int} block with GO2 transistors
DC	Delay comparator
DH	Delay Chain - sense
DL	Delay Chain - ref
AND	AND gates for enabling the clock signal *clk*
CH	MP_charge PMOS for charging the capacitors

Table 4.17: Layout labels.

Additional inverters can be added to the delay chain which would be active when the double range is enabled, and bypassed otherwise. Another way to increase the charge consumption of the delay chain is to add the capacitors at the inverter outputs. Every inverter would then have a switch at the output that can connect or disconnect the capacitor.

4.2.8 RTT implementation

The RTT, described in section 3.2, can be implemented in this iterative delay chain discharge block. This can be realized by adding a current source and a voltage comparator. To compare the voltage V_{DUT} on the wire loop, a reference voltage or the lower supply voltage *vlow* can be used. When using the lower supply voltage, the comparator should be supplied with a higher voltage *vhigh*.
The output of the current source should be connected between the transmission gate and the low-pass filter. The positive input of the comparator is the supply of the **sense** delay chain, and the negative a reference voltage.
The measurement current I_{meas} should be chosen regarding the requirements, as described in section 4.1.11.

Chapter 5

Verification results

In the previous chapter the implementations of the iterative delay chain discharge CTT and the linear slope charging CTT were presented. Each block was described separately. The layout of the iterative delay chain discharge CTT was also introduced.

This chapter focuses on simulation results of the two CTTs. For the verification, an extracted netlist was used. This netlist contains parasitic capacitances that are extracted from the layout implementation.

The simulations include accuracy, temperature behaviour, current consumption and influence of disturbance. During the simulations, it was observed that the layout could be improved to preserve the behaviour obtained by the schematic simulation. The layout change is presented. The simulation results of the double range feature, implemented in linear slope charging CTT, are also included in this chapter.

All simulations were performed with a calibration for $C_{DUT} = 3.5\,\text{pF}$, except for the double range measurement which was calibrated for $C_{DUT} = 7\,\text{pF}$.

5.1 Simulation test benches

The implemented CTTs were simulated to evaluate the transient behaviour. All the voltages in the test benches were provided with ideal voltage sources. The input currents for the linear slope charging CTT come from one ideal current source $I = 250\,\text{nA}$ and are set to the desired value by current mirrors. Verilog-A models were used to provide the controlling signals for the CTTs.

5.2 Accuracy

To determine the accuracy, a transient simulation was performed over the whole measurement range $C_{range} = 2...5\,\text{pF}$ in $250\,\text{fF}$ steps. The measurement was calibrated for capacitance $C_{DUT} = 3.5\,\text{pF}$.
During this simulation, it was observed that the iterative delay chain discharge CTT with extracted parasitic capacitances from the layout, described in section 4.2.6, differs from

the schematic regarding the accuracy. This issue was investigated and the problem, as well as the solution are described in section 5.4. To observe the difference, both the extracted schematics with parasitic capacitances of the initial layout (Extracted) and the fixed layout (Extracted - fixed) were simulated in this section. All the following simulations contain only the fixed layout.
Table 5.1 holds the difference between the counter values of the external and internal measurement path with the calibration value subtracted.

$$\text{Result} = CNT_{ext} - CNT_{int} - CALIB \tag{5.1}$$

Figure 5.1 shows the calculated *Result* for different implementations. The slopes of these curves were chosen to achieve maximum accuracy for the given specifications. It can be observed that the linear slope charging has a higher slope and therefore, a higher accuracy than the iterative delay chain discharge CTT. This slope can be decreased by decreasing the reference voltages or using a slower clock signal for measuring the charging time. The slope of the iterative delay chain discharge CTT can be increased only by decreasing the charge consumption of the delay chains. However, this would result to an increase of the measurement time.

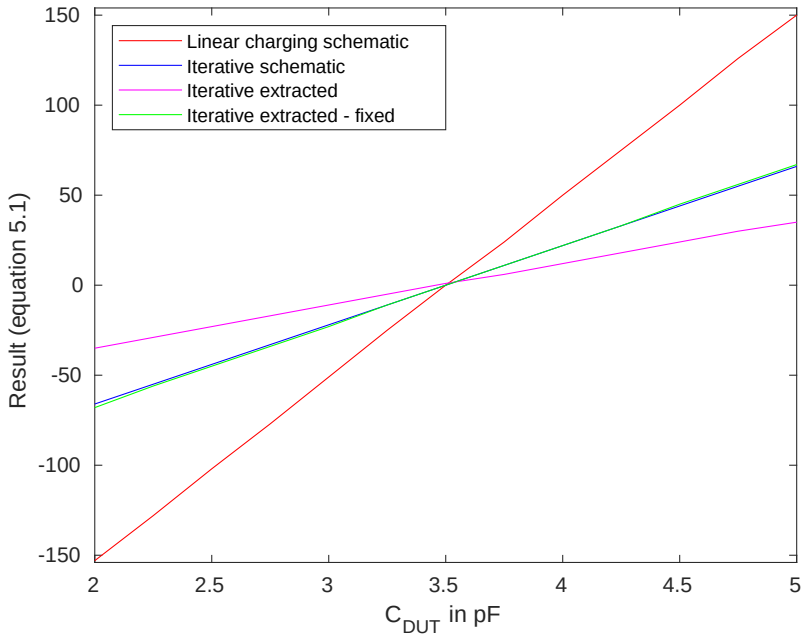

Figure 5.1: Capacitance measurement calibrated for $C_{DUT} = 3.5\,\text{pF}$.

The accuracy was then calculated by dividing the capacitance step size ΔC_{DUT} with the minimum difference of the results $\Delta Result_{min}$ between two adjacent values for C_{DUT}.

$$C_{accuracy} = \frac{\Delta C_{DUT}}{\Delta Result_{min}} \tag{5.2}$$

C_{DUT}	Linear Slope Charging	Iterative Delay-Chain Discharge		
pF	Schematic	Schematic	Extracted	Extracted - fixed
2	−153	−66	−35	−68
2.25	−128	−55	−29	−56
2.5	−102	−44	−23	−45
2.75	−77	−33	−17	−34
3	−51	−22	−11	−23
3.25	−25	−11	−5	−11
3.5	0	0	1	0
3.75	24	11	6	11
4	50	22	12	22
4.25	75	33	18	33
4.5	100	44	24	45
4.75	126	55	30	56
5	150	66	35	67

Table 5.1: Capacitance measurement calibrated for $C_{DUT} = 3.5\,\text{pF}$.

The calculated measurement accuracy $C_{accuracy}$, for the implemented CTTs, can be found in Table 5.2.

-	Linear Slope Charging	Iterative Delay-Chain Discharge		
	Schematic	Schematic	Extracted	Extracted - fixed
$C_{accuracy}$	10.417 fF	22.73 fF	50 fF	22.73 fF

Table 5.2: Determined measurement accuracy $C_{accuracy}$.

5.3 Double range

In linear slope charging block, a double range feature was implemented which changes the measurement range to $C_{range\_dbl} = 4...10\,\text{pF}$. The double range is enabled by setting the *tt_ double_ range_ i* pin to *HIGH* which doubles the charging current for the external capacitor. The simulation result for different temperatures is depicted in Figure 5.2. The measurement was calibrated for a capacitance $C_{DUT} = 7\,\text{pF}$ and a sweep of the C_{DUT} capacitance in 500 fF steps was performed over the measurement range.

5.4 Iterative delay chain discharge CTT layout change

The layout of the iterative delay chain discharge CTT, presented in section 4.2.6, was proven to have less accuracy than the schematic during the simulation with extracted parasitic capacitances in the previous section.

The voltages at the sense delay chain, for the schematic, the extracted netlist of the layout and the fixed layout, are show in Figure 5.3. There are two differences between the schematic and the extracted netlist of the initial layout.

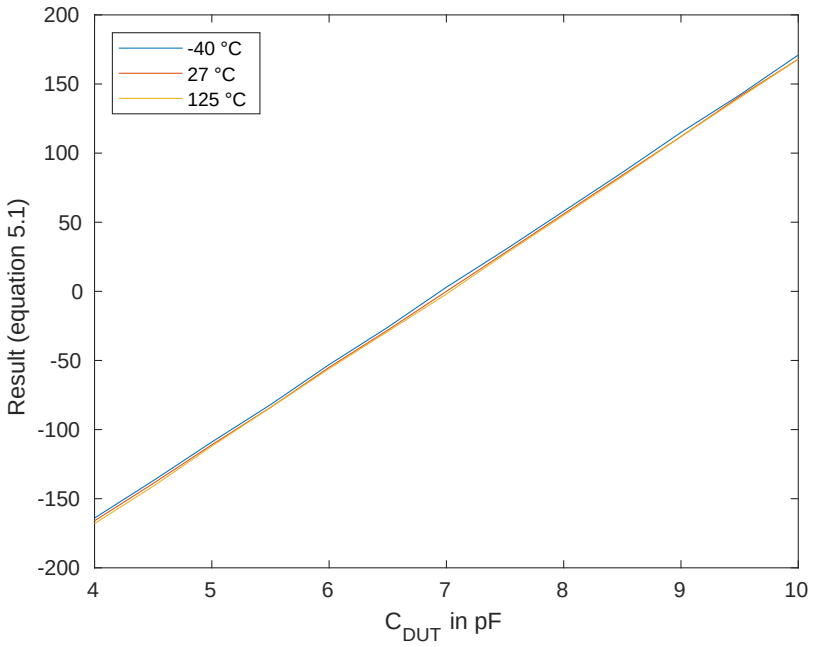

Figure 5.2: Double range capacitance measurement with different temperatures, calibrated for $C_{DUT} = 7\,\text{pF}$.

The first one is the slope. The voltage decreases much faster because of the larger voltage step in the extracted simulation than in the schematic. This happens due to parasitic capacitances in the delay chain block. The voltage step can be decreased by decreasing the charge consumption, which can be realized by removing a few inverters from the delay chain block.
The second difference, which has less impact on the result, is that the measurement finishes at voltage higher than the chosen $V_{low} = 0.75\,\text{V}$. The measurement is done when the delay of the sense delay chain is larger than the delay of the reference delay chain. Usually, this happens when the supply voltage of the sense delay chain reaches the supply voltage at the reference delay chain, which can be observed in the schematic simulation. However, in the layout, the sense delay chain is further away from the delay comparator than the reference delay chain. This results to an additional delay due to parasitic capacitance of the metal line that connects the output of the delay chain with the delay comparator. This can be fixed by connecting both, the sense and the reference delay chain, with the delay comparator using the same layer, same distance and the same surroundings.

The performance of the CTT was improved by minor changes in layout. Figure 5.4 shows the new layout of the sense and the reference delay chain for the internal and the external measurement. Four inverters of each delay chain were removed to decrease the charge consumption and therefore, to improve accuracy. Instead of eight inverters in the initial layout (Figure 4.29), each delay chain is now formed out of four inverters. This results to the same simulated accuracy as with the schematic netlist. In the following sections, only the extracted netlist of the new layout was simulated.

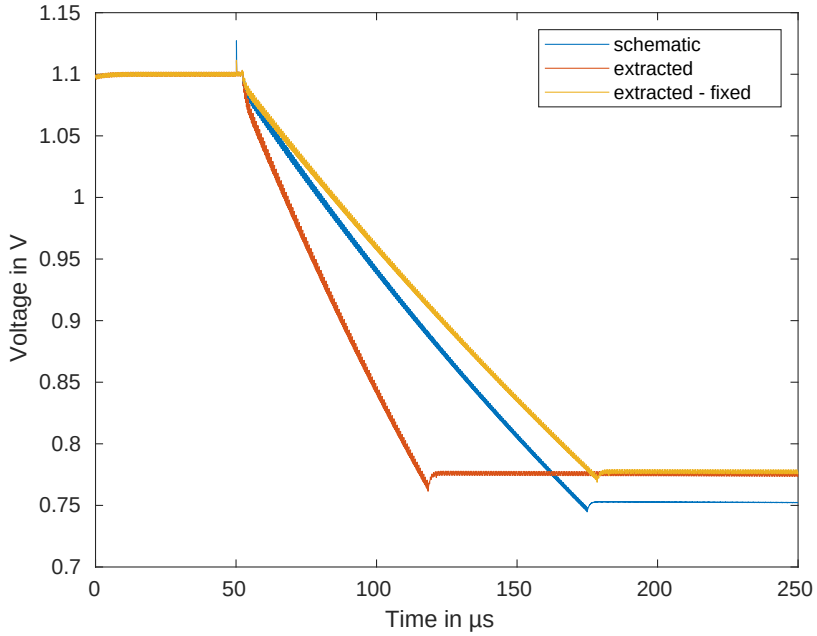

Figure 5.3: Voltage at the supply of the sense delay chain for different netlists.

To reduce the difference regarding the delay between the sense and reference delay chain would result in additional layout changes. Since the wanted accuracy was reached, the arrangement of the initial layout, where the distances between the delay chains and the delay comparator are not equal, was not changed. Furthermore, the circuit implementation for the external and the internal measurement is the same. Both measurements have the same offset and therefore, the difference between the two counter values is not affected.

5.5 Measurement time

The measurement time of the linear slope charging CTT depends on the chosen charging current which defines the charging slope. The current can be selected by the user. It is recommended to selected the current so that the internal and the external measurement have the same charging slopes. Therefore the measurement of the internal reference capacitance C_{int} is used to define the measurement time of this CTT.
The measured capacitance defines the measurement time of the iterative delay chain discharge CTT. Larger capacitances need more time to be discharged and therefore the measurement time increases with the capacitance C_{DUT}. Since the measurement range is defined as $C_{range} = 2...5\,\text{pF}$, the capacitance $C_{DUT} = 5\,\text{pF}$ is used to determine the measurement time of this CTT. The measurement time includes the charging time which is set to $t_{charge} = 50\,\mu\text{s}$.

Table 5.3 contains the measurement times for the implemented CTTs. All implementations fulfill the requirements regarding measurement time specified in Table 1.1. Linear slope charging CTT has the fastet measurement, however, the measurement time could increase

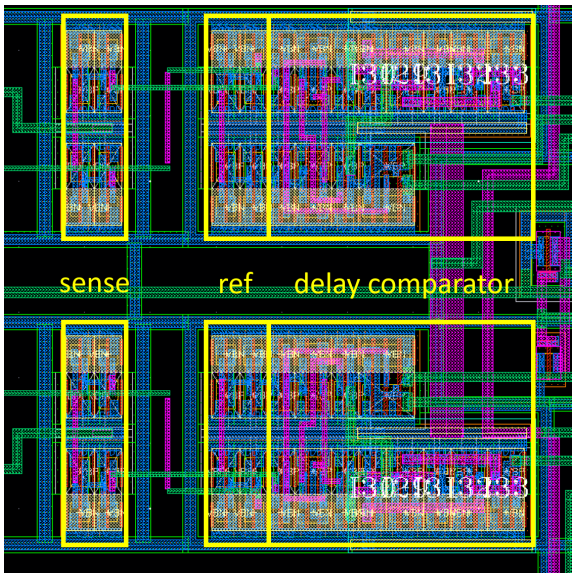

Figure 5.4: New layout of the sense and the reference delay chain.

if the chosen charging current is too low for the measured external capacitance C_{DUT}.

-	Linear Slope Charging	Iterative Delay-Chain Discharge	
	Schematic	Schematic	Extracted
Measurement time	186 µs	214 µs	218 µs

Table 5.3: Measurement time.

5.6 Temperature behaviour

The simulation was performed for three different temperature values (−40, 27 and 125 °C). There is almost no change in the results obtained by the linear charging slope CTT as showed in Figure 5.5. The simulation results for the iterative delay chain discharge CTT are depicted in Figure 5.6. The temperature has less impact on the result for capacitances which values are close to the capacitance value used for calibration. The temperature behaviour is improved in the extracted netlist simulation.

5.7 Current consumption

The current consumption of the linear slope charging CTT depends on the chosen charging current set in the trimmable current mirror block and the chosen filter capacitance. To get the maximum current consumption, the highest current and the largest capacitance was chosen.
The current consumption of the iterative delay chain discharge CTT depends on the measured capacitance C_{DUT} and the reference capacitance C_{int}. Both capacitances were set to 5 pF to obtain the maximum current consumption.

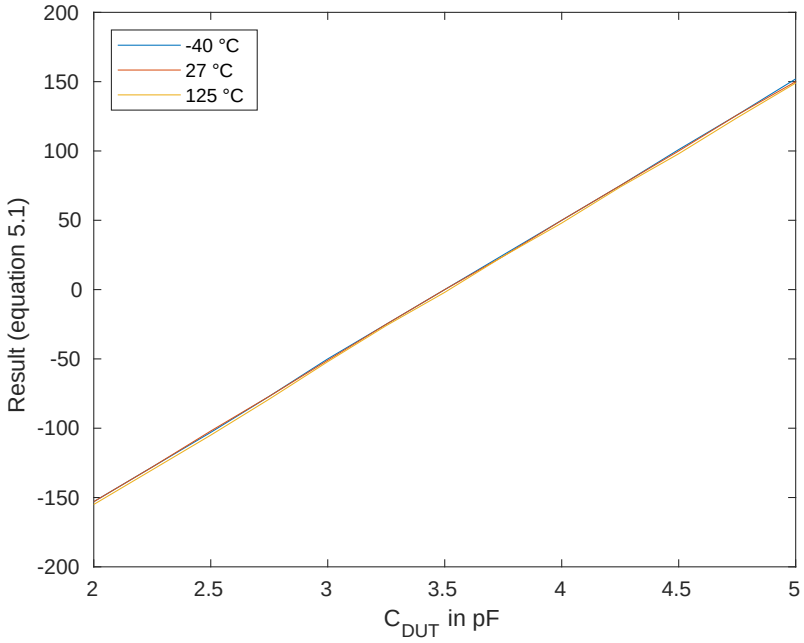

Figure 5.5: Capacitance measurement with the linear charge slope CTT for different temperatures.

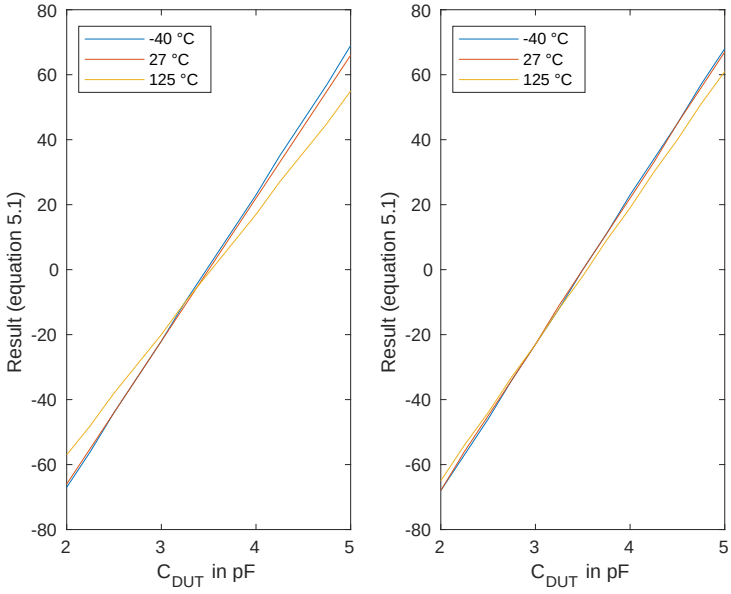

Figure 5.6: Capacitance measurement with the iterative delay chain discharge CTT schematic (left) and extracted netlist (right) for different temperatures.

The current consumption was determined by taking the average value of the current flowing

into the supply pins during the measurement. For the iterative delay chain discharge CTT, the current during charging was also taken into calculation. Table 5.4 contains the current consumption for the two CTTs. The extracted netlist of the iterative delay chain discharge CTT has a slightly higher current consumption than the schematic, due to extracted parasitic capacitances. Furthermore, the current consumption of the linear slope charging CTT is much higher, but still under the specified maximum value of 3 µA (Table 1.1).

-	Linear Slope Charging	Iterative Delay-Chain Discharge	
	Schematic	Schematic	Extracted
Current consumption	1.715 uA	65.898 nA	81.912 nA

Table 5.4: Current consumption.

5.8 Disturbance

For disturbance simulation, the model described in section 2.2.1 was used. The simulation parameters correspond to the values listed in Table 2.2.

The measurement results for the linear slope charging CTT with and without disturbance are depicted in Figure 5.7. Although the variable filter capacitance was set to its maximum value $C = 3\,\text{pF}$, it can be observed that the disturbance has an impact on the measurement for lower capacitances $C_{DUT} < 4\,\text{pF}$. At lower capacitances, some results are wrong and others are missing due to simulation errors.
The reason for these errors is the higher disturbance for lower capacitances, which causes too high voltages at trimmable current mirror output. At some point, the capacitance C_{DUT} is no longer charged and it never reaches the highest reference voltage $V_{ref2} = 900\,\text{mV}$. The voltages with ($V_{reader} = 50\,\text{V}$) and without ($V_{reader} = 0\,\text{V}$) disturbance are shown in Figure 5.8.

The disturbance induced by the reader has little impact on the iterative delay chain discharge CTT as shown in Figure 5.9. With the maximum result difference of 2 for schematic and 3 for the extracted netlist, the accuracy is still high enough.

5.9 Process and mismatch variations

Both CTT implementations, as well as the extracted netlist of the iterative delay chain discharge, were simulated over various process variations (corners) listed in Table 4.13 and described in section 4.2.1. Furthermore, a Monte Carlo simulation was performed to ensure proper functionality of the CTT blocks even with mismatch. Monte Carlo simulations were conducted with 200 runs for global and local mismatch, as well as with 200 runs for local mismatch only. Global mismatch is the variation of devices from wafer to wafer, while local mismatch is the variation of devices within one wafer.
All of the Monte Carlo simulations were performed at nominal temperature (27 °C).

Figure 5.10 and Figure 5.11 depict the process variation (corners) simulation results for the linear slope charging CTT and the iterative delay chain discharge CTT. It can be observed that, due to calibration, the process variations have very little impact on the final results.

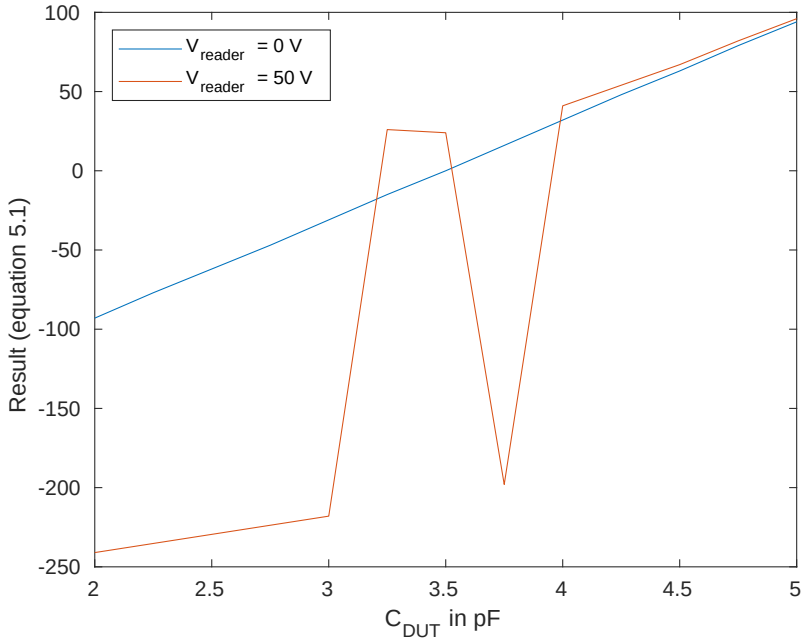

Figure 5.7: Capacitance measurement with the linear slope charging CTT with ($V_{reader} = 50\,\mathrm{V}$) and without disturbance ($V_{reader} = 0\,\mathrm{V}$).

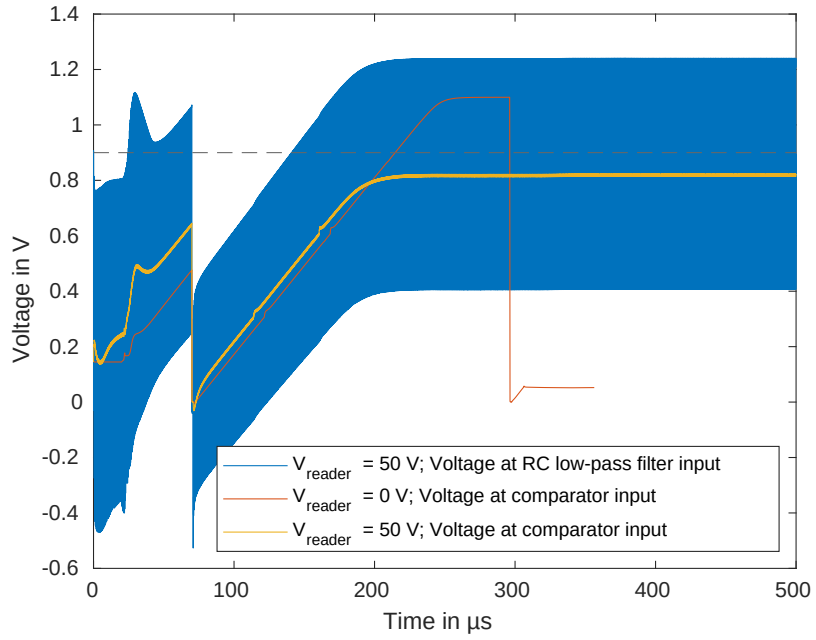

Figure 5.8: Voltages during capacitance $C_{DUT} = 2\,\mathrm{pF}$ measurement with the linear slope charging CTT with ($V_{reader} = 50\,\mathrm{V}$) and without disturbance ($V_{reader} = 0\,\mathrm{V}$).

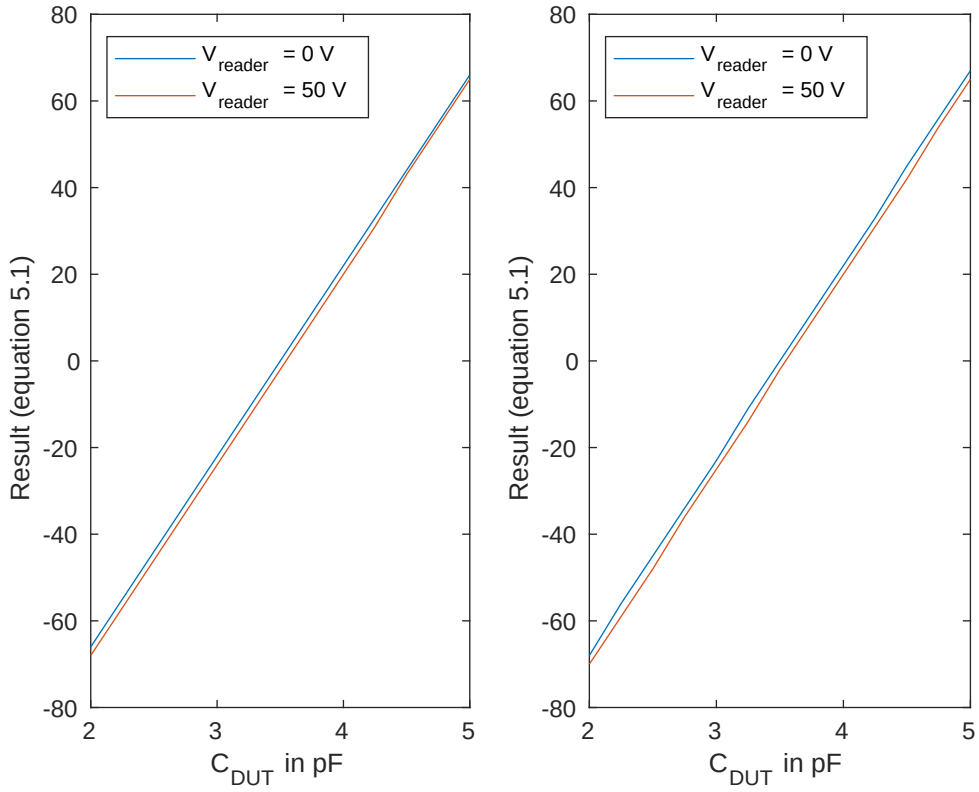

Figure 5.9: Capacitance measurement with the iterative delay chain discharge CTT schematic (left) and extracted netlist (right) for with ($V_{reader} = 50\,\mathrm{V}$) and without disturbance ($V_{reader} = 0\,\mathrm{V}$).

The results for the Monte Carlo simulations are listed in Tables 5.5, 5.6 and 5.7. The simulation was performed for capacitances $C_{DUT} = 3\,\mathrm{pF}$ and $C_{DUT} = 4\,\mathrm{pF}$. The results were calibrated for a capacitance $C_{DUT} = 3.5\,\mathrm{pF}$. Even with the mismatch variation, the accuracy $C_{accuracy\_MC}$ is still higher than the required accuracy $C_{accuracy} = 250\,\mathrm{fF}$.

$$C_{accuracy\_MC} = \frac{\Delta C_{DUT}}{\Delta Result_{min}}. \tag{5.3}$$

The iterative delay chain discharge CTT with extracted parasitic capacitances has a minimum result difference $\Delta Result_{min} = 14$ at $\Delta C_{DUT} = 500\,\mathrm{fF}$. This would result to an accuracy of $C_{accuracy\_MC} = 35.714\mathrm{fF}$ (5.3).

5.10 Comparison with specifications

Table 5.8 shows the comparison of the implemented capacitive tag tamper circuits with the defined specifications. These values may vary with the process and mismatch variations. However, even with these variations, the requirements are fulfilled over a wide temperature range (from $-40\,^{\circ}\mathrm{C}$ to $125\,^{\circ}\mathrm{C}$).

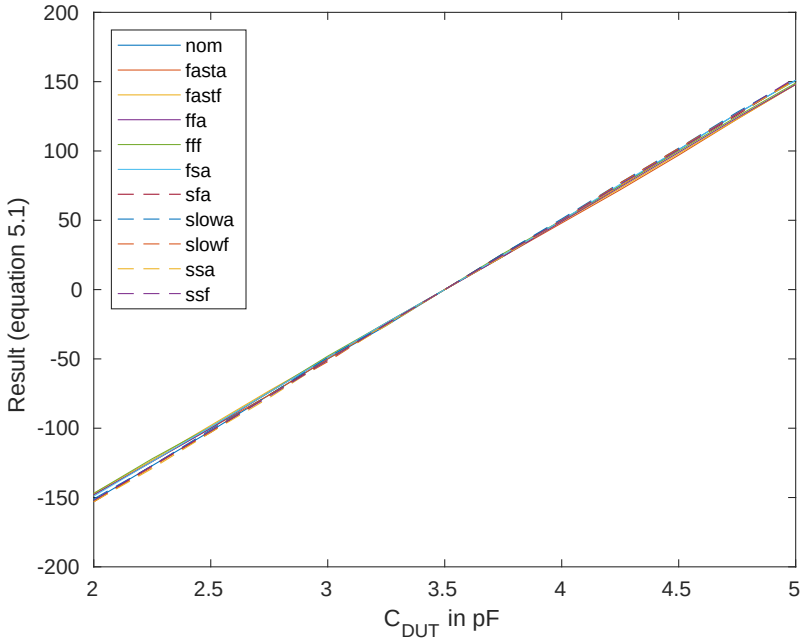

Figure 5.10: Capacitance measurement with the linear slope charging CTT for process variations (corners).

mismatch	C_{DUT} pF	Linear slope charging - schematic Min	Max	Mean	Std Dev
global and local	3	−53	−47	−50.54	1.177
	4	48	53	50.14	1.032
local only	3	−53	−46	−50.425	1.184
	4	47	53	50.16	1.149

Table 5.5: Monte Carlo simulation results of the linear slope charging CTT capacitance measurement.

mismatch	C_{DUT} pF	Iterative delay chain discharge - schematic Min	Max	Mean	Std Dev
global and local	3	−25	−19	−22.1	1.236
	4	19	25	22	1.341
local only	3	−25	−19	−22.115	1.126
	4	19	25	22.085	1.097

Table 5.6: Monte Carlo simulation results of the iterative delay chain discharge CTT (schematic) capacitance measurement.

The implemented CTTs were simulated for the specified measurement range $C_{range} = 2...5\,\text{pF}$. The possibility to double the measurement range $C_{range\_dbl} = 4...10\,\text{pF}$ was implemented only in linear slope charging CTT.

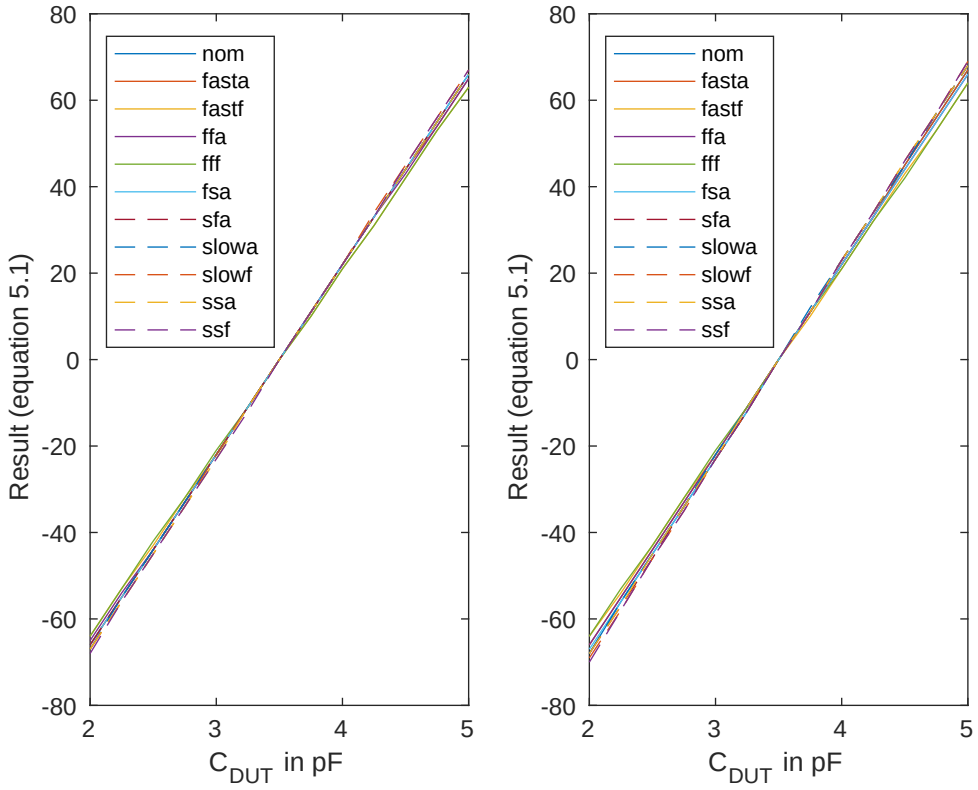

Figure 5.11: Capacitance measurement with the iterative delay chain discharge CTT schematic (left) and extracted netlist (right) for process variations (corners).

mismatch	C_{DUT} pF	Iterative delay chain discharge - extracted Min	Max	Mean	Std Dev
global and local	3	−27	−14	−22.455	1.896
	4	15	28	22.455	1.984
local only	3	−27	−15	−22.43	2.144
	4	15	27	22.425	2.163

Table 5.7: Monte Carlo simulation results of the iterative delay chain discharge CTT (extracted) capacitance measurement.

Specifications		Linear Charging Schematic	Iterative Discharge Schematic	Extracted
$C_{accuracy}$	250 fF	10.417 fF	22.73 fF	22.73 fF
Measurement time	220 µs	186 µs	214 µs	218 µs
Current consumption	3 µA	1.715 µA	65.898 nA	81.912 nA
Area	34000 µm^2	-	9681 µm^2	9681 µm^2

Table 5.8: Defined specifications and the simulation results.

Chapter 6

Conclusion and future work

6.1 Conclusion

This thesis investigates various different capacitance sensing methods for the tag tamper block of an RFID transponder IC. Because of the simple requirements for the resistive sensing circuit, only one method was presented. The capacitance sensing methods are compared regarding the accuracy, area, current consumption and temperature dependence.

The linear slope charging and the iterative delay chain discharge sensing methods were implemented as a CTT block in a 40nm CMOS technology. Both measurements run at a supply voltage of $VDD = 1.1\,\mathrm{V}$. Furthermore, the requirements for measurement time and accuracy are met. The accuracy is also reached over process and temperature variations. The linear slope charging CTT shows better performance regarding temperature variations and has higher accuracy over the whole measurement range. The iterative delay chain discharge CTT has lower accuracy and the temperature variations decrease the accuracy when the value of the measured capacitance C_{DUT} differs from the capacitance value used for calibration.
While the disturbance induced by the reader antenna has little influence on the iterative delay chain discharge CTT, it causes measurement errors in the linear slope charging CTT.

The layout of the iterative delay chain discharge CTT has been implemented and verified. The initial layout has been modified in order to obtain results similar to the ones obtained by schematic simulation.
To implement the layout of the linear slope charging would be more time consuming regarding the number of analog blocks that are used in this design. Therefore, this was not realized in this thesis.

The measurement time of the simulated CTTs depends on measured capacitances and the trimming values for the charging current in one CTT or the internal reference capacitance in the other. The linear slope charging CTT is slightly faster than the iterative delay chain

discharge CTT. However, the notable difference between the two implemented CTTs is the current consumption. The current consumption of the iterative delay chain discharge CTT is roughly twenty times lower than that of the linear slope charging CTT. This could be a crucial point when choosing between the two implementations. Furthermore, the linear slope charging CTT uses a higher frequency to quantize the time. This results in a higher current consumption in the digital processing part.

The implemented capacitive tag tamper blocks show very good performance regarding temperature variations, current consumption and process variations. Both CTTs, as well as the extracted netlist, fulfill all the requirements.

6.2 Future work

The implementation of the layout of the linear slope charging CTT is planned. The performance of this CTT has to be verified and compared with the iterative delay chain discharge CTT. The areas of the two CTTs should be compared.

The linear slope charging CTT requires further investigation regarding measurement errors due to induced disturbance. The possible solutions, which include adding an additional low-pass filter, between the detection pin and the trimmable current mirror block, or decreasing the three reference voltages V_{ref0}, V_{ref1} and V_{ref2}, need to be investigated and compared.

The iterative delay chain discharge CTT lacks the double range feature. The measurement range increase is possible only by increasing the measurement time. Extending the measurement range by connecting additional capacitors to the output of the inverters is planned.

At this point, it is not known if the IC would have other uses for this detection pin (DP) used by CTT. Furthermore, the ESD structures that will be placed at the pin, are not yet defined. A leakage current, flowing through additional components connected to DP could discharge the capacitor C_{DUT} and alter the results. It is necessary to simulate the influence of the leakage current and eventually add a leakage current compensation circuit.

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