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EMI Analysis and Reduction of Inverting Buck/Boost Converters

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Affidavit

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Abstract

Switched-mode power supplies are widely used in many electrical systems. Due to their high switching frequency and the high di/dt and dv/dt values, they generate electrical noise. In this thesis the inverting buck/boost converter is investigated, and two aspects are treated: EMI-analysis and IC design.

The inverting buck/boost type differs from other converters such as the non-inverting boost or buck converters, in that the inductor is connected to the ground, i.e. neither input, nor output is isolated from an EMC perspective. A SPICE model is developed here for analyzing the EMC properties of the circuit. Two EMI-relevant resonances are observed depending on the state of the switch. The simulations are confirmed by measurements using a circuit designed from discrete components. Further, integrated commercially available converters have been analyzed and show EMC properties similar to the general model.

A design model of an integrated inverting buck/boost converter is provided by Dialog Semiconductor. EMI-reducing measures are applied to this model and simulation results are presented. EMI reduction is achieved by designing a programmable slew rate gate driver. The driver settings allow EMI reduction up to 20 dB, but at the cost of efficiency.

Kurzfassung

Schaltnetzteile sind in elektrischen Systemen weit verbreitet. Aufgrund der hohen Schaltfrequenzen und der hohen di/dt und dv/dt Werte erzeugen sie elektromagnetische Störungen. In dieser Arbeit wird der invertierende Buck/Boost-Wandler untersucht und zwei Aspekte behandelt: EMI-Analyse und IC Design.

Der invertierende Buck/Boost-Wandler unterscheidet sich von anderen Wandlern, wie den nicht invertierenden Buck- oder Boost-Wandlern darin, dass die Spule mit Masse verbunden ist. Das bedeutet weder Eingang noch Ausgang der Schaltung ist aus EMV-Sicht isoliert. Für die Analyse der EMV-Eigenschaften der Schaltung wird ein SPICE-Modell entwickelt. Je nach Zustand des Schalters werden zwei EMV-relevante Resonanzen beobachtet. Die Erkentnisse aus den Simulationen werden durch Messungen an einer aus diskreten Bauteilen aufgebauten Schaltung bestätigt. Weiters werden kommerziell erhältliche Wandler analysiert. Diese zeigen ähnliche EMV-Eigenschaften, wie sie bereits anhand des einfachen SPICE-Modells festgestellt wurden.

Ein Simulationsmodel von einem integrierten invertierenden Buck/Boost-Wandler wird von Dialog Semiconductor zur Verfügung gestellt. An diesem Modell werden EMI-reduzierende Maßnahmen angewandt und die Simulationsergebnisse präsentiert. Die Reduzierung von elektromagnetischen Störungen wird mit einem Gate-Treiber erreicht, der es ermöglicht, die Anstiegs- und Abfallzeit am Schaltknoten zu programmieren. Die Einstellungen am Gate-Treiber ermöglichen eine Reduzierung der Störungen um bis zu 20 dB, allerdings auf Kosten des Wirkungsgrades.

Contents

Chapter 1

Introduction

1.1 Motivation

Switched-mode power supplies (SMPS) are widely used in many electrical systems. Due to their high power efficiency, small size, and accurate regulation ability, they are very popular. However, from the electromagnetic interference (EMI) point of view, they also have some drawbacks. Switched DC-DC converters consist of one or several switches, a coil, and/or capacitors. Due to the fast switching, high values of di/dt and/or dv/dt are developed, which can excite resonances in loops and high electromagnetic emissions. The increasing complexity of electronic systems, lead to strong susceptibility to electromagnetic interference. To protect other electrical components in the system, these electromagnetic emissions have to be reduced.

1.2 Specification of the project

An inverting buck/boost converter is a type SMPS, which is currently gaining popularity for display applications in mobile devices. This thesis aims to analyze the EMI behavior of this type of converter and elaborate a solution to decrease the electrical noise.

As a starting point, Dialog Semiconductor provided a converter circuit. This and measurements on commercial circuits and a self-made inverting buck/boost helped to provide the needed insight to analyze the root causes for the EMI noise and to propose a solution to actively control the EMI in an IC design concept. Most work is performed experimentally and by simulation in LT-Spice and Cadence Virtuoso.

Chapter 2

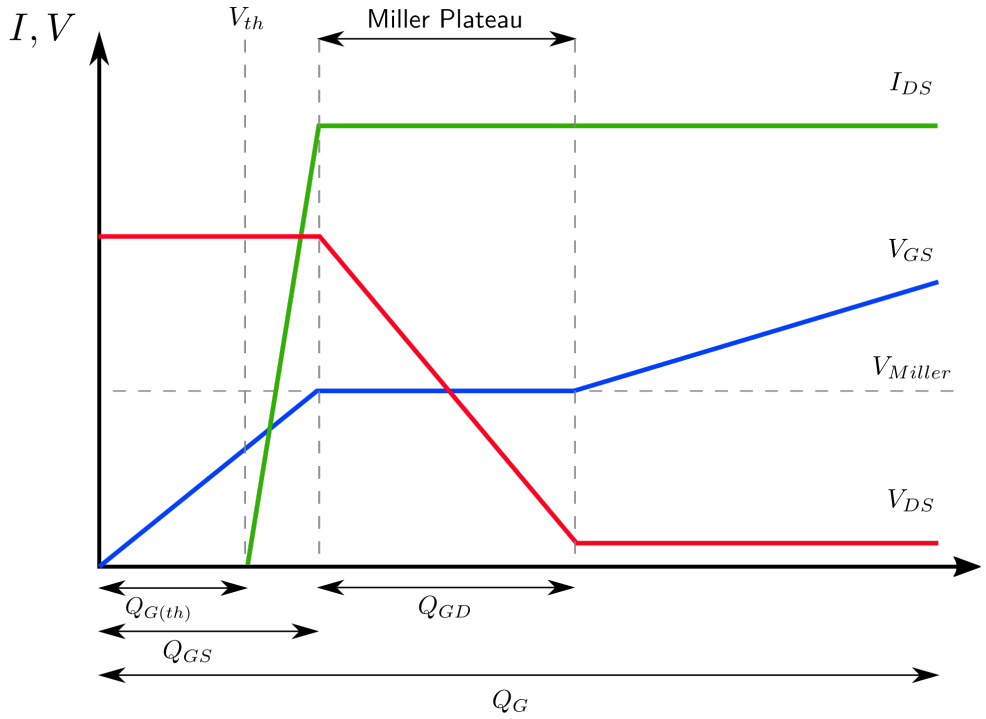
Theoretical background

Switched-mode power supplies (SMPS) are widely used, because of their high efficiency and small size. However, SMPS operate at high frequencies, depending on the power level from kHz to MHz, and even SMPS concepts of hundreds of MHz have been proposed. Due to their fast switching, electrical noise is created. If not handled correctly, which may include the source, filtering, or coupling path control, the noise can disturb modules, such as receivers within the same system, or lead to unacceptable emissions by users or violate regulations.

Consequently, the severity, origin, and coupling of those spectral components in the voltages and currents needs to be understood to create systems with acceptable inference parameters. Controlling the source is the most effective way to provide acceptable solutions, but it may impact on the efficiency and increases complexity. This thesis addresses the EMI of the inverting boost/buck topology for power levels that allow MOSFETs internal to an IC. This thesis is emphasizing on the sources of the EMI.

2.1 Switching behavior of the MOS - transistor

Figure 2.1 shows the turn-on behavior of an n-channel MOSFET. When charge is supplied to the gate, the gate-source voltage V_{GS} is rising. After the certain amount of charge ($Q_{G(TH)}$), V_{GS} equals the threshold voltage and the current from drain to source I_{DS} starts flowing. As the voltage reaches the miller level V_{Miller}, V_{GS} stays fairly constant although, more charge is supplied to the gate. During this period, named the miller plateau, the gate-drain capacitance is charged, and the drain-source voltage decreases. When the capacitance is fully charged, V_{GS} continues rising until the final driving voltage is reached. [1]



- $Q_{G(th)}$ Charge required from 0 V to the threshold voltage of the MOSFET
- Q_{GD} Charge required to move through the Miller region
- Q_{GS} Charge required from 0 V to the Miller plateau voltage
- Q_G Total gate charge required to raise the gate-to-source voltage to the specified value

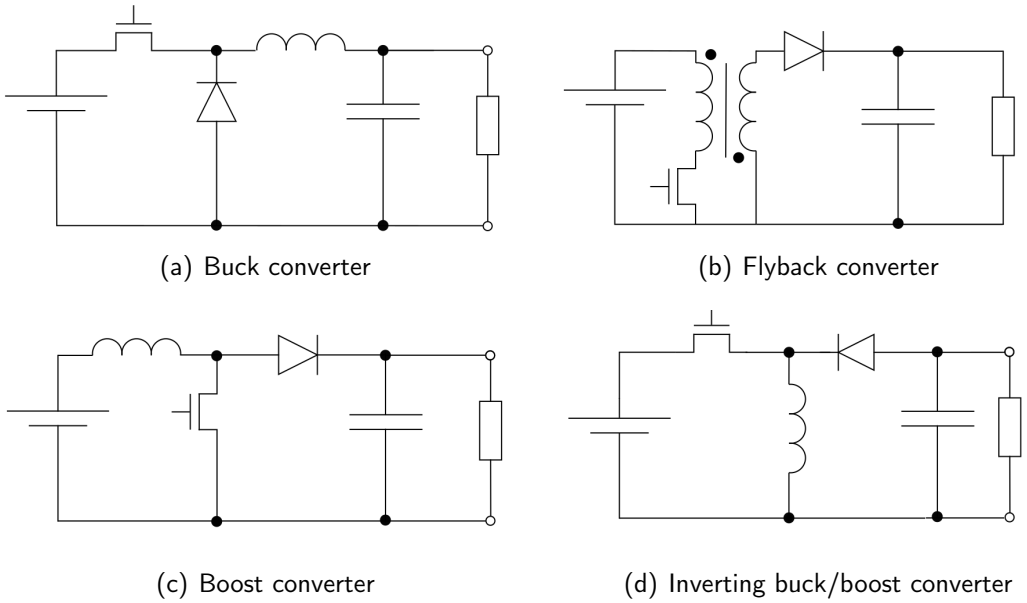
Figure 2.1: Mosfet turn-on response

2.2 Topologies of switched-mode power supplies

There are different topologies of SMPS. The most common topologies are:

- buck converter
- boost converter
- inverting buck/boost converter
- flyback converter

Fig. 2.2 shows a basic schematic of the different converter topologies. The asynchronous topologies are shown. In contrast to the synchronous topologies, they use a diode instead of a second switch. Each of the different converters has its own characteristics. While the boost converter can only produce an output voltage that is higher than the input voltage, the buck converter is only able to produce an output voltage, which is lower than the input voltage. The inverting buck/boost and the flyback converter can create an output voltage that is either higher or lower in magnitude than



(a) Buck converter

(b) Flyback converter

(c) Boost converter

(d) Inverting buck/boost converter

Figure 2.2: Popular dc-dc converter topologies

the input voltage. Without going into further detail, it also needs to be distinguished between isolating and non-isolating converters. The inverting buck/boost converter is a non-isolating converter: Input and output ground terminal are shared.

2.2.1 Function of an inverting buck/boost converter

This section refers to [2]. The inverting buck/boost converter is a SMPS that can convert a DC input voltage into a negative DC output voltage. The magnitude of the output voltage is defined by the duty cycle of the switched signal. In difference to the common buck and boost converters, the output signal's amplitude can be both, higher and lower than the input signal's amplitude. Fig. 2.3 shows the basic topology of an inverting buck/boost converter. The negative output voltage is already taken into account by the arrow direction in the schematic. The converter's main components are the switch, the inductor, the diode, and the in- and output capacitors.
Regarding the function of an inverting buck/boost converter, two cases have to be considered separately:

- Continuous current mode (CCM)
- Discontinuous current mode (DCM)

When the converter is operating in the CCM, the current which is flowing through the inductor is never zero. When the converter is operating in the DCM, the current through the inductor falls to zero during the time, when the switch is off for a sufficient time to remove the energy from the inductor.

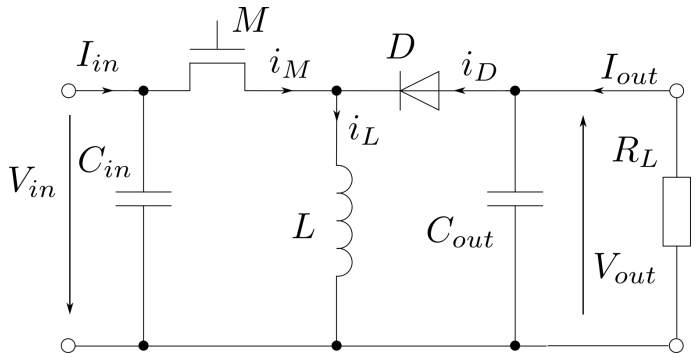


Figure 2.3: Basic topology of an inverting buck/boost converter

2.2.1.1 The inverting buck/boost converter operating in CCM

For the analysis of the function of the converter, two cases are considered:

- The switch is closed. The time when the switch is on is called t_{on}.
- The switch is open. The time when the switch is off is called t_{off}.

During t_{on}, the voltage across the inductor equals the input voltage. So the current through the inductor is rising linearly. As the switch is switched off, the energy stored in the inductor keeps the current flowing through the inductor. The only path the current can flow to create a closed current loop is across the load and the diode back to the inductor. Due to the direction of the current through the load, a negative voltage is created. This voltage is kept at a constant level by the output capacitance. During t_{off}, the current through the inductor is decreasing linearly. When the switch gets turned-on again, the diode starts blocking and the cycle restarts from beginning.

During the steady-state, the described cycle is repeated periodically, which means, that t_{on} and t_{off} are constant for many periods. The inductor current is rising during t_{on} and falling during t_{off}, but the mean of the inductor current is on a constant value.

Based on the steady-state, a simple analysis of the converter is possible. For this analysis, all components are assumed to be ideal. Fig. 2.4 shows the most important currents and voltages in the converter.

Based on fig. 2.4 two equations can be formed:

$$V_{in} = L \cdot \frac{\Delta I}{t_{on}} \tag{2.1}$$

$$V_{out} = L \cdot \frac{\Delta I}{t_{off}} \tag{2.2}$$

During the steady-state, the ΔI during t_{on} and t_{off} has the same value. Also, the integral over time of the voltage across the inductor leads to the same value during t_{on} and t_{off}. This means the area under the voltage curve during t_{on} equals the area during t_{off}.

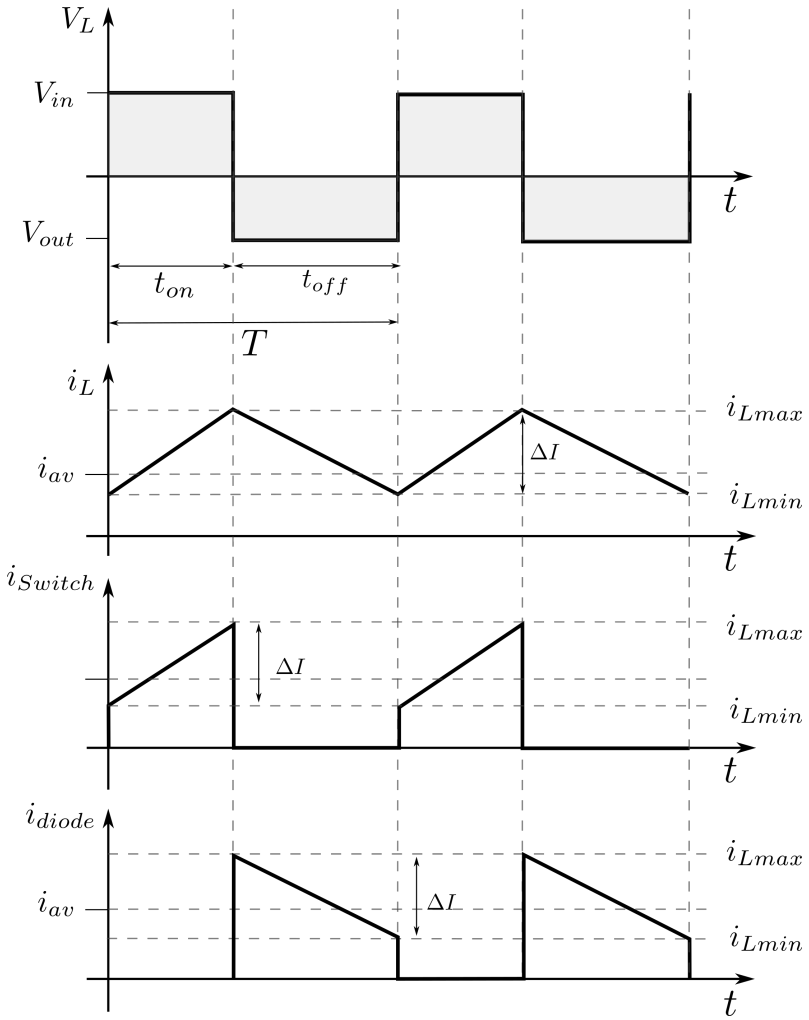


Figure 2.4: Voltages and currents during CCM

Based on the equations (2.1) and (2.2), the voltage transfer function can be derived.

$$d = \frac{t_{on}}{T} \tag{2.3}$$

$$T = t_{on} + t_{off} \tag{2.4}$$

$$\frac{V_{out}}{V_{in}} = \frac{t_{on}}{t_{off}} = \frac{t_{on}}{T - t_{on}} = \frac{d \cdot T}{T - d \cdot T} = \frac{d}{1 - d} \tag{2.5}$$

Looking at equation (2.5), it can be observed, that the transfer function is only dependent on the duty cycle d. But this formula is only valid for the CCM. In practical SMPS a feedback loop controls the duty cycle, based on the output voltage. For DCM the parameter is not the duty cycle but the switching frequency since the coil current goes always back to zero.

Chapter 3

EMC analysis of inverting buck/boost converter

An EMC analysis is presented in this chapter to investigate the root cause of electrical noise in a buck/boost inverting topology. This analysis is performed for a low-power inverting buck/boost converter that can deliver only a few watts. Such a converter is small in size and does not require a heat sink or large power cables. Such a converter is usually mounted within a large printed circuit board that is much larger in size than the converter IC. These characteristics reduce common mode effects in the circuit to a minimum. Therefore, no attempt is made to measure common mode noise. For completeness, two effects that produce common mode noise are presented in section 3.1.

3.1 Common mode effects

Two main effects cause common mode currents in the converter structure:

- Capacitive coupling of high dv/dt nodes to the surrounding
- Flux wrapping around the PCB

All three effects cause a common mode current or voltages, which can drive common mode currents. Supply cables attached to the PCB can act as an antenna, and the common mode currents can cause radiated emission.

3.1.1 Capacitive coupling of high dv/dt nodes

Fig. 3.1 illustrates the $\vec{E}$-field coupling of a PCB to its surrounding. The current through this coupling can drive common mode currents. The capacitance value is strongly dependent on the physical size of the node. The most critical nodes are the nodes that have high dv/dt voltage. Due to the voltage change across the capacitor, a current I_{CM}

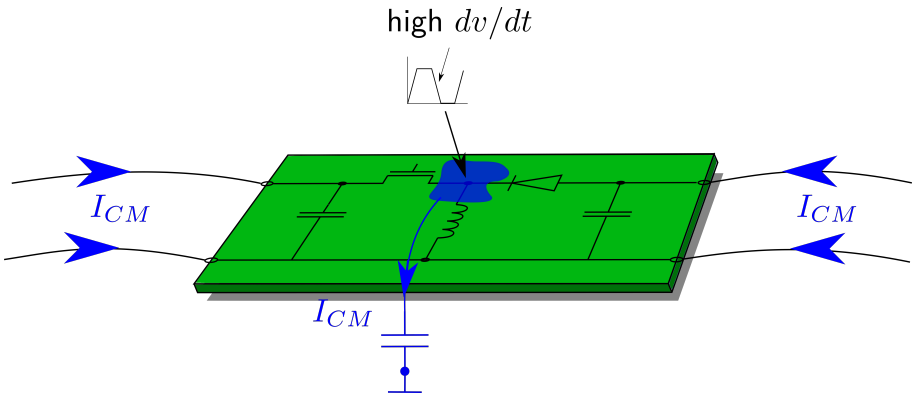


Figure 3.1: Capacitive coupling from high dv/dt node to ground plane

is flowing through it. This current flows back through the reference ground and closes the current loop. Due to the high slew rates on the switching node, which can be in the range of several $\frac{\mathsf{V}}{\mathsf{ns}}$, high common mode currents can also occur if the capacitance value to the surrounding is only in the fF range. The simple calculation example (3.1) shows, that a common mode current of 1 mA is produced due to a 100 fF capacitance from the switching node to ground when the switched signal's slew rate is 10 $\frac{\mathsf{V}}{\mathsf{ns}}$. During the transitions high frequency resonances are excited and couple through the parasitic capacitance. Fig. 3.2 show a simple simulation. Significant high current amplitudes couple through the parasitic capacitance in certain frequency ranges.

Due to the small structures of the low-power inverting buck-boost converter and the lack of long leads, converter's ground path is assumed to be ideal and equal to the reference ground. Due to the assumptions, no common mode signals will be are generated by this effect.

$$ic = C \cdot \frac{d_{V_C}}{dt} = 100\,\mathsf{fF} \cdot 10\,\frac{\mathsf{V}}{\mathsf{ns}} = 1\,\mathsf{mA} \tag{3.1}$$

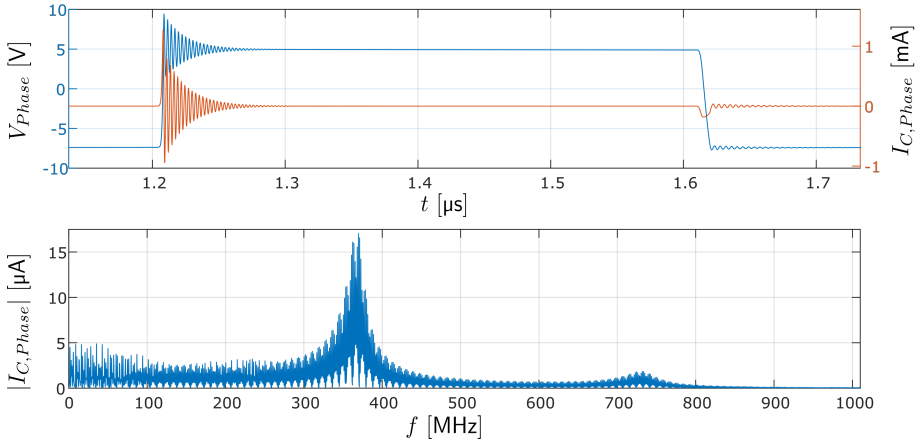


Figure 3.2: Simulation: Capacitive coupling from the phase node to ground

3.1.2 Flux wrapping around the PCB

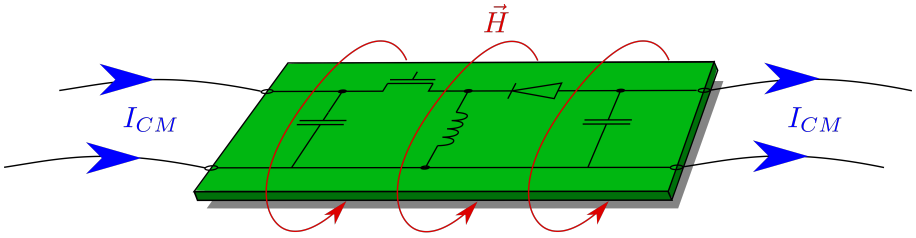


Figure 3.3: Flux wrapping around the PCB

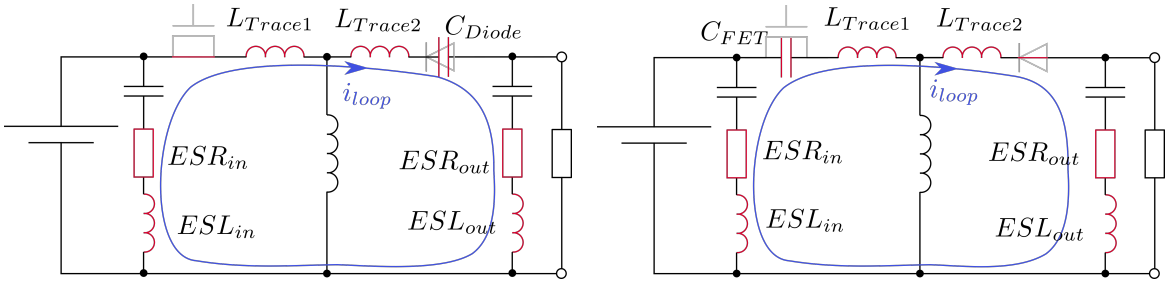
Fig. 3.3 illustrates the $\vec{H}$-field coupling. The current flowing through the PCB is creating a magnetic field $\vec{H}$ around the trace. Most of the field lines run around the trace. But a few field lines run around the PCB. These field lines cause a voltage drop due to induction in the PCB traces and the ground plane. This voltage drop causes a common mode current.

Due to the small size of the low power converter mounted on a large PCB, the field lines around the PCB forcing a common mode voltage are considered to be negligible.

3.2 Differential mode EMI-path

Unlike other switched mode power supply (SMPS) toplogies, the switching noise of an inverting buck/boost converter is visible at the input and the output. This is due to the connection of one inductor terminal to ground. In other topologies, like the buck and the boost converter, the inductor isolates either input or output from the switching noise [3] [4].
To analyze the EMI paths of the inverting buck/boost topology, the following parasitics have to be added to the ideal circuit diagram:

- MOSFET capacitance in its blocking stage (50 pF to 500 pF). The MOSFET's capacitance is strongly dependent on the voltage across it, and it is not linear. As the voltage across the transistor during the blocking stage is in a specific range, the capacitance value is in a specific range. This allows using a fixed value for that condition.
- Diode capacitance in reverse bias (10 pF to 200 pF)
- The inductance of the loop formed by the input capacitor, the diode, and the output capacitor back to the ground plane is broken down into ESL_{Cin}, L_{Trace1}, L_{Trace2}, and ESL_{Cout} .
- Parallel capacitance of the inductor and ESR of the main inductor.



(a) EMI path during turn-on (b) EMI path during turn-off

Figure 3.4: EMI path during turn-on and turn-off

The parallel capacitance does not shunt a significant amount of current because of its small value. So EMI currents can reach the in- and output. The EMI path of an inverting buck/boost converter varies between two stages: in each stage, either the FET or the diode is conducting, but the other of the two components act as a capacitor.

3.2.1 EMI path when the switch is closed

The turn-on of the MOSFET raises the voltage on the phase node [1] and causes a reverse biasing of the diode. The fast transient excites an LC structure which is formed by the loop inductance and the junction capacitance of the reverse-biased diode. Fig. 3.4(a) shows the EMI-path during turn-on.

3.2.2 EMI path when the switch is open

During turn-off, the EMI path changes. While the inductance is the same, the critical capacitance changes from the diode to the MOSFET. Both are non-linear. Fig. 3.4(b) shows the EMI-path during turn-off.

3.3 Simulation model in different levels

The basic function of the circuit is shown using the basic model of the inverting buck-/boost converter. The model is later expanded to include parasitic components to illustrate the EMI behavior of the circuit.

3.3.1 Basic simulation model

The basic simulation model consist of the transistor and the controller replaced by an ideal SPICE switch, driven by a pulse voltage source. As all components and interconnections are ideal, no parasitic resonances or overshoots occur. The simulation results and the circuit are shown in fig. 3.5. The ideal behavior of the converter can be observed, as it is described in section 2.2.1.1.

[1] The phase node, or switching node is abbreviated as LX node in the following chapters

3.3.2 Simulation model including parasitics

To simulate the behavior of a real converter of this topology, some of the parasitics are added to the simulation model. To simulate the drain-source capacitance of a MOSFET, 100 pF capacitor is added in parallel to the switch. For simplicity, a fixed capacitor value is used. Later the switch and the capacitor are replaced by a real transistor model, which describes further non-idealities of a MOSFET including the voltage dependency of the parasitic capacitances. Further, a real Schottky diode model (SL03), a parasitic capacitance of the inductor, and ESL and ESR of the in- and output capacitors are added. Additionally, some inductance is added to describe the loop inductance. It physically not possible to assign an inductance value to a piece of wire or a PCB trace because the closed current loop has to be known to define an inductance. So this inductance describes the inductance formed by the current loop. Even then, it is physically not correct, this method works well for simulation purposes. The extended simulation model is shown in fig. 3.6.

Looking at the simulation results in fig. 3.7, a deviation to the ideal circuit behavior is notable. During the switching edges, some resonances are visible. The resonances during turn-on and turn-off are quite different because of the different ringing paths described in section 3.2.

During turn-on, the dominating resonance is formed by the diode's capacitance and the loop inductance L_{Loop} of the circuit, which is the sum of L_{Trace1},L_{Trce2} and the ESL of the in- and output capacitors. The frequency of the resonance can be calculated by (3.2). The losses causing damping the turn-on ringing are mainly generated due to the losses in the diode and the on-resistance of the switch and the ESR of the input and output capacitor.

$$f = \frac{1}{2\pi\sqrt{L_{Loop} \cdot C_{Diode}}} = \frac{1}{2\pi\sqrt{5\,\text{nH} \cdot 31\,\text{pF}}} = 404\,\text{MHz} \tag{3.2}$$

During turn-off, the dominating resonance is formed by the capacitance of the switch and the loop inductance. The frequency can be calculated by (3.3). The losses causing damping the turn-off ringing are mainly generated due to the losses in the diode and the ESR of the input and output capacitor. In this model, no Ross of the switch is modeled. Therefore, the switch does not contribute to the damping of the turn-off ringing.

During turn-on, another resonance is formed by the parasitic capacitance of the inductor and the loop inductance L'_{Loop}. Which is formed by $(L_{Trace1} + ESL_{in})||((L_{Trace2} + ESL_{out})$. The frequency is calculated in (3.4). This resonance is visible in fig. 3.7 in the time interval from 0.625 µs to 0.64 µs in all current and voltage traces. It can be seen most clearly on I_{C3} . This is the highest resonance frequency in the circuit.

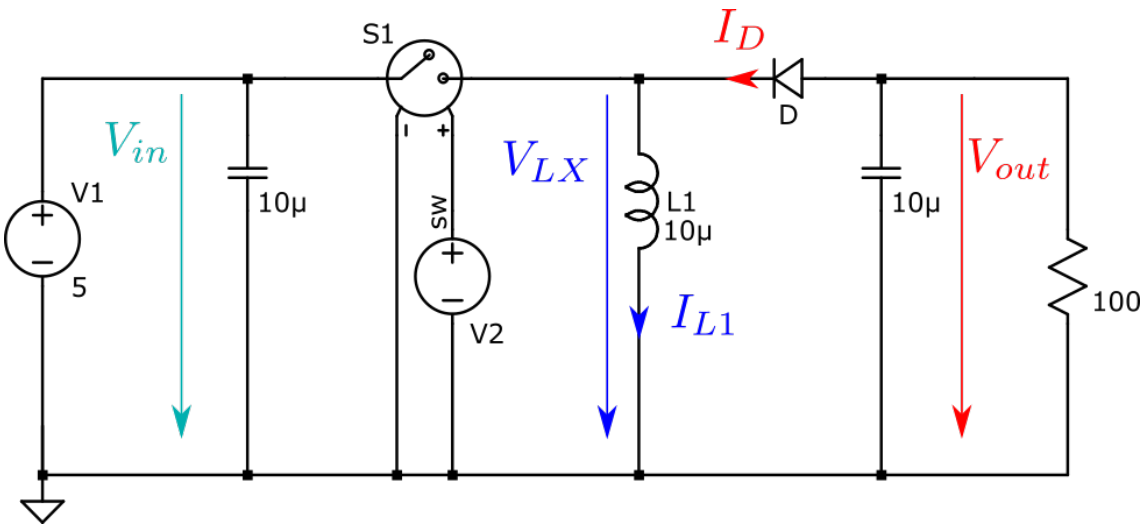
The lowest resonance frequency is found during the discontinuous conduction mode. As no dc current flows through the main inductor, the transistor and the diode act like capacitors. In this case, the main inductor is part of the resonance. Interestingly, the highest and the lowest resonance frequencies are formed by the same loops, but all

inductors are transformed into capacitors and vice versa. The low resonance frequency during the discontinuous conduction mode is visible in fig. 3.8. The ringing frequency is calculated in (3.5).

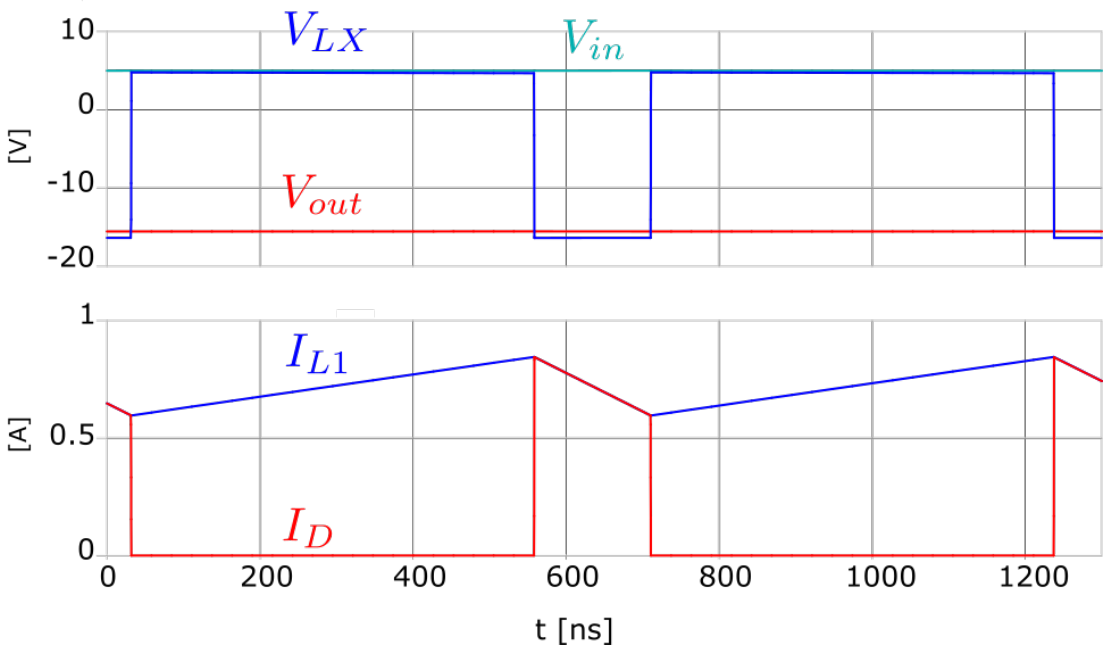
$$f = \frac{1}{2\pi\sqrt{L_{Loop} \cdot C_{FET}}} = \frac{1}{2\pi\sqrt{5\,\text{nH} \cdot 100\,\text{pF}}} = 225\,\text{MHz} \tag{3.3}$$

$$f = \frac{1}{2\pi\sqrt{L'_{Loop} \cdot C_{Inductor}}} = \frac{1}{2\pi\sqrt{1.25\,\text{nH} \cdot 1\,\text{pF}}} = 4.5\,\text{GHz} \tag{3.4}$$

$$f = \frac{1}{2\pi\sqrt{L_{main} \cdot (C_{Switch} + C_{Diode})}} = \frac{1}{2\pi\sqrt{10\,\mu\text{H} \cdot 130\,\text{pF}}} = 4.4\,\text{MHz} \tag{3.5}$$



(a) Ideal model of an inverting buck/boost vonverter



(b) Simulation results of the ideal inverting buck /boost converter

Figure 3.5: Ideal simulation model of an inverting buck/boost converter

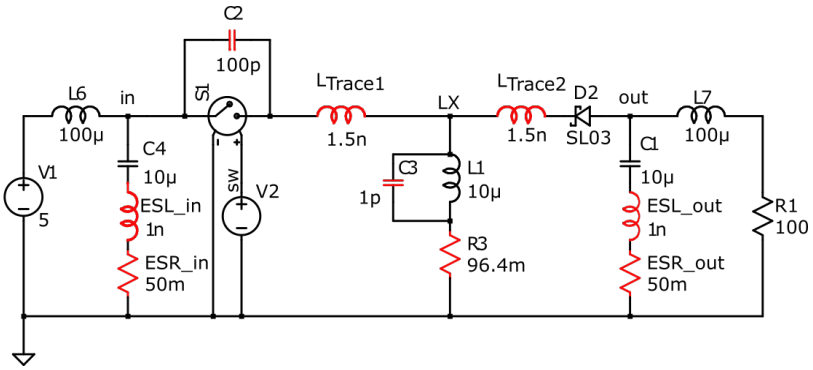


Figure 3.6: Simulation model including parasitics

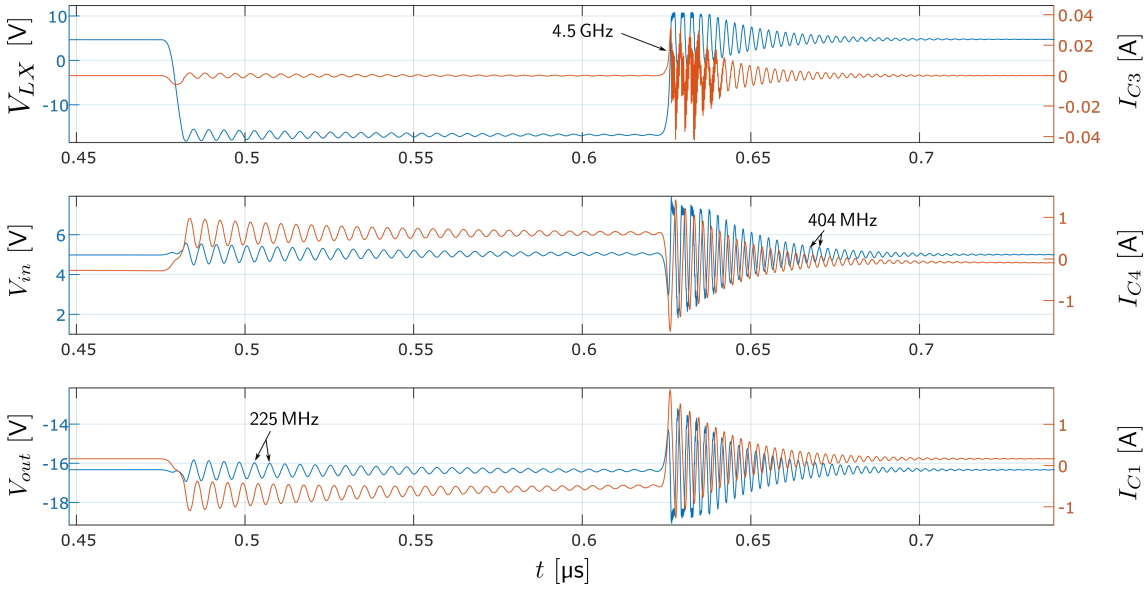


Figure 3.7: Simulation results during turn-on and turn-off of the converter. Parasitics included.

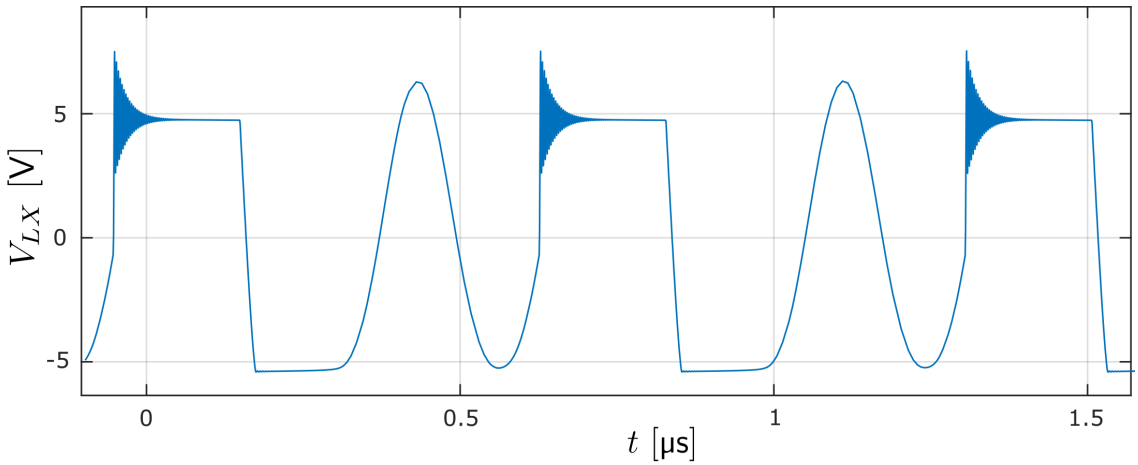


Figure 3.8: Phase voltage in discontinuous current mode

3.4 Converter built with discrete components

To confirm the correctness of the observations obtained by simulation, measurements are taken on inverting buck/boost converters. The measurements are applied to commercial converters and a converter designed from discrete components. The converter built with discrete components allows more control on the circuit, and more details on parasitics and behavior of the different components are known compared to the commercial converters. Further, the SPICE model is adapted to the components used in the circuit. The converter structure is kept as simple as possible, without any control loop to control the output voltage. The assembly uses a minimal area (50x30 mm) on a solid ground plane.

As the purpose of the circuit is to investigate the dominating EMI processes, a fast gate driver was selected. The $20\% - 80\%$ rise time of the gate driver is 2.4 ns, and the slew rate during the rising edge of the gate driver is 1.5 $\frac{\text{V}}{\text{ns}}$. The $80\% - 20\%$ fall time is 1.8 ns. The slew rate during falling is $-2\,\frac{\text{V}}{\text{ns}}$. The output of the gate driver rises from $-3\,\text{V}$ to $3\,\text{V}$. The source of the MOSFET is connected to the input port ($V_{in} = 3\,\text{V}$), so the gate-source voltage rises from $-6\,\text{V}$ to $0\,\text{V}$. To avoid bootstrapping, a P-channel MOSFET was selected. For both the diode and the MOSFET low capacitance devices are selected to increase the $\frac{dv}{dt}$ values. The resulting $20\% - 80\%$ slew rate on the phase node is 2.62 $\frac{\text{V}}{\text{ns}}$ during the rising and $-1.75\,\frac{\text{V}}{\text{ns}}$ during the falling edge. A list of the used components is shown in table 3.1.

To study parametric effects, additional discrete capacitors are added to vary the diode and MOSFET capacitances in both simulation and measurements. Further, inductances are added to observe the resonances when the loop inductance is varied.

3.4.1 Measurements of the converter

Figure. 3.9 shows the principle test setup. It is realized on a solid ground plane. Using GHz bandwidth line impedance stabilization networks (LISNs) on the input and output, the EMI currents can be captured. The LISNs prevent the high-frequency signals from reaching the source and load. Instead, the RF signals are redirected into the $50\,\Omega$ port of the measurement device. Fig. 3.10 shows the circuit board of the converter.

The phase voltage is probed via $1.8\,\text{k}\Omega$ terminated into a $50\,\Omega$ oscilloscope input. No

Table 3.1: Components used in the circuit

Component	Part Number	Properties
MOSFET	ZXMP10A13FTA	$C_{OSS} = 40\,\text{pF}$ @ $V_{DS} = -4\,\text{V}$
Schottky Diode	ZLLS350	$C_{Total} = 5\,\text{pF}$ @ $4\,\text{V}$
Inductor	CDRH4D16FB/NP-100MC	$L = 10\,\mu\text{H}$
Gate Driver	IX4340N	$I_{out} = \pm 5\,\text{A}$

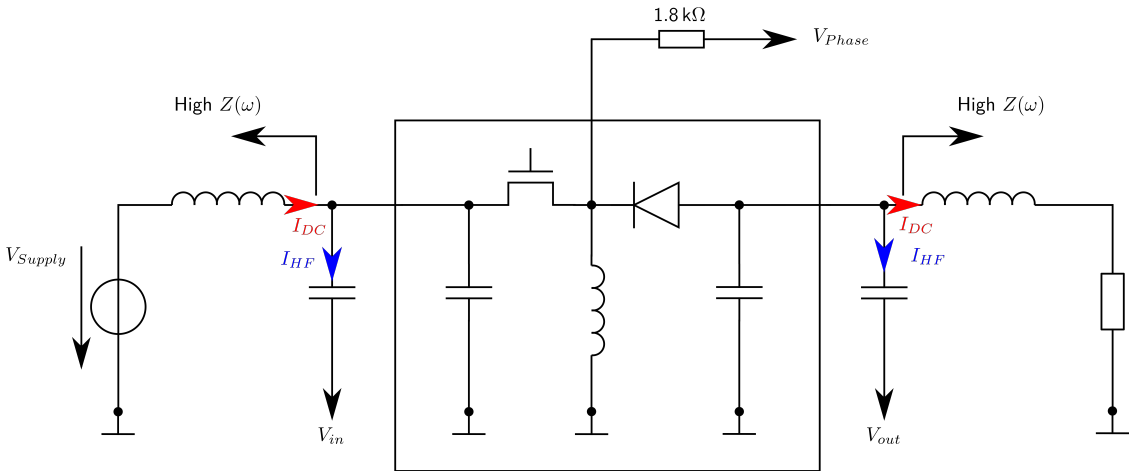


Figure 3.9: Measurement Setup

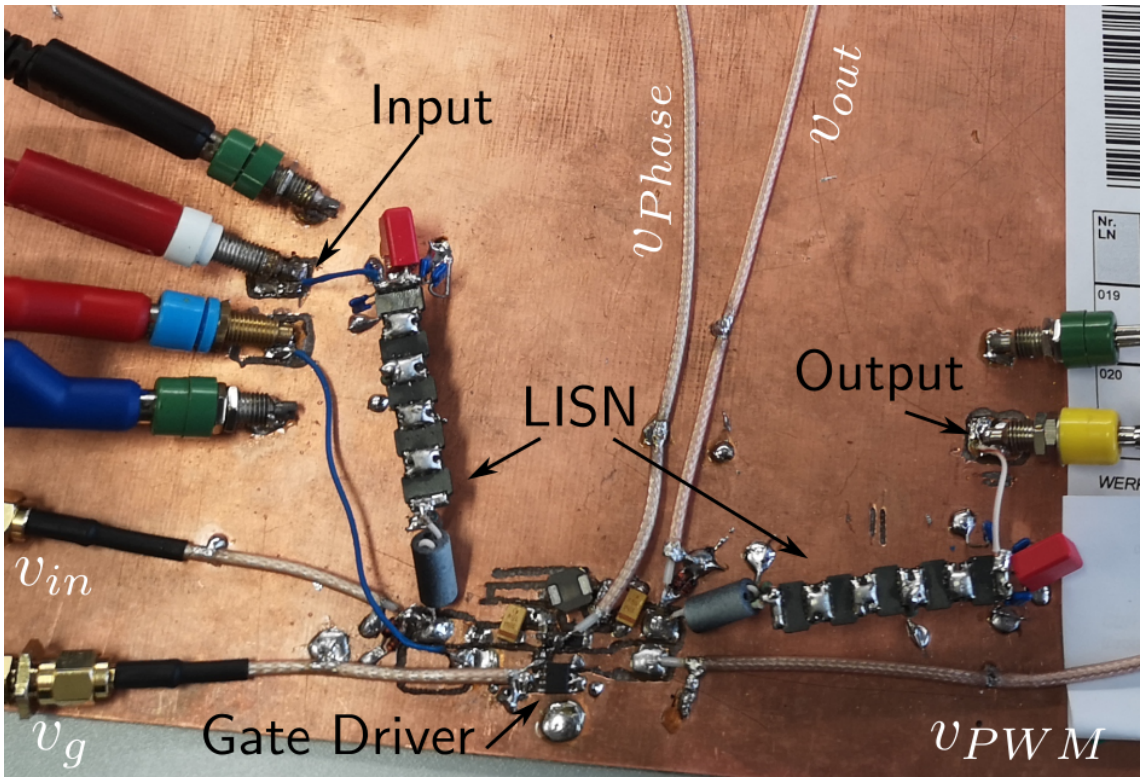


Figure 3.10: PCB of the converter, designed from discrete components

attempt is made to measure the current, as the introduction of any current probe would add at least a few nH of inductance into the loop.

The measurements are taken with an oscilloscope and a spectrum analyzer on the ports V_{in}, V_{out} and V_{phase}.

Figure 3.11 shows the measurement results on the phase node of the converter. The time-domain signal, the frequency spectrum, and the spectrogram of the signal are shown. The difference in resonance frequency in turn-on and turn-off is visible. In the time domain, dominant frequencies can be observed, 333 MHz during the turn-off event and 645 MHz during the turn-on event. Both frequencies are visible as peaks in the frequency spectrum.

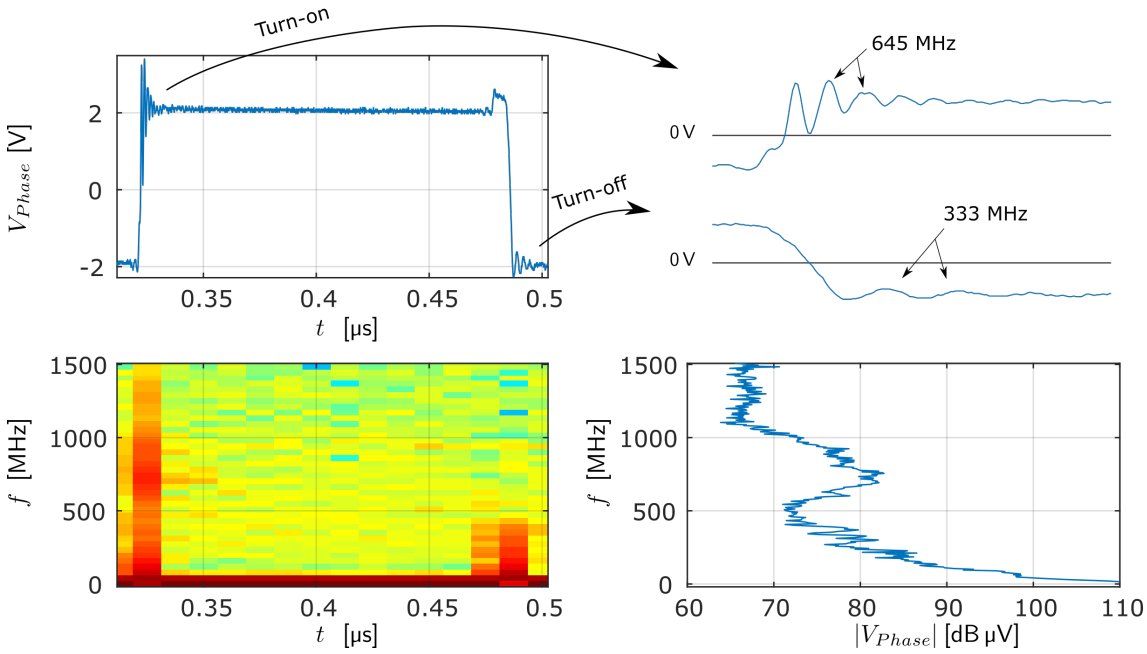
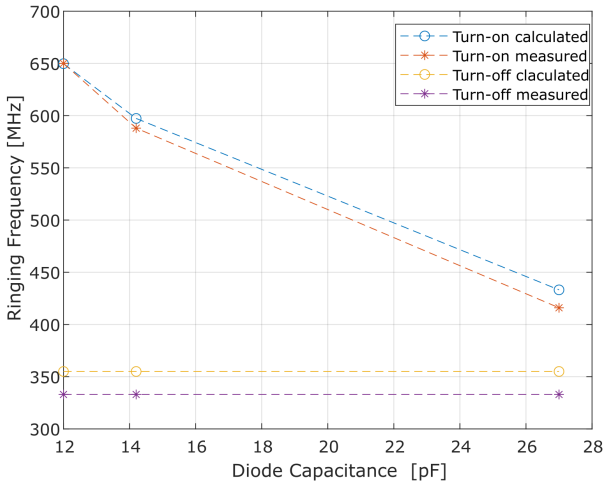


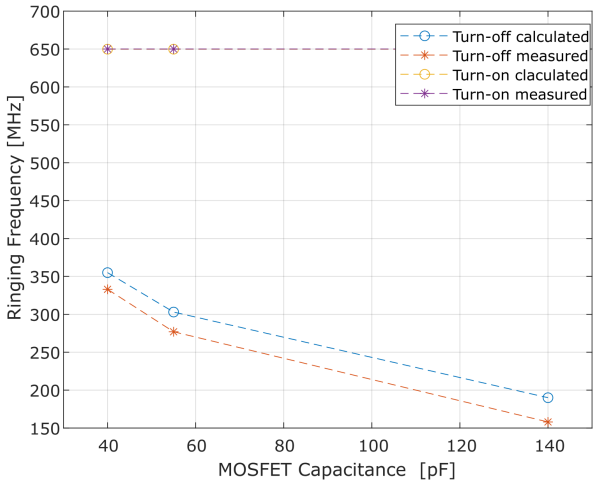
Figure 3.11: Measurement result on the input port of the converter

To provide evidence for the analysis of the two main EMI causing loops, capacitors are placed in parallel with the diode and/or the MOSFET. By adding different capacitors in parallel to the diode, the influence of the diode capacitance is investigated. Figure 3.12(a) shows a comparison of the different oscillation frequencies with different capacitor values. Using (3.3) and (3.4) including the parallel connection leads to the calculated data in figure 3.12(a). It can be observed that the oscillation frequencies during turn-on event are decreased, while the frequencies during turn-off are approx. the same. This confirms the analysis of the resonance during the turn-on given in section 3.2.

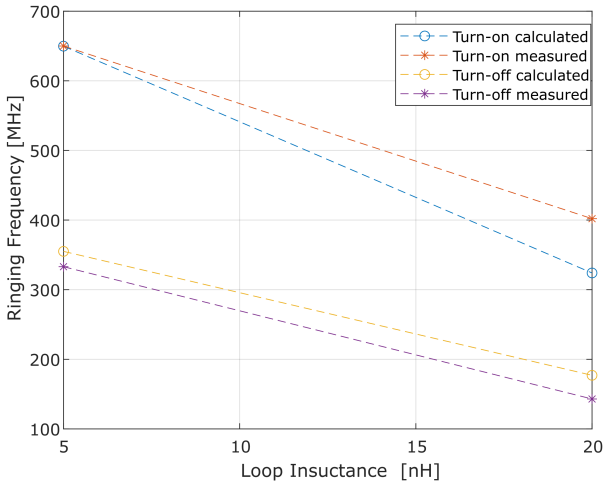
The influence of the loop inductance is investigated by adding a 15 nH inductor in series to the diode. Due to the increased loop inductance, both EMI paths are affected. Both parasitic resonances are shifted to lower frequencies. See figure 3.12(c).The calculated results in figure 3.12(c) are obtained by (3.3) and (3.2) using the resulting loop inductance.



(a) Change of the ringing frequencies due to the diode capacitance



(b) Change of the ringing frequencies due to the MOSFET capacitance



(c) Change of the ringing frequencies due to the loop inductance

Figure 3.12: Change of the ringing frequencies due to variation of parasitic components

By adding different capacitor values across the transistor's drain and source, the influence of the MOSFET capacitance can be observed. Figure 3.12(b) shows a comparison of the different oscillation frequencies with different capacitor values. The calculated values are obtained using (3.3) and (3.2) using the resulting MOSFET capacitance. A decrease in the frequency during turn-off with increasing capacitor value is visible. The frequency during turn-on stays more or less constant. Again confirming the analysis of section 3.2.

The influence of load and input voltage are investigated by measurements while varying these parameters. Fig. 3.13 shows the measured input V_{in}, output V_{out}, phase V_{LX}, and gate voltage V_G in the time domain, and V_{in} and V_{out} in the frequency domain. On V_{LX}, the influence of the input voltage is visible by a change of the high and low value. The high level equals the input voltage. Since the duty cycle is kept constant, the absolute value of the low level decreases with decreasing input voltages. Large input voltages and output voltages cause higher currents, which charge and discharge the parasitic capacitance on the phase node. The capacitance on the phase node consists of the sum of the copper to ground capacitance, the MOSFET capacitance, the diode capacitance and the parasitic capacitance of the main inductor. Larger currents cause higher slew rates on the phase node voltage, because of the faster charging of the pahse node capacitance. Due to that, the ringing amplitude is increased. This can also be observed in the time and frequency domain of the input and output voltage. The voltage peak caused by the gate driver on the input at the beginning of the turn-off event is increased by a higher input voltage because of the higher supply voltage of the gate driver.

Fig. 3.14 shows the influence of the load resistor on the converter behavior. The phase voltage shows lower voltage amplitudes using smaller load resistors. Lower load resistors cause a higher load current. Higher load currents cause a higher coil current. The coil current discharges the phase node capacitance during turn-off. The higher the coil current, the steeper the falling edge. The steeper edges cause a higher ringing amplitude during turn-off. This can be seen in the time domain plots of V_{in}, V_{out}, V_{LX}, and the two frequency domain plots.

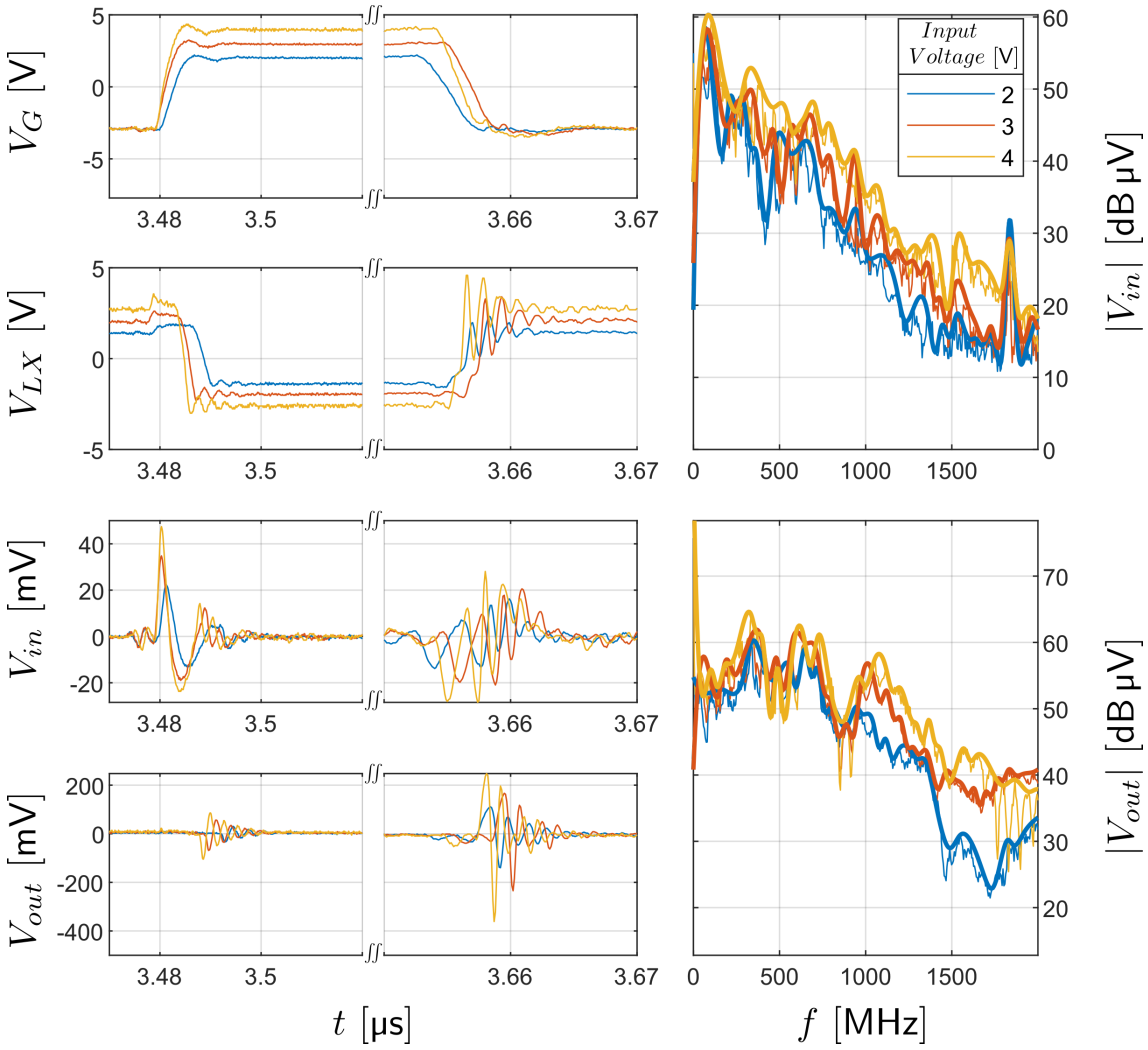


Figure 3.13: Measurement: Influence of the input voltage on the converter behavior

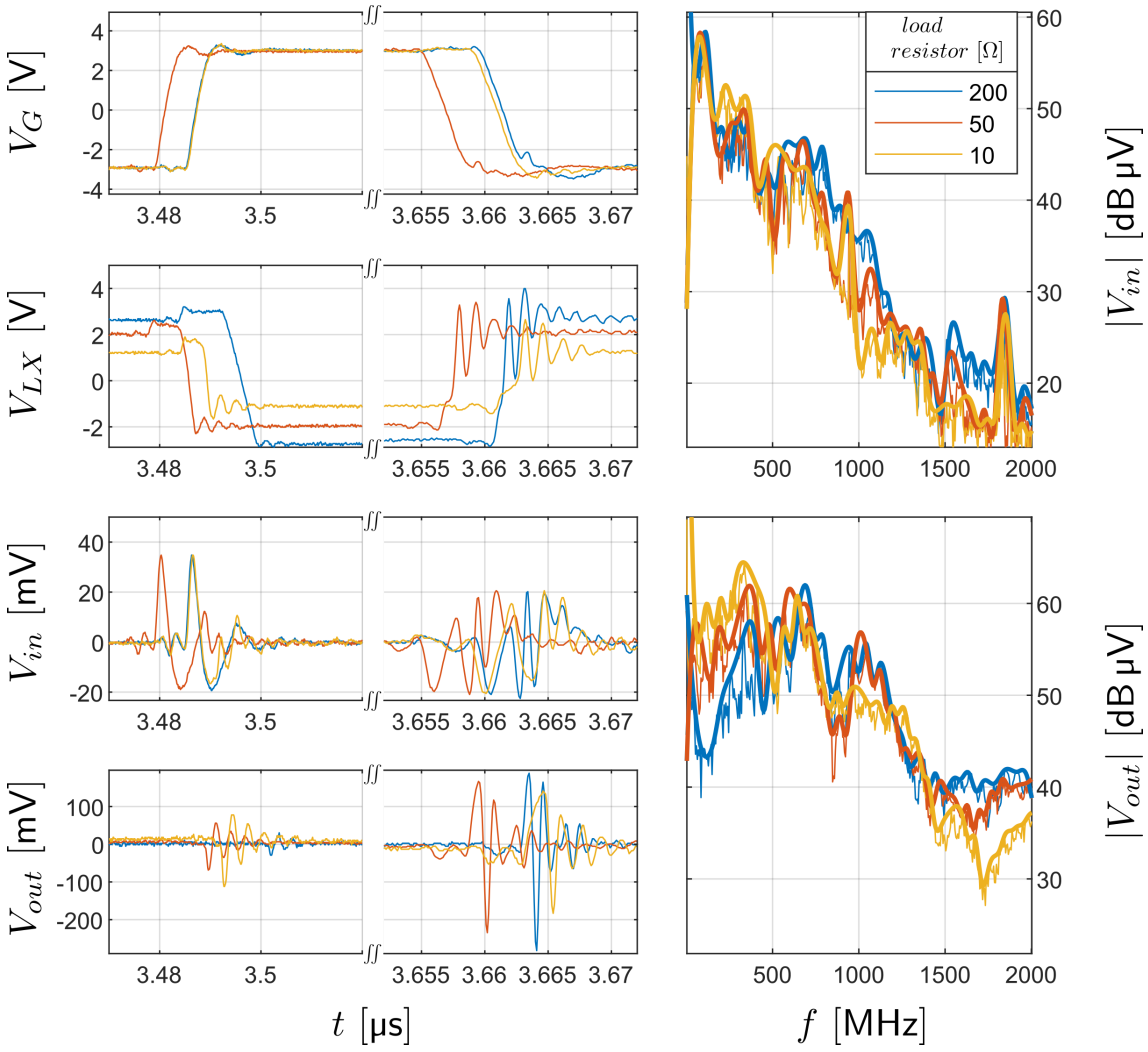


Figure 3.14: Measurement: Influence of the load resistor on the converter behavior

3.4.2 Simulation of the converter

The spice simulation model is adapted to the components used and the estimated parasitics of the circuit board. The SPICE models of the transistor and the diode are provided by the manufacturers. Figure 3.15 shows the simulation results compared to the measurement results on the phase node of the converter. A spike at 650 MHz is shown in the simulation and measurement results. This spike corresponds to the turn-on ringing. The turn-off frequency is nearly not visible in simulation because of the small amplitude of the ringing and the strong low frequency components in the signal.

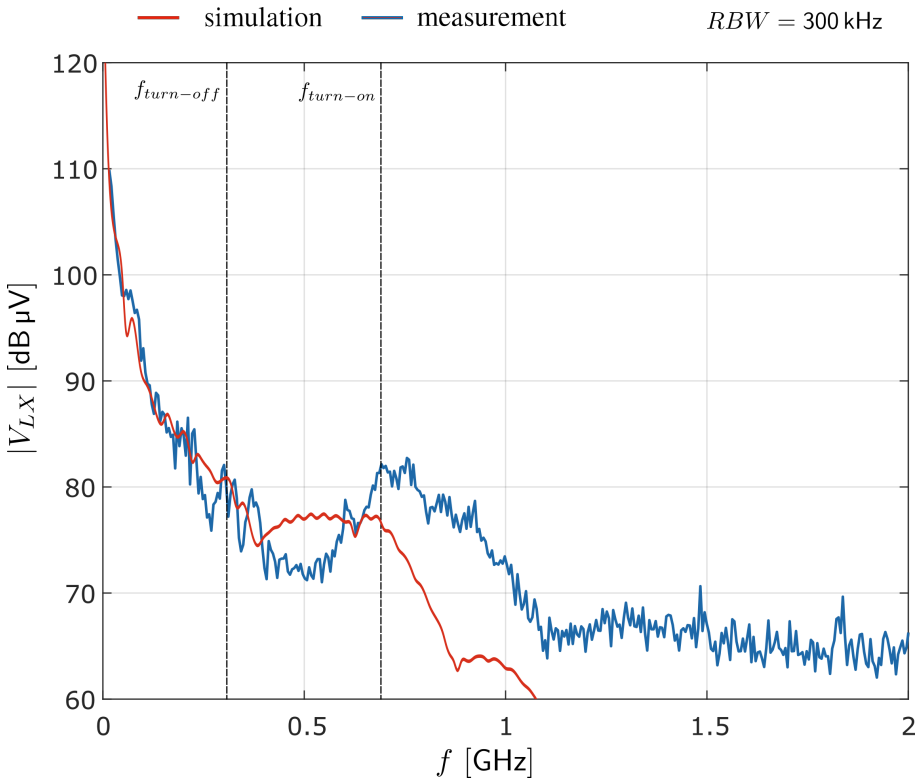


Figure 3.15: Simulation and measurement results of the frequency spectrum of the phase node signal

The frequency spectra of the in- and output ports and the time domain signals are shown in figure 3.16. The spectra of the in- and output show two peaks on the turn-on (330 MHz) and turn-off (650 MHz). The losses causing the damping of the turn-on ringing are generated due to the R_{on} of the MOSFET, the diode and the ESR of the input- and output capacitor. The losses causing the damping of the turn-off ringing are generated due to the R_{oss} of the MOSFET, the diode and the ESR of the input- and output capacitor. In the time domain, the simulated and the measured signals are corresponding. On the input port, before turn-on and turn-off, a pre-pulse is visible. This pre-pulse is generated by the gate driver, which is not modeled properly in the simulation model. This pre-pulse is also observed when the input voltage of the converter is 0 V, and no current flows from the input into the converter circuit. Therefore, a high amplitude in the lower frequency range of the frequency spectrum of the input port is visible. The

influence of the gate driver can be seen in fig. 3.17. The yellow trace indicates the behavior of the circuit with no input voltage and normal operation of the gate driver.

Since there are still differences between measurement results and simulation results, further investigations are planned for the future.

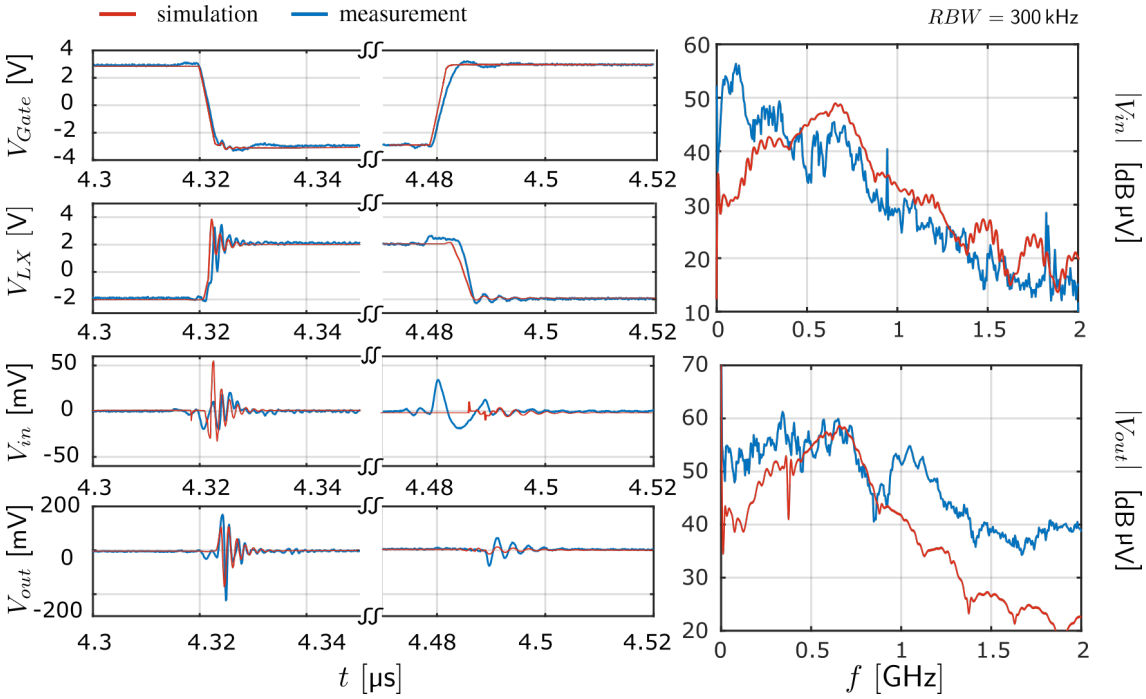


Figure 3.16: Comparison between measurement (blue) and simulation (red)

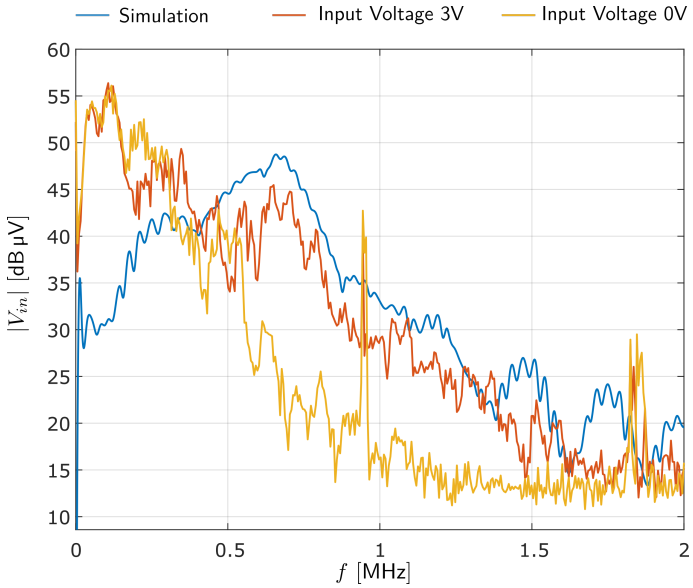


Figure 3.17: Comparison of the frequency spectrum of the voltage on the input port: Measurement in normal operation; Measurement with 0V input voltage; Simulation

Similar experiments are made in simulation as in the measurement. The capacitances across the transistor and the diode and the loop inductance are varied to compare the change in behavior in simulation and measurement. The main effects observed during the measurements are also visible in simulation. By increasing the capacitance across the diode, the frequency of the ringing during turn-on is shifted to lower frequency values. The results are shown in figure 3.19(a).

By increasing the capacitance across the transistor, the frequency during the turn-off event is shifted to lower frequencies. The simulation results are visible in figure 3.19(b).

Increasing the loop inductance affects both the frequency during turn-on and turn-off. Both frequencies are shifted to lower frequency values. The results are shown in 3.19(c).

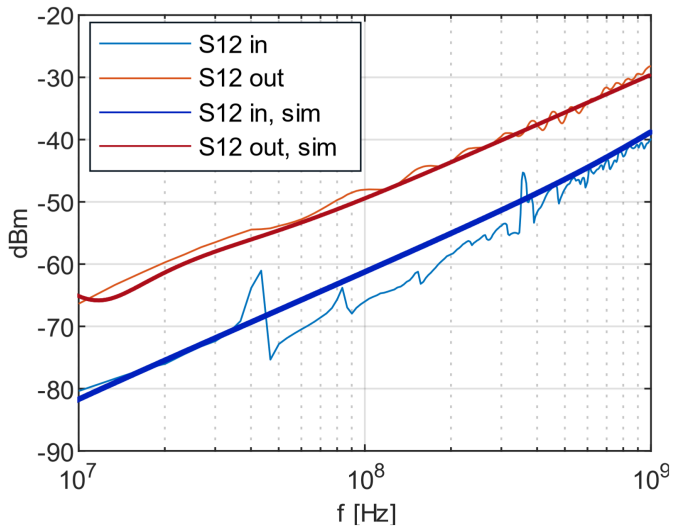
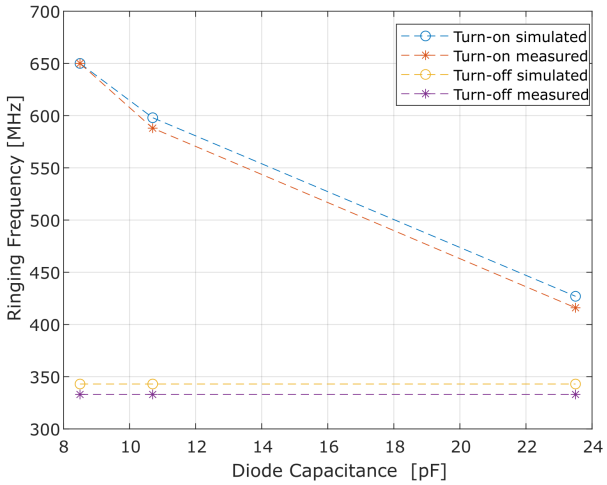


Figure 3.18: S_{12} measurement of the in- and output capacitors

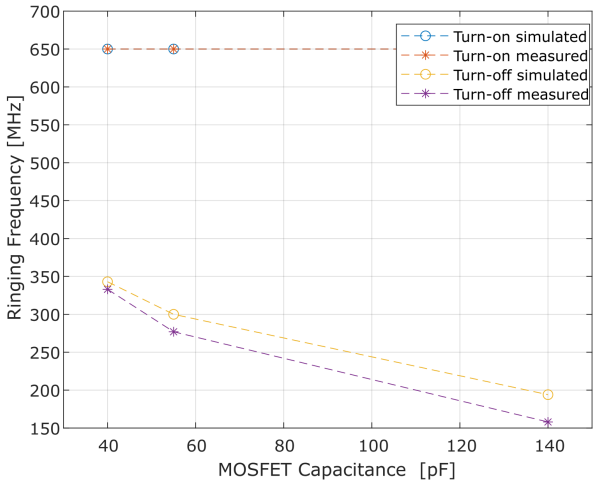
The EMI current can be estimated using the measured EMI voltage on the phase node and the parasitics along the EMI path. The parasitic capacitances are (5 pF @ $V_{Reverse} = 4\,V$) of the diode and (40 pF @ $V_{DS} = -4\,V$) of the transistor . The ESL of the input and the output capacitors is measured by measuring the S_{12} parameter. For the measurement of the S_{12} parameter, a spectrum analyzer with tracking generator is used. The results of the measurements are shown in figure 3.18. The ESL of the input capacitors is approx 0.05 nH, and the ESL of the output capacitors is approx 0.4 nH.

The inductances L_{Trace1} and L_{Trace2} are estimated using the measured ringing frequencies and the known parasitics. The resonance frequency during turn-on is given by (3.2). L_{Loop} is the sum of L_{Trace1}, L_{Trace2} and the ESL of the in- and output capacitor. With this information, Each of the inductances L_{Trace1} and L_{Trace2} can be estimated to approx. 2 nH.

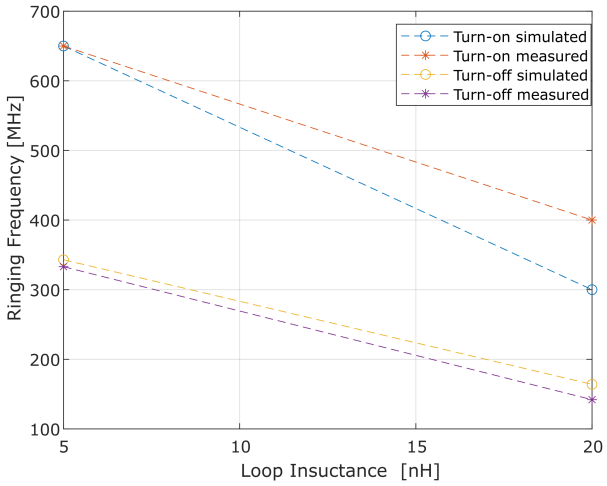
The simple simulation model showed the basic behavior and function of an inverting buck/boost converter. The model, including the parasitics of the circuit, can reconstruct the fundamental resonances which occur during turn-on and turn-off of the MOSFET.



(a) Change of the ringing frequencies due to the diode capacitance



(b) Change of the ringing frequencies due to the MOSFET capacitance



(c) Change of the ringing frequencies due to the loop inductance

Figure 3.19: Change of the ringing frequencies due to variation of parasitic components

The measurements on the circuit designed of discrete components confirm the theories explored by simulation. The influence of the MOSFET during turn-off, and the influence of the diode capacitance during turn-on is confirmed by a modification of the tested circuit in terms of adding additional capacitors in parallel to the diode and the MOSFET.

3.5 Measurements on commercial converters

To apply the analysis to actual circuits, an investigation of different commercial available converters is made. These converters show in principle similar behavior as the previously discussed converter. However, because the internal structure of the converters is not known, only assumptions of the real internal behavior can be made.

Two different evaluation boards have been investigated. Both converters have the same non-insulated inverting buck/boost topology. The differences of the converter specifications are in switching frequency, gate driver, input voltage range, output voltage, and maximum output current. The specifications of the different evaluation boards are listed in table 3.2.

3.5.1 Measurement setup

To achieve a similar measurement setup as shown in figure 3.9, the ground plane of the evaluation board is soldered directly on a large copper reference plane made from a PCB. The GHz bandwidth LISNs are added to the circuit.

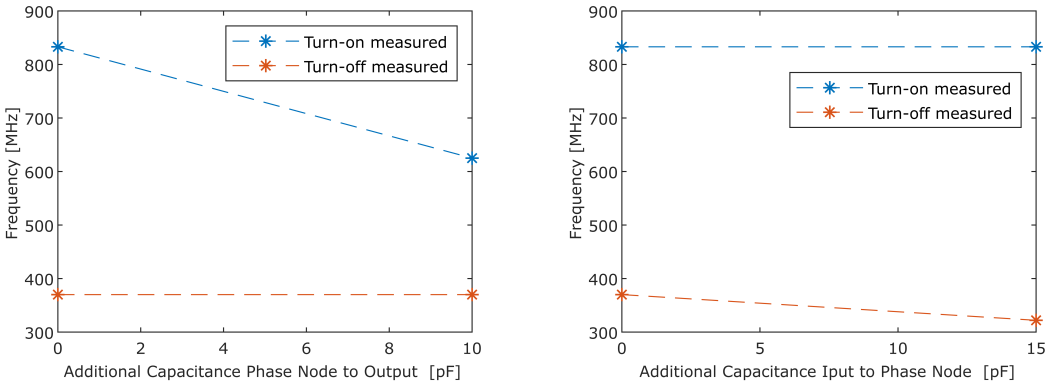
3.5.2 Measurement results of the commercial converters

The measurements on the commercial converters show similar behavior as the measurements on the converter built with discrete components. Different frequencies during turn-on and turn-off can be observed. The frequencies during turn-on are significantly higher than during turn-off, indicating low diode capacitance. Figure 3.20(a) shows the frequency dependency of the ringing on the diode capacitance of the ADP5075.

The influence of the transistor capacitance is shown in figure 3.20(b). For these measurements, an additional capacitor is connected in parallel to the input and the phase node. As the exact internal structure of the converter is not known and the additional capacitor may also influence other operations in the converter, the measured results may

Table 3.2: Specifications of the different evaluation boards

Board	ADP5075	TPS63700
Manufacturer	Analog Devices	Texas Instruments
Switching Frequency	1.2 MHz	1.4 MHz
Output Voltage	−5 V	−12 V
Slew Rate	fast/normal/slow	default



(a) ADP5075: Frequencies depending on the diode capacitance

(b) ADP5075:Frequencies depending on the MOSFET capacitance

Figure 3.20: ADP5075: Ringing frequency dependency on parasitic elements

not describe exactly the influence of the MOSFET capacitance. But as expected, the ringing frequency during turn-off is lowered by additional capacitance across the input and the phase node.

The ADP5075 allows changing its phase node slew rate. The drain voltage slew rate changes from 2.7 $\frac{\text{V}}{\text{ns}}$ to 5.7 $\frac{\text{V}}{\text{ns}}$ during turn on and from $-1.8\,\frac{\text{V}}{\text{ns}}$ to $-3.3\,\frac{\text{V}}{\text{ns}}$ during turn-off. The phase node signal and its slew rate are shown in fig. 3.21. In addition to the time and frequency measurements, also an efficiency measurement is taken. With lower slew rates, the EMI of the converter decreases in the frequency region from 400 MHz to 3.2 GHz (figure 3.22(a)), but the efficiency decreases too. The efficiency is approx. 3% higher in the fast than in the slow mode. The efficiency is not only depending on the slew rate. It also depends on the input voltage. See figure 3.22(b).

The second commercial converter, the TPS63700 shows similar behavior indicating that the SPICE based analysis and the converter designed from discrete components capture the main EMI properties of this class of converters.

Like other converters treated in this paper, two different resonances can be observed. The resonance during turn-on (374 MHz) is faster than the resonance during turn-off (224 MHz). Figure 3.23 shows the spectrogram and the time domain signal on the output port of the converter.

Fig. 3.24 shows the dependency on the input voltage and the load resistor of the commercial converters. Fig. 3.24(a) shows the frequency spectrum of the ADP5075 on the V_{out} port. It can be observed that the amplitude of the 908 MHz turn-on ringing is increased. Due to the increased input voltage rises, the amplitude of the phase node voltage and the slew rate increase. This phenomenon is already seen by the investigation of the converter built with discrete components. However, also a difference in behavior to the discrete component converter is observed. The turn-off ringing amplitude keeps unchanged while varying the input voltage. This is because of the internal regulation

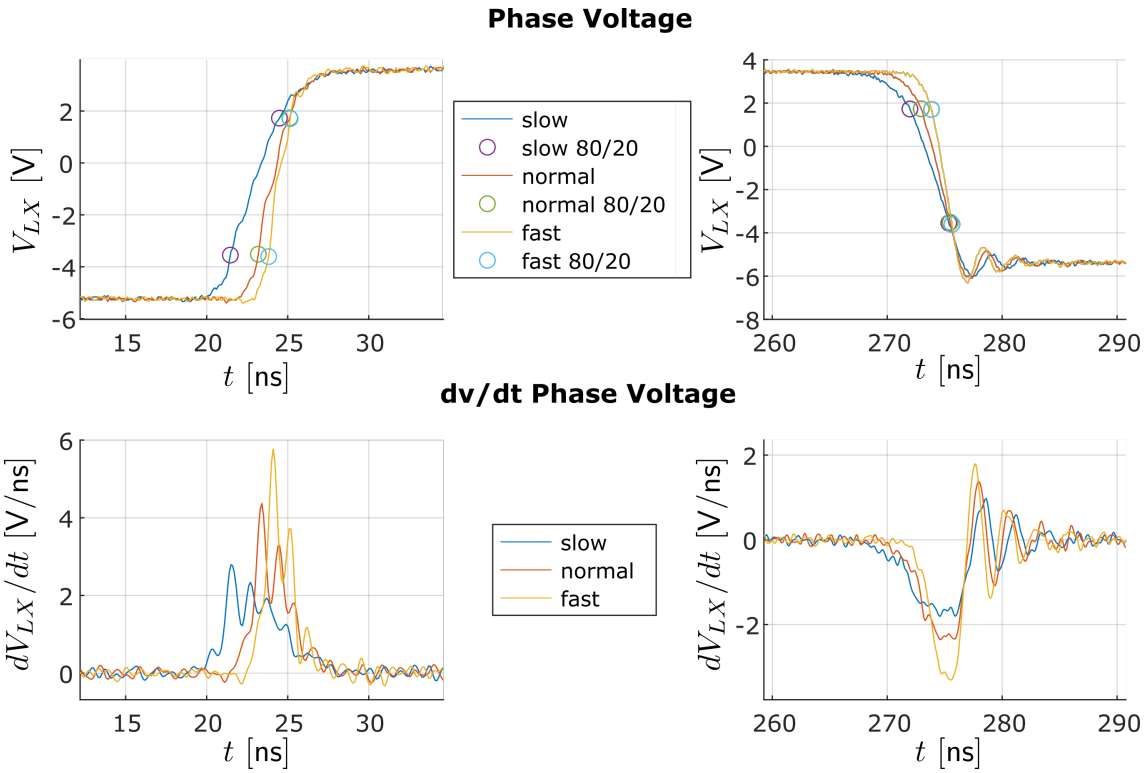
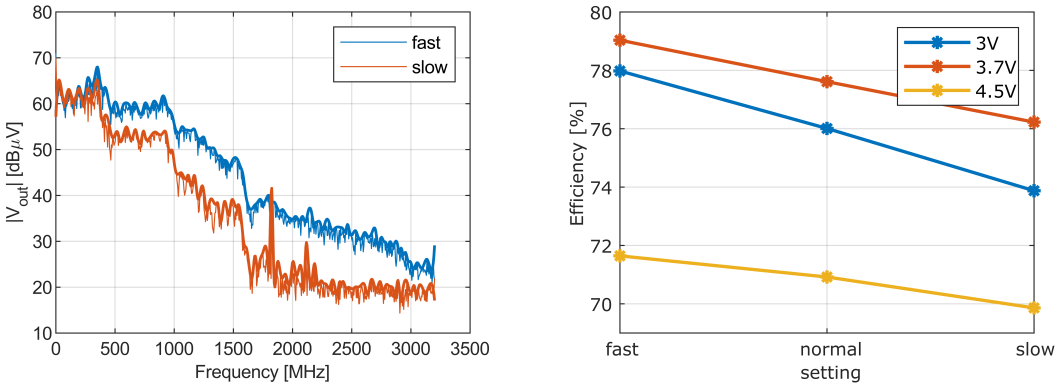


Figure 3.21: Phase node signal and its slew rate during turn-on and turn-off



(a) Frequency spectrum on the output port of the ADP5075 at different slew rate settings

(b) Efficiency depending on the slew rate and input voltage

Figure 3.22: ADP5075: Impacts of different slew rate settings on frequency spectrum and efficiency

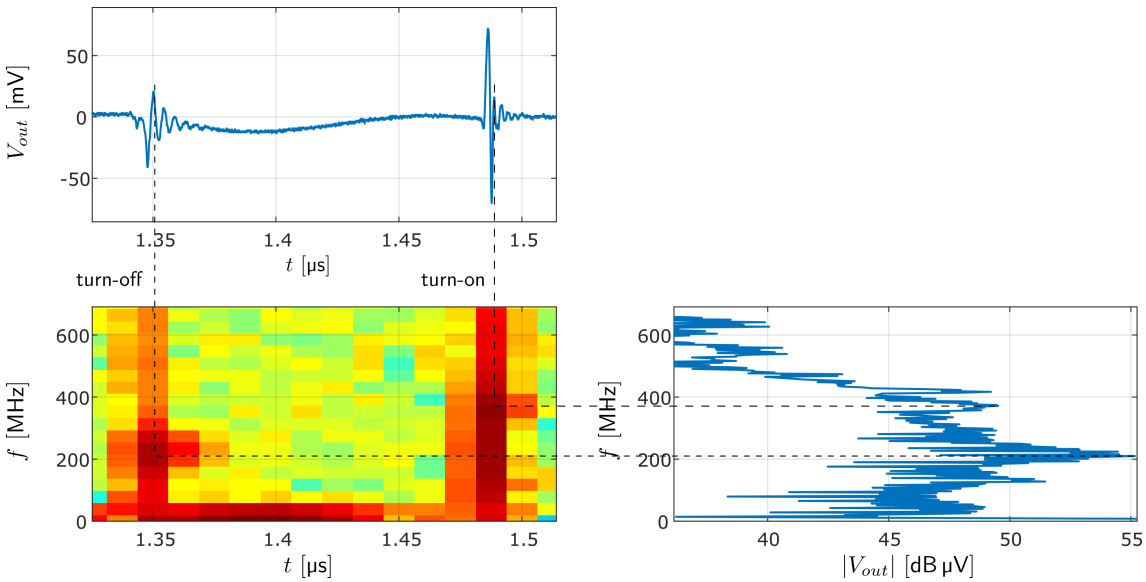
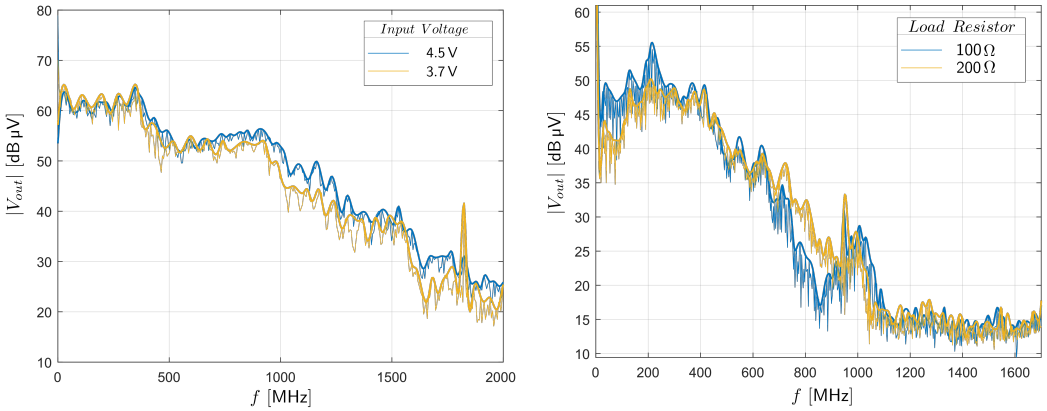


Figure 3.23: Measured EMI on the input port LISN using the TPS63700 at 3.7 V input, −5 V output and 123 mA

of the output voltage. As the output voltage keeps constant and the load resistor is unchanged, the load current is the same. So the coil current which is responsible for discharging the phase node capacitance does not change. The slope of the falling stays the same, therefore no change of the turn-off ringing is visible.

Fig. 3.24(b) shows the frequency spectrum of the TPS63700 on the V_{out} port. It can be observed that the 215 MHz turn-off ringing amplitude is decreased by higher load resistors. This can be explained by the decreased load current with higher load resistors. So the current which discharges the phase node capacitance during turn-off is decreased, and the voltage slew rate on the phase node is decreased during turn-off. This is already seen by the investigation of the discrete component converter. Due to the internal control loop, the output voltage is kept at a constant level. Therefore the voltage difference over the switch is kept constant while varying the load resistor. So the turn-on transition is nearly unchanged.

Figure 3.25 shows a comparison of the frequency spectrum of all tested converters. Some similarities are visible. All three converters have two dominant frequency peaks on the frequency of the ringing during turn-on and turn-off. All of the converters show a faster ringing frequency during turn-on than during turn-off. This is indicating a small diode capacitance in all tested converters. Table 3.3 shows a comparison of the different ringing frequencies of the different investigated converters.



(a) ADP5075: Frequency spectrum, depending on the input voltage

(b) TPS63700: Frequency spectrum depending on the load resistor

Figure 3.24: Dependency of input voltage and load resistance of the commercial converters

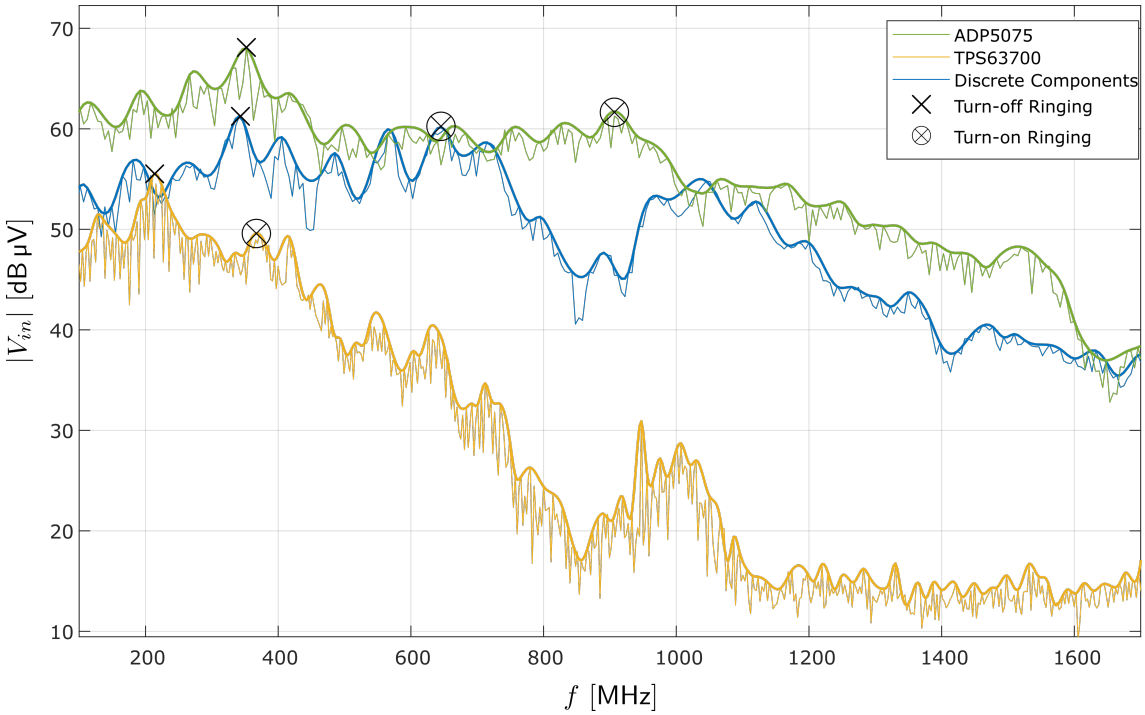


Figure 3.25: Comparison of the frequency spectrum of the different measured converters, measured on the input port

Table 3.3: Comparison of the investigated converters

Board	Turn-on Ringing [MHz]	Turn-off Ringing [MHz]	Switching frequency [MHz]
Discrete Components	645	341	3
ADP5075	906	352	2.4
TPS63700	368	215	1.4

3.6 Conclusion

The EMI analysis of the inverting buck/boost converter shows that two resonances are excited and both, input and the output side of the converter can conduct the EMI signals. One resonance is excited during turn-on, the other is excited during the turn-off. In both cases, the inductance is formed by the loop inductance that includes the input capacitor, the MOSFET, the diode, and the output capacitor. However, for the turn-on, the reverse-biased diode forms the capacitor, while turn-off the MOSFET forms the capacitance, while the diode is conducting currents. The general behavior has been verified in simulation and by the design of a converter from discrete components. The analysis of commercial converters shows the same principle behavior, although the internal structure of the commercial converters is not known and their design dampens ringing strongly.

Chapter 4

Reducing EMI in SMPS

Many different approaches are used in SMPS to reduce EMI. The approaches can be basically subdivided into four big categories:

- Filtering before or after the SMPS
- Component selection, e.g. high Ross
- Return current control on PCB level, reduce the loop inductance
- Advanced control of the switches, spread spectrum, drive to suppress certain frequency ranges, variable frequency control

In table 4.1, some well understood methods to reduce EMI in SMPS are listed. Since it is not possible to investigate each aspect, only the approach to limit the slew rate on the phase node is further investigated in this thesis.

In contrast to methods that shield or filter, this approach addresses the root cause of the EMI: The switching source.

Table 4.1: Different methods to reduce EMI in SMPS

Methodes to reduce EMI	Short description	Reference
Snubber	RC-, and RL-combinations and diodes used to prevent high dv/dt and di/dt peaks in the circuit.	[3], [5], [6]
PCB based passive filters	Additional passive filters are placed on the PCB to filter the noise caused by the converter.	[7], [8]

Table 4.1: Different methods to reduce EMI in SMPS

Methodes to reduce EMI	Short description	Reference
PCB based active filters	Additional active filters are placed on the PCB to compensate the noise caused by the converter.	[9], [7]
PCB routing	Geometry: Routing of traces, planes, and vias influence the current path, thus the inductances and the capacitive coupling. Confining the converter currents into the smallest possible space and avoiding large areas on nets that have large voltage changes improve the magnetic and the electric field coupling pushes resonance frequencies upwards where they are less excited, and the damping is larger.	[10]
Component type selection	The selection of the components placed on the PCB has a big impact on the EMI. Different component types show different parasitics, which are influencing the EMI behavior of the circuit. Capacitors should be selected to have a small size, low ESR, and a sufficient value. For filtering, capacitors can be placed as resonators, but this requires an exact understanding of the resonance frequencies and current paths. The FET selection influences the rise time, capacitances and losses of the circuit and wanted losses of ringing which leads to a fast attenuation. Special attention needs to be placed on reverse recovery.	[11]
Shielding	Shielding the converter prevents disturbances from spreading. Shielding sensitive circuits protects the system of EMI.	[12]
Frequency-, PWM controlling	Varying the PWM parameter leads to a spreading of the frequency spectrum. The signal power is distributed over a wider frequency range. So a reduction of the high peak Amplitudes is achieved.	[13], [14]
Rise and fall time control	Reducing of the slew rate of the phase node signal leads to smaller di/dt and dv/dt values. So a noise reduction can be achieved.	[15], [16], [17], [18]

4.1 Limiting the EMI by limiting the slew rate of the phase node signal

The resonances are less excited by limiting the di/dt and the dv/dt on the switched signals. This means that the differential mode noise is reduced. Furthermore, the common mode signals are limited. Capacitive coupling is reduced by lower dv/dt values across the capacitors to the surrounding. Flux wrapping is reduced by lower di/dt values.

The limitation of the slew rate can be achieved by controlling the gate of the transistor switches. Reducing the switching speed can be achieved by limiting the gate current of the switch. The lower the gate current, the longer the time needed to charge the gate capacitance.

The simplest way to reduce the gate current is the use of a gate resistor [18]. Fig. 4.1 shows the schematic to reduce the slew rate using a gate resistor.

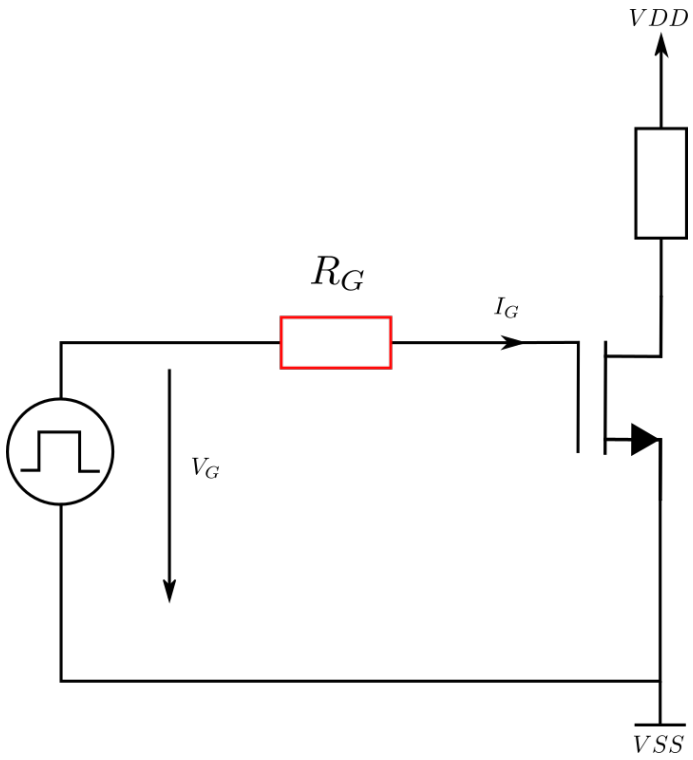


Figure 4.1: Slew rate reduction using a gate resistor for gate current limitation

The gate current resulting using a resistor as current limitation method is shown in fig. 4.3(b). The charging and discharging currents are heavily depending on the capacitance of the power transistors. This causes a large current peak at the beginning, followed by a decreasing current. The gate current stays relatively constant during the miller plateau. After the miller plateau, the current decreases further to zero. A big drawback of the gate resistor is that it limits the current during the whole transition. The current transition takes place during the time interval t_{ct}. During this time interval, the gate

current decreases from the peak at the beginning of the transition. This results in a rather high current slew rate. To achieve a reduction of the current slew rate, the current limit has to be lowered. The consequence is a lower current during the miller plateau and a slower voltage transition than needed. This results in significant switching losses in the transistor.

An improved solution is the use of constant current sources, which charge and discharge the transistor. This approach is shown in fig. 4.2. This approach optimizes the gate current. The current peak at the beginning is avoided. The current during the current and voltage transition are limited. During turn-on, the upper current source is connected to the gate of the pass device. A constant current charges the gate capacitance, and the transistor turns on. During turn-off, the current sink on the lower side of the schematic is applied to the gate of the transistor. The gate capacitance is discharged with a constant current. The lower the current, the slower the turn-on and turn-off transition.

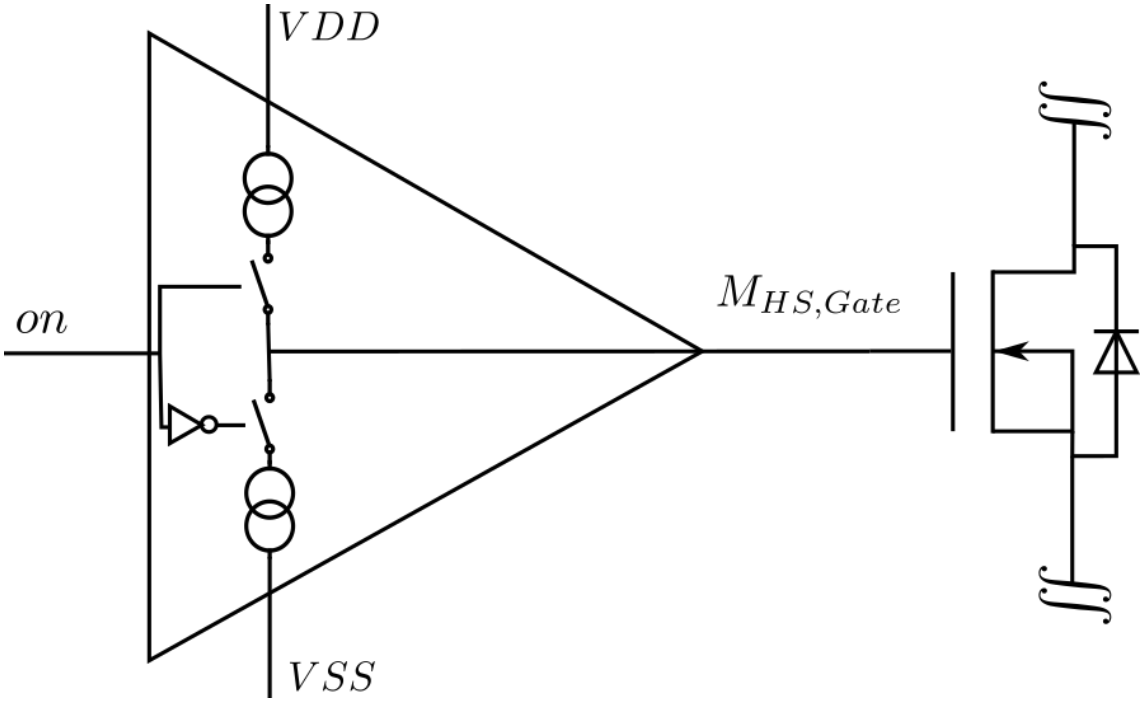
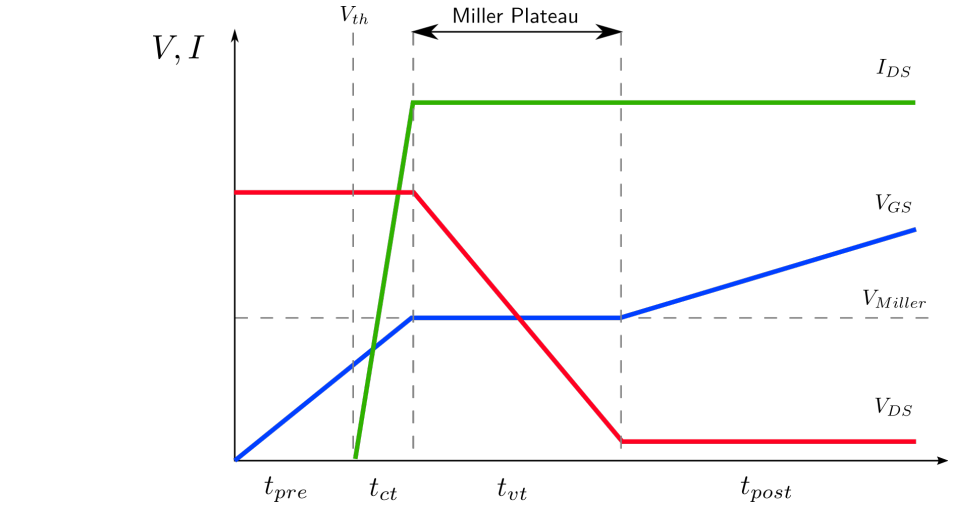


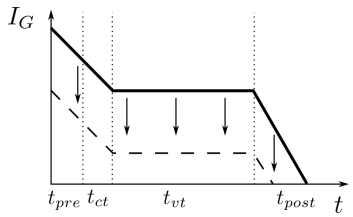
Figure 4.2: Slew rate reduction using current sources for gate current limitation. Shown is the high side FET's gate driver. Lx equals the source potential.

Fig. 4.3(a) shows the turn-on behavior of a MOSFET. The drain current through the transistor changes during the time interval t_{ct} the drain-source voltage of a transistor changes during t_{vt}. So the most efficient way to reduce the slew rate of the phase node signal is to reduce the gate current only during t_{ct} and t_{vt}. So the current slew rate decreases, the miller plateau gets longer, and the voltage transition time gets longer [15], [19]. So the desired gate driver is a gate driver with variable current sources, which provide a high current during t_{pre} and t_{post} to keep the phase delay low and a low current during t_{ct} and t_{vt} to decrease the current and voltage slew rate.

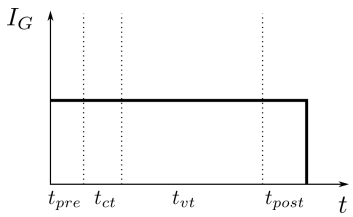
A comparison of the gate current over time of the three different gate drivers is presented in fig. 4.3.



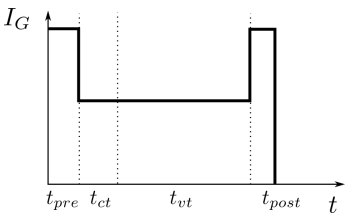
(a) Turn-on behavior of a MOSFET



(b) Gate resistor



(c) Constant gate current



(d) Reduced gate current during the current and voltage transition

Figure 4.3: Comparison of the different gate current limitation methods

4.1.1 Slew rate control driver for an inverting buck/boost converter

As long the inverting buck/boost converter is assumed to work in normal operation mode, with a positive inductor current, only the high-side transistor switching is relevant for the slew rate of the phase node, because during turn-off, the slope is determined by the coil current. In fig. 4.4, the timing diagram of the high side switch M_{HS}, the low side switch M_{LS}, the voltage V_{LX} on the phase node, and the currents during the different time intervals are shown. It can be observed that the voltage on the switching node starts to rise as soon as M_{HS} gets turned on. In the time, when the voltage on the phase node is rising, the capacitance of the switching node gets charged by the current I_{ch} through M_{HS}. The capacitance of the phase node is composed of the physical capacitance of the copper to ground, the parasitic capacitance of the inductor, and mainly the capacitance of the low side switch. The voltage slew rate of this slope can be influenced by the time, the high side transistor is in the miller region. The falling edge of the phase node signal starts as soon, as M_{HS} gets deactivated. During the dead time t_{d2}, the capacitance

on the phase node gets discharged due to the current I_{dch} through the inductor. The slew rate of the falling edge can be influenced by the time, M_{HS} is in the miller region, when M_{HS} gets deactivated. A slower reduction of the current through M_{HS}, leads to a slower slope on the phase node.

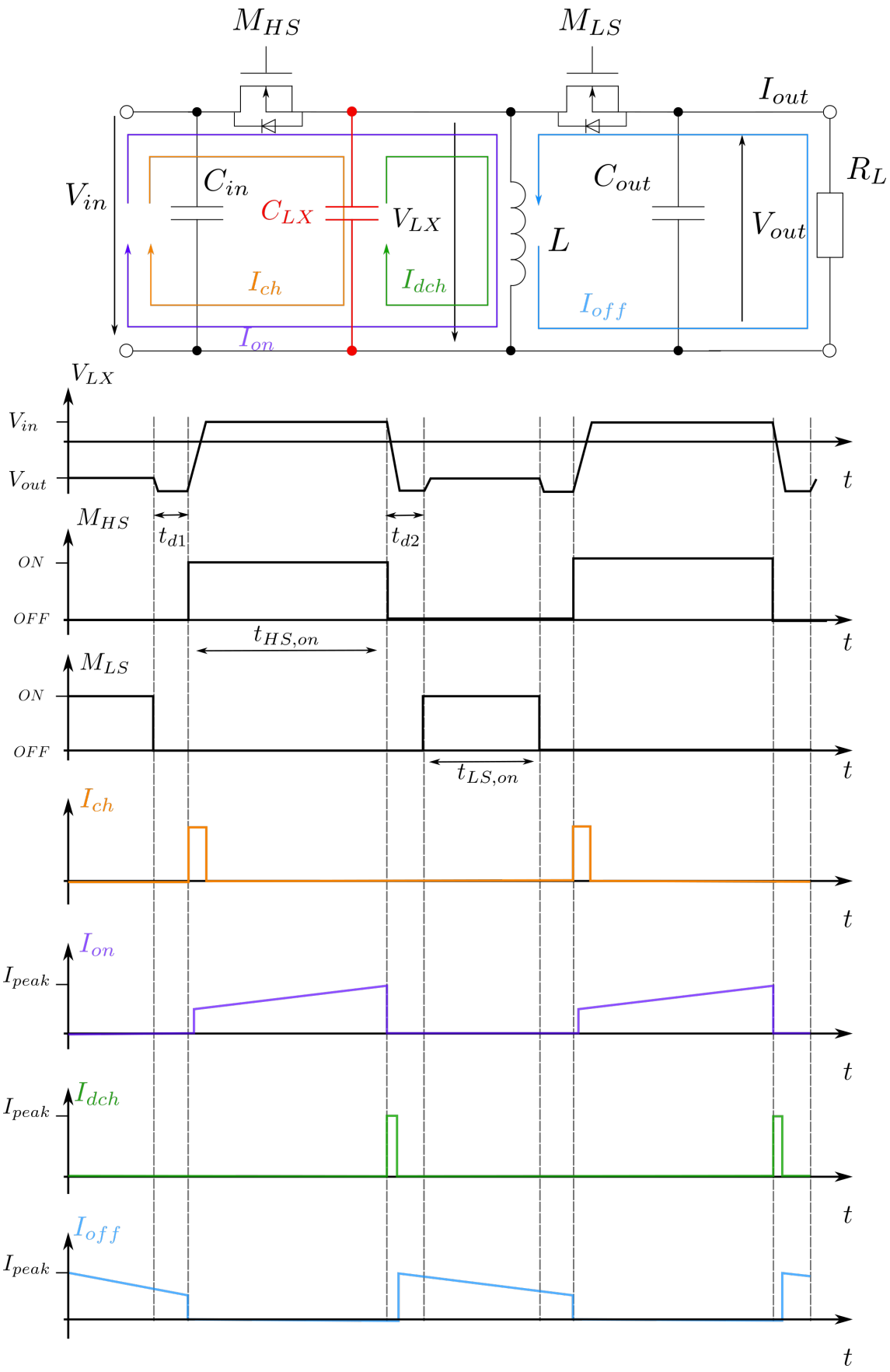


Figure 4.4: Timing diagram of the inverting buck/boost with two transistor switches

4.2 Conclusion

Many different approaches exist to reduce the noise in SMPS. To get the best noise performance, a combination of different methods should be applied to the circuit.

Reducing noise by reducing the slew rate was further investigated in this section. This method is treating the root cause and limits the creation of ringing. To realize a slew rate control for an inverting buck/boost converter, mainly the high side switch is responsible for the rising and falling slew rate. The low side switch influences the rising slope due to the reverse recovery of the body diode.

Chapter 5

Driver design and simulation

In this chapter, a driver is designed to reduce the EMI produced by an inverting buck/-boost converter. Dialog Semiconductor provided the simulation model of the converter, where the driver is tested.

5.1 The provided circuit

The converter topology of the provided model is an inverting buck/boost, but another transistor is used instead of the diode. So the diode losses during t_{off} are reduced. The diode losses in this topology occur only during the dead time, which means the time when no transistor is turned on, and the body diode of the low-side transistor is conducting. The topology is shown in fig. 5.1.

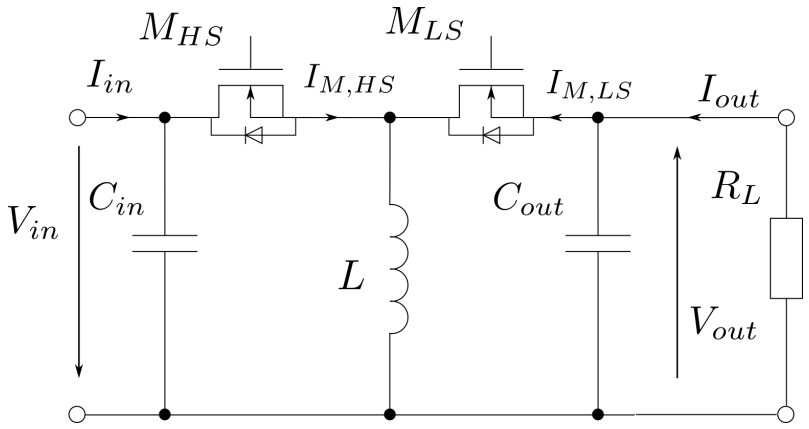


Figure 5.1: Inverting buck/boost converter using two transistors

The provided converter uses two NMOS transistors. This means to turn the high side transistor fully on, a voltage higher than the input voltage of the converter has to be applied to the gate. This is achieved using a bootstrap capacitor which gets charged during the t_{off}, and this bootstrap capacitance supplies the gate driver of the high side transistor during t_{on}.

The used gate drivers for the two transistors are similar. The driver is a push-pull stage, consisting of an inverter chain of different sizes. This gate driver is very fast, and before and after the transition, nearly no cross current is flowing.

To reduce the simulation time, the circuit is reduced to the most relevant parts. The logic and the control loops are removed from the circuit. Only the power stage is used to perform the simulations. The main parts of the power stage are the two pass devices and the gate drivers. Ideal voltage sources generate the PWM signal and the bootstrap voltage. To perform EMI measurements, LISNs are added to the input and output of the provided model.

5.1.1 Parasitics in the circuit

Some parasitics are included in the provided model to simulate the EMI of the converter. To model the parasitics due to the PCB layout, a 400 pH inductor and a 10 mΩ resistor are used on the converter's input and output trace. These values come from an estimation of the PCB, where the original chip is mounted. A 1 nH inductor inductor models the ESL of the input- and output capacitors and the ESR is modeled by a 100 mΩ resistor. The parasitics of the main inductor are already included in the simulation model. The inductor parasitics are modeled by a 2.2 pF capacitor and a 10 kΩ resistor in parallel and a 71 mΩ resistor in series of the inductor.

5.2 Simulation of the original circuit

Fig. 5.2 shows the most important time domain signals of the provided inverting buck/-boost converter. The converter model without any changes is mentioned as the original circuit in the following sections. The figure shows the gate voltages source of the high side and low side switches ($V_{G_{HS}}$ and $V_{G_{LS}}$), the drain currents of the two switches ($I_{D_{HS}}$ and $I_{D_{LS}}$), the signal on the phase node V_{LX} and the signals on the input and output port V_{in} and V_{out}. The in- and output voltages are measured on the terminals of the LISNs.

It can be observed that the high-frequency noise is generated during the transitions of the signal on the phase node. The transition from low to high on the phase nodes starts with the turn-on of the high side switch. The current through the high side switch charges the capacitance of the phase node, and the voltage on the node increases. The turn-off transition starts with the turn-off of the high side switch. The current flowing through the inductor discharges the capacitance of the phase node, and the voltage decreases.

During turn-on, the fast push-pull driver charges the gate with a gate current of 155 mA. This causes a fast transition of the gate-source voltage of the high side switch and in consequence a high current and voltage slew rate (3.97 $\frac{\text{A}}{\text{ns}}$, 7.1 $\frac{\text{V}}{\text{ns}}$) on the phase node. During the falling edge, the voltage slew rate is 8 $\frac{\text{V}}{\text{ns}}$, but the current slew rate is only 1 $\frac{\text{A}}{\text{ns}}$.

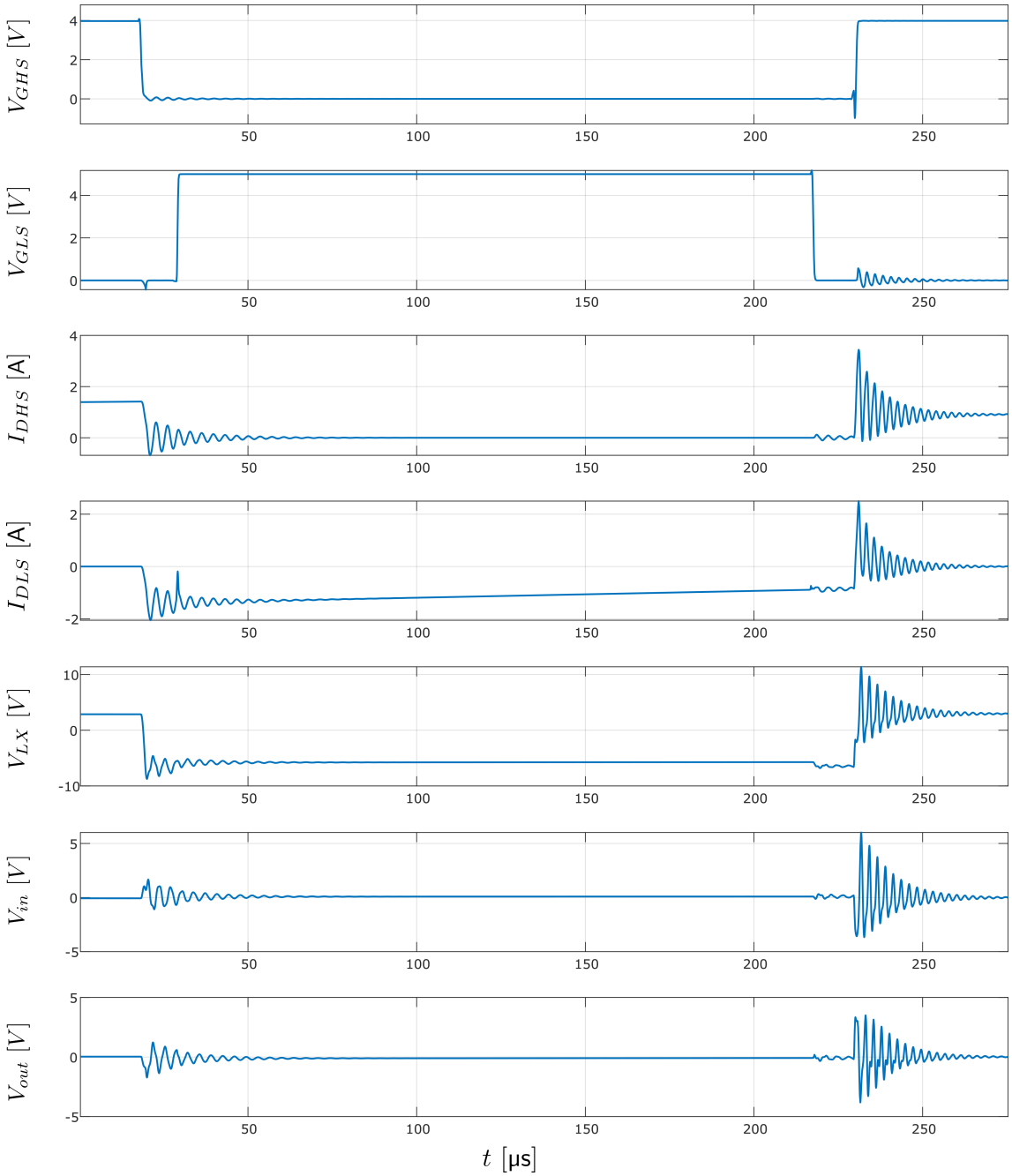


Figure 5.2: Time domain signals of the original converter circuit

Further details of the resonances are investigated by the voltage on the phase node. Fig. 5.3 shows the signal on the phase node. Three resonances are observed. Using the STFFT, the resonances can be assigned to a specific time. A 291 MHz resonance during turn-off, during turn-on a 432 MHz, and an 865 MHz resonance can be found. Parasitic resistors dampen the resonances in the ringing loop. The ringing during turn-on is damped by the ESR of the in- and output capacitors, the R_{on} of the high side switch, and the R_{OSS} of the low side switch. The turn-off ringing is damped by the ESR of the

in- and output capacitors, the R_{on} of the low side switch, and the R_{OSS} of the high side switch. The Q-factor of the ringing during turn-on is 12.76 and of the ringing during turn-off 8.3.

In steady-state, the voltages across the transistors when they are blocking is constant. Due to that, a fixed value of C_{OSS} can be assigned to the switches while they are blocking. The output capacitance of the low side and the high side switch in the blocking state are simulated. The high side switch has an output capacitance of $C_{OSS_{HS}} = 92.4\,\text{pF}$, and the low side switch has an output capacitance of $C_{OSS_{LS}} = 51.2\,\text{pF}$. The loop inductance is composed of the inductance due to the PCB layout $(800\,\text{pH})$ and the ESL of the input and output capacitors 2 nH.

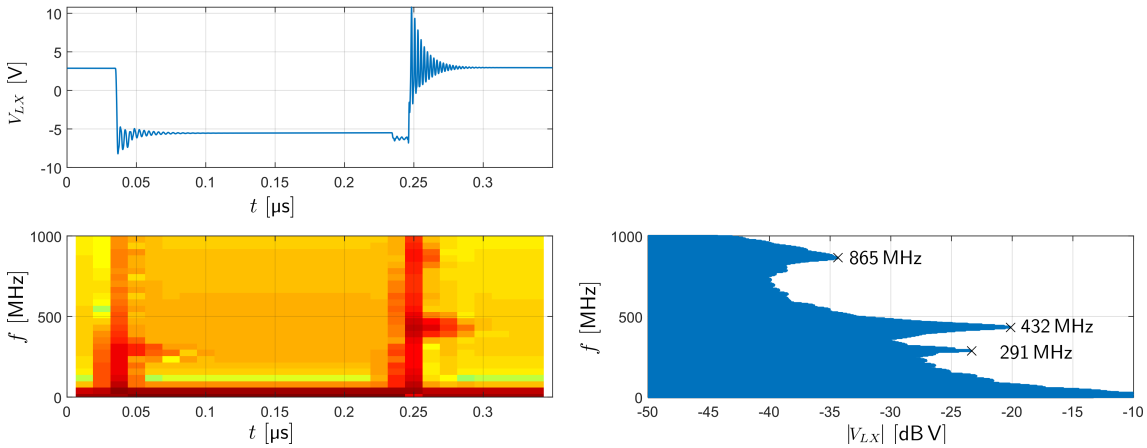


Figure 5.3: Time domain, STFFT, and frequency domain signal on the input port

The turn-on resonance is given by the $C_{OSS_{LS}}$ and the loop inductance of 2.8 nH. The turn-on frequency is calculated in (5.1).

$$f_{turn-on} = \frac{1}{2 \cdot \pi \sqrt{L \cdot C_{L_{main}}}} = \frac{1}{2 \cdot \pi \sqrt{2.8\,\text{nH} \cdot 51.2\,\text{pF}}} = 420\,\text{MHz} \qquad (5.1)$$

The turn-off resonance is given by the $C_{OSS_{HS}}$ and the loop inductance of 2.8 nH. The turn-off frequency is calculated in (5.2).

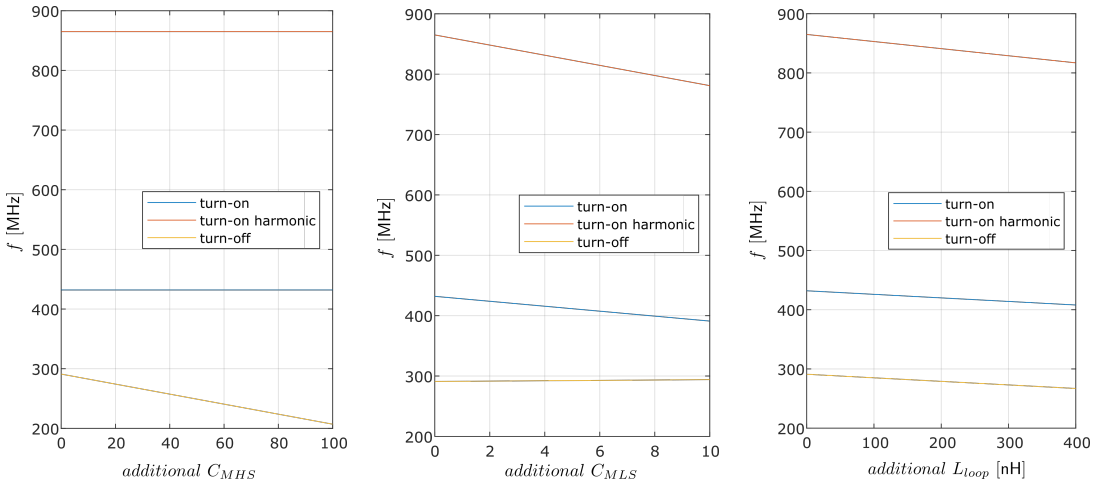
$$f_{turn-off} = \frac{1}{2 \cdot \pi \sqrt{L \cdot C_{L_{main}}}} = \frac{1}{2 \cdot \pi \sqrt{2.8\,\text{nH} \cdot 92.4\,\text{pF}}} = 312\,\text{MHz} \qquad (5.2)$$

The 865 MHz resonance is the first harmonic of the turn-on ringing. The frequency is double the frequency of the turn-on ringing frequency.

The behavior of the circuit is investigated by varying the loop inductance and the transistor capacitance in simulation.

To confirm that the theories presented in chapter 3 are valid also for this type of converter, the experiments carried out on the simple simulation model are reproduced on

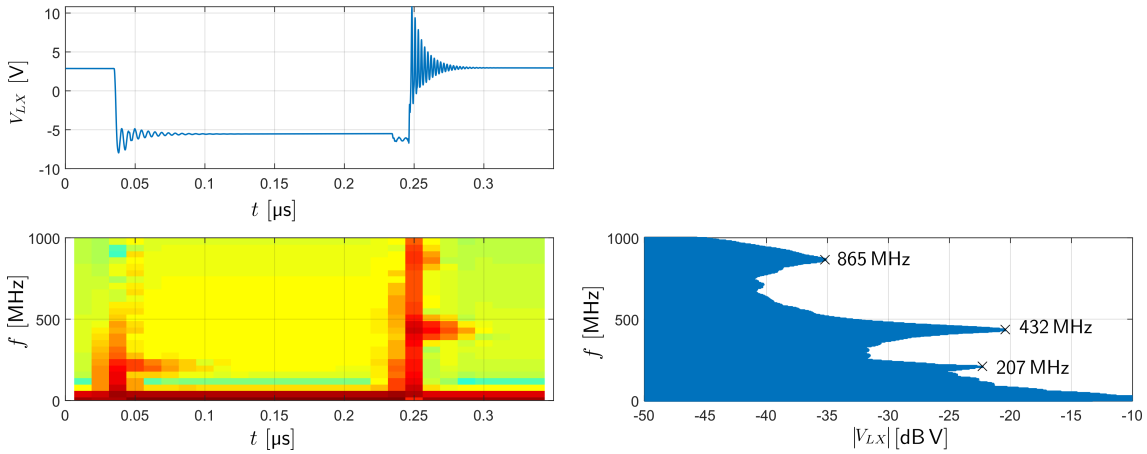
the provided circuit. The transistor capacitance is increased on the high side switch and on the low side switch by connecting a capacitor in parallel. Further, the loop inductance is increased. Figures 5.4, and 5.21 show the outcome of the three experiments.



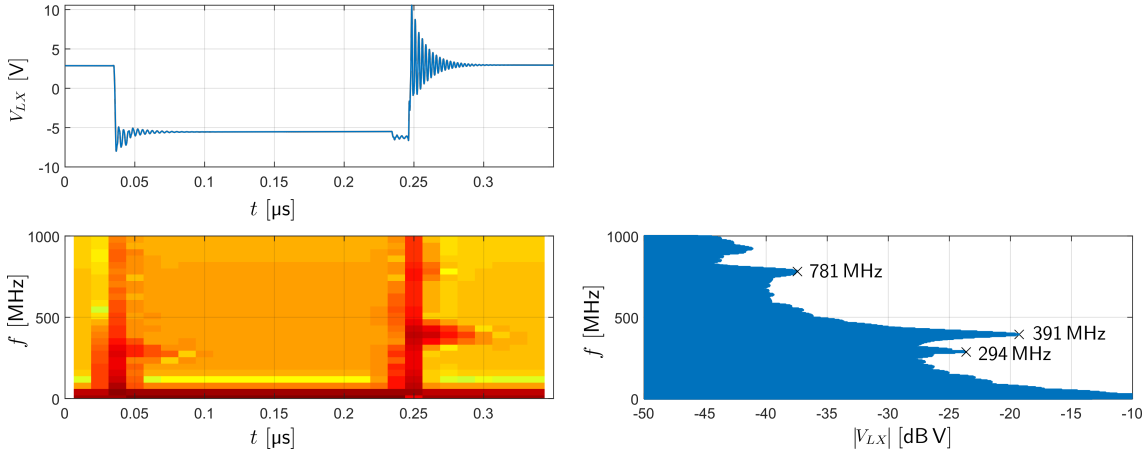
(a) Additional capacitance in parallel to the high side switch (b) Additional capacitance in parallel to the low side switch (c) Additional loop inductance

Figure 5.4: Changes of the ringing frequency due to varying loop inductance and switch capacitance

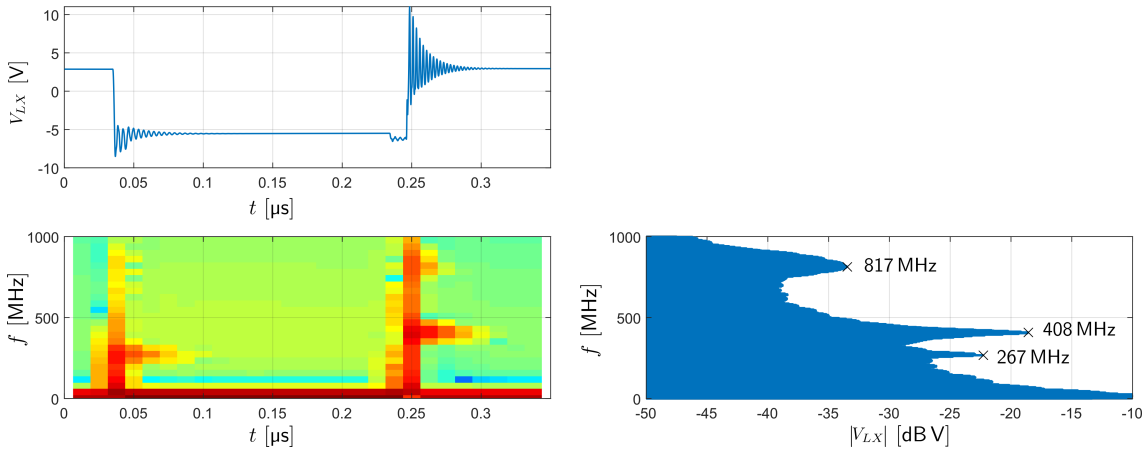
The outcome of the experiments confirms the validation of the presented theories in chapter 3. By increasing the capacitance of the high side transistor, the turn-off resonance gets shifted to lower values. Increasing the capacitance of the low side switch is similar to increasing the diode capacitance in the circuit of chapter 3. The turn-on frequency gets shifted to lower frequency levels. By increasing the loop inductance, both the turn-on and the turn-off frequency are shifted to lower frequency levels.



(a) Increased transistor capacitance on the high side switch



(b) Increased transistor capacitance on the low side switch



(c) Increased loop inductance

Figure 5.5: Parasitic variation on the converter circuit

5.3 Specifications of the driver

A driver should be designed for reducing the electrical noise of the inverting buck/boost converter. The driver circuit should reduce the EMI by slowing down the slew rate of the switched current and the slew rate of the phase node voltage. The slew rate should be programmable. Besides the losses of the driver should be kept as small as possible.

5.4 Driver simulation test bench

To simulate the driver and verify the functionality, a test bench is set up. The test bench is a simple version of the converter topology. For the low side switch, the original driver is used. The high side driver is replaced by the driver, which should be tested. No additional parasitics are added to the test bench. The main advantage of the test bench is the much faster simulation speed and the short time to reach the steady-state. Fig. 5.6 shows the used test bench.

After the functionality of the designed driver circuit is verified, the driver circuit is placed into the converter circuit, where the EMI investigations are made.

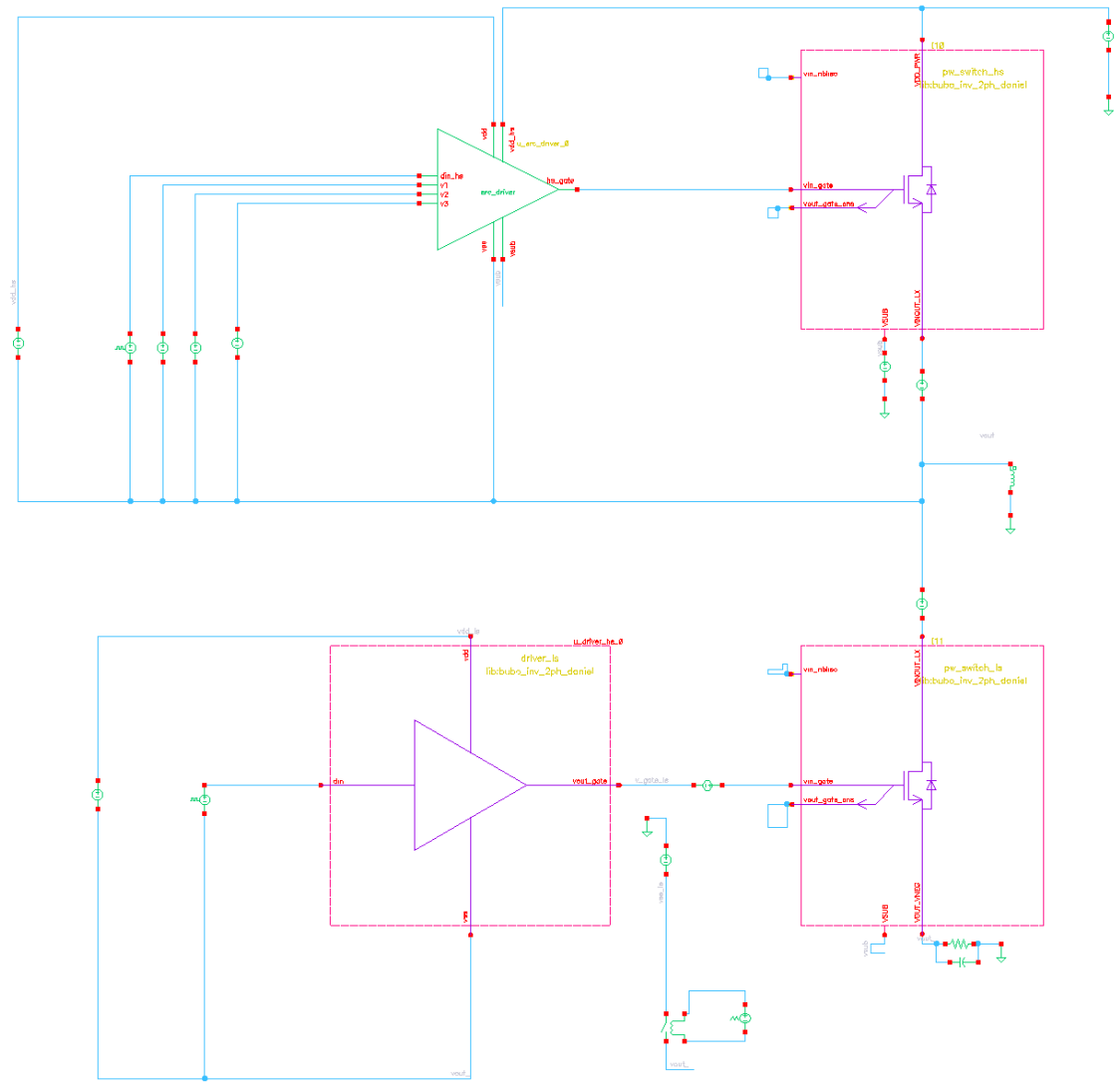


Figure 5.6: Schematic of the used driver test bench

5.5 Driver design using different constant gate currents

The easiest way to reduce the slew rate using a gate driver, is to reduce the gate current of the pass device. Due to the lower gate current, the time to charge the gate capacitance gets longer, so the transition from low to high takes longer. The schematic in fig. 5.9 shows the basic idea of the slew rate driver. This approach has been implemented using two ideal current sources. One current source has been used to charge the transistor's gate and turn it on The other current source is used to discharge the gate and turn it off. Making the current sources variable gives the opportunity to increase or decrease the slew rate.

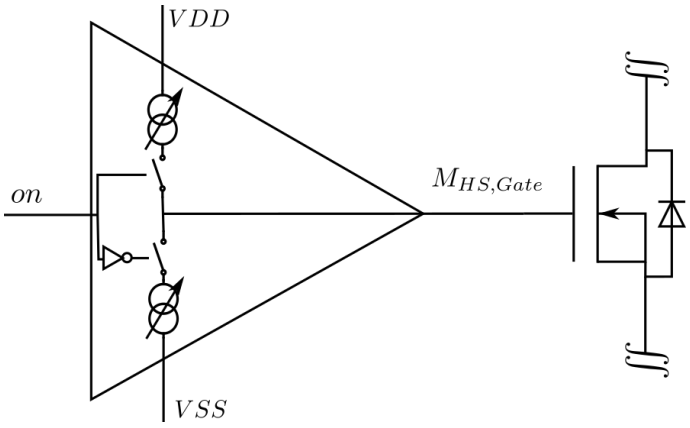


Figure 5.7: Gate driver with two variable current sources, setting a constant gate current

5.5.1 Implementation using ideal elements

The simulation results of the driver implementation using ideal components are shown in fig. 5.8 . This is done to validate the principle. The driver is implemented by an ideal current source and ideal diodes in parallel to prevent the output of non-realistic voltages. One current source is used to charge the gate, and the other to discharge the pass device. Ideal switches are used to switch between the two current sources. As expected, the peaks in the frequency spectrum are reduced.

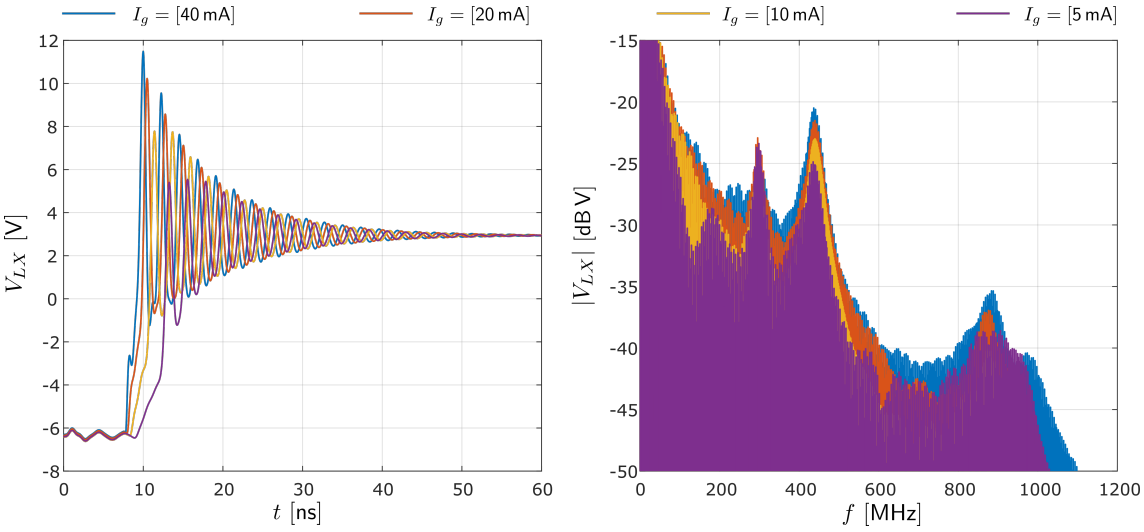


Figure 5.8: Simulation results of the slew rate driver using ideal components

5.5.2 Implementations using transistor models

Since limiting the gate current turned out as an acceptable solution. The driver is modeled with transistor models. The programmable current sources are implemented by three weighted current mirrors in parallel. Each can be activated and deactivated by control bits V_1, V_2 and V_3. The simulation results implemented driver solution is shown in fig. 5.9.

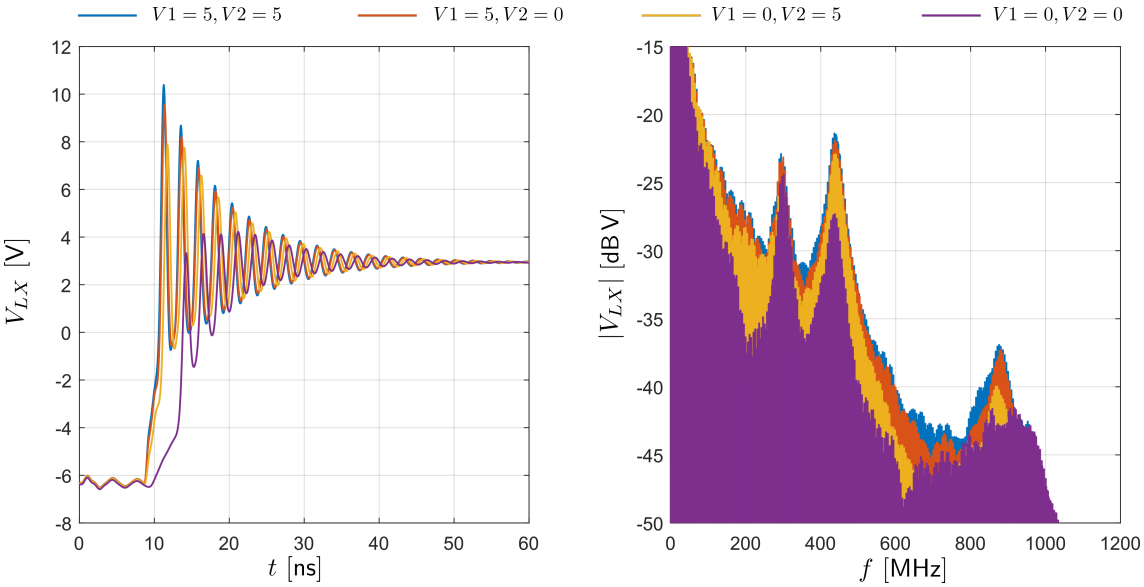


Figure 5.9: Simulation results of the constant gate current slew rate driver. Transistor model implementation

With this driver's slowest slew rate setting, a significant 8 dB reduction of the turn-on ringing is achieved. But due to this measure, the ratio from output to input power is decreased by 5.6 %. Due to the large reduction of efficiency is this driver circuit not desirable for the use in SMPS.

5.6 Slew rate control driver using the gate voltage as feedback signal

To design an efficient gate driver, which can decrease the gate current only during the critical periods, when the current transition and the voltage transition happen, a driver concept with feedback is needed. The feedback is needed to obtain the point in time when the gate currents have to be reduced and can be increased.

5.6.1 The basic principle of the slew rate driver

Fig. 5.10 shows the block diagram of the designed driver with programmable slew rate control. The driver is built up of three different blocks:

- Edge rate control (ERC)
- Strong push-pull driver
- Miller plateau detector

The edge rate control is only active during the switching events. This block controls the slew rate. The strong push-pull driver is activated right after the transition is finished.

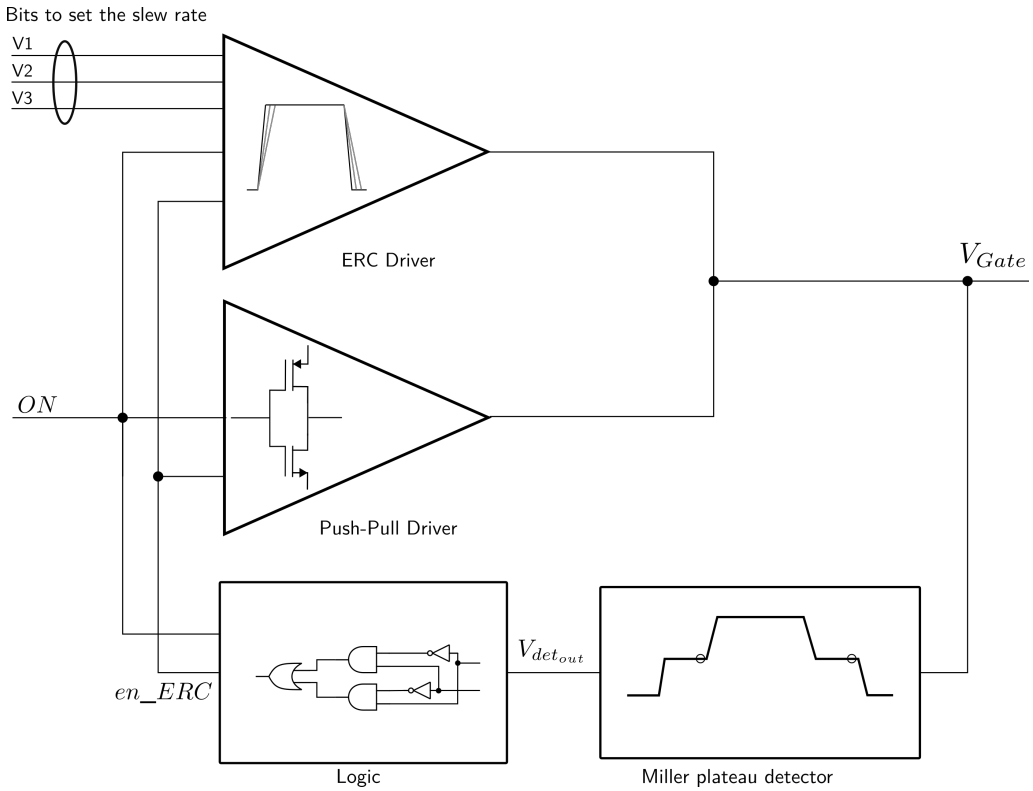


Figure 5.10: Block diagram of the slew rate driver

This driver is needed to switch the high side transistor fully on and off. Because of the architecture of the ERC. The output of the ERC, which is controlling the gate, cannot reach the supplies of the driver. A detector is needed to determine the periods in which either the ERC or the push-pull driver should be active. The detector detects the end of the Miller plateau during turn-on and turn-off. The ERC is active from the beginning of the switching event until the end of the Miller plateau. After the Miller plateau, the voltage on the switching node has settled, and the push-pull stage brings the gate of the pass device to the positive or negative supply of the driver circuit.

5.6.2 Edge rate control (ERC)

The designed circuit is proprietary to Dialog Semiconductor. Therefore the schematic is not published in this thesis. Fig. 5.11 shows the symbol of the edge rate control block. The ERC block has five inputs and one output. The inputs V_1, V_2, and V_3 are used to set the slew rate. The input ON signalizes the driver to turn on when it is high or to turn off, when it is low. en_{ERC} is the enable bit of the driver. The driver is only active, when the bit is active. The enable bit is only set during the tun-on and tun-off transition. The output V_{Gate} of the circuit is connected to the gate of the pass device. The gate current created by the circuit is a constant current, which is decreased during the Miller plateau.

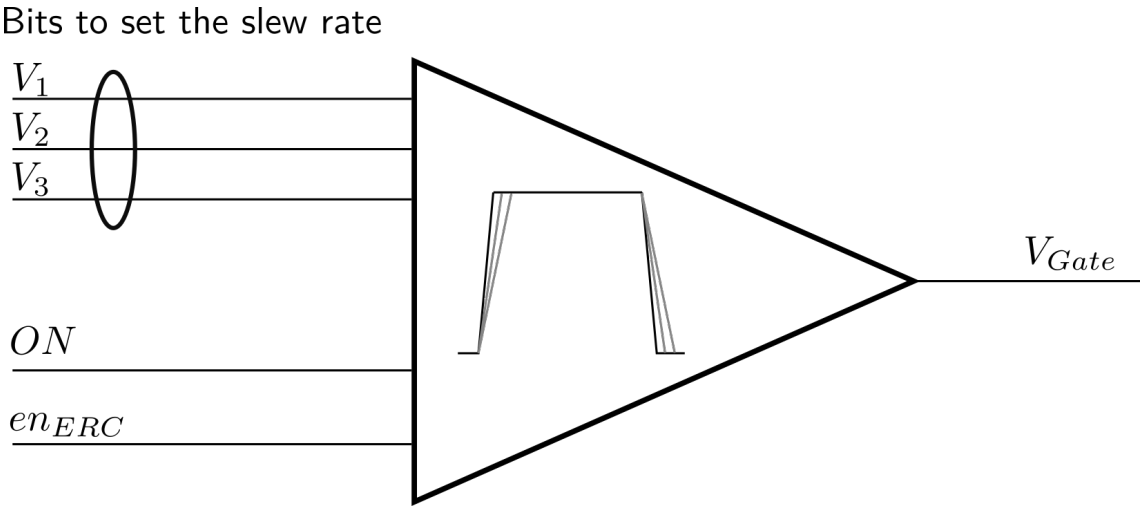


Figure 5.11: ERC driver

5.6.2.1 Functional principle of the ERC

Figure 5.12 shows a qualitative timing diagram of the turn-on transition using the ERC Driver. The transition is shown for two different settings of the slew rate. The dashed line represents the transition with a faster setting. The driver produces a constant output current, which is decreased during the Miller plateau. With slower slew rate settings, the output current has a lower value. It can be seen that the higher gate current during the Miller plateau leads to a faster charging of the Miller capacitance and forces a faster transition time. In addition the current slew rate is affected by the driver settings. Because of the higher constant current the time between V_{th} and the begin of the Miller plateau gets shorter. Also the time until the gate voltage reaches the threshold voltage V_{th} and the time during the increasing of the gate voltage from the Miller level to the positive supply are shorter.

5.6.2.2 Design of the circuit

Since the design aimed to elaborate a circuit concept and not to produce a circuit that is tape-out ready, the circuit is designed as a kind of hybrid circuit. This means some ideal sources are placed in the circuit and not all details are designed on transistor level.

5.6.3 Push-pull driver

Fig. 5.13 The push-pull driver is used to clamp the gate voltage of the pass device to the positive or negative supply voltage of the driver. This driver stage consists of an inverter chain with increasing driver strength. So after the voltage transition on the phase node is finished, the push-pull stage switches on, and the gate voltage is increased rapidly from the Miller level to the positive or negative supply voltage.

Besides the advantage, that the driver's output can reach the positive and negative supply voltage, the driver losses in the steady-state are much less than in the ERC stage.

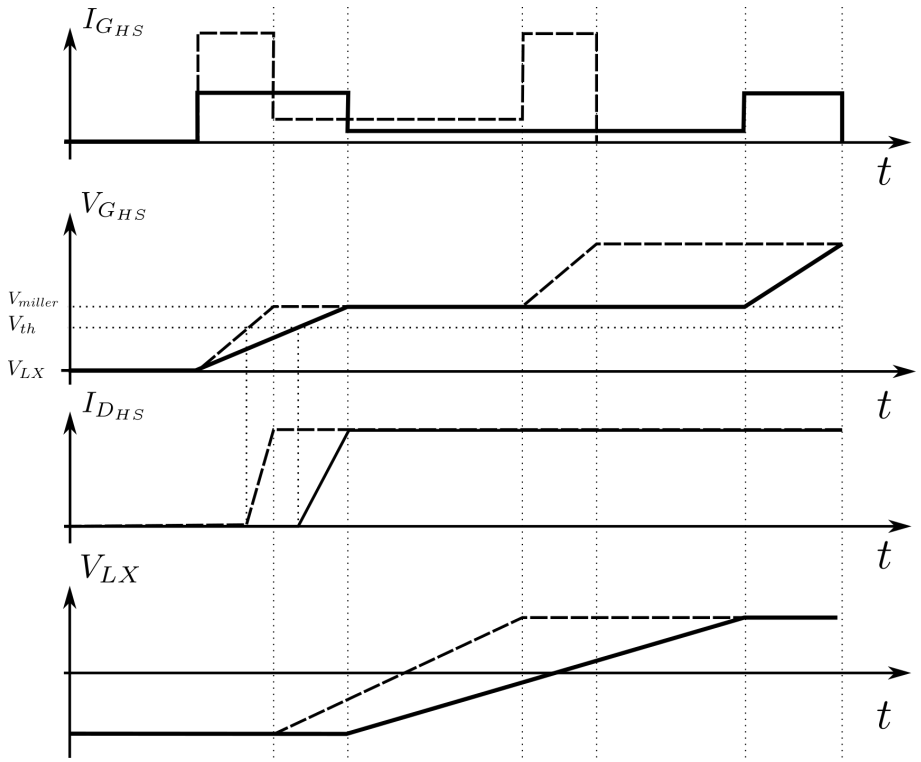


Figure 5.12: Timing diagram of the turn-on transition, using the ERC with two different currents

Due to the inverter structure, nearly no cross current is flowing in steady-state. However, the ERC stage produces significant losses due to the needed biasing networks.

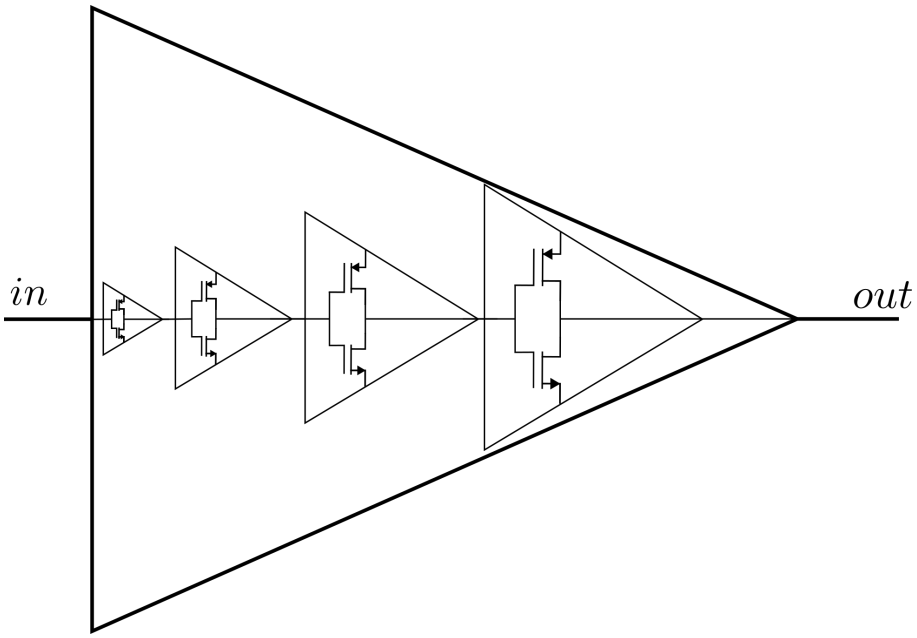


Figure 5.13: Basic structure of the push-pull driver

5.6.3.1 Functional principle of the push-pull driver

As at the output of the push-pull stage, a high current is needed, the last output stage has to be designed with relatively large devices. The control circuit is not strong enough to drive the large inverter. So an inverter chain is designed from inverters with increasing sizes and so with increasing strength.

5.6.4 Miller plateau detector

The Miller plateau detector is an essential block in the slew rate driver. The detector senses the gate voltage and detects the end of the Miller plateau. So the end of the voltage transition on the phase node is detected.

5.6.4.1 Functional principle of the Miller plateau detector

The designed circuit is proprietary to Dialog Semiconductor. Therefore the schematic is not published in this thesis. Fig. 5.14 shows the symbol of the Miller plateau detector. The circuit senses the gate voltage V_{Gate}. The output of the circuit rises to high, at the end of the Miller plateau during turn-on and falls to low at the end of the Miller plateau during turn-off. The timing diagram of the input and output of the circuit are shown in fig. 5.15.

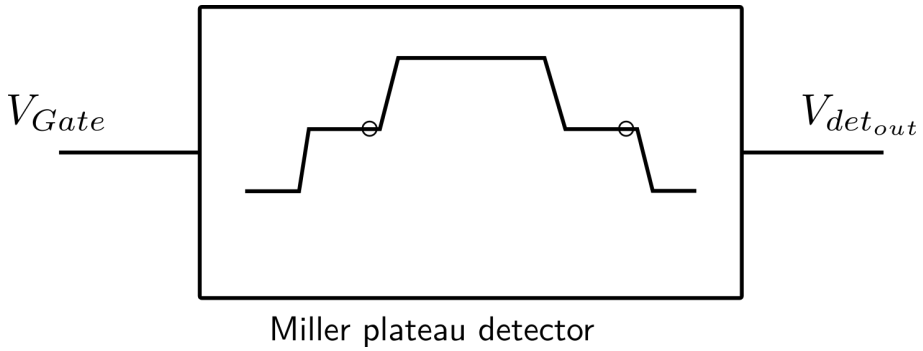


Figure 5.14: Basic schematic of the Miller plateau detector

Additional logic is needed to switch between the ERC and the push-pull driver. The logic circuit and the timing diagram are shown in fig. 5.16. The ERC enable signal en_ERC is high when the ON signal is high, and the output of the detector $V_{det_{out}}$ is low, or the ON signal is low, and $V_{det_{out}}$ is high. This logic ensures, that the ERC driver is only active, from the beginning of the transition until the end of the Miller plateau.

5.6.4.2 Simulation Results

The ERC driver is simulated using the driver test bench. Fig. 5.17 shows the simulation results of the test bench, using the ERC driver for the high side transistor. The gate voltage $V_{G,HS}$, the phase node voltage V_{LX}, the gate current $T_{G,HS}$, the drain current $I_{D,HS}$ and the enable ERC signal en_{ERC} are shown. The simulation is performed with

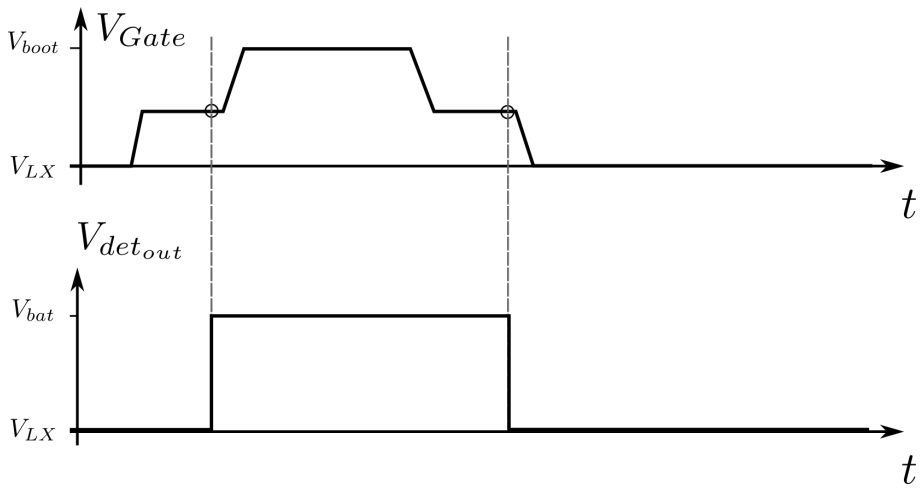


Figure 5.15: Signals in the Miller plateau detector during turn-on and turn-off

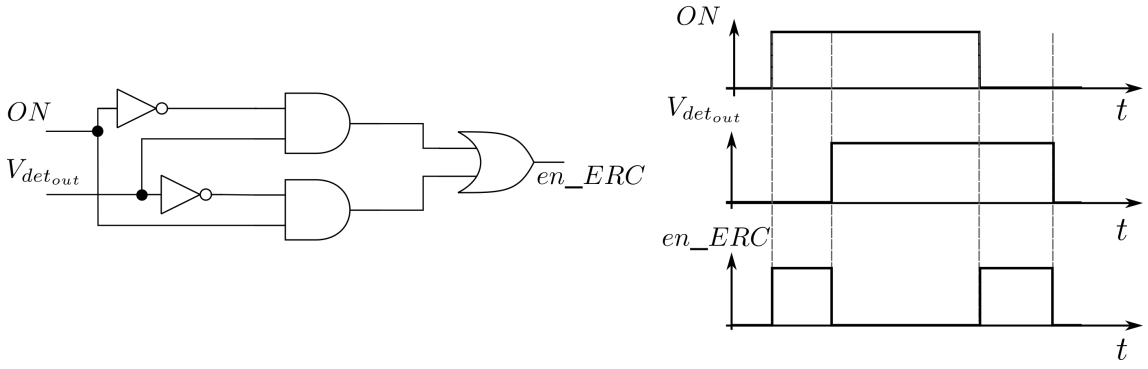


Figure 5.16: Additional logic, to activate the ERC driver

different current settings of the current $I_{DAC_{HI}}$. The current settings are changed by the bits V_1, V_2, and V_3.

Fig. 5.17 shows the turn-on transition of the high side switch. Due to the pre-bias, the switch's threshold voltage reached with all current settings nearly at the same time. The drain current rises until $V_{G,HS}$ hits the Miller level. Due to the different current settings, the current slew rate is decreased. During the Miller plateau, the voltage transition on the phase node takes place. During this time, the gate current $I_{G,HS}$ is further reduced by the ERC circuit. The different current settings lead to different rise times. When the voltage transition is finished, the en_{ERC} signal toggles to low, the push-pull driver is activated, and the ERC circuit is deactivated. The push-pull driver pushes the gate to the bootstrap voltage. It can be observed that the en_{ERC} signal not directly at the end of the Miller plateau, but a bit later. This is because of the delay of the logic gates and the threshold of the Miller detector. By varying these parameters, the timing when the push-pull driver is connected can be improved.

The differences in current and voltage slew rate achieved with the different current settings are listed in table 5.1.

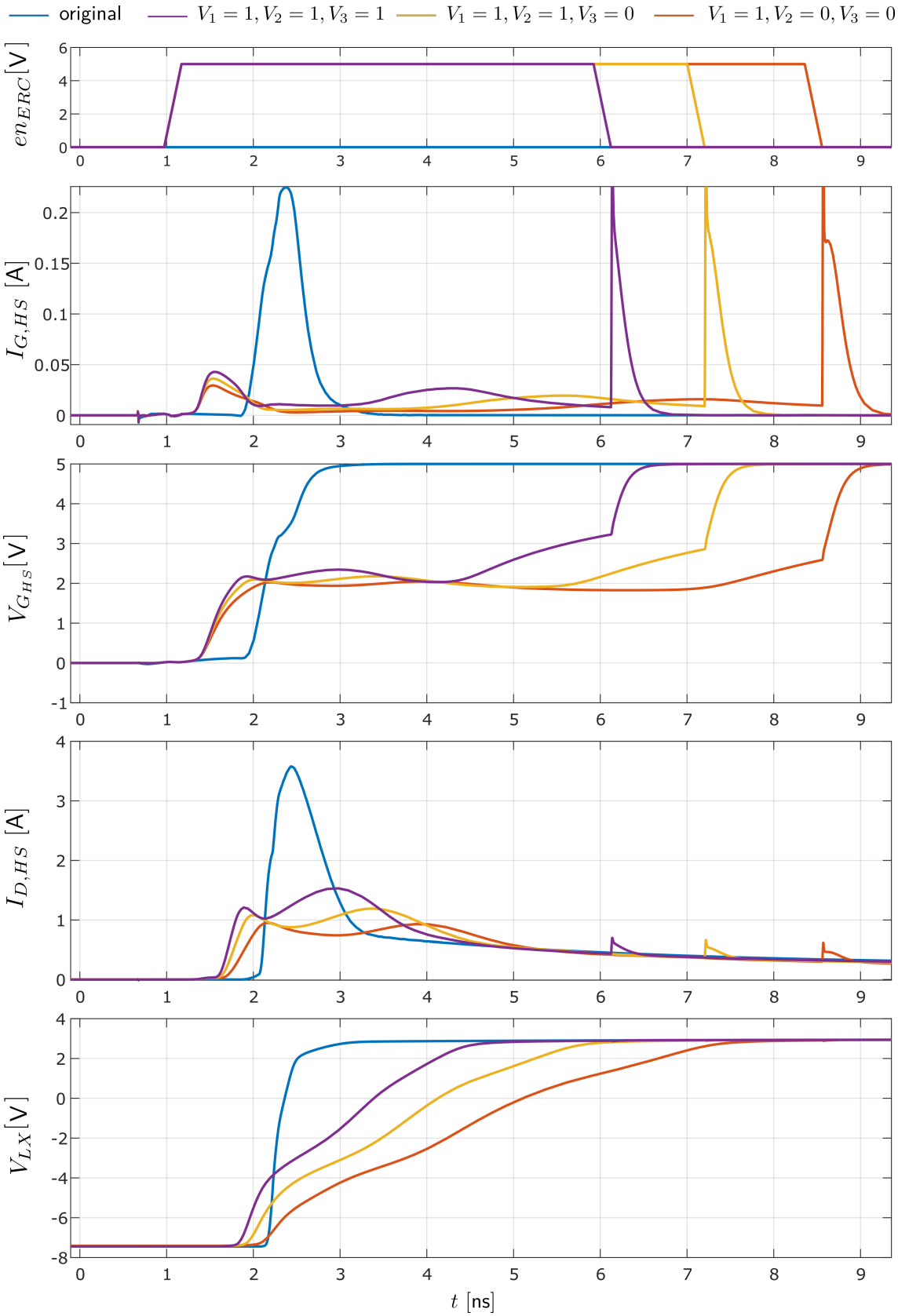


Figure 5.17: Simulation results of the ERC driver, using the driver test bench.
(Steep edges in $I_{G,HS}$ due to an ideal switch in the simulation model switching between ERC and push-pull driver)

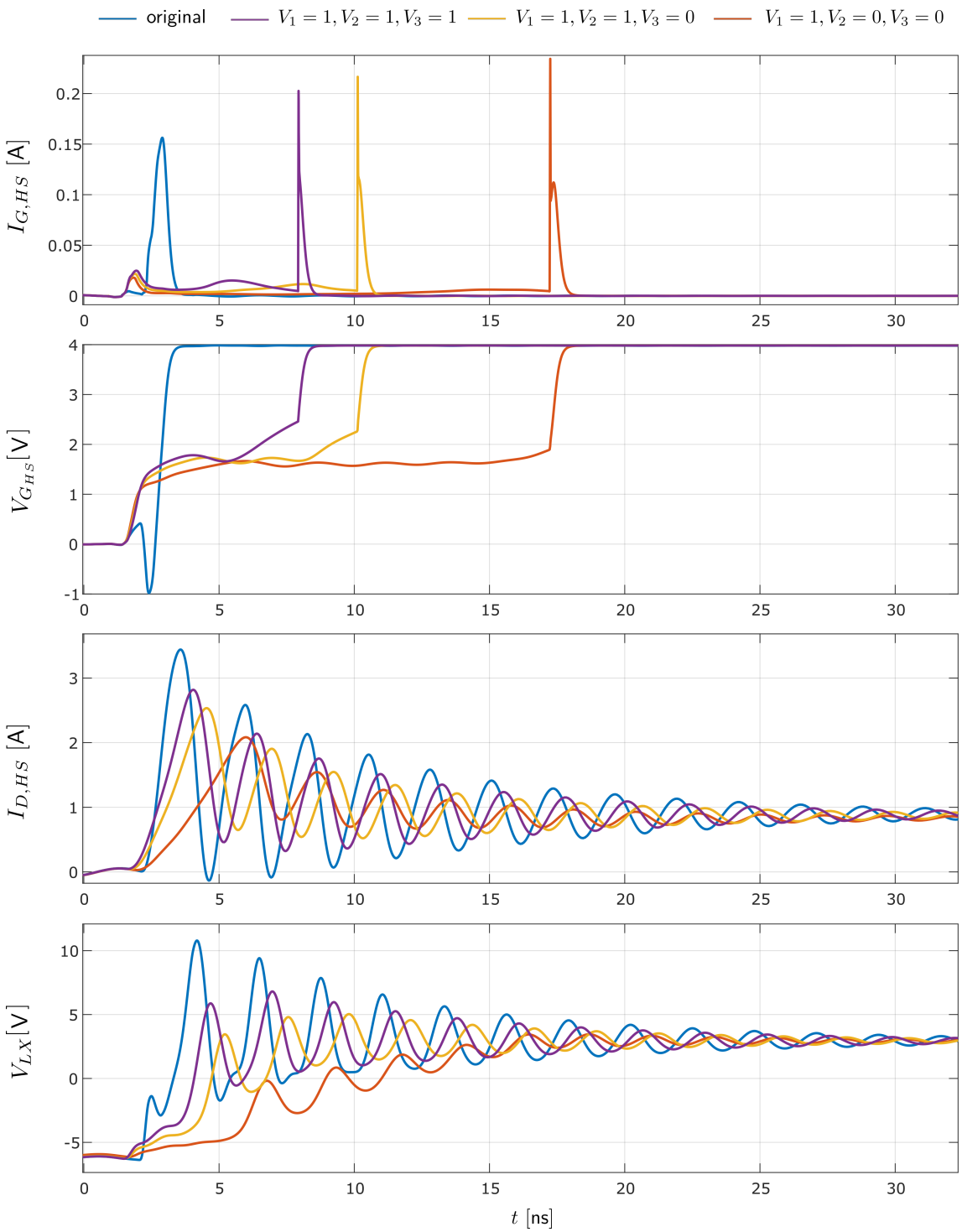


Figure 5.18: Simulation results of the ERC driver included in the converter model
(Steep edges in $I_{G,HS}$ due to an ideal switch in the simulation model switching between ERC and push-pull driver)

Table 5.1: Slew rates of the phase node and the high side drain current simulated with different settings of the ERC (test bench)

Setting	Voltage Slew Rate $[\frac{V}{ns}]$	Current Slew Rate $[\frac{A}{ns}]$
Original Driver	31.5	14.7
$V_1 = 1, V_2 = 1, V_3 = 1$	3.9	5.2
$V_1 = 1, V_2 = 1, V_3 = 0$	2.7	3.2
$V_1 = 1, V_2 = 0, V_3 = 0$	1.96	1.6

Table 5.2: Resulting slew rates using different gate driver settings (included in the converter model)

Setting	Voltage Rise Time [ns]	Voltage Slew Rate $[\frac{V}{ns}]$	Current Rise Time [ns]	Current Slew Rate $[\frac{A}{ns}]$
Original Driver	0.6	8.5	0.49	3.97
$V_1 = 1, V_2 = 1, V_3 = 1$	1	5.12	1.06	1.49
$V_1 = 1, V_2 = 1, V_3 = 0$	2.5	2	1.80	1.07
$V_1 = 1, V_2 = 0, V_3 = 0$	6	0.83	2	0.63

Fig. 5.18 shows the simulation results of the ERC driver included in the provided simulation model. Only the turn-on transition is shown. The turn-off transition shows nearly no difference in respect to the original driver. To treat also the falling edge, the driver design has to be improved.

A clear difference in drain current slew rate and phase voltage slew rate can be observed on the rising edge. The achieved slew rates are listed in table 5.2. At the beginning of the voltage transition, a flat voltage slope is observed. During this time, the current transition takes place. Smaller slew rate settings lead to a longer duration of this flat voltage slope.

The plot of the gate current shows a high current peak at the end of the voltage transition. This is caused by the switch from the ERC driver to the push-pull driver. The power-down of the push-pull driver is realized using an ideal switch of the simulation environment. Therefore is the rising edge of the second peak extraordinary steep.

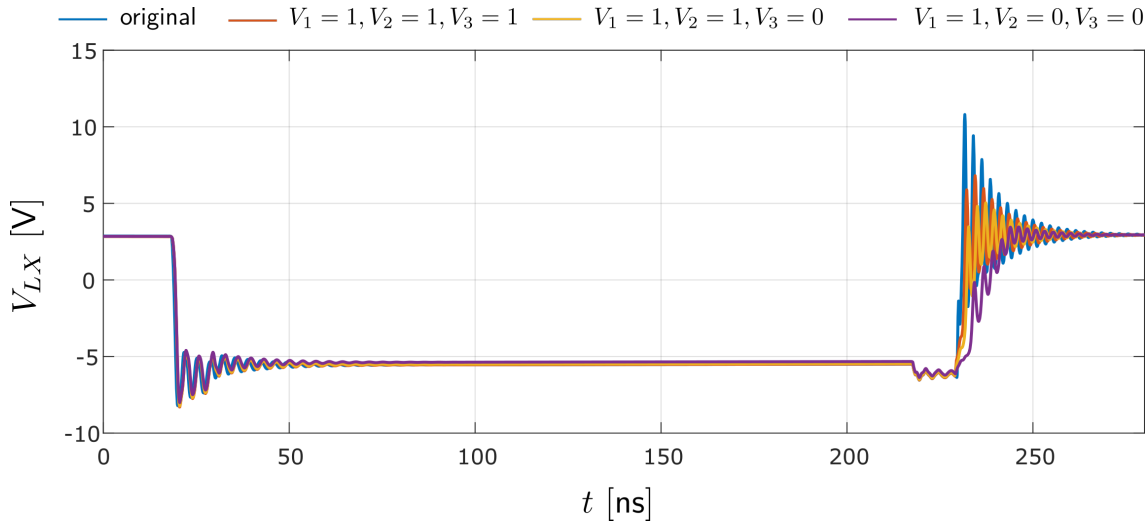
Fig. 5.19(a) shows the turn-off and the turn-on transition on the phase node in time domain. It can be observed that the falling edge is not noticeably influenced by the driver's different settings. This is because of the coil current, which is the main reason for the falling slew rate. For further reduction of the noise, during turn-on, the ERC driver's design has to be modified so that the gate of the high side switch gets slower discharged.

During the rising edge, a reduction of the ringing is observed. The smaller the current

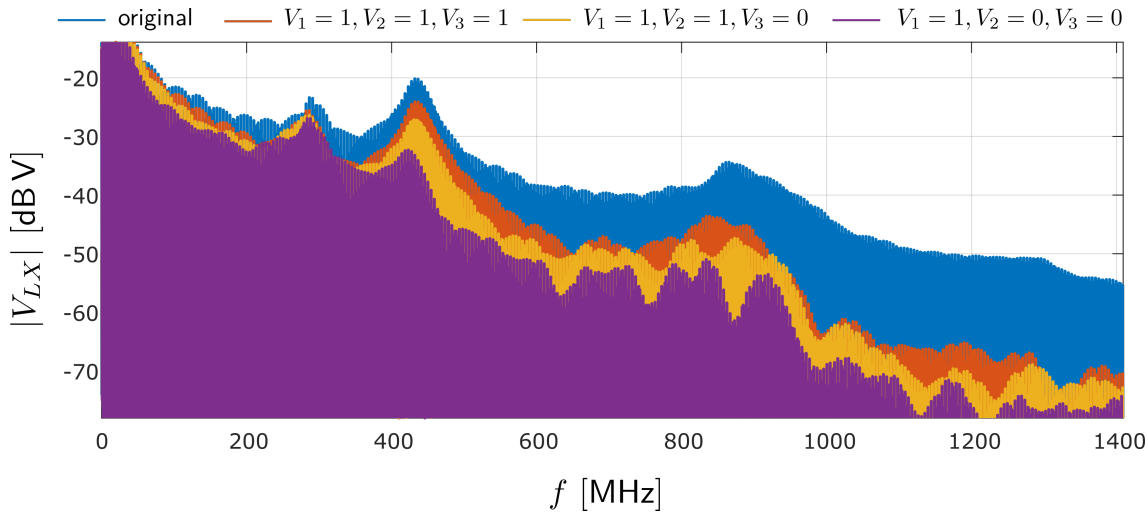
setting, the lower the ringing amplitude.

Fig. 5.19(b) shows the phase node signal in the frequency domain. As expected, the frequency domain signal confirms only a little reduction during the falling edge. The 300 MHz peak is on the same value with the lowest current setting as with the original driver circuit. A significant improvement is observed in the higher frequency range above the turn-off ringing frequency. In contrast to the original driver, the 420 MHz turn-on ringing is damped by 20 dB using the slowest slew rate setting.

Not only the turn-on and turn-off ringing are damped, also the noise behavior of the whole upper frequency range is improved.



(a) Time domain signal



(b) Frequency domain signal

Figure 5.19: Frequency domain signal and time domain signal on the phase node during turn-off and turn-on

Fig. 5.20 shows the simulation results during turn-on in detail. The gate voltage, the

phase node voltage, the input- and the output voltage on the LISNs in time domain are shown during turn-on. The phase node voltage, the input- and output voltage are shown in frequency domain. The simulations show a comparison between the original gate driver, and the ERC driver, with different current settings. In time and frequency domain, a clear reduction of the 420 MHz turn-on ringing is observed. The gate voltage shows the increasing Miller plateau duration caused by smaller gate currents. The slowest setting generates a reduction of the turn-on ringing of 20 dB.

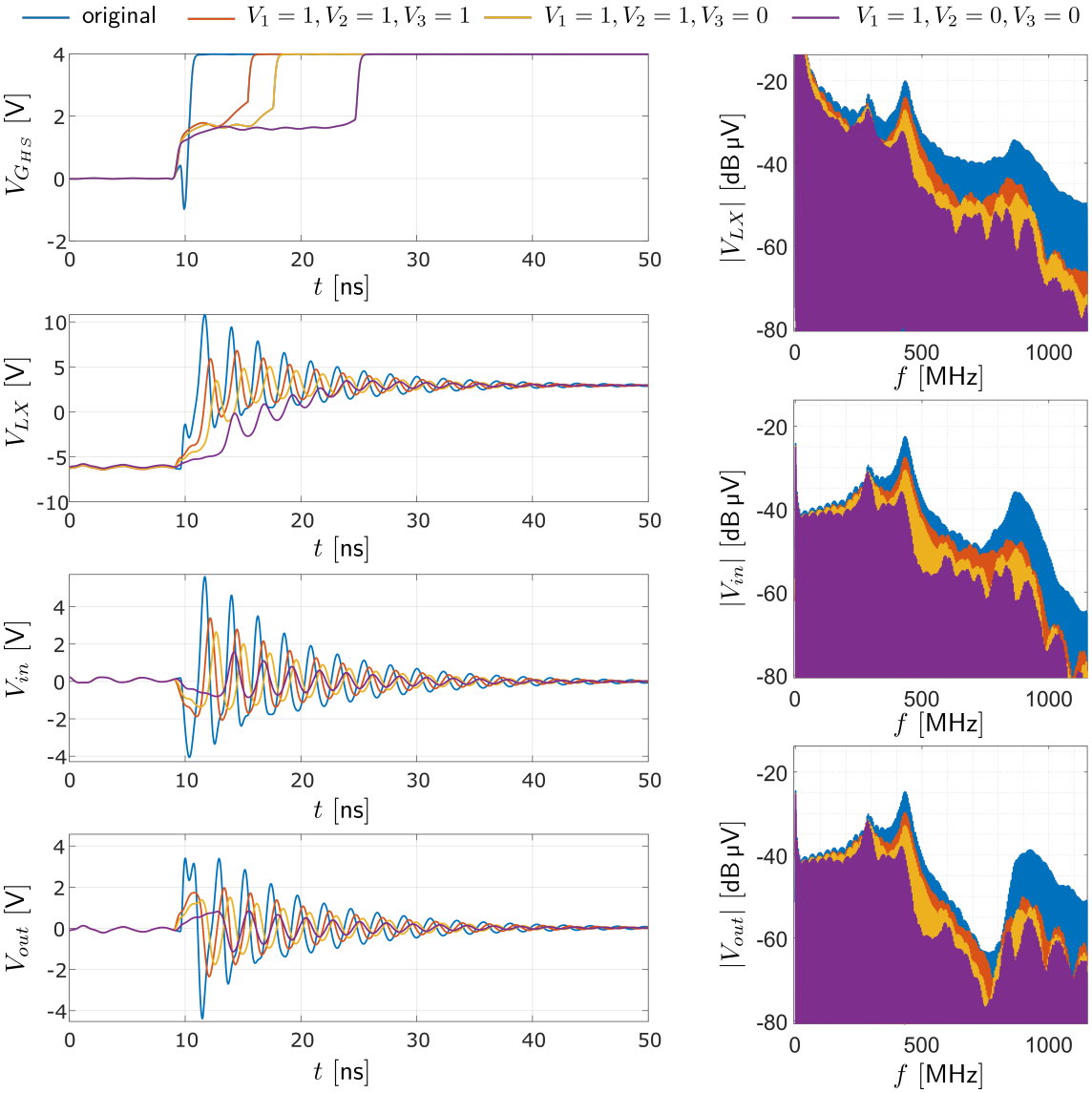


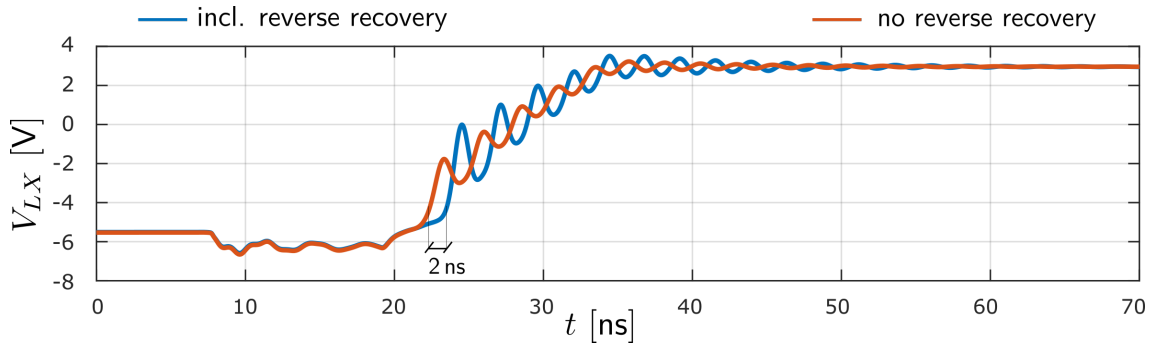
Figure 5.20: Simulation results of the ERC driver, using the converter model

The slew rate of the reduction also causes a reduction of efficiency. The slowest setting of the gate driver causes 1.3 % increase. The losses are investigated by the output- to input power ratio, only regarding the losses in the half bridge. The input power is derived by the drain current of the HS-switch and the input voltage. The output power is derived by the load current and the output voltage. This investigation only regards the losses in

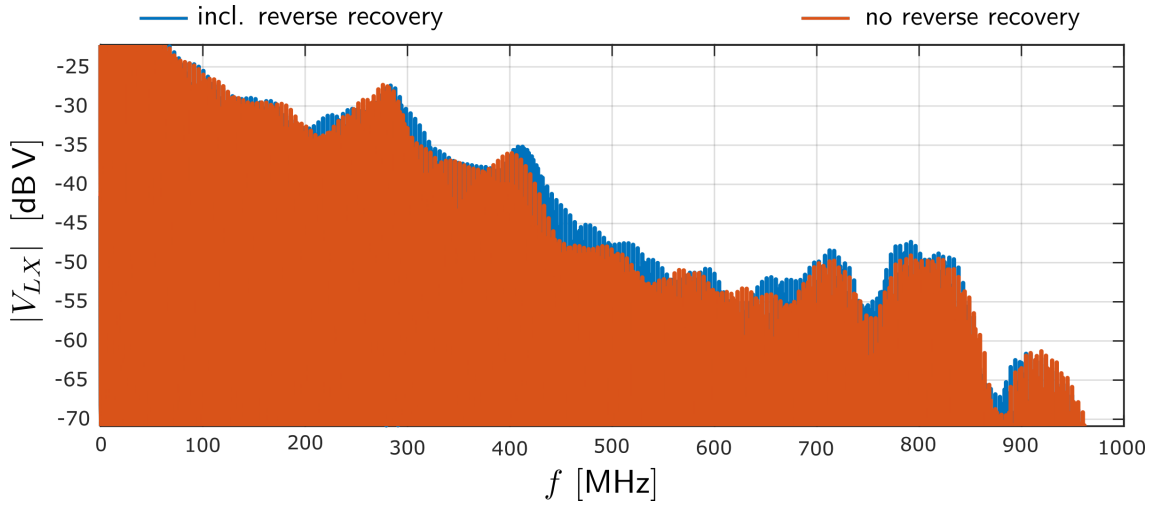
the half bridge. This method does not include the losses of the driver structure. Since the driver circuit is not optimized and using some ideal sources, an efficiency calculation including the driver losses is in this stage of the design process meaningless.

On the beginning of the turn-on transition, the signal on the phase node increases very slowly. The reverse recovery of the low side body diode increases the time with the flat slope. This is visible in fig. 5.21(a). This figure compares the signals on the phase node, simulated with and without the influence of reverse recovery. The simulation shows the slope with the smallest possible slew rate setting of the driver. It can be observed that the flat part of the slope at the beginning of the transition lasts 2 ns longer because of reverse recovery.

Also, the amplitude of the noise signal is slightly larger when reverse recovery is included. This is shown in fig. 5.21(b).



(a) Time domain signal



(b) Frequency domain signal

Figure 5.21: Influence of reverse recovery on the phase node signal

Due to the reverse recovery current, the voltage transition on the phase node starts later in time. This causes for a longer time a large voltage drop and a high current in the transistor. This causes more losses in the switch. Although the different blocks in

the driver are in power down mode, when they are not in use, the bias currents of the different blocks have also to be considered as losses. Since the designed driver is only a concept and not a design ready to tape out, The losses due to the supply and bias of the circuit are not investigated.

The losses in the half bridge, depending on the EMI-reduction are shown in. 5.22, with the EMI reduction in dB on the x-axis and the reduction of the output- to input power ratio on the y-axis. The losses are generated in the high side switch, due to the overlap of high drain current and high drain source voltage.

In comparison to the slew rate setting of the ADP5075, discussed in section 3.5.2, similar effects are observed. The ringing amplitude of the turn-on ringing is lowered significantly. The turn-off ringing amplitude is not much affected by the slower driving of the gate.

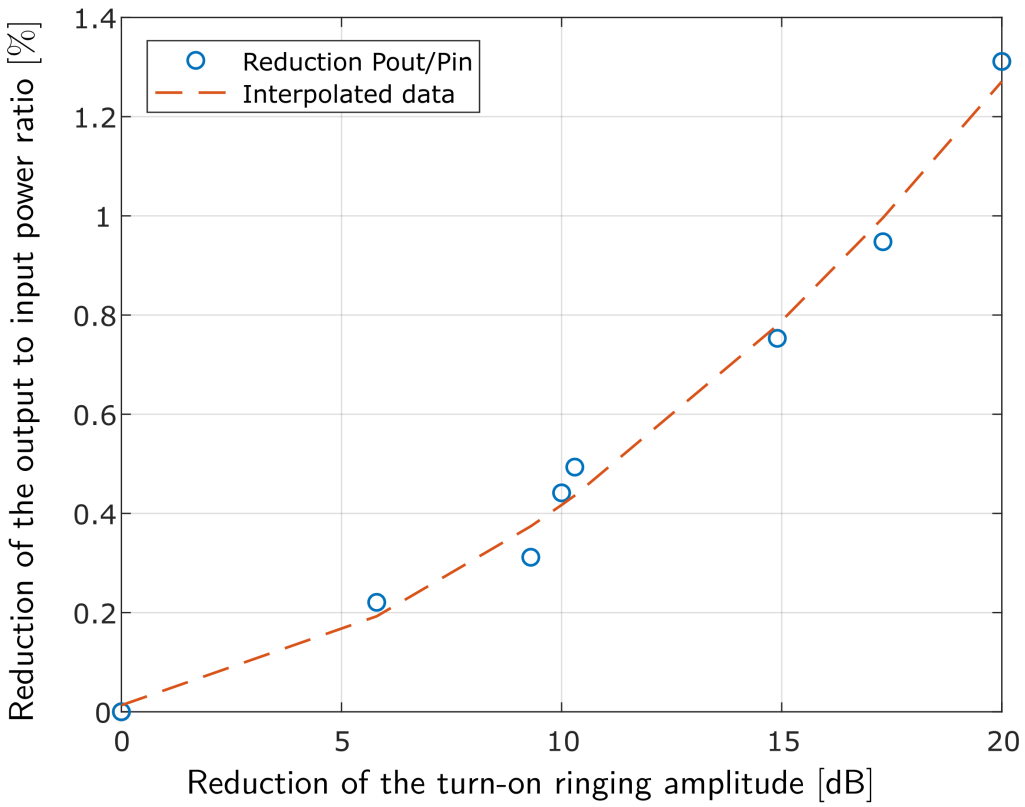


Figure 5.22: Switching losses dependent on the EMI reduction

5.6.5 Conclusion

The presented driver concept is able to get a significant reduction of EMI. The concept is fully integrable on-chip. A drawback is the higher losses due to the increasing switching losses and the supply and biasing of the additional needed blocks. But due to the programmability resulting slew rate, a trade-off between losses and EMI reduction can be set even after the production of the IC. This could be a big advantage when a system using such a converter does not meet the required EMI criteria. In such a case, the slew rate can be set to a lower level, and so less noise is produced. With a conventional driver circuit, this is not possible. In that case either additional filters have to be implemented on the PCB, or a new chip with better EMI performance has to be designed.

Chapter 6

Additional concepts to reduce the EMI of inverting buck/boost converter

Two additional concepts are tried to reduce the EMI of an inverting buck/boost converter:

- An additional capacitance across input to output C_{cross}
- A dynamic switched capacitance from the phase node to ground

Both of the concepts do not give the desired effect on the major noise frequencies. So the investigation was stopped after a few basic simulations. Nevertheless some interesting effects are observed.

6.1 Additional C_{cross} capacitor

An additional capacitor C_{cross} is added across in- and output to the circuit to decrease the current loop for the high-frequency currents. This capacitor should create a shortcut for the high-frequency noise. If C_{cross} is implemented on the IC, the high frequency current is not forced through the in and output capacitor. So the high-frequency currents remain inside the IC. The noise frequency is shifted to a much higher frequency, because the loop inductance is reduced to a minimum.

Fig. 6.2 shows the results of the simulation using different capacitance values for C_{cross}. It can be observed that even a 100 pF capacitor is not big enough to reduce the amplitude of the turn-on and turn-off ringing. Larger capacitor values would decrease the impedance for the high frequency signals and the shortcut path could be be more effective. The first harmonic of the turn-on ringing shows a reduction in amplitude. Further, a shift of the turn-on and turn-off frequencies to lower frequency values is observed. To implement such big capacitors on-chip is not economic. Therefore the

investigation was stopped on this point.

The performed simulations are not enough to judge the effectiveness of this method. Further investigations would be needed.

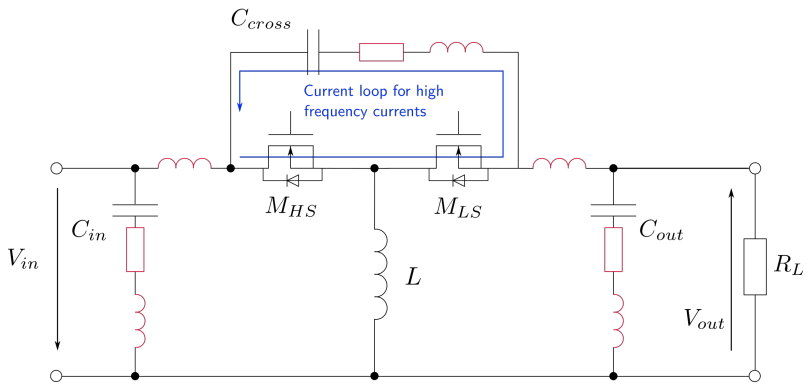


Figure 6.1: Schematic of the converter including cross capacitance C_{cross}

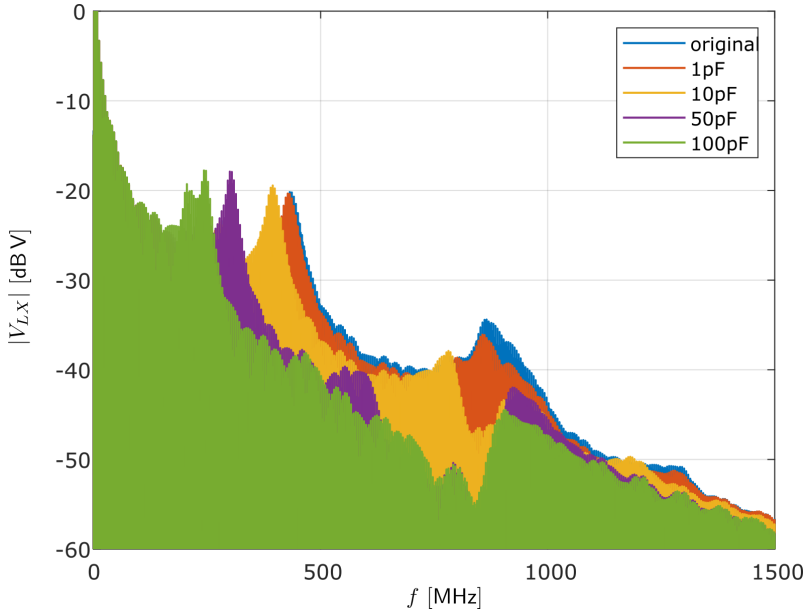


Figure 6.2: Simulation results, using different values of C_{cross}

6.2 Dynamic switched capacitance

An additional external capacitor C_{LX} is added across the phase node and ground. A switch allows to connect and disconnect the capacitor to the circuit. The principal idea is to switch the capacitor at the time on, when the resonance gets excited. The capacitance should disturb the build-up of the ringing.

The biggest problem with this the control of the switch. The controlling of the switch has to be extremely fast and accurate. The results of the simulation of this concept are

shown in fig. 6.4. The fast and precise switching is not achieved in this investigation. The switched capacitance was connected to the circuit for most of the transition time. The simulation results are somehow similar to a permanently connected capacitor in parallel to the inductor, but other interesting and in some cases maybe useful effects can be observed.

The additional capacitance somehow creates a shift in the frequency domain. This must be analyzed in more detail to prove its effectiveness. Actually if the switch was controlled intelligently, the capacitor could charge up in one cycle and discharge in another cycle so it can reuse the energy. It would be turned on and off not always at the same moment, but the turn on and turn off moment would depend on the voltage in the capacitor. But this concept needs more investigation. However, until now it is not clear if it would work.

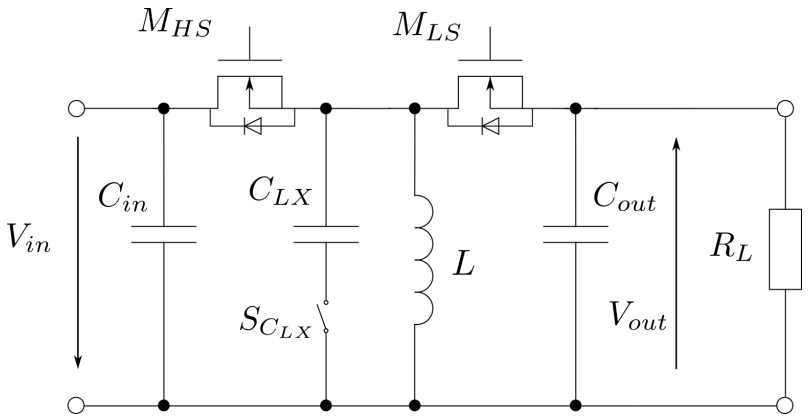


Figure 6.3: Schematic of the converter including the dynamic switched capacitance

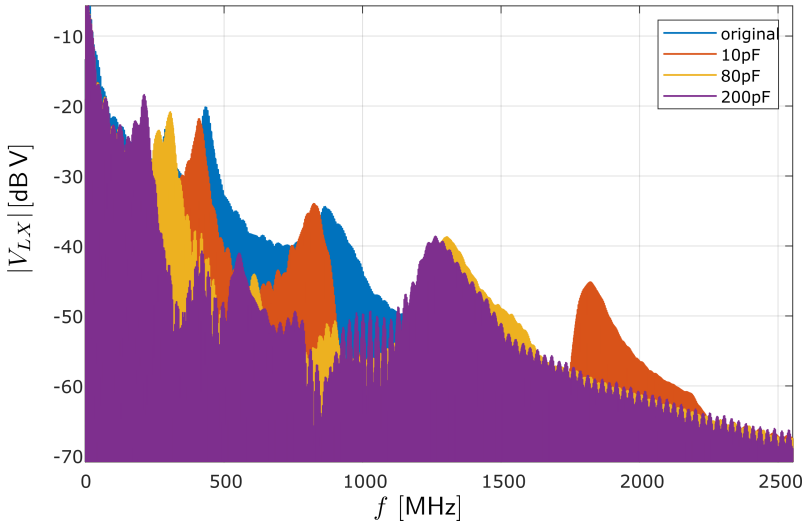


Figure 6.4: Simulation results of the switched capacitance approach

Chapter 7

Conclusion

Inverting buck/boost converters gain popularity for display applications in mobile devices. In order not to disturb the increasingly complex systems, the reduction of electromagnetic interference is indispensable. In addition to their numerous benefits, SMPS are also known to be a source of EMI. In the course of this thesis, an EMI analysis of an inverting buck/boost converter was carried out, and based on this, various circuit concepts for reducing EMI were developed. The EMI analysis shows that two resonances are excited, one during turn-on and one during turn-off. The resonances are mainly dependent on the parasitic elements in the circuit. During turn-on, the diode capacitance, or in the two switch topology, the transistor capacitance of the low side switch, and the loop inductance form the resonance. During turn-off, the loop inductance remains the same, and the critical capacitance is the capacitance of the high side switch. The general behavior has been verified by simulation of the two different typologies and by the design of a converter from discrete components. The gate driver and the gate capacitance linearity provide additional complexity.

Many approaches exist to reduce the EMI of such a converter structure. Mainly four different categories exist:

- Accepting the bad source, instead using filtering and shielding
- Changing the source, but no change of the MOSFET driving (Snubber, Ross)
- Controlling reverse recovery
- Change the source using different driver techniques (Reduce the di/dt and dv/dt by slower driving, variable frequency control)

Reducing the EMI by controlling the switching signal's slew rate is an approach, which can directly be implemented on-chip. The functionality of this method does not depend on external components. A significant reduction of the electrical noise during the turn-on and turn-off is achievable. The presented slew rate driver using constant gate currents can reduce the turn-on ringing by 8 dB. But simultaneously the efficiency decreases by

5 % due to the switching losses. An improved variant of the gate driver was developed by using a feedback system. This driver can reduce the turn-on ringing by up to 20 dB, but the output- to input power ratio decrease is still 1.3 % using the lowest slew rate setting.

The programmability of the slew rate is a useful feature for customers, which have trouble with the EMI-performance of their systems. This feature allows an EMI-reduction without any hardware changes.

To reduce the EMI, one should not only to be pick one method. A combination of different methods would be the best solution. For example in addition to the slew rate reduction, filters on the PCB and EMI optimized PCB layout would help to decrease the noise. Nevertheless it is always dependent on the requirements of the system and it is always a trade-off between functionality, efficiency, and cost.

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Appendix A

Spice Model

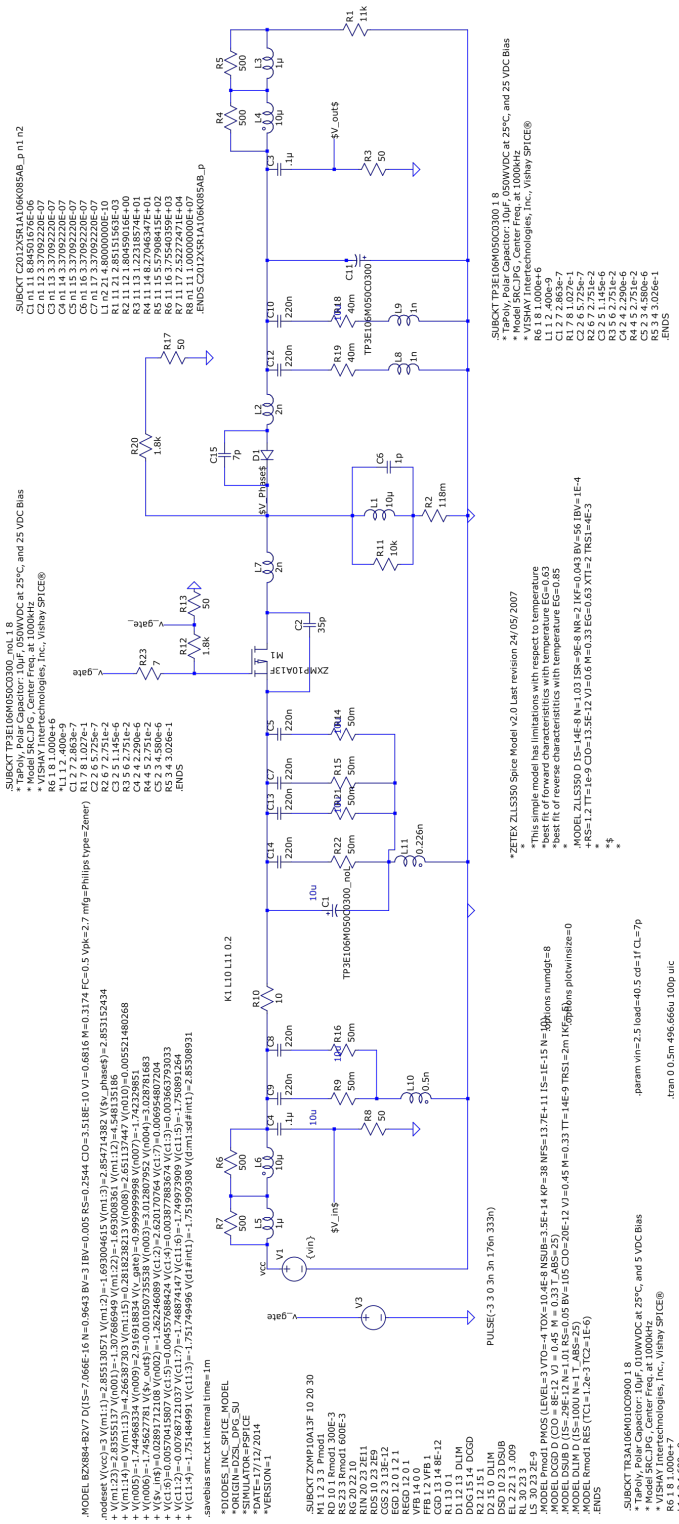

Figure A.1: This spice model was developed during the investigations of section 3.

Appendix B

Generating a spectrogram in Matlab

This matlab code allows to crate a spectrogram of a time signal.

```
function [S,F,T,P] = f_stfft(signal,fs)
ts=1/fs; %sampling info
%------STFFT-----------------------------
t_win=100e-5; %window size expressed in time (seconds)
%window=round(t_win/ts); %window size in number of samples
%window=blackman(t_win/ts);
% window=kaiser(t_win/ts,1);
% window=ractwin(t_win/ts);
% figure;
% plot(window)
% window=rectwin(t_win/ts);
% spectrogram(x,window,noverlap,F,fs);
[S,F,T,P]=spectrogram(signal,250,[],[],fs);


[T,F]=meshgrid(T,F);
end

[S,F,T,P] = f_stfft(data,10e9);
imagesc([min(T) max(T)]*1e6,[min(F) max(F)]/1e6,20*log10(abs
    (S)));
set(gca,'YDir','normal');
grid on;
colormap('jet')
```