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Input Impedance Measurements of HF RFID Transponder Chips

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Abstract

High Frequency (HF) Radio Frequency Identification (RFID) systems experience rising attention due to prospective use cases in the Internet of Things (IoT) as well as for wireless sensing. For well-working and standard-compliant transponder (tag) designs, it is necessary to characterize the nonlinear input impedance of chips. Conventional impedance measuring systems available on the market do not provide the required performance for characterizing chips over the desired voltage range. Several research groups developed measurement systems using Vector Network Analyzers (VNA) that exhibit good accuracy only for a certain range of impedance. In this thesis, a novel measurement system was developed, that is based on the Radio Frequency (RF) current-voltage (I-V) method of impedance measurements, which is capable of providing a high sensitivity over a wide range of chip impedance. A newly developed calibration method enables to calibrate the designed system using three well known calibration standards. Using another set of well known reference standards, it is possible to estimate the accuracy of the measurement system in an impedance range typical for HF RFID chips. With a relative measurement error smaller than 2 %, the developed system exhibits a higher accuracy compared with related measurement systems based on VNA measurements. The proposed measurement system provides a cost-effective, yet accurate method of measuring HF RFID chip impedances. A system analysis shows, how given parameters of a transponder coil can be used to compute if the coil will constitute an effective transponder design together with a characterized chip.

Kurzfassung

Hochfrequenz (HF) Radio Frequency Identification (RFID) Systeme gewinnen zunehmend an Bedeutung durch Einsatzmöglichkeiten im Internet of Things (IoT) oder in Wireless Sensing Anwendungen. Messungen der nichtlinearen Eingangsimpedanz der Transponder-Chips sind essentiell für ein erfolgreiches, standardkonformes Transponderdesign. Gewöhnliche, am Markt verfügbare Impedanzmesssysteme liefern nicht die benötigte Performance, um Chips über einen weiten Spannungsbereich zu charakterisieren. Eine Reihe an Forschungsgruppen haben eigene Messsysteme auf Basis von Vektor-Netzwerkanalysatoren (VNA) entwickelt, die nur in einem kleinen Impedanzbereich eine gute Messgenauigkeit aufweisen. Im Zuge der vorliegenden Arbeit wurde ein Messsystem entwickelt, basierend auf der Radio Frequency (RF) Strom-Spannungsmethode (I-V) von Impedanzmessungen, welches eine gute Genauigkeit über einen weiten Impedanzbereich bietet. Eine neu entwickelte Kalibrationsmethode ermöglicht es, das Messsystem mittels dreier gut bekannter Standards zu kalibrieren. Durch ein weiteres Set von Referenzstandards wird die Messgenauigkeit des Systems in einem Impedanzbereich abgeschätzt, der typisch ist für HF RFID Chips. Mit einem relativen Messfehler kleiner als 2 % weist das entwickelte Messsystem eine höhere Messgenauigkeit auf, als vergleichbare Arbeiten, die auf Messungen mit VNAs basieren. Dadurch ermöglicht das vorgestellte System kosteneffiziente und gleichsam genaue Impedanzmessungen von HF RFID Chips. Gegebene Parameter einer möglichen Transponderspule erlauben es zu berechnen, ob ein charakterisierter Chip in Kombination mit der betreffenden Spule ein valides Transponderdesign darstellt.

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CHAPTER 1

Introduction

Radio Frequency Identification (RFID) is a technology that has been developed for the purpose of wirelessly identifying objects [1]. High Frequency (HF) RFID is a variant of this technology that works through inductive coupling at a frequency of 13.56 MHz. An HF RFID system typically consists of a *reader* that aims to identify objects with a *transponder* (tag) attached. The transponder is in turn composed of a chip and a coil.

Early works that deal with the idea of RFID date back to the year 1948, but it took several decades for the technology to reach fruition [2]. In the 1980s, implementations of the technology started and in the 1990s, RFID exhibited wide scale deployments through road toll systems. Smart cards used for identification have been a particularly popular use case for HF RFID systems in the recent decades. The outbreak of SARS-CoV-2 and the subsequent global COVID-19 pandemic in 2020 raised awareness of the hygienic significance of contactless payments with supermarkets urging customers to use the technology, if possible. The number of devices incorporating smart card technology was estimated to range around ten billion in 2017 with a strong expected market growth in the future [3].

Today, after the vision of the Internet of Things (IoT) has been born, the prospects for the RFID market are even better: The number of IoT devices currently deployed is estimated to range in tens of billions with an exponential growth forecast [4], [5]. The IoT is predicted to be integrated into the environment that surrounds us, in order to connect things of our everyday life. Amongst other technologies, RFID systems are recognized to be one of "the atomic components that will link the real world with the digital world" [6]. Passive RFID tags are considered particularly important because they work battery-less and thus have a virtually unconstrained life span [7]. Deploying vast numbers of IoT devices in the environment also raises the issue of the eco-toxicity of batteries [8], which is overcome by using passive tags. A high production volume, highly integrated design and the low demand of components have made RFID systems a *low-cost*

technology enabling the IoT.
Recent research shows completely new directions for prospective use cases of RFID: HF RFID systems have already surpassed the primary purpose of communication for the sake of identification. Non-communication use cases like wireless sensor tags are explored [9], [10]. They can sense environmental conditions, like temperature [11] or humidity [12], in the vicinity of the tag.
The deployment of a vast number of RFID tags will raise the demand for equipment aiding the design and verification processes of HF RFID chips. These chips usually exhibit a strongly nonlinear input impedance. Knowledge of the chip impedances helps in the design of transponders and may eventually contribute to their successful deployment in widescale IoT scenarios. Furthermore, for the emerging use case of passive sensor tags, complete parametrical knowledge of the electrical transponder characteristic is crucial. Accurate impedance measurements will enable turning this vision into reality.

In this thesis, the available options for measuring the input impedance of HF RFID chips are investigated and a cost-effective, yet accurate implementation of a measurement system will be presented. A range of different DUTs (Device Under Test), i.e., chips, is characterized, where the measurement results are shown along with an exhaustive investigation of the measurement quality. Unlike most related works, this thesis presents an attempt to report measurement results together with an expected measurement uncertainty, which makes the reported results more complete. Knowledge about the measurement uncertainty will be particularly valuable, where small variations of parameters may be of concern. This is the case in the field of passive sensor tags, where small changes of a parameter are related to large changes of a sensing quantity of interest in the vicinity of the transponder. Rounding up the presentation of acquired measurement results, an analysis from a system perspective will provide insights about how the nonlinear chip impedance impacts the transponder behavior.

1.1 HF RFID Systems

In this thesis, two standards of HF RFID systems are considered: ISO/IEC[1] 14443 describes *proximity-coupling smart cards* working in an approximate range between 7 cm and 15 cm [1]. ISO/IEC 15693 describes *vicinity-coupling smart cards* working in a range up to 1 m. Both standards are based on inductive coupling at a carrier frequency of $f_c = 13.56\,\mathrm{MHz}$. HF RFID systems typically consist

[1] The International Organization for Standardization (ISO) and International Electrotechnical Commission (IEC) are international standards organizations.

of a reader and one or multiple transponders. Transponders can be batteryless devices that communicate with the reader wirelessly. Power is delivered from the reader to the transponder by inductive coupling. That is, an alternating magnetic field H is used to induce a voltage in the transponder coil. The load, i.e., the impedance, of the transponder has an impact on the reader due to the inductive coupling. By varying its load, the transponder can communicate with the reader. This is known as Load Modulation (LM). The alternating magnetic field generated by the reader oscillates at the carrier frequency f_c, while the LM is performed at subcarrier frequencies that are derived from f_c, which are typically 848 kHz, 424 kHz or 212 kHz [1]. The subcarrier frequency determines the data transmission speed of the system. The power that is available to the transponder through the alternating magnetic field is limited and decays with the distance to the reader. The distance where the transponder receives just enough energy to operate is termed *energy range* and the corresponding magnetic field *interrogation field strength* H_min [1]. In general, one goal of the design of HF RFID systems is to maximize the energy range.

The transponder is essentially composed of a coil and the chip. For maximizing the energy range of an HF RFID system, the power transfer to the chip has to be maximized. This can be achieved through *impedance matching* of the coil impedance to the chip. Impedance matching of two complex-valued impedances Z_a and Z_b is usually accomplished by choosing them to be complex conjugates of each other:

$$Z_\mathrm{a} \stackrel{!}{=} Z_\mathrm{b}^* \,,$$

where the $\{\cdot\}^*$ operator denotes complex conjugation. Conveniently, the impedance of the transponder coil has a low real part that is typically located in the range of several ohms, while the real part of the chip impedance exhibits much greater values[2]. Consequently, the power dissipated in the transponder coil is low. Impedance matching the chip to the transponder coil is done with respect to the imaginary parts:

$$\Im\{Z_\mathrm{coil}\} \stackrel{!}{=} -\Im\{Z_\mathrm{DUT}\} \,,$$

where Z_coil denotes the impedance of the transponder coil and Z_DUT the chip impedance. A circuit model of a transponder is shown in Figure 1.1, where parts of the frontend are depicted.

[2] This becomes evident from measurements conducted throughout this work (refer to section 4.3) and from measurements conducted in related literature (refer to section 1.3).

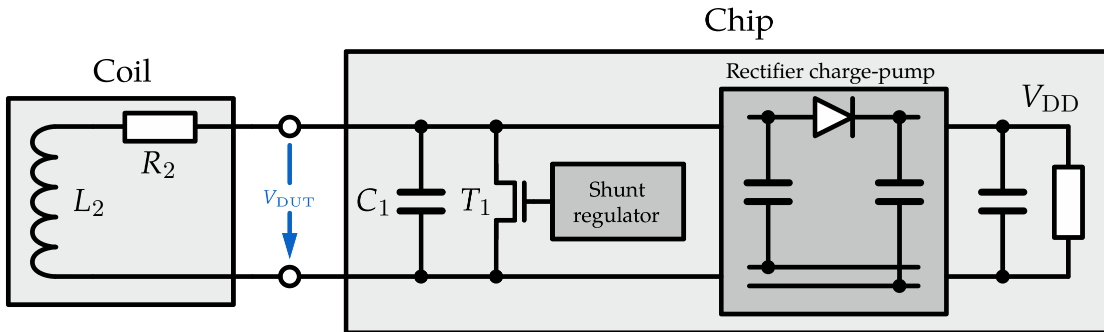

Figure 1.1: Architecture of the analog frontend taken from [13] with a transponder coil.

The chip houses an Integrated Circuit (IC) that usually has a strongly nonlinear impedance which depends on multiple parameters that are defined by the implementation of the shunt regulator and the behavior of the rectifier charge-pump. The shunt regulator is designed to regulate the voltage V_{DUT} supplied to the chip by decreasing its input impedance. The coil on the other hand is a linear component that can be designed to meet desired specifications using either analytical equations [14] or electromagnetic (EM) simulators [15] to estimate its parameters. It is modeled by a coil inductance L_2 and a coil resistance R_2. For system analyses, the chip impedance is generally modeled as a parallel circuit of a capacitance C_{p} and a resistance R_{p} as is depicted in Figure 1.2. Using this approximation allows to compute some important transponder parameters in a straightforward fashion, as will be shown below.

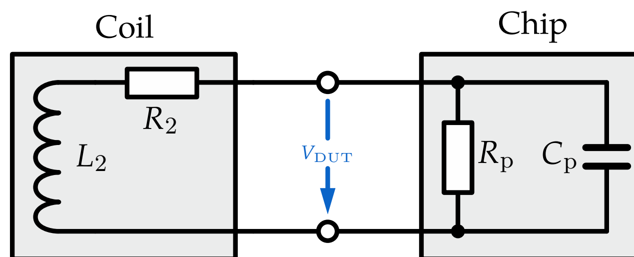

Figure 1.2: Simplified equivalent circuit model of a transponder used for system analyses [16].

Transponder Resonance Frequency:
The transponder resonance frequency f_{res} is determined by the inductance L_2 of the transponder coil and the capacitance C_2:

$$f_{\text{res}} = \frac{1}{2\pi}\sqrt{\frac{1 - C_2 R_2^2}{L_2 \cdot C_2}} \approx \frac{1}{2\pi\sqrt{L_2 \cdot C_2}} \tag{1.1}$$

The total transponder capacitance comprises the input capacitance of the chip C_{p} and a parasitic capacitance[3] C_{par} of the real circuit [1]: $C_2 = C_{\text{p}} + C_{\text{par}}$. For HF RFID chips, the input capacitance of the chip C_{p} usually incorporates a *tuning* capacitance to achieve resonance of the chip with a dedicated transponder coil. From a perspective of the induced voltage in the transponder coil, the simplified transponder equivalent circuit depicted in Figure 1.2 effectively constitutes a series resonant circuit[4]. Theoretically, when excited at its resonance frequency, a series resonant circuit exhibits a high voltage step-up [1], [17]. This helps to reach the minimum required chip voltage to power up the chip, termed $V_{\text{DUT,min}}$, at a minimum interrogation field strength H_{min} and thus increases the energy range. Practically, the transponder resonance frequency is chosen slightly higher than the carrier frequency of the reader. This choice is made for several technical reasons, e.g., to keep the interaction of nearby transponders low [1], and is indicated in various coil design guides [15], [18].

Magnetic Field:
Given the equivalent circuit model from Figure 1.2, the magnetic field H can be computed from the chip voltage V_{DUT} through [1]

$$H = V_{\text{DUT}} \frac{\sqrt{\left(\frac{\omega L_2}{R_{\text{p}}} + \omega R_2 C_2\right)^2 + \left(1 - \omega^2 L_2 C_2 + \frac{R_2}{R_{\text{p}}}\right)^2}}{\omega\, \mu_0\, A\, N_{\text{turns}}}\,, \tag{1.2}$$

where ω is the angular frequency, μ_0 the vacuum permeability, A the cross-section area of the coil and N_{turns} the number of turns in the coil. Equation 1.2 is often used to compute the interrogation field strength at the voltage, where

[3] Note that the parasitic capacitance of the transponder coil is neglected in Figures 1.1 and 1.2.

[4] The voltage induced in the transponder coil is typically modeled as a voltage source in series with the inductance L_2 and the resistance R_2. From the perspective of this voltage source and knowing that the parallel resistance R_{p} is generally large, the equivalent circuit model constitutes a series resonant circuit.

the chip starts operating

$$H_{\mathrm{min}} = H|_{V_{\mathrm{DUT,\,min}}} \,.$$

To operate the chip, a constant core voltage V_{DD} has to be generated from the voltage induced in the coil and it has to be protected from excessive voltages. The chip voltage V_{DUT} is regulated using a *shunt regulator*, which is indicated by the transistor T_1 in Figure 1.1. This voltage regulation greatly contributes to the nonlinear impedance characteristic of chips. At this point, it should be stressed that the nonlinearity is *intended* and serves to *protect* the chip and operate it at an optimum voltage. In this work, Equation 1.2 will be used to investigate the voltage regulation performance of three chips as a function of the magnetic field (compare Figure 4.21).

Transponder Quality Factor:
The transponder quality factor Q_{T} is a measure for the voltage step-up in the series resonant circuit of the transponder. It is computed using [1]

$$Q_{\mathrm{T}} = \frac{1}{R_2\sqrt{\frac{C_2}{L_2}} + \frac{1}{R_{\mathrm{p}}}\sqrt{\frac{L_2}{C_2}}} \,. \tag{1.3}$$

In theory, very high quality factors are desirable for great energy ranges. However, practical designs aim for a quality factor in the range of $Q_{\mathrm{T}} = 40$ [15], [19], [20].

Transponder Bandwidth:
The choice for a limited transponder quality factor is made due to its inverse proportionality to the bandwidth [1]

$$B = \frac{f_{\mathrm{res}}}{Q_{\mathrm{T}}} \,. \tag{1.4}$$

There is a tradeoff between the range of a system, proportional to Q_{T}, and the data transmission speed, proportional[5] to B. Designing for a larger bandwidth (i.e., a lower quality factor) also accounts for deviations of the transponder resonance frequency from 13.56 MHz.

[5] According to the Shannon-Hartley theorem, the channel capacity C_{ch} (given in bit s^{-1}) of an ideal, band-limited communication channel depends on the channel bandwidth and the signal-to-noise ratio $\frac{S}{N}$ according to $C_{\mathrm{ch}} = B\,\log_2\left(1+\frac{S}{N}\right)$ [21].

For the computation of the above mentioned parameters of an HF RFID transponder design, knowledge of the chip input impedance Z_{DUT} is neccessary. In the following, a method for characterizing chips will be introduced.

1.2 Chip Characterization

HF RFID transponder chips are semiconductor devices that fulfill several tasks like harvesting power from the magnetic field H, listening and responding to reader requests, or protecting the chip from excessive voltages. The circuits that the chips are composed of might be complex and differ between different models depending on the intended use. HF RFID chips usually exhibit a strongly nonlinear input impedance characteristic that is commonly modeled as a parallel circuit of a resistor R_{p} and capacitor C_{p}. The computation of R_{p} and C_{p} from an

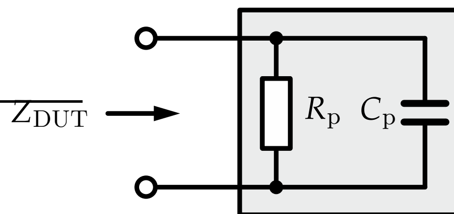

Figure 1.3: Equivalent circuit model of an HF RFID transponder chip.

impedance Z_{DUT} can be achieved easily via computing the admittance

$$Y_{\mathrm{DUT}} = \frac{1}{Z_{\mathrm{DUT}}} \quad \text{with} \quad R_{\mathrm{p}} = \frac{1}{\Re\{Y_{\mathrm{DUT}}\}} \quad \text{and} \quad C_{\mathrm{p}} = \frac{\Im\{Y_{\mathrm{DUT}}\}}{\omega}. \tag{1.5}$$

Completely characterizing chips over a wide range of chip voltage V_{DUT} or input power, respectively, can be a complex task. An impedance measurement system has been developed that works with the Radio Frequency (RF) current-voltage (I-V) method of impedance measurements. In this thesis, all measurements are conducted at the carrier frequency $f_{\mathrm{c}} = 13.56\,\mathrm{MHz}$.

Method of Measurement:
The objective of the method of measurement is the accurate determination of the impedance, i.e., the measurand[6], of a certain chip, i.e., the DUT. There are several methods of measurement that can be used for RF impedance measurements. In the RF I-V method of impedance measurement, signals are measured that are

6 The measurand is the quantity to be measured [22, definition D.1.].

proportional to the voltage V_{DUT} at the DUT and the current I_{DUT} flowing into the DUT [23]. Those signals are eventually related to the impedance of the DUT Z_{DUT}. Voltages are the desired measurable quantities. The voltage across the DUT can be measured directly, since the measured quantity[7] equals the measurand. The current flowing into the DUT can only be measured indirectly using a well-known shunt resistor[8]. The circuit of an RF I-V impedance measurement system is usually impedance matched to a characteristic impedance of $Z_{\mathrm{W}} = 50\,\Omega$ to enable accurate measurements at high frequencies. The impedance matching of the circuit can be achieved by using transformers, for instance.

Calibration:
In practice, when measuring the impedance of a certain DUT, it might be impossible to acquire the measurand directly at the location of the DUT, i.e., the measurement reference plane. The data acquisition plane of the measurement devices, i.e., the plane where the measured quantity is acquired, is usually located at the ports of the respective measurement instrument. Possible cables, connectors and fixtures used for interconnecting the individual devices with the DUT cause a deviation between the measurement reference plane and the data acquisition plane. The process of determining the discrepancy, i.e., the error, between the measurand and the measured quantity is termed *calibration*. It serves to determine how the measurand located at the measurement reference plane is related to the measurement at the data acquisition plane [45]. In order to determine the generally unknown error, a set of well-known *calibration standards* is used.

Measurement Sensitivity:
When talking about measurement instrument specifications, the term measurement *sensitivity* might be used in a broader sense. This thesis will adhere to the definition from the Deutsches Institut für Normung (DIN). According to the DIN standard 1319 [24], the sensitivity of a measurement system is defined as the change of the output quantity, i.e., the measured quantity, related to the change of the input quantity, i.e., the measurand.

Measurement Accuracy:
Determining the measurement *accuracy* helps to evaluate the quality of acquired measurement results. In this thesis, the relative error

$$\delta_Z = \left| \frac{Z_{\mathrm{meas}} - Z_{\mathrm{ref}}}{Z_{\mathrm{ref}}} \right| 100\% \tag{1.6}$$

[7] The measured quantity is also termed the realized quantity [22, definition D.2].
[8] In practice, a low-loss transformer is used in place of this resistor [23].

will be used to evaluate the measurement accuracy, where Z_{meas} is a measured impedance and Z_{ref} is the characterized, assumed "true", reference impedance. Utilizing the relative error δ_Z as a quality indicator for measurements, a performance comparison can be made between different impedance measurement systems.

Measurement Repeatability:
Measurement *repeatability* is a term used to describe the closeness of agreement between the results of several measurements of the same DUT carried out under the same conditions [22]. In this thesis, the measurement repeatability is verified by comparing the measurement results of several series of measurements with each other. The corresponding evaluation is discussed in section 4.2.2 and results are depicted in Appendix B.

Measurement Uncertainty[9]:
When reporting measurement results, it is important to keep the following facts in mind [25]:
A measurand is by nature indeterminate. A measurement result is the best estimate of a measurand. It is is reported completely by a value attributed to the measurand along with information about the *uncertainty* of the measurement [22]. The measurement uncertainty is a statement of the lack of exact knowledge of the measurand [22]. Even after the correction of all errors, the measurement result is still just an estimate of the measurand due to a possible incomplete correction as well as remaining random effects.

1.3 Outline and Related Work

This work is divided into three main chapters: In chapter 2, the measurement system is introduced as a theoretical concept along with the practical implementation. The measurement equipment as well as the realized hardware are presented and discussed in detail.
Chapter 3 is devoted to the calibration of the measurement system, since this is an integral part of accurate RF measurements. A calibration concept had to be developed throughout a separate project[10] for systems that work with the RF I-V method of impedance measurements. The full deviation is based on

[9] Refer to [22, section 2.2.] for a comprehensive definition of the uncertainty of measurement.
[10] The work carrying the title *Calibration Strategy for an RF I-V Impedance Measurement System* can be found in Appendix A and has been submitted as a *Master-Project* to Graz University of Technology on 01.09.2020.

the representation of the linear electrical network as an interconnection of two-ports and can be found in Appendix A. In chapter 3, the derived calibration is analyzed mathematically. The chapter demonstrates, how a calibration can be computed using a set of N known calibration standards and how its accuracy can be evaluated with an additional set of known reference standards.
The actual measurement results and a subsequent analysis from a system perspective complete this work. The achieved measurement accuracy, repeatability and uncertainty are evaluated and the characterized impedance curves of several chips are presented in chapter 4.
The individual chapters are generally structured in three sections: the *concept* section introduces the general idea and provides the theoretical basis of each chapter. The *implementation* section describes, how the presented ideas have been realized practically. The *verification* section evaluates, how well the implementation matches with the concept.

Several methods of measurement can be employed for impedance measurements. Looking at what is available on the industrial market is a good starting point for investigating and comparing those methods with each other. The US based company Keysight Technologies, for instance, offers a wide range of RF measurement devices along with selection guides and handbooks. In their *Selection Guide* [26] for LCR meters, impedance analyzers and test fixtures, they compare the three instruments listed in Table 1.1 for their suitability for impedance measurements.

Instrument	LCR Meter	Impedance Analyzer	VNA
Frequency sweep capability	point / list	continuous (start/stop, center/span)	continuous (start/stop, center/span)
Display	numeric	graphics	graphics
Advantages	low-cost, ease of use	widest meas. range, circuit modeling	versatile, cost-effective

Table 1.1: Instruments for impedance measurement taken from the selection guide [26].

Furthermore, in their *Impedance Measurement Handbook* [23], they compare the common methods available for impedance measurement (see Table 1.2).

Method	Advantages	Disadvantages	f range
Bridge method	high accuracy, low cost	manually balanced, narrow f range	DC to 300 MHz
Resonant method	good Q accuracy	resonant tuning necessary	10 kHz to 70 MHz
I-V method	grounded device measurement	f range limited by probe transformer	10 kHz to 100 MHz
RF I-V method	high accuracy, wide impedance range	f range limited by probe transformer	1 MHz to 3 GHz
Network analysis method	wide f range	narrow impedance measurement range	5 Hz and above
Auto-balancing bridge method	high accuracy, wide impedance range	narrow f range	20 Hz to 120 MHz

Table 1.2: Common methods for impedance measurement taken from the impedance measurement handbook [23].

From the above information given by a company that offers equipment for both industry and research, we can see that using an LCR meter for measuring the impedance of an HF RFID chip would be a good entry point due to its low cost and ease of use. Gebhart et al. [27] investigated whether it was possible to conduct the desired measurements with LCR meters available at the time of their research (their work [27] was published in 2010). They identified the necessity of using a custom measurement system based on the fact that none of the available devices was capable of outputting a voltage higher than $2\,V_{RMS}$. This was the starting point for the research of input impedance measurements for HF RFID transponder chips.
In the following years, several other research groups have come up with subsequent works and their own measurement systems. Table 1.3 lists those works according to the years when they were first published and compares the most distinctive features of their measurement systems: The devices are listed along with the measured quantities. All related works use measurement systems based on the network analysis method of impedance measurement. In most works, *contact based* impedance measurements were implemented, where the IC was embedded in a common package. Other works employed *contactless* measurements where the chip was embedded in a Coil on Module (CoM) [28] device. Some authors made an effort to evaluate the measurement accuracy of

their measurement system by measuring well known reference standards. In Table 1.3, the relative error δ_Z as given in Equation 1.6 has been used to quantify the measurement accuracy and compare related work. Further distinctive features are the abilities to measure the voltage V_{DUT} or the impedance of the DUT during LM. Finally, the works are distinguished based on their supply signalling.
Gebhart et al. [27] presented a measurement system based on a VNA where the output signal is amplified to achieve the desired power at the DUT. They measure the scattering parameter S_{11}, equivalent to the reflection coefficient Γ [29], by separating incident and reflected waves using an external directional coupler next to the DUT.
In their impedance measurement handbook, Keysight Technologies state that the *network analysis method* used in VNAs is generally only suitable for a *narrow* impedance measurement range in the vicinity of the characteristic impedance ($Z_{\mathrm{W}} = 50\,\Omega$). Contrary to that, in another application note [30], they mention two methods to measure impedance over a wider range using a two-port measurement:

- Measurement of S_{21} in the *series connection* for $Z_{\mathrm{DUT}} \geq 50\,\Omega$
- Measurement of S_{21} in the *shunt connection* for $Z_{\mathrm{DUT}} \leq 50\,\Omega$

Gvozdenovic et al. [31], [32] used this approach with the intention of reaching a high measurement accuracy also for impedances $Z_{\mathrm{DUT}} \gg 50\,\Omega$. They conducted a two-port measurement using a VNA, an amplifier, a lowpass filter, and a custom fixture.
Not long after their achievements, Couraud et al. [33] presented their solution for a *low cost* impedance measurement system. Their work is special in a way that it replaces the use of a VNA by a signal generator and a two-channel sampler or oscilloscope. Similar to the work presented by Gebhart et al. [27], an amplifier is used to supply the desired power levels to the DUT and a directional coupler separates signals of incoming and reflected waves from the DUT. They used a remotely controlled oscilloscope as *coherent* receiver that is able to determine the reflection coefficient Γ in magnitude and phase, which is then related to the impedance of the DUT. They also presented an algorithm for the computation of amplitude and phase from the signals that were sampled in the time domain. Some years later, they published another work [34] where they decided to use a *Goertzel algorithm* that allows the computation of individual terms of the Fast Fourier Transform (FFT) using very few samples [35]. They were able to compute one sample of the chip impedance every quarter wavelength of the $13.56\,\mathrm{MHz}$ carrier. Those time domain measurements eventually enabled them

to measure the chip impedance during LM. To verify their measurement accuracy, they compared the results of their low cost measurement system to the results measured with a VNA system as proposed by Gebhart et al.
Couraud et al. were close to be the first researchers to present chip impedance measurements acquired during LM, but in the year before their publication, Rizkalla et al. [36] published a paper where they acquired the parallel resistance R_p of the chip as a function of the RMS voltage V_DUT supplied to the chip in both the *loaded* and *unloaded* state. Initially, they used a measurement approach as proposed by Gebhart et al. for measuring the impedance of a chip using a CoM [37]. For that purpose, they designed a fixture with a coil that is strongly coupled to the CoM. They designed the coils such that they are resonant around the carrier frequency of $13.56\,\mathrm{MHz}$. This increases their measurement *sensitivity*, since a small change of the *measurand* Z_DUT results in a large change of the *measured quantity* Z_{11} acquired by the VNA. Furthermore, they use the strongly coupled coils as a matching network to match the system to the $50\,\Omega$ input impedance of the VNA. In their subsequent work [36], where they measured the impedance of the chip during load modulation, they had to modify their measurement system. They faced the problem that the bandwidth of the modulated signal was too high to measure with the VNA alone, so they separated the VNA from the supply path and used a vector signal generator for the power supply of the DUT and sending a wake-up sequence. The VNA was only used to measure incident and reflected wave signals coming from the directional coupler. Their measurements can also be considered complete in a sense that they have also measured the voltage V_DUT at the DUT using a *differential voltage probe*.

In contrast to related works, in this thesis, the the RF I-V method of impedance measurements is employed to achieve more accurate measurement results. The designed measurement system allows to differentially supply chips over a wide range of input voltage and the voltage V_DUT can be measured. The system concept and hardware allow to conduct LM measurements, but they are not implemented in software yet.

Year	Ref.	Measurement device, measured quantity	Package	Accuracy (rel. error)	V_{DUT} meas.	LM meas.	Supply signal
2010	[27]	LCR meter VNA, S_{11}	chip	not specified	yes	no	single-ended
2014	[31]	VNA, S_{21}	chip	not specified	no	no	differential
2014	[32]	VNA, S_{21}	chip	not specified	no	no	differential
2015	[33]	oscilloscope, Γ	chip	<4%	no	no	single-ended
2017	[37]	VNA, $Z_{11} = f(S_{11})$	CoM	<5%	yes	no	differential
2017	[36]	VNA, $Z_{11} = f(S_{11})$	CoM	<5%	yes	yes	differential
2018	[34]	oscilloscope, Γ	chip	<3.2%	no	yes	single-ended
2021	this work	sampler, $\frac{V_{\mathrm{DUT}}}{I_{\mathrm{DUT}}}$	chip	<2%	yes	no	differential

Table 1.3: A summary of measurement systems used in research to measure HF RFID chip impedances (listed according to the years when they were first published).

CHAPTER 2

Measurement System

This chapter introduces the system designed for measuring chip input impedances. First, the system is presented as a theoretical concept. The measurement principle and general design considerations are outlined in this part. The concept section is followed by the implementation section which focusses on hardware. This includes an overview of the used measurement equipment, the designed Printed Circuit Boards (PCB) and used components.

2.1 Concept

As already mentioned in section 1.2, the measurement system presented in this thesis is based on the RF I-V method of impedance measurement. Signals proportional to the voltage at the DUT and the current flowing into the DUT are used to compute the impedance Z_{DUT}. The network analysis method of impedance measurements has its highest sensitivity when the measurand Z_{DUT} is close to the characteristic impedance Z_{W}. In contrast, the RF I-V method of impedance measurement has a theoretically constant sensitivity regardless of the measurand [23]. However, because of imperfect error correction and non-ideal behavior of the voltage and current meters, the sensitivity varies as a function of the measurand. Therefore, special care has to be taken with respect to the arrangement of the voltage and current meters: For the *low-impedance* arrangement, the voltage meter is placed close to the DUT, while, for the *high-impedance* arrangement, the current meter is placed close to the DUT [23]. The terms *low-impedance* and *high-impedance* are related to the characteristic impedance Z_{W} of the circuit. At the operation frequency of 13.56 MHz, the measurement system can be considered

electrically short[1]. From a perspective of the DUT, the impedance Z_{W} is therefore dominated by the impedance of the rest of the circuit which encompasses the input impedances of the measurement and supply devices. One of the design goals of the presented concept is to be able to supply high powers to the DUT in order to fully characterize it. For a maximum power transfer, an impedance matching to a minimum expected DUT impedance of $Z_{\mathrm{DUT,\,min}} = 50\,\Omega$ is desired which usually occurs at high supply powers. As will be shown in chapter 4, several impedance measurements show that this is a reasonable choice. The impedance is chosen to be $Z_{\mathrm{W}} = Z_{\mathrm{DUT,\,min}} = 50\,\Omega$ because of the design choices made for impedance matching. For lower supply powers, the impedance of the DUT is higher than $Z_{\mathrm{DUT,\,min}}$. The high-impedance arrangement of the RF I-V method of impedance measurement is therefore chosen in this work.

The block diagram in Figure 2.1 shows the high-impedance arrangement of the system concept of this thesis: the current measurement, indicated by the Current Path, is placed close to the DUT. The voltage measurement is implemented in the Voltage Path, which is located farther away from the DUT. Both measurements are taken by a two-channel sampler, which is capable of acquiring both the voltage signal in the voltage path V_{V} and the voltage signal in the current path V_{I} *coherently*. This is crucial for computing the impedance Z_{DUT} in both magnitude and phase, which is in turn used to relate the impedance to the parallel resistance R_{p} and capacitance C_{p}. Clearly, the ratio $\frac{V_{\mathrm{V}}}{V_{\mathrm{I}}}$ is related to the impedance Z_{DUT}, but the actual relation is rather complex to derive analytically if various parasitics and non-idealities shall be accounted for. *Calibrating* the measurement circuit and *de-embedding* it from linear systematic errors is a more practical approach to find this relation. Details on this procedure can be found in chapter 3 and in Appendix A and will not be discussed here. For the sake of completeness, it is desired to determine the input impedance of HF RFID chips as a function of the chip voltage V_{DUT}. Determining Z_{DUT} can be done with the sampler alone, but the voltage V_{DUT} cannot be determined this way, unless its relation to the voltage V_{V} in the voltage path is determined. It is possible to find this relation through a calibration as well, but the calibration process demands at least some linearly independent measurements of the voltage V_{DUT} that are

[1] The free-space propagation wavelength at a frequency of 13.56 MHz is $\lambda \approx 22.1\,\mathrm{m}$. In media, the waves propagate at a wavelength reduced by a factor $\frac{1}{\sqrt{\varepsilon_r}}$. Considering a typical material for PCBs like FR4 with a relative permittivity of $\varepsilon_r \approx 4.4$ (for simplicity considered as effective relative permittivity) would result in a wavelength of $\lambda_{\mathrm{FR4}} \approx 10.5\,\mathrm{m}$. The wavelength exceeds all dimensions of the measurement system by far, thus it can be considered electrically short.

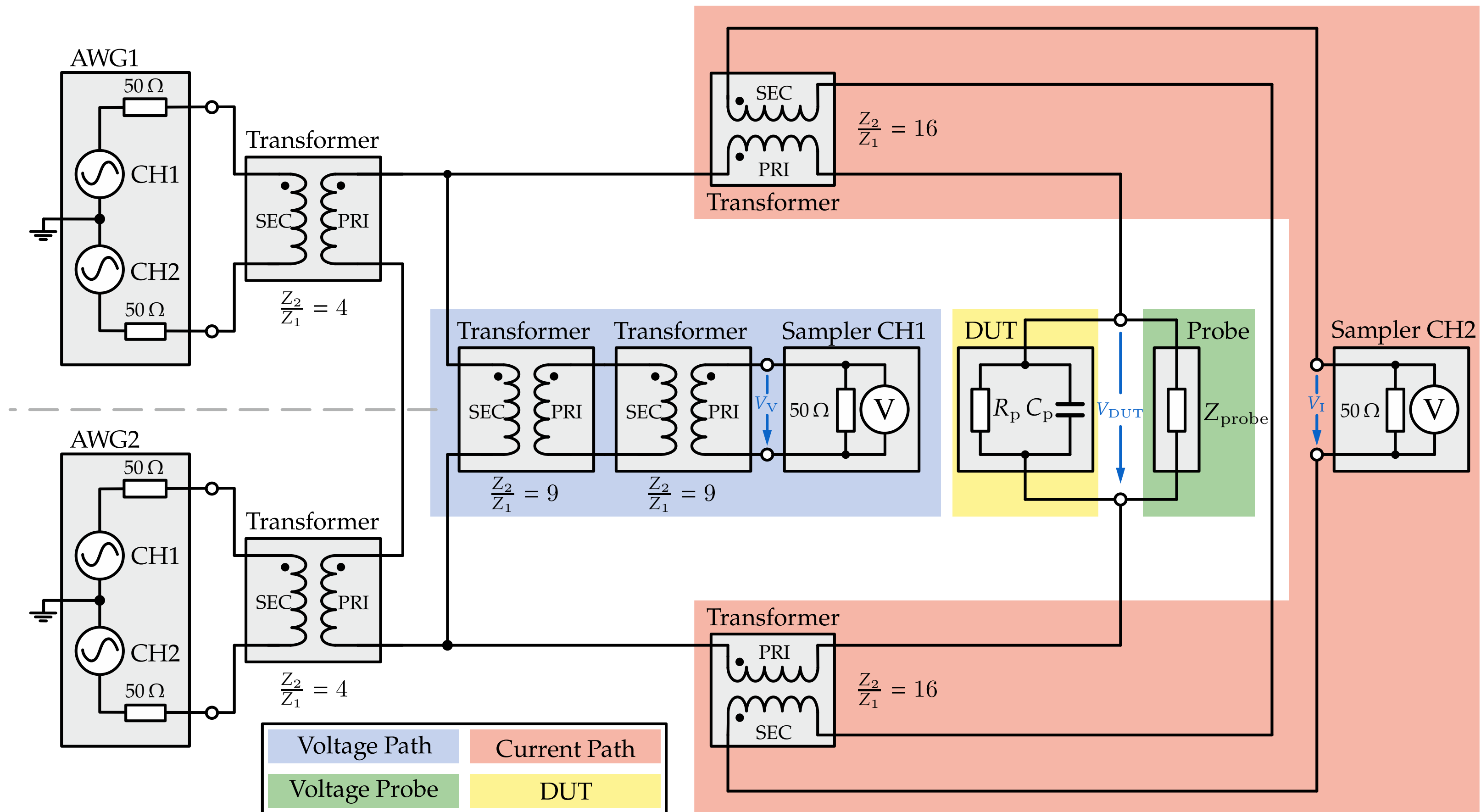

Figure 2.1: Block diagram of the measurement system.

coherent with the voltage V_V. Given the measurement equipment available, it is more practical to measure V_DUT using a Voltage Probe. In this work, an active voltage probe[2] is used that can acquire the voltage V_DUT directly and provides a high input impedance Z_probe. The probe is connected to an oscilloscope that processes the measurement data. A symmetrical, differential system design is chosen as depicted in Figure 2.1. This choice makes it possible to differentially supply the chip as it would be the case within a real chip card. Furthermore, this reduces any unwanted coupling with ground that might occur in single-ended designs.

One notable design choice in the presented concept is the use of two Arbitrary Waveform Generators (AWGs) to supply the chip. The two devices are used in a series connection to increase the available power range, as is evident from the block diagram of Figure 2.1. An AWG is capable of generating any arbitrary signal at its ports and can thus be used to communicate with the chip. This capability makes it possible to send a *wake-up* signal to the chip and acquire the chip response while it performs LM. The measurement of the chip impedance during LM is another desirable feature available in the most recent chip impedance measurement systems (see Table 1.3). One issue that arises from using two separate AWGs for the supply is the synchronization of both devices. While most RF measurement equipment typically offers a Synchronization (Sync) port for synchronizing the devices in frequency, the synchronization in phase has to be done manually. Conveniently, having a sampler that monitors the voltage in the voltage path, this process can be automated if the measurement equipment is remote-controlled via a host Personal Computer (PC): The phase of AWG2 is adapted using a *binary search* algorithm [38]. It aims to maximize the voltage V_V and thereby aligns AWG1 and AWG2 in phase.

In the network interconnecting the individual devices with the DUT, several transformers have been used. Depending on their location, they serve different purposes:
The transformers next to the AWGs are used to match the impedance of the DUT Z_DUT to the output impedance of the channels CH1 and CH2 from the individual AWGs in the point of maximum power transfer. This corresponds to the point where the impedance of the DUT approaches its minimum $Z_\mathrm{DUT,\,min}$ which is assumed to be $50\,\Omega$. The transformers in the voltage path serve the purpose of transforming down the voltage at their input to levels within the input voltage range of the sampler. At the same time, they transform the sampler input

[2] Although the system concept was designed symmetrically, a single-ended voltage probe has been used. Drawbacks arising from this choice will be discussed in section 2.2.

impedance up to a high parallel impedance between the supply lines of the DUT. The transformers in the current path effectively constitute low shunt impedances due to the impedance down-conversion of the sampler input impedance. Simultaneously, they transform the low voltage drop at their Primary Coil (PRI) to higher levels at their Secondary Coil (SEC) that match the input voltage range of the sampler. Using transformers proves beneficial in several ways. *Linearity* is a property of the transformers that becomes particularly advantageous in the calibration concept that aims to correct linear systematic errors. The PRI and SEC of transformers are *galvanically decoupled*. This property is essential for the series connection of the AWGs as well as for performing two-channel measurements with the sampler at reference potentials other than ground, because the sampler channels are single-ended.

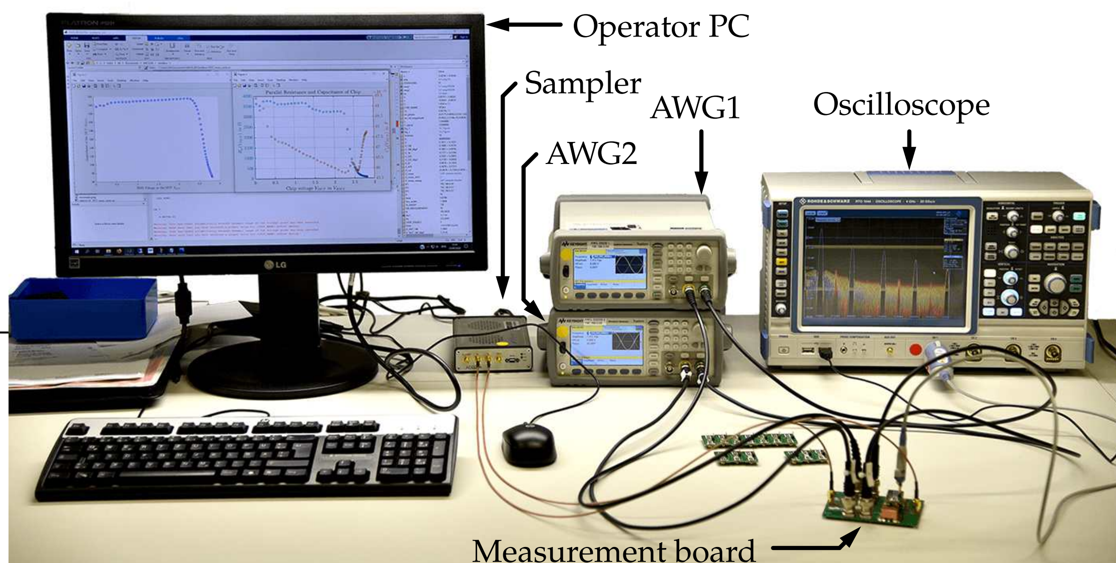

Figure 2.2: Photograph of the complete measurement system in the laboratory.

2.2 Implementation

The theoretical concept of the measurement system is set up in the laboratory where interconnections are made as depicted in Figure 2.1. All devices are capable of being controlled by a PC if respective connections are made. Figure 2.2 shows a photograph of the setup in the laboratory. The operator PC is connected to the AWGs and the oscilloscope via Ethernet, while its connection with the sampler is made via USB (Universal Serial Bus). The initialization, calibration and measurement control of all devices is done in an automated

Device	Model	Manufacturer
AWG1	33522B [39]	Keysight Technologies
AWG2	33522B [39]	Keysight Technologies
sampler	ADQ214 [40]	Teledyne SP Devices
oscilloscope	RTO 1044 [41]	Rohde & Schwarz
active voltage probe	RT-ZS10 [42]	Rohde & Schwarz

Table 2.1: Used measurement devices.

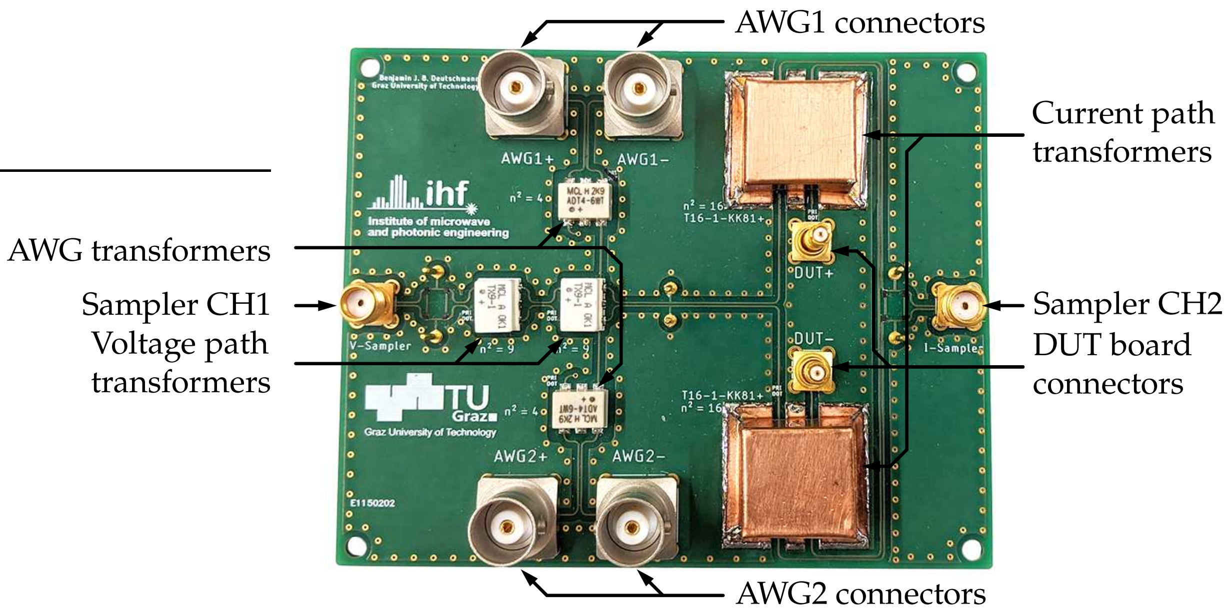

Figure 2.3: Photograph of the manufactured measurement board.

manner via MATLAB. The devices used in the measurement system are listed in Table 2.1 along with their manufacturer and model names.

The rest of the circuit as introduced in the concept is implemented using PCBs. There are two types of PCBs that have been designed for this measurement system: a *measurement board* and several *DUT boards*.
A photograph of the manufactured measurement board is depicted in Figure 2.3. It serves to interconnect the different measurement devices with each other which have different connector types and it has connectors for the specific DUT boards. All transformers are soldered onto the measurement board. The transformers from the current path are covered by boxes made from copper. These custom-designed boxes act as a *magnetic shield* and shall reduce any magnetic interference between the voltage path and the current path. The layout of the

measurement board has been designed symmetrically with differential signal lines routed closely together. Although most of the used components are suitable for Surface-Mount Technology (SMT), a two-layer PCB has been designed to allow a mechanically stable mount of all coaxial connectors. Large top-layer and bottom-layer ground planes are leveraged to reduce inductive coupling of any parasitic loops of the signal traces. Unfortunately, this design choice comes at the price of a higher parasitic capacitive coupling with ground. The inputs of the sampler are protected by an antiparallel connection of two Positive Intrinsic Negative (PIN) diodes[3] in series against excessive voltages. In the intended operating range of input voltages, those diodes are in a non-conductive state and their impact on the circuit can be neglected. For a quick interchange of DUTs and calibration standards, Sub-Miniature Push-on (SMP) connectors are used to connect to DUT boards.
A photograph of a manufactured DUT board is depicted in Figure 2.4. It shows

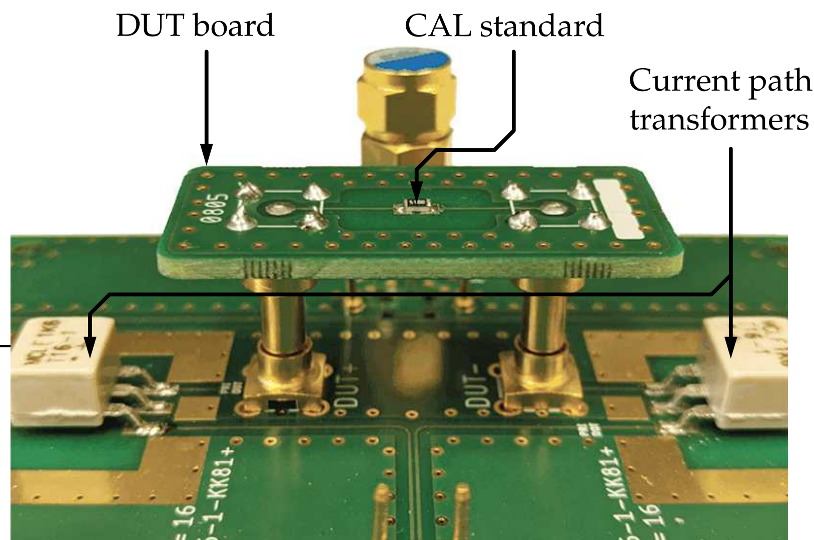

Figure 2.4: Photograph of a manufactured DUT board of an early design stage. In this picture, the current path transformers are not covered by the copper shield.

the DUT board connected to the measurement board via SMP connectors. This particular board has a calibration (CAL) standard soldered onto it. In this work, Surface-Mount Device (SMD) resistors are used as CAL standards. Their characterization will be discussed in section3.2. In the early design stage when the photograph of Figure 2.4 was taken, no pin heads for a connection to the volt-

[3] The diodes BAR90-02EL [43] have been chosen because their forward voltage $V_F \approx 0.9\,\mathrm{V}$ is smaller than half of the maximum rated input voltage of the sampler of $2.2\,\mathrm{V_p}$.

age probe were included in the design (compare Figure 2.5. In the final design (see Figure 2.5), the probe pin heads are soldered onto any DUT board and one general layout is used that incorporates both the footprint of the actual DUTs, i.e., chips, as well as the footprint of CAL standards, i.e., SMD components with a 0603 package size. This allows to solder either a DUT or a CAL standard onto each board and ensures that the electrical characteristics of all boards are equal, which is a crucial requirement of the calibration process.

Figure 2.5 shows a photograph of several DUTs that have been soldered onto DUT boards. Many of the characterized DUTs share the same or similar packages. This is advantageous, because the DUTs can be soldered onto the same footprint and thus only one DUT board layout can be used for most DUTs[4] and all calibration standards. The layout used for the footprints of the DUTs is designed to accommodate chips in a SOT500-4 package, also known as MOA8 package [44]. The DUT boards depicted in Figure 2.5 have pin heads for the voltage probe to measure the voltage V_{DUT} as close as possible to the DUT. Most tips available for voltage probes are intended for contacting signals by hand instead of using fixed connectors. Pin headers are used together with a respective probe tip to guarantee that physical variations of the measurement system are kept as small as possible while connecting and disconnecting the probe as well as for ensuring a good contact throughout a measurement sweep. The voltage probe that has been used in this thesis is a single-ended probe. A differential voltage probe might bring an improvement in performance, because the single-ended probe seems to couple with ground. Unlike the sampler channels, it is not galvanically decoupled from the measurement circuit and is therefore susceptible to parasitic coupling with the large ground planes used in the layout. This also manifests in a lower probe input impedance than specified in the probe characteristics[5]. Nevertheless, the impact can be calibrated and a high measurement accuracy can still be achieved.

[4] All DUTs have been soldered onto the same footprint except chip **EM4200**, which has a slightly smaller footprint.

[5] According to the datasheet [42], the used voltage probe typically exhibits an input impedance of $|Z| \approx 14.6\,\mathrm{k\Omega}$ at a frequency of $f_{\mathrm{c}} = 13.56\,\mathrm{MHz}$.

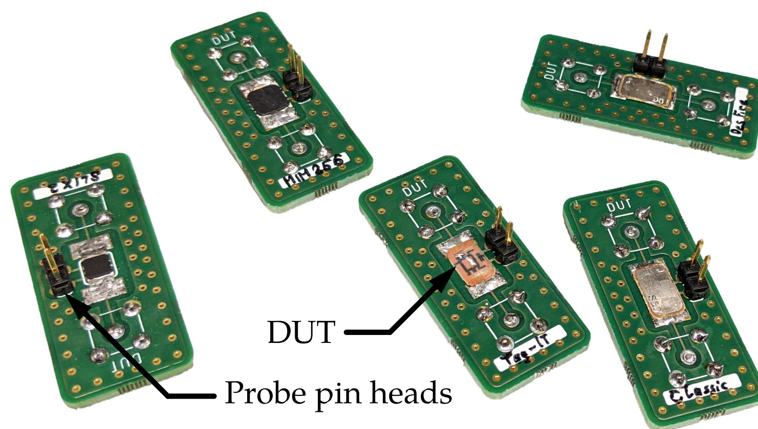

Figure 2.5: Photograph of several DUTs soldered onto DUT boards. Most of the DUTs characterized in this thesis have been extracted out of dissolved chip cards. This way, the availability of samples was better and they could be acquired in lower quantities. The depicted DUTs have been characterized and respective measurement results can be found in chapter 4.

CHAPTER 3

Calibration

In the field of RF measurements, it is common practice to calibrate any used measurement equipment. *Calibration* is an effective method that aims to characterize any systematic errors between the DUT port, i.e., the measurement reference plane, and the actual data acquisition plane, i.e., the sampler [45]. It accounts for non-idealities of any linear components used in the measurement setup like cables, connectors, transformers and PCBs. The correction of these systematic errors is called *de-embedding*, since it aims to compute a measurand embedded into an error network [46].
This chapter starts with the introduction of a calibration concept that has been derived for the RF I-V method of impedance measurement (refer to Appendix A for the full derivation). In a condensed manner, it will be explained how the concept can be applied and its impact on measurements will be analyzed mathematically. A section on the implementation of the calibration concept gives insights into practical considerations that have to be made in order to achieve good calibration results. This includes a discussion about the choice of used calibration standards, which is of particular significance because the theory differs from what is commonly applied when calibrating VNAs [23]. Finally, in the verification section, a novel method is proposed for verifying the validity of a conducted calibration.

3.1 Concept

The measurement setup introduced in chapter 2 and its corresponding electrical network representation, derivable from the block diagram in Figure 2.1, are entirely linear except for the DUT. Linear circuit theory can be applied to model the network and find a suitable way to calibrate for linear systematic errors.

The combination of the measurement board and the DUT board can be considered a fixture. In the field of RF measurements, fixtures are used to connect a DUT with measurement equipment, where the connector types are not matching. This is of particular interest for the characterization of SMT devices, where the DUT is connected via PCBs. The fixture can be a distributed, linear electrical network that is lumped together into a *fictitious error adapter* which is described using multiports [29]. Characterizing these multiports is called *calibration* and using them to compute the actual measurand (e.g., impedance) from the measured quantity (e.g., a voltage ratio) is called *de-embedding*. In RF measurements, this operation is considered as a shift of the measurement reference plane to the connectors (e.g., SMD pins) of the DUT. The linear *error terms* of the multiports are computed using a set of N well known *calibration standards* with N corresponding linearly independent measurements.

This theory is well known and documented in literature for the network analysis method of impedance measurements (e.g., VNA measurements), where the Scattering parameters (S-parameters) are determined by measuring transmitted and reflected waves. The impedance measurement system developed throughout this thesis is based on the RF I-V method of impedance measurements. As indicated by the name, the RF I-V method of impedance measurements aims to compute the impedance of a DUT from current and voltage signals [23]. In the case of the presented measurement system (as depicted in Figure 2.1), a measurement is defined as[1]

$$G = \frac{V_\mathrm{V}}{V_\mathrm{I}},$$

where V_V and V_I are the complex-valued voltage phasors of the voltage path (sampler CH1) and current path (sampler CH2), which are acquired by the sampler. This method is less well documented than the network analysis method of impedance measurements. A novel calibration method for the presented measurement system had to be developed. This has been done throughout a separate, independent project work, that can be found in Appendix A. The outcome of this project work is that a set of $N = 3$ error terms has to be determined to fully characterize the fixture. The error terms are determined using pairs of N well known calibration standards $Z_{\mathrm{cal},i}$ together with N corresponding linearly independent measurements G_i. Each of these pairs contributes to solving

[1] The variable G is not to be confused with a conductivity. It is a ratio of voltages and thus dimensionless. The notation comes from the field of signal flow graphs, where it can be understood as a *gain*.

a linear equation system (compare Equation A.38) of the form

$$a + Z_{\mathrm{cal},i}\, b + Z_{\mathrm{cal},i}\, G_i\, c = G_i\,, \qquad \text{calibration equation} \tag{3.1}$$

where $i \in \{1, 2, 3\}$. $Z_{\mathrm{cal},i}$ and G_i are the pairs of calibration standards and corresponding measurements and $E = \{a, b, c\}$ is the set of complex error terms that has to be computed. These error terms completely characterize the impact of any linear component on the impedance measurements between the sampler and the DUT. This includes the fixture as well as any cables and connectors used in the measurement system.

Rearranging the calibration equation (Equation 3.1) and solving for the impedance yields the de-embedding equation. It can be used to compute the impedance Z_{DUT} of a DUT from the measurement G (see Equation A.39):

$$Z_{\mathrm{DUT}} = \frac{G - a}{b + G\, c} \qquad \text{de-embedding equation} \tag{3.2}$$

With complete knowledge of the error terms E, Equation 3.2 can be used to correct linear systematic errors in any measurement G and compute the impedance of the DUT.

3.1.1 Mathematical Analysis

Solving the calibration equation (Equation 3.1) for G yields the embedding equation

$$G = \frac{b\,Z_{\mathrm{DUT}} + a}{-c\,Z_{\mathrm{DUT}} + 1}\,. \qquad \text{embedding equation} \tag{3.3}$$

From a mathematical point of view, the embedding equation corresponds to what is called a *Möbius transformation*. It has the general form [47], [48]

$$f(z) = \frac{\alpha\,z + \beta}{\gamma\,z + \delta}\,,$$

where z is an arbitrary complex number and α, β, γ and δ are complex-valued coefficients. Möbius transformations are *bijective conformal* maps [49]. Z_{DUT} can take any arbitrary value in the right complex half-plane, thus it is only constrained by $\Re\{Z_{\mathrm{DUT}}\} \geq 0$. In the following, this set of complex numbers will be termed *impedance plane (Z-plane)* while its transformation will be termed *measurement plane (G-plane)*. Möbius transformations map every straight line to a line or circle. *Bijection* gives us that every point in the Z-plane maps to exactly one point in the G-plane and vice versa. *Conformality* is a property of the transformation that preserves angles: two curves in one plane will intersect at the same angle as their respective transformations in the other plane. Figure 3.1 shows a possible Möbius transformation that maps the impedance plane into a circle in the measurement plane. Knowing a number of $N = 3$ points in one plane and their corresponding counterparts in the other plane, the transformation is defined completely [50]. Two characteristic points are of particular interest in the G-plane: The short circuit point is computed by forming the limit

$$G_0 = \lim_{Z \to 0} \frac{b\,Z + a}{-c\,Z + 1} = a\,. \tag{3.4}$$

The open circuit point is computed by forming the limit

$$G_\infty = \lim_{Z \to \infty} \frac{b\,Z + a}{-c\,Z + 1} = -\frac{b}{c}\,. \tag{3.5}$$

Möbius transformations play a role in several fields of electrical engineering. One well-known example is the *bilinear transform* used in digital signal processing that maps the left open half-plane in the complex Laplace plane (s-plane) into the unit circle of the complex z-plane of the Z-transform. Another example

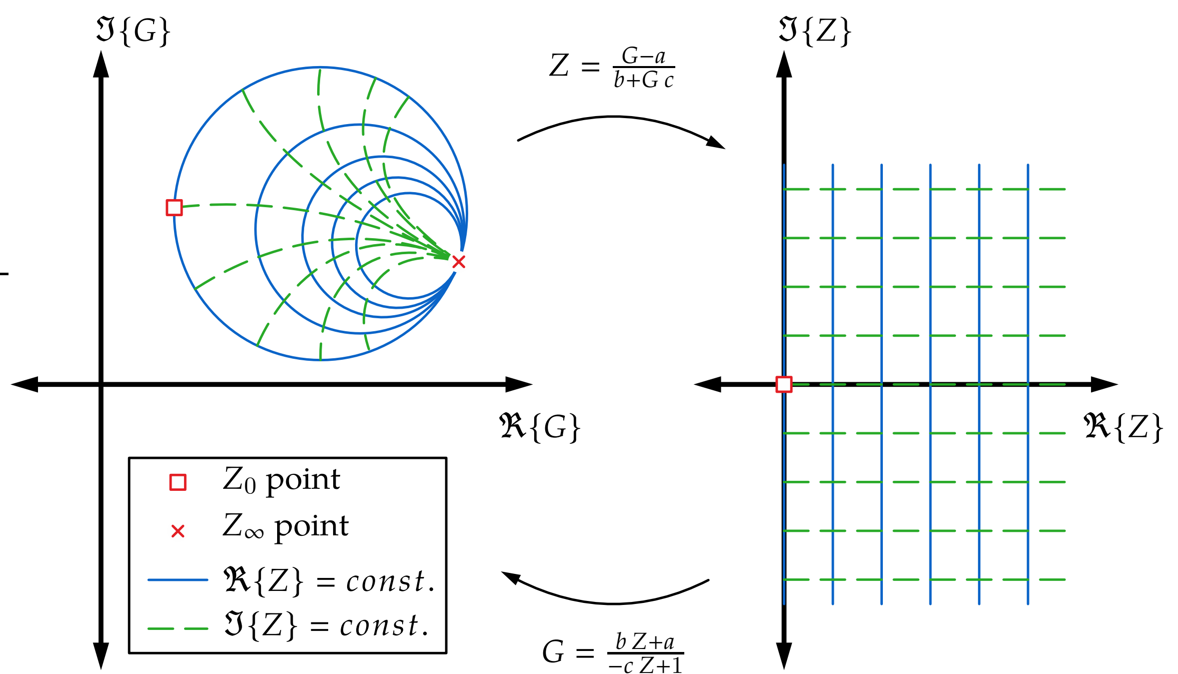

Figure 3.1: Sketch of a Möbius transformation. The $\Re\{Z\} = const.$ curves and $\Im\{Z\} = const.$ curves expand infinitely along the right complex impedance half-plane.

is the mapping of the right open impedance plane into the reflection coefficient plane (Γ-plane) that is used in *Smith charts*. In that case, it is common practice to normalize impedances Z to the characteristic impedance Z_w used in a system [51]:

$$z = \frac{Z}{Z_\mathrm{w}} \tag{3.6}$$

The short circuit point $\Gamma_0 = -1$ and open circuit point $\Gamma_\infty = 1$ are characteristic in the reflection coefficient plane. Applying the normalization of Equation 3.6 brings the benefit of giving the $z = 1$ point a significant physical meaning: the point where perfect matching is achieved and the reflection factor $\Gamma_\mathrm{m} = 0$. In the case of the Möbius transformation from the Z-plane to the G-plane as given in Equation 3.3, applying a normalization of the Z-plane would also be possible. Unfortunately, there would be no benefit to it in the G-plane, as there is no point with a significant physical meaning, that we would like to normalize to.

3.2 Implementation

Goal of the calibration process is the determination of the set of error terms E. The computational implementation of the calibration concept is straightforward. Solving a linear equation system (as given by Equation 3.1) is implemented in MATLAB using the `linsolve` function, which also supports complex numbers. The physical implementation poses a challenge in terms of manufacturing and accurately characterizing calibration standards.

For determining the error terms, $N = 3$ well known calibration standards have to be measured. Mathematically, any set of N linearly independent measurements makes the computation of the error terms possible. Considering a possible measurement uncertainty, it makes sense to choose standards, i.e., points in the Z-plane and G-plane, that are not located too closely to each other.
One-port calibrations of VNAs, for instance, are conducted using an Open Short Match (OSM)[2] calibration kit. This corresponds to a choice of the three characteristic points Z_∞, Z_0 and Z_m in the Z-plane. In an ideal case, that is, no calibration is necessary, the corresponding points in the Γ-plane would be $\Gamma_\infty = 1$, $\Gamma_0 = -1$ and $\Gamma_\mathrm{m} = 0$. If the reflection coefficient is determined as the ratio of reflected voltage waves V^- to the incident voltage waves V^+, the choice of the three

[2] The naming conventions for calibration kits vary between the manufacturers of measurement equipment. The name OSM is used by the company Rohde & Schwarz, while the name Short Open Load (SOL) is used by the company Keysight Technoloies.

Nominal value R	Characterized impedance Z_{cal}
$47\,\Omega$	$(46.984{+}0.112\text{j})\,\Omega$
$470\,\Omega$	$(468.36{-}1.210\text{j})\,\Omega$
$1\,\text{k}\Omega$	$(999.2{-}5.09\text{j})\,\Omega$

Table 3.1: Calibration standards characterized using a VNA (ZVL 3, Rohde & Schwarz) and a custom-built set of a fixture and corresponding calibration kit [52].

characteristic points for the calibration is physically useful since the reflection coefficient takes well measurable values within the unit circle of the Γ-plane.
This is not the case for a system working with the RF I-V method of impedance measurement. A measurement G is defined as the ratio of voltage in the voltage path V_{V} to the voltage in the current path V_{I}. In an ideal case, where no calibration is necessary, using an open circuit as a calibration standard would lead to a diverging voltage in the voltage path $V_{\text{V}} \to \infty$ and a voltage in the current path that would converge towards 0. Consequently, also G_∞ would also diverge towards ∞. Even in a real circuit, where G_∞ takes finite values, they might not be well defined. Especially if V_{I} gets very small and the measurements are dominated by noise. If the $N = 3$ points in the G-plane are not well defined, the mapping between Z-plane and G-plane, i.e., the calibration, may be associated with a high error. This turned out to be the case when conducting calibrations with an open standard and no voltage probe connected to the circuit: The very high impedance of the open standard resulted in a badly defined point G_∞ and thus an erroneous calibration.
For that reason, the calibration standards listed in Table 3.1 have been manufactured for the calibration of the presented measurement system. For making the calibration standards, SMD resistors have been used. The resistances have been chosen such that the first calibration standard is set close to the minimum expected DUT impedance. The resistance of the last calibration standard has been chosen in a range close to the maximum expected DUT impedance, yet small enough to avoid the problem occurring with an open standard. High reliability metal film resistors are used which have a good temperature stability and low tolerance. The resistors were characterized using a VNA (ZVL 3, Rohde & Schwarz) together with a custom-built fixture and corresponding OSM calibration kit. It should be noted that the accuracy of the characterized impedances of the calibration standards in Table 3.1 depends on the measurement accuracy of the used VNA, the uncertainties of the OSM calibration kit and manufacturing tolerances of the fixtures. Consequently, the characterization has an uncertainty

Nominal value R	Characterized impedance Z_{ref}
100 Ω	(99.994+0.005j) Ω
220 Ω	(219.78−0.328j) Ω

Table 3.2: Reference standards characterized using a VNA (ZVL 3, Rohde & Schwarz).

which in turn affects the accuracy of the calibration.

One example of a calibration of the measurement system presented in chapter 2 is shown in Figure 3.2. Depicted is an impedance grid that has been mapped into the G-plane. The calibration standards $Z_{\mathrm{cal},i}$ from Table 3.1 are depicted which have been used to compute the calibration, i.e., the mapping of the Z-plane to the G-plane. The mapping of the characteristic points Z_0 and Z_∞ into the G-plane has been computed using Equations 3.4 and 3.5. Furthermore, reference standards (see Table 3.2) are plotted as red circles, while corresponding measurements are marked as black crosses. All calibration standards and reference standards are located on the $\Im\{Z\} = 0$ curve.

3.3 Verification

After calibrating, the validity of the calibration should be verified. The process of calibrating usually involves connecting and disconnecting calibration standards which inevitably alters the physical geometry of the measurement system and introduces errors. Through elaborate system design and appropriate handling through the operator, these errors are usually kept as small as possible. However, it might happen, that improper connections are made during the calibration process. To avoid such errors, it is good practice to verify that a valid calibration has been conducted.

In this work, for the purpose of quickly detecting such errors, reference standards are measured after the calibration process. The reference standards in Table 3.2 are measured additionally to the calibration standards. After the calibration (i.e., the set of error terms E) has been computed, the operator can check its validity by comparing the measured values of the reference standards with their characterized (assumed "true") target values. This is implemented to be done graphically by comparing a corresponding plot in the G-plane or in the Z-plane.

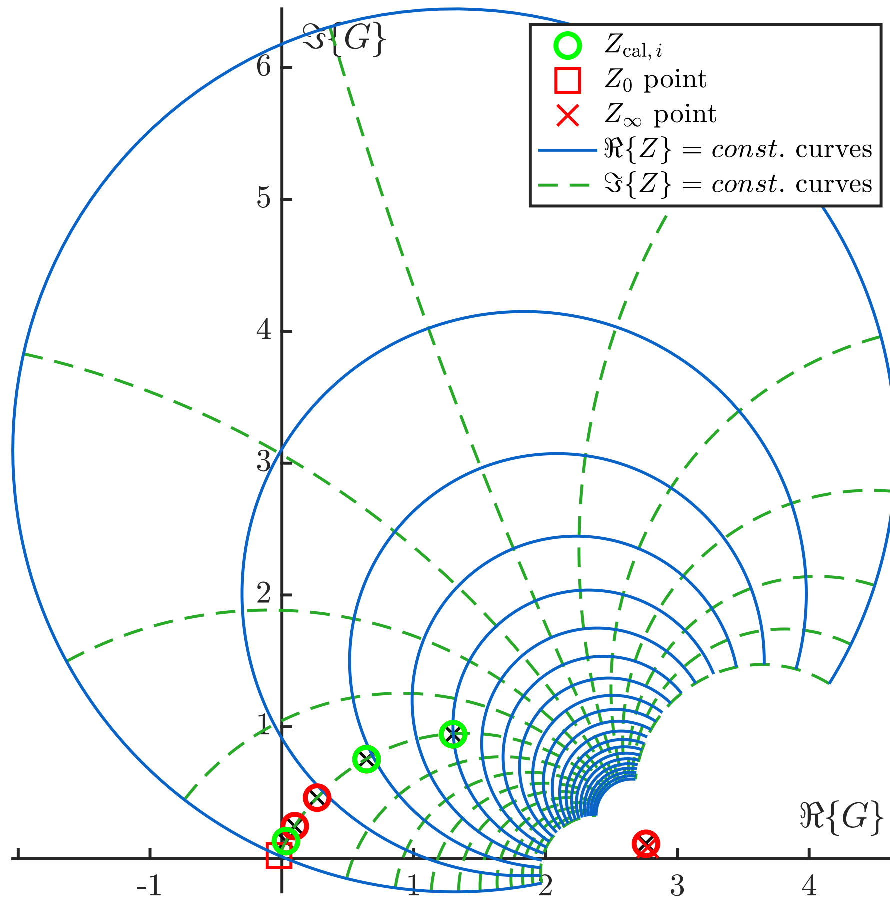

Figure 3.2: G-plane with the transformed grid of $\Re\{Z\} = const.$ curves and $\Im\{Z\} = const.$ curves from the calibration of measurement series No. 56. The corresponding impedance grid is spaced at 250 Ω along both the real and imaginary axes and limited by $-2.5\,\mathrm{k\Omega} \leq \Im\{Z\} \leq 2.5\,\mathrm{k\Omega}$ and $0\,\Omega \leq \Re\{Z\} \leq 5\,\mathrm{k\Omega}$ for computational purposes, thus the $\Re\{Z\} = const.$ circles are incomplete. The calibration standards $Z_{\mathrm{cal},i}$ from Table 3.1 are used to define the mapping.

Isoerror Curves:
For the purpose of verifying the validity of the calibration, a plot of the G-plane is presented to the operator of the measurement system (see Figure 3.3). It shows the standards used for the calibration along with the ideal target positions $Z_{\mathrm{ref,t}}$ of the reference standards and corresponding measured impedances $Z_{\mathrm{ref,m}}$. The chosen standards in Tables 3.1 and 3.2 are ideally purely resistive. Consequently, large deviations from the $\Im\{Z\} = 0$ curve indicate possible errors. To give the operator a notion about the size of this error, curves of constant relative errors $\delta_Z \in \{1\,\%, 5\,\%, 10\,\%\}$ are depicted as *contour plot* around the $\Im\{Z\} = 0$ curve according to Equation 1.6. These curves are termed *isoerror curves*. After conducting a calibration, if the operator identifies that the positions of the measured impedances $Z_{\mathrm{ref,m}}$ of the reference standards do not match well with

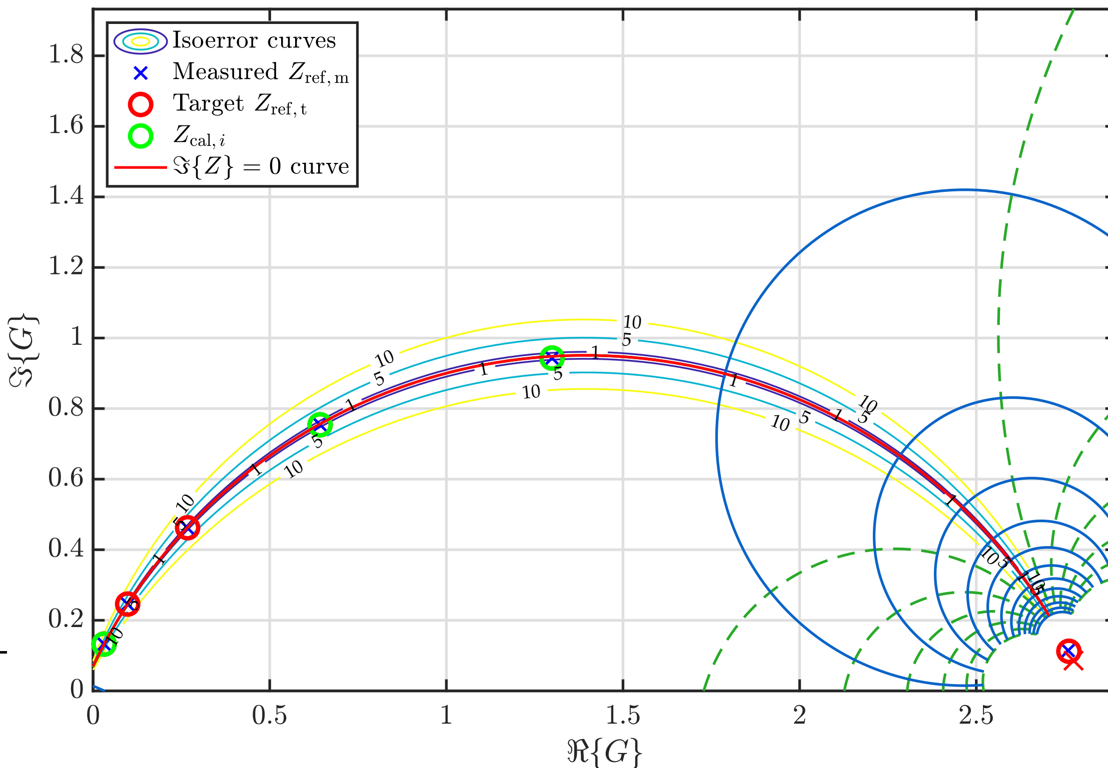

Figure 3.3: Isoerror curves for the calibration of measurement No. 56 in the measurement plane to check the validity of the calibration.

The results presented throughout this work (see section 4.3) have all been generated using valid calibrations. Their accuracy has been verified to lie well within the $\delta_Z = 2\,\%$ error bound and will be discussed in detail in section 4.2.

CHAPTER 4

Measurements

Throughout this chapter, the acquired results of several individual measurement series will be presented. For comparability reasons, all measurement series have been conducted in the same manner. The exact measurement procedure will be introduced in the first section of this chapter. Evaluating the measurement quality is an integral part of accurate RF measurements. The measurement *accuracy* of the system can be estimated by comparing measurements of well known reference standards with their known (i.e., assumed true) values. The *repeatability* of the system is verified by comparing the results of several measurement series with each other. The measurement *uncertainty* is discussed along with the handling of remaining systematic errors. These quality indicators are presented in the second section of this chapter. After having explained the measurement procedure and evaluated accuracy, repeatability and uncertainty, the actual measurement results can be presented. The third section shows the results of all DUTs measured during one particular measurement series. The curves are presented together with an estimated uncertainty range that indicates, how much the measurements can be trusted in a certain region of the supplied voltage V_{DUT}. Along with the results, subsequent analyses are presented: By means of analytic computations, it can be estimated, how well a characterized chip would perform in a parametrically known chip card (see section 4.3.1).

4.1 Measurement Procedure

A measurement procedure is a set of operations performed in order to conduct a measurement [22]. Several *series of measurements* have been conducted throughout the process of developing the measurement system. The final measurement series, i.e., those performed with the final version of the measurement system,

are presented in this thesis. The measurement procedure encompasses the following set of operations which have been performed in the exact same order throughout all measurement series:

1. Initialization
2. Calibration
   a) Measurement of calibration standards
   b) Verification of the calibration using reference standards
3. Characterization of DUTs
4. Accuracy verification by measuring reference standards

Initialization:
Before the measurement system can be used, the operator PC has to make connections with all supply and measurement devices. The devices have to be initialized, i.e., all necessary parameters set, and put into a state ready to conduct the first measurements. Special care has to be taken regarding the AWGs: although the devices can automatically synchronize their clocks in frequency, an alignment in phase can only be achieved by the operator PC with respective voltage measurements of the sampler (see Figure 2.2).

Calibration:
In the calibration step, the AWGs output a small voltage of $1\,\mathrm{V_{pp}}$ on each channel. Three different calibration standards $Z_{\mathrm{cal},\,i}$ with $i \in \{1, 2, 3\}$ are plugged onto the measurement board (see Figure 2.4) by the operator. Corresponding measurements $G_{\mathrm{cal},\,i}$ are taken by the sampler in magnitude and phase. These three linearly independent measurements allow to compute the three error terms needed for the calibration.
For verification purposes, another set of known reference standards is measured and the measurement results are compared against their known impedance using the computed calibration. This allows the operator to quickly evaluate, whether a valid calibration has been achieved or an obvious operating mistake has been made. This method is described in detail in section 3.3.

DUT Characterization:
After the calibration has been validated, the operator can start characterizing DUTs. With a DUT board plugged onto the measurement board, a voltage sweep can be started. Depending on the number of sweep points set by the operator,

the measurement system will start linearly increasing the output voltage of the AWGs. During the sweep, a measurement plot is generated and updated once a new result point of the sweep becomes available. One out of four possible events listed below may end a measurement sweep.

- The chosen maximum sweep voltage has been reached.
- The dynamic range of the voltage path has been exceeded.
- The dynamic range of the current path has been exceeded.
- The dynamic range of the voltage probe has been exceeded.

The latter three of those events will be indicated to the operator by a `warning` in MATLAB. After one sweep has been completed, the results can be saved by the operator and a new DUT can be inserted into the measurement board. The measurements in this thesis have always been conducted in the same order (i.e., starting and ending with the same chips). This order is also reflected by the arrangement of Figures depicting results in this chapter. In this thesis, rather than using the specific name of the characterized DUTs, they are given nicknames and marked with the following tags: **< NAME >** .

Accuracy Verification:
In a final step, the reference standards are measured again, using the same measurement sweeps as for the DUT characterization. This way, a possible measurement drift and systematic errors introduced by the measurement sweep can be detected. An analysis of these measurements resulted in a relative measurement error $\delta_Z < 2\,\%$ for the measurement results presented in this thesis.

4.2 Verification

In the field of RF measurements, it is good practice to verify measurement results. In this chapter, three important quality measures will be investigated: *accuracy*, *repeatability* and *uncertainty*. All three assess the performance of the measurement system and validate the measurement results.
The result of the uncertainty estimation is used together with the measurement results to indicate how much the results can be trusted in certain regions of the measurement.

4.2.1 Measurement Accuracy

The accuracy of a measurement states how close the measurand agrees with the result of the measurement [22]. There are several ways to estimate the accuracy. In the most convenient case, the accuracy of one measurement system can be determined with another, more accurate reference measurement system. Unfortunately, in most cases, more accurate measurement systems are not available. Therefore we have to use another method to assess the measurement accuracy of the system: After the system has been calibrated, the measurement accuracy can be evaluated by measuring known reference standards Z_{ref}. This is also done as a final step of the calibration process.
In this chapter, we want to verify the measurement accuracy where the measurand is in the range of interest. Hence, we measure reference standards, that have an impedance in a range that is typical for the input impedance of chips.

Nominal values		Reference impedance Z_{ref}	Measured impedance Z_{meas}	Relative error δ_Z
R_p	C_p			
100 Ω	68 pF	(75.15−43.80j) Ω	(73.94−43.77j) Ω	1.39 %
220 Ω	68 pF	(85.65−108.3j) Ω	(84.71−107.3j) Ω	1.02 %
10 kΩ	22 pF	(27.38−555.8j) Ω	(31.26−554.5j) Ω	0.74 %

Table 4.1: Reference standards used to evaluate the measurement accuracy.

Table 4.1 shows the reference standards used for evaluating the accuracy of the measurement system. A parallel connection of an SMD resistor and capacitor is used. The characterized impedance values Z_{ref} have been measured with a VNA (ZVL 3, Rohde & Schwarz) and are assumed to be the "true" impedance values. Note, that the "true" value of a measurand is indeterminate [22], [25] and the VNA measurements are the best estimate of the measurand. The impedances Z_{meas} measured with the measurement system are in good correspondence with the VNA measurements. The relative errors δ_Z lie well below 2 %.

Given the values of the relative error in Table 4.1, the accuracy of the system is estimated in three distinct points of the complex impedance plane. Having measured the corresponding three points G_{meas} in the measurement plane, it is possible to compute another conformal mapping of the impedance plane to the measurement plane, i.e., another set of error terms. This corresponds to computing a calibration as explained in chapter 3.1.1. By comparing this second conformal mapping, computed using the reference standards with the conformal mapping computed using the calibration standards, an accuracy estimation can be computed for the entire impedance plane or measurement plane, respectively.

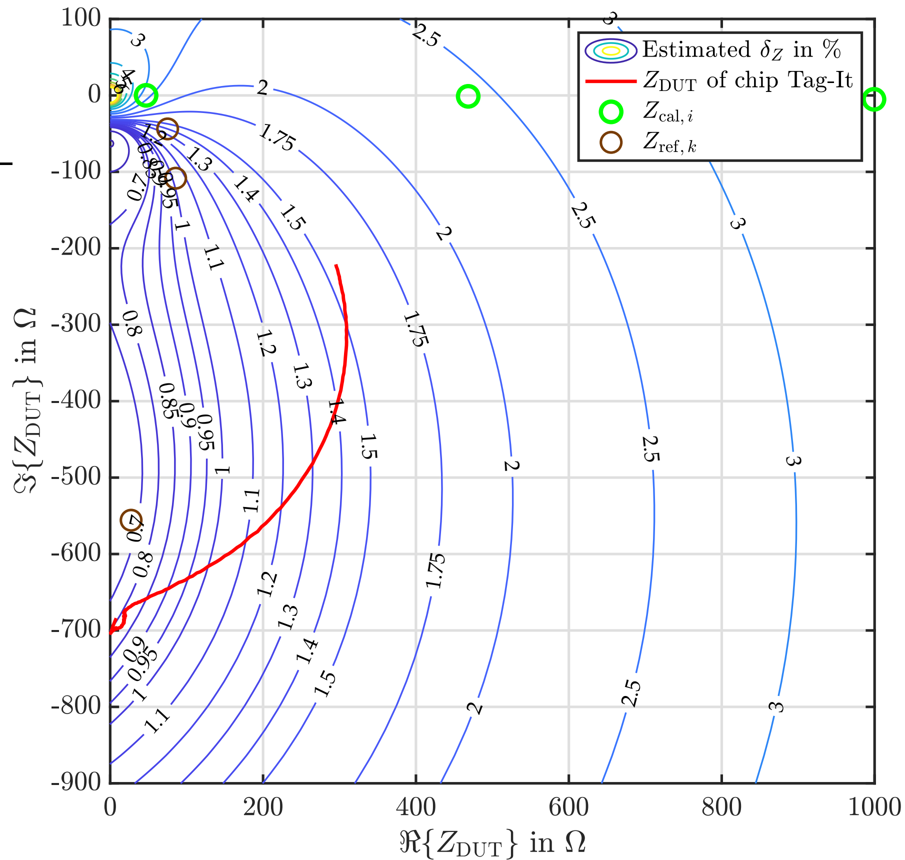

Figure 4.1: Estimated accuracy of a chip measurement in the impedance plane.

TAG-IT

This accuracy estimation in Figure 4.1 has been computed by comparing the conformal mappings computed using calibration standards and reference standards. It shows a portion of the right complex half-plane that encompasses the typical range for input impedances of chips. For demonstration purposes, the measurement curve Z_{DUT} of chip **TAG-IT** from measurement series No. 56 is plotted in this plane. It can be observed that the measurement accuracy is estimated to lie well within the δ_Z error bound of 2 %.

4.2.2 Measurement Repeatability

By comparing the results of different measurement series with each other, the repeatability of the measurement system is evaluated. Figure 4.2 depicts the measurement results of five different measurement series for the chip **NTAG**. Each of those series has been measured with an individual calibration and the measurements have been conducted over the course of several days. The individual curves in Figure 4.2 show a good correspondence and therefore verify that the system has a good measurement repeatability.

NTAG

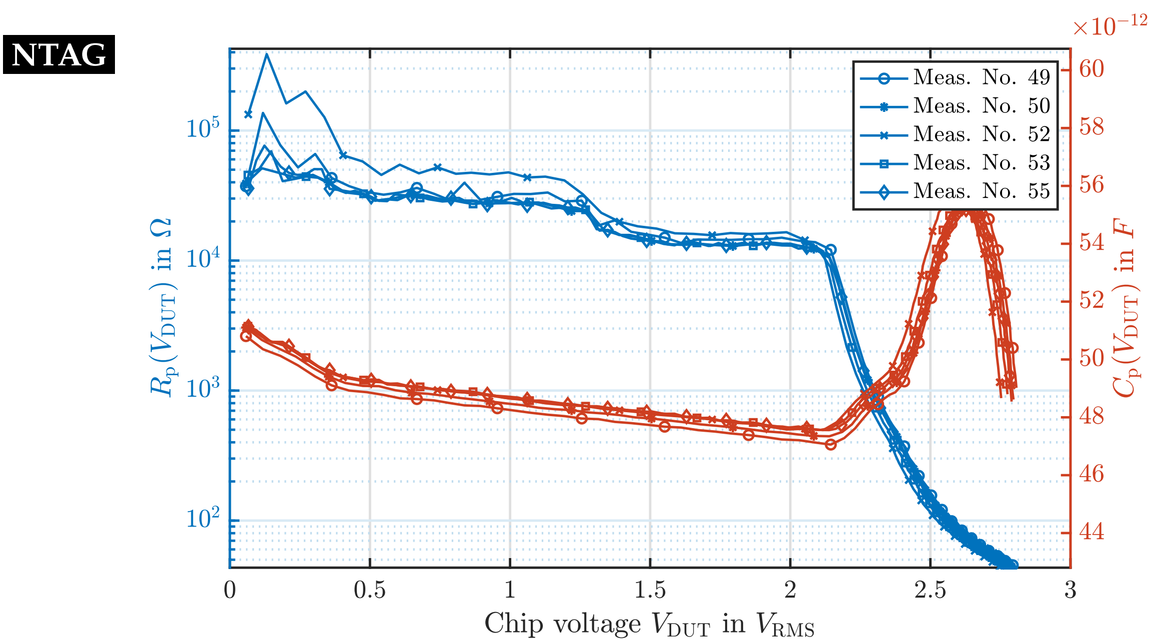

Figure 4.2: Measurement repeatability evaluation.

For the achievement of a good measurement repeatability, it is crucial that a whole measurement series is conducted under conditions that are held as constant as possible. While changing DUTs, the individual DUT boards as well as the voltage probe have to be disconnected and connected again. This causes physical variations of the measurement setup that shall be held as small as possible.

The measurement repeatability has been verified for all chips that have been characterized throughout this thesis. The corresponding measurement data is depicted in Appendix B.

4.2.3 Measurement Uncertainty

Measurement uncertainties can be of random or systematic nature [25]. When dealing with random effects, the estimation of the true value of the measurand improves with the number of observations. For the estimation of the impedance Z_{DUT} at a certain voltage $V_{\mathrm{DUT}} = const.$, the mean

$$\mu_Z = \frac{1}{N_{\mathrm{m}}} \sum_{i=1}^{N_{\mathrm{m}}} Z_{\mathrm{DUT},\,i} \tag{4.1}$$

is computed of $N_{\mathrm{m}} = 10$ measurements of the impedance Z_{DUT}. During the characterization of one particular DUT, for every sweep point of V_{DUT}, the mean μ_Z is taken as the best estimate of the measurand.

When computing the measurement uncertainty, it is assumed that after the correction (i.e., de-embedding) of systematic errors, no further distinction can be made between random and systematic effects [25]. Therefore, they are treated as a contribution to random errors. In the measurement system proposed in this thesis, long observation times and large numbers of measurements N_{m} helped to mitigate the impact of random errors like noise on the signal up to a point, where the random effects are of negligible significance.
However, even after calibrating the measurement system, there is a small systematic error left that might originate from non-idealities of calibration standards or incomplete error modeling. As mentioned in section 4.2.1, there exists knowledge of the remaining systematic error but no further correction is applied after the calibration. In the Guide to the Expression of Uncertainty in Measurement (GUM) [22, Annex F, section F.2.4.5], a method is proposed for reporting a measurement result in cases where a correction for a significant systematic error is not applied. The method aims to expand the "uncertainty" such that the systematic error is incorporated in the reported result. In the following, this method will be applied in order to compute an uncertainty region, sometimes termed *confidence region* [53], around the measurement results. This leads to a more complete way of reporting the measurement results.

Measurement uncertainty incorporating a remaining systematic error:
The following method is a discrete approximation of the mentioned approach stated in the GUM. First, the corrections

$$b_k = Z_{\mathrm{ref},\,k} - Z_{\mathrm{meas},\,k}$$

are computed, where $k \in \{1 \ldots 5\}$ and the reference impedances $Z_{\mathrm{ref},\,k}$ and their corresponding measurement results $Z_{\mathrm{meas},\,k}$ are given in Tables 4.1 and 4.2.

Nominal value R	Reference impedance Z_{ref}	Measured impedance Z_{meas}	Relative error δ_Z
$100\,\Omega$	$(99.99-0.005\mathrm{j})\,\Omega$	$(99.81-0.124\mathrm{j})\,\Omega$	$0.22\,\%$
$220\,\Omega$	$(219.8-0.033\mathrm{j})\,\Omega$	$(219.5-0.570\mathrm{j})\,\Omega$	$0.16\,\%$

Table 4.2: Reference standards used together with those mentioned in Table 4.1 for the estimation of the measurement uncertainty.

From that, a *single mean correction* is computed

$$\overline{b} = \frac{1}{M_{\mathrm{ref}}} \sum_{k=1}^{M_{\mathrm{ref}}} b_k \approx (-0.259 - 0.406\mathrm{j})\,\Omega\,,$$

where $M_{\mathrm{ref}} = 5$ is the number of reference standards that is available.

The *unbiased sample variance* is computed using

$$s_b^2 = \frac{1}{M_{\mathrm{ref}} - 1} \sum_{k=1}^{M_{\mathrm{ref}}} (b_k - \overline{b})(b_k - \overline{b})^* \approx 4.824\,\Omega^2\,.$$

Note that the denominator $M_{\mathrm{ref}} - 1$ comes from the *Bessel correction* [54] which has been applied because of the limited population of size M_{ref}. This unbiased sample variance is used as a single value[1] for the standard uncertainty $u_c = s_b$, that shall be used for all estimates.

This uncertainty is then enlarged by a *coverage factor* k to yield the *expanded uncertainty*

$$U = k\,s_b = k\,u_c \approx 6.589\,\Omega\,,$$

where a large factor $k = 3$ is chosen to compensate for the limited trust in the sample variance due to the small number of reference standards available.

Consequently, the measurand Z_{DUT} yields

$$Z_{\mathrm{DUT}} = Z_{\mathrm{meas}} + \overline{b} \pm U\,. \qquad (4.2)$$

[1] Note that the mean variance of the correction and the mean variance of the measurand mentioned in the GUM [22] have not been computed here, thus their impact is neglected. This choice has been made due to the fact that the statistic variations of $Z_{\mathrm{meas},k}$ in a single measurement point k are already minimized by computing the mean of N_{m} measurements (see Equation 4.1).

This result will be used in the presentation of the measurement results in the next section: using the mean correction $\overline{b}$ and the expanded uncertainty U, an uncertainty region can be plotted around the curves for the parallel resistance R_p and parallel capacitance C_p. This work is the first to examine the measurement uncertainty associated with R_p and C_p, which distinguishes it from related work.

4.3 Results

In this section, the measurement results from the characterization of 17 different DUTs are presented in Figures 4.3 through 4.19. In most related works where the input impedance Z_DUT of chips has been measured, the computed values for R_p and C_p are presented. Impedance measurements show, that a capacitive behavior dominates for low chip voltages V_DUT and a resistive behavior dominates for high chip voltages. This is due to the limiter behavior [55]. While one component is dominant and can be computed accurately, the other might be subject to a high uncertainty. This is also reflected by the uncertainty ranges presented along with the measurement results. For low chip voltages, the uncertainty range for R_p is large, while C_p can be determined accurately. For high chip voltages, the uncertainty range for C_p is large, while R_p can be determined accurately.

All results presented in this chapter show values for the parallel resistance $R_\mathrm{p,\,meas}$ and parallel capacitance $C_\mathrm{p,\,meas}$ which have been computed from the measurement results Z_meas using Equation 1.5. The curves are presented along with the uncertainty ranges ΔR_p and ΔC_p that incorporate the single mean correction $\overline{b}$ as well as the expanded uncertainty U according to Equation 4.2. That is, Equation 1.5 has been used to compute the upper and lower bounds of ΔR_p and ΔC_p through the estimated upper and lower bounds of the measurand Z_DUT incorporating U and $\overline{b}$, according to Equation 4.2. Furthermore, a $1\,\%$ tolerance has been added to these uncertainty ranges in order to incorporate minor systematic errors. This is reasonable, since the results of individual measurement series are subject to minor systematic variations[2] despite the good overall measurement repeatability (see Figure 4.2). In addition to the uncertainty ranges, *average curves* $R_\mathrm{p,\,avg}$ and $C_\mathrm{p,\,avg}$ have been computed using the mean of 5 different measurement series[3].

[2] Note that the uncertainty associated with the measurement of V_DUT is not considered in this work.

[3] For all DUTs, a number of 5 measurement series has been used to compute the mean except for **EM4200** , **GT5652** , **GT5670** and **UNKNOWN** , where 4 measurement series have

The average curves of some DUTs are not covered by the uncertainty ranges ΔR_{p} and ΔC_{p}. This comes from the fact that only the uncertainty of the impedance measurement is taken into account, but the uncertainty of the voltage measurement of V_{DUT} is unregarded. Furthermore, the uncertainty ranges have not been plotted for some chips[4] (e.g., **SLIX2** , see Figure 4.4), where the chip voltage V_{DUT} is not monotonically increasing with the supply voltage V_{AWG}.

been used and **FM388** , where 3 measurement series have been used.

4 The uncertainty ranges have not been plotted for the chips **SLIX2** , **GT5680** and **GT5652** .

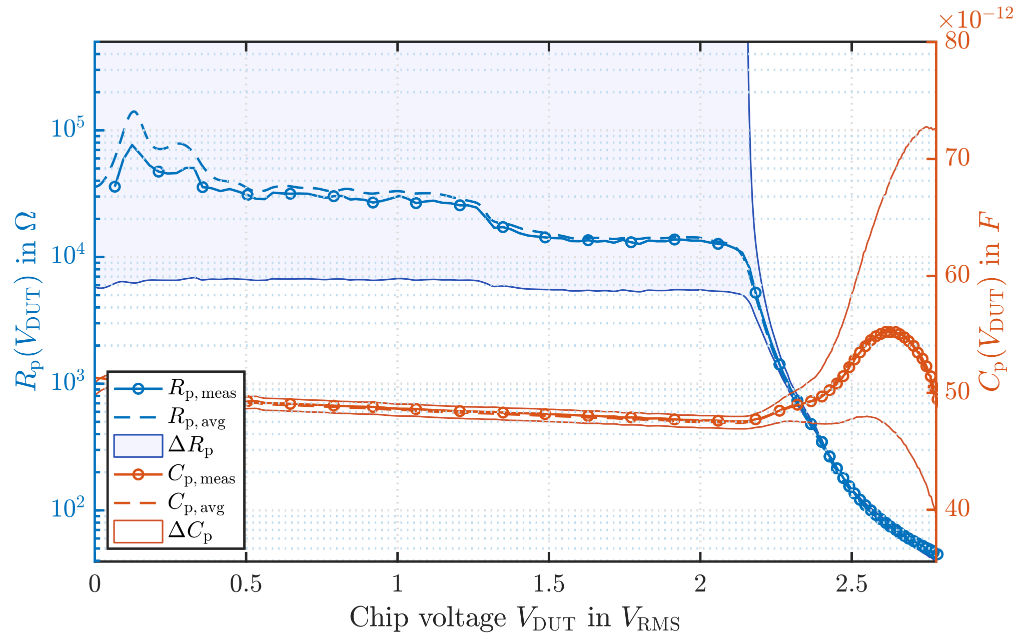

Figure 4.3: Input impedance measurement.

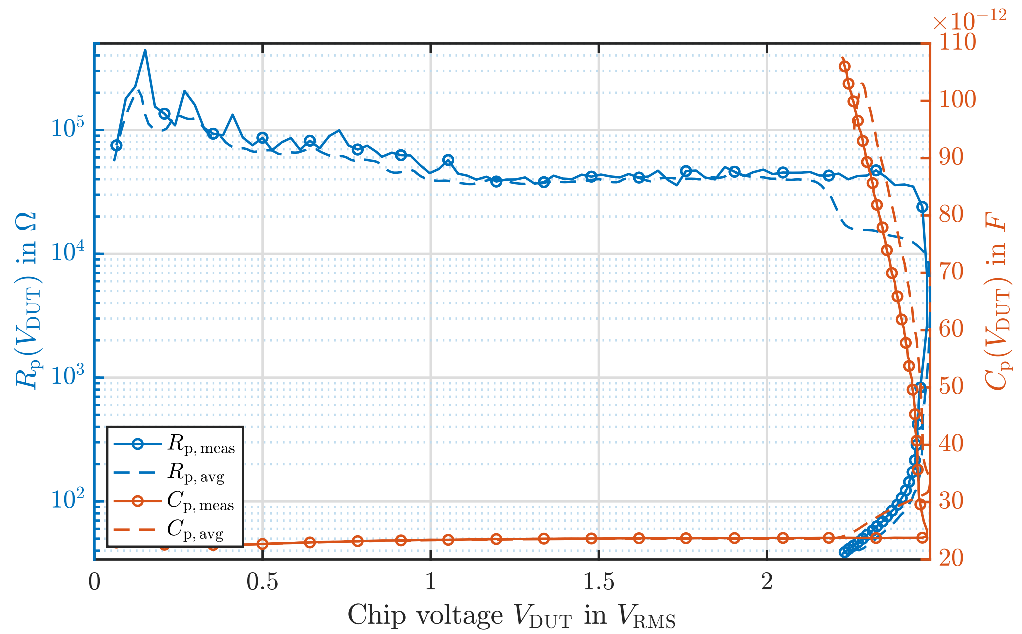

Figure 4.4: Input impedance measurement.

DesFire

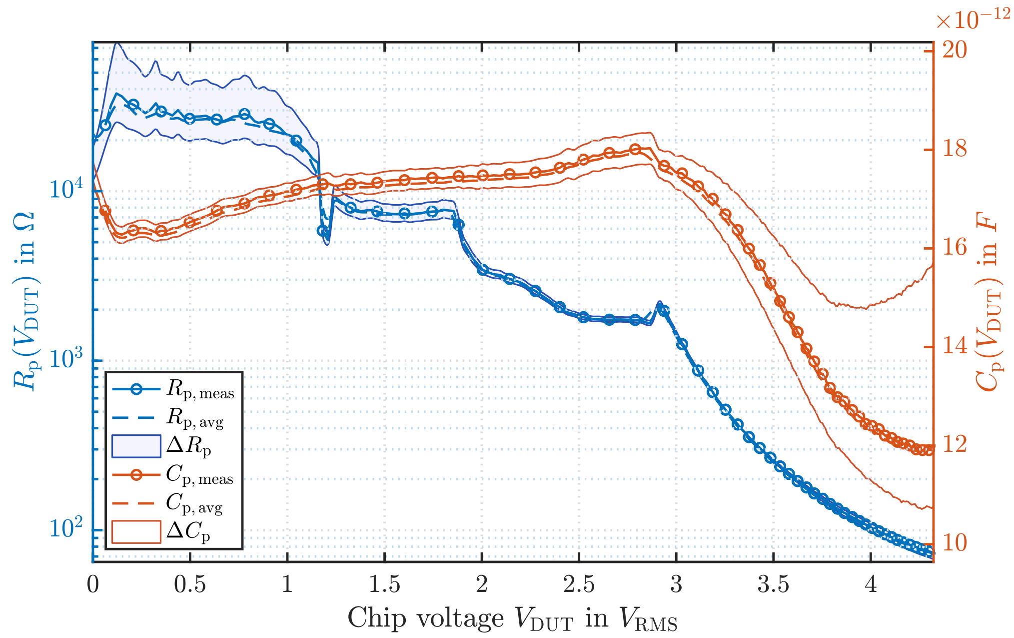

Figure 4.5: Input impedance measurement.

Ultral

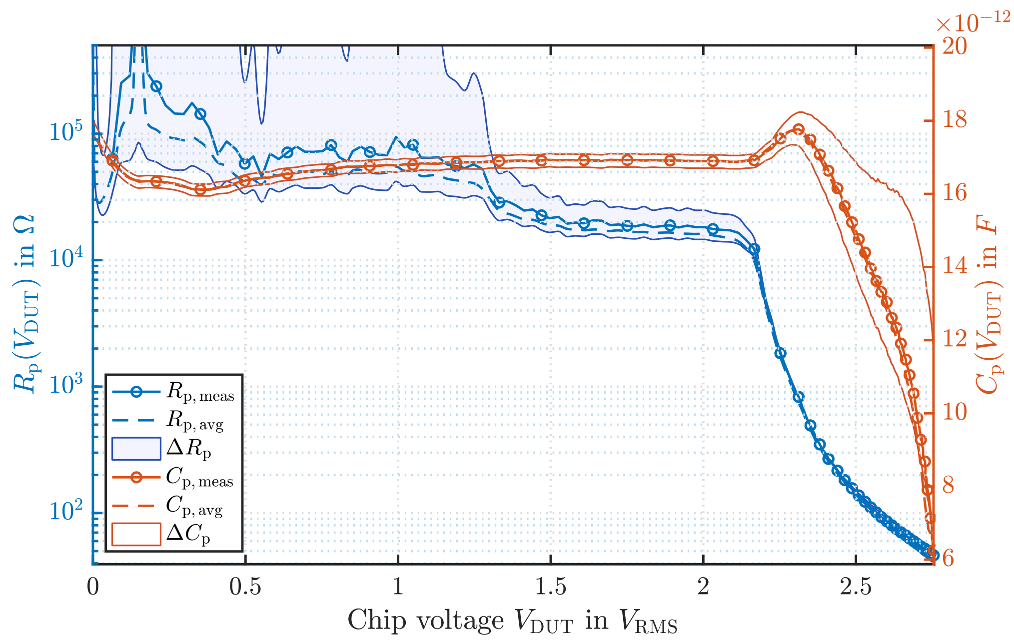

Figure 4.6: Input impedance measurement.

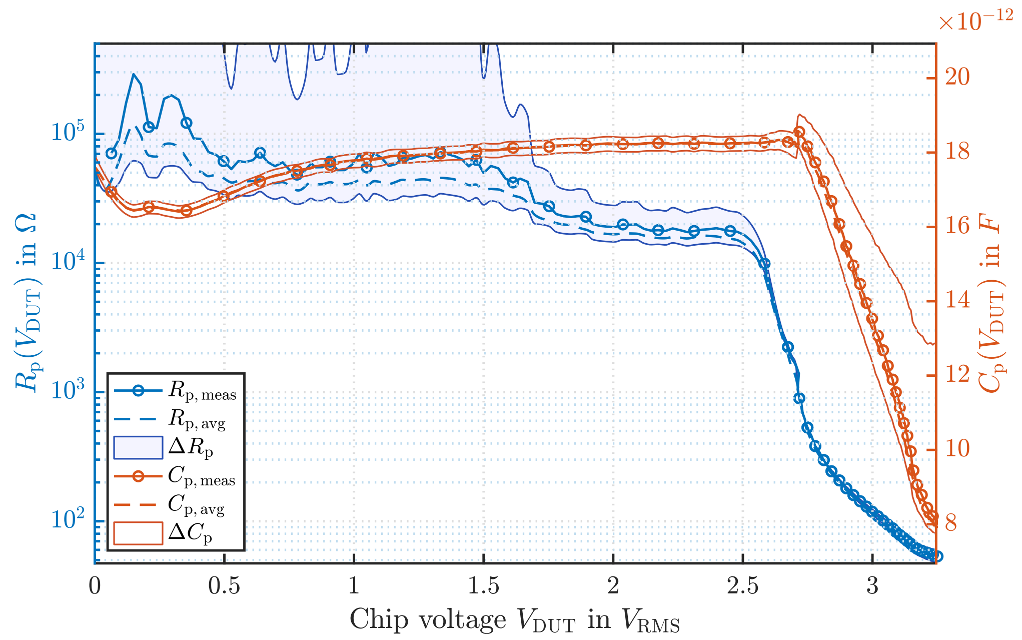

Figure 4.7: Input impedance measurement.

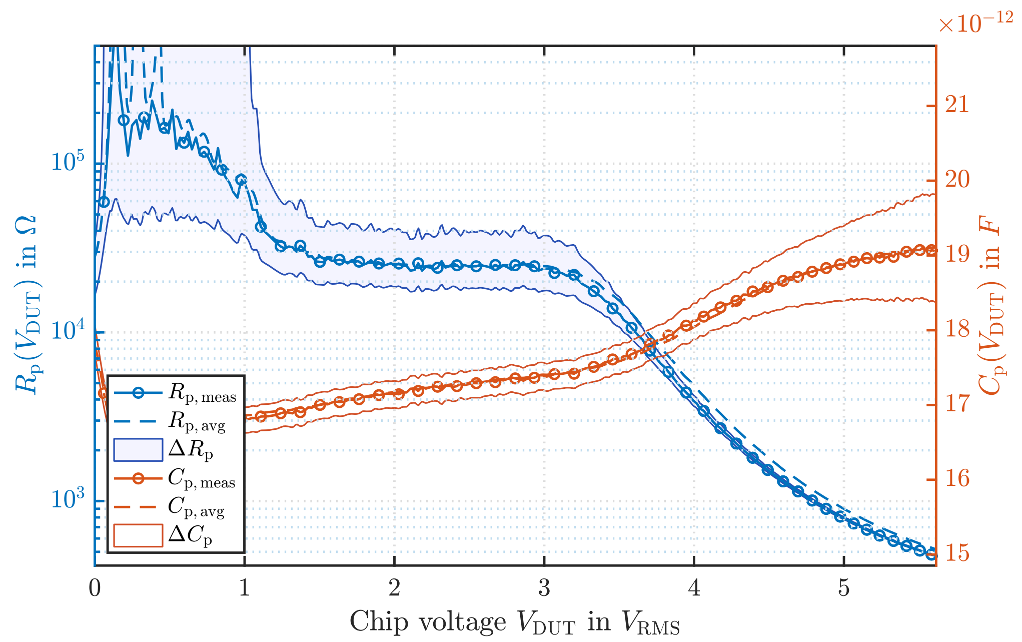

Figure 4.8: Input impedance measurement.

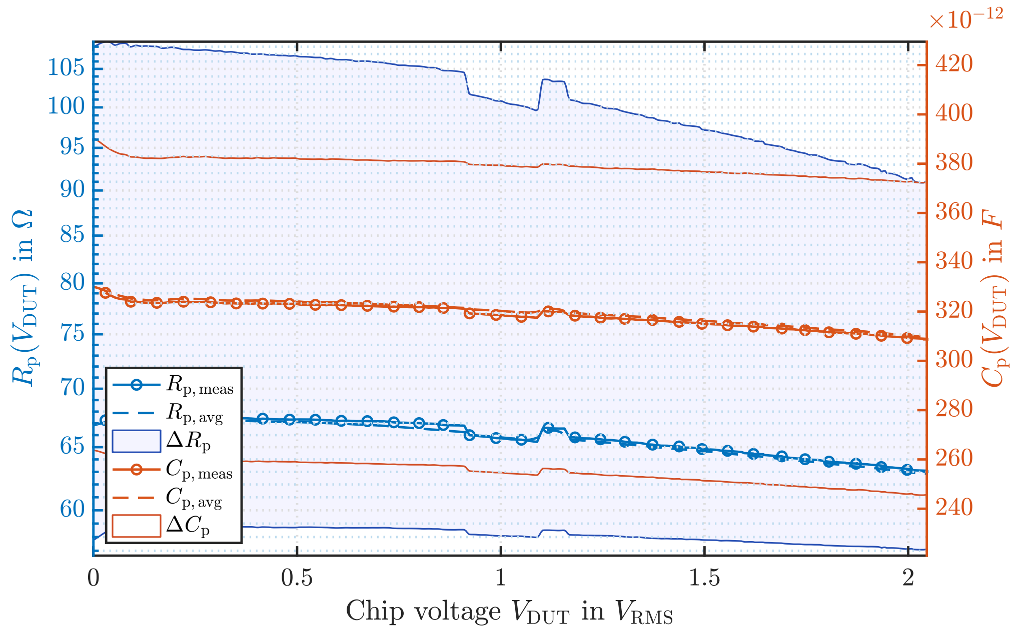

Figure 4.9: Input impedance measurement.

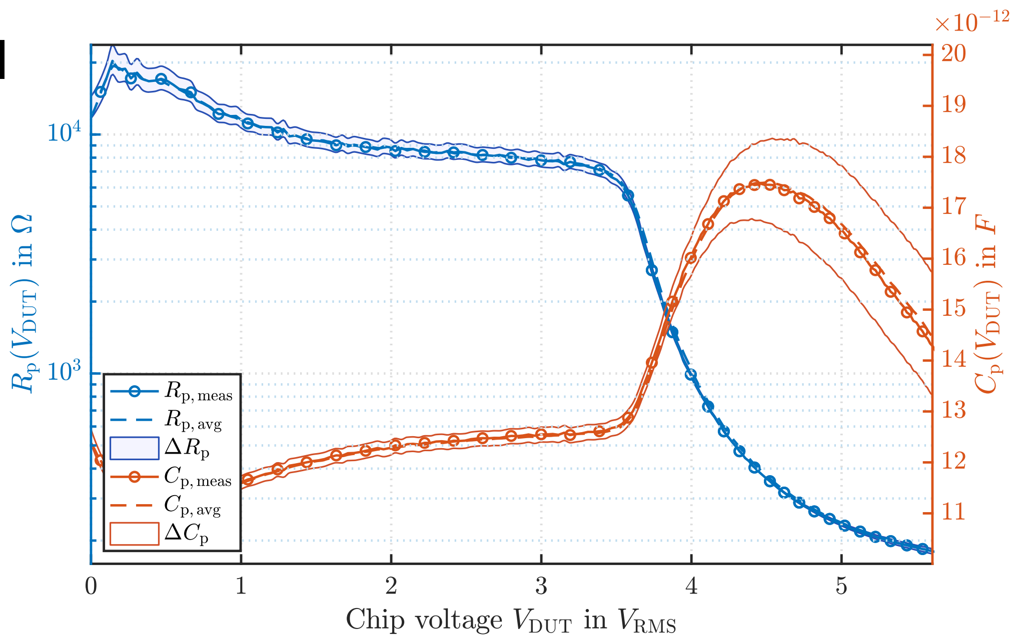

Figure 4.10: Input impedance measurement.

K50

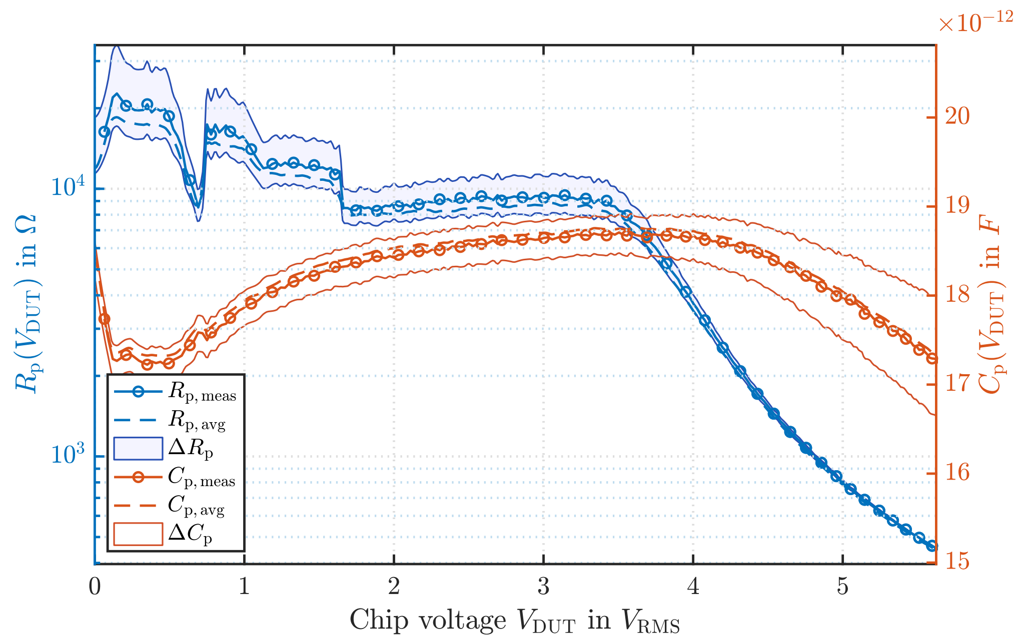

Figure 4.11: Input impedance measurement.

TKS50

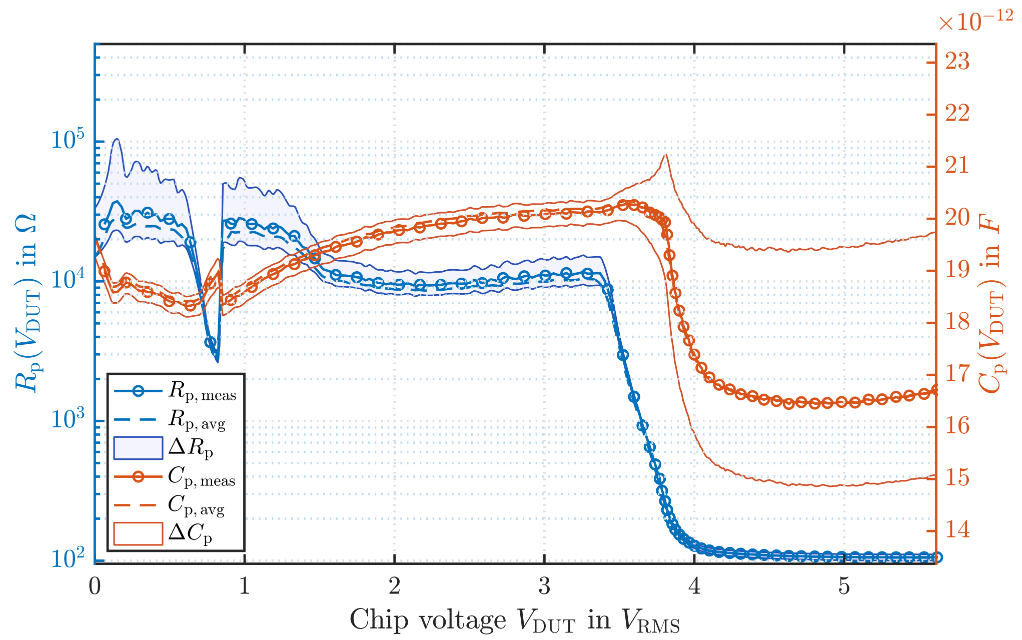

Figure 4.12: Input impedance measurement.

FM248

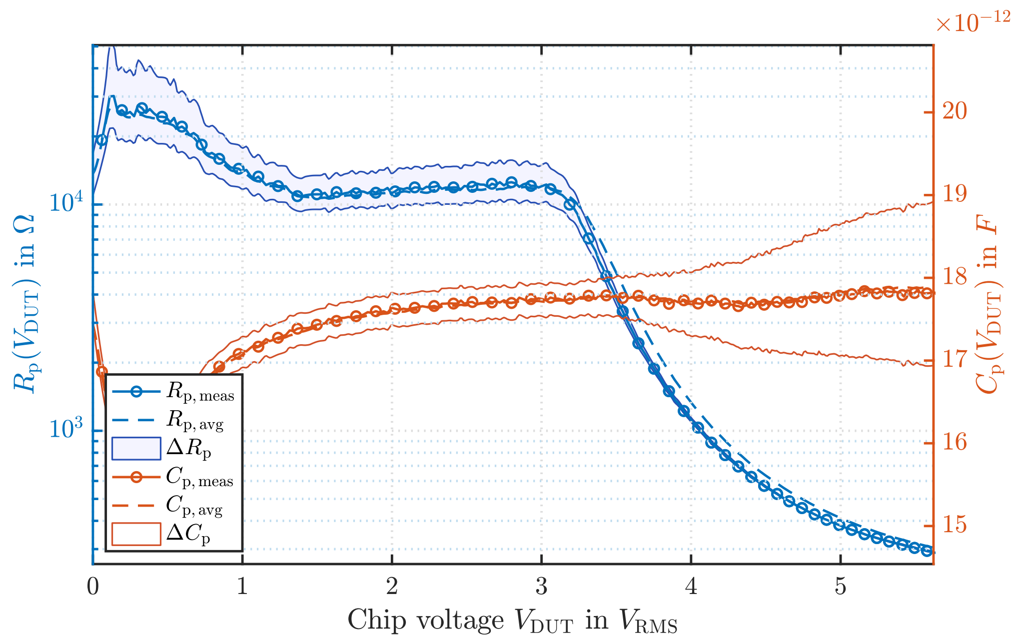

Figure 4.13: Input impedance measurement.

FM388

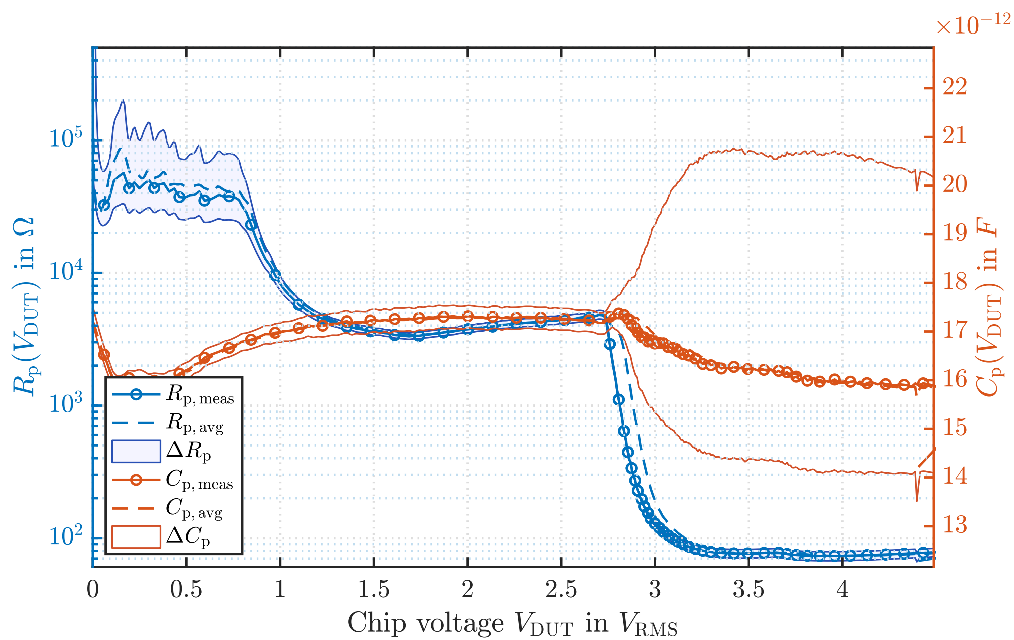

Figure 4.14: Input impedance measurement.

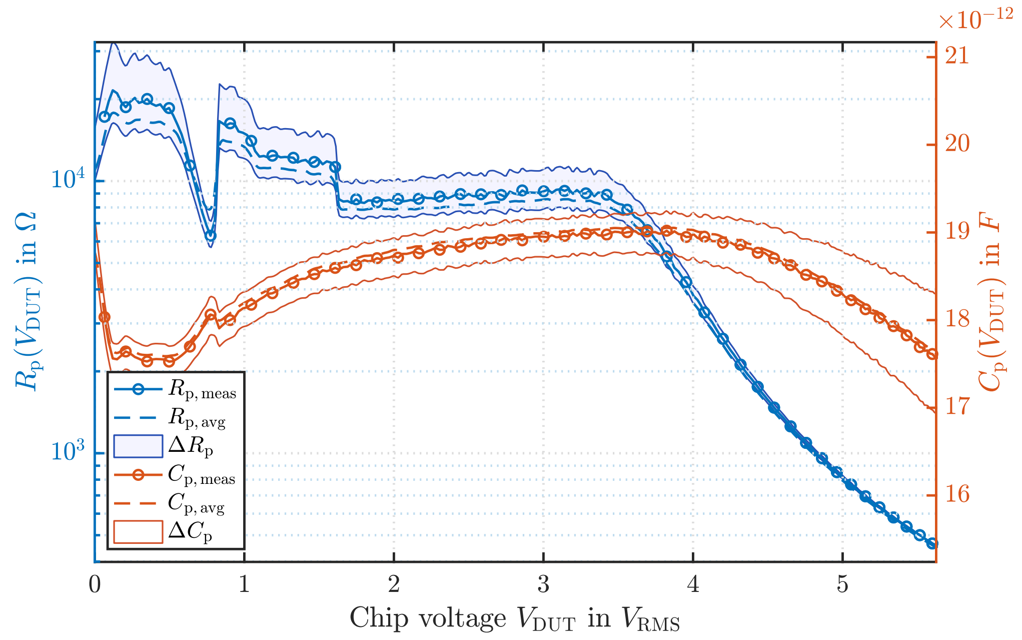

Figure 4.15: Input impedance measurement.

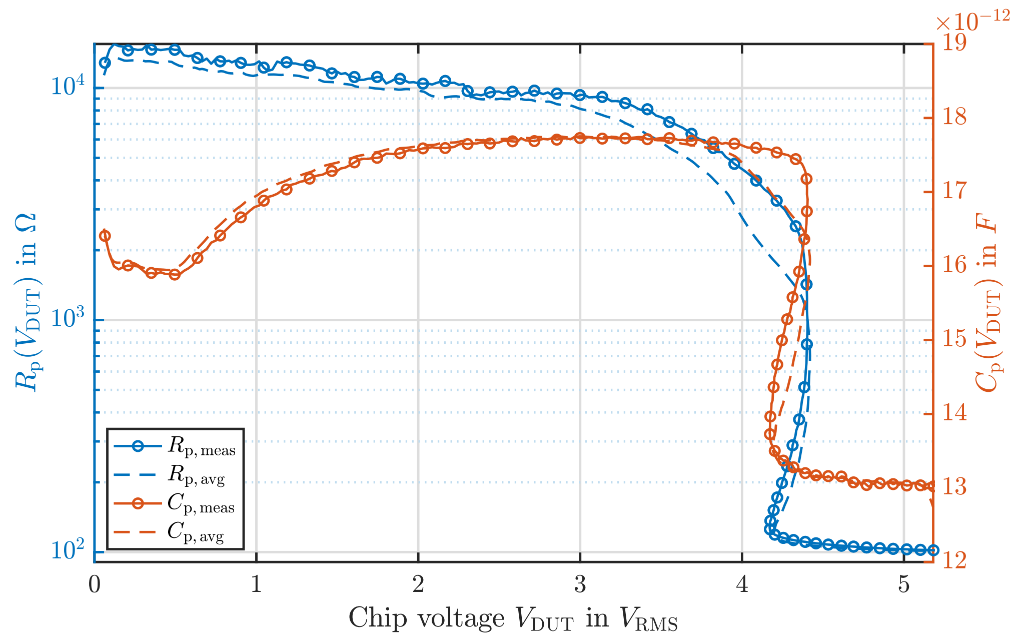

Figure 4.16: Input impedance measurement.

GT5652

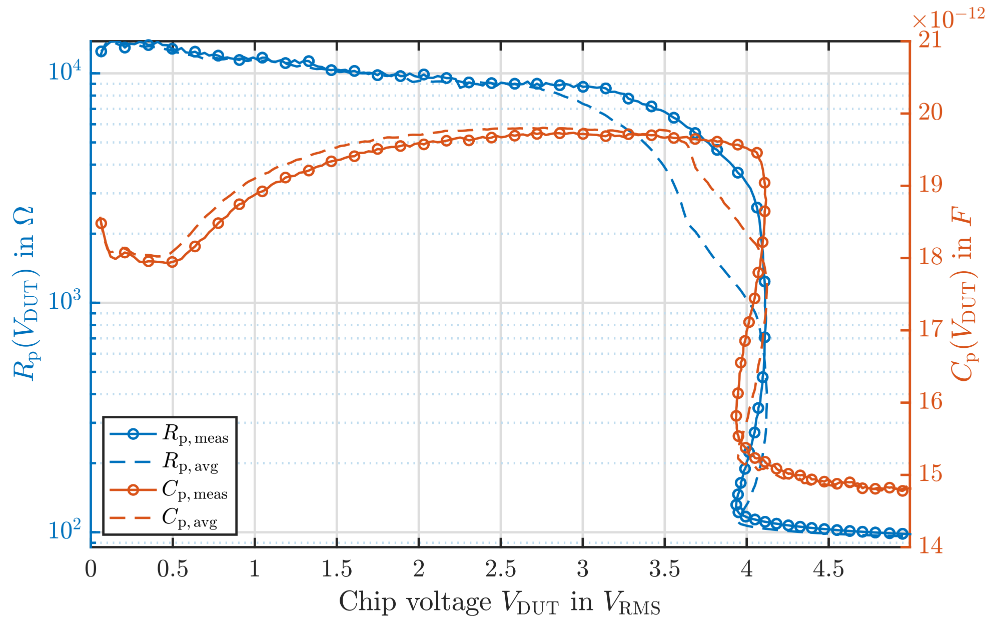

Figure 4.17: Input impedance measurement.

GT5670

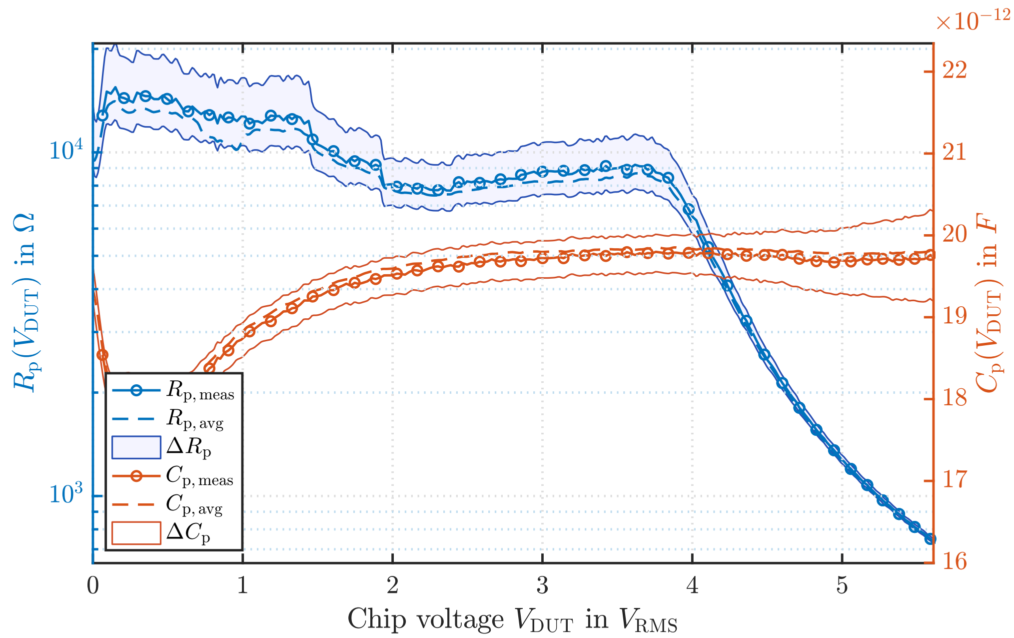

Figure 4.18: Input impedance measurement.

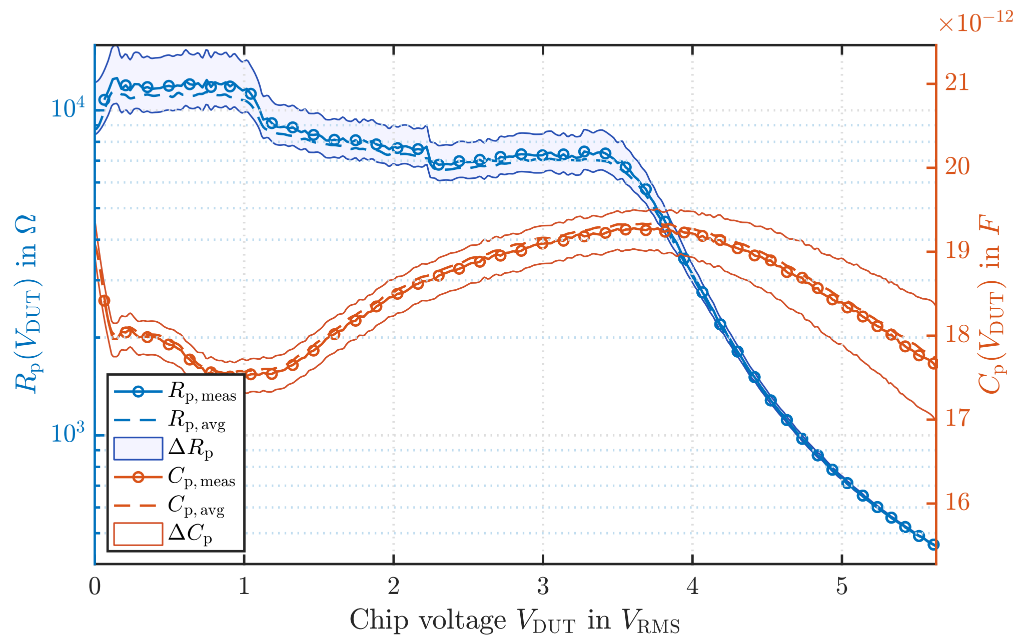

Figure 4.19: Input impedance measurement.

Some curve shapes in Figures 4.3 through 4.19 exhibit characteristic points that can be interpreted if the chip architecture is known. Gebart et al. [27] have characterized a chip from the company NXP Semiconductors that shows a very similar characteristic as the chip **DesFire** (compare Figure 4.5) that is also manufactured by the same company. This suggests that both chips are similar, thus the characteristic points in the measured curves might correspond to the same events of the chip operation. In Figure 4.20 these points are marked: At a low voltage of around 1.2 V, there is a dip in the parallel resistance R_p that was identified as *power-on reset* by Gebart et al. At a higher voltage of around 2.9 V, a spike can be seen in the parallel resistance R_p after which Gebart et al. identified the *start of chip operation*.

DesFire

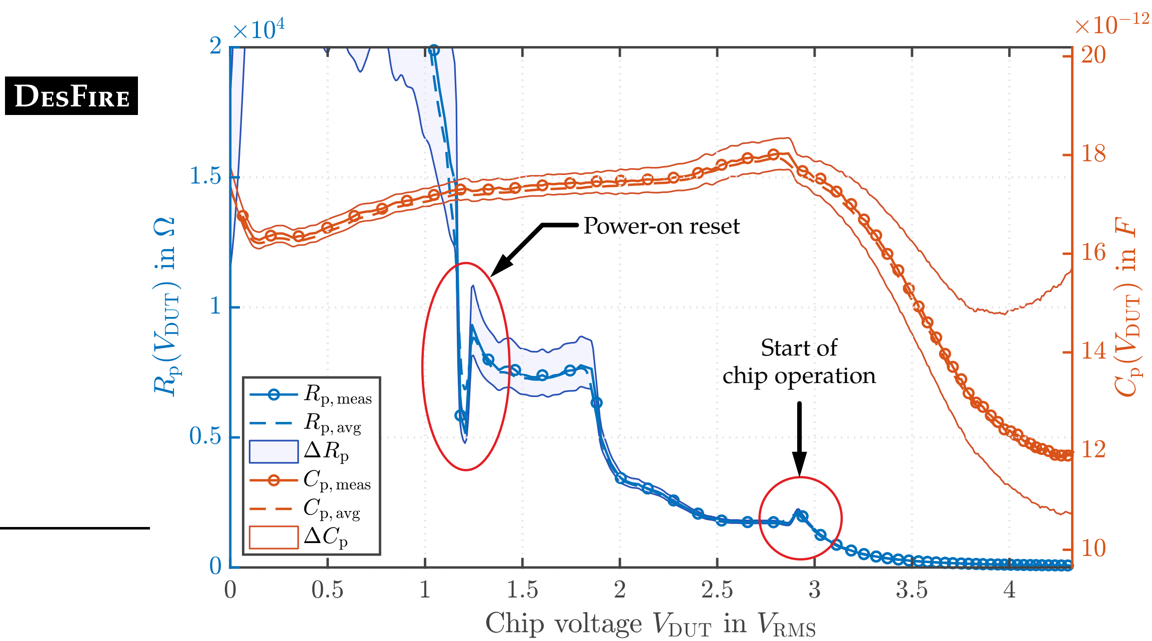

Figure 4.20: Input impedance measurement of chip **DesFire**. Characteristic points have been marked as presented by Gebart et al. [27].

4.3.1 System Analysis: Impact on the Transponder Performance

A nonlinear chip impedance $Z_{\mathrm{DUT}}(V_{\mathrm{DUT}})$ has several impacts on the total reader - transponder system. The design of HF RFID systems is always limited by a trade-off between the *energy range* of the system and its *data transmission speed* [1]. In general, for achieving a high read range, a high quality factor Q_{T} of the transponder is desirable. Unfortunately, the bandwidth B of the transponder is inversely proportional to its quality factor (see Equation 1.4).
From a wireless power transfer perspective, a precise matching of the transponder coil impedance to the chip input impedance is desirable at the interrogation field strength H_{min}. Once the magnetic field exceeded H_{min}, the power supply of the transponder is usually not severely impaired by changes of the chip impedance, since those are a result of the intentional, internal shunt regulation [56]. The communication with the reader on the other hand still suffers from the nonlinear chip impedance that changes with an increasing supplied power. Rizkalla et al. [36] identified that a decreasing resistance $R_{\mathrm{p}}(V_{\mathrm{DUT}})$ impacts the LM communication of the transponder with the reader. For higher voltages V_{DUT}, the resistance R_{p} takes similar values in the loaded and unloaded states, such that LM is no longer possible.
Additionally, the resonance frequency f_{res} is shifted with changing Z_{DUT} and the quality factor Q_{T} of the transponder changes as well (see Equations 1.1 and 1.3). This impairs the LM communication with the reader because a detuning of f_{res} will cause the upper and lower Side Band Amplitudes (SBA) to be transmitted at different levels [1].

Many works that deal with the performance optimization of transponders aim to maximize the power transfer to the chip or minimize H_{min}, respectively, based on system parameters like f_{res} and Q_{T} [57], [58]. For the purpose of maximizing the power transfer, they propose methods for optimal transponder coil designs. Rizkalla et al. [59] state that variations of f_{res} and Q_{T} are merely a result of the nonlinear input impedance of the transponder chip Z_{DUT}. They propose an optimization algorithm that aims to find an optimum transponder coil inductance L_2 which shall make the transponder work with all *basic bit rates* (106 - 848 kbit/s) over a wide range of transferred power. For that purpose, they take the entire reader - transponder system into account.

In this work, rather than designing an optimal transponder coil for the measured chips, it is analyzed, how the chips would perform in a standard Proximity Integrated Circuit Card (PICC) with parameters as proposed by Gebhart and Szoncso [56] (see Table 4.3). The three chips **DesFire**, **Classic** and **Ultral** are chosen, because they are designed to work in a class 1 transponder coil.

Parameter	Meaning	Unit	Value
N_{turns}	transponder coil turns	-	6
A	coil cross-section area	m^2	0.049×0.079
L_2	coil inductance	µH	4.75
C_{par}	parasitic capacitance	pF	3.93
R_2	coil resistance	Ω	2.55

Table 4.3: Class 1 transponder coil parameters measured by Gebhart and Szoncso [56]. The parameters can be used in an equivalent circuit model (compare Figure 1.2).

Chip Voltage:
The correspondence between chip voltage V_{DUT} and magnetic field H can be computed using Equation 1.2. Figure 4.21 shows the measured chip voltage V_{DUT} as a function of the computed magnetic field for the three chips. The shape of all three curves shows the typical characteristic of a voltage limiter: the voltage V_{DUT} rises almost linearly with the magnetic field, until a certain limit is reached after which the voltage stays almost constant with respect to the magnetic field. It is worth mentioning that the voltage V_{DUT} is present at the chip terminals. The actual internal core voltage of the chip depends on the architecture of the RF frontend. The voltage limiting, nonlinear characteristic of Z_{DUT} is intended for the protection of the internal chip circuitry as well as for operating the charge pump in an optimal operating point [13], i.e., where it is working with optimum efficiency. Furthermore, depending on the semiconductor process used to manufacture the chips, the internal core voltages of the individual DUTs may vary. These reasons explain the differences of the curves depicted in Figure 4.21 which may be intended by the chip design.

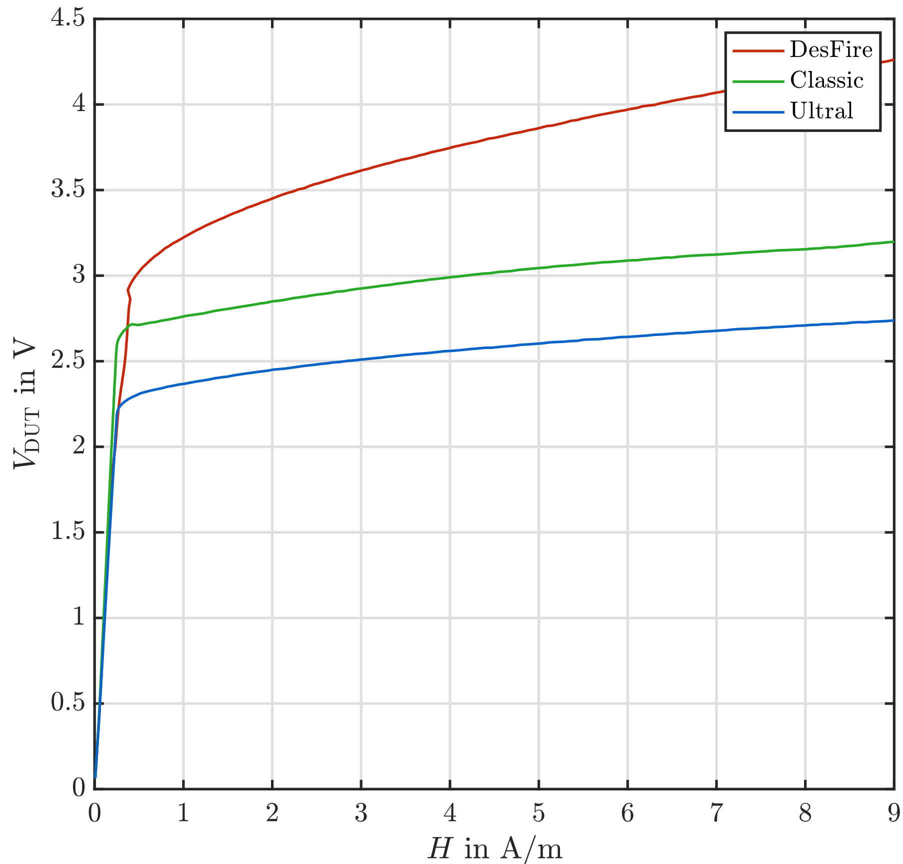

Figure 4.21: Chip voltage V_{DUT} versus computed magnetic field H.

Transponder Resonance Frequency:
The transponder resonance frequency is inversely proportional to the square-root of the coil inductance L_2 times the capacitance $C_2 = C_{\mathrm{p}} + C_{\mathrm{par}}$ according to Equation 1.1. In the particular case of the three chips used in this analysis, the capacitance C_{p} is increasing with a rising chip voltage V_{DUT} or magnetic field H, respectively. Consequently, the computed resonance frequencies f_{res} of these chips are increasing with the magnetic field H. It should be noted that this behavior is typical for these particular chips, since, from Figures 4.3 to 4.19, it can be observed that C_{p} is not generally decreasing with the voltage V_{DUT}.

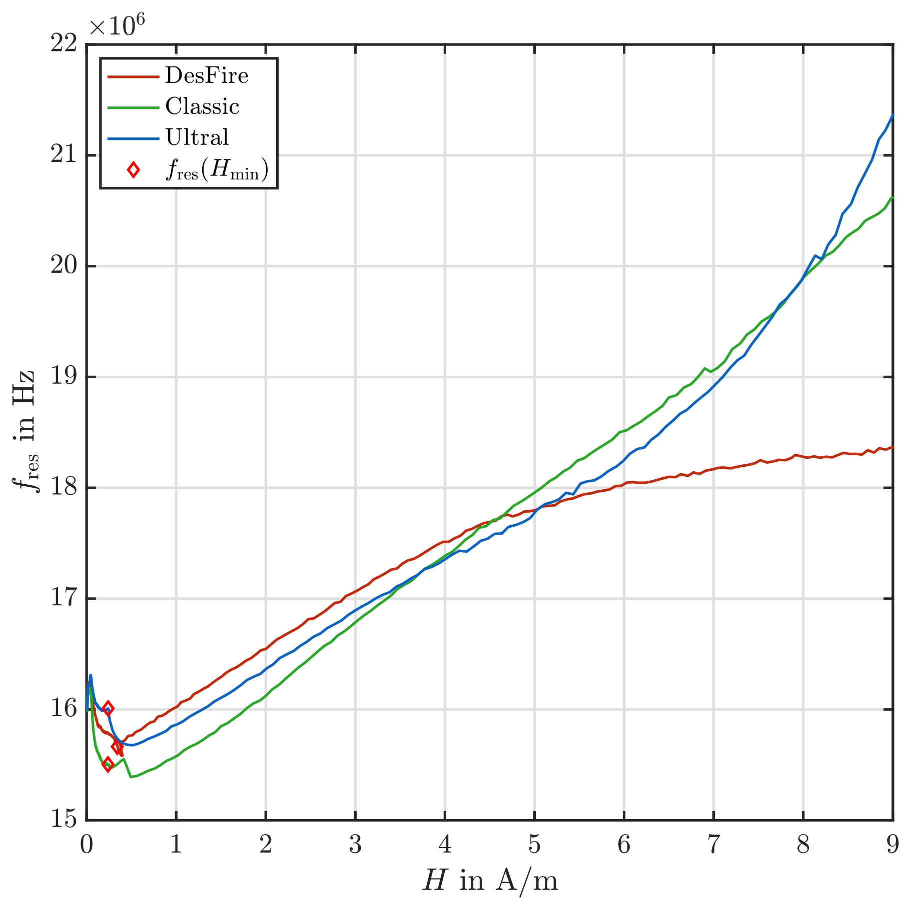

Figure 4.22: Computed transponder resonance frequency f_{res} versus computed magnetic field H.

Transponder Quality Factor:
Figure 4.23 shows the computed quality factor Q_T as a function of the magnetic field H. Looking at the curve of the chip **DesFire** (see Figure 4.22), it can be seen that the resonance frequency $f_\mathrm{res}(H_\mathrm{min})$ is located at $15.6\,\mathrm{MHz}$ which is just within the recommended upper limit of $16\,\mathrm{MHz}$ defined for that chip, but the quality factor $Q_T(H_\mathrm{min})$ (see Figure 4.23) is below the lower bound of 30 as recommended in the card coil design guide for this chip [15]. Consequently, through analysis of the contact based chip impedance measurements, it is possible to say that the chosen chip card will not meet the design recommendations with that chip. Chips **Classic** and **Ultral** on the other hand will exhibit reasonably high quality factors $Q_T(H_\mathrm{min})$ within this chip card and therefore constitute a valid transponder design.

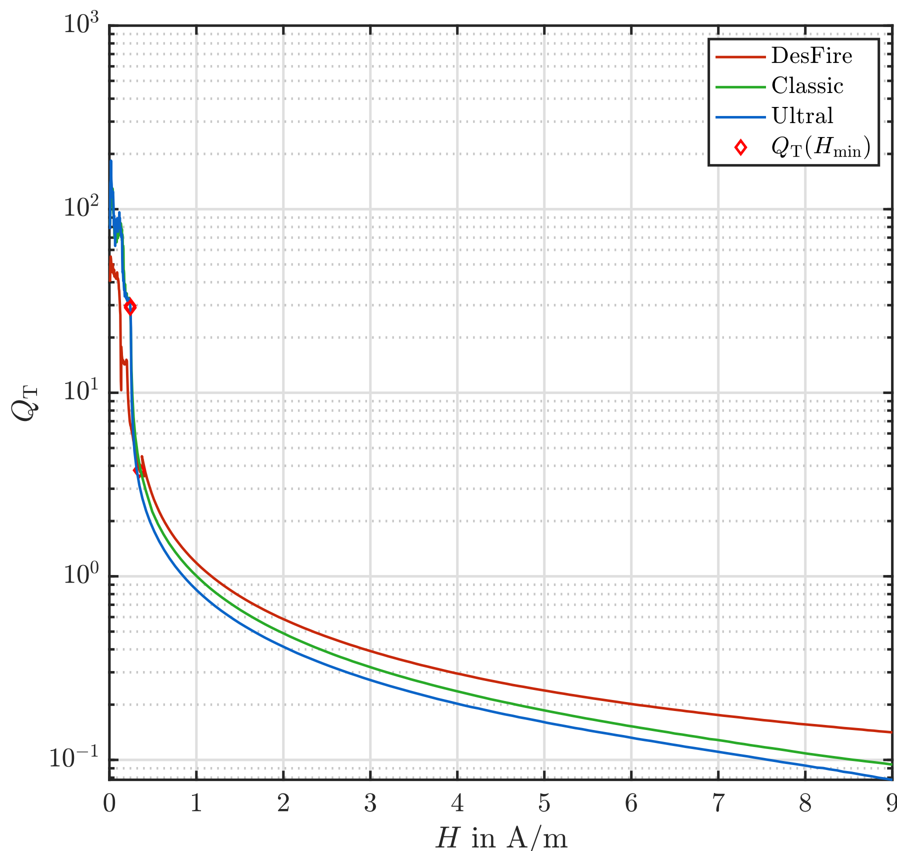

Figure 4.23: Computed transponder quality factor Q_T versus computed magnetic field H.

CHAPTER 5

Conclusions

In this thesis, a measurement system is presented, that is based on the RF I-V method of impedance measurement. The implemented system exhibits a higher measurement accuracy than related works in the field of HF RFID chip impedance measurements. A novel calibration method has been developed, analyzed and compared with well-known calibration methods for VNAs. Using a set of chosen calibration standards, the fixture comprising the chip can be calibrated for linear systematic errors and corresponding measurements can be de-embedded. Moreover, an attempt is made to estimate the measurement uncertainty using an additional set of reference standards. This makes the reported measurement results more complete and raises awareness about a fact, that is commonly ignored: a possible high uncertainty in the determination of one component, R_p or C_p, when the respective other component is dominant. Following the presentation of the measurement results, a subsequent analysis from a system perspective shows, how accurate knowledge of the input impedance of a chip can aid in the transponder design.

Current developments on the smart card market and possible use cases in the IoT hold good prospects for the future of HF RFID systems. Complete system analyses based on contact-based measurements of HF RFID chips will aid system engineers to accurately design transponders, which may contribute to their successful deployment in widescale IoT scenarios. Measurement results reported along with an uncertainty estimation will support verification engineers to assess whether chips meet tight specifications. Today, the use cases for HF RFID systems even exceed the mere purpose of communication. There are non-communication use cases like RFID sensor tags, where a certain sensing quantity shall be estimated as a function of system parameters. Accurate input impedance measurements of chips will enable these technologies to reach unprecedented estimates of the sensing quantity.

The concept of the measurement system was designed to enable LM measurements of chip impedance. In the future, these measurements can be implemented through a software update. Further improvements of the measurement accuracy could be achieved by using a differential active voltage probe and by using smaller ground planes on the PCB. Both actions would decrease a parasitic coupling with ground. The measurement sensitivity may be increased by designing a matching circuit to compensate the reactive parasitic impedance contribution of the interconnection network, i.e., cables, PCBs, connectors etc.

Acronyms

AWG Arbitrary Waveform Generator. 26, 85

CAL calibration. 30

CH1 Channel One. 85

CH2 Channel Two. 86

CoM Coil on Module. 19

COVID-19 Coronavirus Disease 2019. 9

DIN Deutsches Institut für Normung. 16

DUT Device Under Test. 10, 83

EM electromagnetic. 12

FFT Fast Fourier Transform. 20

GUM Guide to the Expression of Uncertainty in Measurement. 49

HF High Frequency. 9

IC Integrated Circuit. 12

IEC International Electrotechnical Commission. 10

IoT Internet of Things. 9

ISO International Organization for Standardization. 10

LM Load Modulation. 11

OSM Open Short Match. 38

PC Personal Computer. 26

PCB Printed Circuit Board. 23, 87

PICC Proximity Integrated Circuit Card. 63

PIN Positive Intrinsic Negative diode. 30, 85

PRI Primary Coil. 27

RF Radio Frequency. 15, 83

RFID Radio Frequency Identification. 9

S-parameters Scattering parameters. 34

SARS-CoV-2 Severe Acute Respiratory Syndrome Coronavirus 2. 9

SBA Side Band Amplitudes. 63

SEC Secondary Coil. 27

SFG Signal Flow Graph. 83

SMD Surface-Mount Device. 30

SMP Sub-Miniature Push-on. 30

SMT Surface-Mount Technology. 29

SOL Short Open Load. 38

Sync Synchronization. 26

TPN Two-Port Network Building Block. 83

USB Universal Serial Bus. 27

VNA Vector Network Analyzer. 84

ZMS Impedance Measurement System. 83

Symbols

a	an error term out of the set E.
A	coil cross-section area.
b	an error term out of the set E.
$\overline{b}$	mean correction.
B	transponder bandwidth.
c	an error term out of the set E.
C	arbitrary capacitance.
C_2	total transponder capacitance.
C_{ch}	communication channel capacity.
C_{p}	chip parallel capacitance.
$C_{\mathrm{p,\,avg}}$	averaged parallel capacitance.
C_{par}	parasitic capacitance.
δ_Z	relative error of an impedance measurement.
ΔR_{p}	uncertainty range for R_{p}.
ΔC_{p}	uncertainty range for C_{p}.
E	set of error terms.
ε_r	relative permittivity.
f	frequency.
f_{c}	carrier frequency.
f_{res}	transponder resonance frequency.
G	measurement proportional to an impedance.
Γ	reflection coefficient.
H	magnetic field.
$H_{i,j}$	hybrid parameters.
H_{min}	interrogation field strength.
I_{DUT}	chip current.
k	coverage factor.
L_2	transponder coil inductance.
λ	wave length.
μ_0	vacuum permeability.
μ_Z	mean value of impedance measurements.
M_{ref}	number of reference standards.

N	number of calibration standards.
N_{turns}	number of coil turns.
N_{m}	number of measurements.
Q_{T}	transponder quality factor.
R	arbitrary resistance.
R_2	transponder coil resistance.
R_{p}	chip parallel resistance.
$R_{\mathrm{p,\,avg}}$	averaged parallel resistance.
s_b^2	unbiased sample variance.
$S_{i,j}$	scattering parameters.
$\frac{S}{N}$	signal-to-noise ratio.
U	expanded uncertainty.
u_c	standard uncertainty.
V^+	incident voltage wave.
V^-	reflected voltage wave.
V_{AWG}	AWG supply voltage.
V_{DD}	IC core voltage.
V_{DUT}	chip voltage.
V_{F}	diode forward voltage.
V_{I}	voltage measured in the current path.
ω	angular frequency.
Y_{DUT}	chip admittance.
z	arbitrary complex number.
Z	arbitrary impedance.
Z_0	short circuit impedance point.
Z_∞	open circuit impedance point.
Z_{cal}	impedance of a calibration standard.
Z_{coil}	transponder coil impedance.
Z_{DUT}	chip impedance.
Z_{probe}	input impedance of the voltage probe.
Z_{ref}	impedance of a reference standard.
Z_{W}	characteristic impedance.

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R&S	registered trademark of Rohde & Schwarz GmbH & Co KG
Teledyne	registered trademark of Teledyne Technologies Inc.
Keysight	registered trademark of Keysight Technologies Inc.
NXP	registered trademark of NXP Semiconductors N.V.
NTAG	registered trademark of NXP Semiconductors N.V.
ICODE	registered trademark of NXP Semiconductors N.V.
DESFire	registered trademark of NXP Semiconductors N.V.
Ultralight	registered trademark of NXP Semiconductors N.V.

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APPENDIX A

Calibration Strategy for an RF I-V Impedance Measurement System

This project work introduces a calibration procedure for an impedance measurement system. In the following, the measurement system will be referred to as ZMS, an abbreviation chosen for Impedance Measurement System. The ZMS is based on the RF I-V method of impedance measurements [23]. The ZMS consists of a *measurement board* with connections for power supply and measurement of voltage and current signals of the connected Device Under Test (DUT). The individual DUTs as well as calibration standards can be connected via *DUT boards*. The main purpose of the measurement board is the interconnection of the individual supply and measurement devices with the DUT as well as impedance matching for optimum power transfer to the DUT. Non-idealities and parasitics of the used components and supply- and signal lines cause the necessity for calibration. The system is assumed to behave *linear* in its intended operation range, but frequency dependent in operation. If impedance measurements shall be conducted over a range of frequencies, a frequency dependent calibration has to be carried out.

A.1 Methodology

The schematic of the ZMS is modeled using *two-port network building blocks* (TPN). Employing a Signal Flow Graph (SFG) on a condensed network of TPNs, the transfer function from voltage- and current signals can be found as a function of the DUT impedance Z_{DUT}. This transfer function leaves us with a set of unknown *error terms* that can be determined using well characterized calibration standards. In Chapter A.3, the TPNs of which the ZMS consists of will be

separated and combined in a convenient way that leaves us with a small number of error terms, thus a reliable calibration can be conducted with few calibration standards.
The calibration strategy is similar to calibrations that are used for *vector network analyzers* (VNA), which are well studied and acknowledged in the field of RF measurements.

A.2 Measurement System Overview

Figure A.1: Schematic of the ZMS.

Supply path:
The design of the ZMS is based on the schematic depicted in Figure A.1. Two *arbitrary waveform generators* (AWG) supply the circuit to achieve a desirable power range at the DUT (e.g. an HF RFID chip). To transfer maximum power to the DUT, the supply has to be impedance matched to the rest of the circuit. The measurement board was designed to match the AWGs to a minimum expected DUT impedance of $\underline{Z}_{DUT,min} \approx 50\,\Omega$. The impedance matching between the supply (i.e., the AWGs) and the load (i.e., the DUT) is performed by the transformers next to the AWGs.

Current path:
To measure the impedance of the DUT, voltages and currents through the DUT are measured using a *sampler*. The current path is closer to the DUT and leverages two transformers that act as serial shunts in the supply path of the DUT. They transform the $50\,\Omega$ input impedance $\underline{Z}_{in}$ of Channel One (CH1) of the sampler down to two low shunt impedances of $\underline{Z}_s = \frac{1}{2}\frac{1}{16}\underline{Z}_{in} \approx 1.56\,\Omega$. At the same time, they match the expected signal range (i.e., voltage drop over the transformers) to the input voltage range of the sampler.
Note: PIN diodes with a low parasitic capacitance have been used to protect the sampler inputs CH1 and CH2 against excessive voltages. They are placed in parallel to the $50\,\Omega$ inputs and have a comparably high impedance in their

non-conducting state.

Voltage path:
The voltage path is connected in parallel to the supply lines of the DUT and uses another two transformers to perform matching of the voltage signal with the input voltage range at Channel Two (CH2). Furthermore, it transforms the input impedance of CH2 to a high parallel impedance of $\underline{Z}_p = 9^2\,\underline{Z}_{in} \approx 4\,\mathrm{k\Omega}$ between the supply lines of the DUT.

A.3 Calibration Strategy

Nonidealities of the used components like transformers and parasitics of connectors, PCB traces, etc. require the implementation of a calibration procedure to compensate for the measurement errors that are introduced inevitably.
In this work, we will split up the given electrical network into as few as possible TPNs and set up an SFG from the current signal $\underline{V}_I$ (starting node; CH1) to the voltage signal $\underline{V}_V$ (end node; CH2). This gives us a transfer function $\underline{G}$ that depends on the error terms and the impedance of the DUT $\underline{Z}_{DUT}$:

$$\underline{G} := \frac{\underline{V}_V}{\underline{V}_I} = f\left(\underline{E}, \underline{Z}_{DUT}\right), \tag{A.1}$$

where $\underline{G}$ is the measured quantity proportional to the impedance of the DUT and $\underline{E}$ denotes the set of error terms. Combining error terms in a convenient way, it is possible to reduce the number of unknowns and find a linear dependence of the error terms on $\underline{G}$ and $\underline{Z}_{DUT}$. Using a set of known calibration standards with a well defined impedance (i.e. $\underline{Z}_{DUT}$), it is possible to solve for the error terms and thereby achieving a calibrated system that compensates for systematic errors.

Note that this procedure assumes a linear network, where the diodes are assumed to have a negligible impact in the intended operating region of the ZMS.

A.3.1 Electrical Network Representation

In order to find the desired SFG that leads to the transfer function $\underline{G}$, the circuit shall be analyzed and represented by TPNs. The schematic of the ZMS depicted in Figure A.1 can be represented as a cascade connection of TPNs. Disregarding the supply, we can redraw the schematic to yield a network as shown in Figure A.3a.

A.3.1.1 TPN Network

We can separate the electrical network in Figure A.3a in a cascade connection of the voltage path and the current path (see dash-dotted lines). Then we can represent each of those parts by a TPN, since they fulfil the port conditions [60]

$$\underline{I}_1 = \underline{I}'_1 \qquad \text{and} \qquad \underline{I}_2 = \underline{I}'_2 \,. \tag{A.2}$$

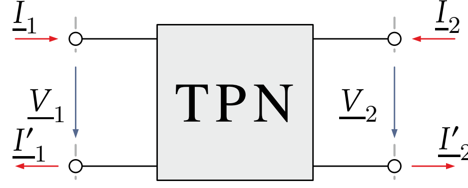


Figure A.2: General four-terminal network.

Now, we are left with a cascade connection of two TPNs as depicted in Figure A.3b. $\underline{\mathbf{H}}_V$ and $\underline{\mathbf{H}}_I$ are TPNs that represent the voltage and current paths through *hybrid parameters*.

Hybrid parameters are defined as

$$\begin{bmatrix} \underline{V}_1 \\ \underline{I}_2 \end{bmatrix} = \begin{bmatrix} \underline{H}_{11} & \underline{H}_{12} \\ \underline{H}_{21} & \underline{H}_{22} \end{bmatrix} \begin{bmatrix} \underline{I}_1 \\ \underline{V}_2 \end{bmatrix} , \tag{A.3}$$

thus they represent the voltage at port one $\underline{V}_1$ and the current at port two $\underline{I}_2$ as a linear combination of the current at port one $\underline{I}_1$ and the voltage at port two $\underline{V}_2$. The network representation in hybrid parameters has been chosen because it allows to set up a convenient SFG (see Section A.3.2.1) for the transfer function $\underline{G}$ given in Equation A.1.

Note that the TPNs may not only represent the ideal schematic of the ZMS but also include the effects of various linear parasitics. The behavior of the real network with its errors can be lumped into *fictitious error adapters* [61].

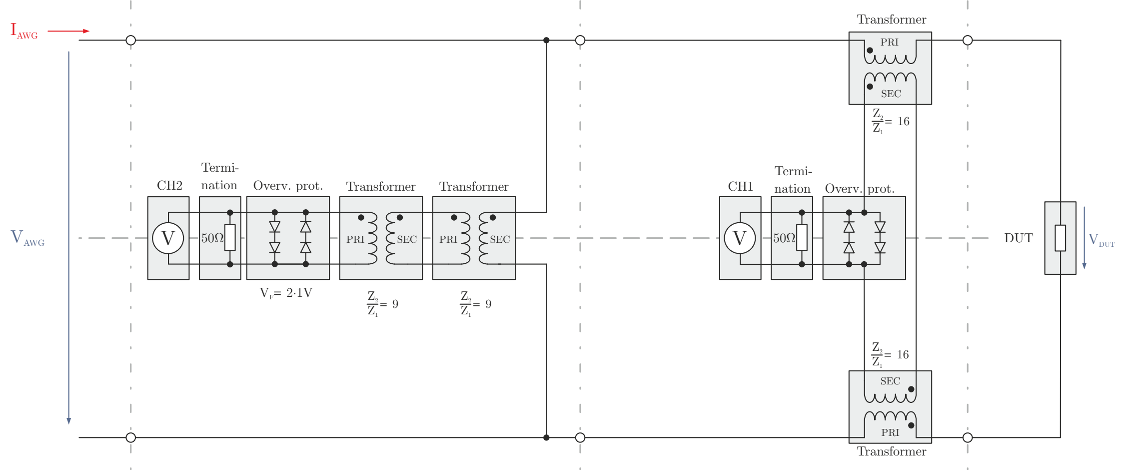
A.3.1.2 Port Decomposition

The transfer function for $\underline{G}$ describes a path of the SFG that starts at a node $\underline{V}_I$ and ends in a node $\underline{V}_V$ which are the measured quantities of the sampler. These have to be available at the interfaces between two TPNs to set up the corresponding SFG. Since a TPN can be represented by any desirable type of network parameters, we choose to work with transmission parameters $\underline{\mathbf{A}}$ instead of hybrid parameters $\underline{\mathbf{H}}$ in the following steps. This is advantageous for the given cascaded topology. We wish to *decompose*

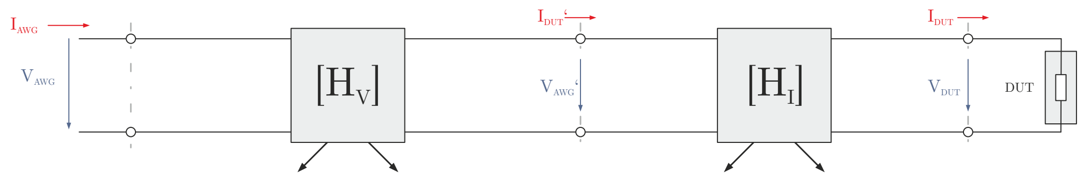
$$\underline{\mathbf{A}}_V := \underline{\mathbf{A}}_{V1}\,\underline{\mathbf{A}}_{V2} \tag{A.4}$$

and

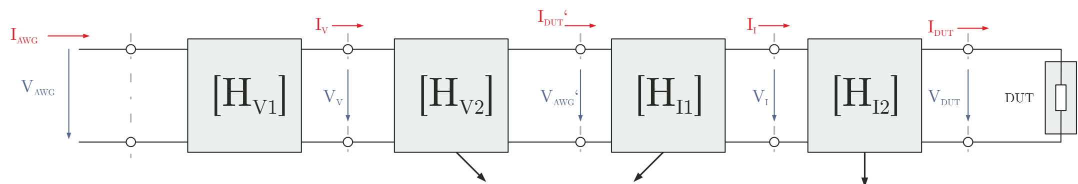
$$\underline{\mathbf{A}}_I := \underline{\mathbf{A}}_{I1}\,\underline{\mathbf{A}}_{I2} , \tag{A.5}$$



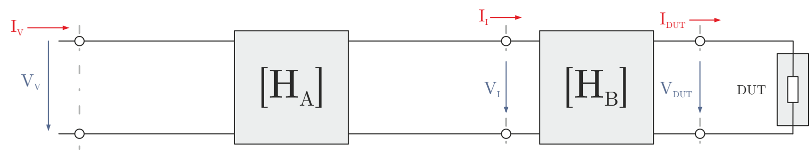
(a) Redrawn network of the ZMS without supply.



(b) Representation of the cascade through TPNs.



(c) Decomposed voltage and current TPNs.



(d) Cascaded combination revealing $\underline{V}_I$ and $\underline{V}_V$.

Figure A.3: Representation of the electrical network of the ZMS through a small number of TPNs while revealing $\underline{V}_I$ and $\underline{V}_V$.

such that the interfaces of their decomposed matrices reveal the desired quantities $\underline{V}_V$ and $\underline{V}_I$ as depicted in Figure A.3c.

A.3.1.2.1 Existence of the Decomposition

The error terms, i.e. the unknown elements of the TPNs, shall be found through calibration and therefore there is no need to compute them analytically. Yet it is necessary to show that a matrix decomposition exists as proposed in Equations A.4 and A.5.

Transmission parameters are defined as

$$\begin{bmatrix} \underline{V}_1 \\ \underline{I}_1 \end{bmatrix} = \begin{bmatrix} \underline{A}_{11} & \underline{A}_{12} \\ \underline{A}_{21} & \underline{A}_{22} \end{bmatrix} \begin{bmatrix} \underline{V}_2 \\ -\underline{I}_2 \end{bmatrix} . \tag{A.6}$$

Voltage Path:
The voltage path of the ZMS as depicted on the left side of Figure A.3a is modeled by

$$\begin{aligned} \underline{A}_{V\,11} &= \left.\frac{\underline{V}_1}{\underline{V}_2}\right|_{\underline{I}_2=0} = 1 \\ \underline{A}_{V\,12} &= \left.\frac{\underline{V}_1}{-\underline{I}_2}\right|_{\underline{V}_2=0} = 0 \\ \underline{A}_{V\,21} &= \left.\frac{\underline{I}_1}{\underline{V}_2}\right|_{\underline{I}_2=0} = \frac{1}{n^4\,\underline{Z}_{in}} \\ \underline{A}_{V\,22} &= \left.\frac{\underline{I}_1}{-\underline{I}_2}\right|_{\underline{V}_2=0} = 1 \end{aligned} \qquad \underline{\mathbf{A}}_V = \begin{bmatrix} 1 & 0 \\ \frac{1}{n^4\,\underline{Z}_{in}} & 1 \end{bmatrix} , \tag{A.7}$$

where $n = 3$ is the turns ratio of one of the transformers within the voltage path. Note that the matrix effectively models a shunt impedance.

The voltage path can be decomposed into two TPNs:

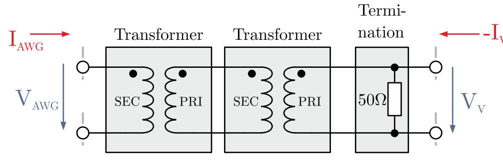


Figure A.4: Topology of $\underline{\mathbf{A}}_{V1}$.

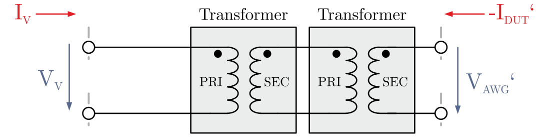


Figure A.5: Topology of $\underline{\mathbf{A}}_{V2}$.

$$\underline{\mathbf{A}}_{V1} = \begin{bmatrix} n^2 & 0 \\ \frac{1}{n^2 \underline{Z}_{in}} & \frac{1}{n^2} \end{bmatrix} \tag{A.8}$$

$$\underline{\mathbf{A}}_{V2} = \begin{bmatrix} \frac{1}{n^2} & 0 \\ 0 & n^2 \end{bmatrix} \tag{A.9}$$

The multiplication of the matrices $\underline{\mathbf{A}}_{V1}$ and $\underline{\mathbf{A}}_{V2}$ results in $\underline{\mathbf{A}}_{V}$ and therefore fulfills the decomposition proposed in Equation A.4.

We further demand that the voltage $\underline{V}_V$ measured by the sampler is available at the interface between the two decomposed TPNs and it shall satisfy the following relation:

$$\underline{V}_{AWG} = n^2\, \underline{V}_V\,, \tag{A.10}$$

where $\underline{V}_{AWG}$ is the supplied voltage at the input of the TPN. We have to show that our choice of $\underline{\mathbf{A}}_{V1}$ satisfies this equation.

If we look at the first of the two linear equations of transmission parameters, i.e. the first row of Equation A.6, we have

$$\underbrace{\underline{V}_1}_{\underline{V}_{AWG}} = \underline{A}_{11}\, \underbrace{\underline{V}_2}_{\underline{V}_V} - \underline{A}_{12}\, \underbrace{\underline{I}_2}_{-\underline{I}_V}\ . \tag{A.11}$$

Equating the coefficients, we see that

$$\underline{A}_{11} = n^2 \qquad \text{and} \qquad \underline{A}_{12} = 0\,, \tag{A.12}$$

thus $\underline{V}_V$ only depends on the supplied voltage $\underline{V}_{AWG}$ that we are interested in and is *decoupled* from the current $\underline{I}_2$ flowing into its second port.

Concluding, the TPN described by $\underline{\mathbf{A}}_{V1}$ models $\underline{V}_V$ as desired and the cascade $\underline{\mathbf{A}}_{V1}\,\underline{\mathbf{A}}_{V2}$ models the behavior of $\underline{\mathbf{A}}_V$, thus the decomposition does not impact the rest of the network.

Current Path:
The current path of the ZMS as depicted on the right side of Figure A.3a is

modeled by

$$\underline{\mathbf{A}}_I = \begin{bmatrix} 1 & \frac{\underline{Z}_{in}}{n^2} \\ 0 & 1 \end{bmatrix}, \quad \text{(A.13)}$$

where $n = 4$ in the current path. Note that the matrix effectively models a series impedance.

For the current path, we have a measured voltage $\underline{V}_I$ that shall only be dependent on the current $\underline{I}_{DUT}$ flowing through the DUT:

$$\underline{V}_I \overset{!}{=} \frac{\underline{Z}_{in}}{n} \underline{I}_{DUT} . \quad \text{(A.14)}$$

If we look at the second of the two linear equations of transmission parameters, i.e. the second row of Equation A.6, we have

$$\underbrace{\underline{I}_1}_{\underline{I}_{DUT}} = \underline{A}_{21} \underbrace{\underline{V}_2}_{\underline{V}_I} - \underline{A}_{22} \underbrace{\underline{I}_2}_{-\underline{I}_I} . \quad \text{(A.15)}$$

Equating the coefficients, we see that

$$\underline{A}_{21} = \frac{n}{\underline{Z}_{in}} \quad \text{and} \quad \underline{A}_{22} = 0 , \quad \text{(A.16)}$$

thus $\underline{V}_I$ only depends on the current $\underline{I}_{DUT}$ that we are interested in and is *decoupled* from the current $\underline{I}_2$ flowing into its second port.

Now, we still have to define the first of the two linear equations in Equation A.6:

$$\underbrace{\underline{V}_1}_{\underline{V}_{AWG}} = \underline{A}_{11} \underbrace{\underline{V}_2}_{\underline{V}_I} + \underline{A}_{12} \underbrace{\underline{I}_2}_{-\underline{I}_I} . \quad \text{(A.17)}$$

We choose $\underline{A}_{11} \overset{!}{=} 0$ to decouple the supplied voltage $\underline{V}_{AWG}$ from the measured voltage $\underline{V}_I$. The parameter $\underline{A}_{12}$ can be chosen independently but has to be unequal to 0 in order to guarantee that $\underline{\mathbf{A}}_{I1}$ is *nonsingular*, i.e. *invertible*. This is necessary to compute a valid decomposition. We define an arbitrary impedance $\underline{Z}_x = \underline{A}_{12} \neq 0\,\Omega$. Now we are left with

$$\underline{\mathbf{A}}_{I1} = \begin{bmatrix} 0 & \underline{Z}_x \\ \frac{n}{\underline{Z}_{in}} & 0 \end{bmatrix} . \quad \text{(A.18)}$$

Having a nonsingular matrix $\underline{\mathbf{A}}_{I1}$, we can compute its inverse $\underline{\mathbf{A}}_{I1}^{-1}$ and therefore the second two-port of the cascade $\underline{\mathbf{A}}_{I2}$ according to Equation A.5:

$$\begin{aligned}\underline{\mathbf{A}}_{I2} &= \underline{\mathbf{A}}_{I1}^{-1}\,\underline{\mathbf{A}}_{I} \\ &= \begin{bmatrix} 0 & \frac{\underline{Z}_{in}}{n} \\ \frac{1}{\underline{Z}_x} & 0 \end{bmatrix} \begin{bmatrix} 1 & \frac{\underline{Z}_{in}}{n^2} \\ 0 & 1 \end{bmatrix} \qquad \text{with} \quad \underline{\mathbf{A}}_{I1}^{-1} = \frac{1}{det(\underline{\mathbf{A}}_{I1})} \begin{bmatrix} 0 & -\underline{Z}_x \\ -\frac{n}{\underline{Z}_{in}} & 0 \end{bmatrix} \\ &= \begin{bmatrix} 0 & \frac{\underline{Z}_{in}}{n} \\ \frac{1}{\underline{Z}_x} & \frac{\underline{Z}_{in}}{n^2\,\underline{Z}_x} \end{bmatrix} \qquad \qquad = \begin{bmatrix} 0 & \frac{\underline{Z}_{in}}{n} \\ \frac{1}{\underline{Z}_x} & 0 \end{bmatrix}\end{aligned} \tag{A.19}$$

The matrices $\underline{\mathbf{A}}_{I1}$ and $\underline{\mathbf{A}}_{I2}$ fulfil Equation A.5, thus the decomposition is valid and it models the original two-port given in Equation A.13. Furthermore, the two-port $\underline{\mathbf{A}}_{I1}$ satisfies Equation A.14, thus the voltage $\underline{V}_I$ is a measure of the current $\underline{I}_{DUT}$ flowing into the DUT.

A.3.1.2.2 Conclusions about the Decomposition:

In section A.3.1.2, we have shown that port decompositions of both the voltage and the current path exist and they can be chosen such that the measured quantities $\underline{V}_V$ and $\underline{V}_I$ appear at the interfaces of their corresponding TPNs.
Throughout the section, we have worked with the idealized electrical network of the ZMS. In reality, parasitics and nonidealities will affect the TPNs, thus their values will vary slightly from what we have computed. This is where the calibration procedure is brought into play: we do not aim to compute the real TPNs analytically, but rather determine their unknowns through measurements with known calibration standards, knowing that the topology of the electrical network can be modeled by the cascade of decomposed TPNs.

A.3.1.3 Cascade Combination

For the creation of the desired SFG, it is sufficient to only consider a subset of the TPN cascade that encompasses the relevant quantities $\underline{V}_V$, $\underline{V}_I$ and $\underline{Z}_{DUT}$. Therefore, the leftmost TPN represented by $\underline{\mathbf{A}}_{V1}$ or $\underline{\mathbf{H}}_{V1}$ respectively can be left out as depicted in Figure A.3d. Furthermore, we can combine

$$\underline{\mathbf{A}}_A := \underline{\mathbf{A}}_{V2}\,\underline{\mathbf{A}}_{I1} \tag{A.20}$$

and define

$$\underline{\mathbf{A}}_B := \underline{\mathbf{A}}_{I2} \tag{A.21}$$

such that we are left with only two TPNs $\underline{\mathbf{A}}_A$ and $\underline{\mathbf{A}}_B$ or their equivalent representations in hybrid parameters $\underline{\mathbf{H}}_A$ and $\underline{\mathbf{H}}_B$.

A.3.2 Error Model and Calibration

We desire to find an equation for $\underline{G}$ as a function of $\underline{Z}_{DUT}$ that is linearly dependent on a set of N unknown error terms, such that those error terms can be determined uniquely using N known calibration standards $\underline{Z}_{DUT\,i}$ and corresponding measurements $\underline{G}_i$ with $i \in \{1 \ldots N\}$.

In this chapter we choose to work with hybrid parameters only, because they allow to set up a convenient SFG for the transfer function $\underline{G} = \frac{\underline{V}_V}{\underline{V}_I}$.

A.3.2.1 Signal Flow Graph Representation

We can set up an SFG for the remaining cascade of the TPNs $\underline{\mathbf{H}}_A$ and $\underline{\mathbf{H}}_B$ shown in Figure A.3d.

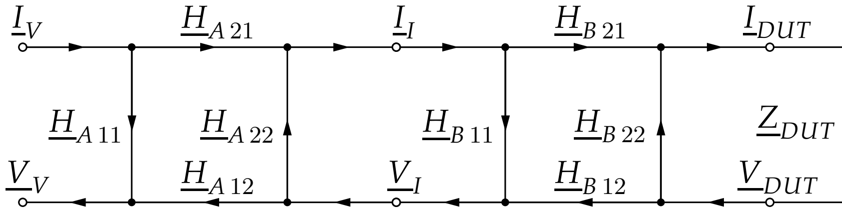


Figure A.6: SFG of the error model.

A.3.2.2 Calibration Equation

Applying *Mason's rule* to the SFG in Figure A.6, we can find the desired equation for $\underline{G}$, which is the transfer function from the node for $\underline{V}_I$ to the node for $\underline{V}_V$.

A.3.2.2.1 Definition of Mason's Rule

Mason's rule is defined as follows [62]:

$$G = \frac{x_k}{x_l} = \frac{1}{\Delta} \sum_{v=1}^{n} G_v \, \Delta_v \,, \tag{A.22}$$

where x_l is the source node, x_k the sink node, Δ the graph determinant, G_v the gain of the vth forward path and Δ_v its respective co-factor.

The determinant Δ of the graph is defined as

$$\Delta = 1 - \sum_i L_i + \sum_{i,j,i\neq j} L_i L_j - \sum_{i,j,k,i\neq j\neq k} L_i L_j L_k + \ldots \tag{A.23}$$

L_i denotes the ith closed loop gain in the system, $L_i L_j$ the product of the loop gains of any two non-touching loops and so forth.

The co-factor Δ_v of the graph is defined as

$$\Delta_v = 1 - \sum_i L_{i,v} + \sum_{i,j,i\neq j} L_{i,v} L_{j,v} - \sum_{i,j,k,i\neq j\neq k} L_{i,v} L_{j,v} L_{k,v} + \ldots , \tag{A.24}$$

where $L_{i,v}$, $L_{j,v}$ and $L_{k,v}$ are again loop gains of closed loops that are not touching the current forward path v.

A.3.2.2.2 Application of Mason's Rule

Looking at the SFG, we can quickly see that there is only one forward path ($n = 1$) connecting the desired nodes:

$$\underline{G}_1 = \underline{H}_{A\,12} \tag{A.25}$$

There is only one loop in the SFG that is not touching the one forward path, thus the co-factor from Equation A.24 reduces to

$$\underline{\Delta}_1 = 1 - \underline{L}_{1,1} , \tag{A.26}$$

where $\underline{L}_{1,1}$ is the loop gain of the one non-touching loop

$$\underline{L}_{1,1} = \underline{H}_{B\,22}\, \underline{Z}_{DUT} . \tag{A.27}$$

Consequently, we have

$$\underline{G}_1 \underline{\Delta}_1 = \underline{H}_{A\,12} - \underline{H}_{A\,12}\, \underline{H}_{B\,22}\, \underline{Z}_{DUT} . \tag{A.28}$$

In our SFG we have three closed loops with respective loop gains

$$\begin{aligned} \underline{L}_1 &= \underline{H}_{A\,22}\, \underline{H}_{B\,11} \\ \underline{L}_2 &= \underline{H}_{A\,22}\, \underline{H}_{B\,21}\, \underline{Z}_{DUT}\, \underline{H}_{B\,12} \\ \underline{L}_3 &= \underline{H}_{B\,22}\, \underline{Z}_{DUT} = \underline{L}_{1,1} \end{aligned} \tag{A.29}$$

The first and third loop are the only non-touching loops in the SFG and therefore the determinant Δ from Equation A.23 reduces to

$$\begin{aligned}\underline{\Delta} &= 1 - \sum_i \underline{L}_i + \sum_{i,j,i\neq j} \underline{L}_i\,\underline{L}_j \qquad \text{with} \qquad i,\,j\,\in\{1,\,2,\,3\}\\ &= 1 - \left[\underline{L}_1 + \underline{L}_2 + \underline{L}_3\right] + \left[\underline{L}_1\,\underline{L}_3\right]\\ &= 1 - \left[\underline{H}_{A\,22}\,\underline{H}_{B\,11} + \underline{H}_{A\,22}\,\underline{H}_{B\,21}\,\underline{Z}_{DUT}\,\underline{H}_{B\,12} + \underline{H}_{B\,22}\,\underline{Z}_{DUT}\right]\\ &\quad + \left[\underline{H}_{A\,22}\,\underline{H}_{B\,11}\,\underline{H}_{B\,22}\,\underline{Z}_{DUT}\right] \end{aligned} \tag{A.30}$$

Inserting the individual results in Equation A.22, we yield for the transfer function

$$\begin{aligned}\underline{G} &= \frac{\underline{V}_V}{\underline{V}_I} = \frac{1}{\underline{\Delta}}\,\underline{G}_1\,\underline{\Delta}_1\\ &= \frac{\underline{H}_{A\,12} - \underline{H}_{A\,12}\,\underline{H}_{B\,22}\,\underline{Z}_{DUT}}{1 - \underline{H}_{A\,22}\,\underline{H}_{B\,11} - \underline{H}_{A\,22}\,\underline{H}_{B\,21}\,\underline{Z}_{DUT}\,\underline{H}_{B\,12} - \underline{H}_{B\,22}\,\underline{Z}_{DUT} + \underline{H}_{A\,22}\,\underline{H}_{B\,11}\,\underline{H}_{B\,22}\,\underline{Z}_{DUT}}\,. \end{aligned} \tag{A.31}$$

Rearranging, we get

$$\begin{aligned}&\underline{G} - \underline{G}\,\underline{H}_{A\,22}\,\underline{H}_{B\,11} - \underline{G}\,\underline{H}_{A\,22}\,\underline{H}_{B\,21}\,\underline{Z}_{DUT}\,\underline{H}_{B\,12} - \underline{G}\,\underline{H}_{B\,22}\,\underline{Z}_{DUT} +\\ &+ \underline{G}\,\underline{H}_{A\,22}\,\underline{H}_{B\,11}\,\underline{H}_{B\,22}\,\underline{Z}_{DUT} = \underline{H}_{A\,12} - \underline{H}_{A\,12}\,\underline{H}_{B\,22}\,\underline{Z}_{DUT}\,, \end{aligned} \tag{A.32}$$

where the known quantities are the impedance of the calibration standard $\underline{Z}_{DUT}$ and the measured quantity $\underline{G}$. We separate all the unknown error terms, i.e. expressions including hybrid parameters from our fictitious error adapters, from the entirely known terms:

$$\begin{aligned}\underline{G} &= \underline{H}_{A\,12} - \underline{H}_{A\,12}\,\underline{H}_{B\,22}\,\underline{Z}_{DUT} + \underline{G}\,\underline{H}_{A\,22}\,\underline{H}_{B\,11} +\\ &+ \underline{G}\,\underline{H}_{A\,22}\,\underline{H}_{B\,21}\,\underline{Z}_{DUT}\,\underline{H}_{B\,12} + \underline{G}\,\underline{H}_{B\,22}\,\underline{Z}_{DUT} - \underline{G}\,\underline{H}_{A\,22}\,\underline{H}_{B\,11}\,\underline{H}_{B\,22}\,\underline{Z}_{DUT} \end{aligned} \tag{A.33}$$

We are left with an inhomogeneous, nonlinear equation system. Now we com-

bine the unknowns to get an inhomogeneous linear equation system:

$$\underline{G} = \underbrace{\underline{H}_{A\,12}}_{:=\underline{d}} + \underline{Z}_{DUT} \underbrace{\left(-\underline{H}_{A\,12}\,\underline{H}_{B\,22}\right)}_{:=\underline{e}} + \underline{G} \underbrace{\left(\underline{H}_{A\,22}\,\underline{H}_{B\,11}\right)}_{:=\underline{f}} \tag{A.34}$$

$$+ \underline{Z}_{DUT}\,\underline{G} \underbrace{\left(\underline{H}_{A\,22}\,\underline{H}_{B\,21}\,\underline{H}_{B\,12} + \underline{H}_{B\,22} - \underline{H}_{A\,22}\,\underline{H}_{B\,11}\,\underline{H}_{B\,22}\right)}_{:=\underline{g}} \tag{A.35}$$

The equation

$$\underline{d} + \underline{Z}_{DUT}\,\underline{e} + \underline{G}\,\underline{f} + \underline{Z}_{DUT}\,\underline{G}\,\underline{g} = \underline{G} \tag{A.36}$$

is linear in the 4 unknowns $\underline{d}$, $\underline{e}$, $\underline{f}$ and $\underline{g}$. The equation is correctly derived and holds information about how a measurement $\underline{G}$ corresponds to an impedance $\underline{Z}_{DUT}$, but it is not computationally useful: by solving a linear equation system, the coefficients, i.e. $\underline{d}$, $\underline{e}$, $\underline{f}$ and $\underline{g}$, shall be found such that they satisfy the given equations. By looking at Equation A.36, we can clearly see that it always holds true for a choice $\underline{f} = 1$ and $\underline{d} = \underline{e} = \underline{g} = 0$. Consequently, the terms $\underline{d}$, $\underline{e}$ and $\underline{g}$ would exhibit very small numbers in a real application.

Therefore, we would like to go back to Equation A.34 and simplify further:

$$\begin{aligned}
\underline{G}\left(1 - \underline{H}_{A\,22}\,\underline{H}_{B\,11}\right) &= \underline{H}_{A\,12} + \underline{Z}_{DUT}\left(-\underline{H}_{A\,12}\,\underline{H}_{B\,22}\right) \\
&\quad + \underline{Z}_{DUT}\,\underline{G}\left(\underline{H}_{A\,22}\,\underline{H}_{B\,21}\,\underline{H}_{B\,12} + \underline{H}_{B\,22} - \underline{H}_{A\,22}\,\underline{H}_{B\,11}\,\underline{H}_{B\,22}\right) \\
\underline{G} &= \underbrace{\frac{\underline{H}_{A\,12}}{1 - \underline{H}_{A\,22}\,\underline{H}_{B\,11}}}_{:=\underline{a}} + \underline{Z}_{DUT} \underbrace{\frac{-\underline{H}_{A\,12}\,\underline{H}_{B\,22}}{1 - \underline{H}_{A\,22}\,\underline{H}_{B\,11}}}_{:=\underline{b}} + \\
&\quad + \underline{Z}_{DUT}\,\underline{G} \underbrace{\frac{\underline{H}_{A\,22}\,\underline{H}_{B\,21}\,\underline{H}_{B\,12} + \underline{H}_{B\,22} - \underline{H}_{A\,22}\,\underline{H}_{B\,11}\,\underline{H}_{B\,22}}{1 - \underline{H}_{A\,22}\,\underline{H}_{B\,11}}}_{:=\underline{c}}
\end{aligned} \tag{A.37}$$

Through this step, we both reduced the number of error terms by one and arrived at a result that is computationally useful.

The equation

$$\underline{a} + \underline{Z}_{DUT}\,\underline{b} + \underline{Z}_{DUT}\,\underline{G}\,\underline{c} = \underline{G} \tag{A.38}$$

is linear in the $N = 3$ unknowns $\underline{a}$, $\underline{b}$ and $\underline{c}$. N linearly independent measurements will give us a *single* result for these unknowns and therefore allow a calibration for linear systematic errors. This calibration is valid only for the single frequency for which the calibration was done. A calibration over a band of frequencies can be achieved if calibration measurements are conducted using a supply signal that is swept in frequency.

A.3.2.3 Correction Equation

After the calibration has been completed and the error terms have been computed, the previously known impedance $\underline{Z}_{DUT}$ given by the well characterized calibration standards will be replaced by the actual DUT with a now *unknown impedance*. We can solve Equation A.38 for $\underline{Z}_{DUT}$ and use the computed error terms to correct the measurement:

$$\begin{aligned}
\underline{a} + \underline{Z}_{DUT}\,\underline{b} + \underline{Z}_{DUT}\,\underline{G}\,\underline{c} &= \underline{G} \\
\underline{Z}_{DUT}\left(\underline{b} + \underline{G}\,\underline{c}\right) &= \underline{G} - \underline{a} \\
\underline{Z}_{DUT} &= \frac{\underline{G} - \underline{a}}{\underline{b} + \underline{G}\,\underline{c}}
\end{aligned} \tag{A.39}$$

Equation A.39 can be used to correct linear systematic errors in any measurement $\underline{G}$ and compute the impedance of the DUT.

A.3.2.4 Dimensions of the Error Terms

The quantity $\underline{G}$ is a dimensionless quantity, since it is the ratio of $\underline{V}_V$ to $\underline{V}_I$, yet it is proportional to the impedance $\underline{Z}_{DUT}$. Consequently, all linear terms in Equation A.38 have to be dimensionless too.

- The denominator of all three error terms is also dimensionless, since $\underline{H}_{A\,22}$ has the dimension siemens and $\underline{H}_{B\,11}$ has the dimension ohms.
- The numerator of $\underline{a}$ is dimensionless, since off-diagonal elements of hybrid parameters like $\underline{H}_{A\,12}$ are dimensionless.

- The numerator of $\underline{b}$ has the dimension of siemens, since it is multiplied with an impedance and the product must be dimensionless. $\underline{H}_{B\,22}$ has the dimension siemens.
- The numerator of $\underline{c}$ has the dimension of siemens as well. The summands of the numerator all have an uneven number of diagonal elements that result in the dimension siemens.

Now that we determined the dimensions of the individual error terms, we also have to check that the dimensions agree for the correction Equation A.39:

$$\left[\underline{Z}_{DUT}\right] = \frac{[\underline{G}] - [\underline{a}]}{[\underline{b}] + [\underline{G}]\,[\underline{c}]} = \frac{[1] - [1]}{S + [1]\,S} = \frac{1}{S} = \Omega \tag{A.40}$$

Consequently, the dimensions of both the calibration Equation A.34 as well as the correction Equation A.39 match the physical meanings of their respective quantities.

TU Graz

APPENDIX B

NTAG

Measurement Repeatability

This chapter shows plots of several different measurement campaigns for the sake of evaluation of the *measurement repeatability* of the designed impedance measurement system.

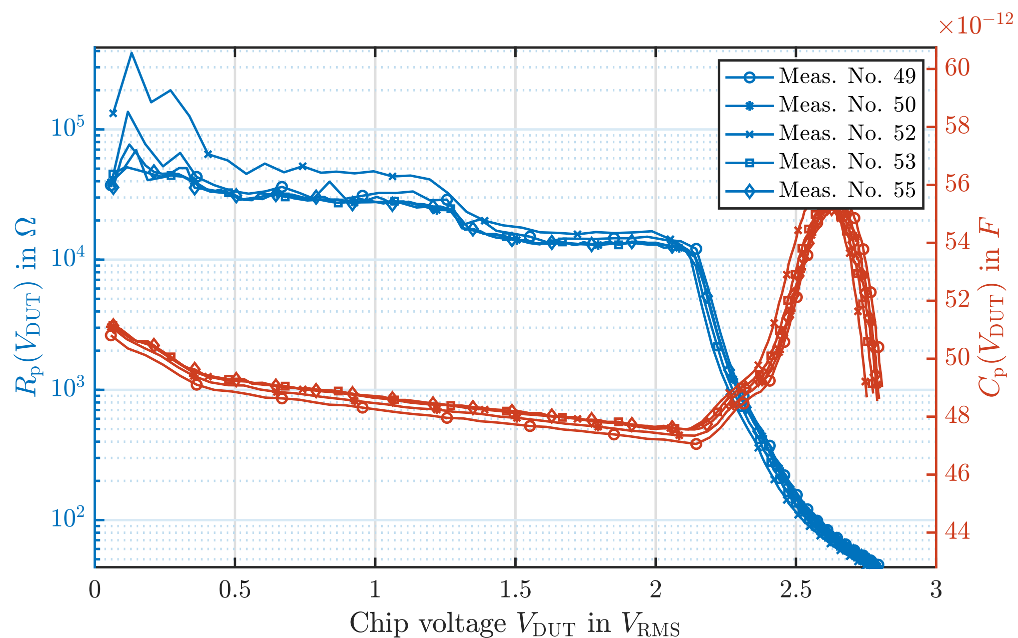


Figure B.1: Meas. repeatability; comparison of several meas. series.

SLIX2

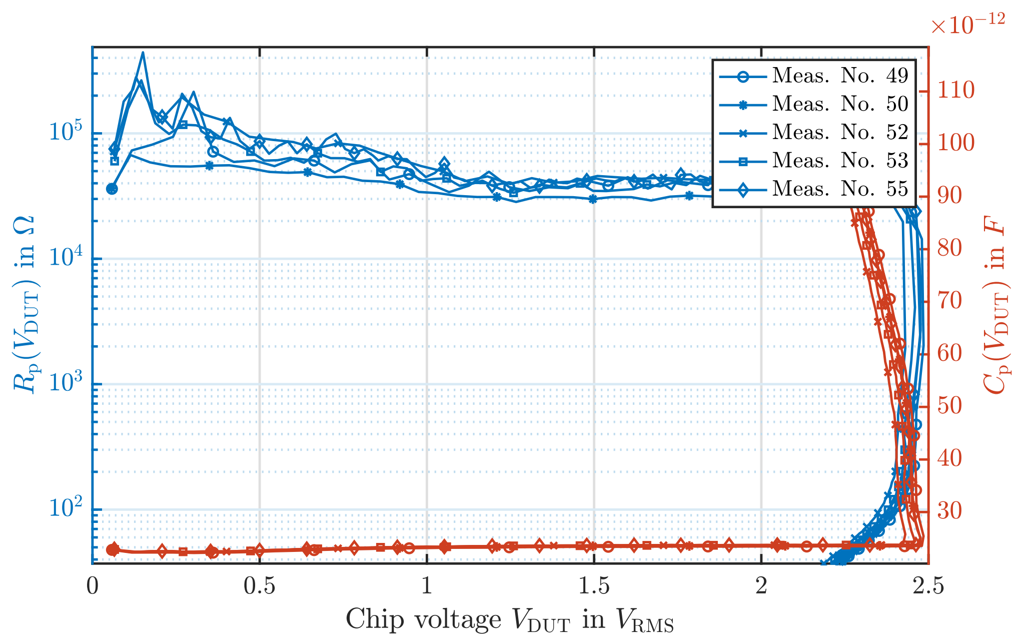


Figure B.2: Meas. repeatability; comparison of several meas. series.

DESFIRE

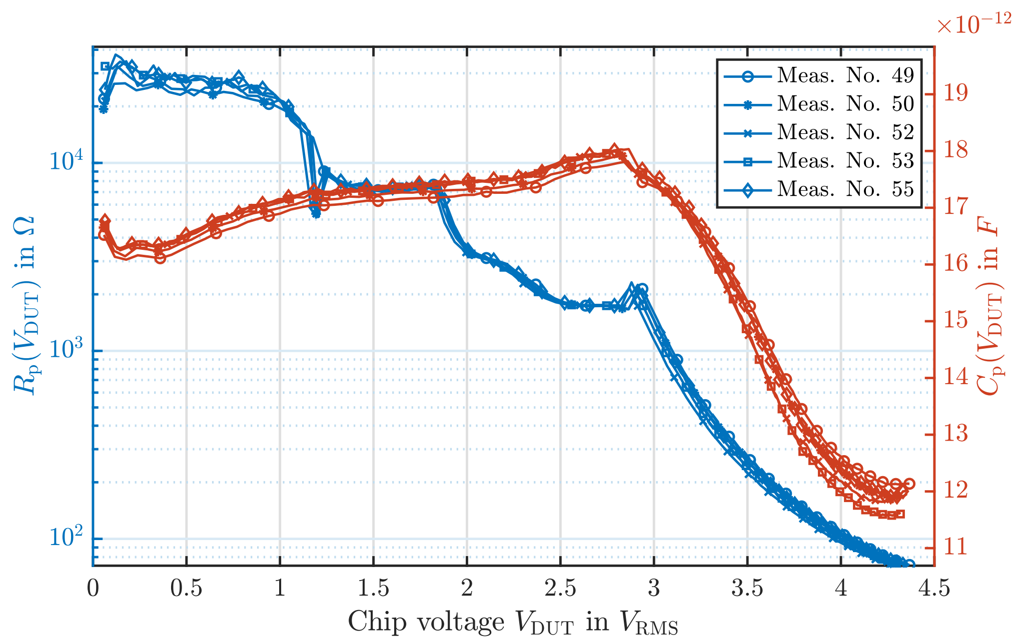


Figure B.3: Meas. repeatability; comparison of several meas. series.

Ultral

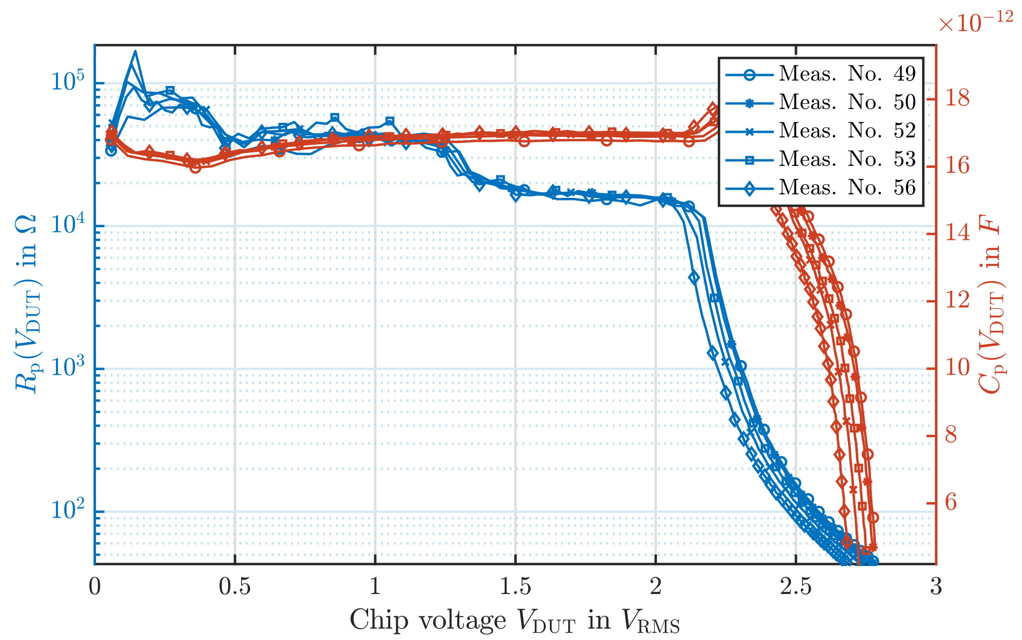


Figure B.4: Meas. repeatability; comparison of several meas. series.

Classic

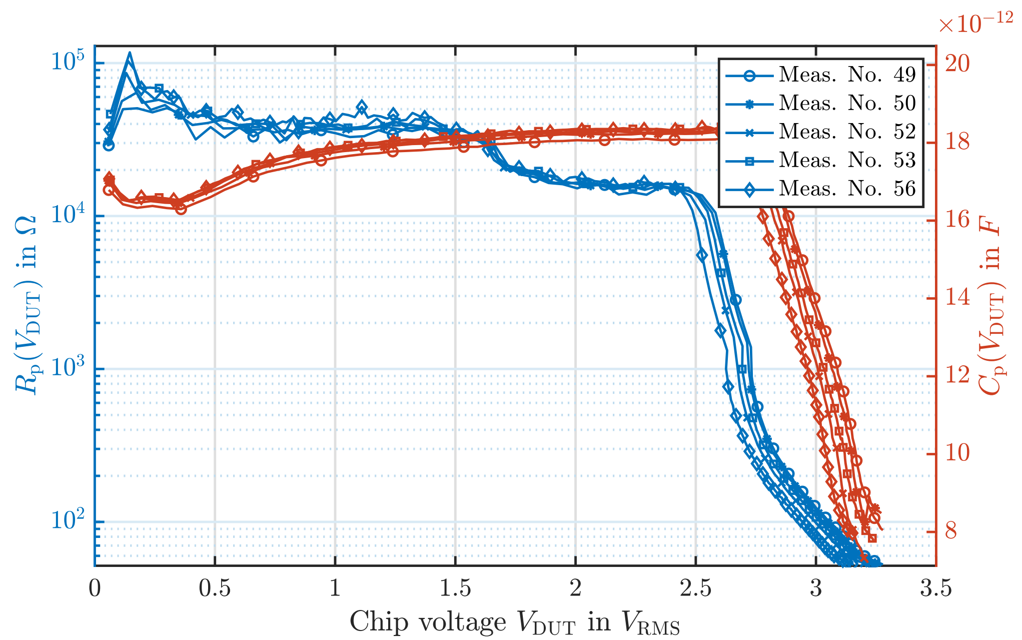


Figure B.5: Meas. repeatability; comparison of several meas. series.

TAG-IT

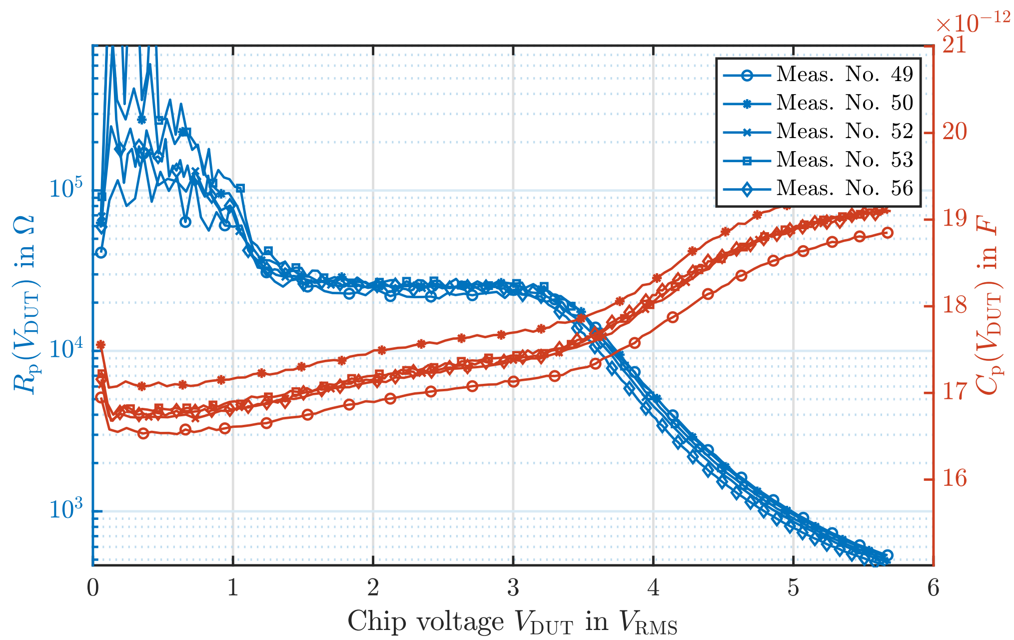


Figure B.6: Meas. repeatability; comparison of several meas. series.

EM4200

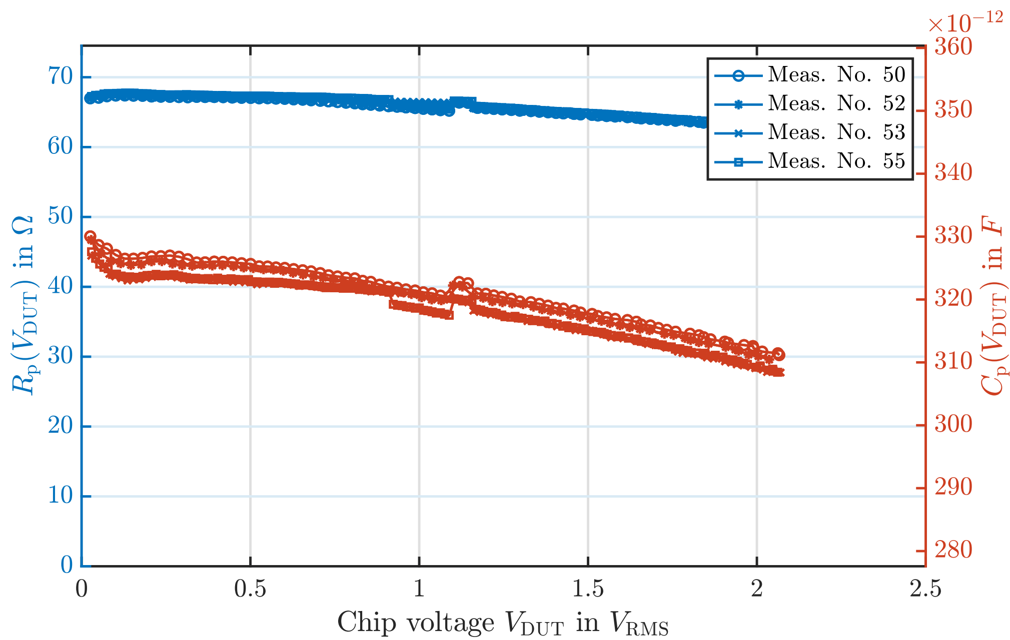


Figure B.7: Meas. repeatability; comparison of several meas. series.

MIM256

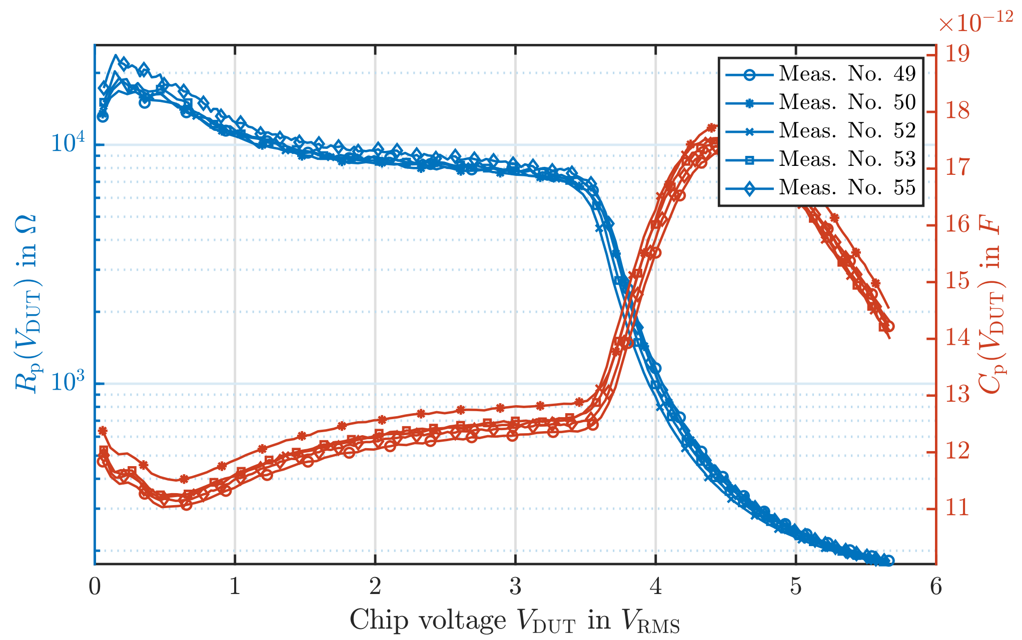


Figure B.8: Meas. repeatability; comparison of several meas. series.

K50

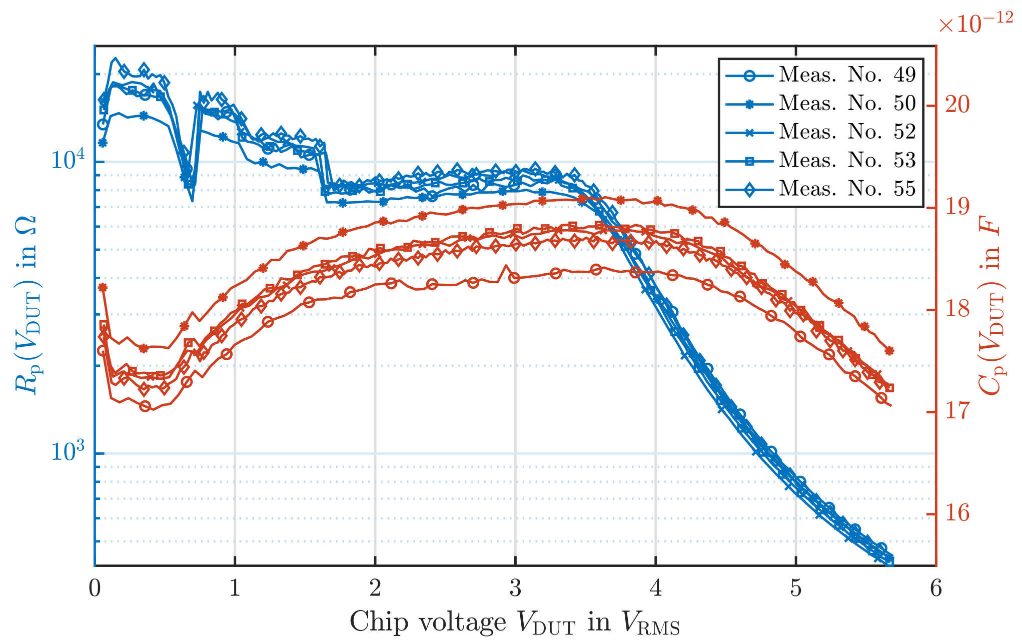


Figure B.9: Meas. repeatability; comparison of several meas. series.

TKS50

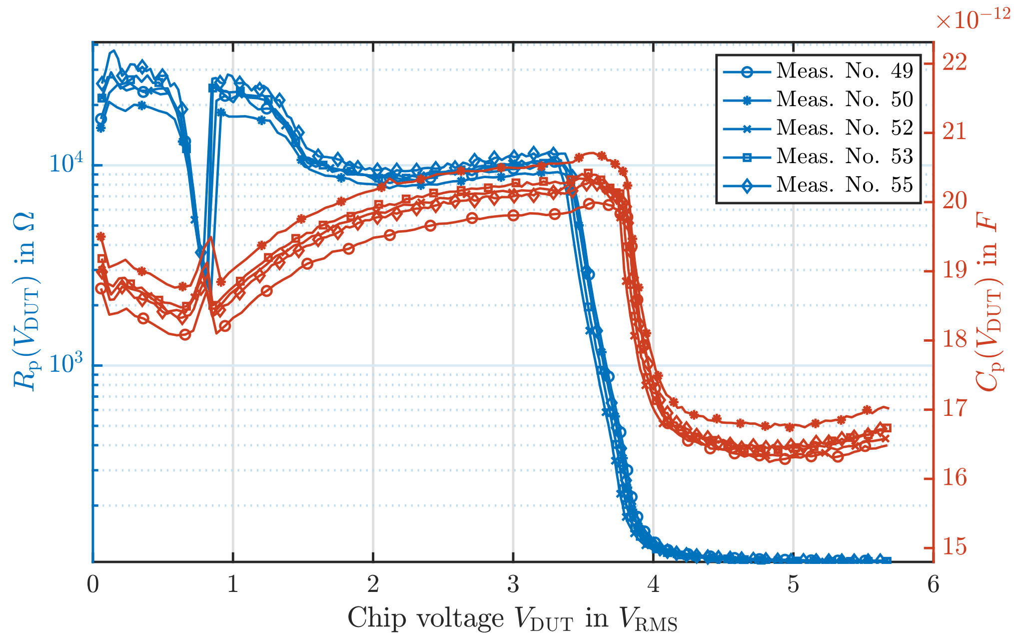


Figure B.10: Meas. repeatability; comparison of several meas. series.

FM248

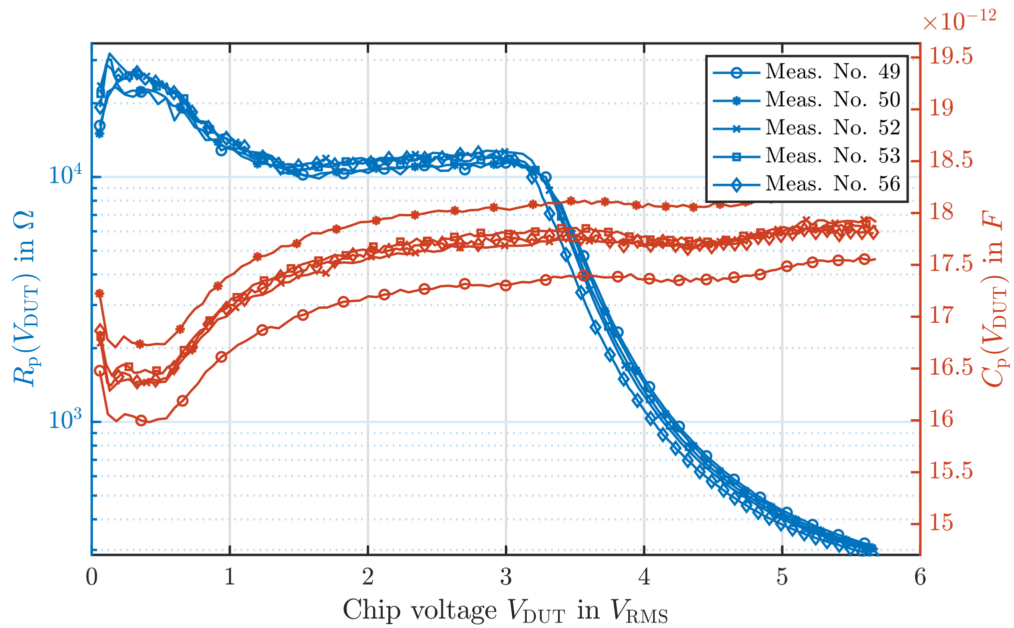


Figure B.11: Meas. repeatability; comparison of several meas. series.

FM388

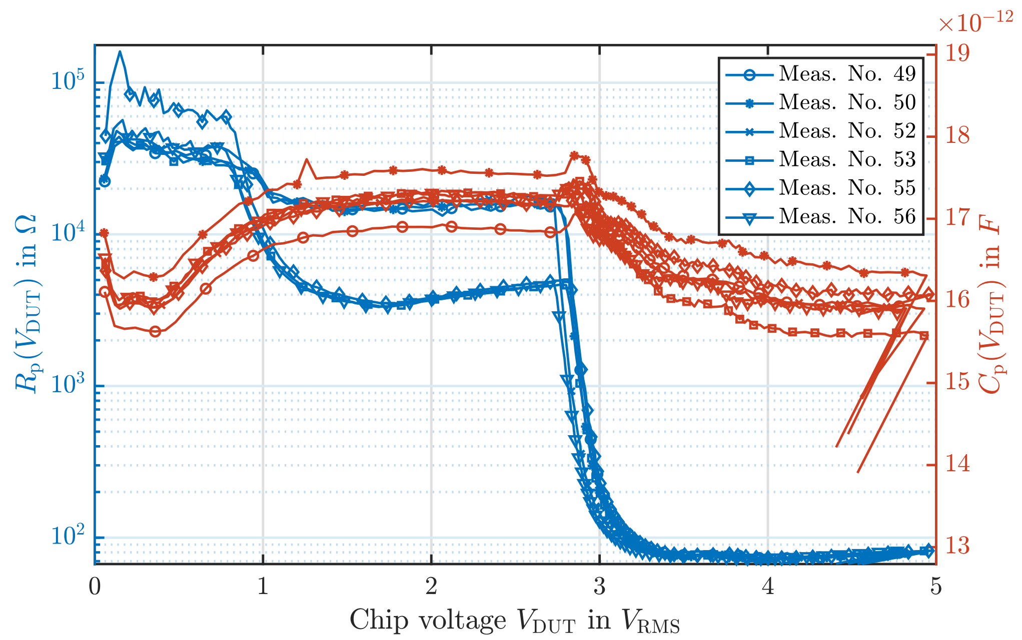


Figure B.12: Meas. repeatability; comparison of several meas. series.

8001Z6

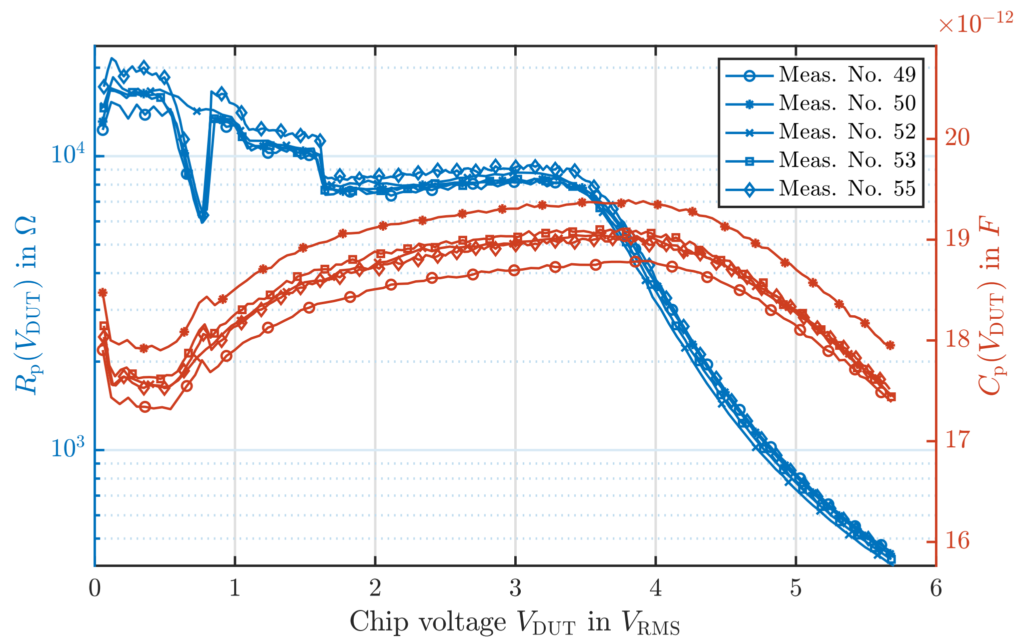


Figure B.13: Meas. repeatability; comparison of several meas. series.

GT5680

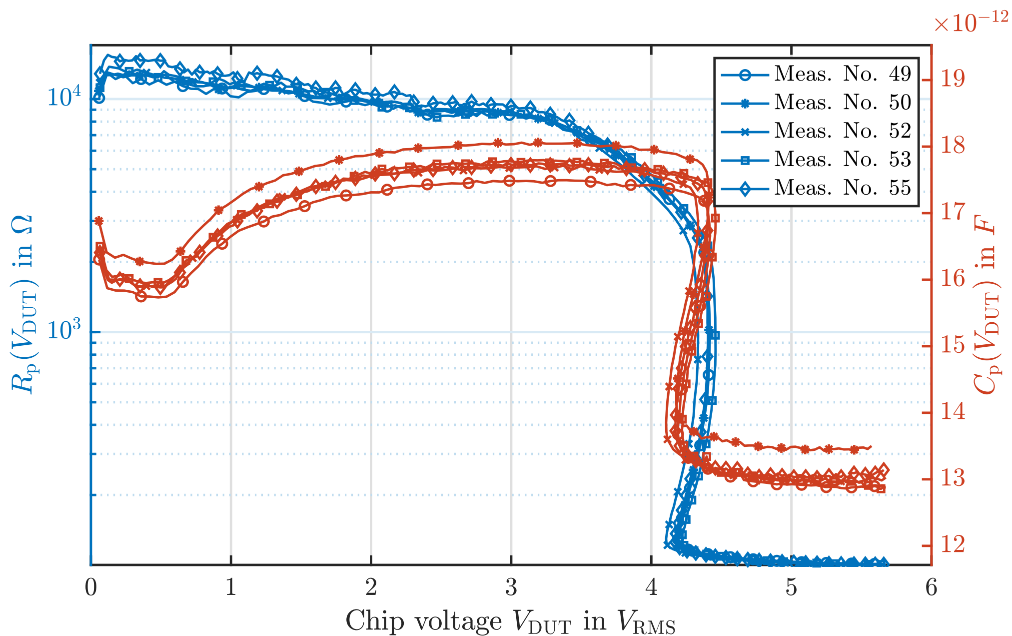


Figure B.14: Meas. repeatability; comparison of several meas. series.

GT5652

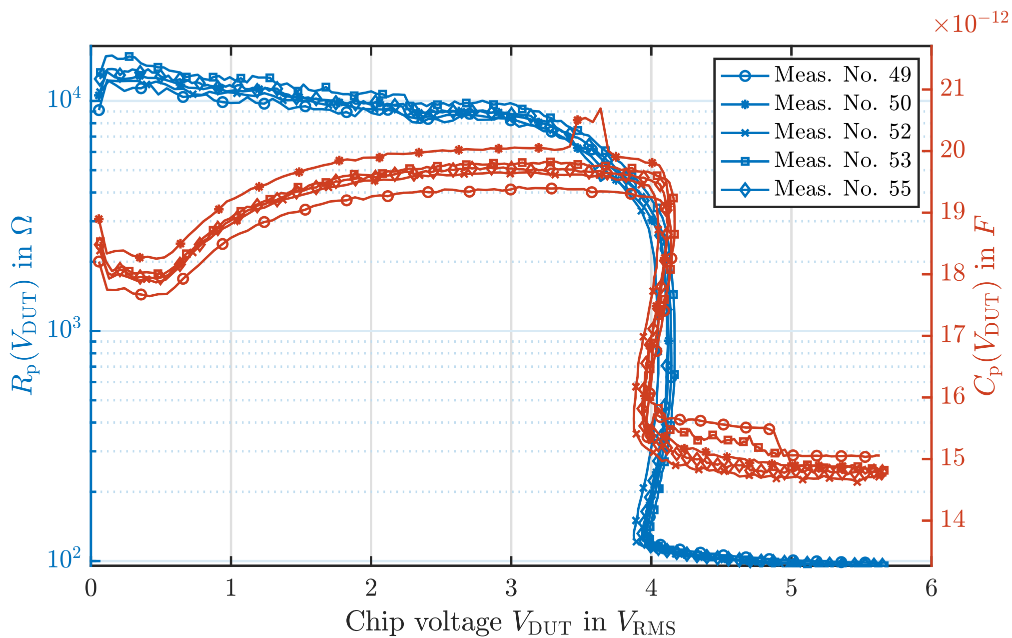


Figure B.15: Meas. repeatability; comparison of several meas. series.

GT5670

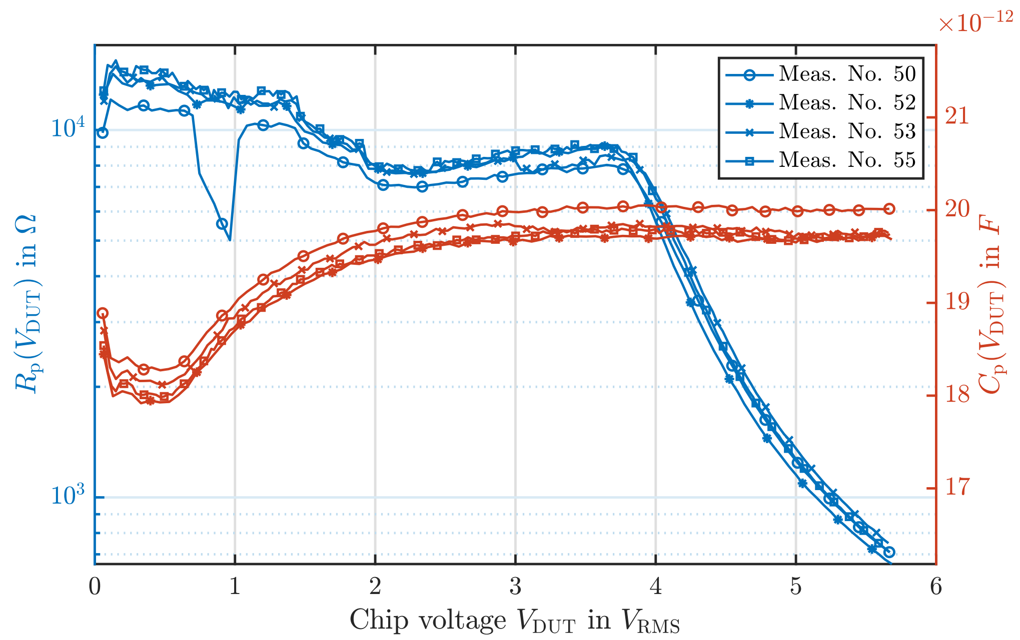


Figure B.16: Meas. repeatability; comparison of several meas. series.

UNKNOWN

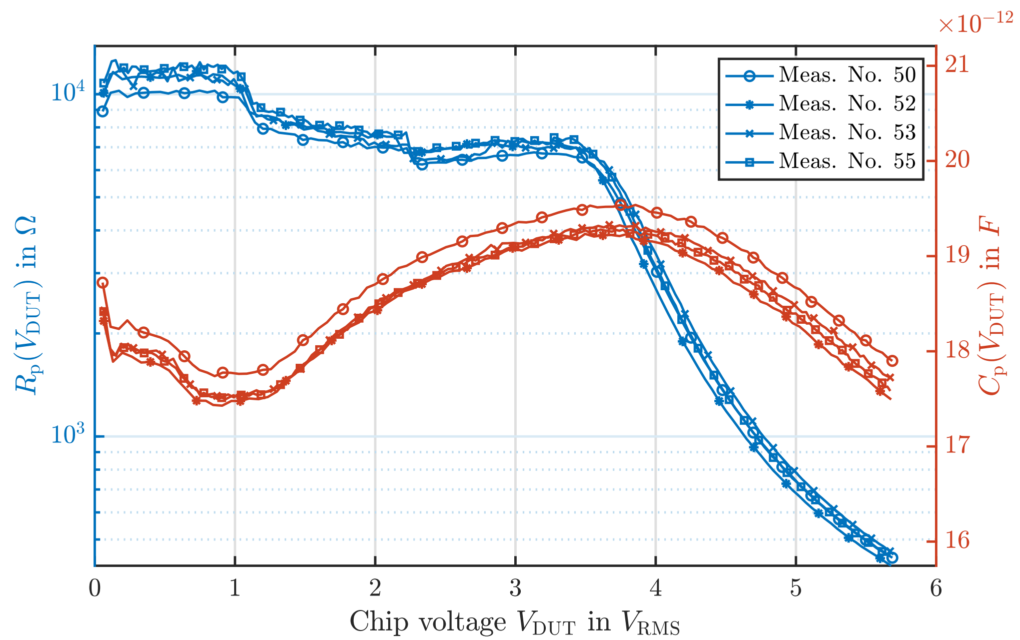


Figure B.17: Meas. repeatability; comparison of several meas. series.