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AnSim: An Analytic Simulator for Electronic Circuits

DISSERTATION

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Abstract

In many fields of electronics, the number of competitors continues to be on the rise. Shortening the market launch, the so-called time to market (TTM), is therefore essential when gaining an advantage over the competition. The electronic development (from prototype to the final design) shall be as efficient as possible. A wide range of applications needs electronic circuits, e.g., from simple analog circuits to switch mode power supplies. The specification (functions or requirements for the circuit design) must be met over the entire product lifetime. In addition to the ambient conditions during operation, additional influencing factors such as component tolerances and component aging have to be taken into account. Electronic circuits can be designed by calculation and/or simulation, respectively. The most efficient method would be to compute the circuit (i.e., by an equation for the function or the worst-case values, and also using mathematical operations directly). However, this is not always possible for reasons of complexity.

The aim of this thesis is to develop a tool for the design of electronic circuits and, most notably, for the sizing of the components that can be used as universally as possible, which supports calculation as well as simulation. Its central element is the development of an analytic forward solver. The electronic circuit is described by switched networks with piecewise-linear models (symbolic state-space equations). A closed-form analytic solution is computed for each model. The advantages of this analytic approach are: no convergence problems (since no numerical integration is required), high simulation speed (especially for small-scale electronic circuits), high accuracy, as well as small data file sizes. In many cases, the exact signal waveforms are not required for the calculation (e.g., forward voltage of a diode as a function of the current), only the minimum and maximum values (to determine if the function or the component specification is fulfilled). More complex electronics circuits are realized by several simpler models. Therefore, even complex electronics circuits can be modeled and analyzed relatively easily. In particular, the sensitivity of an output variable/performance parameter with respect to individual parameters, e.g.,

through a parameter variation can be analyzed.

Zusammenfassung

In vielen Bereichen der Elektronik nimmt die Anzahl der Wettbewerber immer mehr zu. Eine Verkürzung der Markteinführungszeit, die sogenannte Time-to-Market (TTM), ist daher wesentlich, um Wettbewerbsvorteile gegenüber der Konkurrenz zu erzielen. Das Ziel ist es, die Elektronikentwicklung (vom Prototypen bis zum finalen Design) möglichst effizient zu gestalten. Ein großer Bereich der Anwendungen benötigt elektronische Schaltungen, angefangen von einfachen analogen Schaltungen hin bis zu getakteten Stromversorgungen. Dabei muss garantiert werden, dass die Spezifikation (Funktionen bzw. Anforderungen an das Schaltungsdesign) über die gesamte Produktlebensdauer eingehalten wird. Es müssen neben den Umweltbedingungen im Betrieb noch zusätzliche Einflussfaktoren wie Bauteiltoleranzen und Bauteilalterung berücksichtigt werden. Die Dimensionierung einer elektronischen Schaltung kann durch Berechnung und/oder Simulation erfolgen. Die effizienteste Methode wäre die Berechnung (eine Formel für die Funktion oder der Worst-Case-Werte und des Weiteren auch die direkte Anwendung von mathematischen Operationen ermöglichen) der elektronischen Schaltung, was jedoch aus Komplexitätsgründen nicht immer möglich ist.

Das Ziel dieser Dissertation ist es, ein möglichst universal einsetzbares Dimensionierungstool zu entwickeln, welches sowohl Berechnung als auch Simulation unterstützt. Ein wesentlicher Bestandteil dieser Arbeit ist die Entwicklung eines analytischen Vorwärtslösers. Die elektronische Schaltung wird durch geschaltete lineare Netzwerke mit stückweise linearen Modellen (symbolische Zustandsraumgleichungen) beschrieben. Für jedes Modell wird eine analytische Lösung in geschlossener Form berechnet. Die Vorteile dieses analytischen Ansatzes sind: Keine Konvergenzprobleme (da keine nummerische Integration erforderlich), hohe Simulationsgeschwindigkeit (insbesondere bei kleinen elektronischen Schaltungen), hohe Genauigkeit, sowie eine geringe Datengröße der Dateien. Da in vielen Fällen für die Berechnung nicht die exakten Signalverläufe (z.B. Vorwärtsspannung einer Diode in Abhängigkeit des Stromes) benötigt werden, sondern nur Min- und Max-Werte

(um zu bestimmen, ob die Funktion bzw. Bauteilspezifikation eingehalten wird), ist dieser Ansatz möglich. Komplexere elektronische Schaltungen werden durch mehrere einfachere Modelle realisiert. Dadurch können auch komplexere elektronische Schalungen relativ einfach modelliert und analysiert werden. Insbesondere können die Sensitivität einer Ausgangsgröße/eines Performanceparameters gegenüber einzelner Parameter z.B. durch eine Parametervariation beurteilt werden.

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The biggest thanks go to my family, especially my wife and my children for always supporting me.

Chapter 1

Overview

1.1 Introduction

Today, virtual prototyping is the most efficient way for the development of electronic apparatuses. Electronic components always come with certain tolerances; therefore, the sizing of the electronic circuits to consider the worst-case (extreme) values of the different parameters[1], i.e., worst-case sizing of electronic circuits composed of such components, has been gaining more and more in importance. Two essential aspects must be considered: the specification of the device (must be met), and the components are not allowed to be overloaded. This can be succinctly summarized as the design limits of the device and the design limits of the individual components, respectively. The design limits of the device must be determined by the ranges of the components' parameters[2] (so-called worst-case parameter models) and need to stay below the pre-defined limits, e.g., current and voltage limits mainly defined in the specification of the electronic apparatuses. The design limits of the individual components are determined (considering the ranges of the components' parameters, too) and should never exceed the defined limits in the components' datasheets.

Computer-aided circuit simulators are used to identify the design limits of the device and/or the design limits of the individual components, respectively. Some simulators (e.g., LTspice [1] and PSpice [2]) offer the possibility for a Monte Carlo (MC) analysis. This stochastic analysis provides statistical data on the impact of a device parameter's variance. A major disadvantage of such stochastic methods is that they require a high number of simulation runs to reach the device's design limits

[1] The parameters can be constants or variables.

[2] Including the ambient conditions during operation (e.g., ambient temperature T_A), additional relationships (e.g., $f(i)$ or $f(u)$), tolerances, and aging.

or the design limits of the individual components. Other simulators (e.g., Saber [3] and Simplorer [4]) provide numerical optimization methods to perform a worst-case analysis. Here also, several simulation runs are required to reach the device's design limits or the design limits of the individual components. This can be advantageously improved by computing currents and voltages analytically.

For an efficient sizing of electronic circuits, the following building blocks are needed:

- the elemental circuit description (of the electronic circuit) and the formulation of the circuit equations;
- a forward solver[3];
- an optimization method[4];
- the ranges of the components' parameters[2] needed by the optimization method.

AnSim is the basis of the design tool, containing the proposed analytic forward solver approach, and an optimizer package.[5] AnSim can be used as universally as possible, supports calculation as well as simulation and is notably suitable for parameter studies, optimization and worst-case sizing of small-scale electronic circuits.

Generally, two main concepts can be distinguished between: standard simulators which use complex nonlinear models like SPICE [6] and simulators based on switched networks with piecewise-linear (PWL) models. An overview of the different circuit simulator approaches is provided in Chapter 2.

Further distinction may be made based on the elemental circuit description, the formulation of the circuit equations (network formulation) and the method used for solving the circuit equations (details in Section 1.3).

The special challenges of circuit simulators are as follows:

- convergence problems due to the numerical integration for solving the systems of differential equations. The choice of step size for the numerical integration is a compromise between accuracy (size of data files) and simulation speed;

[3] A forward solver provides the solution of the state variables and the signals of interest.

[4] An optimization method varying the values of the components in a meaningful way to minimize the objective function, to identify the design limits of the device or the design limits of the individual components, respectively.

[5] The implemented methods include, e.g., sequential quadratic program (SQP), evolution strategy (1+1) [5], and Monte Carlo (MC) analysis.

- varying the values of the components in a meaningful way to identify the design limits of the device or the design limits of the individual components, respectively; in a few steps even if the worst-case values are not on the boundaries of the parameters;
- determination of the ranges of the components' parameters.[2]

Design tools for different applications (e.g., DC/DC converters) from different semiconductor companies are also available. These tools mostly support only fixed circuits, the companies' own components, and are very limited in the modeling of the individual components and their parameters.

1.1.1 Standard simulators which use complex nonlinear models

The semiconductor devices are modeled with complex nonlinear models. Generally, numerical methods are used for solving the system of differential equations. As an illustration, a simple p-n junction diode model is shown in (1.1) [6] as it is used in SPICE.

$$I_{\mathrm{D}}(V_{\mathrm{D}}, T) = I_{\mathrm{S}}(T)\left(\mathrm{e}^{\frac{qV_{\mathrm{D}}}{nkT}} - 1\right) \tag{1.1}$$

where

I_{D}	diode current
I_{S}	reverse bias saturation current
q	electron charge
V_{D}	voltage across the diode
n	emission coefficient
k	Boltzmann constant
T	absolute temperature of the p-n junction

The advantage is that the properties (switching behavior) of the real components are well approximated. The disadvantages are, relatively slow simulation speed, convergence problems, large data files and the difficulty in changing only one component property without affecting other component properties. For example, the forward voltage of a p-n junction diode (1.1) is not described in an explicit form. In this simple case, it is possible to solve the forward voltage V_{D} from (1.1), but if the model became more complex, then solving for a specific parameter would be more challenging, if possible at all. Therefore, a worst-case forward voltage model (generally referred to as a worst-case parameter model) is difficult to implement.

1.1.2 Simulators based on switched networks with piecewise-linear models

The semiconductor devices are modeled with switched networks with piecewise-linear models. The different conditions (states) of the semiconductors are modeled from a set of constant voltage sources, constant current sources, resistances, inductances and capacitances. The nonlinearities of the inductances and capacitances can be addressed by approximating these elements with PWL models, too. The advantages are: simpler models, much faster simulation speed, and the possibility to change only one component property without affecting other component properties, too. The disadvantages are: the exact switching behavior of the semiconductors cannot be modeled, and a control of the individual PWL models (evaluation of the boundary conditions) is required. For example, the forward voltage of a p-n junction diode is modeled as a constant value, and a worst-case parameter model is easy to implement.

1.2 The proposed approach

The proposed analytic forward solver approach (a resource efficient precision transient circuit simulator without a time step for solving the systems of differential equations) uses analytic solution techniques to identify the time-dependent solution of voltages or currents using proper state equations in closed form and has been developed especially for parameter studies, optimization and worst-case sizing of small-scale electronic circuits. Electronic circuits with linear elements, for example, R, C, L, and independent current and voltage sources, can be described by a system of differential equations, introduced and depicted in the following as SubCircuit-Models.[6] Circuits composed of nonlinear elements, such as $L(i)$, $C(u)$, Diodes, MOSFETs, BJTs, and/or PWM controllers are described by piecewise-linear models and denoted in the following as Circuit-Models.[7] For the elemental circuit description, the proposed forward solver approach uses this special Circuit-Model instead of the widely used netlist as used, for example, in SPICE.

The implemented sequential quadratic program (SQP) is used for optimization (finding the best parameter set to minimize the objective function) and identifying

[6] A SubCircuit-Model is described in Section 2.2.
[7] A Circuit-Model is described in Section 2.3.

the worst-case scenario (the design limits of the device or the design limits of the individual components, respectively). It is found that the worst-case scenario can be obtained with as few solutions to the forward problem as possible by applying an SQP method. The SQP method in combination with the proposed analytic forward solver approach shows that the identification of the worst-case value converges in a few steps even if the worst-case value is not on the boundary of the parameters.

The proposed approach allows for conducting a full search over the parameter space. The ranges of the components' parameters (worst-case parameter model) needed from the SQP method are easy to implement, as explained in Section 1.2.1, and illustrated using an example in Section 1.2.2.

The advantages are:

- the full flexibility in the modeling of the individual components and their parameters referred to as SubCircuit-Models, respectively Circuit-Models;
- the electronic circuit to be simulated can be built from such SubCircuit-Models without the transformation to a state-space model and the final Circuit-Model is only built once and saved;
- simulation results are extremely compact (functions of the state variables and the signals of interest are returned); this creates the opportunity to investigate certain intervals of time in detail without simulating these repeatedly with a smaller step size, as in the case with a numerical solver and can theoretically be stored with arbitrary precision; even with a high number of simulation runs, the generated data remain easy to handle;
- no convergence problems arise because numerical integration for solving the systems of differential equations is not required;
- analytic methods show the potential of more efficient parameter studies; the worst-case scenario can be obtained with as few solutions to the forward problem as possible by applying an SQP method;
- the SQP method in combination with the proposed analytic forward solver approach shows that the identification of the worst-case value converges in a few steps even if the worst-case value is not on the boundary of the parameters.

1.2.1 The proposed approach to model the circuit elements' parameters

In many cases, the exact transient current/voltage curves of the semiconductors do not need do be known. To prove the reliability of the electronic circuit instead, the ranges of the parameters are required. Based on this assumption, the stationary behavior of the semiconductors with constant voltage sources, constant current sources, and resistors can be modeled. The range of the parameters depends on the components used in the electronic circuit and the ambient conditions. The worst-case ranges of the components' parameters are needed. To avoid excessive time consuming datasheet interpolations and scalings, a worst-case parameter model is used instead that describes the range of values the circuit element can take.

In some cases (e.g., more complex electronic system), the simulation is not the most efficient method (time consuming modeling of the real system); thus, prototyping is the better option. The prototype must be tuned to a worst-case prototype, to guarantee each individual function. Worst-case parameter models are also intended to support the construction of the worst-case prototypes. The procedure for a worst-case parameter model is explained in the following. The forward voltage parameter of a diode is chosen for illustration. The forward voltage characteristics of a general purpose (GP) diode for different junction temperatures T_J, usually available in the diode's datasheet, are shown in Figure 1.1. The typical forward voltage characteristic $V_{\mathrm{F\,typ}}(I_\mathrm{F})$ is then approximated with piecewise-linear functions (1.2). The support points (marked by blue dots) are drawn in Figure 1.1.

$$V_{\mathrm{F\,typ}}(I_\mathrm{F}, 25\,^\circ\mathrm{C}) = \begin{cases} 0.5, & I_\mathrm{F} < 0.0001 \\ 0.5 + 15.075\,(I_\mathrm{F} - 0.0001)\,, & 0.0001 \le I_\mathrm{F} < 0.02 \\ 0.8 + 3.75\,(I_\mathrm{F} - 0.02)\,, & 0.02 \le I_\mathrm{F} < 0.1 \\ 1.1 + 0.333\,(I_\mathrm{F} - 0.1)\,, & I_\mathrm{F} \ge 0.1 \end{cases} \tag{1.2}$$

Additionally, the min/max values of V_F are also often provided in a diode datasheet. In all cases, at least the maximum value at one point is given. If only the maximum value is given, the minimum value is evaluated by the tolerance $C_\mathrm{TOL} = \left(1 - \frac{V_{\mathrm{F\,max}}}{V_{\mathrm{F\,typ}}}\right)$. If not otherwise specified in the diode datasheet, the minimum limit and the maximum limit curves are obtained by scaling the typical curve $V_{\mathrm{F\,typ}}(I_\mathrm{F}, 25\,^\circ\mathrm{C})$ with the tolerance $(1 - C_\mathrm{TOL})$ and $(1 + C_\mathrm{TOL})$ respectively, shown in Figure 1.2. The tempera-

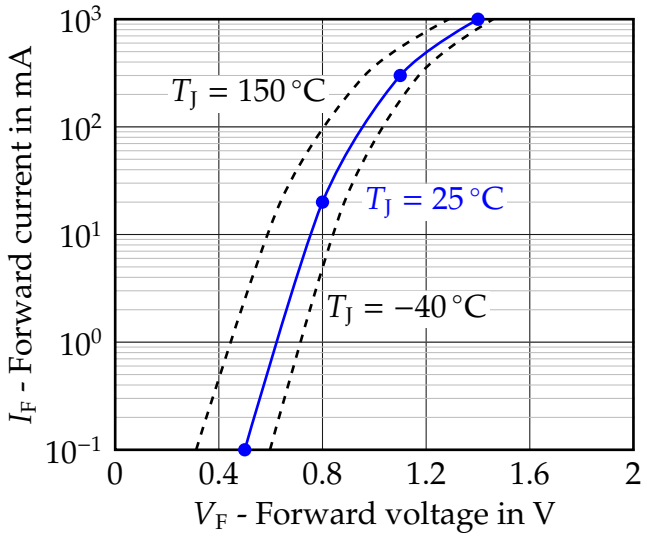

Figure 1.1: Illustrated forward voltage characteristic for different junction temperatures T_J of a GP diode.

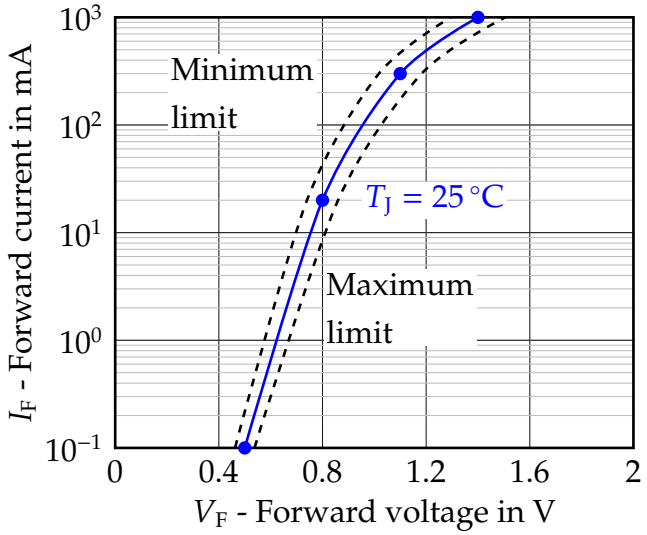

Figure 1.2: Illustrated forward voltage characteristics with limits of a GP diode.

ture dependency of V_F is considered as an offset $\Delta V_{F\,T_J}$ and is modeled by a constant factor $C_{TJ} = \frac{dV_F}{dT_J}\Big|_{I_F=\text{const.}}$ multiplied by $(T_J - 25\,°C)$ and is summarized in (1.3). The factor C_{TJ} is estimated from the forward characteristics at 25 °C and 150 °C shown in

Figure 1.1 at $I_F = 0.1\,\text{mA}$, and is defined by (1.4).

$$\Delta V_{F\,T_J} = C_{TJ}\,(T_J - 25\,^\circ\text{C}) \tag{1.3}$$

$$C_{TJ} = \frac{V_F(0.0001\,\text{A}, 25\,^\circ\text{C}) - V_F(0.0001\,\text{A}, 150\,^\circ\text{C})}{25\,^\circ\text{C} - 150\,^\circ\text{C}} = -1.5\,\text{mV}/^\circ\text{C} \tag{1.4}$$

Scaling the approximated typical forward voltage (1.2) by the tolerance factor $(1 + C_{TOL})$ and adding the temperature dependent part (1.3) results in the final worst-case forward voltage model (equation) as summarized in

$$V_F(I_F, T_J, C_{TOL}) = V_{F\,typ}(I_F, 25\,^\circ\text{C})\,(1 + C_{TOL}) + C_{TJ}\,(T_J - 25\,^\circ\text{C})\ . \tag{1.5}$$

1.2.2 Example case worst-case diode forward voltage model

For illustration purposes, the simple voltage reference circuit shown in Figure 1.3 should be sized, by calculation, illustrating the advantages of the analytic solution techniques in combination with worst-case parameter models. The specification is summarized in Table 1.1. For the diode D_1, the GP diode from the previous Section 1.2.1 is chosen. The self-heating of diode D_1 is neglected (low power dissipation), therefore it follows that $T_J = T_A$. Applying Kirchhoff's Current/Voltage Law to the electronic circuit in Figure 1.3 results in (1.6).

Table 1.1: Specification of the simple voltage reference circuit of Figure 1.3.

Characteristic	Minimum	Typical	Maximum
Product lifetime (operating time) t_L	10 years		
Operating temperature range T_A	0 °C	25 °C	60 °C
Input voltage range V_{DC}	10.8 V	12.0 V	13.2 V
Output current I_{out}	80 µA	100 µA	120 µA
Output voltage V_{out}	0.412 V	0.512 V	0.612 V

Requirements:

1. The resistor R_1 should allow the full range of the output voltage $V_{out} = V_F$.
2. The design limits of the resistor R_1 ($R_{1\,P}$ and $R_{1\,VRMS}$) and the diode D_1 ($D_{1\,VRR}$, $D_{1\,IF(AV)}$, $D_{1\,IFR}$, and $D_{1\,TJ}$) need to stay below their datasheet limits.

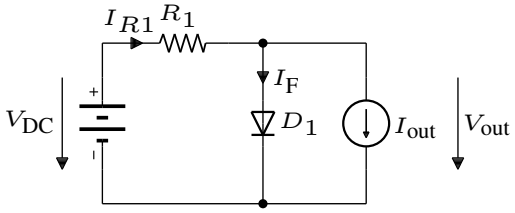

Figure 1.3: Simple voltage reference circuit.

$$I_F = \frac{(V_{DC} - V_F(I_F, T_J, C_{TOL}))}{R_1} - I_{out} \tag{1.6}$$

Before the resistor R_1 can be defined, its lower and upper bounds need to be determined. The boundary parameters $I_{F\,max}$ and $T_{J\,max}$ as well as $I_{F\,min}$ and $T_{J\,min}$, along with $\pm C_{TOL}$ are used to determine $V_{out\,min}$ (1.7) and $V_{out\,max}$ (1.8) respectively.

$$V_{out\,min} = V_F(I_{F\,max}, T_{J\,max}, -C_{TOL}) \tag{1.7}$$

$$V_{out\,max} = V_F(I_{F\,min}, T_{J\,min}, C_{TOL}) \tag{1.8}$$

Then, (1.7) and (1.8) are solved for $I_{F\,max}$ and $I_{F\,min}$, respectively, producing $I_{F\,min} = 0.153\,\text{mA}$ and $I_{F\,max} = 2.466\,\text{mA}$. Using the boundaries of V_{out} from (1.6) instead of $V_F(I_F, T_J, C_{TOL})$, the solutions of I_F and the worst-case parameter sets (to identify $R_{1\,min}$ and $R_{1\,max}$ respectively) from Table 1.1 results in (1.9) and (1.10).

$$R_{1\,min} = \frac{V_{DC\,max} - V_{out\,max}}{I_{F\,min} + I_{out\,min}} = 4.95\,\text{k}\Omega \tag{1.9}$$

$$R_{1\,max} = \frac{V_{DC\,min} - V_{out\,min}}{I_{F\,max} + I_{out\,max}} = 37.96\,\text{k}\Omega \tag{1.10}$$

The value of R_1 can be chosen arbitrarily (no additional requirement e.g., the efficiency of the voltage reference circuit) in the range of $R_{1\,min} \leq R_1 \leq R_{1\,max}$ and was set to $12\,\text{k}\Omega \pm 10\,\%$.[8] The maximum power, element voltage, and resistance change of the resistor R_1 are summarized in Table 1.2. The maximum ratings of the GP diode are summarized in Table 1.3. The new boundaries of V_{out} are calculated, by using (1.6) with the worst-case parameter sets (to identify $I_{F\,min}$ and $I_{F\,max}$, respectively) from Table 1.1 and are described by (1.11)–(1.14).

[8] The tolerance of R_1 includes: the resistance basic tolerance ($\pm 5\,\%$), the resistance change due to temperature ($\pm 0.5\,\%$), the resistance change due to soldering heat ($\pm 0.5\,\%$), the resistance change due to aging ($\pm 2\,\%$, refer $\Delta R/R$ in Table 1.2), and an additional safety margin of $\pm 2\,\%$.

Table 1.2: Maximum ratings (datasheet parameters) for the resistor R_1 and the design limits for the simple voltage reference of Figure 1.3.

Symbol	Parameter	Datasheet limits	Design limits
P_{70}	Power rating for $T_A \leq 70\,°C$	0.25 W	0.016 W[1]
V_{RMS}	Limiting element voltage	200 V	12.8 V[2]
$\Delta R/R$	Max. resistance change at P_{70} after: 225000 h	±2 %	-

[1] $R_{1\,P} = (I_{F\,max} + I_{out\,max})^2\, R_{1\,max} = 0.016\,W$
[2] $R_{1\,VRMS} = V_{DC\,max} - V_{F\,min} = 12.8\,V$

Table 1.3: Maximum ratings (datasheet parameters) for the GP diode D_1 and the design limits for the simple voltage reference of Figure 1.3.

Symbol	Parameter	Datasheet limits	Design limits
V_{RRM}	Peak repetitive reverse voltage	50 V	≤ 0 V[1]
$I_{F(AV)}$	Average rectified forward current	1 A	1.095 mA[2]
I_{FRM}	Peak repetitive forward current	30 A	1.095 mA[3]
T_J	Maximum junction temperature	175 °C	60.1 °C[4]
$R_{\theta JA}$	Thermal resistance, junction to ambient	85 °C/W	-

[1] $D_{1VRR} \leq 0\,V$ limited by design.
[2] $D_{1\,IF(AV)} = I_{F\,max} = 1.095\,mA$
[3] $D_{1\,IFR} = I_{F\,max} = 1.095\,mA$
[4] $D_{1\,TJ} = T_{A\,max} + V_{F\,max} I_{F\,max} R_{\theta JA} = 60.1\,°C$

$$I_{F\,min} = \frac{(V_{DC\,min} - V_F(I_{F\,min}, T_{J\,max}, -C_{TOL}))}{R_{1max}} - I_{out\,max} = 0.658\,mA \tag{1.11}$$

$$V_{F\,min} = V_F(I_{F\,min}, T_{J\,max}, -C_{TOL}) = 0.419\,V \tag{1.12}$$

$$I_{F\,max} = \frac{(V_{DC\,max} - V_F(I_{F\,max}, T_{J\,min}, C_{TOL}))}{R_{1min}} - I_{out\,min} = 1.095\,mA \tag{1.13}$$

$$V_{F\,max} = V_F(I_{F\,max}, T_{J\,min}, C_{TOL}) = 0.59\,V \tag{1.14}$$

$$I_{F\,typ} = \frac{\left(V_{DC\,typ} - V_F(I_{F\,typ}, T_{J\,typ}, 0)\right)}{R_{1typ}} - I_{out\,typ} = 0.857\,mA \tag{1.15}$$

$$V_{F\,typ} = V_F(I_{F\,typ}, T_{J\,typ}, 0) = 0.511\,V \tag{1.16}$$

Table 1.4: Design limits of V_{out} of the simple voltage reference circuit of Figure 1.3.

Characteristic	Minimum	Typical	Maximum
Output voltage V_{out}	0.419 V	0.511 V	0.590 V

With $V_{out} = V_F$ the boundaries for V_{out} are:

$$V_{out\,min} = 0.419\,\text{V} \text{ and } V_{out\,max} = 0.59\,\text{V}.$$

Additionally, the typical output voltage $V_{out\,typ}$ is calculated by (1.15) and (1.16). The boundaries for V_{out} and the typical output voltage are summarized in Table 1.4. The functionality (requirements) of the simple voltage reference circuit summarized in Table 1.1 was proven. The design limits for the resistor R_1 and the diode D_1 are calculated and summarized in Table 1.2 and in Table 1.3. All its parts, i.e., the resistor R_1 and the GP diode D_1, are used within their specifications.

1.3 State of the art in formulation of the circuit equations

Computer-aided circuit simulators can be distinguished by three basic features: The first is the elemental circuit description, which can be carried out via a netlist. The second is the formulation of the circuit equations (network formulation) which can, for example, be done with the Nodal Analysis (NA), Modified Nodal Analysis (MNA), or State-space Approach (SSA). The third is the method used for solving the circuit equations.

1.3.1 Standard approach(es)

An advantage of the widely used NA and MNA [7] is that they can be easily implemented in computer programs for circuit analysis. The algorithm of constructing the set of equations directly from the circuit schematics (netlist) is very simple [8]. NA (1.17) uses Kirchhoff's Current Law for the branch currents at each node in the electronic circuit. The branch constitutive equations (BCE) and Kirchoff's Voltage Law are used to relate the branch currents to branch voltages and the branch voltages

to node voltages, respectively [9].

$$\mathbf{YV} = \mathbf{J} \tag{1.17}$$

where

- $\mathbf{Y}$ nodal admittance matrix
- $\mathbf{V}$ column vector of the node voltages
- $\mathbf{J}$ column vector of the independent source currents

The disadvantage of the NA method is that, it does not enable analyzing circuits containing voltage sources and elements that lack an admittance matrix, such as transformers [8]. For elements which have no admittance representation, the MNA (1.18) [9] must be used.

$$\underbrace{\begin{bmatrix} \mathbf{Y}_R & \mathbf{B} \\ \mathbf{C} & \mathbf{D} \end{bmatrix}}_{A} \underbrace{\begin{bmatrix} \mathbf{V} \\ \mathbf{I} \end{bmatrix}}_{\mathbf{x}(t)} = \underbrace{\begin{bmatrix} \mathbf{J} \\ \mathbf{F} \end{bmatrix}}_{\mathbf{u}(t)} \tag{1.18}$$

where

- $\mathbf{Y}_R$ reduced form of the nodal admittance matrix $\mathbf{Y}$
- $\mathbf{B}$ matrix represents the contribution to the Kirchoff's Current Law at each node of the additional output or controlling current variables, $\mathbf{I}$
- $\mathbf{V}$ column vector of the node voltages
- $\mathbf{J}$ column vector of the independent source currents
- $\mathbf{C}$, $\mathbf{D}$ matrices representing the branch constitutive relations, differentiated with respect to the unknown vector
- $\mathbf{I}$ column vector of the extra branch currents
- $\mathbf{F}$ column vector of the independent source voltages
- $\mathbf{A}$ MNA matrix

The dynamic MNA equations for the linear case can be written as [10]:

$$\mathbf{G}\mathbf{x}(t) + \mathbf{H}\dot{\mathbf{x}}(t) = \mathbf{u}(t) \tag{1.19}$$

where

- $\mathbf{G}$ MNA system matrix
- $\mathbf{H}$ constant matrix arising from the contributions of all the dynamic L and C elements

Approaches for solving the NA and MNA (circuit) equations (1.17) and (1.18), respectively, in the time-domain are:

- Several numerical methods exist for solving a system of differential equations

$$\dot{\mathbf{x}}(t) = \mathbf{f}(\mathbf{x}, t)\,, \tag{1.20}$$

for example, the backward Euler algorithm [11]

$$\mathbf{x}_{n+1} = \mathbf{x}_n + h\mathbf{f}(\mathbf{x}_{n+1}, t_{n+1})\,, \tag{1.21}$$

and the trapezoidal algorithm. Applying the backward Euler algorithm to (1.19), the backward Euler solution is summarized in (1.22) where h is the step size [12].

$$\mathbf{x}_{n+1} = (\mathbf{H} + h\mathbf{G})^{-1}[\mathbf{H}\mathbf{x}_n + h\mathbf{u}(t_{n+1})] \tag{1.22}$$

- Alternatively, numerical integration for discrete circuit models for capacitors and inductors can be applied, [11]. In this case, capacitors and inductors are approximated by a resistive circuit[9] in association with the integration algorithm. The discrete circuit associated with the backward Euler algorithm, in the case of a linear capacitor, is shown in Figure 1.4. The current i_{n+1} through a linear capacitor is approximated using the backward Euler algorithm:

$$i_{n+1} = \frac{C}{h}v_{n+1} - \frac{C}{h}v_n \tag{1.23}$$

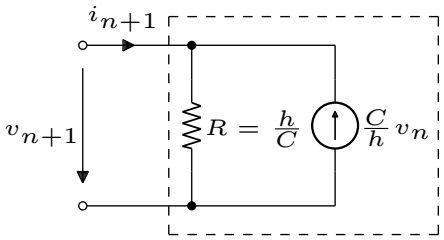

Figure 1.4: Discrete circuit models for a linear capacitor, [11].

1.3.2 State-space equation approach

State-space equations are the smallest possible subset of circuit equations to describe a circuit. The normal matrix form of the state-space model is [8, 11, 13, 14]:

$$\begin{aligned}\dot{\mathbf{x}}(t) &= \mathbf{A}\mathbf{x}(t) + \mathbf{B}\mathbf{u}(t)\\ \mathbf{y}(t) &= \mathbf{C}\mathbf{x}(t) + \mathbf{D}\mathbf{u}(t)\end{aligned} \tag{1.24}$$

[9] The step size divided by the capacitance is seen as a resistance.

where

$\mathbf{x}(t)$	column vector of state variables
$\dot{\mathbf{x}}(t)$	column vector of first order derivative of the state variables
$\mathbf{u}(t)$	column vector of the input
$\mathbf{y}(t)$	column vector of the output
$\mathbf{A}$	state matrix
$\mathbf{B}$	input matrix
$\mathbf{C}$	output matrix
$\mathbf{D}$	feedforward matrix

Several methods to obtain the state-space equations from the circuit description are available and can be found, for example, in [8,11,15–18]. Approaches for solving the state-space (circuit) equations (1.24) in the time-domain are:

- numerical integration:

  applying the backward Euler algorithm, for example, to (1.24), the backward Euler solution is summarized in (1.25) where h is the step size [11].

$$\mathbf{x}_{n+1} = (\mathbf{1} - h\mathbf{A})^{-1}[\mathbf{x}_n + h\mathbf{u}(t_{n+1})] \tag{1.25}$$

- state-transition matrix:

  Closed-form analytic solution of (1.24) (e.g., [11,14]):

$$\mathbf{x}(t) = \mathbf{\Phi}(t)\mathbf{x}(0) + \int_0^t \mathbf{\Phi}(t-\tau)\mathbf{B}\mathbf{u}(\tau)\mathrm{d}\tau \tag{1.26}$$

  where $\mathbf{\Phi}(t)$ is called the state-transition matrix and is defined by

$$\mathbf{\Phi}(t) = \mathrm{e}^{\mathbf{A}t}\,. \tag{1.27}$$

- Laplace transform (e.g., [11,14]):
  the solution for the Laplace transform of (1.24) is

$$\mathbf{X}(s) = \frac{\mathrm{adj}(s\mathbf{I} - \mathbf{A})}{\det(s\mathbf{I} - \mathbf{A})}[\mathbf{x}(0) + \mathbf{B}\mathbf{U}(s)]\,. \tag{1.28}$$

  To obtain the time-domain solution, the inverse Laplace transform is used

$$\mathbf{x}(t) = \mathscr{L}^{-1}\left[\,\mathbf{X}(s)\,\right]. \tag{1.29}$$

1.3.3 Other approaches

Other approaches for the formulation of the circuit equations do exist, too. Due to their complexity, respectively their application class, they are not suitable for the analytic forward solver approach (analytic time-domain transient analysis). Still, for the sake of completeness, an overview, including a briefly assessment, is provided.

- The Sparse Tableau Formulation (Tableau Method) [6, 8, 11–13, 19] is a method where all branch currents, all branch voltages, and all nodal voltages are retained as unknowns. Thus, the formulation is most general (everything is available after solution) but leads to large system matrices [12]. Complicated reordering and solution algorithms are necessary to offset the size of the Tableau [6].

- The Hybrid Formulation (Hybrid Method) [6, 11, 13] is a modification of the state-space method, except that the algebraic relationships are not eliminated (no attempt is made to eliminate them in subsequent calculations) [13]. The selection of a network tree is necessary which is a critical part of the formulation algorithm to obtain well-conditioned Hybrid equations [6].

- The Topological Method (Signal Flow) [8, 11, 13, 20] is based on the Mason's formula [20], which constructs the transfer function of a signal flow graph representation of a source node to any other nonsource node [13].

- The Ports Method [13, 21] is based on the interconnection and reduction of one and two-port networks. The networks are characterized by their e.g., impedance and admittance [13].

The state-space equation approach has been selected for the formulation of the circuit equations for the analytic forward solver approach, because a closed-form analytic solution (1.26) exists. Additionally, the effort for generating the state-space equation from the elemental circuit description is relative low, which is described in Section 2.1.

1.4 List of publications

The work presented in this thesis has resulted in the following journal publications:

1. **Mario Schenk**, Annette Muetze, and Klaus Krischan, *An analytic approach for resource efficient parametric simulation of electronic circuits*, EPE Journal **30** (2020), no. 1, 33–47.
   DOI: https://doi.org/10.1080/09398368.2019.1697077.

2. **Mario Schenk**, Annette Muetze, Klaus Krischan, and Christian Magele, *Worst-case analysis of electronic circuits based on an analytic forward solver approach*, COMPEL - The international journal for computation and mathematics in electrical and electronic engineering **38** (2019), no. 5, 1655–1666.
   DOI: https://doi.org/10.1108/COMPEL-12-2018-0531.

1.5 Overview of the thesis

The introduction of this thesis provides a short overview of the motivation for this work, notably the need for circuit simulators and their unique challenges. The two main concepts of circuit simulators (standard simulators and simulators based on switched networks with piecewise-linear models) are presented. The advantages of the proposed approach are presented as well as the SubCircuit-Models, Circuit-Models (used for the elemental circuit description) and the SQP method (used for optimization and identifying the worst-case scenario). Additionally, the state of the art in formulation of the circuit equations is presented.

Chapter 2 provides an overview of the different circuit simulator approaches. The basic structure of a SubCircuit-Model of the proposed analytic forward solver approach (for solving electronic circuits) is described. The basic structure of a Circuit-Model and the timedomain transient analysis of the proposed method is presented. The SQP approach for optimization and worst-case analysis of electronic circuits is explained in more detail.

Chapter 3 illustrates the claimed advantages of the proposed closed-form analytic approach with respect to small data file size and CPU time in the case of parameter studies by means of the chosen example case applications, an open-loop and a closed-loop flyback converter. The simulation results obtained from the proposed approach with those of two other simulators as well as experimental results are compared.

Chapter 4 shows two example case applications of worst-case analyses, an RLC series resonant circuit and a flyback converter in continuous conduction mode. The SQP method in combination with the analytic forward solver approach illustrates that the identification of the worst-case values converges in a few steps even if the worst-case values are not on the boundary of the parameters.

Chapter 5 illustrates a third example case application, the sizing of a step down converter. In contrast to the previous example case applications, first the SQP method is used in combination with the analytic forward solver approach to optimize the efficiency of the step down converter. In the second step, the different components of the step down converter are sized by applying the SQP method in combination with the analytic forward solver approach.

Chapter 6 summarizes this work and also provides an outlook for further investigations.

Chapter 2

Analytic forward solver approach for solving electronic circuits

Today, many circuit simulators for electronic circuits with different approaches are available. The proposed approach uses analytic solution techniques and has been developed especially for parameter studies, optimization and identification of the worst-case sizing[1] of small-scale electronic circuits.

The advantages are:

- the full flexibility in the modeling of the individual components and their parameters referred to as SubCircuit-Models, respectively Circuit-Models;
- the electronic circuit to be simulated can be built from such SubCircuit-Models without the transformation to a state-space model and the final Circuit-Model is only built once and saved;
- simulation results are extremely compact (functions of the state variables and the signals of interest are returned); this creates the opportunity to investigate certain intervals of time in detail without simulating these repeatedly with a smaller step size, as in the case with a numerical solver and can theoretically be stored with arbitrary precision; even with a high number of simulation runs, the generated data remain easy to handle;
- no convergence problems arise because numerical integration for solving the systems of differential equations is not required;
- analytic methods show the potential of more efficient parameter studies.

[1] Worst-case sizing has been described in Section 1.1.

While a comprehensive review of all existing circuit simulators does not fall within the scope of this thesis, a short overview is provided, for the sake of completion.

Generally, two main concepts can be distinguished between: standard simulators which use complex nonlinear models (e.g., [22–25]) like SPICE [6] along with its multiple derivatives and simulators based on switched networks with piecewise-linear models (e.g., [26–36]). Some of these simulators use simplified piecewise-linear models (e.g., [31, 37, 38]). A method for fast time-domain simulation of networks with switches has been reported [38]. It is based on a discrete-time switch model that consists of a constant conductance in parallel with a current source. The system matrix is constant, independently of the states of the switches. These simulators are much faster than the standard simulators like SPICE (because no iterations over nonlinearities are needed), but at the expense of losing details (e.g., during switching events). The simulators PETS [36] and PECS [30], which support piecewise-linear models, also contain nonlinear elements. The simulator PETS supports smooth nonlinear models using a "delay" approximation [36]. (It is a not iterative method and is presumed faster than but not as accurate as the standard Newton–Raphson method [30]). In contrast to the simulator PECS, nonlinear elements are modeled as equivalent voltage and current sources (updated at every time step and for every nonlinear iteration). The entire circuit is modeled as these equivalent sources connected to a linear time-invariant system during each switching interval. An iterative Newton–Raphson method is used to achieve convergence to high accuracy [30]. Algorithms for solving piecewise-linear networks can be found in [39–46].

Further distinction may be made based on the formulation of the circuit equations: some simulators use state-space equations (SSE) (e.g., [26, 27, 29–34, 45, 47–49]) while others use nodal equations (NE) (e.g., [28, 50]), or modified nodal equations (MNE) (e.g., [6, 36, 51]). The advantage of the state-space equations in contrast to NE or MNE is that an analytic solution, as described in (1.26), exists. The disadvantage is the additional effort needed for generating the state-space equation from the circuit description.

Furthermore, symbolic simulators like ISAAC [52], SAPWIN [53, 54] and Analog Insyde [51] exist. (In the tutorial [55], the basic principles and the scope of application for symbolic computation have been reviewed.) These simulators do not support fully analytic time-domain transient analysis for switched networks with piecewise-linear models. The simulator for integrated switched-mode power supplies circuits (SISMPSC) [26] is based on symbolic calculus tools and supports symbolic

state-space equations (SSSE) but uses numerical methods for solving the systems of ordinary differential equations (ODEs). Analog Insyde is essentially restricted to symbolically-solved linear circuits using the Laplace transform [51]. A method for the simulation of electronic circuits by state variables decoupling (SECSVD) [45] supports analytic closed-form solutions for restricted input excitation functions, but does not support SSSE.

For modeling power electronics systems PLECS [27,56] or GeckoCIRCUITS [28] are frequently used, both of which have their origin at ETH Zurich. Further power electronics simulation tools are available such as Saber [3], Simplorer [4], Portunus [57] and PSIM [58]. Saber and Simplorer are integrated environments for designing and analyzing complex power electronic systems and multi-domain physical systems. Portunus is a system simulator whose applications range from the simulation of drive systems and switched mode power supplies to investigation of the heating of electronic components. PSIM is one of the fastest simulators for power electronics simulation. All these simulators use numerical integration for solving the systems of differential equations. Further interesting references in the context of power electronics modeling can be found in [46, 59–66].

The most important characteristics of time-domains simulators are summarized in Table 2.1. The proposed analytic forward solver approach closes the gap between symbolic simulators which do not fully support analytic time-domain transient analysis for switched networks with piecewise-linear models on the one hand, and the none symbolic simulators based on the switched networks with piecewise-linear models which support analytic time-domain transient analysis (summarized in Table 2.1) on the other hand.

Table 2.1: Comparison of time-domain simulators.

Examples	SPICE [6]	SISMPSC [26]	PLECS [27]	Gecko-CIRCUITS [50]	PECS [30]	PETS [36]	Analog Insyde [51]	SWANN [67]	SECSVD [45]	Proposed method
Formulation	MNE	SSSE	SSE	NE	SSE	MNE	MNE	MNE	SSE	ESSSE
Piecewise-linear modeling	no	yes	yes	yes	yes	yes	no	yes	yes	yes
Analytic solution	no	no	no	no	partly	no	only linear circuits	no	only restricted input excitation functions	yes

2.1 Method overview

The proposed approach is based on Maple [68], a computer algebra system (CAS). For the elemental circuit description, it uses a special Circuit-Model instead of the widely used netlist as, for example, used in SPICE, Analog Insyde, PECS [30, 69] and SWANN [67]. A Circuit-Model describes the electronic circuit with symbolic ordinary differential equations, if state variables are present. In the case of no state variables, the electronic circuit is described by symbolic algebraic equations. The electronic circuit to be simulated may contain linear and nonlinear components. Linear parts are described directly with a SubCircuit-Model and nonlinear ones with a Circuit-Model which comprises several SubCircuit-Models itself, the associated boundary conditions and a state table. The proposed approach uses SubCircuit-Models for piecewise-linear components. A SubCircuit-Model is an extended symbolic state-space model (ESSSM) in which the SSSM is extended by an I/O interface[2] and some additional information. An example of a SubCircuit-Model is provided in Figure 2.1. The associated ESSSM is described by (2.1)–(2.3). Eq. (2.1) represents the

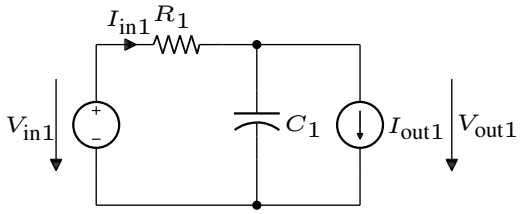

Figure 2.1: SubCircuit-Model: simple RC-circuit.

ordinary differential equation, (2.2) the signal of interest and (2.3) the I/O interface.

$$C_1 \frac{\mathrm{d}V_{C1}(t)}{\mathrm{d}t} = \frac{V_{in1} - V_{C1}(t)}{R_1} - I_{out1} \tag{2.1}$$

$$\mathbf{y_1}(t) = V_{C1}(t) \tag{2.2}$$

I/O interface:

$$\mathbf{y}_{IO1}(t) = \begin{bmatrix} \mathbf{y}_{I1}(t) \\ \mathbf{y}_{O1}(t) \end{bmatrix} \quad \text{with} \quad \mathbf{y}_{I1}(t) = \begin{bmatrix} \frac{V_{in1} - V_{C1}(t)}{R_1} \\ V_{in1} \end{bmatrix} \quad \mathbf{y}_{O1}(t) = \begin{bmatrix} I_{out1} \\ V_{C1}(t) \end{bmatrix} \tag{2.3}$$

A second example of a SubCircuit-Model, without state variables, is shown in Figure 2.2. In case of no state variables, only (2.4), the signal of interest, and (2.5),

[2] The I/O interface is described in Section 2.2.2.

the I/O interface exist. In this example, the output-cell $\mathbf{y}_{O2}(t)$ of the I/O interface is not defined.

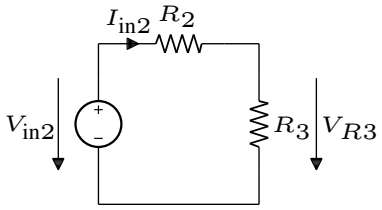

Figure 2.2: SubCircuit-Model: simple voltage divider.

$$\mathbf{y}_2(t) = V_{R3} = V_{in2}\frac{R_3}{R_2 + R_3} \tag{2.4}$$

I/O interface:

$$\mathbf{y}_{IO2}(t) = \begin{bmatrix} \mathbf{y}_{I2}(t) \\ \mathbf{y}_{O2}(t) \end{bmatrix} \quad \text{with} \quad \mathbf{y}_{I2}(t) = \begin{bmatrix} \frac{V_{in2}}{R_2+R_3} \\ V_{in2} \end{bmatrix} \quad \mathbf{y}_{O2}(t) = \begin{bmatrix} \end{bmatrix} \tag{2.5}$$

A collection of predefined SubCircuit-Models is provided. Connecting such simple predefined SubCircuit-Models results in a new SubCircuit-Model and is visualized in Figure 2.3. This results in a large number of possible SubCircuit-Models. As mentioned in the introduction in Section 1.2, the approach allows the electronic circuits from SubCircuit-Models to be simulated without the transformation to a state-space model; only the I/O definitions must be substituted, as shown in more detail in Section 2.2.2. This results in a quasi combination of the compact representation of the state-space equations already available and the immediate further use of the modified nodal equations. From the electronic circuit to be simulated, the

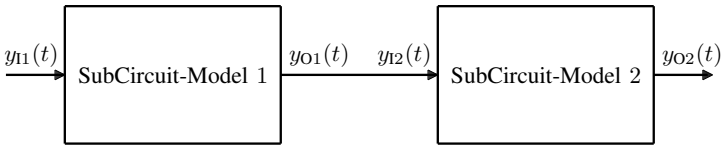

Figure 2.3: Interconnection of two SubCircuit-Models.

final Circuit-Model is only built once and saved. The final Circuit-Model and its analytic solution can be saved, which is especially interesting for parameter studies of small-scale electronic circuits.

The time-domain transient analysis for a Circuit-Model starts at the first SubCircuit-Model, then, the boundary conditions for this SubCircuit-Model are verified. The fulfilled boundary condition determines the next SubCircuit-Model and the analytic solution for that time interval. This is repeated until the final circuit operating time to be simulated, referred to below as simulation time t_{Sim}, is reached.

2.2 Proposed SubCircuit-Model of an electronic circuit

2.2.1 General form of a SubCircuit-Model

A SubCircuit-Model contains only linear elements R, C, L, and independent current and voltage sources, respectively. The general form of the SubCircuit-Model is described by (2.6)–(2.8).

$$\mathbf{Z}\dot{\mathbf{x}}(t) = \mathbf{A}\mathbf{x}(t) + \mathbf{B}\mathbf{u}(t) \tag{2.6}$$

$$\mathbf{y}(t) = \mathbf{f}_{\mathrm{C}}(\mathbf{x}(t)) + \mathbf{f}_{\mathrm{D}}(\mathbf{u}(t)) + \mathbf{E}\mathbf{Z}\dot{\mathbf{x}}(t) \tag{2.7}$$

I/O interface:

$$\mathbf{y}_{\mathrm{IO}}(t) = \mathbf{C}_{\mathrm{IO}}\mathbf{x}(t) + \mathbf{D}_{\mathrm{IO}}\mathbf{u}(t) + \mathbf{E}\mathbf{Z}\dot{\mathbf{x}}(t) \tag{2.8}$$

where

$\mathbf{A}$	state matrix
$\mathbf{B}$	input matrix
$\mathbf{Z}$	constant coefficient diagonal matrix of the first order derivative of the state variables
$\mathbf{x}(t)$	column vector of state variables
$\dot{\mathbf{x}}(t)$	column vector of first order derivative of the state variables
$\mathbf{u}(t)$	column vector of the input
$\mathbf{y}(t)$	column vector of the output signals (voltages, currents, powers etc.) of interest
$\mathbf{f}_{\mathrm{C}}$	output function column vector
$\mathbf{f}_{\mathrm{D}}$	feedforward function column vector
$\mathbf{E}$	constant first order derivative matrix
$\mathbf{y}_{\mathrm{IO}}(t)$	column vector of the I/O interface
$\mathbf{C}_{\mathrm{IO}}$	I/O interface output matrix
$\mathbf{D}_{\mathrm{IO}}$	I/O interface feedforward matrix

Eq. (2.6) represents the system of differential (state) equations. The state variables are the solution to this system. To obtain the signals of interest, (2.7) is used. The signals can be voltages, currents, powers, etc. To expand the SubCircuit-Model with other SubCircuit-Models, an I/O interface is required, (2.8). The references (symbolic values) of the capacitances and inductances of the SubCircuit-Model are summarized in matrix $\mathbf{Z}$. For example, in the case of a capacitor, the left side of (2.6) represents the current flowing through the capacitor, and in case of an inductor, it is the voltage across the inductor.

The desired output variables in (2.7) are composed of three parts. The first part represents the dependency on the state variables, the second shows the input of independent sources and the third stands for the derivative of the state variables. In contrast to (2.7), (2.8) may only contain linear combinations (to obtain a new system of linear ordinary differential equations). The two functions $\mathbf{f}_\mathrm{C}(\mathbf{x}(t))$ and $\mathbf{f}_\mathrm{D}(\mathbf{u}(t))$ describe the contributions of the state and input variables. They can be chosen arbitrarily and do not need to be constant. To minimize the computational costs, the derivations in (2.7) and (2.8) are substituted by the right side of (2.6).

2.2.2 Interconnection of SubCircuit-Models

The I/O interface of a SubCircuit-Model consists of inputs and outputs. The number of inputs and outputs is not limited. An input is connected to an output or vice versa. The construction of an input-cell $\mathbf{y}_\mathrm{I}(t)$ and output-cell $\mathbf{y}_\mathrm{O}(t)$ is illustrated in

$$\mathbf{y}_\mathrm{I}(t) = \begin{bmatrix} I_\mathrm{in}(V_\mathrm{in}, t) \\ V_\mathrm{in} \end{bmatrix} \qquad \mathbf{y}_\mathrm{O}(t) = \begin{bmatrix} I_\mathrm{out} \\ V_\mathrm{out}(I_\mathrm{out}, t) \end{bmatrix}. \tag{2.9}$$

Connecting an input to an output means that the output current I_out1 of the first SubCircuit-Model 1 is replaced by the input current of the connected SubCircuit-Model 2 $I_\mathrm{in2}(V_\mathrm{in2}, t)$ and the input voltage V_in2 is substituted by the output voltages $V_\mathrm{out1}(I_\mathrm{out1}, t)$.

$$I_\mathrm{out1} = I_\mathrm{in2}(V_\mathrm{in2}, t) \tag{2.10}$$

$$V_\mathrm{in2} = V_\mathrm{out1}(I_\mathrm{out1}, t) \tag{2.11}$$

This results in a system of linear equations, (2.10) and (2.11), with two unknowns I_out1 and V_in2. The solution of both variables is substituted in the general equations (2.6)–(2.8) of both SubCircuit-Models. The substituted SubCircuit-Models together

join the new SubCircuit-Model. Figure 2.4 shows an example for the interconnected SubCircuit-Model that connects the SubCircuit-Models shown in Figure 2.1 and Figure 2.2. The associated ESSSM is described by (2.12)–(2.14).

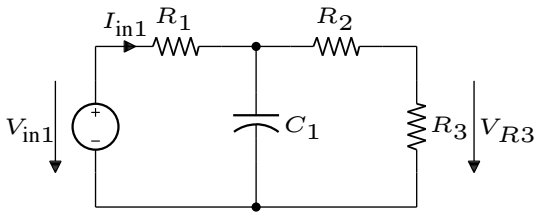

Figure 2.4: Interconnected SubCircuit-Model, connecting the SubCircuit-Models shown in Figure 2.1 and Figure 2.2.

$$C_1 \frac{\mathrm{d}V_{C1}(t)}{\mathrm{d}t} = \frac{V_{in1} - V_{C1}(t)}{R_1} - \frac{V_{C1}(t)}{R_2 + R_3} \tag{2.12}$$

$$\mathbf{y}(t) = V_{R3} = V_{C1}(t)\frac{R_3}{R_2 + R_3} \tag{2.13}$$

I/O interface:

$$\mathbf{y}_{IO}(t) = \begin{bmatrix} \mathbf{y}_I(t) \\ \mathbf{y}_O(t) \end{bmatrix} \quad \text{with} \quad \mathbf{y}_I(t) = \begin{bmatrix} \frac{V_{in1} - V_{C1}(t)}{R_1} \\ V_{in1} \end{bmatrix} \quad \mathbf{y}_O(t) = \begin{bmatrix} \ \end{bmatrix} \tag{2.14}$$

2.2.3 Additional information of a SubCircuit-Model

The additional information is the solver option for the ordinary differential equations (ODEs), for example, series or Laplace (standard method). Optional information can be the solution of the ODE system in symbolic form, especially for small-scale electronic circuits.

2.3 Circuit-Model of an electronic circuit

2.3.1 General form of a Circuit-Model

Nonlinear elements such as $L(i)$, $C(u)$, Diodes, MOSFETs, BJTs, and/or PWM controllers are described by a Circuit-Model. In general, these elements can be described by piece-wise linear models (piecewise-linear functions), and must be linearized first, using, e.g., (2.15) at N points.

Linearization at N points x_i with $i = 1, \ldots, N$, $N > 2$ and the interval $I_i = \frac{x_i + x_{i+1}}{2}$:

$$f_{\text{lin}}(x) = \begin{cases} f(x_1) + \left.\frac{\mathrm{d}f(x)}{\mathrm{d}x}\right|_{x=x_1} (x - x_1), & x < I_1 \\ f(x_2) + \left.\frac{\mathrm{d}f(x)}{\mathrm{d}x}\right|_{x=x_2} (x - x_2), & I_1 \leq x < I_2 \\ \vdots & \\ f(x_N) + \left.\frac{\mathrm{d}f(x)}{\mathrm{d}x}\right|_{x=x_N} (x - x_N), & x \geq I_{N-1} \end{cases} \tag{2.15}$$

To solve the differential equation system analytically, it must consist of linear ordinary differential equations. To make this possible, the original problem described in (2.15) must be modified to piecewise-constant functions, as in (2.16). This can be obtained by setting $\frac{\mathrm{d}f(x)}{\mathrm{d}x} = 0$.

$$f_{\text{const}}(x) = \begin{cases} f(x_1), & x < I_1 \\ f(x_2), & I_1 \leq x < I_2 \\ \vdots & \\ f(x_N), & x \geq I_{N-1} \end{cases} \tag{2.16}$$

2.3.2 Boundary conditions of the Circuit-Model

A Circuit-Model consists of N SubCircuit-Models (states) with $i = 1, \ldots, N$. Each SubCircuit-Model is only valid within a specific interval (2.16). Furthermore, it may be valid only for a certain time-interval, e.g., a certain pulse-width. Therefore, boundary conditions for each SubCircuit-Model are required.

Three different boundary conditions are distinguished from one another:

- initial condition BC_{IC} is met: $g_1(0)$ $<, \leq, \geq, >$ $g_2(0)$
- time BC_t limit is reached: $t \geq t_{\text{limit}}$
- equation BC_{Eqn} is met: $g_1(t) = g_2(t)$

If one of these conditions is met, the actual state i becomes invalid.

2.3.3 State control of the Circuit-Model

For the state control, a state table is used. The i-th SubCircuit-Model has at least $N_{\text{BC}i}$ boundary conditions with $j = 0, \ldots, N_{\text{BC}i}$. The state table has two inputs: the

first one represents the number of the state i, and the second one, the number of boundary condition j. An example for a state diagram including the state table is shown in Figure 2.5.

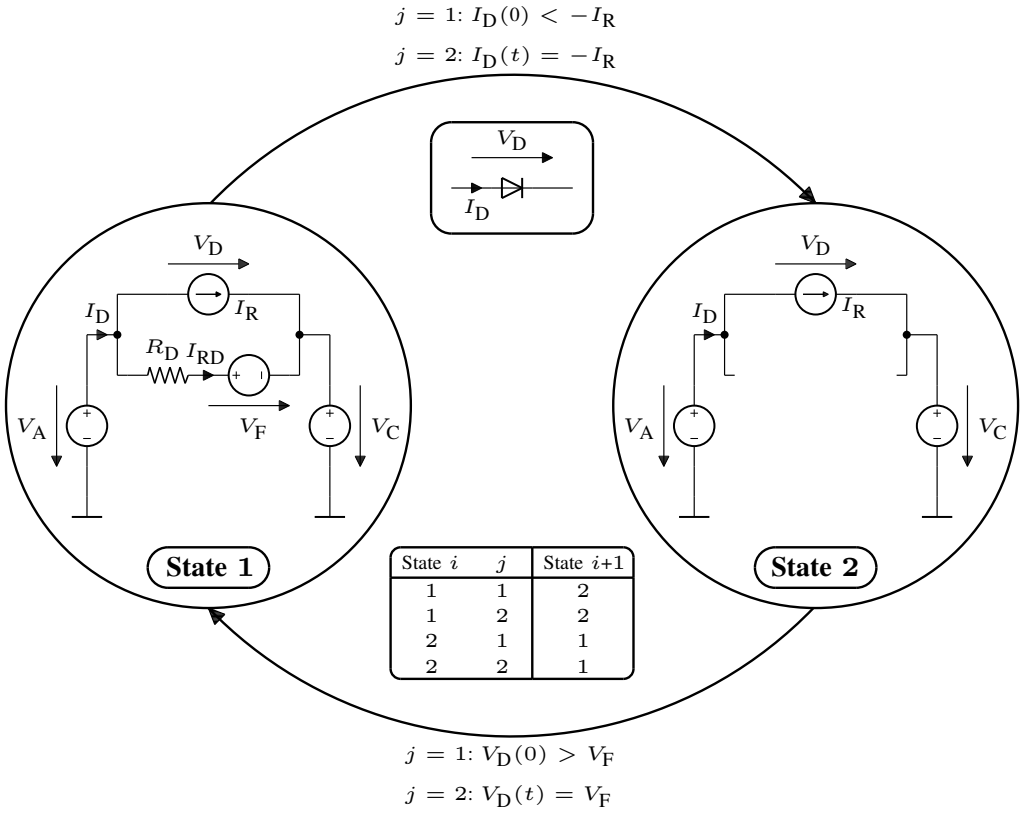

Figure 2.5: Diode state diagram.

2.3.4 Interconnection of Circuit-Models

Two Circuit-Models are interconnected at SubCircuit-Model level:

Circuit-Model 1:

N SubCircuit-Models with $i = 1, \ldots, N$ states and $j = 0, \ldots, N_{BCi}$ boundary conditions

Circuit-Model 2:

M SubCircuit-Models with $k = 1, \ldots, M$ states and $l = 0, \ldots, N_{BCk}$ boundary conditions

Interconnected Circuit-Model 1-2:
$N \times M$ SubCircuit-Models with $m = 1, \ldots, N \times M$ states and $n = 0, \ldots, N_{\mathrm{BC}m}$ boundary conditions

The interconnected Circuit-Model 1-2 has $N \times M$ new states. Each newly generated SubCircuit-Model m has $N_{\mathrm{BC}i}$ boundary conditions from the SubCircuit-Model i and $N_{\mathrm{BC}k}$ from the SubCircuit-Model k. For each state m, the entries for the new state table are computed from the state tables of Circuit-Model 1 and Circuit-Model 2.

2.4 Transient analysis

The flowchart for the transient analysis is shown in Figure 2.6. Before the simulation can start, the initialized state i and the initial conditions $\mathbf{x}(0)$ for the state variables must be defined.

2.4.1 ODE system solver module

The module "Solve ODEs" generally solves the ODE system from the SubCircuit-Model i (2.6). The proposed approach uses the built-in ODE solver from Maple. Out of the different solver methods and options available, the proposed approach uses the Laplace method. When the ODE system from the SubCircuit-Model i has been solved once, the solution is stored and, therefore, a further solving of the ODE system is no longer necessary for this state i. The analytic solution of the ODE System (2.12) from the interconnected SubCircuit-Model in Section 2.2.2 is shown in symbolic form (2.17).

$$V_{\mathrm{C1}}(t) = \left(V_{\mathrm{C1}}(0) - V_{\mathrm{in1}} \frac{R_2 + R_3}{R_1 + R_2 + R_3}\right) \mathrm{e}^{-\frac{(R_1+R_2+R_3)\,t}{C_1 R_1 (R_2+R_3)}} + V_{\mathrm{in1}} \frac{R_2 + R_3}{R_1 + R_2 + R_3} \tag{2.17}$$

2.4.2 Boundary condition module

For the verification of boundary conditions from the SubCircuit-Model i, the module "Verify Boundary Conditions" is needed. It returns the time Δt at which the state is no longer valid, as well as the appropriate boundary condition reference.

This module fulfills three different tasks:

- evaluation of the initial conditions $\mathrm{BC}_{\mathrm{IC}j}$ with
  $j = 0, \ldots, N_{\mathrm{IC}}$

- test if a time limit is reached with BC_{tk} with
  $k = 0, \ldots, N_t$

- evaluation of the smallest time $t > 0$ from the solution set of the equations $\mathrm{BC}_{\mathrm{Eqn}l}$, where t is the unknown with
  $l = 0, \ldots, N_{\mathrm{Eqn}}$
  Several solver algorithms are possible; the default is a modified one-dimensional Newton–Raphson method, (2.18), to find the solution of $g(t) = 0$.

$$t_{n+1} = t_n - \frac{g(t_n)}{\dot{g}(t_n)} \tag{2.18}$$

  Here, the time interval under investigation is divided into subintervals and evaluated at the beginning of each subinterval. Subsequently, the signs of successive function values are compared. If they differ, the smaller value is used as the initial guess for the Newton–Raphson method. The time step for the subintervals is estimated from the (complex) eigenvalues of the state matrix $\mathbf{A}$ (e.g., [59, 70]) and the input vector $\mathbf{u}(t)$. The eigenvalues do not need to be calculated explicitly, instead, the period lengths from the analytic solution of $\mathrm{BC}_{\mathrm{Eqn}l}$ are used from the sine and cosine terms. The lowest period is divided by an additional factor of at least 2 and is used as the time step of the subintervals. In the case of no sine and cosine terms, no subintervals exist.

2.4.3 Initial condition module

The module "Calculate Initial Conditions" is responsible for determining the initial conditions, $\mathbf{x}(0)$, for the next SubCircuit-Model. To this end, the solutions of the state variables from SubCircuit-Model i, $\mathbf{x}_\mathrm{i}(\Delta t)$, are evaluated.

2.4.4 Signal module

The module "Add signals" saves the shapes of the output signals (2.7) with the initial conditions $\mathbf{x}(0) = \mathbf{x}(t_{\mathrm{Sim}})$ in vector **Signal** in analytic form and the time interval $t_{\mathrm{Sim}} \leq t < t_{\mathrm{Sim}} + \Delta t$ in vector **Time**.

2.4.5 State module

At this point, the next state is determined by the module "Get new State" as a function of Δt and the boundary condition reference. The simulation time t_{Sim} is incremented by Δt.

Next, the sequence (Sections 2.4.1 to 2.4.5) is repeated until $t_{\text{Sim}} \geq t_{\text{End}}$.

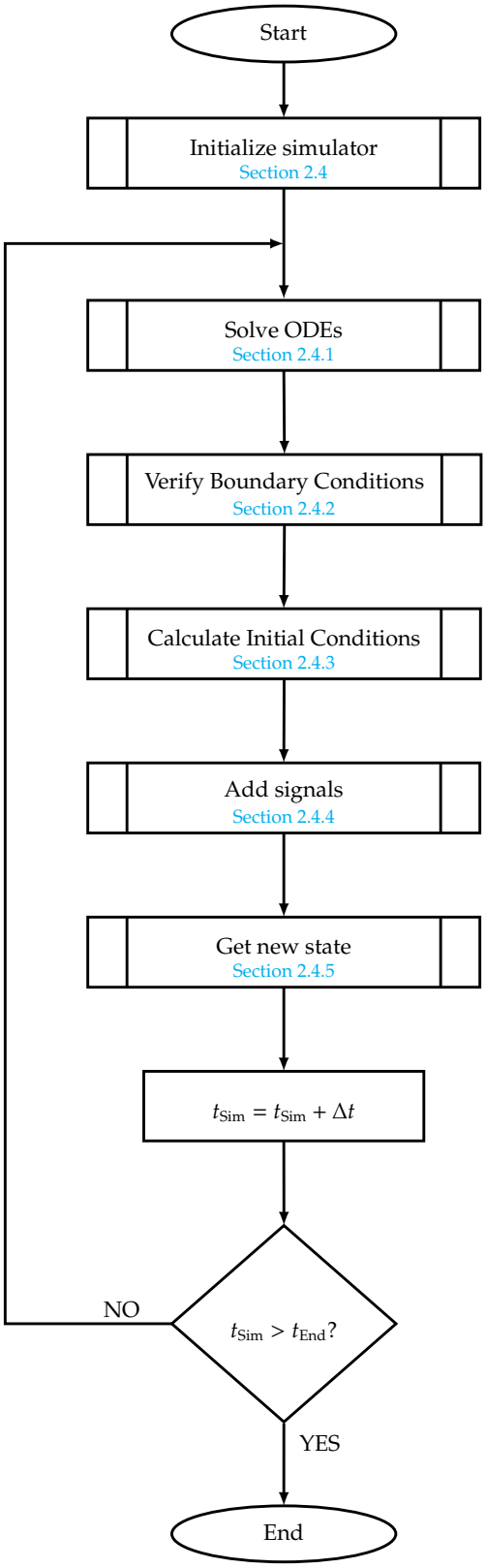

Figure 2.6: Flowchart for transient analysis.

2.5 Optimization and worst-case analysis of electronic circuits

Electronic components always come with certain tolerances; therefore, the worst-case sizing[3] of the electronic circuits composed of such components has been gaining more and more in importance. Some simulators (e.g., LTspice [1] and PSpice [2]) offer the possibility for a Monte Carlo (MC) analysis. This stochastic analysis provides statistical data on the impact of a device parameter's variance. A major disadvantage of such stochastic methods is that they require a high number of simulation runs to reach the device's design limits or the design limits of the individual components. Other simulators (e.g., Saber [3] and Simplorer [4]) provide numerical optimization methods to perform a worst-case analysis. Here also, several simulation runs are required to reach the device's design limits or the design limits of the individual components. This can be advantageously improved by computing currents and voltages analytically. The proposed approach allows for conducting a full search over the parameter space. This, in turn, provides the possibility of worst-case analyses of the different parameters of interest. Additionally, it allows for full flexibility in modeling the individual components and their parameters. Furthermore, simulation results are extremely compact and can theoretically be stored with arbitrary precision. Finally, the objective function $f(\mathbf{x})$ needed for any optimizer is available in an analytic form.

2.5.1 SQP approach

The implemented SQP method (2.19) is based on an active set strategy with linear inequality constraints (2.20) [71].

$$\min_{\mathbf{x}\in\mathbf{R}^n} \quad f(\mathbf{x}) = \frac{1}{2}\mathbf{x}^\mathsf{T}\mathbf{G}\mathbf{x} + \mathbf{g}^\mathsf{T}\mathbf{x} \tag{2.19}$$

$$\text{subject to} \quad \mathbf{A}\mathbf{x} \geq \mathbf{b} \tag{2.20}$$

where

[3] Described in Section 1.1.

$\mathbf{x}$	column vector of the device parameters
$f(\mathbf{x})$	objective function
$\mathbf{G}$	Hessian matrix of the objective function
$\mathbf{g}$	gradient of the objective function
$\mathbf{A}$	constant $m \times n$ matrix
$\mathbf{b}$	constant column vector $\mathbf{b} \in \mathbf{R}^m$
n	number of parameters
m	number of constraints

The optimization process (procedure) starts at an initial feasible point $\mathbf{x}^{(0)}$ and is used as the basis of an iterative process. The Hessian matrix $\mathbf{G}$ is updated in each iteration step until the optimal solution is found. This sequence of feasible solutions for each iteration step $\mathbf{x}^{(k+1)}$ (2.21) converges at the solution with $\mathbf{p}^{(k)}$, the search directions supplied by the optimization method (constrained or unconstrained) used by the SQP method.[4]

$$\mathbf{x}^{(k+1)} = \mathbf{x}^{(k)} + \mathbf{p}^{(k)} \tag{2.21}$$

The state of the constraints (being active or inactive) defines the optimization method for the next iteration step. A constraint is active if $\mathbf{a}_i^\mathsf{T}\mathbf{x}^{(k)} = b_i$ and inactive if $\mathbf{a}_i^\mathsf{T}\mathbf{x}^{(k)} > b_i$. In case of active constraints, the problem is transformed into an easier subproblem or reduced problem, an active constraints matrix $\mathbf{A}_t$ (index t marked as active set) is introduced and is composed of $\mathbf{a}_i^\mathsf{T}$ from the active constraints which is explained in Section 2.5.2. The unconstrained case with no active constraints is described in Section 2.5.3. The iteration step is completed by the feasibility check. The search direction in (2.21) is multiplied by $\alpha^{(k)}$ (2.22) [71], the distance to the inactive constraints boundaries (for all inequalitys $\mathbf{a}_i^\mathsf{T}\mathbf{p}^{(k)} < 0 \ldots$ descent direction) in any direction $\mathbf{p}^{(k)}$ (2.23).[5]

$$\alpha^{(k)} = \min_{\mathbf{a}_i^\mathsf{T}\mathbf{p}^{(k)}<0} \left(1, \frac{b_i - \mathbf{a}_i^\mathsf{T}\mathbf{x}^{(k)}}{\mathbf{a}_i^\mathsf{T}\mathbf{p}^{(k)}}\right), \quad i \notin t \tag{2.22}$$

When inactive constraints are hit, then $\alpha^{(k)} < 1$.

$$\mathbf{x}^{(k+1)} = \mathbf{x}^{(k)} + \alpha^{(k)}\mathbf{p}^{(k)} \tag{2.23}$$

To apply an SQP strategy, the objective function $f(\mathbf{x})$ must be defined, for example, the inductor current (4.2) shown in Figure 4.1. The SQP strategy generally identifies

[4] The search directions $\mathbf{p}^{(k)}$ describe the direction in which the iteration step $\mathbf{x}^{(k+1)}$ is updated.
[5] $\alpha^{(k)}$ scales (limits) $\mathbf{p}^{(k)}$ to the minimum distance to the inactive constraints' boundaries.

the minimum of the objective function $f(\mathbf{x})$, in case of the maximum, $-f(\mathbf{x})$ must be used instead. The inequality constraints (2.20) are constructed at least from the device parameter bounds. In case of n device parameters, it is $m = 2n$. The general form of (2.20) in matrix form is described in (2.24).

$$\begin{bmatrix} 1 & 0 & \cdots & 0 \\ -1 & 0 & \cdots & 0 \\ \vdots & & \ddots & \vdots \\ 0 & 0 & \cdots & 1 \\ 0 & 0 & \cdots & -1 \end{bmatrix} \begin{bmatrix} x_1 \\ x_1 \\ \vdots \\ x_n \\ x_n \end{bmatrix} \geq \begin{bmatrix} x_{1\,\min} \\ -x_{1\,\max} \\ \vdots \\ x_{n\,\min} \\ -x_{n\,\max} \end{bmatrix} \tag{2.24}$$

2.5.2 SQP iteration in case of active constraints

The Lagrange multipliers (2.25) [71] are necessary to identify the (final) active constraints for each iteration. If any component λ_i of $\boldsymbol{\lambda}_t^{(k)}$ is negative, then this active constraint $\mathbf{a}_i^\mathsf{T}$ does not remain active and is deleted from $\mathbf{A}_t$. On the other hand, if the projected gradient $\mathbf{Z}_t^\mathsf{T}\mathbf{g}^{(k)} = \mathbf{0}$ and all elements of $\boldsymbol{\lambda}_t^{(k)}$ are ≥ 0, then, the optimal solution is found at $\mathbf{x}^{(k+1)} = \mathbf{x}^{(k)}$.

$$\boldsymbol{\lambda}_t = \mathbf{Y}_t^\mathsf{T}\mathbf{g} \tag{2.25}$$

The search direction $\mathbf{p}_z$ for the reduced problem is given by (2.26) [71].

$$\mathbf{p}_z = -(\mathbf{Z}_t^\mathsf{T}\mathbf{G}\mathbf{Z}_t)^{-1}\mathbf{Z}_t^\mathsf{T}\mathbf{g} \tag{2.26}$$

The search direction of the original problem is defined by

$$\mathbf{p} = \mathbf{Z}\mathbf{p}_z\,. \tag{2.27}$$

The required matrices $\mathbf{Y}_t$ and $\mathbf{Z}_t$ are obtained by a QR factorization of the matrix $\mathbf{A}_t^\mathsf{T}$ (2.28) [71].

$$\mathbf{A}_t^\mathsf{T} = \mathbf{Q}\begin{bmatrix}\mathbf{R}\\ \mathbf{0}\end{bmatrix} = \begin{bmatrix}\mathbf{Q}_1\mathbf{Q}_2\end{bmatrix}\begin{bmatrix}\mathbf{R}\\ \mathbf{0}\end{bmatrix} = \mathbf{Q}_1\mathbf{R} \tag{2.28}$$

The matrix $\mathbf{Q}$ is $n \times n$ and orthogonal, the matrix $\mathbf{R}$ is $m_\mathrm{a} \times m_\mathrm{a}$ (m_a ...#active constraints) and upper triangular. The matrices $\mathbf{Q}_1$ and $\mathbf{Q}_2$ are $n \times m_\mathrm{a}$ and $n \times (n - m_\mathrm{a})$ respectively. The matrices $\mathbf{Y}_t$ and $\mathbf{Z}_t$ are then obtained by (2.29) and (2.30), respectively [71].

$$\mathbf{Y}_t = \mathbf{Q}_1\mathbf{R}^{-\mathsf{T}} \tag{2.29}$$

$$\mathbf{Z}_t = \mathbf{Q}_2 \tag{2.30}$$

2.5.3 SQP iteration in case of no active constraints

In case of no active constraints, the quasi-Newton method [71] is used to provide the search direction

$$\mathbf{p} = -\mathbf{H}\mathbf{g}\,. \tag{2.31}$$

The matrix $\mathbf{H}$ is the inverse of the Hessian matrix and is update at each iteration step. A line search is performed to find the parameter $\alpha_{\min}$ (the distance to the minimum) along the search direction $\mathbf{p}$ (2.32).

$$\alpha_{\min} = \min_{\alpha} f(\mathbf{x}^{(k)} + \alpha\mathbf{p}) \tag{2.32}$$

The final search direction is obtained by using $\alpha_{\min}$ in (2.31)

$$\mathbf{p} = -\alpha_{\min}\mathbf{H}\mathbf{g}\,. \tag{2.33}$$

2.5.4 SQP method inverse Hessian update

A large number of Hessian updating methods have been developed. Several algorithms are possible; the default is the widely used BFGS update formula (2.34) which is characterized by its fast convergence, and which was introduced by Broyden, Fletcher, Goldfarb and Shanno [71].

$$\mathbf{H}^{(k+1)} = \mathbf{H}^{(k)} + \left(\mathbf{I} + \frac{\gamma^{\mathsf{T}}\mathbf{H}^{(k)}\gamma}{\delta^{\mathsf{T}}\gamma}\right)\frac{\delta\delta^{\mathsf{T}}}{\delta^{\mathsf{T}}\gamma} - \left(\frac{\delta\gamma^{\mathsf{T}}\mathbf{H}^{(k)} + \mathbf{H}^{(k)}\gamma\delta^{\mathsf{T}}}{\delta^{\mathsf{T}}\gamma}\right)$$

where

$$\delta = \mathbf{x}^{(k+1)} - \mathbf{x}^{(k)}$$
$$\gamma = \mathbf{g}^{(k+1)} - \mathbf{g}^{(k)} \tag{2.34}$$

The matrix $\mathbf{H}$ must be positive definite otherwise the search direction $\mathbf{p}$ will not be a descent direction and $\mathbf{x}^{(k+1)}$ will not converge to the minimum (optimal) solution. In some cases, $\mathbf{H}$ will not be positive definite, in this case, the matrix $\mathbf{H}$ is reinitialized to the unit matrix $\mathbf{I}$ which is positive definite.

2.5.5 SQP implementation

The flowchart for the SQP method is shown in Figure 2.7. Before the optimization

starts, the inequality constraints must be constructed (2.20) (**A** and **b**) and an initial feasible point $\mathbf{x}^{(0)}$ must be defined. The initial feasible point $\mathbf{x}^{(0)}$ can be chosen arbitrary inside the parameters, boundary constraints and is set to e.g., the nominal values of the parameters. Then, the iteration is started. At each iteration, the applicability of the constraints is verified. Furthermore, the state of these constraints is determined, as this determines which search direction (reduced problem or quasi-newton) needs to be used. Before the evaluated search direction $\mathbf{p}$ is set to valid, a feasibility check (2.22) is carried out. Finally, the inverse Hessian matrix is updated and the new initial point $\mathbf{x}^{(k+1)}$ for the next iteration is calculated. The iteration process is repeated until one of the following three conditions is met:

- $\left\|\mathbf{Z}_t^{\mathsf{T}}\mathbf{g}^{(k)}\right\| < \epsilon$ and then all $\lambda_i > 0$; or
- $\left\|\mathbf{g}^{(k)}\right\| < \epsilon$; or
- the maximum number of iterations $k_{\max}$ is reached.

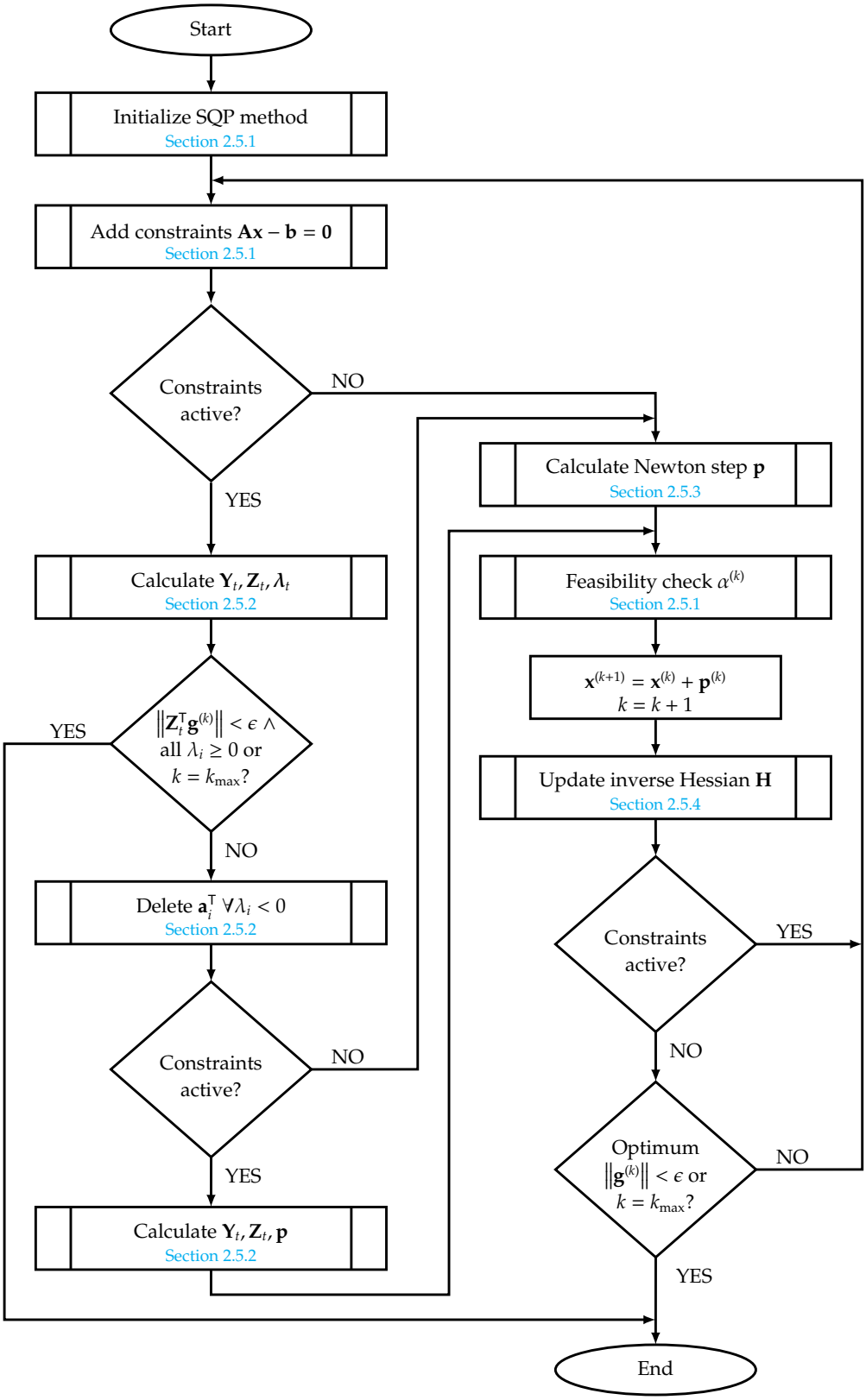

Figure 2.7: Flowchart for SQP method.

Chapter 3

Example cases and experimental validation of the analytic forward solver approach

3.1 Example case flyback converter

The performance of the proposed approach is demonstrated by simulating a flyback converter.[1] The simulation results obtained with the proposed method are compared to those obtained with PLECS [56] and GeckoCIRCUITS [28] as well as experimental ones. In all cases, the models, including the component values, and the initial conditions are identical. The prototype for experimental results is shown in Figure 3.1. First, open-loop steady-state behavior (Sections 3.1.1 and 3.2.1) is analyzed, where-

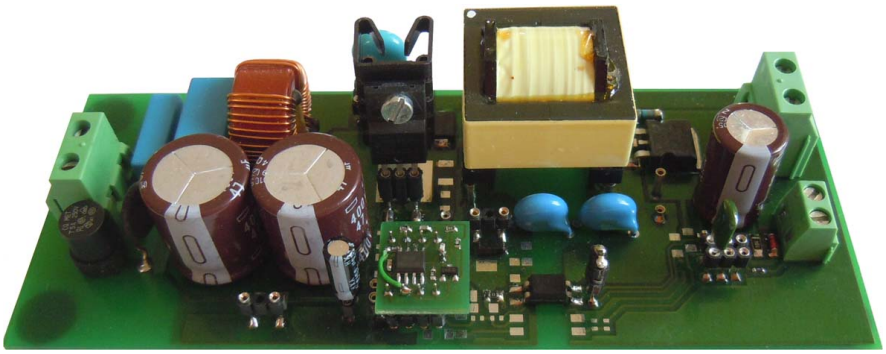

Figure 3.1: Flyback converter prototype.

[1] The choice of the flyback converter was motivated from other work outside of the scope of thesis. This choise of this converter allows illustrating everything that needs to be illustrated to show the performance of the proposed analytic forward solver approach.

after the closed-loop behavior during start-up (Sections 3.1.2 and 3.2.2) is assessed. The schematic diagram of the closed-loop flyback converter is shown in Figure 3.2 and is divided into three parts:

- Power stage: includes a real transformer with the magnetizing inductance L_M, an ideal transformer T_1 and parasitic elements, power switch Q_1, current sense resistor R_{Sense}, primary RCD snubber D_S, R_S, and C_S, the secondary rectifier D_1 and the output filter capacitor C_O. The power switch Q_1 is modeled as a voltage controlled ideal switch with two resistors $Q_{1\,RDS(on)}$ representing the resistance in the on-region and resistance $Q_{1\,RDS(off)}$ for the cut-off region.

- PWM controller: for the control method, peak current mode control with constant switching frequency is chosen and is implemented in the PWM controller block. A detailed structure of the PWM controller is shown in Figure 3.3.

- Compensator: a Type 2 compensator [72,73] is used. This type of compensator is usually reserved for current mode control compensation [72].

3.1.1 Open-loop flyback converter in steady-state

The circuit for the open-loop flyback converter is the same as in Figure 3.2, only without a compensator and with the FB pin left open. Table 3.1 summarizes the values of the components and parameters. Two resonant circuits are on the primary side of the flyback converter: the first one consisting of the leakage inductance L_{Leak} of the transformer and the output capacitance C_{OSS} of the MOSFET Q_1 and the second one consisting of the magnetizing inductance L_M of the transformer and the output capacitance C_{OSS}. To model the damping of these resonance circuits, two resistors R_C and R_{COSS} were added.[2] Since the output capacitance C_{OSS} of Q_1 is highly nonlinear, an approximated constant value for the effective output capacitance $C_{OSS(eff.)}$ from the datasheet of Q_1 is used.[3]

[2] The values of the resistors were determined by trying different resistor values until the damping of the oscillations from the simulation matched those from the measurement curves.

[3] C_{OSS} also includes the stray capacitance (e.g., from the printed circuit board and from the real transformer). This approximation does not affect the result, as shown in Figure 3.8.

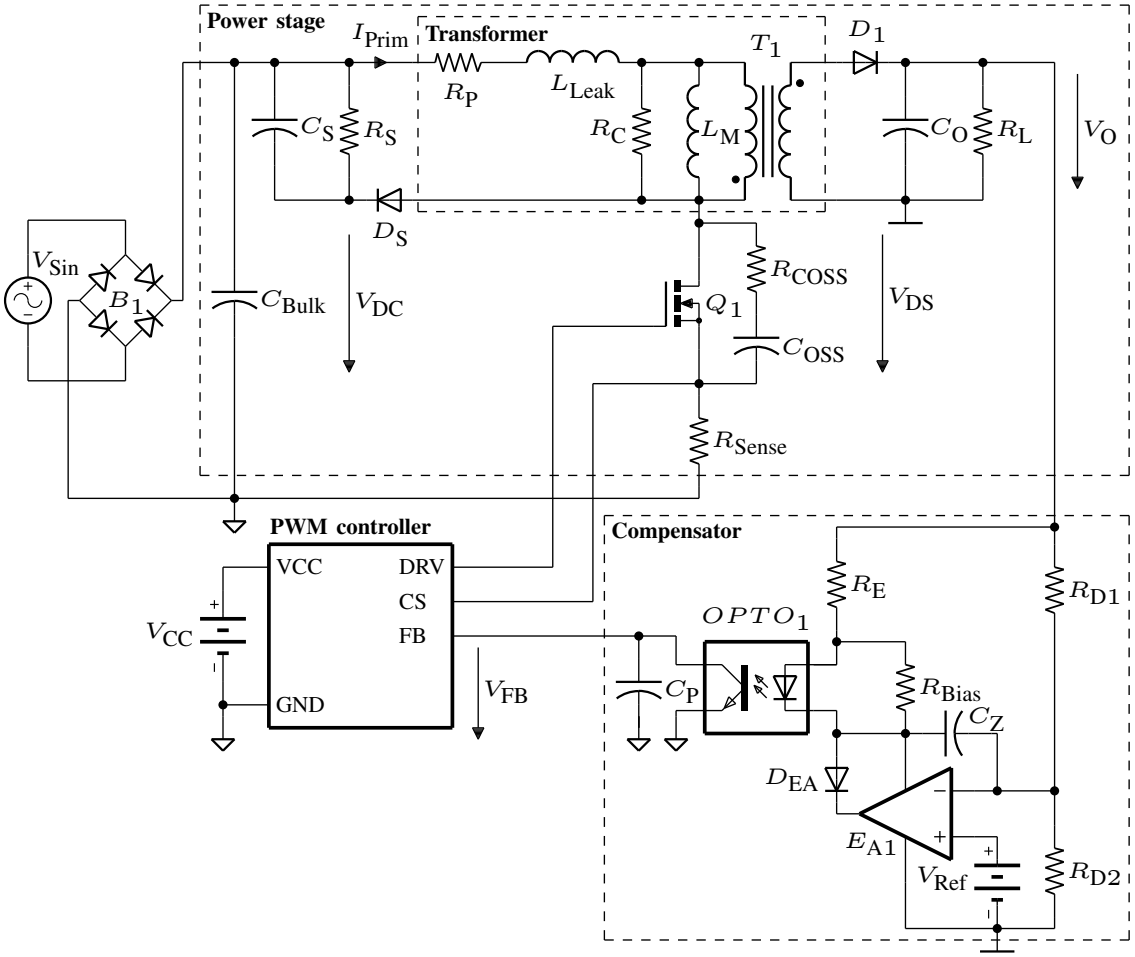

Figure 3.2: Schematic diagram of a closed-loop flyback converter with peak current mode control.

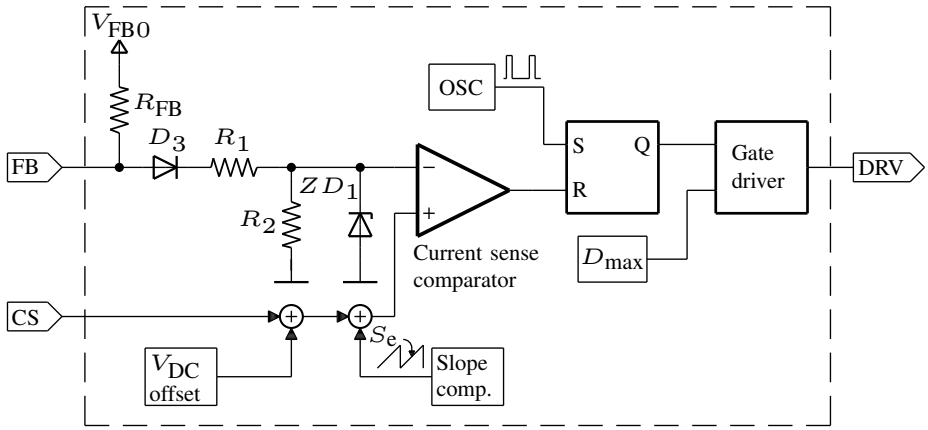

Figure 3.3: Block diagram of the peak current mode PWM controller.

Table 3.1: Component values and parameters for the open-loop flyback converter of Figure 3.2.

Power stage	PWM controller
$V_{DC} = 135\,V$	$F_S = 65\,kHz$
$R_S = 100\,k\Omega$, $C_S = 4.7\,nF$	$D_{max} = 0.31$
$D_{1\,VF} = 0.5\,V$, $D_{1\,RD} = 50\,m\Omega$	$S_e = 0.0203\,V/\mu s$
$D_{S\,VF} = 0.8\,V$, $D_{S\,RD} = 50\,m\Omega$	$V_{DC\,Offset} = 0.536\,V$
$R_P = 0.123\,\Omega$, $R_C = 20\,k\Omega$	$V_{FB0} = 6.6\,V$
$L_M = 390\,\mu H$, $L_{Leak} = 5\,\mu H$	$R_{FB} = 1\,k\Omega$
$T_{1\,Ratio} = 0.25$, $C_O = 330\,\mu F$	$D_{3\,VF} = 1.4\,V$
$R_L = 30\,\Omega$, $R_{Sense} = 95\,m\Omega$	$ZD_{1\,VZ} = 1\,V$
$Q_{1\,RDS(on)} = 0.34\,\Omega$, $Q_{1\,RDS(off)} = 0.1\,G\Omega$	$R_1 = 20\,k\Omega$
$Q_{1\,Vth(on)} = 3.5\,V$	$R_2 = 10\,k\Omega$
$R_{COSS} = 20\,\Omega$, $C_{OSS} = 180\,pF$	

3.1.2 Closed-loop flyback converter during start-up

The error amplifier EA_1, a diode D_{EA}, and the voltage reference V_{Ref} model an adjustable shunt regulator (such as TL431). The error amplifier EA_1 is modeled as an ideal amplifier with infinite gain. The diode D_{EA} is used to add an additional offset to the output level of EA_1 and also ensures that the amplifier can only sink the current. The optocoupler is modeled in the forward linear region by $I_C = CTR \cdot I_F$ and in the saturation region by a constant voltage source $V_{CE(sat)}$. Table 3.2 summarizes the values of the additional as well as modified components and parameters.

Table 3.2: Component values and parameters for the closed-loop flyback converter of Figure 3.2.

Compensator	Power stage	PWM controller
$R_{D1} = 100\,k\Omega$, $R_{D2} = 9.07\,k\Omega$	$V_{DC} = 150\,V$	$D_{max} = 0.475$
$V_{Ref} = 2.5\,V$, $C_Z = 2.4\,nF$		
$R_{Bias} = 1.8\,k\Omega$, $R_E = 1\,k\Omega$		
$OPTO_{1\,VF} = 1.1\,V$, $OPTO_{1\,CTR} = 2$		
$OPTO_{1\,VCE(sat)} = 0.5\,V$		
$D_{EA\,VF} = 2.5\,V$, $C_P = 0\,pF$		

3.2 Results

3.2.1 Results open-loop flyback converter in steady-state

Table 3.3 summarizes the simulator settings and results. The simulation time t_{Sim} was set to 20 μs. The dynamic degeneration, common to the discontinuous conduction

Table 3.3: Simulator settings and results of the open-loop flyback converter.

Simulator	PLECS	GeckoCIRCUITS	Proposed approach
Version	3.7.5	1.72	1.0
Solver	Variable-step RADAU (stiff)	Fixed-step Gear-Shichman	Analytic (Laplace)
Max step size	1e-5	1e-10	-
Required steps			
#time-intervals	241	200000	-
#functions	-	-	8
CPU time in s	0.1	0.71	1.48
Data file size in kB	16	7724	2

operation of the flyback converter, is described in detail for one period $T_S = 1/F_S = 15.385\,\mu$s and leads up to six subintervals. Table 3.4 gives an overview of the states (on/off) from the semiconductor's PWM controller, Q_1, D_1, and D_S. When on, as in the case of the Diode, or MOSFET, it means that the forward current is > 0. Additionally, the active SubCircuit-Model reference and the terminating boundary conditions are summarized in Table 3.4 for each time interval. The SubCircuit-Models are shown in Figures 3.4–3.7 with the inactive components grayed out. For a more comprehensive overview, the SubCircuit-Models from the PWM controller and MOSFET Q_1 are not shown in detail, only the resulting resistance of the MOSFET Q_1 is included: $Q_{1\,RDS(off)}$ when $V_{DRV} < Q_{1\,Vth(on)}$ and $Q_{1\,RDS(on)}$ when $V_{DRV} \geq Q_{1\,Vth(on)}$. The detailed boundary conditions for the diodes D_1 and D_S are shown in Figure 2.5 in Section 2.3.3 with $I_R = 0$. The analytic solutions with the component values and parameters from Table 3.1 for each subinterval $V_{DS}(t)$ and $I_{Prim}(t)$ can be found in (3.1) and (3.2), respectively.

Table 3.4: Semiconductor states for one switching period T_S.

time interval i in μs	Model	DRV	Q_1	D_1	D_S	Boundary conditions
1: $0 \leq t < 4.7692$	I	on	on	off	off	$t \geq T_S D_{max} = 4.7692\,\mu s$
2: $4.7692 \leq t < 4.7942$	II	off	off	off	off	$D_{1\,VD}(t) = D_{1\,VF} = 0.5\,V$
3: $4.7942 \leq t < 4.7985$	III	off	off	on	off	$D_{S\,VD}(t) = D_{S\,VF} = 0.8\,V$
4: $4.7985 \leq t < 4.9376$	IV	off	off	on	on	$D_{S\,IRD}(t) = 0\,A$
5: $4.9376 \leq t < 9.9379$	III	off	off	on	off	$D_{1\,IRD}(t) = 0\,A$
6: $9.9379 \leq t < 15.385$	II	off	off	off	off	$t \geq T_S = 15.385\,\mu s$

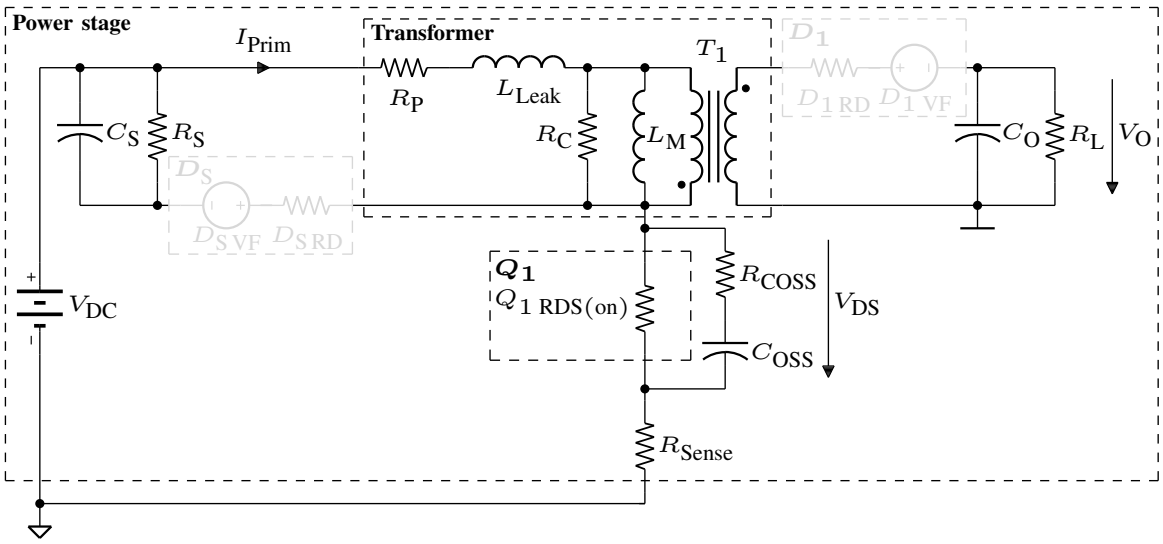

Figure 3.4: Open-loop flyback converter SubCircuit-Model I.

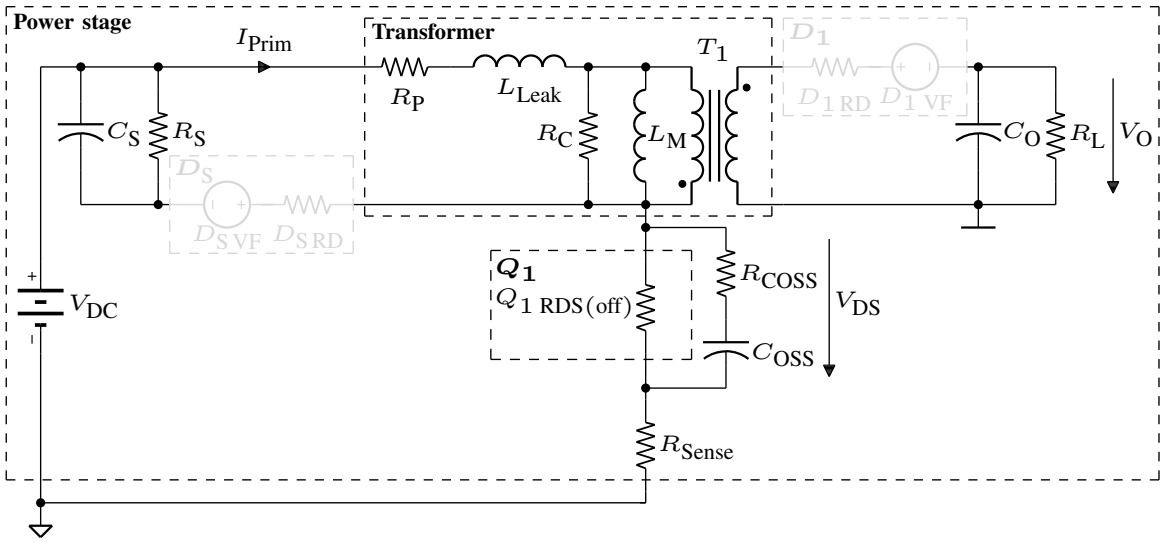

Figure 3.5: Open-loop flyback converter SubCircuit-Model II.

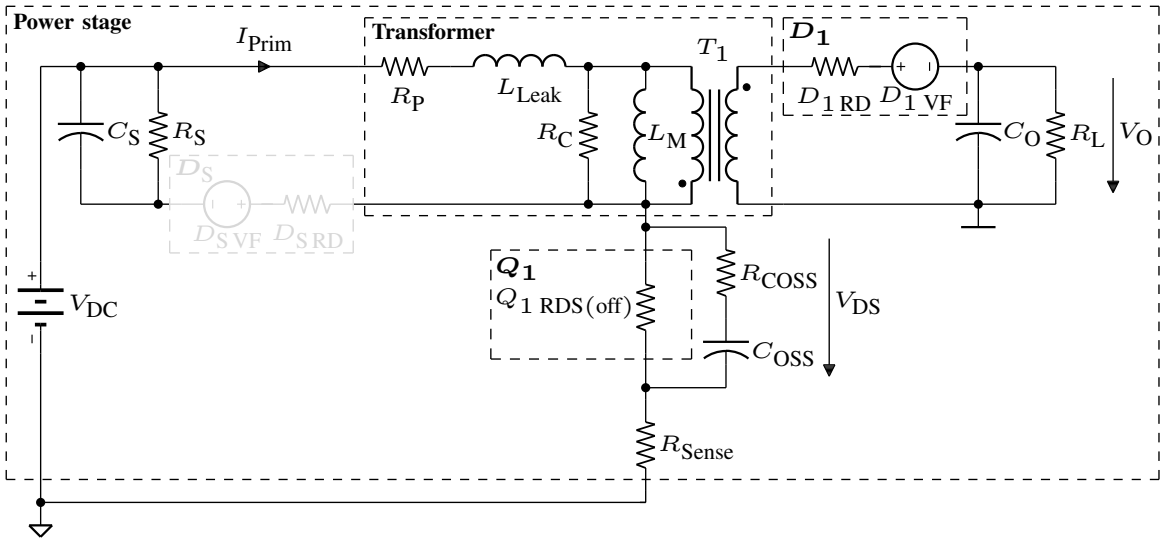

Figure 3.6: Open-loop flyback converter SubCircuit-Model III.

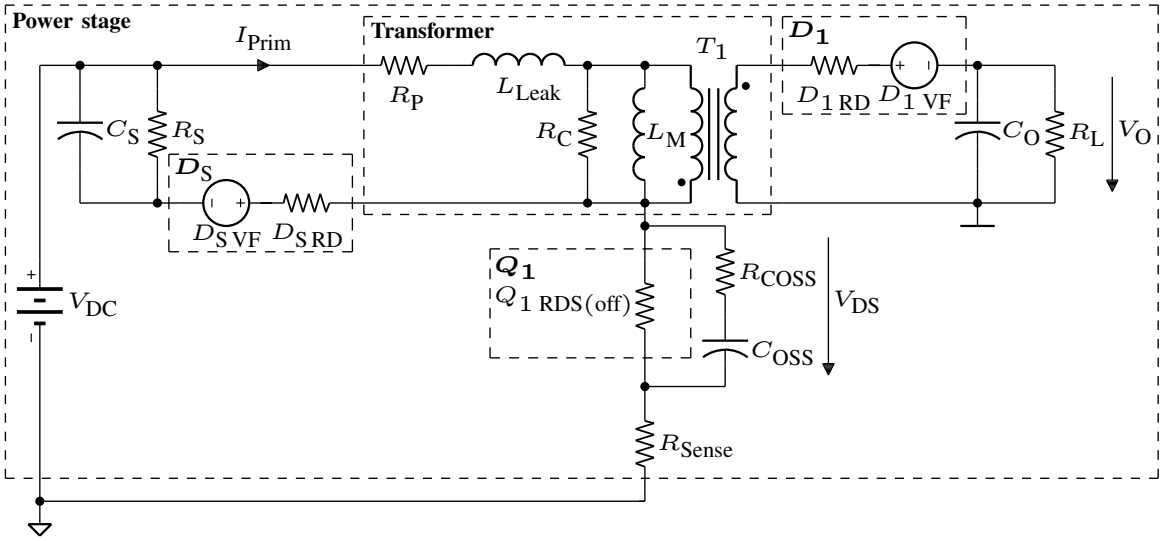

Figure 3.7: Open-loop flyback converter SubCircuit-Model IV.

$$
\begin{aligned}
V_{\mathrm{DS}1}(t) &= 82.26 - 0.002198\,\mathrm{e}^{-4.133\,10^9\,t} - 82.26\,\mathrm{e}^{-1424\,t} - 0.00003289\,\mathrm{e}^{-2.731\,10^8\,t} \\
V_{\mathrm{DS}2}(t) &= 135 + 0.02787\,\mathrm{e}^{-4.137\,10^9\,t} - 101.6\,\mathrm{e}^{-1.611\,10^5\,t}\cos\left(3.76\,10^6\,t\right) \\
&\quad + 2421\,\mathrm{e}^{-1.611\,10^5\,t}\sin\left(3.76\,10^6\,t\right) \\
V_{\mathrm{DS}3}(t) &= 135 + 2.072\,\mathrm{e}^{-2.145\,10^6\,t}\cos\left(3.36\,10^7\,t\right) + 269.2\,\mathrm{e}^{-2.145\,10^6\,t}\sin\left(3.36\,10^7\,t\right) \\
&\quad + 123.2\,\mathrm{e}^{-1085\,t}\cos\left(11150\,t\right) - 4.85\,\mathrm{e}^{-1085\,t}\sin\left(11150\,t\right) \\
V_{\mathrm{DS}4}(t) &= 135 + 123.3\,\mathrm{e}^{-1085\,t}\cos\left(11150\,t\right) - 4.857\,\mathrm{e}^{-1085\,t}\sin\left(11150\,t\right) \\
&\quad + 39.79\,\mathrm{e}^{-1.027\,10^5\,t}\cos\left(6.467\,10^6\,t\right) + 51.51\,\mathrm{e}^{-1.027\,10^5\,t}\sin\left(6.467\,10^6\,t\right) \\
&\quad + 0.9263\,\mathrm{e}^{-2.863\,10^8\,t} \\
V_{\mathrm{DS}5}(t) &= 135 + 64.17\,\mathrm{e}^{-2.145\,10^6\,t}\cos\left(3.36\,10^7\,t\right) - 3.435\,\mathrm{e}^{-2.145\,10^6\,t}\sin\left(3.36\,10^7\,t\right) \\
&\quad + 123.2\,\mathrm{e}^{-1085\,t}\cos\left(11150\,t\right) - 5.045\,\mathrm{e}^{-1085\,t}\sin\left(11150\,t\right) \\
V_{\mathrm{DS}6}(t) &= 135 - 0.001404\,\mathrm{e}^{-4.137\,10^9\,t} + 122.1\,\mathrm{e}^{-1.611\,10^5\,t}\cos\left(3.76\,10^6\,t\right) \\
&\quad + 3.628\,\mathrm{e}^{-1.611\,10^5\,t}\sin\left(3.76\,10^6\,t\right)
\end{aligned}
\tag{3.1}
$$

$$
\begin{aligned}
I_{\text{Prim}\,1}(t) &= 241.9 - 0.006582\,\mathrm{e}^{-4.133\,10^9\,t} - 241.9\,\mathrm{e}^{-1424\,t} + 1.408\,10^{-9}\,\mathrm{e}^{-2.731\,10^8\,t} \\
I_{\text{Prim}\,2}(t) &= 0.001494\,\mathrm{e}^{-4.137\,10^9\,t} + 1.642\,\mathrm{e}^{-1.611\,10^5\,t}\,\cos\left(3.76\,10^6\,t\right) \\
&\quad + 0.02079\,\mathrm{e}^{-1.611\,10^5\,t}\,\sin\left(3.76\,10^6\,t\right) \\
I_{\text{Prim}\,3}(t) &= 1.63\,\mathrm{e}^{-2.145\,10^6\,t}\,\cos\left(3.36\,10^7\,t\right) + 0.0814\,\mathrm{e}^{-2.145\,10^6\,t}\,\sin\left(3.36\,10^7\,t\right) \\
&\quad - 0.0000338\,\mathrm{e}^{-1085\,t}\,\cos\left(11150\,t\right) - 0.00024643\,\mathrm{e}^{-1085\,t}\,\sin\left(11150\,t\right) \\
I_{\text{Prim}\,4}(t) &= -0.000008 + 0.0007656\,\mathrm{e}^{-2.863\,10^8\,t} + 1.609\,\mathrm{e}^{-1.027\,10^5\,t}\,\cos\left(6.467\,10^6\,t\right) \\
&\quad - 1.277\,\mathrm{e}^{-1.027\,10^5\,t}\,\sin\left(6.467\,10^6\,t\right) + 0.0003157\,\mathrm{e}^{-1085\,t}\,\cos\left(11150\,t\right) \\
&\quad - 0.006728\,\mathrm{e}^{-1085\,t}\,\sin\left(11150\,t\right) \\
I_{\text{Prim}\,5}(t) &= 0.001597\,\mathrm{e}^{-2.145\,10^6\,t}\,\cos\left(3.36\,10^7\,t\right) - 0.3897\,\mathrm{e}^{-2.145\,10^6\,t}\,\sin\left(3.36\,10^7\,t\right) \\
&\quad - 0.00003418\,\mathrm{e}^{-1085.\,t}\,\cos\left(11150\,t\right) - 0.0002463\,\mathrm{e}^{-1085.\,t}\,\sin\left(11150\,t\right) \\
I_{\text{Prim}\,6}(t) &= -0.00007523\,\mathrm{e}^{-4.137\,10^9\,t} + 0.0000362\,\mathrm{e}^{-1.611\,10^5\,t}\,\cos\left(3.76\,10^6\,t\right) \\
&\quad - 0.08277\,\mathrm{e}^{-1.611\,10^5\,t}\,\sin\left(3.76\,10^6\,t\right)
\end{aligned}
\tag{3.2}
$$

The measured and simulated voltage $V_{\text{DS}}(t)$ and current $I_{\text{Prim}}(t)$ are shown in Figure 3.8. All simulators provide the same result;[4] however, the number of calculated reference points varies greatly. Here, the fixed-step solver needs a sufficiently small step size to converge, as opposed to the variable-step solver that adopts the step size during simulation.

As mentioned in the introduction in Section 1.2, the proposed approach returns the functions of the state variables and the signals of interest. This creates the opportunity to investigate certain intervals of time in detail without simulating these many times again with a smaller step size, as in the case with a numerical solver. While in this special case, the CPU time of the proposed approach is longer,

the data file size is significantly smaller than that of the other two simulators (e.g., ≈ 1/8, 1/3850).

This advantage, along with the strength of the formulation approach in case of parameter studies, is illustrated in Section 3.2.3.

[4] A small deviation at the beginning of the measured voltage $V_{\text{DS}}(t)$ can be observed from the simulation results of all simulators, which is caused by the slightly fluctuating input voltage of the prototype. The winding capacitance and the inter-winding capacitance of the transformer have not been modeled explicitly, because their influence on the overall system's behavior is very small, as observed only as a small spike at the measured current $I_{\text{Prim}}(t)$ at turn-on.

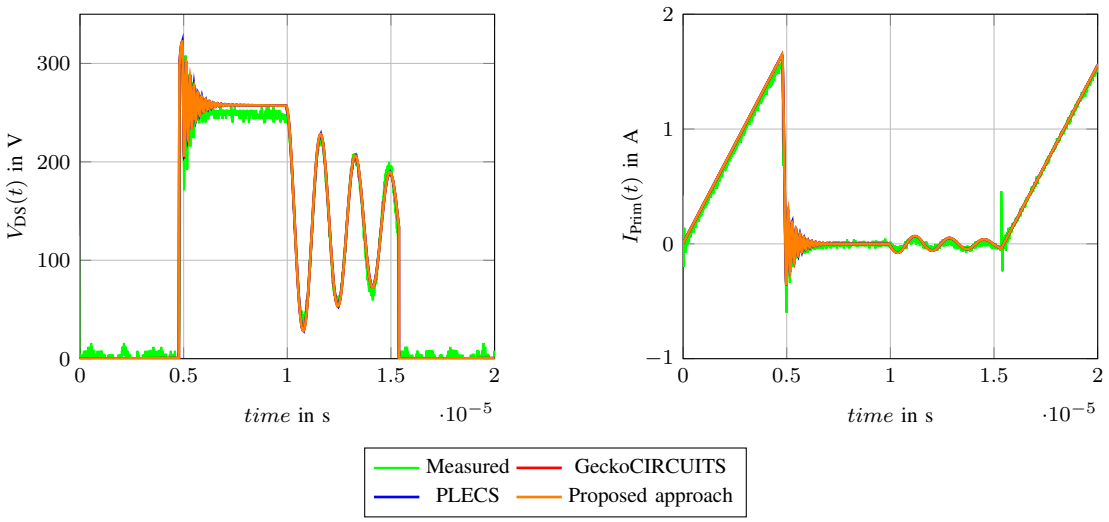

Figure 3.8: Comparison of measurement and simulation results: $V_{DS}(t)$ and $I_{Prim}(t)$ open-loop flyback converter in steady-state.

3.2.2 Results closed-loop flyback converter during start-up

Table 3.5 summarizes the simulator settings and results. The simulation time t_{Sim} was set to 2.5 ms. The measured and simulated voltages $V_O(t)$ and $V_{FB}(t)$ are shown in

Table 3.5: Simulator settings and results of the closed-loop flyback converter.

Simulator	PLECS	GeckoCIRCUITS	Proposed approach
Version	3.7.5	1.72	1.0
Solver	Variable-step RADAU (stiff)	Fixed-step Gear-Shichman	Analytic (Laplace)
Max step size	1e-5	1e-8	-
Required steps			
#time-intervals	32601	250000	-
#functions	-	-	1065
CPU time in s	1.63	1.47	9.52
Data file size in kB	1947	8314	129

Figure 3.9. The simulation results from the proposed approach are very close to the measured data. A small deviation at the beginning and at the end of the measured voltage $V_{FB}(t)$ can be observed from the simulation results of all simulators, which

is caused by the power-up sequence of the adjustable shunt regulator which has not been modeled in the simulators, respectively the constant modeled forward voltage of the $D_{3\,\mathrm{VF}}$ and CTR of the optocoupler $OPTO_1$. Similar observations with respect to CPU time and data file size as in the previous case are made. However, because of the larger circuit,

the small data file size of the proposed approach is significantly smaller than that of the other two simulators (e.g., ≈ 1/15, 1/64).

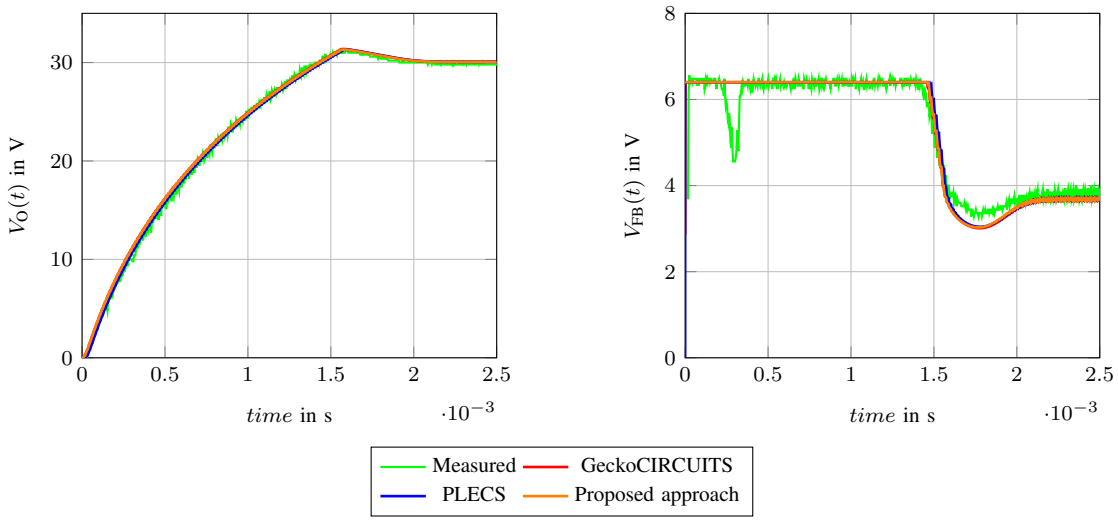

Figure 3.9: Comparison of measurement and simulation results: $V_O(t)$ and $V_{FB}(t)$ closed-loop flyback converter during start-up.

3.2.3 Discussion of parametrization

To demonstrate the efficiency of the proposed approach for parameter studies in case of small-scale electronic circuits, the open-loop flyback converter from Section 3.1.1 was modified to an ideal flyback converter (with a perfectly coupled transformer with losses): the leakage inductance L_{Leak} of the transformer, the primary RCD snubber D_S, R_S, C_S, and the output capacitance C_{OSS} of the MOSFET Q_1 have been removed. The simulation was performed 1000 times, and the value of the magnetizing inductance L_M was updated for each simulation i with $L_{Mi} = 0.003 + \frac{0.007}{1000} i\,\mathrm{H}$. The simulation time t_{Sim} was again set to 20 μs. Table 3.6 summarizes the simulator settings and results. In this case, the total CPU time of the proposed approach is

significantly shorter than that of the other two simulators (e.g., ≈ 1/4, 1/69), illustrating the advantage of the analytic solution (approach).

Table 3.6: Simulator settings and results of the modified open-loop flyback converter.

Simulator	PLECS	GeckoCIRCUITS	Proposed approach
Version	3.7.5	1.72	1.0
Solver	Variable-step RADAU (stiff)	Fixed-step Gear-Shichman	Analytic (Laplace)
Max step size	1e-5	1e-7	-
CPU time in s	17.98	311.22	4.51

3.3 Conclusion

The proposed approach for a precision transient circuit simulator without a time step is presented. A closed-form analytic solution is computed for each of the electronic circuit states. Numerical integration is not required, and therefore, convergence problems are eliminated. The proposed approach returns the analytic functions of the state variables and the signals of interest instead of discrete values. This creates the opportunity to investigate certain intervals of time in detail without re-simulating the whole circuit. Based on the SubCircuit-Model for linear elements, the Circuit-Model for piecewise-linear elements is discussed. With respect to accuracy, the proposed approach shows similar performance to established simulators and the simulation results are well in line with the experimental ones.

Superior performance in terms of total CPU time of the proposed approach was shown and is significantly shorter than that of the other two simulators (e.g., ≈ 1/4, 1/69) for parameter studies of smaller electronic circuits. The proposed tool has been developed to determine the design limits of the device and design limits of the individual components, respectively, by parametric simulation (scanning tool). The proposed tool can be coupled with an optimizer to identify, e.g., these worst-case values in a few steps.

Chapter 4

Example cases for worst-case analyses

4.1 Worst-case analysis of an RLC series resonant circuit

The schematic diagram of the RLC (resistor inductor capacitor) series resonant circuit is shown in Figure 4.1. The maximum peak inductor current $\hat{I}_{L1}$ in steady-state should be determined as a function of two parameters, e.g., t and L_1.

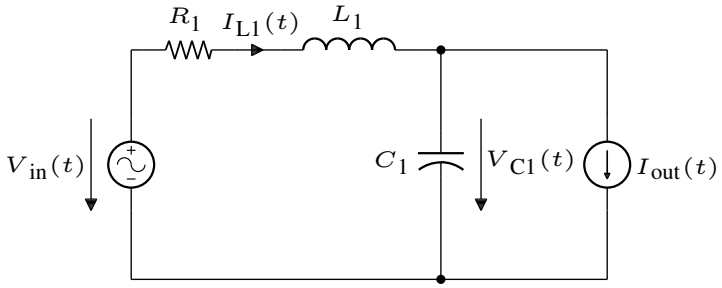

Figure 4.1: SubCircuit-Model: RLC series resonant circuit.

4.1.1 SubCircuit-Model of an RLC series resonant circuit

The associated ESSSM is described by (4.1)–(4.3). Eq. (4.1) represents the system of differential (state) equations, (4.2) the signal of interest, and (4.3) the I/O interface. In this example, the input-cell $\mathbf{y}_I(t)$ of the I/O interface is not defined.

$$\begin{bmatrix} L_1 \frac{dI_{L1}(t)}{dt} \\ C_1 \frac{dV_{C1}(t)}{dt} \end{bmatrix} = \begin{bmatrix} -R_1 & -1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} I_{L1}(t) \\ V_{C1}(t) \end{bmatrix} + \begin{bmatrix} V_{in} \sin(\omega t) \\ -I_{out}(t) \end{bmatrix} \tag{4.1}$$

$$\mathbf{y}(t) = I_{L1}(t) \tag{4.2}$$

I/O interface:

$$\mathbf{y}_{\mathrm{IO}}(t) = \begin{bmatrix} \mathbf{y}_{\mathrm{I}}(t) \\ \mathbf{y}_{\mathrm{O}}(t) \end{bmatrix} \quad \text{with} \quad \mathbf{y}_{\mathrm{I}}(t) = \begin{bmatrix} \ \end{bmatrix} \quad \mathbf{y}_{\mathrm{O}}(t) = \begin{bmatrix} I_{\mathrm{out}}(t) \\ V_{\mathrm{C1}}(t) \end{bmatrix} \tag{4.3}$$

4.1.2 Analytic analysis of an RLC series resonant circuit

The analytic solution of the ODE System (4.1) for $I_{\mathrm{L1}}(t)$ from the SubCircuit-Model in Figure 4.1 is shown (4.4). The initial conditions $I_{\mathrm{L1}}(0)$, $V_{\mathrm{C1}}(0)$, and $I_{\mathrm{out}}(t)$ were set to 0.

$$\begin{aligned}
I_{\mathrm{L1}}(t) &= \frac{M_1}{4kL_1}\left(E_1\left(C_1R_1k\omega + M_2\right) + D_0\right) \\
&\quad - \frac{M_1}{4kL_1}\left(E_2\left(C_1R_1k\omega - M_2\right)\right) \\
k &= \sqrt{\left(C_1\left(C_1R_1^2 - 4L_1\right)\right)} \\
D_0 &= 4V_{\mathrm{in}}C_1L_1k\omega\left(1 - C_1L_1\omega^2\right)\cos\left(\omega t\right) \\
&\quad + 4V_{\mathrm{in}}C_1^2L_1R_1k\omega^2\sin\left(\omega t\right) \\
E_1 &= V_{\mathrm{in}}\left(-C_1R_1 + k\right)\mathrm{e}^{\frac{1}{2}\frac{\left(-C_1R_1+k\right)t}{C_1L_1}} \\
E_2 &= V_{\mathrm{in}}\left(C_1R_1 + k\right)\mathrm{e}^{-\frac{1}{2}\frac{\left(C_1R_1+k\right)t}{C_1L_1}} \\
M_1 &= \frac{1}{\omega^4C_1^2L_1^2 + \omega^2C_1^2R_1^2 - 2\omega^2C_1L_1 + 1} \\
M_2 &= 2C_1^2L_1^2\omega^3 + C_1^2R_1^2\omega - 2C_1L_1\omega
\end{aligned} \tag{4.4}$$

4.1.3 Worst-case analysis of an RLC series resonant circuit

Table 4.1 summarizes the values of the components and the SQP parameters. The maximum peak inductor current $\hat{I}_{\mathrm{L1}}$ in steady-state should be determined as a function of two variable parameters, e.g., t and L_1. The objective function $f(\mathbf{x})$ for the minimum peak inductor current is obtained by the evaluation of the component values from Table 4.1 in (4.4). The objective function for the maximum is

$$f(\mathbf{x}) = I_{\mathrm{L1\,max\,function}}(t, L_1) = -I_{\mathrm{L1}}(t, L_1)\,. \tag{4.5}$$

To identify the maximum peak inductor current in steady-state, the lower bound for t was chosen to be 10 times larger than the period $T = 1/f$. The 3-D plot of

Table 4.1: Component values and SQP parameters RLC series resonant circuit of Figure 4.1.

Components values	Parameter x_i	Lower bound	Upper bound
$V_{\text{in}} = 2\,\text{V}$	t	$t_{\min} = 10.0\,\text{s}$	$t_{\max} = 10.5\,\text{s}$
$R_1 = 50\,\Omega$	L_1	$L_{1\,\min} = 0.1\,\text{H}$	$L_{1\,\max} = 30.0\,\text{H}$
$C_1 = 15\,\text{mF}$			
$\omega = 2\pi f$			
$f = 1\,\text{Hz}$			
$I_{\text{out}}(t) = 0\,\text{A}$			

the objective function $I_{\text{L1 max function}}(t, L_1)$ (4.5) including the solution path of the SQP method is illustrated in Figure 4.2. The implemented SQP method converges to the maximum after 7 iterations (summarized in Table 4.2) with $|\hat{I}_{\text{L1}}| = 0.04\,\text{A}$ and is also visualized in the contour plot in Figure 4.3. The solution of the SQP method is exactly the same as expected: at the resonant frequency, the capacitive and inductive reactances cancel each other out, and the current through the inductor L_1 is only limited by the resistor R_1, hence $\hat{I}_{\text{L1}} = {}^{V_{\text{in}}}/_{R_1} = 0.04\,\text{A}$.

Table 4.2: SQP method on RLC series resonant circuit of Figure 4.1.

k	0	1	2	3	4	5	6
$t^{(k)}$ in s	10.10	10.41	10.46	10.44	10.29	10.24	10.25
$L_1^{(k)}$ in H	15.00	15.00	9.74	6.00	0.46	1.45	1.69
$I_{\text{L1 max}}^{(k)}$ in mA	8.06	−20.53	−24.58	−27.31	−36.25	−39.98	−40.00

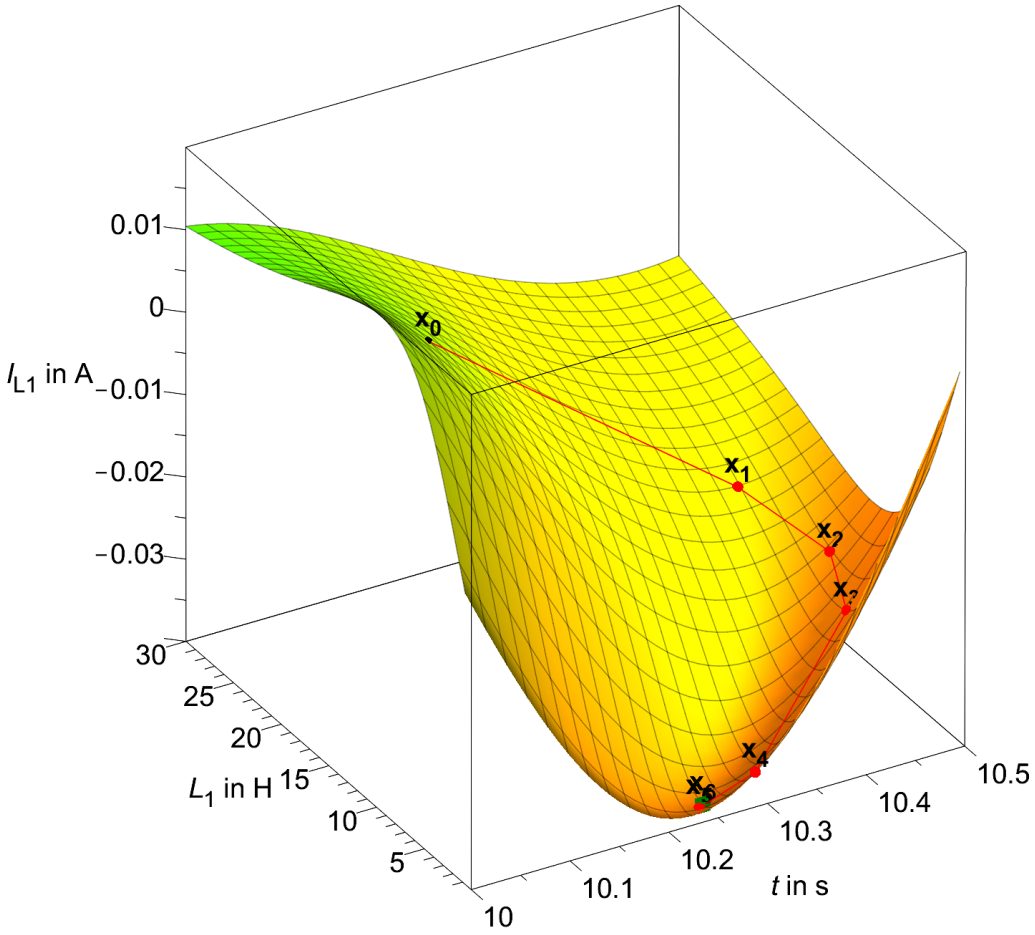

Figure 4.2: RLC series resonant circuit $I_{\mathrm{L1\,max\,function}}(t, L_1)$.

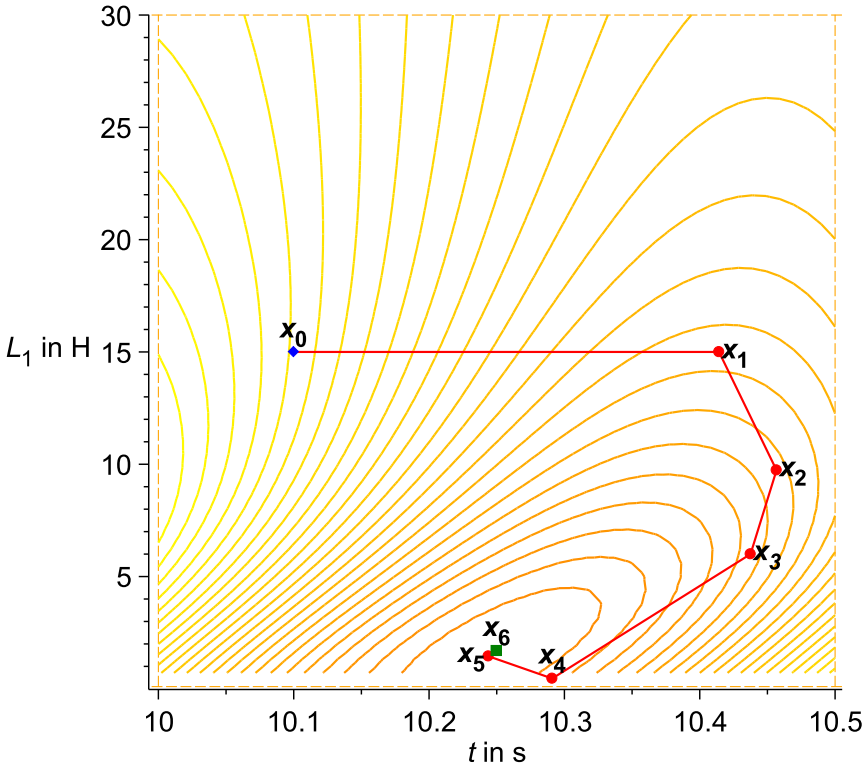

Figure 4.3: RLC series resonant circuit contour plot $I_{\mathrm{L1\,max\,function}}(t, L_1)$.

4.2 Worst-case analysis of a second flyback converter in continuous conduction mode

The performance of the proposed approach is demonstrated, too, by a worst-case analysis of a second flyback converter in continuous conduction mode (CCM). The goal is to determine the maximum magnetizing current $\hat{I}_{\mathrm{LM}}$ from the transformer T_1 in steady-state. This is especially important for the transformer design. The schematic diagram of the closed-loop flyback converter is shown in Figure 4.4 and is divided into the following three parts:

- Power stage: includes a real transformer with the winding resistance R_{P}, the magnetizing inductance L_{M}, an ideal transformer T_1, a power switch Q_1, a current sense resistor R_{Sense}, the secondary rectifier D_1, and the output filter capacitor C_{O}. The power switch Q_1 is modeled as a voltage controlled ideal switch with two resistors $Q_{1\,\mathrm{RDS(on)}}$ representing the resistance in the on-region and the resistance $Q_{1\,\mathrm{RDS(off)}}$ for the cut-off region.

- PWM controller: for the control method, peak current mode control with constant switching frequency F_S is chosen and is implemented in the PWM controller block. A detailed structure of the PWM controller is shown in Figure 4.5.

- Compensator: a Type 2 compensator [72, 73] is used, containing the error amplifier EA_1, a diode D_{EA}, and a voltage reference V_{Ref} to model an adjustable shunt regulator (such as TL431). The error amplifier EA_1 is modeled as an ideal amplifier with infinite gain. The diode D_{EA} is used to add an additional offset to the output level of EA_1 and also ensures that the amplifier can only sink the current. The optocoupler $OPTO_1$ is modeled in the forward linear region by multiplying I_F with a constant factor, the current transfer ratio (CTR) $I_C = CTR \cdot I_F$ and in the saturation region by a constant voltage source $V_{CE(sat)}$.

In general, many switching cycles are necessary until the system has reached the steady-state in the case of switching mode power supply. In steady-state, a PWM signal with constant duty-cycle d_{on} is generated in the way that the average output voltage $\overline{V_O}$ equals $V_{O\,nom}$. The compensator and the PWM controller are responsible for tuning the duty-cycle.

4.2.1 Steady-state analysis

The major advantage of the proposed analytic forward solver approach is that the unknown duty-cycle in steady-state can be calculated based on the analytic solutions of the state variables and/or signal of interest, e.g., (4.2). In addition, the closed-loop flyback converter can be simplified to an open-loop flyback converter or power stage. This means that no additional algorithms are needed for the steady-state analysis, e.g., as used in [74–77]. The flyback converter power stage operating in CCM has two SubCircuit-Models (states) and two state variables (i.e., I_{LM}[1] and V_{CO}[2]). The initial conditions for the state variables are decribed by $I_{LM\,10}$, $V_{CO\,10}$, $I_{LM\,20}$, and $V_{CO\,20}$. Figure 4.6 shows the steady-state waveforms of the state variables for one switching cycle $T_S = 1/F_S$.

[1] The current through the inductor L_M.
[2] The voltage across the capacitor C_O.

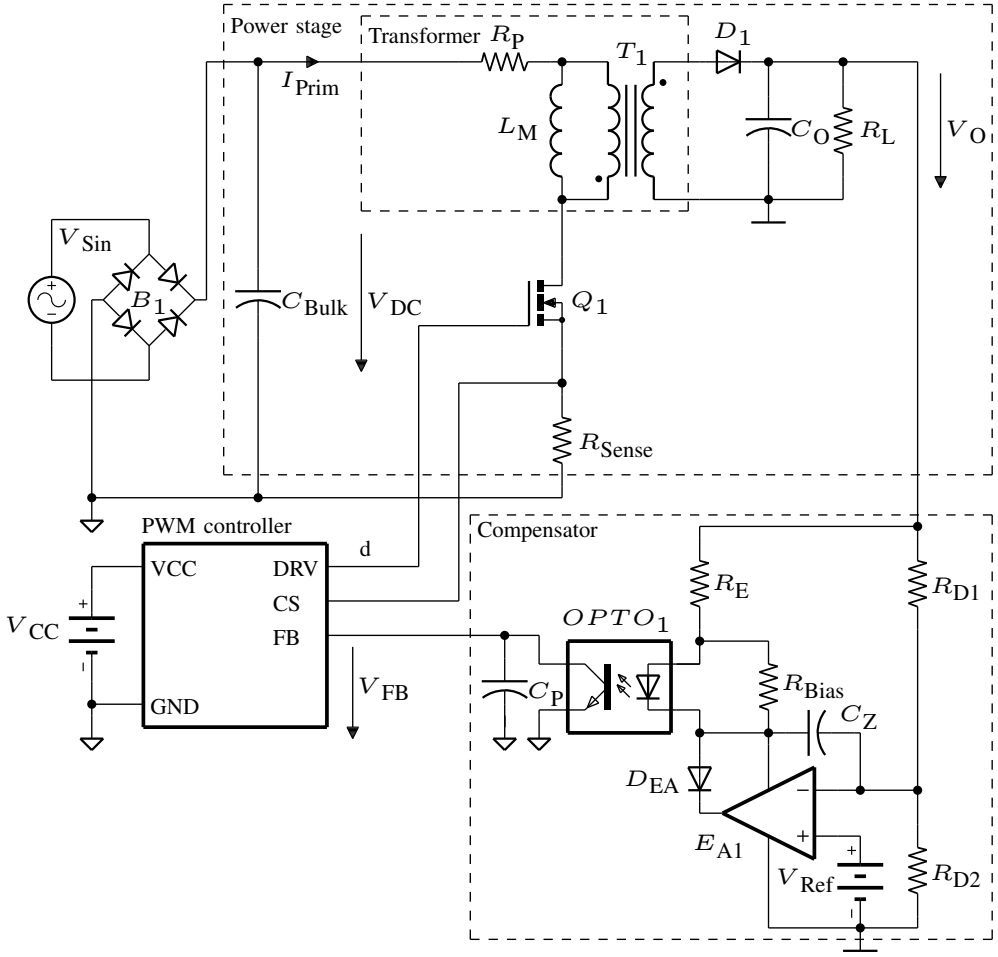

Figure 4.4: Schematic diagram of a closed-loop flyback converter with peak current mode control.

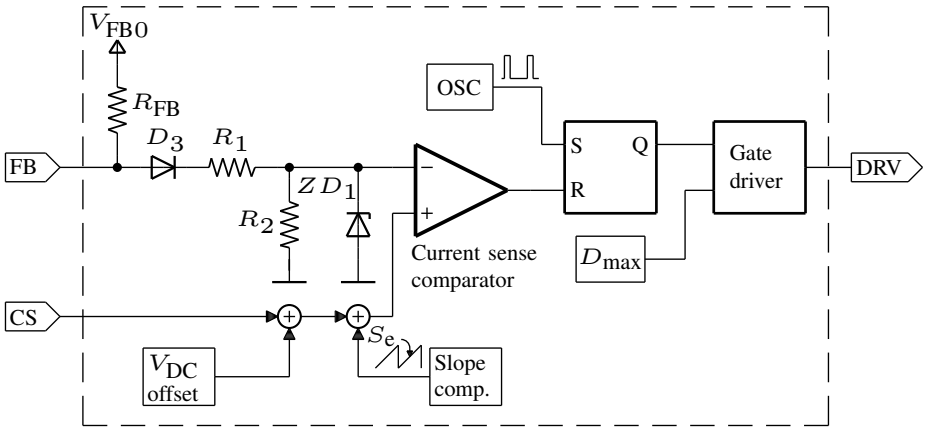

Figure 4.5: Block diagram of the peak current mode PWM controller.

- State 1: DRV high, MOSFET Q_1 is switched on (saturation) and D_1 is in the OFF-state (reverse bias) with $0 < t \leq t_{on}$.
- State 2: DRV low, MOSFET Q_1 is switched off (cut-off) and D_1 is in the ON-state (forward bias) with $t_{on} < t < T_S$.

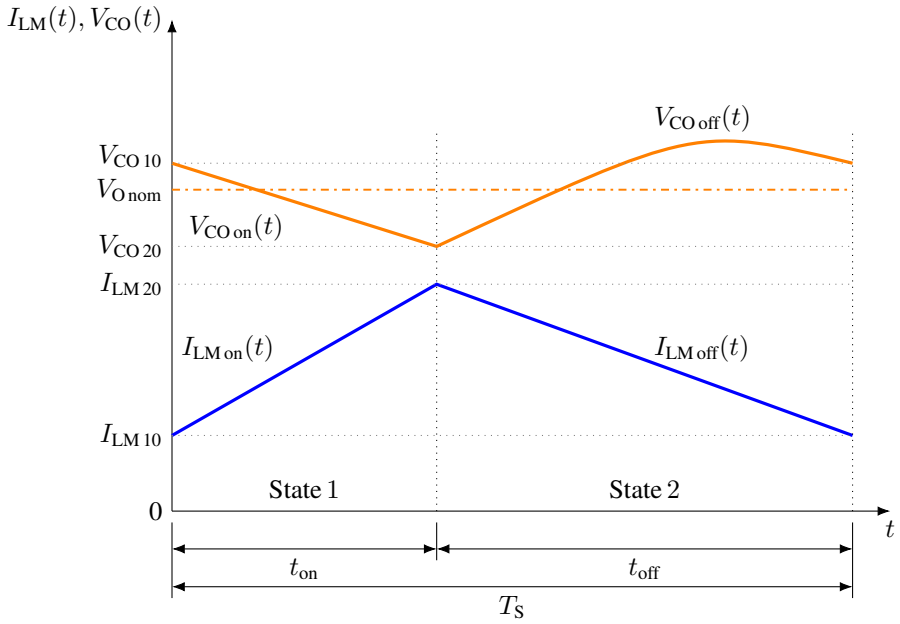

Figure 4.6: Waveforms flyback.

The initial conditions of the state variables in state 1 can be expressed as

$$I_{LM\,10} = I_{LM\,off}(T_S - t_{on}) \tag{4.6}$$

$$V_{CO\,10} = V_{CO\,off}(T_S - t_{on}) \tag{4.7}$$

and for state 2 as

$$I_{LM\,20} = I_{LM\,on}(t_{on}) \tag{4.8}$$

$$V_{CO\,20} = V_{CO\,on}(t_{on})\,. \tag{4.9}$$

$$V_{O\,nom} = \frac{1}{T_S}\left(\int_0^{t_{on}} V_{CO\,on}(t)\mathrm{d}t + \int_{t_{on}}^{T_S} V_{CO\,off}(t)\mathrm{d}t\right) \tag{4.10}$$

Equation (4.10) expresses that the average voltage $\overline{V_{CO}}$ across the capacitor C_O equals $V_{O\,nom}$. Using (4.6) and (4.7) in (4.8) and (4.9) with (4.10), results in a system of equations with three unknowns $I_{LM\,20}$, $V_{CO\,20}$, and t_{on}. For improved performance, the system of equations in analytic form (generated by the analytic forward solver approach) are solved numerically.

4.2.2 SQP result

The solution for the initial condition $I_{LM\,20}$ of the system of equations (4.8)–(4.10) corresponds to $\hat{I}_{LM}$. The objective function for the maximum magnetizing current is

$$f(\mathbf{x}) = I_{LM\,max}(\mathbf{x}) = -I_{LM\,20}\,. \tag{4.11}$$

Table 4.3 summarizes the component values and parameters for the closed-loop flyback converter and Table 4.4 summarizes the values of the SQP parameters. The implemented SQP method converges to the maximum after 6 iterations with $\hat{I}_{LM} = 2.583\,A$.

Table 4.3: Component values and parameters for the closed-loop flyback converter of Figure 3.2.

Power stage	PWM controller	Compensator
$R_P = 0.2\,\Omega$	$V_{DRV\,low} = 0\,V$	$V_{Ref} = 2.5\,V$
$T_{1\,Ratio} = 0.25$	$V_{DRV\,high} = 10\,V$	$R_{D1} = 110\,k\Omega$
$Q_{1\,Vth(on)} = 3.5\,V$	$S_e = 0.01\,\frac{V}{\mu s}$	$R_{D2} = 10\,k\Omega$
$Q_{1\,RDS(on)} = 0.34\,\Omega$	$V_{DC\,Offset} = 0\,V$	$R_E = 1\,k\Omega$
$Q_{1\,RDS(off)} = 0.1\,G\Omega$	$V_{FB0} = 6.6\,V$	$R_{Bias} = 1\,k\Omega$
$D_{1\,RD} = 50\,m\Omega$	$R_{FB} = 1\,k\Omega$	$C_Z = 4.7\,nF$
$C_O = 2200\,\mu F$	$D_{3\,VF} = 1.4\,V$	$C_P = 0\,pF$
$R_L = 10\,\Omega$	$R_1 = 20\,k\Omega$	$D_{EA\,VF} = 2.5\,V$
$V_{O\,nom} = 30\,V$	$R_2 = 10\,k\Omega$	$OPTO_{1\,VF} = 1.1\,V$
	$ZD_{1\,VZ} = 1\,V$	$OPTO_{1\,CTR} = 2$
		$OPTO_{1\,VCE(sat)} = 0.5\,V$

Table 4.4: SQP parameters for the closed-loop flyback converter of Figure 3.2.

Parameter x_i	Lower bound	Upper bound
V_{DC}	$V_{\mathrm{DC\,min}} = 100\,\mathrm{V}$	$V_{\mathrm{DC\,max}} = 300\,\mathrm{V}$
L_{M}	$L_{\mathrm{M\,min}} = 330\,\mu\mathrm{H}$	$L_{\mathrm{M\,max}} = 470\,\mu\mathrm{H}$
F_{S}	$F_{\mathrm{S\,min}} = 95\,\mathrm{kHz}$	$F_{\mathrm{S\,max}} = 105\,\mathrm{kHz}$
$D_{1\,\mathrm{VF}}$	$D_{1\,\mathrm{VF\,min}} = 0.6\,\mathrm{V}$	$D_{1\,\mathrm{VF\,max}} = 1.2\,\mathrm{V}$
R_{Sense}	$R_{\mathrm{Sense\,min}} = 0.14\,\Omega$	$R_{\mathrm{Sense\,max}} = 0.158\,\Omega$

Table 4.5: SQP method on closed-loop flyback converter of Figure 3.2.

k	0	1	2	3	4	5
$V_{\mathrm{DC}}^{(k)}$ in V	202.0	202.0	202.0	202.2	100.0	100.0
$L_{\mathrm{M}}^{(k)}$ in μH	380.0	330.0	330.0	330.0	330.0	330.0
$F_{\mathrm{S}}^{(k)}$ in kHz	100.0	100.0	100.0	100.0	99.9	95.0
$D_{1\,\mathrm{VF}}^{(k)}$ in V	0.7	0.7	1.2	1.2	1.2	1.2
$R_{\mathrm{Sense}}^{(k)}$ in Ω	0.140	0.140	0.142	0.158	0.158	0.158
$I_{\mathrm{LM\,max}}^{(k)}$ in A	−2.215	−2.368	−2.387	−2.387	−2.539	−2.583

4.2.3 Transient simulation

To verify the results from the SQP method in steady-state, for each iteration k (summarized in Table 4.5) a transient simulation of the closed-loop flyback converter has been performed with the same parameters in Table 4.4 and Table 4.3 as shown in Figure 4.7. The transient simulation results are obtained by applying the analytic forward solver approach to the Circuit-Model of the closed-loop flyback converter. The simulation time t_{Sim} was set to 30 ms. The results from the SQP method are shown in Figure 4.7 as horizontal lines, these are marked with $\left|I_{\mathrm{LM\,max}}^{(k)}\right|$. The peak currents of the transient simulations exactly match the SQP results, having the same colors.

4.2.4 Performance comparison

To compare the performance of the SQP method, an MC analysis and evolution strategy (1+1) ES [5] has been implemented in Maple as well. The implemented MC

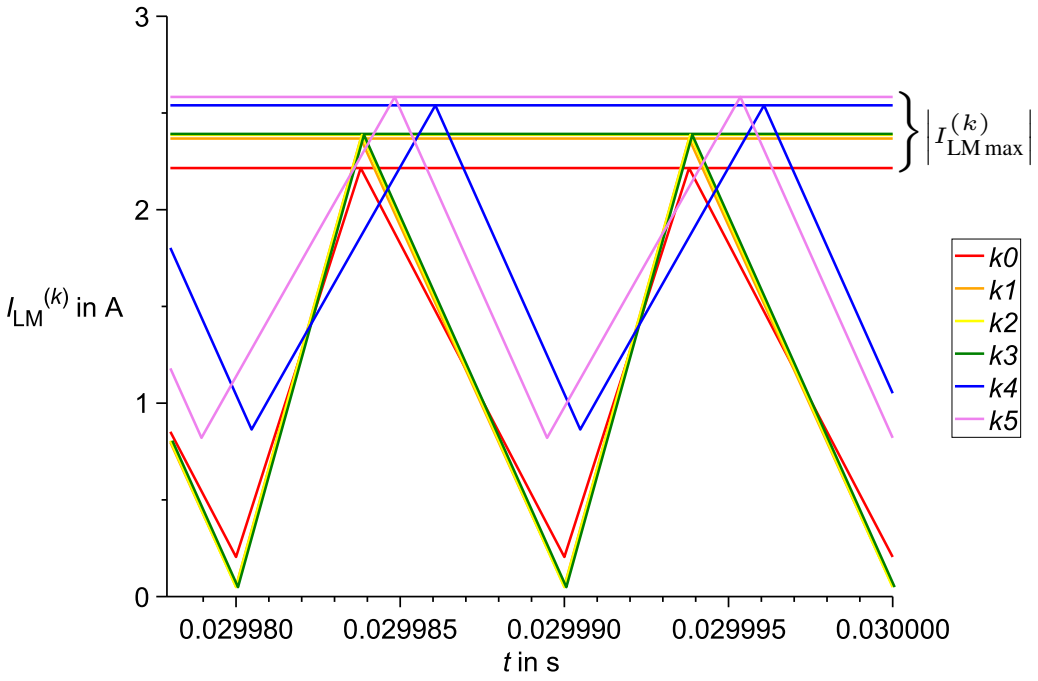

Figure 4.7: Comparison SQP results and transient simulation.

analysis uses the continuous uniform distribution over the parameter ranges. All methods use the same objective function (4.11). Table 4.6 summarizes the iterations for the methods and results. The (1+1) ES method and the SQP methods provide the same result; however, the number of iterations for convergence varies greatly. The MC method could not find the exact worst-case value even at a higher number of iteration runs k.

The total CPU time of the SQP method is significantly shorter than that of the other two methods, i.e., MC and (1+1) ES (e.g., $MC_{k=1000} \approx 1/9$, $MC_{k=10000} \approx 1/95$, (1+1) ES $\approx 1/7$).

Table 4.6: Performance comparison of different solutions methods.

Method	MC	MC	(1+1) ES	SQP
$\lvert\hat{I}_{LM}\rvert$ in A	2.532	2.535	2.583	2.583
#k iterations	1000	10000	712	6
CPU time in s	20.67	211.6	14.88	2.21

4.2.5 A more complex example case

The example of the worst-case tolerance analysis of a flyback converter in CCM was shown. The example can be extended by, e.g., the discontinuous conduction mode (DCM), which arises when the inductor current is zero. Here, the analytic forward solver approach provides the additional needed state for DCM. The initial conditions of the state variables can be expressed as it was done in the CCM example. Both models of the flyback converter can also be combined to one model which also supports switching between CCM and DCM. The CCM model becomes invalid when $I_{\mathrm{LM}\,10}$ is negative. The advantage is, that based on the analytic forward solver approach, it is possible to reduce this flyback converter in steady-state from a closed-loop to an open-loop system, too. This results in much faster simulation speed in contrast to the closed-loop flyback converter.

4.3 Conclusion

The SQP method in combination with the proposed analytic forward solver approach shows that the identification of the worst-case values converges in a few steps even if the worst-case values are not on the boundary of the parameters. Based on the analytic forward solver approach, it is possible to reduce a flyback converter in steady-state from a closed-loop to an open-loop system. These results are well in line with the transient simulation results obtained by applying analytic forward solver approach to the open loop flyback converter described in Section 4.2.3. With respect to accuracy, the SQP method shows similar performance as the (1+1) ES strategy. Superior performance in terms of total CPU time was shown. The total CPU time of the SQP method is significantly shorter than that of the other two methods, i.e., MC and (1+1) ES (e.g., $\mathrm{MC}_{k=1000} \approx 1/9$, $\mathrm{MC}_{k=10000} \approx 1/95$, (1+1) ES $\approx 1/7$).

Chapter 5

Example case sizing of a step down converter

The power stage of the step down converter in Figure 5.1 should be sized. In contrast to the previous example case applications, first the SQP method is used in combination with the analytic forward solver approach to optimize the efficiency of the step down converter. In the second step, the different components of the step down converter are sized by applying the SQP method in combination with the analytic forward solver approach.

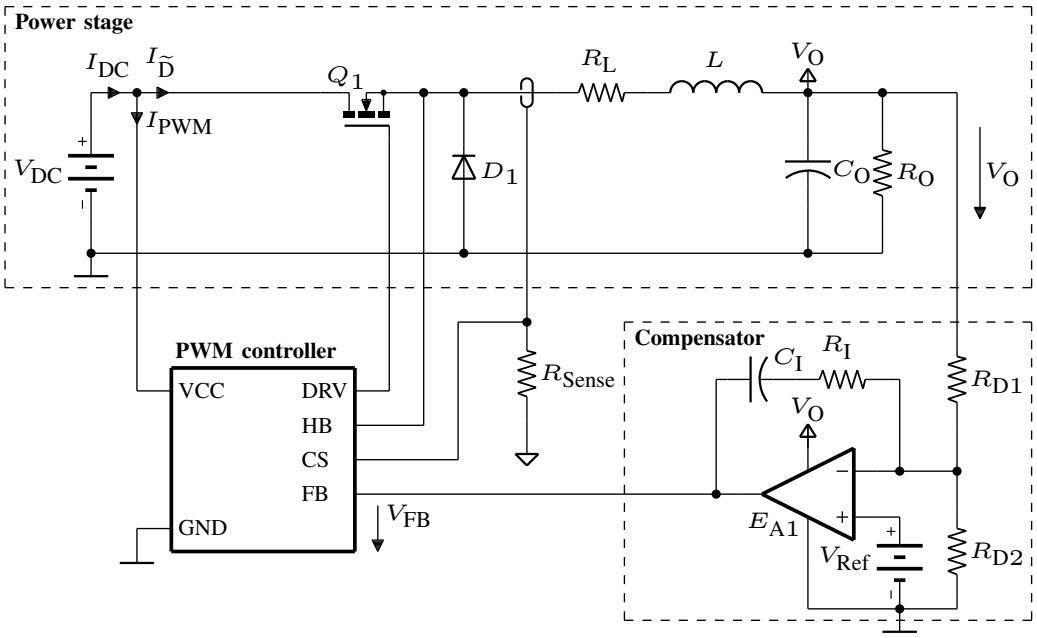

Figure 5.1: Schematic diagram of a closed-loop step down converter with peak current mode control.

5.1 Specification and requirements of the step down converter

The power stage of the step down converter circuit shown in Figure 5.1 should be sized, by calculation and simulation, illustrating the advantages of the analytic solution techniques. The specification is summarized in Table 5.1.

Table 5.1: Specification of the step down converter of Figure 5.1.

Characteristic	Minimum	Typical	Maximum
Product lifetime (operating time) t_L	10 years		
Efficiency η		95 %	
Operating temperature range T_A	0 °C	25 °C	60 °C
Input voltage range V_{DC}	42 V	48 V	52 V
Output current I_{out}	0.1 A	1.0 A	2.0 A
Output voltage V_{out} (V_O)	11.4 V	12 V	12.6 V

Requirements:

1. The typical efficiency η must be $\geq 95\,\%$.
2. The design limits of the MOSFET Q_1 ($Q_{1\,VDS}$, $Q_{1\,IDM}$, and $Q_{1\,TJ}$), the diode D_1 ($D_{1\,VRR}$, $D_{1\,IF(AV)}$, $D_{1\,IFR}$, and $D_{1\,TJ}$), and the output filter capacitor C_O ($C_{O\,V}$ and $C_{O\,IRMS}$) need to stay below their datasheet limits.

5.2 Power stage modeling of the step down converter

The closed-loop step down converter shown in Figure 5.1 is divided into three parts:

- Power stage: includes a real inductance consisting of the inductance L and the winding resistance R_L, a power switch Q_1, the freewheeling diode D_1, and the output filter capacitor C_O. The current through the inductor is measured with a current sensor (the ratio $1 : N_{CT}$, e.g., current transformer) and the output of the current sensor is connected to the current sense resistor R_{Sense}. The power switch Q_1 is modeled as a voltage controlled ideal switch with a resistor $Q_{1\,RDS(on)}$ representing the resistance in the on-region.

- PWM controller: for the control method, peak current mode control with constant switching frequency F_S is chosen and is implemented in the PWM controller block. A detailed structure of the PWM controller is shown in Figure 5.2.

- Compensator: a PI (Type 2 a) compensator [72, 73] is used, containing the error amplifier EA_1 and a voltage reference V_{Ref} to model an adjustable shunt regulator (such as TL431). The error amplifier EA_1 is modeled as an ideal amplifier with infinite gain.

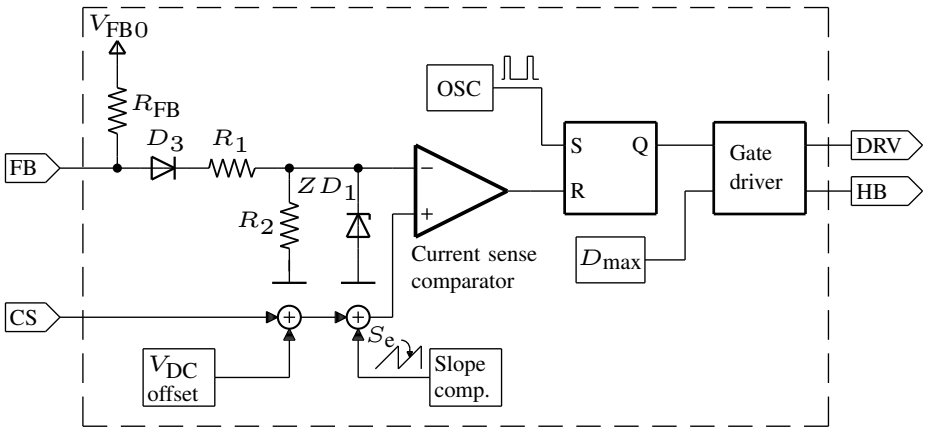

Figure 5.2: Block diagram of the peak current mode PWM controller.

5.2.1 Steady-state analysis

The steady-state analysis of a closed-loop flyback converter has been explored in details in Section 4.2.1. The operating mode of the step down converter for the optimization of the efficiency should not be limited to CCM or DCM, therefore, both modes CCM and DCM must be modeled (supported). The step down converter power stage operating in DCM has three SubCircuit-Models (states):

- State 1: DRV high, MOSFET Q_1 is switched on (saturation) and D_1 is in the OFF-state (reverse bias) with $0 < t \leq t_{on}$.

- State 2: DRV low, MOSFET Q_1 is switched off (cut-off) and D_1 is in the ON-state (forward bias) with $t_{on} < t < t_c$.

- State 3: DRV low, MOSFET Q_1 is switched off (cut-off) and D_1 is in the OFF-state (reverse bias) with $t_c < t < T_S$.

The time t_c indicates the point in time at which the current through the inductor becomes zero. Expressing the initial conditions (i.e., I_{L10}, I_{L20}, I_{L30}, V_{CO10}, V_{CO20}, and V_{CO30}) of state variables as indicated in Section 4.2.1 and using the average voltage $\overline{V_{CO}}$ across the capacitor results in a system of equations with six unknowns I_{L20}, V_{CO10}, V_{CO20}, V_{CO30}, t_{on}, and t_c.[1] The CCM model is derived from the first two states of the DCM model by substituting the time t_c by the switching cycle T_S. The CCM model results in a system of equations of three unknowns I_{L20}, V_{CO20}, and t_{on}. The final step down converter model includes both models and switches to the DCM model when I_{L10} of the CCM model is negative. For improved performance, the systems of equations in analytic form (generated by the analytic forward solver approach) are solved numerically.

5.2.2 Modeling of the switching losses of the MOSFET Q_1

The switching losses of the MOSFET Q_1 are needed for the optimization of the efficiency of the step down converter, as well as to calculate the maximum junction temperature of the MOSFET Q_1. The simulation of the exact switching behavior of the semiconductors is not supported (the analytic forward solver approach bases on switched networks with piecewise-linear models), therefore, an approximation must be used instead. The voltage and current waveforms $V_{DS}(t)$ and $I_D(t)$ during turn-on and turn-off for CCM are approximated by the waveforms shown in Figure 5.3 and Figure 5.4, respectively.[2] In DCM the turn-on losses are zero ($I_L(0) = 0$). The turn-off losses are estimated with the waveforms as shown in Figure 5.4, too.[3]

The analytic forward solver approach provides the steady-state waveforms $V_{DS}(t)$ and $I_D(t)$ of the MOSFET Q_1 for CCM and DCM illustrated in Figure 5.5 and Figure 5.6, respectively. The switching losses of the MOSFET Q_1 are described in (5.1) and (5.2), respectively with $I_{D\,on} = I_{D\,State\,1}(0)$, $I_{D\,off} = I_{D\,State\,1}(t_{on})$, and $V_{DS\,off} = V_{DS\,State\,2}(0)$. The total switching losses of the MOSFET Q_1 are summarized in (5.3).

[1] Due to the DCM mode I_{L10} and I_{L30} are 0.

[2] Theses approximated waveforms use the switching times t_r and t_f mainly available for resistive switching in the MOSFET's datasheet (referred to I_D).

[3] DCM and CCM waveforms for turn-off are equal.

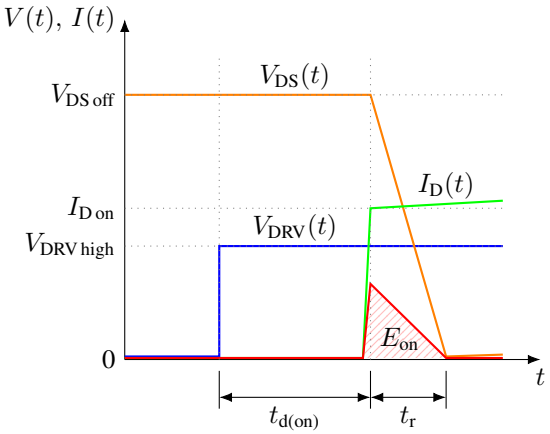

Figure 5.3: Simulated MOSFET switching waveforms during turn-on.

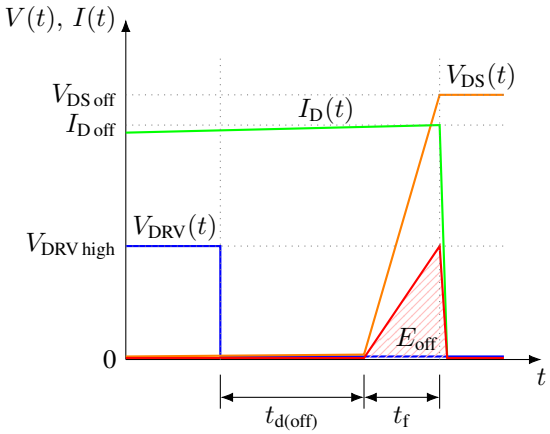

Figure 5.4: Simulated MOSFET switching waveforms during turn-off.

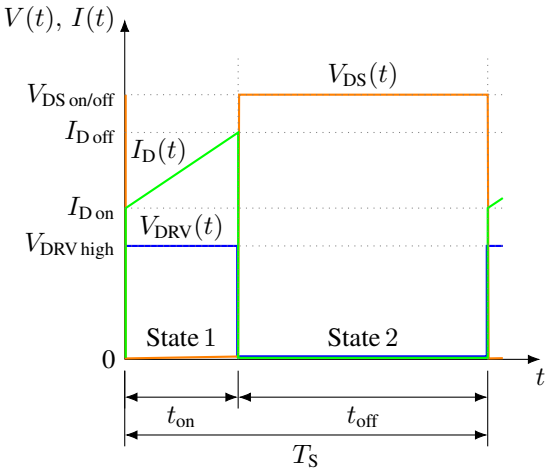

Figure 5.5: Simulated MOSFET switching waveforms for one switching period T_S in CCM.

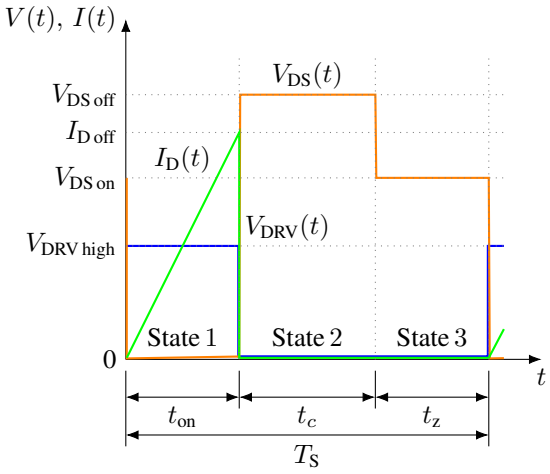

Figure 5.6: Simulated MOSFET switching waveforms for one switching period T_S in DCM.[4]

$$P_{\mathrm{SW\,on}} = \frac{E_{\mathrm{on}}}{T_{\mathrm{S}}} = \frac{1}{T_{\mathrm{S}}} \int_0^{t_{\mathrm{r}}} V_{\mathrm{DS}}(t) I_{\mathrm{D}}(t) \mathrm{d}t = \frac{V_{\mathrm{DS\,off}}\, I_{\mathrm{D\,on}}}{2} \frac{t_{\mathrm{r}}}{T_{\mathrm{S}}} \tag{5.1}$$

$$P_{\mathrm{SW\,off}} = \frac{E_{\mathrm{off}}}{T_{\mathrm{S}}} = \frac{1}{T_{\mathrm{S}}} \int_0^{t_{\mathrm{f}}} V_{\mathrm{DS}}(t) I_{\mathrm{D}}(t) \mathrm{d}t = \frac{V_{\mathrm{DS\,off}}\, I_{\mathrm{D\,off}}}{2} \frac{t_{\mathrm{f}}}{T_{\mathrm{S}}} \tag{5.2}$$

$$P_{\mathrm{SW}} = P_{\mathrm{SW\,on}} + P_{\mathrm{SW\,off}} \tag{5.3}$$

5.2.3 Efficiency calculation

The efficiency of the step down converter is determined by calculation, using (5.4) and simulation.[5] The current consumption of the compensator and the bias current through the resistors R_{D1} and R_{D2} is negligibly small and is assumed to be zero. Therefore, the output power P_{out} can be easily calculated by using (5.5).

$$\eta = \frac{P_{\mathrm{in}} - P_{\mathrm{out}}}{P_{\mathrm{out}}} \tag{5.4}$$

$$P_{\mathrm{out}} = V_{\mathrm{out}} I_{\mathrm{out}} \tag{5.5}$$

The input power P_{in} consists of the switched transferred power P_{T} (5.7) towards the output, the switching losses of the MOSFET Q_1 (5.3) and the total power dissipation of the PWM controller P_{PWM}.[6]

$$P_{\mathrm{in}} = P_{\mathrm{T}} + P_{\mathrm{SW}} + P_{\mathrm{PWM}} \tag{5.6}$$

$$P_{\mathrm{T}} = \frac{1}{T_{\mathrm{S}}} \int_0^{t_{\mathrm{on}}} I_{\mathrm{D}}(t) \mathrm{d}t V_{\mathrm{DC}} \tag{5.7}$$

[4] The inductor current is positive for the time interval t_{c} and zero for the time interval t_{z}.

[5] The analytic forward solver approach provides the steady-state waveform $I_{\mathrm{D}}(t)$ of the MOSFET Q_1 for CCM and DCM.

[6] The current $I_{\widetilde{\mathrm{C}}}$ in Figure 5.1 represents the total current of $P_{\mathrm{T}} + P_{\mathrm{SW}}$.

The supply current of the PWM controller I_{PWM} (5.8), can be decomposed into a constant and a frequency-dependent component.[7] The total power dissipation of the PWM controller P_{PWM} is summarized in (5.9).

$$I_{\mathrm{PWM}} = \max\left(0.35\,10^{-3}, 0.1875\,10^{-3} + 2.5\,10^{-9} F_{\mathrm{S}}\right) + Q_{\mathrm{g}} F_{\mathrm{S}} \tag{5.8}$$

$$P_{\mathrm{PWM}} = \max\left(0.35\,10^{-3}, 0.1875\,10^{-3} + 2.5\,10^{-9} F_{\mathrm{S}}\right) V_{\mathrm{DC}} + Q_{\mathrm{g}} F_{\mathrm{S}} V_{\mathrm{DRV\,high}} \tag{5.9}$$

5.2.4 Calculation of the junction temperature of the MOSFET Q_1

The total losses of the MOSFET Q_1 are obtained by the sum of the switching losses (5.3) and the conduction losses (5.11).[5] The junction temperatures $Q_{1\,\mathrm{TJ}}$ of the MOSFET Q_1 is calculated by (5.12).

$$P_{\mathrm{Total}} = P_{\mathrm{SW}} + P_{\mathrm{Conduction}} \tag{5.10}$$

$$P_{\mathrm{Conduction}} = I^2_{\mathrm{D\,RMS}} R_{\mathrm{DS(on)}} = \frac{1}{T_{\mathrm{S}}} \int_0^{t_{\mathrm{on}}} I^2_{\mathrm{D}}(t)\mathrm{d}t R_{\mathrm{DS(on)}} \tag{5.11}$$

$$Q_{1\,\mathrm{TJ}} = T_{\mathrm{J}} = T_{\mathrm{A}} + R_{\mathrm{th\,JC}} P_{\mathrm{Total}} \tag{5.12}$$

5.2.5 Calculation of the average forward current of the Diode D_1

The average forward current $D_{1\,\mathrm{IF(AV)}}$ of the diode D_1 is calculate by (5.13).[8]

$$D_{1\,\mathrm{IF(AV)}} = \frac{1}{T_{\mathrm{S}}} \int_0^{t_{\widetilde{\mathrm{off}}}} I_{\mathrm{D}}(t)\mathrm{d}t \tag{5.13}$$

[7] The frequency-dependent component is divided into the PWM controller supply current $I_{\mathrm{PWM\,ICC}}(F_{\mathrm{S}})$ and the gate driver current $Q_{\mathrm{g}} F_{\mathrm{S}}$ caused by the total gate charge Q_{g} of the MOSFET Q_1.

[8] The analytic forward solver approach provides the steady-state waveforms $I_{\mathrm{D}}(t)$ of the diode D_1. The time $t_{\widetilde{\mathrm{off}}}$ dependents on the mode of operation (CCM or DCM).

5.2.6 Calculation of the junction temperature of the Diode D_1

The conduction losses of the diode D_1 are obtained by (5.14).[9] The junction temperature $D_{1\,\mathrm{TJ}}$ of the diode D_1 is calculated by (5.15).

$$P_{\mathrm{Conduction}} = \frac{1}{T_{\mathrm{S}}} \int_0^{t_{\widetilde{\mathrm{off}}}} I_{\mathrm{D}}(t) V_{\mathrm{D}}(t) \mathrm{d}t \tag{5.14}$$

$$D_{1\,\mathrm{TJ}} = T_{\mathrm{J}} = T_{\mathrm{A}} + R_{\mathrm{th\,JC}} P_{\mathrm{Conduction}} \tag{5.15}$$

5.2.7 Calculation of the ripple current of the output capacitor C_{O}

The ripple current $C_{\mathrm{O\,IRMS}}$ of the output filter capacitor C_{O} is obtained by (5.16).[10]

$$C_{\mathrm{O\,IRMS}} = I_{\mathrm{C\,RMS}} = \sqrt{\frac{1}{T_{\mathrm{S}}} \int_0^{t_{\mathrm{on}}} I_{\mathrm{C}}^2(t) \mathrm{d}t} \tag{5.16}$$

5.3 Optimization of the efficiency of the step down converter

The efficiency of the step down converter with typical values of the components should be maximized. Before the optimization process can be started the components' parameters must be defined. The semiconductor types for the MOSFET Q_1 and the diode D_1 are preselected.[11] For the MOSFET Q_1, the BSS606N [78], a 60 V/3.2 A type and for the diode D_1, the STPS2H100 [79], a 100 V/2 A power Schottky rectifier type is chosen, respectively. Furthermore, if all the requirements in the specification are met, the parts can be considered suitable. For the winding resistance R_{L} of the real inductance an upper limit is used for the optimization. The real inductor is chosen after the optimization process. Table 5.2 summarizes the values

[9] The switching losses P_{SW} as well as the reverse recovery charge Q_{rr} of the Schottky diode are negligible small and were not considered. The analytic forward solver approach provides the steady-state waveforms $I_{\mathrm{D}}(t)$ and $V_{\mathrm{D}}(t)$ of the diode D_1. The time $t_{\widetilde{\mathrm{off}}}$ depends on the mode of operation (CCM or DCM).

[10] The analytic forward solver approach provides the steady-state waveform $I_{\mathrm{C}}(t)$ of the output filter capacitor C_{O} for CCM and DCM.

[11] For lowest costs, standard components with small packages are preferred.

Table 5.2: Component values and SQP parameters for optimizing the efficiency of the step down converter of Figure 5.1.

Components values	Parameter x_i	Lower bound	Upper bound
$V_{DC} = 48\,V$	F_S	$F_{S\,min} = 30\,kHz$	$F_{S\,max} = 300\,kHz$
$R_L = 0.07\,\Omega$	L	$L_{min} = 25\,\mu H$	$L_{max} = 50\,\mu H$
$Q_{1\,RDS(on)} = 0.047\,\Omega$			
$Q_{1\,tr} = 2.6\,ns$, $Q_{1\,tf} = 2.1\,ns$			
$Q_{1\,Qg} = 5\,nC$, $V_{DRV\,high} = 10\,V$			
$D_{1\,VF} = 0.6\,V$, $D_{1\,RD} = 0.045\,\Omega$			
$R_O = 12\,\Omega$, $C_O = 470\,\mu F$			

of the components and the SQP parameters. The values of the MOSFET Q_1 and the diode D_1 are taken from the datasheets. The maximum efficiency η in steady-state should be determined as a function of two parameters, e.g., F_S and L. The objective function for the maximum is

$$f(\mathbf{x}) = \eta_{max}(\mathbf{x}) = -\eta(F_S, L)\,. \tag{5.17}$$

The 3-D plot of the objective function $\eta_{max}(F_S, L)$ (5.17) including the solution path of the SQP method is illustrated in Figure 5.7. The efficiency η decreases both at lower and at higher frequencies. At lower frequencies, the conduction losses of the Diode D_1 (losses caused by $D_{1\,RD}$) and the MOSFET Q_1 dominate (higher RMS currents). On the other hand, at higher frequencies, the switching losses of the MOSFET Q_1 and PWM controller increase. The efficiency η also increases with the inductance, as this reduces the conduction losses of the Diode D_1 and the MOSFET Q_1.

The implemented SQP method converges to the maximum after 3 iterations (summarized in Table 5.3) with $\eta = 95.1\,\%$. For the inductor L a 47 μH/3.3 A type (closest standard value) is chosen. The typical winding resistance R_L of the chosen inductor is 0.0612 Ω. This value is smaller than the upper limited 0.07 Ω as it was used for the optimization of the efficiency. The switching frequency F_S was rounded to 130 kHz.

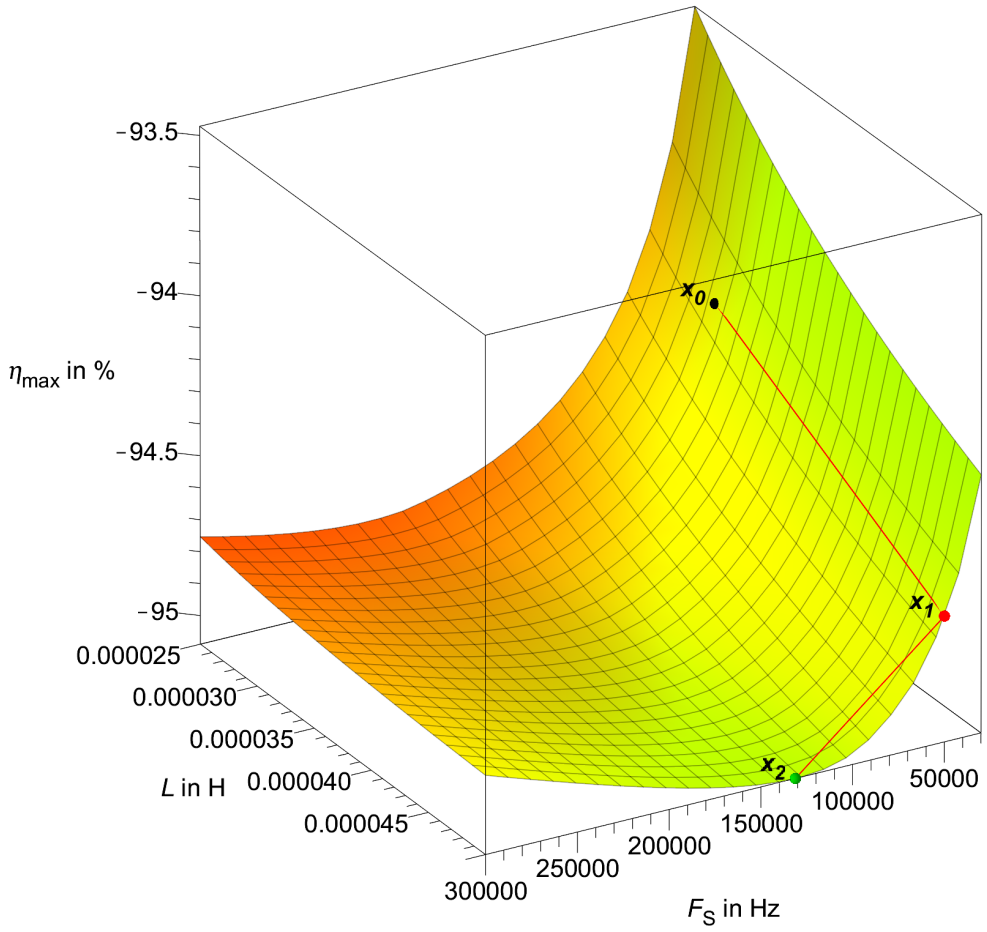

Figure 5.7: Step down converter $\eta_{\max}(F_S, L)$.

Table 5.3: SQP method for $\eta_{\max}$ optimization.

k	1	2	3
$F_S^{(k)}$ in kHz	50.0	50.0	131.2
$L^{(k)}$ in μH	30.0	50.0	50.0
$\eta_{\max}^{(k)}$ in %	−94.2	−94.7	−95.1

5.4 Design limits of the individual components

The design limits of the individual components of the step down converter in steady-state are determined by applying the SQP method in combination with the analytic forward solver approach. The SQP parameters to identify the design limits of the individual components and the ambient temperature are summarized in Table 5.4.

Table 5.4: SQP parameters to identify the design limits of the individual components and the ambient temperature of the step down converter of Figure 5.1.

Ambient temperature	Parameter x_i	Lower bound	Upper bound
$T_A = 60\,°C$[1]	V_{DC}	$V_{DC\,min} = 42\,V$	$V_{DC\,max} = 52\,V$
	V_{out}	$V_{out\,min} = 11.4\,V$	$V_{out\,max} = 12.6\,V$
	R_O	$R_{O\,min} = 6\,\Omega$	$R_{O\,max} = 120\,\Omega$
	F_S	$F_{S\,min} = 123\,kHz$	$F_{S\,max} = 137\,kHz$
	L	$L_{min} = 35.2\,\mu H$	$L_{max} = 58.8\,\mu H$
	R_L	$R_{L\,min} = 0.04\,\Omega$	$R_{L\,max} = 0.072\,\Omega$
	$D_{1\,VF}$	$D_{1\,VF\,min} = 0.46\,V$	$D_{1\,VF\,max} = 0.79\,V$
	$D_{1\,RD}$	$D_{1\,RD\,min} = 0.036\,\Omega$	$D_{1\,RD\,max} = 0.054\,\Omega$
	$Q_{1\,RDS(on)}$	$Q_{1\,RDS(on)\,min} = 0.034\,\Omega$	$Q_{1\,RDS(on)\,max} = 0.06\,\Omega$
	C_O	$C_{O\,min} = 235\,\mu F$	$C_{O\,max} = 564\,\mu F$
	$Q_{1\,tr}$[2]	$Q_{1\,tr\,min} = 1.3\,ns$	$Q_{1\,tr\,max} = 3.9\,ns$
	$Q_{1\,tf}$[2]	$Q_{1\,tf\,min} = 1.05\,ns$	$Q_{1\,tf\,max} = 3.15\,ns$

[1] The ambient temperature is only used for the calculation of $Q_{1\,TJ}$ and $D_{1\,TJ}$.

[2] This parameter is only used for calculation $Q_{1\,TJ}$ in Section 5.4.1.

5.4.1 Design limits of the MOSFET Q_1

The design limits of the MOSFET Q_1 i.e., $Q_{1\,\mathrm{VDS}}$, $Q_{1\,\mathrm{IDM}}$, and $Q_{1\,\mathrm{TJ}}$ must be determined and need to stay below the datasheet limits. The pulse drain current $Q_{1\,\mathrm{IDM}}$ is the same as the maximum through the inductor L.[12] The objective function for the pulse drain current is

$$f(\mathbf{x}) = -Q_{1\,\mathrm{IDM}}(\mathbf{x}) = -I_{\mathrm{L}\,20}\,. \tag{5.18}$$

Section 5.2.4 describes the calculation of the junction temperature $Q_{1\,\mathrm{TJ}}$ in detail. The objective function is built from (5.12) and is summarized in

$$f(\mathbf{x}) = -Q_{1\,\mathrm{TJ}}(\mathbf{x})\,. \tag{5.19}$$

Table 5.5: Maximum ratings (datasheet parameters) for the MOSFET Q_1 and the design limits for the closed-loop step down converter in steady-state of Figure 5.1.

Symbol	Parameter	Datasheet limits	Design limits
$V_{(\mathrm{BR})\mathrm{VSS}}$	Drain-source breakdown voltage	60 V	53 V[1]
I_{DM}	Drain current (pulsed)	12.8 A	3.223 A[2]
T_{J}	Maximum junction temperature	150 °C	77.2 °C[3]
$R_{\theta\mathrm{JA}}$	Thermal resistance, junction to ambient	125 °C/W	-

[1] $Q_{1\,\mathrm{VDS}} = V_{\mathrm{DC\,max}} + D_{1\,\mathrm{VF\,max}} + D_{1\,\mathrm{RD\,max}} Q_{1\,\mathrm{IDM}} = 53\,\mathrm{V}$
[2] $Q_{1\,\mathrm{IDM}} = 3.223\,\mathrm{A}$, limit determined with SQP method summarized in Table A.1.
[3] $Q_{1\,\mathrm{TJ}} = 77.2\,^{\circ}\mathrm{C}$, limit determined with SQP method summarized in Table A.2.

The current rating of the chosen inductor L in Section 5.3 is greater than the design limit $I_{\mathrm{L}\,20}$ and therefore suitable.

5.4.2 Design limits of the diode D_1

The design limits of the diode D_1 i.e., $D_{1\,\mathrm{VRR}}$, $D_{1\,\mathrm{IF(AV)}}$, $D_{1\,\mathrm{IFR}}$, and $D_{1\,\mathrm{TJ}}$ must be determined and need to stay below the datasheet limits. The peak repetitive forward current $D_{1\,\mathrm{IFR}}$ is the same as I_{DM} the maximum pulse current through the MOSFET

[12] $I_{\mathrm{L}\,20}$ has been described in Section 5.2.1.

Q_1. The calculation of the average forward current $D_{1\,\mathrm{IF(AV)}}$ is described in (5.13). The objective function for the average forward current is

$$f(\mathbf{x}) = -D_{1\,\mathrm{IF(AV)}}(\mathbf{x})\,. \tag{5.20}$$

Section 5.2.6 describes the calculation of the junction temperature $D_{1\,\mathrm{TJ}}$ in detail. The objective function is built from (5.15) and is summarized in

$$f(\mathbf{x}) = -D_{1\,\mathrm{TJ}}(\mathbf{x})\,. \tag{5.21}$$

Table 5.6: Maximum ratings (datasheet parameters) for the Schottky diode D_1 and the design limits for the closed-loop step down converter in steady-state of Figure 5.1.

Symbol	Parameter	Datasheet limits	Design limits
V_{RRM}	Peak repetitive reverse voltage	100 V	52 V[1]
$I_{\mathrm{F(AV)}}$	Average rectified forward current	2 A	1.57 A[2]
I_{FRM}	Peak repetitive forward current	30 A	3.223 A[3]
T_{J}	Maximum junction temperature	175 °C	135.5 °C[4]
$R_{\theta\mathrm{JA}}$	Thermal resistance, junction to ambient	53 °C/W	-

[1] $D_{1\mathrm{VRR}} = V_{\mathrm{DC\,max}} = 52$ V
[2] $D_{1\,\mathrm{IF(AV)}} = 1.57$ A, limit determined with SQP method summarized in Table A.3.
[3] $D_{1\,\mathrm{IFR}} = Q_{1\,\mathrm{IDM}} = 3.223$ A, limit determined with SQP method summarized in Table A.1.
[4] $D_{1\,\mathrm{TJ}} = 135.5$ °C, limit determined with SQP method summarized in Table A.4.

5.4.3 Design limits of the output capacitor C_{O}

The design limits of the capacitor C_{O} i.e., $C_{\mathrm{O\,V}}$, and $C_{\mathrm{O\,IRMS}}$ must be determined and need to stay below its datasheet limits. The calculation of the ripple current $C_{\mathrm{O\,IRMS}}$ is described in (5.16). The objective function for the ripple current is

$$f(\mathbf{x}) = -C_{\mathrm{O\,IRMS}}(\mathbf{x})\,. \tag{5.22}$$

Table 5.7: Maximum ratings (datasheet parameters) for the capacitor C_O and the design limits for the closed closed-loop step down converter of Figure 5.1.

Symbol	Parameter	Datasheet limits	Design limits
V_R	Rated DC voltage	16 V	12.6 V[1]
I_{RMS}	Rated ripple current 100 kHz, 105 °C	0.73 A	0.647 A[2]
L	Calculated life time 100 kHz, 60 °C	90510 h[3]	87600 h
T_{max}	Rated temperature	105 °C	-
L_o	Endurance with rated ripple current at 105 °C	4000 h	-

[1] $C_{O\,VR} = V_{out\,max} = 12.6$ V

[2] $C_{O\,IRMS} = 0.647$ A, limit determined with SQP method summarized in Table A.5.

[3] $L = L_o 2^{\frac{T_{max}-T_{A\,max}}{10}} = 90510$ h [80]

5.5 Conclusion

The power stage of the step down converter circuit shown in Figure 5.1 is sized, by calculation and simulation, illustrating the advantages of the analytic solution techniques. The efficiency (requirement) of the step down converter is optimized. The design limits for the MOSFET Q_1, the diode D_1, and the output filter capacitor C_O are calculated and summarized in Table 5.5, Table 5.6, and Table 5.7. All its parts, i.e., the inductor L, the MOSFET Q_1, the Schottky diode D_1, and the output filter capacitor C_O are used within their specifications.

Chapter 6

Conclusion

6.1 Summary

AnSim is the basis of the design tool that comprises the proposed analytic forward solver approach, and an optimizer package, which are all introduced within the context of this thesis. This tool is notably suitable for parameter studies, optimization, and worst-case sizing of small-scale electronic circuits. An overview of standard simulators which use complex nonlinear models like SPICE and simulators based on switched networks with piecewise-linear models is provided. The proposed approach, a resource efficient precision transient circuit simulator without a time step for solving the systems of differential equations, is presented. A closed-form analytic solution is computed for each of the electronic circuit states. The proposed approach returns the analytic functions of the state variables and the signals of interest instead of discrete values. This creates the opportunity to investigate certain intervals of time in detail without re-simulating the whole circuit. Numerical integration is not required, and therefore, convergence problems are eliminated.

An electronic circuit with only linear elements, for example, R, C, L, and independent current, and voltage sources, is described with a SubCircuit-Model. The SubCircuit-Model, an extended symbolic state-space model, is explained in detail. The I/O interface for the dynamic interconnection of a Subcircuit-Model is presented theoretically and is subsequently explained in more detail by means of a simple example. Nonlinear elements, such as $L(i)$, $C(u)$, Diodes, MOSFETs, BJTs, and/or PWM controllers are described with Circuit-Models. Based on the SubCircuit-Model for linear elements, the Circuit-Model for piecewise-linear elements is discussed. Connecting linear and linearized nonlinear elements, results in a linear system of differential equations, and which is described again with a Subcircuit-Model.

With respect to accuracy, the proposed approach performs similarly to established simulators, and the simulation results are well in line with the experimental ones. This was demonstrated by two examples, an open-loop flyback and a closed-loop flyback converter. In these special cases, the CPU times of the proposed approach were longer than those of the two other simulators (e.g., ≈ 14.8, 2.1) and (e.g., ≈ 5.8, 6.5); however, the data file sizes are significantly smaller than those of the other two (e.g., ≈ $1/8$, $1/3850$) and (e.g., ≈ $1/15$, $1/64$). Superior performance in terms of total CPU time was shown for a parameter study of an open-loop ideal flyback converter. In this case, the total CPU time of the proposed approach is significantly shorter than that of the other two simulators (e.g., ≈ $1/4$, $1/69$), illustrating the advantage of the analytic solution (approach). The proposed tool has been developed to determine the design limits of the device and design limits of the individual components, respectively, by parametric simulation (scanning tool). The proposed tool can be coupled with an optimizer to identify, e.g., these worst-case values in a few steps.

The SQP method in combination with the proposed analytic forward solver approach shows that the identification of the worst-case values converges in a few steps even if the worst-case values are not on the boundary of the parameters. Based on the proposed analytic forward solver approach, it is possible to reduce a flyback converter in steady-state from a closed-loop to an open-loop system. These results are well in line with the transient simulation results obtained by applying the proposed analytic forward solver approach to the open loop flyback converter. With respect to accuracy, the SQP method shows similar performance to an (1+1) ES strategy. Superior performance in terms of total CPU time was shown here, too. The total CPU time of the SQP method is significantly shorter than that of the other two methods, i.e., MC and (1+1) ES (e.g., $MC_{k=1000} \approx 1/9$,$MC_{k=10000} \approx 1/95$, (1+1) ES ≈ $1/7$).

The flexible applicability and implementation of the SQP method in combination with the proposed analytic forward solver approach was demonstrated by sizing of a step down converter illustrating the advantages of the analytic solution techniques. First, the SQP method was used in combination with the analytic forward solver approach to optimize the efficiency of the step down converter. In the second step, the different components of the step down converter were sized by applying the SQP method in combination with the analytic forward solver approach.

6.2 Future work

In the future, AnSim may be expanded to allow further exploitation of its benefits. Several component-specific libraries should be derived from the datasheets of the individual components. These libraries should provide the worst-case parameter models for the circuit elements. Notably libraries for resistors[1] (e.g., thick film, thin film, and carbon film resistors), capacitors[2] (e.g., ceramic capacitors, film capacitor, and aluminum electrolytic capacitors and semiconductors (e.g., diodes[3], BJTs[4], and MOSFETs[5]) may be developed. In addition, thermal models of the parameters should be implemented so that their thermal behaviors can be modeled.

[1] These models should include the resistance basic tolerance, the resistance change due to temperature, the resistance change due to soldering heat, and the resistance change due to aging.

[2] These models should include the capacitance basic tolerance, the capacitance change due to the DC bias, the capacitance change due to temperature, the resistance change due the frequency and the capacitance change due to aging. In addition, also a model for the equivalent series resistance (ESR) with different parameters (e.g., temperature T_C, frequency f, and aging t_L) should be included, too.

[3] The forward voltage worst-case parameter model of a diode described by (1.5), should be derived for different diodes.

[4] A model for, e.g., base-emitter voltage V_{BE} and DC current gain h_{FE}.

[5] A model for, e.g., drain-source on-state resistance $R_{DS(on)}$.

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Appendix A

Step down converter SQP iterations of the individual components

Table A.1: SQP iterations to identify the maximum $Q_{1\,\mathrm{IDM}}$ on the closed-loop step down converter of Figure 5.1.

k	1	2	3	4	5	6	7	8	9	10	11
$V_{\mathrm{DC}}^{(k)}$ in V	48.0	48.0	48.0	48.0	48.0	48.0	48.0	48.2	48.5	52.0	52.0
$V_{\mathrm{out}}^{(k)}$ in V	12.0	12.0	12.0	12.0	12.0	12.0	12.5	12.6	12.6	12.6	12.6
$R_{\mathrm{O}}^{(k)}$ in Ω	12.0	12.0	12.0	12.0	12.0	12.0	11.7	11.6	6.0	6.0	6.0
$F_{\mathrm{S}}^{(k)}$ in kHz	135	135	135	135	135	135	135	135	135	135	128
$L^{(k)}$ in μH	47.0	35.2	35.2	35.2	35.2	35.2	35.2	35.2	35.2	35.2	35.2
$R_{\mathrm{L}}^{(k)}$ in $m\Omega$	61.2	61.2	61.3	70.2	72.0	72.0	72.0	72.0	72.0	72.0	72.0
$D_{1\,\mathrm{VF}}^{(k)}$ in V	0.60	0.60	0.60	0.61	0.61	0.61	0.79	0.79	0.79	0.79	0.79
$D_{1\,\mathrm{RD}}^{(k)}$ in mΩ	45.0	45.0	45.1	54.0	54.0	54.0	54.0	54.0	54.0	54.0	54.0
$Q_{1\,\mathrm{RDS(on)}}^{(k)}$ in mΩ	47.0	47.0	47.0	37.9	37.6	34.0	34.0	34.0	34.0	34.0	34.0
$C_{\mathrm{O}}^{(k)}$ in μF	470	470	376	376	376	376	376	376	376	376	376
$-Q_{1\,\mathrm{IDM}}^{(k)}$ in A	1.74	1.988	1.988	1.991	1.992	1.993	2.096	2.122	3.14	3.166	3.223

Table A.2: SQP iterations to identify the maximum $Q_{1\,\mathrm{TJ}}$ on the closed-loop step down converter of Figure 5.1.

k	1	2	3	4	5	6	7	8	9	10	11	12	13
$V_{\mathrm{DC}}^{(k)}$ in V	48.0	48.0	48.0	48.0	48.0	48.0	48.0	48.0	48.0	48.4	48.4	42.0	42.0
$V_{\mathrm{out}}^{(k)}$ in V	12.0	12.0	12.0	12.0	12.0	12.0	12.0	12.0	12.6	12.6	12.6	12.6	12.6
$R_{\mathrm{O}}^{(k)}$ in Ω	12.0	12.0	12.0	12.0	12.0	12.0	12.0	12.0	11.7	11.6	6.0	6.0	6.0
$F_{\mathrm{S}}^{(k)}$ in kHz	135	135	135	135	135	135	135	135	135	135	135	135	142
$L^{(k)}$ in μH	47.0	47.0	47.0	35.2	35.2	35.2	35.2	35.2	35.2	35.2	35.2	35.2	35.2
$R_{\mathrm{L}}^{(k)}$ in $m\Omega$	61.2	61.2	61.2	61.2	61.3	61.3	68.1	72.0	72.0	72.0	72.0	72.0	72.0
$D_{1\,\mathrm{VF}}^{(k)}$ in V	0.60	0.60	0.60	0.60	0.60	0.60	0.60	0.61	0.67	0.79	0.79	0.79	0.79
$D_{1\,\mathrm{RD}}^{(k)}$ in mΩ	45.0	45.0	45.0	45.0	45.1	45.2	54.0	54.0	54.0	54.0	54.0	54.0	54.0
$Q_{1\,\mathrm{RDS(on)}}^{(k)}$ in mΩ	47.0	47.0	47.0	47.0	60.0	60.0	60.0	60.0	60.0	60.0	60.0	60.0	60.0
$C_{\mathrm{O}}^{(k)}$ in μF	470	470	470	470	457	376	376	376	376	376	376	376	376
$Q_{1\,\mathrm{tr}}^{(k)}$ in ns	2.6	3.9	3.9	3.9	3.9	3.9	3.9	3.9	3.9	3.9	3.9	3.9	3.9
$Q_{1\,\mathrm{tf}}^{(k)}$ in ns	2.1	2.3	3.15	3.15	3.15	3.15	3.15	3.15	3.15	3.15	3.15	3.15	3.15
$-Q_{1\,\mathrm{TJ}}^{(k)}$ in °C	64.0	64.9	64.9	65.2	65.8	65.8	65.9	65.9	66.6	66.7	76.5	77.0	77.2

Table A.3: SQP iterations to identify the maximum $D_{1\,\mathrm{IF(AV)}}$ on the closed-loop step down converter of Figure 5.1.

k	1	2	3	4	5	6	7	8	9	10	11	12
$V_{\mathrm{DC}}^{(k)}$ in V	48.0	48.0	48.0	48.0	48.0	48.0	48.0	48.1	48.2	48.9	52.0	52.0
$V_{\mathrm{out}}^{(k)}$ in V	12.0	12.0	12.0	12.0	12.0	12.0	12.0	12.5	12.6	12.6	12.6	12.6
$R_{\mathrm{O}}^{(k)}$ in Ω	12.0	12.0	12.0	12.0	12.0	12.0	12.0	11.5	11.3	6.0	6.0	6.0
$F_{\mathrm{S}}^{(k)}$ in kHz	135.0	135.0	135.0	135.0	135.0	135.0	135.0	135.0	135.0	135.0	135.0	128.2
$L^{(k)}$ in μH	47.0	58.8	58.8	58.8	58.8	58.8	58.8	58.8	58.8	58.8	58.8	58.8
$R_{\mathrm{L}}^{(k)}$ in $m\Omega$	61.2	61.2	50.4	50.4	50.4	50.4	50.4	50.4	50.4	50.4	50.4	50.4
$D_{1\,\mathrm{VF}}^{(k)}$ in V	0.600	0.600	0.593	0.592	0.592	0.591	0.582	0.460	0.460	0.460	0.460	0.460
$D_{1\,\mathrm{RD}}^{(k)}$ in mΩ	45.0	45.0	37.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0
$Q_{1\,\mathrm{RDS(on)}}^{(k)}$ in mΩ	47.0	47.0	44.2	43.4	43.3	42.2	34.0	34.0	34.0	34.0	34.0	34.0
$C_{\mathrm{O}}^{(k)}$ in μF	470.0	470.0	484.4	487.7	564.0	564.0	564.0	564.0	564.0	564.0	564.0	564.0
$-D_{1\,\mathrm{IF(AV)}}^{(k)}$ in A	0.709	0.738	0.741	0.742	0.742	0.742	0.743	0.791	0.814	1.54	1.57	1.57

Table A.4: SQP iterations to identify the maximum $D_{1\,\mathrm{TJ}}$ on the closed-loop step down converter of Figure 5.1.

k	1	2	3	4	5	6	7	8	9	10	11	12
$V_{\mathrm{DC}}^{(k)}$ in V	48.0	48.0	48.0	48.0	48.0	48.0	48.0	48.0	48.6	46.2	52.0	52.0
$V_{\mathrm{out}}^{(k)}$ in V	12.0	12.0	12.0	12.0	12.0	12.0	12.0	12.2	12.6	12.6	12.6	12.6
$R_{\mathrm{O}}^{(k)}$ in Ω	12.0	12.0	12.0	12.0	12.0	11.9	11.9	11.7	11.3	6.0	6.0	6.0
$F_{\mathrm{S}}^{(k)}$ in kHz	135.0	135.0	135.0	135.0	135.0	135.0	135.0	135.0	135.0	135.0	135.0	128.2
$L^{(k)}$ in μH	47.0	35.2	35.2	35.2	35.2	35.2	35.2	35.2	35.2	35.2	35.2	35.2
$R_{\mathrm{L}}^{(k)}$ in $m\Omega$	61.2	61.2	61.0	61.0	72.0	53.7	50.4	50.4	50.4	50.4	50.4	50.4
$D_{1\,\mathrm{VF}}^{(k)}$ in V	0.600	0.600	0.607	0.607	0.671	0.790	0.790	0.790	0.790	0.790	0.790	0.790
$D_{1\,\mathrm{RD}}^{(k)}$ in mΩ	45.0	45.0	54.0	54.0	54.0	54.0	54.0	54.0	54.0	54.0	54.0	54.0
$Q_{1\,\mathrm{RDS(on)}}^{(k)}$ in mΩ	47.0	47.0	47.0	46.9	59.2	54.5	50.7	34.0	34.0	34.0	34.0	34.0
$C_{\mathrm{O}}^{(k)}$ in μF	470.0	470.0	435.9	376.0	376.0	376.0	376.0	376.0	376.0	376.0	376.0	376.0
$-D_{1\,\mathrm{TJ}}^{(k)}$ in °C	84.54	85.79	86.52	86.52	88.92	93.77	93.79	94.71	97.1	132.1	135.4	135.5

Table A.5: SQP iterations to identify the maximum $C_{\mathrm{O\,IRMS}}$ on the closed-loop step down converter of Figure 5.1.

k	1	2	3	4	5	6	7	8	9	10	11	12
$V_{\mathrm{DC}}^{(k)}$ in V	48.0	48.0	48.0	48.0	48.0	48.0	48.0	48.0	48.2	52.0	52.0	52.0
$V_{\mathrm{out}}^{(k)}$ in V	12.0	12.0	12.0	12.0	12.0	12.0	12.2	12.1	12.6	12.6	12.6	12.6
$R_{\mathrm{O}}^{(k)}$ in Ω	12.0	12.0	12.0	12.0	12.0	12.0	12.0	11.6	11.5	11.2	6.0	6.0
$F_{\mathrm{S}}^{(k)}$ in kHz	135.0	135.0	135.0	135.0	135.0	135.0	135.0	135.0	135.0	135.0	135.0	128.2
$L^{(k)}$ in μH	47.0	35.2	35.2	35.2	35.2	35.2	35.2	35.2	35.2	35.2	35.2	35.2
$R_{\mathrm{L}}^{(k)}$ in $m\Omega$	61.2	61.2	61.2	70.1	72.0	72.0	72.0	72.0	72.0	72.0	72.0	72.0
$D_{1\,\mathrm{VF}}^{(k)}$ in V	0.600	0.600	0.600	0.609	0.611	0.614	0.790	0.790	0.790	0.790	0.790	0.790
$D_{1\,\mathrm{RD}}^{(k)}$ in mΩ	45.0	45.0	45.0	54.0	54.0	54.0	54.0	54.0	54.0	54.0	54.0	54.0
$Q_{1\,\mathrm{RDS(on)}}^{(k)}$ in mΩ	47.0	47.0	47.0	37.4	37.2	34.0	34.0	34.0	34.0	34.0	34.0	34.0
$C_{\mathrm{O}}^{(k)}$ in μF	470.0	470.0	376.0	376.0	376.0	376.0	376.0	376.0	376.0	376.0	376.0	376.0
$-C_{\mathrm{O\,IRMS}}^{(k)}$ in A	0.427	0.569	0.569	0.571	0.571	0.571	0.581	0.581	0.594	0.611	0.614	0.647

Appendix B

Semiconductor modeling

B.1 Diode

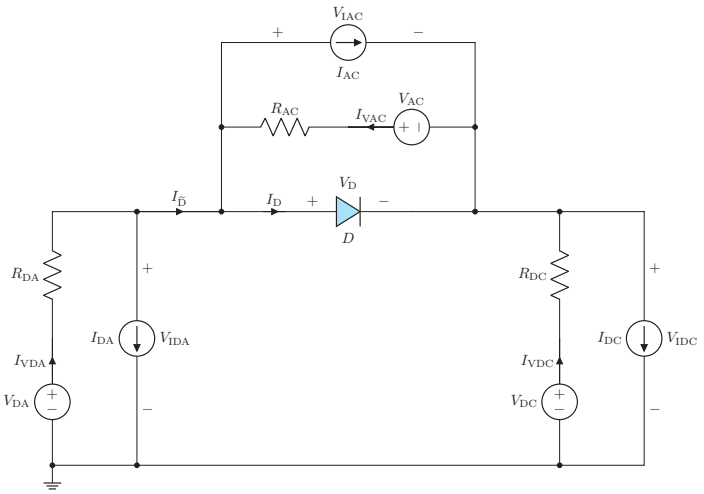

Figure B.1: Diode Circuit-Model with I/O interface.

B.1.1 Diode model parameters

V_F Forward voltage
R_D Differential resistance in forward region
V_B Breakdown voltage (reverse breakdown knee voltage)[1]
R_B Differential resistance in breakdown region[1]
I_R Reverse current

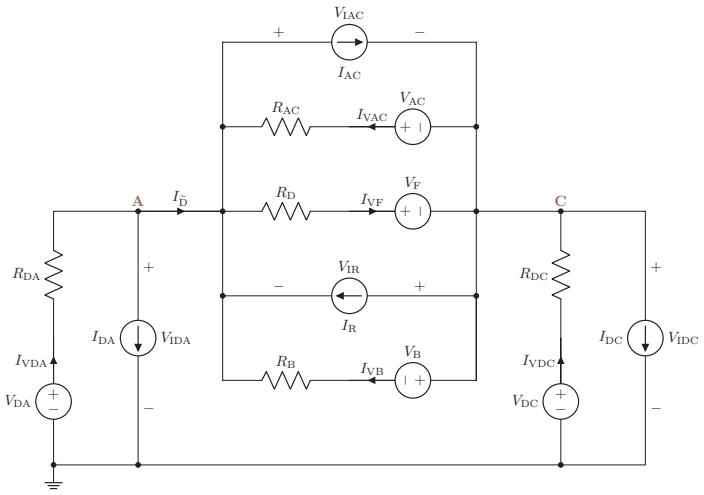

Figure B.2: Universally applicable diode SubCircuit-Model.

Table B.1: Diode level 0 state table and parameter settings of Figure B.2.

State i	State description	Parameters	Boundary conditions	State $i+1$
1	Reverse bias region	$I_{VF} = 0$ $I_{VB} = 0$	$V_{IAC}(0) > V_F$ $V_{IAC}(t) = V_F$	2 2
2	Forward bias region	$I_{VB} = 0$	$I_{VF}(0) < 0$ $I_{VF}(t) = 0$	1 1

[1]Diode level 1 only.

Table B.2: Diode level 1 state table and parameter settings of Figure B.2.

State i	State description	Parameters	Boundary conditions	State $i+1$
1	Reverse bias region	$I_{VF} = 0$ $I_{VB} = 0$	$V_{IAC}(0) > V_F$ $V_{IAC}(t) = V_F$ $V_{IAC}(0) < V_B$ $V_{IAC}(t) = V_B$	2 2 3 3
2	Forward bias region	$I_{VB} = 0$	$I_{VF}(0) < 0$ $I_{VF}(t) = 0$	1 1
3	Reverse breakdown region	$I_{VF} = 0$	$I_{VB}(0) < 0$ $I_{VB}(t) = 0$	1 1

B.1.2 Diode I/O interface

$$\mathbf{y}_{\mathrm{IO\,VDA}}(t) = \begin{bmatrix} \mathbf{y}_{\mathrm{I1}}(t) \\ \mathbf{y}_{\mathrm{O1}}(t) \end{bmatrix} \quad \text{with} \quad \mathbf{y}_{\mathrm{I1}}(t) = \begin{bmatrix} I_{\mathrm{VDA}} \\ V_{\mathrm{DA}} \end{bmatrix} \quad \mathbf{y}_{\mathrm{O1}}(t) = \begin{bmatrix} I_{\mathrm{DA}} \\ V_{\mathrm{IDA}} \end{bmatrix}$$

$$\mathbf{y}_{\mathrm{IO\,VAC}}(t) = \begin{bmatrix} \mathbf{y}_{\mathrm{I2}}(t) \\ \mathbf{y}_{\mathrm{O2}}(t) \end{bmatrix} \quad \text{with} \quad \mathbf{y}_{\mathrm{I2}}(t) = \begin{bmatrix} I_{\mathrm{VAC}} \\ V_{\mathrm{AC}} \end{bmatrix} \quad \mathbf{y}_{\mathrm{O2}}(t) = \begin{bmatrix} I_{\mathrm{AC}} \\ V_{\mathrm{IAC}} \end{bmatrix}$$

$$\mathbf{y}_{\mathrm{IO\,VDC}}(t) = \begin{bmatrix} \mathbf{y}_{\mathrm{I3}}(t) \\ \mathbf{y}_{\mathrm{O3}}(t) \end{bmatrix} \quad \text{with} \quad \mathbf{y}_{\mathrm{I3}}(t) = \begin{bmatrix} I_{\mathrm{VDC}} \\ V_{\mathrm{DC}} \end{bmatrix} \quad \mathbf{y}_{\mathrm{O3}}(t) = \begin{bmatrix} I_{\mathrm{DC}} \\ V_{\mathrm{IDC}} \end{bmatrix} \tag{B.1}$$

B.2 MOSFET

B.2.1 MOSFET model parameters

$V_{\mathrm{GS(th)}}$ Zero-bias threshold voltage
$R_{\mathrm{DS(on)}}$ Static drain-source on resistance
$R_{\mathrm{DS(off)}}$ Static drain-source off resistance

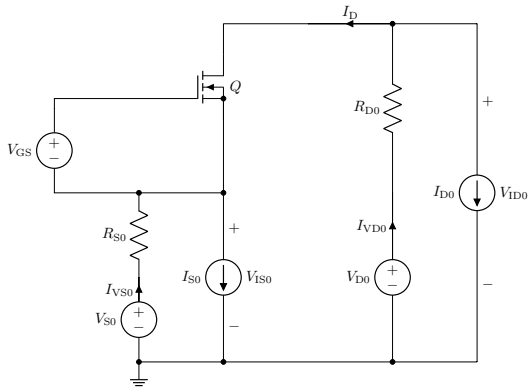

Figure B.3: N-channel MOSFET Circuit-Model with I/O interface.

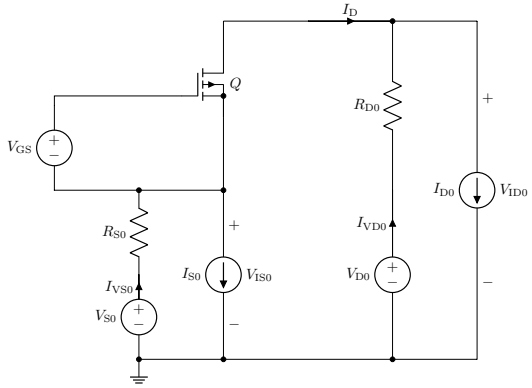

Figure B.4: P-channel MOSFET Circuit-Model with I/O interface.

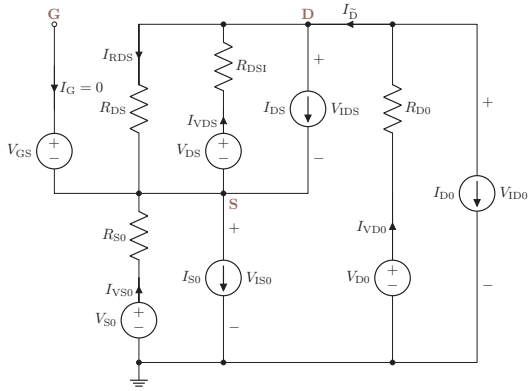

Figure B.5: Universally applicable MOSFET SubCircuit-Model.

Table B.3: N-channel MOSFET state table and parameter settings of Figure B.5.

State i	State description	Parameters	Boundary conditions	State $i+1$
1	Cut-off region	$R_{DS} = R_{DS(off)}$	$V_{GS}(0) > V_{GS(th)}$ $V_{GS}(t) = V_{GS(th)}$	2 2
2	Saturation region	$R_{DS} = R_{DS(on)}$	$V_{GS}(0) < V_{GS(th)}$ $V_{GS}(t) = V_{GS(th)}$	1 1

Table B.4: P-channel MOSFET state table and parameter settings of Figure B.5.

State i	State description	Parameters	Boundary conditions	State $i+1$
1	Cut-off region	$R_{DS} = R_{DS(off)}$	$V_{GS}(0) < V_{GS(th)}$ $V_{GS}(t) = V_{GS(th)}$	2 2
2	Saturation region	$R_{DS} = R_{DS(on)}$	$V_{GS}(0) > V_{GS(th)}$ $V_{GS}(t) = V_{GS(th)}$	1 1

B.2.2 MOSFET I/O interface

$$
\begin{aligned}
\mathbf{y}_{IO\,VGS}(t) &= \begin{bmatrix} \mathbf{y}_{I1}(t) \\ \mathbf{y}_{O1}(t) \end{bmatrix} \quad \text{with} \quad \mathbf{y}_{I1}(t) = \begin{bmatrix} 0 \\ V_{GS} \end{bmatrix} \quad \mathbf{y}_{O1}(t) = \begin{bmatrix} \,\end{bmatrix} \\
\mathbf{y}_{IO\,VDS}(t) &= \begin{bmatrix} \mathbf{y}_{I2}(t) \\ \mathbf{y}_{O2}(t) \end{bmatrix} \quad \text{with} \quad \mathbf{y}_{I2}(t) = \begin{bmatrix} I_{VDS} \\ V_{DS} \end{bmatrix} \quad \mathbf{y}_{O2}(t) = \begin{bmatrix} I_{DS} \\ V_{IDS} \end{bmatrix} \\
\mathbf{y}_{IO\,VS0}(t) &= \begin{bmatrix} \mathbf{y}_{I3}(t) \\ \mathbf{y}_{O3}(t) \end{bmatrix} \quad \text{with} \quad \mathbf{y}_{I3}(t) = \begin{bmatrix} I_{VS0} \\ V_{S0} \end{bmatrix} \quad \mathbf{y}_{O3}(t) = \begin{bmatrix} I_{S0} \\ V_{IS0} \end{bmatrix} \\
\mathbf{y}_{IO\,VD0}(t) &= \begin{bmatrix} \mathbf{y}_{I4}(t) \\ \mathbf{y}_{O4}(t) \end{bmatrix} \quad \text{with} \quad \mathbf{y}_{I4}(t) = \begin{bmatrix} I_{VD0} \\ V_{D0} \end{bmatrix} \quad \mathbf{y}_{O4}(t) = \begin{bmatrix} I_{D0} \\ V_{ID0} \end{bmatrix}
\end{aligned} \tag{B.2}
$$

B.3 BJT

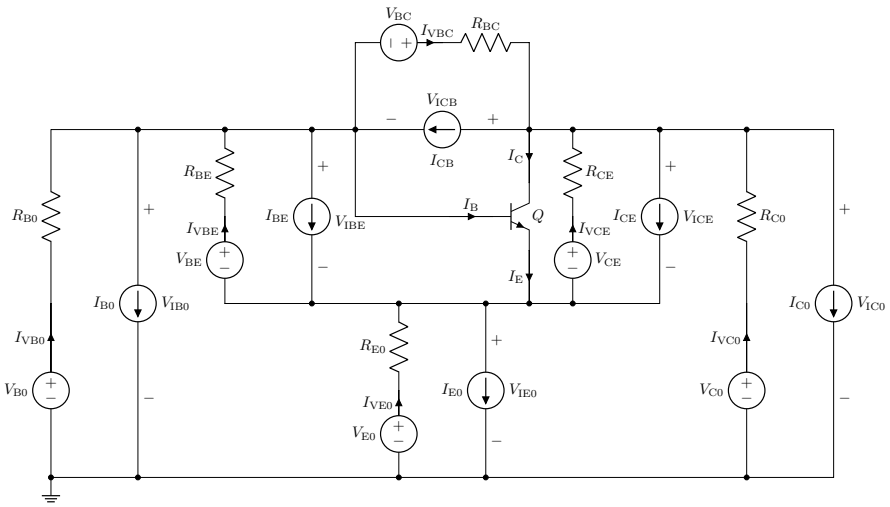

Figure B.6: NPN BJT Circuit-Model with I/O interface.

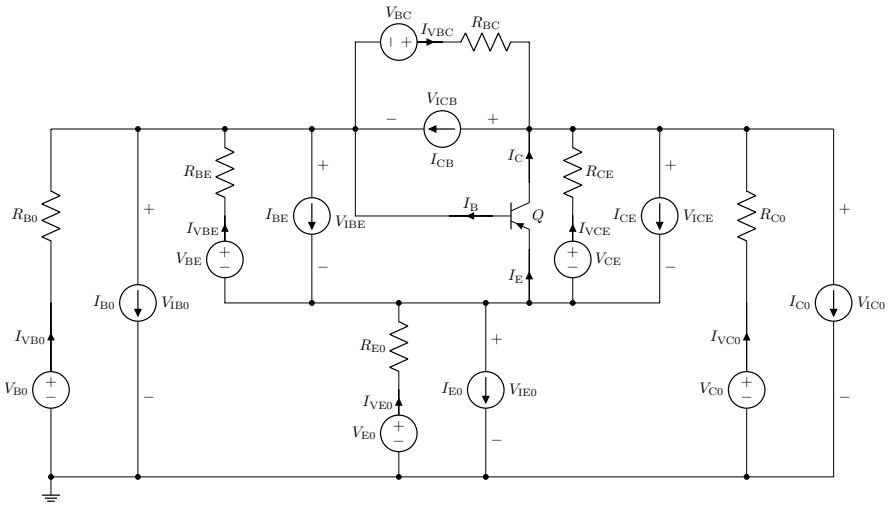

Figure B.7: PNP BJT Circuit-Model with I/O interface.

B.3.1 BJT model parameters

$V_{\mathrm{BE(on)}}$	Base-emitter voltage (NPN type $I_{\mathrm{B}} > 0$ and PNP type $I_{\mathrm{B}} < 0$)
$V_{\mathrm{CE(sat)}}$	Collector-emitter saturation voltage ($I_{\mathrm{B}} \gg \frac{I_{\mathrm{C}}}{h_{\mathrm{FE}}}$)
h_{FE}	DC current gain
I_{CBO}	Collector-base cut-off current

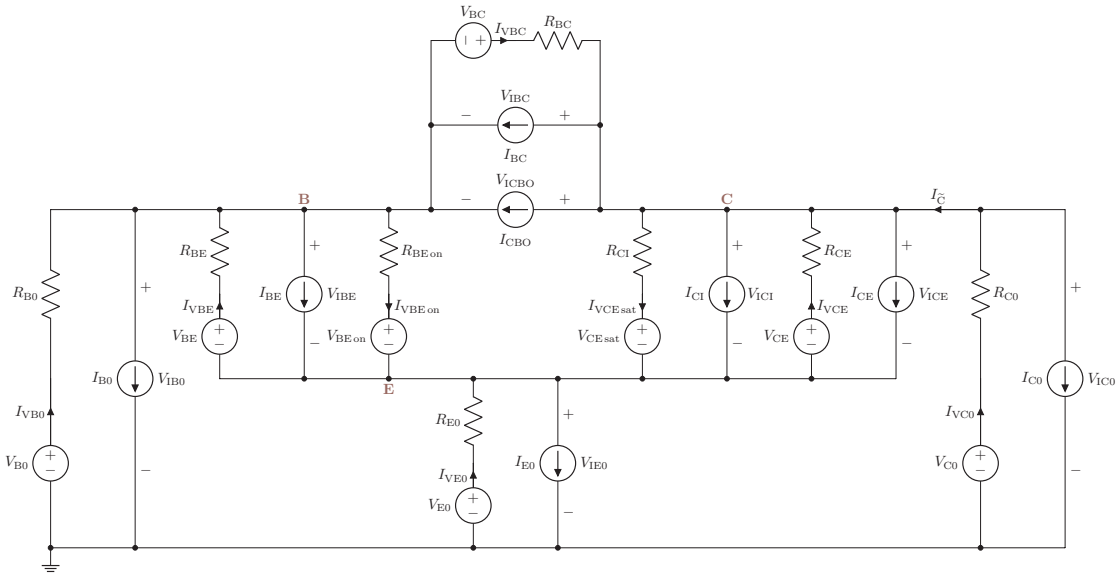

Figure B.8: Universally applicable BJT SubCircuit-Model.

Table B.5: NPN BJT state table and parameter settings of Figure B.8.

State i	State description	Parameters	Boundary conditions	State $i+1$
1	Cut-off region	$I_{\text{VBE on}} = 0$ $I_{\text{CI}} = 0$ $I_{\text{VCE sat}} = 0$	$V_{\text{IBE}}(t) > V_{\text{BE(on)}}$ $V_{\text{IBE}}(t) = V_{\text{BE(on)}}$	2 2
2	Forward region	$V_{\text{BE on}} = V_{\text{BE(on)}}$ $I_{\text{CI}} = I_{\text{VBE on}} h_{\text{FE}}$ $I_{\text{VCE sat}} = 0$	$I_{\text{VBE on}}(0) < 0$ $I_{\text{VBE on}}(t) = 0$ $V_{\text{ICI}}(t) < V_{\text{CE(sat)}}$ $V_{\text{ICI}}(t) = V_{\text{CE(sat)}}$	1 1 3 3
3	Saturation region	$V_{\text{BE on}} = V_{\text{BE(on)}}$ $I_{\text{CI}} = 0,\ R_{\text{CI}} = 0$ $V_{\text{CE sat}} = V_{\text{CE(sat)}}$	$I_{\text{BE on}}(0) h_{\text{FE}} < I_{\text{VCE sat}}(0)$ $I_{\text{BE on}}(t) h_{\text{FE}} = I_{\text{VCE sat}}(t)$	2 2

Table B.6: PNP BJT state table and parameter settings of Figure B.8.

State i	State description	Parameters	Boundary conditions	State $i+1$
1	Cut-off region	$I_{\text{VBE on}} = 0$ $I_{\text{CI}} = 0$ $I_{\text{VCE sat}} = 0$	$V_{\text{IBE}}(t) < V_{\text{BE(on)}}$ $V_{\text{IBE}}(t) = V_{\text{BE(on)}}$	2 2
2	Forward region	$V_{\text{BE on}} = V_{\text{BE(on)}}$ $I_{\text{CI}} = I_{\text{VBE on}} h_{\text{FE}}$ $I_{\text{VCE sat}} = 0$	$I_{\text{VBE on}}(0) > 0$ $I_{\text{VBE on}}(t) = 0$ $V_{\text{ICI}}(t) > V_{\text{CE(sat)}}$ $V_{\text{ICI}}(t) = V_{\text{CE(sat)}}$	1 1 3 3
3	Saturation region	$V_{\text{BE on}} = V_{\text{BE(on)}}$ $I_{\text{CI}} = 0,\ R_{\text{CI}} = 0$ $V_{\text{CE sat}} = V_{\text{CE(sat)}}$	$I_{\text{BE on}}(0) h_{\text{FE}} > I_{\text{VCE sat}}(0)$ $I_{\text{BE on}}(t) h_{\text{FE}} = I_{\text{VCE sat}}(t)$	2 2

B.3.2 BJT I/O interface

$$
\begin{aligned}
\mathbf{y}_{\mathrm{IO\,VB0}}(t) &= \begin{bmatrix} \mathbf{y}_{\mathrm{I1}}(t) \\ \mathbf{y}_{\mathrm{O1}}(t) \end{bmatrix} \quad \text{with} \quad \mathbf{y}_{\mathrm{I1}}(t) = \begin{bmatrix} I_{\mathrm{VB0}} \\ V_{\mathrm{B0}} \end{bmatrix} \quad \mathbf{y}_{\mathrm{O1}}(t) = \begin{bmatrix} I_{\mathrm{B0}} \\ V_{\mathrm{IB0}} \end{bmatrix} \\
\mathbf{y}_{\mathrm{IO\,VBE}}(t) &= \begin{bmatrix} \mathbf{y}_{\mathrm{I2}}(t) \\ \mathbf{y}_{\mathrm{O2}}(t) \end{bmatrix} \quad \text{with} \quad \mathbf{y}_{\mathrm{I2}}(t) = \begin{bmatrix} I_{\mathrm{VBE}} \\ V_{\mathrm{BE}} \end{bmatrix} \quad \mathbf{y}_{\mathrm{O2}}(t) = \begin{bmatrix} I_{\mathrm{BE}} \\ V_{\mathrm{IBE}} \end{bmatrix} \\
\mathbf{y}_{\mathrm{IO\,VE0}}(t) &= \begin{bmatrix} \mathbf{y}_{\mathrm{I3}}(t) \\ \mathbf{y}_{\mathrm{O3}}(t) \end{bmatrix} \quad \text{with} \quad \mathbf{y}_{\mathrm{I3}}(t) = \begin{bmatrix} I_{\mathrm{VE0}} \\ V_{\mathrm{E0}} \end{bmatrix} \quad \mathbf{y}_{\mathrm{O3}}(t) = \begin{bmatrix} I_{\mathrm{E0}} \\ V_{\mathrm{IE0}} \end{bmatrix} \\
\mathbf{y}_{\mathrm{IO\,VBC}}(t) &= \begin{bmatrix} \mathbf{y}_{\mathrm{I4}}(t) \\ \mathbf{y}_{\mathrm{O4}}(t) \end{bmatrix} \quad \text{with} \quad \mathbf{y}_{\mathrm{I4}}(t) = \begin{bmatrix} I_{\mathrm{VBC}} \\ V_{\mathrm{BC}} \end{bmatrix} \quad \mathbf{y}_{\mathrm{O4}}(t) = \begin{bmatrix} I_{\mathrm{BC}} \\ V_{\mathrm{IBC}} \end{bmatrix} \\
\mathbf{y}_{\mathrm{IO\,VCE}}(t) &= \begin{bmatrix} \mathbf{y}_{\mathrm{I5}}(t) \\ \mathbf{y}_{\mathrm{O5}}(t) \end{bmatrix} \quad \text{with} \quad \mathbf{y}_{\mathrm{I5}}(t) = \begin{bmatrix} I_{\mathrm{VCE}} \\ V_{\mathrm{CE}} \end{bmatrix} \quad \mathbf{y}_{\mathrm{O5}}(t) = \begin{bmatrix} I_{\mathrm{CE}} \\ V_{\mathrm{ICE}} \end{bmatrix} \\
\mathbf{y}_{\mathrm{IO\,VC0}}(t) &= \begin{bmatrix} \mathbf{y}_{\mathrm{I6}}(t) \\ \mathbf{y}_{\mathrm{O6}}(t) \end{bmatrix} \quad \text{with} \quad \mathbf{y}_{\mathrm{I6}}(t) = \begin{bmatrix} I_{\mathrm{VC0}} \\ V_{\mathrm{C0}} \end{bmatrix} \quad \mathbf{y}_{\mathrm{O6}}(t) = \begin{bmatrix} I_{\mathrm{C0}} \\ V_{\mathrm{IC0}} \end{bmatrix}
\end{aligned} \tag{B.3}
$$

B.4 Optocoupler

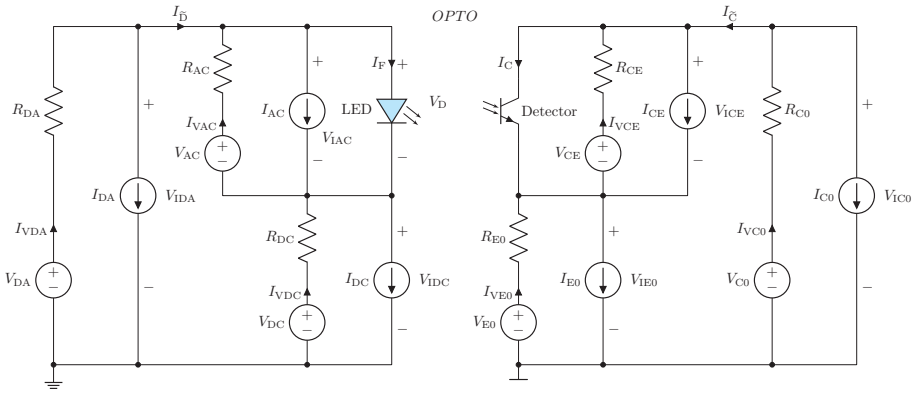

Figure B.9: Optocoupler Circuit-Model with I/O interface.

B.4.1 OPTO model parameters

V_F	Emitter LED forward voltage
$V_{CE(sat)}$	Detector collector-emitter saturation voltage ($I_F \gg \frac{I_C}{CTR}$)
CTR	Current transfer ratio

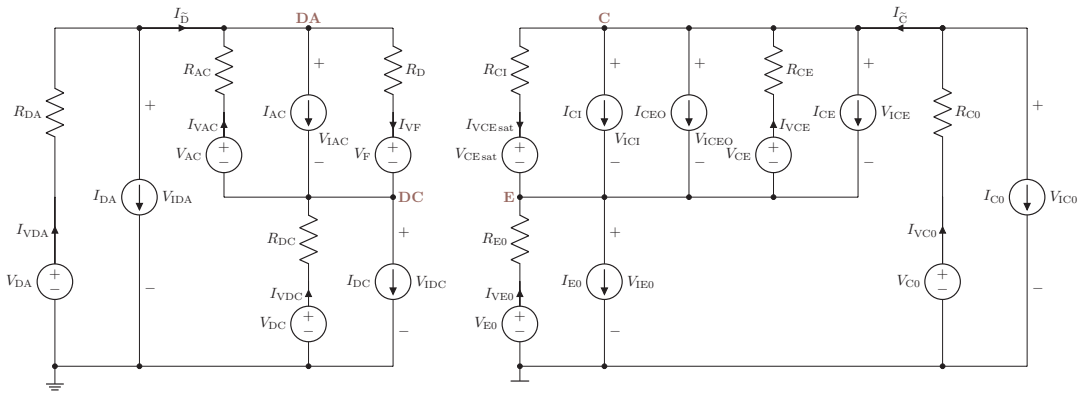

Figure B.10: Universally applicable Optocoupler SubCircuit-Model.

Table B.7: Optocoupler state table and parameter settings of Figure B.10.

State i	State description	Parameters	Boundary conditions	State $i+1$
1	Cut-off region	$I_{VF} = 0$ $I_{CI} = 0$ $I_{VCE\,sat} = 0$	$V_{IAC}(0) > V_F$ $V_{IAC}(t) = V_F$	2 2
2	Forward region	$I_{CI} = I_{VF} CTR$ $I_{VCE\,sat} = 0$	$I_{VF}(0) < 0$ $I_{VF}(t) = 0$ $V_{ICI}(t) < V_{CE(sat)}$ $V_{ICI}(t) = V_{CE(sat)}$	1 1 3 3
3	Saturation region	$I_{CI} = 0$, $R_{CI} = 0$ $V_{CE\,sat} = V_{CE(sat)}$	$I_{VF}(0)CTR < I_{VCE\,sat}(0)$ $I_{VF}(t)CTR = I_{VCE\,sat}(t)$	2 2

B.4.2 Optocoupler I/O interface

$$
\begin{aligned}
\mathbf{y}_{\mathrm{IO\,VDA}}(t) &= \begin{bmatrix} \mathbf{y}_{\mathrm{I1}}(t) \\ \mathbf{y}_{\mathrm{O1}}(t) \end{bmatrix} \quad \text{with} \quad \mathbf{y}_{\mathrm{I1}}(t) = \begin{bmatrix} I_{\mathrm{VDA}} \\ V_{\mathrm{DA}} \end{bmatrix} \quad \mathbf{y}_{\mathrm{O1}}(t) = \begin{bmatrix} I_{\mathrm{DA}} \\ V_{\mathrm{IDA}} \end{bmatrix} \\
\mathbf{y}_{\mathrm{IO\,VAC}}(t) &= \begin{bmatrix} \mathbf{y}_{\mathrm{I2}}(t) \\ \mathbf{y}_{\mathrm{O2}}(t) \end{bmatrix} \quad \text{with} \quad \mathbf{y}_{\mathrm{I2}}(t) = \begin{bmatrix} I_{\mathrm{VAC}} \\ V_{\mathrm{AC}} \end{bmatrix} \quad \mathbf{y}_{\mathrm{O2}}(t) = \begin{bmatrix} I_{\mathrm{AC}} \\ V_{\mathrm{IAC}} \end{bmatrix} \\
\mathbf{y}_{\mathrm{IO\,VDC}}(t) &= \begin{bmatrix} \mathbf{y}_{\mathrm{I3}}(t) \\ \mathbf{y}_{\mathrm{O3}}(t) \end{bmatrix} \quad \text{with} \quad \mathbf{y}_{\mathrm{I3}}(t) = \begin{bmatrix} I_{\mathrm{VDC}} \\ V_{\mathrm{DC}} \end{bmatrix} \quad \mathbf{y}_{\mathrm{O3}}(t) = \begin{bmatrix} I_{\mathrm{DC}} \\ V_{\mathrm{IDC}} \end{bmatrix} \\
\mathbf{y}_{\mathrm{IO\,VE0}}(t) &= \begin{bmatrix} \mathbf{y}_{\mathrm{I4}}(t) \\ \mathbf{y}_{\mathrm{O4}}(t) \end{bmatrix} \quad \text{with} \quad \mathbf{y}_{\mathrm{I4}}(t) = \begin{bmatrix} I_{\mathrm{VE0}} \\ V_{\mathrm{E0}} \end{bmatrix} \quad \mathbf{y}_{\mathrm{O4}}(t) = \begin{bmatrix} I_{\mathrm{E0}} \\ V_{\mathrm{IE0}} \end{bmatrix} \\
\mathbf{y}_{\mathrm{IO\,VCE}}(t) &= \begin{bmatrix} \mathbf{y}_{\mathrm{I5}}(t) \\ \mathbf{y}_{\mathrm{O5}}(t) \end{bmatrix} \quad \text{with} \quad \mathbf{y}_{\mathrm{I5}}(t) = \begin{bmatrix} I_{\mathrm{VCE}} \\ V_{\mathrm{CE}} \end{bmatrix} \quad \mathbf{y}_{\mathrm{O5}}(t) = \begin{bmatrix} I_{\mathrm{CE}} \\ V_{\mathrm{ICE}} \end{bmatrix} \\
\mathbf{y}_{\mathrm{IO\,VC0}}(t) &= \begin{bmatrix} \mathbf{y}_{\mathrm{I6}}(t) \\ \mathbf{y}_{\mathrm{O6}}(t) \end{bmatrix} \quad \text{with} \quad \mathbf{y}_{\mathrm{I6}}(t) = \begin{bmatrix} I_{\mathrm{VC0}} \\ V_{\mathrm{C0}} \end{bmatrix} \quad \mathbf{y}_{\mathrm{O6}}(t) = \begin{bmatrix} I_{\mathrm{C0}} \\ V_{\mathrm{IC0}} \end{bmatrix}
\end{aligned} \tag{B.4}
$$

B.5 Amplifier OPAMP

B.5.1 Amplifier model parameters

$V_{\mathrm{out\,min}}$	Minimum output voltage swing low (V_{OL})
$V_{\mathrm{out\,max}}$	Maximum output voltage swing high (V_{OH})

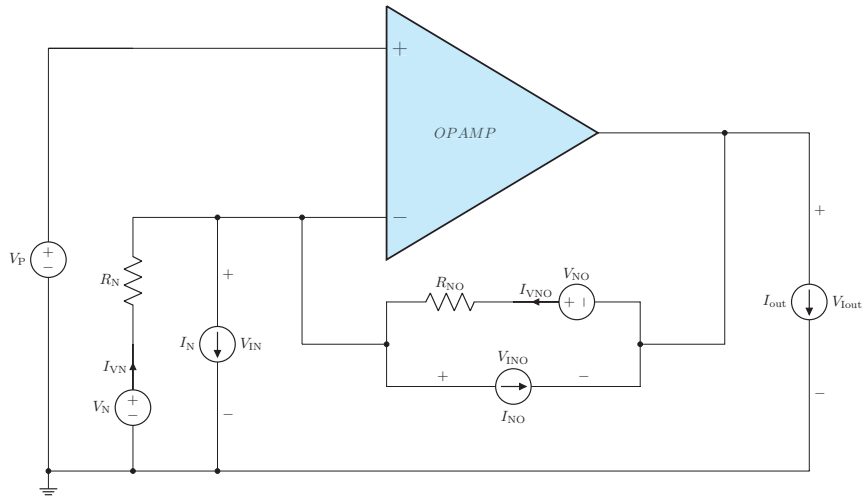

Figure B.11: Amplifier Circuit-Model with I/O interface.

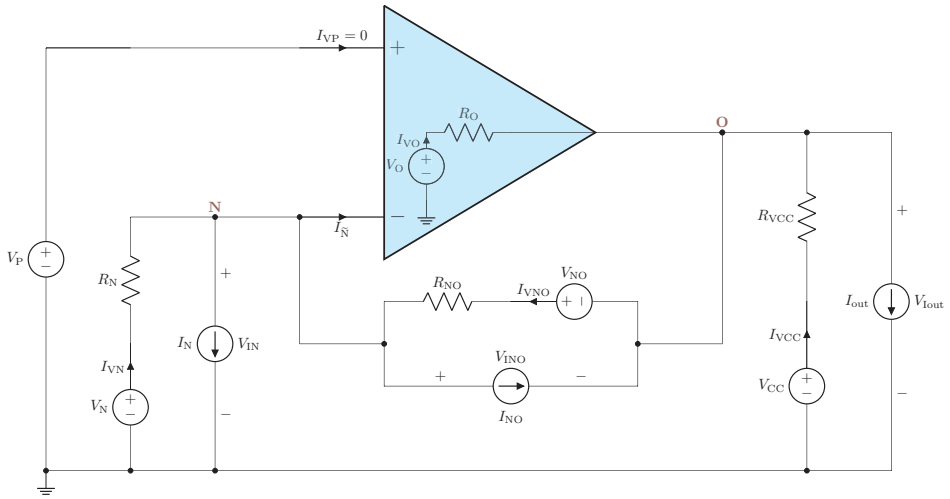

Figure B.12: Universally applicable amplifier SubCircuit-Model.

Table B.8: Amplifier state table and parameter settings of Figure B.12.

State i	State description	Parameters	Boundary conditions	State $i+1$
1	Linear region	$I_{VO} = 0$ $I_{VCC} = 0$	$V_{Iout}(0) < V_{out\,min}$ $V_{Iout}(t) = V_{out\,min}$ $V_{Iout}(0) > V_{out\,max}$ $V_{Iout}(t) = V_{out\,max}$	2 2 3 3
2	Saturation region low	$R_O = 0$ $I_{VCC} = 0$ $V_O = V_{O\,min}$	$I_{\widetilde{N}}(0) < 0$ $I_{\widetilde{N}}(t) = 0$	1 1
3	Saturation region high	$R_O = 0$ $I_{VCC} = 0$ $V_O = V_{O\,max}$	$I_{\widetilde{N}}(0) > 0$ $I_{\widetilde{N}}(t) = 0$	1 1

B.5.2 Amplifier I/O interface

$$
\begin{aligned}
\mathbf{y}_{IO\,VP}(t) &= \begin{bmatrix} \mathbf{y}_{I1}(t) \\ \mathbf{y}_{O1}(t) \end{bmatrix} \quad \text{with} \quad \mathbf{y}_{I1}(t) = \begin{bmatrix} 0 \\ V_P \end{bmatrix} \quad \mathbf{y}_{O1}(t) = \begin{bmatrix} \,\end{bmatrix} \\
\mathbf{y}_{IO\,VN}(t) &= \begin{bmatrix} \mathbf{y}_{I2}(t) \\ \mathbf{y}_{O2}(t) \end{bmatrix} \quad \text{with} \quad \mathbf{y}_{I2}(t) = \begin{bmatrix} I_{VN} \\ V_N \end{bmatrix} \quad \mathbf{y}_{O2}(t) = \begin{bmatrix} I_N \\ V_{IN} \end{bmatrix} \\
\mathbf{y}_{IO\,VNO}(t) &= \begin{bmatrix} \mathbf{y}_{I3}(t) \\ \mathbf{y}_{O3}(t) \end{bmatrix} \quad \text{with} \quad \mathbf{y}_{I3}(t) = \begin{bmatrix} I_{VNO} \\ V_{NO} \end{bmatrix} \quad \mathbf{y}_{O3}(t) = \begin{bmatrix} I_{NO} \\ V_{INO} \end{bmatrix} \\
\mathbf{y}_{IO\,VCC}(t) &= \begin{bmatrix} \mathbf{y}_{I4}(t) \\ \mathbf{y}_{O4}(t) \end{bmatrix} \quad \text{with} \quad \mathbf{y}_{I4}(t) = \begin{bmatrix} I_{VCC} \\ V_{CC} \end{bmatrix} \quad \mathbf{y}_{O4}(t) = \begin{bmatrix} \,\end{bmatrix} \\
\mathbf{y}_{IO\,out}(t) &= \begin{bmatrix} \mathbf{y}_{I5}(t) \\ \mathbf{y}_{O5}(t) \end{bmatrix} \quad \text{with} \quad \mathbf{y}_{I5}(t) = \begin{bmatrix} \,\end{bmatrix} \quad \mathbf{y}_{O5}(t) = \begin{bmatrix} I_{out} \\ V_{Iout} \end{bmatrix}
\end{aligned} \tag{B.5}
$$