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Influence of Process Variations on Avalanche Breakdown in Power Trench MOSFETs

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Abstract

The aim of this master thesis is to investigate the impact of semiconductor production process parameter variations on the avalanche breakdown of complex silicon power trench MOSFETs. This breakdown leads to the creation of trap states varying in location, energy level and donor-/acceptor-like behavior, which all impact certain device parameters. By conducting different electrical measurements like capacitance-voltage measurements and charge pumping, insights are collected about the impact of avalanche breakdown for 12 wafers, each produced with differing process variations. We show that the applied constant current stress results in either positive carrier injection or the creation of hole-like trap states during the avalanche stress.

This thesis was be conducted at the Institute of Solid State Physics at TU Graz in cooperation with Kompetenzzentrum Automobil- und Industrie- Elektronik GmbH (KAI) in Villach.

Kurzfassung

Das Ziel dieser Masterarbeit ist die Untersuchung der Einflüsse von unterschiedlichen Halbleiter Produktionsprozessen auf den Lawinen-Durchbruch in komplexen Silizium Leistungstransistoren mit Trench Isolation. Dieser Durchbruch führt zu der Entstehung von "Trap-Zuständen", welche sich in Position, Energielevel und donor-/akzeptor-ähnlichen Verhalten unterscheiden. Alle diese Zustände beeinflussen spezielle Device-Parameter. Mit unterschiedlichen elektrischen Messungen wie Kapazitäts-Spannungsmessungen oder Ladungspumpen können Informationen über den Einfluss des Lawinen-Durchbruchs für 12 Wafer, die alle mit unterschiedlichen Prozessvariationen produziert wurden, gewonnen werden. Wir zeigen, dass der angewandte Konstantstromstress in einer Einbettung positiver Ladungsträger im Oxid der Feldplatte resultiert oder neue löcherähnliche Traps kreiert werden.

Diese Arbeit wurde am Insitut für Festkörperphysik an der TU Graz in Koorperation mit dem Kompetenzzentrum Automobil- und Industrie- Elektronik GmbH (KAI) in Villach verfasst.

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Chapter 1

Introduction

1.1 Motivation

Since electrical relays and vacuum tubes were mostly replaced by transistors in power electronics, an interest in the efficiency and performance of power transistors arose. During various applications like buck converters in phone chargers and photovoltaic systems, the transistors, mostly power MOSFETs, are reverse biased in the off state and switched in a periodic manner. Due to some inductance in the circuit combined with the switching, high voltage spikes could yield to avalanche breakdown inside the transistors. The result is the creation of so called "trap states" in the oxides and their interfaces to silicon. As this is the region, where the channel forms in a MOS device, this impacts the device characteristics and reliability.

Besides demanding microscopical analysis the drift of the devices can be examined by various charge pumping measurements, which are purely electrical measurements. Combined with controlled constant current stress tests, insights on properties of diverse kinds of trap states differing in location, donor-/acceptor-like behavior and their energy level in the band gap can be acquired. Information on, for example, the location of traps can act as a guide for a better physical understanding of the avalanche effect in power devices as well as an improved design process for future products.

The design process of semiconductor devices is particularly hard as hundreds of process steps can be tweaked, which all result in all so slightly different device parameters. By varying some important process parameters and comparing their behavior regarding trap states, we want to gather insights about the influence of those aforementioned process variations on important device parameters like, for example, the device's on resistance, which is an essential parameter in the industry to keep track of. Besides doping, parameters which change the device's geometry have a big impact on the electric field distribution inside the device and hence, influence the charge carriers during avalanche stress. Variations in trench depth,

the location of the gate and the position of all the contacts may have an effect on how the device will drift, already during tests but maybe also during regular use. That is why a complete understanding of the impact of those process variations is desired.

1.2 Outline

This thesis is structured into five chapters. Chapter 2 provides a general explanation about the used devices and the physical description of the Si-SiO_2 interface degradation and trap states, as well as the investigated process variations. In Chapter 3, the experimental setup is introduced. Chapter 4 presents the measurement results combined with an interpretation of those results. The final chapter 5 summarizes the discovered results and gives and outlook for possible future work.

Chapter 2

MOSFETs

In this chapter we discuss the essentials of power MOSFETs and give an overview on trap states and oxide-channel interface degradation mechanisms.

2.1 First MOSFET

The first metal-oxide-semiconductor field-effect transistor (MOSFET) was invented in 1959 [Kah63]. Since then, many different types of MOSFETs arose with all their various applications [HH89]. Nevertheless, all the variations of the MOSFET obey the same working principle in general: by applying a signal to the gate of the transistor, the resulting field effect forms an inversion channel between source and drain, which makes the transistor low ohmic [Sze02].

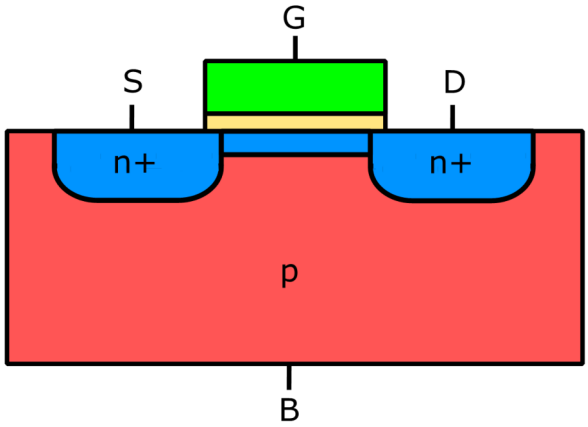


Figure 2.1 Schematic structure of a lateral n-channel MOSFET. The blue channel beneath the gate arises with an applied positive gate voltage due to the field effect.

With this working principle, numerous applications, ranging from simple switches over complex amplifiers and microprocessors, can be created [TSG12]. Figure 2.1 shows the typical layout of a lateral MOSFET.

2.1.1 Power MOSFET

In contrast to lateral MOSFET devices, the channel of power MOSFETs is often orientated vertically in relation to the wafer. This leads to drastically increased packaging densities on the wafer which in turn allows for lower production costs and support for high currents. In this case, one transistor then consists of many interconnected parallel devices.

2.1.2 Structure

The devices which are investigated in this master thesis have a structure as shown in figure 2.2. As source is on top and drain is on bottom, the device is a vertical device. The drain contact is connected to the n-drift region. The p-body region is rather small in comparison to lateral devices. Body is shorted to the n-source region with the source contact (as in most applications, source and body need to be shorted together). The gate contact creates an inversion channel at the gate oxide-body interface like in a normal vertical transistor.

The biggest difference to general power MOSFETs is the existence of a second polysilicon contact, called "field plate". This contact is shorted to the source/-body contact in applications (therefore it is also called "Source-Polysilicon"). To get insights on the trap densities on the field oxide-drift region interface, we have to be able to contact the field plate separately. Therefore, test structures with this property were produced. The purpose of the field plate is described in the next paragraph. Field plate and the gate share a similar structure, they are both embedded in trenches, but their oxide is different in thickness. Compared to the gate oxide the field plate oxide is rather thick.

Compensation Principle

As the field plate is shorted with source, the source potential is present inside the transistor. This impacts the electric field induced by the reverse biased pn junction between body and drain. As a result, the electric field inside the cell no longer only has a vertical component, but also a horizontal component. In figure 2.3 a simplified case for a compensated pn junction is discussed, where the horizontal and vertical

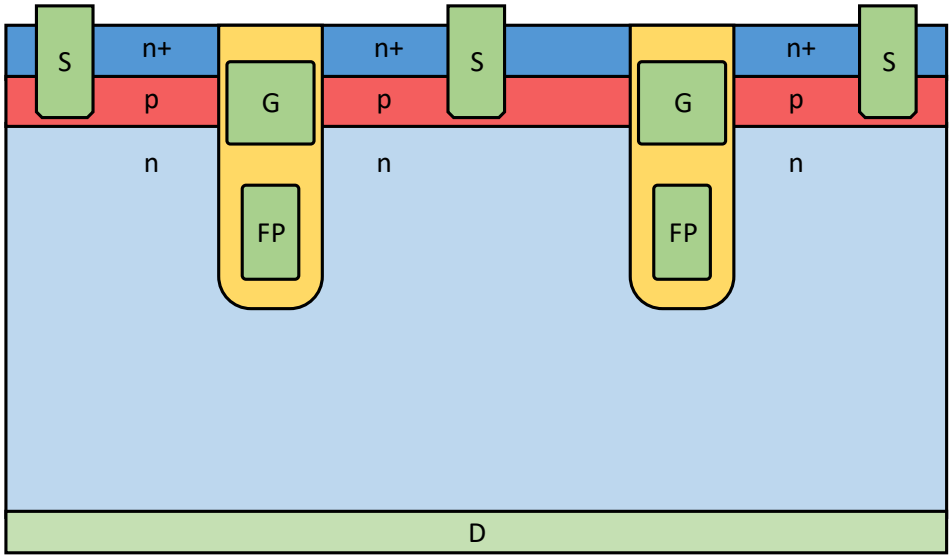
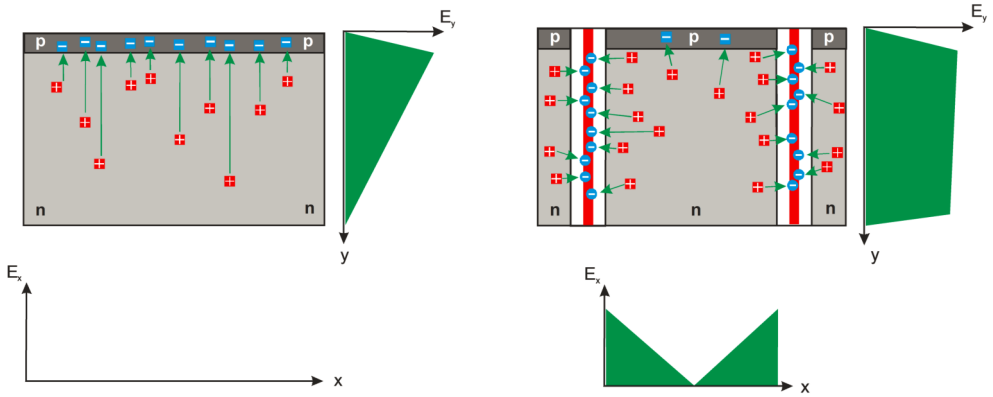


Figure 2.2 Structure of a power trench MOSFET.

components of the electric field are plotted schematically. When examining the vertical component, one can see that it is distributed more evenly in the depletion region and similarly around the trench in our device. Since the voltage between body and drain is just the integral over the electric field [Ruc16]

$$V_{BD} = \int_{\Gamma} \vec{E}(\vec{s}) d\vec{s} \tag{2.1}$$

over an arbitrary trajectory Γ, the voltage between body and drain is increased by this compensation, while keeping the maximum value for the electric field in the cell the same. In turn, this means that a higher reverse bias voltage between drain and body can be sustained until the critical electric field for the avalanche effect to occur is reached in the cell (see section 2.2). This makes a higher doping and shorter drift region with the same breakdown voltage possible, which both decrease the on resistance. However, also the output capacitance is increased [SHB+15].



(a) Uncompensated junction

(b) Compensated junction

Figure 2.3 Compensation of a pn junction. In the compensated device, the vertical component of the E-field is more homogeneously distributed which yields a higher breakdown voltage. Figure taken from [Ruc16].

2.1.3 Manufacturing Process Variations

It takes up to hundreds of processing steps to produce a semiconductor device. For many of those steps a number of parameters can be varied, which results in slightly different devices. To investigate the impact of certain process variations on the avalanche effect, a collection of wafers, called lot, was produced. Each wafer was altered in terms of trench depth, S-Recess, contact depth or a combination of those said variations, which are going to be explained in more detail below.

Trench Depth Variation

One process variation that we investigated in this thesis, is the depth variation of the trenches, as this also results in a larger interface area between the field plate oxide and the channel, which could have an impact on the creation of defects. By etching deeper trenches, the trenches get larger and the doping concentration changes at the trench, as the drift region has a doping gradient. To compensate for this, the epitaxy step is also varied the same way to get a thicker drift region.

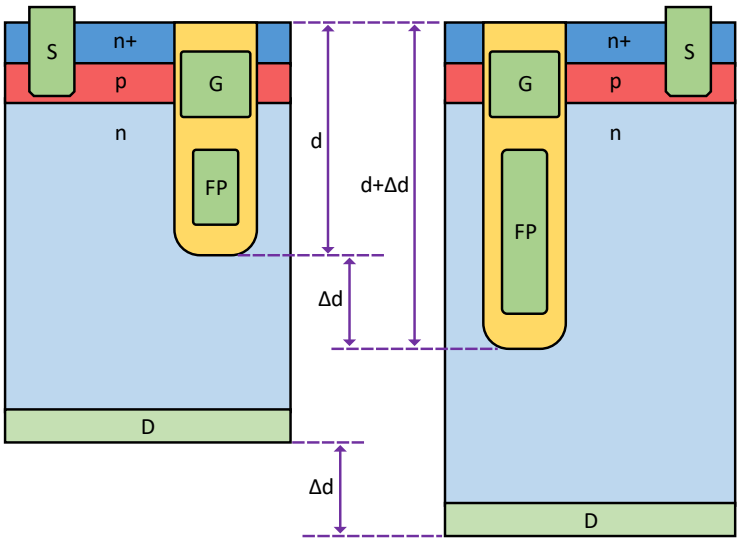


Figure 2.4 Trench depth variation: the structure on the right has a deeper trench and n-drift region of Δd.

S-Recess Variation

The Source-Polysilicon-Recess (S-Recess) describes how much polysilicon on the field plate contact is etched from the top of the wafer. By increasing the S-Recess process step, the field plate is smaller in height. In the following production step, the gate oxide deposition is not varied, so the oxide thickness between both polysilicon contacts is the same for every structure. Therefore, structures with higher S-Recess have also a bigger gate, as the gate height is always the same, but the gate footpoint varies with the different S-Recesses. Those size differences in the gate and field plate could have an impact on how many interface defects can be measured with, for example, charge pumping.

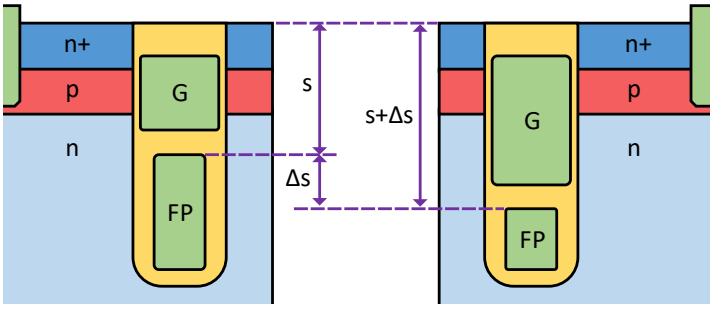


Figure 2.5 S-Recess variation: the fieldplate polysilicon in the structure on the right was etched Δs deeper.

Contact Depth Variation

The third process variation which we investigated in this thesis is the contact depth variation. In our structure, the source and body contact are shorted with one contact. The depth, i.e. how far the contact extends into the body region, is varied (figure 2.6) to get an idea if or how this affects, for example, the avalanche breakdown location.

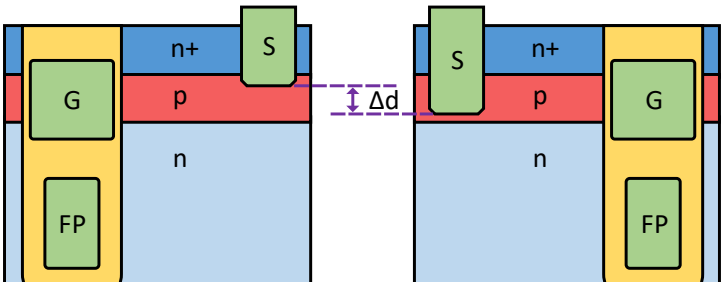


Figure 2.6 Contact depth variation: the structure on the right has a deeper reaching source/body contact.

2.2 Avalanche Breakdown

When looking at a pn junction, it only conducts noticeable current in the forward bias direction. In reverse bias, the depletion region increases with the applied bias voltage. However, there are always some electrons moving around and scattering, which get accelerated from the electric field. If the voltage and therefore the electric field gets bigger, the electrons get accelerated more and have higher energy. Only if the bias voltage is higher than the so called "breakdown voltage" V_{BD}, the electrons have enough energy to put another electron from the valence in the conduction band during the scattering (thus also creating a hole). This is called "impact ionization" [MD85]. Now additional electrons are accelerated by the electric field and the process repeats, leading to an avalanche of charge carriers in the depletion region, which makes the junction conducting again. This phenomenon is called "Avalanche breakdown".

In some applications the transistor is used outside its intended use case scenario and the transistor is forced to conduct current even if it is turned off at the gate. This means that an avalanche breakdown can occur between the body and drain pn junction. This avalanche effect, however, will stress the device. The electrons will degrade the interface between oxide and channel and create so called "trap states", which have an impact on the device's electronic properties (see section 2.3). Therefore, particularly power devices, which conduct high currents, need to be designed to withstand the avalanche breakdown [BAS93].

The location in the devices, where the avalanche breakdown and the degradation of the Si-SiO_2 interface will take place first, can vary. It depends on the electric field

distribution in the depletion region and can be determined by TCAD simulations.

The avalanche breakdown is one of two possibilities to accelerate charge carriers which cause degradation of the Si-SiO_2 interface in semiconductor devices. The second one is called "hot carrier injection" (HCI), where high energetic electrons (called "hot" electrons) break passivated bonds on the interface. This occurs, when the transistor is on, as the electrons are accelerated to the gate oxide because of the applied voltages.

2.3 Trap States

Trap states occur due to physical defects in the transistor material. The defects mostly contribute in the form of trapped charges. These are categorized into 4 kinds of defects [Dea80]:

- *mobile ionic charge*: ionic impurities, like K+ or Li+
- *fixed oxide charge*: positive charge, due primarily to structural defects (ionized silicon) in the oxide layer less than 25 $\mathring{A}$ from the Si-SiO_2 interface
- *interface traps*: structural defects at Si-SiO_2, induced during oxidation or bond-breaking processes
- *border traps*: holes or electrons trapped in the oxide near the interface

Those defects can arise during the manufacturing process of the device or when the device is stressed. According to Deal [Dea80], only interface traps have an electrical communication to the underlying Si. But Fleetwood et. al. [Fle92, FWR$^+$93] also mentions near interface traps, which also contribute to the electrical behavior of the device, called border traps. These trap types are described in more detail below and are shown in figure 2.7.

Interface Traps

The interface between the silicon and the silicon oxide is never perfect, since an amorphous material is adjacent to a crystalline material. This results in many defects in the atomic structure, which are summarized under the term "interface traps". There can be traps which behave acceptor like and therefore trap electrons, hole traps which behave donor like and traps which capture both electrons and holes. One common physical defect at the interface is the so called "dangling bond", where

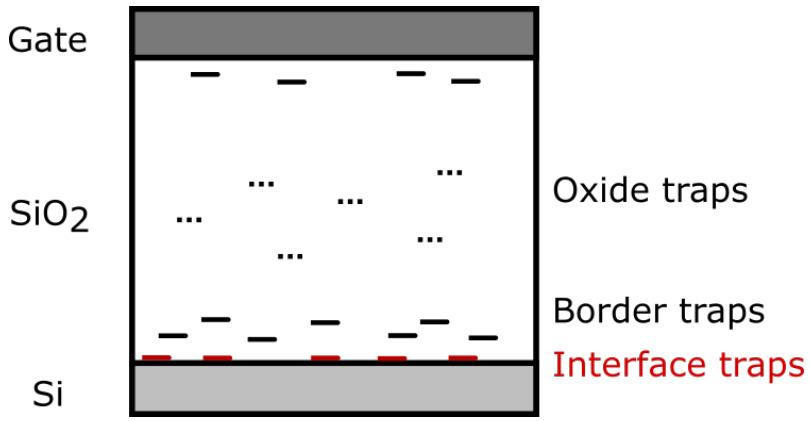


Figure 2.7 Schematic diagram of different kinds of defects in MOS structures.

an atom is missing at the edge of the crystal and therefore an electron is "dangling" around (see figure 2.8). To compensate for this, a hydrogen passivation step is added during the manufacturing process, where a hydrogen atom takes the place of the missing Si atom. However, this passivation can also be again damaged by hot carrier degradation. Rashkeev et. al. [RDVP01] describe many other different possibilities of the interface bonding between the silicon and silicon oxide, while Sakurai et. al. [SS81] show bandstructure calculations for different defects at the interface.

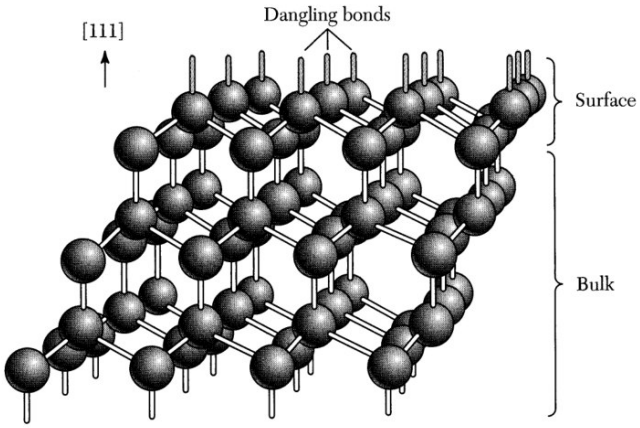


Figure 2.8 Dangling bond defects at the edge of a perfect Si crystal. Figure taken from [Sze02].

Border traps

Traps which are not directly at the Si-SiO_2 interface, but rather a few nanometers into the oxide, are called "Border traps" [Fle92]. They still need to be close enough to the Si to contribute electrically, as they capture and release charges which are coming from the silicon and are tunneling through the oxide, where distance is relevant. In general, these traps have a frequency dependent behavior [PSFW92], which also shows in an influence on the 1/f noise of the structure. The distance into the oxide, where the traps are called border traps, can be estimated with tunneling experiments and lies at around 3 nm [FMO89]. However, with the right conditions even deeper traps can be reached.

2.3.1 Capture and Emission Times

Those defects described above are called trap states as they can capture and re-emit charge carriers. In 1952, a first theory which described these capture and emission processes, was created, called the "Shockley-Read-Hall" (SRH) theory. An exact explanation of the theory can be found in their original paper [SR52] and [Ruc16]. They describe the charge trapping in four different processes, namely electron capture/emission and hole capture/emission (shown in figure 2.9). A process is described with holes, when the charge is captured from or emitted to the valence band, and with electrons, when it is captured from or emitted to the conduction band. Each of those processes have a corresponding time constant τ connected to the process.

$$\tau_{cn} = \frac{1}{\overline{\sigma_n} v_{th_e} n_{cap}} = \frac{1}{\overline{\sigma_n} v_{th_e} N_C} \exp\left(\frac{E_C - E_{Fn}}{kT}\right) \tag{2.2}$$

$$\tau_{en} = \frac{1}{\overline{\sigma_n} v_{th_e} n_{emi}} = \frac{1}{\overline{\sigma_n} v_{th_e} N_C} \exp\left(\frac{E_C - E_t}{kT}\right) \tag{2.3}$$

$$\tau_{cp} = \frac{1}{\overline{\sigma_p} v_{th_p} p_{cap}} = \frac{1}{\overline{\sigma_p} v_{th_p} N_V} \exp\left(\frac{E_{Fp} - E_V}{kT}\right) \tag{2.4}$$

$$\tau_{ep} = \frac{1}{\overline{\sigma_p} v_{th_p} p_{emi}} = \frac{1}{\overline{\sigma_p} v_{th_p} N_V} \exp\left(\frac{E_t - E_V}{kT}\right) \tag{2.5}$$

where $\overline{\sigma}$ is the average capture cross section for holes/electrons and v_{th} the thermal drift velocity. These equations show that the capture processes do not depend on the trap energy level itself, but rather only the quasi fermi levels of holes and electrons. The emission time constants, however, depend on the trap energy level, which

shows, that traps closer to the valence/conduction band have a smaller emission time constant.

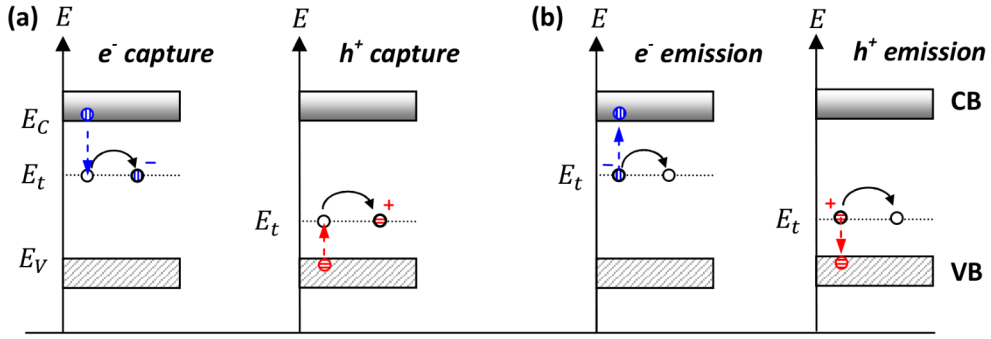


Figure 2.9 The four different capture/emission processes of trap states in the band gap. Figure taken from [AN15].

2.4 Charge Pumping

When trying to gather information about the defects at the Si-SiO_2 interface, the most common method is charge pumping. It was first described in 1969 by Brugler and Jespers [BJ69]. By pulsing the gate (or in our case the fieldplate) and grounding all other contacts, the induced field effect drives the area below the oxide into accumulation or inversion. The accumulated charges at the Si-SiO_2 interface get trapped by the trap states (for example: in an n channel device, the electrons get trapped during the inversion phase) and recombine with the opposite charge carrier to give a measurable charge pumping current [GMBD84]. If the traps reemit the charges before the pulse changes its sign, no current contribution of these traps is observed. Therefore a high slope of the pulse is desired.

The following description treats a n-channel device (like the ones examined in the experimental part of this thesis, analogous for p channel devices). The voltage needed to put the region around the gate/field plate in accumulation (attract holes to the channel in body region) is called charge pumping flat band voltage $\mathbf{V}_{\mathrm{FB}}^{\mathrm{CP}}$ in analogy to the flat band voltage in a MOS capacitor. Nonetheless, it is not the voltage where the bands are flat but rather the voltage needed to reach all interface traps with holes. Similarly, the voltage needed to put the region into inversion (attract electrons to the channel) is called charge pumping threshold voltage $\mathbf{V}_{\mathrm{TH}}^{\mathrm{CP}}$,

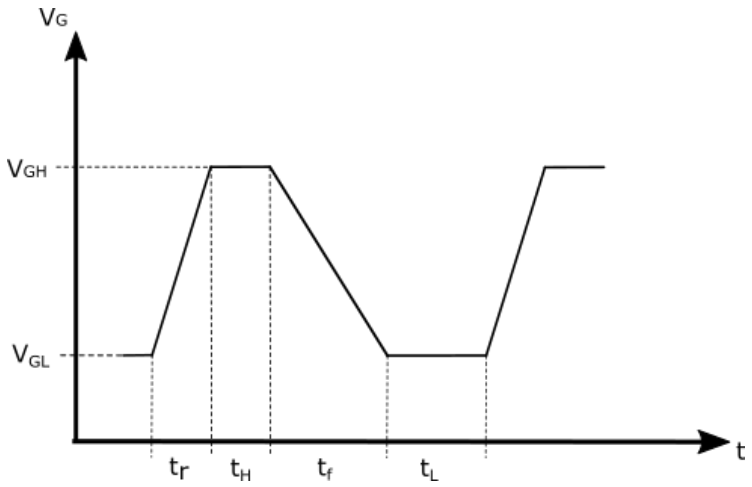


Figure 2.10 Trapezoid pulse applied for charge pumping.

which is the voltage needed to reach all trap states with electrons. These voltages can be determined experimentally (see section 2.4.2) or calculated theoretically (see section 2.4.1). Figure 2.11 shows what is happening during the high and low level of the CP pulse at the gate of a lateral MOSFET.

To get a quantitative description of the traps, one can make the assumption that all trap states N_{CP} are getting charge pumped during one cycle of the pulse within an area A, meaning we get one charge q for all traps [AN15]. This results in a charge pumping current which can be calculated as

$$I_{CP}^{max} = AfqN_{CP} \tag{2.6}$$

Equation 2.6 shows a linear relation between the measurable CP current I_{CP} and the number of trap states N_{CP}, which makes charge pumping a powerful tool for determining defect densities in MOS devices.

In CP measurements, a trapezoidal voltage pulse is used (see figure 2.10), so the free charge carriers have some time to evacuate from the channel as the pulse is changing. Only the trapped ones stay there to recombine. If the frequency (and consequently the slope of the pulse) is chosen too high, that the average emission times of equation 2.3 and 2.5 are in an order of magnitude, where there will still be free charges from the other pulse level left in the device, recombination can happen and hence give a wrong CP current. Low pulsing frequencies give a lower CP current though, so one has to find a compromise, which lies is the range of around 50 kHz to 500 kHz for the examined devices.

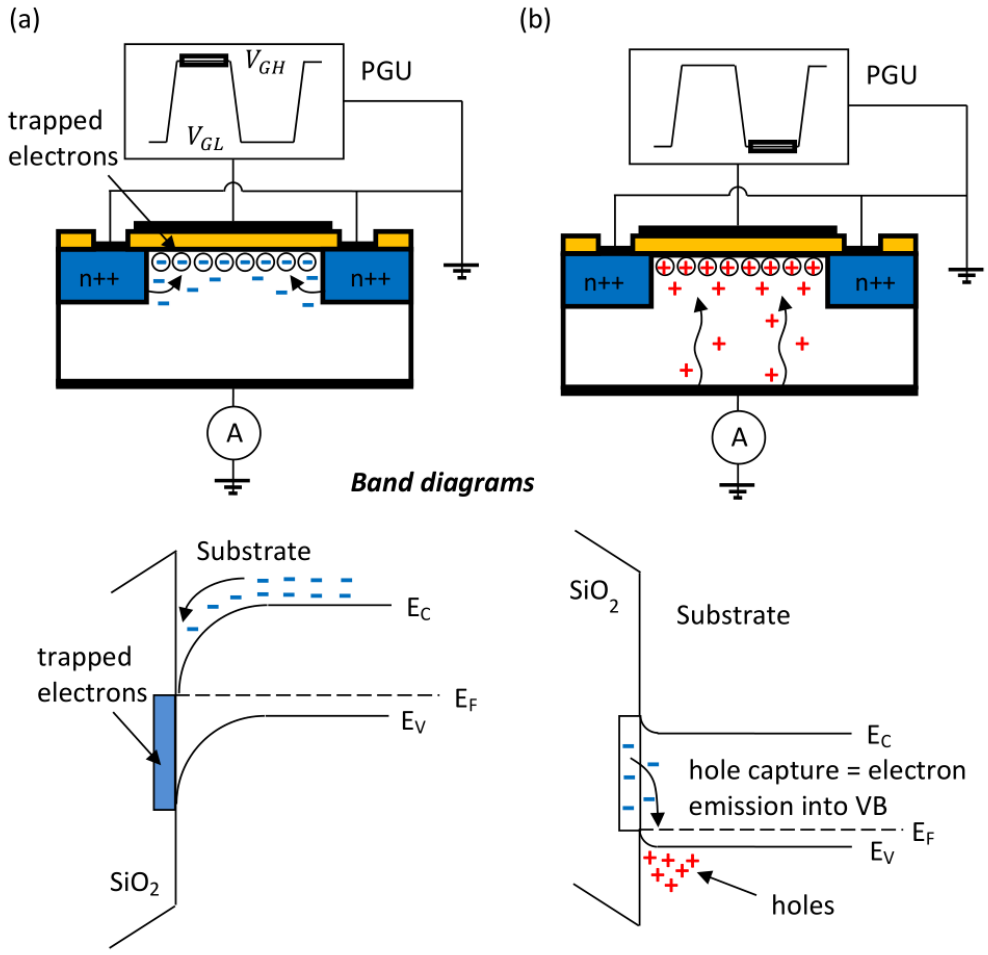


Figure 2.11 Charge pumping on an n channel device: (a) During the high phase of the pulse (inversion) electrons reach the interface traps within the semiconductor band gap and get trapped. (b) During the low phase of the pulse (accumulation) trapped electrons recombine with holes [AN15]. In this plot, the traps behave "acceptor like", which means they trap only electrons. Figure taken from [AN15].

2.4.1 Active Energy Window

One challenge in charge pumping is to measure as many of the interface defects as possible. In an energetic point of view, one cannot measure all trap levels near the bands of the semiconductor. The capture times (equation 2.2 and 2.4) are dependent on the quasi Fermi level position for electrons and holes. When assuming a pulse frequency, where the pulse high and low times t_H and t_L are about

$$t_H \approx \tau_{cn} \tag{2.7}$$

$$t_L \approx \tau_{cp} \tag{2.8}$$

an expression for the needed quasi Fermi energies can be derived out of equations 2.2 and 2.4

$$E_{\mathrm{Fn}}^{\mathrm{crit}} \approx E_{\mathrm{C}} - kT \ln\left(v_{\mathrm{thn}} \sigma_{\mathrm{n}} N_{\mathrm{C}} t_{\mathrm{H}}\right) \tag{2.9}$$

$$E_{\mathrm{Fp}}^{\mathrm{crit}} \approx E_{\mathrm{V}} - kT \ln\left(v_{\mathrm{thp}} \sigma_{\mathrm{p}} N_{\mathrm{V}} t_{\mathrm{L}}\right) \tag{2.10}$$

which are the critical Fermi level positions, which must be exceeded in order to guarantee complete filling [AN15]. The corresponding voltage levels are the same flatband and threshold voltages as the ones previously described, now derived theoretically

$$V_{\mathrm{FB}}^{\mathrm{CP}} = V_{pulse,low}(E_{\mathrm{Fp}}^{\mathrm{crit}}) \tag{2.11}$$

$$V_{\mathrm{TH}}^{\mathrm{CP}} = V_{pulse,high}(E_{\mathrm{Fn}}^{\mathrm{crit}}) \tag{2.12}$$

The maximum CP current is only measured, if the pulse levels are below $V_{\mathrm{FB}}^{\mathrm{CP}}$ and above $V_{\mathrm{TH}}^{\mathrm{CP}}$. Since the rise and fall time of the trapezoidal pulse cannot be infinitely short to allow the evacuation of free charges, those times have to be finite. This results, however, in a shrinking in the so called "active energy window" of charge pumping. During the time, where the voltage level of the pulse is in between $V_{\mathrm{TH}}^{\mathrm{CP}}$ and $V_{\mathrm{FB}}^{\mathrm{CP}}$, the trapped charges have the chance to reemit, before an opposite charge comes by to recombine. The maximum emission time can be calculated from the voltage levels of the pulse and the rise and fall times (illustrated in figure 2.12)

$$t_{\mathrm{en}} = \frac{V_{\mathrm{TH}}^{\mathrm{CP}} - V_{\mathrm{FB}}^{\mathrm{CP}}}{\Delta V_{\mathrm{Pulse}}} t_f \tag{2.13}$$

$$t_{\mathrm{ep}} = \frac{V_{\mathrm{TH}}^{\mathrm{CP}} - V_{\mathrm{FB}}^{\mathrm{CP}}}{\Delta V_{\mathrm{Pulse}}} t_r \tag{2.14}$$

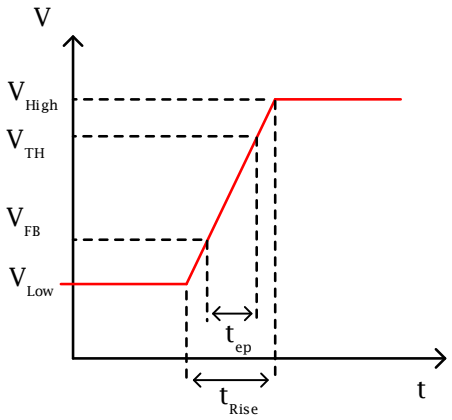


Figure 2.12 Calculation of the emission time t_{ep} for holes during the rising slope of the pulse. Only in the timespan of t_{ep}, emission can occur, which can be calculated out of the relation of the pulse height to $(V_{\mathrm{TH}}^{\mathrm{CP}} - V_{\mathrm{FB}}^{\mathrm{CP}})$ and the rise time, which yields equation 2.14. Similar thoughts at the falling slope lead to t_{en}.

Hence, only traps, which have a smaller emission time τ than the calculated time window above are able to emit their trapped charge and therefore not contribute to the CP current. As traps closer to the bands have a smaller emission time (equations 2.3 and 2.5), they have no impact on the CP current and the active energy window shrinks. The traps with exactly $\tau_{en} = t_{en}$ and $\tau_{ep} = t_{ep}$ resemble the energy border, where traps contribute to the CP current

$$E_{\mathrm{en}} = E_{\mathrm{C}} - kT \ln\left(v_{\mathrm{thn}}\sigma_{\mathrm{n}}N_{\mathrm{C}}\frac{V_{\mathrm{TH}}^{\mathrm{CP}} - V_{\mathrm{FB}}^{\mathrm{CP}}}{\Delta V_{\mathrm{G}}}\right) \tag{2.15}$$

$$E_{\mathrm{ep}} = E_{\mathrm{V}} + kT \ln\left(v_{\mathrm{thp}}\sigma_{\mathrm{p}}N_{\mathrm{V}}\frac{V_{\mathrm{TH}}^{\mathrm{CP}} - V_{\mathrm{FB}}^{\mathrm{CP}}}{\Delta V_{\mathrm{G}}}\right) \tag{2.16}$$

whose difference gives the active energy window

$$\Delta E_{\mathrm{CP}} = E_{\mathrm{G}} - 2kT \ln\left(\sqrt{v_{\mathrm{thn}}v_{\mathrm{thp}}}\sqrt{\sigma_{\mathrm{n}}\sigma_{\mathrm{p}}}\sqrt{N_{\mathrm{C}}N_{\mathrm{v}}}\frac{V_{\mathrm{TH}}^{\mathrm{CP}} - V_{\mathrm{FB}}^{\mathrm{CP}}}{\Delta V_{\mathrm{G}}}\sqrt{t_{\mathrm{f}}t_{\mathrm{r}}}\right) \tag{2.17}$$

2.4.2 Two Level Charge Pumping

There are different variations of charge pumping. In the simple two level charge pumping, the gate/fieldplate is pulsed with a trapezoidal pulse. During both slopes, a current to charge the space charge region with free charge carriers is measured, which overshadows the CP current. As this capacitive "space charge" current is the same for rise and fall slope with opposite sign, it averages out over time, which has to be done to get the CP current (see section 3.2). The slope of the signal (in V/s) should always be held constant to ensure the same active energy windows for all measurements (see section 2.4.1). In the two level charge pumping, either the high pulse level, the low pulse level or both together can be varied, which gives the following types of dual slope CP.

Constant Amplitude

The constant amplitude charge pumping varies the magnitude of low and high level similarly and keeps the amplitude constant. It is the most commonly used method [AN09]. To measure a charge pumping current, the amplitude ΔV of the pulse has to be larger than $V_{FB} - V_{TH}$. As the voltage level increases, the current rises when ΔV starts to overlap both voltage limits and decreases, when one of the limits is no longer inside the interval, which is shown in figure 2.13. This method is not used in our experiments, as it does not yield clear results when the charge pumping current does not saturate (which can be the case in presence of for example border traps).

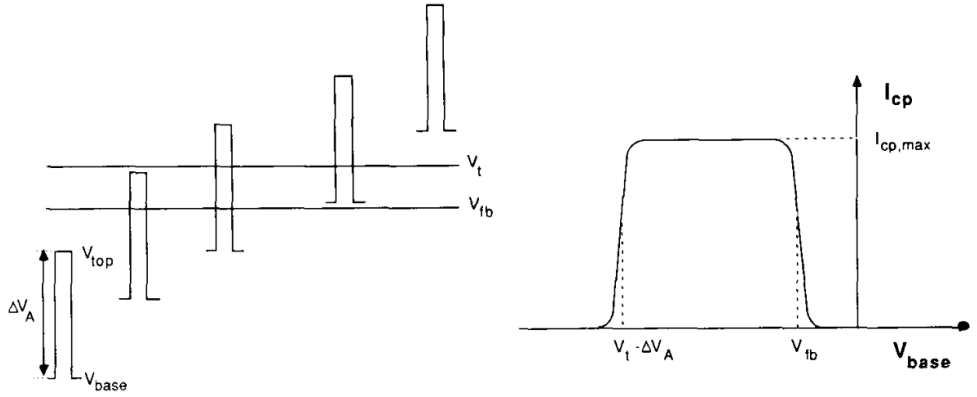


Figure 2.13 Constant amplitude charge pumping. The base level and the high level of the CP pulse are varied the same. A CP current I_{CP} is only observed, if the pulse is below $V_{\mathrm{FB}}^{\mathrm{CP}}$ and above $V_{\mathrm{TH}}^{\mathrm{CP}}$, which gives a form of the CP current over the base level V_B as shown on the right. Figure taken from [HWGM89].

Constant High/Base

In contrast to the constant amplitude charge pumping, one of the two voltage levels is held constant, whereas the other is varied to increase the amplitude ΔV. As either the low or the high voltage level is held constant, one can do a "constant low" or "constant high" measurement. A typical signal and the corresponding CP current is shown in figure 2.14. It is important that the level, which is held constant, is above $V_{\mathrm{TH}}^{\mathrm{CP}}$ or below $V_{\mathrm{FB}}^{\mathrm{CP}}$, otherwise no CP current is measured. As soon as the varied voltage reaches the CP condition (for example $V_{high} > V_{\mathrm{TH}}^{\mathrm{CP}}$ in const. base CP), I_{CP}

rises rapidly and then saturates. This method can be used for spacial profiling as described by Chen et. al. in [CBM93].

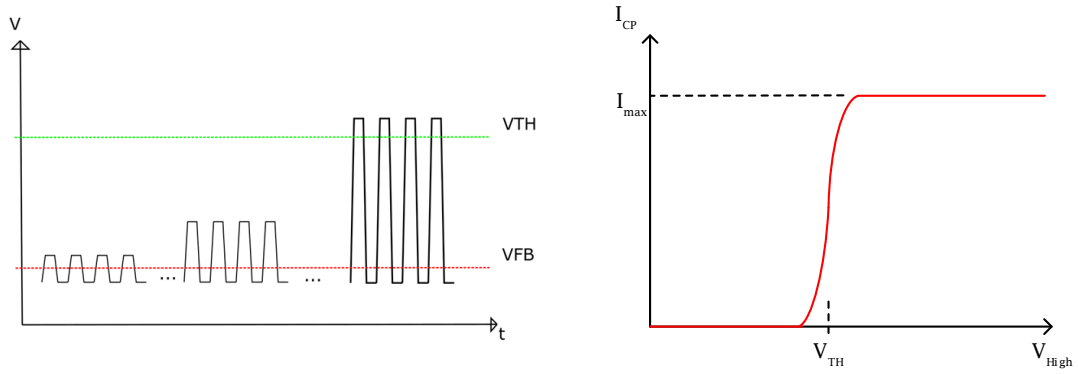


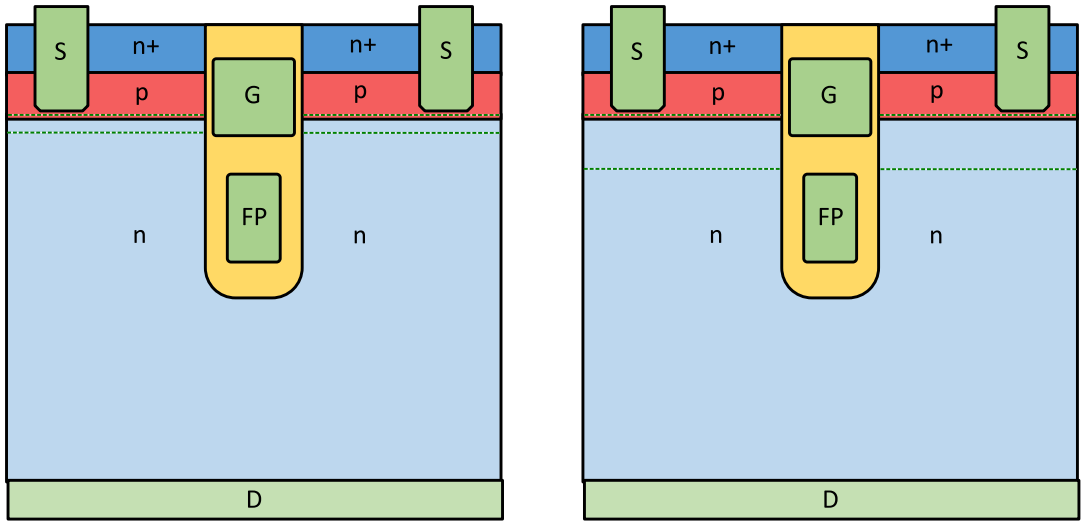
Figure 2.14 Schematic form of a "Constant Low" charge pumping signal. The low voltage level of the pulse is held constant, whereas the high level is increased after measuring the CP current over some cycles. As soon as the high voltage level surpasses $V_{\mathrm{TH}}^{\mathrm{CP}}$, the CP current increases and saturates, as all the traps are getting pumped.

2.4.3 Frequency-Dependent Charge Pumping

In a normal CP measurement, the frequency of the driving pulse is held constant. However, if one is interested in the frequency behavior of the trap states, a frequency-dependent CP measurement can be conducted. Here it is very important to keep the slope of the signal the same, as the active energy window should be held constant, otherwise two effects (frequency and energy dependence) would overlay. If, for example, the CP current decreases for higher frequencies of the pulse, this would mean that the device has some traps, which do not get reached by a high frequency signal, as their capture constant is too high.

2.4.4 Reverse Bias Charge Pumping

During a CP experiment, the trap states at the Si-SiO_2 interface get occupied and recombination with the opposite charge carrier happens. However, it is possible to exclude traps from this process near the junction by reverse biasing the body-drain diode during the CP measurement. The induced space charge region removes the free charge carriers out of this region, so the traps cannot get occupied and therefore do not contribute to the measured CP current. By applying different reverse bias voltages, the thickness of the space charge region can be varied (further information in [MT01]). If the different measurements are compared, insights on localized Si-SiO_2 interface degradation in the device can be gathered. Figure 2.15 shows the change of the depletion region for different drain voltages.



(a) All contacts on ground

(b) V_D= 4 V, other contacts on ground

Figure 2.15 Visualization of the depletion region between body and drain in a power MOSFET (dashed green line). The depletion region of the junction increases with a positive voltage applied at the drain (reverse biasing the junction, as body is on ground).

Chapter 3

Measurement Setup

The utilized measurement tool to measure all the different structures was a needle prober (see figure 3.1). By contacting small needles on designated pads on the wafer, it is possible to connect certain areas of for example a transistor via the needles with the rest of the measurement setup.

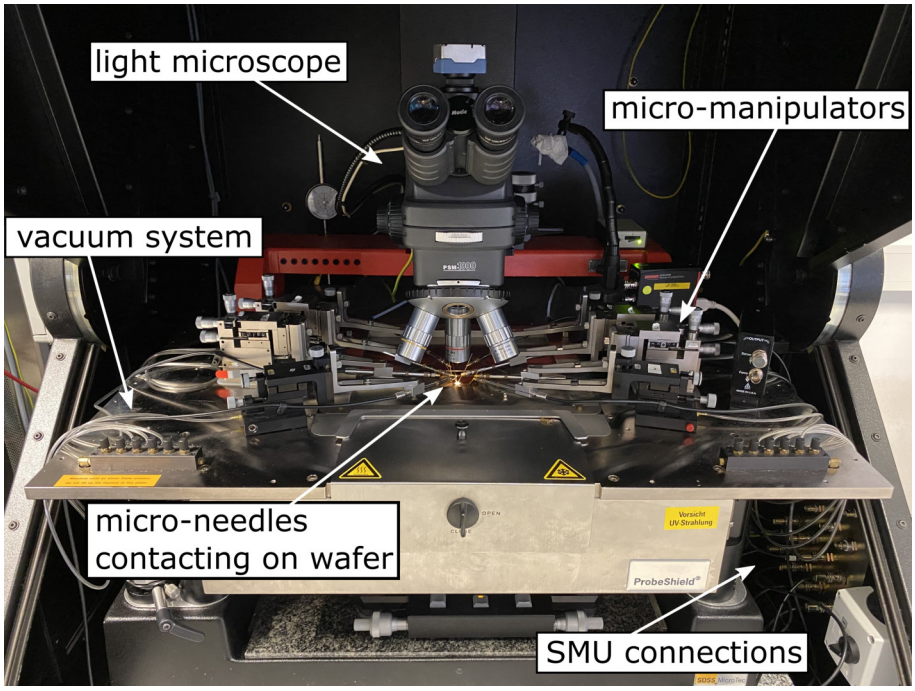


Figure 3.1 Picture of the utilized needle prober. The examined wafer is put on the so called "chuck" to make contact with the backside of the wafer. The structure on the top is then contacted with the use of the needles mounted on the micro-manipulators, which are held in place by a vacuum system.

The cables of the micro-manipulators (used to move the needles) connect to a switching matrix (Keithley 708B), where different measurement devices can be interconnected to the different needles. The control of all the devices was done in software with a LabVIEW program. For most of the measurements and stresses, the Agilent B1500A SMU was used, only for capacitive measurements, an LCR meter (Agilent 4294A) came to use. In all of the measurements, the temperature of the wafers was held constant at 30°C.

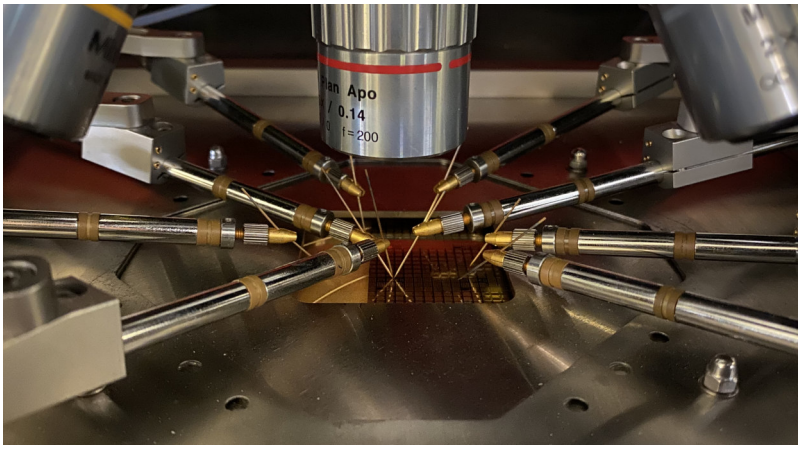


Figure 3.2 A more detailed view of the micro-needles contacting on a structure.

Chapter 4

Results and Interpretation

This section now presents all the measurements which were taken in the course of this thesis. For each device, various measurements have been performed, which are all presented first for the standard device (produced with standard process parameters). To get an insight on the avalanche breakdown and its following Si-SiO_2 interface degradation in the device, constant current stresses with increasing durations were performed between measurement cycles and compared in the following sections.

4.1 Standard Process

The test structures investigated in this thesis (produced with the standard process similar to products) were put on a "process control monitoring" (PCM) unit, which is one small reticle structure besides the product MOSFETs on the wafer to control the process. This PCM structure contains many different variations of a power MOSFET, varying in number of parallel trenches, trench length and therefore active transistor area.

4.1.1 Characteristic Curves of the Transistor

A first investigation of the devices was the measurement of the most common transistor characteristics, mainly the body diode and the transfer characteristic.

Body Diode

The body diode was measured to get an idea about the influence of the avalanche effect on recombination inside the body diode region. The drain was held on ground while the voltage at the body/source contact was swept and the current through the body contact was measured. The results are shown in figure 4.1. To establish a comparison on how the avalanche breakdown effects this characteristic, the device

then was stressed with constant current stress (same stress for all the other following experiments) for different durations, as can be seen in figure 4.1. The diode factor was calculated out of the diode equation [Sze02]

$$I = I_0 \left(e^{\frac{qV}{nkT}-1} \right) \tag{4.1}$$

$$ln\left(\frac{I}{I_0}+1\right) = \frac{q}{nkT}V \tag{4.2}$$

When fitting the logarithmic presentation of the measurement results, one gets a slope, which is equal to the $\frac{q}{nkT}$ term in equation 4.2, out of which the diode factor n can be calculated with k being the Boltzmann constant and T the measurement temperature in K.

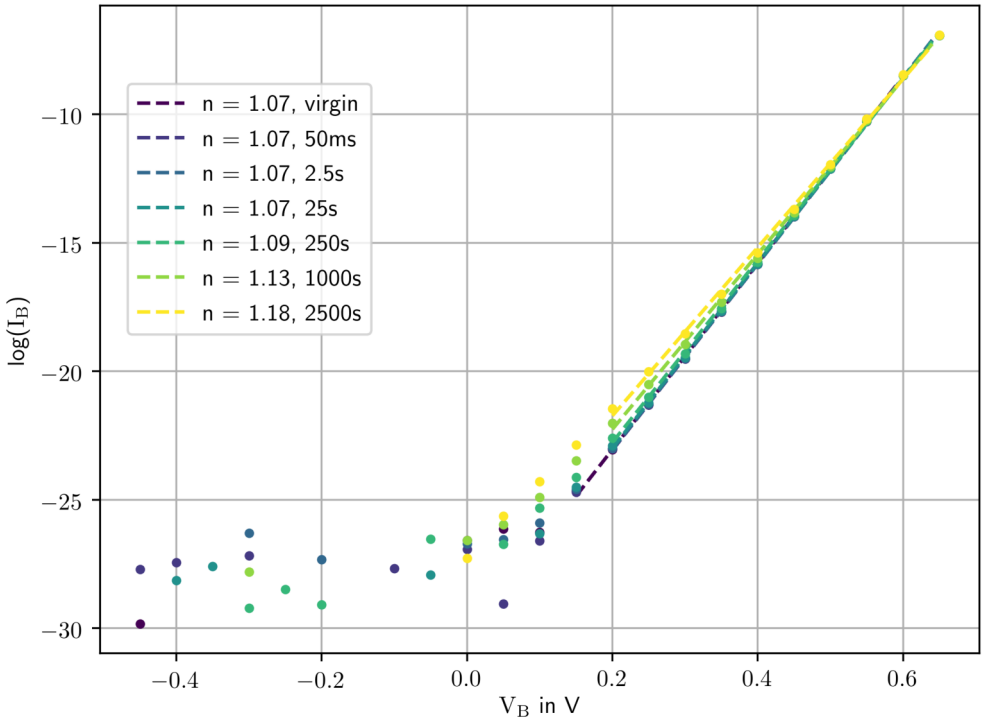


Figure 4.1 Body diode characteristic for different avalanche stresses. The calculated diode factor after equation 4.2 as well as the stress duration are shown in the legend.

When comparing the diode factor for the different stress conditions, a clear increase can be observed with higher stress times. A higher diode factor can be explained

with more recombination occurring inside the diode region. As the device is the same for all the measurements (i.e. same doping and geometry), the increase in recombination can only be because of Si-SiO_2 interface degradation caused by the avalanche breakdown during the stress. New trap states are created, which serve as centers for recombination during the body diode measurement.

Transfer Characteristics

Another characteristic which has been investigated was the transfer characteristic of the transistor. At a certain drain voltage, the gate voltage was swept and the drain current was measured. The result is shown in figure 4.2. Again, constant current stress was applied for different amounts of time to get an idea on the effect of avalanche degradation.

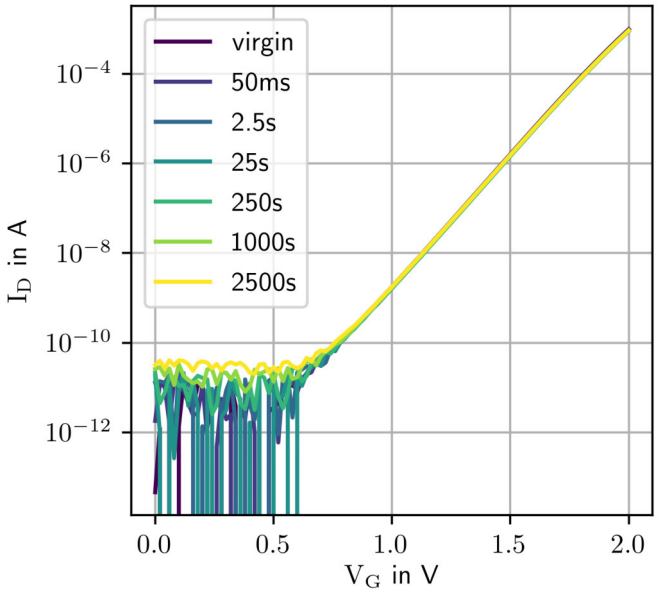


Figure 4.2 Transfer characteristic of a standard device. The applied drain voltage is $V_D = 1\,\mathrm{V}$.

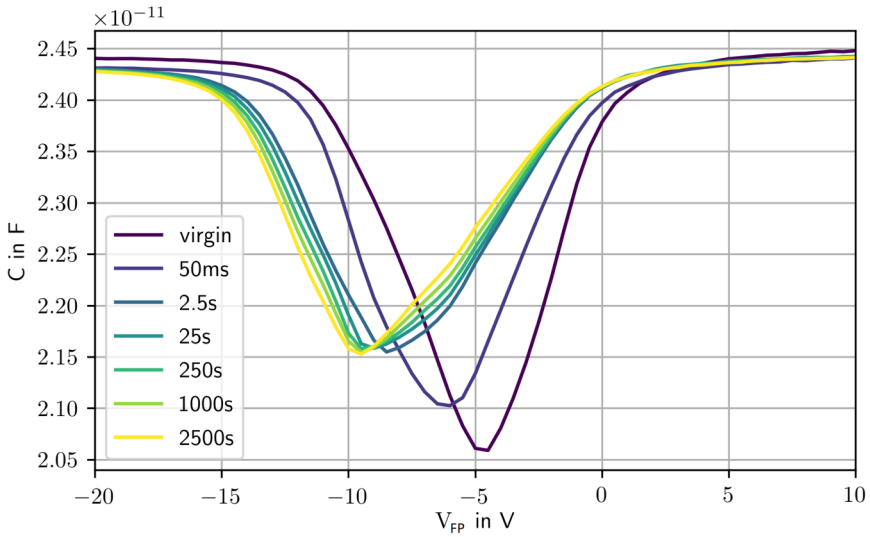
The transfer characteristic shows only insignificantly small deviations between different stress times, all the curves show the same behavior in principle. If there is some degradation at interface of oxide and channel, this has no impact on the transfer characteristic.

4.1.2 Capacitance-Voltage Measurements

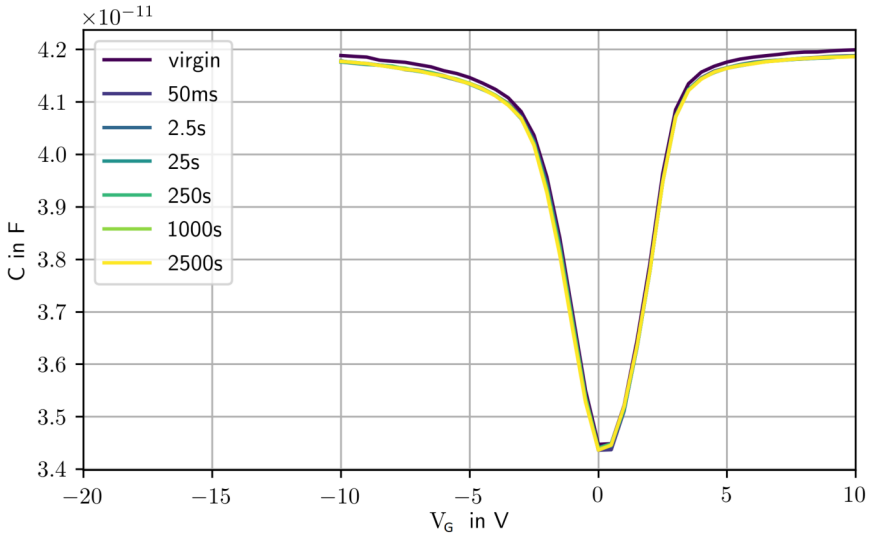
Besides the popular charge pumping method, one can gather insights about the creation of new trap states with capacitance-voltage measurements. With an LCR-meter, the AC capacitance of the contacts can be determined by applying a voltage with a DC component together with an AC component with a small amplitude (0.1 V, 100 kHz in our case). With the DC component applied (seen at the x-axes in figure 4.3), the region near to the contact is put into inversion, depletion or accumulation. The measured capacitance varies between those regions, as for example during inversion and accumulation, the charges are only separated by the $\epsilon_{R,ox}$ of the oxide, whereas during depletion, the $\epsilon_{R,dep}$ of the depletion region also has an impact. Those two can be seen as two capacitors in series and hence the total capacitance drops for those values (compare with [Sze02]).

When looking at the gate capacitance-voltage measurement of our devices in figure 4.3, the usual low frequency behavior of a MOS capacitor is observed. The capacitance is also not impacted by the avalanche stress, as it is hardly changing at all during the constant current stress. There is also no significant difference between the inversion region (positive gate voltages) and the accumulation region (negative gate voltages).

When comparing the CV-measurement at the field plate contact to the gate contact, a clear difference can be observed. Near to the field plate is the drain drift region (n-type), hence this region is put into inversion at negative applied voltages. The minimum of the virgin curve is already shifted to about -5 V compared to the 0 V minimum of the gate capacitance. The stress then results in a deformation of the curve and a shift to even more negative voltages for the field plate capacitance minimum. This phenomenon can be described by the presence of some kind of positive charge after the stress. Positive charge would act as some additional positive voltage, which, combined with the DC component of the applied voltage during the measurement, would result in a shift of the capacitance curve to more negative voltages values. This form of positive charge could mean two things for the Si-SiO_2 interface degradation process: Due to the avalanche breakdown, positively charged carriers could be injected into the field plate oxide and stay there even after the stress is over. On the other hand, new traps with hole-like character could be created during avalanche breakdown which in turn would be occupied during the measurements and hence also would shift the minimum to more negative voltage values. However, it is quite difficult to do interpretation on newly created trap states out of CV-measurements due to the rather complicated geometry in the examined devices (compared to for example planar MOSFETs).



(a) CV characteristic of the field plate contact.



(b) CV characteristic of the gate contact

Figure 4.3 Capacitance-voltage-characteristics of the field plate and gate contact. Measurements done at 100 kHz with 0.1 V AC magnitude.

In addition to the gate and field plate contacts, the capacitance for the drain contact also has been measured. This result can be seen in figure 4.4. As the drain has no oxide between the contact and the silicon area, the measurement cannot be compared to those at gate and field plate and hence, only positive drain voltages were examined, as those resemble the application. The same stress sees an increase in drain capacitance. This increase can also point to the creation of new trap states. Traps, which are energetically close to the band edges can be emptied more easily even close to flat band condition and therefore result in an increase in capacitance [Ent07].

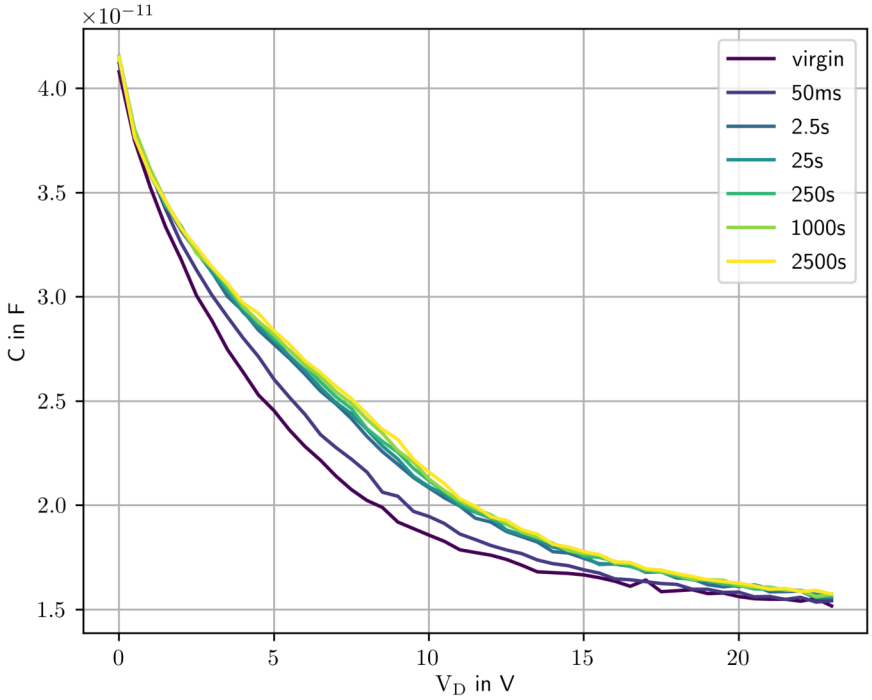


Figure 4.4 Capacitance-voltage-characteristics at the drain contact. Measurements done at 100 kHz with 0.1 V AC magnitude.

4.1.3 Charge Pumping

In all the charge pumping measurements it was important to set the current range of the SMU correctly. During one cycle of the charge pumping pulse, the region at the Si-SiO_2 interface has to be driven into accumulation and inversion. This results in a measured current, which overshadows the smaller CP current, but averages out over time. However, this limits the measuring range, as the range has to be higher than the current needed to charge the field plate capacitance. Otherwise, the data will be wrong. An estimation for the measuring range can be done with the measured field plate capacitance C from section 4.1.2.

$$Idt = CdV \tag{4.3}$$

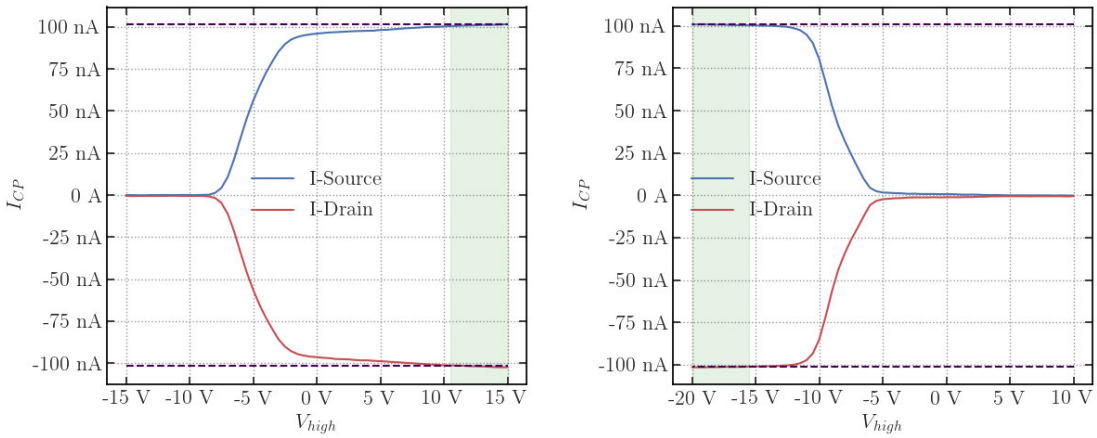
$$I_{max} = C\frac{dV}{dt}_{max} \tag{4.4}$$

As the term $\frac{dV}{dt}_{max}$ is just the maximum slope of the trapezoidal pulse signal, it is straight forward to estimate the maximum current which will occur and set up the range correctly. A range as small as possible is desired to resolve the CP current better. A more detailed description of this can be found in [RPR+19].

Constant High/Base CP

Figure 4.5 shows a constant high and a constant base CP measurement. For both measurements, the current at the source/body contact and at the drain was measured separately. Those have to be the same with different signs to fulfill Kirchhoff's law. The integration time (the time, in which the pulse level stayed constant and the current was averaged around this time to only measure I_{CP} and not the charging of the field plate capacitance) for each separate voltage level was 0.02 s (which has been the same for all other measurements done). One can clearly see at which voltage levels the conditions for inversion/accumulation are fulfilled and where the charge pumping current therefore rises. It quickly saturates, as all traps are getting pumped. To get one value for I_{CP} (which has to be the same for both the const. base and the const. high measurement), the last 10 measurement values are averaged. With this value for I_{CP} it is possible to calculate the trap density in the measured device by using equation 2.6. The active charge pumping area is estimated with the layout dimensions of the trench.

As this measurement gives a good idea about the trap density, one can compare those results for different avalanche degradations by doing charge pumping and afterwards applying constant current stress to the device and repeating the charge



(a) Constant base CP

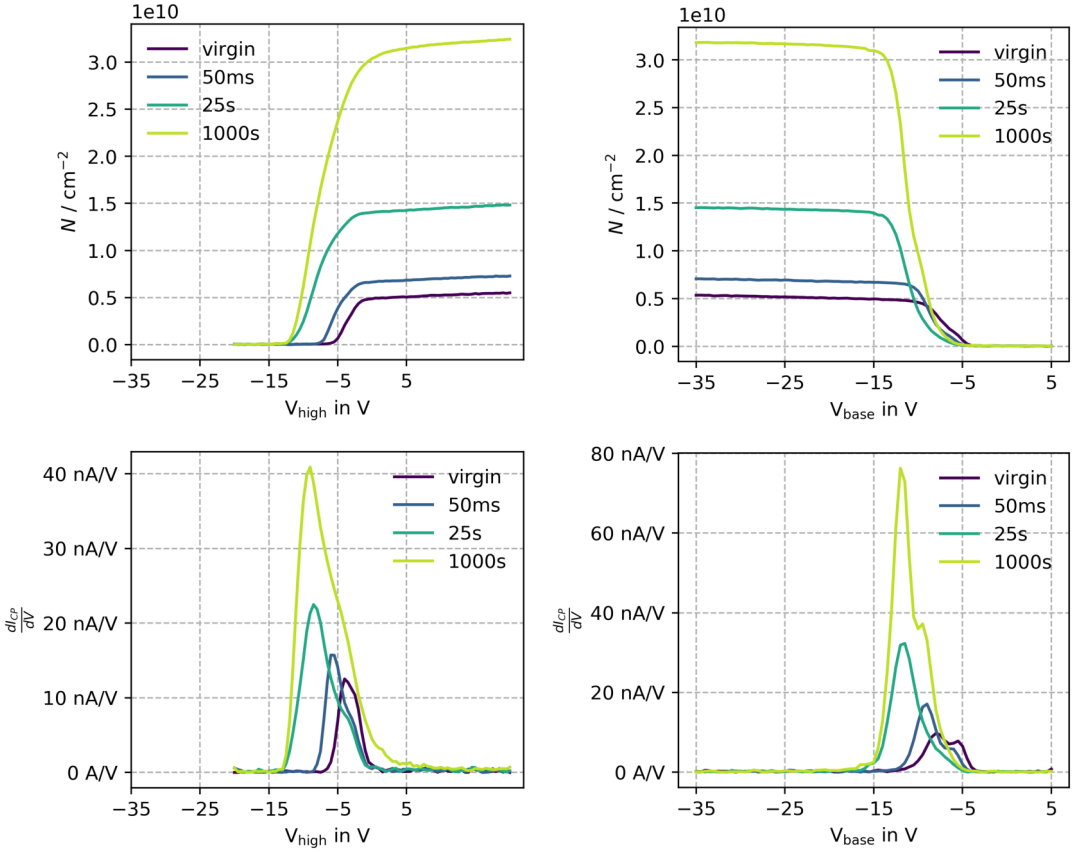
(b) Constant high CP

Figure 4.5 Constant base (left) and constant high (right) CP measurements of a standard device at a pulsing frequency of 120 kHz and a slope of 7.6 V/μs. The green area marks the measurement points which are used to calculate the CP current, which is drawn as a dashed line.

pumping. As the stress forces the avalanche breakdown in the device, it drifts and the trap density is expected to increase after stress. This phenomenon is observed in figure 4.6. Compared to figure 4.5, each value of the charge pumping current is already recalculated to the corresponding trap density. However, only the maximum trap density in those plots can resemble the true one in the device, as all the traps are reached with charge pumping there. It is clearly visible, that the trap density increases after the stress.

Figure 4.6 also shows the numerical derivative of the charge pumping current to visualize the change in I_{CP} at certain CP voltage levels. Peaks can be observed and interpreted. The minimum in the derivative gives an idea, when (i.e. at which CP voltage levels) the trap occupation starts. When comparing the derivative peaks of both the constant base and constant high measurements, it is obvious that the peaks shift to more negative CP voltage levels with higher stress times. This shows that the device with a more degraded Si-SiO_2 interface needs more negative voltage levels to reach the majority of the traps during the charge pumping. This again can be explained in two ways. One reason behind the shift could be the implantation of positive charge carriers during stress into the oxide of the device. Those carriers would stay there even after the stress and act as some kind of positive voltage

in the trench which needs to be neutralized by the field plate voltage during the CP experiment, resulting in a shift of the peaks to more negative values with more positive charge carriers injected. The second explanation follows a similar reasoning, where positive charge acts against the applied CP voltage on the field plate, as the avalanche stress could also generate hole-like traps at the interface, which also would serve as a positive potential.



(a) Constant base CP

(b) Constant high CP

Figure 4.6 Constant base (left) and constant high (right) charge pumping compared after different constant current stresses. The recalculated trap density and the derivative of the CP current is displayed. For both measurements, a shift of the peaks in the derivative is observed towards more negative CP voltages with increasing stress time.

Frequency Dependent CP

There are many different components which influence a charge pumping experiment. One of them is the frequency of the CP pulse on the target terminal of the device (field plate in our case). If the chosen frequency is too small, the total CP current will be very small (as there are less trap occupations and recombinations happening) to the point, where the SNR is not good enough any more. However, if the frequency is chosen too high, also the slope of the pulse has to be increased, which in return increases capacitive currents and therefore the used measurement range in the SMU. So, one has to find a compromise for the chosen frequency. Additionally, there can be frequency dependent traps in the device. To find out if this is the case or not, a frequency dependent CP experiment was done at the standard device. Essentially, it is just a regular two slope CP experiment. However, instead of varying the high or low level of the CP pulse, they are both held constant (in levels that all traps are reached) and the frequency is varied now (with constant slope). By calculating the trap density for every frequency, one can get an idea if there are frequency depended traps in the device or not. If the trap density stays constant over different frequencies, this means that the traps are not influenced by the frequency.

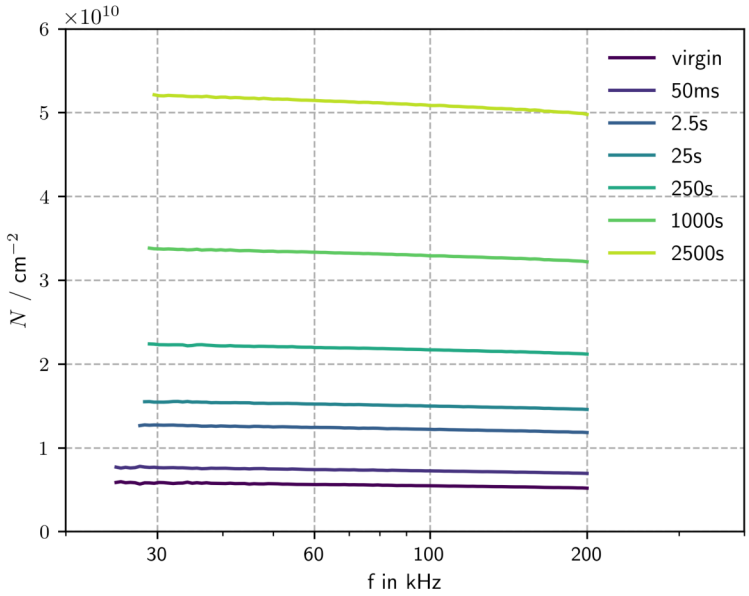
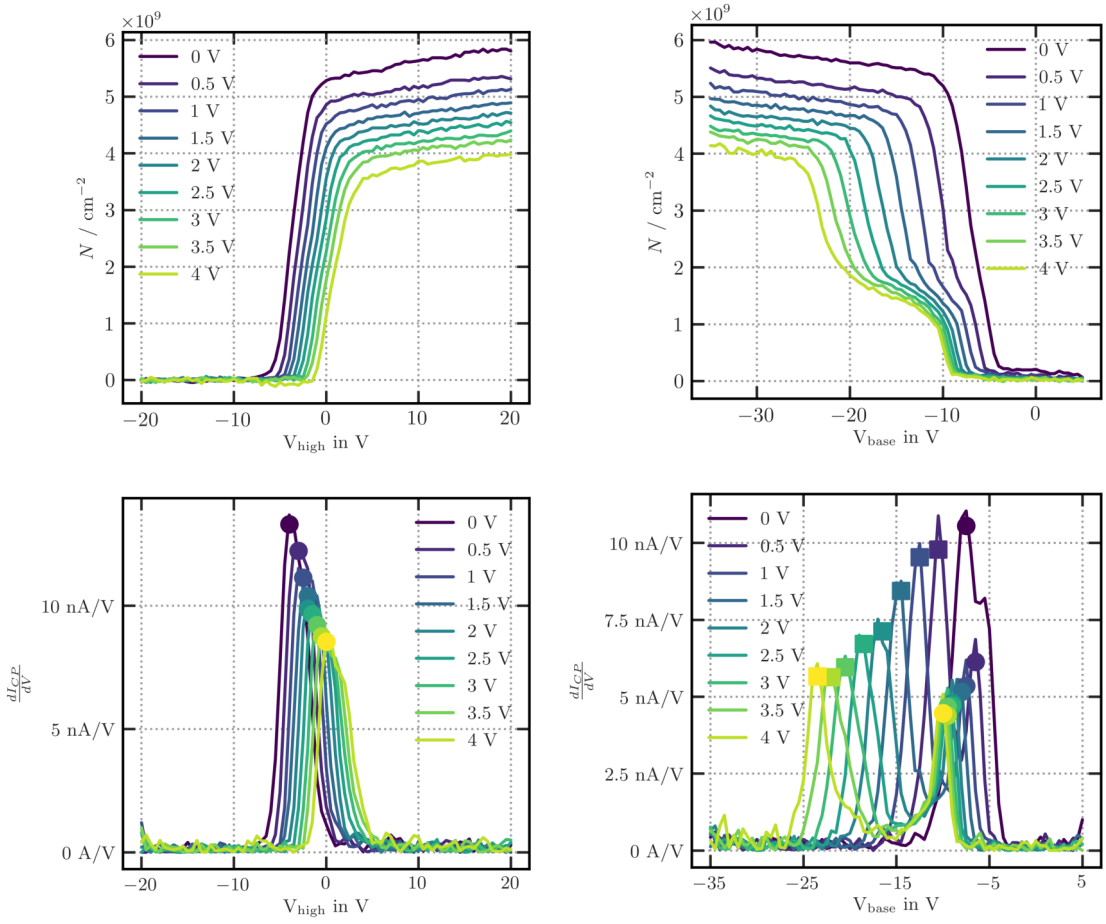


Figure 4.7 Frequency dependent CP compared at different levels of Si-SiO_2 interface degradation.

Figure 4.7 shows the results of this measurement again for different levels of Si-SiO_2 interface degradation. The trap densities stay almost constant for all degradation levels with varying frequency. However, there is a small decrease in trap density observed for all degradation levels, which indicates at least some frequency dependent traps in the device. Those are probably oxide traps with time constants for occupation and emission (see section 2.3.1) and with increasing frequency, those traps do not have enough time during the high or low phase of the pulse to be occupied. Therefore they are not contributing to the trap density at higher frequencies any more.

Reverse Bias Charge Pumping

Up to this point, during the various charge pumping experiments, all terminals on the device except the pumped field plate were held on ground. In this section, so called "reverse bias charge pumping" was performed (see section 2.4.4), in which the size of depletion region of the body drain pn-junction was varied by applying positive voltage levels on the drain in the region of 0-4 V. Different reverse bias voltages are compared for a standard virgin device in figure 4.8.



(a) Constant base CP

(b) Constant high CP

Figure 4.8 Reverse bias CP measurement for a virgin device, constant base (left) and constant high (right).

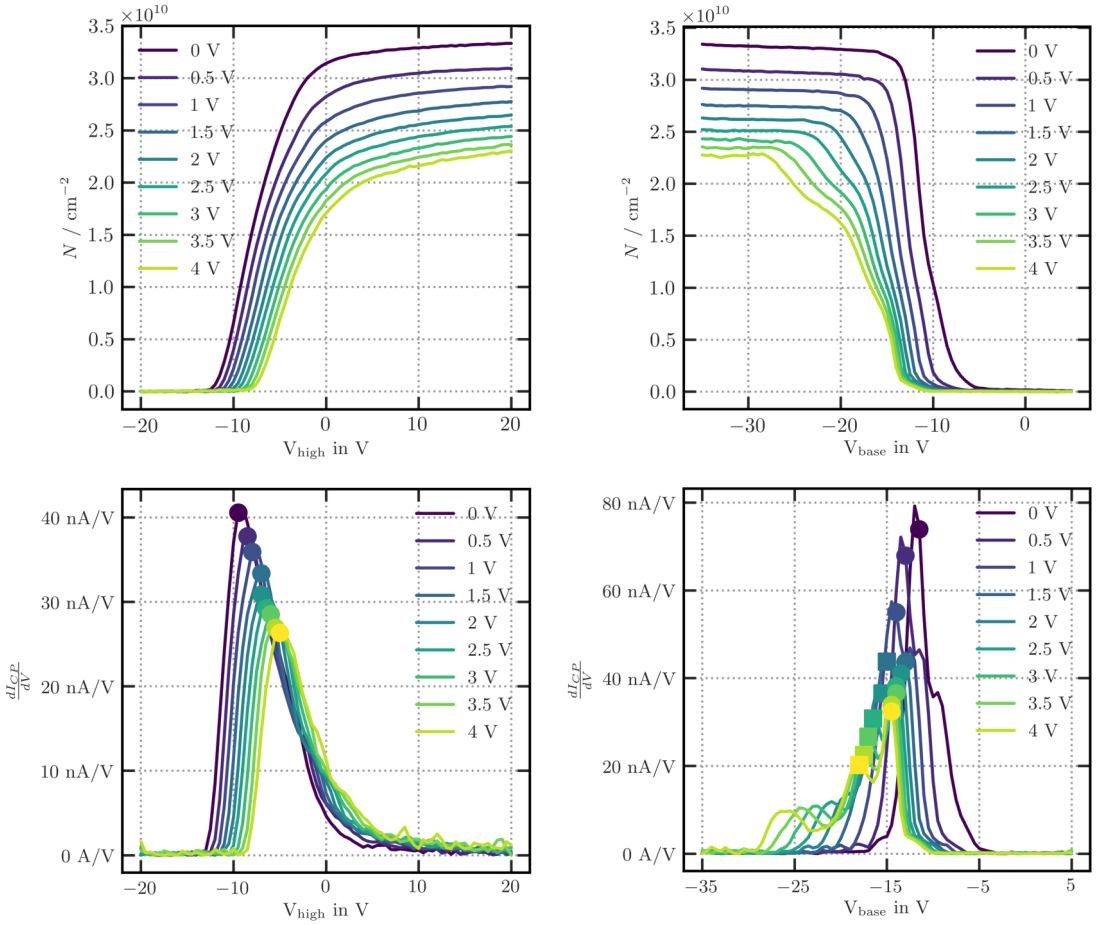
When looking at the displayed trap density in figure 4.8, one can observe a decrease with higher reverse bias voltages. This is exactly what we would predict, as the recalculation from the charge pumping current to the trap density still assumes the same active area, however, the area actually shrinks in size due to the bigger depletion region. This, in turn, cannot be directly measured. So, the trap density might actually be the same, but the measured CP current is less, as less traps are reached.

A second observation is a shift of peaks in the derivative of the CP signal with increasing reverse bias, similar to the shift with increasing Si-SiO_2 interface degradation. In the constant base measurement, it is easily explained. As there is a more positive voltage at the drain terminal, this also has an impact in form of electric fields on the interface between field plate and channel. To compensate for those, one has to apply even more positive voltage on the field plate to start the charge pumping process, hence a shift of the peak to more positive pumping voltages. The constant high measurement features a second peak in the derivative and the peaks shift to more negative CP voltages with increasing reverse bias. To explain this behavior, many simulations have been done by colleagues. One theory was that one peak is for electrons and one for holes, as they can have a different behavior, but this should then also be visible in the constant base measurement, which is not the case. A second approach was the opening of some sort of "hole flow" from body to the field plate-channel interface, which could have a dependence on drain voltage, but this did not result in the same behavior. Further investigations and simulations have to be done to explain this effect.

The same measurements were repeated for a stressed device (constant current stress for 1000 s). The results of those are displayed in figure 4.9. The constant base result shows the same behavior as the stressed device before in terms of reverse bias: With increasing applied drain voltage, the peak of the CP signal shifts to more positive voltages and decreases in height. Again, the higher electric fields caused by the applied drain voltage have to be compensated at the field plate and the depletion region gets larger, preventing some traps from contributing to the CP signal. Compared to the constant base signal of the virgin device, the trap density is increased for all the different drain voltages, which again means that traps were generated inside the whole device because of the avalanche stress. As before, the constant high signal is very difficult to interpret and needs further measurements with different conditions, devices or simulations to get more information.

In general, one would like to get an insight on localized Si-SiO_2 interface degradation with this CP method. If there would be for example a second peak in the derivative after stress (which would suggest some localized degradation, see [AN09],

where they are even called "degradation peaks") and this peak would then decrease more severely compared to the other peak or even vanish, then one can say for sure that there is some kind of localized degradation within the device near the junction at the interface, as an increased depletion region would prevent many localized traps from contributing to the CP signal. This effect may be observed for the devices with different stress conditions, which needs further investigation. As we are not observing a second peak in the constant base signal, no statement can be made about the existence of localized Si-SiO_2 interface degradation.



(a) Constant base CP **(b)** Constant high CP

Figure 4.9 Reverse bias CP measurement for a stressed device (1000s constant current stress), constant base (left) and constant high (right).

4.1.4 Drain Source On Resistance

One very important property of a MOSFET in the industry is the channel resistance between source and drain in the on state, mostly called $R_{DS,on}$. A high $R_{DS,on}$ is not desired, as it results in more ohmic losses when the device is on. Consequently, one is interested in how the avalanche breakdown could influence the change in $R_{DS,on}$ during certain operations. Figure 4.10 shows the result of a $R_{DS,on}$ measurement of a standard device, displaying the relative trend of the on resistance. Again, a constant current stress was applied for some logarithmically spaced time steps to see the effect of the stress (the first point was put as $10^{-4}s$ to show in the logarithmic plot, but really resembles the virgin device).

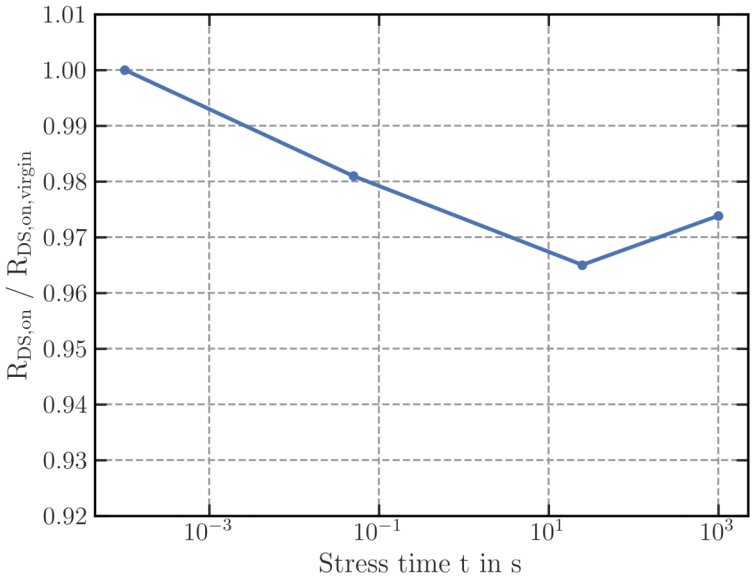


Figure 4.10 $R_{DS,on}$ of a standard virgin device which was then stressed. Measurement done at $V_G = 10\,V$.

The results show that the resistance is influenced by the avalanche stress. The shown $R_{DS,on}$ behavior indicates that trapping occurs and impacts the transistor. The additional charge near and at the oxide-channel interface results in electric fields, which have an impact on the current flow inside the device. However, this drift in $R_{DS,on}$ is expected and the device is designed to account these changes to stay within the datasheet specifications.

4.2 Process Variations

All the described measurements (with the same stress conditions) from the previous chapter were also done with the same devices on differently produced wafers compared to the standard wafer. The variations in the process are as described in chapter 2.1.3 and contain the following dimensions:

- Contact depth variation: deeper contact
- Trench depth variation: deeper trench
- S-Recess variation: a deeper and a more shallow S-Recess

All the different possible combinations between the standard process parameter and the varied ones were investigated, which results in a total of 12 differently produced wafers.

4.2.1 Trap Density Comparison

In this section, the most important measurement results are presented: those of charge pumping, to get a good comparison of the Si-SiO_2 interface degradation levels in terms of trap density. Each process variation is expected to have some sort of impact on the avalanche degradation and hence, the measured trap density.

Single Process Variations

Figure 4.11 shows the results of the charge pumping measurement, again repeated after several constant current stress times only for the devices with one single process variation to get an idea of the impact of those variations, respectively.

When looking at trap density of the device with a deeper **contact depth** (CDepth) etching and comparing it to the one produced with the standard process, one can observe a rather similar trap density at low stresses, whereas N_T is clearly smaller for the CDepth device after more severe stress. This is to be expected, as one explanation of this could be that a deeper contact into the body region of the device would decrease the distance to the drift region and hence, lead to higher electric fields near the contact inside the drift region of the drain. Those higher electric fields would result in more degradation happening near the contact and therefore less degradation near the oxide-channel interface, which shows in the smaller measured trap density.

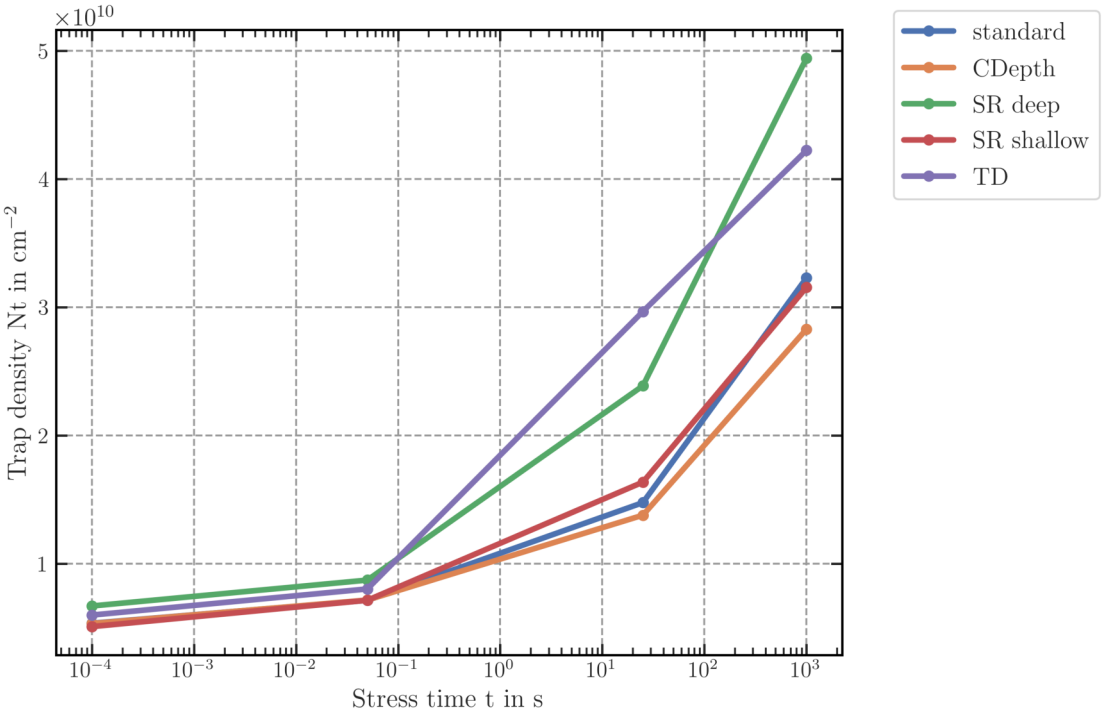


Figure 4.11 Trap density after various constant current stress times for 5 different process variations (CDepth...Contact depth, SR...S-Recess, TD...Trench depth).

The next interesting process variation concerns the devices with a deeper **trench depth** (TD). This is resembled by the yellow line in figure 4.11. In contrast to CDepth, the deeper trench results in a higher initial trap density as well as visibly higher trap densities after more severe stress times. The higher trap density of the virgin device could just be a calculation artifact. As equation 2.6 states, the trap density is depended on i.a. the active charge pumping area. This area was assumed for both the standard trench depth devices as well as the deeper trench devices to be the whole area around the trench. For the deeper TD devices, the area was therefore assumed larger, however, this area calculation was only done roughly with the trench layout and it could be possible, that the active charge pumping area differs slightly from the calculated area. However, the observed increase of N_T for the TD devices cannot be explained with this fact. Further investigation on those devices still needs to be done in order to fully understand this behavior, but it just seems, that there is a nonlinear correlation between trench depth and

Si-SiO_2 interface degradation, meaning a deeper trench and therefore a bigger area of oxide-channel interface results in a more severe degradation.

The following process variation which is to be discussed is the variation of the so called Source-Polysilicon-Recess, also called **S-Recess** (SR). For this variation, two dissimilar alterations for the devices were measured: one with a larger S-Recess (meaning a deeper gate poly footpoint, see figure 2.5) and one with a smaller S-Recess parameter (resulting in a higher gate footpoint) compared to the standard device. First, the larger S-Recess device behavior is discussed, which is resembled by the cyan curve in figure 4.11. Even for the virgin device, a higher trap density is observed. However, unlike the TD devices, the trench area is the same again for the SR devices. When looking at the layout in figure 2.5, one can see that the process variation results in a deeper gate footpoint. As the gate is etched separately into the oxide and the gate oxide is fare more shallow then the field plate oxide, one explanation of the higher trap density could be an influence of the gate etching process on the oxide-channel interface nearby. If this is the case, an increase in N_T could be explained that way. This explanation would also be consistent with the other examined SR process variation, where the gate footpoint lies higher compared to the standard process. This variation has even a slightly smaller trap density than the standard process. The difference is more prominent for the device with deeper SR, as the variation is bigger in terms of nanometers compared to the more shallow SR device. As the stress gets more severe, a big increase of N_T for the deeper SR device can be observed, which could be explained by the fact that accelerated carriers from the avalanche breakdown have a more unconstrained way to degrade the already harmed oxide, resulting in a higher N_T. On the other hand, the more shallow SR device does not have this harm in the oxide near the gate and therefore has a rather similar behavior than the standard device after stress.

Combinations of Process Variations

Now that we have a rough understanding on what every process variation does to the trap density and hence the drift in the different devices, we can have a look at multiple combinations between those particular variations. A total of 12 differently produced wafers and devices were measured in order to gather information on the impact of those process variations on the Si-SiO_2 interface degradation. In figure 4.12, the trap density is displayed for all 12 differently produced devices. Again, all were stressed with constant current stress to force avalanche degradation at the Si-SiO_2 interface.

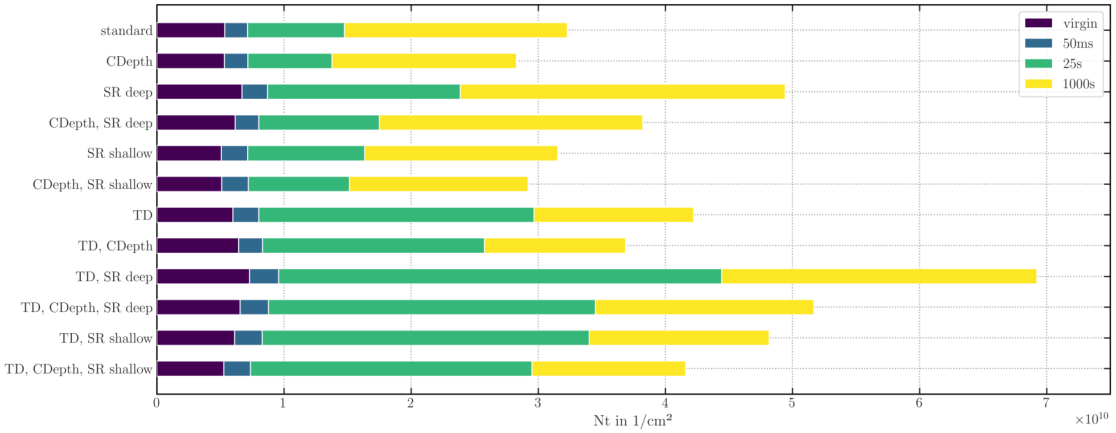


Figure 4.12 Trap density comparison between all 12 different combinations of process variations after various stress times (CDepth...Contact depth, SR...S-Recess, TD...Trench depth).

One initial observation that can be made from figure 4.12 is the consistent impact of contact depth on the trap density. When we compare the devices which have the CDepth process variation to those which do not, we see a clear decrease in N_T, again due to higher degradation near the source/body contact. For all the devices with a deeper TD, an increase in N_T is observed compared to the ones with standard trenches, which is consistent to our assumption above. A deeper SR yields to an increase in trap density across all combinations of wafers, which is also in agreement with our theory of lower gate footpoint and and impact of the gate process. This is also consistent with the more shallow SR devices, as this variation seems to always decrease N_T compared to standard SR or have about the same trap density. In general, the results of those measurements suggest that the examined

process variations have no big impact on each other. The single variations combined still show the same behavior as if they were just the sole variation compared to a standard device.

Since all the examined devices had the same geometry (263 trenches with an area (from top) of $25.7 \cdot 10^{-3}\,\mathrm{mm}^2$), all the measurements above were repeated for a different device area (217 trenches with an area (from top) of $8.8 \cdot 10^{-3}\,\mathrm{mm}^2$). This should eliminate the dependence of the device area and an impact of the border trenches (since the trenches at the border tend to have a higher impact on the total trap density, see ref [RPR+19]). Figure 4.13 contains the same results as figure 4.12, shown in the full bars, representing the standard device size. Additionally, the measurement results of devices of the smaller area are plotted in dashed lines. This way, the same process variations can be compared for both device areas (note that the area used to calculate N_T therefore is also changed, as there are less and shorter trenches in the smaller devices). Considering possible uncertainties in active area calculation, the values for N_T have a reasonable matching for both the device areas. There seems to be the trend that the smaller devices have a slightly higher N_T, but still in the same order of magnitude, which suggests that the border trenches do not have a big influence on the Si-SiO_2 interface degradation inside the device.

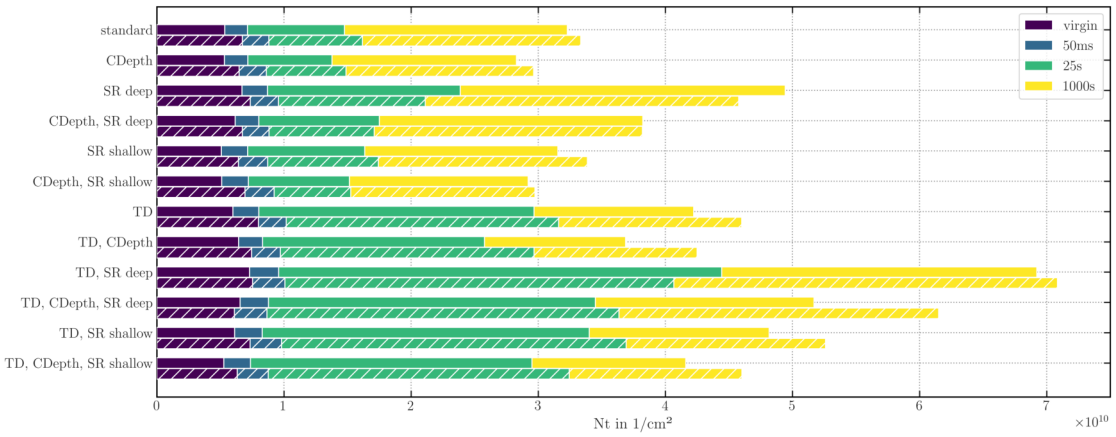


Figure 4.13 Trap density compared for all 12 combinations of process variations, device area: $25.7 \cdot 10^{-3}\,\mathrm{mm}^2$ (full bars) and $8.8 \cdot 10^{-3}\,\mathrm{mm}^2$ (dashed bars) (CDepth...Contact depth, SR...S-Recess, TD...Trench depth).

To further exclude issues such as single device variation, both device sizes were measured a second time with different constant current stress times. Those results are displayed in figure 4.14. As the longest stress was more than double the length as

before, the occurring trap densities are significantly higher compared to the measurement before. But when comparing the same stress times with each other, one can clearly see the similarities. CDepth and more shallow SR yield to lower N_T, deeper SR and TD to a higher trap density and their combinations result in a combination of the single impacts of the variations. The smaller device has a slightly higher N_T for all the wafers, again suggesting an impact of the border trenches.

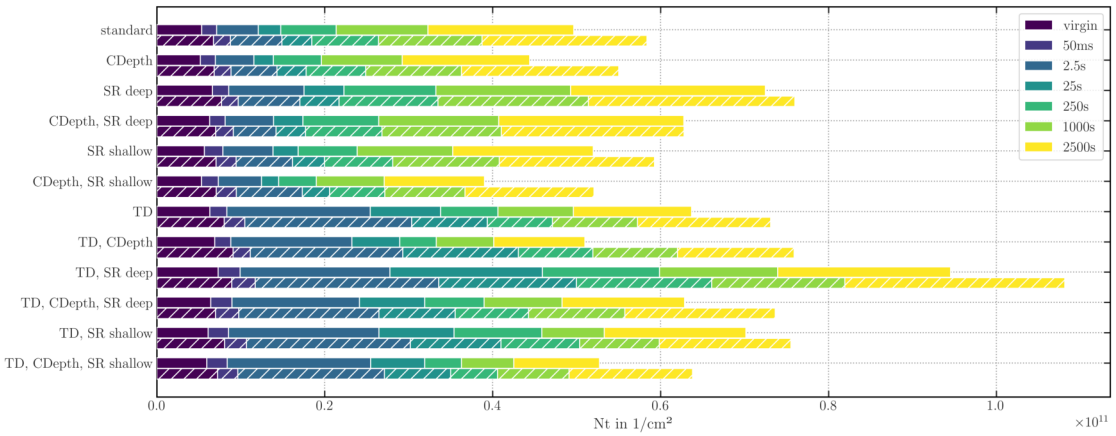


Figure 4.14 Trap density compared for all 12 combinations of process variations, device area: $25.7 \cdot 10^{-3}\,\mathrm{mm}^2$ (full bars) and $8.8 \cdot 10^{-3}\,\mathrm{mm}^2$ (dashed bars), second measurement with different stress times (CDepth...Contact depth, SR...S-Recess, TD...Trench depth).

4.2.2 Drain Source On Resistance

As in the previous section for the standard device, the on resistance $R_{DS,on}$ was measured for all the different wafers and their process variations to get an idea if there is a correlation between process variations, the avalanche stress and the $R_{DS,on}$. The measurement results of devices with only a single process variation are shown in figure 4.15. Every device shows the same behavior as the standard device: a decrease in on resistance in the early stress times and an increase for more severe stress. This drift again is expected, as the devices are designed to account for these changes to stay within the required specifications. To be able to compare the process variations in a reliable way, the plotted values are normalized with the corresponding virgin value for the on resistance. When comparing the single process variations, the contact depth variation shows no notable influence, as the results are nearly identical to the standard device. Similarly, both SR variations show no reasonably

interpretable dependence on $R_{DS,on}$ (this fact also does count for the combined process variations, hence they are not displayed for a clearer view in the plot). The larger Si-SiO_2 interface area of the TD device seems to have bigger impact on $R_{DS,on}$ as it changes more rapidly than the devices with the other variations.

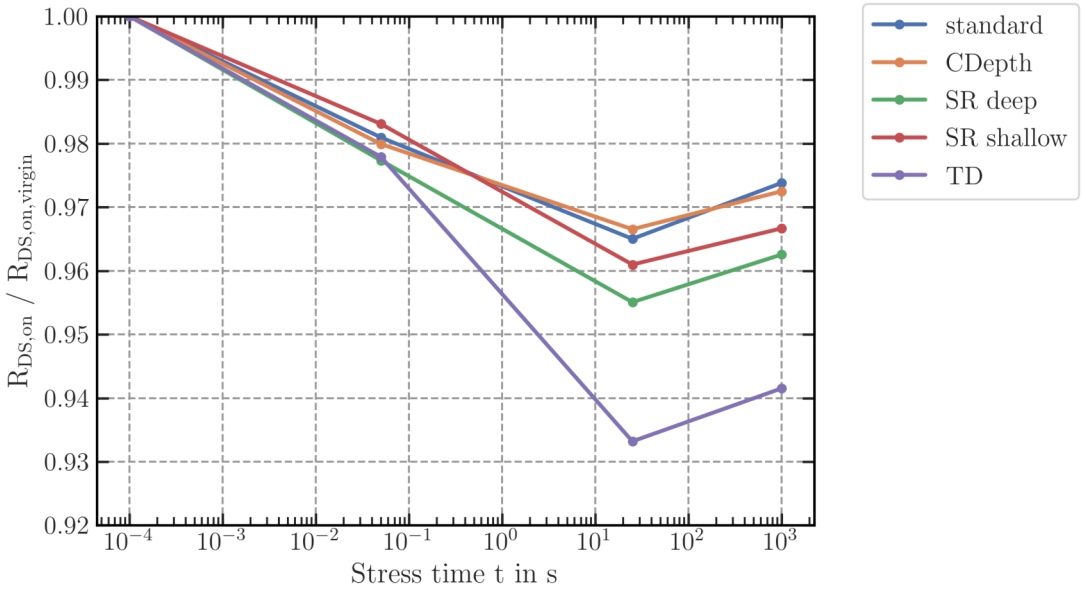


Figure 4.15 Drain source on resistance for 5 different devices, stressed with multiple constant current stresses (CDepth...Contact depth, SR...S-Recess, TD...Trench depth).

Chapter 5

Conclusion and Future Work

This section will give a summary of all the results found in the course of this master thesis. The examined power MOSFET devices all were stressed with constant current stress to force avalanche breakdown which may occur during application and the associated degradation in form of trap creation near the oxide-channel interface. Almost every measurement type showed the effect of the stress in some form. The body diode shows a correlation between stress time and the diode factor, where the factor increases with more severe stress, suggesting more recombination due to trap states. The capacitance voltage measurements present us with an increase in drain capacitance due to more trap states and a shift of the field plate capacitance minimum to more negative voltage levels, which suggests positive charge carrier injection into the field plate oxide or the creation and occupation of hole-like trap states. The charge pumping measurements show an increase in trap density around the field plate, as well as a shift of the charge pumping derivative peak to more negative voltage regions, which again can be explained by positive charge carrier injection or the creation of hole-like trap states. The reverse bias charge pumping experiments show no visible evidence of local degradation at the Si-SiO_2 interface. Additional simulations have to be done in order to understand the device behavior in the constant high measurements and the occurring second peak in the charge pumping signal derivative. With the knowledge of the $R_{DS,on}$ measurements, the theory of positive charge influence is even more strengthened, as those charges would have an impact on the on resistance due to electric fields. With that said, it seems that the avalanche breakdown results in an injection of positive charge carriers inside the field plate oxide or the creation and occupation of hole-like trap states (both have a similar impact on the electrical behavior). With this knowledge, further investigations and simulations can be done in order to avoid those degradation mechanisms and get a better physical understanding on why they are happening.

In regards of the investigated process variations, the results show a clear dependence for all of the examined variations on the trap density. A deeper source/body

contact results in a lower trap density at the oxide-channel interface, as more degradation happens beneath the contact itself. A deeper S-Recess, resulting in a lower gate footpoint, increases the trap density, which is probably due to an impact of the gate process. This information can be used to take a look at the gate process and how exactly it influences the oxide stability. A more shallow S-Recess and therefore a higher gate footpoint decreases the trap density due to the aforementioned of the same aforementioned reason. Future work could try to find out if there come other disadvantages with a higher gate footpoint for the device. A deeper trench results in a higher trap density for the device, but also a more notable on resistance drift during stress. Further investigation needs to be done in order to understand this behavior, maybe also devices with more shallow trenches should be investigated.

Appendix A

List of Abbreviations

CD	Contact depth
CP	Charge pumping
HCI	Hot carrier injection
MOSFET	Metal oxide semiconductor field effect transistor
PCM	Process control monitoring
SNR	Signal to noise ratio
SR	Source-Polysilicon-Recess
SRH	Shockley-Read-Hall
TCAD	Technology computer-aided design
TD	Trench depth

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