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Topological Considerations Regarding EMI-Robustness of Operational Amplifiers

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Graz, November 11, 2020

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ABSTRACT

High robustness against electromagnetic interference (EMI) increases the reliability of modern electronic systems and enables their operation in harsh environments. Interestingly, an often used basic building block, the Miller amplifier, is susceptible to EMI leading to a considerable incorrect output voltage. To counteract this effect, various design criteria and countermeasures are derived for the amplifier pins and simulated with dedicated EMI test benches using capacitive and inductive EMI coupling. The susceptibility of the power supply pins of the Miller amplifier is demonstrated with small-signal models for the power supply rejection ratio (PSRR) and verified by simulations. In order to improve the EMI robustness of amplifiers for a low-power NFC application, a current buffer and a no-capacitor feedforward (NCFF) compensation topology are implemented and compared to the Miller topology using small-signal models. Especially the in the literature less used NCFF compensation topology offers high immunity against EMI with better dynamic performance than the Miller topology.

KURZFASSUNG

Eine hohe Robustheit gegenüber Elektromagnetischen Störungen erhöht die Zuverlässigkeit von modernen elektronischen System und ermöglicht ihren Einsatz in elektronisch gestörten Umgebungen. Der oft verwendete Miller Verstärker ist dabei anfällig gegenüber elektromagnetischen Störungen, die zu einer fehlerhaften Ausgangsspannung führen. Basierend auf diesem Effekt werden Design Vorschriften und Gegenmaßnahmen für die Verstärker Eingänge hergeleitet und mit entsprechenden Test Benches für kapazitive und induktive Einkopplung von Störungen überprüft. Die Anfälligkeit des Miller Verstärkers auf Störungen in der Spannungsversorgung wird mit Kleinsignal-Ersatzschaltbildern für die Power Supply Rejection Ratio (PSRR) demonstriert und mit Simulationen verglichen. Um die Robustheit gegenüber elektromagnetischen Störungen zu erhöhen werden ein Current Buffer und ein No-Capacitor Feedforward (NCFF) kompensierter Verstärker für eine Low-Power NFC Anwendung entwickelt und durch Kleinsignal-Ersatzschaltbilder mit dem Miller Verstärker verglichen. Vor allem die in der Literatur eher unbekannte NCFF Kompensationsmethode zeigt dabei eine hohe Immunität gegenüber elektromagnetischen Störungen und bessere dynamische Eigenschaften als die Miller Kompensationsmethode.

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1 Introduction

1.1 Background

Over decades, engineers all over the world researched on new technologies to keep up with Moore's law. As part of this process, power supply voltages were dropping and frequency ranges are increasing [1], [2]. As well as such modifications work, problems arising from electromagnetic interference (EMI) are getting worse and worse. With the increased frequencies and higher number of integrated devices on single chips, interferences are increasing. Simultaneously immunity is shrinking as supply voltage and dynamic ranges are decreasing [1].

As EMI affects all circuitries, a common design strategy for all components is hard to realize. Therefore a decision must be taken which components are more susceptible then others. Modern technologies often require to use analog and digital circuits on a single chip (mixed-signal integrated circuit (IC)). Thanks to the basic concept of digital signals, a certain threshold for electromagnetic disturbances is given by digital circuits. On the analog side however, signals arising from electromagnetic disturbances often can not be distinguished from intended input signals and can therefore easily spread out over the whole chip [3]. Throughout all analog circuitries operational amplifier (OpAmp) are considered as the predisposed victims of EMI due to their high gain architecture [4]. In Fig. 1.1 a simulation of an OpAmp interfered by short high-frequency EMI strobes with amplitudes of 200 mV is shown. The distorted output voltage demonstrates the susceptibility of OpAmps, which needs to be reduced to guarantee a confidential operation.

In the industry often two-stage amplifiers are used because they provide higher gain than single-stage amplifiers and are able to drive resistive loads. However, frequency compensation must be applied and these compensation methods often are the cause of inferior EMI robustness of two-stage amplifiers [5]–[7]. Especially the well known Miller compensation suffers from a poor power supply EMI performance [8]–[10]. This behavior is to a large degree determined by the used frequency compensation and not by the design of the transistors [7]. Because of the omnipresent Miller compensation, modern

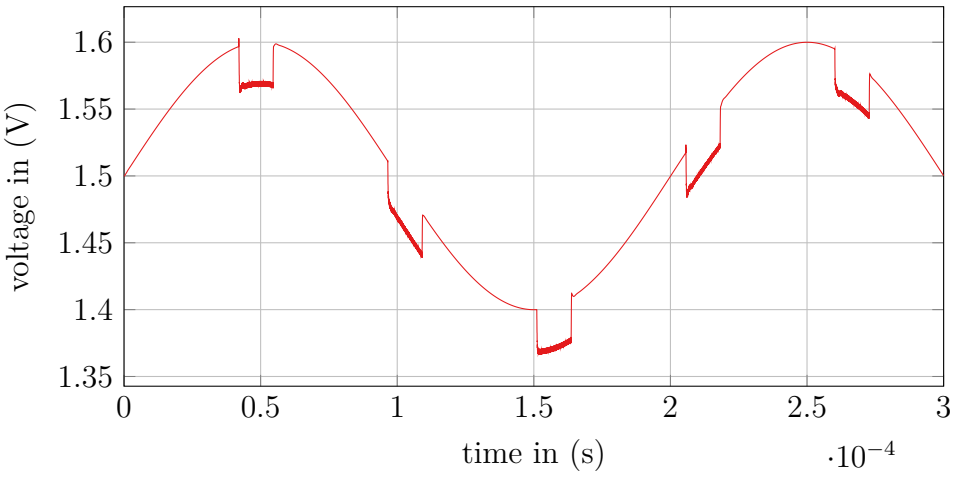


Figure 1.1: Simulation of an amplifier interfered by high-frequency EMI strobes

textbooks do not include other compensation methods very often in their contents [11] and therefore other, often better frequency compensations methods regarding EMI, are not frequently used to compensate two-stage amplifiers.

1.2 Scope of the Thesis

So what can be done to increase the robustness of OpAmps against EMI and which measures are useful for which application? This thesis summarizes different EMI counteractions and gives an overview of the theoretical backgrounds of each measure. The effectiveness of each measure is investigated and impacts on the amplifier ac performance and power consumption are considered. In order to improve the EMI robustness further, the power supply rejection ratio (PSRR) of different frequency compensation methods is investigated with small-signal models. Based on the results of the analyses, a in the literature less mentioned frequency compensation method using feedforward compensation without capacitances theoretically should offer high EMI immunity. But until now no direct EMI considerations were taken of this topology.

In order to investigate the EMI susceptibility, dedicated EMI test benches (TBs) are designed and applied together with a simple simulation framework. Small-signal models of three frequency compensation topologies are constructed to verify the simulations and to deliver design criteria for an increased EMI robustness.

1.3 Outline

In order to investigate the susceptibility of operational amplifiers, the thesis is divided into five chapters: After the introduction, the main effects of EMI entering an amplifier are investigated and linked to the commonly known output voltage shift in Chapter 2. To characterize the EMI susceptibility, two figures of merit (FOM) are defined and compared on their effectiveness to describe the electromagnetic susceptibility (EMS) of amplifiers. Considering these FOM, measurement and simulation setups are examined and discussed with their limitations for EMI measurements on transistor level. Based on the theoretical EMI effects, countermeasures to increase the robustness of amplifiers are introduced in Chapter 3. Hereby measures for the input and output (I/O) pins are considered in a first step while EMI robust frequency compensation methods are presented in the second half of the chapter. Proceeding with the results of the first chapters, a Miller amplifier and dedicated EMI TBs are designed in Chapter 4 and used to evaluate simple EMI measures for the I/O pins of the Miller amplifier. With the simulation results a table is established in order to show the effectiveness of each EMI measure on the amplifier robustness. In Chapter 5 the susceptibility of the Miller amplifier on the power supply is confirmed with small signal models. Current buffer and feedforward compensated frequency compensation topologies are designed and compared to the Miller amplifier. From the simulation results tables are established for the ac and EMI performance in order to give guidelines for future designs.

2 EMI Susceptibility of Operational Amplifiers

Commercially used operational amplifiers need to withstand a large number of disturbances when used together with digital circuitry or in harsh environments. The effects of EMI on amplifiers will be investigated to find critical areas that can be improved. As EMI arising from the power supply often is considered separately from the I/O pins, the well known FOM PSRR is introduced and discussed. In order to measure effects arising from EMI in a correct matter, the last segment of this chapter is dedicated to EMI measurement. With the knowledge of the effects of EMI and the basic principle of EMI-TBs all fundamental and important information are then known in order to harden and test amplifier against EMI in later chapters.

2.1 Effects of EMI on Operational Amplifiers

Some of the most fundamental circuits blocks in analog chip design contain operational amplifier consisting of metal-oxide-semiconductor field-effect transistors (MOSFETs). Such circuitry blocks are used all over the chip and can therefore easily be exposed to conducted EMI on all pins. Once electromagnetic signals are mixed up with the input signals, they can not be distinguished and are therefore difficult to prevent. A common effect of EMI entering an amplifier is a dc shift of the output voltage as demonstrated in Fig. 1.1. Without countermeasures this effect can be quite large under the influence of large disturbances and can debias complete circuitries connected to the OpAmp.

But how does this dc shift occur? A very trivial example from [12] is presented in Fig. 2.1: A source follower stage is influenced by a small sinusoidal electromagnetic disturbance at the gate of transistor M_1. If the frequency of the injected signal is lower then the pole frequency of the output pole composed by the source resistance R and the output capacitance C, the output voltage will be the same as the injected signal. No dc shift occurs as the capacitor is charged and discharged within one period by the output signal. However, if the injected signal has a higher frequency then the output

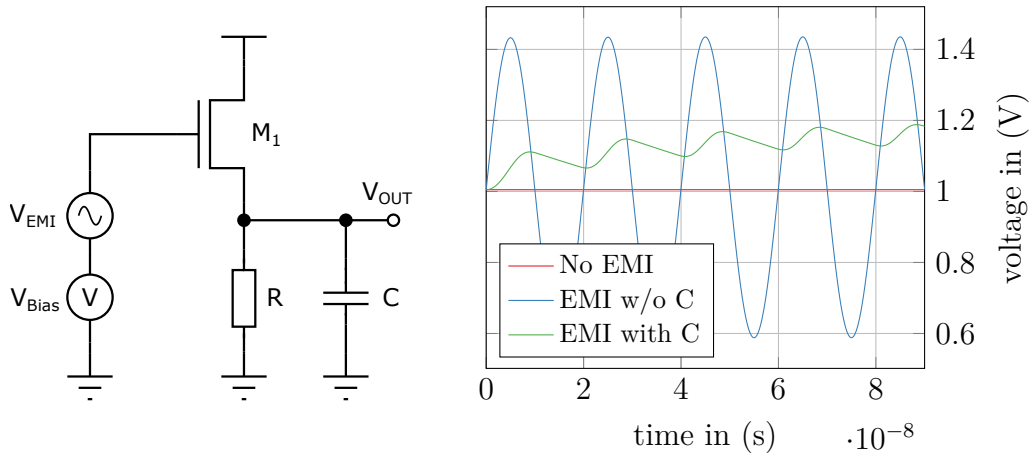


Figure 2.1: Simulation of a basic source follower interfered with EMI and corresponding output voltage shift as result of the excited output-pole frequency.

pole, the capacitor will not be able to charge and discharge within one input period and therefore asymmetric charge rates are produced. The result is a shift of the dc output value which can reach several 100 mV depending on the frequency and the amplitude of the interfering signal.

As demonstrated in this simple example, the output shift can be prevented if the pole frequency is shifted to higher values. Considering an OpAmp, increasing the output pole-frequency would implicate increasing the bandwidth [3]. However, this simple procedure is not easily practicable in real life applications as the bandwidth is limited by a great number of factors. If the accumulation at the output cannot be avoided, the sources of the shift need to be considered. It has been shown that the effect is related to three basic phenomena [13], [14]:

- Slew rate asymmetry
- Parasitic input capacitors
- Non-linear behavior of the input stage

It is well known in the literature that for lower and medium EMI frequencies the effect of slew rate asymmetry plays a major role while for higher frequencies the parasitic capacitances determine the EMI performance of the circuit [14]–[18]. To understand the meaning of this phenomena, they all three are considered further on in the next sections.

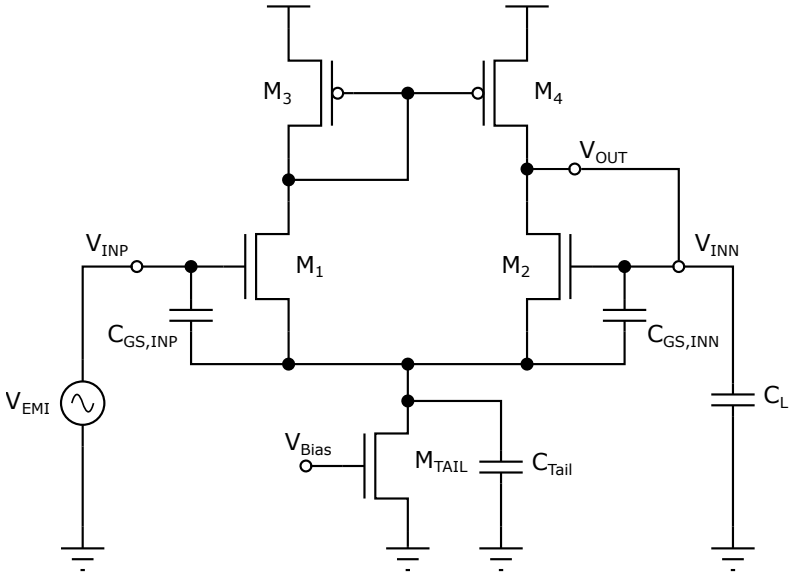


Figure 2.2: Simple CMOS OTA in unity-gain configuration with parasitic capacitances.

2.1.1 Slew Rate Asymmetry

Caused by the limited slew rate of amplifiers, slewing can distort the relationship between input and output signal heavily. As long as both the positive slew rate SR_+ and the negative slew rate SR_- correspond to each other, no dc shift takes place at the output since the output capacitor charges and discharges equally. Unfortunately, SR_+ and SR_- rarely match together. In [1], [3] and [19] mainly three reasons have been mentioned:

- Charge modulation inside the bias transistor: To understand this effect, a basic operational transconductance amplifier (OTA) is assumed to be connected in voltage follower configuration as visible in Fig. 2.2. If a positive voltage step is applied to the non-inverting input, the output follows this step and the voltage at the source of M_1 and M_2 increases. This leads to a higher drain-source voltage of bias transistor M_{Tail} and increases the bias current I_{Bias} due to the channel-length modulation (CLM) effect [1]. Assuming a negative voltage step at the input, the same effect happens but in the opposite direction, I_{Bias} decreases due to the lower V_{DS} of M_{Tail}. Uniting both effects leads to a higher bias current during positive voltage steps then on negative voltage steps. As I_{Bias} directly is linked to SR_+ and SR_-, different slew rates are produced.

- Asymmetries in the circuit topology: Asymmetric circuit architectures itself easily lead to asymmetric slew rates. An example is a basic Miller OpAmp where charging and discharging the dominant output capacitor is not symmetrical. More

symmetric amplifier architectures as the folded-cascode (FC) topology [4] or cross coupled architectures [18] decrease the difference between positive and negative slew rate to a minimum and increase immunity against EMI.

- Parasitic capacitances: The major parasitics capacitances of the amplifier differential input stage according to [19] are indicated in Fig. 2.2. As these parasitics play an important role not only for slew rate asymmetries but also for EMI robustness at higher frequencies, they are considered in more detail in the next section.

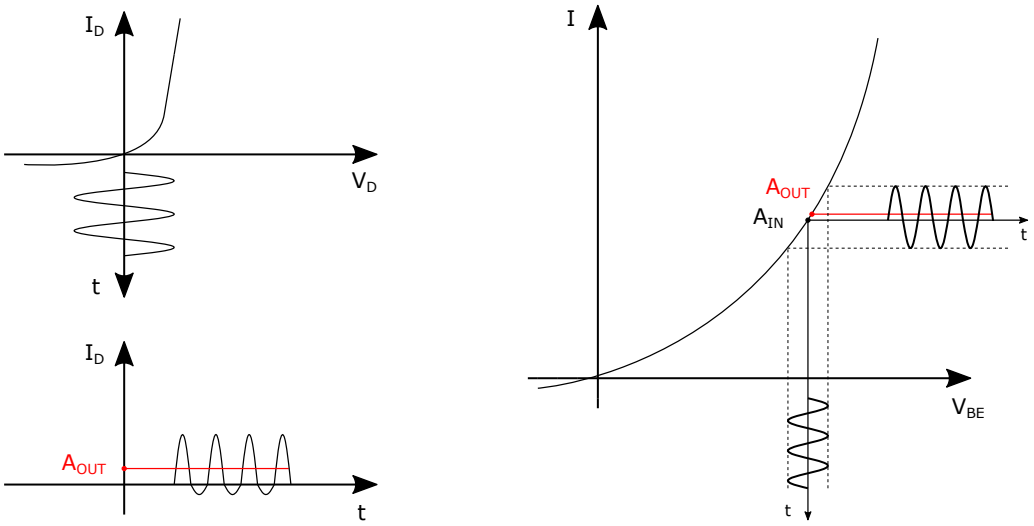
2.1.2 Parasitic Input Capacitances

In the literature, another cause of dc shift often is stated as effect arising from the parasitic capacitances [1], often referred as "Effect of strong nonlinear behavior of the input stage" [3, p. 144]. As for all effects concerning EMI, parasitics play a major role and it is not easy to distinguish between the influences raised by the particular parasitic capacitors. Graffi et al. noted in [1] that the time-dependence of the gate-source voltages and drain currents from both transistors of the input pair are different when the amplifier is connected in feedback. By assuming a voltage follower configuration and setting $C_{GS,INP} = C_{GS,INN} = C_{GS}$, they derived expressions for both gate-source voltages:

$$V_{GS,INP}(t) = V_{IN}(t) \cdot \frac{C_{GS} + C_{Tail}}{2C_{GS} + C_{Tail}} \tag{2.1}$$

$$V_{GS,INN}(t) = -V_{IN}(t) \cdot \frac{C_{GS}}{2C_{GS} + C_{Tail}} \tag{2.2}$$

One can easily see that $V_{GS,INP}$ attains larger values than $V_{GS,INN}$ and so the corresponding drain currents do. Assuming disturbances with high frequencies and high amplitudes that drive the input transistors in cut-off region, (2.1) and (2.2) indicate that the time in cut-off will not be the same for both transistors [1]. In fact, the distortion in transistor M_1 is higher then in transistor M_2. Considering very high EMI amplitudes, not only M_1 but both input transistors are forced to cut-off and alternately produce strong non-linear distortions [3]. The basic principle of such strong non-linear distortion is explained with the concept of a diode in Fig. 3.9a where the output current is heavily distorted by a sinusoidal voltage applied to it. To minimize this effect, the parasitic tail capacitance C_{Tail} can be reduced or the gate-source capacitances can be increased to equalize $V_{GS,INP}$ and $V_{GS,INN}$. To distinguish between the different effects arising from C_{GS} and C_{Tail}, this chapter was devoted to the input capacitors C_{GS} while the next chapter considers C_{Tail} more accurate. Nevertheless, both expressions mentioned at the beginning of this section describe the matter in a truly correct way.



(a) Strong non-linear distortion

(b) Weak non-linear distortion

Figure 2.3: Strong and weak non-linear distortion effects for a diode and a transistor

2.1.3 Non-Linear Behavior of the Input Stage

Differential input pairs are used in almost every OpAmp to amplify voltage differences between the inputs pins and to reject common-mode signals. However, under the presence of high-frequency electromagnetic distortions, the latter changes its behavior. As indicated in Fig. 2.2, there exists a parasitic tail capacitance C_{Tail} from source to ground of the tail current source transistor. This capacitance is to a small extent formed by the parasitic drain-bulk capacitance of the tail transistor itself, but mainly by the well capacitances of the input transistors if they are placed in a separate well [3], [12], [14]. To understand the meaning of this parasitic capacitances, a distinction must be made between low and high frequencies: At low frequencies, C_{Tail} acts like an open circuit and does not influence the behavior of the input differential pair. However, at high frequencies, the situation changes if common and differential mode signals are considered together. Hereby C_{Tail} shorts the tail current source and decouples both sides of the input pair. While the average V_{GS} of both input transistors is equal, the output potential suffers from a dc shift if a common-mode signal is superimposed on the input because of the non-linearity of the input transistors [14]. This is shown in Fig. 3.9b for a single input transistor. A mathematical model for amplifiers interfered by EMI is derived in [3], [20], [21] with the help of a two-input Volterra series:

$$V_{OFF} = \frac{1}{V_{GS1} - V_T} \int_{-\infty}^{\infty} |H_{CM}(j\omega) \cdot V_{CM}(j\omega) \cdot V_{DM}(j\omega)| \cdot \cos\phi \; d\omega \tag{2.3}$$

$$\phi = \arctan\left(\frac{\mathrm{Im}\{H_{CM}(j\omega) \cdot V_{CM}(j\omega) \cdot V_{DM}(j\omega)\}}{\mathrm{Re}\{H_{CM}(j\omega) \cdot V_{CM}(j\omega) \cdot V_{DM}(j\omega)\}} \right) \tag{2.4}$$

In both equations V_{OFF} expresses the input offset voltage, V_T the threshold voltage, V_{CM} the input common-mode voltage, V_{DM} the input differential mode voltage and H_{CM} the transfer function for common-mode signals. Measurements confirmed the good agreement of the model as long as only weak distortion was present and the transistors stayed in their operation regions [21]. The reason that Volterra series were used lies in the existence of memory elements in terms of capacitances. As C_{Tail} is present, the bias current I_{Tail} has to be considered as an input variable and therefore a two-input Volterra series expansion is considered [21]. In agreement with [3] one can see that the input offset voltage V_{OFF} rises with the product of the magnitudes of the common and differential mode EMI signals and the phase between them. Furthermore the offset decreases if the overdrive voltage (V_{GS} - V_T) is increased. Concerning H_{CM}, the parasitic capacitances C_{GS} and C_{Tail} play a huge role and C_{GS} needs to be increased and C_{Tail} decreased. This can be explained with the formula for H_{CM} given in [22]:

$$H_{CM}(j\omega) = \frac{j\omega \cdot C_{Tail}}{2 \cdot gm_1 + j\omega \cdot (C_{Tail} + 2 \cdot C_{GS})} \tag{2.5}$$

2.2 Power Supply Rejection Ratio

In modern processes analog and digital building blocks need to work together on single chips. This leads to unwanted interaction and crosstalk between internal circuitry caused by different EMI coupling paths. One path is formed by the power supply rails. Disturbances and parasitic effects from the package vary the voltage on the supply and ground rail and are often declared as supply bounce respectively ground bounce [23], [24]. This happens because it is not economic to route dedicated supply rails to every single building block. To counteract the supply bounce phenomena, either the generation of the disturbances can be avoided or the susceptibility of the victim can be decreased. As the source of disturbances is not topic of this thesis, only the robustness of the victims is considered. The sensitivity of electronic circuits against fluctuations on the power supply rails is often declared as power supply rejection ratio (PSRR). This ratio is a measure of the ability of the OpAmp to reject ripple noise from the power supply rail [25] and should therefore also be usable for EMI investigations. A high PSRR could imply high robustness against EMI on the supply rails as disturbances are isolated from the amplifier gain nodes and not further feedforwarded to circuitries connected on the output pin. This assumption is investigated further on in the next chapters.

2.2.1 Definition of the Power Supply Rejection Ratio

In a general electric system three main nodes exist: input, output and power supply. Mostly only the voltage transfer function from input to output A(s) is desired but thanks to parasitic effects also a transfer function from the power supply to the output $A_P(s)$ exists. The power supply rejection ratio (PSRR) is defined as the ratio between both transfer functions A(s) and $A_P(s)$ in the frequency domain [5]:

$$PSRR(s) = \frac{A(s)}{A_P(s)} \tag{2.6}$$

As the amplifier gain A(s) and the supply gain $A_P(s)$ are frequency-dependent also the PSRR is frequency-dependent. Increasing A(s) in (2.6) by increasing the unity-gain frequency (UGF) of the amplifier increases PSRR in the same way. To compare different amplifiers, the PSRR is often normalized at the amplifiers unity gain frequency where PSRR equals the inverse of the power supply gain $A_P(s)$ [5].

2.2.2 Parasitic Gains

A different approach to the area of parasitic gains is presented by Saeckinger, Goette and Guggenbuehl in [6]: By applying gauge-invariance they showed that the parasitic gains are not independent of each other and that their sum is close to unity in practical examples. They expressed this in terms of the common-mode rejection ratio (CMRR), the PSRR from the positive and negative power supply and the differential gain A(s):

$$\frac{1}{CMRR(s)} + \frac{1}{PSRR_{VDD}(s)} + \frac{1}{PSRR_{VSS}(s)} = \frac{1}{A(s)} \cdot \frac{Z_{L0}}{Z_{L0} + Z_{OUT}} \tag{2.7}$$

Expressing all the ratios in gains leads to

$$A_{CM}(s) + A_{VDD}(s) + A_{VSS}(s) = \frac{Z_{L0}}{Z_{L0} + Z_{OUT}} \tag{2.8}$$

where all the gains refer to their associated rejection ratios, Z_{OUT} to the output impedance of the amplifier and Z_{L0} to the reference load for which the gains and rejections ratios are specified. Without load Z_{L0} approaches infinity and the parasitic gains sum up to unity [6].

For designing amplifiers with a high PSRR, (2.8) indicates a huge step back as it implies that a decreasing of the parasitic power supply gain increases the common-mode gain.

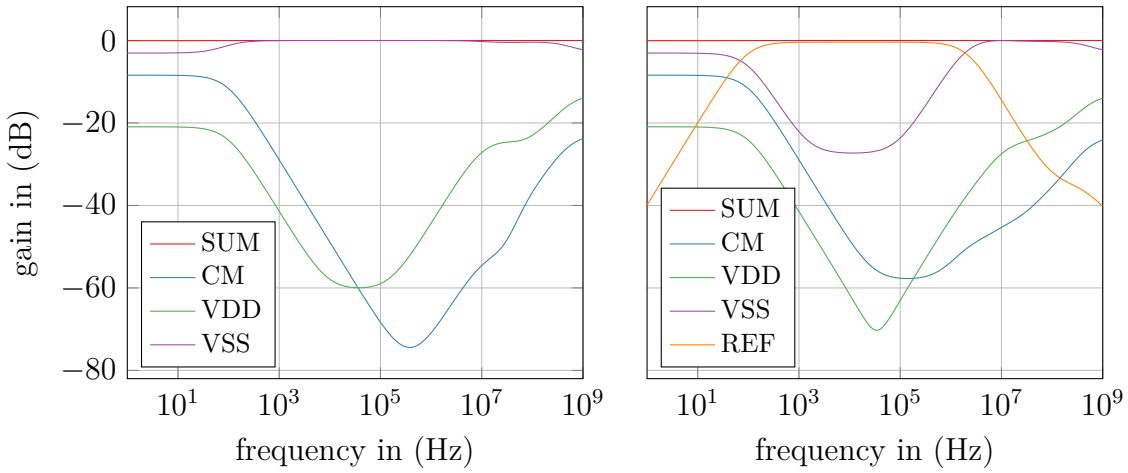


Figure 2.4: Simulation of the parasitic gains of a Miller amplifier without and with an additional noise-free V_{Ref} pin. Clearly the parasitic gains add to a calculated overall sum A_{Sum} of one. By including an additional V_{Ref} pin other parasitic gains are forced to lower values.

Furthermore it implies that at least one of the three parasitic gains need to be in the order of unity which in practice often applies to one of the power supply gains considering classic two-stage amplifiers [6].

So what can be done to increase the PSRR without influencing CMRR? Saeckinger et al. explained this in [6] by introducing an additional input terminal V_{Ref} which gives an additional degree of freedom (e.g. V_{Ref} as bias voltage for cascodes). By designing the circuit with the additional input in a way that the parasitic gain A_{Ref} to the output is unity, the remaining parasitic gains tend to zero. It is worth noting that in order to decrease the parasitic gains, V_{Ref} needs to be connected to a noise-free potential against which the signals can be defined. Otherwise the newly added input terminal adds noise to the output too. By designing the additional circuitry in a way that A_{Ref} is close to unity over a wide range of frequencies, A_{VDD} and A_{VSS} and hence the PSRR are improved as demonstrated in the simulation in Fig. 2.4 which proves the stated concept.

As explained in [6], the concept holds also for fully differential (FD) amplifier where the additional input terminal gets used as input for the desired output common-mode voltage. Due to the fact that the common-mode feedback (CMFB) circuit should work for the whole frequency range, the additional parasitic gains are forced close to zero. This is one mathematical expression why basic FD amplifiers outperform single-ended (SE) amplifiers in terms of CMRR and PSRR without additional or extra circuity measures. Moreover Saeckinger et al. indicated that thanks to the CMFB also the parasitic gains of the individual outputs of a FD amplifier are improved significantly when the FD amplifier is used in a SE version.

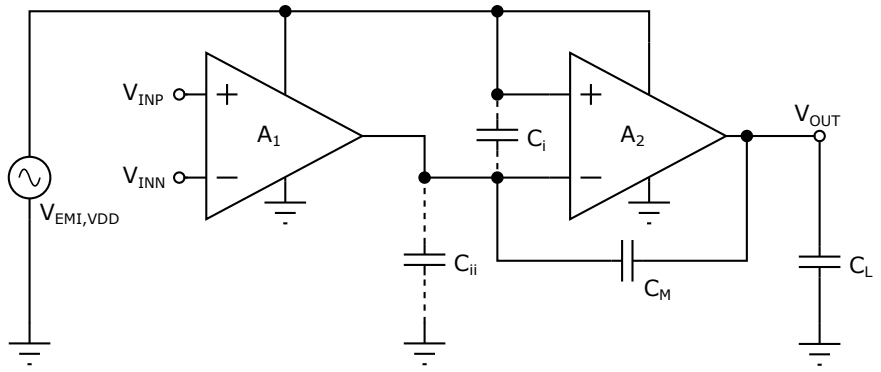


Figure 2.5: Miller amplifier at high frequencies with parasitic capacitances $C_{i,ii}$ and the Miller capacitance C_M as proposed in [5]

2.2.3 Power Supply Rejection Ratio of a Miller Amplifier

As indicated in the introduction, two-stage amplifiers are often used in modern processes. Dealing with the fact that the Miller compensation is the basic frequency compensation technique up to now, the PSRR of the Miller amplifier is considered in more detail. It is well known in the literature that the main problem of the poor PSRR performance arises from the compensation capacitor which shorts the gate and the drain of the output transistor at higher frequencies [5]–[10]. This results in a voltage follower configuration at the second stage at higher frequencies as indicated in Fig. 2.5. The voltage follower is formed by the constant biasing of the output common-source transistor, therefore its gate source voltage needs to remain constant. As V_{GS} is constant, the gate voltage of the output transistor needs to follow ripple on the power supply line and disturbances are directly coupled over the Miller capacitor to the output [7]. The transfer function $A_p(s)$ from the considered power line to the output is hereby approximately one.

Steyaert and Sansen presented in [5] a method based on curves and cuts to calculate a rough PSRR number of the basic Miller amplifier for low and high frequencies. As mentioned in [26] the latter gets too complex for greater systems and the result is inaccurate. However, the results for the basic Miller amplifier can be used to identify simple design criteria. Reference [5] gives the PSRR equations of a Miller amplifier using a p-channel MOSFET (PMOS) differential input pair with:

$$PSRR_{VDD} = \frac{g_{m1} \cdot g_{m6}}{g_{ds7} \cdot (g_{ds2}+g_{ds4}) + s \cdot g_{ds7} \cdot (C_M+C_{n1})} \tag{2.9a}$$

$$PSRR_{VSS} = \frac{g_{m1}}{\frac{2 \cdot g_{ds4} \cdot g_{ds6}}{g_{m6}} + s \cdot C_M} \tag{2.9b}$$

From the result one can see that the PSRR is directly linked to g_{m1} which needs to be increased as much as possible (transistor indexing as in Fig. 4.1). The Miller capacitance C_M needs to be as small as possible in order to shift the forming of the voltage follower

to higher frequencies. However, at very high frequencies, this capacitor shorts the gate and drain of M_6 anyway and leads to a PSRR close to zero. Mismatch in the input differential stage leads to a lower PSRR as currents do not split equally. If no mismatch is considered, the first stage is immune to EMI arising from the V_{DD} rail when a PMOS input stage is used.

At this point also a distinction between the used MOSFET configuration must be made as the PSRR is determined by the input differential pair. Using a differential pair based on PMOS gives a higher immunity against disturbances on the V_{DD} rail as the voltage follower formed by the compensation capacitor is connected towards the V_{SS} rail. Vice versa the use of n-channel MOSFET (NMOS) for the input stage leads to a higher PSRR towards the V_{SS} supply rail as the voltage follower is formed at V_{DD}.

2.3 EMI Measurement Setups

As seen in the previous sections, OpAmps suffer from different issues that make them susceptible to conducted EMI. To distinguish between EMI hardened OpAmps and susceptible OpAmps, EMI measurement setups are needed [23]. As EMI extends over various frequency up to GHz, dedicated measurement equipment is needed to ensure that the results are not influenced by the measurement itself. Especially with high-frequency measurements, effects arising from the printed circuit board (PCB) or the measurement equipment can influence EMI results. To compare different EMI countermeasures also some FOM need to be defined to investigate large differences in the susceptibility. Concerning EMI measures also the cost-benefit ratio between a reduction of EMS and factors like area, power consumption or ac influence need to be considered. Poor or incorrect EMI measurement setups can lead to sufficient immunity under test situations but faulty EMI robustness in real life application and needs therefore to be avoided under all circumstances.

2.3.1 EMI Standards

Measurement setups for electromagnetic compatibility on system level are defined in different standards such as the ISO 11452 [27] or the CISPR 25 [28]. As the effects of EMI in ICs caused by their complexity and small size are more difficult to predict than EMI on system-level, the International Electrotechnical Commission (IEC) established the specific subcommittee 47A in 1996 [29]. Working group 9 of this subcommittee released standard IEC 62132 for radio frequency (RF) immunity of ICs [30] in 2006.

In this standard several measurement methods for EMS are defined containing among other the TEM-Cell, Bulk Current Injection (BCI), Direct RF Power Injection (DPI) and the Work Bench Faraday Cage method. While the TEM and the Work Bench Faraday Cage method are included also in the IEC emission standard, BCI and DPI are purely for conducted interferences. Hereby the BCI method tries to reproduce currents that could be generated in wires of electronic systems by electromagnetic fields in the real world [23] and DPI uses direct RF injection.

2.3.2 Direct Power Injection Method

The Direct RF Power Injection (DPI) method uses direct injection of RF disturbances into the desired test pin of the device under test (DUT) through a decoupling block [31]. To block dc signals, a dc-block is realized by a capacitance with or without an additional resistor [23]. For confident measurement results a $50\,\Omega$ system from RF source to the pin under test is strongly advised to avoid unnecessary reflections. This corresponds also to the connection cables of the RF generator and the connections at the test board to bring the RF signal as close as possible to the desired test pin [32]. Though the coupler and the pin of the DUT can not meet $50\,\Omega$ regulations, reflections will be caused which need to be measured. The monitoring of the RF signal is accomplished through a directional coupler which measures the forward power of the signal and the reflected power. However, to ensure that not too much power from the unmatched input stage is reflected back to the RF amplifier and reflected again by the $50\,\Omega$ output impedance, an attenuator is inserted between coupler and injection capacitor [33]. A block diagram of the whole measurement setup is shown in Fig. 2.6. As mentioned in [23] it is not absolutely necessary the use a Faraday cage for the DPI method as the radiated electromagnetic fields of this method are rather low. As an injection signal a continuous sinusoidal wave or a sinusoidal signal with amplitude modulation can be used [23]. Hereby the injected frequency can range from dc up to 1 GHz.

Because of the easy measurement method, the basic principle of the DPI technique will be used to implement EMI TBs in following sections. As the DPI method is standardized for universal ICs measurements, a failure criterion of the DUT is difficult to define. Reference [23] suggests jitter, undesired I/O behavior or reset triggering as failure criteria for digital circuits. For analog systems, however, other criteria must be defined. As seen in the previous chapters output dc shift is a common effect for amplifier under electromagnetic disturbances and can therefore be used as a possible failure criteria for this standardized method.

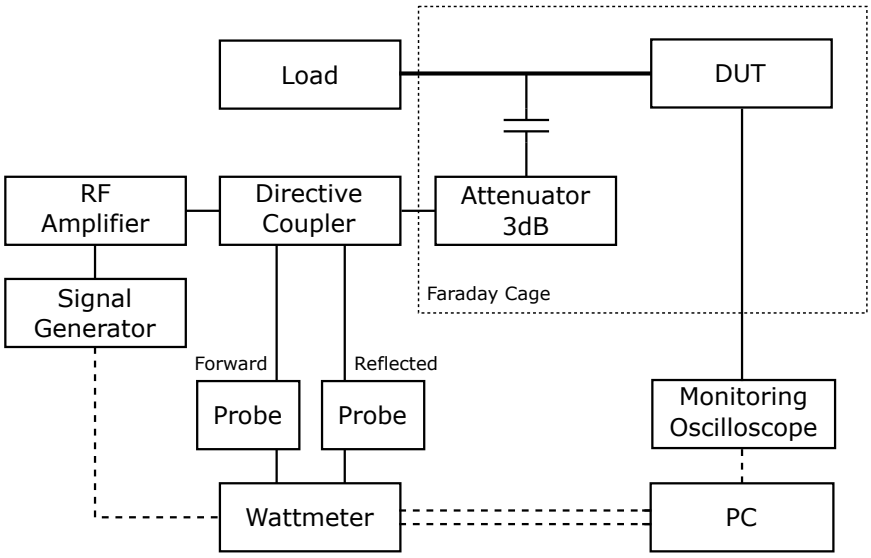


Figure 2.6: Proposed block diagram in [23] for DPI measurements

2.3.3 Amplifier Configurations for EMI Measurements

The previously considered DPI method is commonly used to inject electromagnetic disturbances into different DUTs. As in this thesis the DUT will be an analog amplifier, more details of the measurement setup need to be specified. Especially the amplifier closed-loop configuration needs significant attention as it varies the susceptibility of the OpAmp [34]. In (2.3) a maximal offset is indicated if both the common-mode and differential-mode signals are not zero and in phase. As it is desired to reproduce the worst-case offset voltage, a closed-loop configuration causing this behavior is needed for a broad range of frequencies. Redouté and Steyaert presented in [3] different configurations for different frequencies:

- Voltage follower: The unity gain buffer as closed-loop configuration is throughout the literature the most used and indicated setup method [19], [32], [34]–[37]. With the feedback from the output to the inverting input, the dc shift at the output directly occurs at the input of the amplifier. By applying resistors as for example in the non-inverting amplifier configuration, the input signal gets attenuated which is not the case for a unity gain configuration. As the inputs witness the largest voltage difference in unity gain configuration, the voltage follower is considered as the worst case configuration [34]. Redouté and Steyaert confirm this behaviour in [3] but note that this is only true above UGF. For frequencies below or close to the UGF, the differential voltage between the input is close to zero as the output follows the positive input and so the negative input does. Therefore the differential part in (2.3) is eliminated and the configuration does not represent the worst-case measurement anymore.

- Double OpAmp measurement: To solve the UGF problem of the voltage follower, Redouté and Steyaert propose in [38] a measurement method were ac and dc feedback are separated from each other. The double OpAmp measurement method uses an additional amplifier in integrator configuration to complete the dc feedback loop. This configuration allows measurements independent from the UGF down to the values of the used passive components $1/(R_1 \cdot C_1)$ [38]. A drawback of this configuration lies in the increased number of needed components for the measurement. Also stability problems can occur from the combination of two amplifiers in the feedback loop.

Which one of the two indicated methods is used for carrying out EMI tests is determined by the assumed test-frequencies. For frequencies below UGF, the double OpAmp method should be used while for higher frequencies the voltage follower configuration offers an easier solution in terms of used components. Concerning the RF disturbance signal, a sinusoidal signal can be used as stated in the DPI section. Electromagnetic disturbances often decay in time and therefore the use of such a continuous signal represents a worst-case situation [34]. Reference [33] notes that standalone simulations are different from system-level measurements where the amplifier under test is inserted in a bigger IC with other circuitries that influence the EMS. Often also electrostatic discharge protection is used which can affect the EMI measurement of the pure amplifier.

As now measurement methods and configuration are considered, further details can be taken into account. To measure the susceptible of each individual pin, it is important to ensure that only the pins under test experience injected RF signals. Otherwise other pins could influence the obtained output effect so that the measured shift is not a pure result from the pin under test any more [32]. This can be ensured with capacitors and resistors. Special care must be taken if the injection point is connected to multiple pins by circuit configuration itself. Examples for such configurations are injections into the inverting pin or the output pin when closed feedback is used. Possible solutions to isolate different pins are shown in [32]. It should be noted that for such measurements the previously mentioned setup measurements are not possible. If no shielding is used between different pins, no statement of the EMI susceptibility of each single pin can be made. However, regarding real world application these measurements are more realistic than measurements with isolated pins.

Uniting all these considerations, the used measurement setups always need to be specified to allow repeatability of the measurements. In order to simulate EMI injection special care must be taken on ideal voltage sources. Without the use of an additional resistance or impedance, injected signals are absorbed by the sources [35]. The measurement procedure itself can be adapted similarly to the measurement algorithm for DPI by changing the EMI amplitude and frequency.

2.3.4 Figures of Merit for EMI Measurements

As now the susceptibility of OpAmps in terms of output offset can be measured, some figures can be defined in order to compare different implementations on their EMI robustness. For disturbances arising from the power supply, the already mentioned power supply rejection ratio (PSRR) is available. However, for other pins no figure of merit (FOM) was defined for a long time. Therefore Texas Instruments Incorporated introduced in [32] and [39] a parameter called electromagnetic interference rejection ratio (EMIRR). This parameter links the mentioned dc output shift to the injected RF disturbance in order to quantitatively describe the EMS. By definition EMIRR is given by

$$EMIRR = 20 \cdot \log\left(\frac{V_{RFPeak}}{\Delta V_{OFF}}\right) \tag{2.10}$$

where V_{RFPeak} is the amplitude of the injected unmodulated RF disturbance and ΔV_{OFF} the resulting offset shift referred to the input of the amplifier. V_{RFPeak} is standardized to 100 mV. In order to use also other injection voltages, reference [39] offers a conversion based on a quadratic relationship where the RF interference is scaled to $100\,mV_P$:

$$EMIRR = 20 \cdot \log\left(\frac{V_{RFPeak}}{\Delta V_{OFF}}\right) + 20 \cdot \log\left(\frac{V_{RFPeak}}{100\,mV_P}\right) \tag{2.11}$$

Here V_{RFPeak} is the peak value of the injected RF signal different to $100\,mV_P$. EMIRR is given in a logarithmic scale in dB where higher values correspond to a higher immunity against EMI. As noticeable in the definition, the method is not limited to a single OpAmp pin and can be used to characterize the electromagnetic immunity of all pins. One can see that the definition of EMIRR is different from that of the PSRR in (2.6). Nevertheless both figures describe the ability of the amplifier to reject electromagnetic disturbances. Texas Instruments Incorporated describes the EMIRR measurement in [32] as following:

- Applying an RF signal to the pin under test: This can be done by the mentioned DPI method. To ensure good accordance of the measurements, the influence of the test setup itself should be kept at a minimum. Hall and Kuehl mention in [39] that the desired dc bias voltage at the input should lie at about halfway between both supply rails in order to receive a linear OpAmp behavior. Do inject dc and RF signals simultaneously, a bias tee is used where a capacitor blocks the dc signal from entering the RF generator and an inductor the RF signal from entering the bias source. As indicated in the DPI-standard, the injection capacitor should have a capacitance of 6.8 nF while the inductor should have an ac impedance of at least 400 Ω over the whole test frequency range [31]. The standard also notes that to ensure an ac impedance of 400 Ω usually multiple inductors with different values are needed.

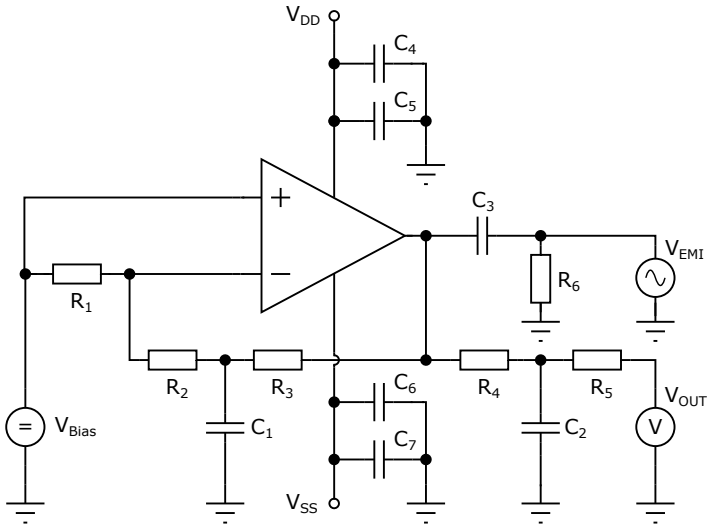


Figure 2.7: EMIRR measurement setup for the V_{OUT} pin as proposed in [32]

- Measurement of ΔV_{OFF} at the output: To measure ΔV_{OFF}, the offset voltage at the output of the amplifier needs to be measured with and without RF signals to get the resulting offset solely by the RF injection.

- Calculating input-referred offset shift and EMIRR: From the resulting output shift the input-referred offset shift can be calculated. In voltage follower configuration this is easily done as the output shift equals the input shift, for other configuration the gain factor needs to be taken into account. This corresponds especially to the measurement of $EMIRR_{VINN}$ and $EMIRR_{OUT}$ when the RF injection is isolated from other pins. If the resulting offset shift is above the noise level of the amplifier and no saturation has taken place, the EMIRR of the tested pin can be calculated with (2.10) or (2.11) depending on the injected signal.

As the output pin is one of the hardest pins to isolate, an exemplary measurement setup suggested in [32] is shown in Fig. 2.7. The often indicated voltage follower configuration is not usable for measuring $EMIRR_{Out}$ as the inverted input pin would not be isolated from the RF injection into the output. The input-referred offset shift can be calculated with the gain of the amplifier closed-loop configuration, in case of the example in Fig. 2.7 with $1 + (R_2 + R_3)/R_1$ [32]. To isolate the measured dc voltage from the RF injection a low-pass (LP) filter is used, otherwise the RF signal would be directly seen at the output.

However, as shown in [40], the characterization of the susceptibility of OpAmps against EMI with the EMIRR is not always practicable. The main drawback lies in the fact that the EMIRR scaling bases on a quadratic relationship between the RF signal and

the offset voltage shift. According to reference [40], this relationship is only accurate if the amplitude of the injected RF voltage appearing between the gate and the source of the input MOSFETs is lower than the overdrive voltage (V_{GS} - V_T). This ensures that they are not switched off periodically, otherwise the assumed quadratic relationship is not valid any longer. Simulations in Spectre using non-quadratic transistor models confirmed the change of calculated EMIRR values with different injection voltages. The usage of EMIRR is therefore restricted to a single injection voltage as the scaling within (2.10) does not work properly. Another drawback is the loss of the offset voltage sign as the logarithm requires absolute values. To solve this problem [40] proposes to measure the offset for different injection voltages at different frequencies and plot them directly without the EMIRR calculations. This however is not usable for a large number of different amplifiers as a very limited number of injection voltages can be used. Otherwise the plots would be overfilled and injection voltages usable for EMI hardened amplifiers would lead to heavy clipping of standard amplifiers as they can handle only lower injections amplitudes.

Another missing factor comes with some proposed circuits to improve the EMI robustness in the next chapter. With the mentioned PSRR and EMIRR methods the result of the improvement in terms of output or input referred offset is countable and the sources of EMS are known, but not the costs in terms of power consumption or ac modifications. These factors will be considered in the next chapter in order to define guidelines and to evaluate EMI measures.

3 Increasing the Immunity of Operational Amplifiers

As the effects of EMI entering an amplifier are now known, measures to increase the immunity need to be taken. The basic principle is to reduce the impact of the mentioned parasitics and circuit properties which increase the EMS. However, the causes of the susceptibility of an amplifier on the power supply pins are different to that of the I/O pins as the main problem lies in the frequency compensation. Therefore this section is divided into measures for I/O pins and power supply pins.

3.1 Increasing the Immunity of the Input and Output Pins

To decrease the susceptibility of the input and output pins, the known causes from Section 2.1 need to be investigated and mitigated. Reference [14] tries to group EMI measures into four groups:

- Removing EMI before it enters the amplifier
- Reducing parasitic capacitances
- Linearization of non-linear devices
- Compensation of the ac shift

As already discussed it is not possible to draw a hard boundary between EMI measures as the can decrease the EMI robustness of an amplifier in multiply ways. However, caused by the large number of different amplitudes and frequencies of electromagnetic disturbances, measures can work properly for specified situations while being less

effective for other EMI frequencies and amplitudes. This comes from the different EMI sources at different frequencies and amplitudes. Therefore it is useful to investigate the expected critical EMI frequencies before designing the amplifier in order to take dedicated measures at susceptible frequencies.

3.1.1 General Design Criteria

Dedicated circuit design can help to increase the electromagnetic immunity without the use of additional circuitry. This includes the reduction of parasitic capacitances with adapted device dimensions and the use of advanced processes with decreased parasitic capacitances [34]. Moreover, charge accumulation in the circuit can be reduced by decreasing slew rate asymmetries, which can be achieved by [1], [12]:

- Decrease CLM effects inside the bias transistor by increasing the length
- Higher bias current as slew rate is linked to I_{Bias}
- Usage of symmetric circuitries like the FC topology
- Symmetric design also in the layout

Another advisement considers the used output topology. As mentioned in [3], the resulting dc offset shift of a common-source (CS) stage is about two orders of magnitude lower than the shift of a common-drain (CD) structure when EMI is injected into the output note. Redouté and Steyaert explain this with the variation of the gate-source voltage of the CD stage when the output/source is disturbed with RF signals. As the drain current is linked to the gate-source voltage, the average drain current flowing in the output stage is unequal to the original state. The matter is different in the case of CS stages where the EMI injection into the output is not disturbing the gate-source voltage directly. Moreover, only capacitive coupling to the gate over the parasitic drain-gate capacitance C_{DG} occurs. This capacitance forms a voltage divider with the gate-source capacitance C_{GS}. However, as mentioned in [3], C_{DG} is typically smaller than C_{GS}. By using larger transistor lengths and smaller widths the spread between both capacitances can be increased further. Therefore a CS stage remains longer linear than a CD stage which can clip at higher EMI amplitudes more easily [3].

However, as mentioned in [17], [23], [35], the main focus should lie on the input stage as the output is fed back to the input. Therefore EMI injected into the output is also visible at the input, especially for voltage follower configurations. Reference [23] indicates that

mostly the input differential stage needs EMI improvements as disturbances injected into this stage are strongly amplified in the proceeding stages. This corresponds also to the previously recognized problems in Section 2.1 where the dc shift only gets accumulated at the output and not generated. Clearly the mentioned effects of the output CD or CS stage influence the susceptibility but as indicated in the papers, the main focus should lie on the input stage, especially the differential pairs.

3.1.2 Input Filter

Unfortunately, the input stage is the most difficult to protect. Once RF signals are distorted at the non-linear nodes, they cannot be distinguished from the desired signals anymore [3]. Therefore the most straight forward solution is to filter RF signals before they can reach the input pair. This is usually done with low-pass (LP) filters. Filtering works quite well for the power supply [41] but is not so straightforward for the input pair as it may seem at first look. Filters at the input affect the bandwidth and stability of the amplifier [12]. To avoid this drawback, the additional pole formed by the RC LP has to be pushed beyond the dominant pole of the amplifier to about 10 times of the gain-bandwidth product (GBW) [14]. As resistors introduce thermal noise at the input, the corresponding values should be as small as possible which implicates larger capacitor values. However, larger capacitors implicate also more area required by the amplifier.

To overcome the GBW and stability problems, reference [42] suggests the use of a replica input differential stage for the RC LP. A sample circuit of the idea from Richelli is shown in Fig. 3.1 where M_1 and M_2 form the effective differential stage with the corresponding active load and bias transistors. M_{1Rep} and M_{2Rep} form the replica input pair which is to a large degree immune to high-frequency EMI and matched to the effective input pair. As indicated in [42], the whole circuit exhibits an increased immunity against EMI with less modification to the GBW and the phase margin (PM) than a directly connected RC LP filter. For both indicated measures the EMI frequencies of interest must be known beforehand in order to design the RC LP to be effective in the desired frequency region.

3.1.3 Parasitic Capacitances

If it is not possible to prevent the RF disturbance from reaching the differential pair, the effects of the parasitic capacitances can be taken into account. The transfer function H_{CM} from the input common-mode signal to the common-source node of the differential

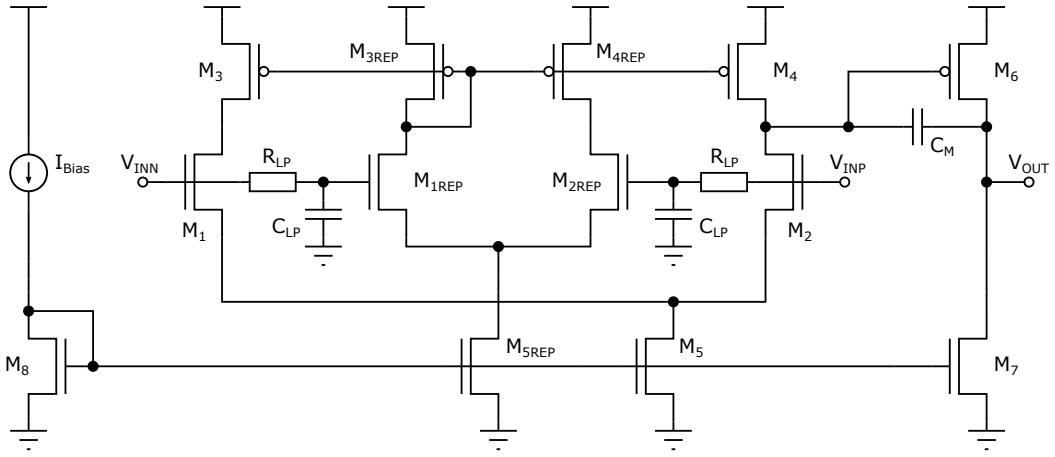


Figure 3.1: OpAmp with replica input stage and RC LP filter proposed in [42]

pair is given in (2.5) and by decreasing H_{CM} the output offset can be reduced [43]. This can be done by decreasing the parasitic tail capacitance C_{Tail} and increasing C_{GS}. Note that this also can be obtained from the equations for the gate-source voltage (2.1) and (2.2) where C_{Tail} needs to be decreased and C_{GS} increased in order to equalize both gate-source voltages of the input pair. Especially the reduction of the parasitic capacitance C_{Tail} is crucial as it shorts the bias transistor at higher frequencies as discussed in Section 2.1.3.

To decrease C_{Tail}, an additional well for the input transistors must be avoided as this forms the main contributor to C_{Tail}. This can be done by connecting the bulk pins to V_{DD} or V_{SS} for PMOS or NMOS transistors. A drawback of the method is a shift of the threshold voltage V_T caused by the body effect. To avoid this, a replica stage as presented in Fig. 3.2 can be used where the bulk connections of the nominal input differential pair are biased by a replica differential pair to reduce the body effect [22]. Doing so C_{Tail} is reduced and the susceptibility of the amplifier against high-frequency EMI is decreased. However, to ensure correct biasing, the parasitics of both input pairs need to be matched which is not easy to accomplish [33].

Another way to reduce H_{CM} and to equalize the gate-source voltages of the input pair is to increase the parasitic gate-source capacitances C_{GS}. Doing so the capacitive voltage divider between C_{Tail} and C_{GS} is minimized at higher frequencies. Equations (2.1) and (2.2) indicate that an optimal value for the added capacitance should exist. References [1] and [44] derive this, whereby [44] indicates that the additional external capacitance $C_{GS,INP}$ is dependent on frequency and $C_{GS,INN}$. This implies that for a dedicated value of $C_{GS,INN}$, an almost frequency independent $C_{GS,INP}$ can be found which is realizable by an integrated capacitor as shown in [44]. Moreover, reference [1] denotes that thanks to the small value of the added capacitors, the frequency behavior of the amplifier is nearly unchanged. To reduce H_{CM} further, the increased gate-source capacitances can

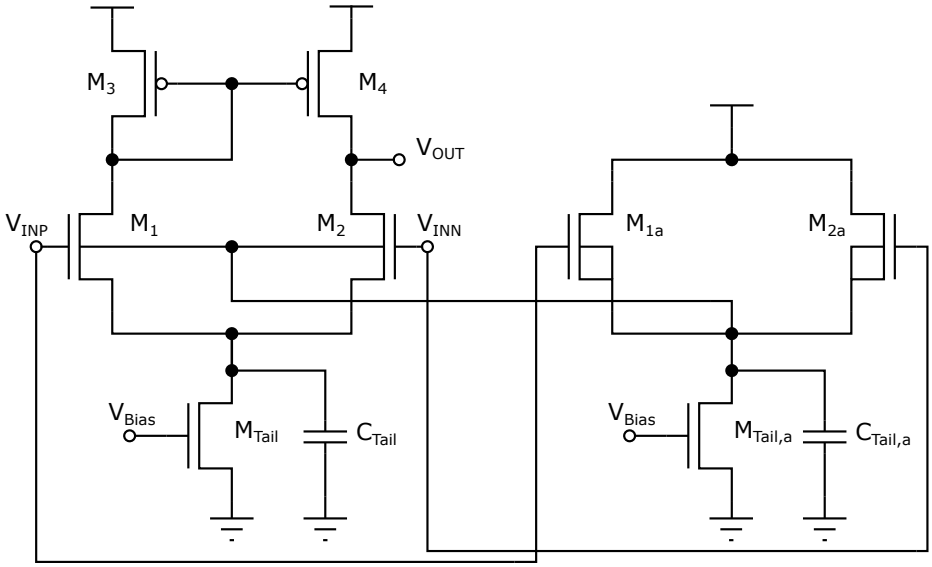


Figure 3.2: Source buffered input stage

be combined with a source buffered stage which gives a high immunity against EMI at higher frequencies.

With the increase of the gate-source capacitances also a new approach for LP filtering is available. As presented in [13], a small resistor connected to the gate of the input differential pair can be used. The resistor forms together with the increased gate-source capacitances C_{GS} a LP that filters EMI.

3.1.4 Linearization

Another measure to reduce EMS of an amplifier is to reduce distortion inside the input transistors. A simple method is introduced in [13] where source degeneration is used to form an internal feedback loop and to improve the linearity of the stages. With the insertion of simple source resistances in the input stage, the immunity against EMI can be increased as shown by Corradin et al. He mentions also the drawbacks of source degeneration as I_{Bias} needs to be increased to compensate for the reduced gm. Also mismatch plays a role as the resistors can increase input offset in absence of EMI. Redouté and Steyaert derive the increased robustness against EMI in [3] mathematically, however, they mention also the increased input equivalent noise as the degeneration resistors are present in the signal path. Moreover [14] mentions that source degeneration resistors are shorted by the parasitic tail capacitance C_{Tail} at higher frequencies and will not increase the robustness against EMI anymore.

Other possibilities to increase the linearity of the input transistors consist in using transistors in triode region [14] or bulk driven input pairs [12]. However, both variants suffer from mature drawbacks and are therefore not considered further.

3.1.5 Cancellation

If none of the previously mentioned measures can be used or if the measures are insufficient, a cancellation scheme can be applied. This can be done by directing the RF disturbances to a node with a contrary effect on the dc shift [14]:

- Common-Mode Cancellation Circuit: As observable in equation (2.3), the reduction of the common-mode transfer function H_{CM} is a possible way to reduce the EMI introduced offset. In [45] an on-chip common-mode cancellation circuit (CMCC) has been presented which increases the CMRR and hence the robustness against EMI as it removes the common-mode part. The latter consists of a cross-connection of two inverters with dedicated resistors. By designing the resistors according to the equations given in [45], the common-mode gain can be decreased and the differential gain increased. The CMCC in Fig. 3.3 works the following: Rising common-mode signals at the inputs are applied as decreased potential to both R_1 resistors. Due to the voltage divider formed by R_1 and R_2, the potential at the gate of the input transistors ideally should stay constant. Differential signals, however, are amplified as the potential at both resistors R_1 and R_2 changes in the same direction and the gate of the transistors changes accordingly. Richelli and Redouté indicated improved robustness against EMI also under the presence of mismatch. Reference [4] improves the circuit for disturbances with higher amplitudes by decreasing the inverter slope with current starved transistors. While the latter works for low to medium EMI frequencies, the EMI robustness at high frequencies is improved too as the inserted resistors form a LP together with the parasitic capacitances of the input stage. In order to ensure that the CMCC does not influence the frequency performance, it must be ensured that the introduced pole lies above GBW. Drawbacks of the circuit are the increased area and the elevated input noise generated by the resistors. Also power consumption is increased by the inverters.

- Cross Coupled Differential Pairs: Another cancellation scheme was presented in [36] which consists of two cross-coupled differential input stages separated by an RC high-pass. Both input stages are considered as perfectly matched. Below GBW the additional input pair does not introduce any signals as the input is decoupled by means of the high-pass. At higher EMI frequencies the second pair becomes active and generates an output current shift like the primary input

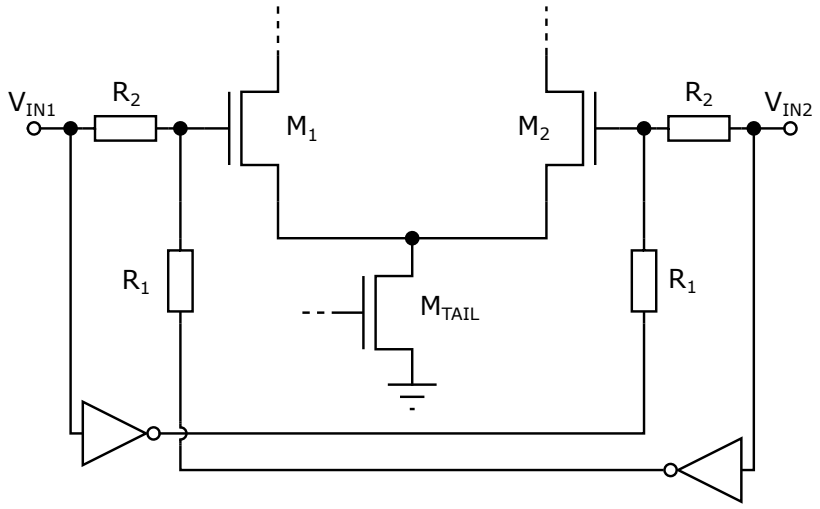


Figure 3.3: Common-mode cancellation circuit proposed in [45]

pair. By cross-coupling the outputs the offset currents sum up do zero under the assumption of perfect matching. However, as indicated in [3], the latter includes some huge drawbacks: The input noise is increased by the additional input pair and the inserted resistors as well as the area. Moreover perfect matching of the input devices and the current sources is important, the power consumption is increased and an additional voltage reference is needed to biases the gate of the secondary differential pair in the middle of the input common-mode range. This however does not work well for changing dc voltages at the primary input pairs. An improvement of the circuit has been presented in [20], [43] which uses different sizing of the input transistors stages instead of a passive high pass. Fiori derives in the mentioned papers formulas for the design of such an improved differential pair with cross-coupling. However, this method strongly depends on perfect matching and increases the noise of the input stage too [3].

Summarizing the EMI countermeasures it can be mentioned that input filters increase the immunity of amplifiers against EMI at frequencies above the GBW as they prevent disturbances from entering the amplifier. This however does not work for lower and middle frequencies close to GBW. Solutions based on minimizing slew rate offsets work well for lower frequencies as they minimize the charge accumulation, while at higher frequencies other measures must be taken. A good compromise lies in the reduction of the parasitic tail capacitance C_{Tail} and the insertion of additional gate-source capacitances C_{GS} which form a LP with the parasitic line resistances. Cancellation and feedback rely on good matching and increases circuitry area, especially for more complex structures. Concluding the most important factor lies in knowing the expected EMI frequencies beforehand. This gives the opportunity to choose the correct EMI measure. It is also beneficial when the desired UGF does not coincide with critical EMI frequencies as this increases the number of possible EMI measures.

3.2 Increasing the Immunity of the Power Supply Pins

As already mentioned, the main PSRR reduction of a two-stage amplifier is caused by the used frequency compensation method. The PSRR is mainly determined by configuration and only little improvement is possible in design [7]. Therefore improved frequency compensation methods are considered in the next section on their own. Small improvements by design however still can be made:

- Decreasing compensation and parasitic capacitances
- Increasing G_m and R_{Out} of both stages in order to increase A(s) and GBW
- PMOS input structure for EMI problems arising from the V_{DD} supply rail and NMOS input structures for problems arising from the V_{SS} supply rail.
- Using folded-cascode (FC) topologies
- Applying supply rail filter
- Power supply independent biasing circuits

Most of this guidelines can directly be derived from (2.9). As suggested in [1], [7], [46], the usage of a symmetric single-stage FC topology instead of a two-stage topology increases the PSRR. Moreover the symmetric structure of the FC increases the immunity against EMI on the I/O pins too as slew rate asymmetries are minimized.

In contrast to the input pins it is relative easy to insert filters for the power supply pins. This is emphasized in [3], [41], where the usage of an external or internal RC LP for the power supply grid increases the robustness against high-frequency ripples. However, it is not always possible to implement internal decoupling capacitors in the range of a few hundred pF or nF caused by their required area. Therefore this approach is not assumed any further. Admittedly it has to be mentioned that it is a general intend to insert decouple capacitances wherever it is possible what helps to filter out EMI disturbances before they reach the amplifier.

Regarding biasing, [7] suggests using current sources that are independent from power supply changes. This is especially crucial for the second stage as the fluctuating bias current is multiplied by the resistance of the bias transistor and appears as voltage ripple at the output of the amplifier [7]. To prevent this it must be ensured that the

gate-source voltages of the bias transistors stay at the same level while the power supply changes. This can be accomplished by referring all bias voltages and currents of PMOS transistors towards V_{DD} and all bias voltages and currents of NMOS transistors towards V_{SS}.

3.2.1 Single Ended and Fully Differential Topologies

An effective way to deal with disturbances arising from the power supply lies in the use of fully differential (FD) amplifier topologies. Thanks to the use of differential signals, fluctuating common-mode signals and noise are suppressed as both outputs experience the same common-mode shift what results in zero differential shift. Especially in noisy environments as in mixed-signal circuits the use of FD topologies is highly considered [24]. This is also discussed in Section 2.2.2 where an additional input like the reference voltage for the CMFB circuit increases parasitic rejection ratios as CMRR and PSRR. As indicated in [6], [37] even the use of a SE version of the FD topology increases the robustness of an amplifier against EMI. The immunity against EMI can even be more improved with the use of a cross-coupled output buffer [37] which ensures a symmetric slew rate which is important to minimize charge accumulation at lower and medium frequencies. Another advantage of the FD topology is the increased signal swing which rises by a factor of two in comparison to single-ended (SE) signals. This gives an advantage in low voltage power supply circuits [7].

However, the improvement in terms of noise and voltage swing comes not for free. FD two-stage circuits increase the power consumption as two output circuits need to be driven and an additional CMFB circuit is required. This CMFB circuit is needed to define a common-mode voltage at the output. Also perfect noise-canceling due to the differential output voltages is only ensured under the absence of mismatch. Hereby a symmetric layout and symmetric surrounding characteristics are important [24].

3.2.2 Current Injection

A relative easy way to achieve a higher PSRR is presented in [6]. In Section 2.2.2 the assumption of all parasitic gains summed up to one was presented. With the introduction of an additional noise-free input pin, other parasitic gains are reduced. This is carried out by Saeckinger et al. with the use of a capacitor C_{Inj} connected between the current mirror of the active load and a noise-free potential. This capacitor injects a compensation current into the current mirror which corrects the current fluctuations of the compensation capacitor of the second stage [6].

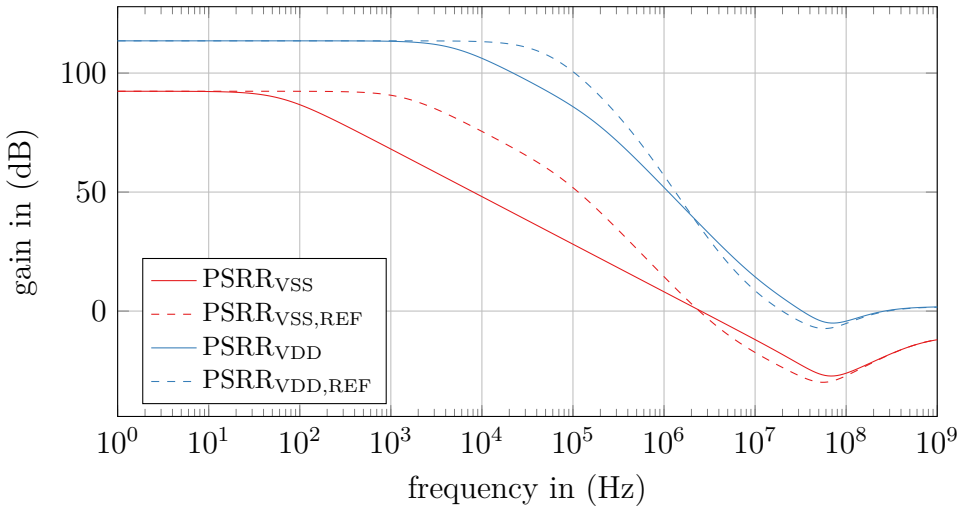


Figure 3.4: PSRR simulation of a Current Injection amplifier with an additional noise-free V_{REF} path.

By choosing $C_{Inj} = C_{Miller}$, Saeckinger et al. claim a reduction of the parasitic power supply gain without influences on the frequency performance or common-mode range of the amplifier. Simulations confirmed this behavior with a slight decline of the achieved UGF and PM as the newly introduced capacitance contributes to the mirror-pole. However, the improvement in terms of lower parasitic gains is significant. This method was also used to insert an additional V_{Ref} path in Fig. 2.4. One clearly can see the attenuation of the parasitic gains from both power supplies as A_{Ref} equals one over a wide range of frequencies. The improved PSRR figure is plotted in Fig. 3.4. Especially for $PSRR_{VSS}$ a great improvement of more than 20 dB is obtainable from around 500 Hz to 200 kHz.

To ensure reasonable results, the potential of the additional path needs to be noise-free. This needs to be considered as a simple connection of the injection capacitor to V_{DD} or V_{SS} is not noise-free. Connecting the injection capacitor to V_{SS} increases the PSRR from the V_{DD} rail but worsens the PSRR from the V_{SS} rail as an additional path for disturbances is formed. However, if V_{SS} is assumed to be more immune to EMI then V_{DD}, current injection represents a method to shift immunity between V_{DD} and V_{SS} by scaling the injection capacitor C_{Inj}. This is also confirmed by EMI simulations of a Miller amplifier with PMOS input transistors where an increase of the robustness on the V_{OUT} and V_{SS} pins was visible if C_{Inj} is chosen equal to the Miller capacitance. On the V_{DD} pin no improvement was visible while the robustness on the V_{INP} pin was slightly decreased, perhaps by the reduced ac performance.

3.3 Frequency Compensation Methods

Two-stage amplifiers are often used in modern mixed-signal design because they offer high gain. However, both gain stages introduce a pole which leads to significantly reduced PM and instability. Therefore frequency compensation is needed which often is carried out by Miller compensation. This gives an easy and efficient way to ensure stability but influences the PSRR seriously and leads to weak robustness against EMI. Therefore other, more robust compensation techniques are needed as frequency compensation is the main contributor for weak PSRR performance.

3.3.1 Miller Compensation

Without frequency compensation, the dominant poles of a two-stage amplifier are given by the respective output impedances. This impedances are often close together and reduce the PM:

$$p_1 \approx -\frac{1}{R_{n1} \cdot C_{n1}} \tag{3.1}$$

$$p_2 \approx -\frac{1}{R_{n2} \cdot C_{n2}} \tag{3.2}$$

In order to ensure stability, the poles needs to be separated. Doing so gain drops much earlier and a sufficient PM is present. To shift the dominant pole to lower frequencies, a large capacitor would be needed if the capacitance is directly connected to the output of the first stage [47]. To avoid the use of such large capacitances, the Miller effect can be used where a capacitance C coupled across a gain stage is seen as much larger capacitance C_1 at the input:

$$\frac{1}{sC_1} = \frac{\frac{1}{sC}}{1 - A_V} = \frac{1}{(1 - A_V) \cdot sC} \tag{3.3}$$

Thanks to this Miller multiplication the shift can be ensured with much smaller values. This leads also to the name of the Miller compensation [47]. The newly composed poles are approximately given in [10] with

$$p_1 \approx -\frac{1}{(1 + G_{m2} \cdot R_{n2}) \cdot C_M \cdot R_{n1}} \tag{3.4}$$

$$p_2 \approx -\frac{G_{m2} \cdot C_M}{C_{n1} \cdot C_{n2} + C_{n1} \cdot C_M + C_{n2} \cdot C_M} \tag{3.5}$$

where R_{n1} and C_{n1} indicate the output resistance respectively capacitance of the first stage, R_{n2} and C_{n2} the output resistance and capacitances of the second stage including

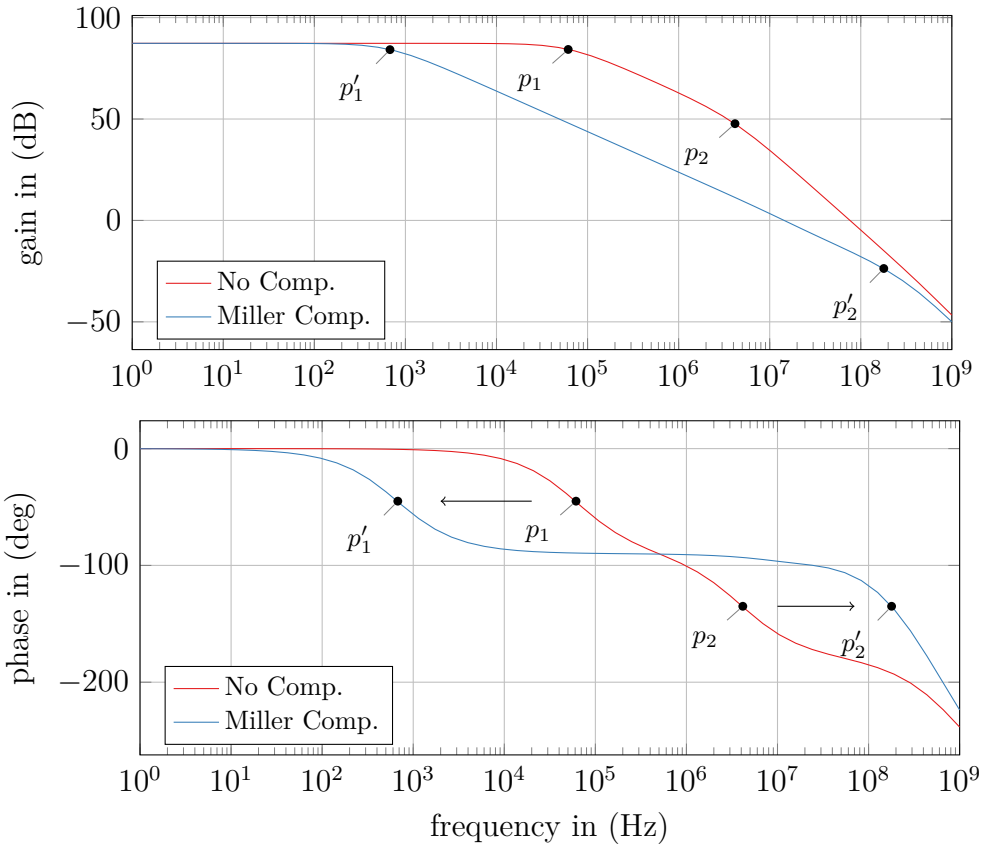


Figure 3.5: Simulation of the pole splitting effect using Miller compensation. With the increased capacitive load pole p_1 is shifted towards the origin and pole p_2 towards higher frequencies ensuring stability.

the load capacitance, G_{m2} the transconductance of the second stage and C_M the Miller compensation capacitance. The dominant pole p_1 is shifted towards lower frequencies and p_2 is shifted towards higher frequencies. Therefore this compensation technique often is also called pole splitting as it pushes the poles apart [10]. The effect can also be seen in the simulation of a basic two-stage amplifier in Fig. 3.5 where both poles are pushed away from each other ensuring a sufficient PM which is not the case without Miller compensation.

Unfortunately, this concept is not without drawbacks. One downside lies in stability issues when load capacitances in the same order of magnitude as the compensation capacitance are used [48]. The more harmful drawback lies in the newly introduced low impedance feedforward path across the second gain stage by the compensation capacitor at higher frequencies. Due to the fact that the path over the compensation capacitance is a short at high frequencies, no signal-inverting takes place. This happens in conflict to the path over the second gain stage where the signal gets inverted.

As the polarity of both signal paths is opposite, a right half-plane (RHP) zero located at

$$z \approx +\frac{G_{m2}}{C_M} \tag{3.6}$$

is produced [10]. This zero increases the gain while it decreases the phase shift leading to decreased PM [7]. A simple approach to eliminate this RHP zero is the insertion of a nulling resistor R_N in series to the Miller capacitor C_M. Doing so the zero is given by [24]

$$z \approx \frac{1}{C_M \cdot (\frac{1}{g_{m2}} - R_N)} \tag{3.7}$$

where G_{m2} represents the transconductance of the gain transistor of the second stage. As Sansen notes the zero is pushed towards infinity for $R_N = 1/G_{m2}$ and is even inserted in the left half-plane for higher values of R_N. Razavi [47] notes that a pole-zero compensation can be realized by choosing R_N equal to:

$$R_N \approx \frac{C_L + C_M}{G_{m2} \cdot C_M} \tag{3.8}$$

As this relies on the difficult matching of a resistor with the transconductance of a transistor, a different approach uses the resistance of a transistor in linear region which ensures better matching and less consumed area [24]. To encounter process and temperature variations, [47] propose the usage of transistors in diode configuration to bias the linear nulling transistor. This method only relies on the ratio of the used quantities and except C_L on no absolute values, matching is therefore much easier to accomplish. However, even if matching between transistors is much more precisely, the value of the load capacitance must be known and fixed, otherwise exact compensation is not possible.

3.3.2 Voltage Buffer Compensation

One way to eliminate the feedforward path lies in the use of voltage buffers. As described in [47], [49], a simple source follower can be used in series to the compensation capacitance. The gain of a source follower stage is approximately equal to one and a feedback path from the amplifier output over the source follower and the compensation capacitor C_C to the output of the first stage can be established. With the avoided feedforward path, the RHP zero is shifted to high frequencies [47]. As derived in [49], a left half-plane (LHP) zero is established which can be used to compensate a pole by setting $g_{m,SF}$ of the source-follower transistor equal to G_{m2} of the output stage times the ratio from C_C to C_L:

$$g_{m,SF} = G_{m2} \cdot \frac{C_C}{C_L} \tag{3.9}$$

With pole-zero compensation, the original third pole becomes the new non-dominant pole which does not depend on the load capacitance anymore [49]. However, to ensure

pole-zero compensation the load capacitance needs to be fixed to achieve a stable C_C to C_L ratio.

The main drawback of the voltage buffer compensation lies in the reduced output swing. The source follower limits the minimal output voltage to V_{GS} of the source follower plus the voltage across the additional bias source to supply the source follower [47]. Caused by the additional bias source power consumption increases and limits the usage of the voltage buffer compensation.

3.3.3 Current Buffer Compensation

To overcome the drawback of the reduced output voltage swing, another approach uses current buffer to eliminate the feedforward path. With the usage of a common gate stage, the feedforward path is avoided. However, the current from the second stage can flow into the output of the first stage but not in the other direction through the compensation capacitor C_C [50]. In the literature various versions of this concept exist:

- Additional Stage: Also described as "grounded gate cascode compensation" [10] or "Ahuja-stage" [48], an additional stage between the first and second gain stages is used to isolate C_C from the first stage potential while preserving feedback. This is achieved by connecting C_C to the source of the common-gate transistor M_{CB} as visible in Fig. 3.6. Due to the grounded gate connection, virtual or ac ground is provided for the compensation capacitor and a current gain from the output of the second stage to the output of the first stage equal to one is ensured [10], [48], [50], [51]. By matching both bias sources M_{B1} and M_{B2}, all the current from the output of the second stage is directly guided to the output of the first stage providing the needed feedback for pole splitting [48]. Caused by the avoided direct diode-connection from gate to drain of the second stage output transistor, the overall PSRR is increased [48], [51].

  Mathematically the prevented feedforward path is expressed by the elimination of the RHP zero if an ideal current buffer with an input impedance equal to zero and an output impedance equal to infinity is assumed [48], [50]. Considering a non-ideal current buffer, a LHP zero located at

$$z \approx -\frac{g_{m,CB}}{C_C} \tag{3.10}$$

  is introduced, where $g_{m,CB}$ corresponds to the transconductance of the current buffer transistor [52]. Concerning poles, the dominant real pole correspondents to the dominant pole of a basic Miller compensation while p_2 and p_3 can not

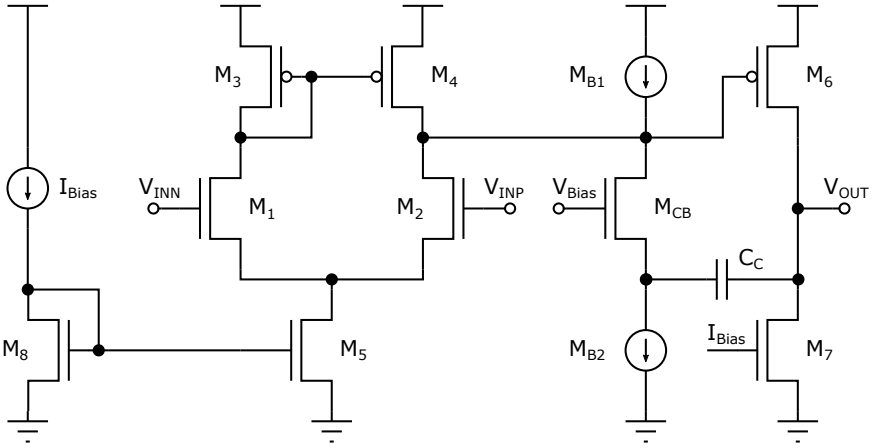


Figure 3.6: Frequency compensation using an additional current buffer stage

be expressed as simple general expressions as the can be real or complex conjugates [50]. However, the assumption of an ideal current buffer in [48] indicates p_3 at infinity. Assuming large values for transconductance gm_{CB}, p_2 can be found by approximately:

$$p_2 \approx -\frac{G_{m2} \cdot C_C}{(C_L + C_C) \cdot C_{n1}} \tag{3.11}$$

where G_{m2} correspondents to the transconductance of the second stage output transistor and C_{n1} to the sum of the parasitic capacitances at the output of the first stage [50]. Comparing (3.11) to the non-dominant pole of the standard Miller compensation in (3.5), a shift to higher frequencies is recognizable.

A drawback of the current buffer approach lies in the increased noise and current consumption due to the additional circuitry and an increased amplifier offset determined by the matching of both current sources M_{B1} and M_{B2} [50]. The increased current consumption indeed can not be improved by limiting the cross current through the additional stage as this current limits the slew rate. For equal positive and negative slew rate, the current from the additional current sources M_{B1} and M_{B2} needs to be the same or bigger as the current through the input tail current source [47]. Furthermore [52] notes that, depending on the PM of the internal feedback loop, peaking behavior in the transfer function can occur when the PM of the internal current buffer loop is designed too small.

- Embedded Stage: To overcome the increased current consumption, the common-gate stage can also be embedded into the first stage by cascoding the active loads of the first stage and connecting C_C to the source of the cascode devices [50]. Doing so three poles and one LHP zero are produced as in the additional stage variant, but with no additional current consumption. Furthermore, the output resistance of the first stage is increased which directly increases the gain too.

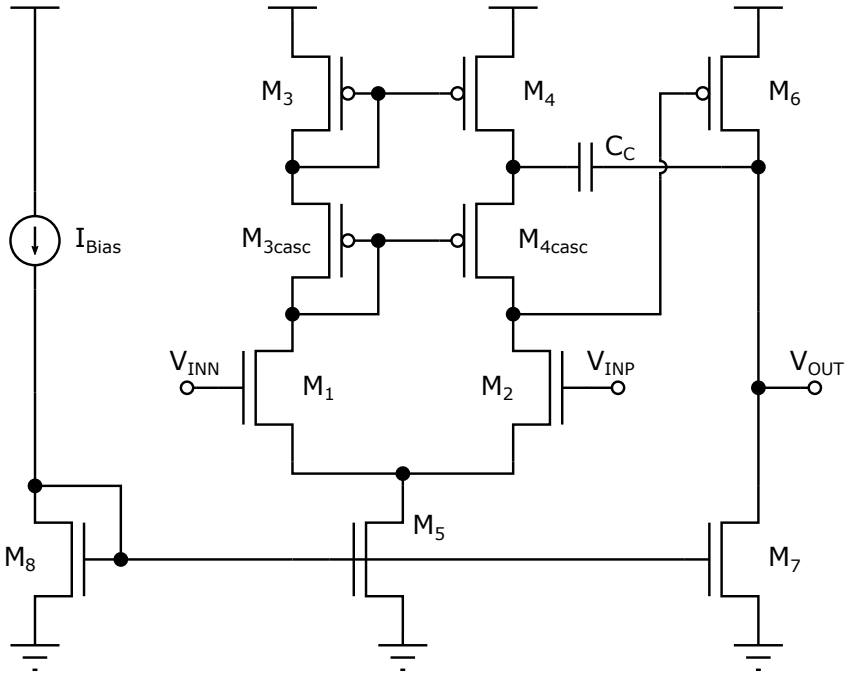


Figure 3.7: Frequency compensation using an embedded current buffer stage by cascoding the active loads transistors.

The design of the transconductance of the common-gate transistor however is much less flexible than in the variant with the additional stage [50] and the input common-mode range is limited by the bias voltage of the cascode devices.

Cascoding is also possible for the differential pair. By using a cascoded differential pair, a new connection point for the compensation capacitor is available at the sources of the cascode devices. Doing so the RHP zero is not eliminated as noted in [50], but the feedforward path is decreased and the magnitude of the RHP zero is increased compared to the standard Miller approach. Furthermore a LHP zero is introduced lying at approximately the same magnitude as the RHP zero. The zero can be calculated with the transconductance of the second stage G_{m2} and the transconductance of the cascode transistors $g_{m,Casc}$ [50]:

$$z_{1,2} \approx \pm\sqrt{\frac{G_{m2} \cdot g_{m,Casc}}{C_{n1} \cdot C_C}} \tag{3.12}$$

- Current Mirrors: Another concept lies in the use of current mirrors to buffer the feedback path. By choosing a current mirror gain of $m = 1$, the latter is functionally equal to the variant with the additional stage [50]. However, by choosing a current mirror gain $m > 1$, the feedback of the current from the second to the first stage is increased by factor m. Therefore the compensation

capacitor C_C can be decreased by m to receive the same frequency behavior as before. This leads do a decreased circuit area as the compensation capacitor can be much smaller. On the downside, an increased current consumption and lower output resistance of the current mirrors compared to the common-gate stage is visible [50]. Moreover noise and parasitic capacitances are increased, the common-mode loop may suffer from problems as C_C does not affect the common loop in the same way as the differential loop and the connections of the current mirrors need to be crossed over in order to receive negative feedback [50].

3.3.4 Feedforward Compensation

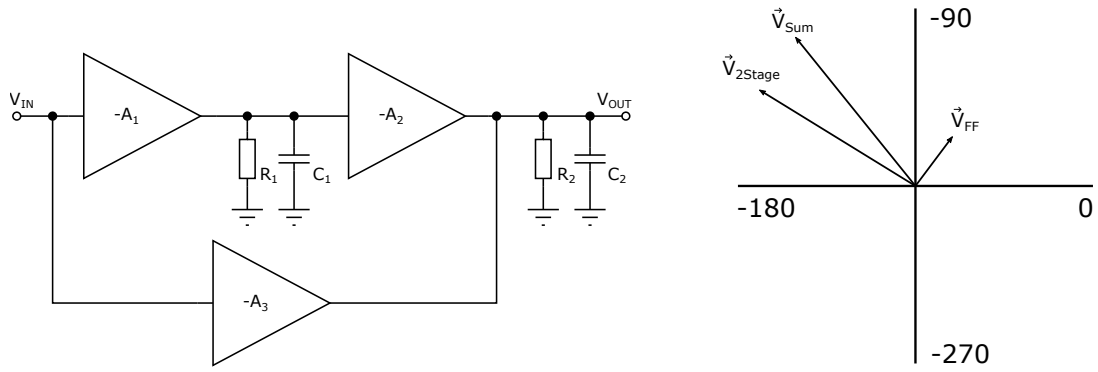
All the previously mentioned methods rely on the use of a compensation capacitor as main element to split the dominant and non-dominant poles of the amplifier. These methods are quite easy to implement, however, other topologies exist which do not shift the dominant pole to lower frequencies. A in the literature less known compensation method avoids the shift of the dominant pole by adding a parallel feedforward gain stage to the two-stage amplifier.

The main idea is presented in Fig. 3.8a [53], [54]: A two-stage amplifier with two gain stages A_1 and A_2 provides good low-frequency performance with high gain. Parallel to the two-stage amplifier a single-stage amplifier with gain stage A_3 is used with low gain but improved high-frequency performance. Therefore the second amplifier processes signals at higher frequencies where the first two-stage amplifier is not capable to provide enough gain. Reference [11] explains the improved phase performance with the use of vectors where the signal of the feedforward stage $\vec{V}_{FF}$ is added with little phase shift to the amplified signal of the uncompensated two-stage amplifier $\vec{V}_{2Stage}$. The resulting vector $\vec{V}_{Sum}$ has a magnitude similar to the uncompensated vector $\vec{V}_{2Stage}$ of the two-stage amplifier but with better phase behavior as visible in Fig. 3.8b. Therefore good frequency behavior up to high frequencies is guaranteed without the use of frequency compensation capacitors.

The basic principle for no-capacitor feedforward (NCFF) compensation was introduced by Thandri and Silva-Martinez in [55] where the latter is investigated analytically. The dc gain is given with $(A_{V1} \cdot A_{V2} + A_{V3})$ and the overall voltage gain with:

$$H(s) = -\frac{\left(A_{V1} \cdot A_{V2} + A_{V3}\right)\left(1 + \frac{A_{V3} \cdot s}{(A_{V1} \cdot A_{V2} + A_{V3}) \cdot \omega_{P1}}\right)}{\left(1 + \frac{s}{\omega_{P1}}\right) \cdot \left(1 + \frac{s}{\omega_{P2}}\right)} \tag{3.13}$$

The pole of the first stage is given by $p_1 = G_{m1}/C_{n1}$ and the pole of the second and third stage by a common $p_2 = G_{m2}/C_{n2}$ [55]. As one can see the overall transfer function has



(a) Block diagram (b) Phase diagram

Figure 3.8: Block and phase-diagram for feedforward compensation

two poles and a LHP zero created by the fast feedforward path through gain stage G_{m3}. This zero is used to compensate the second pole by introducing a positive phase shift and is located at [55]:

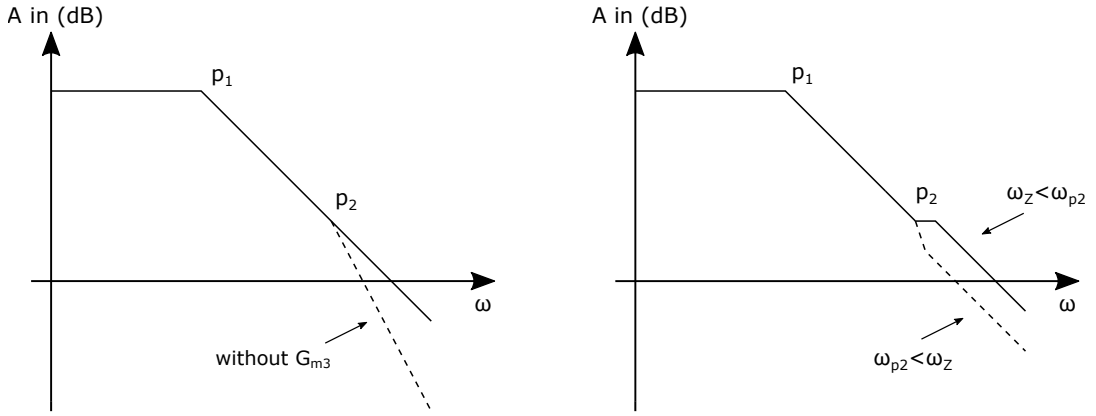
$$z_1 = -p_1 \cdot \left(1 + \frac{A_{V1} \cdot A_{V2}}{A_{V3}}\right) \approx -\frac{G_{m1}}{C_{n1}} \cdot \frac{G_{m2}}{G_{m3}} \tag{3.14}$$

As Thandri and Silva-Martinez indicate, this zero lies at about G_{m2} /G_{m3} times the GBW of the first stage. If the zero lies at exactly the same magnitude as the non-dominant pole, the pole is compensated. This results in a PM equal to 90° and an overall GBW equal to A_{V2}· G_{m1}/C_{n1} [55]. Compared to the Miller amplifier an improvement is achieved as the poles are not split and the dominant pole is not slowed down [56]. As no compensation capacitor is used this technique also should offer a high PSRR.

Considering all these positive aspects regarding NCFF compensation, why is this method not used more often? Several works in the literature point out that a pole-zero doublet in the transfer functions generally ruins the settling behavior [24], [53], [55]–[57]. As such a doublet is present in a NCFF compensated amplifier, some additional considerations must be taken. Reference [55] notes that especially low-frequency doublets degrade the settling performance. Therefore pole-zero cancellation in NCFF compensated amplifier should take place at high frequencies in order to not affect the settling time. Reference [53] differentiates two situations:

- A parasitic pole and a zero are placed between the dominant pole and the origin: In this configuration the settling time is determined by the location of the pole-zero pair and the gap between them.

- A pole is the first root close to the origin: In this configuration the settling time is determined by the dominant pole or pole pair if no zero is located near them.



(a) Feedforward stage (b) Pole-zero mismatch

Figure 3.9: Gain of a NCFF amplifier under the assumption of pole-zero mismatch

Summarizing this aspects, pole-zero cancellation should not occur before the dominant pole. However, considering component tolerances, perfect pole-zero cancellation never will occur. Depending on the constellation of the pole-zero doublet, a positive or negative gain step will be visible in Bode plots [53]. If the zero is placed slightly before the corresponding pole, a horizontal gain step is present. If the zero is placed above the pole, the gain will fall with $-40\,\mathrm{dB}$ as demonstrated in Fig. 3.9. However, as [55] emphasizes, mismatch between the pole-zero double does not affect the amplifier low and medium frequency performance when the doublet is placed at high frequencies. Summing up these considerations, three general design rules need to be considered when designing NCFF compensated amplifier [55]:

- High gain for the overall amplifier
- Pole-zero cancellation at high frequencies

Reference [11] points out that caused by those constraints the feedforward technique is not usable for high capacitive loads as this would lower the non-dominant poles towards GBW. Concerning power consumption, reference [54] compares a basic Miller compensation with NCFF compensation and comes to the conclusion that for the usage at low frequencies the Miller approach is more economic as no third gain stage is needed. For the usage at higher frequencies however, the NCFF variant is more economic than an improved high-frequency Miller configuration. As [56] points out it is also possible to reuse the bias current from the second stage of the two-stage amplifier to realize the fast feedforward stage.

3.3.5 Other Frequency Compensation Methods

In the literature also other, less known frequency compensation methods are listed which should offer improved PSRR performance. A selection of them is listed below. Hereby the main idea is always to avoid the degradation of the PSRR through the diode-connected output transistor caused by the compensation capacitor.

- Blakiewicz Compensation: Blakiewicz presented in [58] a topology based on an additional stage in which the compensation capacitor is not connected to the signal path between the first and second stage, but between a newly introduced current branch and the gate of the output transistor. The additional stage introduces a LHP zero which can be adjusted through a bias transistor in an easy way. By placing the zero between the second pole and GBW, smaller compensation values are needed, but a non-monotonic phase behavior is present which might be problematic for some applications [25]. However, the GBW is increased, the compensation capacitor decreased and the PSRR is increased by 20 dB as described by Blakiewicz.

- Whatley Stage: A slight modification of the current buffer variants is presented in [51] which bases on a cancellation principle. Whatley uses the standard Miller compensation and adds a grounded gate stage in which a second capacitor C_{Canc} is connected to V_{SS}. Therefore two signal paths from V_{SS} to the output are present at high frequencies: one over the diode-connected output transistor of the second stage and a second one over C_{Canc}, the grounded gate stage and the Miller capacitor towards the output. The key point of this variant is that the introduced currents have opposite polarity and therefore cancel out each other. A drawback of this solution is the increased current consumption and the increased area caused by the second capacitor. In terms of PSRR the Whatley variant exhibits high values at dc and high frequencies, but lower values at medium frequencies.

4 Design of Two-Stage EMI-Immune Amplifiers

In order to harden amplifier against EMI, different measures for the first and second stage can be taken. As seen in previous sections, the first stage is the main contributor for output dc shift while the frequency compensation method in the second stage is responsible for the PSRR performance. Taking this separation into account it seems natural to split up the design process of an EMI hardened amplifier into two parts: In this chapter a basic Miller amplifier is designed and EMI measures from Section 3.1 are simulated. EMI robust frequency compensation methods will then be discussed in Chapter 5.

4.1 Amplifier Application and Specification

As a target design application, a low power amplifier for usage in near-field communication (NFC) powered devices is considered. As the power supply in NFC applications is derived directly from high-frequency signals, a high immunity against those disturbances is fundamental. The power supply of such applications is filtered by means of a low-dropout regulator (LDO) in order to guarantee a stable supply. Nevertheless, such elements are not capable to filter all disturbances and EMI signals can enter the amplifier through all pins. In order to put the surroundings in numbers, a few spare amplifier specifications are considered:

- Maximum power consumption of 100 µW at 3 V power supply
- Varying load impedance between 80 kΩ – 80 MΩ and 0 – 10 pF
- Capability to drive 10 µA load current
- UGF of at least 1 MHz and an open loop gain of at least 60 dB

Caused by the NFC application, the most critical EMI frequencies are set with the frequency of the NFC signal itself at 13.56 MHz and the first harmonics. As digital switching signals derived from the NFC supply can occur, the frequency range of interest is limited from approximately 5 MHz to around 30 MHz. At higher frequencies the LDO attenuates the NFC signal quite well and no EMI is considered. With the NFC power supply also the polarity of the input differential pair is fixed to PMOS transistors as this configuration offers higher immunity against disturbances on the V_{DD} rail than a NMOS configuration.

4.1.1 Design of a Miller Amplifier

The design procedure for the Miller amplifier is based on the guidelines given in [7]. In order to receive a PM of 60°, the needed Miller capacitor C_M can be calculated with the maximum load capacitance $C_L = 10\,\text{pF}$ by

$$C_M > \frac{2.2}{10} \cdot C_L = 2.2\,\text{pF} \tag{4.1}$$

With the chosen compensation capacitor, the required transconductance of the input stage can be calculated by

$$g_{m1} = 2\pi \cdot UGF \cdot C_M = 2\pi \cdot 1\,\text{MHz} \cdot 2.2\,\text{pF} = 13.8\,\mu\text{S} \tag{4.2}$$

With a gm/ID approximately equal to ten, the bias current for the first stage can be calculated. Neglecting the design of the NMOS current mirrors and the PMOS bias transistors, the transconductance of transistor M_6 is calculated by

$$g_{m6} = 2.2 \cdot g_{m1} \cdot \frac{C_L}{C_M} = 2.2 \cdot 13.8\,\mu\text{S} \cdot \frac{10\,\text{pF}}{2.2\,\text{pF}} = 138\,\mu\text{S} \tag{4.3}$$

With the knowledge of g_{m6} also the needed minimal current for the second stage can be calculated ensuring identical current densities in the NMOS transistors. Using the calculated values, the dimensions of the transistors can be calculated with the formulas given in [7]. However, the simulated amplifier suffers from diverse drawbacks:

- UGF of 1 MHz not reached because the achieved transconductances of the input and output stage were to small.
- Drive current of 10 µA not reached
- Miller capacitor is with 2.2 pF rather big

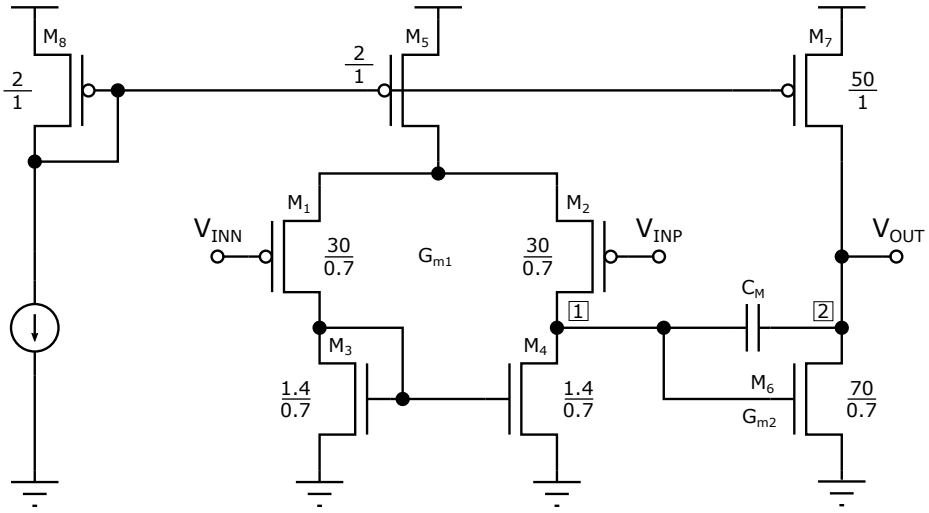


Figure 4.1: Schematic of the basic Miller amplifier with the transconductance of the first stage $G_{m1} = 13.3\,\mu S$ and of the second stage $G_{m2} = 542.4\,\mu S$.

In order to deliver sufficient drive current for the load without cutting-off M_6, the current in the second stage was increased. Doing so the gm/ID limitation of transistor M_6 is avoided and a higher GBW is possible. Considering the PSRR design guidelines given in previous sections, the value of the Miller capacitor was decreased using the Miller theorem. Equation (3.3) implies that by increasing the gain of the second stage by a factor of three, the capacitance seen at the input also is increased by a factor of approximately three. Therefore the second stage was redesigned with

$$g_{m6,new} = 3 \cdot g_{m6} = 3 \cdot 138\,\mu S = 414\,\mu S \tag{4.4}$$

$$C_{M,new} \approx \frac{1}{3} \cdot C_M = \frac{1}{3} \cdot 2.2\,pF = 733\,fF \tag{4.5}$$

To include the changes of the output resistance of M_6 and the effects of the increased parasitic capacitances, the final dimensions were adjusted in simulation. With the increased bias current and bigger transistor dimensions in the second stage, power consumption and parasitic capacitances were traded for a smaller C_M. This was possible as the achieved power consumption is below the specification of 100 µW. The final dimensions of the Miller amplifier given in µm are indicated in Fig. 4.1.

4.1.2 Ac Simulation of the Miller Amplifier

Considering mismatch and process variations, a Monte Carlo analysis using 100 runs was used to define the mean ac performance in Table 4.1 under different load configurations. To attain a stable ac performance with changing load configurations, the amplifier was

Parameter	$ZL_{80M,10p}$	$ZL_{80k,10p}$	$ZL_{80M,0p}$	$ZL_{80k,0p}$
UGF	2.4 MHz	2.2 MHz	2.5 MHz	2.4 MHz
A_0	88.8 dB	69.9 dB	88.8 dB	69.9 dB
PM	68.1°	63.4°	85.3°	84.6°

Table 4.1: Mean results of Monte Carlo simulations of the Miller amplifier for different load conditions

designed to work without a nulling resistor or transistor by pushing the non-dominant pole beyond UGF. Doing so a stable phase behavior is achieved as visible in Fig. 4.2. To achieve comparable results for other compensation methods, a generalized load of 10 MΩ ∥ 10 pF is considered for further analysis from now on. All simulations are performed in Cadence Spectre using a 0.13 µm CMOS technology.

The simulated dominant and non-dominant poles using PZ-analysis coincident with −94.4 Hz and −6.7 MHz pretty well with the calculated ones −97.5 Hz and −7.5 MHz using (3.4) and (3.5). The used values for R_{n1}, R_{n2}, C_{n1}, C_{n2} and C_M were

$$R_{n1} = \frac{1}{g_{ds2} + g_{ds4}} = 9.0\,\mathrm{M\Omega}, \tag{4.6}$$

$$R_{n2} = \frac{1}{g_{ds6} + g_{ds7} + 1/R_L} = 416.6\,\mathrm{k\Omega}, \tag{4.7}$$

$$C_{n1} = C_{gs,6} + C_{gb,6} = 114.5\,\mathrm{fF}, \tag{4.8}$$

$$C_{n2} = C_L = 10\,\mathrm{pF}, \tag{4.9}$$

$$C_M = 800\,\mathrm{pF}. \tag{4.10}$$

All other poles and zeros are placed beyond 10 MHz and are therefore not considered for the ac performance.

4.2 Test Benches for EMI

To evaluate EMI measures, dedicated simulation TBs are needed. A simulation setup for realistic DPI simulations is given in [59]. The presented TBs include many components to simulate automotive environments. Such components model automotive cable harnesses which are not suitable for consumer IC. In contrast to the TBs for automotive EMI simulations, much simpler TBs are presented in [32] were amplifier configurations for all amplifier pins are given.

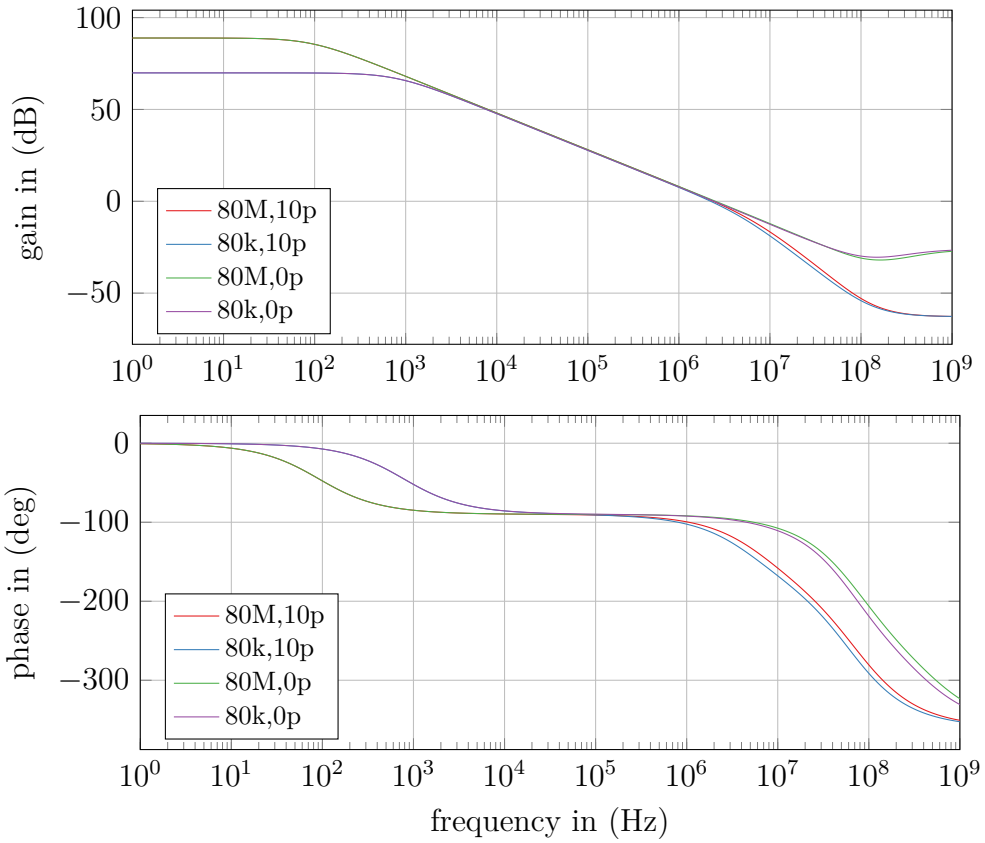


Figure 4.2: Miller ac simulations for different load conditions

With the knowledge of the theoretical background of EMI and the basic DPI standard, different criteria for EMI simulation TBs can be assumed:

- Basic configuration: In order to simulate EMI, the amplifier is configured in a voltage follower configuration with its standard load. In reference [32] V_{OUT} and V_{INN} are considered separately and decoupled by means of an RC LP. However, this does not represent the common amplifier application in real life where EMI easily can disturb V_{OUT} and V_{INN} directly. Therefore EMS for both V_{OUT} and V_{INN} pins is considered in one TB without isolation.

- LP and Z_{IN}: To measure the pure dc shift at the output of an amplifier, a LP filter is needed. Depending on the used measurement setup, a voltmeter or oscilloscope without the use of an LP could be used. However, it is not confident to rely on the device-intern averaging, especially at higher frequencies. Therefore a simply RC LP as suggested in [32] and [59] is used with different component values in order to reduce the additional load on the DUT. The values of the used LP components are given with with $R_{LP} = 22\,k\Omega$ and $C_{LP} = 500\,pF$. Furthermore

the input impedance of the measurement device is modeled with 10 MΩ resistiv load, which corresponds to the input impedance of a voltmeter.

- Bias tee: To injected dc and ac signals simultaneously, a bias tee is used. In contrast to [46] an injection capacitor of 6.8 nF is used with corresponds to the DPI standard. The suggested capacitance value of 4.7 pF in [46] is not reasonable in the considered simulation range from 5 MHz to 30 MHz as the injection impedance is quite high producing a large voltage drop. Moreover, a voltage divider with the amplifier load is formed when the V_{OUT} pin is tested since 4.7 pF is in the range of the amplifier load capacitance. With the used 6.8 nF a stable injection factor is ensured as the load capacitance is much smaller. The used capacitance of 6.8 nF however is quite large and therefore amplifier stability must be ensured. To keep the TB simple, ideal capacitances and inductances for the bias tee are used. A comparison with components including parasitics indicated no difference in the simulation results.

- RF source: To generate EMI, a power source with an internal resistance of 50 Ω producing sinusoidal signals is used. As implied in the DPI standard the termination resistance is chosen with 50 Ω.

- Decouple capacitances: In contrast to [32], an unipolar power supply is considered where V_{SS} lies on the same potential as ground. Therefore two decouple capacitances of 100 pF and 10 µF are connected only to the V_{DD} supply rail.

- Blocking devices: In [46] a resistance of 50 Ω is suggested to block RF from ideal dc sources. Simulations showed that 50 Ω is a rather small value to block the signals and a large amplitude of the EMI signal was absorbed from ideal sources. Therefore an ideal inductance with at least 400 Ω over the whole simulation frequency range was used for the bias tee. For biasing of components without direct EMI injection, no blocking devices where used as simulation showed no difference in the results.

- Injection time: In order to allow the DUT to reach a stable operating point, the RF disturbance is injected via a switch after a short delay. [59]

As simulation showed the specification of the used simulation TB is exceedingly important. Changes in the results were visible in simulations if the amplifier load, LP or bias tee components where changed. Without TB specification no confident valuation of the simulation or measurement results can be accomplished.

4.2.1 Simulation Setup

As already discussed, the output dc shift and the EMIRR FOM will be used to characterize EMI measures. Due to the logarithmic scale the usage of EMIRR offers advantages if large differences are present in the results. However, the EMI injection voltage is limited to 100 mV and a sign change of the output dc shift produces huge EMIRR values complicating the readability of figures. Therefore both dc shift and EMIRR will be used depending on the simulation results.

The simulation procedure itself is based on the EMIRR procedure discussed in [32]:

- Measuring the amplifier offset without RF interference after the amplifier reached a stable operation point
- Applying the RF interference
- Measuring the amplifier offset with RF interference after the amplifier reached his new operation point. In addition to the LP an averaging function in simulation is implemented to measure pure dc values.
- Calculating the EMI induced dc shift and EMIRR

The overall simulation time is equal to 300 µs and allows a settling of the LP output within the first 150 µs for all EMI frequencies. The averaging and measuring is then applied for the time frame between 150 µs and 300 µs and compared with the amplifier offset measured at 1 µs, right before the EMI injection starts.

4.2.2 Test Bench for the Non-Inverting Input Pin

The complete TB for V_{INP} is indicated in Fig. 4.3. The amplifier under test is supplied with $V_{DD} = 3\,V$ and $V_{SS} = 0\,V$ and biased in the middle of the supply range. Z_L, which represents the standard application load, was chosen to $10\,M\Omega \parallel 10\,pF$. With an injection capacitor of 6.8 nF, an input impedance between 4.7 Ω and 0.8 Ω is achieved over the whole frequency range which enables a consistent simulation. The simulated output dc shift at the NFC frequency of 13.56 MHz and an EMI amplitude of 100 mV is equal to −860.2 µV. In terms of EMIRR 41.31 dB are reached.

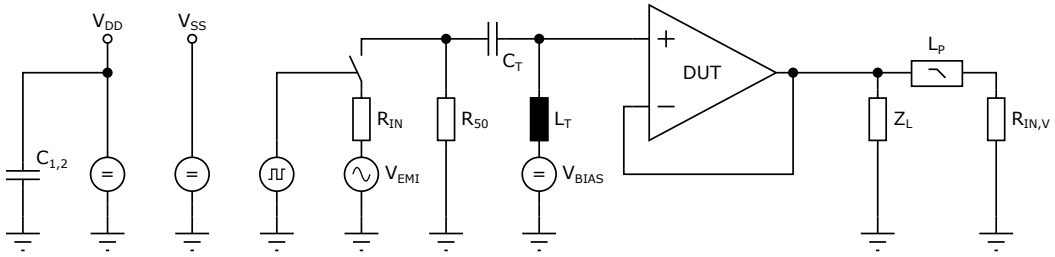


Figure 4.3: EMI TB for V_{INP}

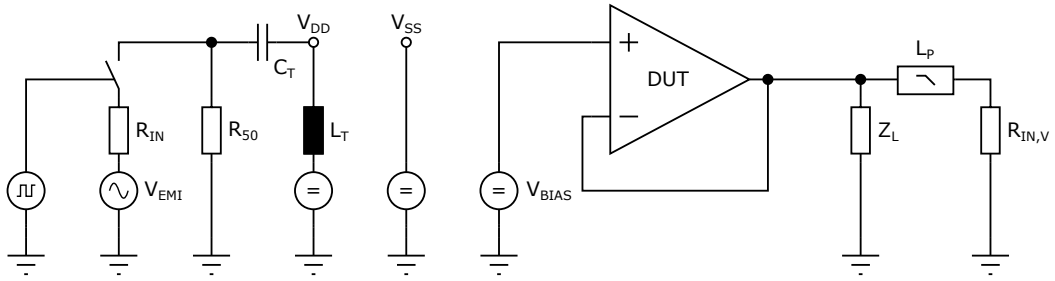


Figure 4.4: EMI TB for V_{DD}. For injection into V_{SS} the decouple capacitances need to be added to the V_{DD} rail as carried out in other TBs.

4.2.3 Test Bench for the Power Supply Pins

To simulate the susceptibility of the amplifier on the power supply rails, the TB in Fig. 4.4 is used. For the injection into V_{DD}, the decoupling capacitances need to be removed as otherwise the RF signals are shorted to V_{SS}. For the injection into V_{SS} these capacitances are reconnected again. The simulated output dc shift for injection into V_{DD} is equal to $-74.1\,\mu V$ while for injection into V_{SS} a shift of 1.2 mV is simulated at 13.56 MHz. The associated EMIRR values are calculated with 62.6 dB and 38.2 dB. As expected, the amplifier is more susceptible on one supply rail than on the other caused by the used Miller frequency compensation. At 13.56 MHz the Miller capacitor is already conducting and feeds the disturbances to the output of the amplifier. Therefore not only the V_{SS} pin is interfered, but also the V_{OUT} and V_{INN} pins are influenced which explains the high susceptibility.

4.2.4 Test Bench for the Output Pin

In difference to the other pins, the RF disturbance is inductively coupled into V_{OUT} and hence also V_{INN} in Fig. 4.5. This yields from the application in a NFC powered system where it is much more likely that EMI enters the output pin via inductive

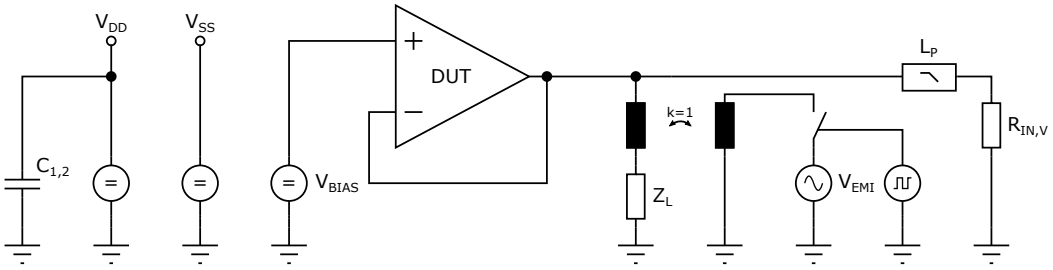


Figure 4.5: EMI TB for $V_{OUT,INN}$

loops on the PCB than from capacitive couplings. The inductive coupling in simulation is implemented with two inductances with a coupling coefficient k = 1. Simulations confirmed the correct behavior of the EMI injection and showed good accordance with capacitive injection as carried out for other pins. The simulated output dc shift is considerable with 4.9 mV at 13.56 MHz. Therefore also the simulated EMIRR value is pretty low with 26.2 dB. This can be explained by the direct connection of the output to the inverting input. Doing so the entire RF signal is applied to two pins at the same time and bigger demodulation is achieved.

4.3 Circuitry Measures to Increase the EMI Robustness

In order to improve the robustness against EMI, different measures can be taken as discussed in Section 3.1. To test the efficiency of the measures, several implementations will be designed and directly compared to the standard design. The focus hereby lies on simple and small implementations that do not require huge design modifications. The valuation will be carried out for all amplifier pins over the considered EMI frequency range as measures on one amplifier pin also can have a positive effect on the susceptibility of other pins.

4.3.1 Reducing Channel Length Modulation Effects

A possibility to increase the robustness of amplifiers against EMI lies in the reduction of CLM effects in the bias transistors. As discussed, CLM effects produce asymmetric slew rates caused by increased or decreased drain-source voltages. In order to reduce CLM effects, the length of the bias transistors can be increased as CLM effects are directly linked to transistor length. Considering PSRR, further improvements are expected as the channel resistance of the bias transistors is increased and therefore the transfer

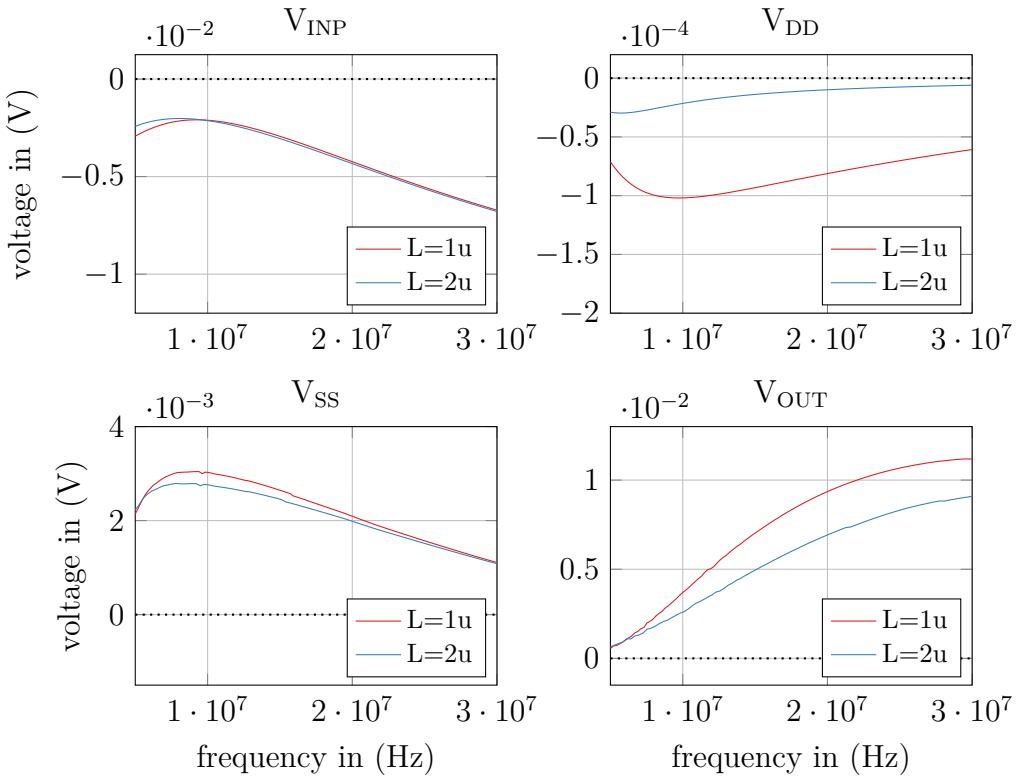


Figure 4.6: EMI-induced offset simulation results for different bias transistor lengths

function (TF) from V_{DD} to V_{OUT} is reduced. On the downside, an increased amplifier area is required, especially if high mirror factors for the bias transistor of the second stage are used.

The simulation result for different bias transistor lengths and constant transistor widths is shown in Fig. 4.6. As expected, the dc shift at the output decreases with increasing transistor lengths. In particular for V_{DD} an improvement of the EMI robustness is recognizable where the output shift is reduced by a factor of fourteen at the NFC frequency of 13.56 MHz. Also for V_{OUT} an improvement by a factor of nearly two is noticeable. By increasing the transistor lengths further to $L = 4\,\mu m$ about the same improvement as from 1 µm to 2 µm is visible for V_{SS} and V_{OUT}. For V_{INP} and V_{DD} however the output shift worsens slightly compared to $L = 2\,\mu m$ which can be explained by the increased parasitic capacitances which dominate the impedance from V_{DD} towards V_{OUT} at higher frequencies.

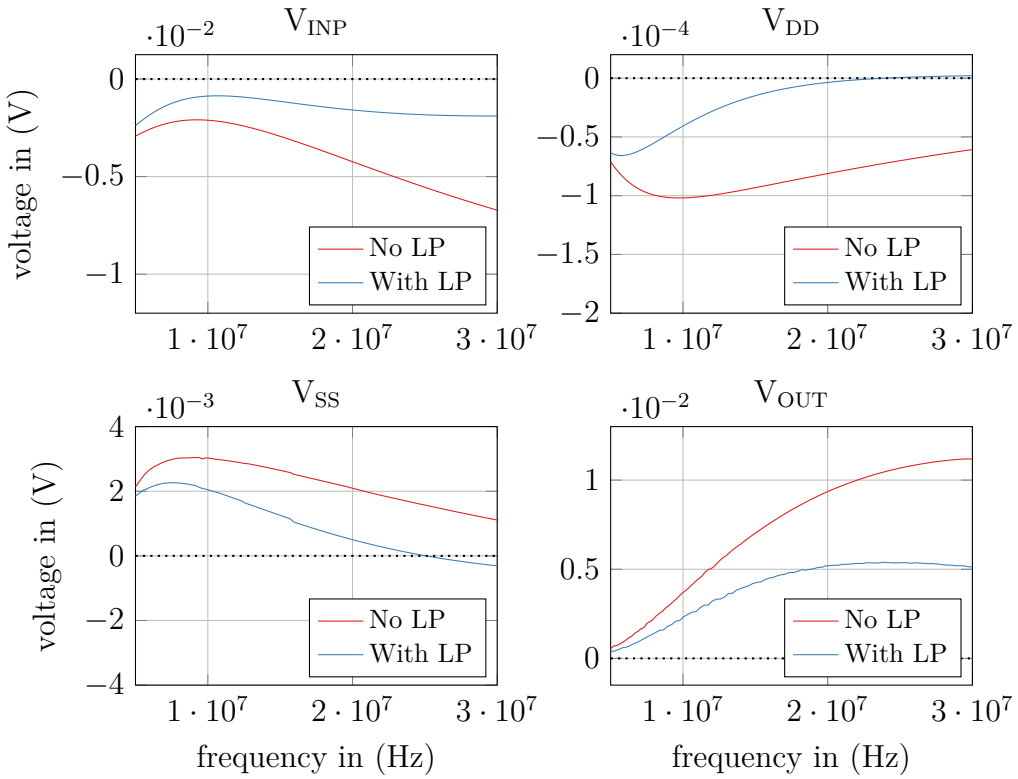


Figure 4.7: EMI-induced offset simulation results for added RC LP at the inputs

4.3.2 Input Filter

A highly effective way to increase the robustness against EMI on the inputs relies on the use of RC LP filters. Directly connected between input pins and gate of the input transistors, they prevent the RF signals from entering the amplifier. However, the additional pole must be pushed above 10·UGF in order to achieve a PM degradation below 5° [14]. Additionally, noise is increased as resistors are present in the signal path. Michel and Steyaert derive in [14] that for $C_{LP} = C_L$ the resistor noise is negligible. For practical applications, this is not always possible as the additional area is not reasonable. Therefore a trade-off between noise and area must be found. As no limiting specifications for area and noise are given, a maximal increase of the input noise $\Delta noise$ of 20 % was considered as acceptable for this design. A rough estimation for the maximal allowable resistance value and the corresponding capacitance value can be calculated with the transconductance of the input pair Gm_1 and factor k to account other noise sources as taken from [13]:

$$R_{LP} = \frac{\Delta noise \cdot k}{100 \cdot G_{m1}} = \frac{20 \cdot 1.5}{100 \cdot 13.26\,\mu S} \approx 22\,k\Omega \tag{4.11}$$

$$C_{LP} = \frac{1}{2\pi \cdot 10 \cdot UGF \cdot R_{LP}} = \frac{1}{2\pi \cdot 10 \cdot 2.4\,MHz \cdot 22\,k\Omega} \approx 300\,fF \tag{4.12}$$

It should be noted that with lower resistance values, lower noise is possible. With the additional RC LP a PM degradation from 68° to 61° was visible which applies to the estimated 5° beforehand. The EMI simulations with the added LP can be found in Fig. 4.7 and show a great improvement on all pins. Regarding V_{SS} a slight decline in immunity is visible at 30 MHz. This can be explained with the connection of the LP to V_{SS}. Doing so disturbances on the V_{SS} rail can couple over the LP capacitances to the amplifier inputs. Smaller capacitances can shift this phenomenon to higher frequencies at the cost of higher resistance values and hence higher noise. If the V_{DD} supply is considered more immune, the LP capacitances can be connected towards V_{DD} to shift the phenomena from V_{SS} towards V_{DD}. The usage of an additional LP-filtered input pair is not considered, because of the assumed low power NFC application.

4.3.3 Input Capacitances

As seen in the second chapter of this thesis, parasitic capacitances play an important role when dealing with EMI. To reduce the EMI-induced offset, C_{GS} can be increased by adding extra gate-source capacitances $C_{GS,Ex}$ [14]. By choosing $C_{GS,Ex}$ larger then C_{Tail}, a capacitive voltage divider between C_{GS} and C_{Tail} is formed and V_{GS} is set to zero for high-frequency EMI. A similar procedure is based on (2.1) and (2.2): They indicate a difference in the gate-source voltages of the input transistors in feedback configuration caused by parasitic capacitances. Due to the asymmetric gate-source voltage, different currents are produced and an offset at the output is visible. Reference [44] tries to minimize the differences between $V_{GS,INP}$ and $V_{GS,INN}$ by deriving an optimal solution for the added gate-source capacitances:

$$C_{GS,INP} = \frac{t_0 + t_1}{s_2} \tag{4.13}$$

$$C_{GS,INN} = \frac{s_0 + s_1}{s_2} \tag{4.14}$$

As [44] indicates, the needed factors s_0, s_1, s_2, t_0 and t_1 can be calculated in a way that both capacitances $C_{GS,INP}$ and $C_{GS,INN}$ can be realized by constant capacitances values:

$$m_a = g_{m1} + g_{mbs1} \tag{4.15}$$

$$m_b = 1 + 2 \cdot g_{mbs1} \cdot r_5 \tag{4.16}$$

$$s_0 = g_{m1} \cdot (g_{m1} + 2 \cdot g_{mbs1}) \cdot (1 + 2 \cdot m_a \cdot r_5) \tag{4.17}$$

$$s_1 = 2 \cdot m_a \cdot r_5 \cdot (C_{Tail} \cdot g_{m1} \cdot (1 - 2 \cdot m_a \cdot r_5) + 2 \cdot m_a \cdot m_b \cdot C_{GS1}) \cdot (-\omega_{UGF}) \tag{4.18}$$

$$s_2 = 4 \cdot m_a^2 \cdot m_b \cdot r_5 \cdot \omega_{UGF} \tag{4.19}$$

$$t_0 = g_{m1}^2 \cdot (1 + 2 \cdot m_a \cdot r_5) \tag{4.20}$$

$$t_1 = 2 \cdot m_a \cdot r_5 \cdot (C_{Tail} \cdot g_{m1} \cdot (1 + 2 \cdot m_a \cdot r_5) - 2 \cdot m_a \cdot m_b \cdot C_{GS1}) \cdot \omega_{UGF} \tag{4.21}$$

Hereby equal g_m, g_{mbs} and C_{GS} are assumed for both input transistors. r_5 is composed by the resistance of the tail current source transistor and C_{Tail} by the overall sum of the

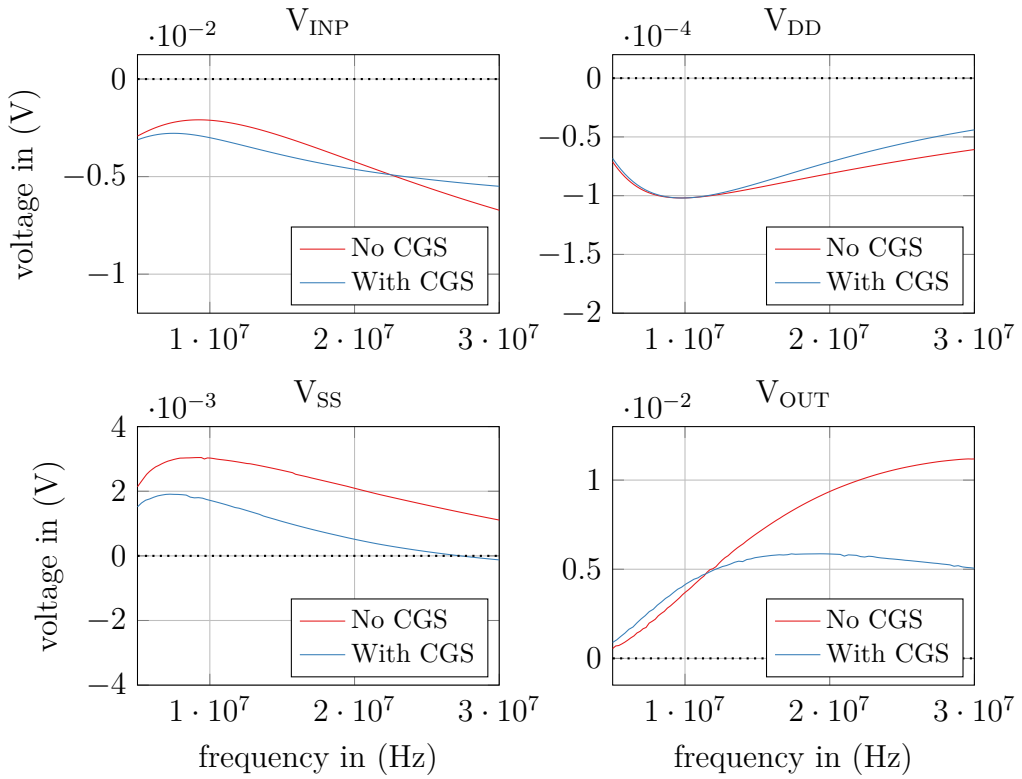


Figure 4.8: EMI-induced offset simulation results for $C_{GS,INP} = 68\,fF$ and $C_{GS,INN} = 72\,fF$

capacitances from the common source node of the input transistors towards ac ground. At this point it must be noted that if no well-capacitances are implemented in a given process, these capacitances need to be added manually as they influence the overall EMI behavior drastically.

Using (4.13) and (4.14), the external capacitances can be calculated with $C_{INP} = 68\,fF$ and $C_{INN} = 72\,fF$. Caused by the small values no influence on the ac performance is assumed in theory and proven in simulation. The results in Fig. 4.8 show an improved EMI robustness on the V_{SS} and V_{OUT} pins. For V_{INP} and V_{DD} however, only a high-frequency improvement is visible. As [44] indicates, not the calculated values were used for simulations in the reference, rather optimized capacitance values gained from simulation results. This procedure can be carried out to increase the robustness of single amplifier pins even further.

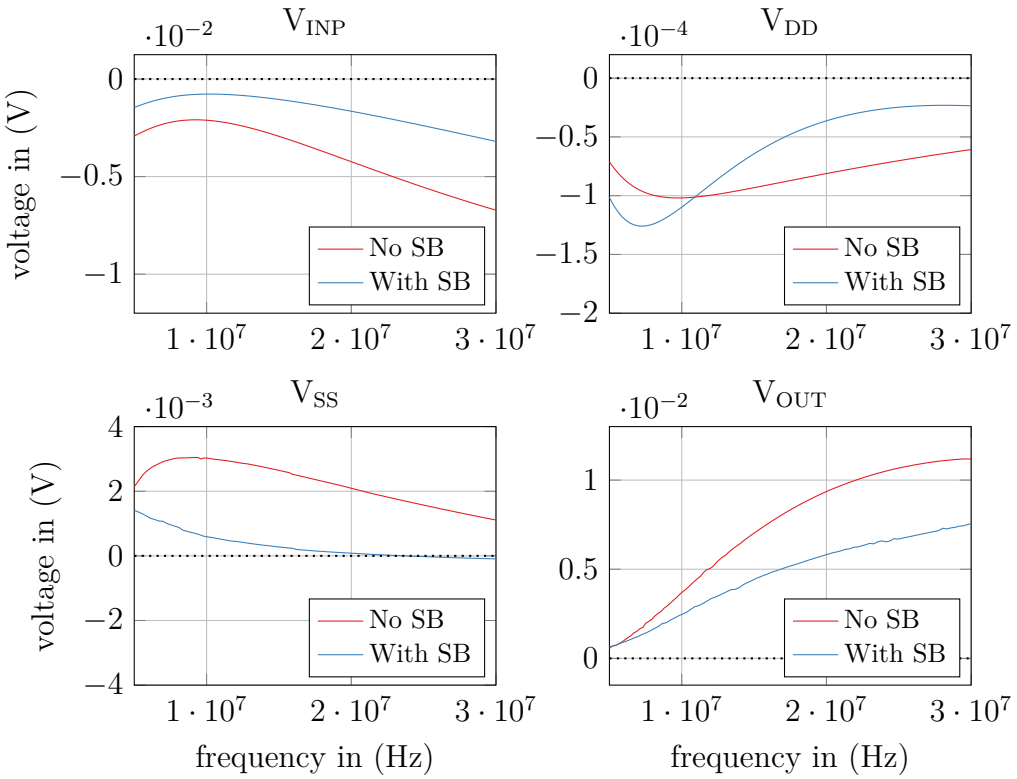


Figure 4.9: EMI-induced offset simulation results for source buffering (SB) with bulk pins connected to V_{DD}

4.3.4 Source Buffering

Another way to reduce the differences in (2.1) and (2.2) lies in the reduction of C_{Tail}. As mentioned in previous sections, C_{Tail} is mainly formed by the large well capacitances. In order to reduce C_{Tail}, the bulk-source connection of the input transistors need to be removed which avoids the usage of an additional well. In the literature this is often considered when NMOS transistors are used in the input differential pair, however, the matter can also be applied to PMOS input transistors.

By connecting the bulk connection to V_{DD} or V_{SS}, C_{Tail} is minimized. However, V_{BS} induces a threshold voltage shift known as body effect. This can be prevented with the use of a second input differential pair indicated in Fig. 3.2 that bias the bulk connections of the main amplifier input transistors. By doing so, the threshold voltage shift is avoided at the cost of an increased power consumption. The method based on a direct bulk connection towards $V_{DD,SS}$ sacrifices threshold voltage shift for lower power consumption. The outcome for EMI robustness however is to a large degree independent from the potential of the bulk connection as long as C_{Tail} is minimized.

From the simulation results in Fig. 4.9, an improvement of the EMI robustness up to a factor of four on the V_{SS} supply rail is visible when the bulk pins are connected to V_{DD}. When an additional input pair is used, a similar EMI behavior is visible in the simulations. The overall result is in contrast to the usually practiced manner to put susceptible elements in extra wells. The latter works fine to shield elements against a disturbed substrate. However, from an EMI point of view, parasitic capacitances are increased by a large factor and the amplifier is much more susceptible to EMI then without extra wells.

4.3.5 Common-Mode Cancellation Circuit

Another measure to reduce the EMS lies in the reduction of the common-mode part in (2.3). In [45], a common-mode cancellation circuit (CMCC) using inverters is presented, which attenuates common-mode signals and increases differential-mode gain. The differential gain A_{DM} is modified by a factor K_{DM} and the common-mode gain A_{CM} by a factor K_{CM}. Reference [4] improves the CMCC by using current-starved inverters to slow down the inverter slope. As the considered application for the designed amplifier lies in a low-power application, the current-starved variant with diode-connected transistors was used with a maximal crowbar current of 2.6 µA. Reference [4] calculates K_{DM} and K_{CM} of the circuit in Fig. 3.3 by:

$$K_{DM} = \frac{R_2 + R_{INV}}{R_1 + R_2 + R_{INV}} + R_2 \cdot G_{m,INV} \tag{4.22}$$

$$K_{CM} = \frac{R_2 + R_{INV}}{R_1 + R_2 + R_{INV}} - R_2 \cdot G_{m,INV} \tag{4.23}$$

The factors R_{INV} and $G_{m,INV}$ can be found by

$$R_{INV} = \frac{1}{g_{ds,p} + g_{ds,n}} + \frac{1}{g_{m,p'} + g_{m,n'}} + \frac{g_{m,p} + g_{m,n}}{(g_{m,p'} + g_{m,n'}) \cdot (g_{ds,p} + g_{ds,n})} \tag{4.24}$$

$$G_{m,INV} = \frac{g_{m,p} + g_{m,n}}{1 + \frac{g_{m,p}+g_{m,n}}{g_{m,p'}+g_{m,n'}} + (R_1 + R_2 + \frac{1}{g_{m,p'}+g_{m,n'}}) \cdot (g_{ds,p} + g_{ds,n})} \tag{4.25}$$

where $g_{m,p'}$ and $g_{m,n'}$ correspond to the transconductance of the diode-connected PMOS and NMOS transistors and $g_{m,p}/g_{m,n}$ as well as $g_{ds,p}/g_{ds,n}$ to the values of the inverter transistors. As R_{INV} normally is much bigger then R_1 and R_2, the first term of K_{DM} and K_{CM} is approximately one. Hence, the value of R_2 can be calculated with (4.22) and (4.25) by

$$R_2 \approx \frac{2 + \frac{g_{ds,p}+g_{ds,n}}{g_{m,p'}+g_{m,n'}}}{g_{m,p} + g_{m,n}} = \frac{2 + \frac{181.43\,\text{nS}}{29.2\,\mu\text{S}}}{29.89\,\mu\text{S}} = 67.1\,\text{k}\Omega \tag{4.26}$$

Doing so K_{CM} theoretically equals zero and K_{DM} is increased to two. As this relies on the matching of resistors with transistors, perfect canceling will not occur. Reference [45]

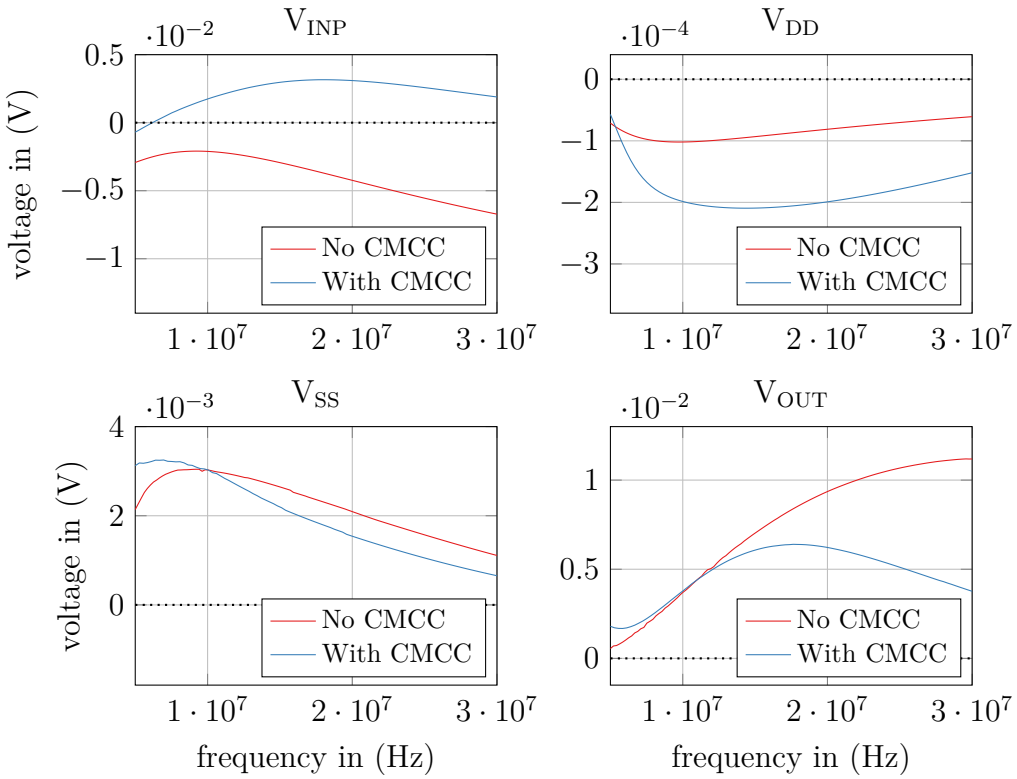


Figure 4.10: EMI-induced offset simulation results for a common-mode cancellation circuit

indicates that the circuit is not very sensitive to mismatch. However, Monte Carlo simulation showed an increased standard derivation for the output shift for V_{DD} up to a factor of two larger than without CMCC. On the other pins the standard derivation with CMCC was 1.5 times larger than without CMCC. From an ac and EMI performance point of view, the value of R_1 is not from big importance. However, R_1 can not be designed too small as it influences the input common-mode range of the amplifier and was chosen with 1 kΩ.

Simulations confirmed the positive effect of the CMCC on ac-performance: The dc gain was raised from 88.6 dB to 94.3 dB and the UGF from 2.4 MHz to 4.1 MHz. With the increased UGF a reduction of the PM from 67.8° to 47.8° was observable, while the dominant and first two non-dominant poles were not changed from the CMCC. Concerning EMI performance, the biggest improvements are observable on the output and non-inverting input, especially at higher frequencies. However, on the V_{DD} rail even a slight increase of the EMI-induced offset is visible, which could result from the additional V_{DD} paths.

	CLM	RC LP	C_{GS}	SB	CMCC
V_{INP}	∼	+	-	+	++
V_{DD}	++	+	∼	∼	-
V_{SS}	∼	+	+	++	∼
V_{OUT}	∼	++	+	+	+
Ac	+	-	+	+	∼
I_{DD}	+	+	+	∼	-

Table 4.2: Evaluation of the simulated EMI measures

Based on the simulation results for each measure, different effectiveness for the amplifier pins can be determined in Table 4.2. To calculate the rating of the amplifier pins simulation results at 5 MHz, 6.78 MHz, 13.56 MHz, 20 MHz and 30 MHz were evaluated. The ratings of the simulated EMI measures were classified from very good (++) to poor (- -). To evaluate the effects of the measures on the circuit, ac performance and current consumption was grated too. The medium ac rating for the CMCC can be explained by the improved dc gain and UGF values in contrast to the degraded PM. Considering power consumption, the CMCC uses more power than a second input pair for SB while all other measures do not influence the power consumption. Based on Table 4.2 also different measures can be combined to achieve better EMI robustness depending on the critical EMI frequencies. From the results a combination of a RC LP and source buffering is advised to improve the EMI robustness of all amplifier pins.

5 Design of EMI-Immune Frequency Compensation Methods

With the knowledge of different EMI measures for the amplifier input-differential pair, the design of the amplifier frequency compensation method can be investigated. Two frequency compensation methods from Section 3.3 will be designed and validated with small-signal models and compared to the results of the Miller approach. In order to investigate the capabilities of the different frequency compensation methods also in terms of ac performance and current consumption, the same NFC-powered application as for the Miller amplifier is assumed. Doing so the same basics are set for all amplifier topologies and the capabilities and drawbacks of each topology can easily be compared.

5.1 Miller Amplifier

As already discussed, the Miller capacitor is responsible for the poor PSRR performance at higher frequencies. To prove this, the PSRR from the basic Miller amplifier designed in the previous chapter is simulated and small-signal models are constructed. Doing so not only the PSRR simulations can be verified but also circuit elements influencing the PSRR performance easily can be determined.

5.1.1 Notation for the Small-Signal Models

For the calculation of all small-signal models the following notation is used:

- Output resistance: R_{nx} indicates the output resistance at gain node x.
- Output capacitance: C_{nx} indicates the output capacitance at gain node x.

- Seperation: The usage of a comma indicates the sum of the mentioned values $A_{\text{value x,y}} = A_{\text{value x}} + A_{\text{value y}}$.

- Capitalization: Strict capitalized variables indicate the combination of different variables.

- Division: The usage of an apostrophe indicates an individual term $C_{\text{nx}'} \neq C_{\text{nx}}$. The definition of the individual term in indicated in the corresponding specification.

5.1.2 Small-Signal Models of the Miller Amplifier

To investigate the PSRR performance, XF-analysis in Spectre was used. Reference [7] indicates that the usage of a voltage follower configuration gives an easy way to calculate the PSRR as $TF_{\text{VIN,VOUT}}$ equals one. Therefore the PSRR can be found by the reciprocal of the TF from power supply to output. Doing so valid results are achieved until GBW where the voltage follower begins to attenuate input signals caused by the low-pass behavior of the OpAmp. As the EMI frequencies of interest lie above GBW, both TFs for input and output need to be considered separately. For the design of the small-signal models of the Miller amplifier in feedback configuration, the basic structure is constructed of two gain stages which are coupled by means of the Miller capacitor. To simplify the models, the voltage at the common source of the input differential pair is considered as virtual ground for all models [7]. As calculations will show, this simplification works well for small-signal models of the input TF, but may be inaccurate for PSRR calculations.

- V_{IN}: For the small-signal model of $TF_{\text{VIN,VOUT}}$ in Fig. 5.1, all capacitances between the output of the first and second stage towards ac ground are summarized in C_{n1} and C_{n2}. R_{n1} includes the drain-source conductances of the transistors $M_{2,4}$ and R_{n2} the drain-source conductances of the transistors $M_{6,7}$ as well as the load resistance R_{L}. Caused by the closed-loop configuration, feedback transistor M_1 is modeled as voltage-controlled current source in opposite direction to the model of transistor M_2 associated with the non-inverting input. The nodal equations are given by

$$V_1 \cdot (1/R_{n1} + sC_{n1,M}) + g_{m2} \cdot V_{IN} - V_{OUT} \cdot (g_{m1} + sC_M) = 0 \tag{5.1}$$

$$V_{OUT} \cdot (1/R_{n2} + sC_{n2,M}) + V_1 \cdot (g_{m6} - sC_M) = 0 \tag{5.2}$$

  with $R_{\text{n1}} = r_{\text{ds2}} \parallel r_{\text{ds4}}$ and $R_{\text{n2}} = r_{\text{ds6}} \parallel r_{\text{ds7}} \parallel R_{\text{L}}$. In order to shorten the TF equations, capitalized variables are used for all TF calculations to compromise the used small-signal values.

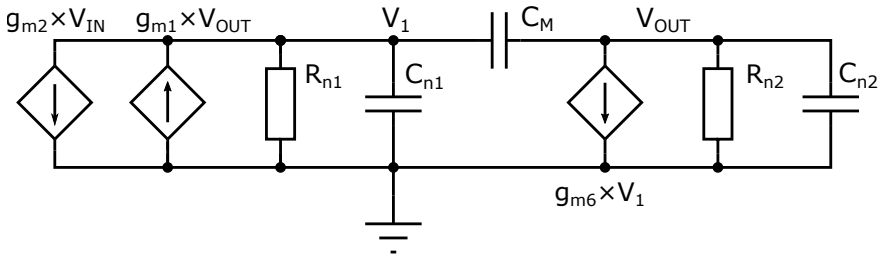


Figure 5.1: Small-signal model for $TF_{VIN,VOUT}$ of the Miller amplifier.

Solving the nodal equations for V_{OUT}/V_{IN} gives

$$\frac{V_{OUT}}{V_{IN}} = \frac{g_{m2} \cdot (sC_M - g_{m6})}{-GOUT \cdot GDS2 + GM1 \cdot (sC_M - g_{m6})} \tag{5.3}$$

with the capitalized variables

$$\begin{aligned} GM1 &= g_{m1} + sC_M, \\ GDS2 &= g_{ds2,4} + sC_{1,M}, \\ GOUT &= g_{ds6,7} + 1/R_L + sC_{2,M}. \end{aligned}$$

- V_{SS}: For the small-signal model of $TF_{VSS,VOUT}$ in Fig. 5.2, the model of $TF_{VIN,VOUT}$ is split up between V_{DD} and V_{SS}. To model the effect of the current mirror in the first stage, a voltage-controlled current source with a gain of g_{ds1} is used [7]. Allen and Holberg explain the usage of the current source with the current in the input stage branch containing M_1 and the diode-connected M_3:

$$I = g_{m1} \cdot V_{OUT} + g_{ds1} \cdot (V_{SS} - \frac{I}{g_{m3}}) \tag{5.4}$$

With the assumption $g_{m3} \gg g_{ds1}$ the current is approximately equal to

$$I \approx g_{m1} \cdot V_{OUT} + g_{ds1} \cdot V_{SS} \tag{5.5}$$

Due to the diode connection of M_3, voltage ripples on the V_{SS} rail are conducted to M_1 and then re-injected over the current mirror into the output of the first stage. This can also be explained with the CLM effect in M_1. Supply ripples on V_{SS} influence the drain-source voltage of M_1 and a displacement current is produced. To simplify the overall small-signal model, the parasitic capacitances towards the V_{DD} rail are neglected as the considered capacitances towards V_{SS} are relatively large. The nodal equations of the small-signal model for $TF_{VSS,VOUT}$ are given by

$$V_1 \cdot (g_{ds2,4} + sC_{n1,M}) - V_{SS} \cdot (g_{ds1,4} + sC_1) - V_{OUT} \cdot (g_{m1} + sC_M) = 0 \tag{5.6}$$

$$V_{OUT} \cdot (g_{ds6,7} + 1/R_L + sC_{n2,M}) - V_{SS} \cdot (g_{ds6} + g_{m6} + sC_{n2}) - V_1 \cdot (sC_M - g_{m6}) = 0 \tag{5.7}$$

were C_{n1} includes all capacitances from the output of the first stage towards V_{SS} and C_{n2} all capacitances from the output of the second stage towards V_{SS}. The

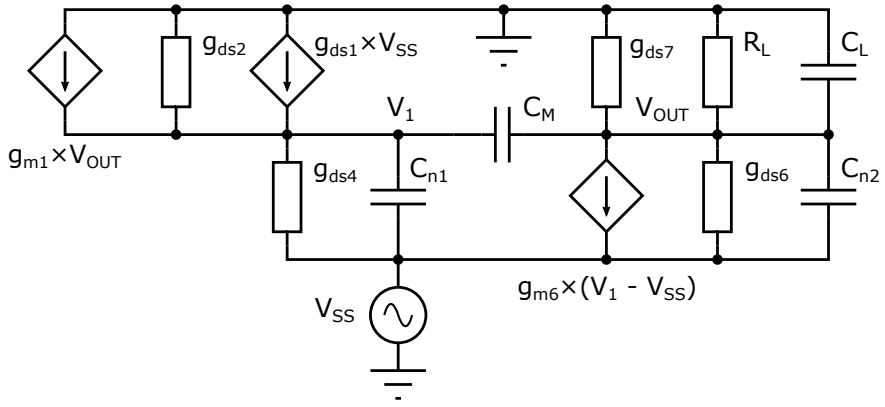


Figure 5.2: Small-signal model for $TF_{VSS,VOUT}$ of the Miller amplifier

load R_L and C_L is assumed to be connected to a noise free potential. Solving the nodal equation for V_{OUT}/V_{SS} gives

$$\frac{V_{OUT}}{V_{SS}} = \frac{GDS2 \cdot GM6 + GDS1 \cdot (sC_M - g_{m6})}{GDS2 \cdot GOUT - GM1 \cdot (sC_M - g_{m6})} \tag{5.8}$$

with

$$\begin{aligned} GM1 &= g_{m1} + sC_M, \\ GM6 &= g_{m6} + g_{ds6} + sC_{n2}, \\ GDS1 &= g_{ds1,4} + sC_{n1}, \\ GDS2 &= g_{ds2,4} + sC_{n1,M}, \\ GOUT &= g_{ds6,7} + 1/R_L + sC_{n2,M}. \end{aligned}$$

- V_{DD}: As for the small-signal model for $TF_{VSS,VOUT}$, the model for $TF_{VDD,VOUT}$ in Fig. 5.3 is constructed by splitting up all paths from the output of the stages towards V_{DD} and ac ground. As fewer paths from V_{DD} toward both stage outputs are present, parasitic capacitances are getting more important and influence the accuracy of the model. Concerning the bias system, the CLM effect of the bias transistors influences the behavior of the bias system as a realistic reference bias source has a certain impedance. V_{DD} voltage ripples are conducted via diode-connected transistor M_8 to the internal impedance of I_{Bias} and then re-injected into the circuit. For the present simulations, I_{Bias} is produced by an ideal current source and therefore influences of the bias system are neglected. The nodal equations of the small-signal model are given by

$$V_1 \cdot (1/R_{n1} + sC_{n1,n1',M}) - V_{DD} \cdot sC_{n1'} - V_{OUT} \cdot (g_{m1} + sC_M) = 0 \tag{5.9}$$

$$V_{OUT} \cdot (1/R_{n2} + g_{ds7} + sC_{n2,n2',M}) - V_{DD} \cdot (g_{ds7} + sC_{n2'}) - V_1 \cdot (sC_M - g_{m6}) = 0 \tag{5.10}$$

with $R_{n1} = r_{ds2} \parallel r_{ds4}$, $R_{n2} = r_{ds6} \parallel R_L$. C_{n1} includes the capacitances from the output of the first stage towards V_{SS} and C_{n2} the capacitances from the output of

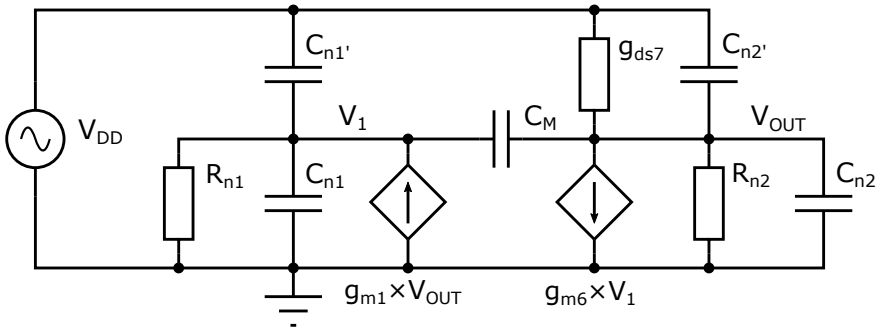


Figure 5.3: Small-signal model for $TF_{VDD,VOUT}$ of the Miller amplifier

the second stage towards V_{SS}. All capacitances from the output of the first stage towards V_{DD} are modeled in $C_{n1'}$ and from the second stage in $C_{n2'}$. Solving the nodal equation for V_{OUT}/V_{DD} gives

$$\frac{V_{OUT}}{V_{DD}} = \frac{GDS2 \cdot GDS7 + sC_{n1'} \cdot (sC_M - g_{m6})}{GDS2 \cdot GOUT - GM1 \cdot (sC_M - g_{m6})} \tag{5.11}$$

with

$$\begin{aligned} GM1 &= g_{m1} + sC_M, \\ GDS2 &= g_{ds2,4} + sC_{n1,n1',M}, \\ GDS7 &= g_{ds7} + sC_{n2'}, \\ GOUT &= g_{ds6,7} + 1/R_L + sC_{n2,n2',M}. \end{aligned}$$

5.1.3 PSRR Simulation of the Miller Amplifier

With the calculated TFs, the corresponding PSRRs can be determined using (2.6). The values of the considered small-signal variables are extracted from the Spectre simulations and directly used to calculate the PSRR figures. Doing so impacts of design changes are instantly visible in the simulated and calculated PSRR figures. With the usage of both PSRR figures, the previously mentioned voltage follower can be demonstrated in Fig. 5.4 when $TF_{VIN,VOUT}$ is considered as unity. Considering the position of the 0 dB PSRR point at 4 MHz, the formed voltage follower at the V_{SS} supply rail lies in the range of the critical NFC frequencies and above the UGF of the amplifier. This voltage follower needs to be avoided as disturbances on the supply rail couple directly to the output of the amplifier and can interfere with connected circuits. Moreover the amplitude of interfering signals is not attenuated and EMI appears not only on the V_{SS} rail but also at the output and inverting input pins if a feedback configuration

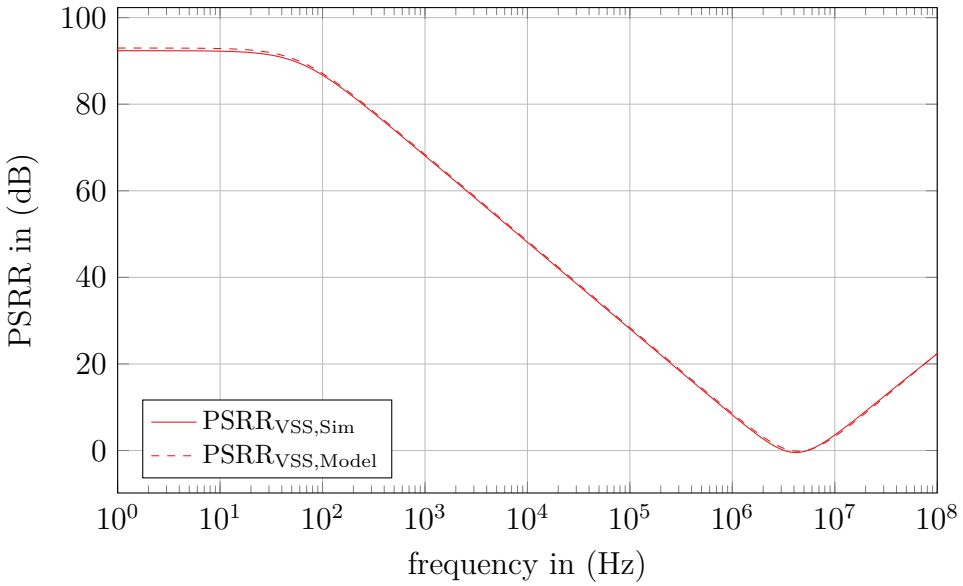


Figure 5.4: Demonstration of the voltage follower for V_{SS} in simulation and calculation considering a ideal $TF_{VIN,VOUT}$

is used. This influences the resulting dc shift as simulation will show. The increase of the PSRR at higher frequencies in Fig. 5.4 is caused by the connection of the load towards noise-free ground. By connecting the load towards V_{SS}, the PSRR sticks to values around 0 dB also at higher frequencies and therefore influences dc shift.

Considering a non-ideal voltage follower for $TF_{VIN,VOUT}$, the resulting PSRR figures are presented in Fig. 5.5. In contrast to the very precise matching of simulation and calculation for $PSRR_{VSS}$, the figures for $PSRR_{VDD}$ show a slight deviation. This is caused by the structure of the Miller amplifier as less dominant connections from V_{DD} compared to V_{SS} are present, demanding for exact modeling of parasitic parameters. For $PSRR_{VSS}$ the voltage follower effect takes a predominate role and therefore modeling is much easier. Referring to the deviation of the $PSRR_{VDD}$ figures, the concept of virtual ground at the common source point of the input pair may be incorrect as the influence of bias transistor M_5 is neglected. Though both PSRR calculations for V_{DD} and V_{SS} describe the rough behavior relatively well and indicate design factors that can be improved:

- Smaller Miller capacitor and low parasitic capacitances
- Low channel conductance of all bias transistors
- High G_{m1} with low mismatch and low gds

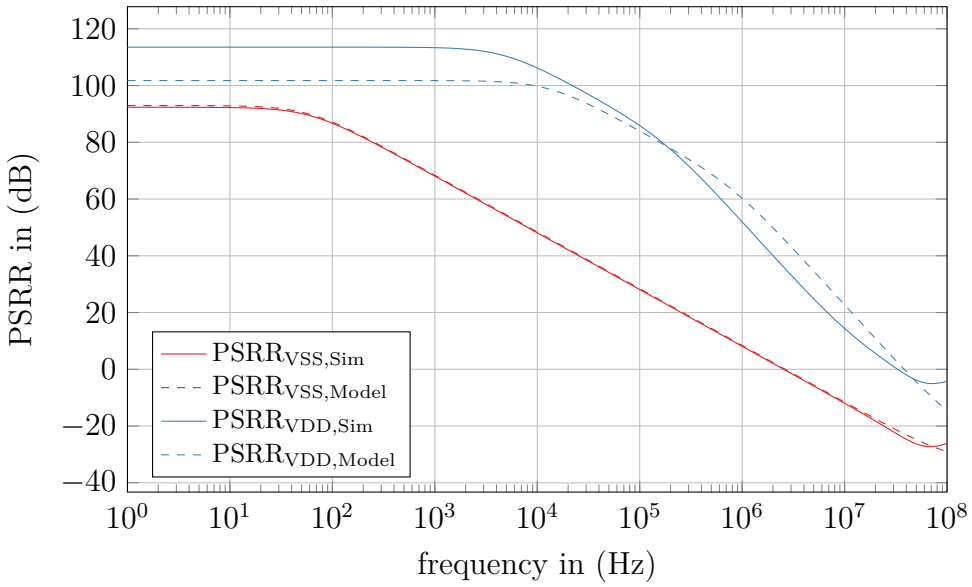


Figure 5.5: Simulated and calculated PSRR of the Miller amplifier

Hereby especially a low channel conductance g_{ds} of the bias transistors is important. Increasing the length of the PMOS bias transistors $M_{5,7,8}$ from 1 µm to 2 µm increases the low-frequency $PSRR_{VDD}$ by 6 dB in simulation and calculation. Vice verse an increase of the transistor length of the NMOS transistors $M_{3,4,6}$ from 700 nm to 1.4 µm increases the low-frequency $PSRR_{VSS}$ by 13 dB in simulation and calculation. By increasing the lengths much further parasitic capacitances are increased and the high-frequency PSRR performance, especially for V_{DD}, is influenced. The usage of nulling resistors reduces the effect of the voltage follower in simulation and calculation as they are placed in the feedback loop. Hereby the gained improvement is reasonable only at very high frequencies beyond 100 MHz. The voltage follower around 4 MHz is only attenuated by a few dB, depending on the resistance of the nulling device, but not avoided.

5.2 Current Buffer Topology

As discussed in the frequency compensation section, the usage of a current buffer topology to decouple the Miller capacitor avoids the formation of the voltage follower. In theory, a smaller Miller capacitor should be required leading to a higher UGF. On the downside, a lower dc gain and higher current consumption is expected.

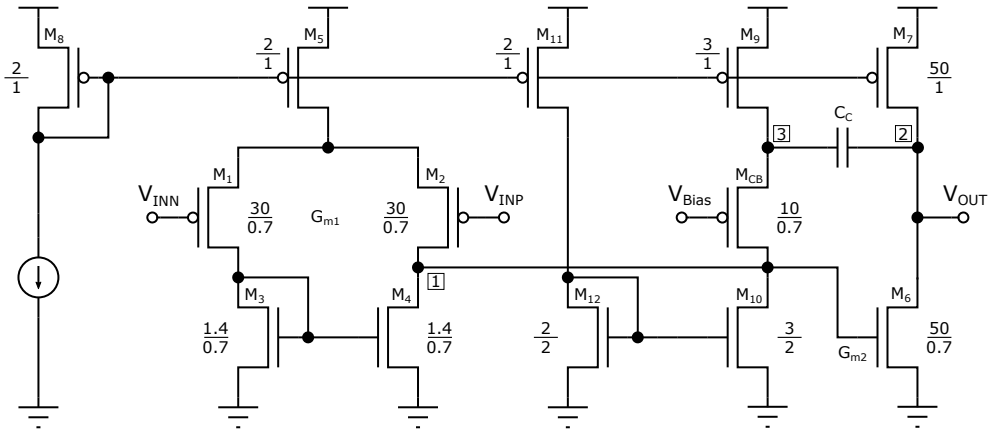


Figure 5.6: Schematic of the current buffer amplifier with the transconductance of the first stage $G_{m1} = 13.3\,\mu S$ and of the second stage $G_{m2} = 542.2\,\mu S$.

5.2.1 Design of a Current Buffer Amplifier

To restrict possible improvements of the PSRR performance on the frequency compensation method, the basic Miller amplifier from Section 4.1.2 was implemented with identical dimensions and only the compensation method was changed. For the design of the current buffer, the methodology presented in [52] considering the internal feedback loop was used. To avoid peaking, Aloisi et al. propose a PM of the internal loop equal to $\tan(\phi_i) = 2$. By choosing the desired PM of the amplifier equal to 70°, ω_{GBW} / ω_{GBWi} can be calculated to

$$\frac{\omega_{GBW}}{\omega_{GBWi}} = \left(\sqrt{1 + \frac{4}{(\tan(\phi_i) - 1)^2 \cdot \tan(\phi)}} - 1\right) \cdot \frac{\tan(\phi_i) \cdot (\tan(\phi_i) - 1)}{2} = 0.567 \quad (5.12)$$

With a current gain of $B = 1$, a rough value for the compensation capacitor C_C can be found to

$$\begin{aligned} C_C &\simeq \frac{1}{B} \cdot \left(\sqrt{\frac{G_{m1} \cdot \omega_{GBWi} \cdot C_{n1} \cdot C_L}{G_{m2} \cdot \omega_{GBW}}} - \frac{C_L}{2 \cdot G_{m2} \cdot R_{n1}}\right) \\ &\simeq \sqrt{\frac{13.3\,\mu S \cdot 114.5\,fF \cdot 10\,pF}{542.4\,\mu S \cdot 0.567}} - \frac{10\,pF}{2 \cdot 542.4\,\mu S \cdot 9.0\,M\Omega} = 221\,fF \end{aligned} \quad (5.13)$$

The needed transconductance $g_{m,CB}$ of the current buffer transistor M_{CB} can then be estimated with

$$g_{m,CB} \simeq \frac{1}{B} \cdot G_{m1} \cdot \tan(\phi_i) \cdot \frac{\omega_{GBWi}}{\omega_{GBW}} = 13.3\,\mu S \cdot 2 \cdot \frac{1}{0.567} = 46.9\,\mu S \quad (5.14)$$

Using the calculated values, a stable amplifier can be designed, however some minor adjustments in simulation were needed to improve the PM. With gm/ID ≈ 10, the

Parameter	$ZL_{80M,10p}$	$ZL_{80k,10p}$	$ZL_{80M,0p}$	$ZL_{80k,0p}$
UGF	7.5 MHz	6.9 MHz	7.4 MHz	7.2 MHz
A_0	83.6 dB	64.5 dB	83.6 dB	64.5 dB
PM	71.3°	64.4°	101.5°	100.3°

Table 5.1: Mean results of Monte Carlo simulations of the current buffer amplifier for different load conditions

current in the current buffer branch had to be chosen higher than the current of the first gain stage in order to achieve the desired value for $g_{m,CB}$. Moreover the additional NMOS current mirror influences the output impedance of the first stage and therefore an increased length of 2 µm was used for those transistors. The schematic with all transistor dimensions is given in Fig. 5.6.

5.2.2 Ac Simulation of the Current Buffer Amplifier

The ac simulation results using 100 Monte Carlo runs are listed in Table 5.1. As expected, the UGF raises thanks to the smaller compensation capacitor in comparison to the Miller amplifier. The dc gain declines as the output resistance of the first stage is influenced by the newly introduced current buffer branch. The behavior under different load situations is less stable than the Miller compensated design and caused by the additional zero. However, the zero is placed beyond UGF and therefore only a slight performance change under varying load variations is visible in Fig. 5.7. As with the Miller amplifier all further simulations are performed with a standard load of 10 MΩ ‖ 10 pF.

5.2.3 Small-Signal Models of the Current Buffer Amplifier

Aloisi et al. indicate in [52] an improved high-frequency PSRR performance by avoiding the voltage follower but also a reduction of the low-frequency PSRR performance. To investigate these properties in the same way as for the Miller amplifier, small-signal models are created for each TF to compare the calculated PSRR with the simulated one.

- V_{IN}: The basic structure for the small-signal model of the current buffer amplifier in Fig. 5.8 is based on the model of the Miller amplifier. However, there is no direct connection by means of the compensation capacitor between both gain nodes. To

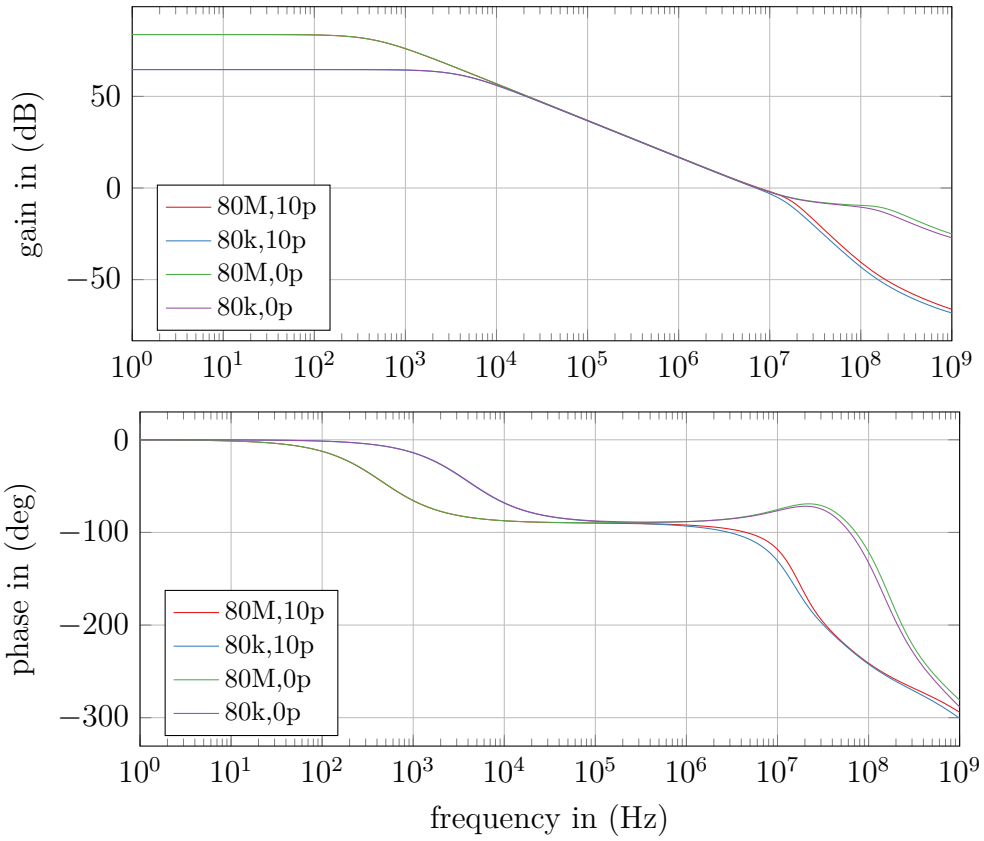


Figure 5.7: Current buffer ac simulation for different load corners

model the common-gate stage, the input resistance seen from the feedback current over C_C is modeled with $1/g_{m,CB}$ [52]. The current flowing through C_C and the input resistance of the common-gate stage is injected into the first gain node and modeled with a voltage-controlled current source. Doing so the current feedback to the first stage gain node is retained while no direct connection between both gain nodes exists. The nodal equations for $TF_{VIN,VOUT}$ are given by

$$V_1 \cdot (1/R_{n1} + sC_{n1}) + V_{IN} \cdot g_{m2} - V_{OUT} \cdot g_{m1} - V_3 \cdot g_{m,CB} = 0 \tag{5.15}$$

$$V_{OUT} \cdot (1/R_{n2} + sC_{n2,C}) + V_1 \cdot g_{m6} - V_3 \cdot sC_C = 0 \tag{5.16}$$

$$V_3 \cdot (g_{m,CB} + s \cdot C_C) - V_{OUT} \cdot sC_C = 0 \tag{5.17}$$

with $R_{n1} = r_{ds2} \parallel r_{ds4} \parallel r_{ds10}$, $R_{n2} = r_{ds6} \parallel r_{ds7} \parallel R_L$ and C_{n1} and C_{n2} as the output capacitances of the respective stages. Solving the equations for V_{OUT}/V_{IN} gives

$$\frac{V_{OUT}}{V_{IN}} = \frac{g_{m2} \cdot g_{m6}}{GDS2 \cdot (sC_C \cdot GMCB + GOUT) + g_{m6} \cdot GM1} \tag{5.18}$$

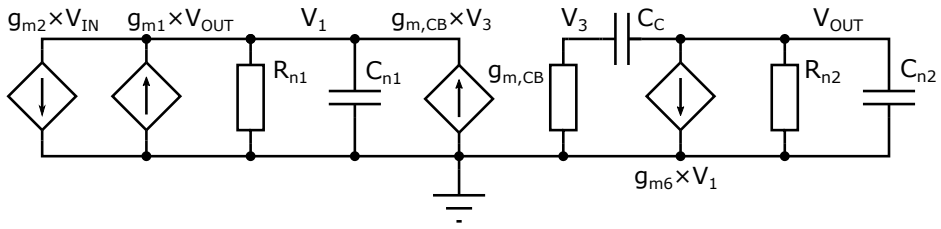


Figure 5.8: Small-signal model for $TF_{VIN,VOUT}$ of the current buffer amplifier

with

$$\begin{aligned} GDS2 &= g_{ds2,4,10} + sC_{n1}, \\ GOUT &= g_{ds6,7} + 1/R_L + sC_{n2,C}, \\ GMCB &= sC_C/(g_{m,CB} + sC_C), \\ GM1 &= g_{m1} + g_{m,CB} \cdot GMCB. \end{aligned}$$

- V_{SS}: By splitting up all paths between V_{DD} and V_{SS}, the small-signal model for $TF_{VSS,VOUT}$ in Fig. 5.9 is designed. Special attention needs to be given to the connection of the gate from the common-gate transistor. When the gate is connected to V_{SS}, no stable ac ground is ensured for the compensation capacitor and the voltage follower is not avoided. Therefore the gate must be connected to a noise-free voltage, for example in the middle of the power supply range. As for the Miller amplifier, the CLM effect of the input transistor M_1 is taken into account. However, also M_{12} is connected in diode configuration and the CLM effect of transistor M_{11} produces a disturbance current similar to the calculated one in (5.5). Therefore also the bias systems influence the PSRR even if power supply independent biasing is assumed. The current mirror gain factor between M_{10} and M_{12} amplifies the offset current even further and needs to be considered in the calculations. The nodal equations for the $TF_{VSS,VOUT}$ model are given by

$$V_1 \cdot (g_{ds2,4,10} + sC_{n1,n1'}) - V_{SS} \cdot (g_{ds1,4,10,11} + sC_{n1}) - V_{OUT} \cdot g_{m1} - V_3 \cdot g_{m,CB} = 0 \quad (5.19)$$

$$V_{OUT} \cdot (g_{ds6,7} + 1/R_L + sC_{n2,C}) + V_1 \cdot g_{m6} - V_{SS} \cdot (g_{ds6} + g_{m6} + sC_{n2}) - V_3 \cdot sC_C = 0 \quad (5.20)$$

$$V_3 \cdot (g_{m,CB} + s \cdot C_C) - V_{OUT} \cdot sC_C = 0 \quad (5.21)$$

were C_{n1} and $C_{n1'}$ include the output capacitances of the first stage towards V_{SS} and V_{DD} and C_{n2} the output capacitances of the second stage towards V_{SS}. Solving the equations for V_{OUT}/V_{SS} gives

$$\frac{V_{OUT}}{V_{SS}} = \frac{GM6 \cdot GDS2 - g_{m6} \cdot GDS1}{GDS2 \cdot (GOUT + sC_C \cdot GMCB) + g_{m6} \cdot GM1} \quad (5.22)$$

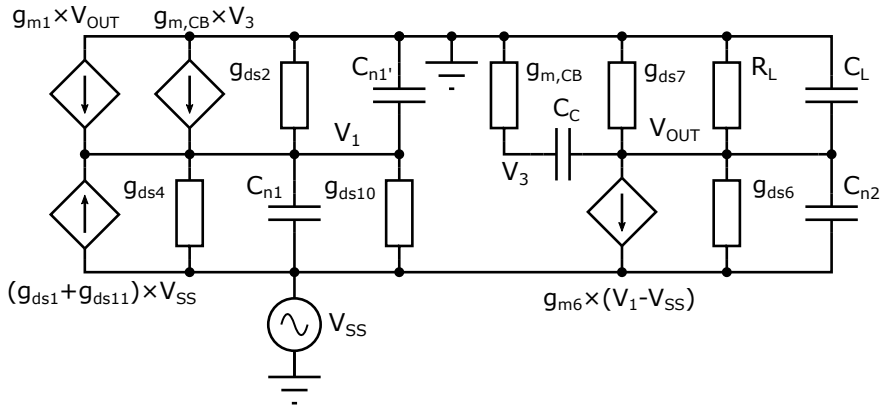


Figure 5.9: Small-signal model for $TF_{VSS,VOUT}$ of the current buffer amplifier

with

$$\begin{aligned} GDS1 &= g_{ds1,4,10,11} + sC_{n1}, \\ GDS2 &= g_{ds2,4,10} + sC_{n1,n1'}, \\ GOUT &= g_{ds6,7} + 1/R_L + sC_{n2,C}, \\ GMCB &= sC_C/(g_{m,CB} + sC_C), \\ GM1 &= g_{m1} + g_{m,CB} \cdot GMCB, \\ GM6 &= g_{m6} + g_{ds6} + sC_{n2}. \end{aligned}$$

- V_{DD}: The small-signal model for $TF_{VDD,VOUT}$ in Fig. 5.10 is more complicated to design as parasitic capacitances play a greater role due to fewer dominant connections from V_{DD} to the outputs. In contrast to both small-signal models beforehand, transistor M_9 is taken into account too as disturbances from V_{DD} can couple over. These disturbances influence the feedback current, especially at higher currents, when the parasitic capacitances of M_9 have a low impedance. The nodal equations for the $TF_{VDD,VOUT}$ model are given by

$$V_1 \cdot (1/R_{n1} + sC_{n1,n1'}) - V_{DD} \cdot sC_{n1'} - V_{OUT} \cdot g_{m1} - V_3 \cdot g_{m,CB} = 0 \quad (5.23)$$

$$V_{OUT} \cdot (1/R_{n2} + g_{ds7} + sC_{n2,n2',C}) - V_{DD} \cdot (g_{ds7} + sC_{n2'}) + V_1 \cdot g_{m6} - V_3 \cdot sC_C = 0 \quad (5.24)$$

$$V_3 \cdot (g_{ds9} + g_{m,CB} + sC_{n3',C}) - V_{DD} \cdot (g_{ds9} + sC_{n3'}) - V_{OUT} \cdot sC_C = 0 \quad (5.25)$$

with $R_{n1} = r_{ds2} \parallel r_{ds4} \parallel r_{ds10}$ and $R_{n2} = r_{ds6} \parallel R_L$. C_{n1} and $C_{n1'}$ include the output capacitances of the first stage towards V_{SS} and V_{DD}, and C_{n2} and $C_{n2'}$ the output capacitances of the second stage towards V_{SS} and V_{DD}. The capacitance from the current buffer stage towards V_{DD} is modeled in $C_{n3'}$. Solving the equations for V_{OUT}/V_{DD} gives

$$\frac{V_{OUT}}{V_{DD}} = \frac{GMCB \cdot (GDS7 - g_{m6} \cdot GM6) + sC_C \cdot GDS9}{GMCB \cdot (GOUT + g_{m6} \cdot GM1) - (sC_C)^2} \quad (5.26)$$

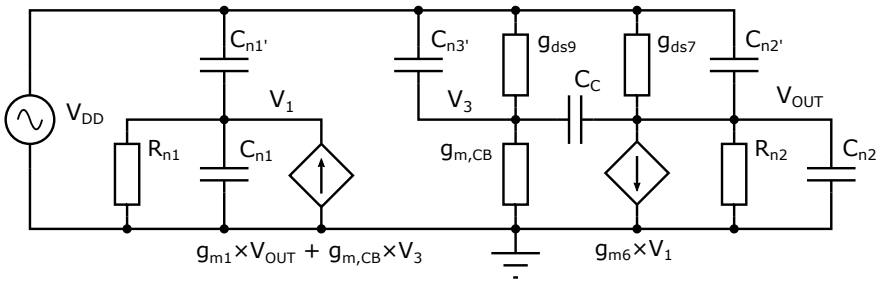


Figure 5.10: Small-signal model for $\mathrm{TF_{VDD,VOUT}}$ of the current buffer amplifier

with

$$
\begin{aligned}
GDS2 &= g_{ds2,4,10} + sC_{n1,n1'},\\
GDS7 &= g_{ds7} + sC_{n2'},\\
GDS9 &= g_{ds9} + sC_{n3'},\\
GMCB &= g_{ds9} + g_{m,CB} + sC_{n3',C},\\
GOUT &= g_{ds6,7} + 1/R_L + sC_{n2,n2',C},\\
GM1 &= g_{m1}/GDS2 + g_{m,CB} \cdot sC_C/(GDS2 \cdot GMCB),\\
GM6 &= sC_{n1'}/GDS2 + g_{m,CB} \cdot GDS9/(GDS2 \cdot GMCB).
\end{aligned}
$$

5.2.4 PSRR Simulation of the Current Buffer Amplifier

The simulated and calculated PSRR of both power supply rails is given in Fig. 5.11. As for the PSRR figures of the Miller amplifier, the $\mathrm{PSRR_{VSS}}$ figures match better than the figures for $\mathrm{PSRR_{VDD}}$. A comparison of the current buffer results to the PSRR figures of the Miller amplifier clearly show a huge improvement around medium frequencies as the voltage follower at the output stage is avoided. However, for lower frequencies, the $\mathrm{PSRR_{VSS}}$ from the current buffer amplifier is worse than the $\mathrm{PSRR_{VSS}}$ of the Miller amplifier as $\mathrm{M_{10}}$ introduces a new path from $\mathrm{V_{SS}}$ to the output of the first stage. Also an additional NMOS bias system is present. This is even more visible in the $\mathrm{PSRR_{VDD}}$ figures where the Miller amplifier results in overall better PSRR performance. While the disturbances in the first stage still are attenuated with good matching of the input pair, $\mathrm{M_7}$ and $\mathrm{M_9}$ double the direct connections from $\mathrm{V_{DD}}$ to the output in comparison to the Miller amplifier where only $\mathrm{M_7}$ is presented.

To improve the PSRR performance, the same criteria as for the Miller amplifier can be named. As the current buffer topology introduces an additional direct branch, special care needs to be taken to guarantee a low $\mathrm{g_{ds}}$ of the bias transistors.

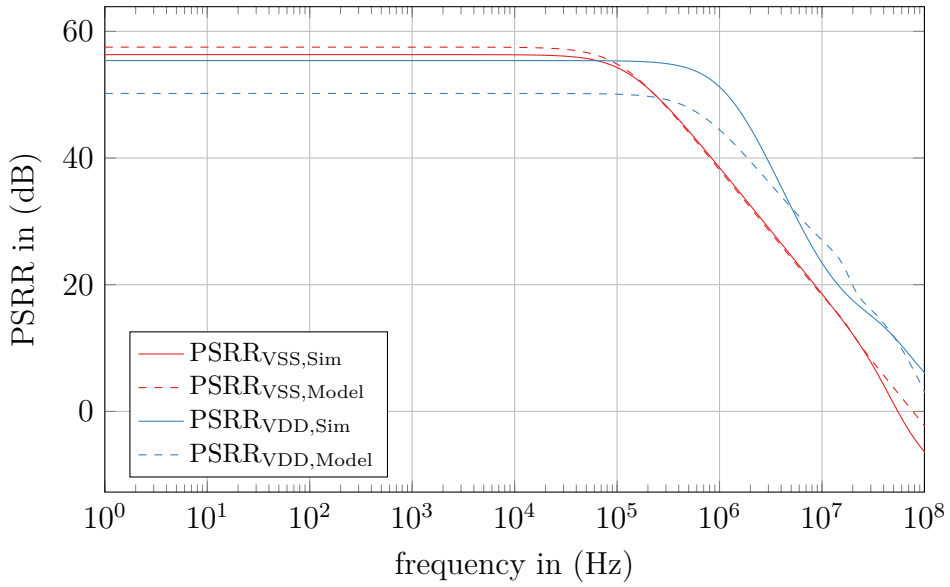


Figure 5.11: Simulated and calculated PSRR of the current buffer amplifier

5.3 No-Capacitor Feedforward Topology

Another topology that avoids the voltage follower at the second stage is the no-capacitor feedforward (NCFF) topology [55]. As introduced in Section 3.3.4, an uncompensated two-stage amplifier is used for good low frequency performance and combined with a fast single-stage amplifier for high frequencies. In the frequency range of interest, the single-stage amplifier should be dominant and therefore superior PSRR performance is expected as very few connections towards the power supply rails are present.

5.3.1 Design of a NCFF Amplifier

The fundamental equation for the design of a NCFF compensation topology is (3.14) to calculate the LHP zero of the feedforward path. By removing the Miller capacitor from the basic Miller amplifier in Fig. 4.1, the required G_{m3} of the feedforward single-stage amplifier can be found with

$$G_{m3} \approx \frac{G_{m1} \cdot G_{m2}}{C_{n1} \cdot z_1} = \frac{13.3\,\mu\text{S} \cdot 542.4\,\mu\text{S}}{114.5\,\text{fF} \cdot 7.48\,\text{MHz}} = 8.4\,\text{mS} \tag{5.27}$$

At this point it is clear that in contrast to the current buffer topology a redesign of the two-stage amplifier is needed. With gm/ID ≈ 10, the required current lies in the range of 800 µA and is therefore not suitable for the low-power requirements. In order

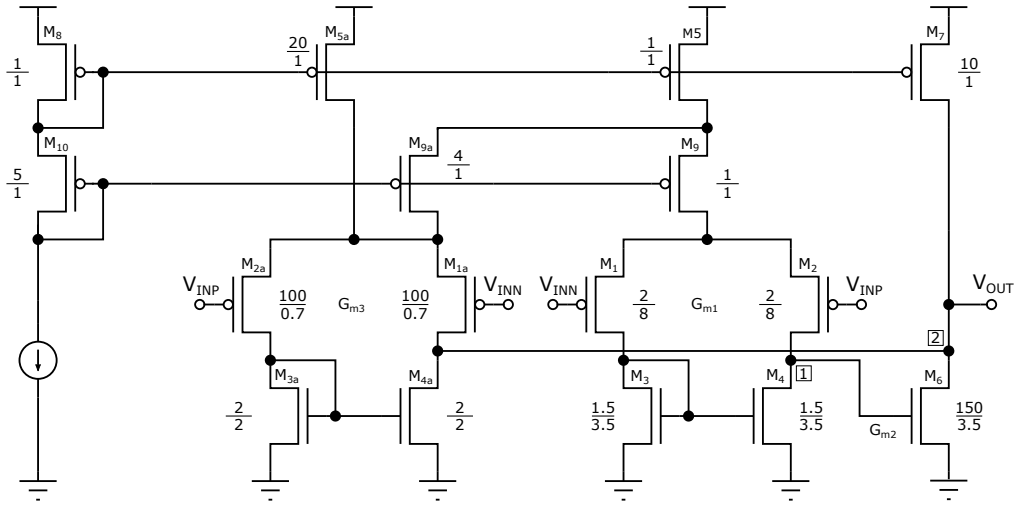


Figure 5.12: Schematic of the NCFF amplifier with the transconductance of the first stage $G_{m1} = 1.4\,\mu S$, of the second stage $G_{m2} = 200\,\mu S$ and of the feedforward stage $G_{m3} = 242\,\mu S$.

to achieve a power consumption below 100 µW, different design changes can be taken to decrease G_{m3}:

- Reducing G_{m1} or G_{m2}
- Increasing C_{n1} with bigger transistors or additional capacitors.
- Increasing the position of z_1.

In order to stick to the low-power application, the transconductance of the first stage was reduced by lowering the bias current of the first stage to a few 100 nA. The decrease of the bias current was possible as no slew rate requirements were considered in the amplifier specifications. To increase G_{m3}, the current in the feedforward stage I_{FF} should be as high as possible. The maximal allowed current I_{FF} can be determined by the given amplifier specifications and the currents in the two-stage OpAmp:

$$I_{FF} = \frac{P_{MAX}}{V_{DD}} - I_{1,Stage} - I_{2,Stage} \tag{5.28}$$

As the PMOS mirror factor between the bias current of the first stage and the bias current of the feedforward stage is increased to a factor of 115, a new bias system is required. In order to reduce additional current consumption, a second PMOS current mirror was used instead of an auxiliary NMOS current mirror. The second PMOS current mirror limits the current of the first stage and injects the residual current into the feedforward stage as indicated in Fig. 5.12.

With the usage of the M_1, M_2 and M_6 transistor dimensions from the basic Miller amplifier in Fig. 4.1 for both the two-stage OpAmp and single-stage OTA transistors, a value for the required parasitic capacitance C_{n1} can be estimated from simulation:

$$C_{n1} \approx \frac{G_{m1} \cdot G_{m2}}{G_{m3} \cdot z_1} \approx \frac{2.8\,\mu S \cdot 220\,\mu S}{185\,\mu S \cdot 7.48\,MHz} = 445\,fF \tag{5.29}$$

Capacitance C_{n1} is hereby mainly formed by $C_{GS,GB}$ from M_6 and $C_{DB,DS}$ from M_2 and M_4. Because C_{GS} and C_{GB} are proportional to the transistor length [3], transistor M_6 was designed with a higher length to increase C_{n1} without influencing C_{DG} and the used amplifier area extensively. However, in order to satisfy equal current density in the NMOS current mirror transistors, M_6 is rather large caused by the high current gain factor between both stages. Therefore also G_{m2} is increased and a trade-off between C_{n1} and G_{m2} must be found. A reduction of G_{m2} with lower bias current is not possible as a minimal drive current of 10 µA is required by specifications. One degree of freedom lies in the design of the input stage where long transistors were used. In order to stick to the valid transistor-model regions, M_1 and M_2 are designed as series connection of two transistors. The final dimensions gained from optimization in simulation are presented in Fig. 5.12.

5.3.2 Ac Simulation of the NCFF Amplifier

Because of the compensation of the non-dominant pole with a LHP zero, a constant ac performance throughout all load conditions is not possible. Although a stable behavior is achieved at all load conditions, a pure ohmic load increases the UGF considerably and produces a mismatched pole-zero doublet as considered beforehand in Fig. 3.9. Therefore, good ac performance is possible only at a specific load as calculated in (3.14). Nevertheless, the results of the Monte Carlo simulation are given in Table 5.2 and the ac performance in Fig. 5.13.

For the load of 10 MΩ ∥ 10 pF, pole-zero compensation is achieved with the calculated G_{m3}. It must be mentioned that the performance for the standard load is limited by the current consumption. With a higher current a higher UGF could by achieved as the speed is limited by the single-stage OTA.

5.3.3 Small-Signal Models of the NCFF Amplifier

Until now, no direct PSRR and EMI analysis of the NCFF topology were performed in the literature. Caused by the no-capacitor construction and the avoiding of the supply

Parameter	$ZL_{80M,10p}$	$ZL_{80k,10p}$	$ZL_{80M,0p}$	$ZL_{80k,0p}$
UGF	3.6 MHz	3.7 MHz	156.2 MHz	152.6 MHz
A_0	92.4 dB	47.8 dB	92.4 dB	47.8 dB
PM	88.7°	91.9°	53.0°	55.2°

Table 5.2: Mean results of Monte Carlo simulations of the NCFF amplifier for different load conditions

rail voltage follower, the NCFF amplifier should offer improved PSRR performance. To verify this assumption, small-signal models are constructed and compared with simulation results as carried out for the other topologies.

- V_{IN}: The basic topology of the small-signal model for $TF_{VIN,VOUT}$ in Fig. 5.14 consists of the first stage of the OpAmp and the second stage in parallel to the single-stage, feedforward connected OTA. As no compensation capacitor is present, both small-signal stages are separated and no direct interaction takes place. To simplify the nodal equations, the small-signal values from the second stage of the OpAmp and from the feedforward stage are summarized in R_{n2}, $R_{n2'}$, C_{n2} and $C_{n2'}$. In order to distinguish the feedforward stage values from the two-stage amplifier values in the TF calculations, the small-signal values from the single-stage feedforward OTA are marked with an additional subscript. The nodal equations are given by

$$V_1 \cdot (1/R_{n1} + sC_{n1}) + V_{IN} \cdot g_{m2} - V_{OUT} \cdot g_{m1} = 0 \tag{5.30}$$
$$V_{OUT} \cdot (1/R_{n2} + sC_{n2} + g_{m1a}) + V_1 \cdot g_{m6} - V_{IN} \cdot g_{m2a} = 0 \tag{5.31}$$

  with $R_{n1} = r_{ds2} \parallel r_{ds4}$, $R_{n2} = r_{ds6} \parallel r_{ds7} \parallel R_L \parallel r_{ds1a} \parallel r_{ds4a}$. C_{n1} includes the output capacitances of the first stage and C_{n2} the output capacitances of the second stage and feedforward stage. Solving the equations for V_{OUT}/V_{IN} gives

$$\frac{V_{OUT}}{V_{IN}} = \frac{g_{m2} \cdot g_{m6} + GDS2 \cdot g_{m2a}}{g_{m1} \cdot g_{m6} + GDS2 \cdot (GOUT + g_{m1a})} \tag{5.32}$$

  with

$$GDS2 = g_{ds2,4} + sC_{n1},$$
$$GOUT = g_{ds2a,4a,6,7} + 1/R_L + sC_{n2}.$$

- V_{SS}: The small-signal model for $TF_{VSS,VOUT}$ is given in Fig. 5.15. The current injection through the conductance of the input transistor is used also for the single-stage OTA as seen in the Miller and current buffer amplifier.

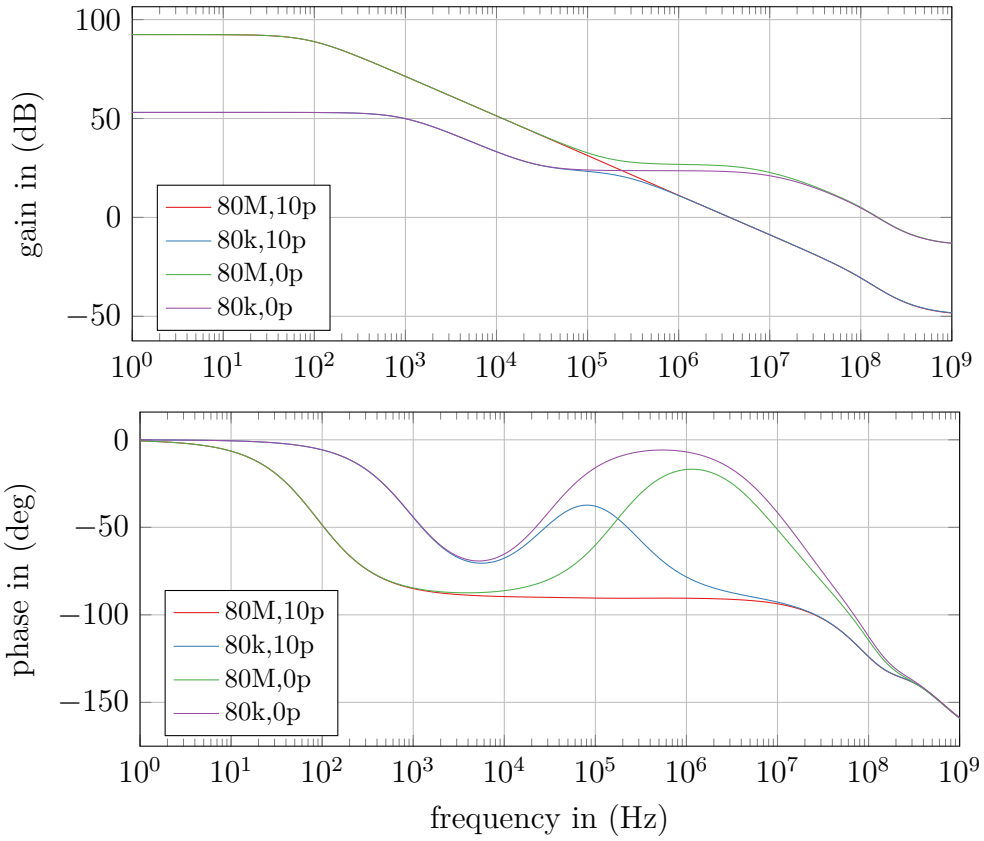


Figure 5.13: NCFF ac simulation for different load corners. The ac performance of the standard load equals the Bode plot for 80 MΩ ∥ 10 pF.

The nodal equations of the NCFF topology for $\mathrm{TF_{VSS,VOUT}}$ are given by

$$V_1 \cdot (g_{ds2,4} + sC_{n1,n1'}) - V_{SS} \cdot (g_{ds1,4} + sC_{n1}) - V_{OUT} \cdot g_{m1} = 0 \tag{5.33}$$

$$V_{OUT} \cdot (1/R_{n2} + 1/R_{n2'} + g_{m1a} + sC_{n2,n2'}) + V_1 \cdot g_{m6} - V_{SS} \cdot (1/R_{n2} + g_{ds2a} + g_{m6} + sC_{n2}) = 0 \tag{5.34}$$

with $\mathrm{R_{n2}} = \mathrm{r_{ds6}} \parallel \mathrm{r_{ds4a}}$ and $\mathrm{R_{n2'}} = \mathrm{r_{ds7}} \parallel \mathrm{r_{ds1a}}$. $\mathrm{C_{n1}}$ and $\mathrm{C_{n1'}}$ include the output capacitances of the first stage towards $\mathrm{V_{SS}}$ and $\mathrm{V_{DD}}$, $\mathrm{C_{n2}}$ and $\mathrm{C_{n2'}}$ the output capacitances of the second and feedforward stage towards $\mathrm{V_{SS}}$ and $\mathrm{V_{DD}}$. Solving the equations for $\mathrm{V_{OUT}/V_{SS}}$ gives

$$\frac{V_{OUT}}{V_{SS}} = \frac{GDS2 \cdot GDS6 - g_{m6} \cdot GDS1}{GDS2 \cdot GOUT + g_{m1} \cdot g_{m6}} \tag{5.35}$$

with

$$\begin{aligned} GDS1 &= g_{ds1,4} + sC_{n1}, \\ GDS2 &= g_{ds2,4} + sC_{n1,n1'}, \\ GDS6 &= g_{ds2a,4a,6} + g_{m6} + sC_{n2}, \\ GOUT &= g_{ds1a,4a,6,7} + g_{m1a} + 1/R_L + sC_{n2,n2'}. \end{aligned}$$

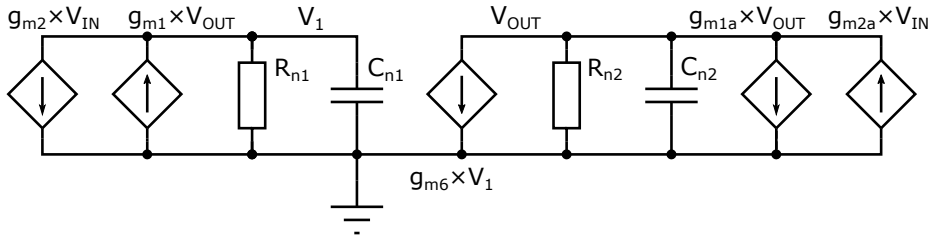


Figure 5.14: Small-signal model for $TF_{VIN,VOUT}$ of the NCFF amplifier

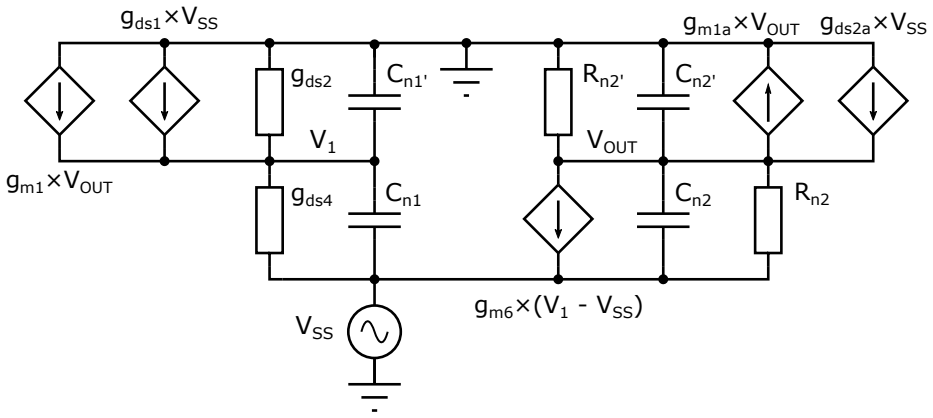


Figure 5.15: Small-signal model for $TF_{VSS,VOUT}$ of the NCFF amplifier

- V_{DD}: Considering the small-signal model for $TF_{VDD,VOUT}$ in Fig. 5.16, the new bias system increases the impedance between V_{DD} and the first OpAmp stage. Fault currents over M_5 are split up between both input stages and attenuated by the matching of the input transistors. Considering capacitive coupling between V_{DD} and the output of the first stage, the resulting capacitance is a series connection between $C_{DS,\,DB}$ of M_2 and C_{DB} of M_9. As M_9 is quite small, the resulting parasitic capacitance is in the order of a few 100 aF and can therefore be neglected. For the Miller and current buffer amplifiers, bias transistor M_5 had bigger dimensions and the capacitance was formed by $C_{DS,\,DB}$ in the order of a few fF and was therefore included. The nodal equations for the $TF_{VDD,VOUT}$ are given by

$$V_1 \cdot (1/R_{n1} + sC_{n1}) - V_{OUT} \cdot g_{m1} = 0 \tag{5.36}$$

$$V_{OUT} \cdot (1/R_{n2} + g_{ds7} + g_{m1a} + sC_{n2,n2'}) - V_{DD} \cdot sC_{n2'} + V_1 \cdot g_{m6} = 0 \tag{5.37}$$

with $R_{n1} = r_{ds2} \parallel r_{ds4}$ and $R_{n2} = r_{ds6} \parallel r_{ds1a} \parallel r_{ds4a}$. C_{n1} includes the output capacitances of the first stage towards V_{SS}, C_{n2} and $C_{n2'}$ the output capacitances of the second and feedforward stage towards V_{SS} and V_{DD}. Solving the equations for V_{OUT}/V_{DD} gives

$$\frac{V_{OUT}}{V_{DD}} = \frac{GDS2 \cdot GDS7}{GDS2 \cdot GOUT + g_{m1} \cdot g_{m6}} \tag{5.38}$$

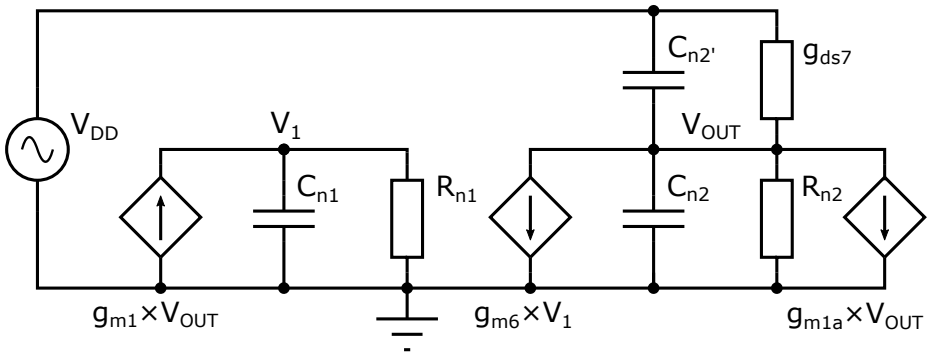


Figure 5.16: Small-signal model for $\mathrm{TF_{VDD,VOUT}}$ of the NCFF amplifier

with

$$GDS2 = g_{ds2,4} + sC_{n1},$$
$$GDS7 = g_{ds7} + sC_{n2'},$$
$$GOUT = g_{ds1a,4a,6,7} + g_{m1a} + 1/R_L + sC_{n2,n2'}.$$

5.3.4 PSRR Simulation of the NCFF Amplifier

Due to the simple topology, the NCFF amplifier offers high PSRR on both supply rails as indicated in Fig. 5.17. Hereby the advantage is not gained from the new bias system, since parasitic capacitances from $\mathrm{V_{DD}}$ towards $\mathrm{V_1}$ of the Miller and current buffer variants were just slightly bigger than the capacitances of the NCFF amplifier. This is expressed also in the high correlation between the $\mathrm{PSRR_{VDD}}$ from the Miller amplifier and the $\mathrm{PSRR_{VDD}}$ from the NCFF amplifier. The $\mathrm{PSRR_{VDD}}$ of a single-stage OTA is considered as high and therefore only the two-stage OpAmp contributes to the PSRR performance. Because of that, the same design criteria as for the Miller amplifier in Section 5.1.3 apply. Considering mismatch between simulation and model, the $\mathrm{PSRR_{VSS}}$ figures offer high accordance, while the offset of the $\mathrm{PSRR_{VDD}}$ figures lies in the same range as for the other topologies. Hereby the same restrictions as for the model of the Miller amplifier including the virtual ground concept are assumed.

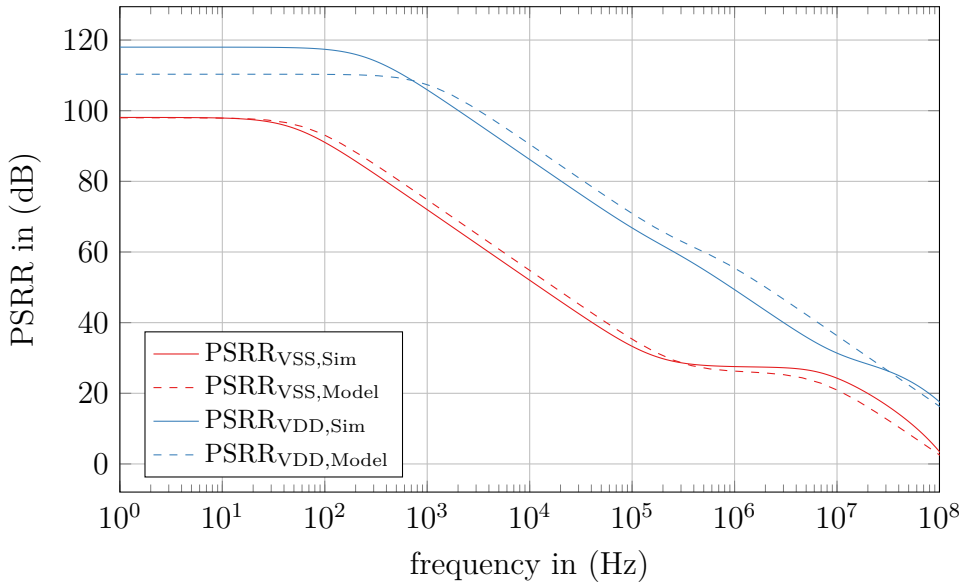


Figure 5.17: Simulated and calculated PSRR of the NCFF amplifier

5.4 Comparison Amplifier Topologies

As now all three amplifier topologies are investigated, a comparison between them is possible in order to choose the best topology for a given application. With the limited power consumption and the same assumed application for all three topologies, performance changes are limited to the frequency compensation methods.

5.4.1 Ac Performance

Comparing the dynamic performance of the topologies in Fig. 5.18, the current buffer offers the highest UGF with an improvement in the order of three in comparison to the Miller amplifier. However, because of the low output impedance of the first stage, the dc gain is low. Considering speed and UGF, the NCFF amplifier is placed in between both topologies. The UGF of the NCFF is hereby determined by the single-stage OTA and the current consumption.

Considering dc gain, the NCFF offers slightly higher gain than the Miller amplifier. The reason for higher gain is the increased output resistance/capacitance of the first stage which has been carried out to achieve pole-zero compensation. With identical dimensions of both input stages, identical gains are expected. Concerning stability, the simulated PM for both, the Miller and current buffer amplifier, is around 70° while the

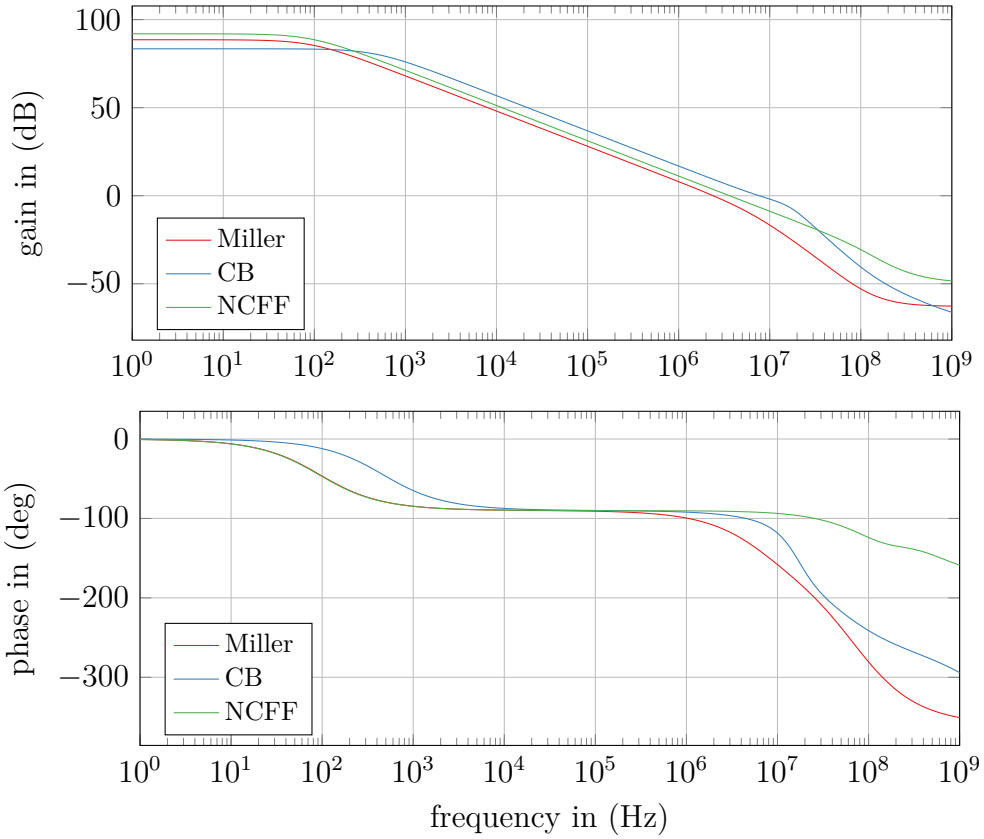


Figure 5.18: Comparison of the ac performance of all three amplifier topologies

PM of the NCFF amplifier is determined by the OTA with around 90°. However, as seen in [47], a PM of 70° theoretically offers faster settling than a PM of 90°. As simulations of the NCFF amplifier showed a higher slew rate than in the Miller amplifier is achieved. This can be explained with the Miller capacitance which needs to be charged in the Miller amplifier and therefore limits the slew rate. The effect of the theoretical slower settling behavior in the NCFF amplifier is therefore counteracted with the higher slew rate. Considering load variations, the NCFF topology clearly shows weak stability behavior caused by the pole-zero compensation. Here the Miller topology without nulling devices clearly provides the best load-variations performance while the current buffer amplifier is placed in between the two other topologies regarding load changes.

5.4.2 PSRR Performance

To compare the PSRR performance of all topologies, all PSRR figures for V_{DD} and V_{SS} are plotted together in Fig. 5.19. As already discussed, the poor low-frequency PSRR performance of the current buffer amplifier stands out in comparison to the

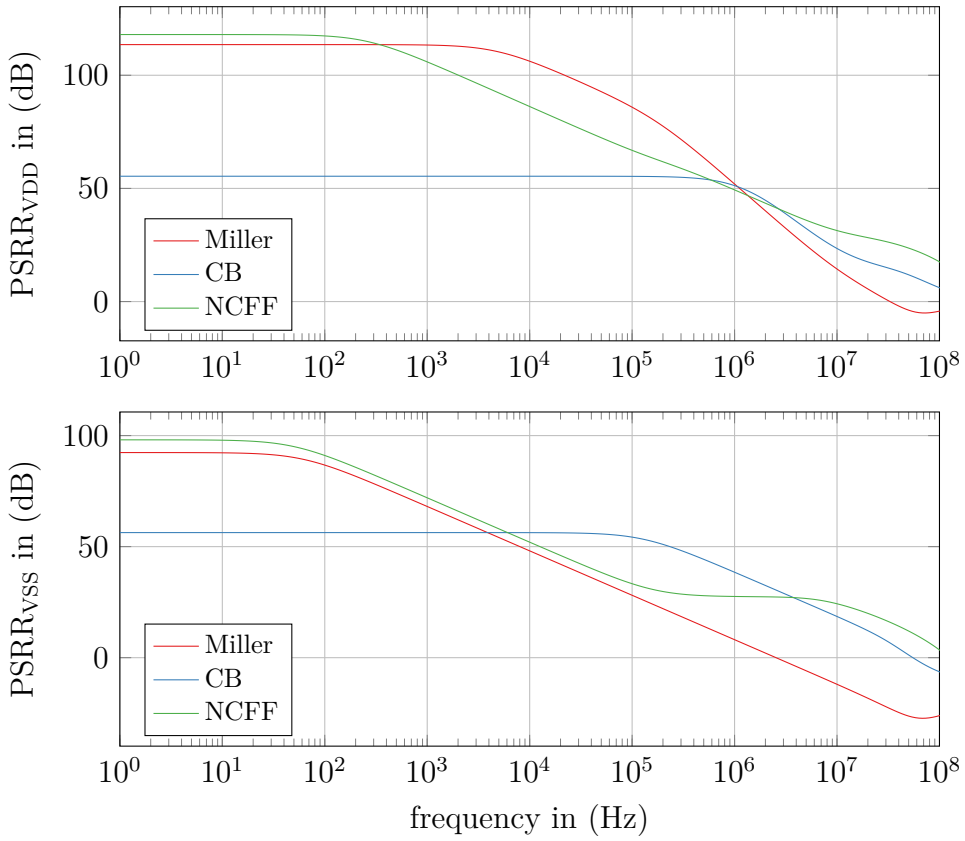


Figure 5.19: Comparison of the PSRR performance of all three amplifier topologies

other two topologies which both reach dc values above 100 dB. Because of their pretty equal basic structure, good correlation for low-frequency operation is given for both supply rails. However, at higher frequencies the often considered voltage follower decreases the $PSRR_{VSS}$ of the Miller amplifier and both other topologies clearly offer better performances. This is also visible in the simulation results for the critical NFC frequencies of 6.78 MHz and 13.56 MHz in Table 5.3. Here clearly the NCFF topology sticks out on both frequencies and supply lines with improvements in the order of 35 dB for V_{SS} and 15 dB for V_{DD} in comparison to the Miller amplifier. However, if the concept from Saeckinger, Goette and Guggenbuehl in [6] considering the sum of the

Topology	6.78 MHz		13.56 MHz	
	V_{DD}	V_{SS}	V_{DD}	V_{SS}
Miller	20.0 dB	−8.6 dB	10.3 dB	−14.7 dB
CB	28.1 dB	21.9 dB	20.5 dB	15.9 dB
NCFF	33.8 dB	25.9 dB	29.9 dB	22.6 dB

Table 5.3: Evaluation of the simulated PSRR values at the critical NFC frequencies

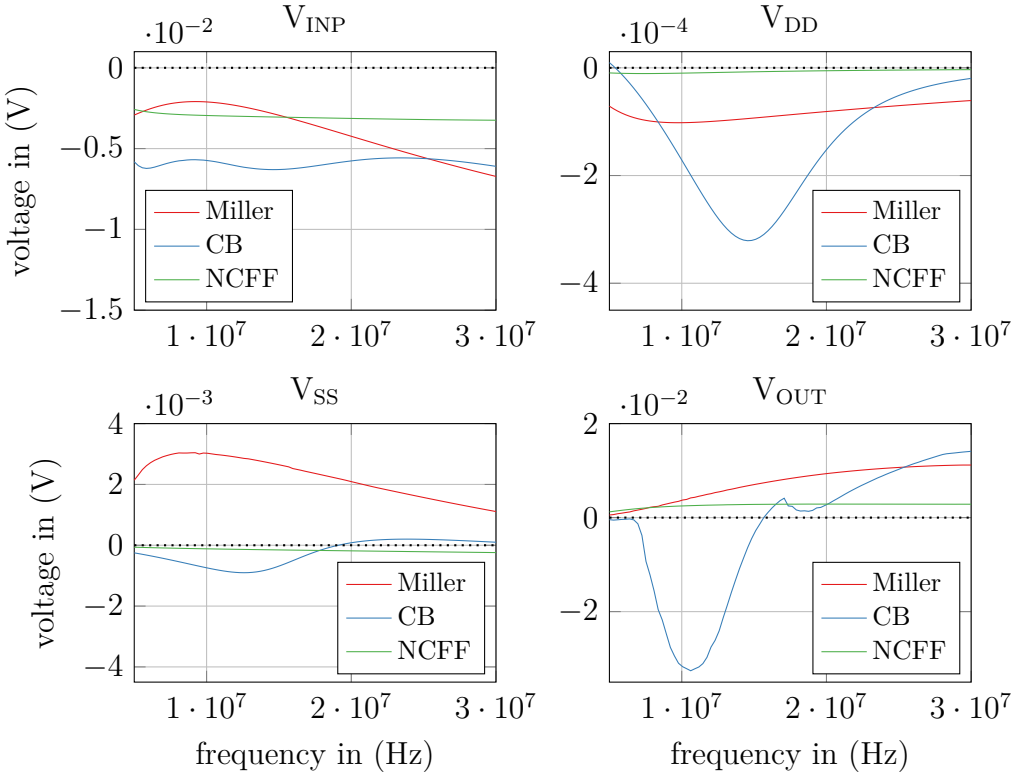


Figure 5.20: EMI-induced offset simulation results for the amplifier topologies

parasitic gains is valid, a lower A_{VDD} and A_{VSS} implies a higher A_{CM} if no additional pins are added. Simulations confirmed the thesis in [6] as the NCFF amplifier has a slightly higher A_{CM} than the Miller amplifier. It has do be mentioned once again that a high PSRR is not per se linked to a high immunity against EMI for all frequencies. It is however a good indicator how efficiently disturbances from the supply rail can reach the amplifier output. Therefore more pins are penetrated at the same time by EMI if the PSRR is low.

5.4.3 EMI Performance

In order to compare the EMI performance of the amplifier topologies, the TBs from Section 4.2 were used. As for the EMI countermeasures a pure sinusoidal signal with an amplitude of 100 mV in the range between 5 MHz and 30 MHz was used as injection signal. The resulting simulated output dc shift for all three amplifiers is plotted in Fig. 5.20. As one can see, the NCFF topology offers higher EMI robustness than the other two topologies. Especially for V_{DD} and V_{SS} a high EMI robustness is observable. The simulated V_{DD} output dc offset at 13.56 MHz is with −8.3 µV a few orders lower than

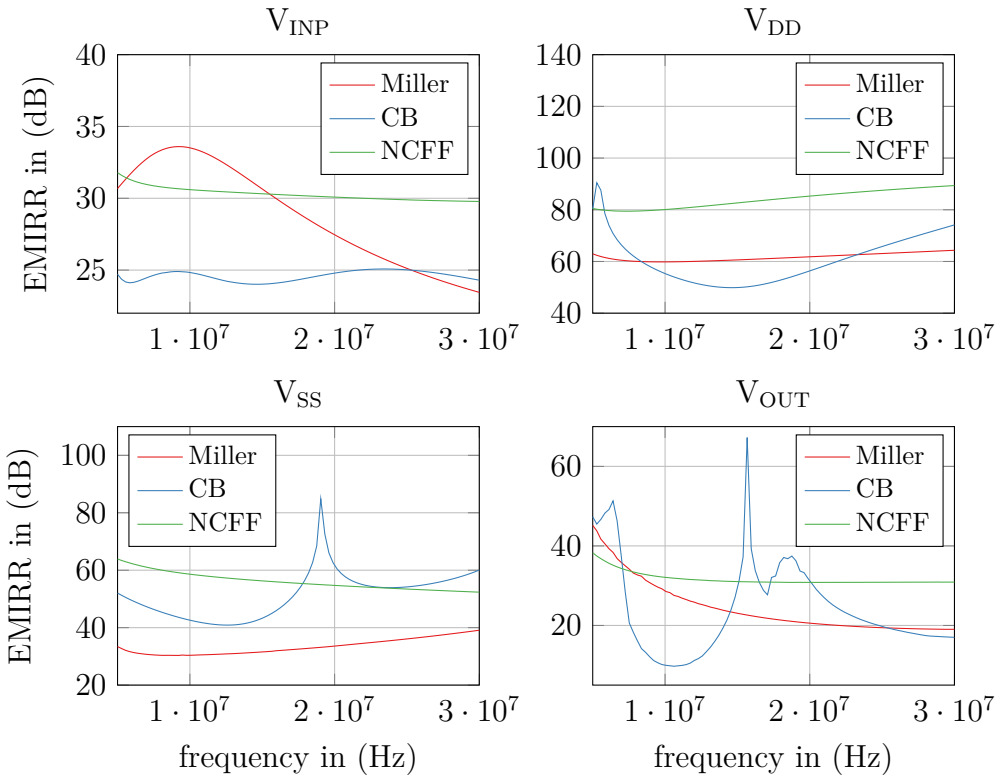


Figure 5.21: EMI-induced offset simulation results for the amplifier topologies in EMIRR

the offset of the Miller amplifier with −96 µV. To put the improvement in comparable numbers, the simulated EMIRR is plotted in Fig. 5.21. Doing so, the advantages in this FOM clearly stand out as it is much easier to compare the higher EMI robustness of the NCFF amplifier with the other topologies. One mentioned drawback of the EMIRR lies in the loss of the voltage sign. This is visible in Fig. 5.21 in the current buffer plots for V_{SS} and V_{OUT} were EMIRR drastically rises during sign changes of the dc shift. Especially for V_{OUT} around 18 MHz inconsistent values determined by the resolution of the frequency sweep are produced. Therefore a combination of the pure dc output shift in volt and the EMIRR figure in dB is advised.

A possible explanation for the higher EMI robustness of the NCFF topology lies in the symmetric slew rate with SR_+ equal to 2.2 MV s^{-1} and SR_- equal to 2.3 MV s^{-1}. The designed Miller amplifier is with $SR_+ = 1.1\,\text{MV s}^{-1}$ and $SR_- = 1.2\,\text{MV s}^{-1}$ also quite symmetric, but slower than the NCFF amplifier. Therefore it is much more likely that distorted signals are accumulated at the output of the amplifier which produces a dc shift. The current buffer topology is with $SR_+ = 2.4\,\text{MV s}^{-1}$ and $SR_- = 3.3\,\text{MV s}^{-1}$ even faster than the NCFF, but unsymmetrical and therefore very susceptible to EMI. For the higher robustness of the NCFF topology also the high PSRR is influential as power supply ripples are not feed forwarded to the output and the inverting input.

	Miller	Current Buffer	NCFF
V_{INP}	$\sim$	-	$\sim$
V_{DD}	$\sim$	-	+
V_{SS}	-	$\sim$	+
V_{OUT}	-	$\sim$	$\sim$
PSRR	$\sim$	$\sim$	+
Ac	-	$\sim$	$\sim$
Area	$\sim$	+	-
I_{DD}	+	$\sim$	-
Var. Load	+	$\sim$	- -

Table 5.4: Evaluation of the amplifier topologies on their robustness against EMI on all pins

The overall performance of the amplifier topologies is summed up in Table 5.4. Regarding EMI robustness, the NCFF topology outperforms the other two topologies with up to 20 dB improvement in EMIRR. Interestingly a lower robustness on the V_{INP} and V_{OUT} is found by simulation which might be explained by the two amplifier input stages that are affected by the EMI injection. The susceptibility of the current buffer topology is determined by the asymmetric slew rate. However, thanks to the avoided voltage follower, higher EMI robustness on the V_{SS} pin is achieved compared to the Miller topology which shows a much greater susceptibility due to the high-frequency voltage follower over the Miller capacitor.

Summing up the results from the ac analysis in Table 5.4, no preferably topology for all applications can be specified as the NCFF amplifier offers the highest gain and highest PM, but not the highest UGF. The current buffer offers high UGF but low gain. Calculating the active circuit area of the amplifiers, the current buffer topology uses less area than the miller amplifier caused by the smaller frequency compensation capacitor. The NCFF topology contains a big output NMOS transistor in the second stage. This transistor was designed with large dimensions to attain the same current density as in the first stage NMOS current mirrors with very small bias current. The increased area of this transistor causes the bad rating of the NCFF as the area of the feedforward stage attains smaller area then the compensation capacitor of the Miller amplifier.

Regarding power consumption and load variation, the Miller amplifier outperforms the other two topologies whereby the NCFF is not capable to provide a stable dynamic performance caused by the compensation strategy. Considering the overall performance, the NCFF topology clearly offers the best EMI and PSRR performance but it less suitable for low-power applications where the limited current influences frequency performance and area.

6 Conclusion

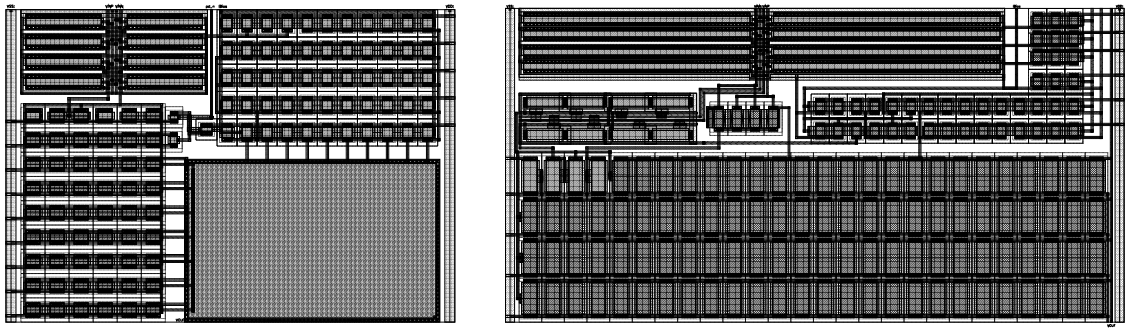
So what can now be done to increase the robustness of OpAmps against EMI? In this thesis different EMI measures were investigated based on their basic principle to avoid a dc shift at the output of the amplifier. Hereby the susceptibility can be explained with mainly three basic phenomena:

- Slew Rate Asymmetry: Caused by asymmetric slew rates, low-frequency EMI signals can be accumulated at the output of an amplifier. Symmetric amplifier topologies and the reduction of CLM effects in the bias transistors increase the robustness against EMI for lower and medium frequencies.

- Parasitic Input Capacitances: Caused by an asymmetry in the parasitic capacitances in voltage follower configuration, the input transistors are asymmetrically distorted under EMI disturbances with high amplitudes. To counteract such strong non-linear distortions, additional gate-source capacitances in the order of a few ten fF can be used to equalize the input parasitics. Due to the small values little ac performance influence is visible, but especially for the output pin higher robustness is achieved.

- Non-Linear Behavior of the Input Stage: At high-frequency EMI disturbances, both sides of the input differential pair are separated caused by the parasitic capacitance C_{Tail} of the bias transistor. Due to the non-linear MOSFET transfer function, signals are distorted if both common-mode and differential-mode signals are present at the input pair. In order to counteract these weak distortions, dedicated RC LP filters in series to the input pair can be used to improve the robustness of all pins. Decreasing C_{Tail} by using source buffering leads to a similar effect for high-frequency disturbances.

In order to implement EMI countermeasures it is of significant importance to know which EMI frequencies are expected and which pins are more likely to be interfered. Based on these considerations, engineers can take different countermeasures to increase the robustness against EMI. In order to simulate and evaluate the EMS of OpAmps, dedicated TBs are required. To guarantee a fair comparison of the results, the used



(a) Miller amplifier (b) NCFF amplifier

Figure 6.1: Layout of the designed Miller and NCFF amplifiers

measurement methods and TBs always have to be indicated. As FOM to evaluate the EMS of amplifiers, a combination of the pure output dc shift and the EMIRR is advised as both figures offer advantages and disadvantages.

A rarely mentioned influence on the susceptibility of amplifiers lies in the used frequency compensation method if two-stage amplifiers are used. Here a correlation with the achieved PSRR was recognized in simulations. Low PSRR values enable the transfer of power supply ripples to several amplifier pins and therefore decrease the robustness. This is especially true for the Miller amplifier were disturbances can couple over the Miller capacitance directly to the output of the amplifier. By doing so not only the supply pin but also the output, the inverting input and further connected circuitries are influenced by EMI. This explains also the high susceptibility of the basic Miller amplifier on one supply rail in comparison to other topologies where the power supply voltage follower due to the Miller capacitor is avoided.

One topology that avoids the voltage follower is the no-capacitor feedforward (NCFF) topology. This in the literature less known topology exhibits higher PSRR values then a Miller amplifier with improvement of up to 35 dB on higher frequencies. The use of a single-stage OTA in combination with a two-stage amplifier offers also a better EMI performance, where improvements of more than 20 dB in EMIRR compared to other topologies were achieved. For this superior performance, presumable the symmetric OTA topology is responsible. In contrast to single-stage amplifiers, also high dc gain and the ability to drive resistive loads thanks to the low-speed two-stage amplifier is offered by the NCFF topology.

However, in order to give clear statements about the EMI robustness of the NCFF amplifier and the considered EMI countermeasures, hardware measurements are needed to confirm the positive results attained from simulation and calculation. Layouts of the Miller, current buffer and NCFF amplifiers were constructed and a tape-out of the design is planned. To evaluate the effect of the mentioned EMI countermeasures, two

Miller amplifiers will be implemented whereby one amplifier is EMI hardened. The layouts of the basic Miller amplifier and the NCFF amplifier are given in Fig. 6.1.

With different tables regarding ac and EMI performance as well as other parameters, all investigated measures and topologies are summed up at the end of the thesis to give a quick and easy overview how to increase the EMI robustness of two-stage amplifier. Electromagnetic interference can not be fully avoided and will always constitute a limitation in future designs, but with the right design measures, a stable and robust amplifier operation can be assured. The author hopes that this thesis contributes to this intention and concludes with a statement from [2], [3]:

> *By designing EMC robust and resisting ICs, let's hope that we can keep up with Moore's Law for a long time.*

List of Abbreviations

BCI	Bulk Current Injection
CD	Common-Drain
CLM	Channel-Length Modulation
CMCC	Common-Mode Cancellation Circuit
CMFB	Common-Mode Feedback
CMRR	Common-Mode Rejection Ratio
CS	Common-Source
DPI	Direct RF Power Injection
DUT	Device Under Test
EMI	Electromagnetic Interference
EMIRR	EMI Rejection Ratio
EMS	Electromagnetic Susceptibility
FC	Folded-Cascode
FD	Fully Differential
FOM	Figure of Merit
GBW	Gain-Bandwidth Product
I/O	Input and Output
IC	Integrated Circuit
IEC	International Electrotechnical Commission
LDO	Low-Dropout Regulator
LHP	Left Half-Plane
LP	Low-Pass
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NCFF	No-Capacitor Feedforward
NFC	Near-Field Communication
NMOS	N-Channel MOSFET

OpAmp	Operational Amplifier
OTA	Operational Transconductance Amplifier
PCB	Printed Circuit Board
PM	Phase Margin
PMOS	P-Channel MOSFET
PSRR	Power Supply Rejection Ratio
RF	Radio Frequency
RHP	Right Half-Plane
SB	Source Buffering
SE	Single-Ended
TB	Test Bench
TF	Transfer Function
UGF	Unity-Gain Frequency

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