Lara Marie Novak, BSc

Capacitance- and Current-Voltage Characterization of Metal-Insulator-Semiconductor Structures with Topography

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Univ.-Prof. Peter Hadley, Ph.D.
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Abstract

Many electrical properties of metal-oxide-semiconductor (MOS) structures are determined by the quality of the insulator and its interfaces to the other materials. The dielectrics investigated in this thesis are produced by chemical vapor deposition (CVD). In contrast to stoichiometric thermally grown oxides - which have been studied and documented in many ways - they show significantly more defects, charges and states not only in the insulator bulk but also at its interfaces.
As the characterization of MOS structures has almost exclusively been done for planar structures a significant part of this theses was the comparison of such simple planar samples to corresponding ones with additional features of topography. With the well established methods of Capacitance- and current-voltage (CV and IV respectively) characterization it was found that the underlying structure, the so-called trenches, leads to a higher amount of interface states as well as oxide charges. The additional investigation of the film structure showed that the insulating layer is thinner at the trench bottoms and walls which can be one of the reasons for the higher level of conduction found in such samples.
Furthermore different thermal treatments were applied and their influence on the insulator-semiconductor formation determined. The stoichiometric composition was also looked at for a more detailed picture. It was shown that annealing in oxygen atmosphere resulted in less defects than in nitrogen.

This thesis was conducted at the Institute of Solid State Physics of the TU Graz and carried out at Infineon Technologies in Villach. All samples were produced and all equipment was provided there.

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Contents

Glossary

AC Alternating Current.

Al Aluminum.

CG Capacitance- and Conductance Voltage (Measurement, Curve).

CV Capacitance Voltage (Measurement, Curve).

CVD Chemical Vapour Deposition.

DC Direct Current.

FTIR Fourier Transform Infrared (Spectroscopy, Spectrum).

HF High Frequency (Measurement, Curve).

IV Current Voltage (Measurement, Curve).

LF Low Frequency (Measurement, Curve, Behaviour).

MOS Metal Oxide Semiconductor.

PECVD Plasma Enhanced Chemical Vapour Deposition.

RTP Rapid Thermal Processing.

SEM Scanning Electron Microscopy.

Si Silicon.

SiO_x (Non-stoichiometric) Silicon Oxide.

Part I
Fundamentals

Metal-oxide-semiconductor (MOS) structures are important building blocks of many semiconductor devices. Capacitance- and current-voltage (CV and IV respectively) characterization of such structures are well established methods in the analysis of bulk properties and interface quality of insulator-semiconductor systems. However, such characterization is almost exclusively performed using planar structures.
In this thesis the electrical properties of such simple structures are compared to those of corresponding ones with the additional feature of topography. Thus the consequences of imperfect step coverage of the insulating material is to be addressed. This is important for the production of semiconductor devices since their structures are rarely planar. Furthermore the thickness, coverage and stoichiometric composition of the oxide films of such samples is looked at for a more detailed picture.
The focus is on dielectrics deposited by chemical vapor deposition (CVD). CVD oxides are non-stoichiometric and show more defects than thermally grown ones. Therefore additionally the influence of various thermal anneal variants is investigated to improve the insulator quality.

1 Materials

To build a MOS capacitor (see f.e. fig. 32) three materials are needed: metal (M), oxide (O) and a semiconductor (S). The specific materials used in this master's thesis are briefly described in the following sections.

1.1 Substrate Wafers

Wafers made of silicon (Si) are used as substrate for further structuring and deposition processes. The wafers used in this thesis are produced with the Czochralski process, which is a growth process used to make single crystal semiconductors. All wafers have a diameter of 8 inch, but vary in other parameters such as thickness, crytal orientation or doping and therefore have different material specification numbers (M118[1] and P032[2]).

M118 silicon wafers

Material:	silicon (Si)	
Diameter:	200	mm
Thickness:	725 ± 25	μm
Crystal orientation:	<100>	
Dopant:	boron	
Type:	p-type	
Resistivity:	1 - 1000	Ω cm
Dopant concentration[3]:	(1512.0 - 1.3) $\cdot 10^{13}$	cm^{-3}

P032 silicon wafers

Material:	silicon (Si)	
Diameter:	200	mm
Thickness:	725 ± 15	μm
Crystal orientation:	<100>	
Dopant:	boron	
Type:	p-type	
Resistivity:	(23 -30) $\cdot 10^{-3}$	Ω cm
Dopant concentration[3]:	(3.079 - 2.247) $\cdot 10^{19}$	cm^{-3}

1.2 Thin films

For the aim of material characterization dielectric thin films are deposited on planar as well as non-planar substrates and the results of electrical measurements are evaluated and compared. The thin film material used in this thesis is silicon oxide.
The ideal and thermodynamically most stable stoichiometry of this dielectric is silicon dioxide $Si : O = 0.5$ (SiO_2). Most used processes such as plasma enhanced chemical vapour deposition (see section 2.2) are far from equilibrium processes, thus the stoichiometry of the thin films is different from the theoretical one and gets denoted as SiO_x.
This also results in a variability of the dielectric constant ϵ: it lies in a defined range for those dielectrics, but cannot be determined exactly without knowing the (quantitative) chemical composition of the films.
For SiO_2 the dielectric constant is $\epsilon_{SiO_x} = 3.7 - 3.9$[4].

1.3 Metal electrodes

The material used to form the metal electrodes of the MOS capacitor is Aluminium-Silicon-Copper (AlSiCu). Al is the desired material for the electric contact and is therefor the main component of the alloy with only small amounts ($\leq$ 1 %) of Si and Cu. Si is mixed in to avoid spiking[5] and Cu, in combination with tempering, helps saturating dangling bounds in the material.
The work function of the material is close to that of the main component $\Phi_{Al} = 4.1\ eV$[6]. For Al alloys there is an almost linear relation (at a low concentration of the other materials)[7] and the alloys work function calculates via $\Phi_{alloy} = x\Phi_A + y\Phi_B + z\Phi_C$, where $\Phi_{A,B,C}$ are the work functions of the pure elements and x, y and z are the percentage amounts of the element in the alloy ($x + y + z = 1$).

2 Insulator Formation

Different methods of thin film deposition techniques are compared in this thesis regarding the amount of occurring trapped charges in the oxide bulk as well as at the interfaces. These charges affect electric properties and performance of the MOS capacitor and other devices making use of such structures. To optimize film properties annealing is performed after deposition (see section 8).

2.1 Chemical Vapor Deposition (CVD)

In a CVD process a volatile material reacts chemically with other gases to form a solid thin film. The basic steps of a CVD process can be seen in fig. 2.
A wafer which is the substrate for the film is placed in the reaction chamber. The gases acting as precursors pass by (typically in a viscous flow). Once brought together they form new reactive species and byproducts in the gas phase. Then they are transported to the substrates surface together with the initial gases. Therefore they need to cross the so-called boundary layer: Beneath the viscous flow regime with uniform velocity is a gas layer adjacent to the surface in which the velocity goes to $\vec{v}_s = 0$ rapidly. This can be described by the Hagen-Poiseuille law.

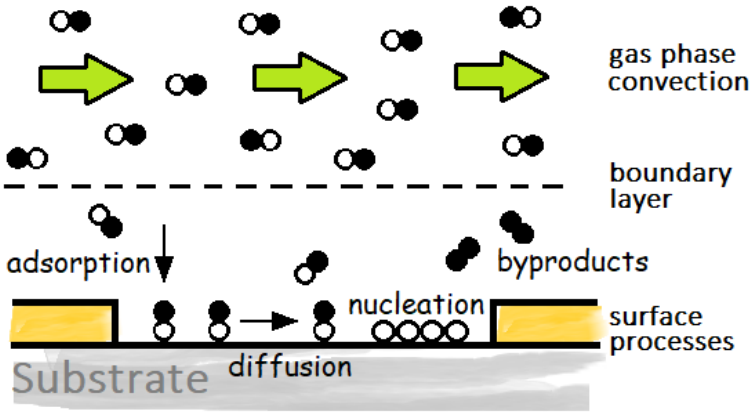


Figure 2: Illustration of the basic steps of a CVD process.

Once inside the boundary layer diffusion of the reactants to the surface takes place and the particles physi- as well as chemisorb. Surface diffusion may occur as well, depending on the materials used. The film formation process starts with nucleation and is followed by island growth until a whole layer is completed where the substrate acts as a catalyst for the heterogeneous reactions creating the final species forming this film. Volatile byproducts desorb and get transported out of the reaction zone via pumping.[8]

A CVD process which depends on transport and chemical reactions can be either diffusion- or surface reaction limited. This means that either the reaction or the flow rate is slower than the other one. At low temperatures there is normally a slow reaction rate usually forming uniform films and good step coverage. At higher temperature the reaction rate rises exponentially. When it

is hot enough for all gas molecules to react at the surface the rate of gas transport limits the film growth. Film properties and deposition rates can therefore be controlled by temperature, pressure and transport kinetics. [9]

2.2 Plasma Enhanced Chemical Vapor Deposition (PECVD)

Compared to purely thermally activated processes, plasma driven ones enable much lower temperatures at high deposition rates. This is possible because the plasma delivers enough energy to decompose the precursor molecules to reactive species. [8]
Plasma is a state of matter which is reached when electric energy is added to a gaseous phase until frequent collisions of the gas particles create free electrons and positively charged ions. [10] As plasma collisions are hard to control the stoichiometry of the deposited film is not constant in contrary to thermal CVD . Also the amount of trapped hydrogen is higher in PECVD processes which has to be considered in furnace processes. [9]

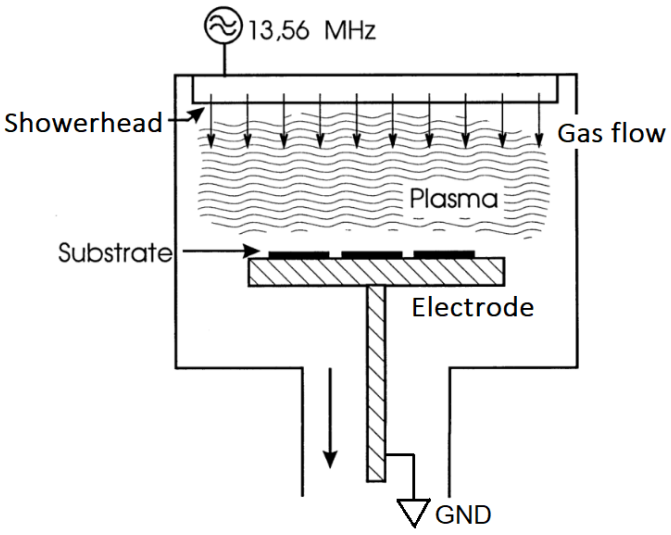


Figure 3: Scheme of a PECVD parallel plate reactor, figure reproduced from [11]

To create a plasma two electrodes are used generating a radio frequent (RF) field that ionizes gas (f.e. Argon). In a typical parallel plate PECVD reactor (fig. 3) the substrate is placed on a heated electrode. The precursor gas is fed into the chamber via a shower head electrode and is dissociated in the plasma (see fig. 4 (1)). Typical pressures in a PECVD reactor are in the range of $5 \cdot 10^{-2}$ and 5 torr and ion- respectively electron densities are between 10^9 and 10^{11} cm^{-3}. [8]
After the decomposed species reach the surface by diffusion (2), surface diffusion (3) and finally the chemical reactions (4) take place and reaction products are transported away (5). Gas phase reactions are to be avoided in such a process as they lead to particle formation.

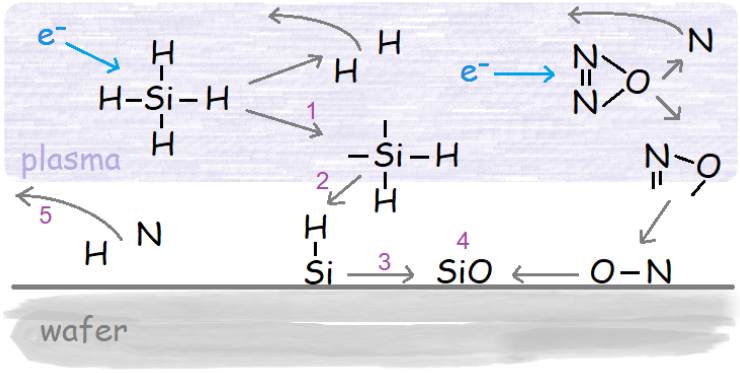


Figure 4: Exemplary reaction chain taking place in the PECVD reactor.

The basic silane (SiH_4) based PECVD reactions for SiO_x taking place at the substrate surface are the following:

$$SiH_x + N_2O = SiO_x \ (+ \ H_2 + N_2 + \text{byproducts}) \ [12]$$

where the reaction partner N_2O is nitrous oxide.
In addition to the parameters that control a conventional CVD process sometimes also the RF frequency can be tuned in PECVD . The frequency of the RF field determines the amount of ion bombardment and therefore several film properties like composition or structure. The higher the RF the more ionized particles are created in the plasma. This leads to a higher deposition rate and denser and more stable films. The deposition rate reaches saturation when the maximum of dissociation is reached. Further increase of the power might decrease the deposition rate due to ion bombardment of the film which might also induce stress and trapped gases. In contrast, a very low RF power can lead to distortions and dangling bonds at the surface of the film. [13]
In this thesis an industrial standard of 13.56 MHz is used for which electrons but hardly any ions are fast enough to follow the field and therefore ion bombardment is reduced. [9]

3 Metal-Oxide-Semiconductor Capacitor

The books *Physics of Semiconductor Devices* by Sze and Ng [14], *Devices for Integrated Circuits* by Casey [6] and *MOS (metal oxide semiconductor) physics and technology* by Nicollian and Brews [15] are good references for MOS structures.
As the name implies a MOS capacitor is made of an oxide layer between a metal and a semiconductor resulting in a capacitance. MOS capacitors are simple structures and very useful for the investigation of both the insulating and semiconducting material, as well as the insulator-semiconductor interface. The obtained properties by electrical measurements of the MOS capacitor include information about band bending and the depletion width at the semiconductor surface, oxide thickness and breakdown field, trapped charges and many more. These properties are interesting for electric devices used in integrated circuits such as MOSFETs (Metal Oxide Semiconductor Field Effect Transistor), as improvement of the MOS structure directly applies to the functional devices themselves.
In this thesis, aluminum - mixed with small amounts ($\leq$ 1 %) of copper and silicon and therefore labeled as AlSiCu - is used for the metal component, p-doped Si for the semiconductor and SiO_x for the insulating layer as described in section 1.

3.1 Band Diagram

Considering an ideal insulator and interfaces free of charge, the energy band diagram at initial contact shows a lower Fermi energy (= bigger work function) in a p-type Silicon semiconductor with doping concentrations in the range of the used samples than in AlSiCu.

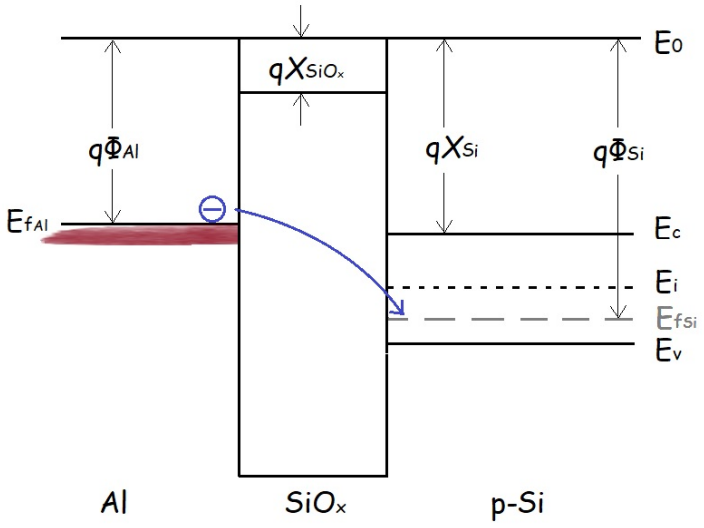


Figure 5: Energy-band diagram for Al, SiO_2 and p-type Si before equilibrium.

The difference in Fermi- and vacuum level determines the work function of

a material Φ and for a metal it simply calculates via

$$q\Phi_{Al} = E_0 - E_{F\,Al} \tag{1}$$

where q denotes unit charge and E_0 is the vacuum level energy.
For semiconducting and insulating materials one uses the electron affinity $q\chi$ to determine the work function, in combination with the valence- and conduction band energies E_v and E_c as well as the band gap E_g:

$$q\Phi = q\chi + (E_c - E_{FSi}) = q\chi_{Si} + E_g - (E_{FSi} - E_v) \tag{2}$$

For a semiconductor the Fermi energy and therefore the work function are doping dependent.
When a metal and semiconductor are brought together in an MOS structure the system seeks thermodynamic equilibrium and therefore electrons will immediately move from the metal to the semiconductor, aligning the Fermi level E_F of the materials, while the vacuum level E_0 has to stay continuous. This results in bending of the energy band of the semiconductor towards the insulator which can be seen in fig. 6 and can be calculated using Poisson's equation (see section 3.2).
The difference in the work functions for semiconductor and metal determines in which direction (up or down) and how much the bands of Silicon bend when no external voltage is applied and is referred to as built in voltage $V_{bi} = \Phi_{Al} - \Phi_{Si}$.

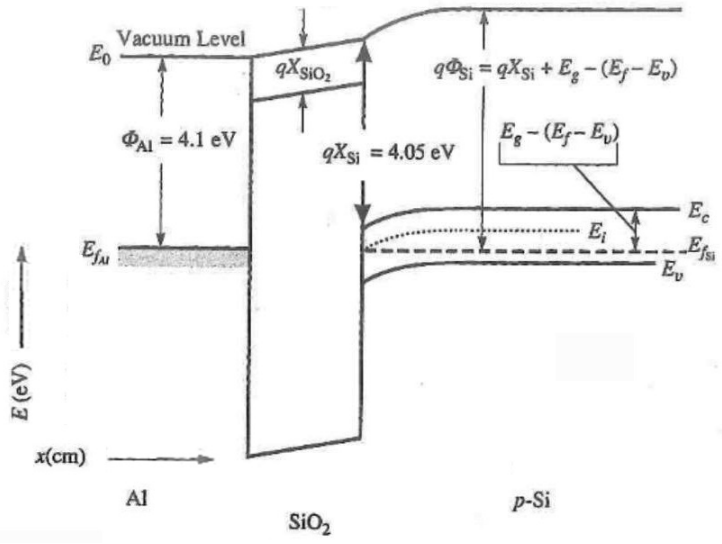


Figure 6: Energy-band diagram for Al, SiO_2 and p-type Si at equilibrium. Figure reproduced from [6]

The band bending can be modified by applying an external voltage to the metal electrode - the gate voltage V_G - resulting in different regimes, which are further explained by means of a p-type semiconductor. This regimes can be defined by the value of the surface potential Ψ_s.

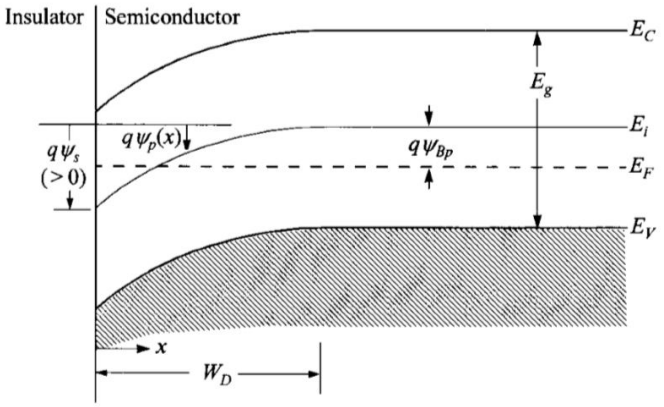


Figure 7: Energy-band diagram at the surface of a p-type semiconductor. Figure reproduced from [14]

The surface potential is the difference in potential at the semiconductor surface and in the bulk. Therefore it determines the bending of the valence- and conduction band.

Accumulation

Accumulation is the result of applying a more negative voltage than the built-in voltage $V_G < V_{bi}$ to the metal electrode resulting in a negative surface potential Ψ_s. The majority carriers of the semiconductor (holes) are attracted by this negative potential and accumulate at the surface adjacent to the insulator. The conduction- and valence band bend up and the positive space charge at the surface Q_s causes a negative charge $Q_m = -Q_s$ at the metal surface.

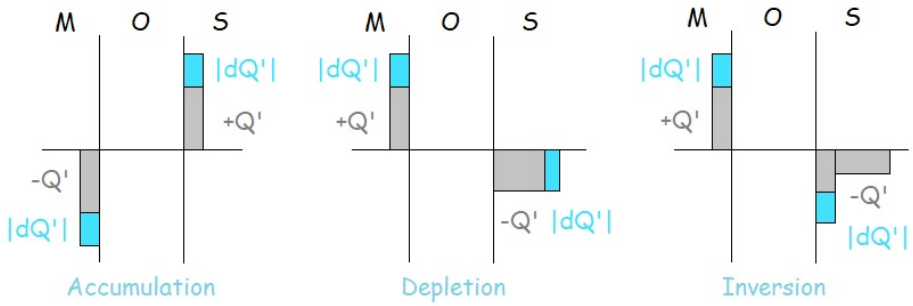


Figure 8: Charge distribution for the different MOS regimes. The blue part $|dQ'|$ shows how charge added on the metal side is balanced on the semiconductor side in for each regime.

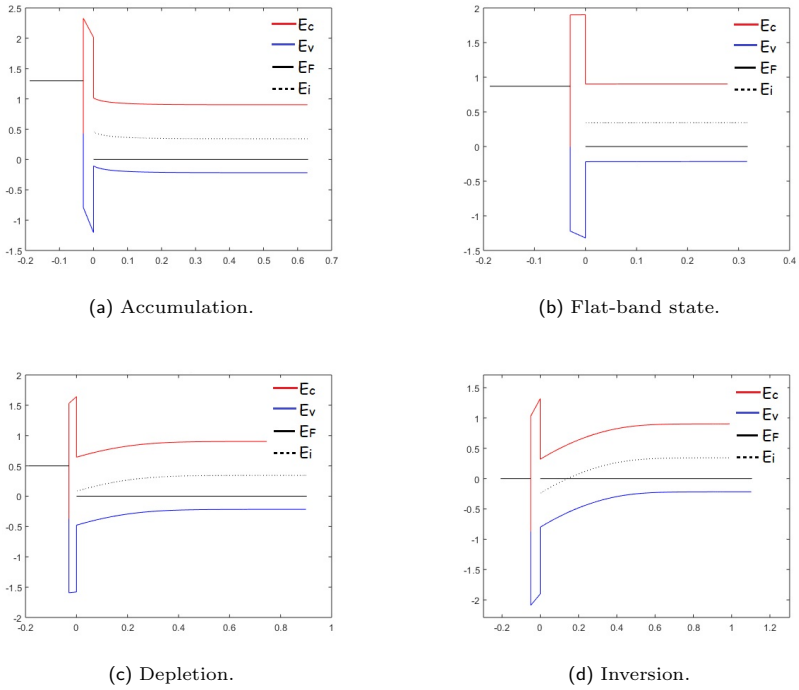
Flat-band Case

If V_G exactly compensates V_{bi} there is no bend banding, i.e. the bands are flat and $\Psi_s = 0$. This also means that there is no charge redistribution and so no electric field throughout the structure. The compensating voltage is called flat-band voltage and is calculated in the same way as the built in voltage

$V_{fb} = V_{bi} = \Phi_{Al} - \Phi_{Si}$ and is the boundary between two of the main regimes in a MOS capacitor, accumulation and depletion.

Depletion

If a voltage slightly more positive than V_{bi} is applied the bands bend downwards. The voltage is pushing the holes away from the insulator-semiconductor surface leaving behind negatively charged ions there. This space-charge region grows with the voltage applied as it compensates the positive charge at the metal electrode. The MOS capacitor is in depletion when $\Psi_B > \Psi_s > 0$ holds for the surface potential Ψ_s.
The MOS structures produced and measured in this thesis are in depletion when no voltage is applied. This is due to the work function differences of the materials used where $\Phi_{Al} < \Phi_{Si}$ and can be seen in fig. 6.



(a) Accumulation.

(b) Flat-band state.

(c) Depletion.

(d) Inversion.

Figure 9: Band structure of a MOS capacitor in the different regimes - simulated with Matlab.

Inversion

As soon as the surface potential exceeds the potential between midgap and Fermi energy $2\Psi_B > \Psi_s > \Psi_B$ the MOS capacitor is in weak inversion. Then the number of minority carriers exceeds that of the majority carriers at the surface $n_s > p_s$ which is therefore inverted.
Applying even more voltage $V_G > V_T$ strong inversion is reached. V_T is the so-called threshold voltage. In this regime $\Psi_s > 2\Psi_B$ and the number of electrons at the interface exceeds the number of acceptors ($n \geq N_A^-$). A layer of mobile electrons forms between the oxide and the semiconductor which is known as

inversion channel.
In the strong inversion regime the depletion width reaches a maximum x_d^{max} and stays, as well as the electric field, constant in the semiconductor from then on.[16]

Deep Depletion

Deep depletion is an effect due to minority carriers not being able to follow the change in the bias voltage (DC). This can happen if the speed of the voltage sweep performed to measure the capacitance is too high. The result is that the MOS structure is not in equilibrium relative to the applied voltage. A detailed explanation of the effects is given in section 7.2.2.

3.2 Poisson Equation

The Poisson equation describes how an electrostatic potential ϕ depends on the charge density and can therefore be used to calculate the band bending of a MOS structure.
To derive Poisson's equation one starts with Gauss' Law

$$\overrightarrow{\nabla} \cdot \overrightarrow{\mathscr{E}} = \frac{\rho}{\epsilon_s \epsilon_0} \tag{3}$$

and uses the negative gradient of the potential for the electric field $-\overrightarrow{\nabla}\phi = \overrightarrow{\mathscr{E}}$:

$$\triangle\phi = -\frac{\rho}{\epsilon_s \epsilon_0} \tag{4}$$

ϵ_s and ϵ_0 are the semiconductor- and the vacuum permittivity. The charge density ρ of a semiconductor is $\rho = q \cdot (p + N_D^+ - n - N_A^-)$, where N_D^+ and N_A^- are the concentrations of ionized donor and acceptor atoms, n is the density of electrons and p the density of holes. If the semiconductor is *nondegenerate*, meaning that the doping concentrations are smaller than the effective density of states for the according band, the Boltzmann approximation can be used for calculating n and p (instead of the Fermi-Dirac integral):

$$n = N_c \exp\left(-\frac{E_c - E_F}{k_b T}\right) \tag{5}$$

$$p = N_v \exp\left(-\frac{E_F - E_v}{k_b T}\right) \tag{6}$$

where k_b is the Boltzmann constant and N_c and N_v denote the effective density of states in the conduction- or valence band, respectively. N_c and N_v depend not only on the temperature, but also on the effective mass of the carriers in each band.
The product of n and p is constant in nondegenerate semiconductors $np = n_i^2$ which is known as mass-action law, with n_i being the intrinsic carrier concentration.
According to [16] knowing ρ and using the relations $q\frac{dV}{dx} = -\frac{dE_v}{dx}$ and $E_c = E_g + E_v$ the Poisson equation for a p-type semiconductor can be written as

$$\frac{d^2 E_v}{dx^2} = \frac{q^2}{\epsilon_s \epsilon_0}\left(-N_A^- - N_c exp\left(\frac{E_F - E_g - E_v}{k_b T}\right) + N_v exp\left(\frac{E_v - E_F}{k_b T}\right)\right) \tag{7}$$

where the donor concentration $N_D = 0$. As E_F can be thought of as some energy relative to E_c [17] it can simply be excluded from eq. (7) when simulating the bending of the bands as shown in fig. 3.1.

3.2.1 Depletion Approximation

The depletion width stays constant at its maximum x_d^{max} when the MOS capacitor is in the strong inversion regime. x_d^{max} and the threshold voltage V_T can be calculated with the help of the depletion approximation.
The charge density has a rectangular profile in this approximation. In the depletion layer the mobile charge carrier concentration is assumed to be negligible compared to the charge due to the ionized acceptor concentration. In the bulk charge neutrality is given, meaning that the number of charge carriers equals the number of dopants ($n = N_D^+$, $p = N_A^-$). Therefore the intrinsic carrier concentration n_i in the semiconductor can be written as

$$n_i^2 = np = N_c exp\left(\frac{E_F - E_c}{k_b T}\right) N_A^- \tag{8}$$

yielding

$$(E_c - E_F)_{bulk} = -k_b T ln\left(\frac{n_i^2}{N_A^- N_c}\right) \tag{9}$$

in the bulk of the semiconductor.
For charge neutrality to be given in the MOS capacitor, it is required that the sum of all charge densities results in zero. This means that the absolute values of the charge density on the metal and the space charge Q_s, i.e. the total charge per unit area in the semiconductor, are equal.

$$Q_m = -Q_n - q x_d^{max} N_A^- = -Q_s \tag{10}$$

Q_n is only present in the strong inversion regime as it gives the electrons per unit area in the inversion channel, $qx_p^{max}N_A^-$ gives the charge due to the ionized acceptors in the depletion layer.
Using the condition for the beginning of strong inversion at the surface $n = N_A^- = N_c exp\left(\frac{E_F - EC}{k_b T}\right)$ (number of electrons equals the number of ionized acceptors) one obtains

$$(E_c - E_F)_{interface} = k_b T ln\left(\frac{N_c}{N_A^-}\right) \tag{11}$$

at the semiconductor-insulator interface.
The difference in the conduction band energy (with respect to the Fermi energy) in the semiconductor bulk and surface corresponds to the surface potential Ψ_s (see fig. 7)

$$\begin{aligned} q\Psi_s = (E_c - E_F)_{bulk} - (E_c - E_F)_{interface} = \\ = -k_b T ln\left(\frac{n_i^2}{N_A^- N_c}\right) - k_b T ln\left(\frac{N_c}{N_A^-}\right) = \\ = 2k_b T ln\left(\frac{N_A^-}{n_i}\right) \end{aligned} \tag{12}$$

In the regimes of depletion and weak inversion where no layer of mobile electrons is present it can (according to [14]) be shown that

$$Q_s = \sqrt{2q\epsilon_0\epsilon_s N_A^- \Psi_s} \tag{13}$$

Together with eq. (10) and (12) one obtains the maximum depletion width

$$\longrightarrow x_d^{max} = 2\sqrt{\frac{\epsilon_0\epsilon_s k_b T}{q^2 N_A^-} ln\left(\frac{N_A^-}{n_i}\right)} \tag{14}$$

Using Gauss' Law the electric field in the semiconductor $\mathscr{E}_s$ is obtained from the space charge. Using the expression for x_d^{max} given in eq. (14) yields

$$\mathscr{E}_s = \frac{q x_d^{max} N_A^-}{\epsilon_0\epsilon_s} = 2\sqrt{\frac{N_A^-}{\epsilon_0\epsilon_s} k_b T ln\left(\frac{N_A^-}{n_i}\right)} \tag{15}$$

and can be used to calculate the threshold voltage V_T. According to [6] V_T is the sum of the voltage drops across the insulator and the semiconductor and the flat-band voltage

$$V_T = V_i + \Psi_s + V_{fb} \tag{16}$$

where $V_i = \mathscr{E}_i t_i$ is the electric field in the oxide times the oxide thickness. The field in the oxide is obtained by $\mathscr{E}_i = \mathscr{E}_s\left(\frac{\epsilon_s}{\epsilon_i}\right)$ and the treshold voltage becomes

$$\longrightarrow V_T = \frac{2t_i}{\epsilon_i}\sqrt{\frac{\epsilon_s}{\epsilon_0} k_b T ln\left(\frac{N_A^-}{n_i}\right)} + \frac{2k_b T}{q} ln\left(\frac{N_A^-}{n_i}\right) + V_{fb} \tag{17}$$

3.2.2 Numerical Solution

To obtain the band diagram of a MOS structure the Poisson equation was solved numerically with *MATLAB* by using the shooting method, following the example of [16].
One starts in the semiconductor bulk far from the oxide where the valence band energy is constant

$$\frac{dE_v}{dx} = 0 \tag{18}$$

and the Fermi energy is defined as $E_F = 0$. The valence band energy at this point can be calculated via

$$E_v = k_b T ln\left(\frac{N_A}{N_v}\right) = E_{v0} \tag{19}$$

specifying the starting point E_{v0}. For the numerical integration of the Poisson equation a small value has to be chosen for $\frac{dE}{dx}$. The midpoint method, a second order numerical method to solve one dimensional differential equations, is then applied until the semiconductor-oxide interface is reached yielding the voltage V_s and the electric field $\mathscr{E}_s$ at this point. The voltage at the gate of the MOS capacitor V is a sum of the voltages across the insulator and the interface V_s

$$V = \frac{\epsilon_s \mathscr{E}_s}{\epsilon_i} t_i + V_s \tag{20}$$

where index i denotes the insulating material. This gate voltage is correct for the chosen boundary conditions in the semiconductor bulk (eq. (18) and eq. (19)) but does not have to be the true gate voltage (which is an input parameter in this program). If this is not the case the starting point for the integration is adjusted to the left or right side and the integration is done again until the true gate voltage is reached.

3.2.3 Simulation of the Electric Field

A simulation of the electric field in a sample with trenches was provided by Peter Oles whom this author wants to thank at this point.
This simulation uses the **finite element method** (FEM) and is done using the simulation software *COMSOL Multiphysics*.
The idea of the finite element method is to approximate the solution of a differential equation like the Poisson equation (4) with the help of a linear combination of basis functions. These basis functions are obtained by dividing the three dimensional space into geometrical shapes, f.e. tetrahedra. The basis functions then depend on the values at the corners of the elements and are very localized in space. In regions where the change in potential is strong the numerical solution can be refined by using more smaller elements. For more details on FEM the *Computer Simulations* script by *H.G.Evertz* [18] is recommended for further reading.
In the first part of the simulation the trenches are represented by cylinders and periodical boundary conditions were applied to generate the effect of an infinite oxide area. This was done for six directions as one trench is surrounded by six others as can be seen in fig. 10. From the electric potential simulated also the electric field within such a structure can be obtained.

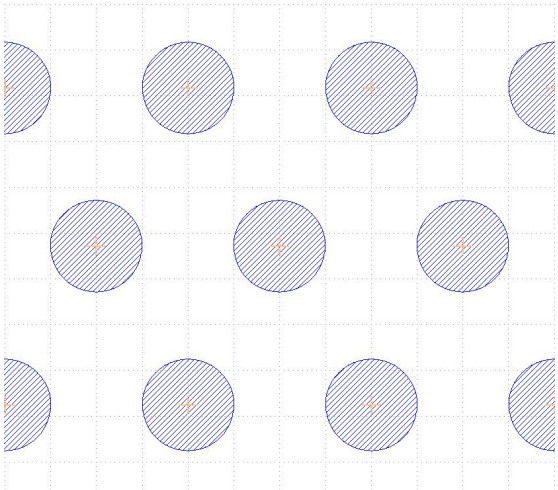


Figure 10: Top view of a sample with trenches.

fig. 11 shows the simulation of the electric potential. Note that in this whole simulation the structure is presented upside down (metal at the bottom, semiconductor on top) in opposite to how it is presented in this thesis elsewhere. As the metal is electrically conductive it sees no potential drop. The semiconductor

is also assumed to be conductive. This is because another more detailed current density simulation of an insulator semiconductor[1] stack performed at *Infineon* showed that the potential drop in the depletion zone of the semiconductor is only 1 V for a voltage of 100 V applied.

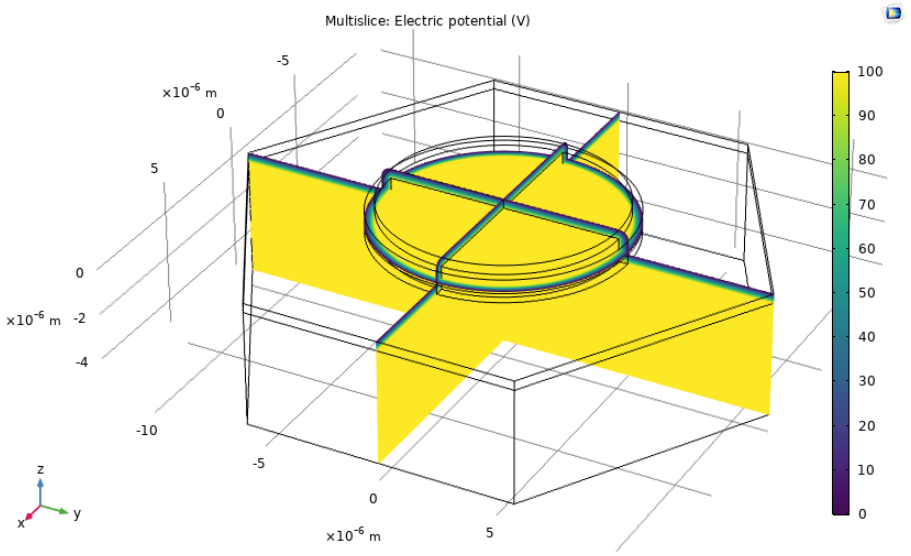


Figure 11: Simulation of a sample with trenches. A voltage of 100 V is applied from the metal side (here: down-side).

Having a closer look at the cross section one can see that the electric field builds up at the corners of such a sample.

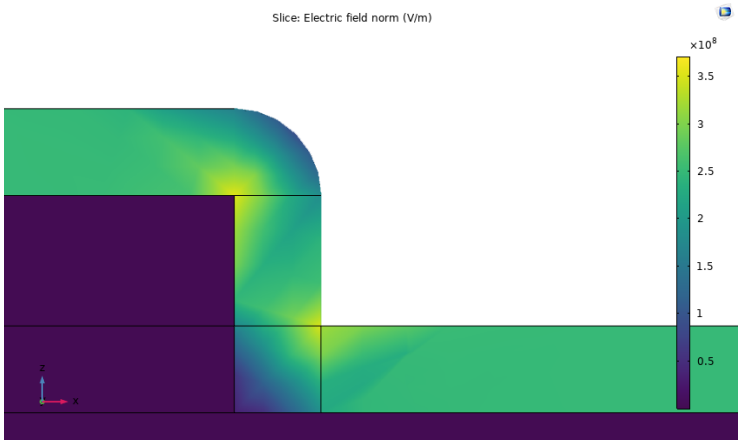


Figure 12: Electric field within a sample with trenches. Again a voltage of 100 V is applied from the metal side.

Therefore the edges were simulated in greater detail in a more sophisticated model as second step. The edges were also rounded with with a radius of 10

[1] with similar doping concentration.

nm. In fig. 13 one can see the reduced size of the elements in the corners of the sample.

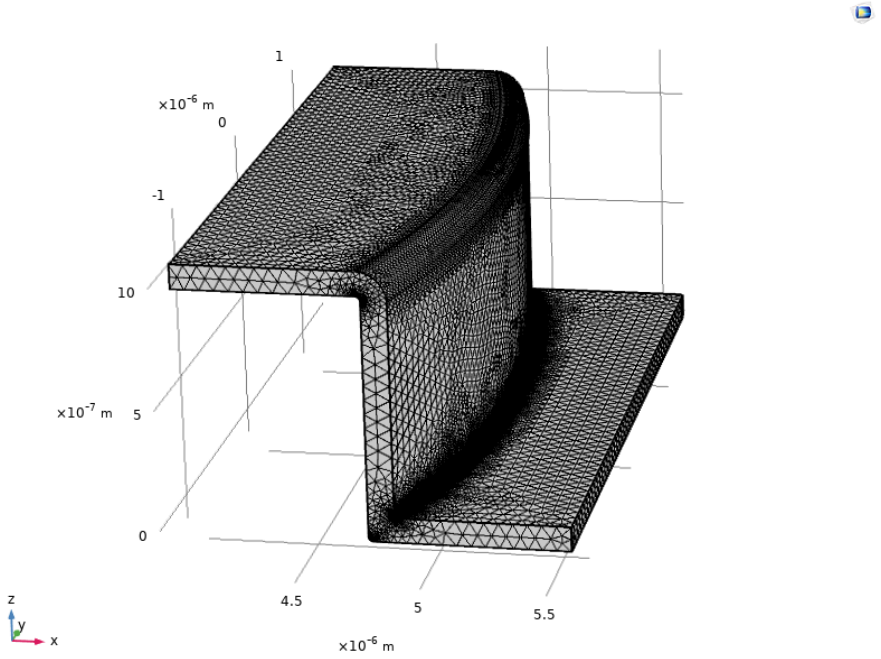
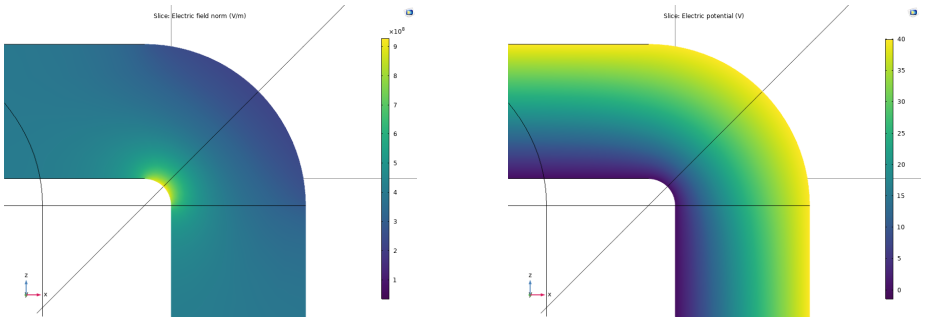


Figure 13: Refinement of the corners using the finite element method.

In fig. 14 a close-up of the lower edge of a trench (pointing towards the semiconductor) is shown. The 45° line in the x-z plane is used to plot the electric field and potential in this direction which is shown in fig. 16.



(a) Electric Field.

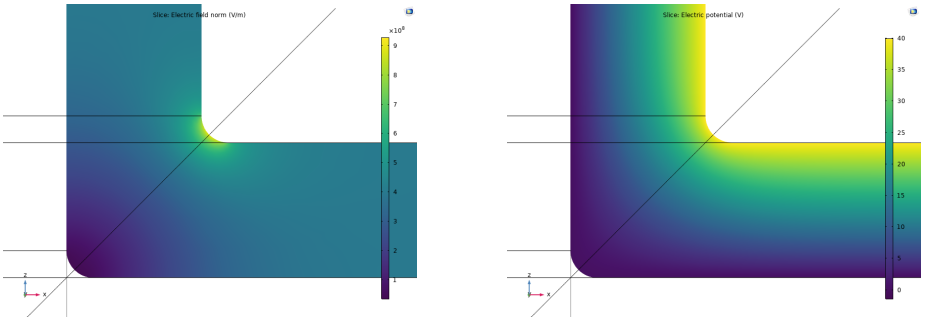
(b) Electric Potential.

Figure 14: Simulation of the corner pointing towards the semiconductor. A voltage of 40 V is applied from the semiconductor side.

To estimate the electric field the corners were assumed to be round and assumed to act like concentric cylinders.

$$E = \propto \frac{1}{\ln \frac{r_a}{r_i} r} \tag{21}$$

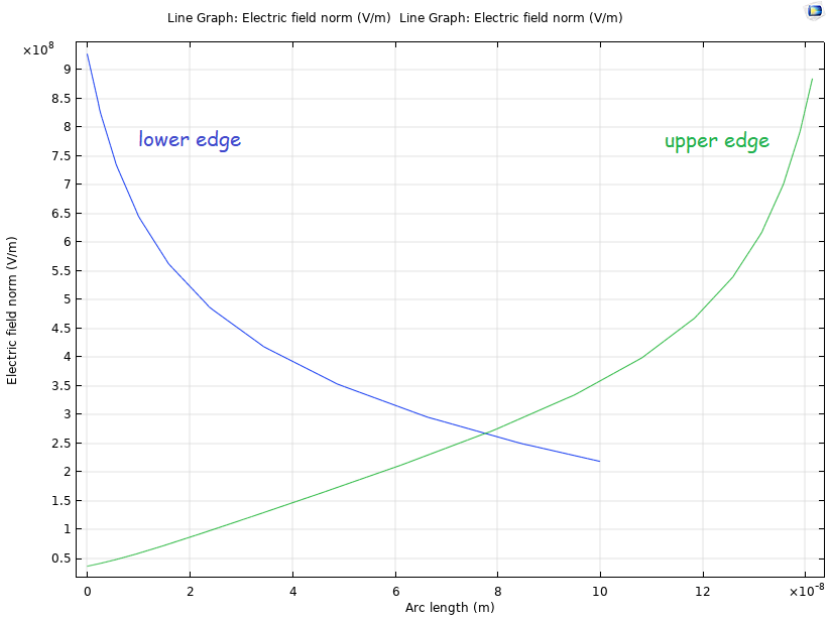
The *COMSOL* simulated curves fit this result pretty well pretty well as can be seen in fig. 16b.



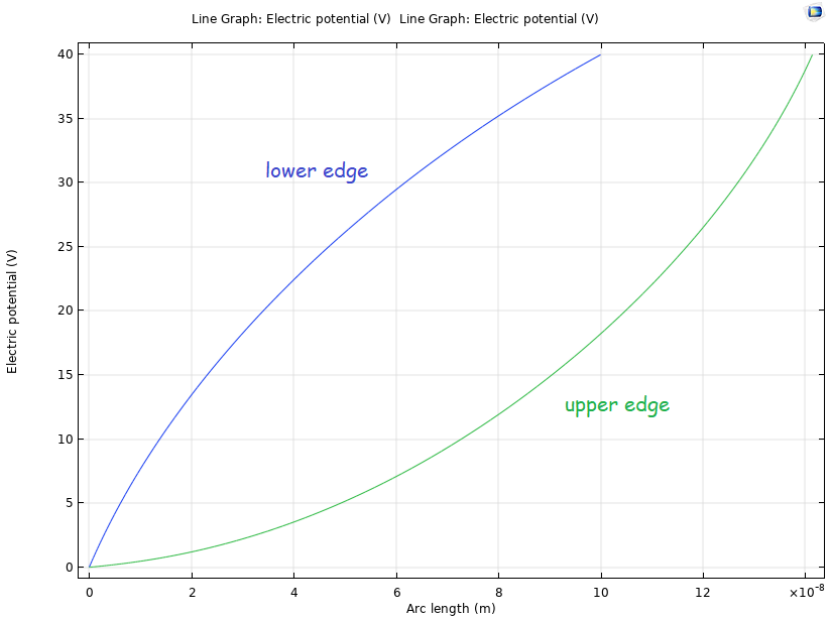
(a) Electric Field. (b) Electric Field.

Figure 15: Simulation of the corner pointing towards the metal. A voltage of 40 V is applied from the semiconductor side.

Those simulations show that for the trenched samples localized higher electric fields appear compared to the planar structures. This can further lead to higher leakage currents (which are discussed in sec.18).



(a) Electric Potential.



(b) Electric Potential.

Figure 16: Plot of the electric field and potential towards the marked 45° line for both edges towards semiconductor (lower) and metal (upper).

3.3 Metal-Semiconductor Contact

When the semiconductor is in direct contact with a metal an abrupt junction called **Schottky contact** is obtained. A barrier is formed at the interface between the materials. Carrier transport as well as capacitance behaviour depend on this barrier which itself depends on the work function of the metal Φ_{Al} and the electron affinity χ of the semiconductor. For a p-type semiconductor the barrier height in equilibrium (excluding the influence of interface states) is given by

$$\Phi_B = \frac{Eg}{q} - (\Phi_{Al} - \chi) \tag{22}$$

As the impurity concentration changes abruptly such a Schottky contact is similar to an p-n junction. Therefore it leads to a depletion layer with capacitance C_D. When the semiconductor is homogeneously doped plotting $\frac{1}{C_D^2}$ versus voltage yields a straight line where the intercept on the voltage axis gives the built-in potential and the slope can be used to calculate the carrier density. [14]

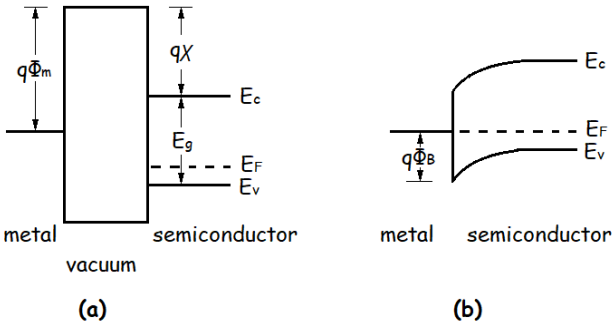


Figure 17: Band diagrams of a metal and a p-type semiconductor (a) in separated systems and (b) in contact.

When electrically measuring a MOS capacitance a Schottky contact between the chuck of the measuring unit and the backside of the wafer can sophisticate the outcome. Therefore additional doping and on-chip backside metalization should always be the connection between the MOS capacitor and the measurement device ensuring an **ohmic contact**.

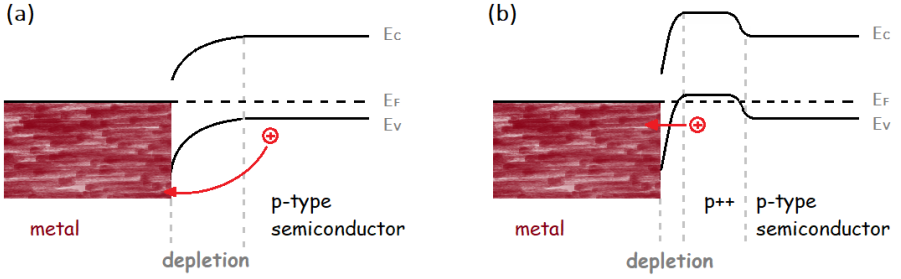


Figure 18: Band diagrams of a metal and a p-type semiconductor with $\Phi_{Al} < \Phi_{Si}$ building a (a) Schottky contact and (b) ohmic contact.

According to [6] a metal-semiconductor contact is ohmic if the contact resistance R_c is negligible compared to the bulk resistance of the semiconductor. If the semiconductor has a low impurity concentration (which is the case for the used M118 substrates) thermionic emission is the main kind of transport. In this regime the contact resistance which mainly depends on the interface energy barrier is relatively high. Therefore the contact region of the semiconductor with the metal has to be more heavily doped. The higher the impurity concentration gets the narrower the depletion width and from a certain point on the holes tunnel through the barrier (see fig. 18). In this tunneling regime the contact resistance $R_c \propto exp\left(\frac{\Phi_B}{\sqrt{N_A}}\right)$ varies with the doping and gets very small.

4 Conduction in Insulators

Insulators by definition are materials not containing free charge carriers. In an ideal MOS structure the insulating layer would not conduct at all. This is not the case in real insulators where different types of conduction processes may occur when the electric field and/or the temperature are high enough.
To calculate the current densities of the different mechanisms the electric field in the insulating material $\mathscr{E}_i$ is used and can be approximated by the ratio of the applied voltage V and the thickness of the oxide d. The assumption holds when there are nearly no oxide charges and the flat-band voltage of the MOS structure is small compared to V.

$$\mathscr{E}_i = \mathscr{E}_s \left(\frac{\epsilon_s}{\epsilon_i} \right) \approx \frac{V}{d} \tag{23}$$

where $\mathscr{E}_s$ is the electric field in the semiconductor and $\epsilon_{i,s}$ are the dielectric constants. This relation can then be used to determine the voltage dependence from the field dependence of the different conducting processes. Together with the temperature dependence it can be used to distinguish between the processes in measurements. [14]
The different conduction mechanisms can be be grouped in bulk-limited and electrode-limited conduction processes. Latter are Fowler-Nordheim tunneling and thermionic emission. Space-charge-limited-, ionic- and impurity conduction as well as Frenkel-Poole emission are bulk limited mechanisms. [19]
Details to the different conduction mechanisms which are briefly described in the following sections can be found in *Physics of Semiconductor Devices* by Sze and Ng [14].

4.1 Tunneling

Tunneling is the most common current mechanism in MOS structures. Tunneling means that an electron wave function has a non-zero probability to cross energy barriers. Tunneling depends strongly on voltage ($J \propto V^2 exp\left(-\frac{b}{V}\right)^{\dagger}$, J ... current density), but not on temperature and therefore might dominate at low temperatures.
It can be distinguished between direct tunneling, which occurs at lower fields and thinner insulators (below ≈ 5 nm for oxides), and **Fowler-Nordheim tunneling**. Latter occurs at high fields and mainly for thicker insulators. In Fowler-Nordheim tunneling the electrons only tunnel through part of the insulating layer (compared to direct tunneling where the whole layer is crossed). The energy barrier has a triangular shape and, once tunneled through it, the charge carriers can move freely in the conduction or valence band of the insulator. This mechanism works best in thermally grown SiO_2 layers as there are very little structural defects.

4.2 Thermionic Emission

If charge carriers have enough (thermal) energy they are able to overcome the energy barrier between metal electrode and the insulator. They can hop from

[†] b...constant

the metal to the conduction band of the insulating material and contribute to the thermionic-emission current. It is an majority carrier current which is mainly temperature dependent (the higher the temperature the more electrons contribute), but it also exponentially depends on the voltage and the barrier height Φ_B.

$$J \propto T^2 exp\left(\frac{q}{k_b T}\left(\beta\sqrt{\mathscr{E}_i} - \Phi_B\right)\right)$$

where $\beta = \sqrt{\frac{q}{4\pi\epsilon_i d}}$. In the presence of an electric field image-forces change the height of the barrier for charge carrier emission. A charge in the semiconductor induces a so-called image charge in the metal leading to a potential energy. When an external electric field is applied it lowers the barrier height on one side with sign depending on the direction of the field applied. The difference between the maximum of this combined potential curve and the vacuum energy then gives the image- or **Schottky-barrier lowering** $q\beta\sqrt{\mathscr{E}_i}$. Note that this implies that the barrier height is bias dependent.

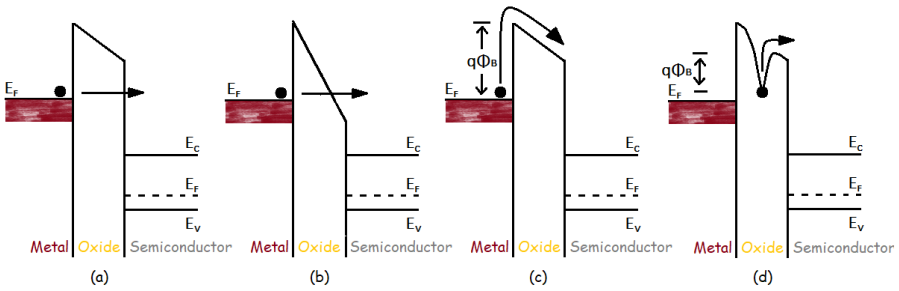


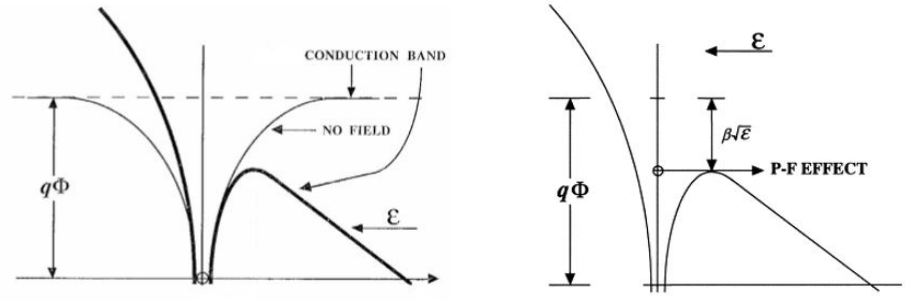
Figure 19: Energy-band diagrams showing (a) direct tunneling, (b) Fowler-Nordheim tunneling, (c) thermionic emission and (d) Frenkel-Poole emission.

4.3 Frenkel-Poole Emission

Frenkel-Poole emission is a field-assisted thermally activated hopping process. The high density of structural defects in deposited oxides causes energy states in the band gap close to the bands which are called traps. Due to thermal excitation electrons hop from those traps to the conduction band causing a current. This is the main conduction mechanism in insulators with many defects such as CVD silicon nitride.[20]

$$J \propto \mathscr{E}_i exp\left(\frac{q}{k_b T}\left(2\beta\sqrt{\mathscr{E}_i} - \Phi_B\right)\right)$$

Frenkel-Poole emission occurs mainly at high fields as the current is linearly as well as exponentially voltage dependent. It also depends exponentially on the temperature as well as on the barrier height.
In this case Φ_B is the depth of the potential well of a trap without any voltage applied. Barrier height reduction here is two times the field-dependent Schottky-barrier lowering $q\beta\sqrt{\mathscr{E}_i}$.



(a) Potential well of a trap.

(b) Frenkel-Poole effect.

Figure 20: Change of the barrier height of a trap due to the electric field, figure reproduced from [21]

4.4 Ohmic Conduction

The current-voltage measurements show Ohmic behaviour (J $\propto Vexp\left(-\frac{c}{T}\right)$, c...constant) which is exponentially dependent on T when the electric field is low and thermally excited electrons carry the current through the oxide by hopping between the isolated states.

4.5 Ionic Conduction

Mobile ionic charges are mainly Na^+ and Li^+ as closer described in section 5.2.2. In DC measurements the current caused by this charges decreases over time and space-charge regions - and therefore internal electric fields - close to the metal- and semiconductor-insulator interfaces build up as the charges move there. When the external electric field is removed from the structure not all ions are pulled back to their origin by internal electric fields and therefore a hysteresis can be seen in the I(V) curves. The voltage- and temperature dependence of ionic conduction is $J \propto \frac{V}{T} exp\left(-\frac{d}{T}\right)$, where d is a constant.

4.6 Space-Charge-Limited Conduction

As mobility is very low in insulating materials also space-charge limited conduction is of relevance. This drift current occurs when more charge carriers than the equilibrium amount in the material are injected. Then this injected charge carriers control the space-charge and the electric field profile in the material. This electric field then drives a current which again creates the field. The current dependence on the voltage is quadratic ($J \propto V^2$) and it is only mobility- and not carrier density dependent.

4.7 Dielectric Breakdown

If the electric field $\vec{\mathscr{E}} = \vec{\nabla} V$ applied to an insulating material gets too high breakdown occurs. Breakdown means failure of the insulating properties of the material and results in current flow as the material becomes conductive. This can be explained by the so-called percolation theory which states that this electric field causes defects distributed randomly in the bulk of the insulating layer.

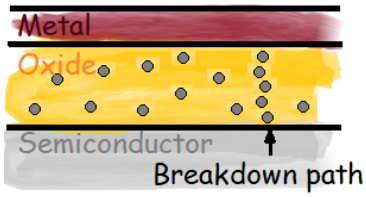


Figure 21: Schematic view of a breakdown path in oxide.

When there are enough defects they may get close enough to build a path connecting the metal and the semiconductor electrically. The voltage at which this happens is called breakdown voltage and the field implied by this voltage gives the dielectric strength.

Experimentally a breakdown can be detected by increasing the voltage until a very large current flows.[14]

4.8 Oxide Pinhole defects

Oxide pinholes are basically points where oxide is missing. When they occur in single oxide layers as shown in fig. 22 they can cause a short between the metal and the semiconductor[22]. Then the MOS structure is like one without an oxide layer and therefore acts like a Schottky diode.

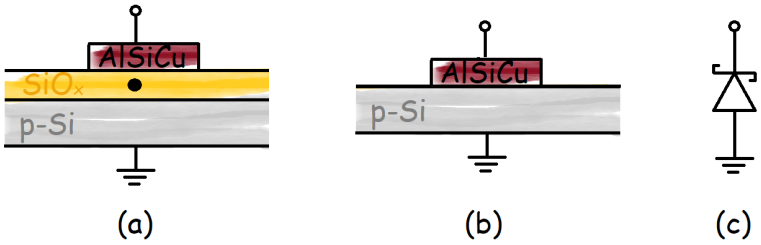


Figure 22: Schematic view of (a) an oxide pinhole defect (black dot), (b) the metal and the semiconductor in contact and (c) the circuit symbol of the resulting Schottky diode.

This behaviour can be detected by IV measurements. If the p-doped Si is connected to ground the Schottky diode is forward biased when a negative voltage is applied to the metal contact.

5 Si/SiO_x States and Charges

In a SiO_x layer there are two general types of charges or states: interface trapped charges (often also called surface states) and oxide charges. Oxide charges can be subdivided in three groups, namely fixed oxide charges Q_f, mobile ionic charges Q_m and oxide trapped charges Q_{ot}.
Oxide trapped charges are described to be defects in a silicon dioxide layer which are neutral and can be charged if electrons ore holes can get into the oxide layer – there are several conduction mechanisms that enable a current flow through the oxide (see sec.4) and may therefore lead to oxide trapped charges. The important thing about all oxide charges is, that they do not depend on the applied bias voltage and can therefore shift the MOS regimes to different voltages. This means that the flat-band point of the structure is shifted and the voltage shift can be calculated by eq. (24).

$$V_{fb} = \Phi_{Al} - \Phi_{Si} - \frac{Q_m + Q_f + Q_{ot}}{C_i} \tag{24}$$

The difference to interface trapped charges is that latter vary their occupancy and therefore charge with the bias voltage whereas oxide charges do not.
There are also charges in the silicon controlling the MOS behaviour, some of them on purpose (dopant ions) and others (bulk traps) unintentionally.

5.1 Interface Trapped Charges

Interface trapped charges result from structural defects implemented in the film deposition step or may be induced by irradiation. These charges are located at the semiconductor-insulator interface. They have random energy levels somewhere in the bandgap or the bands of the semiconductor, but do not communicate with each other (they do not form bands). Interface traps can change their occupancy and therefore their charge with the bias voltage. This happens if the Fermi energy is swept past their energy level. Such traps can be of acceptor type – those are neutral when empty and negative when full - or donor type, which are positive when empty and neutral when full. Both types of traps are located in one device and it is assumed that donor traps are below and acceptor type traps above the intrinsic Fermi level (see fig. 23). They capture and emit electrons or holes, depending on if they are in communication with the valence or conduction band. This interface trapped charges are matter of interest as they are responsible for leakage currents in electrical devices including MOS structures revealing information about the presence of such traps. When performing CG measurements interface trapped charges lead to a broadening of the MOS structures capacitance curves and a peak in the conductance. The reason for the flatter CV curve can be explained by looking at a structure with and one without interface traps. When no interface traps are present, each charge induced in the metal electrode needs to be balanced by a change in the silicons surface charge to ensure charge neutrality, meaning that the bands bend. If there are interface trapped charges present, this band bending leads to a change in their charge density as well. Because of this additional charge density change the silicon surface charge itself needs to change less, which also reduces the band bending. Therefore one simply needs more change in bias voltage to sweep the MOS capacitor through its regimes.

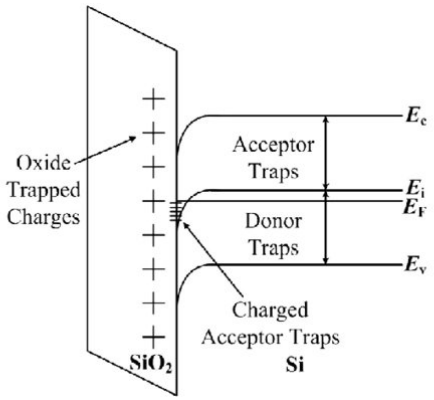


Figure 23: Band diagram of a Si/SiO_x system showing oxide trapped charges as well as donor- and acceptor-like interface traps. Figure reproduced from [23]

Furthermore, the low frequency capacitance C_{LF} curves have a less deep minimum, as the interface trap capacitance C_{it} adds parallel to the semiconductors space charge layers capacity C_{sc}.

$$C_{LF}^{-1} = \frac{1}{C_i} + \frac{1}{C_{it} + C_{sc}} \tag{25}$$

There is a simple method to detect interface traps, namely by measuring the conductance at different frequencies. When surface states are present one can see a peak in the conductance curve due to interface trap loss that changes its position on the voltage axis and its height with the frequency - the peak roams towards the flat band voltage at higher frequencies. This is because the biggest loss occurs at a gate bias voltage where the trap capture rate is comparable to the AC signals frequency. The trap capture rate depends on the number of majority carriers present at the surface – there are a lot of holes in accumulation, so the capture rate is fast, and so little of them towards inversion, that the traps hardly respond and nearly no loss occurs as well. The conductance peak is in between those regimes somewhere in depletion, as less holes than in accumulation are present and the capture rate is reduced, so that the traps cannot keep up with the AC frequency and a loss occurs.
When measuring CV curves at high AC frequencies a hysteresis in the inversion regime can occur. This happens when the traps cannot keep up with the changing DC bias voltage. In the case of a p-type semiconductor interface traps fill with electrons during an up-sweep which basically means that they emit holes. When this process is too slow the depletion layer needs to grow beyond its maximum width and lowers the capacitance. This hole emission delay kind of shifts the flat-band voltage and thus the down-sweep curve is shifted to more positive voltage values compared to the up-sweep curve until the traps regain equilibrium by electron capture at a certain DC bias voltage. [15]

5.2 Oxide Charges

5.2.1 Fixed Oxide Charges

These positive charges are located at the SiO_x-Si interface as well and are distributed randomly. As the name implies they are localized charge centers that cannot be charged or discharged by potential sweeps (in contrast to interface trapped charges). They are built up either during film creation dependant on the process used, the temperature and the crystal orientation of the silicon substrate.[24]
Note that charges located at the silicon-semiconductor interface, namely fixed oxide charges and interface trap charges, can cause the potential at the interface to vary with the lateral location along the interface.[15]

5.2.2 Mobile Ionic Charges

Mobile ionic charges mainly originate from positively charged ions (especially Na^+, K^+ and Li^+) which get enclosed in the material in any of the device processing steps.[25] Na^+ and Li^+ are mobile at relatively low temperatures when a voltage is applied whereas K^+ needs higher temperatures. Therefore measurements at different temperatures make it possible to distinguish between them.
When performing the measurements these positive charges are pulled towards the Si- or the AlSiCu interface inside the SiO_x depending on the polarity of the voltage leading to a hysteresis between up- and down-sweep of a CV measurement. There the flat-band voltage of the down-sweep is shifted to more negative voltages compared to the up-sweep because the mobile ions are located at the interface when starting with a positive bias. As it needs some time to get from one side to the other those ions do not reach the interface during the up-sweep and therefore the hysteresis is bigger for faster DC voltage sweeps.

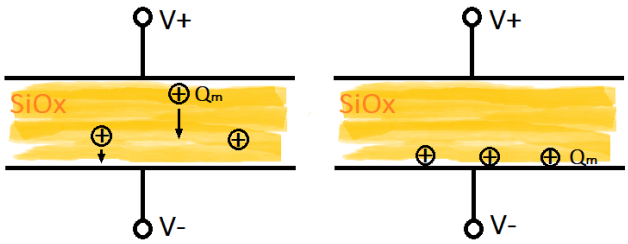


Figure 24: Mobile ionic charges Q_m moving due to voltage.

Heavy metals as well as negatively charged ions also contribute to this charges, but they are only mobile at temperatures higher than 500 °C.[24]

5.2.3 Oxide Trapped Charges

Oxide trapped charges are usually located at the Si/SiO_x or $metal/SiO_x$ interface, but can also be inside the oxide bulk. One reason for them to occur is due to ionizing radiation,[24] another one might be the non-perfect crystal structure of the SiO_x. As bond angles are shifted in the structure it can be energetically favorable to embed or remove an electron in some positions.

5.3 Charges in Silicon

Dopant ions in the Si crystal are randomly distributed and have energies within the bandgap of the semiconductor close to the conduction- or valence band. As their ionization energy is rather small (approximately the thermal energy kT) they are normally completely ionized at room temperature.
Bulk traps usually have one or more energy level near midgap and are evenly distributed in the substrate. Usually bulk traps are heavy-metal impurities that get implanted into the material together with the dopant ions.
Bulk traps fulfill both conditions for efficient generation and recombination of charge carriers. The first one is that the capture and emission rate of charge carriers is about the same. As these rates vary exponentially with the distance from the trap energy level to the valence band for holes and the conduction band for electrons they have to be close to midgap. The second one is that their energy E_T is around the Fermi energy E_F. Then a small change in bias voltage will change the occupancy of these traps a lot resulting in capturing or emitting a lot of charge carriers.
When CG measurements are performed bulk- and interface traps lead to similar shaped CV curves, but can be distinguished by their conductance. Interface traps are best to detect in depletion whereas bulk traps can be detected best in the inversion regime. In strong inversion bulk trap energy levels close to the midgap energy will be crossed by the Fermi energy somewhere in the depletion layer. As the depletion layer width is fixed in this regime this so-called crossover point does not change its position relative to the interface with bias. Thus recombination and generation rates are bias independent. Therefore the conductance stays constant when performing a voltage sweep through the MOS regimes.
Bulk traps dominate the charging of the inversion layer in the strong inversion regime. In weak inversion also interface states can play a role in those processes.[15]

6 Physical Characterization of Oxides

6.1 Ellipsometry

Ellipsometry can be used to measure thickness, uniformity and index of reflection (RI) of a film. Film thickness is an important parameter used for example to calculate the dielectric constant ϵ from electrical measurements. The index of refraction gives information about the composition of the film as it is material dependent. For example stoichiometric SiO_2 has a reflective index of 1.46 [26].

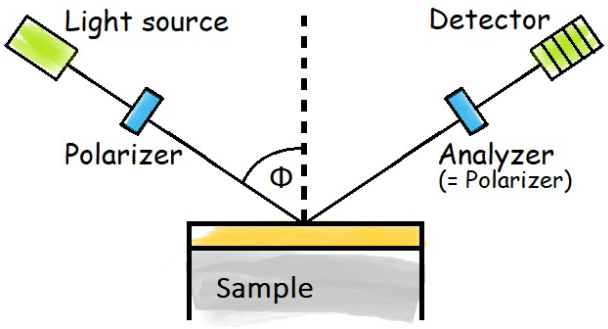


Figure 25: Schematic view of an ellipsometry measurement.

The schematic view of an ellipsometry setup can be seen in fig. 25. Monochromatic light is linearly polarized in a polarizer and hits the sample in a defined angle Φ. The phase difference as well as the amplitude of the s- and p-polarized[‡] parts of the reflected beam change depending on Φ and the thin films properties, namely thickness and refractive index. The light passes a second polarizer to get analyzed in terms of its state of polarization and its intensity is then measured by a detector. [8]

6.2 Fourier Transform Infrared (FTIR) Spectroscopy

Infrared Spectroscopy studies the interaction of matter with light in the infrared range yielding information about what molecules in which concentration are present in a sample. A polychromatic IR light beam gets partly reflected and partly transmitted by the insulating layer of the sample. The transmitted part is reflected by the substrate and both beams hit a collimating mirror and enter the interferometer which acts as basis of any FTIR spectrometer. It splits each IR light beam in two via a beam splitter, one part being reflected by a fixed and one by a moving mirror. The moving mirror induces a position dependent time delay and therefore a phase difference so when the beams are recombined at the beam splitter positive and negative interference alternate resulting in an interferogram. This interferogram is the sum of the interference patterns of each frequency included in the incoming beam.
Each interference pattern is a cosine wave and has a frequency which is called Fourier frequency. The amplitude of the Fourier frequency is the amount of light hitting the detector at that frequency and gets smaller if the sample absorbs

[‡]The electric field of a light beam can be polarized parallel (p) and perpendicular (s) to the plane of incidence.

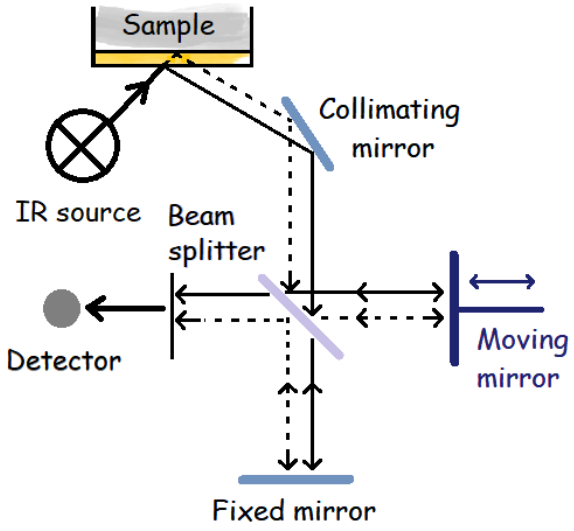


Figure 26: Schematic view of a FTIR measurement setup.

parts of it. This reduction in intensity is a peak in the absorbance spectrum which is obtained from a Fourier transformation of the interferogram.
As molecules with different structures interact with light in different ways they can be distinguished by plotting the IR light intensity for different wavelengths. It is a common way to plot the absorbance over the wavenumber in an IR spectrum. The position of the peaks gives information about the species and the height can be used to calculate the concentration. In this thesis two spectra - one of the plain Si wafer and one with an insulating layer on top - are measured and subtracted from each other. In this way the peaks from the substrate are removed and the species in the insulator can be identified.
More detailed information can be found in *Fundamentals of Fourier Transform Infrared Spectroscopy* by Smith [27] and *Infrared Characterization for Microelectronics* by Lau [28] which were also used to interpret the FTIR spectra measured in this thesis (see sec.14).

6.3 Scanning Electron Microscopy (SEM)

For a high resolution in microscopy the imaging radiation must have a short wavelength. This can be achieved by high energy electrons which are used in SEM. These electrons hit the sample and set free secondary-, Auger- and backscattered electrons, x-rays and photons. Detecting secondary electrons leads to the highest resolution in topography as they can only come from atoms close to the surface where they get knocked out of their orbitals. The contrast for different materials can be seen because also some backscattered electrons reach the secondary electron detector. [29]
In this thesis SEM analysis was used to check trench form and dimensions and to verify the stacking of the desired layers respectively check for unwanted residues occurring from deposition process steps. The resulting images can be seen in section 15.

7 Electrical Characterization

7.1 Four-Point Resistivity Measurements

The advantage of four-point measurements over two-point ones is that no cable or contact resistance enter the measured sheet resistance R_s and therefore the calculated resistivity. Especially when measuring semiconducting materials a Schottky contact with the probing needle may emerge leading to a high contact resistance complicating the result in two point measurements. [30]

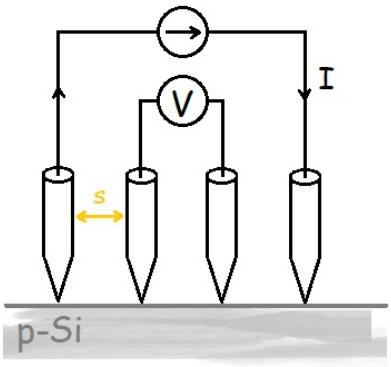


Figure 27: Schematic view of a four-point resistivity measurement.

Four probing needles are placed on the semiconductor in a straight line with equal spacing a between adjacent probes. A current I is sent through the outer probes while the potential V is measured between the inner ones. As the wafer thickness ($t_w = 725$ μm, see sec. 1.1) is about the probe spacing ($a = 1016$ μm, see sec. 12.1) an image charge calculation as deduced in [30] has to be performed to get the resistivity of the measured material.

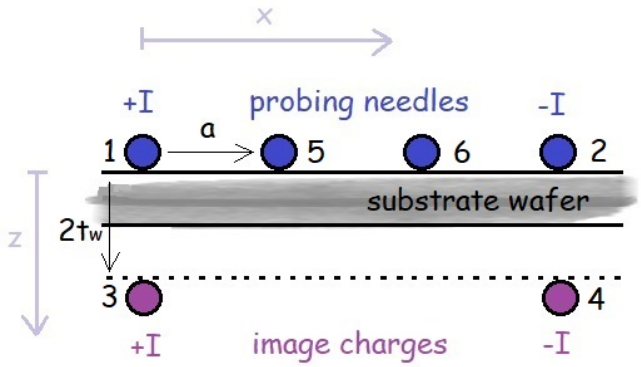


Figure 28: Schematic view of a sample with real and additional mirror current sources.

As all needles and mirror images are placed in one plane the y-coordinate can be chosen to be $y = 0$ for all points. The z-coordinate for the image points is $z = 2t_w$ and their x-coordinates are the same as those of the current contacts

(+I and -I) as can be seen in fig. 28. Therefore the spacing s_{mn} between two points m and n can be calculated by

$$s_{mn} = \sqrt{(x_m - x_n)^2 + (z_m - z_n)^2} \tag{26}$$

resulting in

$$s_{51} = s_{62} = a$$
$$s_{61} = s_{52} = 2a$$
$$s_{53} = s_{64} = \sqrt{a^2 + 4t_w^2}$$
$$s_{54} = s_{63} = \sqrt{4a^2 + 4t_w^2}$$

The resistivity ρ can then be calculated via

$$\rho = \frac{-2\pi V}{I}\left(\frac{1}{s_{61}} + \frac{1}{s_{63}} + \frac{1}{s_{52}} + \frac{1}{s_{54}} - \frac{1}{s_{51}} - \frac{1}{s_{53}} - \frac{1}{s_{62}} - \frac{1}{s_{64}}\right)^{-1} \tag{27}$$

Since the measurement unit (described in sec. 16) assumes a thin film ($t_w << a$) and calculates the sheet resistance via

$$R_s = \frac{4\pi V}{I} \tag{28}$$

this equation has to be rearranged and inserted for $\frac{V}{I}$ in eq.(27). Simplification of this equation yields

$$\rho = \frac{-R_s}{2}\left(-\frac{1}{a} + \frac{1}{\sqrt{a^2 + t_w^2}} - \frac{2}{\sqrt{a^2 + 4t_w^2}}\right)^{-1} \tag{29}$$

Inserting the values for a and t_w the resistivity can be calculated by

$$\rho = R_s \cdot r \tag{30}$$

where the constant $r = 380.9\ \mu$m. The results are shown in sec. 16.

7.2 Capacitance Measurements

The capacitance is defined as the change of charge due to a change of voltage

$$C = \frac{dQ}{dV} \tag{31}$$

The total capacitance C of the MOS system is a series connection of the insulator capacitance C_i and the semiconductor space-charge-layer capacitance C_{sc}

$$C = \frac{C_i C_{sc}}{C_i + C_{sc}} \tag{32}$$

where

$$C_i = \epsilon_0 \epsilon_i \frac{A}{d} \tag{33}$$

depends on the insulating layers thickness d and the area A of the chip measured. C_i corresponds to the maximal measured capacitance. Contrary to this

$C_{sc} = \frac{dQ_s}{d\Psi_s}$ is dependent on the applied bias and on the frequency of the AC signal. The bias voltage varies the space-charge density Q_s as well as the surface potential Ψ_s of the MOS capacitance resulting in the different regimes mentioned in 3.1 which are briefly summarized here for clarity:

$\Psi_s < 0$	Accumulation
$\Psi_s = 0$	Flat-band condition
$\Psi_b > \Psi_s > 0$	Depletion
$2\Psi_b > \Psi_s > \Psi_b$	Weak inversion
$\Psi_s > 2\Psi_b$	Strong inversion

Table 1: Different regimes of a MOS capacitor defined by means of surface potential [14]

where Ψ_b is the potential between Fermi-level E_F and intrinsic Fermi-level E_i in the bulk of the semiconductor (see sec.3).

7.2.1 Space-Charge-Layer Capacitance at Low and High Frequencies

In the accumulation regime (that is, for a p-type semiconductor, when a negative voltage is applied to the metal electrode) there is no space-charge layer (and therefore no C_{sc}) due to the accumulation of holes at the semiconductor surface. Therefore there is no series connection of capacities and the total capacitance is that of the insulator C_i.
In the simplest model the flat-band capacitance is also C_i as the depletion layer width $x_d = 0$. This is often far off the real MOS curve value as any charge variations within the semiconductor are ignored. The semiconductors capacitance at flat-band $C_{s,fb} = \frac{\epsilon_s}{L_D}$ is therefore calculated using the extrinsic Debye Length[†] for holes L_D and adds in series to C_i. Therefore it follows from eq. (32) that $C < C_i$ meaning that the total capacitance sinks.
Increasing the DC voltage depletion is reached and the space-charge layer starts to form and the total capacitance becomes a series connection of C_i and C_{sc}. In depletion and weak inversion C_{sc} can be obtained using the bias dependent depletion width x_d. To get this width the depletion approximation is used. As the space-charge-layer capacitance can be seen like a plate capacitor it can be calculated via $C_{sc} = \frac{\epsilon_s}{x_d}$ and gets smaller while the depletion region gets wider. Therefore the total capacitance further decreases and eventually reaches its low-frequency minimum C_{min} somewhere in the weak inversion regime.
When increasing the DC bias from that point on the measurement curves show a difference for high- and low-frequency AC signals as the steady state CV curve in inversion is defined by (frequency dependant) minority carrier response.
For low frequencies in the inversion regime electron generation and recombination begin balancing the change in voltage to restore the system to equilibrium. When one AC period is longer than the response time for the electrons (the minority carriers in a p-type semiconductor) generation and recombination can follow the signal. Then they can be transported through the depletion layer and only the oxides capacitance is in effect.
When the frequency is too high it is not possible to generate minority carriers in the semiconductor fast enough. The inversion layer cannot form and the

[†]The Debye length is the characteristic length at which the electrostatic potential of a charge has fallen to $\frac{1}{e}$ of its value.

depletion layers capacitance C_{sc} adds to C_i in series. Therefore the capacitance of the MOS structure sinks to an even lower value than C_{min} and reaches its minimum when the depletion layer width reaches its maximum $x_d = m_d^{max}$ in strong inversion. From then on it saturates in high-frequency equilibrium measurements.

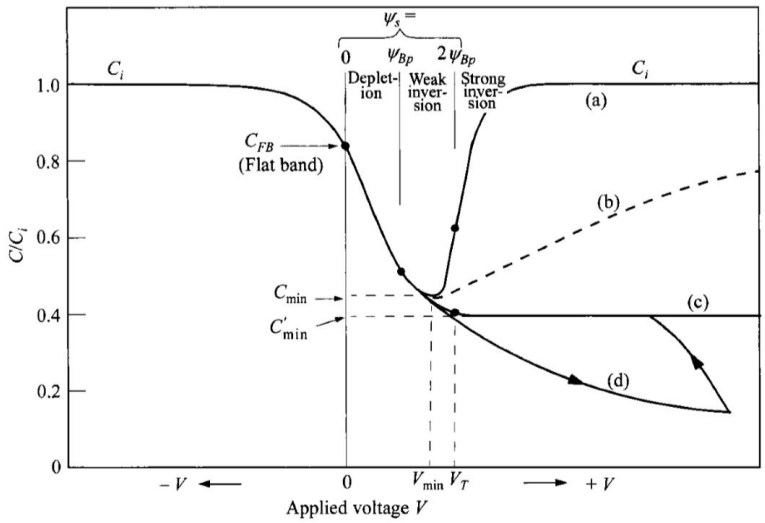


Figure 29: MOS CV curves when V is applied to the metal and the semiconductor side is on ground for a (a) low (b) intermediate (c) high AC frequency. (d) shows deep depletion (fast DC sweep and high frequency). Figure reproduced from [14]

The theoretical CV curves for measurements with different frequencies can be seen in fig. 29. This graphic assumes a flat band voltage of 0 V.[14]

7.2.2 Space-Charge-Layer Capacitance in Deep Depletion

As already mentioned deep depletion occurs when the DC voltage sweep is performed too fast. This effect occurs because positive charges at the metal electrode are built up too quickly for the minority carriers (in the case of p-Si those are electrons) to be generated in an amount needed to compensate those positive charges - and form the inversion layer. Therefore the depletion layer has to fill this role and grows beyond its maximum width to compensate the change in voltage V_a. The total capacitance therefore decreases beyond the high-frequency minimum value and does not saturate. This effect can be seen in curve (d) of fig. 29.
For deep depletion to occur the voltage changes so fast that the MOS structure is out of thermal equilibrium. The speed with which the voltage changes is given by

$$\frac{dV_a}{dt} > \frac{qn_i x_{dd}}{2\tau C_i} \tag{34}$$

x_{dd} is the depletion layer width in deep depletion, n_i is the intrinsic carrier concentration and τ is the minority carrier lifetime.[20] In this case τ refers to the generation life time as there is a paucity of charge carriers in the depletion layer. Generation life time is longer than recombination lifetime (for Si

$\tau_g \approx 50 - 100\tau_r$).[31] As for Si both lifetimes can be rather high (up to $\tau_r = 1$ ms[32]) it might take up to a few seconds to reach equilibrium resulting in deep depletion measurement curves. When increasing the temperature the intrinsic carrier concentration rises as well. Therefore it needs a faster voltage sweep to see deep depletion at higher temperatures.[20]
For a silicon semiconductor it is often the case that the CV measurement curve is in equilibrium for the sweep in the direction of decreasing inversion (down-sweep), but not in the one of increasing inversion (up-sweep) when measuring at room temperature. The reason for this is that the minority carrier recombination rate in Si is bigger than the generation rate. Therefore when sweeping in up-sweep direction no inversion layer can form and charge neutrality has to be ensured by widening the depletion layer width over its equilibrium-maximum x_d^{max} as the bias gets more positive. Therefore the capacitance curve decreases. Still a net current due to minority carrier generation flows towards the Si surface. When the bias is stopped the current flows until an inversion layer is formed, and equilibrium is reached causing an increase in the capacitance as the depletion layer goes back to its equilibrium size. Then in the down-sweep the normal equilibrium curve can be measured. The result is a widening of the measurement curve in the inversion regime.[15]

7.3 Conduction Measurements

The measurement units used always measure two components of the complex impedance modeled for the wafers (see sec.12.2.1 and 12.2.2). Conduction measurements can be used to detect oxide states and charges. As this type of measurement is not the main concern of this thesis this author would recommend *MOS (metal oxide semiconductor) physics and technology* by Nicollian and Brews [15] for further reading.

7.4 Current Measurements

Current-voltage (IV) characteristics can be obtained using either direct- (DC) or alternating current (AC) measurements. Both show a conduction behaviour sensitive to the silicon oxide film structure. In this thesis the focus is on DC measurements which show a much higher dependence on deposition conditions and the following thermal treatment than the AC ones.
As already mentioned conduction in a metal-oxide semiconductor(MOS) capacitor highly depends on the structure and therefore it is also dependent on the purity of the silicon oxide. Improving the quality of the oxide electronic conduction may be observed instead of only conduction due to impurities (mainly mobile ionic charges). It is possible to observe switching between several conduction mechanisms depending on the voltage regime and composition of the oxide. In stoichiometric SiO_2 with high purity it is found that Fowler-Nordheim tunneling is the limiting mechanism.
The field dependencies of the different conduction mechanisms are given in the corresponding sections above (see sec.4). Generally at low electric fields conductance is mainly due to ionic charges whereas at high fields electronic conduction dominates in silicon oxide.When performing the IV measurements several up- and down-sweeps of the voltage between low and high values should be performed, otherwise the curves are not reproducible.[33,19]

8 Treatment after Deposition

Different types of charges are found in Si/SiO_x structures. They affect several properties of the MOS capacitor like threshold and breakdown voltage, leakage currents and stability of the device.[25] Thermal processing can be used to decrease the charge densities and therefore improve device quality.
This chapter will mainly explain the charges and effects of annealing at the example of a silicon - silicon oxide structure.
In general CVD oxides are less dense and include more hydroxyl (OH) groups than thermal ones. Certainly it depends on the precursors and the process used, for example TEOS plasma processes lead, due to ion bombardment, to less OH groups than TEOS LPCVD or silane oxide processes. To get rid of the OH groups and densify the film annealing is performed: the energy provided by the temperature breaks O-H bounds and the hydrogen diffuses to the surface, which also leads to rearrangement of Si-O_x bonds.
In this thesis annealing steps are performed in different gas environments and temperatures.
When a CVD oxide is annealed in oxygen (O_2) atmosphere after deposition the Si/SiO_x interface gets oxidized again which results in less dangling bonds (fast surface states, see sec.5.1). As opposed to this nitrogen (N_2) does not react with the materials and is used to create an inert gas atmosphere.
Annealing thermal oxides with such gases and a high enough temperature is used to reduce mechanical stress in the interface region due to deposition, which can lead to a reduction of fixed oxide charges. The annealing time has to be considered in this case as experiments show that annealing for very long times with high temperatures can as well lead to a re-increase of the density of those charges.[34]
Stress is not always reduced under such conditions. For example in CVD oxides with a typical compressive stress around 100 MPa N_2 annealing with temperatures of around 900 °C and higher leads to even more stress. This is because the silicon contracts more than the oxide when cooling.
Hydrogen annealing is, in contrast to the other two methods mentioned, performed after metalization. The annealing temperature enables hydrogen diffusion to the Si/SiO_x interface where it saturates remaining dangling bonds.
When the annealing process takes place for short times of several seconds at high temperature one speaks of **rapid thermal processing (RTP)**. According to [35] a short O_2 anneal at high temperature ($T > 1000\,°C$) reduces electron traps within thermal SiO_2 which are caused by empty oxygen sites. Furthermore such a rapid thermal anneal (RTA) in oxygen atmosphere does not increase the density of surface states or fixed oxide charges according to this paper.

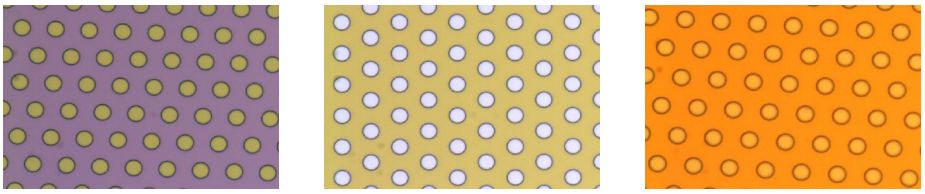
Part II
Experimental

9 Process Flow

The process starts with a lot containing 25 blank Si wafers which get cleaned and imprinted with an identification number by laser encarving. Then the lot is split. 13 Wafers get a trench structure while 12 of them stay planar as reference.
For producing the non-planar structures a SiO_x layer is deposited on the Si substrate. This SiO_x is made via low pressure CVD (LPCVD) using TEOS (Tetraethyl orthosilicate) and oxygen and serves as hard mask in the trench etching process, as photoresist gets decomposed in this process.
In the lithography step a positive photoresist is applied. The so-called L9999 optical mask with the desired trench pattern is placed above it, so that the trench holes get exposed to light and the resist becomes soluble to the developer. The resist then has the shape of the optical mask (fig. 31a) and the wafer can be patterned by means of plasma- and wet chemical etching.

Figure 30: Schematic view of the wafer after structuring of the hardmask.

First, the trenches get formed in the hardmask by a plasma etching process process, then the resist is removed by running both etching processes successively. Afterwards the trenches are plasma etched into the substrate and the SiO_x is removed via wet chemical etching.



(a) Resist after lithography. (b) Etched hardmask. (c) Finished trenches.

Figure 31: Top view of a sample wafer with trenches, photos taken with a microscope.

To check if the etching process yields the right trench form, diameter and depth, scanning electron microscopy (SEM) analysis was performed for several wafers. The SEM images can be found in section 15.
The rest of the process is the same for both, the planar and the non-planar wafers.
For one experiment regarding the series resistance (see sec.17.3.1) and to ensure an ohmic contact between the electric measurement unit and the backside of the wafer a high dose of boron is implanted and activated in a furnace process as preparation for a backside metallization. This step is only done for some

samples and explicitly mentioned then.
Using a PECVD process SiO_x films with different thickness are deposited. Afterwards some of the wafers undergo different annealing steps (shown in table 3) to achieve improvements of the insulating layer by trying to minimize the amount of interface and oxide bulk states. If no annealing process is mentioned explicitly in this thesis the sample did not undergo any annealing process at all. The topmost layer of the structure is a 750 nm thick AlSiCu film which is deposited by sputtering.
It gets tempered to improve electric conductivity of the material. Therefore the wafers are heated in presence of a forming gas (H_2 and N_2 in a non-explosive ratio) also used to saturate dangling bounds in the grain boundaries of AlSiCu, which is where conduction takes place.

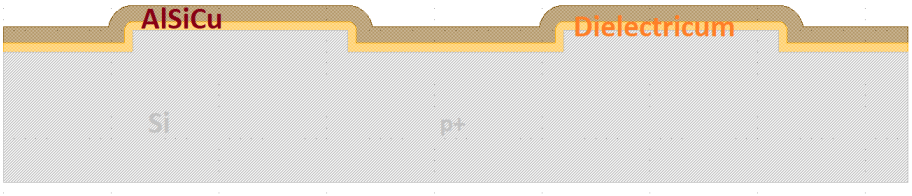
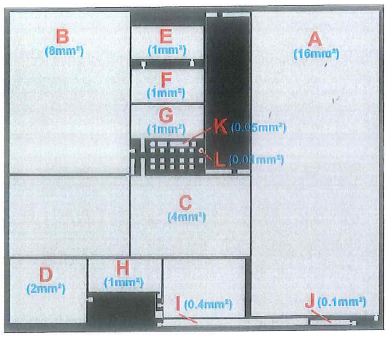
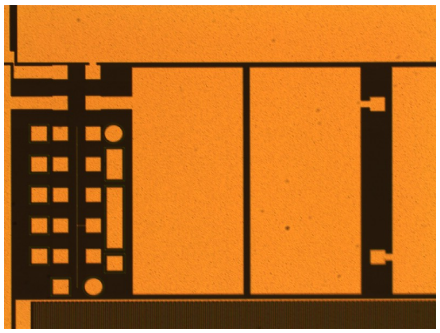


Figure 32: Schematic view of the final front side design of a non-planar wafer.

To structure the electrical contacts again a positive resist is used in combination with the so-called G0900 mask (see fig. 33a). This is followed by a wet chemical etching process and another cleaning process to remove the rest of the resist.



(a) Reticle of G0900 mask.



(b) Microscope picture of a planar wafer.

Figure 33: G0900 mask - electrode areas go from 0.01 mm^2 (L) to 16 mm^2 (A).

Finally another etching process is applied at the backside of the wafers that removes impurities from previous processes to ensure good contact. After this the backside metalization is applied on the wafers that got an additional Boron implant before in a sputtering process.

10 Insulator Formation

To create the silicon oxide layers the PECVD system *Producer* from *Applied Materials* was used. fig. 34 shows the setup of such a reactor.

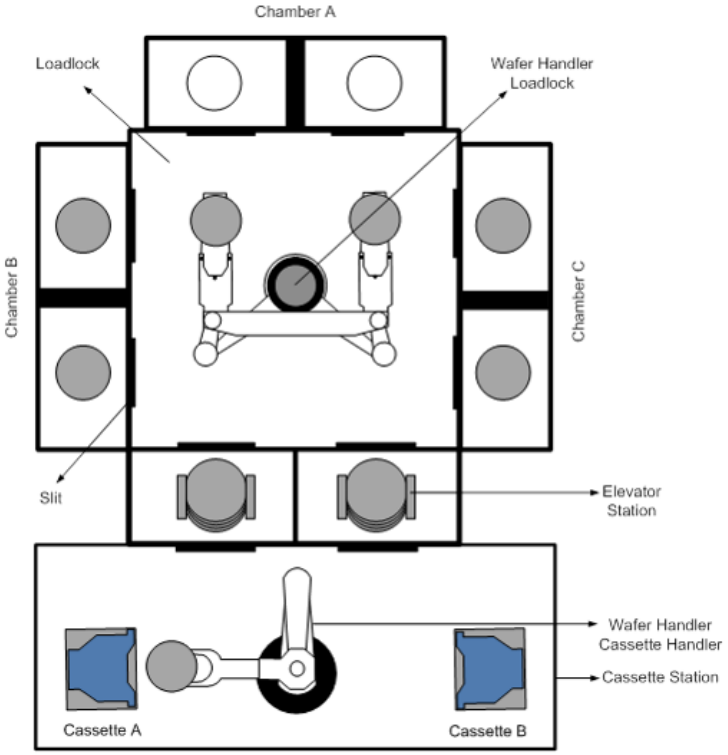


Figure 34: Schematic view of a *Producer* PECVD reactor.

A lot containing up to 25 wafers is placed on the cassette station. The wafers are placed on the elevator station by the automated wafer handler. The twin wafer handler takes two wafers from the elevator station and places them in the two sub-chambers of either chamber A,B or C - depending on which was specified in the recipe. Also depending on the recipe the gas flow, pressure and temperature inside the chamber are adjusted. Once the ambient is stabilized the RF generator initiates the plasma. The reactions taking place in the reactor are shown in fig. 4. After the deposition time specified is up the process is completed and the wafers are removed from the chamber. For the deposition rate to be the same from one deposition process to the next the chambers are cleaned after each wafer. The wafers are cooled in the elevator station and then put back to the cassette of origin.

10.1 Process Parameters

For the deposition of silicon oxide the molecule silane (SiH_4) is used as a precursor. It reacts with nitrous oxide (N_2O) in the presence of plasma in the PECVD system *Producer*. The recipe for deposition was written directly on the tool us-

ing an integrated software. The process parameters can be found in table 2[†]. The temperature T is held constant over the whole process. The pressure p is controlled by a throttle valve which is fully open in the purge-, pump- and first stabilization (Stab1) step. The HF power p is turned on only in the deposition step. The time t of this step controls the film thickness and has to be calculated with the help of the deposit growth rate first.

Step Name	Stab1	Stab2	Dep (100 nm)	Purge	Pump
T	1	1	1	1	
p	open	1	1	open	open
t	0.20	1.00	0.75	0.40	0.08
P	0	0	1	0	0
SiH_4 flow	1	1	0.95	- 1 PU[‡]	- 1 PU
N_2O flow	0.98	0.98	1	0.98	- 1 PU

Table 2: Process parameters in a.u. for the deposition of a 100 nm SiO_x layer with the *Producer* PECVD system.

10.2 Treatment after Deposition

To improve oxide quality by reducing the density of the different oxide states and charges six different annealing steps were performed and evaluated by electrical measurements afterwards. The different anneals were done using different temperatures T for different times t under either nitrogen (N_2) or oxygen (O_2) atmosphere. The different processes used are summarized in table 3.
Two different tools were used for this purpose - a single wafer reactor for rapid thermal processing (RTP) and a horizontal furnace for the longer annealing processes. In the traditional horizontal furnace up to 150 wafers are placed in a quartz boat and heated by heater catridges while in a RTP reactor one wafer at a time is put in a relatively small chamber and heated by a quartz lamp. Latter enables much faster heating and cooling ramps.

Experiment	T in °C	t in min	N_2	O_2	RTP
N1	970	30	x		
N2	1100	30	x		
O1	970	30		x	
O2	1100	30		x	
RTPN	1100	1	x		x
RTPO	1100	1		x	x

Table 3: Process parameters for the the different annealing processes. The **x** mark when a case is true for the according experiment.

[†]As the parameters are taken from productively used processes at *Infineon* they cannot be published here. Therefore they are divided by the biggest occurring value of each variable and given in arbitrary units (a.u.).

[‡]A pump removes the gases from the supply line with open valve between the chamber and the gas box.

11 Physical Characterization

11.1 Thickness and Index of Refraction

The thickness and index of refraction of the thin films were obtained using ellipsometry performed by the *Therma-Wave Opti-Probe 5240* measurement unit. It is suitable for 150 mm and 200 mm diameter wafers and is able to perform in different operation modes. In Beam Profile Reflectometry (BPR) mode it uses a fixed wavelength (670 nm) to measure reflectivity as a function of the angle of incidence. Thickness is measured in spectrometry mode where a wavelength range of (450 - 840) nm is used. [36]
For the *Opti-Probe* to produce reliable results one has to specify the material one wants to measure beforehand (in this thesis the material specified was always oxide). This is because the measuring device compares the measured refractive index (RI) and film thickness with modeled parameters for the specified thin film material. The *Opti-Probe* then provides a parameter called Goodness of Fit (GOF). The GOF gives an idea of how accurate the measured values are for this specified material of the thin film.

11.2 Absorbance Spectrum

The FTIR absorbance spectrum was obtained using the *Bio-Rad QS-500* measurement tool. A wafer has to be measured twice to get the spectrum for the oxide film, once before and once after deposition. The spectrum of the bare Si wafer has to be chosen as background spectrum and gets subtracted from the spectrum of the wafer with the oxide layer on top by the *QS-500*.
Typically a wavenumber range of (400 - 4000) cm^{-1} is chosen for which the absorbance of the sample is measured.

12 Electrical Characterization

Capacitance and conductance (CG) as well as current (IV) measurements with voltages covering all different regimes of a MOS capacitor were used to spot interface and oxide charges as well as to find out about the conduction mechanisms in the insulator for wafers with different topography and differently fabricated insulating layers with varying thickness. Therefore high- and low frequency AC measurements as well as DC measurements were performed with two different measurement units (sec.12.2.1 and 12.2.2).
All CG and IV measurements were done using a two-point measurement method. A DC voltage sweep - in the case of CG measurements with a small overlying AC signal - were performed. Therefore the backside of the wafer was connected to ground via the chuck of the measurement unit while the voltage was applied on the front side connecting a chip of the G0900 mask with a needle.
The sheet resistance of the unprocessed Si substrates was obtained by a four-point measurement (sec.12.1).

12.1 Sheet Resistance Measurements

According to the manual [37] the *OmniMap RS75* is a four-point probe sheet resistance measurement unit for (50 - 200) mm wafers. It enables sheet resistance measurements from 5 mΩ/sq to 5 MΩ/sq with an accuracy of ±1 %. Sheet resistance is the resistance per unit area and for a substrate way thinner than the probe spacing - which is specified to be $a = 0.04$ inches ($a = 1016\mu$m) - the output value of the RS75 is calculated via

$$R_s = \frac{4\pi V}{I} \tag{35}$$

where V is the applied voltage and I the flowing current. As in this thesis the wafer thickness is about the probe spacing eq. (30) is used to get the resistivity instead of the proposed formula $\rho = R_s \cdot t_w$ by the manual.
The sheet resistance measurements were performed on five points per wafer.

12.2 Capacitance, Conductance and Current Measurements

12.2.1 UF2000 Wafer Probing Machine

The *UF2000 Wafer Probing Machine* is the hardware used to transmit the electrical signals from a measurement unit to the wafers. A wafer is contacted with the chuck on the backside and a probing needle on the metal gate of pad B (fig. 33a) on the front side to close the electrical circuit. The needle used for the measurements is the middle one of three of the $L4x - L7x$ needle card. An important parameter to adjust for the prober is the overdrive. After the machine auto-adjusted its needle height for a sample the overdrive controls how much deeper than this value the needles get pushed for the measurement. Due to small height differences of the different chips on a wafer (due to non-uniformity within the sample or due to the measurement setup) a few micrometers of overdrive enables a good contact between all chips and the needle used for measurement. On the other hand one has to choose this parameter carefully because a value too big might result in pushing through some layers (in the worst case the whole

SiO_x film) of the sample to be measured.
Two different devices were used in combination with the *UF2000 Wafer Probing Machine*, namely the *E4980 A/AL LCR Meter* and the *B1505A Power Device Analyzer* both from the company *Keysight*.
The software controlling the cooperation of the prober and the measurement units is *KNPMP*. It is developed by *Infineon Technologies* in cooperation with *KAI GmbH* using the underlying software *LabVIEW* from *National Instruments*. It is responsible for communicating entered measurement parameters as well as for processing and storing the measured data. It was found that an overdrive between 30 and 40 μm works best for the samples with 100 nm SiO_x thickness used in this thesis.

E4980 A/AL LCR Meter

This measurement unit can be used to evaluate electrical components - namely inductance (L), capacitance (C) and resistance (R) - as well as semiconductor devices and other materials. As all real electrical components have parasitic components they are modeled as a complex impedance. The LCR meter then measures two components of this impedance simultaneously. For the measurements performed in this thesis capacitance (C) and conductance (G) as well as current (I) and voltage (V) were chosen as pairs.
The *E4980 A/AL LCR Meter* provides a DC bias voltage in the range of up to ±40 V and AC signals with frequencies in a range between 20 Hz and 2 MHz.

CG Measurements

Based on the expected small capacitance of the MOS structure a parallel circuit mode was chosen over a series one for the capacitance measurements. The equivalent circuit for the impedance is shown in fig. 35.
For the results to be reliable the parallel resistance R_p must not be smaller than 10 kΩ according to the manual [38].

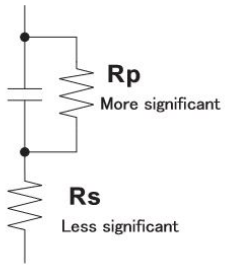


Figure 35: Equivalent circuit of the measured impedance. When the capacitance is small the parallel resistance R_p has more effect on the impedance than the series resistance R_s. [38]

As already mentioned the CG measurements were performed with an additional AC Voltage superposing the DC voltage. The amplitude of the AC voltage was chosen to be 1 V.

IV Measurements

To detect possible leakage currents through the oxide and determine the con-

duction mechanism(s) present IV measurements were performed using a DC bias voltage. The test signal voltage and current are measured at the same time here.[38] In the best case the accuracy of the measured current is 45 nA for an impedance > 30 kΩ.[39] As the measured leakage currents of the MOS structure can be as small as a few nanoampere this resolution was simply too bad and therefore, after rough characterization, the second measurement unit -the *B1505A Power Device Analyzer*- was used for IV Measurements.

B1505A Power Device Analyzer

The *B1505A Power Device Analyzer* in combination with a High Power Source Monitor Unit (HPSMU) as a plugged-in module enables a measurement range of up to ± 200 V and ± 1 A. Therefore this analyzer is suitable for breakdown measurements even at 100 nm oxide thickness. Using the HPSMU an accuracy of the applied DC bias voltage of 2 mV for measurements in the range of ± 40 V and 5 mV in the used measurement range above is possible. The accuracy of the measured current can be as good as 50 fA in a current range smaller than 1 nA and 500 fA between 1 and 11.5 nA.[40]

12.2.2 Parameter Analyzer

In this case the wafer was hand-placed on a movable chuck and fixed using vacuum. The needle used for the measurements was contacted to metal pad B (fig. 33a) using a micropositioner and a light microscope. Needle as well as chuck were then connected to the *Keithley Parameter Analyzer 4200A-SCS*, which is a fully-integrated measurement unit able to perform the desired CG as well as IV measurements. For this purpose it includes i.a. a Source-Measure Unit (SMU) and a Multi-frequency capacitance-voltage unit (CVU).
It uses the *4200A-SCS Clarius* software to control the measurement and analyze the obtained data.

CG Measurements

The CVU enables frequencies between 1 kHz to 1 MHz and an AC root mean square voltage between (10 - 100) mV with an DC bias of $\pm$ 30 V[41]. The DC bias can be swept in time while the magnitude of the AC voltage and the frequency are fixed.

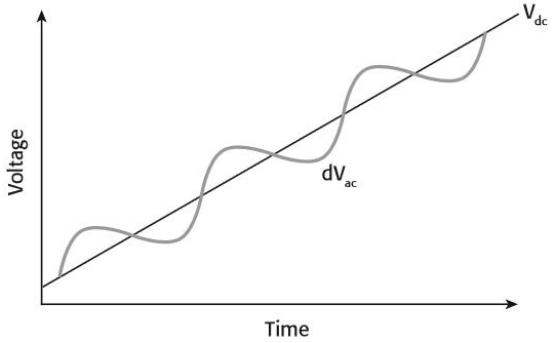


Figure 36: DC voltage sweep with overlying AC voltage for the CG measurements.[42]

IV Measurements

To measure such low currents as leakage currents in a MOS capacitor the *Keithley Parameter Analyzer 4200A-SCS* enables very low current measurements with a resolution of 10^{-16} A. Therefore it uses a very sensitive ammeter. As there are small leakage currents from the *Parameter Analyzer* itself, the cables, probes and so on a measurement of the noise floor has to be performed. This offset current can then be subtracted from the measured current to obtain more accuracy.

DC voltage ramp measurements can be performed to detect the breakdown voltage of the insulating layer in the MOS capacitor. The breakdown can be seen by a sudden increase in the measured current.[43] The SMU enables voltage measurements in a range up to 210 V.[42]

Part III
Results and Discussion

13 Film Thickness

The thickness of the silicon oxide films was obtained as described in sec.11.1 for nine points per wafer. For annealed samples a measurement before and after the treatment was performed to see if the thickness of the layer changed during such a process.
The results showed that differences in SiO_x thickness within one wafer averagely were in the range of $1 - 2$ nm. The thickness variation of the layer thickness within one lot was a bit higher with up to 5 [†] nm. This is mainly because the two different sub-chambers used (see fig. 34) have slightly different deposition rates.
The different anneals shown in table 3 resulted in different outcomes of the final layer thickness.
As during thermal treatment in nitrogen atmosphere (Experiments N1, N2, RTPN) the silicon oxide film got nitrided the *Opti-Probe* did not provide exact results when measuring afterwards. This could be seen in a GOF lower than 0.97. As already mentioned in sec.11.1 the measurement unit compares measured data to a model of a specified material - in this case oxide - and then calculates the GOF giving an idea of the accuracy of the results. Still it seems that the layers did not grow by annealing in nitrogen ambient.
Also the rapid thermal anneal in oxygen atmosphere (RTPO) did not result in additional layer thickness Δd, other than the two 30 minute anneals in nitrogen atmosphere (O1, O2). During thermal treatment in oxygen atmosphere the O_2 diffuses to the silicon - silicon dioxide interface and oxidizes the silicon there increasing the amount of SiO_x. Apparently the time of the rapid thermal anneal is not long enough for this process to lead to noticeable effects.

Experiment	Δd in nm	GOF
N1	0	<0.97
N2	0	<0.97
O1	+15	≥ 0.97
O2	+60	≥ 0.97
RTPN	0	<0.97
RTPO	0	≥ 0.97

Table 4: Layer thickness growth after the different anneals for samples with an initial SiO_x thickness of 100 nm.

[†] Before thermal treatment.

14 FTIR Absorbance Spectra

Before discussing the electrical measurements of the MOS capacitors the FTIR absorption spectra of different SiO_x layer are shown.
The spectra were fitted with a *MATLAB* program written by Daniel Pieber [44] using several polynomial functions in different areas to obtain a flat baseline. The program also calculates the position of the maxima and the peak heights according to the spectrum.

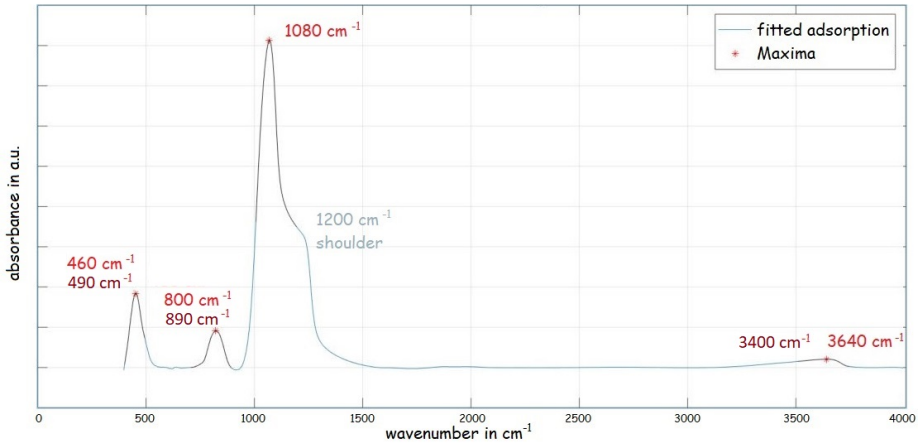


Figure 37: Fitted absorbance spectrum of an 800 nm SiO_x layer.

The position of the different peaks seen in the spectrum reveal the chemical content and the type of molecular vibration and were identified using the infrared spectrum of silicon dioxide from [28] as a reference.
The three peaks marked at 460, 800 and 1080 cm^{-1} result from Si-O bonds in the SiO_x film. The most prominent peak at 1080 cm^{-1} is due to Si-O bond stretching while the other two are due to bending of O-Si-O and Si-O-Si bonds. Si-N asymmetric (890 cm^{-1}) and symmetric (490 cm^{-1}) stretching close to the SiO bending peaks and may as well be present and contributing to the peaks.
The fourth marked peak at 3640 cm^{-1} indicates water contamination. It is attributed to O-H stretching in Si-OH bonds. Water contamination also can lead to a second peak due to O-H stretching at 3400 cm^{-1} - this time in H_2O structures. This peak cannot be seen directly in fig. 37 but there is a rise in the absorbance spectrum around this wavenumber. This peak is to be avoided in MOS devices as hydrogen containing species can lead to a lot of electron trapping.
Using silane (SiH_4) as a precursor reactions with the water present in the ambient may take place leading to SiOH bonds in the silicon oxide layer. Those SiOH bonds make the film more hydrophilic also leading to the adsorption of water molecules that can cause performance problems in a device. [45]
Close to the prominent 1080 cm^{-1} peak a shoulder can be seen at about 1200 cm^{-1}. According to [46] it is due to Si-O-Si stretching in a large void. It is stronger the lower the refractive index and therefore the density of the material is indicating a high porosity.

In high quality thermally grown silicon dioxides a peak at 1255 cm^{-1} can often be seen. It occurs due to the Berreman effect as an additional feature of the Si-O peak at 1080 cm^{-1}. It occurs when thin films are deposited on metal or semiconductor surfaces due to leaky waveguiding. Its absence together with a broadening of the Si-O peak gives rise to a disordered silicon oxide layer. [47,48]

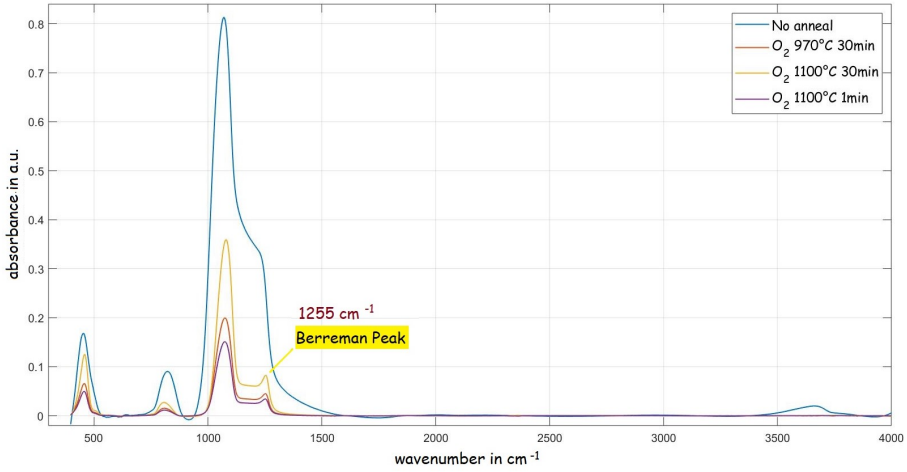


Figure 38: Fitted absorbance spectrum of four wafers with differently treated SiO_x layers.

In fig. 38 one can see that the oxygen annealed samples clearly show this Berreman peak whereas the untreated PECVD layer does not. It is either not present or covered under the shoulder at 1200 cm^{-1} mentioned before which would both indicate a disorder in the unannealed SiO_x layer.
Together with the fact that the water contamination peak at 3640 cm^{-1} is not visible in the annealed samples anymore this indicates a quality improvement of the layer after annealing.
Another indicator for quality is the exact position of the highest peak due to Si-O stretching. The closer it is to the theoretical value of 1080 cm^{-1} for SiO_2 the closer the composition of the PECVD SiO_x layer to that of stoichiometric silicon oxide. The exact positions of this peak obtained for the differently treated samples can be seen in table 5 which shows that the 30 min oxygen anneal at 1100 °C (experiment O2, see tab.3) leads to the best result.

Thermal treatment	Peak position in cm^{-1}
none	1069
O1	1076
O2	1080
RTPO	1072

Table 5: Wavenumber of the Si-O stretching for differently treated wafers.

The height difference in the peaks for the different samples shown in fig. 38 is mainly due to the thickness of the insulating layers as a thicker layer is to absorb a higher amount of radiation. Standardizing the curves by division by their maximum value shows that the FTIR spectra of the three anneals in oxygen atmosphere are nearly identical which can be seen in fig. 39.

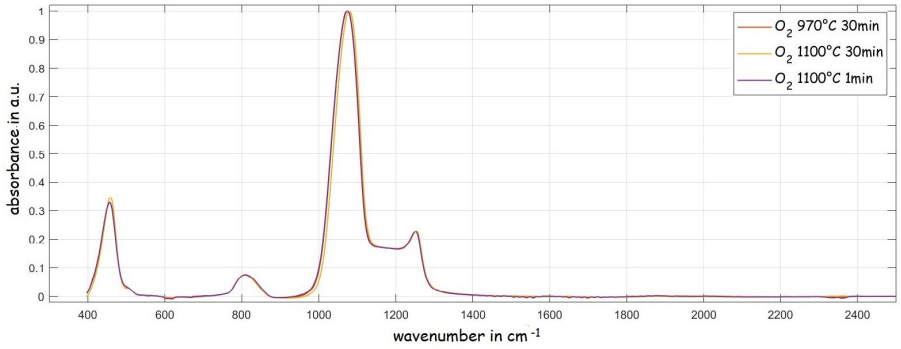


Figure 39: Standardized absorbance spectrum of the annealed wafers.

15 Cross-Sections

The following pictures obtained by scanning electron microscopy (SEM) were performed by the department for failure analysis (FA) at *Infineon*.
SEM was performed to validate the production process, i.e. the form of the trenches, the thickness of the oxide layer inside the trenches etc. In fig. 40 the cross-section of a trench is shown. This picture was chosen for measuring the dimensions of a trench because the wafer was broken in a way that pretty much half of the trench was left and the diameter could be obtained. The measurement was performed using the software *DIPS - Digital Image Processing System* developed by *Infineon Technologies*. It was done by calibrating the measurement cursors of the software with the help of the size scale that is imprinted in the right lower edge by the FA.

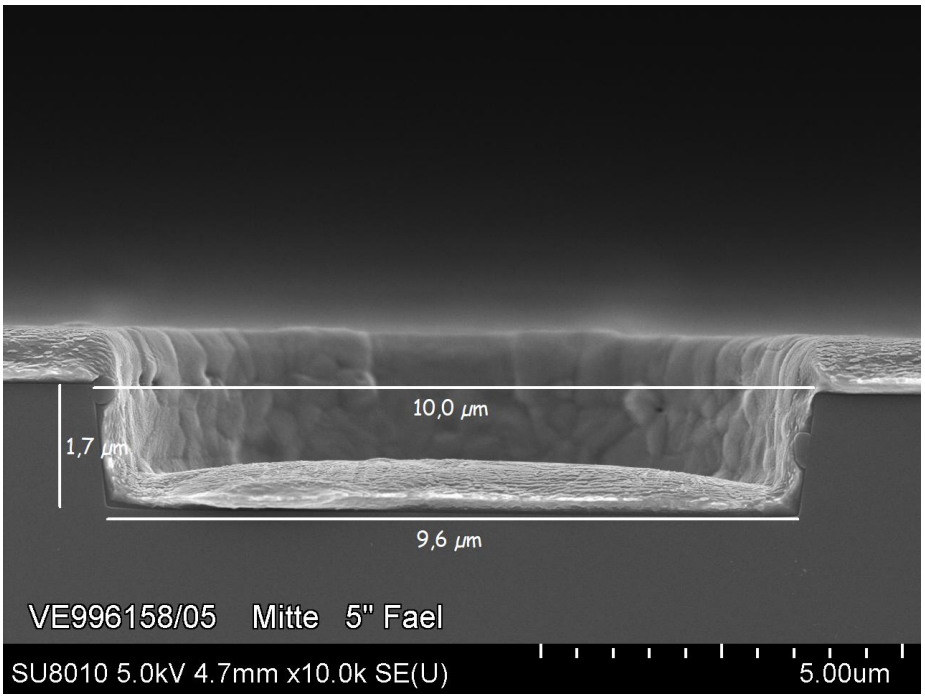


Figure 40: SEM picture of wafer 05 of a completely processed lot used to determine the dimensions of a single trench. The size scale equals 5 μm.

Also SEM pictures of other wafers were measured with *DIPS* and showed the same dimensions as wafer 05. The trench height was $h = 1.7$ μm, the diameter at the trench bottom is $d_{T,b} = 9.6\mu$m and the one at top is $d_{T,t} = 10.0$ μm. Using these values and the spacing between two trenches which was also 10 μm the additional area for the wafers with trenches was calculated via

$$A_t = \frac{(d_{T,t} + d_{T,b})}{2} m\pi \tag{36}$$

Where $m = \sqrt{(\frac{(d_{T,t} - d_{T,b})}{2})^2 + h^2}$ is the length from one lower edge to the upper one. From the ratio of the total surface area of a wafer with trenches and a planar

one $\frac{A_t+A_p}{A_p}$ a correction factor $c_A = 1.17$ was calculated. This correction factor was multiplied with the size of the pad on which the electrical measurements were performed for wafers with topography to calculate the dielectric constant (eq. (33)) an will be further discussed in section 17.2.

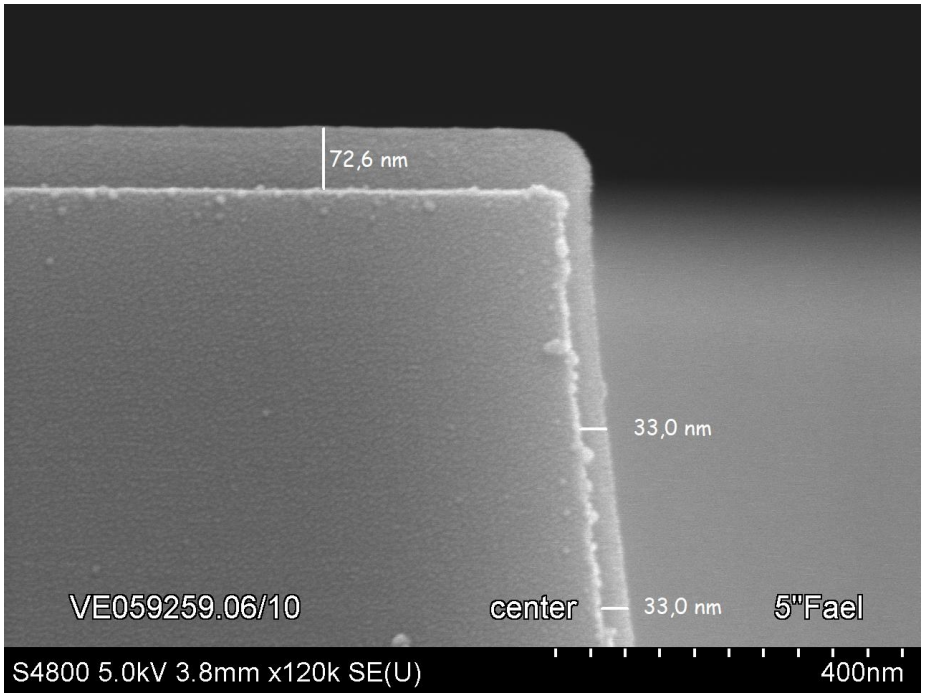


Figure 41: SEM picture of the upper edge of a trench in the center of wafer 10 with a target oxide thickness of 70 nm. The size scale equals 400 nm.

Also a correction factor for the oxide thickness was calculated from *DIPS* measurements of SEM pictures, this time of another wafer with a target oxide thickness of 70 nm. As step coverage is not as good as the coverage of a planar area the oxide layer is thinner at the side walls and the bottom of the trench. In fig. 41 one can see the oxide thickness on the area without trenches (72.6 nm) versus the thickness on a trench wall (33.0 nm). These values are only as accurate as the placement of the cursors is possible. Furthermore it is not clear how uniform the oxide thickness inside different trenches is and therefore an error of 2 nm was estimated.
In fig. 42 the bottom of the same trench is shown where the oxide thickness is 59 nm. Using those thickness values and the calculated areas where they apply an correction factor for the SiO_x thickness of a trenched sample of $c_d = 0.88$ is obtained.

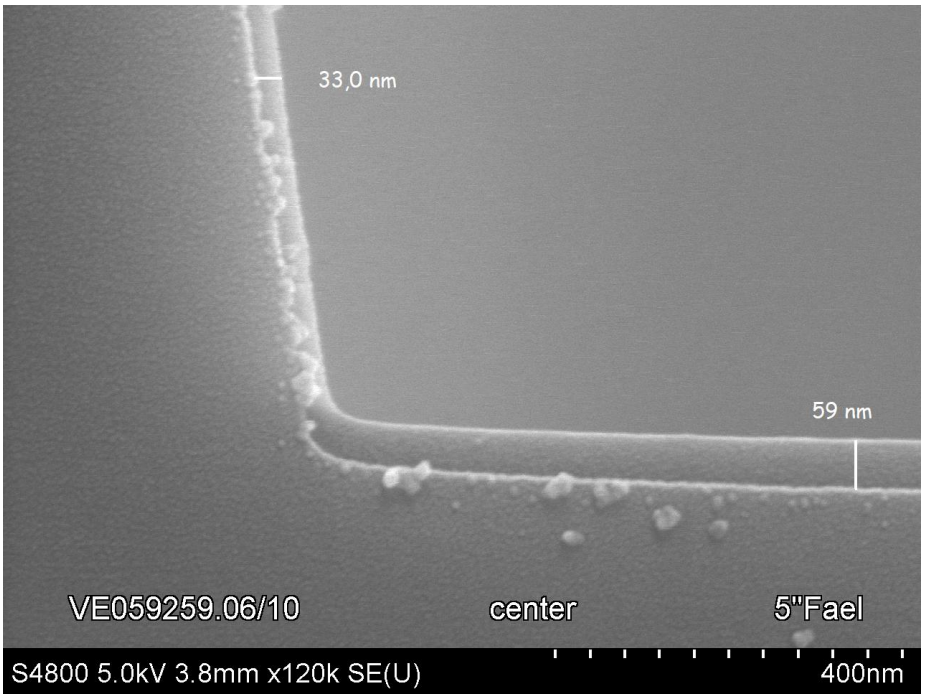


Figure 42: SEM picture of the lower edge of a trench in the center of wafer 10 with a target oxide thickness of 70 nm. The size scale equals 400 nm.

In fig. 43 one can see a close-in of a trench of the same wafer as in fig. 40 where 10 nm SiO_x was deposited. The layer thickness was measured on the planar wafers coated in the same chamber and process run using the *Opti-Probe* measurement unit described in sec.11.1. The results for 10 nm deposition in chamber A1 in which this wafer (05) was coated were (13.5 ± 0.2) nm and (13.4 ± 0.2) nm. Looking at fig. 43 one can see the oxide layer as very thin bright line directly at the Si-substrate. On top of it there is the AlSiCu layer for the gate electrode. The oxide thickness was measured at the trench bottom using *DIPS* again and gave about 12.9 nm oxide thickness. The accuracy of this value is again limited by the resolution of the image and the precision of placing the measurement cursors in the software and had to be estimated depending on the scaling of the SEM picture. For the oxide layer in this SEM image at least 3 nm have to be taken as an error value as the film becomes blurred towards the substrate and is very thin.

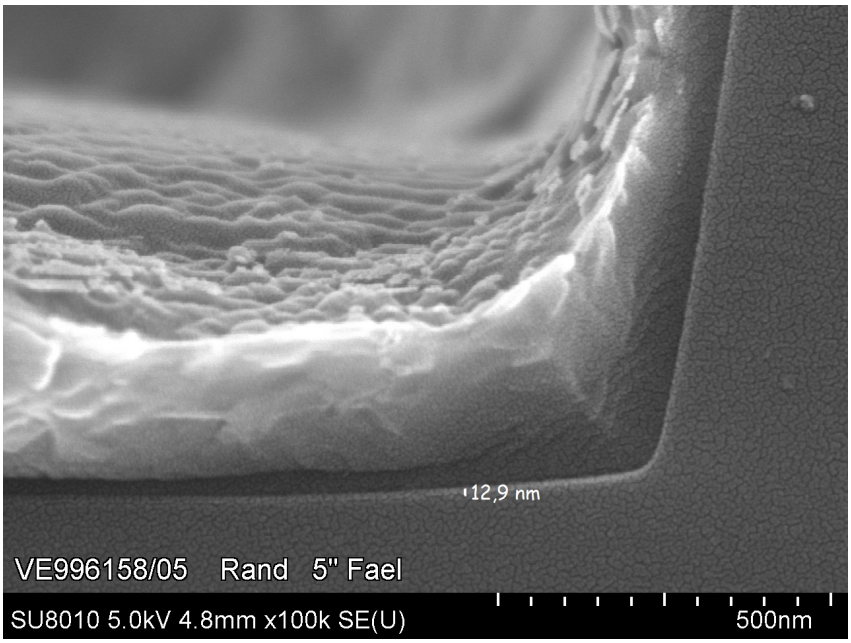


Figure 43: SEM picture of a trench of wafer 05 from a completely processed lot. The size scale equals 500 nm.

A less detailed picture of the same wafer can be seen in fig. 44. It shows the grains of the electrode material AlSiCu and gives a good overview over the topography of the trenched wafers.

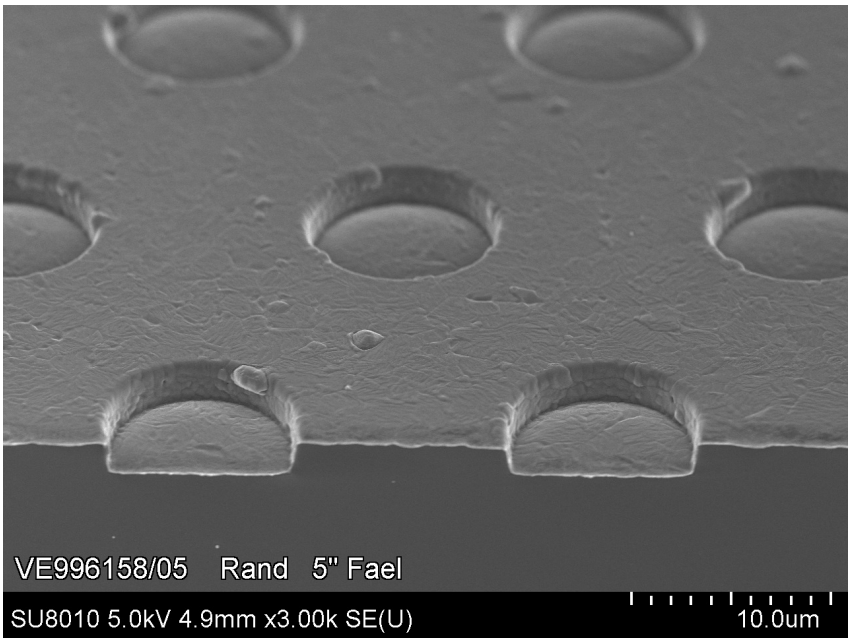


Figure 44: SEM picture of wafer 05 from a completely processed lot. Several trenches covered in AlSiCu can be seen. The size scale equals 10 μm.

16 Resistivity

As mentioned in sec.1.1 two different p-doped substrate materials were used. CG and IV measurements using the *P032* substrates did not provide any useful results but noise. Therefore *M118* was the substrate material of choice and all further measurements presented in this thesis were done using wafers of this material only.
As the specified resistivity range for *M118* substrate wafers is quite high (between $\rho = 1 - 1000\ \Omega cm$) 4 point sheet resistance measurements (as described in sec.7.1) were performed using the OmniMap RS75 sheet resistance mapping system (see sec.12.1).
The sheet resistance R_s was measured in 5 different locations on each wafer before any process steps were performed. At least three wafers per lot were measured. Resistivity- as well as SiO_x layer thickness measurements were only performed on planar samples, as both measurement devices are not able to deal with topography on a wafer.
Table 6 shows typical sheet resistance values for the samples used.

Measurement point	R_s in Ω/sq		
	Wafer 14	Wafer 19	Wafer 25
1)	112.6	110.3	110.8
2)	111.4	109.0	111.7
3)	110.4	111.9	112.6
4)	112.0	112.4	113.7
5)	113.2	112.6	113.6

Table 6: Results of the resistivity measurements for an example lot 1.

To get the resistivity ρ the values measured had to be multiplied by the the factor $r = 380.9\ \mu$m as described in sec.7.1. Using the average sheet resistance $\bar{R}_s$ for each wafer the average resistivity $\bar{\rho}$ for this exemplary lot is

	Wafer 14	Wafer 19	Wafer 25
$\bar{R}_s$ in Ω/sq	111.9	111.3	112.5
$\bar{\rho}$ in Ωcm	4.3	4.2	4.3

Table 7: Average sheet resistance $\bar{R}_s$ and average resistivity $\bar{\rho}$s for example lot 1.

As can be seen in table 6 the sheet resistance - and therefore the resistivity - of one wafer and within a lot was basically constant within a small tolerance. Most of the lots used in this thesis showed an average sheet resistance between $\bar{R}_s = 100 - 130\ \Omega/sq$ and therefore $\bar{\rho} = 3.8 - 5.0\ \Omega cm$. With the help of [3] the corresponding Boron doping concentration was calculated to be in the range of $N_A = (2.8 - 3.6) \cdot 10^{15}\ cm^{-3}$.
Only one of the lot showed higher resistivity. The measurement results are shown in table 8.

Measurement point	R_s in Ω/sq		
	Wafer 18	Wafer 21	Wafer 23
1)	302.0	297.7	300.8
2)	err.	err.	err.
3)	297.9	296.2	306.9
4)	298.3	301.9	306.1
5)	303.7	298.6	304.8

Table 8: Results of the sheet resistance measurements for an example lot 2. The second point was not measurable and produced an error.

	Wafer 18	Wafer 21	Wafer 23
$\bar{R_s}$ in Ω/sq	300.5	298.6	303.1
$\bar{\rho}$ in Ωcm	11.4	11.4	11.5

Table 9: Average sheet resistance $\bar{R_s}$ and average resistivity $\bar{\rho}$s for example lot 2.

For this lot the doping concentration was around $N_A = 1.2 \cdot 10^{15}\ cm^{-3}$ [3]. With the doping concentrations further physical quantities could be calculated. One example is the flat-band voltage of the MOS capacitor, which depends on the work function difference of the metal and the semiconductor used and is therefore altered by the doping concentration of the silicon substrate. It lies around $V_{fb} = -0.88\ to\ 0.89\ V$ for the lots with lower resistivity and at $V_{fb} = -0.86\ V$ for the lot with the higher one according to [16]. This simply means that for different doping concentrations the MOS regimes are shifted a little on the voltage axis†.

†As the work function of silicon does not change a lot within such doping concentration variations there is only a slight shift of the regimes and V_{fb}.

17 General Electrical Characterization

All electrical measurements (CG as well as IV) were performed on the 8 mm^2 chip of the G0900 mask (see fig. 33a). This chip was used in every measurement for reasons of reproducibility.

CG measurements were performed using the *LCR Meter* combined with the *UF2000* (sec.12.2.1) prober as well as the *Parameter Analyzer* (sec.12.2.2).
Performing those measurements a DC bias voltage combined with an AC signal was swept through the different MOS regimes. The amplitude of the overlying AC signal was chosen to be 0.1 V for measurements with the Parameter Analyzer and 1 V for measurements with the UF2000 measurement unit as measurements were most stable with these values. The frequencies of the AC signal were chosen between 50 Hz and 100 kHz. Above that too many disruptive interference from different parts of the measurement unit and the environment play a part and therefore those measurements are not representative. Below 50 Hz signal noise was too strong.

IV measurements were performed using the *LCR Meter* and the *B1505A* measurement unit together with the *UF2000* probing machine (sec.12.2.1). In this case only a DC bias voltage was applied.
Other than in the CG measurements DC voltages higher than those needed to cover the MOS regimes were applied in the IV measurements for the aim of identifying the different conduction mechanisms through the oxide layer (the most common ones for silicon dioxide are described in section 4).

17.1 Open Measurements

To determine the offset of the different current measurement units open measurements were performed. Therefore the probing needles were lifted so that no contact to the sample was given. The following figures show the outcome for the *B1505A*, the *LCR Meter* and the *Parameter Analyzer*.
As can be seen in fig. 45 the IV measurement using the *LCR Meter* shows noise around -1.7 nA with deviations of up to 2 nA. As already mentioned in sec.12.2.1 the accuracy given by the manufacturer is 45 nA. This measurement unit was therefore only used for a rough IV characterization of the samples.

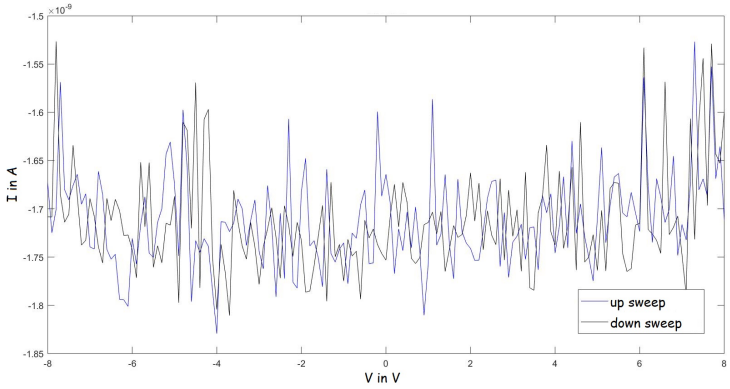


Figure 45: Open IV measurement performed with the *LCR Meter*.

Measurements performed with the *B1505A* measurement unit reveal more accuracy. Looking at fig. 46 the noise is way smaller (~ 10 pA), but bigger than the one given by the manufacturer (see sec.12.2.2) in the femtoampere regime.

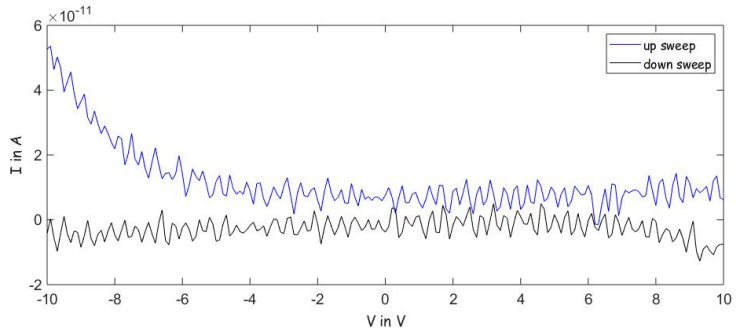


Figure 46: Open IV measurement performed with the *B1505A*.

When measuring up to higher voltages a small ohmic influence of the measurement setup can be seen (fig. 47). The current rise towards zero volt that can be seen here and in the up-sweep of fig. 46 is most probably an artefact due to the measurement setup.

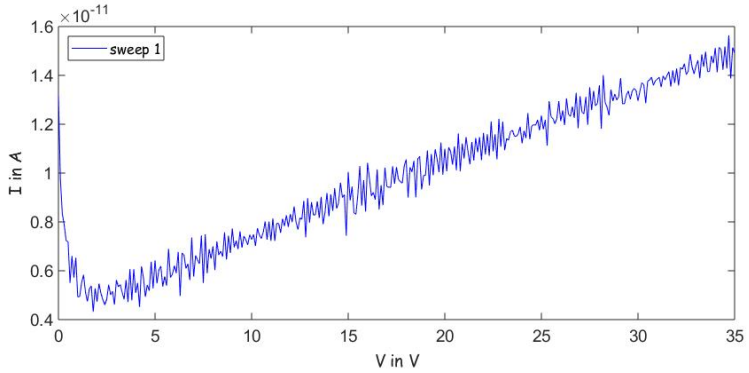


Figure 47: Open IV measurement performed with the *B1505A*.

In comparison almost no noise can be seen in the open IV measurement (fig. 48) using the *Parameter Analyzer*. In the measured voltage range of ±10 V the current rises from about −0.8 to 0.8 nA in a rather linear and symmetric way and covers noise that is visible in smaller current ranges. This linear behaviour is very likely a result from some parasitic ohmic resistance from the cables used for measurements.

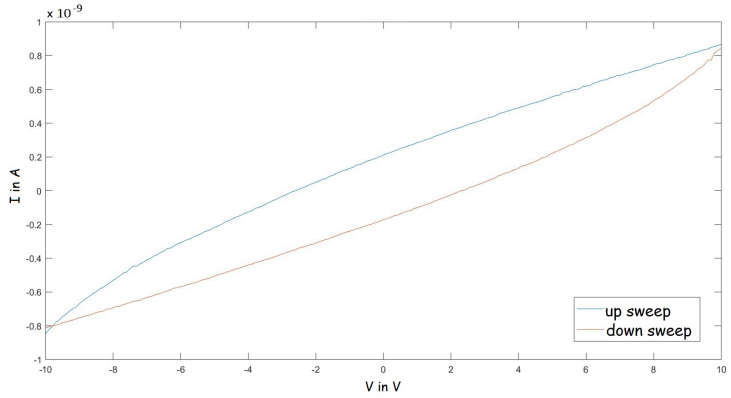


Figure 48: Open IV measurement performed with the *Parameter Analyzer*.

17.2 Dielectric Constant

From the capacitance value in accumulation obtained from CG measurements the dielectric constant was calculated via eq. (33)

$$C_i = \epsilon_0 \epsilon_i \frac{A}{d}$$

The values of the dielectric constant of the unannealed samples are higher than the literature values for thermally grown silicon dioxide ($\epsilon_{SiO_2} = 3.7-3.9$) which can be explained by the non-stoichiometric structure of the PECVD SiO_x. Impurities in the film like water and nitrogen contamination can be seen in the FTIR spectrum of the oxide film. Water ($\epsilon_{H_2O} = 80.4$[49]) as well as silicon nitride ($\epsilon_{Si_3N_4} = 7-8$[50]) have a higher dielectric constant than stoichiometric silicon dioxide and may therefore increase the value of the films dielectric constant.

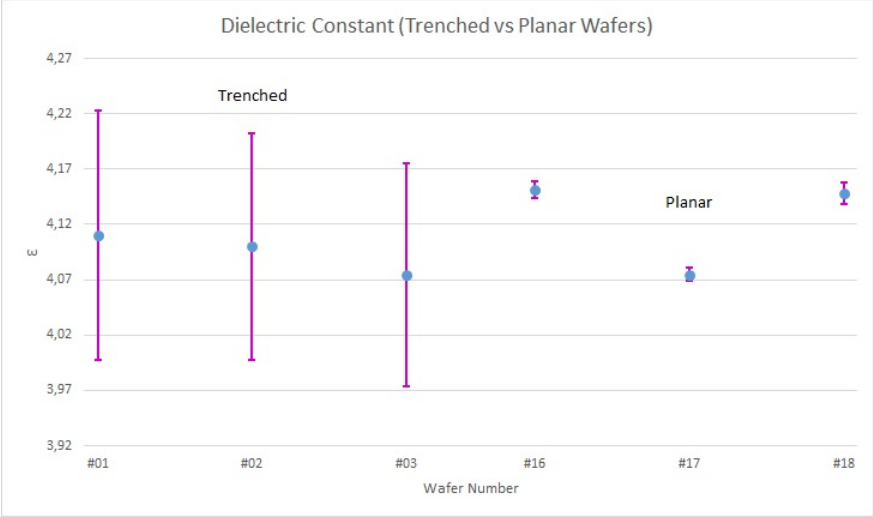


Figure 49: Diagram showing the values for the dielectric constant for wafers of one lot.

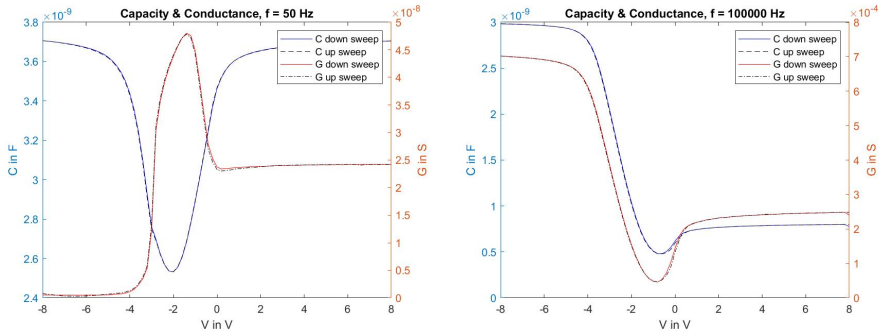
fig. 49 shows values of the dielectric constant obtained from capacitance measurements. All wafers are from the same lot and have an unannealed 100 nm SiO_x layer. The error bar was calculated using the standard error of the mean and for the trenched wafers the error due to area calculations was added. As already mentioned before a correction factor $c_A = 1.17$ was calculated for the area and $c_d = 0.88$ for the oxide laxer thickness of the trenched samples. Assuming an error of 2 nm for the measured oxide thicknesses in the SEM images (sec.15) the error for this correction factor is calculated to be $5 \cdot 10^{-4}$. For this calculation the method of propagation of uncertainty was used.
In the same way the error for the dielectric constant was calculated. For samples with an oxide layer thickness of 100 nm with a thickness variation of 2 nm[†] this error was calculated to be $\Delta\epsilon = 0.09$.

[†]According to the thickness measurements of the planar samples.

17.3 Ohmic Backside

17.3.1 Series Resistance

Conductance measurements show a rise in the inversion regime (fig. 50a, positive voltage regime) if a series resistance is present. Such a series resistance can result from the measurement setup, for example from the contact between wafer and needle or chuck, the cables, etc. Another hint of a series resistance can be seen in higher frequency measurements ($\geq$ 100 kHz), where the capacitance in the accumulation regime is lower than for the measurements at lower frequencies [51] - looking at fig. 50 the value for the capacity in the negative voltage regime is higher with $C \sim 3.7$ nF for $f = 50$ Hz than for $f = 100$ kHz with $C \sim 3.0$ nF. Both effects were seen in the measurements of all wafers with a bare silicon backside performed in this thesis.



(a) $f = 50$ Hz (b) $f = 100$ kHz

Figure 50: Capacitance and conductance at different frequencies f of a wafer with bare silicon backside and 100 nm SiO_x.

As the conductance reveals a lot of information about traps it should not be covered by the conductance due to the series resistance. Therefore *Nicollian and Brews* [15] provide formulas to extract it from the measurements and obtain corrected values for capacitance C_c and conductance G_c. Those formulas are given here for the sake of completeness.

$$C_c = \frac{\left(G_m^2 + \omega^2 C_m^2\right) C_m}{a^2 + \omega^2 C_m^2} \tag{37}$$

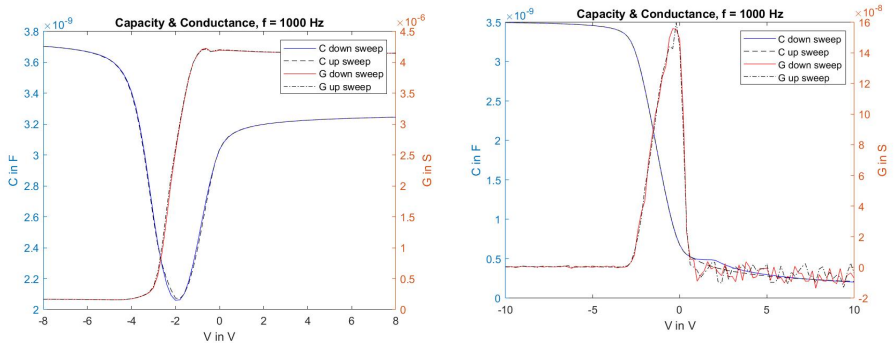
$$G_c = \frac{\left(G_m^2 + \omega^2 C_m^2\right) a}{a^2 + \omega^2 C_m^2} \tag{38}$$

G_m and C_m are the measured conductance and capacitance values, $\omega = 2\pi f$ and $a = G_m - \left(G_m^2 + \omega^2 C_m^2\right) R_s$. The series resistance is calculated from the measured values in accumulation G_{ma} and C_{ma} via

$$R_s = \frac{G_{ma}}{G_{ma}^2 + \omega^2 C_{ma}^2} \tag{39}$$

As this attempt did neither result in a close to zero inversion conductance nor in an accumulation capacitance that is stable over all frequencies the attempt of an ohmic backside via Boron implantation and backside metallization was made

to make sure that the described phenomena do result from a series resistance. fig. 51 and fig. 53 show a direct comparison of samples with and without backside processing[†] at low and high frequencies.



(a) Wafer with bare Si backside.

(b) Wafer with processed backside and nitrogen anneal.

Figure 51: Capacitance and conductance at 1 kHz of two samples with differently processed backsides. SiO_x thickness is 100 nm for both.

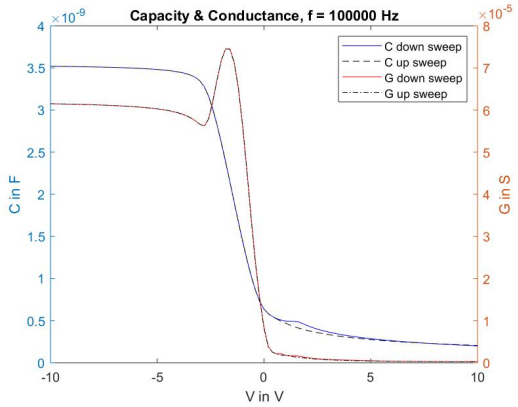
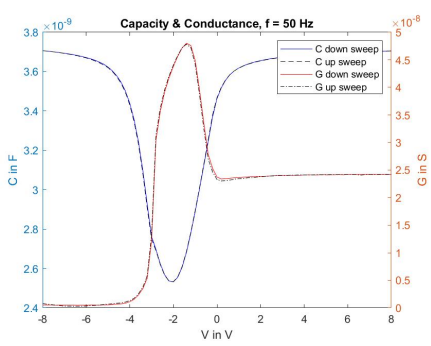


Figure 52: Capacitance and conductance at 100 kHz of a nitrogen annealed sample with processed backside. SiO_x thickness is 100 nm.

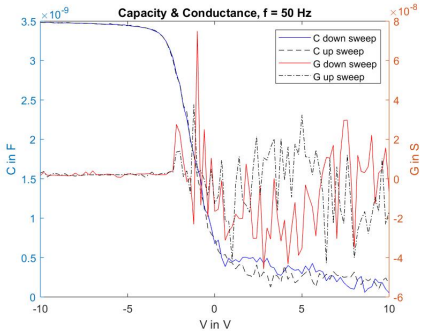
Looking at the conductance curves at an AC frequency of 1 kHz one can clearly see that the conductance rise on the inversion side does not occur for the wafer with backside metal. Furthermore the capacitance in accumulation at high frequencies shown in fig. 52 is the same as in the lower frequency measurements with a value of 3.5 nF.
It was assumed that the additional doping profile should not affect the MOS behavior as the implantation depth is low compared to the silicon bulk thickness and so it is far away from the maximum depletion layer edge. Still the furnace process after implantation seems to alter the semiconductor bulk properties. As all samples that did undergo backside treatment (and also all annealed samples)

[†]The backside processed samples used for comparison here were annealed in nitrogen atmosphere; for unannealed samples see sec.17.3.3

did not show any low frequency MOS capacitance curves at all (fig. 53) it is assumed that the temperature reduces the number of generation centers for charge carriers in the bulk and therefore prevents the formation of an inversion layer.



(a) Wafer with bare Si backside.

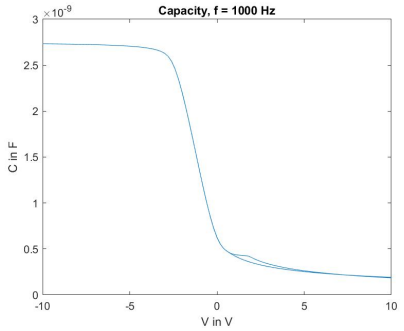


(b) Wafer with processed backside and nitrogen anneal.

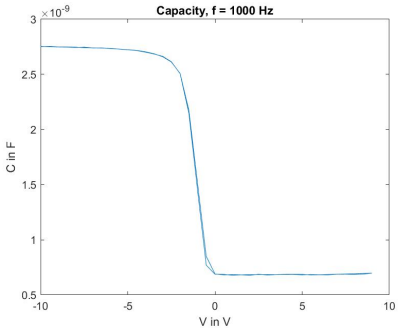
Figure 53: Capacitance and conductance at 50 Hz of two samples with differently processed backsides. SiO_x thickness is 100 nm for both.

17.3.2 Generation lifetime

As for the CV measurements backside processed samples deep depletion is seen in nearly all CV curves experiments concerning minority carrier lifetime were performed. As deep depletion is less likely to occur at higher temperatures (see sec.34) the sample was heated to $T = 100\,°C$ using the UF2000 prober. In



(a) Wafer at room temperature.



(b) Wafer at $T = 100\,°C$.

Figure 54: CV measurements on the same chip at different temperatures. SiO_x thickness is 100 nm, the sample is backside processed and nitrogen annealed, AC frequency is 1 kHz.

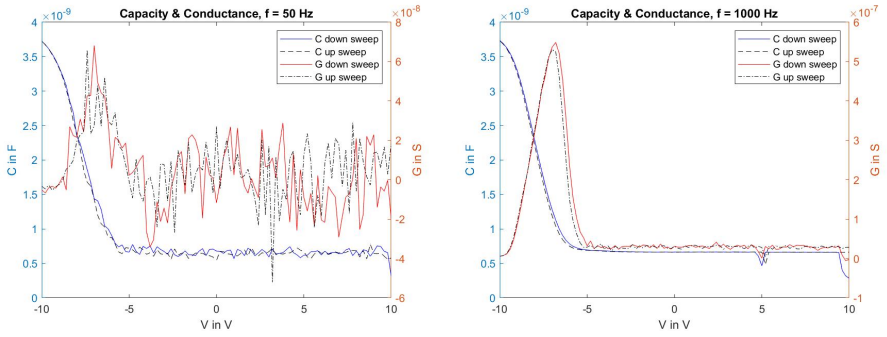
fig. 54 measurements on one chip at the two different temperatures are shown. At $T = 100\,°C$ no deep depletion can be seen. The reason for deep depletion to occur at room temperature might be a very high carrier generation lifetime τ_g of the doped p-Si substrate.
As this does not occur for samples of the same lot without backside metallization[†] it is believed that this behaviour is either an own effect caused by the

[†]without anneal after deposition

furnace step of the backside process as well or simply an effect due to too little minority carrier generation. As already mentioned the elevated temperature process is believed to improve the bulk properties of the semiconductor in a way that too little generation centers are present to form an inversion layer.
This theory is reinforced by the fact that also no low frequency behaviour can be seen for thermal processed samples with and without backside metal and will again be discussed in section 20.

17.3.3 Oxide Charges

The measurement curves of backside processed samples shown before all underwent a nitrogen annealing step after oxide deposition. When no anneal took place the curves are shifted to the negative voltage regime by a lot as can be seen in fig. 55. This shift of the MOS regimes is attributed to oxide charges present in the unannealed samples (see eq. (24) and sec.5). It is believed that those charges get into the oxide layer in one of the process steps used for backside processing which are described in sec.9.



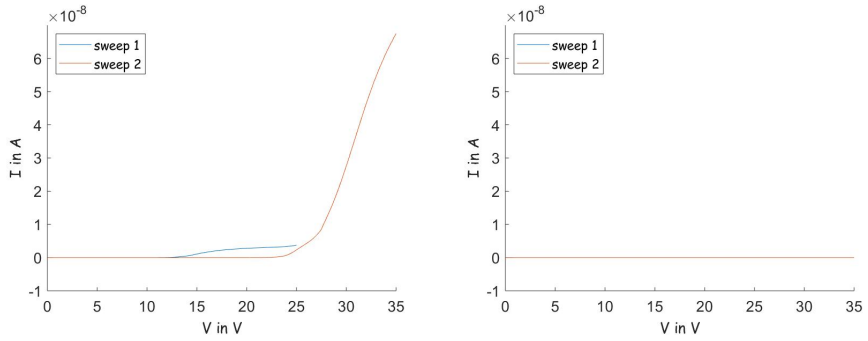
(a) $f = 50\text{Hz}$ (b) $f = 1$ kHz

Figure 55: Capacitance and conductance at different frequencies f. SiO_x thickness is 100 nm, the sample is unannealed and backside processed.

Even if no LF behaviour is to be seen in backside processed samples and considerably more oxide charges are present for the unannealed wafers the experiment was useful to show that the conductance and accumulation capacitance are actually altered by a series resistance resulting from the contact between wafer backside and measurement chuck. Also those wafers were useful to prove that the missing of the LF behaviour does result from annealing the substrate and not the oxide layer as the furnace process for backside metallization takes place before oxide deposition.

18 Conduction in the SiO_x layer

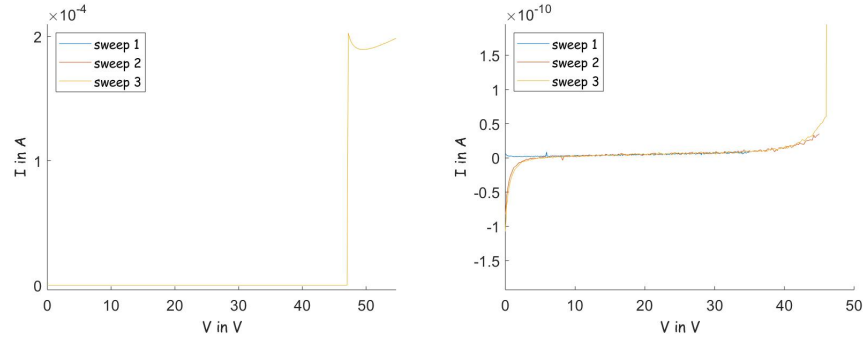
Comparing the current voltage measurements of the planar and the trenched samples it is clear that the current flow in the trenched samples is way higher. This results were expected as simulations showed that for the trenched samples (localized) higher electric fields occur in the SiO_x layer than for the planar ones (see sec.3.2.3).
fig. 56 shows a comparison of the typical outcome for the two different types of chips in a positive voltage regime. The current axis is scaled to the same values in fig. 56 to highlight this fact.



(a) Trenched. (b) Planar.

Figure 56: IV characteristics of samples with 100 nm SiOx layer.

For all measured planar samples the IV characteristics stayed noise around zero in the picoampere regime until breakdown occurred as shown in fig. 57.

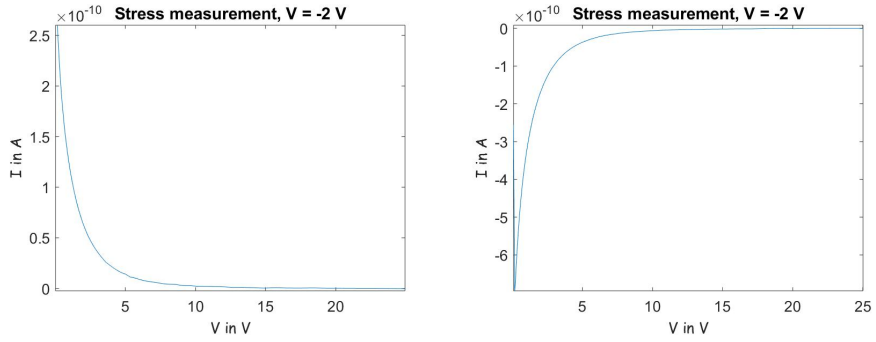


(a) Current jump at breakdown. (b) Current flow before breakdown.

Figure 57: IV characteristics of a planar sample with 100 nm SiO_x layer. Breakdown occurs at $V = 47$ V.

Afterwards the samples did not show the same current behaviour as before and only Schottky curves could be obtained. A rule of thumb suggests that CVD oxides withstand breakdown fields of around 1 MV/cm and thermally grown SiO_2 withstands around 10 MV/cm. With a PECVD SiO_x thickness of 100 nm the breakdown voltage should therefore be around $V = \mathscr{E}d = 10$ V in the worst and $V = 100$ V in the best case.

All measured samples were stable up to voltages above 20 V, but there was no other pattern found concerning the voltage where the breakdown happened. Some chips showed stable behaviour until up to 80 V, others only until 20 V. This holds for the planar as well as the trenched samples and therefore it is believed that the point of breakdown is correlated to structural defects of the SiO_x layer.
Looking at fig. 57b the differently poled transient currents in the beginning of the measurement of sweep 1 compared to sweep 2 and 3 is due to the movement of mobile ions which are distributed differently before the first sweep than before the following ones which were started instantaneously after each other. Reinforcing this theory are the results from stress measurements. The samples were stressed two times at a voltage of $V_{stress} = -2$ V. Before each of those stress tests once a small positive bias (1 V) and once a negative bias (-10 V) were applied for 30 seconds. The results show that the current is poled in two different directions in the beginning and then it reached a stable value. [19]



(a) After stressing with 1 V.

(b) After stressing with -10 V.

Figure 58: Current flow in a planar sample with 100 nm SiO_x when stressing at $V_{stress} = -2$ V with different pre-bias conditions.

Other than that no deviations between the curves of planar chips can be seen.
This is different for the trenched samples. In the double logarithmic plot (fig. 59) it becomes better visible that the first and the second up-sweep do not overlap.

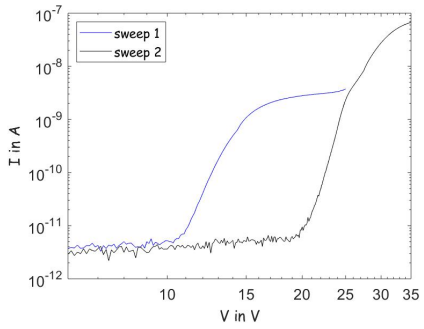
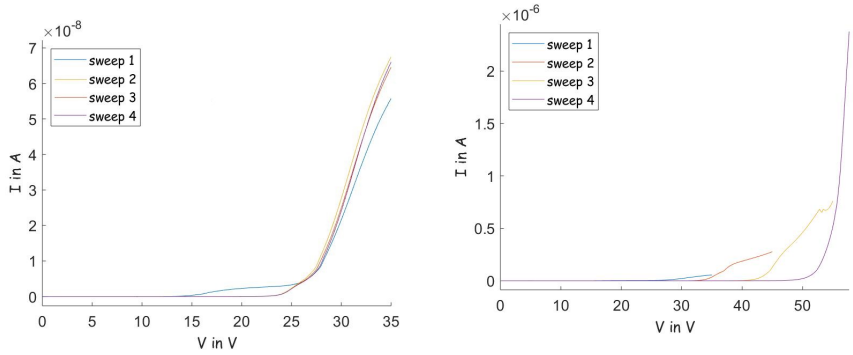


Figure 59: Logarithmically plotted IV characteristics of a trenched sample with 100 nm SiOx layer.

When performing several measurements up to different bias voltages the slopes and shapes of the curves are similar but the voltage where the current flow increased visibly rose with every measurement. In contrast to that measurements up to the same bias voltage showed curves that coincide after the first or second sweep.



(a) Measurements in the same voltage range.

(b) Measurements with increasing voltage range.

Figure 60: Outcome of two different types of IV measurements of trenched samples with 100 nm SiOx layer.

To identify the different conduction mechanisms the measured current was plotted in specific proportion (described in sec.4) to the voltage or the electric field calculated from it (eq. (23)).

18.1 Frenkel-Poole Emission

The most distinct thing when looking at fig. 59 is the linear dependence of the logarithmic current on the voltage. Therefore a fit was performed to check whether thermionic or Frenkel-Poole emission is the responsible mechanism.

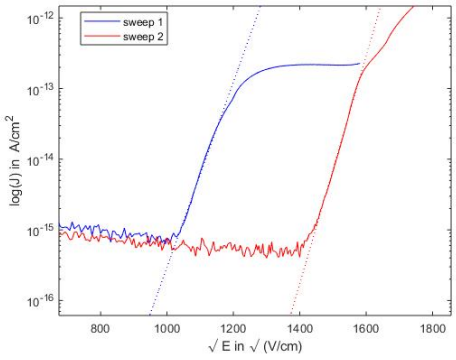
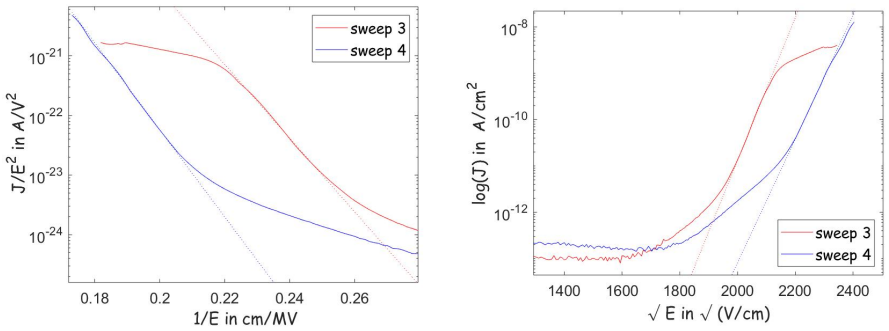


Figure 61: Logarithm of the current plotted over the square root of the electric field. The dotted lines are the fits of the curves in the same color.

As the slope of the fit must equal the exponent of the current-voltage relation

$$slope = \frac{q}{k_b T}(a\beta) \tag{40}$$

when plotted over $\sqrt{\mathscr{E}}$. The constant a is 2 for Frenkel-Poole and 1 for thermionic emission and $\beta = \sqrt{\frac{q}{4\pi\epsilon_i d}}$.[33]
Both theoretical values where calculated and compared to the slope of the fit giving rise to the assumption that Frenkel-Poole emission takes place in the trenched samples. The value for the slope was calculated to be $slope_{FP} = 7.5\ \mathrm{E}^{-5}\sqrt{Vm}$ for a SiO_x thickness of $d = 100$ nm. The values for the measured curves shown in fig. 61 were $slope_1 = 7.7\ \mathrm{E}^{-5}\sqrt{Vm}$ for the first and $slope_2 = 8.5\ \mathrm{E}^{-5}\sqrt{Vm}$ for the second sweep. About the same set of values is obtained for all trenched samples measured in this bias range.
When measuring up to higher fields is gets hard to judge whether Frenkel-Poole emission or Fowler-Nordheim Tunneling is the predominant mechanism.



(a) $J/\mathscr{E}^2$ over $1/\mathscr{E}$ - Fowler-Nordheim plot.

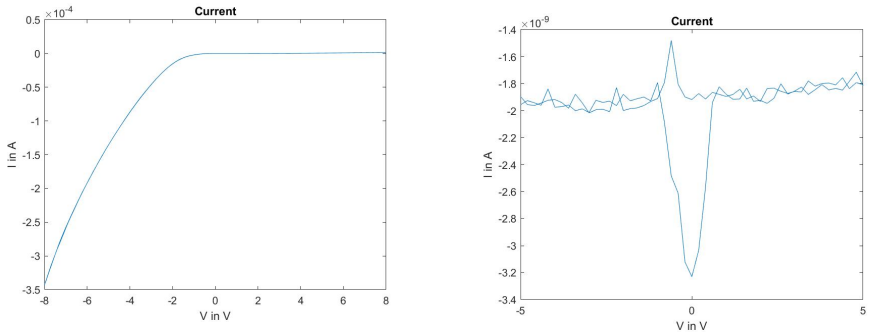
(b) $log(J)$ over $\sqrt{\mathscr{E}}$ - Frenkel-Poole plot.

Figure 62: Differently plotted current measurements of a sample with 100 nm SiOx layer.

The slopes of the measured curves would again fit Frenkel-Poole behaviour but also a $J/\mathscr{E}^2$ over $1/\mathscr{E}$ shows straight lines at least in the last part of the current measurement before breakdown occurred which would be an indicator for Fowler-Nordheim tunneling[52].

18.2 Pinhole defects

Measurements in a low bias voltage regime around zero showed two different general types IV curves shown in fig. 63. This measurements were performed on samples with 10, 20, 50 and 100 nm SiO_x without any thermal treatment after deposition.



(a) IV curve of a trenched wafer showing diode behaviour.

(b) IV curve of a planar wafer.

Figure 63: Exemplary measurements of two wafers of the same lot. Oxide thickness is 100 nm.

Looking at fig. 63a one can see that the diode is forward biased when a negative voltage is applied and nearly no current flows in the positive voltage regime. Considering this it is very probable that a Schottky contact exists between the silicon bulk and the metal electrode prodding to pinhole defects in the silicon oxide layer (sec.4.8).
Experiments showed that the thinner the silicon oxide layer is the more often such Schottky curves occur.

Oxide thickness in nm	Amount of Schottky Curves in %	
	planar	trenched
10	97	99
20	90	97
50	61	66
100	4	13

Table 10: Percentage of different measured chips showing Schottky behaviour.

Tab.10 shows the percentage amount of measurements of chips with differently thick SiO_x layers resulting in Schottky curves. It can be seen that the samples with 10 and 20 nm thin insulating layers hardly led to any other results. Even a lot of chips of the samples with an 50 nm SiO_x layer showed this behaviour a lot. The trenched samples with 100 nm layer thickness had comparatively few Schottky-conductive chips and the highest number of useful results came from planar samples of this kind. It has to be pointed out that it is not foreclosed that some of this Schottky curves results from the prober needle piercing the sample due to height differences of the wafers combined with a fixed needle height and pressure. However such curves were not only measured

using the *UF2000* prober but also the *Parameter Analyzer* where the needles are placed on the chips per hand.

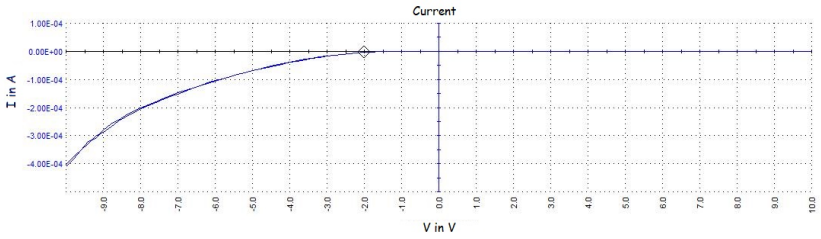


Figure 64: Schottky behaviour measured with the *Parameter Analyzer*. Oxide thickness is 100 nm.

In the up-sweep of fig. 63b a small peak up and in the down-sweep a bigger peak more to the negative can be seen. Those are typical for the samples produced in this thesis and are described in more detail later on in sec.19.1.1.

19 Si/SiO$_x$ States and Charges

19.1 Oxide Charges

To determine the oxide charge density of the samples a calculator[†] based on the description and formulas from *Physics of Semiconductor Devices* by Sze and Ng [14] was used. It provides the theoretical LF and HF CV curve for a MOS capacitor where the flat band voltage, the doping concentration of the semiconductor, the thickness and dielectric constant of the insulator. Also the oxide charge density can be specified which causes a shift of the calculated curve along the voltage axis.
The basic idea is to plot the theoretical and measured curve in one figure and adjust the oxide state density N_{ox} until both curves overlap.

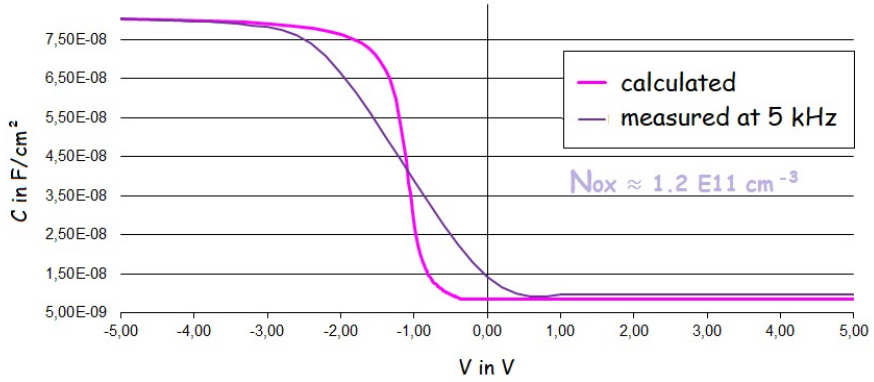


Figure 65: HF CV up-sweep of a trenched wafer with 50 nm unannealed SiO$_x$ in comparison to a shifted calculated HF curve.

Figure 65 shows such a plot for a high frequency curve obtained from a trenched sample with a 100 nm SiO$_x$ layer. Moving the curves till they overlap proved difficult due to a stretch-out of the measured CV curve. This stretching can be caused by interface- and/or bulk traps (see sec.5.3). Therefore the curve was moved on the voltage axis by adjusting the number of oxide charges until the slopes of the two curves crossed at about the middle. The same was done with the minima of the LF curves shown in fig. 66.
In this way a value of approximately $N_{ox} = 1.2\ E11\ \mathrm{cm}^{-3}$ was obtained. As the up- ad down-sweep of this sample do not show a hysteresis it is believed that the shift is due to fixed oxide charges. The charge density was also calculated by the Terman method which is explained in sec.19.3 and probably results in more accurate values. Still the adjustment of the theoretical curves for a comparison with the measurement curves is very picturesque and therefore included at this point.

[†]provided by Dr. Gerhard Schmidt

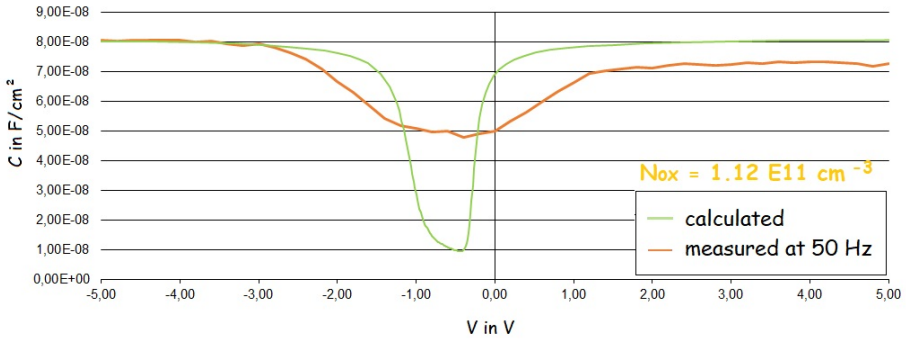
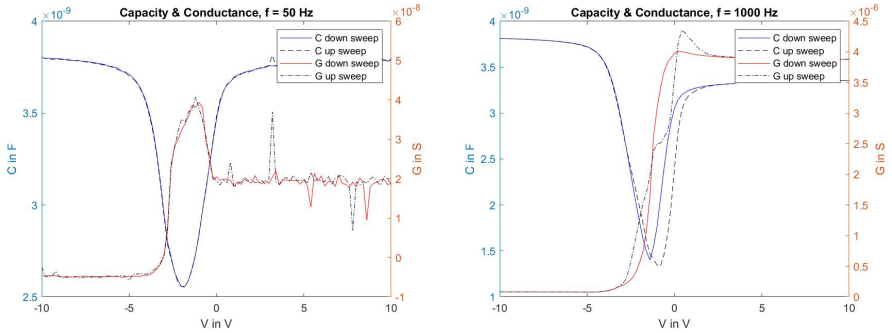


Figure 66: LF CV up-sweep of a trenched wafer with 50 nm unannealed SiO_x in comparison to a shifted calculated LF curve.

19.1.1 Mobile Ionic Charges

Many samples showed a hysteresis in the recorded capacitance and conductance signal between up- and down-sweep of the voltage. This effect was observed to be more prominent for higher frequencies $f \geq 1$ kHz (fig. 67). The first impulse was to think about interface traps, but for those the down-sweep is shifted towards the wrong voltage side compared to the up-sweep (as described in sec.5.1). As the shift direction suits mobile ionic behavior - the hystere-



(a) $f = 50$Hz (b) $f = 1$ kHz

Figure 67: Capacitance and conductance at different frequencies f. The sample is trenched and has a SiO_x thickness is 100 nm.

sis occurs clockwise[53] meaning that the down-sweep is shifted towards more negative voltages compared to the up-sweep - experiments concerning the DC voltage sweep speed and hold times between measurements were performed. As the *LCR Meter* averages over a certain amount of measurements per measurement point a sweep with a higher AC frequency can be performed faster than one with a lower frequency. If the voltage sweep is performed too fast for the mobile ions to react to the bias change a hysteresis can be present. As this might explain that it is more visible at higher frequencies, CG measurements at $f = 1$ kHz were performed with different delay times† and compared to the

†Each voltage step is held for a given amount of time, the so-called delay time. The higher this relay time, the longer the whole DC bias sweep takes.

results without any delay time. The frequency of $f = 1$ kHz was chosen as the hysteresis could be seen very good for this specific frequency (and also for higher ones). Measurements with lower frequency hardly showed this behaviour.
For vividness also the sweep times for the different measured frequencies and delay times for $f = 1$ kHz were plotted.

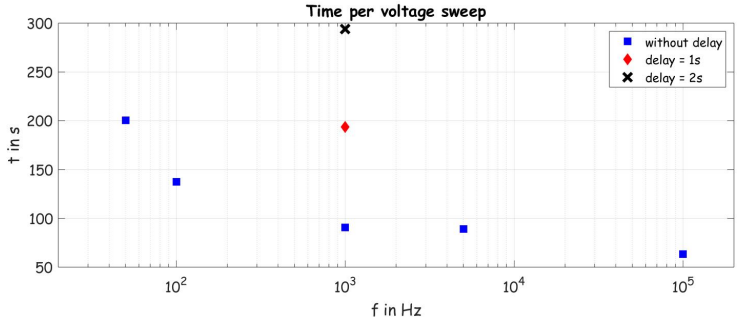
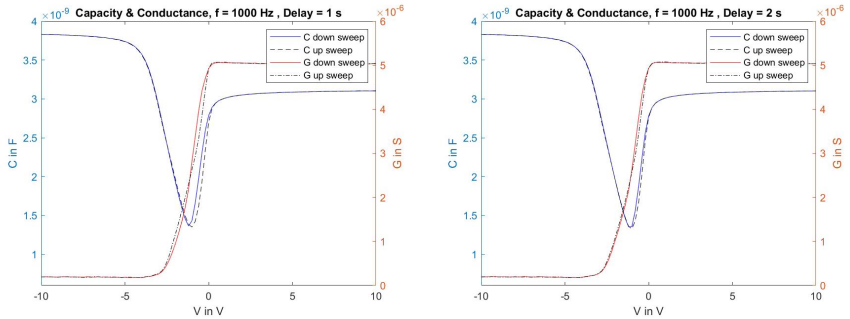
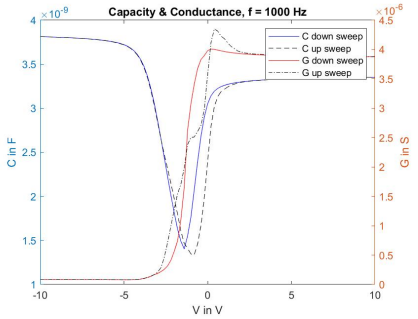


Figure 68: Time t per DC sweep at different AC frequencies f and delay times t.

In fig. 68 one can see that a voltage sweep takes less time for higher frequencies. The delay time for each measurement point increases the sweep time and for $f = 1$ kHz a delay of 1 s is already enough for the sweep to take nearly as long ($t = 192$ s) as at $f = 50$ Hz ($t = 201$ s).



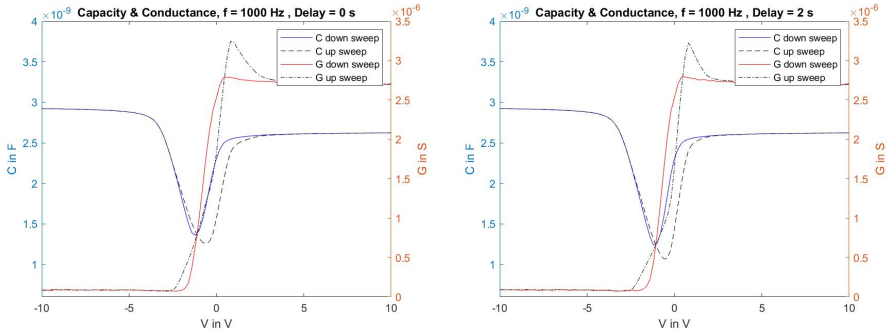
(a) $t = 1$ s (b) $t = 2$ s



(c) $t = 0$ s

Figure 69: Capacitance and conductance at a frequency $f = 1$ kHz and different delay times t. The sample is trenched and has a SiO_x thickness is 100 nm.

The results of the CG measurements with (and without) delay time for each measurement point are shown in fig. 69.
Comparing the 1 kHz measurement without delay time to the measurements at the same frequency with 1 and 2 seconds delay shown in fig. 69 one can see that the hysteresis is getting smaller the slower the DC sweep is performed (the longer the delay time is) speaking for mobile ions being the source of the hysteresis.
Still one can notice that the minimum value of the CV curve reaches lower values when the delay time gets longer. As a raised value of this minimum capacity can result from interface or bulk traps (see sec.5.1) and this effect also occurs when two measurements with the same delay time are performed after each other it is believed that such traps are filled and not completely emptied during the first sweep cycle and some of them simply do not contribute in later measurements.
Performing the same experiment with planar samples the results look a little different. The change of the minimal capacitance is stronger while the size of the hysteresis does only change marginally as can be seen in fig. 70.



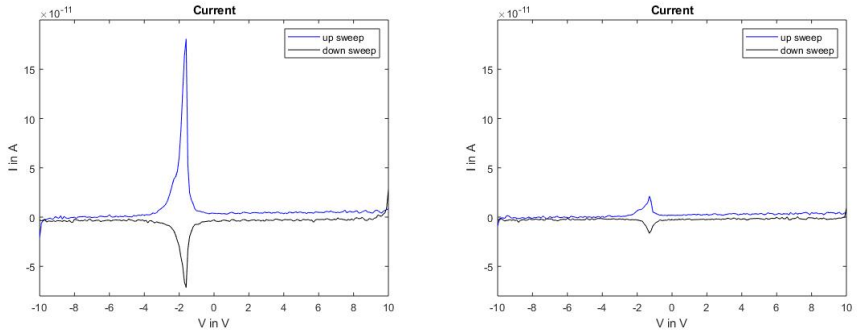
(a) Without delay

(b) $t = 2$ s

Figure 70: Capacitance and conductance at a frequency $f = 1$ kHz and different delay times t. The sample is planar and has a SiO_x thickness is 100 nm.

The reason could be more oxide charges as well as traps present in the planar samples than in the trenched ones. Another explanation could be that the structured samples have a thinner oxide layer at the trench bottoms and walls. Therefore the mobile ions need to travel shorter ways through the oxide probably taking them a shorter amount of time.

Looking at the IV measurements (fig. 71) of both types of samples latter is more probable as the planar sample show a way smaller peak around the flat-band voltage that the trenched ones show which is also an indicator for mobile ions [15,54]. Therefore it is not really probable that the planar samples do contain more mobile species than the trenched ones but vice versa.
Comparing the magnitude of the current peak in fig. 71 the trenched sample shows a magnitude of ~ 170 pA for the up-sweep and ~ -70 pA for the down-sweep while the planar one has magnitudes of ~ 20 pA and ~ 15 pA respectively. Even if a higher oxide thickness is correlated with a smaller current peak [54] the average oxide thickness in the trenched samples is relatively not that small compared to the planar ones that such a peak height difference could occur.



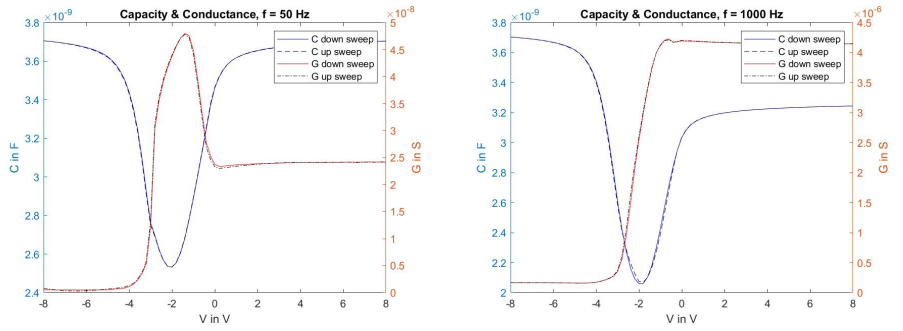
(a) Trenched wafer.

(b) Planar wafer.

Figure 71: Current voltage measurement of two different samples. SiO_x thickness is 100 nm for both.

19.2 Interface Trapped Charges

The first thing about the conductance of trenched unannealed samples catching the eye is the big peak in the depletion regime.



(a) $f = 50$ Hz (b) $f = 1$ kHz

Figure 72: Capacitance and conductance at different frequencies f. SiO_x thickness is 100 nm.

To determine if it comes from interface trapped charges the conductance was measured at different frequencies and the peak position on the voltage axis and height were determined (see sec.5.1).

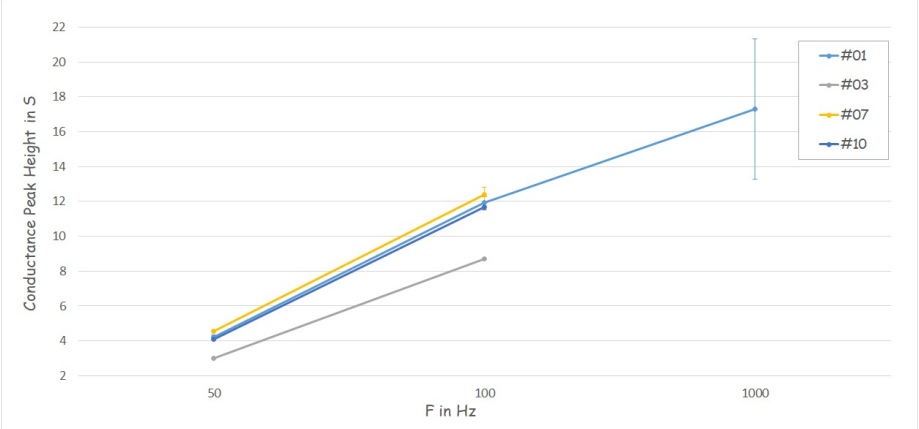


Figure 73: Averaged height of the conductance peak for different frequencies.

The most stable results for the peak height were obtained for the measurements at $f = 50$ and 100 Hz. This is because the conductance peak vanished under the influence of the series resistance at higher frequencies as described before in section 17.3.1. Even if the top of this peak is visible in some $f = 1$ kHz measurements (f.e. fig. 72b) its height is hard to determine causing a big error for that frequency.
For wafer #01 and #03 six chips each were measured, for wafer #07 and #10 three measurements per wafer were done. As the results are very similar for the lower frequencies ($f = 50$ and 100 Hz) a small error bar results for each wafer which was calculated using the standard error of the mean.

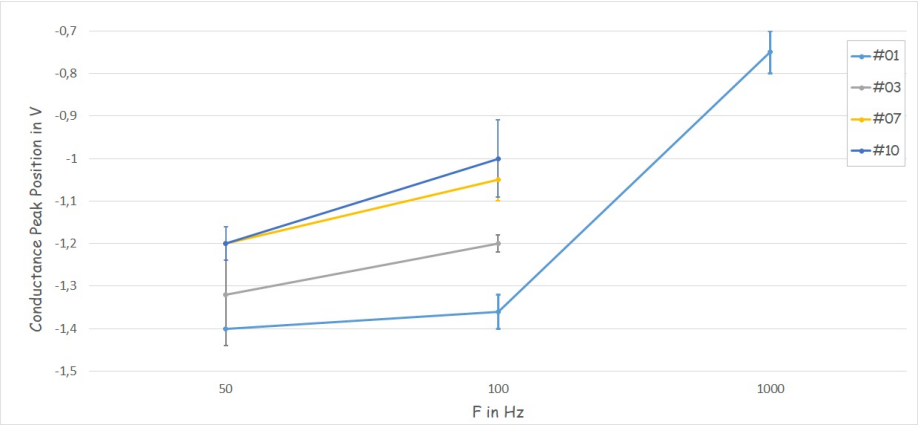
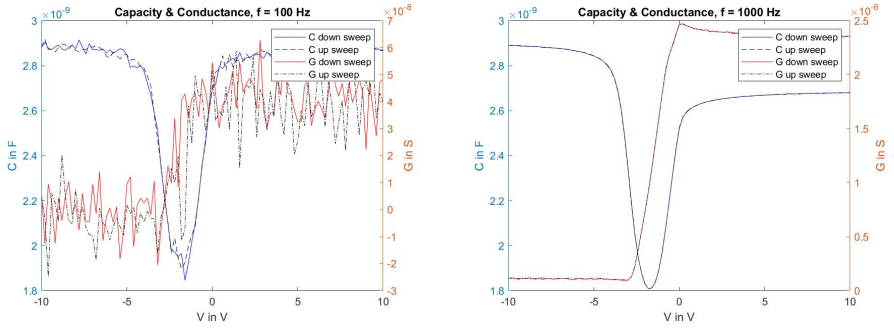


Figure 74: Averaged position of the conductance peak on the voltage axis for different frequencies.

One can clearly see in fig. 73 that the peak in the $f = 100$ Hz measurements grows with respect to the one in the 50 Hz measurements suggesting that interface traps are the cause for it. Also the positions suit this theory as the peak drifts towards the flat band voltage with rising values of the AC frequency. Via [16] the flat band state was determined to be at $V_{fb} = -0.86$ for the lot containing wafer #01 and #03 and $V_{fb} = -0.88$ for the lot of the other two. The peak position could be determined for frequencies up to 1 kHz and was again averaged over all chips for each wafer. The error bar is simply the standard error of the mean not including the error in position on the voltage axis due to the voltage step $V_{step} = 0.2$ V in the CG sweep.
Having a look at the planar samples without thermal treatment after deposition hardly a conductance peak is visible at any measured frequency. An example of a CG measurement of such a sample is shown in fig. 75.



(a) $f = 100$ Hz

(b) $f = 1$ kHz

Figure 75: Capacitance and conductance of a planar sample at different frequencies f. SiO_x thickness is 100 nm.

The conductance is in the same order of magnitude as that of the trenched samples but is missing a peak at all frequencies. Therefore it is concluded that the trenched samples have way more interface trapped charges than the planar ones. This assumption was also checked using the Terman method in sec.19.3.

19.3 Terman Method

To determine the interface state density as well as the number of oxide states a simplified version of the *Terman* method was used. This method again is a comparison of a calculated theoretical HF CV curve to a measured one. Therefore the voltage difference ΔV of the two curves has to be determined for each capacitance value. Further the density of all present charges N is calculated via

$$\Delta V = \frac{Nq}{C_i} \tag{41}$$

and plotted over the bias voltage. The resulting curve is a sum of oxide charge- and interface trap densities. To separate the two parts it is assumed that the interface trap density is zero at midgap. Latter is defined as the point where the surface potential Ψ_s equals the bulk potential Ψ_b and the corresponding surface potential can be calculated via $\Psi_s = \Psi_b = E_i - E_F$ where E_i is the intrinsic Fermi level. The charge density at this point can therefore be assigned to oxide charges N_{ox}. As this value is constant and does not vary with band bending it gets subtracted from the overall charge density curve at any bias value and what remains is the part due to interface traps.
The first sample here is the one of sec.19.1 for comparison.

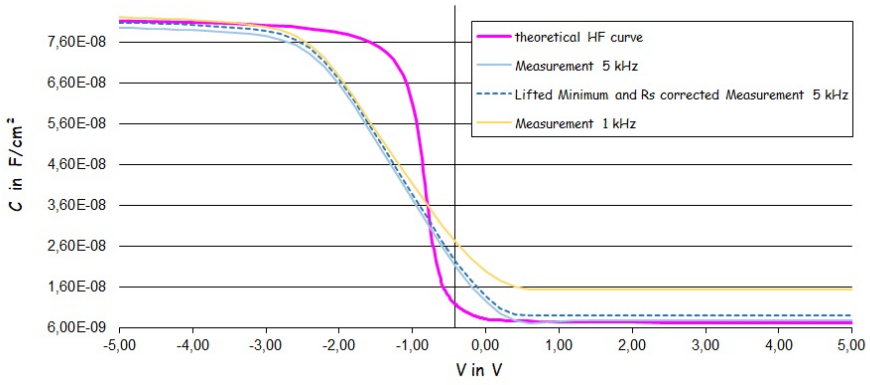


Figure 76: Theoretical HF curve versus 1 and 5 kHz measurement of a trenched sample with 50 nm SiO_x thickness.

Looking at fig. 76 and fig. 77 the measurement at $f = 5$ kHz was plotted in two versions, one time as it was measured and one time with a series resistance and minimum correction lifted to the same accumulation value as the $f = 50$ Hz measurement of the same chip. The series resistance correction performed[†] did not stretch the CV curve as expected or make any difference at all, neither for this nor for any of the other evaluated samples but was still calculated to check for correctness. Still it was shown in the experiments in sec.17.3.1 that the lower accumulation capacitance at higher frequencies is an effect due to such a series resistance. Lifting the measured curve therefore seems valid but causes a gap in the inversion capacitance values to the theoretical curve changing the outcomes in this section and will be discussed further on.

[†] with formulas from *MOS (metal oxide semiconductor) physics and technology* by Nicollian and Brews [15] given in sec.17.3.1

While the mentioned minimum correction did not make a big difference for this specific sample it is decisive for other samples that will be seen later on (see fig. 80 and fig. 81). This correction is considered to be valid as the undershoot in the higher frequency CV measurements did not occur for the $f = 1$ kHz curves of the same sample (a comparison of such measurements at different frequencies can be seen in fig. 76) and therefore it is believed that the minimum is an effect due to the series resistance which is emphasised by time dependent species like ions at certain frequencies.
The inversion capacitance in the positive voltage regime decreasing with rising frequency seen here ($f = 1$ and 5 kHz) is also caused by the series resistance R_s (see sec.17.3.1) according to Rejaiba *et al.* [51] as the MOS capacitance is dependent on a product $2\pi f R_s C_i$.

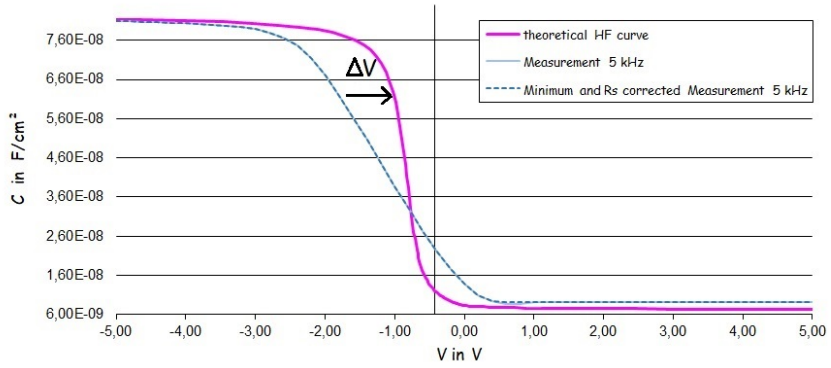


Figure 77: Theoretical HF curve versus a lifted measured curve at 5 kHz of a trenched sample with 50 nm SiO_x thickness.

For the theoretical curve in fig. 77 the oxide state density was defined to be zero so it was not shifted along the voltage axis. Then the voltage difference ΔV of those two curves at every measured capacitance value was determined.

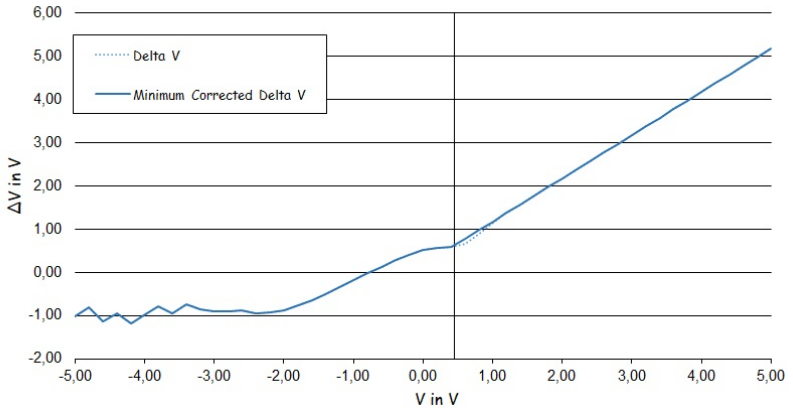


Figure 78: Plot of the voltage difference of the measured and theoretical CV curves ΔV over the DC bias voltage.

From this voltage difference the overall density of charges N was determined via eq. (41) and plotted over the DC bias voltage as shown in fig. 79. Assuming the interface trapped charge density to be zero at midgap the charge density could be split in two. As already mentioned a constant part is due to positive oxide charges ($N_{ox} = 1.46\ E11\ q/\mathrm{cm}^3$) - which suits the results of sec.19.1 pretty well for this sample - shifting the measured CV curve towards more negative voltages. The other part is varying with band bending due to interface traps stretching the CV curve.

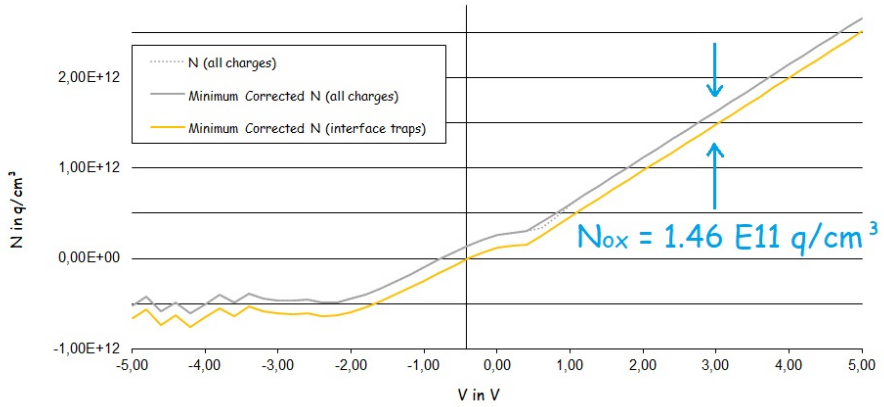


Figure 79: Plot of the charge density N over the DC bias voltage.

The slope of the linearly increasing ΔV as well as charge density curves from ~ 0.5 V upwards results from a combination of two effects. First, the theoretical curve shows a slight downward tendency while the measured curve slightly rises. Second, the difference in the minimum of the inversion capacitance of the measured and theoretical curve leads to big differences in the bias voltage where a certain capacitance value occurs and therefore to a rather steeply linearly increasing ΔV. Latter leads to a rather big error in interface trap density and therefore it is not very accurate in the inversion regime.

The same method was also applied to some other samples with and without trenches with a SiO_x thickness of 100 nm, all of one lot. As already mentioned the undershoot of the CV measurement was more obvious for those samples.
As ΔV is the voltage difference for equal capacitance values of the measured and theoretical curves the rather low values at this undershoot are found far in the positive bias regime of the theoretical curve. This leads to an increase of the voltage difference to the negative (and therefore also charge density) until the minimum of the dip is reached. Then the voltage difference decreases again as the two curves become more similar again causing a relatively big negative pole in ΔV and N making the minimum correction of the CV curves crucial.

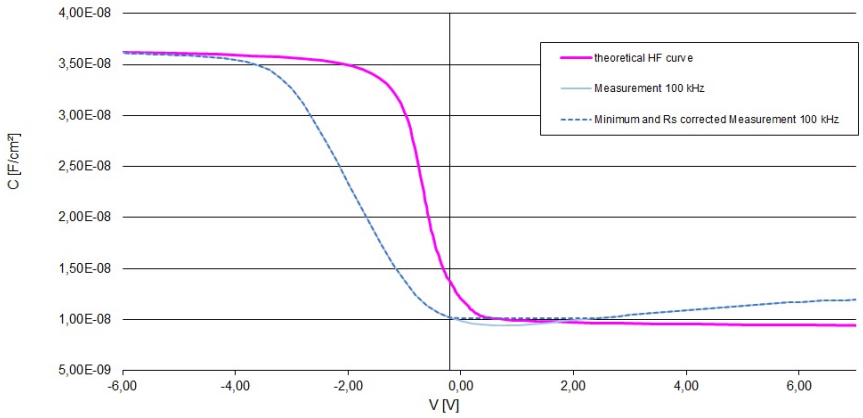


Figure 80: Theoretical HF curve versus a measured curve at 100 kHz of a trenched sample with 100 nm SiO_x thickness.

Comparing only the interface trapped charge density in the negative voltage regime (accumulation and depletion) one can see that in general the trenched samples show more negative charges than the planar ones. This is also in agreement with the findings of sec.19.2. Also the planar samples showed a little higher oxide charge density in average (about 2 to 4 times higher than the trenched ones). The reason for that is believed to be the difference in production of the two types of samples as oxide charges can be induced in any of the process steps. An example for the charge density obtained by the *Terman* method of a planar chip can be seen in fig. 81. The oxide charge density obtained for this sample is $N_{ox} = 2.28\ E11\ q/cm^3$. The dotted curve given here is the overall charge density before minimum correction. As mentioned before this minimum can cause a large dispersion in the voltage values for a specific capacitance value. This is because the undershoot is deeper for the samples of this lot as can be seen in fig. 80.

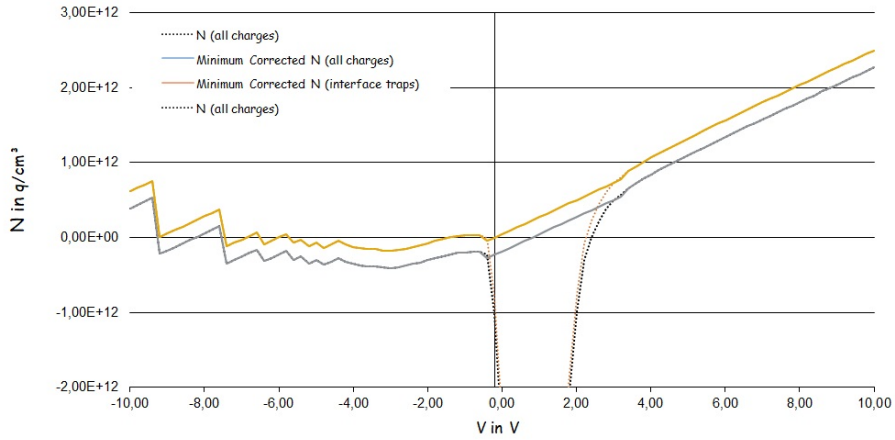


Figure 81: Plot of the charge density N over the DC bias voltage for a planar sample with 100 nm SiO_x thickness.

Also the inversion capacitance slightly rising towards more positive voltages influences the slope of the charge density in inversion.

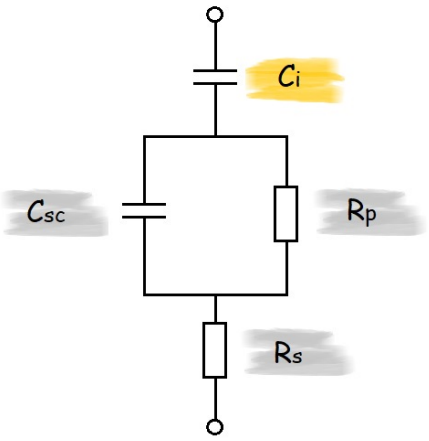
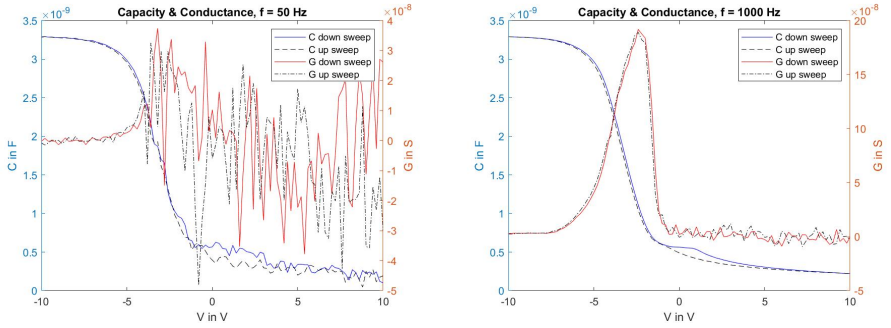


Figure 82: Equivalent circuit of a MOS capacitor at high frequencies including a series resistance for the contact between wafer and measurement unit and a parallel resistance in the space charge layer of the semiconductor.

This increase after the dip (see f.e. fig. 80) is proposed to be due to a parallel resistance R_p in the space charge layer by [51]. Low values for this resistance - which is depending on the doping density N_A of the semiconductor - combined with the frequency of the AC signal can lead to strong changes in the minimal inversion capacitance. This can be explained by looking at the equivalent circuit of a MOS capacitor including R_p in fig. 82. When R_p is low then electrons can easily make their way through the space charge layer to the inversion layer and therefore the capacitance rises towards C_i again.

20 Thermal Treatment after Oxide Deposition

The thermal treatments described in sec.10.2 of course yield very different results. One thing they all have in common though is that no low frequency curves can be seen for any measured frequency. As shortly mentioned in sec.17.3.2 the reason for this might be that there are too little centers for electron hole pair production in the bulk. The thermal treatment is believed to improve silicon bulk properties and according to [55] it is quite typical for high quality devices to not show LF behaviour. The effects of those annealing experiments were therefore investigated with the help of the obtained HF curves of both, backside processed and unprocessed samples. As for latter a comparison was easier because the influence of the series resistance could be excluded this chapter is dedicated to them.



(a) $f = 50$ Hz (b) $f = 1$ kHz

Figure 83: Exemplary CG measurement of an O_2 annealed trenched sample with backside metal at different frequencies f.

The unannealed trenched samples showed more interface traps (conductance measurements) and mobile ions (current measurements) than the planar ones. Only the shift of the MOS regimes due to oxide charges is also seen in a similar amount for the planar samples. Due to the higher amount of charges and states, quality improvements due to thermal treatment were better visible for the trenched samples. Therefore the discussion of results concerning thermal treatment is confined to those samples.
Furthermore it has to be mentioned that the annealed wafers are from a different lot than the unannealed ones. As both lots were produced together and the sheet resistance measurements performed showed similar results for both (leading to doping concentrations also very close to each other) they are considered comparable.

20.1 Dielectric Constant

fig. 84 shows the dielectric constant of different types of samples. On the right side the unannealed samples are shown, on the left side are the ones thermally treated in nitrogen atmosphere and in the middle those in oxygen atmosphere.

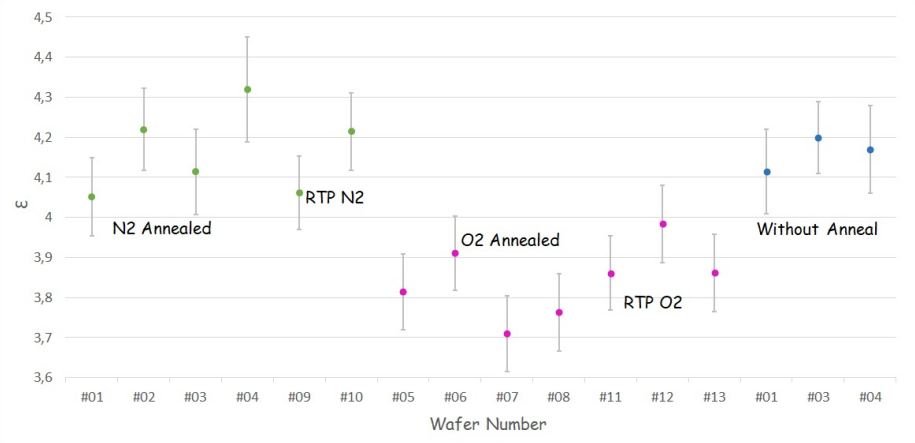


Figure 84: Dielectric constant of thermally differently treated samples with backside metal.

Two wafers each were annealed in a furnace process at $T = 970$ and $1100°C$ and two underwent RTP in nitrogen and oxygen atmosphere respectively. It has to be mentioned here that the furnace processes in oxygen atmosphere increase insulator thickness as already described in sec.13. The dielectric constant was then calculated using this new measured thickness for those samples.
The values plotted in fig. 84 are the mean of all chips measured per wafer. The error is the standard error of the mean plus the error due to area calculations (see sec.17.2).
The samples without any thermal treatment show an dielectric constant clearly above the literature value for thermally grown SiO_2 of $\epsilon_{SiO_2} = 3.7 - 3.9$. While the the O_2 process at $T = 1100°C$ (wafer #07 and #08) show ϵ values closest to this all three types of oxygen anneals of such samples (both furnace anneals as well as RTP) improve the measured values towards the literature one whereas the nitrogen treatments failed to do so. The reason for this behaviour could be that such anneals increase (or at least do not lower) the amount of nitrogen contamination in the SiO_x layer and therefore also do not lower the value of ϵ as silicon nitride has a higher dielectric constant of $\epsilon_{Si_3N_4} = 7 - 8$ [50].
It is also to notice that the results for ϵ of the single wafers of one type deviate more from each other for thermal treatment in nitrogen atmosphere. Neither the dielectric constant values for samples #01 and #02 annealed at $T = 970°C$ nor those of #03 and #04 annealed at $T = 1100°C$ or those of the two nitrogen rapidly thermal processed samples #09 and #10 are close to each other. Also the variations within one wafer were bigger using nitrogen resulting in a bigger error bar. Latter is a bit harder to see as the main part of the error bar results from the area calculation as described in sec.17.2.
It is also visible that wafers with an uneven wafer number show a lower dielectric constant than those with an even one. This is due to small oxide thickness dif-

ferences resulting from the two different production chambers used (see sec.10).

20.2 Oxide Charges

To get an idea of the amount of oxide charges being left after the different anneals the positions of the peaks appearing in the current as well as conductance measurements were compared. Both of them reveal information about the flat-band voltage as the current peak - due to mobile ionic charges (see sec.19.1.1) - is located at about V_{fb} [54] and the conductance peak wanders towards it with rising frequency of the AC signal [15]. The flat-band voltage then is a good indicator for the shift of the MOS regimes due to oxide charges.

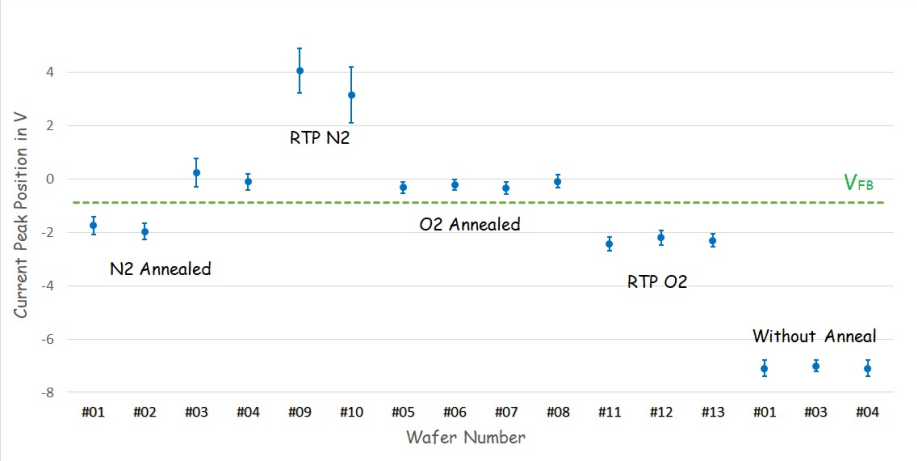


Figure 85: Position of the current peak of the IV up-sweep on the voltage axis for the differently treated wafers with backside metal.

Again the values plotted are mean values for each wafer and the error bar is a result of the standard error of the mean plus the voltage step of $V_{step} = 0.2$ V between each measurement point.
Looking at fig. 85 and fig. 87 the error bar is always bigger for the N_2 annealed samples meaning that different chips of one wafer showed big differences in the position of the peaks on the voltage axis. This can be interpreted as a high variation of oxide charge density within those wafers. Also the chips on such a wafer showed no consistent behaviour concerning the different peaks. The conductance peaks at lower frequencies ($f = 50$ and 100 Hz) were only present for some of the chips while those at higher frequencies differed in height. Together with the non-uniformity of the dielectric constant described earlier it is concluded that thermal treatment in nitrogen atmosphere leads to unpredictable results. Furthermore, when looking at eq. (24)

$$V_{fb} = \Phi_{Al} - \Phi_{Si} - \frac{Q_m + Q_f + Q_{ot}}{C_i}$$

the RTP in N_2 atmosphere seems to induce negative charges in the oxide as the current- as well as the conductance peak position is shifted to more positive values than the flat-band voltage which was calculated to be $V_{fb} = -0.87$ V.

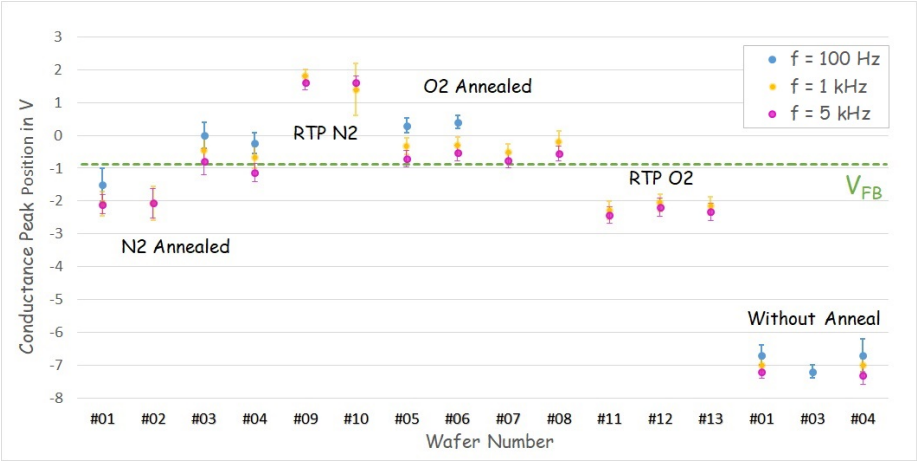


Figure 86: Position of the conductance peak of CG measurements at three different frequencies f on the voltage axis for differently treated wafers with backside metal.

As already described in sec.17.3.3 the backside processed samples without any anneal showed a high amount of oxide charges shifting the CG curves towards more negative bias voltages. The RTP in oxygen atmosphere obviously reduces oxide charge density as the peaks shift towards the flat-band voltage for those samples. The furnace processes in oxygen atmosphere and the hotter one in nitrogen atmosphere also show current peak positions slightly above the flat-band voltage. As this voltage difference is quite small it is believed to be either due to uncertainties in the determination of the flat-band voltage[†] or due to resolution of the measurement rather than due to induced negative charges. Furthermore the conductance peak wanders towards the flat band voltage with rising frequencies for those chips as can be seen in fig. 87 leading to the conclusion that the oxygen furnace processes are the best way tested to reduce oxide charges and shifting the MOS regimes towards the theoretical values.

[†]including the sheet resistance measurement, further the calculation of the resistivity and doping concentration and finally of the flat-band voltage

20.3 Interface Trapped Charges

fig. 87 also reveals the presence of interface states. A peak in the conductance measurements wandering towards the flat-band voltage is a clear indicator for such. Comparing the height of this peak for the different measured frequencies the furnace processes in oxygen atmosphere also show the lowest values suggesting that those samples also have the lowest interface trap density.

Figure 87: Height of the conductance peak of CG measurements at different frequencies for differently treated wafers with backside metal.

Looking at samples without backside metallization the result is basically the same. All anneals in oxygen atmosphere provided improved results compared to the unannealed samples. The anneals performed in nitrogen atmosphere did not give stable results again and were only sometimes an quality improvement of the PECVD SiO_x layer.

Part IV
Summary and Conclusion

The goal of this thesis was to compare metal oxide semiconductor (MOS) structures with and without topography. The oxides with different film thicknesses were deposited using a PECVD process resulting in a non-stoichiometric molecular structure. Improving their quality via thermal anneals was an additional task.

The comparison of planar samples and those with additional features of topography as well as of the differently thermally treated samples was done by electrical characterization, namely current-voltage and capacitance-conductance (IV and CG respectively) measurements. With those methods charges and states within the oxide as well as at the semiconductor-oxide interface could be identified and their density could be estimated. Furthermore the IV characteristics revealed information about the conductivity of the oxide layer.
The most important results are summarized here.

Film Thickness

When depositing a SiO_x film via PECVD on a planar sample the film thickness can be controlled very precisely. Looking at samples with topography the coverage at the trench bottom and walls is not the same as on the somewhat higher area without trenches. It was found that the SiO_x thickness at the walls of a trench is as thin as around half of the target thickness. Therefore a correction factor $c_d = 0.88$ for the average film thickness of those samples was calculated. This difference in film thickness between the planar and the trenched samples had to be kept in mind in other fields of comparison.

Conduction in the SiO_x Layer

Where the planar samples only showed noise in the picoampere regime until dielectric breakdown occurred the trenched samples showed at least Frenkel-Poole conduction. Also hints for Fowler-Nordheim tunneling where found in higher voltage regimes. As Frenkel-Poole emission is a trap assisted process this goes well together with the findings concerning the higher density of Si/SiO_x states for the trenched samples. Fowler-Nordheim tunneling is also not unlikely for the trenched samples as their SiO_x thickness at some points is very much thinner than that of the planar samples with the same target thickness making the tunneling probability higher.

Si/SiO_x States and Charges

Several different experiments showed that not only the oxide- but also the interface trap density is higher in the samples with trenches. The samples with topography showed higher conductance peaks (indicator for interface trapped charges), current peaks around the flat-band voltage (indicator for mobile ions) and bigger shifts of the CV MOS regimes (indicating a higher density of oxide charges). A reason for this might be more different crystal orientations in the SiO_x layer due to topography. To check if that is the case a x-ray diffraction measurement is suggested.

Thermal Treatment after Deposition

The first thing that attracts ones attention when looking at the CV curves of all differently annealed samples is that no low frequency behaviour can be seen. The same happens when a backside metallization is made to ensure ohmic contact. It is believed that the higher temperature processes improve the quality of the silicon semiconductor in a way that too little generation centers are left to form an inversion layer that leads to the increase of the capacitance curve in the inversion regime. If this is the case measuring the capacitance in the inversion regime over time should give the LF value C_i as recombination and generation processes would go to equilibrium. Therefore such time dependent capacitance measurements are suggested as future experiments.
Experiments concerning the different anneals performed to improve SiO_x quality showed that thermal treatments in oxide atmosphere show better results that are more continuous throughout all measured samples than in nitrogen atmosphere. Latter seem to induce negative charges in the oxide and do not really decrease the density of interface trapped charges. Furthermore the values for the dielectric constant fluctuate a lot after such anneals indicating that sometimes more and sometimes less nitride compounds get integrated in the SiO_x structure.
On the other hand all three types of anneals in oxide atmosphere lead to values for the dielectric constant close to the literature value ($\epsilon_{SiO_2} = 3.7 - 3.9$) and decrease all different types of Si/SiO_x states and charges. Here the two different furnace anneals worked significantly better than the RTP and the hotter furnace process ($T = 1100$ °C) then showed slightly improved results compared to the cooler one ($T = 970$ °C).

Series Resistance

Performing a backside metallization of some samples proved that the hints of a series resistance found in the CG curves of the samples with blank Si backside are really due to such. Therefore backside processing of the wafers is seen as an improvement and should therefore always be performed.
As already mentioned this process also improves the silicons quality as no LF behaviour is to be seen.

Outlook

The overall goal of further research is supposed to find a correction factor for the SiO_x thickness of structures with topography in contrast to planar ones. Such can be helpful to decrease layer thickness and therefore the size of different semiconductor components in the future. To achieve this objective different types of experiments are proposed to be performed.
Difficulties in comparing the planar and trenched structures arose due to the non-uniform film thickness of latter. Therefore future experiments are suggested with trenched structures that either have an oxide layer whose average thickness or thinnest part equals that of the planar ones. In this case a more precise quantitative analysis of the different charges and states is possible.
Performing IV measurements to determine conduction mechanisms within annealed silicon oxide layers can reveal information of the film quality in the different samples.
Furthermore detailed stress tests and breakdown measurements of the raw as well as thermally treated SiO_x layers will be useful to find a ratio of how the thickness of such films has to be dimensioned for MOS structures with topography.

Appendix

***MATLAB* Code used for plotting the band diagrams (fig. 3.1)**

```
close all;
%Ev = double.empty;  %valence band energy
%d arrays used for plotting
dEv = double.empty;  %Ev
dEF = double.empty;  %EF
dEc = double.empty;  %Ec
dn = double.empty;  %n
dp = double.empty;  %p
drho = double.empty;  %rho
dE = double.empty;  %E-Feld

 echarge = 1.60217733E-19;
 kb = 1.380658E-23/echarge;  %eV/K
 %dEvdx0 = 1e3;

 tox = 50*1e-9; %thickness oxide in nm
 na = 1e6*2.2e19*1e-4;%*1e-4; %Aceptor concentration (1e6
     cm^-3 to m^-3, 1e-4 to make Boltzmann approx valid)

%  num = xlsread('ConcentrationProfileAsImplant.xlsx');
%  depth = num(:,1)*1e-6;
%  datacAs = num(:,2);
%  f = fit(depth,datacAs,'gauss1');
%  c = coeffvalues(f);
%  gauscAs = @(x) 1e6*1e-4*c(1)*exp(-((x-c(2))/c(3)).^2);
     % (1e6 cm^-3 to m^-3, 1e-4 to make Boltzmann valid)

 Nv = 1e6*9.84e18;
 Nc = 1e6*2.78e19;
 T = 300;
 Eg = 1.166-4.73E-4*T*T/(T+636);
 eps = 8.854187817e-12*12; %eps semi = 12
 phi_m = 4.08;
 chi_s = 4.05;
 eps_ox = 8.854187817e-12*4;
 ni = sqrt(Nc*Nv*(T/300)^3)*exp(1.6022e-19*(-Eg)
     /(2*1.380658e-23*T)); %intrinsic carrier
     concentration
 cox= eps_ox/tox; % C Oxide

 Va = 0; % applied Voltage

 VT = 2*tox*sqrt(eps*na*1.380658e-23*T*log(na/ni))/eps_ox
     +2*kb*T*log(na/ni);  %threshold voltage in depletion
     approximation
```

```
40  Ev0 = kb*T*log(na/Nv); %valence band far from the oxide
41  xp = 2*sqrt(eps*kb*T*log(na/ni)/(echarge*na)); % maximum
        depletion width in depletion approximation
42
43  phi_s = chi_s + Eg + Ev0; % work function of
        semiconductor
44
45  Vfb = phi_m  - phi_s; % flat band voltage
46  V = Va - phi_m + phi_s; %zero bias should result in a
        built-in voltage corresponding to the work function
        difference
47  VT = VT + Vfb;
48 % This section starts with somewhat arbitray initial
      conditions for Ev(x) and its derivative
49 % dEv(x)/dx inside the bulk of the semiconductor and then
        integrates the Possion equation
50 % to the left to calculate the voltage at the
      semiconductor/oxide interface and then the
51 % voltage at the gate. The calculated voltage at the gate
        is compared to the desired voltage at the gate
52 % the initial conditions are adjusted to get the
      calculated value closer to the desired value.
53
54   xr = 3.6*xp; %right position for binary search
55   xm = 1.8*xp; %middle position for binary search
56   xl = 0;      %left position for binary search
57   for j = 1:15
58     Ev = Ev0;
59     dEvdx = 0;
60     if (V>0)
61         dEvdx = 1e3;
62     end
63     if (V<0)
64         dEvdx = -1e3;
65     end
66     dx = xm/300;
67
68     for i = 1:300  %numerical integration using the
           midpoint method
69       x = xm*(1-i/300);
70
71       %nd = gauscAs(x);
72
73       Ev_mid = Ev - dEvdx*dx/2;  %Ev at the midpoint
74       rho_mid = - na - Nc*exp(-(Eg+Ev_mid)/(kb*T)) + Nv*
             exp(Ev_mid/(kb*T)); %+nd
75       dEvdx_mid = dEvdx - echarge*rho_mid*0.5*dx/eps;
76       Ev = Ev - dEvdx_mid*dx;
77       dEvdx = dEvdx - echarge*rho_mid*dx/eps;
78     end
```

```
79
80      Vs = Ev0 - Ev;
81      Es = dEvdx;
82      Eox = Es*eps/eps_ox;
83      Vtmp = Vs + Eox*tox;
84
85  %binary search
86      if (V<0)
87        if (Vtmp > V)
88            xl = xm;
89            xm = (xr + xl)/2;
90        end
91        if (Vtmp < V)
92            xr = xm;
93            xm = (xr + xl)/2;
94        end
95      elseif (V>=0)
96        if (Vtmp < V)
97            xl = xm;
98            xm = (xr + xl)/2;
99        end
100       if (Vtmp > V)
101           xr = xm;
102           xm = (xr + xl)/2;
103       end
104     end
105   end
106
107 % This section solves the Possion equation one more time
      using the optimized initial conditions
108 % and saves the data in arrays so it can be plotted.
109
110     Ev = Ev0;
111     dEvdx = 0;
112     if (V>0)
113         dEvdx = 1e3;
114     end
115     if (V<0)
116         dEvdx = -1e3;
117     end
118     dx = xm/300;
119
120     %save = zeros(300,2);
121     for i = 1:300  %numerical integration using the
          midpoint method
122       x = xm*(1-i/300);
123
124       %nd = gauscAs(x);
125       %save(i,1) = x;
126       %save(i,2) = nd;
```

```
127
128
129         Ev_mid = Ev - dEvdx*dx/2;  %Ev at the midpoint
130         rho_mid = - na - Nc*exp(-(Eg+Ev_mid)/(kb*T)) + Nv*
                exp(Ev_mid/(kb*T)); %+ nd
131         dEvdx_mid = dEvdx - echarge*rho_mid*0.5*dx/eps;
132         Ev = Ev - dEvdx_mid*dx;
133         dEvdx = dEvdx - echarge*rho_mid*dx/eps;
134
135         dEv{i} = [1e6*x,Ev]; %Zugriff auf array: d1{i}(1
                oder 2)
136         dEc{i} = [1e6*x,Ev+Eg];
137         n = Nc*exp(-(Eg+Ev)/(kb*T))/1e21;
138         p = Nv*exp(Ev/(kb*T))/1e21;
139
140         % add ionized donors
141 %         Naminus = na/(1+4*exp(eVtoJ*(Ea-Ef)/(kB*T)));
142 %         Ndplus = nd/(1+2*exp(eVtoJ*(Ef(i+1)-Ed)/(kB*T)));
143
144         dn{i} = [1e6*x,n];
145         dp{i} = [1e6*x,p];
146         drho{i} = [1e6*x,p-n-na/1E21]; %+nd
147         dE{i} = [1e6*x,dEvdx*1E-6];
148       end
149
150       dn{301} = [0,0];
151       dn{302} = [-1E6*(0.25*xp+tox),0];
152       dp{301} = [0,0];
153       dp{302} = [-1E6*(0.25*xp+tox),0];
154       drho{301} = [0,0];
155       drho{302} = [-1E6*tox,0];
156       drho{303} = [-1E6*tox,-drho{300}(1)];
157       drho{304} = [-1E6*(tox-xm/100),-0.92*drho{300}(1)];
158       drho{305} = [-1E6*(tox+xm/100),-0.92*drho{300}(1)];
159       drho{306} = [-1E6*tox,-drho{300}(1)];
160       drho{307} = [-1E6*tox,0];
161       drho{308} = [-1E6*(0.25*xp+tox),0];
162       dEF{1} = [1E6*xm,0];
163       dEF{2} = [0,0];
164       VIB = Ev0 - Ev;
165       Es = dEvdx;
166       Eox = Es*eps/eps_ox;
167
168       Q = -Es*eps; % the charge on the semiconductor
169       Vtmp = VIB + Eox*tox;
170       dEF{4} = [0,0]; %null;
171       dEF{5} = [-1E6*tox,-Va];
172       dEF{6} = [-1E6*(0.25*xp+tox),-Va];
173       dE{301} = [0,Eox*1E-6];
174       dE{302} = [-tox*1E6,Eox*1E-6];
```

```
175       dE{303} = [-tox*1E6,0];
176       dE{304} = [-1E6*(0.25*xp+tox),0];
177       dEc{301} = [0,dEc{300}(2)+1];
178       dEc{302} = [-1E6*tox,dEc{300}(2)+1- Eox*tox];
179       dEc{303} = [-1E6*tox,-Vtmp];
180       dEv{301} = [0,dEv{300}(2)-1.1];
181       dEv{302} = [-1E6*tox,dEv{300}(2)-1- Eox*tox];
182       dEv{303} = [-1E6*tox,-Vtmp];
183
184       if (V==0)
185         dEv{1} = [1E6*xp,Ev0];
186         dEF{1}  = [1E6*xp,0];
187         dEc{1}  = [1E6*xp,Ev0+Eg];
188         dn{1} = [1E6*xp,0];
189         dp{1}  = [1E6*xp,na/1E21];
190         drho{1}  = [1E6*xp,0];
191         dE = [];
192         dE{1} = [1E6*xp,0];
193         dE{2} = [-1E6*(0.25*xp+tox),0];
194       end
195
196
197       %plot bands
198  dEc = reshape(cell2mat(dEc'),[303,2]);
199  dEv = reshape(cell2mat(dEv'),[303,2]);
200  dEF = reshape(cell2mat(dEF'),[5,2]);
201  dEi = zeros(size(dEc));
202  dEi(:,1) = dEc(:,1);
203  dEi(:,2) = dEc(:,2) - Eg/2;
204  dEi = dEi(1:300,:);
205
206  figure
207  plot(dEc(:,1),dEc(:,2),'r',dEv(:,1),dEv(:,2),'b',dEF
         (1:3,1),dEF(1:3,2),'k',dEF(4:end,1),dEF(4:end,2),'k',
         dEi(:,1),dEi(:,2),':k')
208  legend('E_c','E_v','E_F','E_i')
209  title('Band diagram')
210
211 %plot charge density
212  dp = reshape(cell2mat(dp'),[302,2]);
213  dn = reshape(cell2mat(dn'),[302,2]);
214  drho = reshape(cell2mat(drho'),[308,2]);
215
216  figure
217  % p & n are divided by 1e21 so plot N_a & N_d divided by
         1e21 as well
218  plot(dn(:,1),dn(:,2),'r',dp(:,1),dp(:,2),'b',drho(:,1),
         drho(:,2),'k')
219  legend('n','p','\rho')
220  title('charge densities')
```

```
221
222 figure
223 subplot(3,1,1)
224 plot(dn(:,1),dn(:,2)*10e21)
225 title('n')
226 subplot(3,1,2)
227 plot(dp(:,1),dp(:,2)*10e21)
228 title('p')
229 subplot(3,1,3)
230 plot(dp(:,1),na*ones(length(dp),1))
231 title('N_a')
232
233 %plot electric field
234 dE = reshape(cell2mat(dE'),[304,2]);
235
236 figure
237 plot(dE(:,1),dE(:,2))
238 title('E field')
```

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