# Realization and Verification of Wirebond Interconnects for Heterogeneous 2.5D Integration of RF Chips

Master's Thesis

*By*

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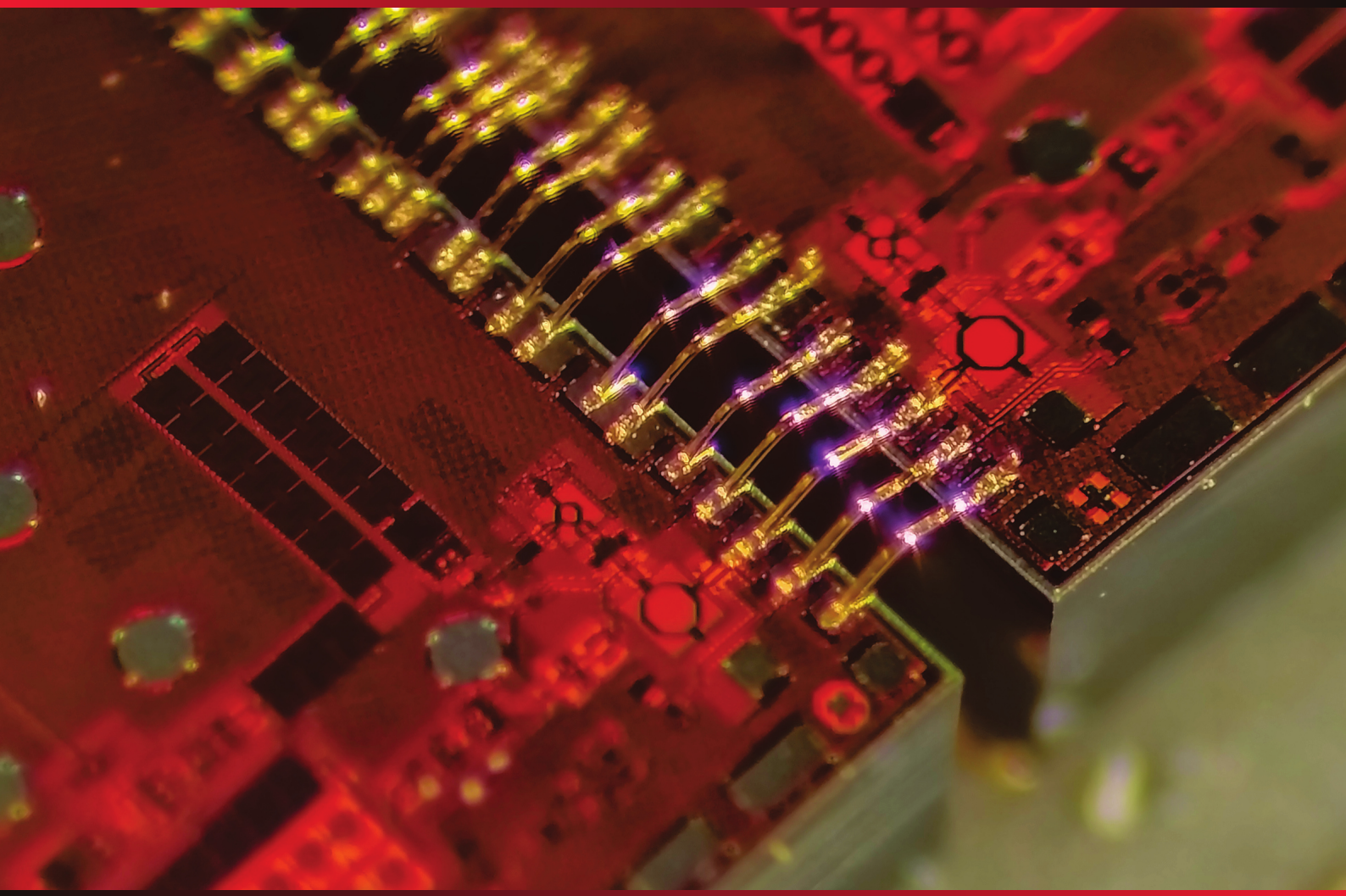
Graz University of Technology



# Realization and Verification of Wirebond Interconnects for Heterogeneous 2.5D Integration of RF Chips

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# Declaration

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# Abstract

In order to reduce costs in chip manufacturing, the semiconductor industry is moving towards chip-to-chip integration on silicon interposer technology. Wire bonding is one of the available interconnect technologies, which is investigated and verified in this work. The aim of this thesis is to demonstrate the performance of wirebonds for 2.5D integration of RF chips and to show their implementation. Because RF chips use GSG (Ground-Signal-Ground) pads, interconnecting GSG pads can offer short return paths. Furthermore, because of the strong mutual coupling in GSG interconnects, the loop inductance can be further reduced.

In this work, wirebonds are investigated for RF applications, from theory to practice. Specifically, GSG wirebonds are simulated, implemented and measured. From the measurements, an equivalent circuit model is extracted and analyzed. The main finding of this work is that GSG wirebonds demonstrates the optimal wirebond configuration for "Heterogeneous 2.5D Integration of RF Chips".

# Kurzfassung

Um Kosten in der Chipherstellung zu reduzieren, bewegt sich die Halbleiterindustrie in Richtung Chip-zu-Chip Integration auf Silizium-Interposer-Technologie. Wire-Bonding ist eine der verfügbaren Verbindungstechnologien, welche in dieser Arbeit untersucht und verifiziert wurde. Das Ziel dieser Arbeit ist die Fähigkeiten von Wirebonds für 2.5D-Integration von RF-Chips zu demonstrieren und deren gute Implementierungsmöglichkeit zu zeigen. Weil RF-Chips GSG-Pads (Ground-Signal-Ground) verwenden, können GSG-Verbindungen kurze Stromrückwege bieten, was in dieser Arbeit von besonderer Bedeutung ist. Darüber hinaus kann durch die starke Gegeninduktion in GSG-Verbindungen die Schleifeninduktivität weiter reduziert werden.

In dieser Arbeit, wurden Wirebonds für HF-Anwendungen untersucht, von der Theorie zur Praxis. Insbesondere wurden GSG-Wirebonds simuliert, implementiert und gemessen. Aus den Messungen wurde ein Ersatzschaltbild extrahiert und analysiert. Die wichtigsten Ergebnisse und Erkenntnisse dieser Arbeit ergaben dabei, dass GSG-Wirebonds die optimale Wirebond-Konfiguration für "Heterogeneous 2.5D Integration of RF Chips" darstellen.

# Acknowledgment

I would like to show my appreciation towards few people who have helped me throughout my journey on this thesis. First, I would like to thank Erich Leitgeb for supervising my work and being very supportive when I first suggested the topic to him. I also thank Michael Gadring for always offering me his time for fruitful discussions on many RF topics. I thank Dominik Amschl for showing me how to operate the bonder machine and the wafer probe station. I am also grateful to Daniel Eisenkölbl from the Institute of Electronics for his additional support and guidance on how to use the bonder machine. In general, I am very grateful to all who helped me, whether it was technical discussions or social interactions, or even just by waving and saying hello. To conclude, many thanks goes to my family for their continuous support... THANK YOU!

# Contents

# Chapter 1

# Introduction

The trend of increasing the frequency in mobile communication systems is becoming more popular than ever, thus resulting in using shorter waves, e.g., millimeter-waves (mm-waves). This can especially be observed nowadays with the deployment of the 5th Generation (5G) communication systems, which use mm-waves. Because of the very short wavelength of these frequencies, it is becoming difficult and cost inefficient to build transceivers on Printed Circuit Boards (PCBs) that uses multiple Integrated Circuits (ICs). There are several reasons for the difficulty to integrate on PCBs at higher frequencies. For example, at mm-waves the wavelength[1] is—as the names suggest—in the millimeter range, hence the waves themselves can in many cases be shorter than the size of the IC itself. Therefore, designing systems on PCBs at these frequencies require careful considerations. One way to overcome these issues is by designing all functional blocks on the same IC, hence System on a Chip (SoC). While SoCs are popular, they have their own drawbacks. For example, by increasing the functionalities, hence the complexity, of a SoC, the die size on the wafer also increases, which has a negative impact on the production yield. Furthermore, thermal management of SoC becomes challenging because of the high-density design. A middle solution to overcome these issues is by integrating and interconnecting the individual functional blocks (i.e., chips) in a single module, e.g., 2.5D or 3D integration. This can solve several issues:

- A better yield compared to SoC solutions.
- Shortening the electrical connection between the chips, thus reducing inductance and improving signal integrity.
- Miniaturization of the overall design compared to PCB approach.
- IP reuse; this allows for simpler designs and cost reduction in manufacturing.
- Temperature decoupling, i.e., if one chip heats, the rest should not be affected significantly (this is not the case in SoC).

The integration methods can vary depending on the used technology. In this thesis the focus is on 2.5D integration, i.e., the chips are integrated on an interposer in a planar fashion. This type of integration requires technologies to achieve ideal electrical connection between the chips. The most popular (and adopted by the industry)

[1] After the consideration of the dielectric constant of the board.

interconnect technologies are: **1.** wirebonds; **2.** flip-chip. An illustration of these two methods is depicted in Figure 1.1. With wirebonds the chips are connected with fine wires of gold or aluminum, usually with a diameter of 25 $\mu$m. With flip-chip, however, the chip's pads are connected directly on the interposer by flipping the chip upside down. For each own advantages and disadvantages. For example, wirebonds tend to have higher inductance compared to flip-chip, but the implementation process for wirebonds is much simpler than flip-chip, and fewer restrictions are imposed.

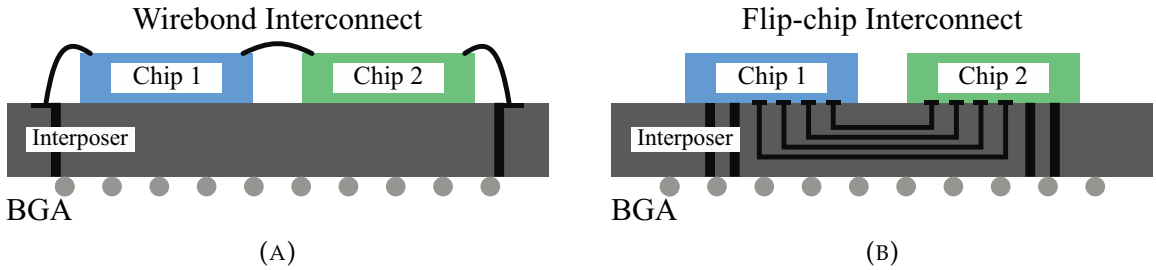



FIGURE 1.1: Illustration of interconnects in 2.5D integration. (A) Wirebond; (B) Flip-chip.

Another advantage of chip integration is the possibility to integrate between optical and RF (Radio Frequency) domains, e.g., interconnecting photonic chips (e.g., photo diodes, lasers,...etc.) with RF chips (e.g., TIA (Transimpedance amplifier), limiting amplifier,...etc.). By having optical interfaces, we can build modules where the modules are interconnected with each other in the optical domain e.g., using optical PCBs [1]. By utilizing heterogeneous integration between the optical and the RF domains, we can eliminate most of the inherent issues of RF signals (e.g., mismatching) and increase the data rate up to hundreds of Gbps [2]. Figure 1.2 depicts an illustrative sketch on how a heterogeneous integration between optics and RF can be implemented.

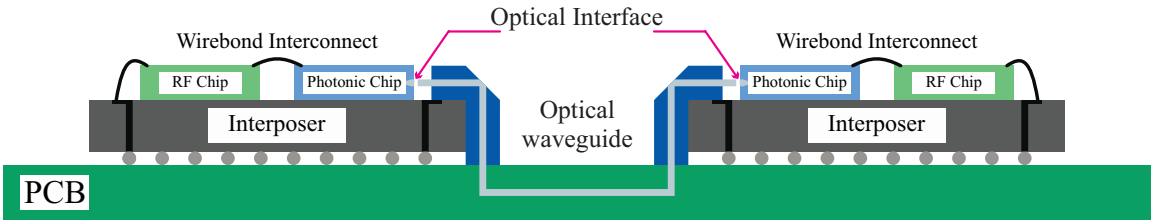



FIGURE 1.2: Illustration of using optical signals to interconnect between heterogeneous integrated systems.

## 1.1 Thesis Objectives

The aim of this thesis is to investigate the performance and the limitation of wirebonds as interconnects for 2.5D integration of RF chips. The thesis covers the principles of wire bonding and its mechanical limitation and the available technologies. Using interposers as the basis for 2.5D integration is also discussed. Afterwards, the discussion goes to the modeling aspect of wirebonds and presenting Electromagnetic (EM) simulations and comparing them with their equivalent analytical solutions. Later in the

thesis, methods for estimating the equivalent circuit model from S-parameters measurements are presented. Finally, GSG (Ground-Signal-Ground) wirebonds measurements are presented and analyzed.

The motivation behind this thesis was the requirement of using wirebonds as chip-to-chip interconnect in the project *TriTon* at the *Institute of Microwave and Photonic Engineering, TU Graz*. This project tries to demonstrate the possibility of reliable heterogeneous integration between the optical and the RF domains. Achieving such integration can bridge new technologies to use optical signals.

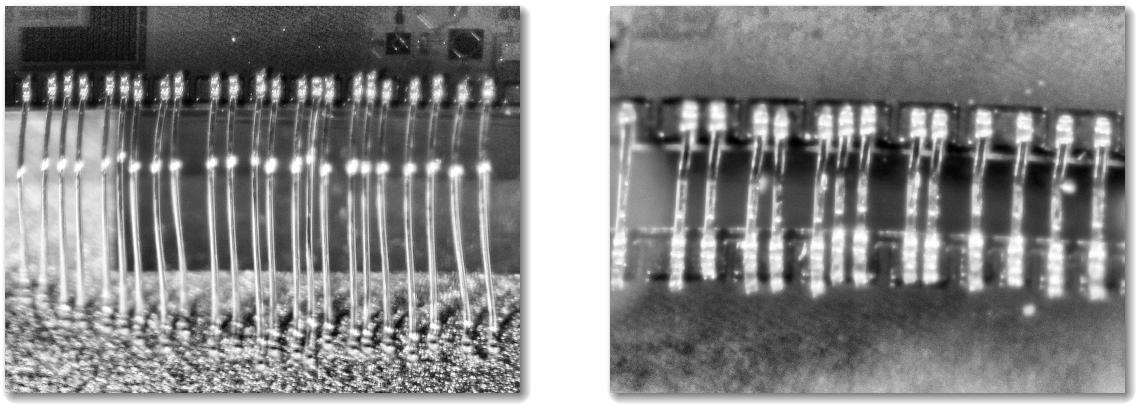
## 1.2 Thesis Outline

The thesis is divided as follows: Chapters 2 covers the topic wire bonding in various aspects, from the mechanical standpoint to the electrical proprietaries for RF applications. Chapter 3 covers the principle of 2.5D integration and discuss how such technology is implemented. Chapter 4 discuss the electrical modeling of wirebonds, in both EM simulations and analytical solutions. Chapter 5 discuss the principles used to extract wirebond models from S-parameters measurements. This involves deembedding, and optimization to extract circuit parameters. Chapter 6 presents psychical implementation of GSG wirebonds and their measurements. From the obtained measurements, a circuit model is extracted and analyzed. Finally, Chapter 7 summarizes the work and presents possible future work. Miscellaneous topics are found in appendices—this includes discussion on Bézier curves and MATLAB scrips which were used in this thesis.

# Chapter 2

# Wire Bonding

The aim of wire bonding is to create electrical interconnection, e.g., chip-to-substrate or chip-to-chip. This chapter covers the basics of wire bonding and discuss different technologies.



(A) (B)

FIGURE 2.1: 25 $\mu$m Au wedge wirebonds. (A) Chip-to-substrate; (B) Chip-to-chip.

## 2.1 Wire Bonding Technologies

There are three majorly used wirebond technologies in the industry [3], [4]: **1)** Thermocompression Bonding; **2)** Ultrasonic Bonding; **3)** Thermosonic Bonding. In the following subsections, the mechanical processes of these technologies are discussed.

### 2.1.1 Thermocompression Bonding

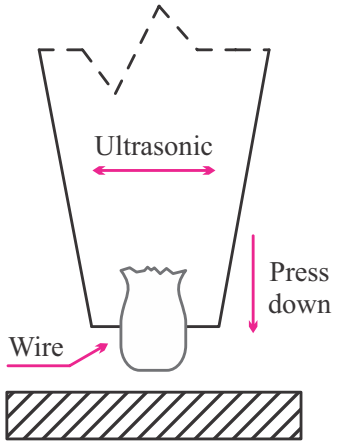
Thermocompression bonding is the most trivial way of welding two metals, i.e., with heat and pressure. The process is simple, the bonding interface is heated to a very high temperature to softener both the wire and the bonding surface. With force the wire is pressed on the bonding surface, thus sweeping any contamination away. Afterwards, a plastic deform is achieved to create a solid-state fusion between the metals. The most common wirebond material used for this process is Au (gold), and it is also commonly used on Au pads [3].

This method of wire bonding is not used nowadays, as thermosonic bonding took its place. The major limitation of thermocompression is the high temperature (> 300°C), as few chips can handle such temperatures. Thermosonic bonding solved this problem by reducing the temperature with the addition of ultrasonic energy.

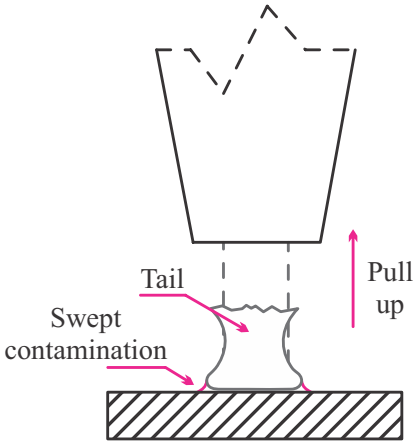
### 2.1.2 Ultrasonic Bonding

In ultrasonic bonding, the bonding process is friction based, where the ultrasonic energy at a frequency around 63.3 kHz [5] cause the wire to vibrate laterally, thus causing it to scrub on the bonding surface when pushed down on it. Doing so results in the sweep of any contamination and expose a clean interface for the bonding (see Figure 2.2). There are three main parameters for controlling ultrasonic bonding:

- **Ultrasonic Power:** The higher the power, the more vibration takes place. This parameter is the key ingredient for the entire process. Having it too high will most likely damage the bond, while having it too low will not remove the contamination, thus resulting in poor bonding (if any). Choosing the optimal power level is highly dependent on the bonder machine and how the power is applied (e.g., applied only on the wire, or both wire and bonding surface), but it mainly depends on the force parameter. In general, by increasing the applied force, lesser ultrasonic power is required[1].
- **Force:** To achieve a fusion between two metals you need force. Like ultrasonic power, the optimal value for force depends on various factors, e.g., wire diameter, flatness of the bonding tool (wedge tool), ultrasonic power...etc.
- **Time:** This is the time duration for how long the wire is pressed on the bonding surface. This should be long enough to ensure that enough ultrasonic energy is transferred. For example, in [5] they recommend $100 - 200$ ms.




The wire is in motion (horizontal) due to ultrasonic, while being pressed down.



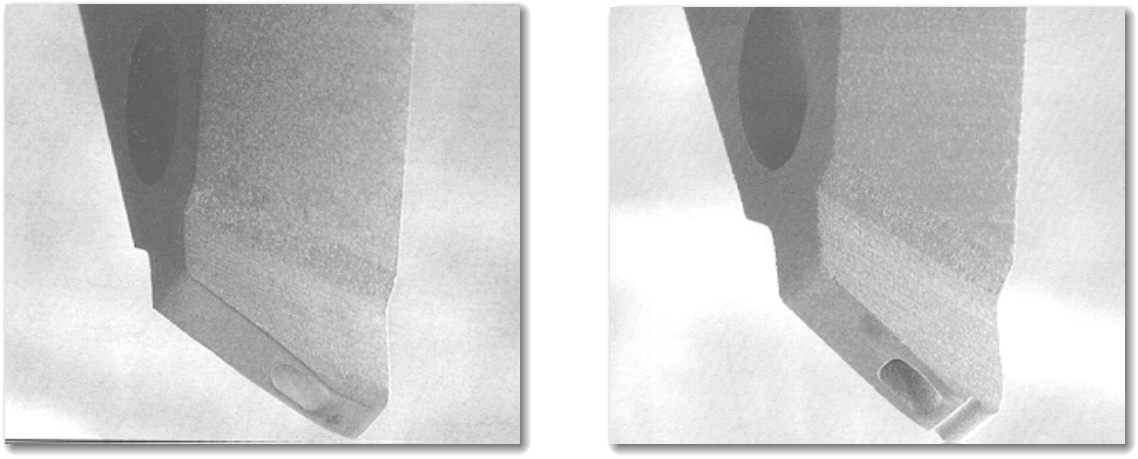

Contamination is cleared, thus allowing for friction based welding.

FIGURE 2.2: Ultrasonic bonding process.

[1] This is true to a certain limit. The main keyword is vibration. If reducing ultrasonic power causes the vibration effects to disappear—then that is the limit. Without vibration, all bonds will be poorly done.

You can notice that the process does not require heat, thus it can be performed at room temperature. Because of the lack of heat from the process, usually Al (aluminum) wires are used, whereas bonding pads can either be Al or Au. There is also the possibility of using Au wires, but because Au requires additional heat (~120°C) to achieve a solid-state fusion, Au wire bonding with ultrasonic is listed under thermosonic bonding (see following subsection). Because of ultrasonic bonding being used at room temperature, it is mainly used for applications where bonded chips are sensitive to heat.

The most common tool used for ultrasonic bonding is a wedge tool. Figure 2.3 depicts two variants of wedge tools; the one on the left (A) is a wedge tool for ultrasonic Al bonding, since it has a flat tip[2]; while on the right image (B) is used for thermosonic Au bonding because of the cross groove on its tip. The groove is necessary to improve the gripping between the Au wire and the wedge during bonding (this is not necessary with Al wires). Wedge tools have many parameters to adjust. For example, for low stress looping, it is advised to use a wedge tool that has a feeding angle of 30°. Though, companies that manufacture these tools usually provide a manual guide for selecting appropriate wedge tool for an application.



(A) (B)

FIGURE 2.3: Wedge tools. (A) for Al wires; (B) for Au wires.
(after K&S Micro-Swiss [6, Sec. A2.3.2])

Last, Figure 2.4 depicts a simplified illustration of wedge bonding process, from first bond to second bond. The process starts by applying force and ultrasonic on the first bond (Figure 2.4a). Afterwards, the wire is looped towards the second bond and bonded similar to the first bond (Figure 2.4b). Finally, the wire is broken, and the bonding is completed (Figure 2.4c). There are various ways to break the wire after the second bond, e.g., *Table Tear* or *Clamp Tear*. Depending on the method used to break the wire, the length of the wire tail can influence later bonds. For example, if too much wire is torn, later bonds might fail, as less wire would be expose underneath the wedge tool. The wire breaking mechanism is very important for automatic bonding machines, and selecting the right tool has an important impact on the quality of the tearing process. It should also be noted that when looping towards the second bond, the wedge tool needs to stay in a straight line. If the tool is moved slightly, this can cause the wire to slip from underneath the wedge tool, resulting in the second bond to fail (this is not the case in thermosonic ball bonding).

[2]In some designs, the tip might be slightly concave, see Section 2.3.2.

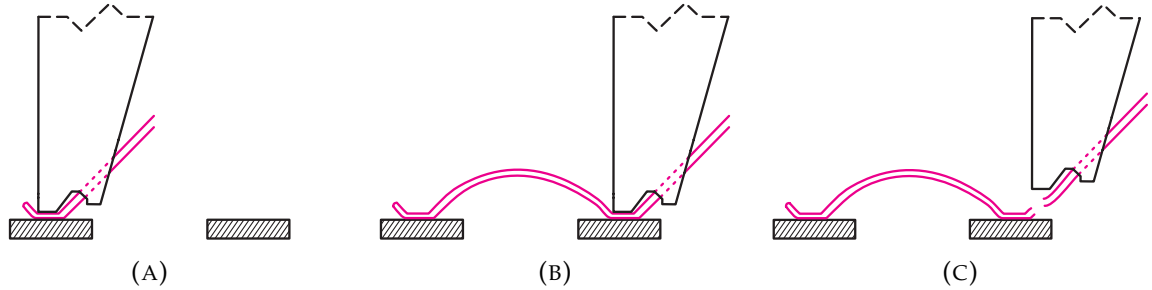



FIGURE 2.4: Wedge bonding process.

### 2.1.3 Thermosonic Bonding

Thermosonic bonding is the combination of ultrasonic and thermocompression bonding with the approach of optimizing the best qualities of each method [4]. As discussed previously on thermocompression bonding, this method requires very high temperatures (> 300°C). Such temperatures can be damaging for some sensitive chips. However, in thermosonic bonding the interface temperature can be much lower, around 120°C, thus avoiding problems of damaging chips because of high temperatures. The ultrasonic energy in this process helps to sweep contamination during the bonding cycle, which helps mature the solid-state fusion in combination with thermal energy.

Essentially, thermosonic bonding is identical to ultrasonic bonding, and it follows the same consideration on choosing the process parameters (i.e., ultrasonic power, force, time). The only difference is the addition of temperature in which inherently will require the reduction of ultrasonic power and force. The most common bonding wire is Au, and typically ball bonding is the adopted method for performing thermosonic bonding. In ball bonding process, the used bonding tool is a capillary (usually made of ceramic), which presses on the 'ball' to form a bond. Figure 2.5 shows an image of a capillary tool and ball bonds.

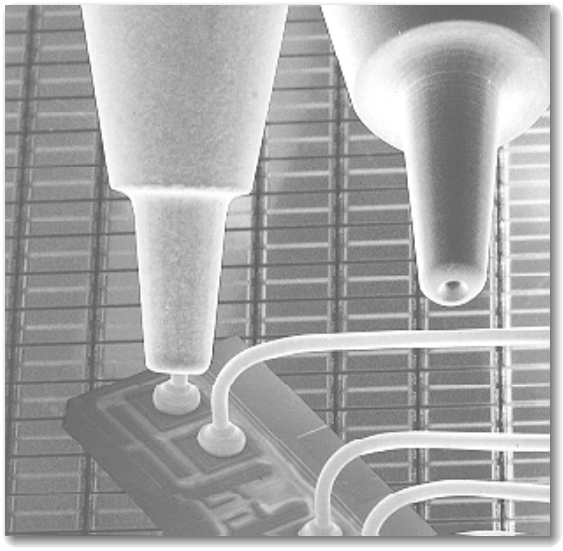


FIGURE 2.5: Capillary for Au ball bonding (after K&S Micro-Swiss [6, Sec. A2.3.2]).

As mentioned in the section of ultrasonic bonding, wedge bonding can also be used in thermosonic Au bonding, but it is less commonly used as it requires special wedge

tools (see Figure 2.3b). Last, Figure 2.6 shows a step-by-step process of thermosonic ball bonding.

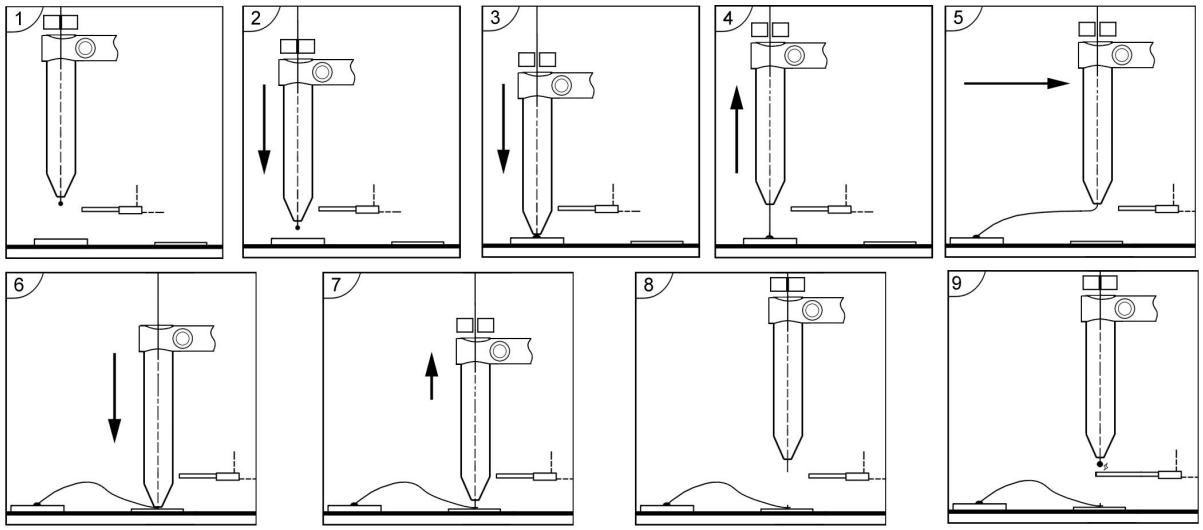



FIGURE 2.6: Thermosonic Au ball bonding (Source: TPT [5]).

1. Start position; the capillary is positioned over the targeted spot. The wire clamp is closed.

2. The wire clamp opens, and the capillary moves down to the bonding spot.

3. Formation of first bond; the capillary presses the ball down and touches the pad—the creation of the first bond is underway. With force being applied and ultrasonic power getting transmitted through the capillary, the ball is squashed, and the first bond is formed.

4. Raises to loop height; the looping of the wire begins. The capillary pulls upwards to the loop height.

5. Loop formation; there are many methods in which the loop can be formed, all depend on the trajectory of the capillary. The loop of the wire is very important for mechanical stability and longevity of wirebonds.

6. Second bond formation; similar process to the first bond.

7. Determination of tail length; the clamp opens, and the capillary rises to a position just enough to make the new ball. This height provides the equivalent ball volume from the tail length. Longer tail creates larger balls.

8. Wire tearing; the clamp closes and holds the wire. The capillary moves upwards, thus tearing the wire at the weakest point.

9. The capillary reaches the same height of the Electronic Flame-Off (EFO). The EFO discharges a very high voltage and melts the wire, which causes the ball to form. The amount of EFO current, the gap between the electrode, and the spark duration can all affect the ball size and shape.

## 2.2 Ultrasonic and Thermosonic Bonding Comparison

Table 2.1 summarizes the pros and cons of ultrasonic and thermosonic bonding[3]:

TABLE 2.1: Comparison between ultrasonic and thermosonic bonding [3].

| Bonding Technology | Pros | Cons |
|---|---|---|
| Ultrasonic | • Least susceptible to contamination.<br>• Reliable Al bonds at room temperature.<br>• Fine pitch.<br>• Shortest loops available. | • Automatic wedge bonders are slower ($< 1/2$) than automatic ball bonders.<br>• X-Y wire to pad orientation required (slows bonding processes).<br>• Poorly Au wirebonds without heat. |
| Thermosonic | • Less ultrasonic energy needed compared to ultrasonic bonding.<br>• All direction bonding from ball bonding.<br>• Automatic bonders are fast. | • Longer loops.<br>• More susceptible to contamination, compared to ultrasonic bonding.<br>• Fine pitch bonding is limited. |

## 2.3 Wire Bonding for RF Applications

Wire bonding for application at microwave and mm-wave frequencies are very challenging, as the parasitic of the wire become very apparent and can have a major impact on the performance of a chip. Wirebonds can be modeled as series inductance (see Chapter 4), and a general rule of thumb is to estimate its inductance in pH with the same length in $\mu$m. For example, if a wirebond has a length of 400$\mu$m, its inductance can be approximated to be 400pH. Later in Chapter 4 we learn that this rule is an overestimate of the actual value, but it gives a fast insight to what to expect from a wirebond. Figure 2.7 depicts the transmission coefficient (i.e., S21) of a series inductance in the range $L \in [0, 1]$ nH at 3 frequencies, $f = \{20, 30, 40\}$ GHz. Notice that only about 0.5 nH of inductance (around 500$\mu$m of wire length) is required to reduce the transmitted power by half at $f = 30$ GHz.

[3]Thermocompression bonding is neglected, as this method is no longer used anymore.

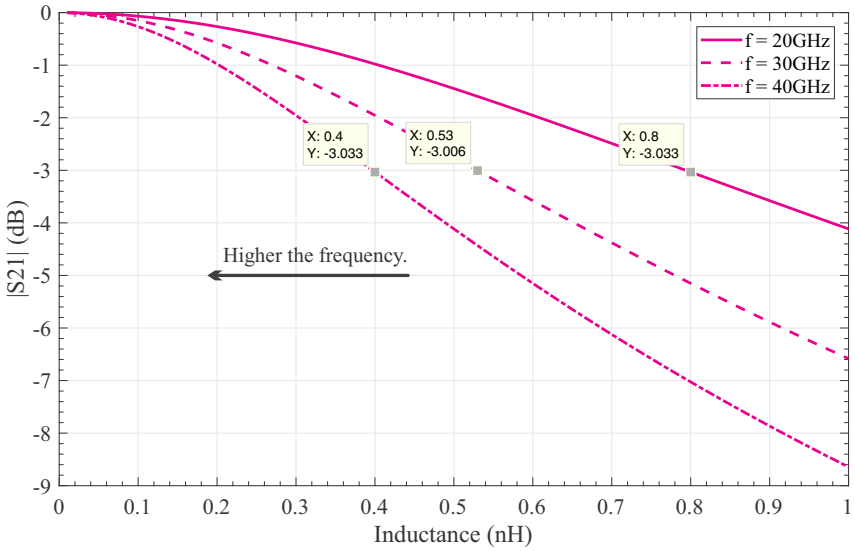



FIGURE 2.7: Transmission coefficient of a series inductance.

As seen, wirebonds with large inductance can cause a bottleneck in the performance of an RF chip. Luckily, the industry developed several methods to combat wirebond's inductance. Specifically, the focus will be on *Ribbon Bonding* and *(Ultra) Fine Pitch Bonding*. It is important to highlight that there are other methods to improve the performance of wirebonds without changing the bonding process, e.g., pad tuning in which the bonded pad is design to have specific properties to reduce the effects of the wirebond. Unfortunately, pad tuning can only do so little if the wires are long.

### 2.3.1 Ribbon Bonding

Ribbon bonding uses wedge process, but it differs from the traditional wedge bonding in the used wire—as the name suggests—the wire is a ribbon, which has a rectangular cross-section rather than circular. By using ribbon wires, we can achieve minimal bond deformation, thus allowing to bond on small pads. As a result, ribbon bonds are more preferred for RF applications because of the small bond deformation. For example, if we want to bond a pad with the dimensions $70 \times 70\,\mu$m using standard wirebonds, we would use a wire with a diameter of $25\,\mu$m. With ribbon bonds, however, we can use ribbons with a width of $50\,\mu$m. The question becomes: what is the difference between the two methods if both can provide reliable bonds? The answer is simple—the surface area. At high frequencies, currents flow at the surface of a conductor due to skin effects. In our example, if we assume the ribbon to have a thickness of $20\,\mu$m, then its surface area per unit length is calculated as

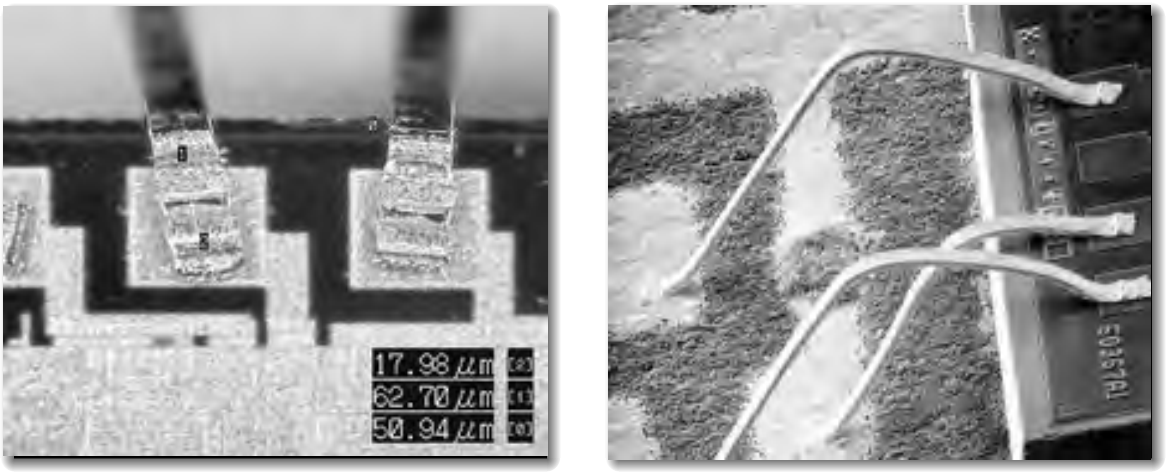
$$A_{ribbon} = 50 \times 2 + 20 \times 2 = 140\,\mu\text{m}^2/\mu\text{m}. \tag{2.1}$$

On the other side, the surface area per unit length of an $25\,\mu$m wirebond is equal to

$$A_{wire} = 25\pi = 78.54\,\mu\text{m}^2/\mu\text{m}. \tag{2.2}$$

We can observe that ribbons can achieve higher surface area, thus having less inductance. Another benefit of ribbons is the stress relief when looping. Because ribbons have wider cross-section relative to their thickness, they experience less stress when

forming loops. This allows for shorter bonds while not affecting the mechanical stability of the ribbons, hence less inductance. Generally, ribbon bonding is more robust than traditional wedge wire bonding, but the process itself is more challenging in terms of tooling and fine ribbon manufacturing. Ribbons are typically made either from Al or Au. Typically, Al ribbons are wider and thicker and are used to bond large pads for power electronics. On the other hand, Au ribbons can be made as fine as $20 \times 6\,\mu$m and used typically for low power RF electronics [7]. Later in Chapter 4 we compare both ribbons and wirebonds via EM simulation in a GSG configuration.




(A) (B)

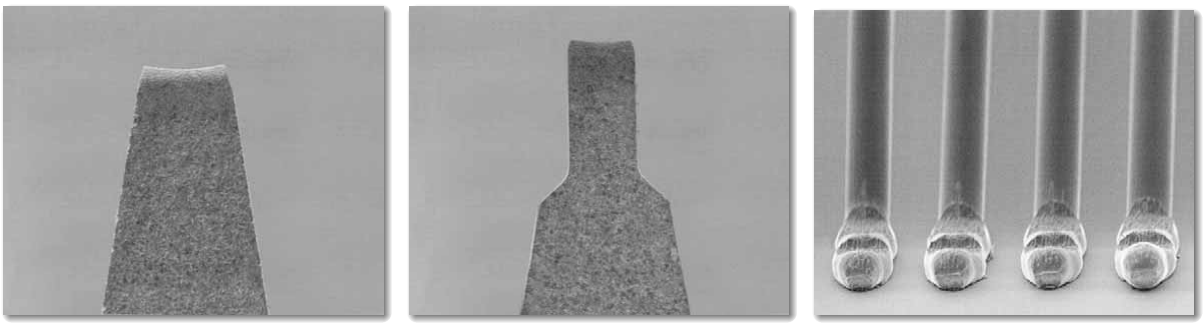
FIGURE 2.8: Fine ribbon bonding.
(Source: Adapted from Palomar Technologies [8])

### 2.3.2 Fine Pitch Bonding

The principle of fine pitch bonding is to get many bonds as close as possible. This can be done with both ball and wedge bonding processes. RF electronics can benefit from fine pitch bonding by being able to perform multiple wirebonds on the same pad, hence reducing wire inductance. Aside from being able to connect multiple wires at the same pad, fine pitch bonding allows designers to make chip pads smaller, thus reducing unwanted pad parasitic. Alternative, by having small pads, they can be placed very close to each other. If every two pads are assigned to have opposite polarity (e.g., signal and ground), this allows for the reduction of loop inductance due to the higher mutual inductance between the wires, which causes the overall inductance to decrease. Generally, pitch distances between pads are getting smaller than ever, and chips are becoming smaller than ever, therefore, fine pitch bonding is necessary to address these issues.

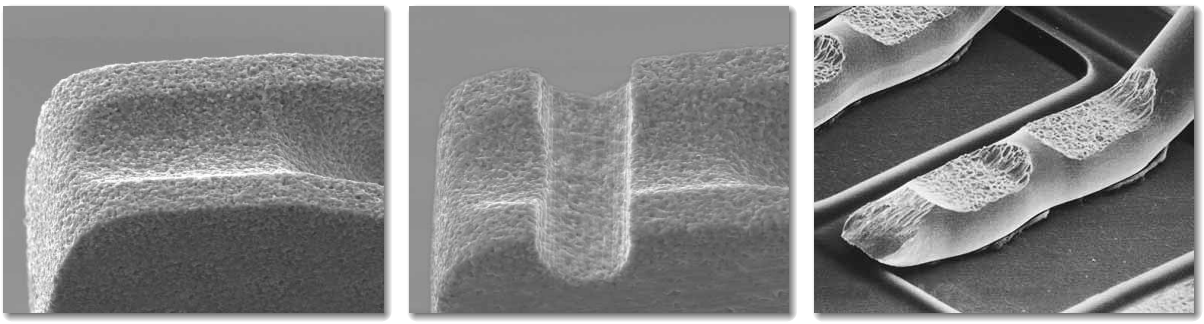
The design concept of fine pitch tools is relatively simple, but the implementation can be challenging due to the required precision in manufacturing of these tools. Figure 2.9 depicts images of both standard and fine pitch wedge tools. We can observe that in fine pitch tool we have a Vertical Side Relief (VSR) that cuts into the wedge sides. This relief exists to create a clearance between the loop and the adjacent wire when bonding. Another improvement on wedge fine pitch tools is the inclusion of a linear groove (concave cutout) on the tip of the wedge. The linear groove has the functionality of maintaining the wire inside the groove during bond creation. This prevents the wire

from deforming outside the groove, thus allowing for smaller bond deformation (see Figure 2.10).



(A) (B) (C)

FIGURE 2.9: Standard and fine pitch wedge tools (Source: Micro Point Pro [9]). (A) Standard wedge tool; (B) Fine pitch wedge tool; (C) Fine pitch wirebonds.



(A) (B) (C)

FIGURE 2.10: Reducing deformation width of wirebonds by incorporating a linear groove in wedge tools (Source: Micro Point Pro [9]). (A) Linear grooved wedge tool for Al bonding; (B) Linear and cross grooved wedge tool for Au bonding; (C) Au wirebond with linear and cross groove wedge tool.

# Chapter 3

# 2.5D Integration

The principle of 2.5D integration is to place multiple chips on a substrate and interconnect them electrically such that the overall functionality of the design is the interoperability of all chips together as if they were one unit. The concept itself as abstract is not new, rather this is always the case in PCBs. The premise of PCB design is to interconnect multiple functional blocks (passive components and various ICs) together to build an overall system that behave as a single unit. The problem in PCBs is their long interconnects, as they are often one of the many reasons for signal degradation with the increase of frequency. The solution for this problem is rather simple: *connect the bare chips together in a tighter footprint*. That is, we collect the chips on a substrate such that short interconnects are possible (e.g., flip-chip or wirebond). Another approach for chip integration is 3D integration, where chips are staked on each other. This method does indeed reduce interconnect lengths better than 2.5D integration, however, it has its own inherent problems that diminish its benefits in par with 2.5D integration. Figure 3.1 shows the evolution of chip integration.

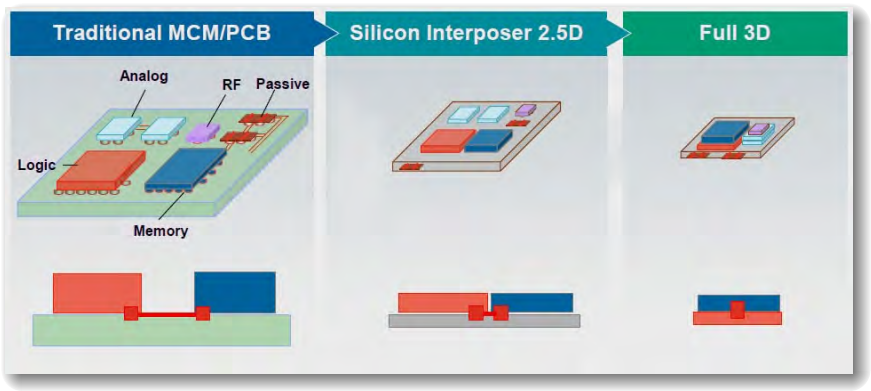



FIGURE 3.1: Evolution of chip integration (Source: Adapted from [10]).

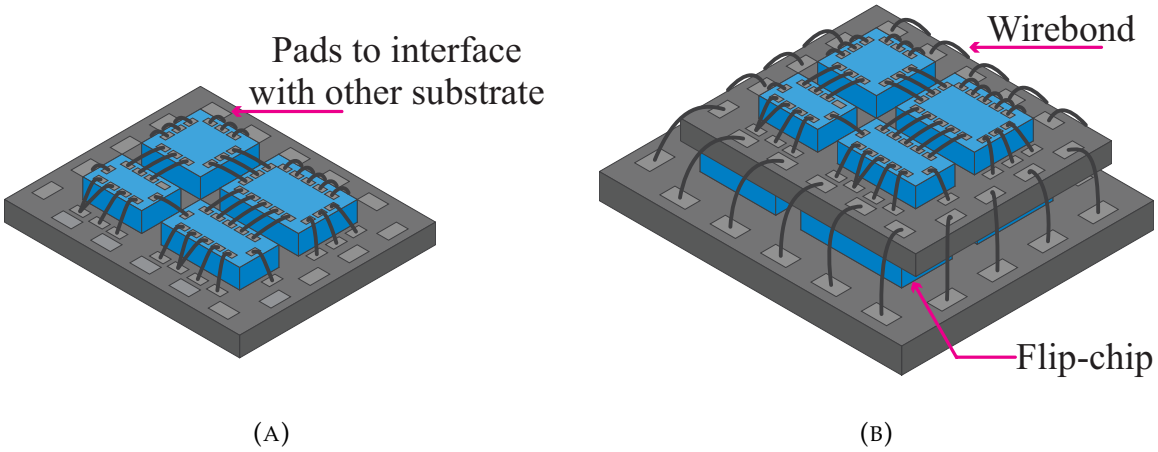
Before the adoption of silicon interposer 2.5D integration, the industry kept in the trend of 2D monolithic System on Chip (SoC) where all functional blocks are integrated in a single chip in the initial design. This approach became difficult to manage and cost inefficient, as many new processes and equipment are required. Moreover, SoC tend to take large space on a wafer, thus decreasing fabrication yield. These issues caused the semiconductor industry to shift its focus to concepts as 2.5D/3D heterogeneous integration [11].

## 3.1 Silicon Interposer

Implementation of 2.5D integration can be performed on many technologies, e.g., PCBs, but the problem with such technologies is the limitation of pad dimensions and clearances, e.g., nowadays PCBs can achieve 75 $\mu$m clearance [12]. To overcome such limitation, the industry shifted its focus to silicon interposer, e.g., using CMOS technology. The advantages are the compact structure and the ability to use Through Silicon Via (TSV) as short connection path to further expand the connection of the module to package or PCB (e.g., BGA). Depending on how the interposer is utilized, there are two types of silicon interposers: Passive and Active.

### 3.1.1 Passive Interposer

A passive interposer has the sole purpose of providing electrical routing between chips. It also provides interface, e.g., BGA, to further connect the module in a package or on a PCB. As a result of passive interposers not having active technologies within them, they are used similarly to PCBs, but with the advantages of the design rules of semiconductor processes. Typologies on how passive silicon interposers are used can vary depending on the application. For example, if we talk about 2.5D integration, then the interposer is used similar to Figure 3.2a. We can also use them as a carrier for 3D integration of multiple 2.5D modules (see Figure 3.2b).




(A) (B)

FIGURE 3.2: Illustration of usage of passive silicon interposer.
(A) 2.5D Integration; (B) 3D stacking of 2.5D modules.

### 3.1.2 Active Interposer

Even though the original purpose of using silicon interposer is to create interface routing for the integrated chips, we still can take advantage of the fact that silicon interposers are made using CMOS technology. As a result, we can implement special functionalities in the interposer. Below are few ideas:

- **Power Distribution:** The interposer will provide all the necessary DC voltages for all chips. The idea here is to build voltage regulators (e.g., DC-DC converters and LDOs) inside the interposer to convert the main DC rail to all different

voltage levels. This solution can help with the reduction in both the needed decoupling capacitors and the parasitic that comes from long traces in PCBs.

- **ADC/DAC Interfaces:** Having Analog-to-Digital (ADC) and Digital-to-Analog (DAC) converters on the interposer can allow for seamless heterogeneous integration and eliminate the need to implement ADC/DAC inside the chips, thus reducing their design complexity.
- **Clock Distribution:** Often multiple chips need different digital clock rates. To achieve these rates, there is usually a global clock in which it gets divided by an integer factor $M$ to produce the other clocks. The concept here is to have a global clock connected to the interposer, and the interposer then generates and distribute all necessary clocks. For example, this can be achieved by implementing a network of D-latches to divide the global clock.

## 3.2 Interconnect Technologies

### 3.2.1 Wirebond

The chips are placed next to each other, and their pads are bonded together. Other pads, e.g., DC supply or control buses, are connected to the interposer which then get routed in a package or on a PCB. The advantage of this type of interconnect is the flexibility and the low cost given the maturity of the technology. However, the disadvantage of such solution is the inductance the comes with it, which is proportional to the length of the wire. As a result, wirebonds for RF interfaces need to be kept as short as possible to reduce their inductance. This topic is further discussed in coming chapters.

### 3.2.2 Flip-chip

The abstract principle of flip-chip is rather simple, it consists mainly of connecting chips upside down on the interposer. The process starts by placing bumps (e.g., ball bumps) on the interposer's pads, and the chips are picked and flipped on the bumps. There are many ways to implement the bumps, e.g., solder bump, hard bump, or ball bump. The bonding process in the ball bump flip-chip is similar to wirebonds (see Chapter 2), i.e., applying ultrasonic, force and heat. Flip-chip is ideal for size constrained applications, as it does not require any extra overhead space for wire looping as in wirebonds. It also performs better in high-frequency applications as the interconnect lengths are kept to a minimum. Also, flip-chip are more reliable for packaged applications. More so, flip-chip technology is more efficient than wire bonding, as bonding of all pads happens simultaneously, whereas with wire bonding only one bond is made at a time. In practice, however, flip-chip is still considered cost ineffective for many applications, especially at low volumes. Additionally, the technology requires stricter design rules, e.g., bump pitch is kept in the 100 $\mu$m range. Another challenge is the interposer inter-routing. Flip-chip devices are often assembled on a high-dense multi-layer interposer. This increases the complexity of the interposer design and adds routing strategy requirements to account for signal integrity [11].

Although flip-chip is considered superior compared to wirebond, it is still not widely used, even though the technology existed for so long. This has to do with the process

being fairly restricted in availability. The question then becomes: *would flip-chip completely replace wirebond after it becomes widely available?*—probably not, mainly because of the flexibility of wirebonds. For example, let us consider a situation where a design of a chip is already finished and got manufactured. Now, depending on the chip design, an appropriate interposer must be made for it. Consider the situation if a company already has interposers (IP reuse), but are not designed for the specified chip. Assuming the interposer has all the necessity traces and number of pads, but the pads' location differ slightly from what it is required. The question now: how would you solve this issue?—In such scenarios, you have two choices, **1.** invest in making a new interposer for your design, **2.** connect it using wirebonds. In such a scenario, wirebond would be the cheaper solution, given that it fulfills the electrical requirements. In conclusion, wire bonding is here to stay and would probably co-exist with flip-chip technology (e.g., 3D stacking in Figure 3.2b).

# Chapter 4

# Wirebond Electrical Model

Understanding the electrical properties of wirebonds is necessary when designing chips or performing 2.5D integration. Having this knowledge allows for better designs, especially in RF applications. As discussed in Chapter 2, wirebonds are mostly inductive and their value depends on the length of the wire. The general rule of thumb is to estimate the inductance of wirebonds by their length, such that every micro-meter length corresponds to a pico-henry. This rule of thumb is a good first approximation, but it does not tell the full story. For example, it is known that the inductance of any conductive structure also depends on neighboring objects through mutual inductance. Modern 3D electromagnetic (EM) simulation software (e.g., CST Studio, Ansys HFSS, Ansys Q3D) can provide an accurate insight to the performance of wirebonds, and can handle very complex structures. However, even with the flexibility offered by these software, most designers still approximate the actual wirebond by segmentation into straight wires and compute their lumped values via analytical expression [13]. In many scenarios, a simple model consistent of series inductance and resistance often is enough to model wirebonds, even at high frequencies[1]. The discussion in this chapter revolves around estimating wirebond lumped elements via analytical expression and compare their results with EM simulation.

## 4.1 EM Simulation with Ansys Q3D

This section shows how basic simulations are done in Ansys Q3D. This is mainly for the purpose of reference and reproducibility of presented results in Examples 4.2.1, 4.2.2 and 4.2.3. The Q3D package software is a quasi-static EM simulator that has the functionality of extracting RLCG parameters (Resistance, Partial Inductance, Capacitance, Conductance) from an interconnect structure. The software is used in this thesis to compare its results with analytical expressions and show their validity. Below, I summarize the steps I took when performing the simulations:

1. Draw the 3D geometry.
2. Set a net for every solid object. This can be done by right-clicking on Nets in the Project Manager window and choosing Auto Identify Nets.

[1] This highly depends on neighbor objects and the location of ground plan. Parasitic capacitance often cause this simple model to fail at mm-wave frequencies.

3. Define a source and sink for every simulated object. This is done by selecting a face on the object and right click and choose Assign Excitation.

4. Add a new analysis setup. Here we define the frequency and the modeled quantity (R,C,L). A frequency sweep can also be defined.

5. If a parameter is to be swept, this is done in the Project Manager under Optimetrics.

6. Validate everything with the Validate bottom and click Analyze All.

7. After the simulation is done, the solution matrix can be reduced in dimension by clicking the according option in the Reduce Matrix in the Project Manager. For example, in Example 4.2.2 the ground plane is defined as a return path, thus reducing the solution dimension to give the loop inductance instead of partial self-inductance of each structure separately.

The results are accessed from the Results menu and can be extracted either in RLCG or S-parameters format (Touchstone).

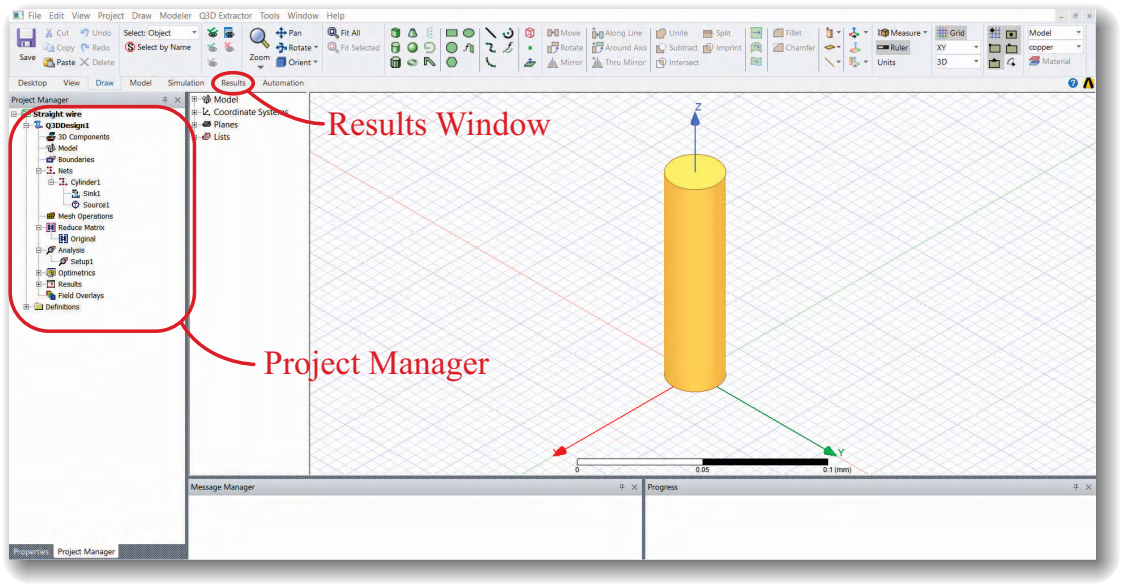



FIGURE 4.1: Ansys Q3D interface.

## 4.2 Equivalent Circuit Models of Wirebonds

As already highlighted in the introduction, wirebonds can be modeled with lumped elements. Figure 4.2 depicts the suggested models. The simple model of series inductance (partial inductance) and resistance can be enough to model wirebonds if capacitance parasitic from bond pad or neighboring ground lines are not too high relative to the frequency. If we want to include capacitance effects (e.g., ground plane), we extend on the simple model by including capacitors (see Figure 4.2c). Last, in special cases, if wirebonds are implemented to have a uniformly distributed structure between signal and ground nets, transmission line model can be used (see Figure 4.2b).

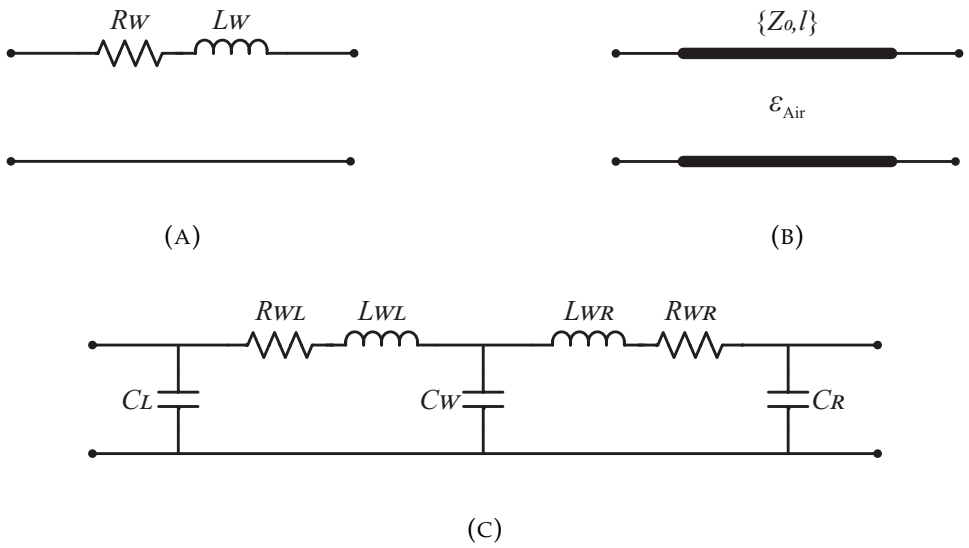



FIGURE 4.2: Equivalent circuit model of wirebonds. (A) A simple lumped model when parasitic capacitance is negligible. (B) Transmission line (typically lossless) model when wirebonds have uniform geometry around a ground net (e.g., coplanar structure). (C) A more complex lumped model to account for capacitance.

Following subsections provide analytical expressions to calculate wirebond equivalent circuit parameters and compare their results with EM simulation.

### 4.2.1 Straight Wirebonds

The first configuration to present is the case when the wirebond is straight. Even though it is almost impossible to get a straight wirebond, it is still a good approximation for various scenarios where the wire loop is not strongly curved. Such wirebonds are typically found in chip-to-chip interconnect applications, where the chips have the same thickness and bonding is done with a wedge tool. Even in cases where the looping of the wire is prominent, e.g., if the chips have different heights, we can still segment it into straight segments and analyze each segment and compute the overall effect from the individual segments (e.g., JEDEC standard [14]). Therefore, analyzing the effects of wirebonds as a straight wire is a good start. Figure 4.3 shows an illustration of a straight wirebond connecting two substrates (e.g., two chips). Generally, the wires are not fully floating in air, but there are few microns offset (e.g., 30 $\mu$m) after the pads to protect the chip from damaging during the process of die-sawing [15]. For now, however, we assume that the wire is fully floating in air.

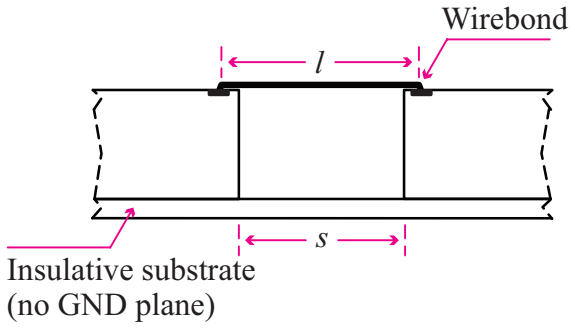



FIGURE 4.3: Illustration of straight wirebond.

Notice that no ground plane is considered here, as the purpose now is to investigate the effects of the wirebond as a discrete element. Therefore, the simple series inductance and resistance model is sufficient to describe the wirebond as a discrete element. The partial self-inductance of a wire with a circular cross-section is given by [16]

$$L = \frac{\mu_0}{2\pi} l \left[ \sinh^{-1}\left(\frac{l}{r}\right) - \sqrt{1 + \left(\frac{r}{l}\right)^2} + \frac{r}{l} \right] \qquad \text{(H)}, \tag{4.1}$$

where $r$ and $l$ are the radius and length of the wire, respectively. $\mu_0$ is the vacuum permeability. Eq. (4.1) can be further simplified if $l \gg r$ [16]

$$L \approx \frac{\mu_0}{2\pi} l \left[ \log\left(\frac{2l}{r} - 1\right) \right] \quad \text{if, } l \gg r. \tag{4.2}$$

Both Eqs. (4.1) and (4.2) describe the external inductance of the wire, i.e., the inductance seen when the current resides on the surface of the wire. This is the case at high frequencies due to 'skin effect'. If we want to include the 'DC' inductance[2], we need to add the term $l\mu_0/(8\pi)$ to Eq. (4.1) [16]. It should be noted here that the internal inductance approaches zero quickly with the increase of frequency, as the skin depth is inversely proportional to the frequency [16]

$$\delta = \frac{1}{\sqrt{\mu_0 \pi \sigma f}} \qquad \text{(m)}, \tag{4.3}$$

where $\sigma$ is conductivity of the wire in S/m, $f$ is the frequency, and $\mu_0$ is Vacuum permeability. The DC resistance of a cylindrical wire is given by

$$R_{DC} = \frac{l}{\sigma A} \qquad (\Omega), \tag{4.4}$$

where $\sigma$ is also here the conductivity of the wire in S/m, $A$ is the cross-section area of the wire, and $l$ is the wire length.

**Example 4.2.1** Inductance and Resistance of Straight Wire

To compare results of Eqs. (4.1) and (4.4) with EM simulation, we consider an Au wirebond, which has a diameter of 25 $\mu$m. The conductivity of Au equals $4.11 \times 10^7$ S/m. The simulated structure is depicted in Figure 4.4.

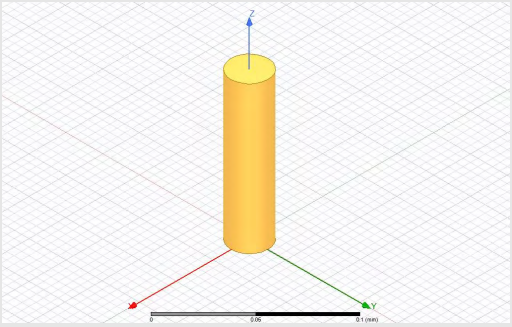


FIGURE 4.4: Simulated structure.

[2]To be correct here, there is no such thing called 'DC' inductance, because DC currents do not see inductance. It is just very common in various texts to write "DC" to refer to low frequencies.

The partial self-inductance is computed via Eq. (4.1) and the DC resistance via Eq. (4.4). For comparison, we use Ansys Q3D to extract the resistance and self-partial inductance of the wire. We run the simulation at 20 GHz while sweeping the length of the wire from 0.1 mm to 2 mm. From Figure 4.5, we can observe the almost perfect overlapping of the analytical expression with simulation.

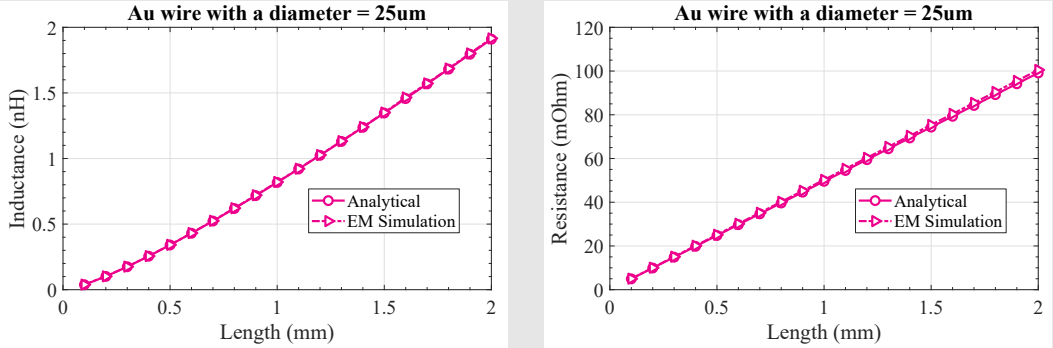



FIGURE 4.5: Inductance and Resistance of straight wire.

We now shift our focus now to the case when there is a ground plane underneath the wirebond—this is shown in Figure 4.6.

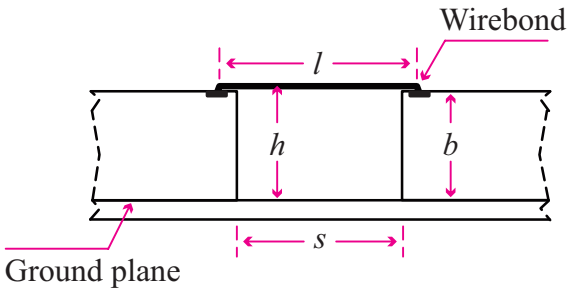



FIGURE 4.6: Straight wirebond over ground.

Because of the distributed capacitance between the straight wirebond and the ground plane, we can use a lossless transmission as a model. A lossless transmission line is characterized by its characteristic impedance $Z_0$. For a cylindrical wire with a length $l$ over a dielectric $\epsilon_r$ backed with a ground plane, the characteristic impedance is given by [17], [18]

$$
\begin{aligned}
Z_0 &= \frac{\eta_0}{2\pi\sqrt{\epsilon_{eff}}}\cosh^{-1}\left(\frac{1-u^2}{2R}+\frac{R}{2}\right), \quad \text{where...} \\
R &= \frac{2}{\frac{4h}{r}-\frac{r}{h}}; \qquad u = \frac{1}{\left(\frac{2h}{r}\right)^2-1}; \qquad \eta_0 = \sqrt{\frac{\mu_0}{\epsilon_0}} = 120\pi \\
\epsilon_{eff} &\approx \begin{cases} \dfrac{\log\left(\frac{2h}{r}\right)}{\log\left(\frac{2(h-b)}{r}+\frac{2b}{r\epsilon_r}\right)}, & \text{if } h-b > r \\ \dfrac{\epsilon_r+1}{2}, & \text{if } h-b = r \end{cases}
\end{aligned}
\tag{4.5}
$$

where the parameters in Eq. (4.5) are defined as follows:

- $\mu_0$ is the permeability of vacuum.
- $\epsilon_0$ is the permittivity of vacuum.
- $\eta_0$ is free-space impedance.
- $\epsilon_r$ is the relative permittivity of the substrate (dielectric constant).
- $\epsilon_{eff}$ is the relative effective permittivity. It is the effective averaged dielectric constant due to the presence of different materials around the wirebond.
- $r$ is the radius of the wirebond.
- $h$ is the height of the wirebond from the ground plane (see Figure 4.6).
- $b$ is the thickness of the substrate (see Figure 4.6).

The distributed lumped elements of a lossless transmission line, i.e., $L'$ and $C'$, can be calculated from the characteristic impedance $Z_0$ as

$$L' = \frac{Z_0\sqrt{\epsilon_{eff}}}{c_0} \qquad (\mathrm{H/m}) \tag{4.6}$$

$$C' = \frac{\sqrt{\epsilon_{eff}}}{Z_0 c_0} \qquad (\mathrm{F/m}) \tag{4.7}$$

where $c_0$ is the free-space velocity $\approx 3 \times 10^8\,\mathrm{m/s}$.

### 4.2.2 Curved Wirebonds

Although a simple and accurate equivalent circuit model of a straight wirebond can be easily developed, a perfect straight wirebond itself is not practically possible. This is because wirebonds require a loop for stress relief. Further, if we consider ball bonding specifically, there will always be a loop because of the ball. Figure 4.7 illustrate two cases of wirebond loops.

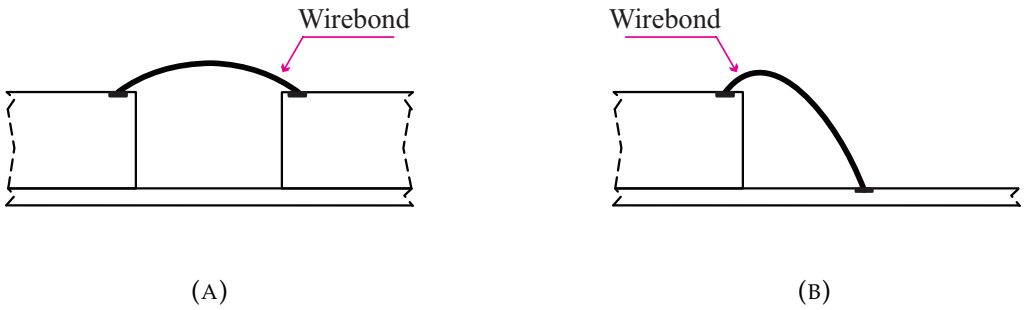



FIGURE 4.7: Illustration of curved wirebonds.
(A) Substrates at same heights (B) Substrates with different heights.

Because of the looping, we cannot model the wires as transmission lines, even if there exists a ground plane underneath the wirebonds. This is because the capacitance

of the wire to ground plane is height depended, and this parameter changes with wire curvature. Therefore, curved wirebonds must be modeled with discrete lumped elements. Similar to the non-grounded case, the wirebonds are modeled as series inductance and resistance, however, to count for ground effects, we need to include capacitors to the model. This can be done by placing a capacitor at each end (see Figure 4.8). A more comprehensive model would be achieved by using a T-structure and including the capacitors at both ends (see Figure 4.2c).

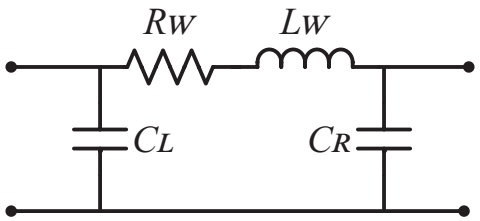



FIGURE 4.8: Simplified lumped model for curved wirebond.

To calculate the inductance of a wirebond while it is curved requires from us to have a parametric model of the wire geometry. Because wirebond loops tend to have non-consistent shapes, as the looping process depends on various mechanical factors. There is no general mathematical description for wirebonds. However, the next two subsections discuss how to approximate wirebond's loop and how to compute its equivalent circuit parameters.

### Straight Wire Segmentation

The concept of segmenting wirebonds into straight wire segments is a common practice by many engineers. This is done to estimate the loop shape of the wire, hence making it possible to compute the wire inductance and capacitance. Figure 4.9 depicts an example of segmenting a curved wirebond into three segments.

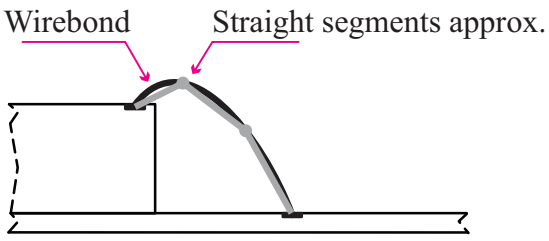



FIGURE 4.9: Illustration of line segmentation of curved wirebonds.

In the JEDEC Standard No. 59 [14], the wire is segmented into four straight segments (or even three). The idea behind this standard is to define a standardized geometric model of wirebonds, which later can be used in EM simulators. This approximation is widely accepted by the industry, and the model error is considered low.

However, this is only true at low frequencies. As a result of increasing the frequency, the slight addition or subtraction of inductance due to the approximation can give an inaccurate characterization of a wirebond.

Now, after discussing how to approximate the shape of the wirebond, the question becomes: how to analytically computes its inductance? For that, we use Neumann integral of mutual inductance in combination with the concept of partial inductance. The Neumann integral of mutual inductance describes the mutual inductance of two filamentary[3] current-carrying wires of arbitrary shape. This is given by [16]

$$M = \frac{\mu_0}{4\pi} \int_{l_2} \int_{l_1} \frac{d\mathbf{l}_1 \cdot d\mathbf{l}_2}{R} \qquad \text{(H)}, \tag{4.8}$$

where $l_1$ and $l_2$ are the lengths of the two wires, and $R$ is the distance between $dl_1$ and $dl_2$ (see Figure 4.10).

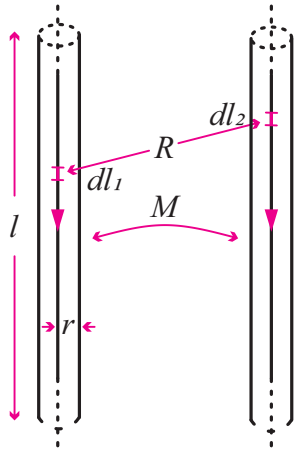



FIGURE 4.10: Illustration of partial mutual inductance of two wires.

The Neumann integral for mutual inductance in Eq. (4.8) can also be used to determine the partial self-inductance of a wire by letting the two wires to coincide [16]

$$L = \frac{\mu_0}{4\pi} \int_{l'} \int_{l} \frac{d\mathbf{l}' \cdot d\mathbf{l}}{R} \qquad \text{(H)}, \tag{4.9}$$

where $R$ is the distance from the wire core $dl$ to the interior edge of the wire surface $dl'$ (see Figure 4.11). Note that, even though the wires coincide, the integration is done over two different paths. This is because solving Eq. (4.9) while assuming $d\mathbf{l}' = d\mathbf{l}$ is impossible as $R$ can equal zero. To overcome this, we assume the current resides only on the surface of the wire, thus allowing us to integrate along the surface path. In other words, we assume full skin effect.

The capacitance of a wire above a ground plane can be accounted for by using the capacitance per unit length formula in [19]

$$C' = \frac{2\pi\epsilon}{\cosh^{-1}\left(\frac{h}{r}\right)} \qquad \text{(F/m)} \tag{4.10}$$

[3] Essentially, assuming an uniform flow of current.

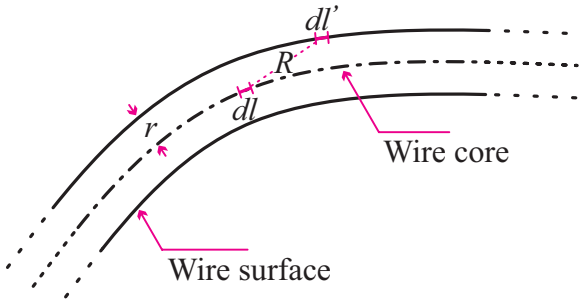



FIGURE 4.11: Neumann partial self-inductance of a wire.

where $\epsilon$ is the permittivity of the martial between the two conductors, $h$ is the height of the wire above ground, and $r$ is the wire radius (see Figure 4.12). The total capacitance of the wire is then computed by integrating along the wire length

$$C = \int_l C' \, dl = \int_l \frac{2\pi\epsilon}{\cosh^{-1}\left(\frac{h}{r}\right)} dl \qquad \text{(F)}. \tag{4.11}$$

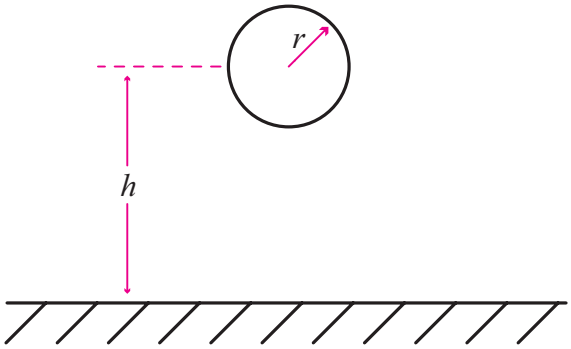



FIGURE 4.12: Capacitance of a wire above a ground plane.

To determine the values of the left and right capacitance shown in Figure 4.8, the integration is performed according to the wire length on each half.

The DC resistance does not differ from the capacitance. This is computed from the resistance per unit length equation, which happens to be the exact formula in Eq. (4.4) but without $l$. Thereafter, the resistance value is obtained by integrating along the wirebond curve. This turns to be exact to Eq. (4.4) if the cross-section area does not change with $l$.

$$R_{DC} = \int_l \frac{dl}{\sigma A} \xrightarrow{\text{if } A \text{ is independent from } l} \frac{1}{\sigma A} \int_l dl = \frac{l}{\sigma A} \qquad (\Omega). \tag{4.12}$$

### Spline Modeling

As seen in the previous discussion, to get $L$ or $C$ we need to approximate the wirebond with straight segments. Even if we use as many segments as we want to improve the approximation, we still need a reference image of the wirebond to be able to perform the segmentation in the first place. Otherwise, we just make assumptions on how the wirebond would look like. Most times, it is not even possible to some people to get wirebond samples, especially if one does not have a bonder machine or bonded sample chips in her/his disposal. Therefore, it is almost impossible to know exactly how the wirebonds would look like[4]. In [18], [20] it is suggested to use a circle arc to model the wirebond loop (see Figure 4.13). The inductance and capacitance of this model are given by

$$L = 10 \int_0^{s/2} \log\left(p(x)\right)\, dx \qquad \text{(nH)}, \tag{4.13}$$

$$C' = \frac{1.4337}{\log\left(p(x)\right)} \qquad \text{(pF/in)}, \tag{4.14}$$

$$p(x) = \frac{2}{r}\left(\sqrt{\left(\frac{s\csc\beta}{2}\right) - x^2} + \left(b - \frac{s}{2}\cot\beta\right)\right), \tag{4.15}$$

where $r$ is the wirebond radius, $s$ is the separation distance between the substrates, $b$ is the thickness of the substrate, and $\beta$ is the tilt angle of the wirebond (see Figure 4.13).

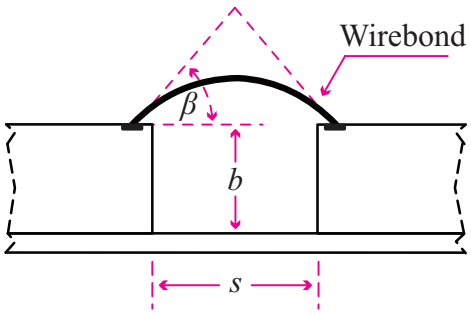


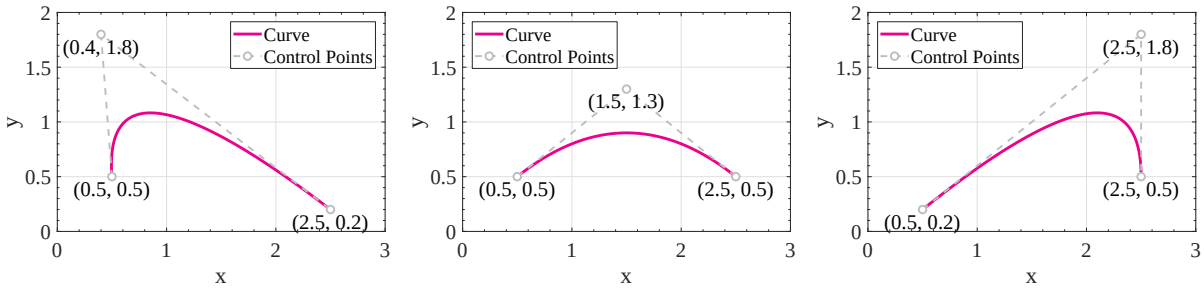

FIGURE 4.13: Curved wirebond modeled as a circle arc.

The disadvantage of above model is the limitation to circle arc shaped wirebonds, which is not always possible to achieve depending on the mechanics of the bonder machine. Therefore, in this thesis I suggest the use of parametric spline curve to describe the wirebond loop. Specifically, a popular spline curve used in various vector graphic applications is the Bézier curve (also commonly written as Bezier). More specifically, we are interested in the quadratic form of the Bezier curve, which is parametrically defined in 2D by

$$\begin{aligned} x(t) &= (1-t)^2 x_0 + 2(1-t)t x_1 + t^2 x_2 \\ y(t) &= (1-t)^2 y_0 + 2(1-t)t y_1 + t^2 y_2 \end{aligned} \qquad t \in [0,1] \tag{4.16}$$

[4]To be clear, JEDEC standard No. 59 [14] provides already a standardized method to approximate the expected wirebond shape, but this method is very limited and requires playing with many variables.

where $(x_0, y_0)$ and $(x_2, y_2)$ are the endpoints, and $(x_1, y_1)$ is the control point of the curve[5]. Figure 4.14 shows the versatility of a quadratic Bezier curve to model various shapes of wirebonds.




(A) (B) (C)

FIGURE 4.14: Illustration of quadratic Bezier curve.

The total length of a quadratic Bezier curve is given as below (the detailed derivation can be found in Appendix A)

$$\begin{aligned} l_B =& \frac{(2A+B)\sqrt{A+B+C} - B\sqrt{C}}{4A} + \cdots \\ & \cdots \frac{4AC - B^2}{8A\sqrt{A}} \left[ \sinh^{-1}\left( \frac{2A+B}{\sqrt{4AC-B^2}} \right) - \sinh^{-1}\left( \frac{B}{\sqrt{4AC-B^2}} \right) \right] \\ & \text{where—} \\ & A = 4(a_x^2 + a_y^2); \quad B = 4(a_x b_x + a_y b_y); \quad C = b_x^2 + b_y^2 \\ & a_x = x_0 - 2x_1 + x_2; \quad a_y = y_0 - 2y_1 + y_2 \\ & b_x = 2(x_1 - x_0); \qquad b_y = 2(y_1 - y_0). \end{aligned} \tag{4.17}$$

We can find an approximation for Eq. (4.17) through discretization, which can be written as

$$l_b \approx \sum_i \Delta l_{B_i} = \sum_i \sqrt{(x(t_{i+1}) - x(t_i))^2 + (y(t_{i+1}) - y(t_i))^2}. \tag{4.18}$$

The calculation of the self-inductance of a Bezier wirebond is obtained via the Neumann integral in Eq. (4.9). If there is a ground plane underneath the wire, the self-inductance will be affected. To account for ground effects in the computation of inductance, we combine between the imaging method and Neumann integral (see Example 4.2.2). The capacitance and DC resistance are determined via Eqs. (4.11) and (4.12), respectively.

Now, if we consider cases where having a physical wirebond sample or taking a side view photo is not possible, it becomes difficult to estimate the wirebond shape. For such cases we can estimate the wirebond shape via a Bezier model. We know from Eq. (4.16) that we need 6 constants to describe the quadratic Bezier curve in 2D, 4 of them for the endpoints coordinates, and 2 for the control point coordinate. If we know the location of the bond pads (i.e., substrate thickness and pad-to-pad spacing), the endpoints $(x_0, y_0)$ and $(x_2, y_2)$ of the Bezier curve are also known. Therefore, only the

[5]To be honest, all points are considered control points, I just distinguished endpoints here because their location is typically known and fixed.

control point $(x_1, y_1)$ is unknown. If we further assume that the wirebond is symmetric[6] (e.g., Figure 4.14b), then $x_1$ equals the half of the distance between the pads, i.e., $x_1 = (x_2 - x_0)/2$. Thus, we are only left with $y_1$ to determine. Now, if we assume that we know the final length of the wirebond, we can solve for $y_1$ from Eq. (4.17).

The question now becomes: how to estimate the length of the wirebond? This is simple, by considering the mechanics of wire bonding and how wire bonding is actually performed. In Chapter 2, I mentioned that the loop shape of a wirebond depends on the movement of the wedge tool (or capillary for ball bonding). Therefore, the length of the wirebond also depends on movement of the wedge tool. If we consider the simple bonding scenario in Figure 4.15, we recognize that the wirebond length must equal at most[7] the square root sum of the vertical pull and the horizontal drag

$$l_b = \sqrt{(\text{vertical pull})^2 + (\text{horizontal drag})^2}. \tag{4.19}$$

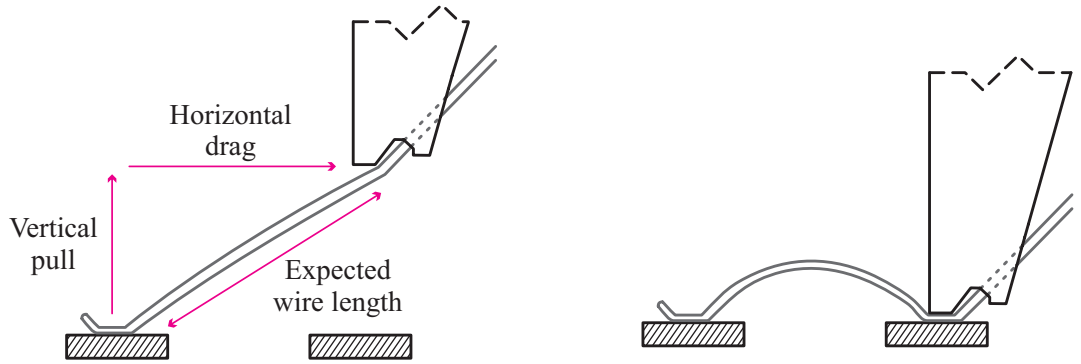



FIGURE 4.15: Simple wedge wire bonding steps.

As a result, we can get a good approximation of the wirebond length, thus allowing us to solve for $y1$.

To conclude the discussion on curved wirebonds, Example 4.2.1 presents a comparison between curved wirebond based on Bezier model, in both using EM simulation and analytical expressions.

**Example 4.2.2** Curved Wirebond above Ground Plane

We consider a curved Au wirebond with a diameter of 25 $\mu$m. The wirebond is modeled after 2D quadratic Bezier curve with the following parameters:

$$\begin{aligned} x_0 &= 0; \quad x_1 = 250; \quad x_2 = 500 \\ z_0 &= 200; \quad z_1 = 450; \quad z_2 = 200, \end{aligned} \qquad (\mu\text{m})$$

[6]Symmetry is not obligatory. For example, chip-to-substrate bonding—in such cases, it is better to choose $x1$ to be closer to the first bond.

[7]I say 'at most' because no extra wire will be pulled from the tool after reaching horizontal end, but depending on the bonder machine and the used tool, some wire might retract back when lowering the tool down for bonding. Thus, slightly reducing the final length.

The length of the wirebond is calculated via Eq. (4.18), which results in $l = 573.9\,\mu$m. Now, because the wirebond is symmetric, both capacitors in the model of Figure 4.8 are identical, i.e., $C_L = C_R = C$. Their values are calculated via Eq. (4.11)

$$C = \int_0^{l/2} \frac{2\pi\epsilon_0}{\cosh^{-1}\left(\frac{h}{r}\right)} dl = 0.0042\,\text{pF}.$$

Due to the ground plane, which carries the return path current on the opposite direction, the total inductance of the wirebond can be determined using the imaging method as depicted in Figure 4.16.

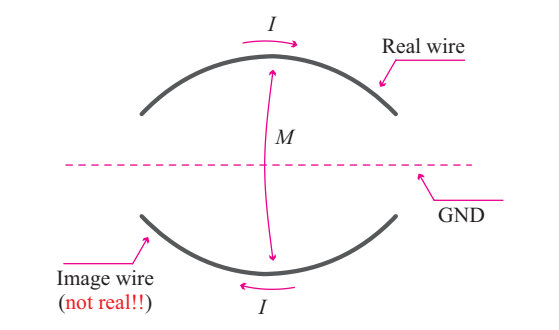



FIGURE 4.16: Image method to estimate effective loop inductance.

$M$ is the mutual inductance of the wirebond with its image. Both $L$ and $M$ of the wirebond can be determined via Neumann integral

$$L = \frac{\mu_0}{4\pi} \int_{l'} \int_{l} \frac{d\mathbf{l}' \cdot d\mathbf{l}}{R} = 374\,\text{pH}$$
$$M = \frac{\mu_0}{4\pi} \int_{l_2} \int_{l_1} \frac{d\mathbf{l}_2 \cdot d\mathbf{l}_1}{R} = 40.8\,\text{pH}.$$

Therefore, the total effective inductance of the wire is given as

$$L_W = L - M = 334.2\,\text{pH}$$

In generally, we would also need to include the self-inductance of the ground plane. However, the assumption here is that the ground's inductance is negligible compared to the wirebond. This is also considered in the simulated structure by making the ground plane large in area. The DC resistance of the wire is calculated via Eq. (4.12), which gives

$$R_{DC} = 28.45\,\text{m}\Omega$$

Figure 4.17 depicts both the equivalent circuit model, which uses the obtained values from the analytical equations, and the 3D simulated structure.

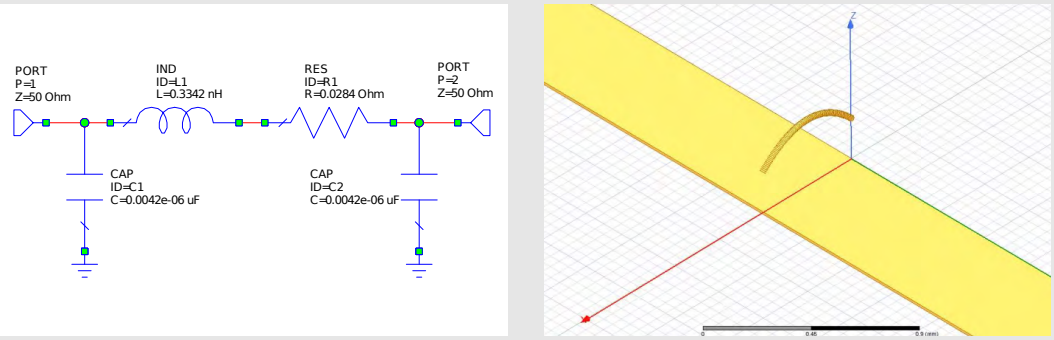



FIGURE 4.17: Left: Circuit simulation based on analytical results. Right: Simulated structure.

The reflection (S11) and transmission (S21) coefficients of the equivalent circuit and the simulated structure are depicted in Figure 4.18 (50 Ω reference impedance). Similar to previous example, we also observe here an excellent agreement between the analytical model and simulated results.

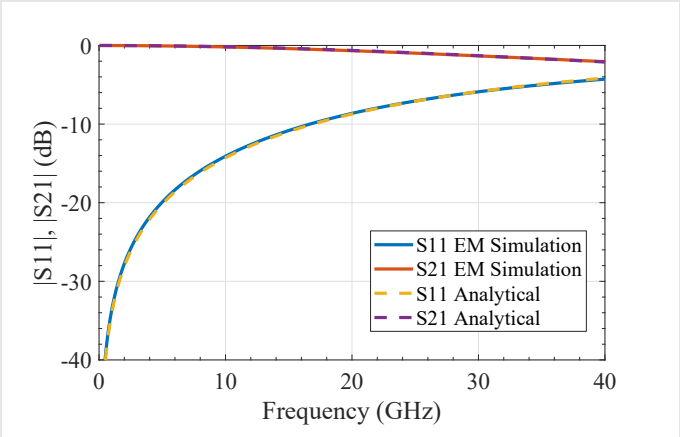



FIGURE 4.18: Comparsion between analytical and simulation results.

### 4.2.3 Coplanar Wirebonds

It is known by now that loop inductance is the inductance of the wirebond and the inductance of the return path (including mutual inductance coupling). In the cases of a ground plane, we notice that the mutual inductance has an effect of reducing the loop inductance. In generally, the smaller the loop and closer the signal wire to ground, the lesser the loop inductance becomes. A solution to create such an environment is by placing the ground paths next to the signal wire, hence both ground and signal are coplanar. Figure 4.19 depicts an 3D illustration of GSG (Ground-Signal-Ground) wirebonds.

In general, it is assumed that there is no ground plane underneath the wires, but if there is a ground plane this needs to be included in the model. Now, given there is no ground plane beneath the wires, GSG wirebonds will have a uniform coplanar structure along their path. Under those circumstances, the wirebonds can be thought as coplanar waveguide (CPW). Therefore, the model used here is a lossless transmission

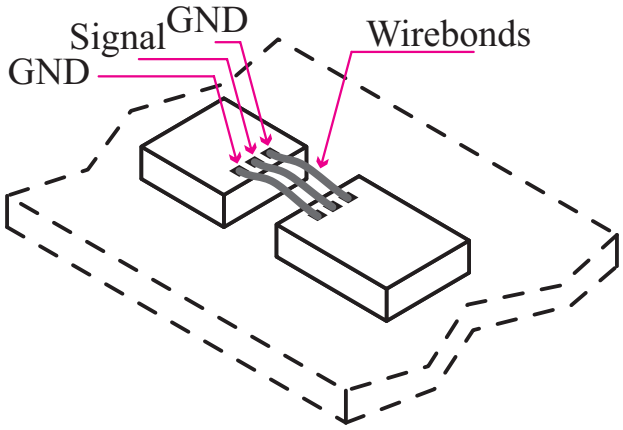



FIGURE 4.19: Illustration of GSG wirebonds.

line, where its characteristic impedance is approximated in [21] to be

$$Z_0 \approx \frac{140}{\sqrt{\epsilon_{eff}}} \frac{s/d - 1}{1 + 0.6(s/d - 1)}; \qquad \text{for... } 2 < s/d < 10 \tag{4.20}$$

where $s$ is the pitch distance between the wires, and $d$ is the wire diameter. Unfortunately, the effective dielectric constant $\epsilon_{eff}$ does not have a general formula (unless it is air, then $\epsilon_{eff} = 1$), but in [21] a model fit is developed if the wires are above a GaAs substrate, which has a dielectric constant of 13.1,

$$\begin{aligned} \log(\epsilon_{eff} - 1) &= \alpha_0 - \alpha_1(a/d) + \alpha_2 e^{-5(a/d)} \\ \alpha_0 &= 1.1 - \frac{2.2}{(s/d - 1)^{1/2}} \\ \alpha_1 &= 0.3 + \frac{0.7}{(s/d - 1)^{1/3}} \\ \alpha_2 &= 0.7 + \frac{1.4}{(s/d - 1)^{1/2}} \end{aligned} \tag{4.21}$$

Now, let us consider a scenario of interconnecting two substrates with GSG wirebonds, where $d = 25\,\mu$m, $s = 100\,\mu$m, and $\epsilon_{eff} = 1$, i.e., air. Entering these values into Eq. (4.20), we obtain $Z_0 = 150\,\Omega$. This high impedance value is to be expected as wirebonds are more inductive than capacitive. Generally, we can still work with this impedance value if we design the ports on the chips to be $150\,\Omega$, but if the chips need to have $50\,\Omega$ port impedance, then the objective now becomes to reduce the characteristic impedance of the wirebonds. From Eq. (4.20), we recognize that there are three parameters that control the impedance: pitch distance $(s)$, wire diameter $(d)$, and effective dielectric constant $(\epsilon_{eff})$. Figure 4.20 shows a plot of Eq. (4.20) in three cases, where in each time one parameter is varied while fixing the others.

From Figure 4.20, we learn that adjusting the diameter of the wirebond does not have a major impact on $Z_0$, and even if we further increase the diameter, we only hit a physical constraint due to pad size. On the other hand, both the pitch distance and

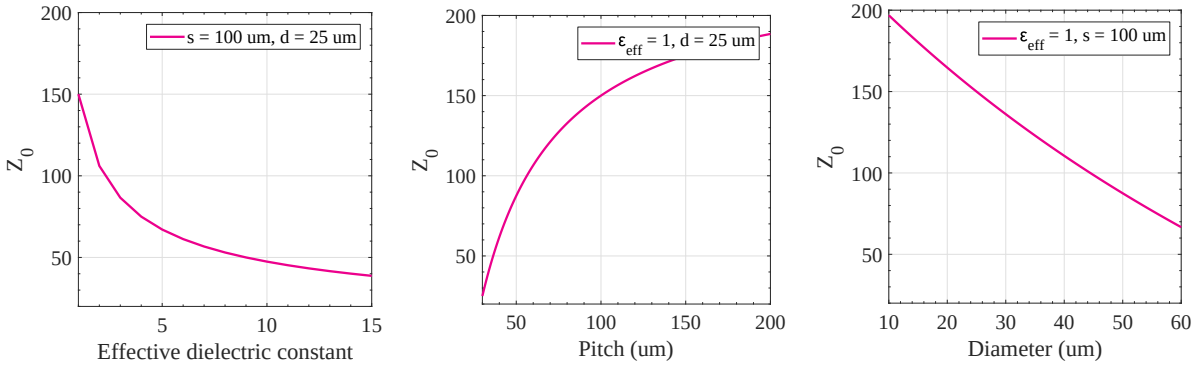



FIGURE 4.20: Characteristic impedance of GSG wirebonds.
(A) Varying $\epsilon_{eff}$, (B) Varying pitch distance, (C) Varying wire diameter.

effective dielectric constant have a recognizable impact. We can show a practical case where we can reduce the characteristic impedance of the wires to a reasonable value. For example, if we make $s = 41\,\mu$m and $\epsilon_{eff} = 3.2$, while using a wire with a diameter $d = 20\,\mu$m, we obtain $Z_0 \approx 50.4\,\Omega$. These values are not hypothetical, but actual achievable with current technologies. For example, the company Micro Point Pro LTD, at time of writing, is providing *Ultra Fine Pitch* wedge tools which are able to achieve minimum pitch of 35 $\mu$m while using wires with diameter down to 20 $\mu$m [22]. To achieve $\epsilon_{eff} = 3.2$, we only need to apply an epoxy around the wirebonds which has a dielectric constant of 3.2. For example, the company DELO has various epoxies solutions for chip packaging applications.

Alternative to GSG wirebonds, there are GSG ribbon bonds. The process is similar to what we discussed above, but with ribbon bonds we can take advantage of skin effect to carry more current, thus offering less inductance (ribbons have larger surface area). Generally, ribbon bonding will almost always outperform normal wire bonding in RF applications. For interested readers, you can find analytical equations to compute the characteristic impedance of a rectangular CPW structures in [23], which are actually developed for PCBs traces, but they also hold valid for ribbon bonds because of the similar rectangular geometry.

**Example 4.2.3** Comparison between GSG Wirebonds and GSG Ribbon Bonds

This example shows the effects of applying epoxy to GSG wirebonds and ribbon bonds. The assumption made here is that $\epsilon_{epoxy} = 3.2$. Through EM simulation, we investigate 4 cases:

- GSG wirebonds with and without epoxy.
- GSG ribbon bonds with and without epoxy.

The simulated structures are depicted in Figure 4.21. The epoxy was implemented in the 3D structure as a solid object, covering the wires while exposing their top and bottom surfaces.

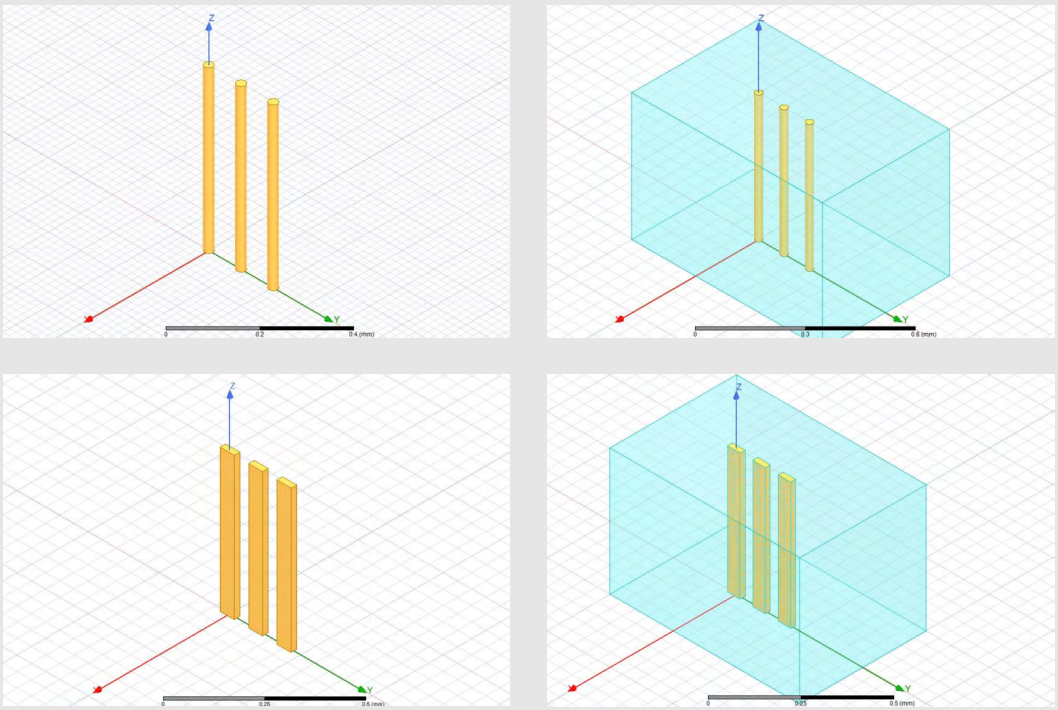


FIGURE 4.21: Simulated structures.

The martial of the wires is Au, and they have a length of 0.5 mm. The wirebonds have a diameter of 25 $\mu$m, and the ribbon bonds have dimensions of $50 \times 20$ $\mu$m. The reflection (S11) and transmission (S21) coefficients of all four structures are depicted in Figure 4.22. As can be seen, the ribbon bonds are much better than wirebonds, even without epoxy. However, by using an epoxy we are able to reduce the reflection in the wirebonds from $-7.9$ dB to $-10.3$ dB. Overall, the ribbon bonds show even better results, an improvement from $-11.7$ dB to $-18.7$ dB in the reflection coefficient.

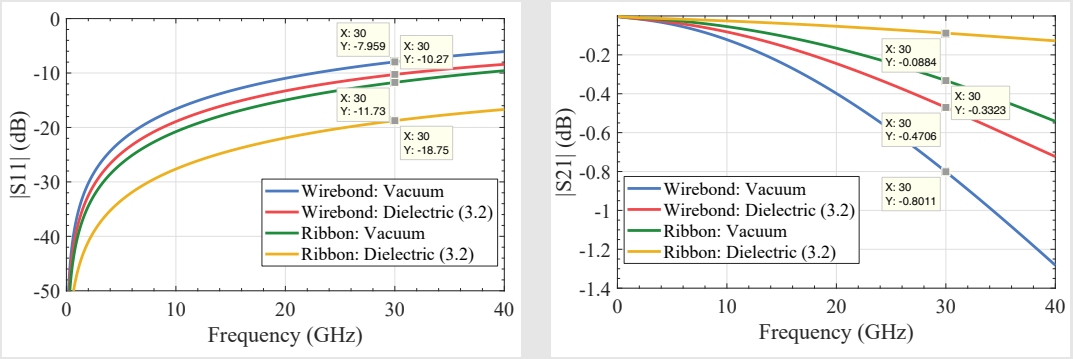



FIGURE 4.22: $|S_{11}|$ and $|S_{21}|$ of the simulated strcutures.

From the simulation results we can extract the equivalent inductance and capacitance of the structures. Furthermore, assuming the dielectric (epoxy) is near lossless, we can also compute the characteristic impedance of the lines as follows:

$$Z_0 = \sqrt{\frac{L}{C}} \qquad (\Omega).$$

From the values in the table below, we learn that the dielectric martial (epoxy) did indeed cause the increase of the capacitance, thus reduced the value of $Z_0$. We can also observe the significant differences between GSG wirebonds and GSG ribbon bonds.

TABLE 4.1: Equivalent circuit parameters of the simulated structures.

| | Wirebonds $\epsilon_{eff} = 1$ | Wirebonds $\epsilon_{eff} = 3.2$ | Ribbons $\epsilon_{eff} = 1$ | Ribbons $\epsilon_{eff} = 3.2$ |
|---|---|---|---|---|
| Inductance (nH) | 0.26476 | 0.26476 | 0.18542 | 0.18541 |
| Capacitance (pF) | 0.01096 | 0.03330 | 0.01586 | 0.04791 |
| Characteristic Impedance ($\Omega$) | 155.43 | 89.17 | 108.13 | 62.21 |

The lumped parameters of GSG wirebonds can also be calculated analytically. The inductance of a GSG structure is determined by considering the self and mutual inductance of each wire and computing the total inductance using Kirchhoff's current and voltage laws. Figure 4.23 illustrates the schematic of inductance wired in a GSG configuration.

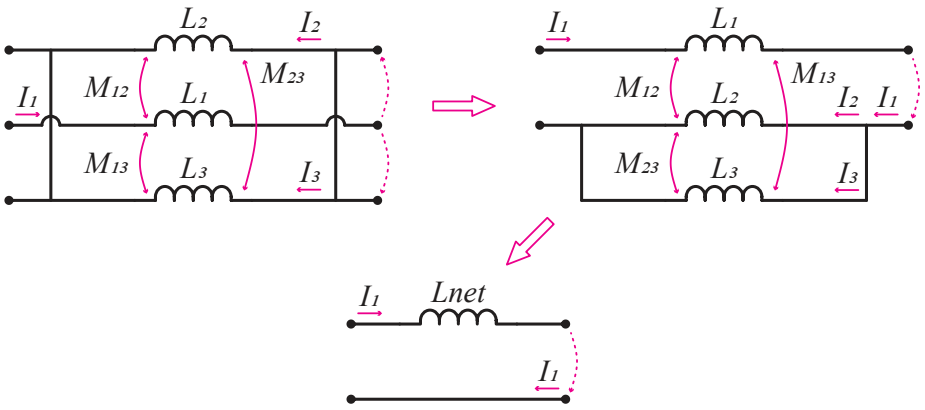



FIGURE 4.23: Equivalent circuit of GSG connected inductors.

From Figure 4.23, we can write down the Kirchhoff's voltage and current laws [24]

$$L_{net}\frac{di_1}{dt} = L_{s1}\frac{di_1}{dt} - M_{12}\frac{di_2}{dt} - M_{13}\frac{di_3}{dt} + L_{s2}\frac{di_2}{dt} - M_{21}\frac{di_1}{dt} - M_{23}\frac{di_3}{dt} \tag{4.22}$$

$$0 = L_{s2}\frac{di_2}{dt} + M_{23}\frac{di_3}{dt} - M_{21}\frac{di_1}{dt} - L_{s3}\frac{di_3}{dt} - M_{32}\frac{di_2}{dt} - M_{31}\frac{di_1}{dt} \tag{4.23}$$

$$i_1 = i_2 + i_3 \tag{4.24}$$

Because of symmetry between the ground wires, $L_2 = L_3$. By the same token, the reciprocity property of mutual inductance results in $M_{23} = M_{32}$, $M_{13} = M_{31}$ and $M_{12} = M_{21}$. Therefore, after the algebraic manipulation of Eqs. (4.22) and (4.24), the

net inductance of a GSG structure is given as [24]

$$L_{net} = L_1 - M_{12} + \frac{L_2 + M_{23} - M_{12} - M_{13}}{2} + \frac{(M_{12} - M_{13})(L_2 - M_{12} - M_{23} + M_{13})}{2(L_2 - M_{23})} \tag{4.25}$$

The calculation of the mutual and self-inductance depends on the geometry of the wires and can be determined via Eqs. (4.8) and (4.9), given they have a circular cross-section. Figure 4.24 shows a comparison between the inductance of GSG wirebonds and the traditional single wirebond backed by a ground plane. We clearly see that a 100 $\mu$m-pitch GSG wirebonds give similar results to wirebond 100 $\mu$m above a ground plane. However, by increasing the wirebond height from ground, the loop inductance increases as well. This shows that GSG wirebonds give optimal results, even if the chips are thick, hence the wires are far away from any ground planes. In general, chips tend to have thickness $>$ 150 $\mu$m, therefore, results shown in Figure 4.24 for wirebond 100 $\mu$m above ground is considered optimistic. Additionally, wirebonds will have loops, which further increase the wire height from ground. A further observation is the agreement between the analytical result of the inductance value in Figure 4.24 at $l = 0.5$ mm with the simulation in Example 4.2.3 for the same structure in vacuum. Therefore, the inductance of GSG wirebonds can be accurately calculated using Eq. (4.25) in combination with Neumann integrals in Eqs. (4.8) and (4.9).

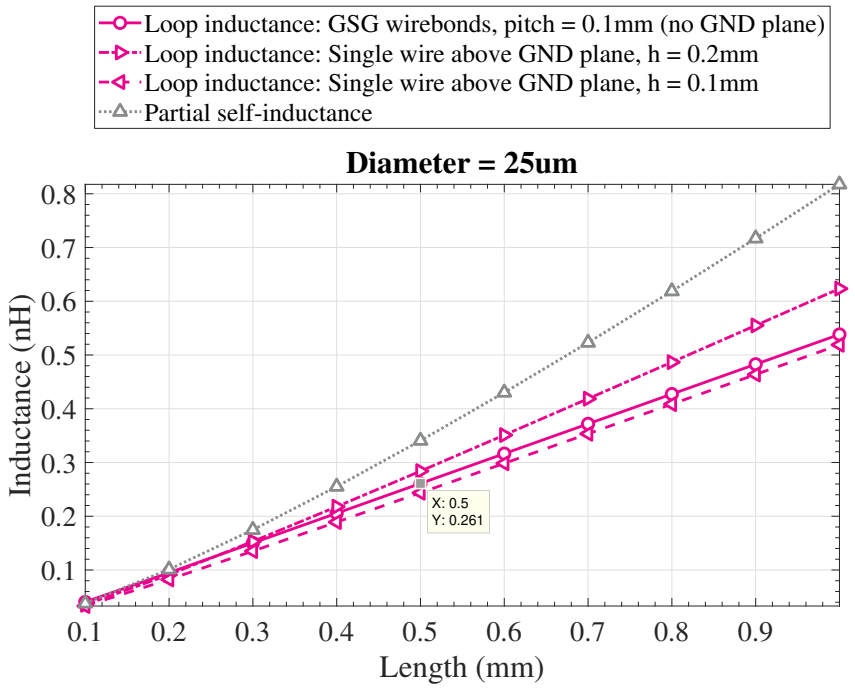



FIGURE 4.24: Inductance of 25 $\mu$m wirebond as function of wire length.

The capacitance of GSG wirebonds is given by the addition of the two capacitance of the wires in parallel, which results in double the capacitance of one wire

$$C = 2\int_l \frac{\pi\epsilon}{\cosh^{-1}\left(\frac{s}{2r}\right)} dl \qquad \text{(F)}. \tag{4.26}$$

The DC resistance is determined by adding the resistance of ground wires in parallel and in series with the signal wire. This results in a factor of 3/2 if all wires are

identical

$$R_{DC} = \frac{3}{2} \int_l \frac{dl}{\sigma A} \qquad (\Omega). \tag{4.27}$$

# Chapter 5

# De-embedding and Model Extraction

In the previous chapter, the focus was mainly on modeling wirebonds through analytical expressions and EM simulations. In this chapter the focus shifts to measuring wirebonds and how to extract an equivalent circuit model from 2-port measurements.

## 5.1 2-Port Networks

The first topic we need to discuss is how RF circuits are measured and how they are described. The 2-port (or generally n-port) networks are an abstract description of arbitrary 2-port circuits. Any circuit can be thought as a black box that has an input and output (see Figure 5.1). The 2-port description of a circuit summaries the relation between input and output in a matrix notation.

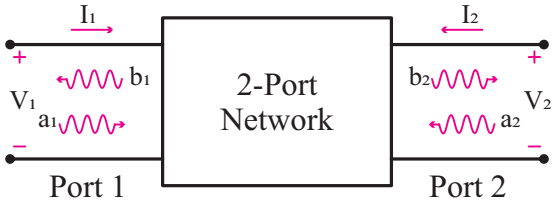



FIGURE 5.1: Illustration of a 2-port network.

There several quantities in a circuit to measure. Depending on what is measured, we can develop several matrices to describe the circuit's ports. To name few:

- The Z-Parameters and the Y-Parameters: They describe the relation between the current and voltage. Their matrix notation is given in Eq. (5.1). Notice that the **Z** and the **Y** matrices share an inverse relationship.

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}; \quad \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{5.1}$$

- The ABCD-Parameters: They describe the voltage and current input/output relation. Because of this property, cascaded circuits can be described as the multiplication of the individual **ABCD** matrices of each circuit.

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \tag{5.2}$$

- The S-Parameters (Scattering Parameters): They are a generalized description of any circuit. One of the problems of previous mentioned parameters is that they do not take wave effects at high frequencies into account, e.g., a short circuit at high frequencies might not behave as a 'short circuit'. The S-parameters are described via incident and reflected waves. The waves can be expressed in terms of voltage and current (given a reference impedance $Z_0$) or in terms of power waves ($a_i$ and $b_i$).

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{5.3}$$

- The T-Parameters (Transmission Scattering Parameters): These parameters are similar to the ABCD-parameters, in the sense they can be cascaded to describe the overall circuit. The difference between the ABCD-parameters and T-parameters is that the T-parameters—similar to S-parameters—are described by waves, and hence do not require a reference impedance when converted from S-parameters (see Table 5.2).

$$\begin{bmatrix} b_1 \\ a_1 \end{bmatrix} = \begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} \begin{bmatrix} b_2 \\ a_2 \end{bmatrix} \tag{5.4}$$

### 5.1.1 ABCD-Parameters of Common Circuit Elements

This section presents the ABCD matrices of some fundamental circuit elements, which can be cascaded in any form to give the ABCD matrix of more complex circuits. This is relevant for later discussion on wirebond model extraction. Table 5.1 lists the ABCD matrices of 4 fundamental circuit elements.

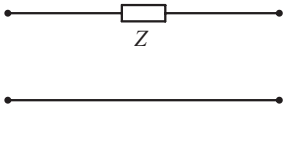
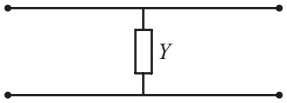
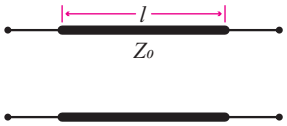
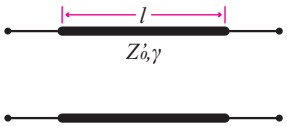
### 5.1.2 Properties of S-Parameters

S-Parameters are ubiquitous and are commonly measured by Vector Network Analyzers (VNAs). Therefore, it is important to know the properties of these parameters and their relation to the Device Under Test (DUT).

#### Reciprocity

Reciprocity refer to reciprocal circuits in the sense they can be connected either side. Generally, passive components are reciprocal (excluding magnetic coupled element). In the S-matrix of a 2-port network, this is given as $S_{21} = S_{12}$. More general, the transpose of an S-matrix of an n-port network equals the original matrix, i.e., reciprocal

TABLE 5.1: ABCD parameters of fundamental circuit elements [25].
($Z, Y, \gamma, Z_0' \in \mathbb{C}$, while $l, \beta, Z_0 \in \mathbb{R}$)

| Circuit element | Circuit schematic | ABCD matrix |
|---|---|---|
| Series Impedance |   | $\begin{bmatrix} 1 & Z \\ 0 & 1 \end{bmatrix}$ |
| Shunt Admittance |   | $\begin{bmatrix} 1 & 0 \\ Y & 1 \end{bmatrix}$ |
| Lossless Transmission Line |   | $\begin{bmatrix} \cos(\beta l) & jZ_0 \sin(\beta l) \\ j\frac{1}{Z_0} \sin(\beta l) & \cos(\beta l) \end{bmatrix}$ |
| Lossy Transmission Line |   | $\begin{bmatrix} \cosh(\gamma l) & Z_0' \sinh(\gamma l) \\ \frac{1}{Z_0'} \sinh(\gamma l) & \cosh(\gamma l) \end{bmatrix}$ |

networks have symmetrical S-matrices ($S = S^T$).

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \xrightarrow{\text{Reciprocity}} \begin{bmatrix} S_{11} & S_{12} \\ S_{12} & S_{22} \end{bmatrix} \tag{5.5}$$

**Lossless**

Circuits are called lossless when no energy 'leaks' from the circuit, e.g., in form of heat, radiation, or low resistant dielectric. The S-matrix of a lossless circuit is an unitary matrix, i.e.,

$$\mathbf{S}\mathbf{S}^H = \mathbf{I} \tag{5.6}$$

where $\mathbf{I}$ is the identity matrix, and $(.)^H$ is the hermitian transpose (conjugate transpose). This result implies two things:

1. The columns of $\mathbf{S}$ are orthogonal.
2. Each column has a unit magnitude, i.e., energy must either get transmitted or reflected.

In terms of 2-port network, this is given as

$$|S_{11}|^2 + |S_{21}|^2 = 1; \qquad |S_{22}|^2 + |S_{12}|^2 = 1. \tag{5.7}$$

**Symmetry**

A circuit is called symmetric if it is reciprocal and its ports are symmetric. For every two symmetric ports in a reciprocal circuit the following relation holds

$$S_{ii} = S_{jj}, \qquad S_{ij} = S_{ji} \tag{5.8}$$

where $i$ and $j$ are the symmetric ports.

### 5.1.3 Conversion Between Parameters

Because we almost always measure S-parameters with VNAs, we should also know how to convert between parameters. For convenience, the conversion equations between the various parameters are listed in Table 5.2.

## 5.2 De-embedding Methods

When measuring 2-port parameters of a DUT, measurements at the calibrated planes might not be possible. Figure 5.2 depicts the general problem of de-embedding. The concept of de-embedding is to remove those unwanted effects from measurements to get the correct characterization of the DUT.

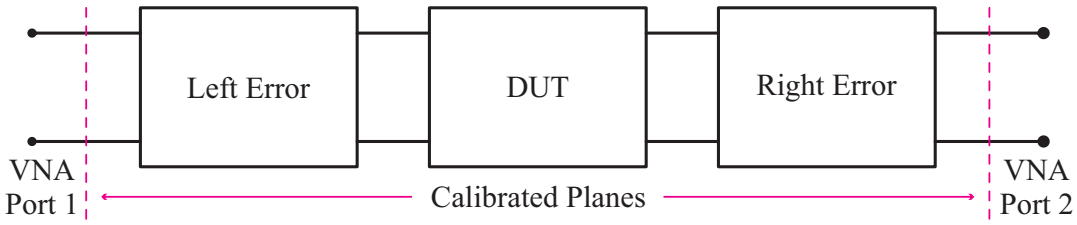



FIGURE 5.2: The de-embedding problem.

The objective is to estimate the error blocks and to remove their effects via matrix inverse multiplication. Mathematically, this is given using either T-parameters or ABCD-parameters, as they have the property of cascade multiplication.

$$\mathbf{T}_{\text{Meas}} = \mathbf{T}_{\text{L}}\mathbf{T}_{\text{DUT}}\mathbf{T}_{\text{R}} \tag{5.9}$$

$$\mathbf{T}_{\text{DUT}} = \mathbf{T}_{\text{L}}^{-1}\mathbf{T}_{\text{Meas}}\mathbf{T}_{\text{R}}^{-1}. \tag{5.10}$$

### 5.2.1 Direct De-embedding

The simplest and most straightforward way to remove the effects of fixture elements in measurements is to measure these structures directly and eliminate their effects by means of inverse operation. For example, we can consider a case where we are measuring a DUT that requires the use of an attenuator (e.g., high-gain amplifier). Now, because the attenuator is not ideal and will have an influence on the measurements, we want to exclude its effects by de-embedding it from the measurements. To do so, we measure the attenuator directly at the calibrated planes, and with the T-parameters

TABLE 5.2: Parameters conversion [26], [27].

| | **S** | **T** | **Z** | **Y** | **ABCD** |
|---|---|---|---|---|---|
| $S_{11}$ | $S_{11}$ | $\frac{T_{21}}{T_{11}}$ | $\frac{(Z_{11}-Z_0)(Z_{22}+Z_0)-Z_{12}Z_{21}}{(Z_{11}+Z_0)(Z_{22}+Z_0)-Z_{12}Z_{21}}$ | $\frac{(Y_0-Y_{11})(Y_0+Y_{22})+Y_{12}Y_{21}}{(Y_0+Y_{11})(Y_0+Y_{22})-Y_{12}Y_{21}}$ | $\frac{A+B/Z_0-CZ_0-D}{A+B/Z_0+CZ_0+D}$ |
| $S_{12}$ | $S_{12}$ | $\frac{T_{11}T_{22}-T_{12}T_{21}}{T_{11}}$ | $\frac{2Z_{12}Z_0}{(Z_{11}+Z_0)(Z_{22}+Z_0)-Z_{12}Z_{21}}$ | $\frac{-2Y_{12}Y_0}{(Y_0+Y_{11})(Y_0+Y_{22})-Y_{12}Y_{21}}$ | $\frac{2(AD-BC)}{A+B/Z_0+CZ_0+D}$ |
| $S_{21}$ | $S_{21}$ | $\frac{1}{T_{11}}$ | $\frac{2Z_{21}Z_0}{(Z_{11}+Z_0)(Z_{22}+Z_0)-Z_{12}Z_{21}}$ | $\frac{-2Y_{21}Y_0}{(Y_0+Y_{11})(Y_0+Y_{22})-Y_{12}Y_{21}}$ | $\frac{2}{A+B/Z_0+CZ_0+D}$ |
| $S_{22}$ | $S_{22}$ | $\frac{-T_{12}}{T_{11}}$ | $\frac{(Z_{11}+Z_0)(Z_{22}-Z_0)-Z_{12}Z_{21}}{(Z_{11}+Z_0)(Z_{22}+Z_0)-Z_{12}Z_{21}}$ | $\frac{(Y_0+Y_{11})(Y_0-Y_{22})+Y_{12}Y_{21}}{(Y_0+Y_{11})(Y_0+Y_{22})-Y_{12}Y_{21}}$ | $\frac{-A+B/Z_0-CZ_0+D}{A+B/Z_0+CZ_0+D}$ |
| $T_{11}$ | $\frac{1}{S_{21}}$ | $T_{11}$ | $\frac{(Z_{11}+Z_0)(Z_{22}+Z_0)-Z_{12}Z_{21}}{2Z_{21}Z_0}$ | $\frac{-(Y_0+Y_{11})(Y_0+Y_{22})+Y_{12}Y_{21}}{2Y_{21}Y_0}$ | $\frac{A+B/Z_0+CZ_0+D}{2}$ |
| $T_{12}$ | $\frac{-S_{22}}{S_{21}}$ | $T_{12}$ | $\frac{(Z_{11}+Z_0)(Z_0-Z_{22})+Z_{12}Z_{21}}{2Z_{21}Z_0}$ | $\frac{(Y_0+Y_{11})(Y_0-Y_{22})+Y_{12}Y_{21}}{2Y_{21}Y_0}$ | $\frac{A-B/Z_0+CZ_0-D}{2}$ |
| $T_{21}$ | $\frac{S_{11}}{S_{21}}$ | $T_{21}$ | $\frac{(Z_{11}-Z_0)(Z_0+Z_{22})-Z_{12}Z_{21}}{2Z_{21}Z_0}$ | $\frac{(Y_{11}-Y_0)(Y_0+Y_{22})-Y_{12}Y_{21}}{2Y_{21}Y_0}$ | $\frac{A+B/Z_0-CZ_0-D}{2}$ |
| $T_{22}$ | $\frac{S_{12}S_{21}-S_{11}S_{22}}{S_{21}}$ | $T_{22}$ | $\frac{(Z_0-Z_{11})(Z_{22}-Z_0)+Z_{12}Z_{21}}{2Z_{21}Z_0}$ | $\frac{(Y_0-Y_{11})(Y_0-Y_{22})-Y_{12}Y_{21}}{2Y_{21}Y_0}$ | $\frac{A-B/Z_0-CZ_0+D}{2}$ |
| $Z_{11}$ | $Z_0\frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}$ | $Z_0\frac{T_{11}+T_{12}+T_{21}+T_{22}}{T_{11}+T_{12}-T_{21}-T_{22}}$ | $Z_{11}$ | $\frac{Y_{22}}{Y_{11}Y_{22}-Y_{12}Y_{21}}$ | $\frac{A}{C}$ |
| $Z_{12}$ | $Z_0\frac{2S_{12}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}$ | $Z_0\frac{2(T_{11}T_{22}-T_{12}T_{21})}{T_{11}+T_{12}-T_{21}-T_{22}}$ | $Z_{12}$ | $\frac{-Y_{12}}{Y_{11}Y_{22}-Y_{12}Y_{21}}$ | $\frac{AD-BC}{C}$ |
| $Z_{21}$ | $Z_0\frac{2S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}$ | $Z_0\frac{2}{T_{11}+T_{12}-T_{21}-T_{22}}$ | $Z_{21}$ | $\frac{-Y_{21}}{Y_{11}Y_{22}-Y_{12}Y_{21}}$ | $\frac{1}{C}$ |
| $Z_{22}$ | $Z_0\frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}$ | $Z_0\frac{T_{11}-T_{12}-T_{21}+T_{22}}{T_{11}+T_{12}-T_{21}-T_{22}}$ | $Z_{22}$ | $\frac{Y_{11}}{Y_{11}Y_{22}-Y_{12}Y_{21}}$ | $\frac{D}{C}$ |
| $Y_{11}$ | $Y_0\frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}$ | $Y_0\frac{T_{11}-T_{21}-T_{12}+T_{22}}{T_{11}-T_{12}+T_{21}-T_{22}}$ | $\frac{Z_{22}}{Z_{11}Z_{22}-Z_{12}Z_{21}}$ | $Y_{11}$ | $\frac{D}{B}$ |
| $Y_{12}$ | $Y_0\frac{-2S_{12}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}$ | $Y_0\frac{-2(T_{11}T_{22}-T_{12}T_{21})}{T_{11}-T_{12}+T_{21}-T_{22}}$ | $\frac{-Z_{12}}{Z_{11}Z_{22}-Z_{12}Z_{21}}$ | $Y_{12}$ | $\frac{BC-AD}{B}$ |
| $Y_{21}$ | $Y_0\frac{-2S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}$ | $Y_0\frac{-2}{(T_{11}-T_{12}+T_{21}-T_{22})}$ | $\frac{-Z_{21}}{Z_{11}Z_{22}-Z_{12}Z_{21}}$ | $Y_{21}$ | $\frac{-1}{B}$ |
| $Y_{22}$ | $Y_0\frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}$ | $Y_0\frac{T_{11}+T_{21}+T_{12}+T_{22}}{T_{11}-T_{12}+T_{21}-T_{22}}$ | $\frac{Z_{11}}{Z_{11}Z_{22}-Z_{12}Z_{21}}$ | $Y_{22}$ | $\frac{A}{B}$ |
| $A$ | $\frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{2S_{21}}$ | $\frac{1}{2}(T_{11}+T_{12}+T_{21}+T_{22})$ | $\frac{Z_{11}}{Z_{21}}$ | $\frac{-Y_{22}}{Y_{21}}$ | $A$ |
| $B$ | $Z_0\frac{(1+S_{11})(1+S_{22})-S_{12}S_{21}}{2S_{21}}$ | $\frac{Z_0}{2}(T_{11}-T_{12}+T_{21}-T_{22})$ | $\frac{Z_{11}Z_{22}-Z_{12}Z_{21}}{Z_{21}}$ | $\frac{-1}{Y_{21}}$ | $B$ |
| $C$ | $\frac{(1-S_{11})(1-S_{22})-S_{12}S_{21}}{2S_{21}Z_0}$ | $\frac{1}{2Z_0}(T_{11}+T_{12}-T_{21}-T_{22})$ | $\frac{1}{Z_{21}}$ | $\frac{-(Y_{11}Y_{22}-Y_{12}Y_{21})}{Y_{21}}$ | $C$ |
| $D$ | $\frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{2S_{21}}$ | $\frac{1}{2}(T_{11}-T_{12}-T_{21}+T_{22})$ | $\frac{Z_{22}}{Z_{21}}$ | $\frac{-Y_{11}}{Y_{21}}$ | $D$ |

$Z_0$ is the reference (port) impedance. $Z_0 \in \mathbb{R}$; $Y_0 = 1/Z_0$

of both measurements and attenuator, we can use Eq. (5.10) to recover the correct measurements of the DUT.

### 5.2.2 Thru-Only De-embedding (TOD)

Chip pads tend to be small (e.g., $80 \times 80\,\mu$m), therefore, trying to measure them directly with wafer probes is often difficult. To this end, we need to develop a method to measure and estimate the characteristic of the pads so that their effects can be de-embedded when measuring the chip. The method of TOD requires a dummy structure of two pads connected together with an ideal short. Figure 5.3 depicts a general block diagram of the embedded DUT with left and right fixtures, and a thru structure of those fixtures (in the chip example, the fixtures represent the pads).

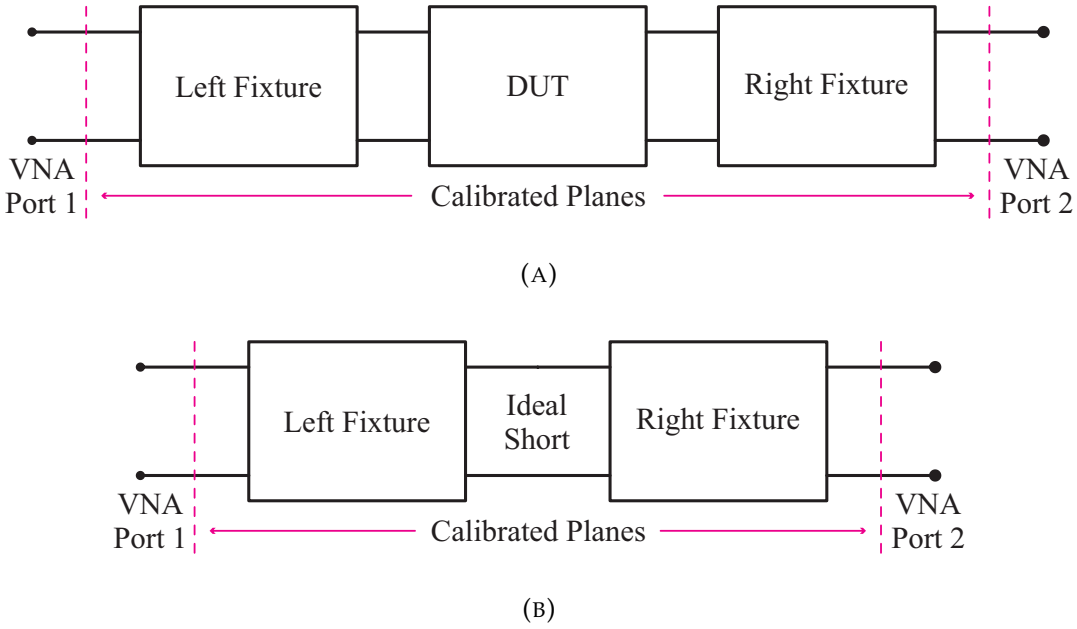



FIGURE 5.3: Illustration of TOD. (A) DUT with left and right fixtures; (B) left and right fixtures connected with an ideal short.

The T-parameters[1] of the embedded DUT and the thru structure are given by

$$\mathbf{T}_{\text{Meas}} = \mathbf{T}_{\text{L}}\mathbf{T}_{\text{DUT}}\mathbf{T}_{\text{R}} \tag{5.11}$$

$$\mathbf{T}_{\text{Thru}} = \mathbf{T}_{\text{L}}\mathbf{T}_{\text{R}}, \tag{5.12}$$

where $\mathbf{T}_{\text{DUT}}$ is the T-matrix of the DUT, while $\mathbf{T}_{\text{L}}$ and $\mathbf{T}_{\text{R}}$ are the left and right T-matrices of the fixtures, respectively. To explain how the de-embedding process works, we start by writing down the left and right fixtures' S-matrices (assuming symmetry)

$$\mathbf{S}_L = \mathbf{S}_R = \begin{bmatrix} S_{11} & S_{12} \\ S_{12} & S_{11} \end{bmatrix}. \tag{5.13}$$

[1]ABCD-parameters can also be used, but they require the use of a reference (port) impedance, in contrast to T-parameters, which are a direct conversion from the S-parameters.

Afterwards, the S-parameters are converted into T-parameters (see Table 5.2)

$$\mathbf{T}_L = \mathbf{T}_R = \frac{1}{S_{12}} \begin{bmatrix} -\Delta & S_{11} \\ -S_{11} & 1 \end{bmatrix}; \quad \Delta = S_{11}^2 - S_{12}^2 \tag{5.14}$$

Therefore, the T-matrix of the thru structure is given by

$$\mathbf{T}_{\text{Thru}} = \mathbf{T}_L \mathbf{T}_R = \frac{1}{S_{12}^2} \begin{bmatrix} \Delta^2 - S_{11} & (-\Delta + 1)S_{11} \\ (\Delta - 1)S_{11} & 1 - S_{11}^2 \end{bmatrix}, \tag{5.15}$$

or equivalently, in terms of S-parameters

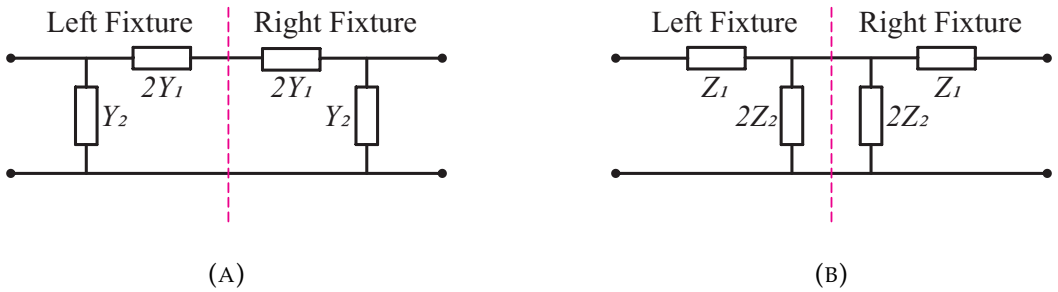
$$\mathbf{S}_{\text{Thru}} = \frac{1}{1 - S_{11}^2} \begin{bmatrix} (S_{12}^2 - S_{11}^2 + 1)S_{11} & S_{12}^2 \\ S_{12}^2 & (S_{12}^2 - S_{11}^2 + 1)S_{11} \end{bmatrix}. \tag{5.16}$$

From Eq. (5.16), both $S_{11}$ and $S_{12}$ can be solved given $\mathbf{S}_{\text{Thru}}$ measurements. This is of course would only be possible in the ideal case, where the $\mathbf{S}_{\text{Thru}}$ measurements are not error-prone. Assuming error-prone measurements, we can find an estimate for $S_{11}$ and $S_{12}$ in the optimization sense, where the optimization problem is given as

$$\begin{bmatrix} \hat{S}_{11} \\ \hat{S}_{12} \end{bmatrix} = \underset{S_{11}, S_{12}}{\text{argmin}} \left\| \mathbf{S}_{\text{Thru}} - \frac{1}{1 - S_{11}^2} \begin{bmatrix} S_{11}(S_{12}^2 - S_{11}^2 + 1) & S_{12}^2 \\ S_{12}^2 & S_{11}(S_{12}^2 - S_{11}^2 + 1) \end{bmatrix} \right\|_F^2, \tag{5.17}$$

where $\mathbf{S}_{\text{Thru}}$ is the measured thru structure, and $\|\cdot\|_F$ is the Frobenius norm.

An alternative approach to perform TOD is by defining a symmetric model (e.g., T or Π model) for the fixtures. Figure 5.4 shows the equivalent T and Π bisection models of the thru structure.




(A) (B)

FIGURE 5.4: Bisection of (A) Π and (B) T equivalent circuits.

The Y-parameters of the Π model is given by

$$\mathbf{Y}_{\text{Thru},\Pi} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} Y_1 + Y_2 & -Y_1 \\ -Y_1 & Y_1 + Y_2 \end{bmatrix}, \tag{5.18}$$

while the Y-parameters of the left and right bisections are provided in [28] as

$$\mathbf{Y}_{\mathrm{L},\Pi} = \begin{bmatrix} Y_{11} - Y_{21} & 2Y_{21} \\ 2Y_{21} & -2Y_{21} \end{bmatrix} \; ; \; \mathbf{Y}_{\mathrm{R},\Pi} = \begin{bmatrix} -2Y_{21} & 2Y_{21} \\ 2Y_{21} & Y_{11} - Y_{21} \end{bmatrix}. \tag{5.19}$$

For the T model, we obtain the following results [28]

$$\mathbf{Z}_{\mathrm{Thru,T}} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} Z_1 + Z_2 & Z_2 \\ Z_2 & Z_1 + Z_2 \end{bmatrix}. \tag{5.20}$$

$$\mathbf{Z}_{\mathrm{L,T}} = \begin{bmatrix} Z_{11} + Z_{21} & 2Z_{21} \\ 2Z_{21} & 2Z_{21} \end{bmatrix} \; ; \; \mathbf{Z}_{\mathrm{R,T}} = \begin{bmatrix} 2Z_{21} & 2Z_{21} \\ 2Z_{21} & Z_{21} + Z_{22} \end{bmatrix}. \tag{5.21}$$

The conversion of Z and Y parameter into S and T parameters are found in Table 5.2.

## 5.3 Wirebond Model Extraction

The discussion in this section revolves around how to estimate the model parameters of wirebonds from port measurements. The layout of this section is divided into two pieces: **i)** The development of the mathematical equations of wirebond models in terms of ABCD-parameters. **ii)** The optimization problem and the procedures to solve it.

### 5.3.1 Discrete Lumped Model

The assumption here is that the wirebonds can be described by discrete lumped elements. There are two cases to distinguish:

#### Non-grounded wirebonds

If a wirebond is not floating above a ground plane or the height between the wirebond and the ground plane is large enough to neglect the capacitance between them, then the wirebond can be modeled as series inductance and resistance. If the bond pads are not de-embedded, they can also be included as a bisection split of a T-structure (similar to Figure 5.4b). Even if the measurements were de-embedded, there might remain residual error which can be included in the pads' model.

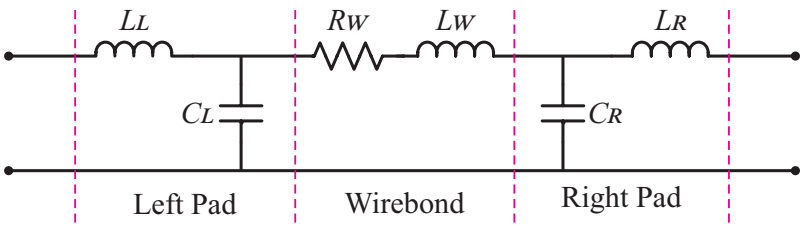



FIGURE 5.5: Non-grounded wirebond model.

The overall ABCD matrix of the cascaded structure in Figure 5.5 can be found by multiplying the ABCD matrices of each structure (see Table 5.1 for reference)

$$\mathbf{A}_{\text{Model}}(\omega,\mathbf{p}) = \underbrace{\begin{bmatrix}1 & j\omega L_L\\ 0 & 1\end{bmatrix}\begin{bmatrix}1 & 0\\ j\omega C_L & 1\end{bmatrix}}_{\text{Left pad}}\underbrace{\begin{bmatrix}1 & R_W + j\omega L_W\\ 0 & 1\end{bmatrix}}_{\text{Wirebond}}\underbrace{\begin{bmatrix}1 & 0\\ j\omega C_R & 1\end{bmatrix}\begin{bmatrix}1 & j\omega L_R\\ 0 & 1\end{bmatrix}}_{\text{Right pad}}, \tag{5.22}$$

where $\mathbf{p} = [L_L, C_L, L_W, R_W, C_R, L_R]^T$ is the vector containing the model parameters, and $\omega = 2\pi f$ is the radial frequency. Generally, pad parameters need not to have the same values, i.e., $L_L \neq L_R$ and $C_L \neq C_R$, but by imposing the equality of their values we can reduce the complexity of the optimization. To find the equivalent S-parameters of Eq. (5.22), equations in Table 5.2 can be used.

### Grounded wirebonds

In the case a wirebond is above a ground plane and the parasitic capacitance can not be neglected, a T-structure can be used to model the wirebond. Figure 5.6 shows the schematic of the equivalent circuit model. Similar to before, pads are included as L-structure at both ends. It should be noted that the left and right capacitors will also include some capacitance from the wirebond.

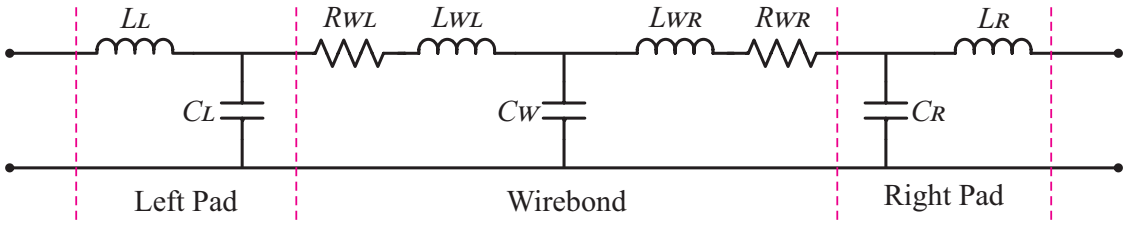



FIGURE 5.6: Grounded wirebond model.
The pad capacitors also share some capacitance from the wirebond.

The ABCD description of Figure 5.6 is written—similar to before—as the multiplication of the ABCD matrices of the individual elements (see Table 5.1 for reference)

$$\begin{aligned}\mathbf{A}_{\text{Model}}(\omega,\mathbf{p}) = {} & \underbrace{\begin{bmatrix}1 & j\omega L_L\\ 0 & 1\end{bmatrix}\begin{bmatrix}1 & 0\\ j\omega C_L & 1\end{bmatrix}}_{\text{Left pad}}\cdots\\ & \cdots\underbrace{\begin{bmatrix}1 & R_{WL} + j\omega L_{WL}\\ 0 & 1\end{bmatrix}\begin{bmatrix}1 & 0\\ j\omega C_W & 1\end{bmatrix}\begin{bmatrix}1 & R_{WR} + j\omega L_{WR}\\ 0 & 1\end{bmatrix}}_{\text{Wirebond}}\cdots\\ & \cdots\underbrace{\begin{bmatrix}1 & 0\\ j\omega C_R & 1\end{bmatrix}\begin{bmatrix}1 & j\omega L_R\\ 0 & 1\end{bmatrix}}_{\text{Right pad}},\end{aligned} \tag{5.23}$$

where $\mathbf{p} = [L_L, C_L, L_{WL}, R_{WL}, C_W, L_{WR}, R_{WR}, C_R, L_R]^T$ is the vector containing the model parameters, and $\omega = 2\pi f$ is the radial frequency. Also, here, the S-parameters can be computed via the conversion equations in Table 5.2.

### 5.3.2 Distributed Model

If the wirebond is a straight wire and above a ground plane, or it is implemented in a GSG structure (coplanar wirebonds), a lossless transmission line model can be used. Figure 5.7 depicts the model in which the wirebond is assumed to be surrounded by air (i.e., $\epsilon_{eff} = \epsilon_{Air} = 1$).

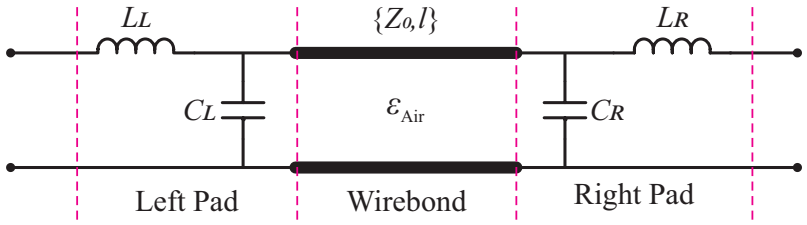



FIGURE 5.7: Wirebond modeled as one section transmission line.

The ABCD-parameters of above figure is given by

$$\mathbf{A}_{\text{Model}}(\omega, \mathbf{p}) = \underbrace{\begin{bmatrix} 1 & j\omega L_L \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ j\omega C_L & 1 \end{bmatrix}}_{\text{Left pad}} \underbrace{\begin{bmatrix} \cos(\beta l) & jZ_0 \sin(\beta l) \\ j\frac{1}{Z_0}\sin(\beta l) & \cos(\beta l) \end{bmatrix}}_{\text{Wirebond}} \cdots$$
$$\cdots \underbrace{\begin{bmatrix} 1 & 0 \\ j\omega C_R & 1 \end{bmatrix} \begin{bmatrix} 1 & j\omega L_R \\ 0 & 1 \end{bmatrix}}_{\text{Right pad}} \tag{5.24}$$

where $\mathbf{p} = [L_L, C_L, l, Z_0, C_R, L_R]^T$ is the vector of the model parameters. The lossless assumption is generally valid at high frequencies since the impedance of both the distributed inductance and capacitance dominate compared to the distributed resistance and conductance. However, if very thin wirebonds are used, or the wires are covered with lossy dielectric (e.g., epoxy), then a lossy transmission line model must be used (see Table 5.1).

A further improvement of the model in Figure 5.7 is obtained by including the transition effects of the wirebond from different substrates. If the dielectric constant is not the same along the wire, the transmission line can be divided into segments, where each segment has an effective dielectric constant $\epsilon_{Eff}$. Such a model is reasonable in scenarios of wire bonding two chips, where their pads are not located at the edge of the chip. The offset of the pads is common in chip designs, as this is a prevention measure to protect the pads from getting damage during die-sawing [15]. The effective dielectric constant is usually difficult to estimate, as it depends on how far the wirebonds from the substrate. Nevertheless, we can include $\epsilon_{Eff}$ in the optimization problem while limiting its value to: $\epsilon_{Air} < \epsilon_{Eff} < \epsilon_{Sub}$.

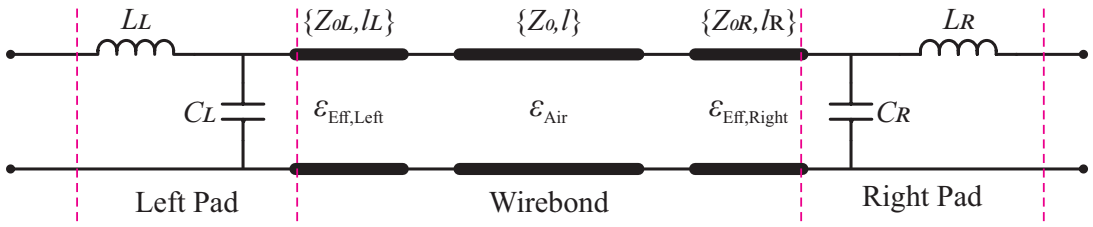



FIGURE 5.8: Wirebond modeled as multi-segmented transmission line.

### 5.3.3 The Optimization Problem

To this end, only mathematical equations of the models were presented. This subsection, however, explains how to solve for the model parameters and obtain the optimal fitting. We start by defining an error function that describes the error between the measured S-parameters ($\mathbf{S}_{\text{Meas}}$) and the S-parameters of the model ($\mathbf{S}_{\text{Model}}$). The error can be defined in various ways, but we limit our focus to the most popular formulations:

- **Average L1 Norm**:

$$E_{L1}(\omega, \mathbf{p}) = \frac{1}{N^2} \sum_{i=1}^{N} \sum_{j=1}^{N} \left| S_{ij,\text{Meas}}(\omega) - S_{ij,\text{Model}}(\omega, \mathbf{p}) \right| \tag{5.25}$$

- **Average L2 Norm**:

$$E_{L2}(\omega, \mathbf{p}) = \frac{1}{N^2} \sum_{i=1}^{N} \sum_{j=1}^{N} \left| S_{ij,\text{Meas}}(\omega) - S_{ij,\text{Model}}(\omega, \mathbf{p}) \right|^2 \tag{5.26}$$

where $N$ is the number of ports, $\omega$ is the radial frequency, and $\mathbf{p}$ is the vector containing the parameters of the model. As it is apparent, the differences between L1 norm and L2 norm lies in the square on the magnitude. Generally, L2 norm is considered more robust as it emphasizes more on the error via the square operator. On the other hand, L2 norm has the disadvantage at outlier rejection compared to L1 norm, which treats everything linearly. That is, if the measurements have outliers, the error in L2 norm will explode, while L1 norm treats the outliers linearly.

Typically, S-parameters are used to define the error function, and although we can use other parameters (e.g., ABCD-parameters), the measurements themselves are usually taken as S-parameters with a VNA, thus it makes the most sense to define the model also in the S-domain. Another advantage of defining the model in the same parameters as the measurements is to avoid affecting the noise statistics in the measurements. For example, if noisy S-parameters were measured, we can assume that the noise is additive Gaussian. If we convert the measurements into e.g., the ABCD-domain, we are affecting the noise by performing non-linear operations, hence affecting the quality of the optimization.

The optimization problem is formulated by defining a cost function comparing the error function in Eq. (5.25) or (5.26) to a desired goal at all frequencies. This is written as

$$F(\mathbf{p}) = \frac{1}{M} \sum_{m=1}^{M} \left| G(\omega_m) - E(\omega, \mathbf{p}) \right|^L, \tag{5.27}$$

where $M$ is the number of measured frequencies, $G(\omega_m)$ is the desired goal at $\omega = \omega_m$, and $L$ is the norm order (similar to before, this is typically either 1 or 2). To find the optimal solution of $\mathbf{p}$, the cost function is minimized

$$\hat{\mathbf{p}} = \underset{\mathbf{p}}{\operatorname{argmin}}\, F(\mathbf{p}). \tag{5.28}$$

Because Eq. (5.28) is a non-linear optimization problem, we can only solve it using iterative numeric methods. For example, we can use gradient based algorithms (e.g., Newton's methods) or non-gradient based algorithms (e.g., Differential Evolution). The procedures to solve Eq. 5.28 are as follows:

1. Choose a reasonable initial value for $\mathbf{p}$.
2. Set constraints on $\mathbf{p}$, i.e., we limit the search range to reduce the complexity of the problem.
3. Start solving with a non-gradient based algorithm, because gradient based algorithms tend to get hung at the nearest local minimum, which might not be the global minimum.
4. After obtaining a satisfactory result from the non-gradient algorithm, switch to gradient based algorithm while using the result from the previous step as an initial value. Doing so should provide the optimal solution, as using only non-gradient based algorithms do not guarantee optimal solution.

In Chapter 6 these procedures are applied on S-parameters measurements of GSG wirebonds to extract their equivalent circuit model.

# Chapter 6

# GSG Wirebonds Measurements

The aim of this chapter is to present and evaluate GSG (Ground-Signal-Ground) wirebonds measurements. From the measurements, a proper equivalent circuit model is extracted and analyzed.

## 6.1 Measurement Setup

The setup consists of 2 chips connected together with GSG wirebonds. They are measured on a wafer probe station, which is connected to a VNA.

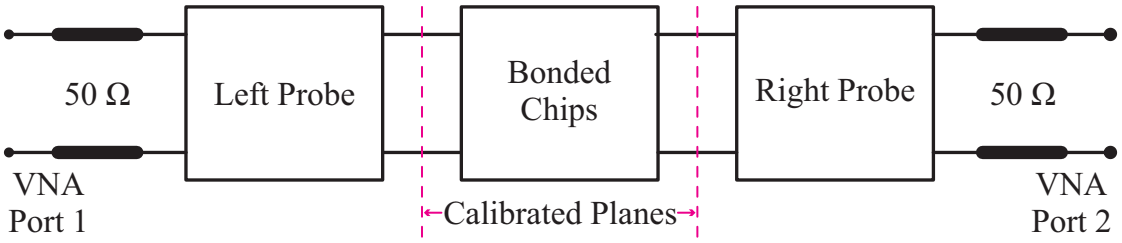


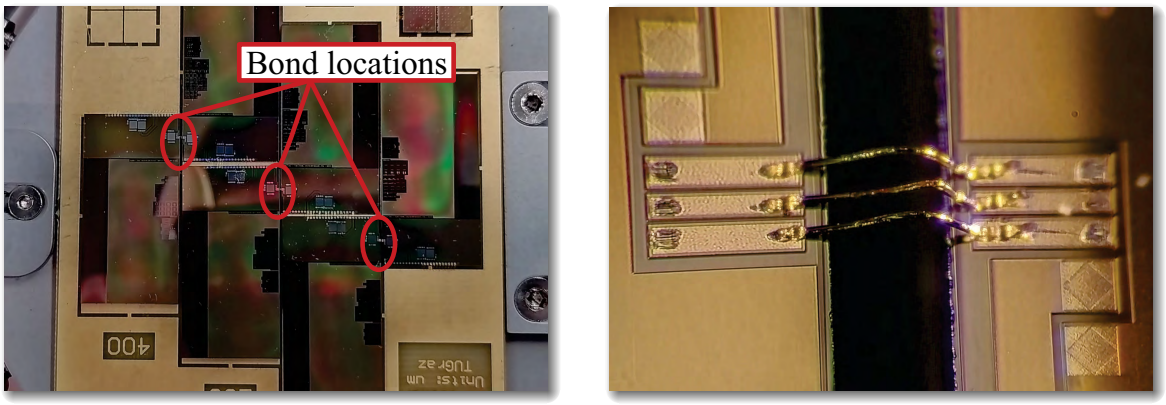

FIGURE 6.1: Block diagram of the measurement setup.

The bonded chips are 750 $\mu$m thick passive silicon interposers[1], which were fabricated by AMS AG using 0.35$\mu$ CMOS technology. On one side of each interposer there exist 400 $\mu$m long GSG pads, which are used to realize the GSG wirebonds. The pads are made of Al and have a 100 $\mu$m pitch. The wirebonds are implemented by placing 2 interposers such that the GSG pads of each chip is aligned and faced towards the GSG pads of the other chip. The alignment is achieved by gluing the interposers on a custom designed PCB, which has markings on it to indicate where to place the interposers and how far they are from each other. The PCB can hold 6 interposers, hence 3 pairs of GSG pads. Finally, the pads are bonded with 25 $\mu$m Au wire using wedge tool. Figure 6.2 depicts both the interposers on the PCB and the GSG wirebonds.

A photo of the used bonder machine is shown in Figure 6.3. The machine is semi-automatic and is only motorized in two axes: Up-down and back-forth. Because there is no motorization in the sideways axis, one can expect to see few bonds being slightly

[1] I designed the interposers for the project TriTon (see Chapter 1). It was a fortunate coincident that I included GSG pads on the edge of the chips.

off. Additionally, the loop height of the wirebonds was difficult to maintain. Nonetheless, these disparities are not significant when seen under the microscope.




(A) (B)

FIGURE 6.2: Photo of bonded interposer chips. (A) Interposers glued on a carrier PCB. (B) A zoomed photo of the GSG wirebonds ("Wirebond 400").

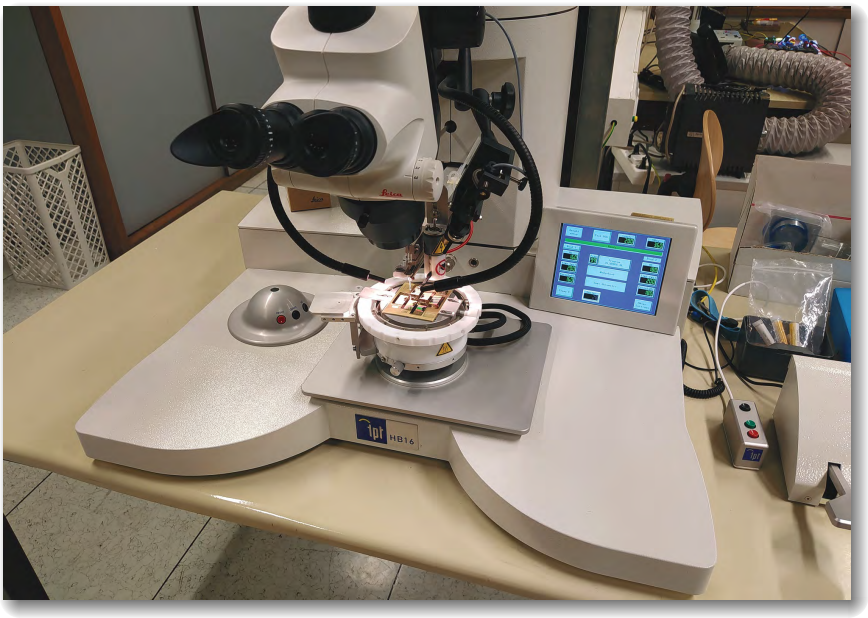


FIGURE 6.3: Bonder machine (TPT-HB16).

On the wafer probe station, a pair of 100 $\mu$m pitch wafer probes are mounted. The probes are connected directly to a VNA (R&S 10 MHz . . . 67 GHz). The initial cabling from the VNA was done using long cables with 3.5 mm connectors. Afterwards, short flexible cables with 2.92 mm connectors are used to connect from the long 3.5 mm cables to the probes. The purpose of these short flexible cables is to allow for the probes to move freely without affecting the measurements.

The probes and the 2.92 mm cables are specified up to 40 GHz, however, the 3.5 mm cables are specified up to 34 GHz. Therefore, measurements after and around 34 GHz are likely to be error-prone (see Section 6.3). Figure 6.4 shows the wafer probes in contact with the chips, and Figure 6.5 shows the full setup of the wafer probe station.

Before performing any measurements, the VNA needs to be calibrated. The used calibration method is SOLT (Short-Open-Load-Thru), and the stimulus parameters of the VNA were set as following:

- Start frequency: 50 MHz.
- Step frequency: 50 MHz
- Stop frequency: 40 GHz.
- Power: 0 dBm.
- IF bandwidth: 1 kHz.

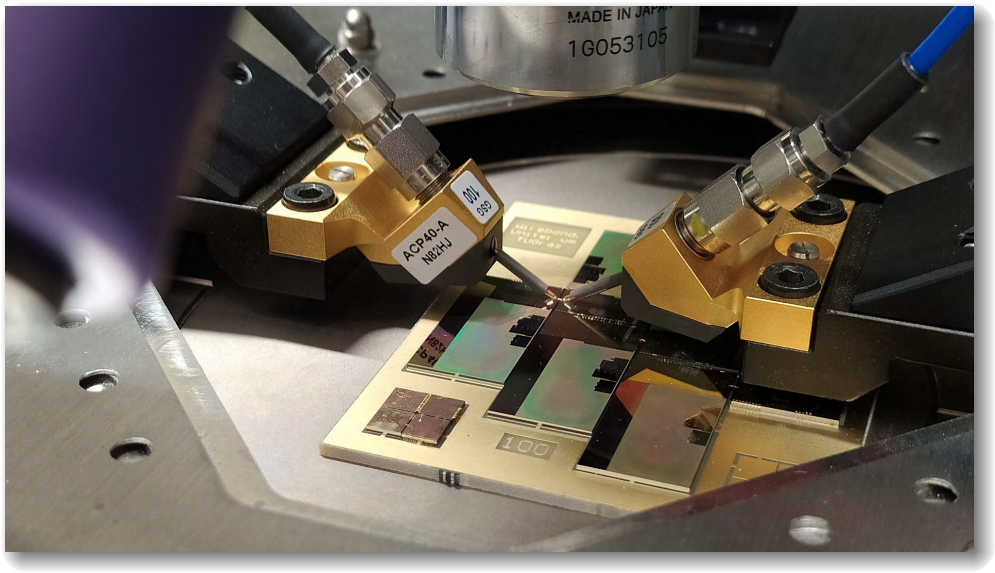



FIGURE 6.4: Wafer probes.

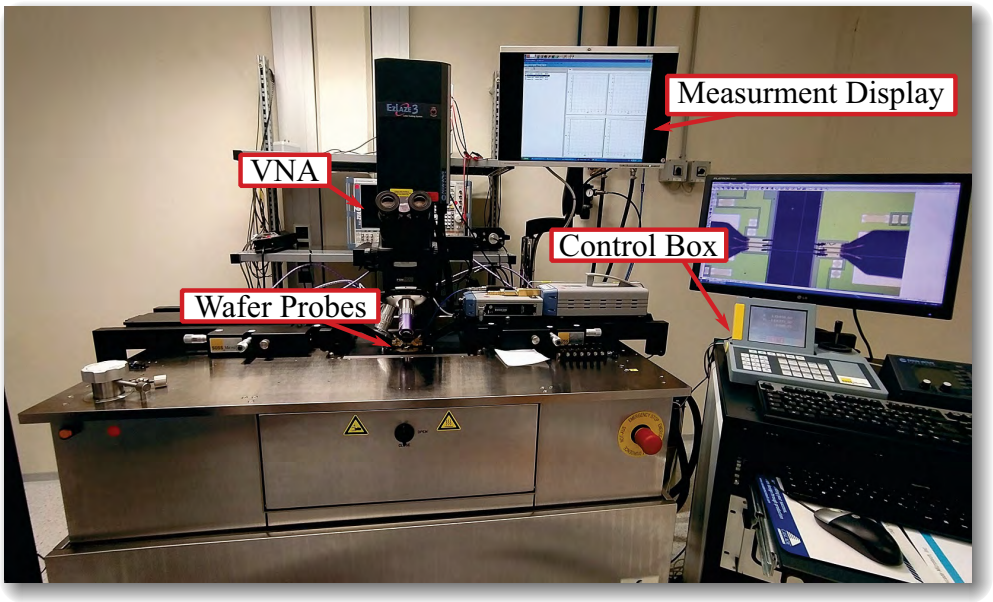



FIGURE 6.5: Wafer probe station.

## 6.2 Measured Structures

Several GSG wirebonds with different length were implemented and measured. The bond pads were also measured separately—this allows later to de-embed their effects from the wirebonds measurements.

### 6.2.1 Bond Pads

First structures to measure are the bond pads. This is necessary for de-embedding purposes. A screenshot of the pads is depicted in Figure 6.6. Because the pads are identical across all interposers, we only need to measure one set of them. The obtained measurements can be later mirrored to represent the pads of the opposite side.

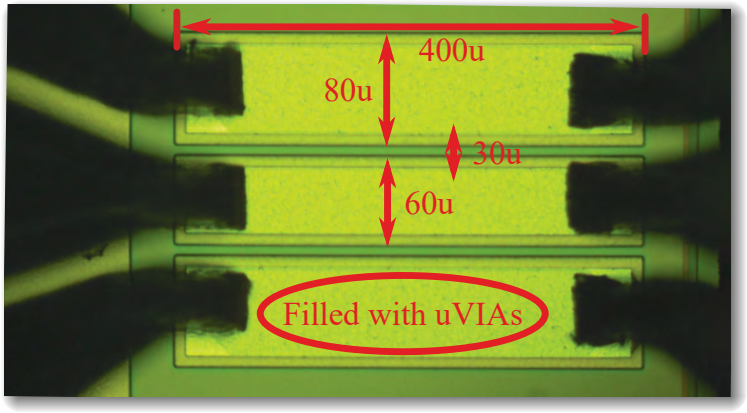



FIGURE 6.6: Measured bond pads.

Later in the measurements, we learn that the pads are lossy. This is probably due to the structure of the pads, which consists of 4 metallic layers connected together with a massive amount of uVIAs. The VIAs are necessary to provide support for the pads when bonding. At time of writing, the exact reason for the losses is unclear, but it is most likely due to the oxide substrate between the metal layers, and the fact that the pads are long and have many uVIAs within them.

### 6.2.2 Wirebonds

A sample of the measured GSG wirebonds is depicted in Figure 6.7. In the figure, two parameters are highlighted: **i)** the air gab between the interposers ($d_{AIR}$). **ii)** the pad-to-pad spacing ($d_{PP}$). The measurements were taken for different separation distances, hence different wire lengths. Table 6.1 lists the implemented wirebonds with their corresponding $d_{AIR}$ and $d_{PP}$ (distances were measured using the microscope-camera on the probe station). The label numbers for the wirebonds in Table 6.1 were meant to represent the air gab in $\mu$m between the chips. These values were used in the design of the carrier PCB to indicate the exact location where to glue the interposers. Unfortunately, it was difficult to get the interposers glued at the exact position because the alignment was done manually and the markings on the PCB have an accuracy of $\pm 50\,\mu$m.

The loop height of the wirebonds is not controlled, i.e., each wire in the GSG bonds might have different heights, hence different wirebond lengths. However, this should not be significant. In general, the loop height is dependent on the separation distance. The longer the distance, the longer the loop.

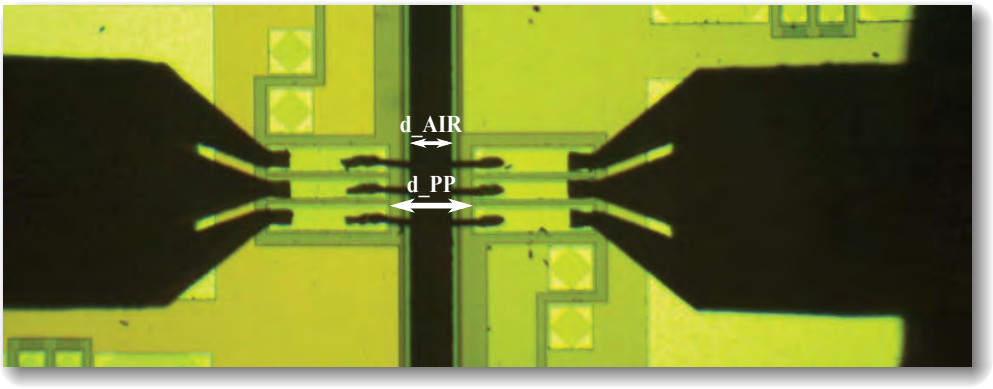
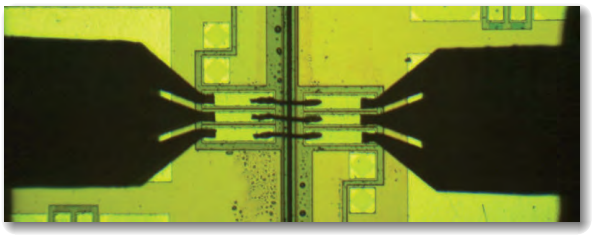


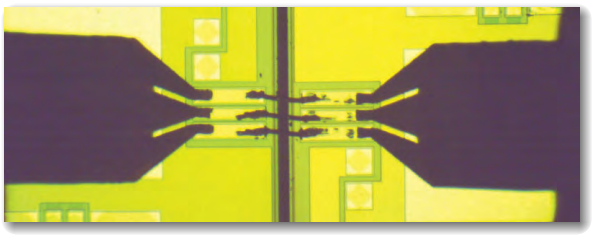

FIGURE 6.7: Wirebond 200.

TABLE 6.1: Measured GSG wirebonds.

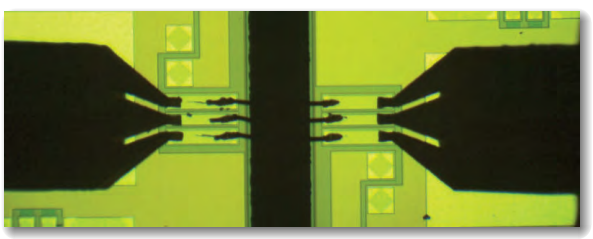
| Wirebonds | $d_{AIR}$ ($\mu$m) | $d_{PP}$ ($\mu$m) | Wirebonds | $d_{AIR}$ ($\mu$m) | $d_{PP}$ ($\mu$m) |
|---|---|---|---|---|---|
| 100 | 28 | 160 | 900 | 854 | 984 |
| 100B | 61 | 193 | 1000 | 906 | 1036 |
| 200 | 145 | 277 | 1200 | 1131 | 1264 |
| 400 | 340 | 475 | 1500 | 1342 | 1475 |
| 600 | 502 | 630 | 2000 | 1865 | 1999 |
| 800 | 707 | 840 | | | |



(A) Wirebond 100.

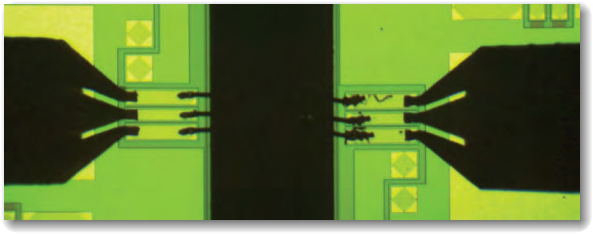


(B) Wirebond 100B.

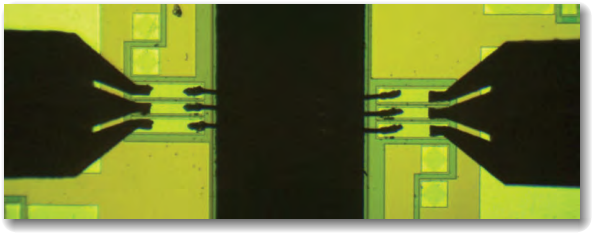


(C) Wirebond 400.

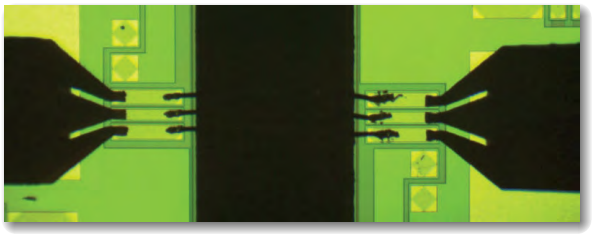
(D) Wirebond 600.



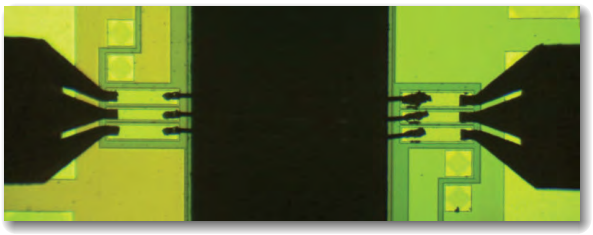
(E) Wirebond 800.



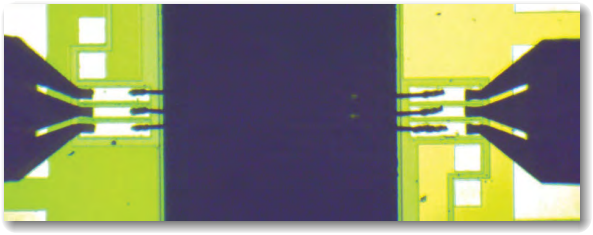
(F) Wirebond 900.



(G) Wirebond 1000.



(H) Wirebond 1200.



(I) Wirebond 1500.

(J) Wirebond 2000.

FIGURE 6.8: Screenshots of all measured wirebonds.
(Wirebond 200 is shown in Figure 6.7)

## 6.3 Raw Measurements

Figure 6.9 shows the raw S-parameters measurments of the pads and the wirebonds. As mentioned earlier, we can observe the significant losses in the pads. Furthermore, the measurements have spike noise at two discrete frequencies around 28 GHz and 37 GHz. This is likely due to the used 3.5 mm cables. Nevertheless, because spike noise are considered outliers in the measurements, we can remove them with a median filter. Figure 6.10 shows the filtered measurements, where the used filter is Hampel algorithm with $k = 9$, and $nsigma = 1$. As can be seen, the spike noise are eliminated without affecting the rest of the measurements.

From the measurements, one can recolonize the increase in the resonance frequency with the decrees of the wire length. This is the result of reduction in the wirebonds inductance because of the shorter bonds ($\omega = 1/\sqrt{LC}$).

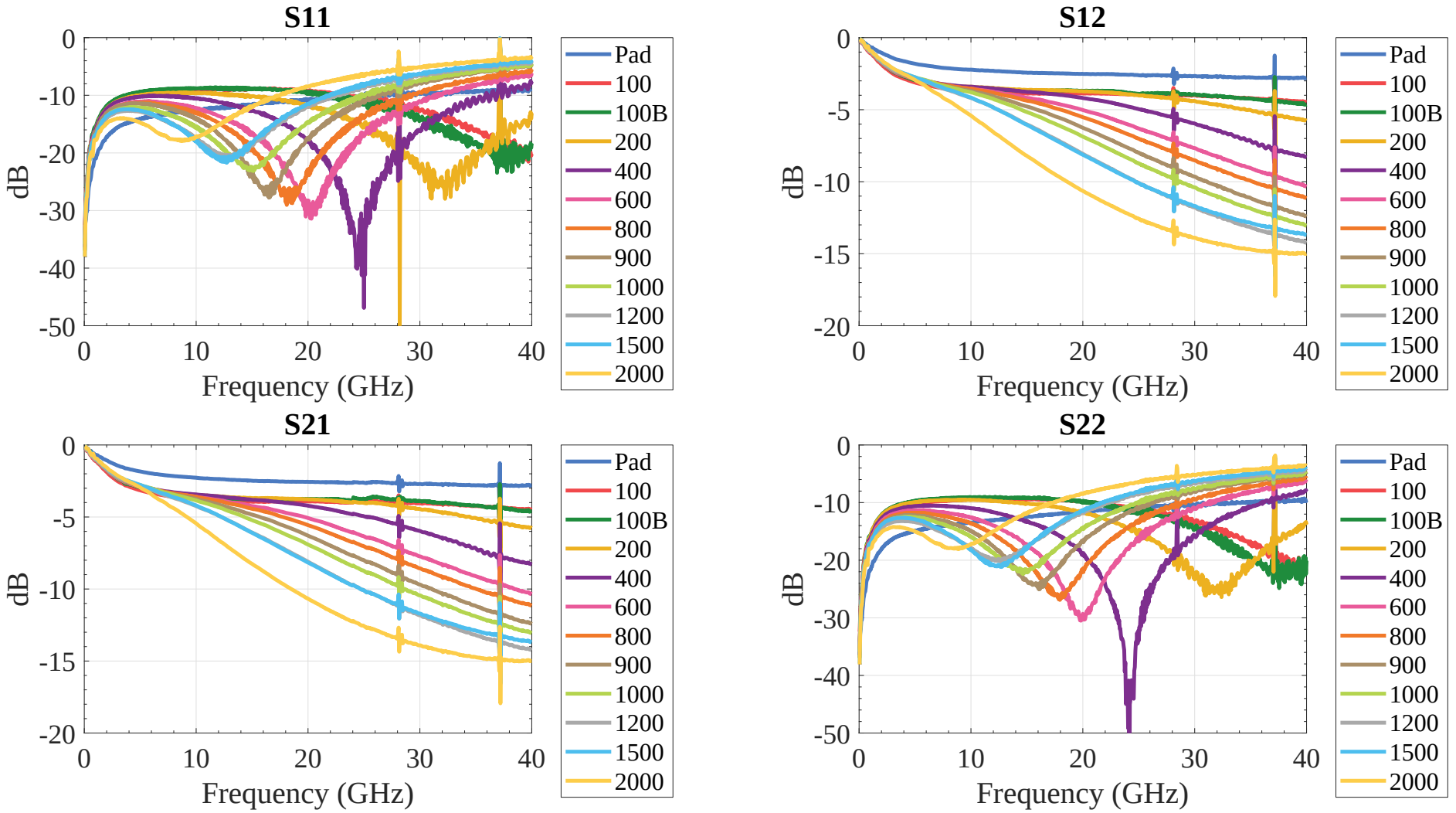



FIGURE 6.9: Wirebonds raw measurements.

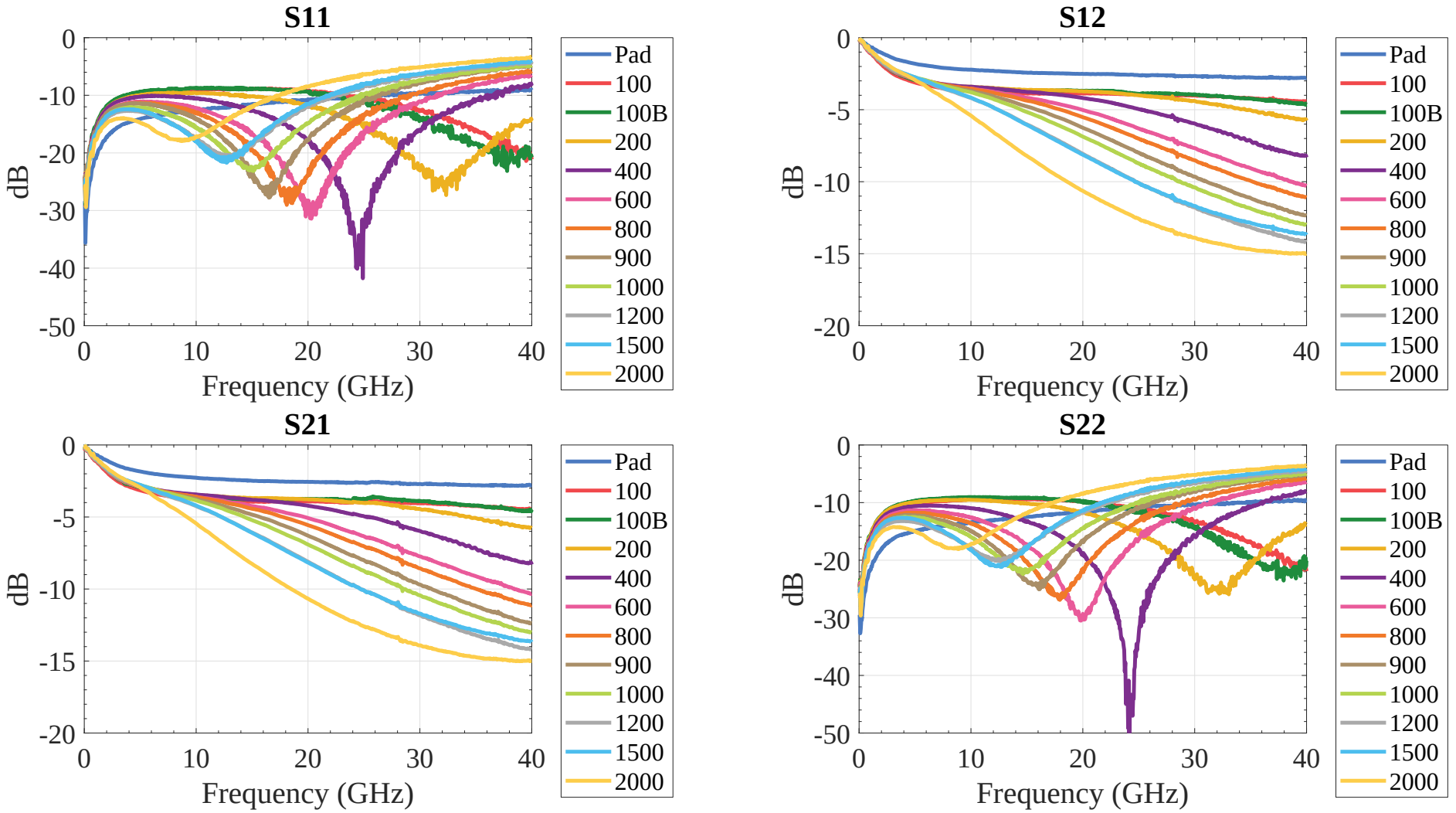



FIGURE 6.10: Filtered measurements.
(Both real and imaginary parts were filtered with Hampel algorithm **hampel(x,k,nsigma)**, where $k = 9$, and $nsigma = 1$)

## 6.4 De-embedded Measurements

To obtain the actual measurements of the wirebonds, we need to de-embed the pads from the raw measurements. For that, we use the direct de-embedding method, which was discussed in Chapter 5. In our case, the DUT is the wirebonds and the fixtures are the pads. The de-embedding is done using the T-parameters as follows:

$$\mathbf{T}_{\text{DUT}} = \mathbf{T}_{\text{L}}^{-1}\mathbf{T}_{\text{Meas}}\mathbf{T}_{\text{R}}^{-1}, \tag{6.1}$$

where $\mathbf{T}_{\text{L}}$ and $\mathbf{T}_{\text{R}}$ are the T-parameters of the measured left and right pads, respectively, and $\mathbf{T}_{\text{Meas}}$ is the T-parameters of the embedded measurements. Since the original measurements were taken as S-parameters, these need to be converted into T-parameters according to the conversion equations in Table 5.2. Also, in Appendix B you find MATLAB functions for several parameter conversions.

Because only one side of the pads were measured, we need to mirror the measured pads' S-parameters to obtain the S-parameters of the other pads. In our case, we recognize from Figure 6.6 that the left pads were measured, therefore, the S-parameters of the right pads are given in terms of the S-parameters of the left pads,

$$\mathbf{S}_{\text{L}} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}; \qquad \mathbf{S}_{\text{R}} = \begin{bmatrix} S_{22} & S_{12} \\ S_{21} & S_{11} \end{bmatrix}. \tag{6.2}$$

Ideally, because the pads are passive and symmetric, $S_{11} = S_{22}$ and $S_{12} = S_{21}$, but because of measurements inaccuracies, slight deviation can be observed in the measurements.

Figure 6.11 shows the de-embedded measurements from the filtered raw measurements. Because of slight measurement inaccuracy, we can observe an overshoot in both de-embedded transmission coefficients: $S_{21}$ and $S_{12}$. The overshoot has almost a constant value among all measured wirebonds, equals 0.4 dB (see Figure 6.11). This is an indication that the measurements were slightly 'over de-embedded', i.e., the de-embedding removed more than just the pads out from the measurements. In general, this offset value of 0.4 dB is considered low and should not affect model extraction. Nevertheless, there are methods to estimate and correct for this error mathematically. For example, MATLAB offers a function `makepassive()` that can detect and correct non-passive S-parameters measurements. This function, however, cannot be used in our case because the de-embedded measurements have some error at the outlier frequencies: 28 GHz and 37 GHz. Although, these spikes were filtered forehand with the median filter, some residuals remain which causes discontinuity when applying the function `makepassive()`.

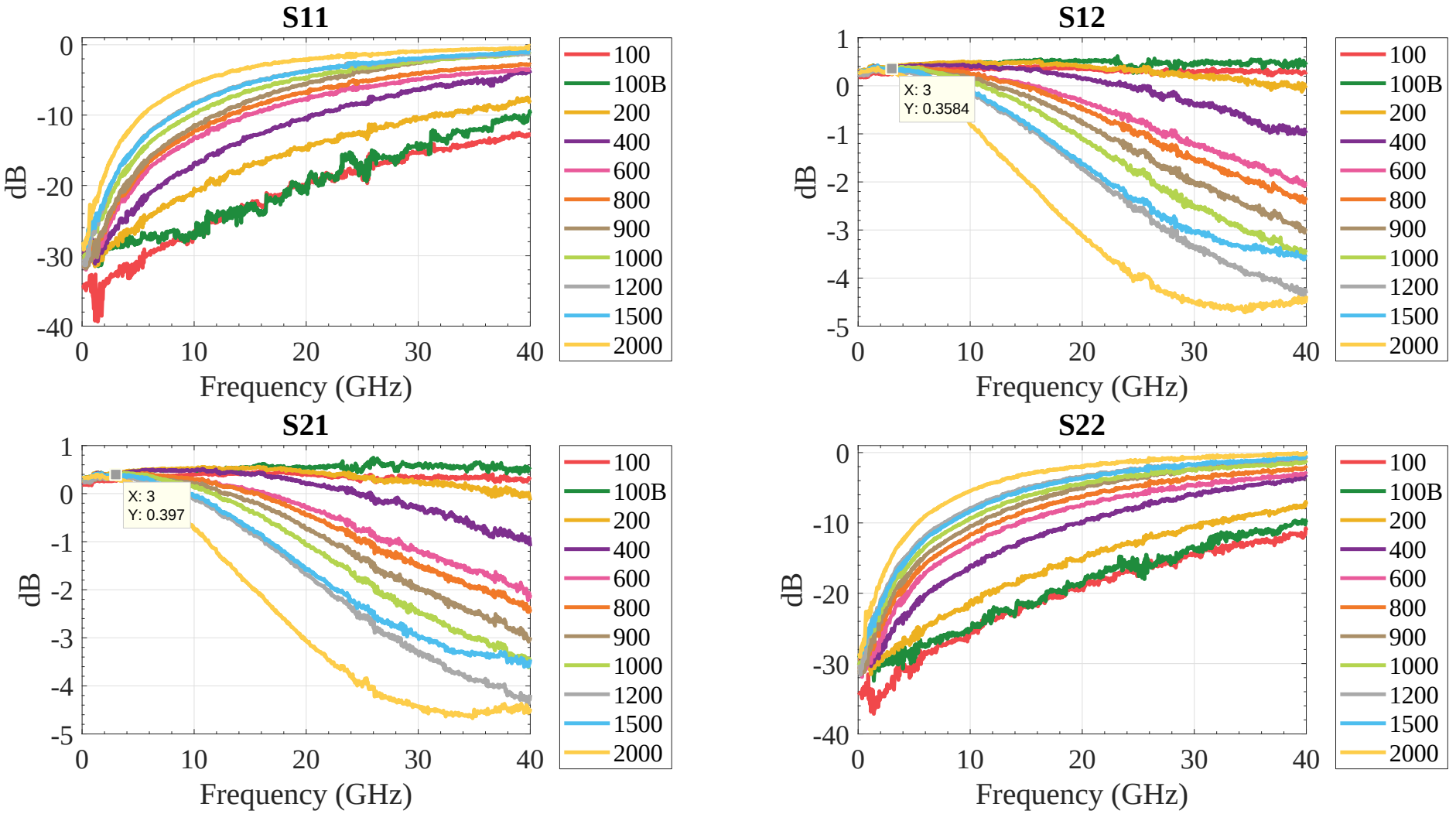



FIGURE 6.11: Wirebonds de-embedded measurements.

## 6.5 Model Extraction

### 6.5.1 Optimization with AWR

The software package AWR Design Environment offers versatile optimization functionality that can be used to find circuit models from S-parameters measurements. In this subsection, the basic steps of using the AWR optimization tool is presented. For in-depth explanation, please refer to [29]. The preparations for using the optimization tool are as follows:

1. Import the de-embedded measurement[2]. This is done in the project window on the left side.

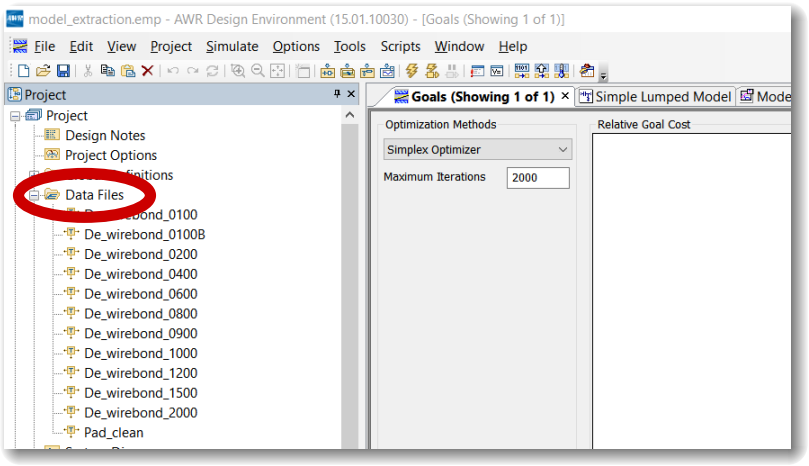



FIGURE 6.12: Import touchstone files in AWR.

2. Draw the circuit model and define the optimization variables. The variables are defined with the equation button on the toolbar. At first, the variables are in black, but after defining them as optimization variables (from property menu) they turn into blue.

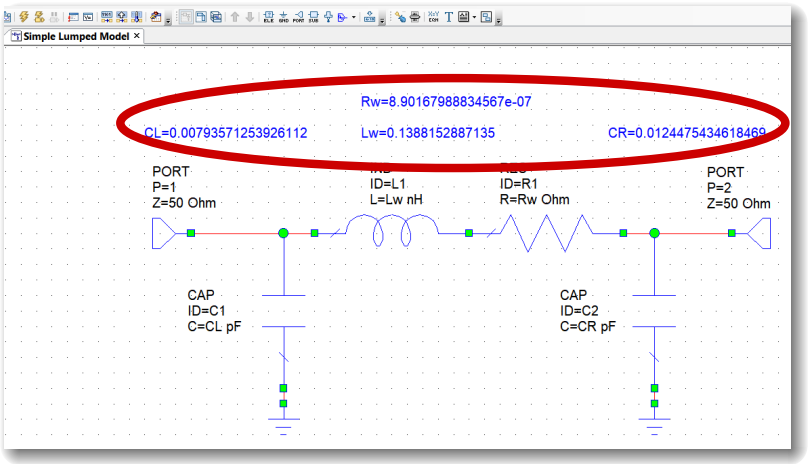



FIGURE 6.13: Schematic and optimization variables in AWR.

[2]AWR can also perform de-embedding, but because the measurements had to be filtered first in MATLAB, the de-embedding was also done in MATLAB.

3. Define an S-model error function in the 'Graphs' menu. This implements the error function that compares the circuit model with the measurements. This is similar to the discussion in the last section of Chapter 5.

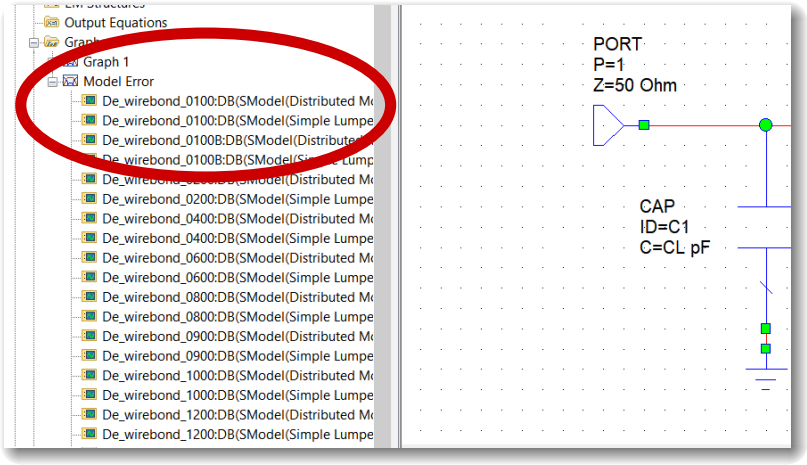



FIGURE 6.14: Defining S-model error function.

4. Finally, define a goal for the cost function given the S-model. Generally, a $-50\,\mathrm{dB}$ residual error is a good goal to hit (see last section in Chapter 5 for mathematical details).

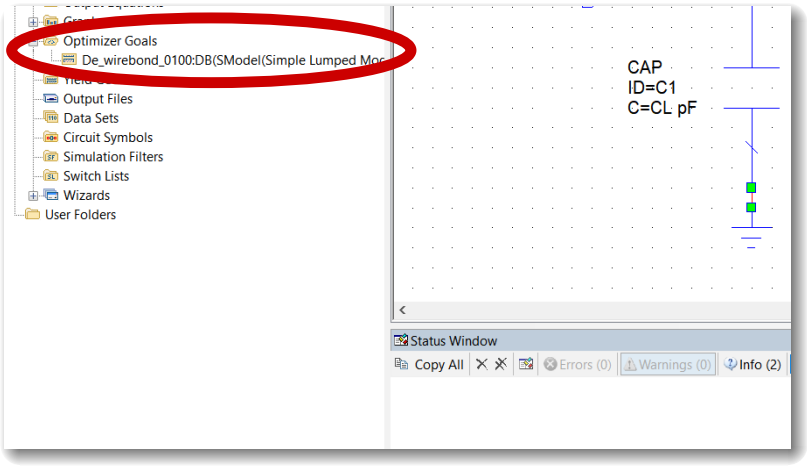



FIGURE 6.15: Defining goal criterion.

Now, after having everything prepared, we go to the 'Simulate' menu and open 'Optimize'. The prompted window is depicted in Figure 6.16. To start solving for the modeled parameters, following steps are recommended (more details are found in [29]):

1. Set constraints on the optimized variables. This speeds the process and helps to reduce false solutions.

2. Tune the variables manually with the tuner tool in the 'Simulate' menu and try to find a good initial guess by checking the results of the tuning in the S-model graph. A good initial guess can improve the speed and quality of the solution.

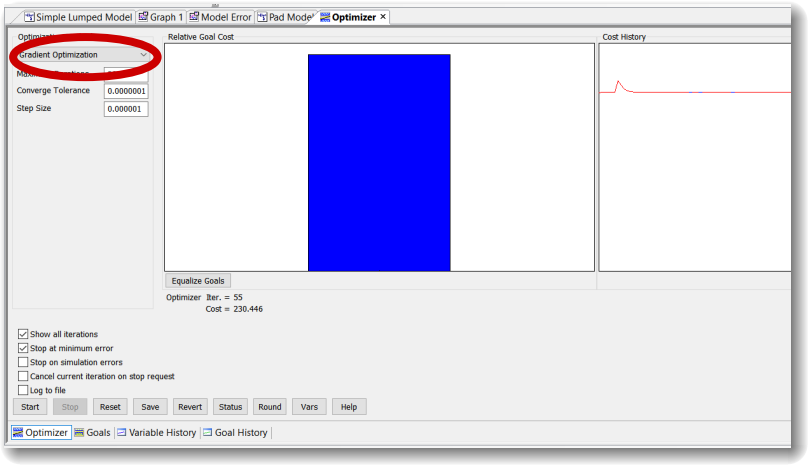



FIGURE 6.16: Optimization window.

3. Start the optimization using a non-gradient based algorithm, e.g., Differential Evolution. This allows to obtain a very close to optimal solution, while not getting hung at non-optimal local minimum.

4. After obtaining a satisfactory result from the previous step, switch the optimization algorithm to gradient based, e.g., Simplex Optimizer or Gradient Optimization. This allows to obtain the exact optimal solution. Generally, this will be very fast given the initial guess was obtained from the previous step, which is near the optimal solution.

### 6.5.2 Bond Pads Model

The bond pads are modeled as a Π structure, which is shown in Figure 6.17. The reason for this choice is to account for symmetry of the pads and to distribute the shunt impedance on both ends.

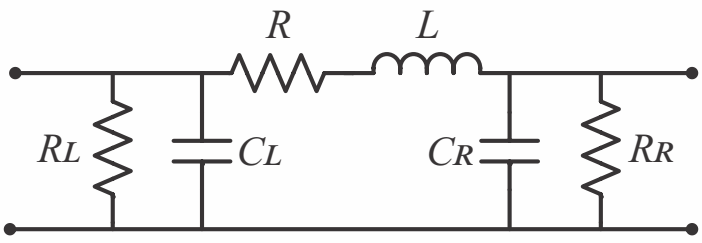



FIGURE 6.17: Bond pads circuit model.

After running the optimization in AWR, the obtained results is given in Table 6.2. We learn that the causation of the losses seen on the pads is due to leakage between the signal and ground paths. This is evidential from the low resistance value of $R_L$ and $R_R$. As highlighted previously, the losses are likely due to the VIAs and the oxide substrate between the metal layers. A comparison between the S-parameters of the model and the measurements is depicted in Figure 6.18.

TABLE 6.2: Optimal model parameters of the bond pads.

| $C_L$ (pF) | $R_L$ (Ω) | $L$ (pH) | $R$ (Ω) | $C_R$ (pF) | $R_R$ (Ω) |
|---|---|---|---|---|---|
| 0.056 | 164.27 | 59.961 | 2.72 | 0.051 | 316.057 |

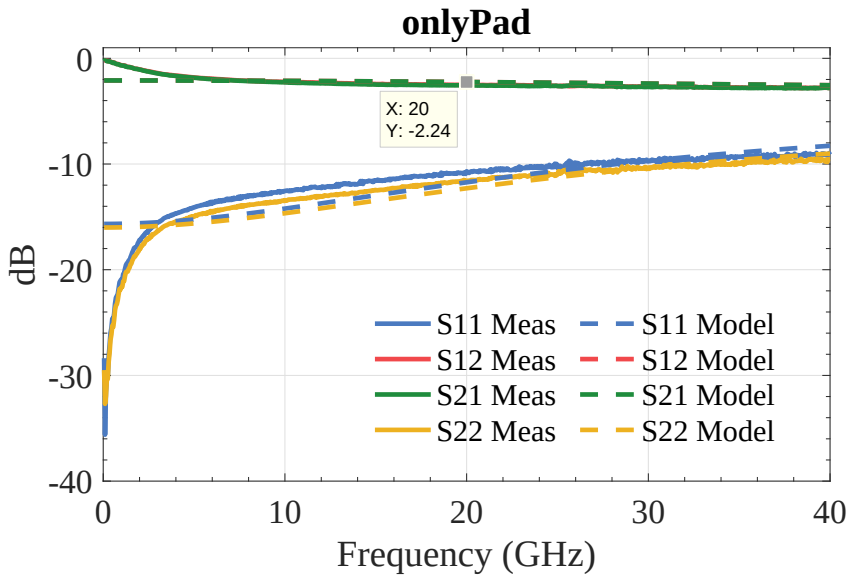



FIGURE 6.18: S-parameter of both circuit model and measurements of the bond pads. Dashed lines represent the model, while solid lines the measurements.

### 6.5.3 Wirebonds Model

Like the bond pads, a circuit model for the wirebonds is also defined—this is shown in Figure 6.19. The choice of this model was determined by experimenting with various configurations. For example, transmission line model was tested, however, the model only gave reasonable results when the wirebonds are longer than 0.5 mm. A more complex version of Figure 6.19 was tested; this involves the splitting of the inductance and resistance into two parts and using 3 capacitors (similar to the model in Figure 5.6 in Chapter 5). However, the results obtained did not improve significantly from the suggested model in Figure 6.19. Therefore, the choice was decided on using the simplest model, as it has fewer variables to work with, and its results are good for the measured frequency range.

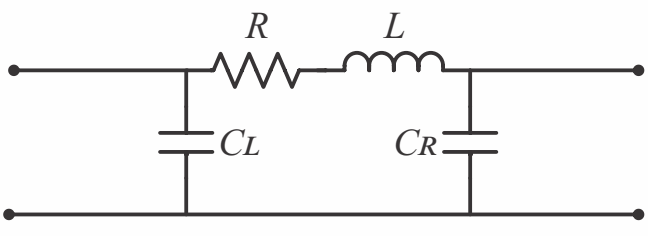
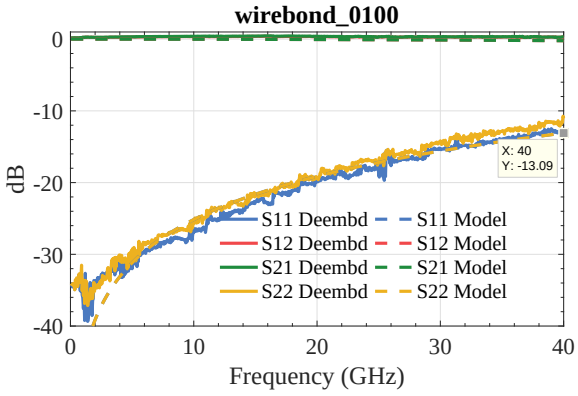



FIGURE 6.19: Wirebonds circuit model.

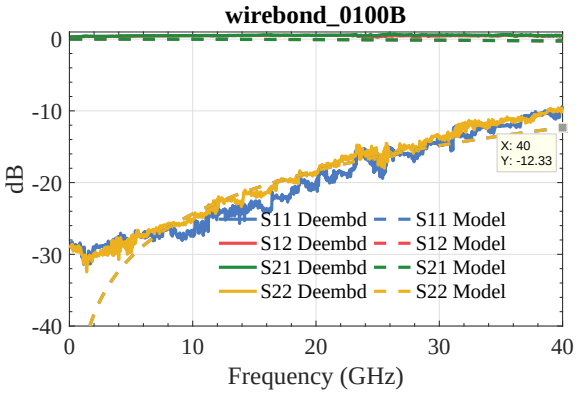
The extracted model parameters of all measured wirebonds are listed in Table 6.19. From the values in the table we can observe the increase of both capacitance and inductance with the increase of wire length. The resistance, however, kept fluctuating due to its negligible value. The S-parameters of both the model and measurements are overlapped and shown in Figure 6.20. We clearly see the strong agreement between the model and measurements. However, starting from "Wirebond 1200" we can observe at frequencies above 30 GHz the slight deviation of the model from the measurements. To obtain a better fitting at those frequencies, a more complex model is needed, e.g., cascade version of the used model. The 3 dB bandwidth of the wirebonds can be read starting from "Wirebond 800" plot (shorter wirebonds have wider bandwidth).

TABLE 6.3: Extracted model parameters of the measured wirebonds.

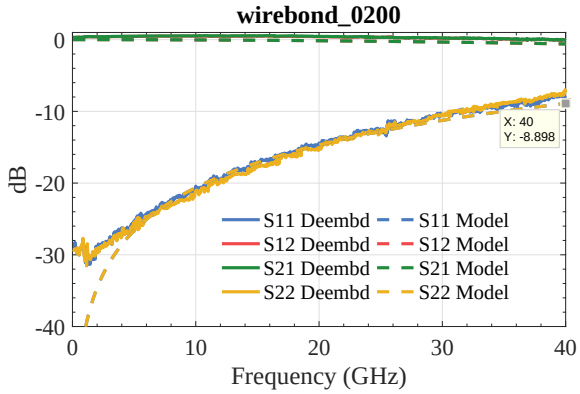
| Wirebonds | $C_L$ (pF) | $L$ (pH) | $R$ ($\mu\Omega$) | $C_R$ (pF) | Cost Residual |
|---|---|---|---|---|---|
| 100 | 0.008 | 138.816 | 0.924 | 0.012 | 15.93 |
| 100B | 0.012 | 151.124 | 1.559 | 0.010 | 117.96 |
| 200 | 0.012 | 208.613 | 0.473 | 0.012 | 65.79 |
| 400 | 0.013 | 320.722 | 7.052 | 0.012 | 106.38 |
| 600 | 0.017 | 423.283 | 8.356 | 0.017 | 20.19 |
| 800 | 0.019 | 478.772 | 8.175 | 0.017 | 51.24 |
| 900 | 0.018 | 560.256 | 2.280 | 0.015 | 141.34 |
| 1000 | 0.020 | 615.653 | 4.386 | 0.018 | 75.24 |
| 1200 | 0.024 | 728.036 | 2.059 | 0.020 | 70.49 |
| 1500 | 0.028 | 729.974 | 8.202 | 0.026 | 147.02 |
| 2000 | 0.032 | 1024.7 | 3.441 | 0.028 | 230.45 |



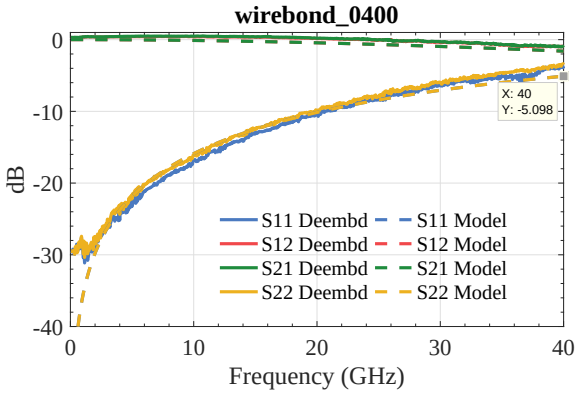

(A) Wirebond 100.



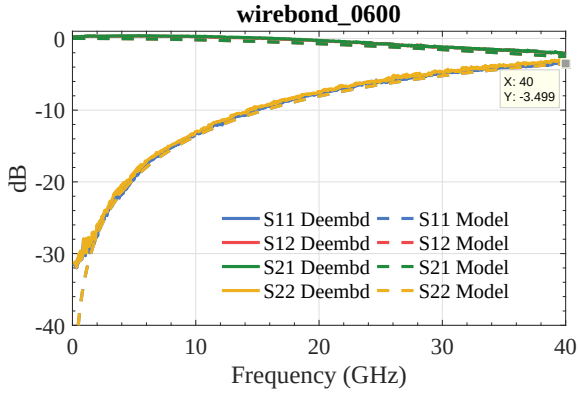

(B) Wirebond 100B.



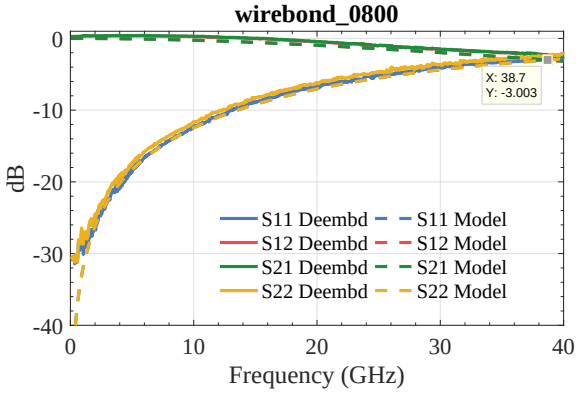

(C) Wirebond 200.



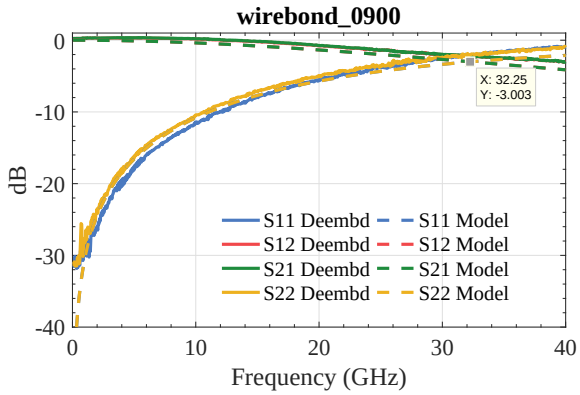

(D) Wirebond 400.



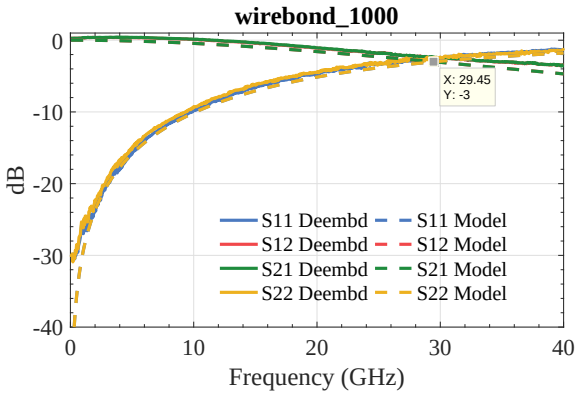

(E) Wirebond 600.



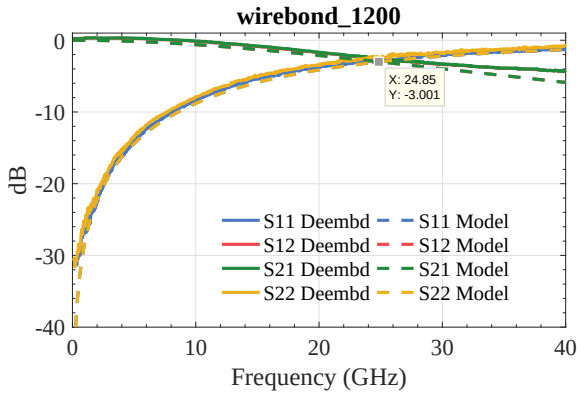

(F) Wirebond 800.



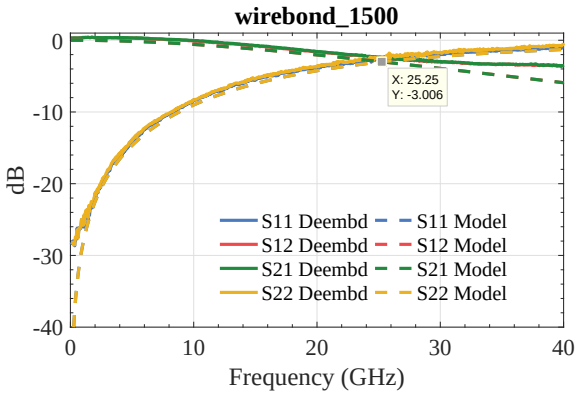

(G) Wirebond 900.



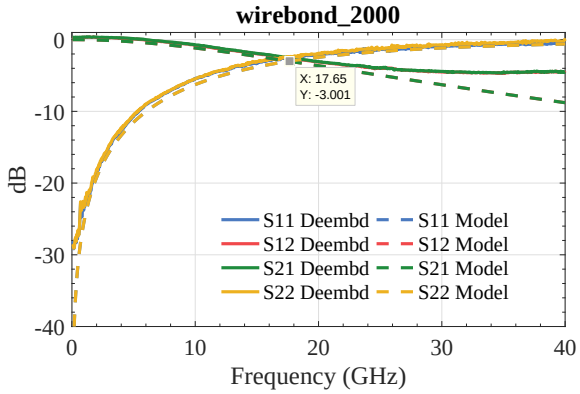

(H) Wirebond 1000.




(I) Wirebond 1200.




(J) Wirebond 1500.




(K) Wirebond 2000.

FIGURE 6.20: S-parameters of the de-embedded measurements and the extracted model of the GSG wirebonds.

## 6.6 Discussion

The almost perfect agreement bweteen the model and the measurements prove to us that wirebonds can be perfectly characterized with a simple lumped model as the one used. Furthermore, if we compare the results of "Wirebond 400" with the simulation done in Chapter 4, Example 4.2.3, we can see the similarity between the two results. Additionally, we know from Table 6.1 that the "Wirebond 400" must have a length longer than 475 $\mu$m because of its curved structure. As a matter of fact, if we look at the angled microscope photo of the "Wirebond 400" in Figure 1.1b, we recognize that the wirebonds must be longer than 475 $\mu$m and definitely shorter than 650 $\mu$m, which includes the length 500 $\mu$m that was simulated in Chapter 4. In conclusion, this finding indicates that the analytical expressions and simulations discussed in Chapter 4 do agree with the practical measurements. We can also see the similarity between the extracted inductance values and the theoretical counterpart of straight GSG wirebonds in Figure 6.21.

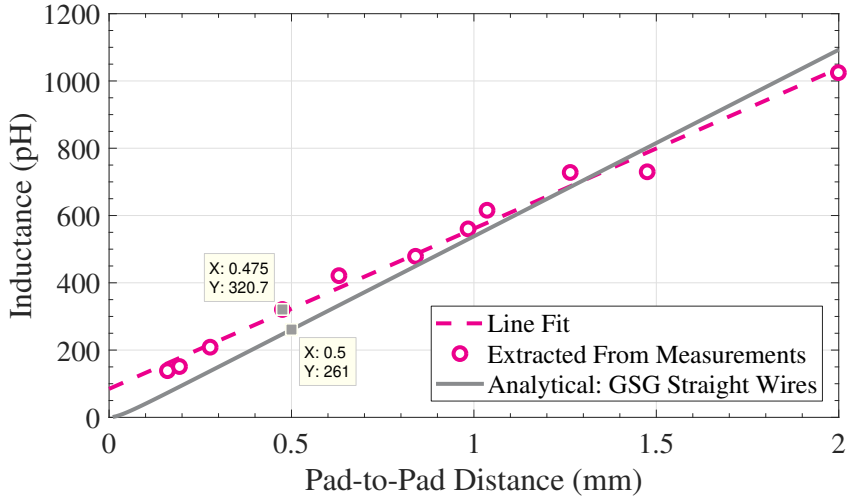



FIGURE 6.21: Extracted inductance as a function of pad-to-pad distance.

Due to wire looping, it is hard to say how long exactly the wirebonds are. Of course, we know that they are longer than the pad-to-pad distance, however, it is difficult to

say how much extra length the curved introduced. For the purpose of discussion, and to keep things simple, we assume the wirebonds are straight. From the obtained inductance values we can reverse calculate the length of the wirebonds using the analytical equations in Chapter 4. Figure 6.21 shows the inductance from Table 6.3 and its corresponding expected straight wire length.

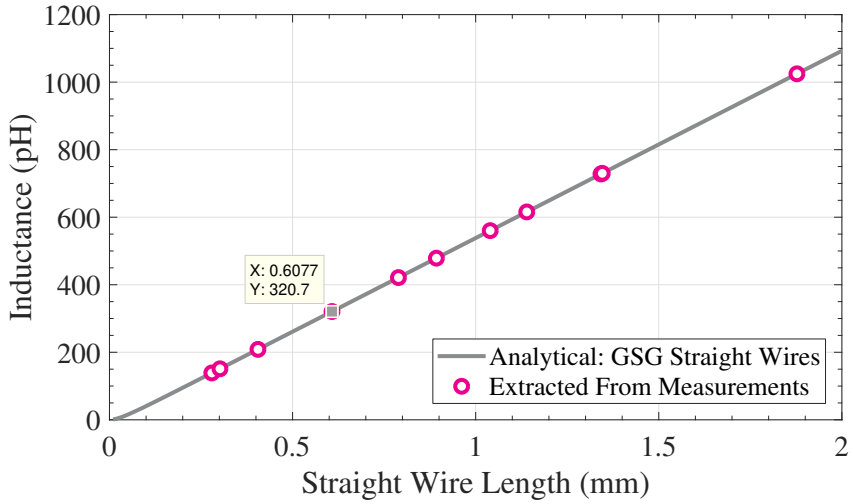



FIGURE 6.22: Expected straight wire length from the extracted inductance values.

Obliviously, the straight wire approximation presented in above figure is only valid for short wirebonds ($< 0.5\,\text{mm}$). An alternative and more accurate approach is to use Bezier curve modeling. The idea here is to formulate an optimization problem in which the objective is to find the parameters of the Bezier model that gives the most accurate inductance value given the extracted one. The cost function is defined as the error between the calculated inductance via the Neumann integrals and the extracted inductance from the measurements. For curious readers, MATLAB functions for the Neumann mutual and partial self-inductance are provided in Appendix B.

Another method to estimate the wirebonds length is to parametrically define the wirebonds in an EM simulator as Bezier curve and apply optimization to fit the simulation with the measured S-parameters.

# Chapter 7

# Conclusion

In this work, wirebond interconnects for the purpose of 2.5D integration of RF chips are investigated, from theory to practice. In conclusion, the main finding of this thesis is that GSG wirebonds demonstrate the optimal wirebonds implementation for RF 2.5D integration due to their low loop inductance. Additionally, based on simulation, using GSG ribbon bonds can provide even better performance. Alternatively, the characteristic impedance of the wires can be decreased by, e.g., increasing the mutual inductance by reducing the pitch distance, or increasing the distributed capacitance by covering the wires in epoxy.

## 7.1 Conclusion and Summary

Chapter 2 highlighted the process of wire bonding and explained how the two major wirebond technologies work (thermosonic and ultrasonic) and the tools used for each method. The discussion further went to cover wirebond technologies, which are suited for RF applications, i.e., ribbon bonding and fine pitch bonding. It turns out that ribbon bonding is the best option for RF interconnects. Chapter 3 briefed on 2.5D integration and discussed the importance of the technology for future advancement in the semiconductor industry, which was the main motivation for this thesis.

Beginning from Chapter 4, the focus went on finding analytical expressions and performing EM simulations to model wirebonds. Also, several examples were presented, which showed the agreement between the analytical solutions with EM simulations. One of the interesting aspects of modeling wirebonds is finding an appropriate geometric model. For that, the concept of spline curves was introduced. Specifically, the focus was on Bezier curve, which is versatile to model many wirebond shapes. By using Neumann integrals, the partial self-inductance of any wire shape can be accurately calculated, which is beneficial when combined with Bezier curve description to assess the performance of wirebonds without the need to perform an EM simulation. In the last section, GSG wirebonds were investigated with EM simulation and analytical formulas. The performance improvement that GSG wirebonds provide is of significant importance for interconnecting RF chips, as it provides low loop inductance, independent of chip thickness.

Chapter 5 started the discussion on how to measure wirebonds and how to apply optimization to extract models from port measurements. When measuring wirebonds we are not just measuring the wires themselves, but also parasitic of the bond pads.

We showed that by inverse matrix multiplication, one can eliminate the effects of the pads from the measurements. This process is called de-embedding, and two methods were presented. First method is the simplest one, which is measuring the part that we want to de-embed and convert its S-parameters into T- or ABCD-parameters and apply inverse operation and convert back to S-parameters. The second method is TOD (Thru-Only De-embedding), which was not used in this thesis for the lack of a thru structure of the pads. Even though this was not used in this thesis, it is still of an importance when trying to de-embed wirebonds on small pads. Last section of the chapter discussed the mathematics behind optimization formulation for fitting S-parameters measurements to an equivalent circuit model.

Chapter 6 presented the physical implementation of GSG wirebonds and their S-parameters measurements. Methods discussed in Chapter 5 were used to obtain a correct characterization of the wirebonds. The extracted model from the de-embedded measurements showed high agreement with the theory discussed in Chapter 4.

Overall, the main takeaway from this work is that GSG wirebonds are the best wirebond choice for RF interconnect in 2.5D integration applications, as they offer low loop inductance. Another aspect is the wire length. Keeping wirebonds as short as possible should be the primary objective, especially for RF chips. However, there are innovative solutions to reduce the inductance level of wirebonds, e.g., ribbon bonds or ultra fine bonding. Alternative, Using epoxy to increase the capacitance of GSG wirebonds can reduce the characteristic impedance $Z_0$.

## 7.2 Future Work

The major issue with wirebonds is their relative high inductance. When they are used in GSG configuration, they can be modeled as a transmission line. Because of the high inductance of the wires, the characteristic impedance of the line is also high. Now, assuming a lossless scenario, $Z_0$ is given by

$$Z_0 = \sqrt{\frac{L}{C}}. \tag{7.1}$$

For example, using 25 $\mu$m wirebonds and 100 $\mu$m pitch, $Z_0 \approx 150\,\Omega$. This value is considered very high for 50 $\Omega$ chips. Therefore, the question on hand is: how to reduce $Z_0$? From Eq. (7.1) we have two options: **1.** Reduce $L$ or **2.** Increase $C$. In the case of reducing $L$, this requires the physical modification of the wirebonds, e.g., ribbon bonds, or fine pitch bonding. However, in the case of increasing $C$, we can achieve that by modifying the dielectric constant around the wires, e.g., applying epoxy.

Another interesting topic is the estimation of the wirebond geometry from port measurements. The general idea is to use a parametric curve (e.g., Bezier) to model the wirebond, and then apply optimization methods to find the best curve parameters. The idea sounds simple, but the complexity of finding a unique solution requires a great attention to mechanics of wirebonds and the technology limitations. With such knowledge, one can impose constraints on the optimization, thus limiting the degree of freedom of the problem.

There are many other applications that can take advantage of wirebonds. For example, because newer technologies are using higher frequencies, it becomes possible

to assemble antennas via wirebonds on chips, hence “wirebond antennas”.

Lastly, while working on my thesis I learned a lot, from working with a bonder machine, to operating a wafer probe station. Overall, my journey with wirebonds will probably not end here, and I’m excited for what to come. For now, however, and with my current knowledge on wirebonds, I will say this: *When designing anything with wirebonds, make it your objective to keep the wirebonds as short as physically possible.*

# Appendix A

# Bézier Curve

The Bézier (or also written as Bezier) curve is a parametric curve which was first developed in the end of 1950s by Paul de Casteljau using numeric methods. In the early 1960s Pierre Bézier developed the notation and used the curve in mechanical Computer Aided Design (CAD). P. Bézier had popularized the curve, thus was named after him [30]. Nowadays, Bezier curves are ubiquitous and used in various vector graphic applications and CAD softwares, and even used for motion animation. For a comprehensive tutorial on Beizer curves, please refer to the online resource in [31].

## A.1 Definition

The Bezier curve is defined as a vector parametric polynomial of degree $n$, with $n+1$ 'control points'

$$\mathbf{B}(n,t) = \sum_{k=0}^{n} \binom{n}{k} t^k (1-t)^{n-k} \mathbf{P}_k, \qquad t \in [0,1], \tag{A.1}$$

where $\mathbf{B}(n,t) = [x(t),\ y(t),\ z(t)]^T$ is the parametric coordinates of the Bezier curve, and $\mathbf{P}_k = [x_k,\ y_k,\ z_k]^T$ is the $k$-th control point. Because the Bezier curve is mainly used in 2D applications, we can discard the $z$-coordinate. Figure A.1 depicts an example of a cubic Bezier curve, i.e., $n = 3$. By adjusting the control points we can control the shape of the curve. Furthermore, by increasing the polynomial order we can draw even more complex shapes.

The length of the curve can be computed by integrating an infinitesimal length segment over the span of the independent variable $t$.

$$l_B(n,\tau) = \int_0^{\tau} \left\| \frac{d\mathbf{B}(n,t)}{dt} \right\| dt, \qquad \tau \in (0,1]. \tag{A.2}$$

Generally, Eq. (A.2) has no closed form for $n > 2$, and we need to rely on numerical methods to approximate the curve length. A simple method is by discretizing Eq. (A.2)

$$l_B(n,M) \approx \sum_{i=0}^{M-1} \left\| \mathbf{B}(n,t_{i+1}) - \mathbf{B}(n,t_i) \right\|, \qquad t_i \in [0,1],\ \forall\, i \in [0,M). \tag{A.3}$$

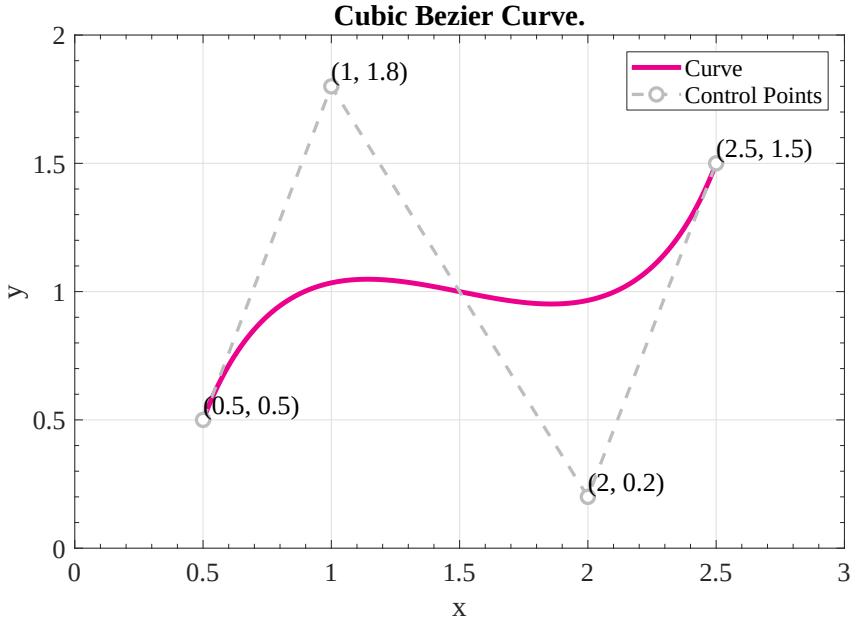



FIGURE A.1: Example of cubic 2D Bezier curve.

The quality of the approximation in Eq. (A.3) depends on how the variable $t$ is discretized and how many samples are used (i.e., $M$).

## A.2 The Quadratic Form

The quadratic form of the Bezier curve (i.e., $n = 2$) is very useful for modeling shapes that have concave or convex structure. The parametric equation for this case is given by

$$\mathbf{B}(t) = (1-t)^2\mathbf{P}_0 + 2(1-t)t\mathbf{P}_1 + t^2\mathbf{P}_2, \qquad t \in [0,1], \tag{A.4}$$

where $\mathbf{P}_0$ and $\mathbf{P}_2$ are the start and endpoints, respectively, and $\mathbf{P}_1$ is the control point with which we can control the shape of the curve. Figure A.2 plots Eq. (A.4) in 2D and indicate the location of the control points.

As mentioned in previous section, up to $n = 2$, there exist a closed form for the curve length. We derive this closed form equation for the 2D case. We first start with derivative terms, which are written as

$$\mathbf{B}'(t) = 2(\mathbf{P}_0 - 2\mathbf{P}_1 + \mathbf{P}_2)t + (2\mathbf{P}_1 - 2\mathbf{P}_0) \tag{A.5}$$

The total curve length is then calculated following Eq. (A.2)

$$l_B = \int_0^1 \left\|\mathbf{B}'(t)\right\| dt = \int_0^1 \sqrt{B'_x(t)^2 + B'_y(t)^2}\, dt = \int_0^1 \sqrt{At^2 + Bt + C}\, dt, \tag{A.6}$$

where the constants $A$, $B$, and $C$ are defined as

$$\begin{aligned} A &= 4(a_x^2 + a_y^2); \quad B = 4(a_x b_x + a_y b_y); \quad C = b_x^2 + b_y^2 \\ a_x &= x_0 - 2x_1 + x_2; \quad a_y = y_0 - 2y_1 + y_2 \\ b_x &= 2(x_1 - x_0); \qquad b_y = 2(y_1 - y_0), \end{aligned} \tag{A.7}$$

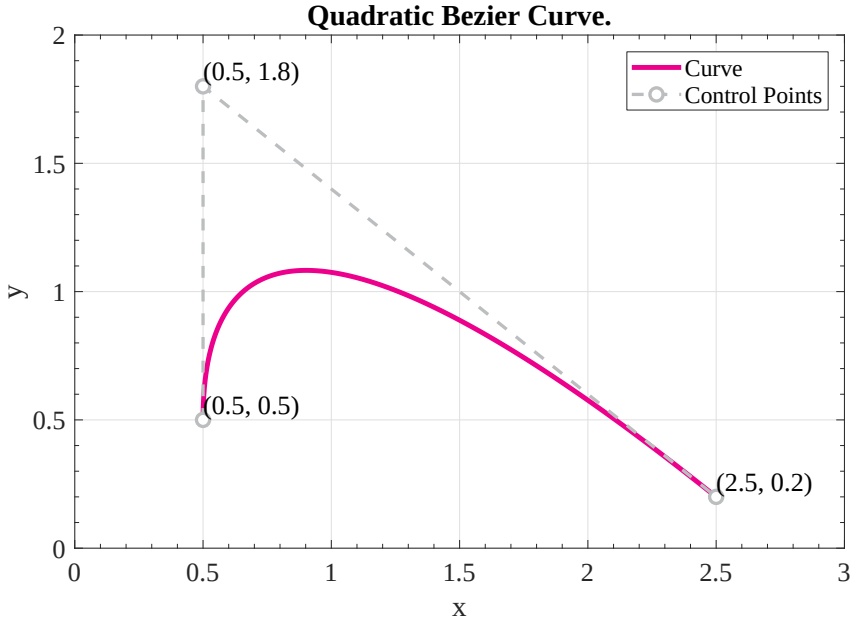



FIGURE A.2: Example of quadratic 2D Bezier curve.

where $x_i$ and $y_i$ are the coordinate of the $i$-th point $\mathbf{P}_i$ (start, end, and control points). The solution of the integral of the form of Eq. (A.6) can be found in [32, Sec. 2.26], which reads

$$\int_0^1 \sqrt{At^2+Bt+C}\,dt = \left[\frac{(2At+B)\sqrt{At^2+Bt+C}}{4A} + \cdots \right. \\ \left. \cdots \frac{4AC-B^2}{8A\sqrt{A}} \sinh^{-1}\left(\frac{2At+B}{\sqrt{4AC-B^2}}\right)\right]_0^1. \quad \text{(A.8)}$$

Thus, by evaluating the boundaries, we obtain the total length of the quadratic Bezier curve

$$l_B = \frac{(2A+B)\sqrt{A+B+C}-B\sqrt{C}}{4A} + \cdots \\ \cdots \frac{4AC-B^2}{8A\sqrt{A}}\left[\sinh^{-1}\left(\frac{2A+B}{\sqrt{4AC-B^2}}\right) - \sinh^{-1}\left(\frac{B}{\sqrt{4AC-B^2}}\right)\right]. \quad \text{(A.9)}$$

# Appendix B

# Matlab Scripts

## B.1 Lumped Element of Wires

### B.1.1 Self-Inductance via Neumann Integral

```
function [L, l] = neumannSelf2D(x,y,r)
    % This function computes the partial self inductance of wire in 2D.
    % The method of calculation assumes full skin effect, i.e., current is
    % flowing on the surface.
    % Although this script can only do 2D, it should be easy to modify it
    % to include the z-axes.

    mu0 = 1.25663706e-6;
    x = x(:);
    y = y(:);

    dx = diff(x);
    dy = diff(y);

    dl = sqrt(dx.^2 + dy.^2);     % segments length
    l = sum(dl);                  % total length

    ratio =  dl/r;
    numGood = sum(ratio < 0.6);  % number of short segments (good)
    numBad = sum(ratio >= 0.6);  % number of long segments (bad)

    fprintf('Wire total length approx: %g\n', l)
    fprintf('Max length of a segment: %g\n', max(dl))
    fprintf(['Ratio of max segment length to wire radius: %g'...
        '(less than 0.6 is good)\n'], max(dl)/r)
    fprintf('Good segments (<0.6): %g; Bad segments (>=0.6): %g\n',...
        numGood, numBad)

    % 0.6 seems to be a good threshold (based on experimenting)
    if max(dl)/r > 0.6
        warning(['The ratio of max segment length to wire radius is'...
            'greater than 0.6. This can impact the solution accuracy.'])
    end
    if numGood <= numBad
        warning(['number of Good segments (<0.6) are less than bad'...
            'segments (>=0.6). Increase the sample rate to improve this!'])
```

```
    end

    % center points of segments
    xcen = movmean(x,2);
    xcen = xcen(2:end);
    ycen = movmean(y,2);
    ycen = ycen(2:end);

    % defining the second wire by shifting the original in the normal
    % direction by the value r.
    nnn = r*[-dy dx]./sqrt(sum([-dy dx].^2,2));
    xcen2 = xcen + nnn(:,1);
    ycen2 = ycen + nnn(:,2);

%     % using loops to perform the integral (very slow)
%     for inx1 = 1:(length(xcen))
%         for inx2 = 1:(length(xcen))
%             v1 = [xcen(inx1) ycen(inx1)]';
%            dv1 = [dx(inx1) dy(inx1)]';
%             v2 = [xcen2(inx2) ycen2(inx2)]';
%            dv2 = [dx(inx2) dy(inx2)]';
%            intag(inx1,inx2) = (dv1'*dv2)/norm(v1-v2);
%         end
%     end

    % Matrix multiplication to perform the integral
    % (very fast, but it takes lots of memory)
    [XX, YY] = meshgrid(xcen,ycen);
    [XX2, YY2] = meshgrid(xcen2,ycen2);
    [dXX, dYY] = meshgrid(dx,dy);
    intag = (dXX.*dXX' + dYY.*dYY')./sqrt((XX2-XX').^2 + (YY2'-YY).^2);
    L = (mu0/4/pi)*sum(intag(:));

end
```

### B.1.2 Mutual Inductance via Neumann Integral

```
function M = neumannMutual2D(x1,y1,x2,y2)
    % Implementation of neumann integral to compute
    % mutual inductance between 2 wires in 2D

    mu0 = 1.25663706e-6;
    x1 = x1(:);
    y1 = y1(:);
    x2 = x2(:);
    y2 = y2(:);

    dx1 = diff(x1);
    dy1 = diff(y1);
    dx2 = diff(x2);
    dy2 = diff(y2);

    % center points of segments
    xcen1 = movmean(x1,2);
    xcen1 = xcen1(2:end);
    ycen1 = movmean(y1,2);
```

```
    ycen1 = ycen1(2:end);
    xcen2 = movmean(x2,2);
    xcen2 = xcen2(2:end);
    ycen2 = movmean(y2,2);
    ycen2 = ycen2(2:end);

    % Matrix multiplication to perform the integral
    % (very fast, but it takes lots of memory)
    [XX1, YY1] = meshgrid(xcen1,ycen1);
    [XX2, YY2] = meshgrid(xcen2,ycen2);
    [dXX1, dYY1] = meshgrid(dx1,dy1);
    [dXX2, dYY2] = meshgrid(dx2,dy2);
    intag = (dXX1.*dXX2' + dYY1.*dYY2')./sqrt((XX2-XX1').^2 + ...
        (YY2'-YY1).^2);
    M = (mu0/4/pi)*sum(intag(:));

end
```

### B.1.3 Wire Capacitance to Ground plane

```
function [C] = wireCapGNDPlane(x,y,r,er,ref)
    % capacitance of wire above ground plane, 2D

    % x and y need to have the same length
    x = x(:);
    y = y(:);
    if nargin < 5
        ref = 0;
    end
    if nargin < 4
        ref = 0;
        er = 1;
    end
    e0 = 8.8541878128*1e-12;

    ycen = movmean(y,2);
    ycen = ycen(2:end);
    h = ycen-ref;
    dx = diff(x);
    dy = diff(y);
    dl = sqrt(dx.^2 + dy.^2);

    C = 2*pi*e0*er*sum(dl./acosh(h./r));

end
```

### B.1.4 Wire DC Resistance

```
function R = wireRDC(x,y,r,sigma)
    % DC resistance of wire 2D

    if nargin < 4
        % gold
```

```
        sigma = 4.11e7;
    end
    x = x(:);
    y = y(:);

    A = pi*r^2;

    dx = diff(x);
    dy = diff(y);
    dl = sqrt(dx.^2 + dy.^2);
    l = sum(dl);
    R = l/A/sigma;

end
```

## B.2 2-Port Parameters Conversion

### B.2.1 S <—> ABCD

```
function S = ABCD2S(ABCD, Z0)

    if nargin < 2
        Z0 = 50;
    end

    A = ABCD(1,1);
    B = ABCD(1,2);
    C = ABCD(2,1);
    D = ABCD(2,2);
    S = [A+B/Z0-C*Z0-D, 2*(A*D-B*C);...
    2, -A+B/Z0-C*Z0+D]/(A+B/Z0+C*Z0+D);

end
```

```
function ABCD = S2ABCD(S, Z0)

    if nargin < 2
        Z0 = 50;
    end

    ABCD = [(1+S(1,1))*(1-S(2,2))+S(1,2)*S(2,1), Z0*( ...
        (1+S(1,1))*(1+S(2,2)) - S(1,2)*S(2,1));...
    (1/Z0)*((1-S(1,1))*(1-S(2,2))-S(1,2)*S(2,1)), ...
        (1-S(1,1))*(1+S(2,2))+S(1,2)*S(2,1)]/(2*S(2,1));

end
```

### B.2.2 S <—> T

```
function S = T2S(T)

    S = [T(1,2) det(T); 1 -T(2,1)]/T(2,2);
```

```
end
```

```
function T = S2T(S)

    T = [-det(S) S(1,1); -S(2,2) 1]/S(2,1);

end
```

### B.2.3 S <—> Z

```
function [S] = Z2S(Z,Z0)

    if nargin < 2
        Z0 = 50;
    end

    Z11 = Z(1,1);
    Z21 = Z(2,1);
    Z12 = Z(1,2);
    Z22 = Z(2,2);
    S = [(Z11-Z0)*(Z22+Z0)-Z12*Z21, 2*Z12*Z0;...
        2*Z21*Z0, (Z11+Z0)*(Z22-Z0)-Z12*Z21]/((Z11+Z0)*(Z22+Z0)-Z12*Z21);
end
```

```
function [Z] = S2Z(S,Z0)

    if nargin < 2
        Z0 = 50;
    end

    S11 = S(1,1);
    S21 = S(2,1);
    S12 = S(1,2);
    S22 = S(2,2);
    Z = Z0*[(1+S11)*(1-S22)-S12*S21, 2*S12;...
        2*S21, (1-S11)*(1+S22)+S12*S21]/((1-S11)*(1-S22)-S12*S21);
end
```

### B.2.4 S <—> Y

```
function [S] = Y2S(Y,Y0)

    if nargin < 2
        Y0 = 1/50;
    end

    Y11 = Y(1,1);
    Y21 = Y(2,1);
    Y12 = Y(1,2);
    Y22 = Y(2,2);
    S = [(Y0-Y11)*(Y0+Y22)+Y12*Y21, -2*Y12*Y0;...
```

```
        -2*Y21*Y0, (Y0+Y11)*(Y0-Y22)+Y12*Y21]/((Y0+Y11)*(Y0+Y22)-Y12*Y21);
end
```

```
function [Y] = S2Y(S,Y0)

    if nargin < 2
        Y0 = 1/50;
    end

    S11 = S(1,1);
    S21 = S(2,1);
    S12 = S(1,2);
    S22 = S(2,2);
    Y = Y0*[(1-S11)*(1+S22)+S12*S21, -2*S12;...
        -2*S21, (1+S11)*(1-S22)+S12*S21]/((1+S11)*(1+S22)-S12*S21);
end
```

## B.3 Implementation of Bezier Curve

```
function B = bezier(n,t,P)
% Implementation of Bezier curve.

    t = t(:)';

    % check if t within [0,1]
    if ~((all(t <= 1)) && (all(t >= 0)))
        error('t is not in the valid range, i.e., t = [0,1].')
    end

    % check if P has the correct dimensions
    if ~all(size(P) == [3 n+1])
        error('Your P matrix does not have the correct dimensions!')
    end

    B = zeros(3,1);
    for k = 0:n
        B = B + nchoosek(n,k).*(t.^k).*(1-t).^(n-k).*P(:,k+1);
    end
end
```

## B.4 Arc Length of Quadratic Bezier Curve

```
function L = QBLength2D(x0,x1,x2,y0,y1,y2)
    % arc length of quadratic Bezier curve.

    ax = x0 - 2*x1 + x2;
    ay = y0 - 2*y1 + y2;
    bx = 2*x1 - 2*x0;
    by = 2*y1 - 2*y0;
    A = 4*(ax^2 + ay^2);
    B = 4*(ax*bx + ay*by);
```

```
    C = bx^2 + by^2;

    L = ((2*A+B)*sqrt(A+B+C) -B*sqrt(C))/4/A + (4*A*C-B^2)/8/A/sqrt(A)*...
        (asinh((2*A+B)/(sqrt(4*A*C-B^2)))- asinh(B/(sqrt(4*A*C-B^2))));

end
```

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