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An Ultra-Low Power Oscillator for RFID Transponder ICs in a 40nm CMOS Technology

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Abstract

UHF radio frequency identification (RFID) technology enables a communication with low-cost passive UHF RFID transponders and is thus used in a variety of fields. Since a passive UHF RFID transponder does not use a battery, the available power to supply a UHF RFID transponder IC is limited to a few μW, which constrains the overall circuit complexity. UHF transponders use a local oscillator for data decoding and encoding for the communication with an interrogator. Since the power budget is very small, a low power consumption of the oscillator is critical.

In this thesis, different ultra-low power oscillators in a 40-nm CMOS technology for RFID transponder ICs are discussed. The oscillators run with a frequency of 1.3 MHz and use a supply voltage of 600 mV. Three different oscillator topologies are compared with respect to temperature behaviour, power consumption, process and mismatch variations, phase noise and power supply rejection. The most promising oscillator topology is complemented by a frequency trimming circuit and is implemented in layout.

Post-layout simulations of the oscillator including the trimming circuit, reveal a current consumption of 135 nA and a temperature drift of the frequency of less than 250 ppm/°C over a temperature range of -40 °C to 85 °C. The overall frequency deviation due to process and mismatch variations is less than 5 % and the needed layout area equals 1500 μm^2.

Keywords - ultra-low power, low voltage, clock generator, CMOS integrated circuits, ring oscillator, relaxation oscillator

Kurzfassung

UHF-Radiofrequenz-Identifikations-Technologie (RFID) ermöglicht eine Kommunikation mit preisgünstigen passiven UHF-RFID-Transpondern und wird daher in vielen Bereichen eingesetzt. Der Leistungsverbrauch eines passiven RFID Transponder ICs ist auf einige μW beschränkt, da dieser keine eigene Batterie zur Versorgung besitzt. UHF Transponder besitzen einen lokalen Oszillator der für die Dekodierung und Kodierung während der Kommunikation mit einem Lesegerät verwendet wird. Aufgrund der limitierten Versorgungsleistung, ist es notwendig, dass der Oszillator einen geringen Leistungsverbrauch aufweist.

Diese Arbeit untersucht verschiedene Ultra-Low-Power-Oszillatoren für RFID-Tranponder-Chips in einer 40-nm CMOS Technology. Die Oszillatoren laufen mit einer Frequenz von 1.3 MHz und werden mit einer Spannung von 600 mV versorgt. Drei Oszillatortopologien werden bezüglich Temperaturverhalten, Leistungsaufnahme, Prozess- und Mismatch-Variationen, Phasenrauschen und Versorgungspannungsunterdrückung untersucht. Auf Basis der gewonnen Ergebnisse, wird ein Oszillator ausgewählt, um eine Trimmschaltung ergänzt und im Layout umgesetzt.

Post-Layout-Simulation zeigen, dass der Stromverbrauch bei 135 nA liegt und die Frequenzabweichung unter 250 ppm/°C, über einen Temperaturebereich von -40 °C bis 85 °C, liegt. Die absolute Frequenzabweichung beträgt weniger als 5 % und die Layout-Fläche beträgt 1500 μm^2.

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Chapter 1

Introduction

Radio frequency identification (RFID) systems include two main components. First, a transponder and second a reader. The transponder is a small storage device which typically stores an identification number, with an antenna to communicate with a reader. Transponders can be mounted on objects and their geometry is adjusted to applications. Passive RFID transponders do not have their own supply but are driven by the electromagnetic field of the reader. The reader emits an electromagnetic field and a transponder within range modulates this field in order to communicate with the reader. For the data exchange different communication standards are used. The used standard depends on the application and the operation mode of the RFID system [4].

For RFID systems there is a variety of different implementations including full-duplex, half-duplex and sequential. If the application uses a full-duplex or half-duplex mode the response of the transponder is transmitted while the reader field is on. The communication from the transponder to the reader is achieved by load modulation [4].

Besides full and half duplex mode, there is also a sequential mode where the field of the reader is periodically switched off for a short time. These gaps are recognized by the transponder and used to send its data to the reader. A drawback of this method is that the transponder needs decoupling capacitors in order to avoid power supply problems during the field gaps [4].

Data rates of RFID transponders reach from a few bits/s until several hundred kilo-bits/s. An exception are the so called 1-bit transponders because they just use 1-bit in order to determine whether a transponder is in the field or not. This type is used in shops. When someone tries to leave the shop with a good, which still has the transponder attached to it, then an alarm is triggered [4].

Another distinguishing characteristic of RFID systems is the programmability of the transponder. When very simple systems are used, the programming of the transponder (e.g. serial

number) is already taking place during the manufacturing process and cannot be changed anymore afterwards. In contrast programmable transponders can be reprogrammed by the reader by sending certain commands [4].

An important characteristic of RFID systems is the power supply. Passive transponders do not have their own supply. They are supplied by the energy of the electromagnetic field emitted by the reader. Active transponders use a battery in order to supply the chip.

A further differentiating characteristic is the operating frequency and hence the operating distance. The operating frequency is the transmission frequency of the reader. The different transmission frequencies are grouped into four domains [4]:

- Low frequency (LF) 30 kHz ... 300 kHz
- High frequency (HF) respectively radio frequency (RF) 3 MHz ... 30 MHz
- Ultra high frequency (UHF) 300 MHz ... 3 GHz
- Microwave $>$ 3 GHz

Additionally, there is a classification between close-coupling (0..1 cm), remote coupling (0..1 m) and long range systems ($>$ 1 m).

The data transmission from transponder to reader can be grouped in categories [4]:

- Backscatter modulation:
  The frequency of the reflected wave is the same as the transmission frequency of the reader.
- Load modulation:
  The field of the reader is changed (modulated) by the transponder. The frequency does not change.

Nowadays, RFID systems are used in a variety of fields. Since 2006 Austria is using passports with RFID chips to identify persons. Furthermore, RFID transponders are also used in the daily live for public transport tickets [5, 6] or in ski resorts for lift tickets [7].

In the 1990s first pilot projects for the usage of HF RFID transponders in public transport were launched. Since then contactless smart cards have gained a wide spread usage in this area [5, 6].

However, HF RFID technologies are limited in range and hence different RFID technologies are investigated in order increase user comfort. An alternative for HF RFID system are UHF systems because they allow an increased operating range [8]. With UHF systems a transaction between a transponder and a reader could be performed without an action

of the user.

1.1 UHF RFID systems

UHF RFID systems operate at a frequency of 860 MHz and 960 MHz and fall into the category of so called long-range systems ($>$ 1 m) [4].

Fig. 1.1 depicts the operating principle of passive UHF RFID systems. UHF transponders operate mainly in the far-field of reader antennas and hence they include a resonating antenna that allows the efficient emission and reception of electromagnetic waves [7].

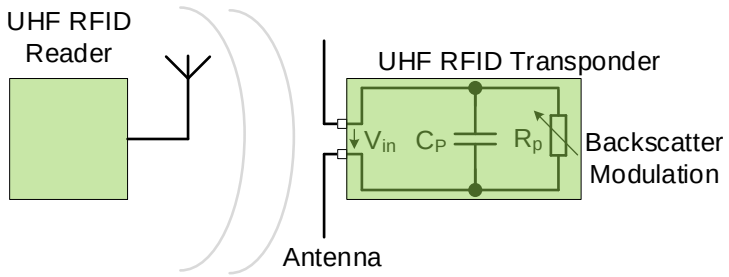

Figure 1.1: Operating principle of passive UHF RFID systems

Passive UHF RFID systems have the advantage that they are cheaper and they have a longer lifetime compared to active UHF RFID systems [4]. Especially the low costs enable a large scale implementation of passive UHF RFID technologies in cost sensitive applications such as supply chain management [4]. The most important communication standards are the ISO/IEC 18000-63 [9] and EPC Generation-2 [1] UHF RFID standard. Since passive UHF RFID transponders are implemented in a variety of fields certain standards including ISO/IEC 18000-63 and EPC Generation-2 were established. State of the art transponders are able to achieve communication ranges above 10 m, but it strongly dependants on the specific operating conditions such as the material to which the tag is attached to [7]. A passive UHF RFID transponder IC is supplied entirely by the RF power impinging upon the transponder antenna. Hence, a transponder IC with a high sensitivity is required in order to achieve a high reader range. The sensitivity of a passive transponder IC is directly linked to the DC power consumption of its core circuitry. The available power for supplying a highly sensitive transponder IC is limited to a few μW [10, 11].

Fig. 1.2 depicts a block diagram of an UHF transponder IC. The antenna is connected between the terminals RF1 and RF2. After an RFID signal is received, it is demodulated by the demodulator. The UHF charge pump converts the voltage level of the impinging signal to the DC supply voltage VDDA for the transponder chip. VDDA is limited by a

limiter in order to avoid overvoltage stress at connected circuits. A low drop-out (LDO) regulator takes VDDA as input and provides a defined output voltage VDDD. VDDD is used as supply voltage for bias generation, digital part, oscillator and non-volatile memory. The bias generation provides bias currents. The oscillator generates a clock signal, which is used by the digital part for encoding and decoding during the communication.

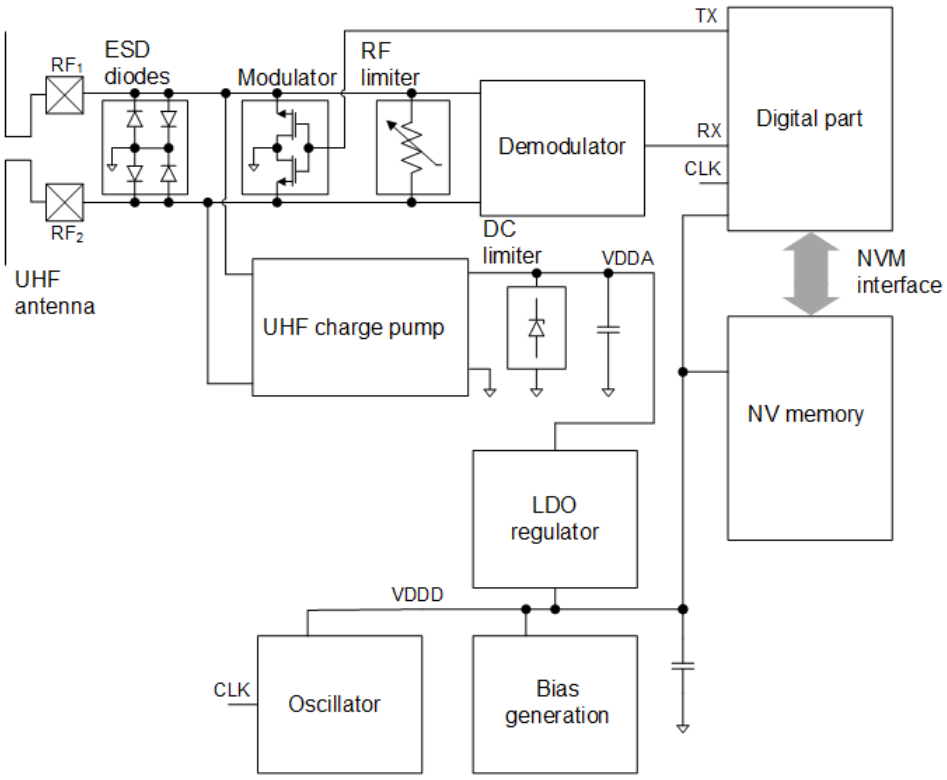

Figure 1.2: Block diagram of a UHF RFID transponder

The majority of present UHF RFID systems are based on the EPC Generation-2 UHF RFID standard which specifies a communication protocol for an RFID interface, operating from 860 MHz to 960 MHz [1]. The specific operating bands for a certain country are defined by local regulations like in [12, 13].

1.1.1 EPC Generation-2 UHF RFID standard

The EPC Genereation-2 UHF RFID standard defines the requirements for the digital control unit which is embedded in the transponder IC [14]. The control unit uses a clock signal for synchronisation in order to allow precise coding and decoding of data [14]. For compliance with the codification tolerances defined in the EPC Generation-2 UHF RFID standard, the clock signal must have a minimum frequency of 1.28 MHz, as investigated in [15]. Using a clock signal with the smallest possible clock frequency minimizes the power

consumption of the clock generator. Furthermore, it also minimizes the power consumption of the digital circuitry.

Decoding

The EPC Generation-2 UHF RFID standard defines the usage of pulse-interval encoded (PIE) symbols for the forward link (reader to transponder). The length of the symbols is defined by the reader with the Tari value which can range from 6.25 μs to 25 μs. At the beginning of a communication the reader sends a preamble, to define RTcal for the forward link and TRcal for the backlink. RTcal is equal to the length of data-0, plus the length of data-1 [1]. Symbols shorter than the RTcal/2 value correspond to data-0 and symbols longer than the RTcal/2 value correspond to data-1. Fig. 1.3 depicts the symbols representing logical data-0 and data-1.

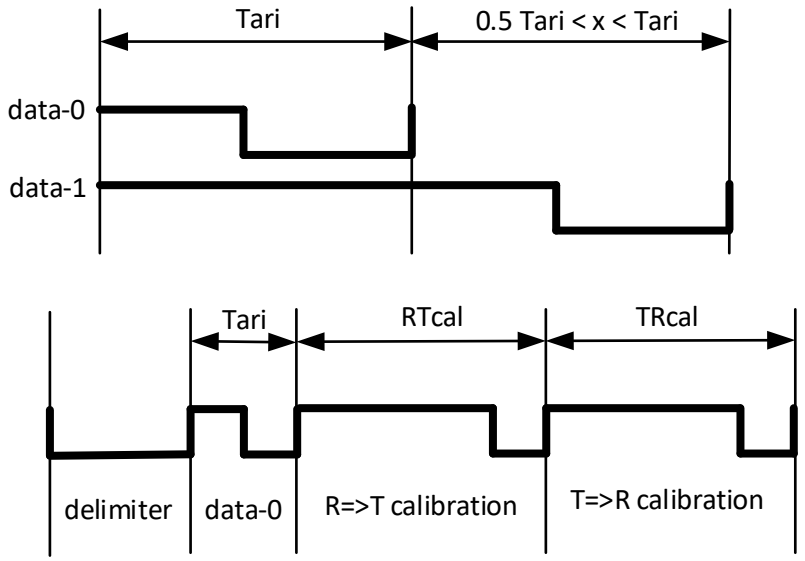

Figure 1.3: Pulse-interval encoded data and preamble [1]

Encoding

The backlink from transponder to reader is established by using backscatter modulation. The transponder chip switches its reflection coefficient with reference to the antenna impedance between to states [1].

The EPC Generation-2 standard defines two different encoding types. The first one is called bi-phase space encoding (FM0) baseband modulation. FM0 inverts the phase at the beginning of each symbol and data-0 symbols have an additional phase inversion in the middle [1]. Besides FM0 baseband modulation EPC Generation-2 defines an encoding scheme using a Miller modulated sub-carrier. Miller modulation inverts the phase between to consecutive data-0 symbols. An additional phase inversion takes place in the middle of data-1 symbols [1].

The frequencies for the backlink range from 40 kHz to 640 kHz [1] and it is also set by the reader by means of the preamble. The reader defines the backscatter-link frequency (BLF) by using TRcal (see Fig.1.3) and a divide ratio (DR).

$$BLF = \frac{DR}{TRcal} \tag{1.1}$$

Depending on the BLF different tolerances ranging from 4% to 22% are defined [1]. To be compliant with the BLF tolerances a minimum system frequency of 1.28 MHz is required as reported in [15].

1.2 Literature review

In literature, various circuits are reported for generating a clock signal for a passive UHF RFID transponder. In [16], Baghaei-Nedjad et al. presented a method to extract a clock signal from the 860 MHz to 960 MHz RF signal by using injection-locked dividers. Their approach does not include a local oscillator, but it is very power costly due to the high frequency part of the circuitry which derives the clock signal from the 960 MHz carrier.

A different approach is the implementation of local oscillators. There are different oscillator topologies available including ring and relaxation oscillators. Ring oscillators use an odd number of stages to achieve an unstable behaviour of the loop output [17]. A variety of literature about ring oscillators is already available including the work reported in [18, 19, 20]. An ordinary current controlled ring oscillator as reported in [21], suffers from a strong temperature dependency, hence a compensation mechanism must be implemented. In [18], an additional temperature and process compensation circuit is introduced, to compensate temperature and process variations of the oscillator core. The design combines two complementary temperature coefficients resulting in a temperature stable behaviour.

Another ring oscillator design was presented in [22]. This design focuses on ultra-low power operation. In difference to [18, 19, 20], just two delay stages are used to generate a stable clock signal. As elaborated, its frequency is tuneable and it can operate at very low supply voltages (< 1 V).

Another oscillator type found in literature is the relaxation oscillator like reported in [2, 23, 24, 25]. Here, the clock is generated by charging and discharging a reference capacitor. The clock generator presented by Denier in [2] combines different temperature coefficients to achieve a very good temperature behaviour of the oscillator output. Furthermore, it is possible to run the oscillator with a supply voltage lower than 1 V.

1.3 Scope

The clock generation is a crucial block of an RFID transponder chip, since it is used for data decoding and encoding during a communication. This thesis considers three ultra-low power oscillators for UHF RFID transponder chips, which are suitable for an operation at supply voltages lower than 1 V. The oscillators were designed for a nominal frequency of 1.312 MHz to assure compliance with the EPC Generation-2 standard. The oscillator frequency variation has to be lower than 10 % with respect to process and mismatch variations over a temperature range from -40 °C to 85 °C.

The first investigated oscillator topology is a ring oscillator using a switched-capacitor feedback control, which has been published in [26]. The design includes a switched-capacitor circuit to convert the output frequency to a voltage signal.

The second oscillator topology is a ring oscillator with integrated temperature compensation. The oscillator topology is based on an existing circuit, which was designed by Robert Entner in an older CMOS technology. The oscillator uses different complementary MOS transistor types in the individual delay stage, to compensate temperature shifts of the transistor threshold voltages.

The third considered circuit topology is a relaxation oscillator, which has been previously published in [2]. The reported design in [2], is implemented in a 0.35-μm CMOS technology and has a nominal frequency of 3.3 kHz. The circuit includes a reference voltage generation with a positive temperature coefficient to compensate temperature shifts of the pulse-generating logic. A current comparator is used to control the pulse-generating logic, which allows a low power consumption.

The three oscillator circuits are implemented in a 40-nm CMOS technology and investigated concerning the power consumption, temperature behaviour, process and mismatch variations, frequency controllability, phase noise, and power supply rejection. The parameter comparisons are based on initial circuit designs with estimated layout parasitics. The relaxation oscillator showing the best performance furthermore has been implemented in layout and is verified by means of layout-extracted simulations.

The oscillator specifications are summarized in Table 1.1. In addition, the oscillator must be able to change the frequency between ±5 % in 5 defined steps.

Environmental specifications	Unit	Min.		Max.
Junction temperature	°C	-40		85
DC specifications				
Bias current	nA	6.25	12.5	18.75
Current consumption	nA		140	
Transient specifications				
Frequency	MHz	1.18	1.312	1.443
Duty cycle	%	49	50	51
Frequency variation				
during backscatter modulation	%	-1.5		1.5
RMS value of period jitter	ns			2.7
Frequency settling time	μs			10
Area	μm^2			1500

Table 1.1: Oscillator specifications

1.4 Outline

In Ch. 2, different oscillator topologies are reviewed, starting by deriving the frequency defining parameters. After finding an expression for the frequency, considerations about the temperature coefficients of the frequency defining parameters and their impact on the output frequency are carried out. As a next step, the influence of noise and supply disturbances on the frequency is investigated. Finally, a comparison between the investigated oscillators is shown.

The focus in Ch. 3 is on the implementation of the oscillators in a 40-nm CMOS technology. Simulation results on the frequency variations with respect to temperature, process and mismatch variations, noise and supply disturbances, build the basis for deciding which circuit topology to implement finally. As a next step, two frequency trimming circuits are presented for compensating process and mismatch variations. Finally, the circuit layouts of the oscillator and trimming circuit are discussed.

Ch. 4 shows the verification results for the extracted layout simulations. The results include temperature drift, power consumption, process and mismatch variations, noise and power supply rejection. Finally, the results are compared with previously reported oscillator designs.

Chapter 2

Oscillator topologies

The previous chapter aimed for an understanding of the basic blocks of a UHF transponder. Furthermore, an introduction on the UHF communication standard was given in order to get an idea why the oscillator is such a crucial block of a transponder chip.

In this chapter, theoretical considerations for three ultra-low power oscillators are presented. A major topic is the temperature variation of the oscillator output frequency. Three different temperature compensation techniques are investigated including a switched-capacitor feedback structure and a compensation of the threshold voltage temperature variations.

2.1 Ring oscillator with switched-capacitor feedback

Ring oscillators can be implemented in different ways, since the output frequency depends on the delay introduced by several cascaded gain stages. One way to control the delay is to control the amount of current available for charging and discharging the capacitive load of each stage. Fig. 2.1 depicts a standard current-starved ring oscillator structure as discussed in [18, 19, 20].

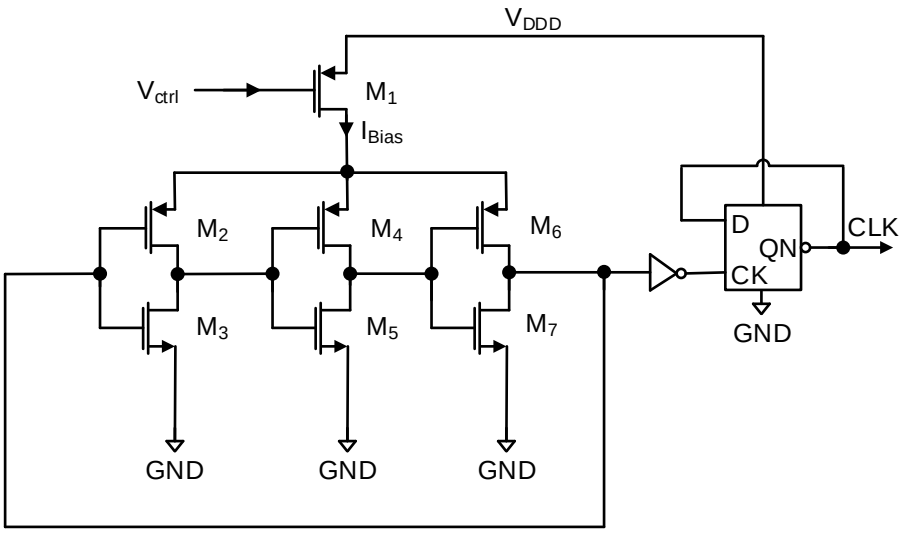

Figure 2.1: Three-stage ring oscillator

The current through each stage, hence the delay can be controlled by M_1. Transistors M_2 to M_7, form the three delay stages necessary for an oscillation. By assuming all three delay stages are identical, the delay of one stage can be expressed by [27]

$$T_d = \frac{C_p \cdot (V_{DDD} - V_{dsp})}{I_{Bias}}, \tag{2.1}$$

where C_p is the parasitic capacitance at the output of the stage, V_{dsp} is the drain-source voltage of $M_2,\ M_4,\ M_6$. Furthermore, I_{Bias} is the bias current and can be expressed by

$$I_{Bias} = \frac{\mu C_{ox}}{2}\frac{W_1}{L_1}(V_{DDD} - V_{ctrl} - V_T)^2, \tag{2.2}$$

where μ is the electron mobility, C_{OX} is the capacitance of the oxide layer, W is the transistor width, L is the transistor length, V_{DDD} is the supply voltage, V_{ctrl} is the gate voltage of M_1 and V_T is the threshold voltage.

By combining (2.1) and (2.2), the oscillator frequency can be expressed as a function of V_{ctrl}

$$f = \frac{1}{3 \cdot T_d} = \frac{I_{Bias}}{3 \cdot C_p \cdot (V_{DDD} - V_{dsp})} = \frac{\frac{\mu C_{ox}}{2}\frac{W_1}{L_1}(V_{DDD} - V_{ctrl} - V_T)^2}{3 \cdot C_p \cdot (V_{DDD} - V_{dsp})}. \tag{2.3}$$

In order to maintain a constant frequency over temperature, V_{ctrl} must track the oscillator output frequency. Fig. 2.2 depicts a switched-capacitor feedback structure which enables a tracking of the output frequency, using the principle of frequency to voltage conversion

as described in [26]. As one can see from (2.4), the voltage V_C is proportional to the frequency. V_C is compared with a reference voltage and the output (V_{ctrl}) is used to control the transistor M_1. The averaged voltage across C can be approximated by

$$V_C = \frac{1}{f \cdot C} I_B, \tag{2.4}$$

where f is the oscillator frequency, C is the switched-capacitor and I_B is the bias current of the frequency-to-voltage converter.

Table 2.1 includes all the key parameters for the switched-capacitor feedback loop. The reference voltage V_{ref} is generated by a resistor. It is not useful to use resistors bigger than a few MΩ due to the large required layout area. A value of $R_{ref} = 2.6$ MΩ was chosen to generate a reference voltage $V_{ref} = 32.5$ mV. In order to reduce the voltage ripple of V_C a filter capacitor $C_{fb} = 3$ pF is connected.

By rearranging (2.4) and applying the parameters from Table 2.1 one obtains

$$C = \frac{I_B}{f \cdot V_{ref}} = 293 \text{ fF}. \tag{2.5}$$

f	I_B	V_{ref}	R_{ref}	C_{fb}	C_{P1}, C_{P2}	C_{P3}
MHz	nA	mV	MΩ	pf	fF	pF
1.312	12.50	32.5	2.6	3	35	3.5

Table 2.1: Parameters for the circuit depicted in Fig. 2.3

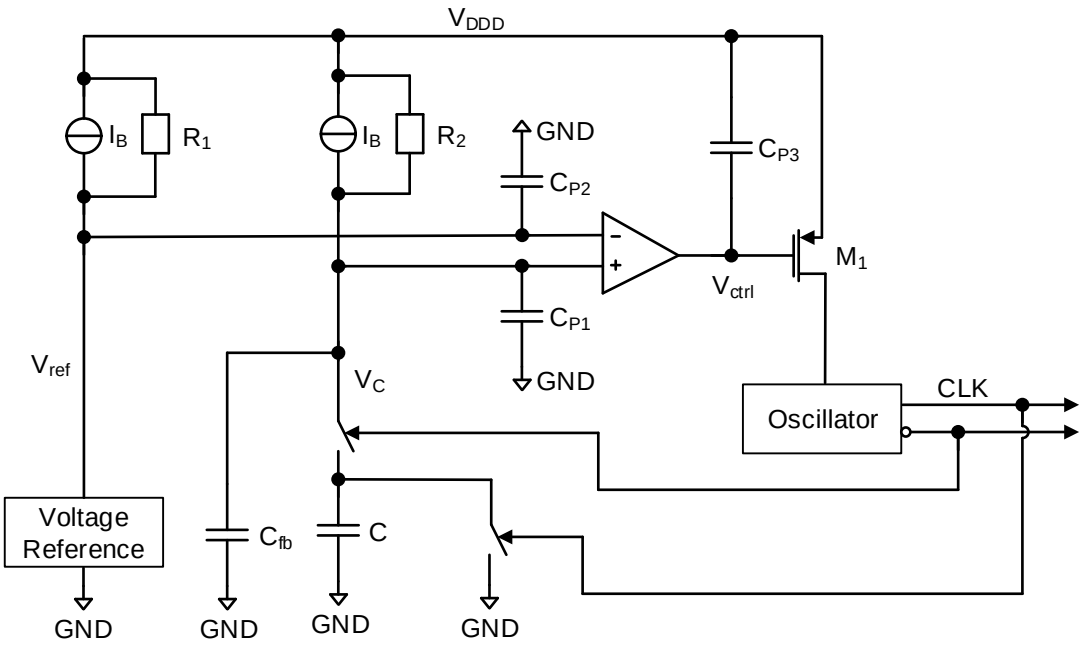

Figure 2.2: Oscillator with switched-capacitor feedback

One important topic, which must be addressed considering the feedback structure is the stability. The control loop in Fig. 2.2 has two significant poles. The first pole is formed by the capacitor C_{fb} and the equivalent resistance of the switched-capacitor C. From (2.4) one can see that the equivalent resistance can be expressed by

$$R_{equ} = \frac{dV_C}{dI_B} = \frac{1}{f \cdot C} = 2.6 \text{ M}\Omega. \tag{2.6}$$

Hence, the first pole is

$$f_{P1} = \frac{1}{2\pi \cdot R_{equ} \cdot C_{fb}} = 20.4 \text{ kHz}, \tag{2.7}$$

where R_{equ} and C_{fb} are the switched-capacitor equivalent resistance and the filter capacitance for V_C.

The second pole is formed by the output resistance of the operational transconductance amplifier (OTA) and the stabilisation capacitor C_{P3}.

$$f_{P2} = \frac{1}{2\pi \cdot R_3 \cdot C_{P3}} = 124 \text{ Hz}. \tag{2.8}$$

Fig. 2.3 depicts the linearised small-signal model of Fig. 2.2 including the gain factor of the switched-capacitor feedback A, the transconductance gm and the output resistance R_3 of the OTA and the frequency-gain factor of the oscillator K.

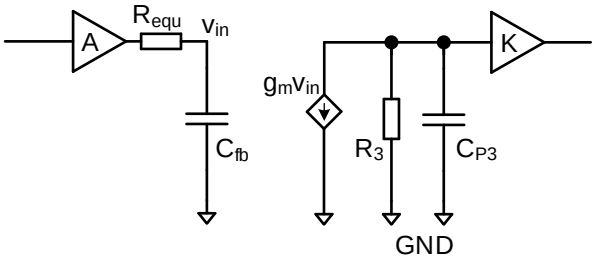

Figure 2.3: Small-signal model of the oscillator

By assuming the switched-capacitor is transforming a frequency change into a voltage change, one can derive a frequency to voltage gain.

$$A = \frac{dV_C}{df} = \frac{-I_B}{C \cdot f^2} = -25 \ \frac{\text{nV}}{\text{Hz}}. \tag{2.9}$$

Furthermore, by assuming an oscillator transforms a voltage change (V_{ctrl}) into a frequency change, one can derive a voltage to frequency gain. Fig. 2.4 depicts the frequency behaviour over the control voltage. By calculating the slope around 1.312 MHZ one obtains

$$K = \frac{\Delta f}{\Delta V_{ctrl}} = -13.35 \ \frac{\text{MHz}}{\text{V}}. \tag{2.10}$$

The stability of the circuit depicted in Fig. 2.2, can be checked by analysing the phase margin at the open loop unity gain frequency. The linearized model depicted in Fig. 2.3 is used to determine the open loop frequency response.

Fig. 2.5 and Fig. 2.6 depict the magnitude and phase frequency response, respectively. The magnitude reaches unity at 2.5 kHz. The phase margin at this frequency equals 85 °. Hence, the feedback circuit is stable.

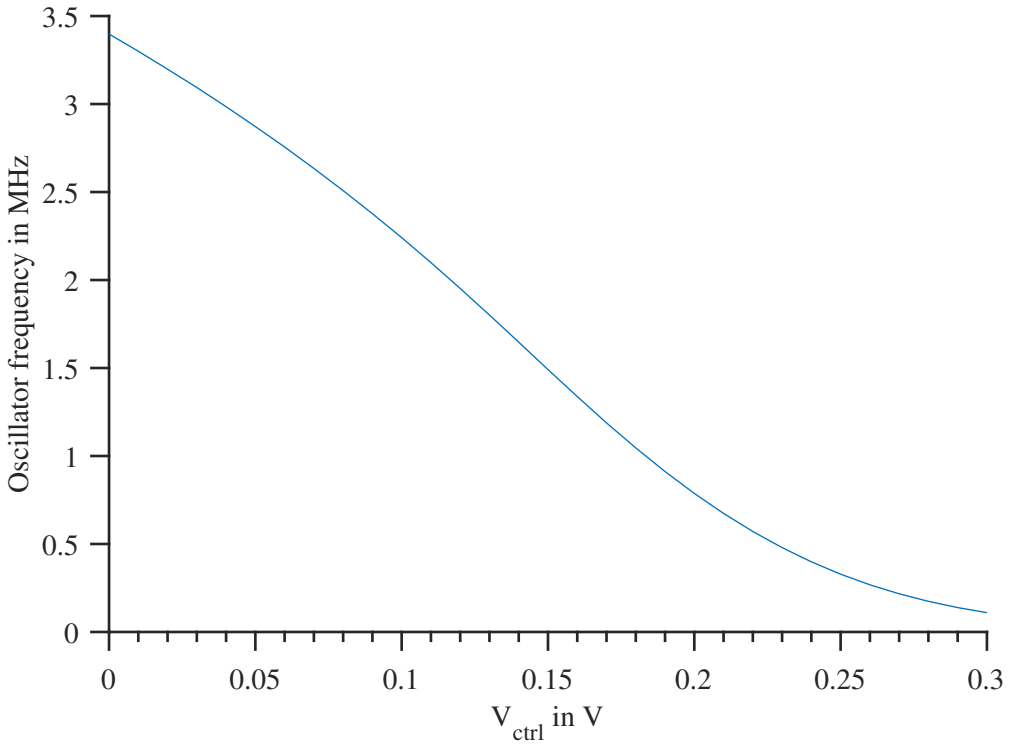

Figure 2.4: Frequency over V_{ctrl}

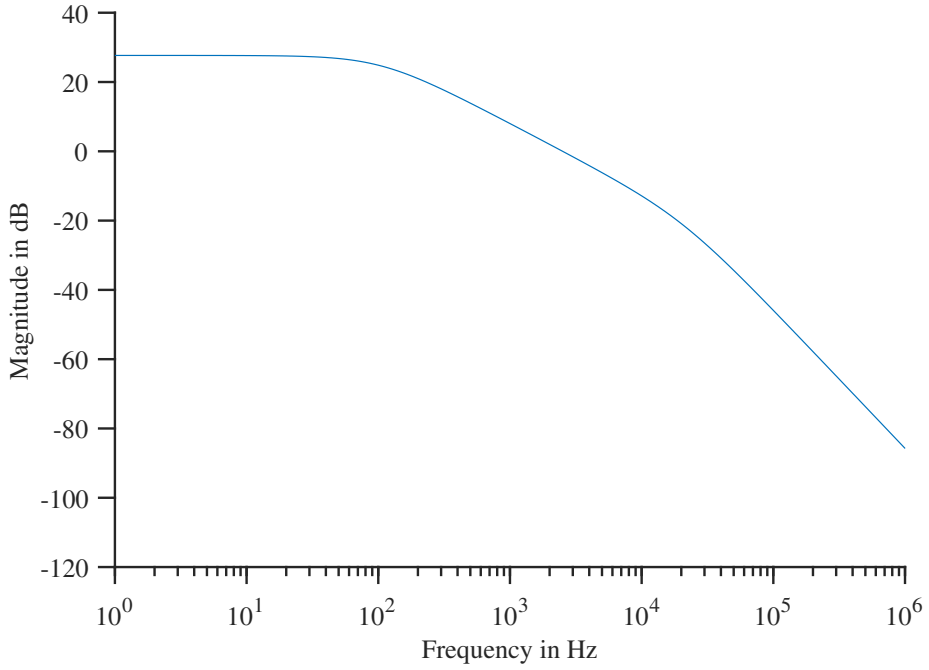

Figure 2.5: Magnitude response of the linearised small-signal model depicted in Fig. 2.3

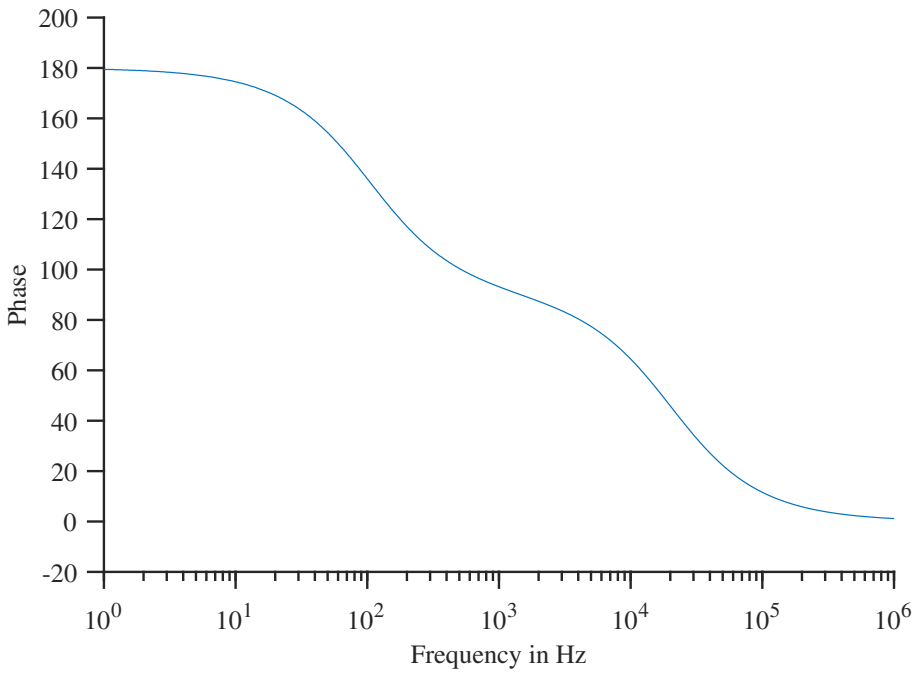

Figure 2.6: Phase response of the linearised small-signal model depicted in Fig. 2.3

As a final step it is important to derive the relation between the bias current I_B and the reference voltage V_{ref} in order to describe the controllability of the the whole feedback structure depicted in Fig. 2.3.

$$\frac{dV_C}{dI} = \frac{1}{f \cdot C} = 1.28 \ \frac{\mathrm{V}}{\mathrm{A}}. \tag{2.11}$$

One limitation of the feedback regulated oscillator is the slow reaction time on an input change. Hence, the settling time of the frequency after an input change, is already limited by the feedback structure itself. Due to the fact that the output frequency must settle within 10 μs, the feedback regulated oscillator topology is not suitable for the demanded specifications in Table 1.1.

2.2 Ring oscillator with temperature compensation

Fig. 2.7 depicts a three stage ring oscillator concept with an integrated temperature compensation. Unlike a traditional three stage oscillator, it has an additional current mirror formed by M_3 and M_4. This allows the usage of a PMOS device (M_5) in the output stage. Since the threshold voltage decreases by increasing the temperature (2.12), the drain-source voltage of M_1, M_2 and M_5 also decreases. Hence, the amplitude of V_{C1} and V_{C2} show complementary to absolute temperature (CTAT) behaviour and the amplitude of V_{out} shows positive to absolute temperature (PTAT) behaviour. By increasing the gain of the first two stages the overall temperature dependency can be made more CTAT and by increasing the gain of the third stage the temperature behaviour can be made more PTAT. From the Bsim3V3 model reported in [28], the temperature behaviour of the threshold voltage and the mobility can be approximated by

$$V_{th} = V_{th0} + K_{T1} \cdot (\frac{T}{T_{NOM}} - 1), \tag{2.12}$$

$$\mu_{eff} = \mu_0 \cdot (\frac{T}{T_{NOM}})^{\mu_{TE}}, \tag{2.13}$$

where V_{th0} is the zero-bias threshold voltage, K_{T1} is a negative temperature coefficient, T_{NOM} is the temperature at which the parameters are extracted, μ_0 is the mobility at $T = T_{NOM}$ and μ_{TE} is the mobility temperature exponent.

Assuming the voltage across C_1 is zero, I_B charges C_2 until the gate-source voltage of M_5 becomes lower than its threshold voltage. V_{out} is pulled to ground and M_1 is switched off. The voltage across C_1 starts to increase until it reaches the threshold voltage of M_2. M_2 discharges C_2 very fast and M_5 switches V_{out} back to V_{DDD}.

The oscillator generates a square wave shaped signal. The duty cycle of the signal depends on the gain of the individual stages. In order to achieve a duty cycle of 50 %, a frequency divider is connected to the output. The frequency divider is implemented as a D-FF.

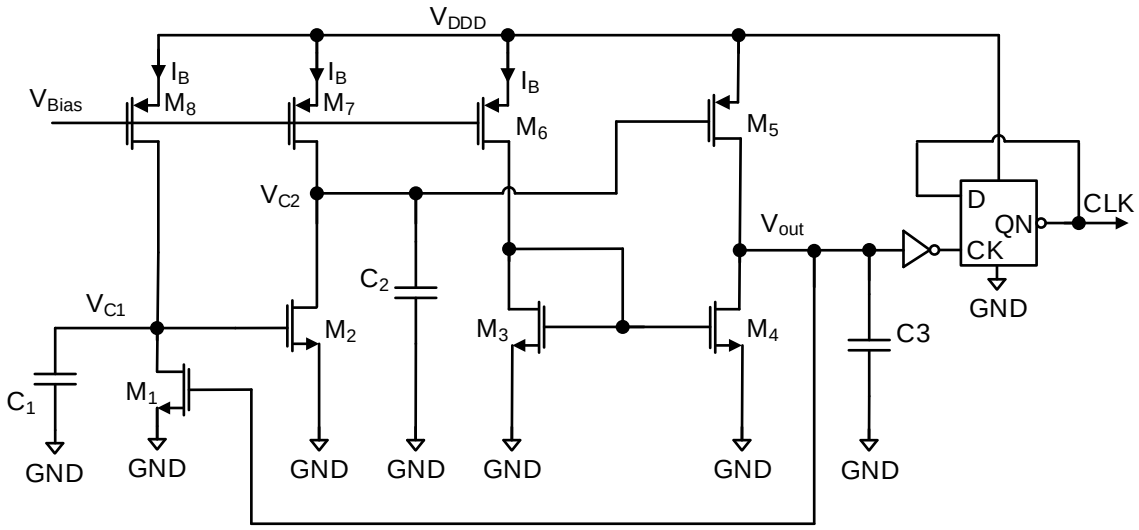

Figure 2.7: Ring oscillator with temperature compensation

The output frequency can be approximated by considering three delay stages. The delay of each stage can be approximated by

$$T_{d_1} = \frac{C_1 \cdot V_{thn}}{I_B}, \tag{2.14}$$

$$T_{d_2} = \frac{C_2 \cdot (V_{DDD} - V_{thp})}{I_B}, \tag{2.15}$$

$$T_{d_3} = \frac{C_3 \cdot V_{thn}}{I_B}, \tag{2.16}$$

where $C_{1,2,3}$ is the capacitance at the output of the corresponding stage, V_{thn} and V_{thp} is the threshold voltage of NMOS and PMOS devices, respectively and I_B is the bias current of the stage. The output frequency of the oscillator can be determined by adding the three delays

$$f_{OSC} = \frac{1}{2 \cdot (T_{d_1} + T_{d_2} + T_{d_3})}. \tag{2.17}$$

By substituting (2.14) (2.15) (2.16) into (2.17) one obtains

$$f_{OSC} = \frac{I_B}{2 \cdot (C_2 \cdot (V_{DDD} - V_{thp}) + (C_1 + C_3) \cdot V_{thn})}. \tag{2.18}$$

From (2.12) it can be see that V_{thn} and V_{thp} show a CTAT. By choosing the values in (2.18) for C_1, C_2, C_3 properly, the temperature induced threshold change can be compensated and thus a stable output frequency over temperature can be achieved. One major draw back of this oscillator structure is that the temperature compensation is very sensitive to $C_{1,2,3}$ which are strongly affected by process variations.

One can see from (2.18) that the oscillator frequency is proportional to the current through the delay stages, whereas the current can be expressed in terms of V_{Bias} by

$$I_B = \frac{\mu C_{ox}}{2} \frac{W}{L} (V_{DDD} - V_{Bias} - V_T)^2. \tag{2.19}$$

V_{Bias} is the gate voltage of $M_{6,7,8}$. As (2.18) indicates, the overall frequency can be controlled by V_{Bias}.

2.3 Relaxation oscillator

A relaxation oscillator circuit includes a feedback loop with a switching device, such as a transistor that repetitively discharges a capacitance [29]. The frequency of the oscillator depends on the size of the capacitance [2].

Relaxation oscillators are usually employed for low-power operations with relatively good accuracy because they do not require any external components and can be cheaply implemented in a CMOS technology [2]. The absolute frequency accuracy is dictated by the tolerances of on-chip capacitors and resistors that can range up to 40 % [2]. Nevertheless, the impact of tolerances can be reduced by trimming.

A major disadvantage of relaxation oscillators is their susceptibility to temperature variations. Oscillators in UHF RFID applications operate typically in a temperature range from -40 °C to 85 °C. The allowed tolerance for the oscillator frequency is about ±10 % in order to be compliant with the EPC Generation-2 standard [15]. Assuming a maximum frequency variation of 4% after trimming (at room temperature), it is essential that the oscillator exhibits a temperature drift of less than 700 ppm/°C to achieve an overall accuracy of 10% over the considered operating temperature range.

The oscillator depicted in Fig. 2.8 includes a reference voltage generation, which is supplied by a bias current I_B, and a reference capacitor C_R [2]. This capacitor is charged with a bias current I_B and its voltage is compared to the reference voltage V_{REF}. When the capacitor voltage exceeds the reference voltage, the output of the comparator triggers the pulse generator. The RESET signal closes the switch S_R and C_R gets discharged. The reset pulse has to be sufficiently long in order to completely discharge the capacitor.

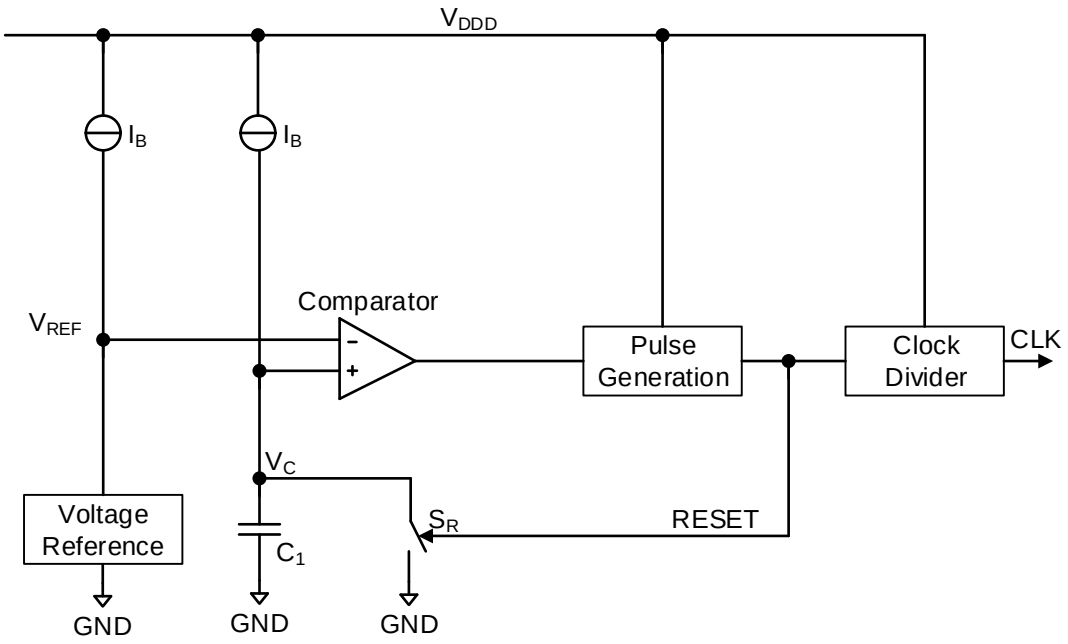

Figure 2.8: Principle circuit diagram of the relaxation oscillator [2]

The pulse generator in Fig. 2.8 is formed by two inverters and a RS-latch and its dynamic current consumption is proportional to the operating frequency, the total load capacitance and the supply voltage.

The output of the pulse generator is a periodical signal with duty cycle $\ll 50$ %, since the discharging of C_R is much faster than the charging. In order to achieve a 50 % duty cycle, a frequency divider is added at the output. As reported in [2], the oscillator period can be expressed by

$$T_{OSC} = \frac{C_1 \cdot (V_{REF} + \Delta V)}{I_B} + t_p, \tag{2.20}$$

where C_1, V_{REF}, I_B and t_p are the reference capacitor, the reference voltage, the bias current and the pulse width of the pulse generator, respectively. ΔV is the comparator overdrive voltage to generate a sufficient high voltage level at the comparator output to activate the generator output. t_p can be typically neglected because $T_{OSC} \gg t_p$. Therefore, the oscillator frequency can be approximated by

$$f_{OSC} = \frac{I_B}{C_1 \cdot (V_{REF} + \Delta V)}. \tag{2.21}$$

In order to reduce the current consumption of a circuit, the amount of current conduct-

ing branches should be as small as possible. Thus, the comparator in Fig. 2.8 has been implemented as a current comparator as depicted in Fig. 2.10 [2]. The comparator input differential pair is formed by M_3 and M_4, biased by a current I_B. The non-inverting input at the source of M_4 is connected to the capacitor C_1, while the inverting input at the source of M_3 is connected to a reference voltage V_{REF} which is generated by a MOS divider.

Unlike proposed in [2], the capacitance C_1 is not implemented as a MOS capacitor because the voltage level of V_C stays below 200 mV, and thus it is not possible to operate the MOS capacitor in strong inversion. Fig. 2.9 depicts the capacitance of an NMOS capacitor with respect to the applied gate-source voltage. As one can see, the capacitive value in weak and moderate inversion depends strongly on the gate-source voltage. Only in strong inversion and accumulation region, the MOS capacitor approaches a stable value. Since the voltage across the capacitor in Fig. 2.10 is below 200 mV, an NMOS capacitor would not operate in strong inversion. Therefore, the spread of the reference capacitor C_1 would be large.

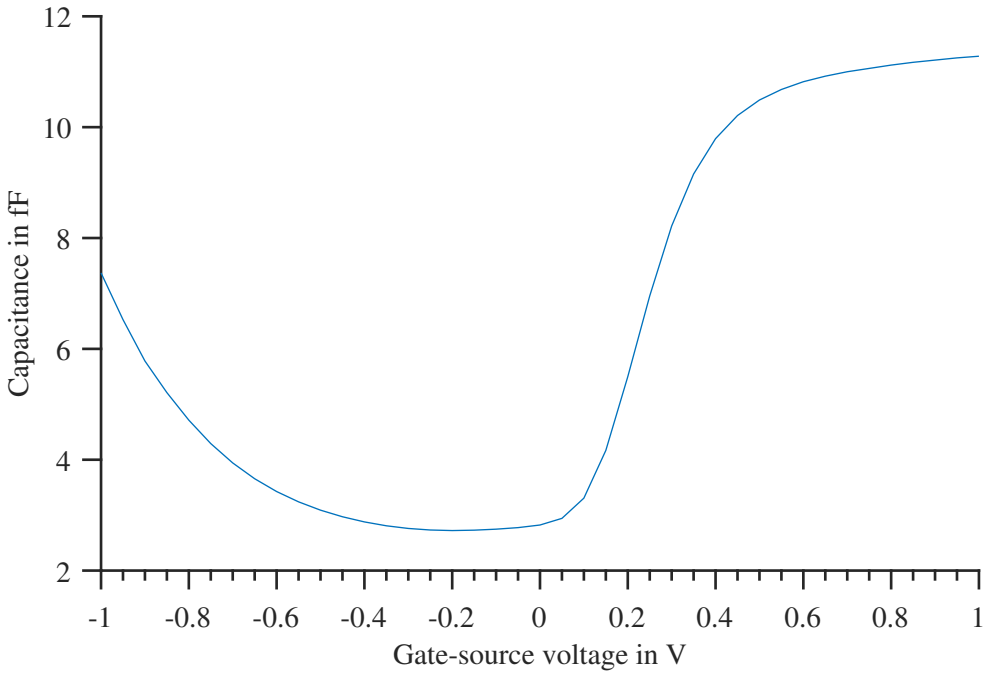

Figure 2.9: Capacitance versus gate-source voltage of an NMOS capacitor

In order to improve process and mismatch variations, a metal capacitor is used as reference capacitor. A metal capacitor has the advantage that the capacitance is independent of the bias voltage. A drawback of metal capacitors is the large required area compared to MOS capacitors.

The operation of the oscillator in Fig. 2.10 can be divided into two parts. First, the charging of the reference capacitor and second the discharging. Assuming the reset signal is

high, the capacitor C_1 gets discharged by M_6. After the reset signal changes to low, V_C is steadily increasing due to the bias current I_B. As soon as V_C approaches the reference voltage V_{REF}, M_4 is turning off and the comparator output V_{comp} rises instantaneously. This triggers the connected RS-latch and C_1 is immediately discharged by M_6. As soon as C_1 is discharged, the comparator output changes to low and the RS-latch resets. This operation results in a sawtooth waveform of V_C and produces a narrow clock pulse at the output of the RS-latch.

As mentioned earlier, it is not favourable to use a MOS capacitor because it cannot be driven in strong inversion due to the low supply voltage of the oscillator (0.6 V). A metal fringe capacitor using metal layer no. two to metal layer no. four was chosen to implement C_1. Metal fringe capacitor feature a low resistivity, a voltage-independent capacitance, a and low leakage. The control of capacitance is a beneficial feature because it reduces the impact of process and mismatch variations compared to a MOS capacitor.

The threshold voltage of the inverter and the RS-latch depicted in Fig. 2.10 decreases at increasing temperature (2.12). The temperature behaviour is illustrated in Fig. 3.3. Since ΔV in (2.21) is depending on the threshold voltage of the inverter and the RS-latch, the output frequency would increase with increasing temperature. In order to obtain a temperature stable output frequency, V_{REF} has to increase while ΔV decreases. V_{REF} is generated by a MOS divider which has a PTAT behaviour [3]. Fig. 2.11 depicts the circuit for the reference voltage generation V_{REF}.

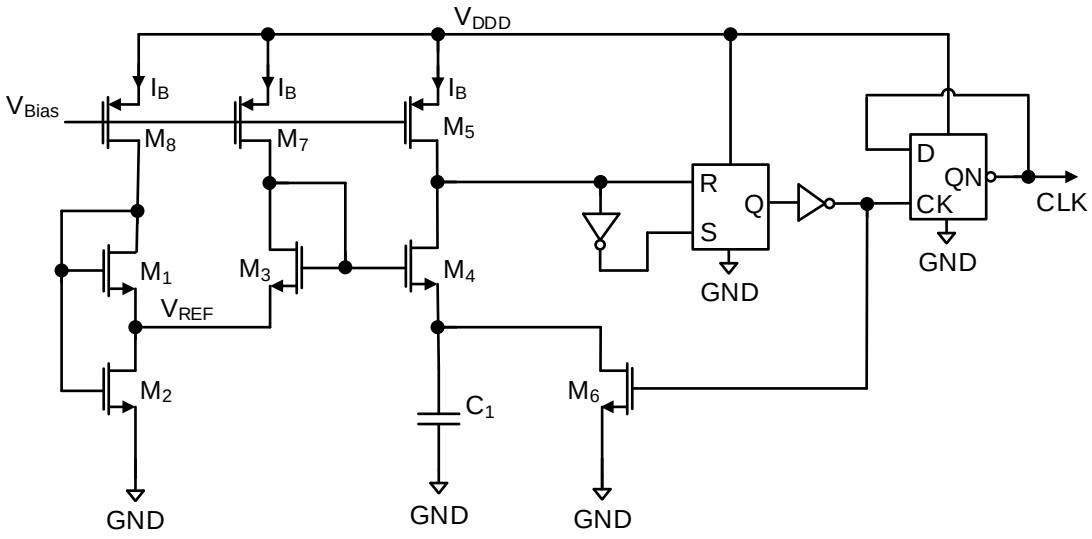

Figure 2.10: Relaxation oscillator with current comparator [2]

2.3.1 Reference generation

The MOS divider depicted in Fig. 2.11 generates a PTAT output voltage assuming both transistors operate in weak inversion that can be approximated by [3]

$$V_{REF} = V_T \cdot ln(1 + 2 \cdot \frac{S_1}{S_2}) + \Delta V_0, \tag{2.22}$$

where $S = \frac{W}{L}$ and V_T is the thermal voltage. ΔV_0 describes the influence of the mismatch between the two transistors.

As reported in [3], the voltage V_{REF} is almost independent of the bias current of the transistors as long as the bias current is low enough to maintain the transistors in weak inversion and larger than the leakage current. When the current increases the transistors approach the moderate inversion region, which leads to an increase of V_{REF}.

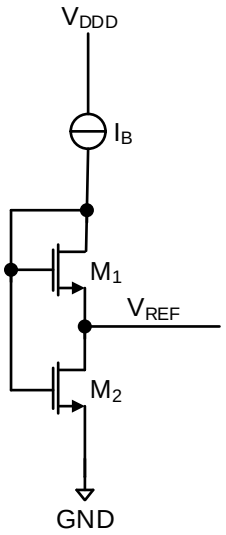

Figure 2.11: PTAT voltage generating MOS divider [3]

2.4 Summary

It is not possible to fulfill the specification for the settle time with the oscillator using a switched-capacitor frequency control. Hence, an oscillator implementation with an integrated temperature compensation is necessary.

A disadvantage of the presented three-stage ring oscillator with integrated temperature compensation is the strong dependency of the temperature behaviour on parasitic capacitances. Hence, the accuracy of the temperature compensation sufferers from process and mismatch variations.

The temperature compensation approach applied in the relaxation oscillator has the advantage that it is less susceptible to parasitic capacitances as the three-stage ring oscillator. Furthermore, the overall temperature characteristic can be adapted.

Chapter 3

Circuit implementation

In the previous chapter, three different oscillator concepts were introduced. As discussed, the ring oscillator concept using a switched-capacitor feedback is not suitable with respect to the defined specifications regarding the settling time. Therefore, the oscillator concept with switched-capacitor feedback is not further considered in this work.

This chapter describes circuit implementations of the ring oscillator and the relaxation oscillator with integrated temperature compensation in a 40-nm CMOS technology. The focus is put on the comparison between the two oscillators regarding controllability, temperature variation, process and mismatch variations, phase noise, and power supply rejection.

In addition to the implementation of the oscillators, two trimming structures are presented. The trimming circuits use a 6-bit digital control word to cover the whole frequency spread due to bias current, process, and mismatch variations.

The relaxation oscillator, which shows a performance advantage, and a corresponding trimming circuit have been implemented in layout. The circuit layouts are discussed in detail.

3.1 Oscillator

3.1.1 Design parameters

Table 3.1 and Table 3.2 summarize the design parameters of the temperature compensated ring oscillator (Fig. 2.7) and the relaxation oscillator (Fig. 2.10), respectively. The design parameters were determined in two steps. At first, the equations discussed in the previous chapter were used to estimate coarse values for the parameters. The estimated parameters were used as basis for circuit simulations to optimize the design in terms of temperature behaviour and frequency controllability.

	W/L
M_1, M_2	300nm/600nm
M_3	320nm/10μm
M_4	1.28μm/10μm
M_5	1.25μm/1.2μm
C_1, C_2, C_3	7fF

Table 3.1: Design parameters of the temperature compensated ring oscillator

By rearranging (2.18) and assuming $f_{OSC} = 1.312$ MHz, $V_{DDD} = 0.6$ V, $C = C_1 = C_2 = C_3 = 7$ fF, $V_{thn} = 280$ mV and $V_{thp} = 300$ mV one obtains a current

$$I_B = 15.8 \text{ nA}. \tag{3.1}$$

Neglecting parasitic capacitances and the current consumption of the inverter and D-Flip-Flop depicted in Fig. 2.7, the oscillator current consumption can be approximated by

$$I = 4 \cdot I_B = 60 \text{ nA}. \tag{3.2}$$

	W/L	Multiplier
M_1	1μm/1μm	33
M_2	1μm/2μm	1
M_3, M_4	1μm/2μm	1
M_5, M_7, M_8	320nm/10μm	1
M_6	300nm/250nm	1
C_1	7fF	

Table 3.2: Design parameters of the relaxation oscillator

The reference capacitance C_1 depicted in Fig. 2.10 is composed of a metal fringe capacitor with a capacitance $C = 7$ fF and the parasitic gate-source capacitance C_{GS} of M_4. When M_4 operates in linear region C_{GS} can be approximated by [30]

$$C_{GS} = W \cdot L_D \cdot C_{OX} + \frac{1}{2} \cdot W \cdot L \cdot C_{OX}, \tag{3.3}$$

where W, L and L_D is the transistor width, the transistor length, and the gate overlapping length, respectively. C_{OX} is the gate oxide capacitance per unit area. By using the parameters from Table 3.2 one obtains $C_{GS} = 14$ fF. Hence the overall capacitance $C_1 = C + C_{GS} = 21$ fF.

By rearranging (2.21), and considering a nominal frequency $f_{OSC} = 1.312$ MHz, a capacitance $C_1 = 21$ fF and $V_{REF} + \Delta V = 370$ mV one obtains a bias current

$$I_B = 10.2 \text{ nA}. \tag{3.4}$$

The relaxation oscillator comprises three current branches with an identical weighting factor. Therefore, the overall power consumption is

$$I = 3 \cdot I_B = 30.6 \text{ nA}. \tag{3.5}$$

By neglecting ΔV_0 in (2.22) and considering the values from Table 3.2 and assuming an absolute temperature $T = 300$ °K, one obtains

$$V_{REF} = 126 \text{ mV}. \tag{3.6}$$

3.1.2 Frequency controllability

To evaluate the frequency controllability of both oscillators, the characteristic of the oscillator frequency versus the bias current was simulated and plotted in Fig. 3.1. Table 3.3 summarizes the frequency controllability of the two oscillators defined as

$$\frac{\Delta f}{\Delta I_B}, \tag{3.7}$$

at the target frequency of 1.312 MHz.

	relaxation oscillator	ring oscillator
	kHz/nA	kHz/nA
$\Delta f/\Delta I_B$	76	67

Table 3.3: Frequency controllability with respect to the bias current at a frequency of 1.312 MHz

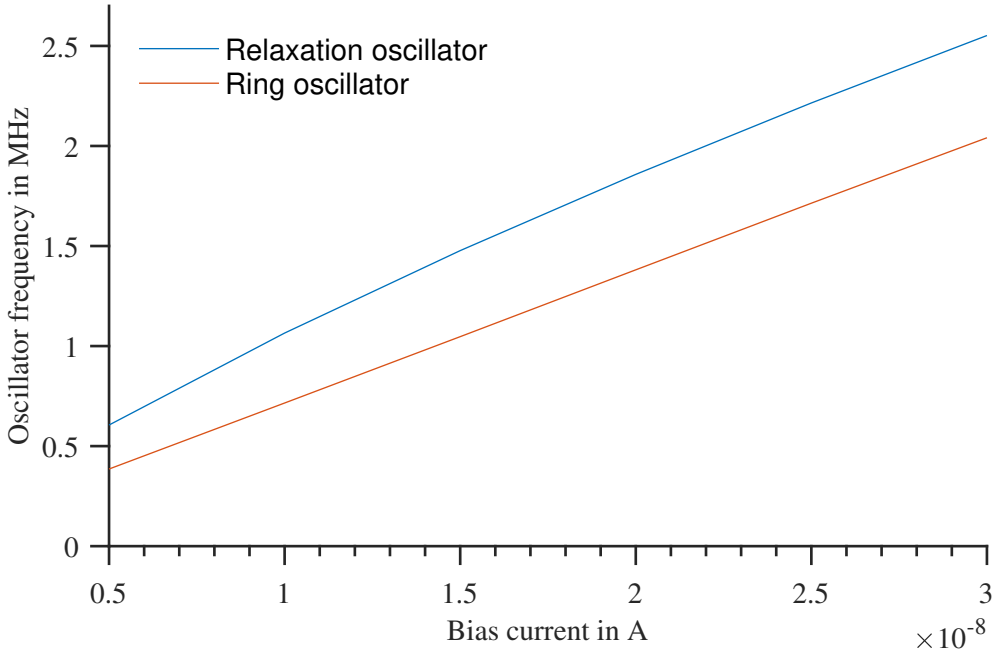

Figure 3.1: Frequency of the temperature compensated ring oscillator and the relaxation oscillator versus the bias current

The frequency controllability is an important property regarding the sensitivity of the oscillator frequency with respect to process and mismatch variations and the required trimming range. By increasing the frequency gain versus the bias current, the needed trimming range to compensate the intrinsic frequency spread of the oscillator core due to process and mismatch variations decreases, but the frequency spread induced by bias current variations increases.

3.1.3 Temperature behaviour

Fig. 3.2 depicts the frequency deviations versus a varying temperature. The frequency is normalized to the nominal frequency $f = 1.312$ MHz. As one can see the frequency varies less than $\pm$ 1 % within a temperature range from -40 °C to 85 °C. Therefore, the temperature drift is less than 167 ppm/°C. The temperature behaviour depicted in Fig. 3.2 was simulated using nominal process corner models.

As discussed in chapter 2, the temperature coefficient of the ring oscillator strongly depends on the output capacitance of each stage, and thus is strongly affected by layout parasitic capacitances. In contrast to this, the relaxation oscillator shows less dependence to parasitic capacitances but the temperature behaviour is predominately defined by the reference voltage and the digital threshold voltage of the pulse-generating logic (the inverters and the RS-latch in Fig. 2.10).

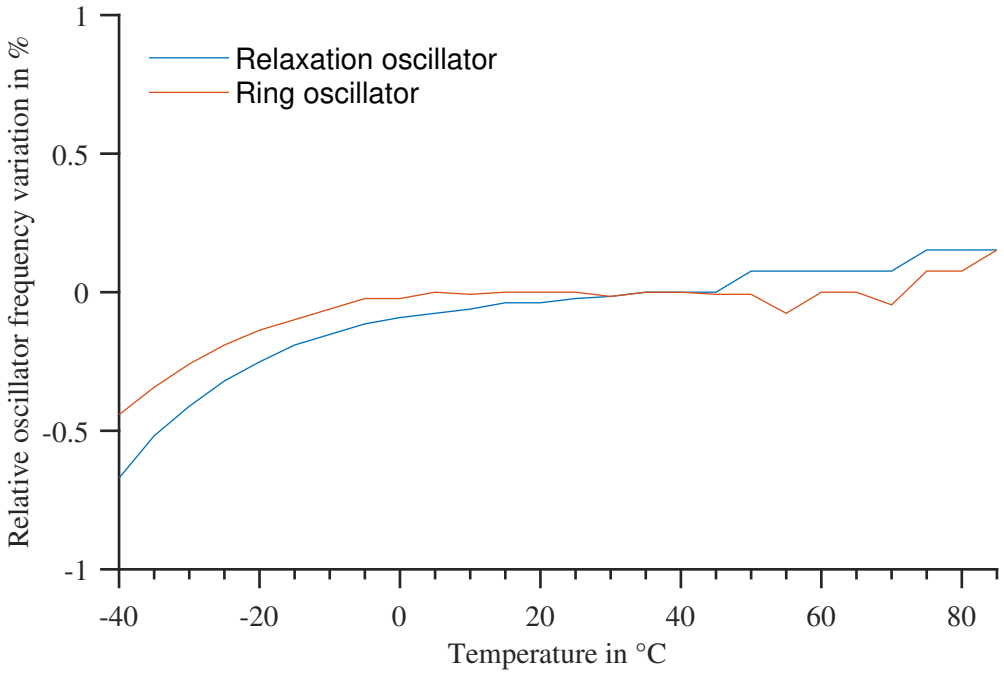

Figure 3.2: Normalized frequency of the temperature compensated ring oscillator and the relaxation oscillator over temperature

Another advantage of the relaxation oscillator is the controllability of the temperature coefficient. By adjusting the gain of the comparator stage, which corresponds to changing ΔV in (2.21), the frequency characteristic versus temperature can be balanced, as shown in Fig. 3.2.

Fig. 3.3 depicts the temperature behaviour of the reference voltage of the relaxation oscillator and the threshold voltage of the pulse-generating logic. As indicated by (2.22), the reference voltage increases linearly with the temperature. The comparator overdrive voltage ΔV is a function of the threshold voltage of the pulse-generating logic and therefore ΔV decreases as the threshold voltage decreases. The reference voltage and the threshold voltage of the pulse-generating logic have opposite temperature coefficients and can be used to compensate each other.

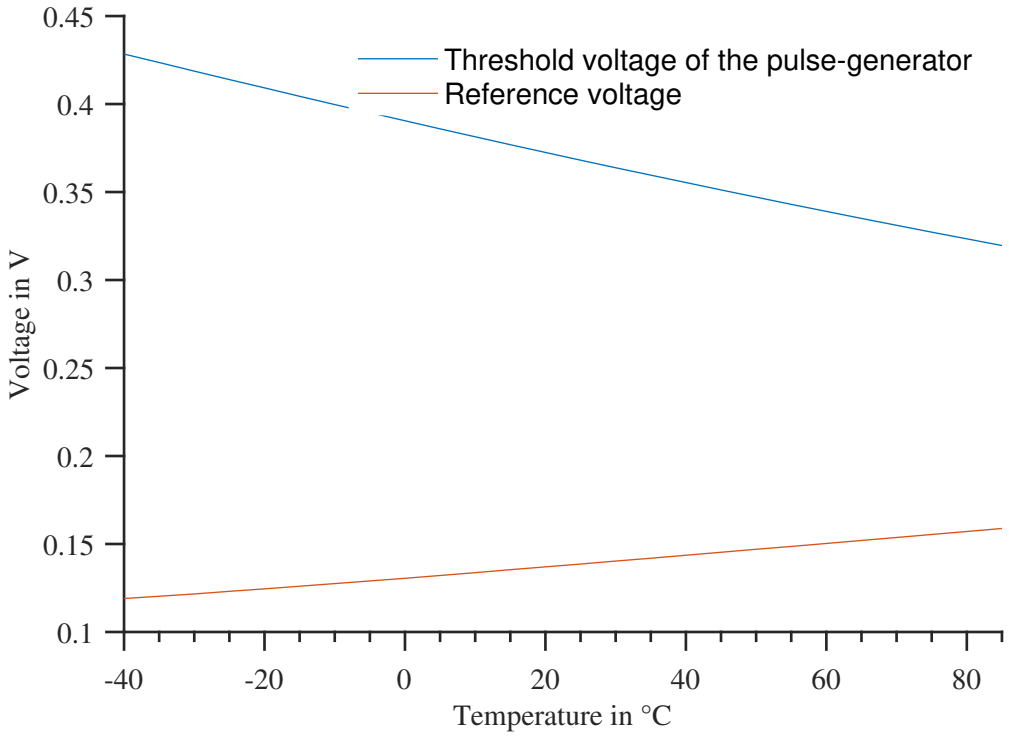

Figure 3.3: Reference voltage of the relaxation oscillator and the threshold voltage of the pulse-generating logic versus temperature

3.1.4 Power consumption

An important parameter of the oscillator is the power consumption, since an RFID transponder IC is supplied entirely by the RF power impinging upon the transponder antenna. To achieve a high reader range, the power consumption of the oscillator should be as low as possible.

Table 3.4 compares the current consumption of the temperature compensated ring oscillator and the relaxation oscillator. As one can see, the power consumption of the ring oscillator is nearly twice as high as the power consumption of the relaxation oscillator. Furthermore, the difference in the power consumption becomes more pronounced, by considering 1 fF parasitic capacitance between each node and ground.

The ring oscillator is sensitive with respect to parasitic capacitances, which results in an increase of the current consumption due to layout parasitic capacitances. In case of the relaxation oscillator, the effect of the parasitics is less significant, and thus the relaxation oscillator is the preferable design with respect to power consumption.

	Ring oscillator	Relaxation oscillator
Schematic	131 nA	75 nA
Estimated parasitic capacitances	220 nA	98 nA

Table 3.4: Power consumption of the temperature compensated ring oscillator and the relaxation oscillator, with and without estimated parasitic capacitances of 1 fF at each internal node

3.1.5 Process and mismatch variations

Fig. 3.4 and Fig. 3.5 depict the frequency variation of the two oscillators after a trimming procedure at room temperature (27 °C). As one can see, the frequency variation of the relaxation oscillator is slightly worse in comparison to the ring oscillator. The larger frequency spread is a result of to the higher current to frequency gain of the relaxation oscillator (Fig. 3.1), since the same variation of the bias current causes a higher variation of the frequency.

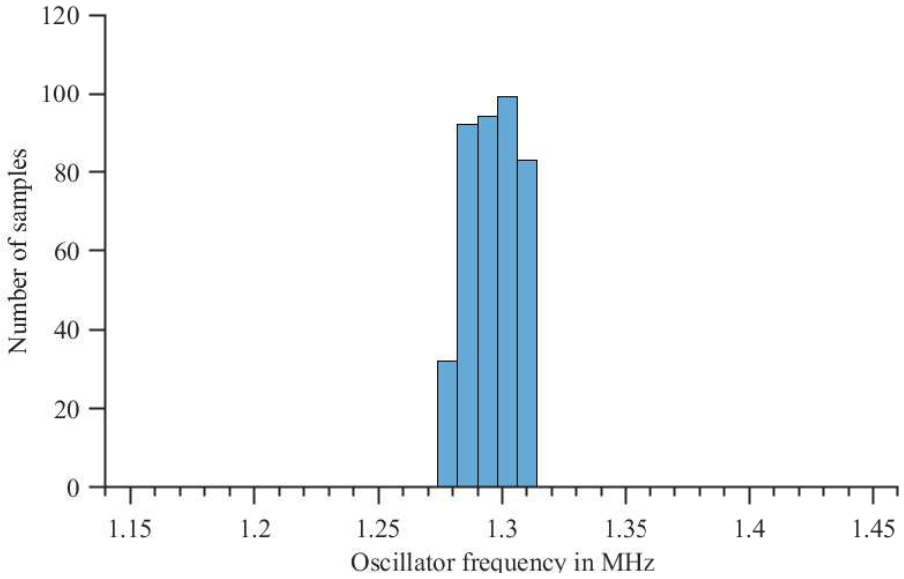

Figure 3.4: Ring oscillator process and mismatch variations at 27 °C after the trimming procedure

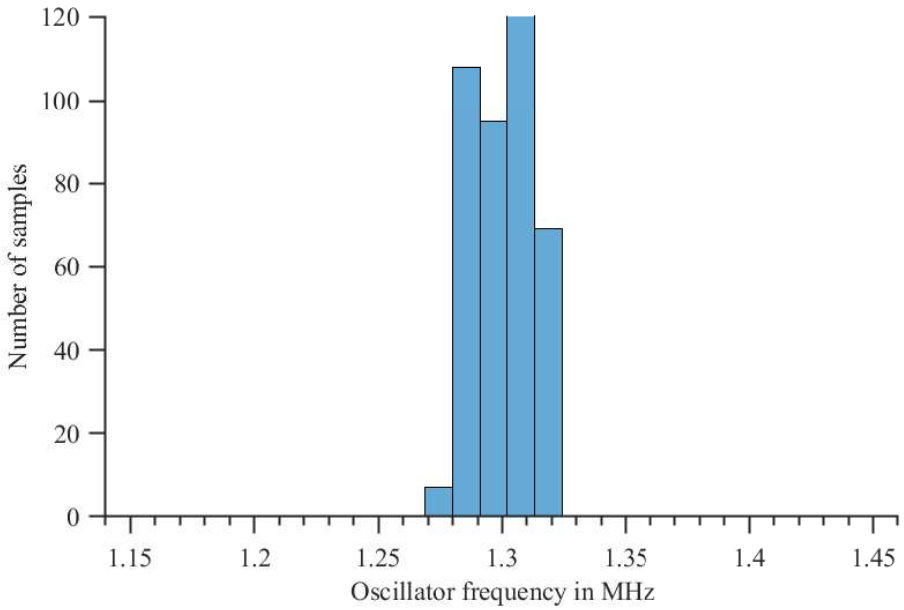

Figure 3.5: Relaxation oscillator process and mismatch variations at 27 °C after the trimming procedure

Fig. 3.6 and Fig. 3.7 illustrate the influence of process and mismatch variations on the temperature compensation of the ring oscillator. In short channel devices, the threshold voltage depends on the effective gate length due to a non-uniform doping profile [31]. This effect is known as reverse short channel behaviour. Variations of the effective transistor channel length thus augment the threshold voltage spread due to doping variations, which has an impact on the frequency spread of the ring oscillator versus temperature.

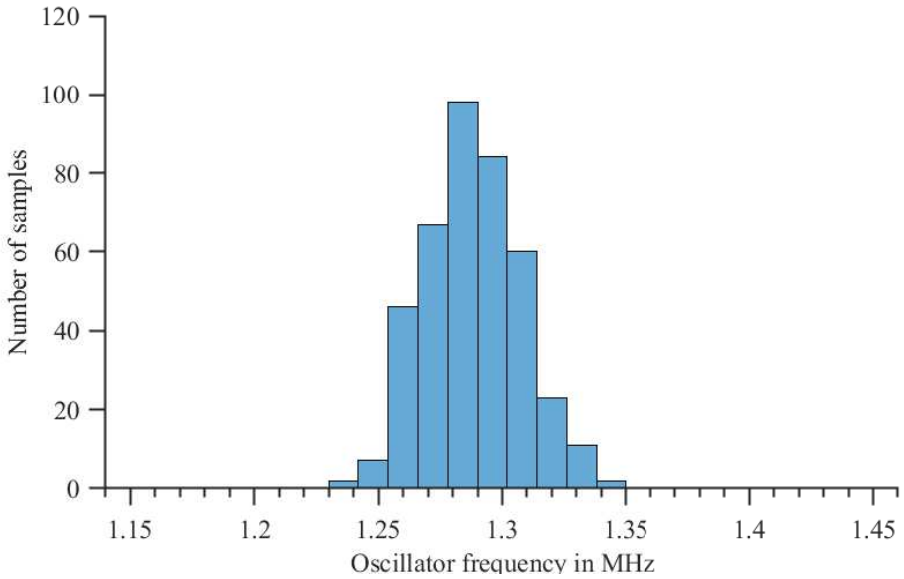

Figure 3.6: Ring oscillator process and mismatch variations at -40 °C after the trimming procedure

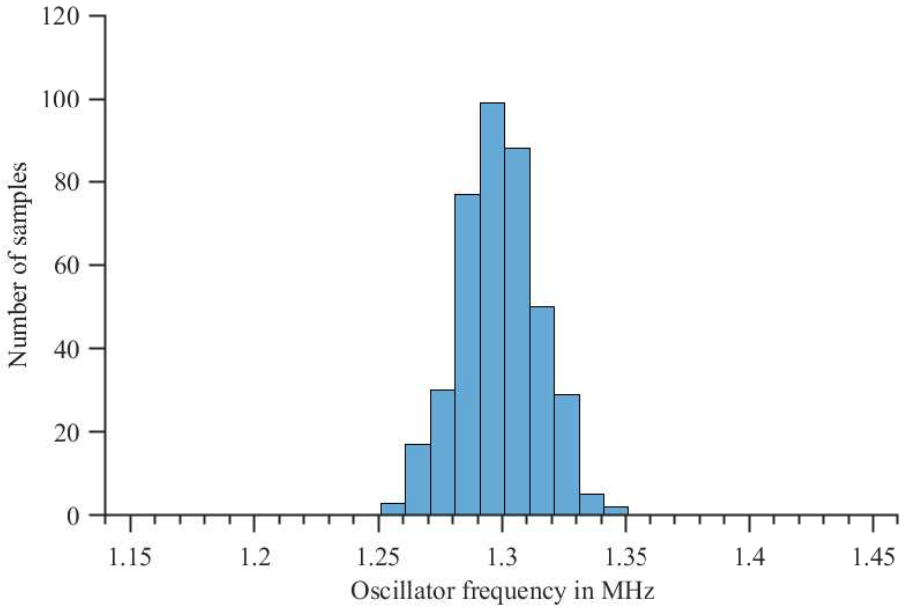

Figure 3.7: Ring oscillator process and mismatch variations at 85 °C after the trimming procedure

Fig. 3.8 and Fig. 3.9 depict the influence of process and mismatch variations on the relaxation oscillator temperature compensation. Also the threshold voltage of the pulse-generating logic varies due to process and mismatch variations. Furthermore, the reference voltage generated by a MOS divider depends on the matching of the individual devices (2.22).

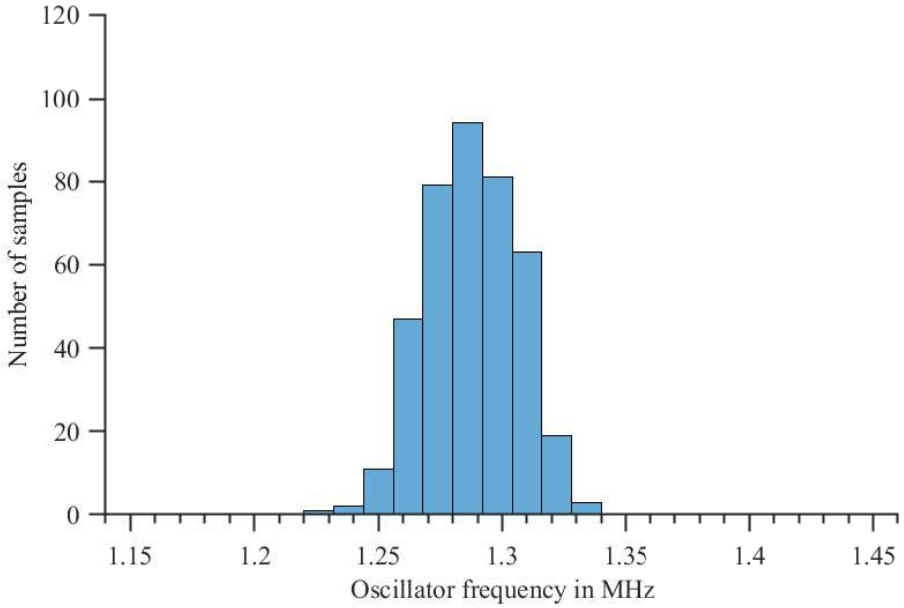

Figure 3.8: Relaxation oscillator process and mismatch variations at -40 °C after the trimming procedure

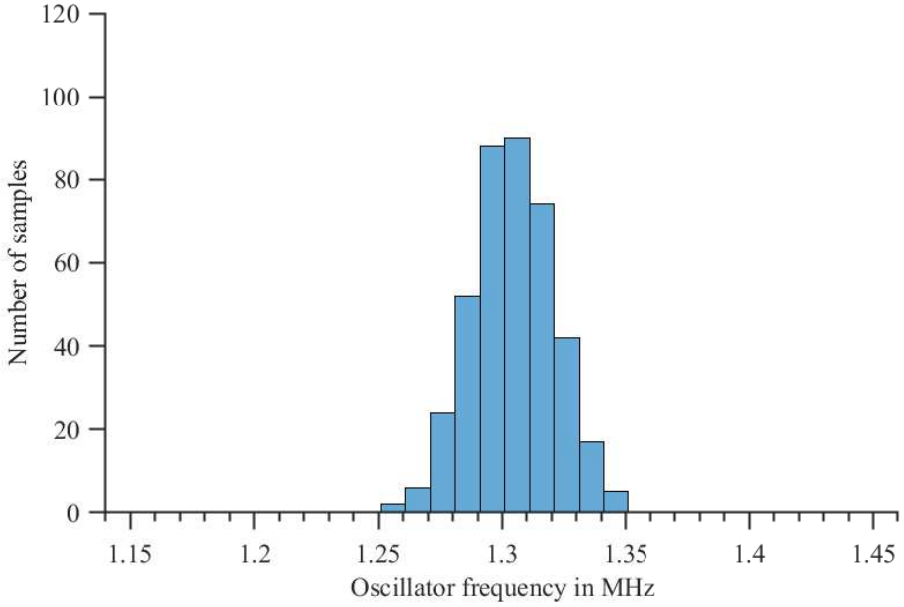

Figure 3.9: Relaxation oscillator process and mismatch variations at 85 °C after the trimming procedure

3.1.6 Phase noise

In an ideal oscillator, the period between signal transitions is constant. In practice however, the signal period varies, which is termed as clock jitter [32]. The cause of clock jitter is noise in the oscillator circuit. As reported in [33], the dominant noise in an oscillator is phase noise which can be characterized by a phase noise spectrum. The reason why phase noise is dominant, is the unity loop gain, as demanded by the Barkhausen criterion for achieving a stable oscillation. If the loop gain is larger than one, the oscillation amplitude increases until the amplifier goes into compression and the effective loop gain reduces to one [33]. As a result, the amplitude variations caused by noise are suppressed leaving only phase noise components.

When phase noise is dominated by white Gaussian noise, the root mean square (RMS) value of the time-domain phase jitter can be directly calculated by [34]

$$J = \sqrt{\frac{L(\Delta f)\Delta f^2}{f_0^3}}, \tag{3.8}$$

where $L(\Delta f)$ is the phase noise spectral density at a certain relative frequency, Δf is the relative frequency to the carrier and f_0 is the carrier frequency.

As described in [35], the phase noise is dominated by white Gaussian noise, if the slope of the phase noise spectrum is equal to -20dB/decade. Fig. 3.10 depicts the phase noise spectrum of the temperature compensated ring oscillator and the relaxation oscillator. As one can see, the phase noise can be well approximated by a white Gaussian noise dominated phase noise spectrum at around 10 kHz. Therefore, (3.8) can be used to calculate the time-domain phase jitter from the phase noise.

In Table 3.5 and Table 3.6 the phase noise induced time-domain jitter is summarized. The calculated value was obtained by considering the simulated phase noise at 10 kHz form Fig. 3.10 and using (3.8). Additionally, Cadence Virtuoso was used to calculate the period jitter from the simulated phase noise spectrum. Virtuoso provides two ways to simulated the phase noise.

The first method is called time-averaged noise simulation and it simulates the phase noise components averaged over an oscillation period, as describe in [36]. The second method is called sampled noise simulation. For sampled noise simulations an ideal sampler, is connected virtually at the oscillator output and only the noise at the instant of time is considered where the trigger event is generated.

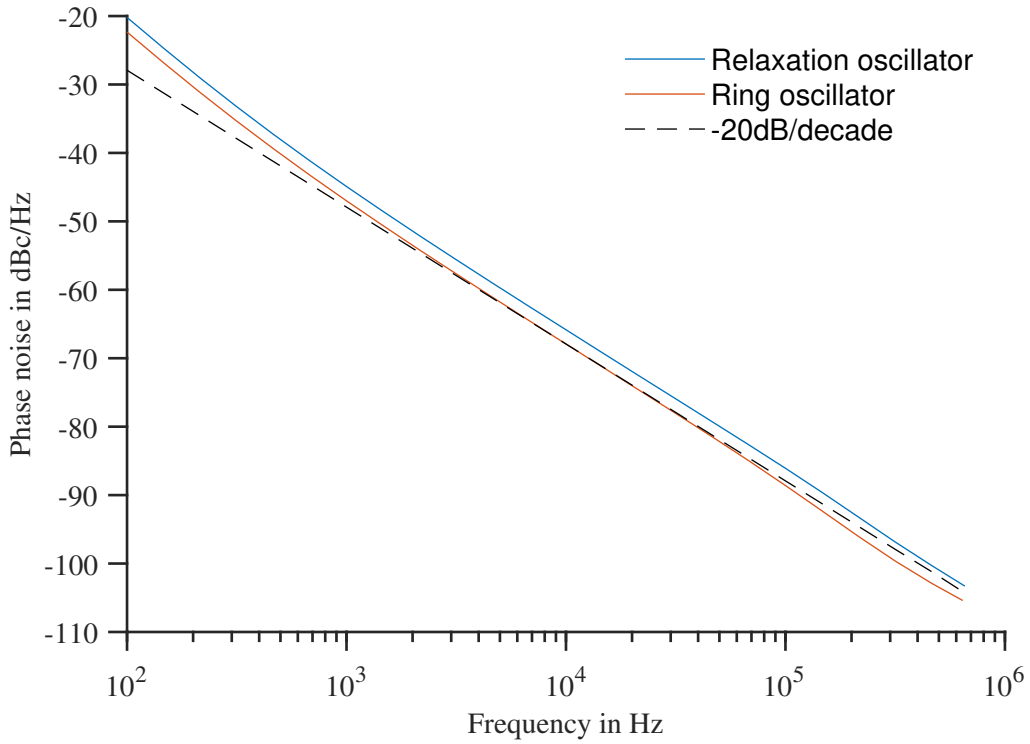

Figure 3.10: Phase noise spectrum for the temperature compensated ring oscillator and relaxation oscillator

To determine the long term jitter a divide ratio k is introduced. The divide ratio is the number of oscillation cycles (periods) used for calculating the jitter. As elaborated in [37], the jitter scales with $\sqrt{k}$ assuming a white noise dominated phase noise spectrum.

Divide ratio	Time averaged	Sampled	Calculated
k	ns	ns	ns
1	2.71	2.82	2.31
2	4.2	4.35	3.26
32	11.17	11.23	13.08

Table 3.5: RMS value of the period jitter due to phase noise of the ring oscillator

Divide ratio	Time averaged	Sampled	Calculated
	ns	ns	ns
1	2.748	3.003	2.331
2	4.298	4.442	3.29
32	11.16	11.65	13.19

Table 3.6: RMS value of the period jitter due to phase noise of the relaxation oscillator

3.1.7 Power supply rejection

An additional noise source in ring oscillators is the power supply [38]. Usually noise on the power supply appears as voltage steps or spikes due to the switching of digital logic gates. Power supply noise affects the oscillator frequency as well as the phase causing cycle-to-cycle jitter [38]. The point where a ring oscillator is most sensitive to power supply induced noise is during switching the stages [38].

The output stage in Fig. 2.7, formed by M_4 and M_5, is most sensitive to power supply induced noise because M_5 is directly connected to the supply rail V_{DDD}. The other two delay stages are connected via a current mirror to the supply rail. The current mirrors suppress disturbances due to supply voltage noise.

Fig. 3.11 depicts the small-signal model of the ring oscillator output stage while changing the output from logic level low to high. The switching voltage threshold of the first stage connected to the output is approximately 280 mV. At this output voltage, M_5 as well as M_4 are operating in the saturation region, and thus the drain source resistance can be approximated by [27]

$$R_O = \frac{1}{\lambda \cdot I_D}, \tag{3.9}$$

where λ and I_D are the channel length modulation factor and the drain current.

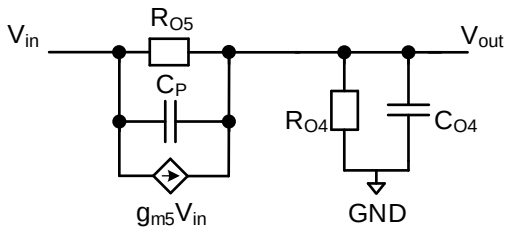

Figure 3.11: Equivalent small-signal model of the ring oscillator output stage

In order to simplify the power supply rejection calculation, the capacitors are transformed into laplace domain. By building the transfer function of the circuit in Fig. 3.11 one obtains

$$\frac{V_{out}}{V_{in}} = \frac{Z_{O4}(1 + g_{m5} \cdot Z_{O5})}{Z_{O4} + Z_{O5}}, \tag{3.10}$$

with

$$Z_{O4} = \frac{R_{O4}}{1 + sC_{O4} \cdot R_{O4}},\ Z_{O5} = \frac{R_{O5}}{1 + sC_P \cdot R_{O5}}, \tag{3.11}$$

where g_{m5}, $R_{O4,O5}$, C_{04} and C_P are the transconductance of transistor M_5, the drain-source resistances in saturation, the capacitance at the delay stage output, and the parasitic capacitance towards the supply rail. As one can see, the influence of supply noise can be reduced by decreasing the transconductance of M_5.

Similar as in the case of the ring oscillator, supply noise also causes frequency and phase variations of the relaxation oscillator output signal. The relaxation oscillator is most sensitive in the instant of time when the comparator output changes from logic level low to high. When the current comparator switches, the output voltage exhibits a peak approaching the supply voltage level, which causes a change in the operating point of M_5. M_5 changes from the saturation operating region into the linear operating region, and hence the drain-source resistance decreases. Fig. 3.12 depicts the small-signal model of the comparator output stage while changing from logic level low to high. The output voltage reaches about 520 mV, and hence M_5 changes into the linear operating region. The drain-source resistance can therefore be approximated by [27].

$$R_{O5} = \frac{1}{\mu \cdot C_{OX}(V_{GS} - V_t)} \cdot \frac{L}{W}, \tag{3.12}$$

where μ, C_{OX}, V_{GS}, V_t, W and L are the charge carrier mobility, the oxide capacitance, the gate-source voltage, the threshold voltage, the transistor width and length, respectively.

By building the transfer function of the circuit in Fig. 3.12 one obtains

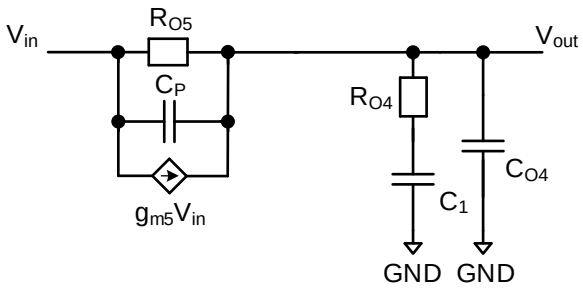

Figure 3.12: Equivalent small signal model of relaxation oscillator comparator output

$$\frac{V_{out}}{V_{in}} = \frac{Z_{O4}(1 + g_{m5} \cdot Z_{O5})}{Z_{O4} + Z_{O5}}, \tag{3.13}$$

with

$$Z_{O4} = \frac{1 + s \cdot C_1 \cdot R_{O4}}{s \cdot C_{O4} + s^2 \cdot C_1 \cdot C_{04} \cdot R_{O4} + s \cdot C_1}, \tag{3.14}$$

$$Z_{O5} = \frac{R_{O5}}{1 + s \cdot C_P \cdot R_{O5}}, \tag{3.15}$$

where g_{m5}, R_{O5}, R_{O4}, C_{04} and C_P are the transconductance of transistor M_5, the drain-source resistances in linear region of M_5, the drain-source resistances in the saturation region of M_4, the capacitance at the comparator output, and the parasitic capacitance towards the supply rail, respectively.

Similar as in case of the ring oscillator, the influence of the supply induced noise can be reduced by decreasing the transconductance of M_5. Another way of increasing the suppression of supply noise is to increase the W/L-ratio of the current comparator (M_3 and M_4 in Fig. 2.10). By increasing the W/L-ratio of M_3 and M_4, the peak value of the output voltage decreases, and thus M_5 can be maintained in the saturation operating region. It is not possible to increase the W/L-ratio of M_3 and M_4 arbitrarily because the comparator output voltage has to reach a level above the threshold voltage of the pulse generator logic to maintain a stable oscillation.

Fig. 3.13 depicts the frequency variation of the two oscillator implementations. As one can see, the frequency variation due to supply noise is much lower in the relaxation oscillator. This is due to the transistor M_5 which suppresses disturbances from the supply. The frequency variation of the relaxation oscillator due to supply noise is less than 1%.

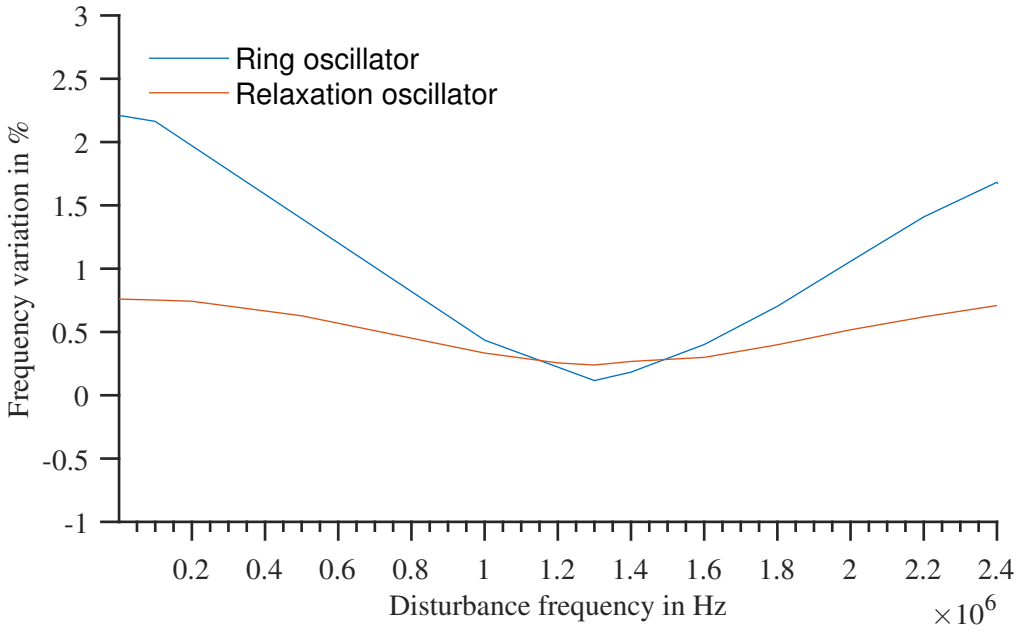

Figure 3.13: Max. frequency variation of the oscillators for a sinusoidal supply disturbance with 10 mV peak amplitude

3.2 Summary

One can see that the ring oscillator with integrated temperature compensation and the relaxation oscillator show a very similar behaviour with respect to frequency controllability, temperature stability, process and mismatch variations and phase noise. Nevertheless, the relaxation oscillator shows a superior power supply rejection and a lower power consumption. Therefore it was decided to focus on the relaxation oscillator concerning the implementation of the trimming circuit and physical layout.

3.3 Trimming circuit

3.3.1 Design considerations

As discussed in the previous section, the investigated ring oscillator as well as the relaxation oscillator show process and mismatch variations. To guarantee an output frequency that complies with the specifications, a trimming circuit is necessary. The trimming circuit allows a control of the bias current fed to the oscillator core, and thus an adjustment of the oscillation frequency to compensate for process and mismatch variations.

Furthermore, the trimming circuit is required to compensate bias current variations from the bias generation. As specified in Table 1.1, the oscillator must be able to cover a bias current spread of ± 50 %. If the trimming range is not sufficiently wide, the output frequency spread increases due to uncompensated bias current shifts.

Besides the static frequency trimming, the circuit also must provide a dynamic frequency control which allows the oscillator output frequency to be adjusted between ±5% in 5 defined steps. The dynamic frequency control requires the output frequency to be settled within 10 μs, as indicated in Table. 1.1.

In this section two trimming structures are presented. The trimming circuits basically work as current mode converters (DAC) with 6 bits. The minimal resolution corresponding to the lest significant bit (LSB) is defined by

$$LSB = \frac{I_{ref}}{2^N}, \tag{3.16}$$

where I_{ref} and N are the bias current from the bias generation and the number of bits, respectively.

A DAC is characterized by an offset and a gain error. Fig. 3.14 and Fig. 3.15 illustrate the influence of the offset and the gain error of a DAC.

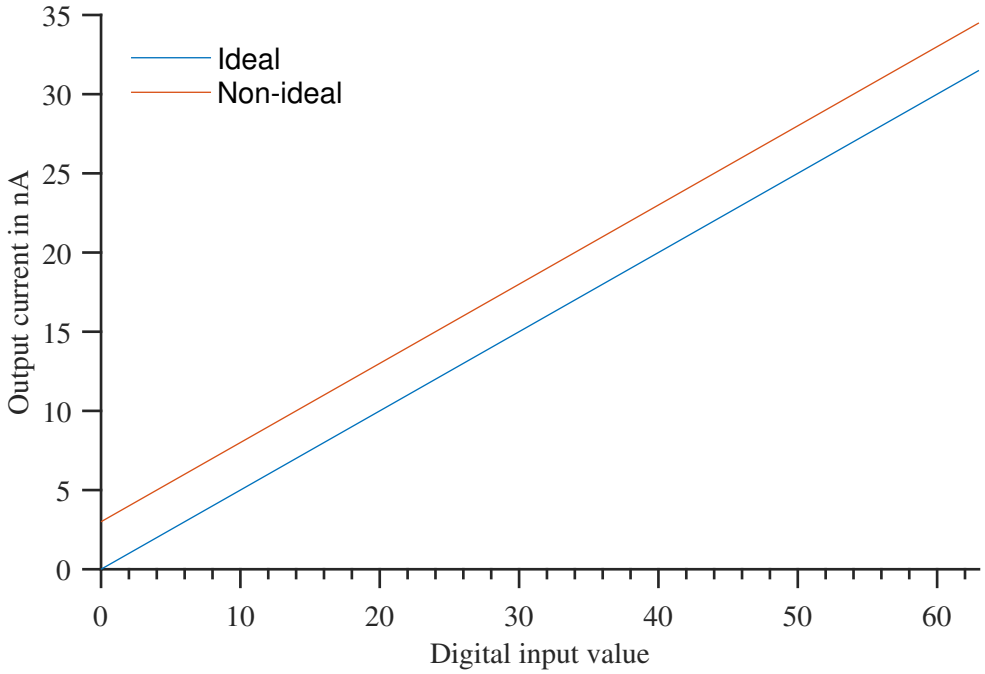

Figure 3.14: Offset error of current mode DAC

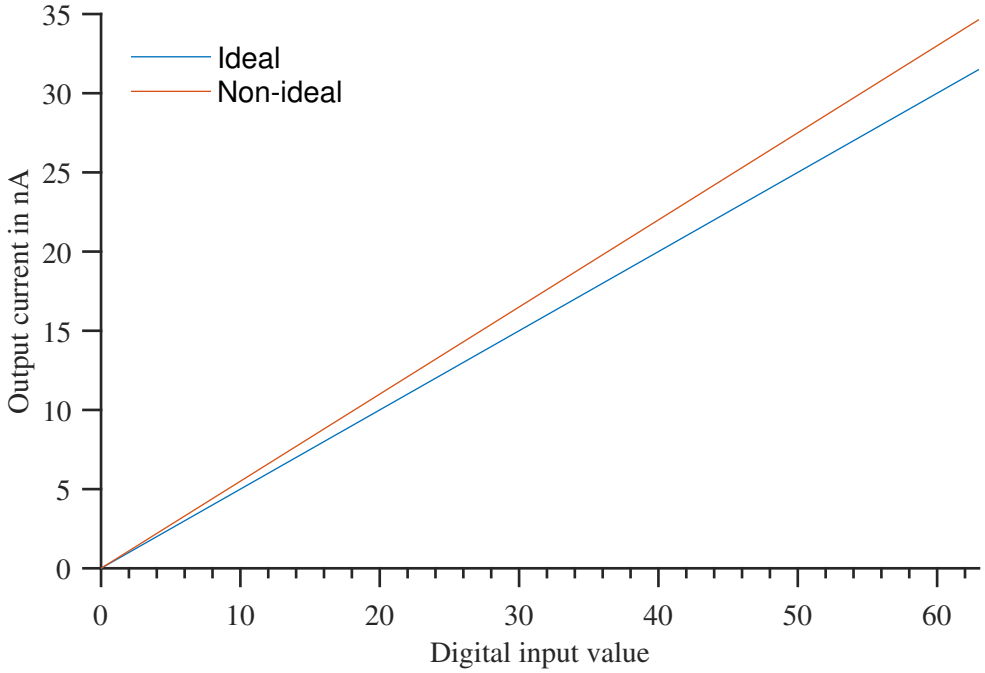

Figure 3.15: Gain error of current mode DAC

Offset and gain error need to be considered for analysing the differential non-linearity (DNL) of a DAC. The DNL describes the difference of the step sizes with reference to the ideal step size [39]

$$DNL = \frac{I_{n+1} - I_n}{I_{LSB}}, \tag{3.17}$$

where I_{n+1} and I_n are the current values corresponding to two consecutive digital values and I_{LSB} is the current value of the ideal LSB. If the $DNL > 1$, then missing codes are possible. Therefore, the DNL is a crucial parameter for the trimming accuracy.

In the following two trimming concepts are discussed. The first concept uses NMOS current mirrors for the trimming of the bias current. The trimming circuit uses NMOS switches to switch current branches to the output, which is fed to the oscillator core.

In contrast to the first concept, the second concept uses PMOS current mirrors for trimming the bias current. An additional NMOS current mirror is used to feed the bias current to the oscillator core.

3.3.2 Trimming architecture

Fig. 3.16 depicts the first trimming concept. The bias current is via M_1 mirrored to the other current branches. The current branches formed by transistors M_2 to M_7 are binary weighted and switchable via NMOS transistors M_8 to M_{13} to the output.

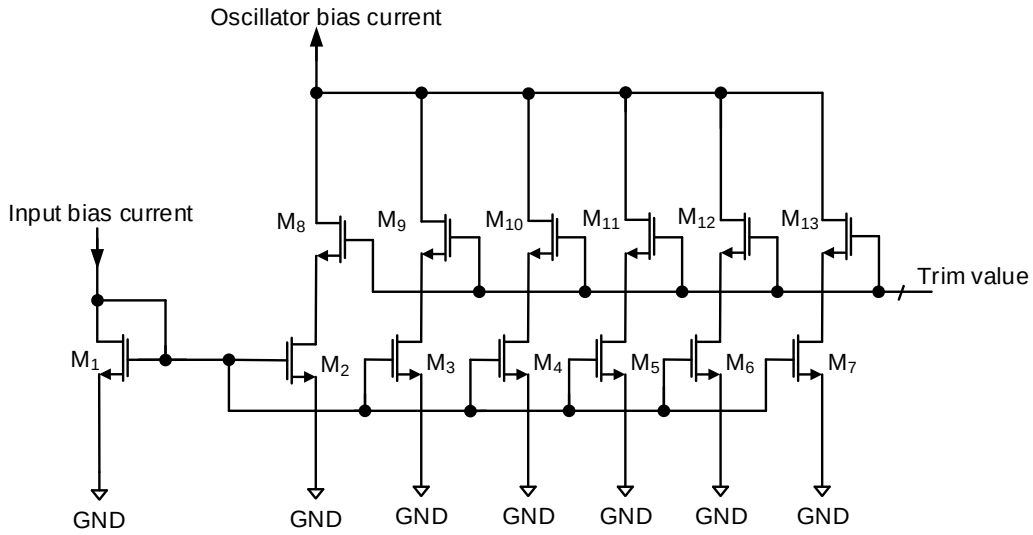

Figure 3.16: Trimming circuit with NMOS current mirrors

M_1 is implemented as a stack of 16 transistors. The transistor stacking is necessary to provide a dynamic frequency control within ± 5% during operations. After the trimming procedure is completed, the oscillator bias current and thus the frequency can be changed by controlling the number of stacked devices of M_1.

	W/L	Multiplier	Stacked devices
M_1	320nm/2.5μm	4	16
M_2	320nm/2.5μm	4	10
M_3	320nm/2.5μm	2	10
M_4	320nm/2.5μm	1	10
M_5	320nm/2.5μm	1	20
M_6	320nm/2.5μm	1	40
M_7	320nm/2.5μm	1	80
$M_{8,..,13}$	500nm/150nm	1	1

Table 3.7: Design parameters of the NMOS current mirror trimming circuit

As one can see in Table 3.7, the total amount of needed transistors is large, which increases the required layout area. Furthermore, the capacitance at the gate node of M_1 increased by the parasitic capacitances of transistors M_2 to $M7$. The parasitic capacitance has a negative impact on the frequency settling time. After a frequency change is initiated, the charge of the parasitic capacitances has to balance before the oscillator output frequency settles. The frequency settling time is proportional to the capacitance at the gate node of M_1. Fig. 3.17 illustrates the frequency settling behaviour after initiating a dynamic frequency change of 5 %. The frequency settles after approximately 30 μs, which exceeds the specified settling time of 10 μs, as shown in Table 1.1.

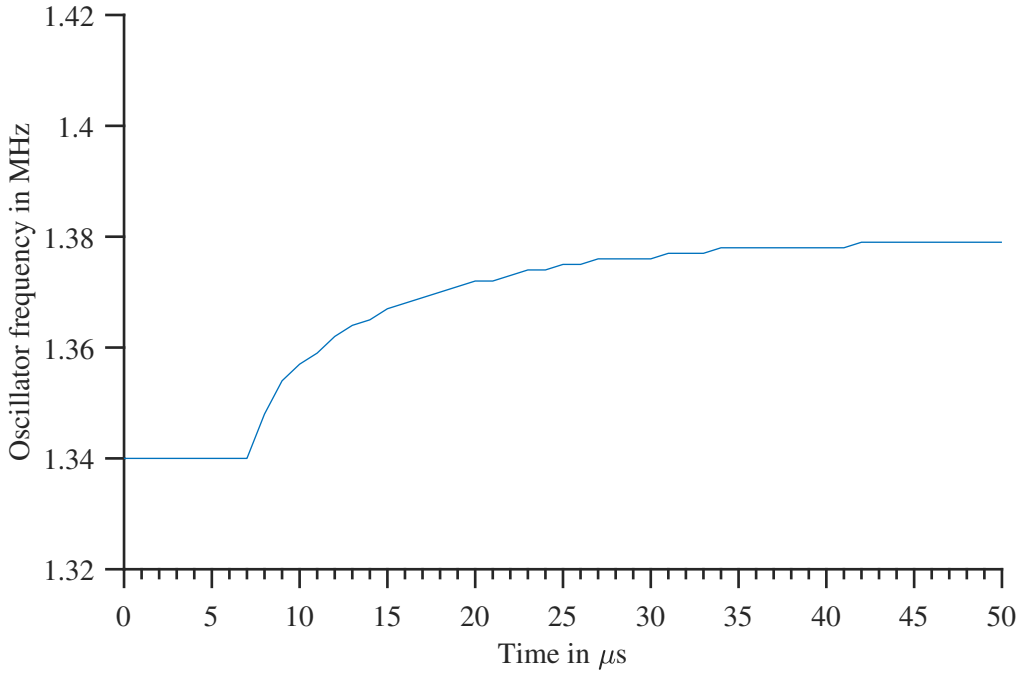

Figure 3.17: Frequency settling behaviour after initiating a frequency change of 3 % using NMOS trimming circuit)

A different circuit concept, which allows a reduction of the frequency settling time is depicted in Fig. 3.18. The new concept uses PMOS current mirrors for trimming and an additional NMOS current mirror to implement a dynamic frequency control.

As shown in Table 3.8 the circuit compromises a low number of transistors in comparison to the NMOS trimming circuit, resulting in a lower layout area. The settling time is determined by the NMOS current mirror formed by transistors M_8 and M_9. M_8 is implemented by a controllable number of stacked devices, which enable a dynamic frequency control of $\pm$ 5 %. Since the parasitic capacitance at the gate node of M_8 is low, the oscillator frequency settles fast after a frequency change is initiated. Fig. 3.19 depicts the settling behaviour of am applied 5 % frequency change using the PMOS current mirror trimming circuit. As shown, the frequency settles after 5 μs, which complies to the specified settling time of 10 μs (see Table 1.1).

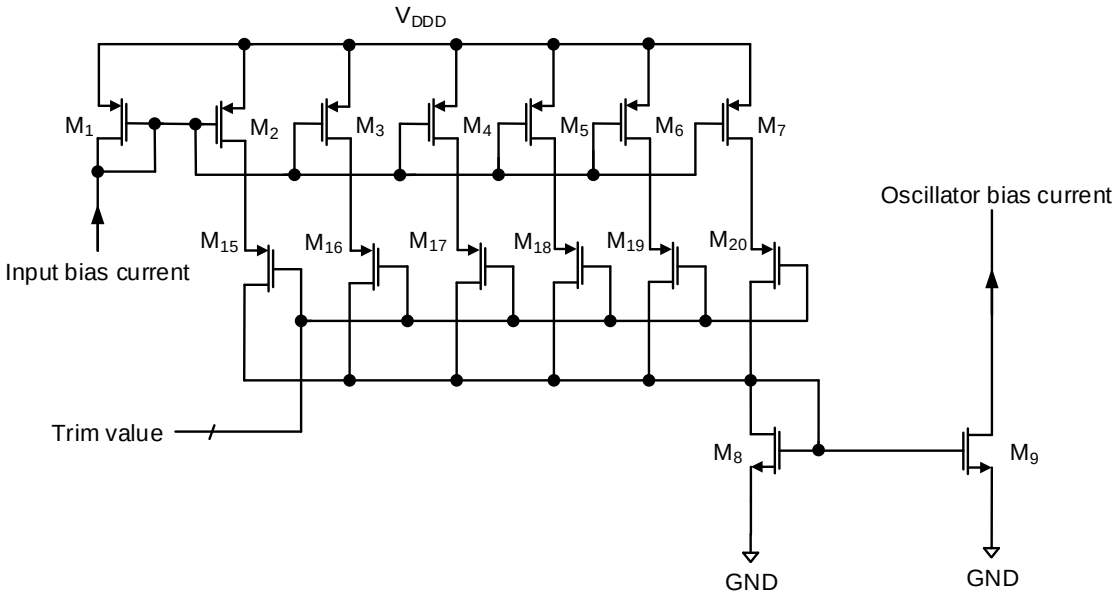

Figure 3.18: Trimming circuit with PMOS current mirrors

	W/L	Multiplier	Stacked devices
M_1	320nm/10μm	4	1
M_2	320nm/10μm	4	1
M_3	320nm/10μm	2	1
M_4	320nm/10μm	1	1
M_5	320nm/10μm	1	2
M_6	320nm/10μm	1	4
M_7	320nm/10μm	1	8
M_8	320nm/2μm	1	15
M_9	320nm/2μm	1	10
$M_{15,..,20}$	500nm/150nm	1	1

Table 3.8: Design parameters of the PMOS current mirror trimming circuit

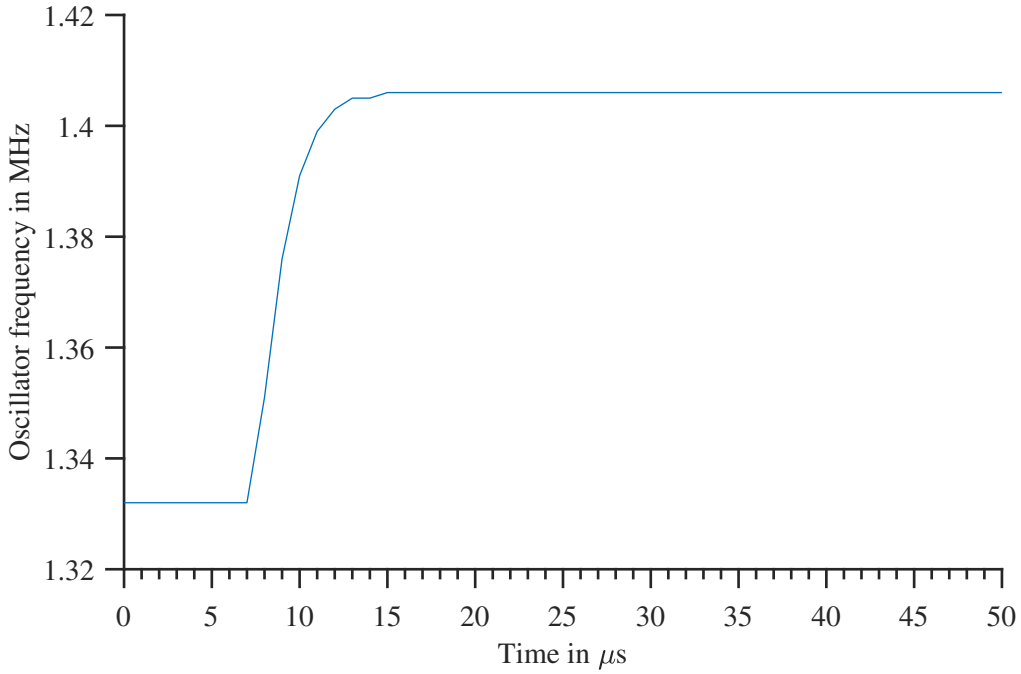

Figure 3.19: Frequency settling behaviour after initiating a frequency change of 5 % using PMOS trimming circuit

3.3.3 Differential non-linearity (DNL)

As discussed in Sect. 3.3.1, the DNL is a parameter, which represents the trimming accuracy. A $DNL < 1$ is preferable to achieve a high trimming accuracy. By considering the values from Table 3.7 and (3.16), and assuming a bias current of 12.5 nA and a 6 bit digital trim value, one obtains

$$LSB = \frac{I_{Bias}}{2^N} \cdot \frac{S_1}{S_2} = 312 \text{ pA}, \tag{3.18}$$

where S_1 and S_2 are the W to L ratios of the transistors M_1 and M_2.

Fig. 3.20 and Fig. 3.21 depict the digital-to-analog transfer functions of the trimming circuits. As shown, the output current follows proportionally the digital trim value. Due to leakage currents of the switches, the effective LSB values of the NMOS and the PMOS trimming circuits increases to

$$LSB_{nmos} = \frac{I_{63} - I_0}{64} = 439 \text{ pA}, \tag{3.19}$$

$$LSB_{pmos} = \frac{I_0 - I_{63}}{64} = 438 \text{ pA}, \tag{3.20}$$

respectively. I_{63} and I_0 in (3.19) and (3.20) are the output currents corresponding to the digital trim values 63 and 0 in Fig. 3.20 and Fig. 3.21.

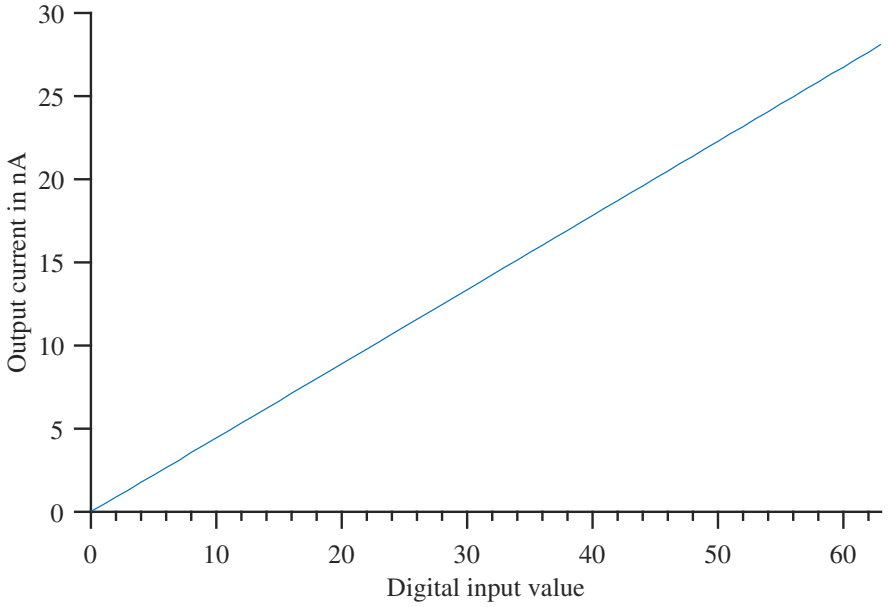

Figure 3.20: Transfer function of the trimming circuit with NMOS currents mirror

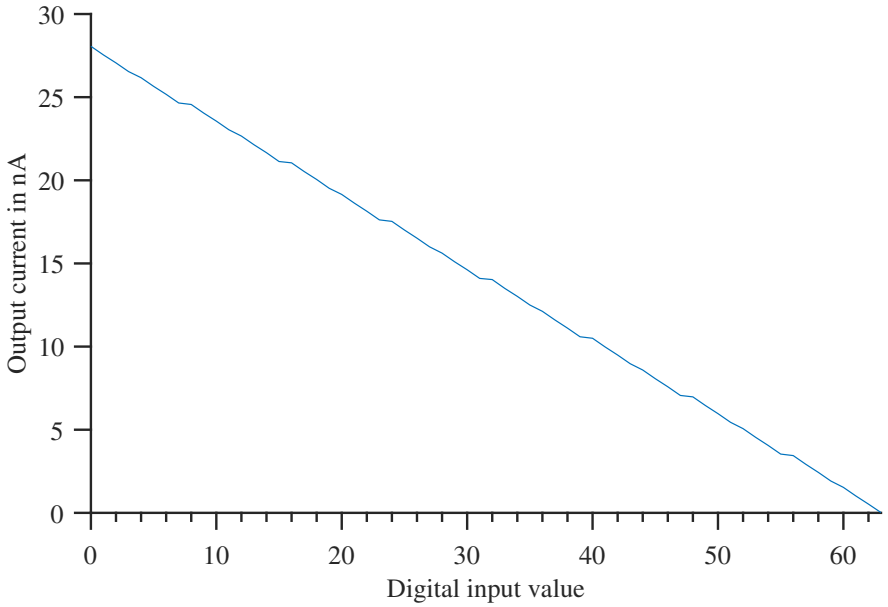

Figure 3.21: Transfer function of the trimming circuit with PMOS current mirrors

The current conducted by the individual current branch varies due to mismatch variations, and thus the step intervals vary. Fig. 3.22 and Fig. 3.23 illustrate the influence of process and mismatch on the DNL by means of Monte Carlo simulations.

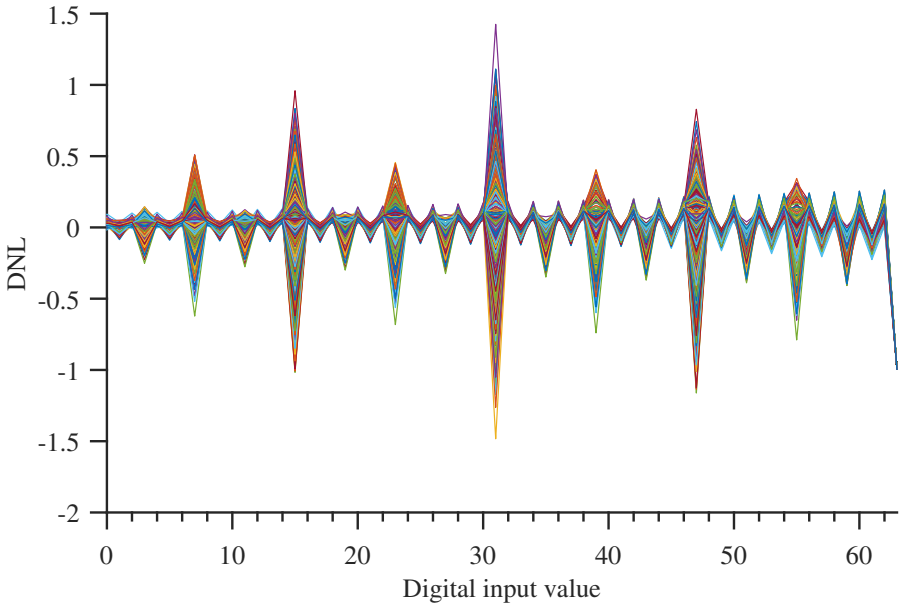

Figure 3.22: DNL of the trimming circuit with NMOS current mirrors

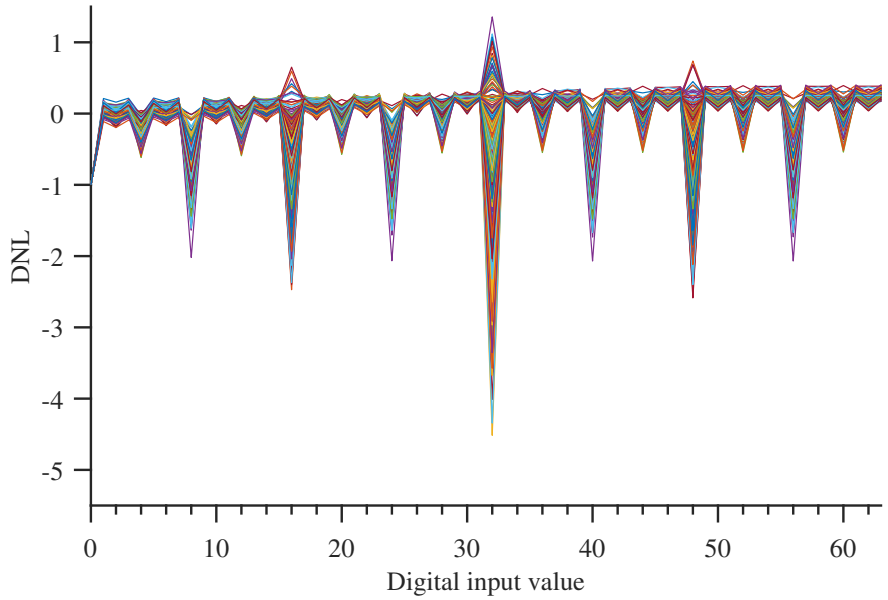

Figure 3.23: DNL of the trimming circuit with PMOS current mirrors

3.3.4 Summary

The presented trimming circuit using NMOS current mirrors shows better DNL characteristic with respect to process and mismatch variations and thus a higher trimming accuracy. Nevertheless, the circuit shows a slow settling time in response to an initiated frequency change and does not meet the requirement of a settling time lower than 10 μs. Therefore the trimming circuit using PMOS current mirrors is used for verifying the oscillator.

3.4 Layout

3.4.1 Oscillator

The focus in this section is on the layout implementation of the sensitive parts of the design. Fig. 3.24 depicts the relaxation oscillator core without the pulse generating logic. Additional dummy devices to improve the transistor matching are included in the layout. The most sensitive parts in the design are the reference voltage generation (M_1, M_2), the bias transistors (M_5, M_7, M_8) and the current comparator (M_1, M_2), since they directly influence the output frequency. In addition, the layout of the pulse generating logic was designed to minimize parasitic capacitances and thus to keep the switching delay low.

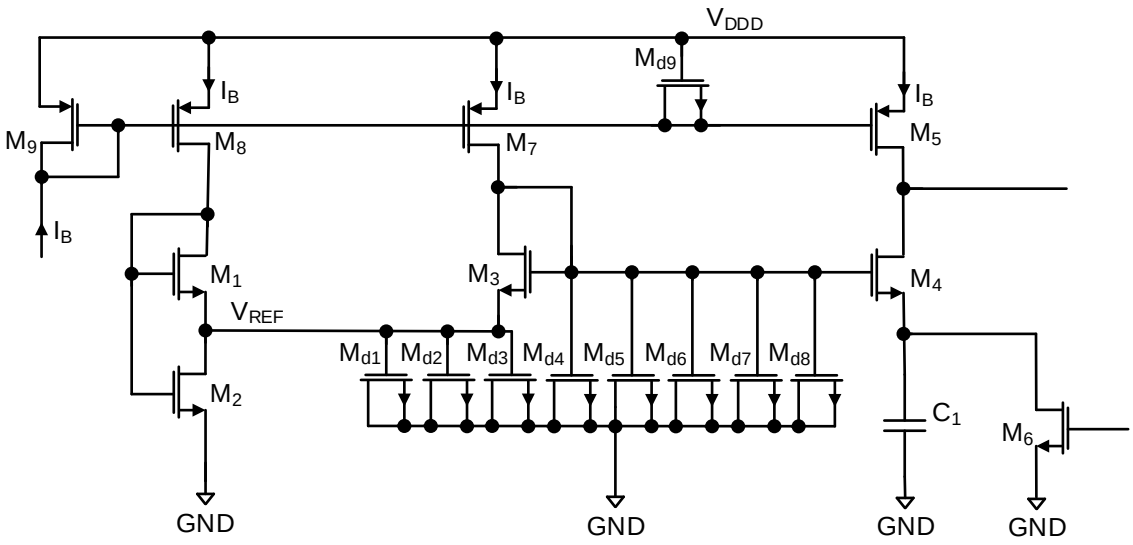

Figure 3.24: Implementation of the oscillator shown in Fig. 2.8

Fig. 3.25 depicts the layout of the reference voltage generation. Transistors, which are placed in the middle of the structure, have neighbouring devices on each side. Transistors at the edge of the device array do not have a neighbouring device on one side. Therefore, dummy devices are included to avoid a systematic mismatch of transistor characteristics.

The well proximity effect (WPE) needs to be considered in circuit layouts in this technology, since it can significantly alter the characteristic of MOS transistors [40]. The well proximity effect has a major impact on the transistor threshold voltage up to a distance of 1 μm [40], hence for the oscillator layout a minimum distance of 1.5 μm to the well edges is chosen.

As shown in Table 3.2, M_1 and M_2 are formed by a total number of 35 devices. To optimize the layout area, the matching devices are placed in a 5x7 grid. A total number of 28 dummy devices is included to achieve a good device matching.

A mismatch between the transistors M_3 and M_4 causes an offset voltage, which alters the switching point. Fig. 3.26 depicts the layout of the current comparator structure. To suppress voltage ripples on the common gate node, the MOS capacitors M_{d6}, M_{d7} and M_{d8} are added. Additionally, the dummies M_{d3} and M_{d4} are added to improve device matching.

The bias current of the reference generation and the current comparator is provided by transistors M_5, M_7 and M_8. Mismatches between the current mirror branches result in a

current comparator offset and a variation of V_{REF}. Four additional dummy devices (M_{d9}) are included (two on each site) to reduce the current mismatch. Table 3.9 summarizes the design parameters of the included dummy devices.

	W/L	Multiplier
M_{d1}	500nm/1μm	10
M_{d2}	1μm/500nm	14
M_{d3}	500nm/500nm	4
M_{d4}	320nm/1μm	4
M_{d5}	320nm/2μm	3
M_{d6}	3.28μm/1μm	2
M_{d7}	3.2μm/1μm	4
M_{d8}	3.2μm/2μm	2
M_{d9}	320nm/10μm	4

Table 3.9: Design parameters of dummy devices

Fig. 3.27 depicts the layout of the reference capacitor C_1 and the discharge transistor M_6. C_1 is placed on top of M_6 to save area. C_1 is implemented as a metal fringe capacitor using metal layers number two and four.

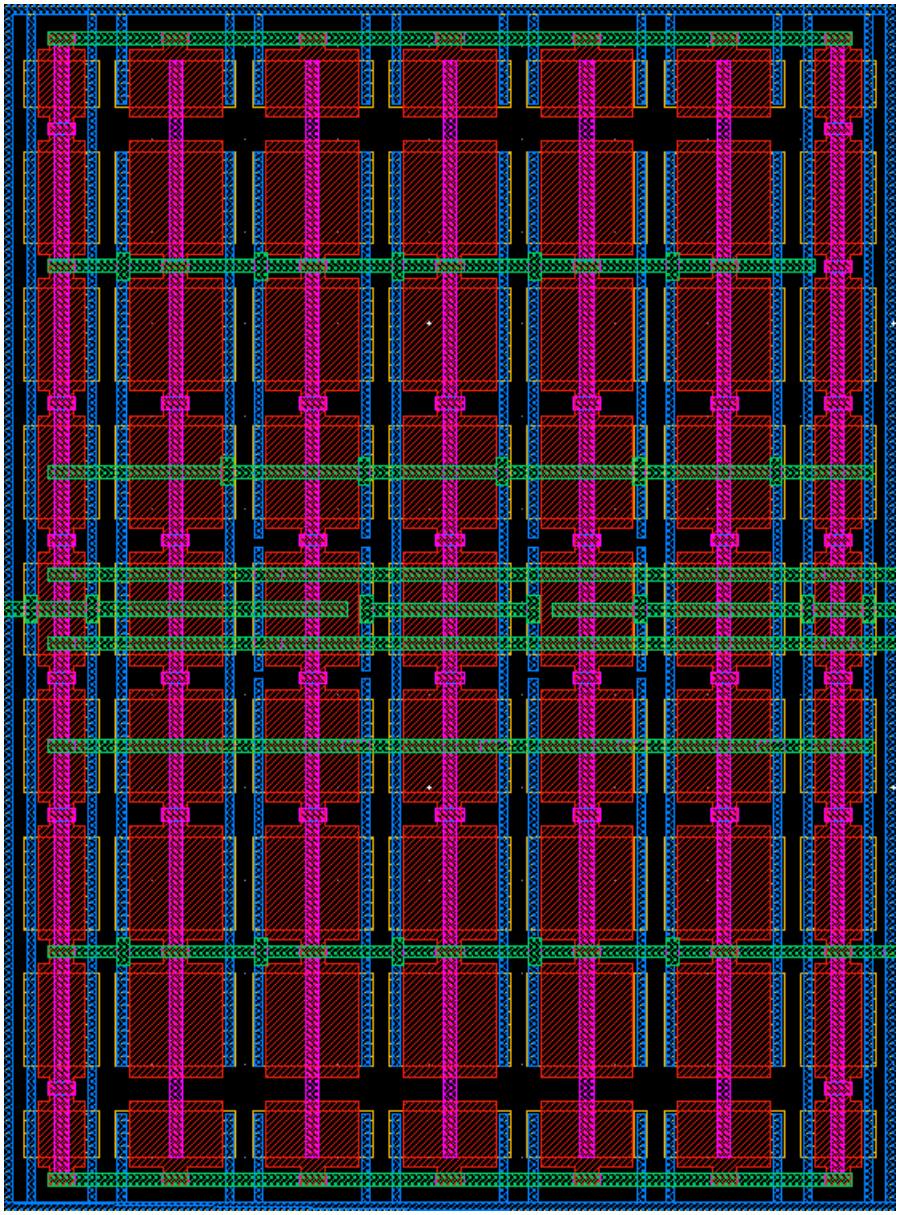

Figure 3.25: Layout of the reference generation

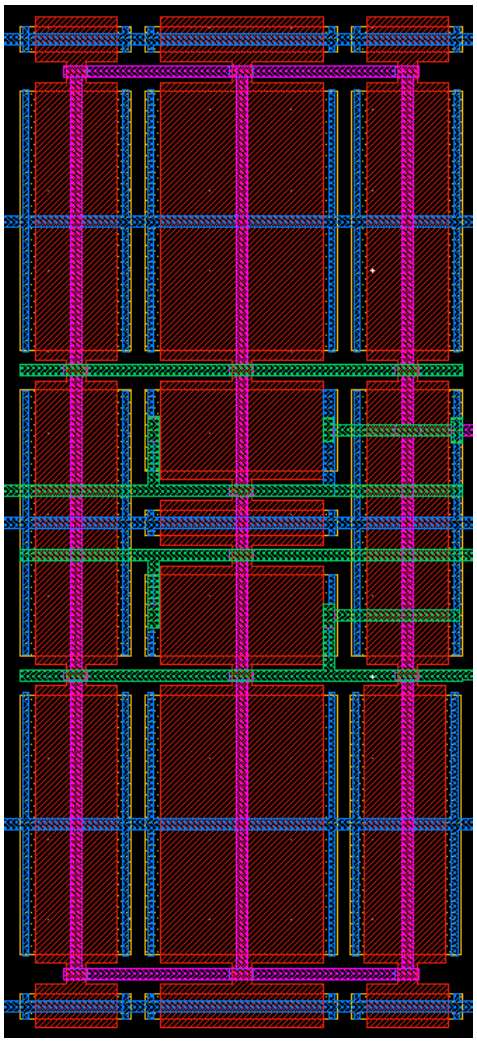

Figure 3.26: Layout of the current comparator

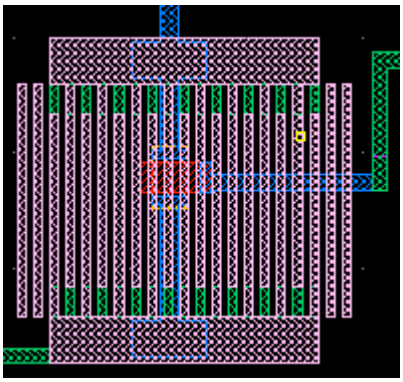

Figure 3.27: Layout of the reference capacitor and the discharge transistor

Fig. 3.28 depicts the complete oscillator layout. The overall area is 420 μm^2. As one can see, the reference voltage generation, the current comparator and the bias current mirrors need most of the area.

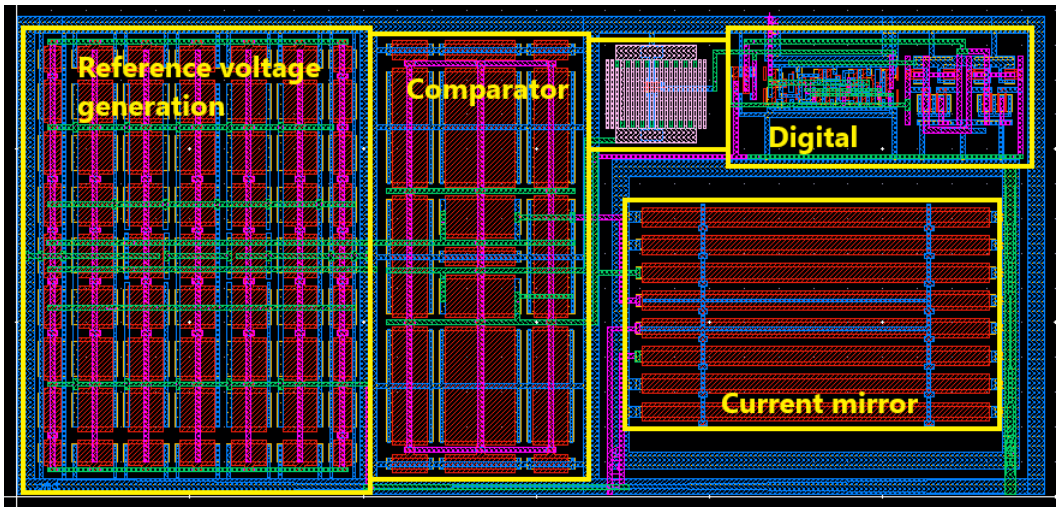

Figure 3.28: Layout of the relaxation oscillator

3.4.2 Trimming circuit

Fig. 3.29 depicts the implementation of the trimming circuit including the dummy devices for optimizing device matching in the layout. Table 3.10 summarizes the design parameters of the dummy devices included the trimming circuit.

	W/L	Multiplier
M_{d1}	320nm/10μm	3
M_{d2}	320nm/2μm	5
M_{d3}	320nm/500nm	60

Table 3.10: Parameters for dummy devices

The device matching of the current mirrors formed by M_1 to M_7 is crucial because current matching influences the DNL. Therefore, the frequency trimming accuracy depends on the matching accuracy.

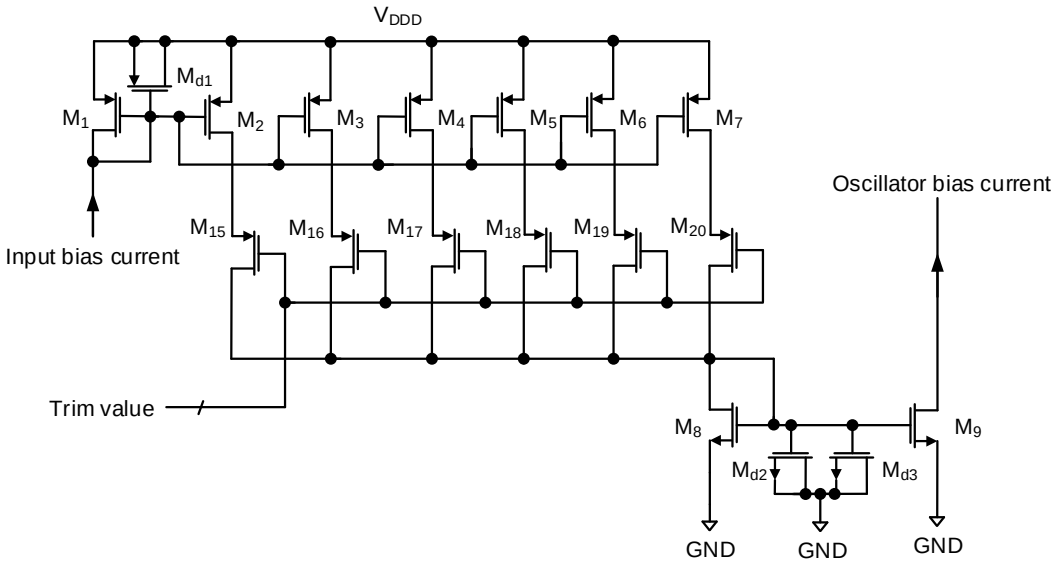

Figure 3.29: Implementation of the trimming circuit in Fig. 3.18, including dummy devices

The NMOS current mirror formed by transistors M_8 and M_9 is critical with respect to the accuracy and the settling time of the dynamic frequency control of the oscillator. The stacked transistors of M_8 are sensitive to capacitive coupling to digital input control lines. Therefore, special attention is paid to the routing of the control lines to minimize the coupling to the drain and source terminals of the stacked transistors.

Fig. 3.30 depicts the layout of the PMOS current mirrors (M_{1-7}) of the trimming circuit. For symmetry reasons, three additional dummy PMOS devices are added to achieve a good matching structure.

As shown in Fig. 3.31, the NMOS current mirror comprising M_8 and M_9 is surrounded by 64 dummy devices to achieve a symmetrical layout structure. The digital control lines routed over the transistor gates enable a change of the effective number of stacked devices, and thus a dynamic control of the oscillator frequency during operations.

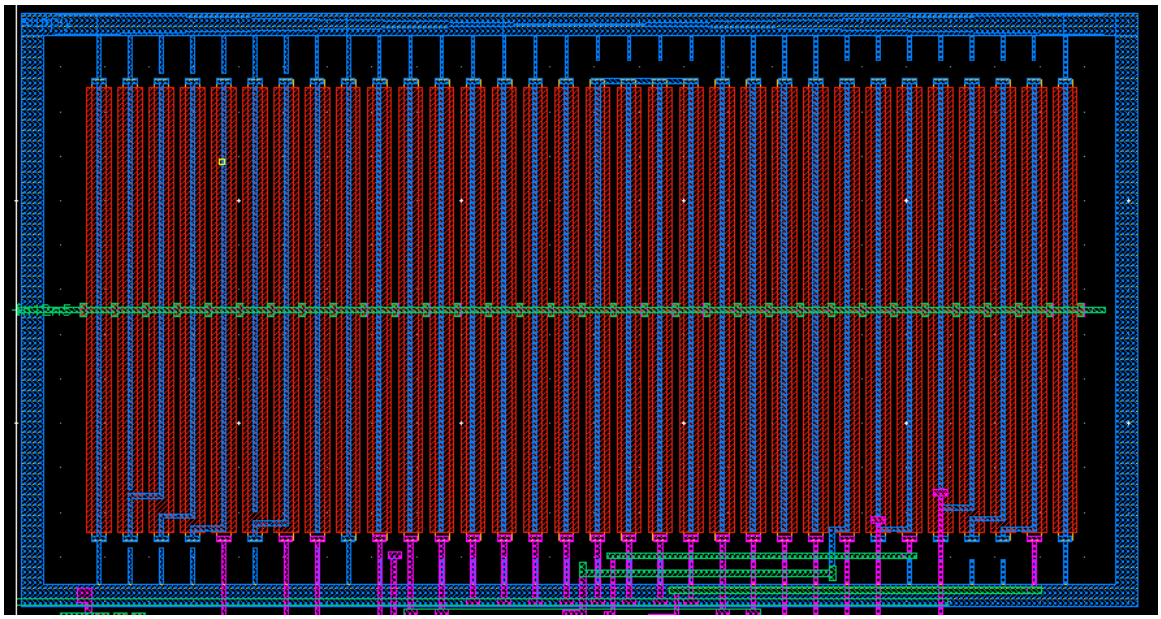

Figure 3.30: Layout of the PMOS current mirror of the trimming circuit

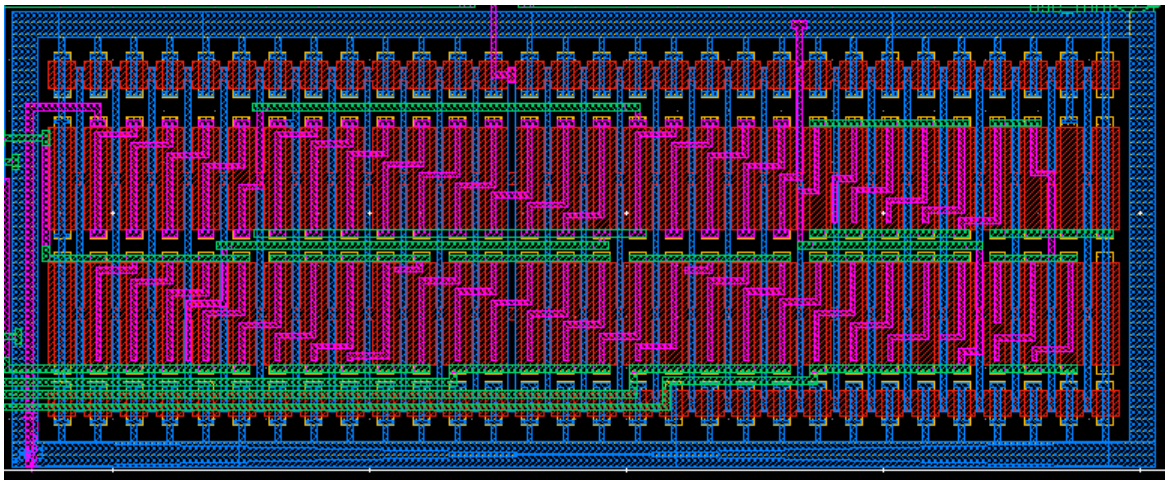

Figure 3.31: Layout of the NMOS current mirror of the trimming circuit

Fig. 3.32 depicts the complete layout of the trimming circuit. The total area is 1500 μm^2. The digital logic controlling the number of stacked devices of M_8 includes two NAND gates, two NOR gates and five NMOS switches. The control logic is located in the lower left corner in Fig. 3.32.

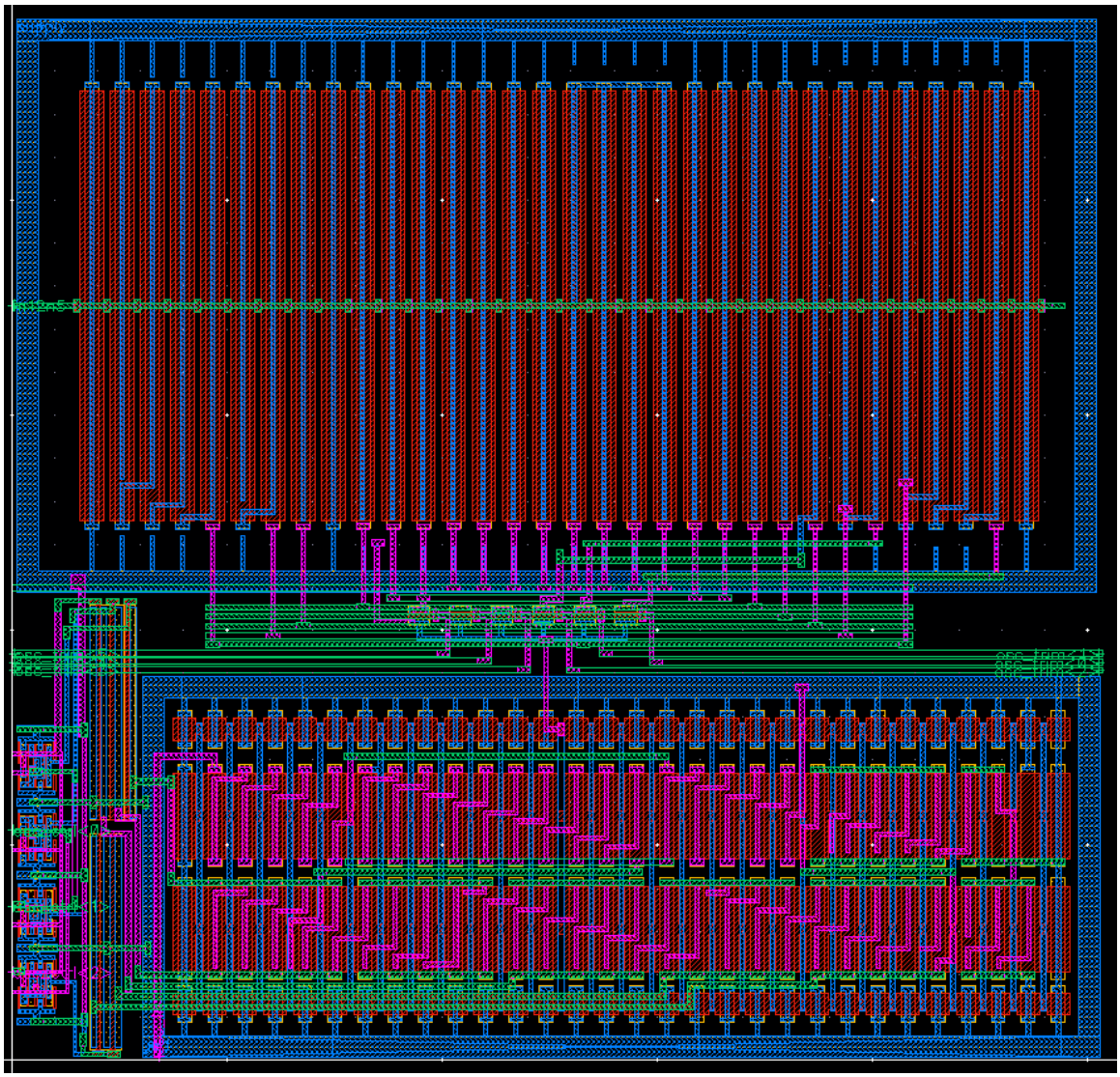

Figure 3.32: Layout of the trimming circuit

3.5 Summary

The implementations of the temperature compensated ring oscillator and the relaxation oscillator, which were introduced in Ch. 2, perform similar regarding temperature stability, phase noise, and the frequency accuracy versus process and mismatch variations. Nevertheless, the performance of the relaxation oscillator shows clear advantages in terms of power consumption and the suppression of supply disturbances. The difference in the power consumption becomes even more significant by considering parasitic capacitances. Furthermore, the relaxation oscillator exhibits a lower sensitivity with respect to parasitic capacitances, which simplifies the layout design.

The two investigated trimming circuits show a sufficient performance regarding the trimming accuracy. Nevertheless, the trimming circuit using only NMOS current mirrors shows an exhaustive settling time after a frequency change is initiated exceeding the specific limit of 10 μs. In contrast, the second trimming circuit, which uses PMOS current mirrors for the static frequency trimming, achieves a settling time lower than 10 μs for dynamic frequency changes applied during operations.

Chapter 4

Verification results

In the previous chapter the circuit implementations of the temperature compensated ring oscillator and the relaxation oscillator were introduced. As discussed, the relaxation oscillator shows a superior performance regarding power consumption and power supply rejection. Furthermore, two trimming circuits were implemented and as discussed, the trimming circuit using PMOS current mirrors is required for compliance with the frequency settling time specified in Table 1.1. Finally, the circuit layouts of the oscillator and trimming circuit were discussed.

This chapter focuses on the verification of the implemented oscillator including the frequency trimming circuit. For the verification of the oscillator and the trimming circuit a parasitic extracted netlist of the layouts depicted in Fig. 3.28 and Fig. 3.32 is used.

The verification is performed regarding the parameters: frequency controllability, temperature stability, power consumption, frequency accuracy versus process and mismatch variations, phase jitter and power supply rejection. Two simulation test benches are used to verify the performance characteristics of the oscillator.

4.1 Simulation test benches

Fig. 4.1 shows a block diagram of the used test bench to evaluate the transient behaviour of the oscillator design. The supply voltage is regulated by a voltage regulator, which is supplied by a 1 V input voltage. The regulator is trimmed to obtain a nominal output voltage of $V_{DDD} = 0.6$ V at 27 °C. A Verilog-A model, with a 3-bit digital output bus is used for the regulator output voltage V_{DDD}. V_{DDD} changes with process variations and temperature shifts and its maximum and minimum values range from 520 mV to 680 mV.

The bias current is generated by a current source, which provides a Gaussian distributed current with a nominal value of 12.5 nA and a standard deviation σ of 2 nA. The bias

current is fed into the trimming block, which controls the oscillator. Besides compensating bias current variations, the trimming circuit compensates process and mismatch variations of the oscillator core. The trimming circuit uses a 6-bit digital input bus to trim the bias current of the oscillator. The trimming control is performed by a Verilog-A model with a 6-bit digital output bus.

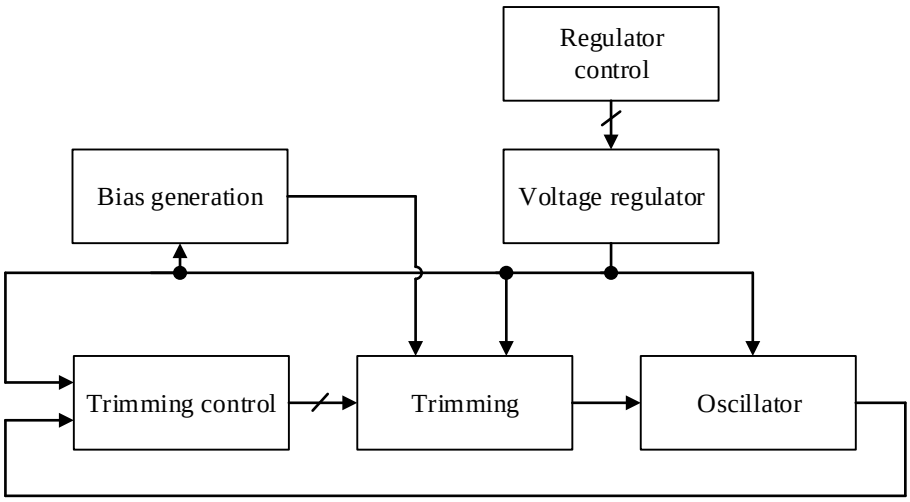

Figure 4.1: Test bench for the transient characterization of the oscillator

Fig. 4.2 and Fig. 4.3 illustrate the trimming procedure. The trimming procedure is performed at 27 °C and it starts after the supply voltage and the bias current are settled. A successive approximation algorithm is used to perform the frequency trimming, starting from the most-significant-bit (MSB) of the trimming word.

During the trimming procedure the oscillator may need more than 10 μs to settle. To avoid inaccurate trim values a settling time of 30 μs is considered. The trimming control measures the oscillator output frequency and compares it to a target frequency of 1.312 MHz. The trim value corresponding to the 6-bit digital output bus is initialized with a value equal to 32 ($MSB = 1$). If the current trim value results in a frequency higher than the target frequency, the trim value will be update to

$$trim\ value_{n+1} = trim\ value_n + \frac{32}{n+1}, \tag{4.1}$$

where n is the current trimming step.

After the successive approximation procedure is performed, the oscillator frequency is checked again. If the frequency is lower than the target frequency, the previous trim value is restored and (4.1) is applied again. The trimming procedure takes in total 6 cycles to determine the trim value for the oscillator.

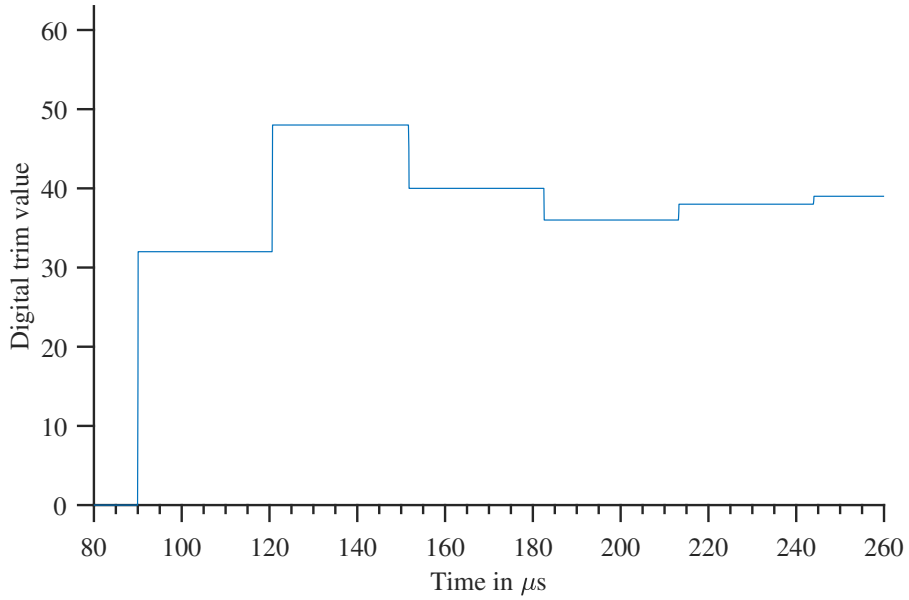

Figure 4.2: Successive approximation of the digital trim value of the oscillator frequency

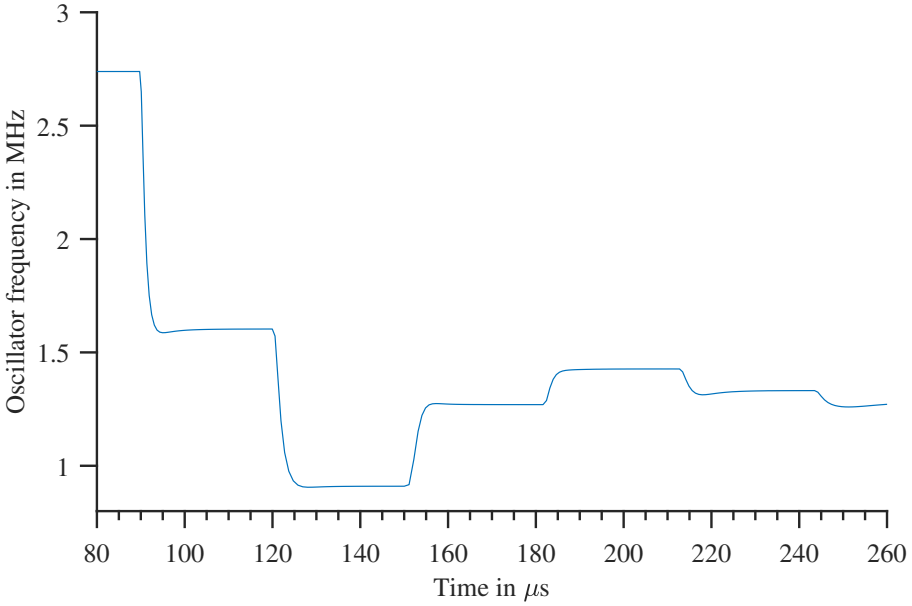

Figure 4.3: Successive approximation of the oscillator frequency

Fig. 4.4 shows the simulation test bench, which is used for the characterization of the phase noise and the power supply rejection. The test bench includes the oscillator circuit, a DC supply voltage $V_{DDD} = 600$ mV, and a bias current $I_B = 22$ nA, which results in an oscillator output frequency of 1.312 MHz. A sinusoidal voltage source with an amplitude of $V_{sin} = 10$ mV is used to evaluate the impact of supply voltage variations.

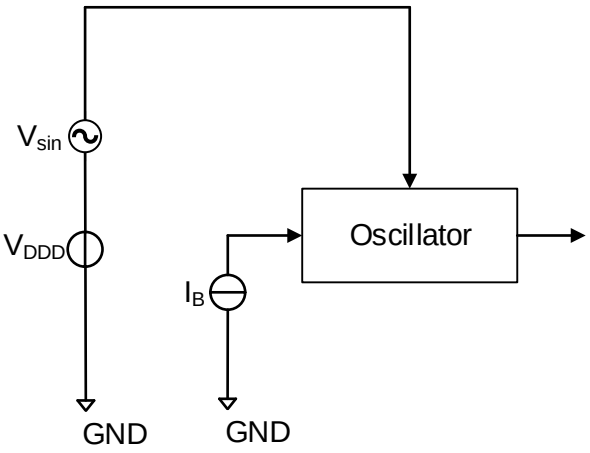

Figure 4.4: Test bench for simulating phase noise and power supply rejection

4.2 Frequency controllability

As implied by (2.21), the oscillator frequency is a function of the capacitance connected to the non-inverting input of the current comparator. The layout introduces parasitic capacitances, and thus the trimming circuit has to provide a higher current to compensate the additional capacitance.

The characteristics of the oscillator frequency versus the bias current, were simulated and plotted in Fig. 4.5 to evaluate the frequency controllability. Table 4.1 summarizes the frequency controllability of the oscillator for schematic and extracted netlist simulations.

	Schematic	Extracted
	kHz/nA	kHz/nA
$\Delta f/\Delta I_B$	76	45

Table 4.1: Frequency controllability with respect to the bias current at a frequency of 1.312 MHz

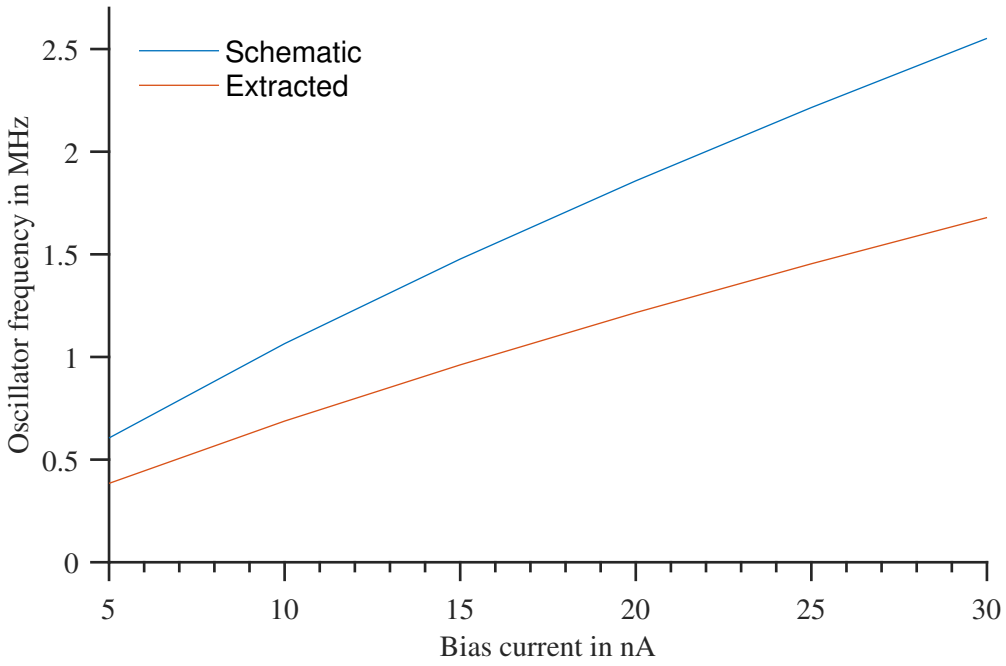

Figure 4.5: Frequency of the relaxation oscillator versus the bias current for schematic and extracted netlist simulations

To compensate the decreased frequency gain versus bias current, the LSB in the trimming circuit is increased by a factor of 2.5. Therefore, the new LSB is equal to 775 pA.

4.3 Temperature behaviour

Fig. 4.6 depicts the frequency deviation versus a varying temperature. The frequency is normalized to the nominal frequency $f = 1.312$ MHz. As shown, the frequency variation increased due to parasitic capacitances of the layout to about $\pm$ 2 %. The relative temperature drift is less than 320 ppm/°C.

The increase of the temperature induced frequency variation is caused by the increased capacitance at the comparator output, which effectively increases the delay of the pulse generating logic (see Fig. 2.8).

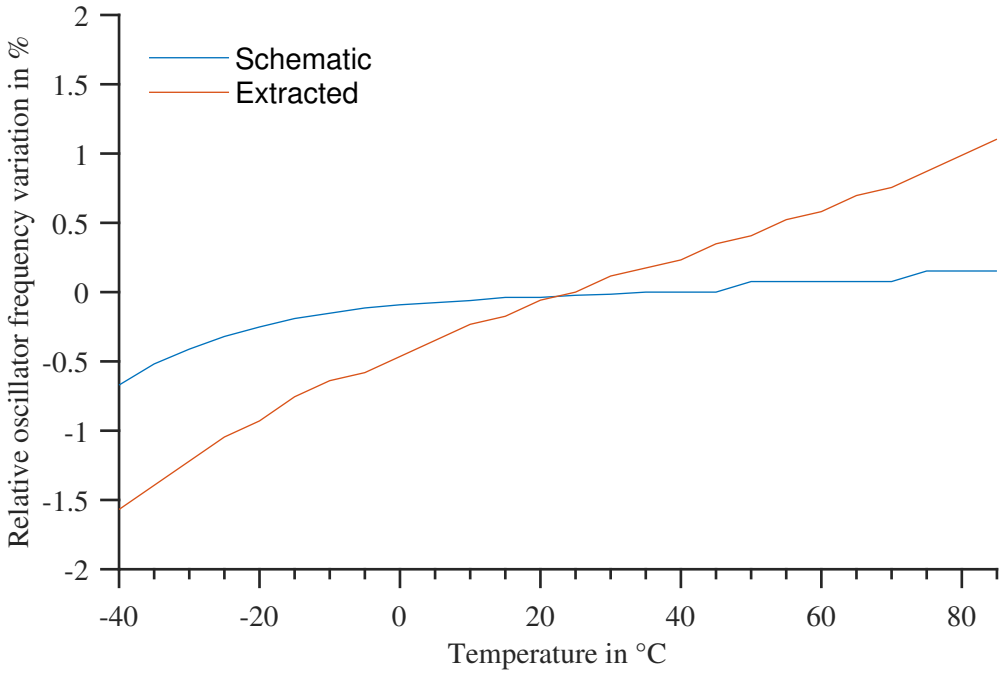

Figure 4.6: Normalized frequency of the relaxation oscillator over temperature

4.4 Power consumption

Table 4.2 summarizes the current consumption of the oscillator resulting from schematic and extracted netlist simulations. The current consumption increased from 75 nA to 135 nA. The increased current consumption observed in extracted netlist simulations is a result of the reduced frequency gain versus the bias current due to the additional parasitic layout capacitances.

	Current consumption
Schematic	75 nA
Extracted	135 nA

Table 4.2: Power consumption of the relaxation oscillator for schematic and extracted netlist simulations

The current consumption of the oscillator considering parasitic layout capacitances is lower than the specified current consumption of 140 nA, in Table 1.1.

4.5 Process and mismatch variations

To evaluate the sensitivity towards mismatch and process variations, a Monte Carlo (MC) simulation using the Latin Hypercube sampling method and 400 simulation runs is performed. The trimming of the oscillator frequency is performed for each MC run at room temperature (27 °C). The trimming accuracy of the least significant bit (LSB) is equal to 775 pA. The bias current deviation reaches up to ± 3 σ for 400 MC runs corresponding to a bias current spread of ± 50 %. The design must comply with the specifications in Table 1.1 considering process mismatch and temperature variations.

Table 4.3 summarizes the maximum, minimum and mean frequency observed in MC simulations at a temperature of -40 °C, 27 °C, and 85 °C. Furthermore, included is the standard deviation of the frequency.

The upper and lower limit for the output frequency are defined by ± 10% of the nominal value, which equals 1.18 MHz and 1.443 MHz, respectively. The specified upper and lower limits are not exceeded. The values in Table 4.3 correspond to the histograms of the oscillator frequency depicted in Fig. 4.7, Fig. 4.8 and Fig. 4.9.

Temperature	Max.	Min.	Mean	Std. dev.
°C	MHz	MHz	MHz	kHz
-40	1.238	1.361	1.29	18.77
27	1.31	1.363	1.33	12.36
85	1.273	1.392	1.334	22.78

Table 4.3: Maximum, minimum, and mean value of the frequency variation due to process and mismatch variations

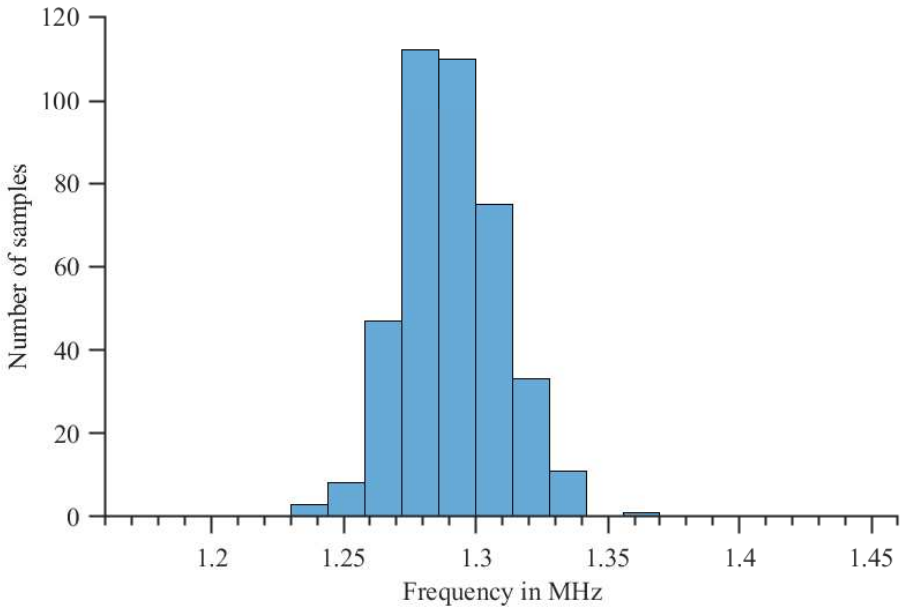

Figure 4.7: Relaxation oscillator process and mismatch variations considering layout parasitic effects at -40 °C after the trimming procedure

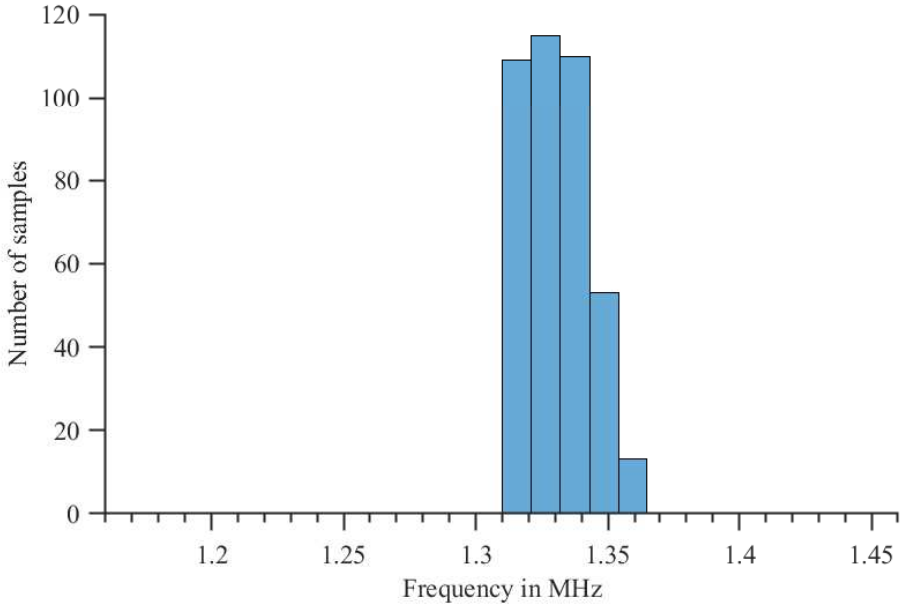

Figure 4.8: Relaxation oscillator process and mismatch variations considering layout parasitic effects at 27 °C after the trimming procedure

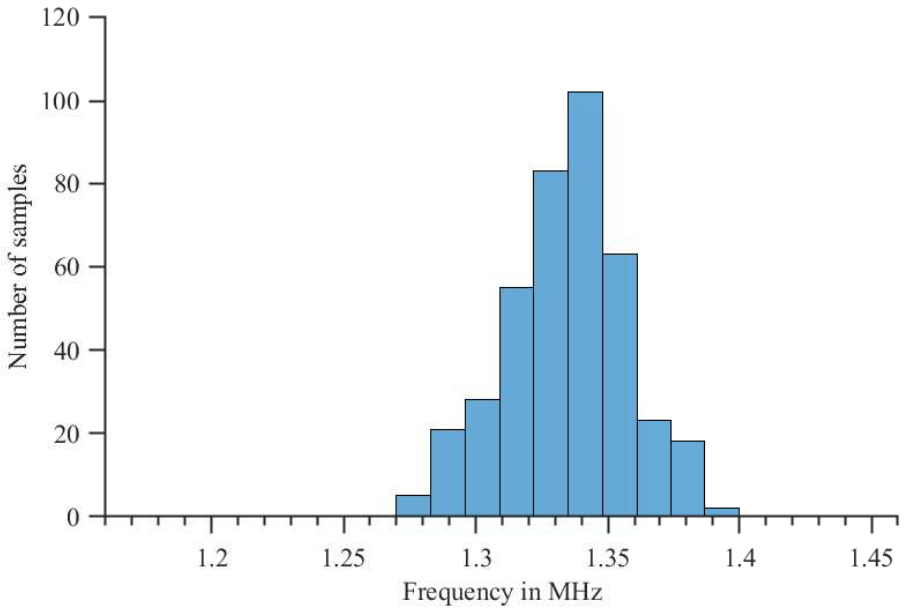

Figure 4.9: Relaxation oscillator process and mismatch variations considering layout parasitic effects at 85 °C after the trimming procedure

4.6 Phase noise

Table 4.4 and Table 4.5 summarize the phase noise induced period jitter for schematic and layout-extracted netlist simulations. The period jitter observed in extracted netlist simulations is reduced. This reduction is a result of the higher oscillator bias currents required to compensate for the additional parasitic capacitances.

As described in Ch. 3, the jitter is simulated using time-averaged and sampled noise simulation methods. The long term jitter is determined considering a division ratio of 2 and 32 (no. of periods).

Divide ratio	time averaged	sampled	calculated
	ns	ns	ns
1	2.748	3.003	2.331
2	4.298	4.442	3.29
32	11.16	11.65	13.19

Table 4.4: RMS values of the period jitter due to phase noise of the relaxation oscillator obtained by schematic simulations

Divide ratio	time averaged	sampled	calculated
	ns	ns	ns
1	1.878	2.035	1.621
2	2.926	3.001	2.19
32	7.581	7.861	9.17

Table 4.5: RMS values of the period jitter due to phase noise of the relaxation oscillator obtained by layout-extracted simulations

Fig. 4.10 depicts the phase noise spectrum obtained by schematic and layout-extracted simulations. The calculated period jitter values in Table 4.4 and Table 4.5 are determined by using (3.8) and considering the noise density at 20 kHz.

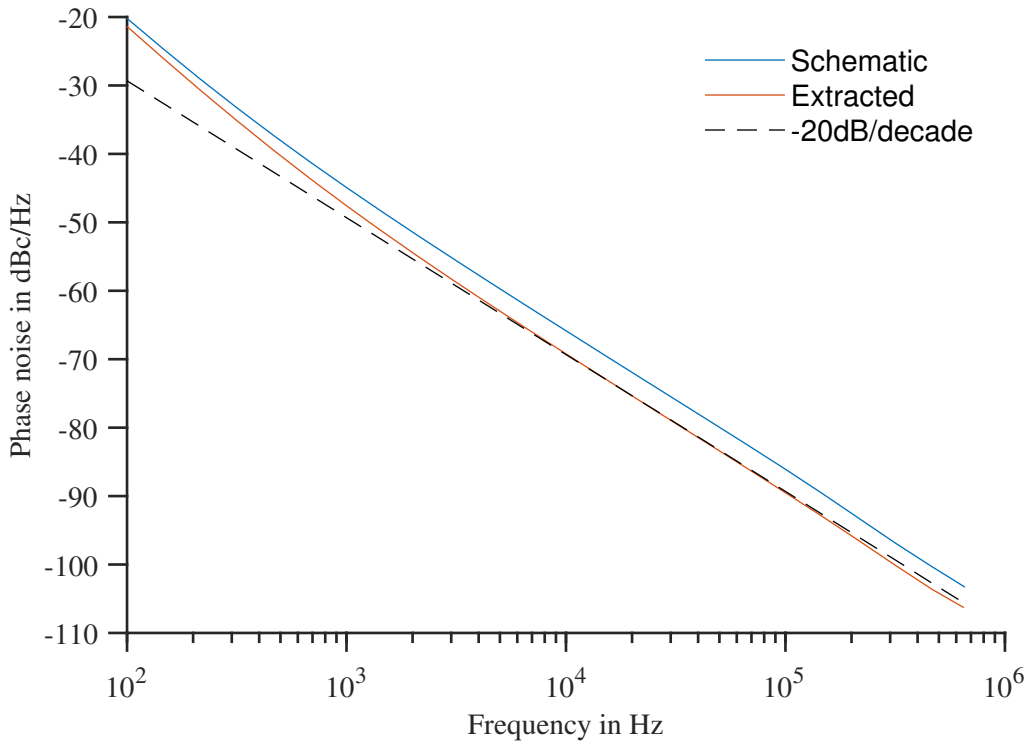

Figure 4.10: Phase noise spectrum of the relaxation oscillator for schematic and layout-extracted simulations

4.7 Power supply rejection

Fig. 4.11 depicts the frequency variation caused by a transient sinusoidal disturbance on the supply voltage. The difference between simulations of the schematic and the extracted-layout netlist is lower than 0.1%. As implied by (3.13), (3.14), and (3.15), the change in the frequency variation is caused by the additional parasitic capacitance between the drain and the source of transistor M_5 and the additional capacitance at the source terminal of M_4 shown in Fig. 2.10

As specified in Table 1.1, the frequency variation due to disturbances superimposed on the voltage supply must not exceed 1.5 %, which is well above the observed maximum frequency deviation of less than 0.9 %.

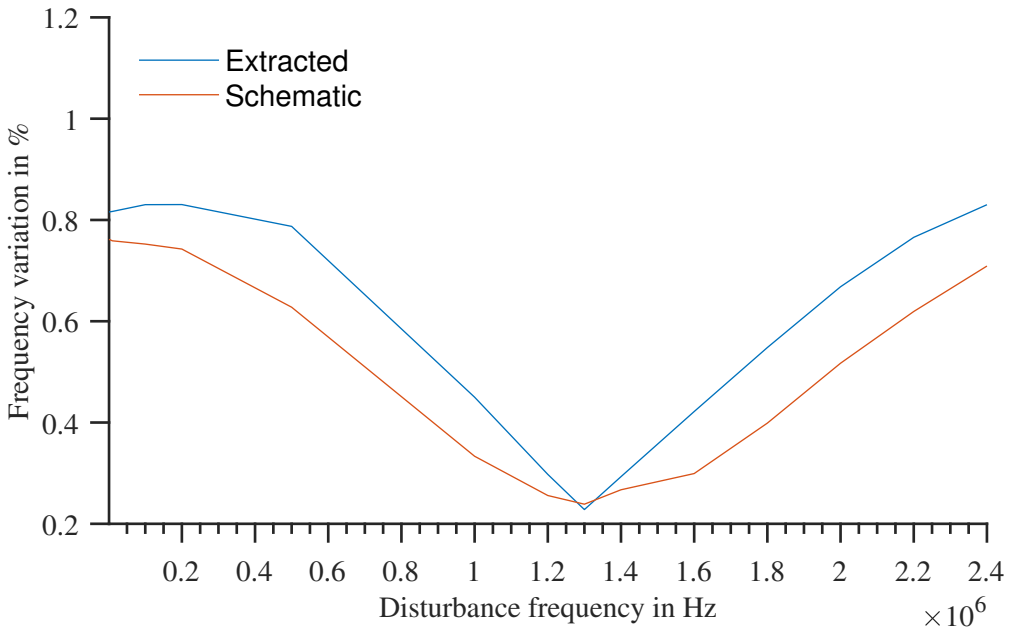

Figure 4.11: Max. frequency variation of the oscillator for a sinusoidal supply disturbance with 10 mV peak amplitude

4.8 Comparison with related work

Reference	[2]	[18]	[19]	This work
Technology	0.35 μm	0.18 μm	0.14 μm	40 nm
Frequency	3.3 kHz	1.28 MHz	1.28 MHz	1.312 MHz
Power	11 nW	1.18 μW	440 nW	81 nW
Supply voltage	1 V	1 V	0.9 V	0.6 V
TC	$<$ 260 ppm/°C	N/A	N/A	$<$ 250 ppm/°C
3σ deviation	20 %	6 %	8 %	5 %
Area	0.1 mm^2	0.0137 mm^2	N/A	0.0015 mm^2

Table 4.6: Comparison with related work

Table 4.6 shows a comparison of the implemented oscillator with previous publications. The oscillator investigated in this work shows good results in terms of power consumption compared to other reported designs with similar operation frequency. Furthermore, the frequency accuracy with respect to temperature, process and mismatch variations is similar to the previously reported work.

Chapter 5

Conclusion and future work

5.1 Conclusion

This work investigates three different ultra-low power oscillator topologies for the clock generation of a UHF RFID transponder IC. The oscillators are compared with respect to power consumption, temperature behaviour, process and mismatch variations, frequency controllability, phase noise and power supply rejection.

The ring oscillator using an integrated temperature compensation and the relaxation oscillator are implemented in a 40-nm CMOS technology. The oscillators run at a frequency of 1.312 MHz at a low supply voltage of 600 mV. The relaxation oscillator topology, which has been previously reported in [2], shows the best performance with respect to power consumption and power supply rejection.

The relaxation oscillator includes a reference voltage with a PTAT temperature characteristic to compensate the CTAT behaviour of the threshold voltage of the pulse generating logic, resulting in a temperature drift of the frequency of less than 250 ppm/°C. The temperature characteristic of the oscillator frequency can be flexibly adjusted in the design by changing the dimensioning of the reference voltage generation and the current comparator stage. Bias current variations, besides process and mismatch variations are compensated by a trimming circuit with a 6-bit digital input word, which allows a frequency adjustment by changing the bias current of the oscillator core.

The relaxation oscillator shows fast frequency settling behaviour in contrast to the ring oscillator using a switched-capacitor feedback loop. Furthermore, the implemented relaxation oscillator shows a power consumption of less than 140 nA, a maximum frequency variation of less than 5 %, and a good power supply rejection as verified by layout-extracted simulations.

The implemented relaxation oscillator is suitable for the clock generation of a UHF RFID transponder IC which must comply with the EPC Generation-2 standard. The oscillator

has a high flexibility regarding temperature stability and current sensitivity which can be utilized. Compared to other oscillator structures available today it shows very good performance regarding area, power consumption, temperature stability, and frequency accuracy versus process and mismatch variations.

5.2 Future work

The presented oscillator design bas been verified by simulations. For a final validation of the circuit, further steps are required. The bias generation was modelled so far as an ideal current source with a Gaussian distributed current. The final implementation of the bias generation may show a different statistical distribution of the bias current and deviations in the temperature characteristics. A final optimization and verification of the oscillator requires a co-simulation together with the bias generation circuit, which was not available at the point in time of writing this thesis.

The digital circuit part of an RFID transponder IC causes disturbances on the voltage supply lines, which exhibit fast transient voltage spikes. Therefore, simulations including a model of transient disturbances due to the operation of the digital part are necessary to determine the effective power supply rejection of the oscillator.

The oscillator is planned to be manufactured as part of a test chip and validated by measurements. The validation of manufactured samples of the oscillator was out of scope of this thesis.

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