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Design of an Integrated Switched Capacitor DC-DC Converter for Negative Supply Voltage Generation

Master's Thesis

to achieve the university degree of
Diplom-Ingenieur
Master's degree programme: Information and Computer Engineering

submitted to

Graz University of Technology

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Institute of Electronics

Faculty of Electrical and Information Engineering

Graz, February 2018

This document is set in Palatino, compiled with pdfLaTeX2e and `Biber`.

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Abstract

This thesis describes a development flow for a Switched-Capacitor DC-DC converter creating a negative voltage. This includes conceptual considerations, such as topology and approximate performance calculations, as well as the design of the circuit in Bipolar-CMOS-DMOS (BCD) technology and the verification of the design in comparison to the conceptual approximations.

The use of triple-well NMOS and DeMOS devices is reviewed. Additionally, needed circuits such as level shifters and voltage buffers are explained. Furthermore, an approach for area optimisation of the used switch transistors is presented. Other considerations such as external devices and the introduced parasitics and their effects are also modelled and discussed.

Keywords: switched capacitor; DC-DC converter; charge pump; series-parallel topology; negative voltage creation; switches; triple-well NMOS; DeMOS; area optimisation; external capacitor; parasitics.

Kurzfassung

Diese Masterarbeit beschreibt den Entwicklungsprozess eines Switched-Capacitor DC-DC Konverters, zum Erzeugen einer negativen Spannung. Dies inkludiert konzeptionelle Betrachtungen, wie die Topologie und rechnerische Abschätzungen der Leistung, als auch das Design der Schaltung in Bipolar-CMOS-DMOS (BCD) Technologie und die Verifikation des Designs im Vergleich zu den konzeptuellen Abschätzungen.

Die Verwendung von triple-well NMOS und DeMOS wird aufgearbeitet. Zusätzlich benötigte Schaltungen wie Levelshifter und Spannungsbuffer werden erklärt. Weiters wird ein Ansatz zur Flächenoptimierung der verwendeten Transistorschalter präsentiert. Andere Betrachtungen, wie externe Komponenten und deren parasitäre Effekte, werden modelliert und diskutiert.

Stichworte: switched capacitor; DC-DC converter; charge pump; series-parallel topology; negative voltage creation; switches; triple-well NMOS; DeMOS; area optimisation; external capacitor; parasitics.

Acknowledgement

I would like to thank everyone who helped me creating this thesis. In particular I would like to thank:

- **Prof. Peter Söser** for being my supervisor for my master's thesis as well as for my seminar project and for being my mentor in my master's programme,
- **Infineon Technologies** for making it possible to work in a highly professional environment during the time of my study,
- **Dr. Gerhard Maderbacher** for being my supervisor at Infineon Technologies, guiding me into the right direction and
- all my **family and friends** for supporting me and for helping making all of this possible.

Contents

Contents

1 Motivation

Most integrated circuits require different voltage levels for different modules to increase efficiency and performance, e.g. 1.5 V for digital supply, 3.3 V for analog domain, I/O supply voltages,...

Nevertheless, there are basically two possibilities, that these voltages can be provided:

- The first option is to externally place separate power supplies for all the different voltages needed. However this leads to higher costs, as additional external components are needed, in system integration.
- The second option therefore is to create different voltage domains internally, by deriving all voltages from a single supply voltage. This of course leads to higher design efforts, but is beneficial in having a more compact design and lower costs in system integration, if the needed power is not too high.

For today's system integration density it is important to focus on the second possibility mentioned. This of course includes downscaling as well as upscaling the given supply voltage. For upscaling, the use of Switched-Capacitor (SC) approaches is very common.

In this thesis the development of a Switched-Capacitor DC-DC (SC DC-DC) converter is explained, which is capable of creating an output voltage of ideally $-2 \cdot V_{\mathrm{DD}}$ from a positive supply voltage (V_{DD}). In general the principles for positive and negative charge pumps, that have to be applied, are the same. However, there are a few more things to consider for dealing with node voltages below substrate voltage, that will also be explained in this thesis.

Additionally, the use of mathematical models for estimating the circuits performance is convenient, as this allows to determine the circuit's performance beforehand. By this, the influence of the circuit parameters such as flying capacitance values, switch on-resistances and switching frequency on the output resistance can be approximated in an easy way.

The main goal of this thesis is to provide a full development flow, starting from conceptual considerations, design and implementation of these concepts in Bipolar-CMOS-DMOS (BCD) technology and ending with verification of the concept by simulation results. Another important topic in IC development is saving area, therefore considerations of how to size the switches should also not be neglected. Considering the most important switches of the Switched-Capacitor (SC) design, there is quite a big potential in saving area, however keeping same circuit performance.

2 Literature Research

Before starting with the analog design of the SC DC-DC converter it is important to do some literature research in order get an overview of similar projects. From these projects some approaches respectively some ideas might also be applicable to this project.

Basically the research covers different parts of the circuit. This includes the overall design of the SC DC-DC converter, as well as smaller parts. For instance also level shifters will be needed for both shifting the phases for a full positive supply voltage (V_{DD}) as well as transferring voltage levels from digital domain to analog domain. Furthermore, voltage buffers are needed in order to maintain appropriate gate voltages on the transistors during switching.

Therefore, mainly IEEE Xplore Digital Library has been searched for appropriate papers and the following documents have been selected and analysed.

2.1 Level Shifters

It is expected that level shifters will be needed in order to be able to properly drive some switches of the Switched-Capacitor DC-DC. In [1] the authors present a level shifting circuit that is capable of shifting the input voltage by V_{DD} respectively a multiple of V_{DD}. Firstly, a standard level shift circuit is explained. In this they introduce capacitances that couple the gates of the two input transistors with the gates of the output transistors and explain the influence of these capacitances.

Furthermore, a different approach is presented, having only one coupling capacitor but an additional inverter between the two output gates. Simulations show that this led to smaller rise and fall times. In the next steps, approaches for reaching higher offsets with multiples of V_{DD} are explained, based on the presented level shift circuit.

In the SC DC-DC converter design the following things can be considered from this paper:

- Designs for shifting by one time as well as two times of V_{DD} are presented. It is also expected that the design will need both approaches in order to properly drive the gates of the transistors. The main difference is that in this case the voltages do not have to be shifted up, but they need to be shifted down, which leads to mirroring of the whole circuit.
- For the examples the authors use standard 1.2 V technologies in order to compare the differences. However, the approaches should be generally applicable in the 3.3 V domain too, as the explanation can be generalised to shifting multiples of V_{DD}.
- The paper assumes a triple well process, such that every bulk can be directly connected to the source of the n-channel MOSFET (NMOS), in order to omit substrate losses. This might not be possible in other processes. However, as a triple well process is fundamentally needed in this project because the drain or source voltages of some NMOS are below substrate potential, this does not represent a problem.

2.2 Gate Driving Circuits

Apart from using level shifters, there are also other options for gate-control circuits of the switches. In [2] the authors are implementing an SC DC-DC converter that is capable of creating an output voltage that is about three times higher than the given input voltage. The converter should be able to start up without additional power sources. Converters that are based on inductors could omit this problem, but have the disadvantage of needing external inductive components that could cause interference. Furthermore the Dickson charge pump is mentioned as possible solution, however requiring a minimum start-up voltage [3].

In [2] the series-parallel approach is used, where in one phase all capacitances are charged to V_{DD} and in the other phase these capacitances are connected in series on top of V_{DD}, in order to reach three times V_{DD}. Altogether seven switches are needed. Four are used for charging the two capacitances, two for each capacitor, so for the parallel connection. The other three are needed for the series connection in order to charge the output capacitance.

A main issue in both either the series-parallel or the Dickson type approach is the design of the switches. In general, the highest voltage that is applied to either drain or source terminal of a metal-oxide-semiconductor field-effect-transistor (MOSFET), which is used as a switch, needs to be available for properly driving the gate. Therefore, usually a separate power supply is needed, in order to turn the switches on or off.

Basically there are different possibilities to drive the gates of the switches.

- On the one hand, an additional step-up converter can be applied to supply the gates, which reduces the efficiency of the design. These could be for example created by either of the previously mentioned approaches.
- On the other hand, the needed gate voltages can be taken from the created output voltage, which implies that there is energy stored or it needs another circuit to ensure start-up.

In this paper the authors explain the control of the gate voltages of the non-trivial cases. Therefore, they mainly focus on the switches to V_{DD} as well as to the output switch. For the V_{DD}-switches they simply use an inverting structure.

The output switch needs to be off in one phase having V_{DD} and $3 \cdot V_{DD}$ on its drain, respectively source and it needs to be on in the second phase when on both pins $3 \cdot V_{DD}$ is applied. In this case, they make use of the voltages that are available on the flying capacitors during the two phases, to avoid the issue of having to create separate gate voltages.

The proposed series-parallel topology itself can be applied in this thesis, as the output voltage needs to be shifted by two times of V_{DD} too. The difference lies in the direction the voltage needs to be shifted. Therefore, the author's circuit can be used, mirrored to negative voltage direction.

However, in this thesis the design of the switches is not as trivial as in the paper as there is a limit to the maximum drain-source voltage, that is applied to a single transistor. The authors do not face this problem as their V_{DD} is smaller referred to the used technology, so that they do not exceed the save operating area (SOA) when applying two times V_{DD} as drain-source voltage (V_{DS}).

In the SC DC-DC design, V_{DD} is defined as 3.3 V and also the SOA is fixed to 3.3 V $\pm$ 10 %. This means that the allowed maximum voltages are easily exceeded when only using single devices. To circumvent this problem either the transistors have to be cascoded or so-called drain-extended MOSFET (DeMOS) [4] [5] have to be used. The disadvantage in all these ideas comes with the increased R_{ON}. However, also in the paper R_{ON} is not at a minimum as the gate-source voltage is not at the transistor's extremum.

2.3 Drain Extended MOS Transistors

Papers [4] and [5] explain the advantages of drain-extended MOSFET (DeMOS). In general, transistors are designed for specific operating voltages. Digital parts of an integrated circuit usually have voltages of about 1.2 V or even lower, whereas analog circuits are commonly operated with 3.3 V or 5 V. In order to save costs, for these different voltages transistors have to be used accordingly. Commonly, the allowed drain-source voltage is the limiting factor in a circuit. This is also the case in the SC DC-DC design. Standard NMOS and p-channel MOSFET (PMOS) are available in this technology for the digital as well as for the analog (3.3 V) domain.

Presumably, there will be voltages of about two times V_{DD} on some transistors which usually makes the usage of a single transistor impossible. Therefore so called drain-extended MOSFET (DeMOS) can be used. Unlike standard MOSFETs, these have a prolonged drain region, that allows them withstand higher voltages. Taking an NMOS as an example the n+ doped area, where the drain is usually connected is moved further away from the gate oxide. In the gap below the gate oxide and the n+ drain region an n-well is placed, in order to prolong the channel. This is visible in figure 2.1.

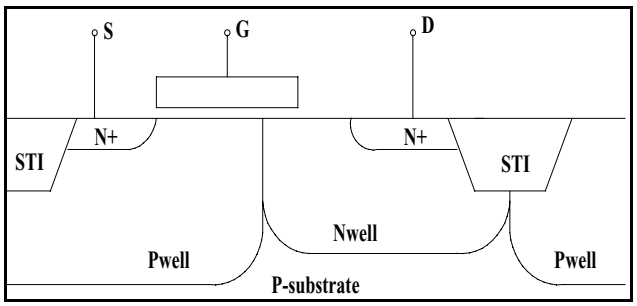


Figure 2.1: Cross section of a DeMOS-NMOS [4].

The same is also valid for PMOS by interchanging p-doped and n-doped regions.

Another possibility to increase the operating voltage is the use of two gate oxides and two lightly-doped drain (LDD) implants, but this might not be available in every process as it leads to higher costs due to increased complexity. This approach is working in such a way that the LDD extension reduces the electric field below the gate at the drain end. Therefore, a higher drain breakdown voltage is achieved.

The authors mainly focus on the creation of the DeMOS without introducing additional process steps. Mainly, there are three parameters that can be chosen: the length of the gate, the overlap of the gate and the drain well and the distance between gate and drain edge.

As DeMOS transistors are available in this thesis' technology the use of these for some switches might be taken into consideration. However, the performance between these and cascaded MOSFETs has to be compared first.

2.4 Analysis and Optimization of Switched-Capacitor DC-DC Converters

In papers [6] and [7] the output impedance and therefore the performance of an SC converter is calculated. Therefore, the converter is modelled as an

ideal converter with an additional output impedance that represents the voltage drop from the ideal result. The authors analyse a two phase 3 V to 1 V ladder circuit. On this topology they determine the maximum limits that can be reached depending on the capacitor size, the switches' on-resistance (R_{ON}) and the switching frequency (f_{sw}).

The equivalent output resistance is calculated based on the charge flow during both phases. Therefore charge multiplier vectors are defined that describe the charge flow over the parts that cause efficiency loss. Further information can also be found in [8], [9] and [10].

2.4.1 Slow Switching Limit

For the slow switching limit (SSL) the charge flow over all capacitors and voltage sources is looked at [7, pp. 8-10]. Here it is assumed that these ideal voltage sources are similar to precharged capacitors with infinitely high values of capacitance. For every phase the charge flow over every capacitor is written into a vector. This vector is normalised to the charge that is flowing into the output voltage source respectively out of the converter. Equation 2.1 shows the definition of such a vector for a specific phase Φ, containing n capacitors.

$$\begin{aligned} a^{\Phi} &= \begin{pmatrix} q_{out}^{\Phi} & q_{1}^{\Phi} & \cdots & q_{n}^{\Phi} & q_{in}^{\Phi} \end{pmatrix}^{T} \cdot \frac{1}{q_{out}} \\ &= \begin{pmatrix} a_{out}^{\Phi} & a_{c,1}^{\Phi} & \cdots & a_{c,n}^{\Phi} & a_{in}^{\Phi} \end{pmatrix}^{T} \\ &= \begin{pmatrix} a_{out}^{\Phi} & a_{C}^{\Phi} & a_{in}^{\Phi} \end{pmatrix}^{T} \end{aligned} \tag{2.1}$$

Furthermore, one comes to the conclusion that $a_C^{\Phi_1} = -a_C^{\Phi_2}$, which obviously means that the sum of the charges that is flowing in and out of the capacitors in both phases is equal to zero. In a two phase system the vector a_C^{Φ} only needs to be determined for one phase as the other vector can be achieved by changing the sign of every element. With given charge flow through every capacitor, the corresponding capacitor size and the switching frequency, the

slow switching limit can be determined by equation 2.2.

$$R_{SSL} = \sum_{\substack{i \\ capacitances}} \frac{a_{c,i}^2}{C_i \cdot f_{sw}} \tag{2.2}$$

By equation 2.2 also a suggestion of choosing the capacitances is given. In order to keep the resistance R_{SSL} low the capacitance should be chosen larger if more charge is flowing over this specific capacitance. Therefore, it is important to note that not every capacitance must necessarily have the same influence on the efficiency of the circuit. This is depending on the used topology.

2.4.2 Fast Switching Limit

The other restriction is the fast switching limit (FSL) [7, pp. 10-12]. It depends on the charge that is flowing over the switches. Here it is not distinguished between phases, as only the charge flow over switches in their respective conducting phase is important. This yields a vector containing the charge flow over every switch (1 to m) as shown in equation 2.3. This vector can be simply derived from the capacitance charge vectors from the slow switching limit. Here it is important to notice that this vector is normalised to output charge flow too.

$$\begin{aligned} a_r &= \begin{pmatrix} q_{r,1} & \cdots & q_{r,m} \end{pmatrix} \cdot \frac{1}{q_{out}} \\ &= \begin{pmatrix} a_{r,1} & \cdots & a_{r,m} \end{pmatrix} \end{aligned} \tag{2.3}$$

By having this vector the output impedance of fast switching limit (FSL) can be derivated. The result is shown in equation 2.4.

$$R_{FSL} = 2 \cdot \sum_{\substack{i \\ switches}} R_i \cdot a_{c,i}^2 \tag{2.4}$$

Again it is obvious that best results will be achieved by appropriate choice of the switches' on-resistance (R_{ON}). The more charge is flowing over the switch the smaller the on-resistance should be made.

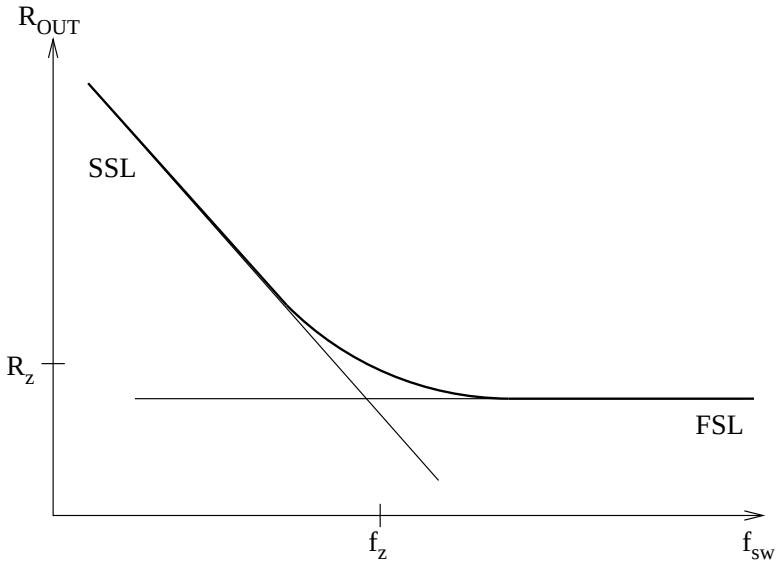


Figure 2.2: Output impedance depending on the switching frequency (f_{sw}) showing the slow switching limit and fast switching limit [7, p. 19].

2.4.3 Combining SSL and FSL

The results of SSL and FSL can be approximated by a curve that is described by equation 2.5 [7, p. 19].

$$R_{out} = \sqrt{R_{SSL}^2 + R_{FSL}^2} \tag{2.5}$$

Figure 2.2 shows the approximated curve for the output impedance. At low frequencies the slow switching limit is dominating which is inversely proportional to switching frequency (f_{sw}). For higher frequencies the fast switching limit becomes more important, as R_{FSL} is independent of f_{sw} and therefore a constant. Therefore, the best result, when operating the charge pump in open loop, is achieved by selecting a switching frequency that is at the intersection of the two curves at f_z.

2.4.4 Comparison of SC Converter Topologies

In [7, pp. 20-23] five different step-up converter topologies are evaluated:

1. Ladder,
2. Dickson Charge Pump,
3. Fibonacci,
4. Series-Parallel and
5. Doubler.

The topologies are compared for different conversion ratios. The series-parallel converter performs well in SSL, but has drawbacks in FSL, whereas the Dickson Charge Pump and Ladder topology are better in FSL, but worse in SSL. Exponential converters (Fibonacci, Doubler) perform well in both cases, but would require devices that have different voltage ratings, which is usually not the case when using standard complementary metal-oxide-semiconductor (CMOS) processes.

2.5 Triple-Well NMOS Switch

Standard NMOS transistors in CMOS have no isolation between substrate and the bulk terminal, as the bulk only represents a p+ doped region within the p-substrate. Therefore, it is not possible to put the bulk to another potential different than substrate potential. Triple-well NMOS transistors have a different structure. Based on a standard NMOS transistor two additional wells are added. The inner well is p-doped (p-well) whereas the outer well is n-doped (deep n-well) [11].

This leads to some advantages compared to standard NMOS transistors.

- The bulk terminal can be put to potentials that differ from the substrate, which can be beneficial in two ways.
  - Firstly, the body-effect (change in threshold voltage as effect of non-zero bulk-source voltage) can be avoided, by connecting the bulk on the source terminal, as this can also be done in PMOS transistors.

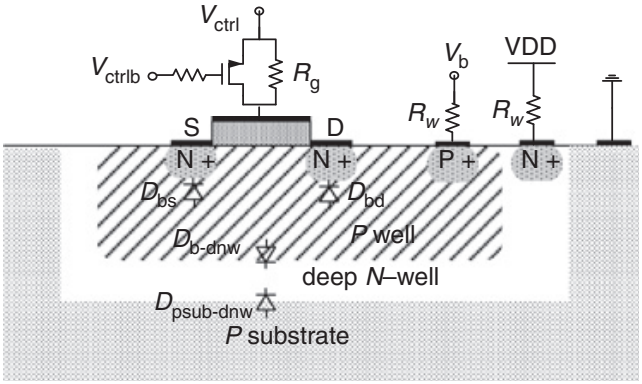


Figure 2.3: Cross section of a triple-well NMOS transistor [11].

  - Secondly, the drain- respectively source-terminal of the transistor may go below substrate potential. With a standard NMOS this would not be possible without forward biasing the bulk-source diode. In triple-well transistors the bulk voltage can be set accordingly not to forward bias the mentioned diode.
- Furthermore, the triple-well structure also reduces substrate coupling effects, leading to a higher isolation of the transistor channel. Of course this is only the case if the well is set to a fixed and stable potential (AC ground).

The introduction of two additional wells also leads to two new well diodes, which are a diode from p-substrate to deep n-well and another diode from p-well to deep n-well. Therefore the n-well has to be set to a potential that is higher or equal than the bulk and the substrate potential. These diodes are also visible in figure 2.3.

As in this project a negative output voltage has to be generated and NMOS transistors will be needed as switches, it is inevitable to make use of NMOS devices whose bulk can be set to a different potential than substrate. However the main reason lies in preventing the forward biasing of the bulk-source diode and not in reducing substrate coupling effects.

2.6 Voltage Buffers

In paper [12] the authors describe different ways of implementing voltage buffers. One standard way is to use a two-stage operational amplifier (OPAMP) with negative feedback that is operated as voltage follower. However, when designing an OPAMP bandwidth and stability considerations have to be made. Therefore, another approach is described in this paper, which is the use of a complementary source follower, that has no closed loop feedback.

The first circuit that is presented is a simple complementary source follower. This circuit basically consists of two current paths. One path is responsible for biasing. Furthermore, all gate voltages of the diode connected transistors have to be kept at a reasonable operating point by the input voltage. The bias current is then mirrored by a predefined factor of the bias current to the second path. It is very effective as it has low quiescent current, good frequency characteristics and low voltage offset.

The other two circuits are a combination of the previously mentioned complementary source follower combined with a common source stage, that is driven by two error OPAMPs or by internal feedback. This topology combines the advantages of the two topologies, resulting in a higher voltage swing. The drawback lies in higher power and current consumption.

Basically, in this project the voltages V_{DD}, $V_{\mathrm{SS}} = 0 \cdot V_{\mathrm{DD}}$ and $-2 \cdot V_{\mathrm{DD}}$ will be available during all phases as these are either provided by the power supply or by the output capacitance. However, it is to be expected that a voltage buffer will be needed for creating $-1 \cdot V_{\mathrm{DD}}$ in order to correctly drive the gates of some switches. In some phases it might be possible to use the voltages that are provided by the flying capacitance.

There is no possibility to use additional capacitances as only four external capacitors are allowed to be used. These are two flying capacitors, one input and one output capacitor. Furthermore, also internal capacitances are restricted to a size of about 1 pF which should obviously not be sufficient for charging and discharging the gates of the switches without significant spikes on that voltage domain. Too large voltage spikes might cause problems when exceeding save operating area (SOA) as the allowed voltages

might be transcended. Furthermore, it would be of advantage if the current consumption during non-switching could be lower than during switching of phases.

The authors also mention the possible voltage or current swing. However, this is not important in this case, as the input voltage will not vary and stay constantly at negative supply voltage or at the output voltage. Furthermore, also good linearity can be put aside. As the voltage buffer has to be fast it is important to have a low output resistance, that is why the third proposal seems most useful.

Further voltage buffers, including enabling and power-down circuits with high-voltage switches can be found in [13].

2.7 Gate Drivers for Stacked MOSFETs

Nowadays, manufacturing processes are optimised towards, less power consumption, higher speed and maximum integration density. Therefore, also the operating voltage as well as the breakdown voltage is decreased. However, there are still many applications that require higher voltages. In general, there are two different possibilities to deal with high-voltage switching. One could either use specific devices, that can withstand these voltages, or the circuit can be adjusted so that the SOA is not exceeded [14].

Paper [14] presents a circuit technique of using stacked MOSFETs, where high voltages are equally split on all transistors. It is important that a minimum number of devices is used. If there were too many MOSFETs connected in series, this would unnecessarily increase the on-resistance of the switches and therefore lead to slower charging of the capacitances.

Basically, two MOSFETs are connected in series, where the gate of the lower NMOS is controlled by a control signal and the other NMOS is controlled by a voltage divider and with an additional capacitor. Furthermore, this capacitor needs to be scaled according to the gate-source capacitance (C_{GS}) of the upper transistor and the switching frequency. The lower the switching frequency, the higher C_2 has to be made. Even though the authors explain

their derivations only on a circuit with a multiplication factor of 2 the same can also be applied for a factor of n reaching $n \cdot V_{DD}$.

Finally, the authors prove their equations in a process rated for 5 V operation using 2 and 8 stacked devices. This is done by simulation as well as by experimental results.

As the devices in this project's technology are only specified for about $3.3\,V \pm 10\,\%$ (with the exception of DeMOS, see section 2.3), it is therefore necessary to think about stacked MOSFETs that are used as switches, that can handle voltages of about 6.6 V.

However the following problems could arise:

- The voltage divider that is located between the output voltage and ground consumes current all the time. This reduces the efficiency of the converter. This current can be decreased by increasing the resistor values, but then the voltage drop increases, when current is taken from the voltage divider.
- To counteract this problem the capacitor for keeping the gate voltage stable could be increased, but it has to be considered, that the size of the integrated capacitors is limited and additional external ones may not be used.

The same principle for five stacked MOSFETs is also analysed in [15].

2.8 DC Voltage Dependent Capacitor

The capacitance value of a real capacitor can be described either as a static capacitance (C_S) or a dynamic capacitance (C_D). The difference between these lies in their definitions. C_S is defined as the ratio of charge (Q) and voltage (V) as shown in equation 2.6.

$$C_S = \frac{Q}{V} \tag{2.6}$$

On the other hand C_D is defined as the differential change of charge for a change in voltage as described in equation 2.7.

$$C_D = \frac{dQ}{dV} \tag{2.7}$$

For an ideal capacitor that is independent in terms of DC voltage or other effects the static capacitance and the dynamic capacitance are equal ($C_S = C_D$) and therefore also the energy stored in such a capacitor can be calculated easily by equation 2.8.

$$E_{C,ideal} = \frac{C_S \cdot V^2}{2} = \frac{C_D \cdot V^2}{2} \tag{2.8}$$

However if the capacitance depends on the applied voltage this equation is not valid any more. By transforming equation 2.7 and taking the integral an equation for the charge at a specific voltage can be derived [16].

$$\begin{aligned} C_D(V) &= \frac{dQ}{dV} \\ dQ &= C_D(V)\,dV \\ \int_{q=0}^{Q(V)} dQ &= \int_{v=0}^{V} C_D(v)\,dv \\ Q(V) &= \int_{v=0}^{V} C_D(v)\,dv \end{aligned} \tag{2.9}$$

Inserting equation 2.6 into 2.9 yields a relation between static capacitance and dynamic capacitance that is shown in equation 2.10.

$$C_S(V) = \frac{Q(V)}{V} = \frac{\int_{v=0}^{V} C_D(v)\,dv}{V} \tag{2.10}$$

In general the dynamic capacitance (C_D) and not the static capacitance (C_S) is given in a datasheet. It is specified depending on the DC voltage applied to the capacitance.

In order to calculate the stored energy the power needs to be integrated over time, starting with the initial voltage on the capacitor until the desired voltage is reached. Inserting the I-V relation $I = \frac{\mathrm{d}Q}{\mathrm{d}t} = C_\mathrm{D}(V) \cdot \frac{\mathrm{d}V}{\mathrm{d}t}$ for capacitors gives equation 2.12. It is visible that the energy is depending on the voltage (V) over the capacitor and the dynamic capacitance (C_D) function.

$$\begin{aligned} E(V) &= \int_{t=t(v=0)}^{t=t(v=V)} v \cdot I \,\mathrm{d}t = \\ &= \int_{v=0}^{v=V} v \cdot C_\mathrm{D}(v) \cdot \frac{\mathrm{d}v}{\mathrm{d}t} \,\mathrm{d}t \end{aligned} \tag{2.11}$$

$$E(V) = \int_{v=0}^{v=V} v \cdot C_\mathrm{D}(v) \cdot \mathrm{d}v \tag{2.12}$$

These considerations in terms of DC dependency of the external capacitors have to be taken into account in order make good estimates in terms of slow switching limit. that ensures accurate simulation results. Furthermore it is also important to use capacitance models with whom the simulator is able to model charge conservation [17]. Basically there are two possible capacitance models. One is capacitance based where the capacitance is described as a function of voltage. In this case the function for dynamic capacitance is needed. The second model is charge based where the charge needs to be described by static capacitance function and applied voltage [18, pp. 167-176].

Only the charge based model is capable of charge conservation. If charge conservation is not considered, this could lead to wrong results as there might be charge appearing or disappearing at a change in capacitance without any physically possible explanation.

3 Concept

In this section the basic, ideal concept of the Switched-Capacitor DC-DC converter is described. Furthermore also some calculations are explained that are used for estimating and optimising the overall performance. Moreover also the influence of flying capacitor sizes as well as different switch on-resistances is discussed.

3.1 Topology

As already mentioned in subsection 2.4.4 there are different topologies possible for SC DC-DC converters. All of these have certain advantages and disadvantages. In this paper a series-parallel topology will be used. This decision is based on the better performance in slow switching limit (SSL) comparison. In this way the influence of the switches' on-resistance on the converter's performance can be minimised. This also yields less area requirements as the switches can have a higher resistance and therefore can be made smaller. Additionally having good performance in SSL comparison means, that the switching frequency can be smaller compared to other topologies. This might also be beneficial as external capacitances have to be used, which automatically introduces inductances from bond wires and external wiring. These inductances can be a critical factor when using higher switching frequencies.

For the series-parallel topology two flying capacitors, one output capacitor and seven switches are needed. Basically there are two switching phases for controlling the switches. In first phase all the capacitors are connected in parallel, where each one is charged to V_{DD} by the input voltage. In the second phase the capacitors are put in series, where the top plate of the

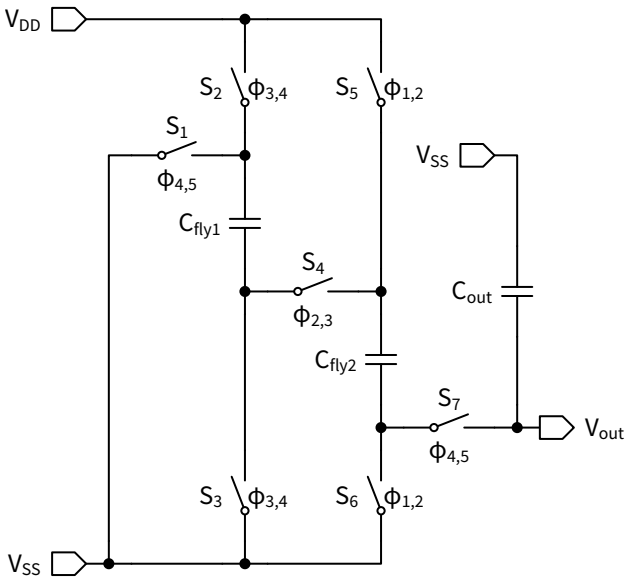
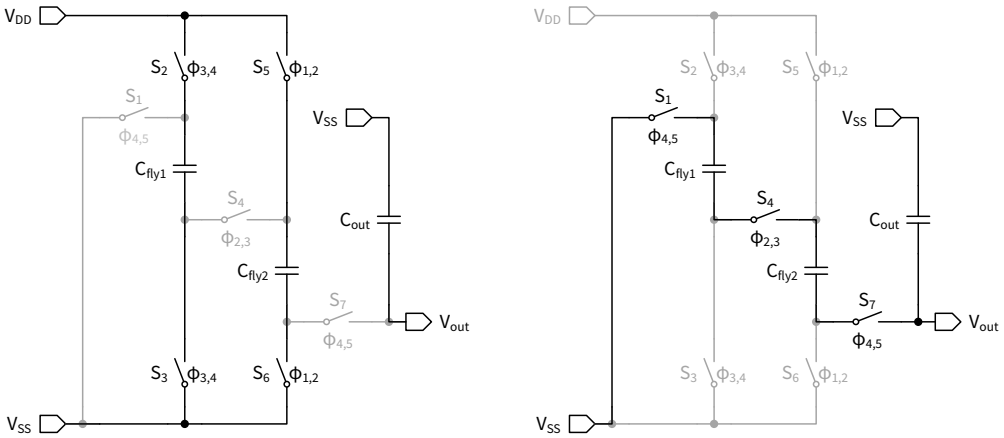


Figure 3.1: The basic concept of the series-parallel SC DC-DC converter.

first flying capacitor is set to ground. In this way the two capacitors push the output node to $-2 \cdot V_{\mathrm{DD}}$ and the output capacitance is charged. The simplified circuit is shown in figure 3.1, whereas the switches that are on (conducting) in parallel phase are aligned vertically and the switches that are on in series phase are aligned horizontally.

In the following, referring to phases, means the major states the circuit can be in. This does not include states that need to be introduced for non-overlapping switching. However referring to the signals that drive the switches, the greek letter $\phi_{x,y}$ is used, whereas x and y denote the states that are split by the the driving signal's transition. This includes all signals from non-overlapping approaches too. State refers to all points of operation the circuit can be in, i.e. phases and non-overlapping transitions.



(a) The resulting circuit for parallel phase (phase 1).

(b) The resulting circuit for series phase (phase 3).

Figure 3.2: Comparison between the circuits for parallel and series phase. All parts (switches) that are not used in a specific phase are greyed out.

3.2 Phase Selection

As in every Switched-Capacitor design it is important to define the phases that are needed. In general two phases would be sufficient. This is shown in figure 3.2. There the resulting circuit for the first phase is shown in subfigure 3.2a and the circuit in second phase is visible in subfigure 3.2b. In order to not have any short circuits on the transition from one to the other phase it is important, that the driving signals ($\phi_{1,2}$ and $\phi_{2,3}$) are non-overlapping.

For the ideal case two phases ($\phi_{1,2} = \phi_{3,4}$ and $\phi_{2,3} = \phi_{4,5}$) are enough, as the switching is happening at exactly the same point in time for switches S1, S4, S7 respectively S2, S3, S5, S6. However this is not the case in a real circuit, as the switching will not happen exactly simultaneous.

This may lead to a problem if the concepts that are described in section **??** (**??**) are used. By using this idea, it could occur, that C_{fly1} is pushed down earlier than C_{fly2}. If this happens the voltage over S4 can exceed save operating area as the bottom of C_{fly1} might already be on a potential of $-V_{\mathrm{DD}}$, whereas the potential on the top of C_{fly2} is still on $+V_{\mathrm{DD}}$. For this case two countermeasures can be applied:

State	Phase	Driving Signal	Switches						
			S1	S2	S3	S4	S5	S6	S7
1	1	$\phi_{1,2}$	off	on	on	off	on	on	off
2	-	$\phi_{2,3}$	off	on	on	off	off	off	off
3	2	$\phi_{3,4}$	off	on	on	on	off	off	off
4	-	$\phi_{4,5}$	off	off	off	on	off	off	off
5	3		on	off	off	on	off	off	on

Table 3.1: States of the switches in between the three phases.

- The switch S4 can be cascaded in order to withstand $2 \cdot V_{\mathrm{DD}}$.
- It can be ensured, that switch S4 is closed before S1. In this way the described problem is avoided.

Therefore an applicable solution is to use three phases. This leads to five different states the circuit can be in.

- In first state both flying capacitances are charged in parallel to $\mathrm{V_{DD}}$ (phase 1).
- In second state C_{fly2} is disconnected and floating, whereas C_{fly1} is still connected to $\mathrm{V_{DD}}$ and $\mathrm{V_{SS}}$ (non-overlapping transition 1).
- In third state the top of C_{fly2} is connected to the bottom of C_{fly1} (phase 2).
- The fourth state consists of opening the switches that are responsible for charging C_{fly1} to $\mathrm{V_{DD}}$. By this the flying capacitances are in series and floating (non-overlapping transition 1).
- In fifth and last state the switch for pulling the top of the first flying capacitor to $\mathrm{V_{SS}}$ is closed as well as the output switch. In this way the output capacitance is charged (phase 3).

In summary table 3.1 shows the operation of the switches through the five different states, respectively in between the four phase transitions, that have been mentioned before.

3.3 Slow and Fast Switching Limits

The ideal conceptual circuit has to analysed in order to determine appropriate capacitor values and switching frequencies. Therefore the slow switching limit (SSL) and the fast switching limit (FSL) can be calculated. These can be represented by an equivalent output resistance, which is also shown in figure 3.3. This leads to a decrease in the absolute value of the output voltage, as there is a resistor added in series as this is the case with every non-ideal (real) voltage source.

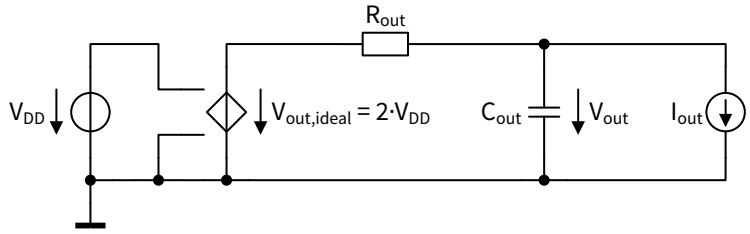


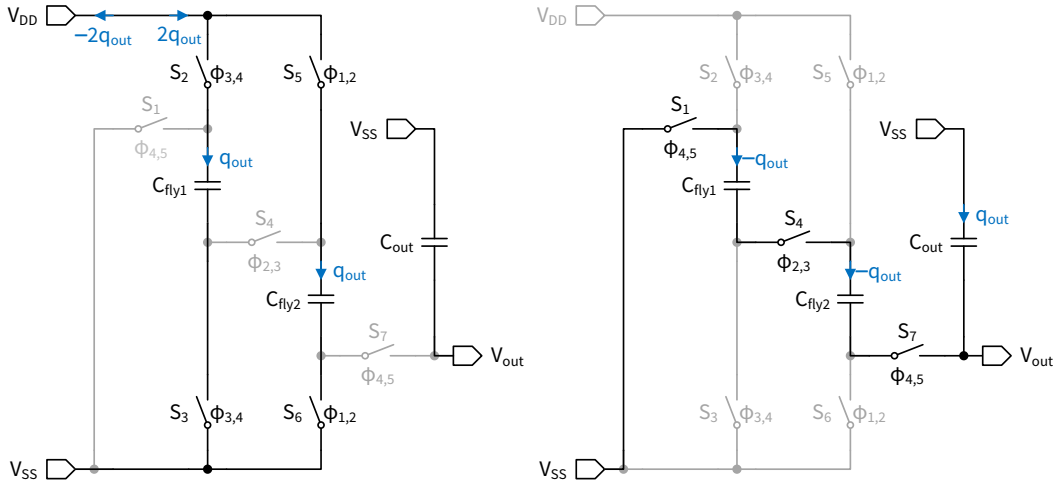
Figure 3.3: Equivalent circuit with output resistance and load (current source) for SC DC-DC converter.

This equivalent output resistance can be determined by analysis of the basic conceptual circuit and mainly depends on

- the size of the **capacitors**,
- the switching frequency,
- the **on-resistance** of the used switches and
- the **topology** of the converter defining the amount of charge that is flowing over the capacitors and switches.

Basically two limits define the converter's efficiency with respect to the switching frequency (f_{sw}). There is a slow respectively fast switching limit. The slow switching limit is determined by the capacitances, whereas the fast switching limit is defined by the on-resistance of the switches. In the following sections this will be explained in detail. Furthermore simulated and calculated results are compared, when sweeping f_{sw} [6].

For determining SSL and FSL the charge flow over the capacitances as well as resistances needs to be known. These values have to be normalised to the



(a) Charge flow in parallel phase.

(b) Charge flow in series phase.

Figure 3.4: The charge flow over the capacitances (Cs) and switch resistances (Rs) for both series and parallel phase.

charge that is flowing into the output capacitance. For this series-parallel topology the analysis can be done as shown in figure 3.4. It is important to note that for reasons of simplification phase 2 is assumed to be much shorter compared to phase 1 and phase 3 and is therefore neglected.

3.3.1 Slow Switching Limit

For determining the slow switching limit (SSL) the charge flow over the capacitances has to be analysed for both phases 1 and 3. The charge flow in both phases is shown in figure 3.4. Furthermore it is important to notice that the charge is normalised to the output charge. The sum of charges over all phases, flowing into or out of the flying capacitances gives zero. Equations 3.1 and 3.2 represent the charge multiplier vectors for each of the phases and are taken from section 2.4.1.

$$\begin{aligned} a^{phase1} &= \begin{pmatrix} 0 & q_{out} & q_{out} & -2 \cdot q_{out} \end{pmatrix}^T \cdot \frac{1}{q_{out}} = \\ &= \begin{pmatrix} 0 & 1 & 1 & -2 \end{pmatrix}^T \end{aligned} \tag{3.1}$$

$$\begin{aligned} a^{phase3} &= \begin{pmatrix} q_{out} & -q_{out} & -q_{out} & 0 \end{pmatrix}^T \cdot \frac{1}{q_{out}} = \\ &= \begin{pmatrix} 1 & -1 & -1 & 0 \end{pmatrix}^T \end{aligned} \tag{3.2}$$

For calculation of R_{SSL} only the charge flow over the flying capacitances is important. Therefore the charge multiplier vector from equation 3.3 is needed for further calculations.

$$a_c = \begin{pmatrix} 1 & 1 \end{pmatrix}^T \tag{3.3}$$

Using equation 2.2 and inserting the charge multiplier vector yields 3.4. The flying capacitances are assumed to be 50 nF in size.

$$R_{SSL} = \sum_{\substack{i \\ capacitances}} \frac{a_{c,i}^2}{C_i \cdot f_{sw}} = \frac{a_{c,1}^2 + a_{c,2}^2}{C_{fly} \cdot f_{sw}} = \frac{2}{50\,\mathrm{nF} \cdot f_{sw}} \tag{3.4}$$

This leads to a slow switching limit resistance, that is depending on the switching frequency, as it is visible in equation 3.5.

$$R_{SSL}\left(f_{sw}\right) = \frac{40\,\mathrm{M\Omega\,s^{-1}}}{f_{sw}} \tag{3.5}$$

3.3.2 Fast Switching Limit

For the fast switching limit (FSL) the charge flow over the switches is important. In this case the on-resistance is the limiting factor. In order to determine the charge flow vector for the switches figure 3.4 needs to be looked at again. In this case the charge flow over the switches in their respective on-phase is used. In the first phase switches S2, S3, S5 and S6 are

on, all conducting a charge of q_{out}. In the third phase switches S1, S4 and S7 are conducting $-q_{out}$. This leads to the normalised charge flow vector for the switch resistances in equation 3.6. However the direction of charge flow is not important in this analysis.

$$a_r = \begin{pmatrix} -1 & 1 & 1 & -1 & 1 & 1 & -1 \end{pmatrix}^T \tag{3.6}$$

In order to determine the fast switching limit resistance the charge flow vector for every switch as well as every switches' on-resistance is needed. In this conceptual circuit it is assumed that R_{ON} is $1\,\Omega$ for every switch. Equation 3.7 shows that the resulting R_{FSL} is independent of switching frequency (f_{sw}) and therefore constant.

$$\begin{aligned} R_{FSL} &= 2 \cdot \sum_{\substack{i \\ switches}} R_{ON,i} \cdot a_{r,i}^2 \\ &= 2 \cdot \left(R_{ON,1} \cdot a_{r,1}^2 + R_{ON,2} \cdot a_{r,2}^2 + \cdots + R_{ON,7} \cdot a_{r,7}^2 \right) \\ &= 2 \cdot R_{ON,1} \cdot 7 = 14 \cdot R_{ON,1} = 14 \cdot 1\,\Omega = 14\,\Omega \end{aligned} \tag{3.7}$$

3.3.3 Results

Combining the results from slow switching limit and fast switching limit can be done by the approximation shown in equation 2.5 from subsection 2.4.3. It is important to notice that this is only a coarse approximation, as the correctly calculated output resistance is depending on the output ripple voltage, the time-constant for charging and discharging the capacitance as well as the average current flowing in the circuit [19, pp. 21-23]. However for the conceptual design using this approximation is sufficient.

Table 3.2 shows the approximated and the simulated output resistance depending on the switching frequency. For the simulation result the settled output voltage of the converter is measured. By Ohm's law the resulting output resistance can be determined as shown in equation 3.8, whereas $V_{out,sim}$ can be determined by averaging the output voltage of the already ramped up SC DC-DC converter. Additionally $V_{out,ideal} = -6.6\,\text{V}$ and $I_{out} = 6\,\text{mA}$ are known beforehand by specification.

$$R_{out,sim} = \frac{V_{out,sim} - V_{out,ideal}}{I_{out}} \tag{3.8}$$

A comparison between the calculated and simulated output resistance can also be seen in figure 3.5, where the output resistance is plotted in dependency of the switching frequency. Both axes are in logarithmic scale. It is visible that especially when being clearly in slow switching limit or fast switching limit region both results match very good. However the approximating formula from equation 2.5 leads to an error, between calculated and simulated results for R_{out} within the region from 1 MHz to 10 MHz, where both limits have noticeable impact on the output resistance.

Nevertheless the approximation gives a good estimate for selecting an appropriate switching frequency, when the size of the flying capacitances and the switches' on-resistance are given. The best tradeoff for operation in open loop without any control feedback is achieved by selecting a switching frequency near the crossing of slow switching limit resistance and fast switching limit resistance. In this case a good selection of f_{sw} would be about 3 MHz.

It can be said, that the switching frequency can be selected lower the greater the flying capacitances. The switches' R_{ON} is the limiting factor at higher frequencies meaning that an increase in frequency does not yield a decrease in output resistance.

3.4 External Capacitances

As the SC DC-DC converter needs to provide up to a maximum of 6 mA at the output it is necessary to have a large output capacitance (about 1 µF) in order to act as an energy storage in the parallel phase (phase 1) as well as to reduce ripple on the output voltage. Also the flying capacitances need to be selected larger (25 nF to 50 nF) as these have to be able to transport the needed amount of charge from the input voltage source to the output capacitance. In this context referring to large capacitances means speaking of capacitance values that are too high to be reasonably integrated on an

Set		Calculated			Simulated	
Index	f_{sw}	R_{SSL}	R_{FSL}	$R_{out,calc}$	$V_{out,sim}$	$R_{out,sim}$
	MHz	Ω	Ω	Ω	V	Ω
1	0.1	400	14	400.2	−4.197	400.58
2	0.2	200	14	200.5	−5.398	200.40
3	0.5	80	14	81.2	−6.118	80.26
4	1	40	14	42.4	−6.358	40.28
5	1.2	33.3	14	36.2	−6.397	33.82
6	1.5	26.7	14	30.1	−6.435	27.54
7	1.7	23.5	14	27.4	−6.452	24.70
8	2	20	14	24.4	−6.468	21.96
9	3	13.3	14	19.3	−6.498	17
10	4	10	14	17.2	−6.504	15.92
11	5	8	14	16.1	−6.508	15.27
12	6	6.7	14	15.5	−6.511	14.83
13	7	5.7	14	15.1	−6.512	14.66
14	8	5	14	14.9	−6.513	14.54
15	9	4.4	14	14.7	−6.513	14.45
16	10	4	14	14.6	−6.514	14.37
17	20	2	14	14.1	−6.515	14.12
18	50	0.8	14	14	−6.516	14.05
19	100	0.4	14	14	−6.516	14.06

Table 3.2: Calculation and simulation results for R_{out} assuming flying capacitance of 50 nF and on-resistance of 1 Ω.

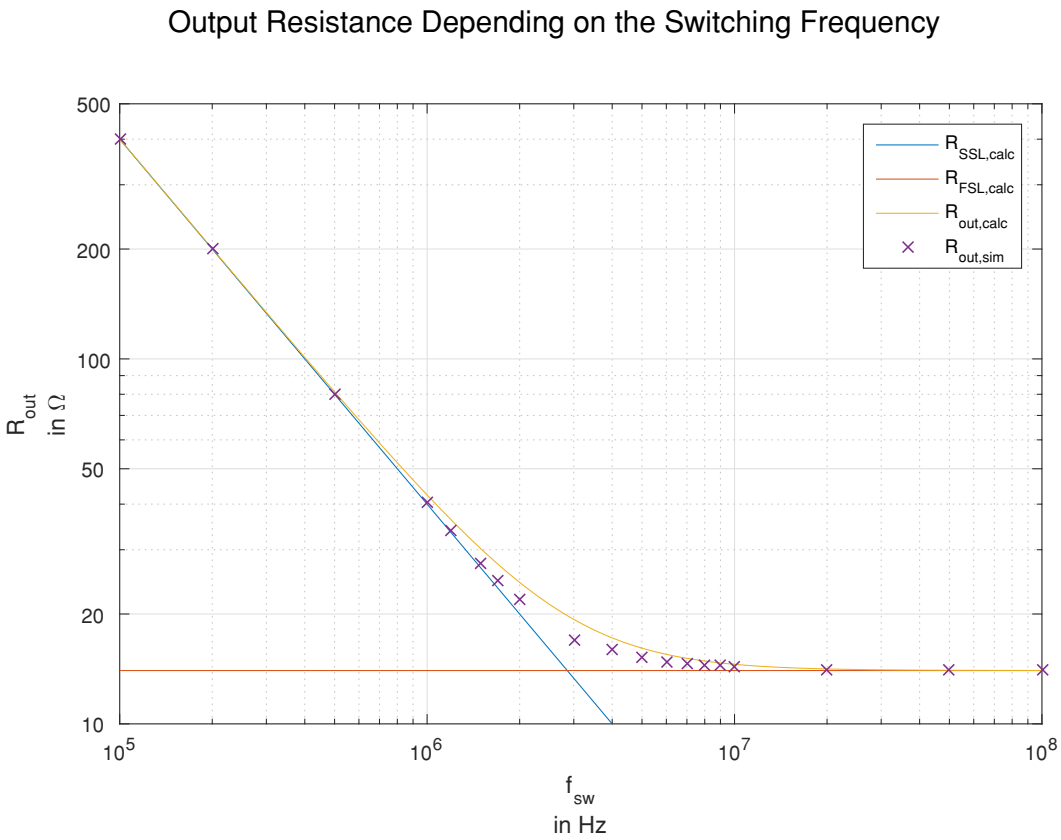


Figure 3.5: Calculated slow switching limit and fast switching limit resistance and approximated output resistance compared to output resistance obtained by simulation, sweeping over switching frequency. The flying capacitances are assumed to be 50 nF and the switches' on-resistance is estimated to be 1 Ω.

integrated circuit (IC). Therefore these three capacitances need to be placed as external components. This introduces additional parasitics through bonding and external wiring. Additionally for these pins electrostatic discharge (ESD) countermeasures need to be considered. Furthermore also a change in the capacitance values of the external components has to be regarded. Furthermore the degradation of the capacitance's effective value due to DC voltage and temperature dependency needs to be considered. The influence of DC voltage dependency is analysed in section 3.4.1.

3.4.1 DC Voltage Dependency

In the following section the influence of DC dependent capacitors (assuming linear DC dependency for simplification) in the circuit is investigated. Therefore charge-based models of capacitors are used that are capable of correctly modelling charge conservation. Basically a dynamic capacitance that is linearly decreasing by an increase in voltage is analysed. With given $C_D(V)$ function, the charge on the capacitance can be modelled as shown in equation 3.9.

$$Q(V) = \int_{v=0}^{V} C_D(v)\,\mathrm{d}v \tag{3.9}$$

The linear DC dependency can be described with equation 3.10.

$$C_D(V) = C_0 + C_1 \cdot |V| \tag{3.10}$$

Therefore the description of the charge being stored on the capacitance is calculated from equation .

$$Q(V) = C_0 \cdot V + \frac{C_1}{2} \cdot V^2 \tag{3.11}$$

For the flying capacitors and the output capacitance the values for C_0 and C_1 that are shown in table 3.3 are taken.

Capacitor	C_0	C_1	V_{max}	$C(V_{max})$
C_{fly}	50 nF	$-\frac{25}{3.3}\,nF\,V^{-1} = -7.58\,nF\,V^{-1}$	3.3 V	25 nF
C_{out}	1 µF	$-\frac{0.5}{6}\,\mu F\,V^{-1} = -83.3\,nF\,V^{-1}$	6.6 V	0.450 µF

Table 3.3: The used values for the flying capacitances and output capacitance and the respective effective capacitance at their maximum voltage.

However as the size of the flying capacitances defines the slow switching limit and therefore also influences the choice of f_{sw} it is important to investigate the influence of this dependency. In this case the voltage swing over the flying capacitance is important as this also determines its effective capacitance. For lower frequencies the voltage swing is obviously greater than for higher frequencies. As the modelled capacitance is linearly decreasing with voltage, one comes to the conclusion that also the effective capacitance is becoming smaller as the voltage across the capacitance does not deviate from V_{DD} that much.

The mentioned dependencies can also be modelled in theory: For steady state when the charge pump is already started up the increase and decrease of voltage is the same for both phases. Therefore the average voltage on both flying capacitances is approximately the median of the maximum and minimum voltage. Therefore the average effective capacitance (C_{avg}) can be calculated by integrating from the minimum to the maximum voltage of the flying capacitance as shown in equation 3.12.

$$C_{avg} = \frac{1}{V_{C_{fly},max} - V_{C_{fly},min}} \cdot \int_{v=V_{C_{fly},min}}^{V_{C_{fly},max}} C_D(v)\,dv \tag{3.12}$$

For a linear DC dependency equation 3.12 simplifies to 3.13.

$$C_{avg} = \frac{C_D\left(V_{C_{fly},max}\right) + C_D\left(V_{C_{fly},min}\right)}{2} \tag{3.13}$$

In general only the slow switching limit is altered by the DC dependent capacitance, as the fast switching limit only depends on resistances. Therefore for the next considerations the behaviour at lower frequencies, where

$R_{\text{out}} \approx R_{\text{SSL}}$ holds true, is analysed. From figure 3.3 the ratio between V_{out} and $V_{\text{out},ideal}$ can be described as a simple voltage divider as shown in equation 3.14.

$$V_{\text{out}} = V_{\text{out},ideal} \cdot \frac{R_{\text{load}}}{R_{\text{out}} + R_{\text{load}}} \tag{3.14}$$

Assuming the fact, that the voltage over both flying capacitances (C_{fly}s) is equal and therefore exactly half of the output voltage, the average effective capacitance can be described by equation 3.15. The maximum voltage $V_{C_{\text{fly}},max}$ is therefore half of the ideal output voltage and the minimum flying capacitance voltage is half of the real output voltage.

$$C_{\text{avg}}\left(V_{\text{out}}\right) = \frac{C_{\text{D}}\left(\frac{V_{\text{out},ideal}}{2}\right) + C_{\text{D}}\left(\frac{V_{\text{out}}}{2}\right)}{2} \tag{3.15}$$

Substituting C_{fly} in equation 3.5 and combining equations 3.10, 3.14 and 3.15 yields 3.16.

$$\begin{aligned} R_{\text{out}} &= \frac{2}{C_{\text{avg}}\left(V_{\text{out}}\left(V_{\text{out},ideal}\right)\right) \cdot f_{\text{sw}}} = \\ &= \frac{2}{\frac{\left(C_0 + C_1 \cdot \frac{\left|V_{\text{out},ideal}\right|}{2}\right) + \left(C_0 + C_1 \cdot \frac{\left|V_{\text{out},ideal}\right|}{2} \cdot \frac{R_{\text{load}}}{R_{\text{out}} + R_{\text{load}}}\right)}{2} \cdot f_{\text{sw}}} \end{aligned} \tag{3.16}$$

Transforming equation 3.16 leads to a quadratic equation for R_{out} . For better readability $2 \cdot C_0 + C_1 \cdot \frac{\left|V_{\text{out},ideal}\right|}{2}$ is substituted by C_x.

$$\underbrace{R_{\text{out}}^2}_{x^2} + \underbrace{R_{\text{out}}}_{x} \underbrace{\left(R_{\text{load}}\left(1 + \frac{C_1}{C_x} \cdot \frac{\left|V_{\text{out},ideal}\right|}{2}\right) - \frac{4}{C_x \cdot f_{\text{sw}}}\right)}_{p(f_{\text{sw}})} + \underbrace{\frac{-4}{C_x \cdot f_{\text{sw}}} \cdot R_{\text{load}}}_{q(f_{\text{sw}})} = 0 \tag{3.17}$$

Solving equation for R_{out} gives the result shown in equation 3.18, whereas one result can be neglected as it would lead to a negative output resistance. However the coefficients p and q depend on

- the load resistance (1 kΩ defined by output current),
- the dynamic capacitance (see equation 3.10 and table 3.3),
- the ideal output voltage ($2 \cdot V_{DD}$) and
- the switching frequency,

but since the first three parameters are already defined by specification, the output resistance can be regarded as only being dependent of switching frequency.

$$R_{out}(f_{sw}) = -\frac{p(f_{sw})}{2} \underset{(-)}{+} \sqrt{\left(\frac{p(f_{sw})}{2}\right)^2 - q(f_{sw})} \tag{3.18}$$

Figure 3.6 shows the calculated and simulated results for using the already specified parameters and sweeping the switching frequency. Obviously for very low frequencys the output capacitance is completely discharged in first phase (parallel) and therefore also the voltage swing over the flying capacitances is at its maximum of V_{DD}. This implies that there is a voltage of half the positive supply voltage on each flying capacitance on average, which leads to an average effective capacitance of about 37.5 nF. The higher the switching frequency becomes, the less the output capacitance is discharged. In this case the voltage swing is minimised too. The slow switching limit resistance then behaves such as there were flying capacitances used that are about 25 nF in size. This transition is happening over about two decades from 10 kHz to 1000 kHz. Finally for higher frequencys (fs) the fast switching limit is dominating again.

However as this Switched-Capacitor circuit should be operated at the transition where slow switching limit and fast switching limit have nearly the same impact, these investigations lead to an increase of the optimum switching frequency. Therefore when operating such an SC DC-DC converter at optimum switching frequency and estimating its performance, it is important to not use the nominal capacitance values, but to use the effective capacitance in a specific operating point. Obviously in this conceptual circuit

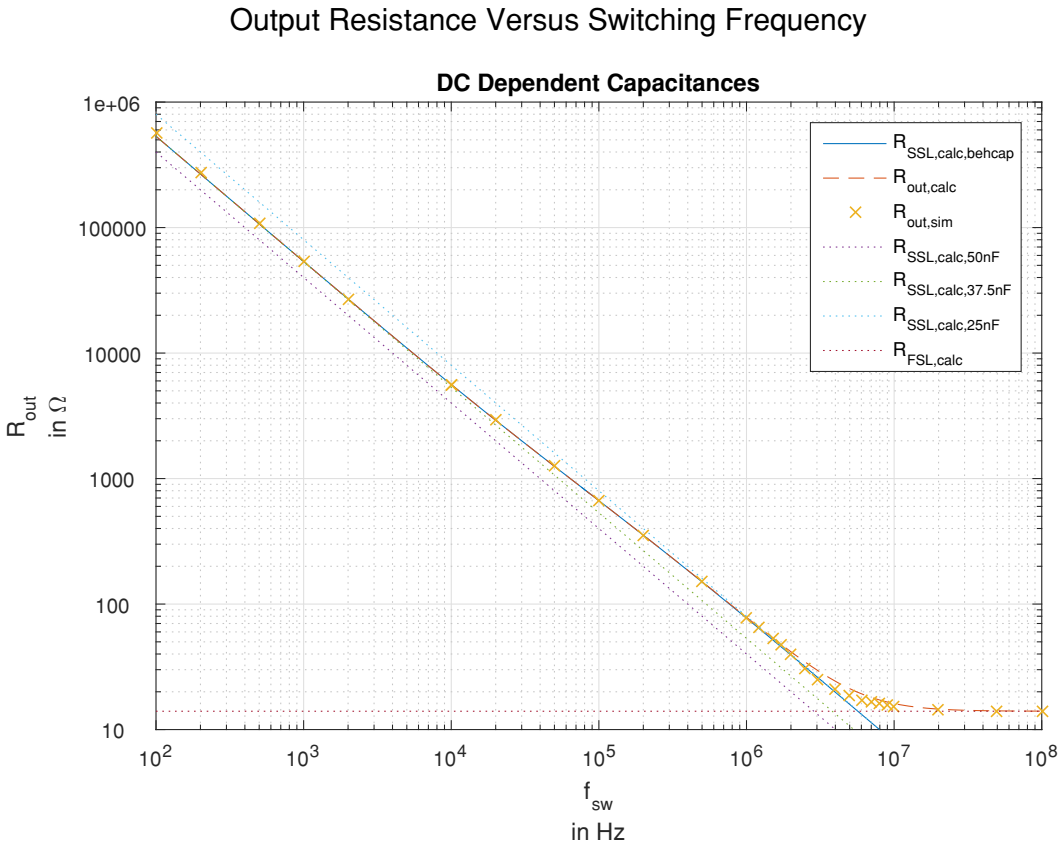


Figure 3.6: Calculated and simulated slow switching limit resistance and output resistance when using DC dependent capacitances. For low frequencies the circuit behaves as if the flying capacitances were about 37.5 nF in size (average effective capacitance for full voltage swing of V_{DD}). As the frequency increases the flying capacitances seem to be 25 nF in size (nearly no voltage swing).

the nominal capacitance nearly had no influence, which is also visible in figure 3.6 (see $R_{\mathrm{SSL},calc,50nF}$), as the simulated output resistance is always greater than the slow switching limit resistance for the capacitance's nominal value.

To conclude, in order to achieve accurate simulation results the mentioned non-ideal DC voltage dependent behaviour needs to be considered. Therefore it is necessary to model the presumably used capacitances in the design phase, according to the manufacturer's datasheet or to use its effective values for that specific operating point.

4 Design

This chapter explains the implementation of the concepts that were described in chapter 3 (Concept), in CMOS technology. This includes phase generation, design of switches, voltage buffers, level shifters and external component modelling.

4.1 Phase Creation

As in most SC designs also in this design non-overlapping clock phases need to be used. However there have to be four transition signals, that have to be non-overlapping each. This leads to the conclusion that a combination of more two-phase non-overlapping clock generators cannot be used. In general creating more than two non-overlapping transitions often leads to higher design efforts. Therefore a different approach, which is easily extendable, is described in this section.

In this project's design the transition delay is created by the use of simple reset-set flip-flops (RS-flip-flops). The basic idea lies in propagating the set signals from first RS-flip-flop to last on the rising edge of clock and propagating the reset signal from last to first on the falling edge of clock.

Before describing the use of the RS-flip-flop another circuit is described in order to prevent getting into metastable state. This is the case, if set and reset signals are high at the same time. In order to prevent this, the circuit shown in Figure 4.1 is used. The signals *sig_a* and *sig_b* represent the *set* and *reset* signals. When both signals are set to high, then a zero is selected on the multiplexer. This prevents, that both inputs of the RS-flip-flop are set to high as either *sig_a* is propagated if *sig_b* is low or zero is propagated.

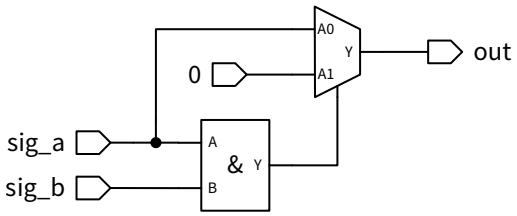


Figure 4.1: Circuit for selecting signals to prevent metastable state in RS-flip-flop.

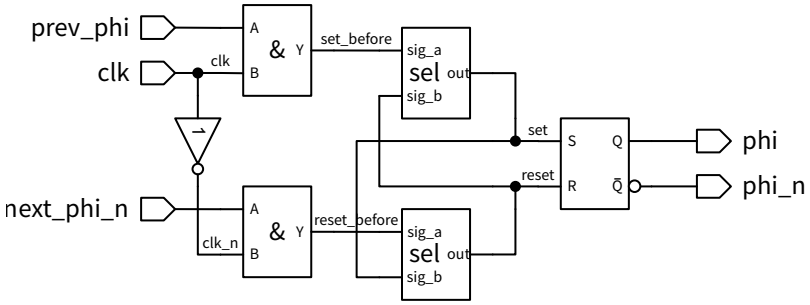


Figure 4.2: Circuit for a single non-overlapping stage.

The described circuit can further on be used in a single stage of the non-overlapping clock generator that is shown in Figure 4.2. Basically there are three inputs for a single stage. These are the transition signal of the previous stage, the inverted signal of the subsequent stage and the clock. The outputs are the transition signal and the inverted signal of the current stage. In principle the previous transition signal *prev_phi* is only propagated through the AND-gate if the clock is high, therefore setting the RS-flip-flop. The similar is true after the falling edge of clock, when the inverted subsequent transition signal *next_phi_n* is propagated and resetting the RS-flip-flop. In between there is the already mentioned circuit for preventing a metastable RS-flip-flop state.

These single stages can then be combined in order to create more non-overlapping signals. When needing four transition signals this can be done as shown in Figure 4.3. It is important to note that the previous transition signal of the first stage and the next/subsequent transition signal of the last stage have to be set to high all the time, as there is no previous respectively subsequent stage that has to be waited for. The advantage with this approach lies in the expandability, as for more non-overlapping transition signals

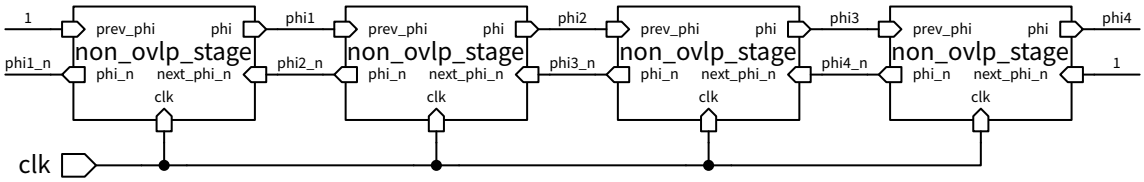


Figure 4.3: Circuit combining single stages to get four non-overlapping transition signals.

simply more stages can be added. Furthermore also existing approaches for adding more delay, that are used in simple two-phase non-overlapping clock generators, can be used with this principle. This can either be done by adding inverters in the *phi* and *phi_n* branch or by adding capacitances. In this way also different delays for rising and falling edge of clock can be created.

Figure 4.4 shows the resulting signals when applying a clock signal to the described circuit. It is visible that the transition signals are non-overlapping each.

4.2 Switches

The following section describes the design of the seven switches sequentially. In some circuits some transistors are greyed out for better understanding. Table 4.1 shows a summary of the voltages on the switches and the used topology.

4.2.1 Switch One (S1)

The first switch is used for connecting the top plate of the first flying capacitance (C_{fly1}) to V_{SS}. Therefore one terminal is always on V_{SS}, whereas the other terminal switches between V_{DD} and V_{SS}. In this way the maximum drain-source voltage over this switch does not exceed the save operating area for one transistor device. Additionally the gate can be directly driven by $\phi_{4,5}$, for what reason a simple NMOS can be used.

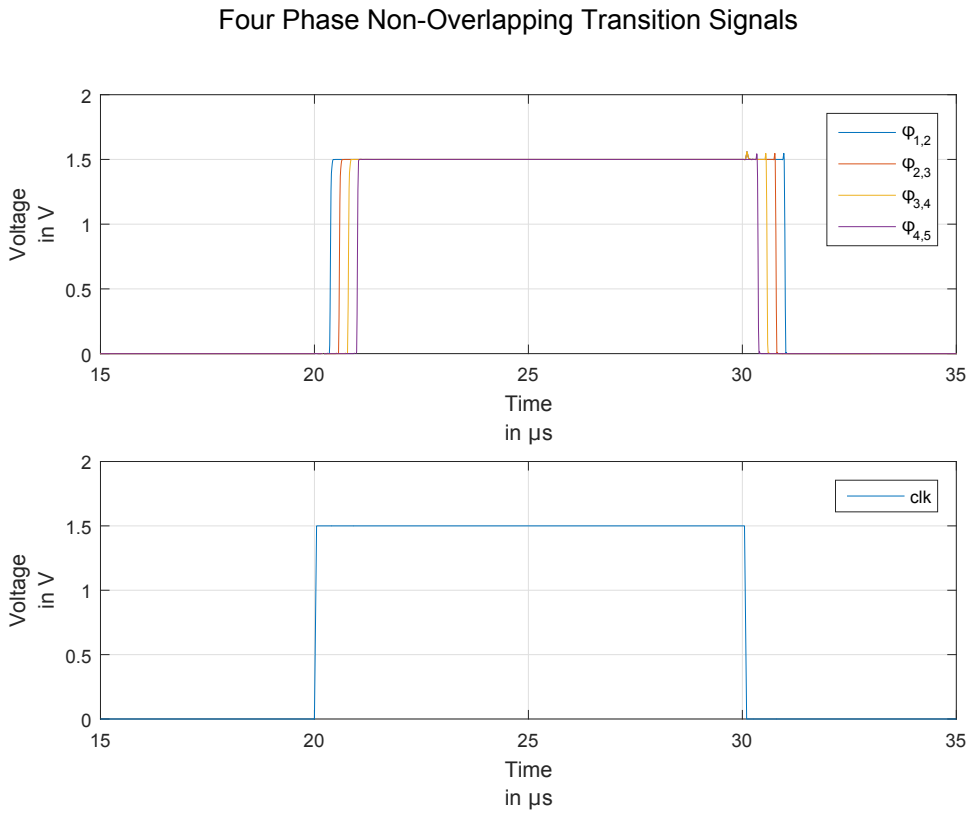
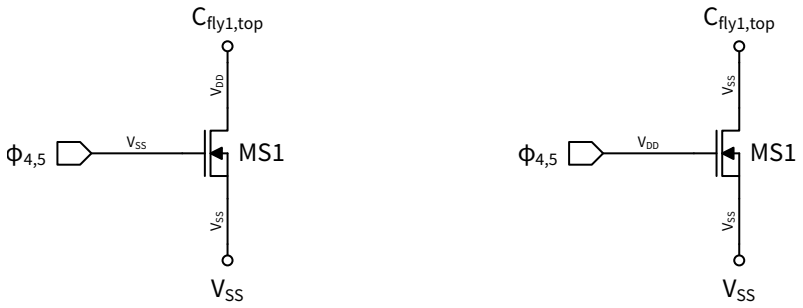


Figure 4.4: Resulting transition signals to control the states of the SC circuit.

Switch	Phase				Topology
	Parallel		Series		
S1	V_{DD}	V_{SS}	V_{SS}	V_{SS}	NMOS
S2	V_{DD}	V_{DD}	V_{DD}	V_{SS}	PMOS
S3	V_{SS}	V_{SS}	V_{SS}	$-V_{DD}$	NMOS
S4	V_{SS}	V_{DD}	$-V_{DD}$	$-V_{DD}$	NMOS
S5	V_{DD}	V_{DD}	V_{DD}	$-V_{DD}$	2 PMOS in series
S6	V_{SS}	V_{SS}	V_{SS}	$-2 \cdot V_{DD}$	2 PMOS in series
S7	V_{SS}	$-2 \cdot V_{DD}$	$-2 \cdot V_{DD}$	$-2 \cdot V_{DD}$	2 NMOS in series

Table 4.1: States of the switches in between the four phases.



(a) Node voltages for switch one in states one to four (before transition of $\Phi_{4,5}$).

(b) Node voltages for switch one in phase five (after transition of $\Phi_{4,5}$).

Figure 4.5: For implementing switch one a simple NMOS transistor can be used.

Figure 4.5 shows the different states the switch and its terminals can be in. Basically there are only two different states:

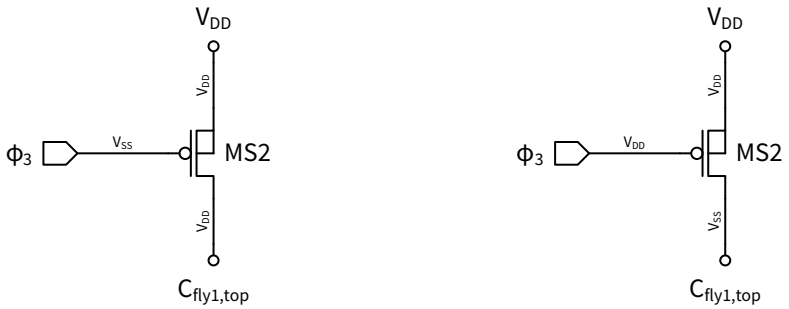
- In state one to four (before the transition of $\Phi_{4,5}$), the transistor is not conducting, as the flying capacitance is charged in parallel. It has to be mentioned that the node voltage of $C_{\text{fly1},top}$ in phase 4 is not very well defined as it only sees high impedances.
- In the fifth state (after the transition of $\Phi_{4,5}$, the switch is closed and therefore pulling the capacitance's top plate to V_{SS}.

4.2.2 Switch Two (S2)

The second switch is responsible for connecting the first flying capacitance's top plate to V_{DD}. Basically it is analogous to switch one, with the difference that a PMOS transistor suits better, in order to be able to drive the gate directly by $\Phi_{3,4}$.

Again there are two states the switch can be in. These are shown in figure 4.6.

- In the first three states the transistor is conducting and therefore the flying capacitance is charged.



(a) Node voltages for switch two in states one to three (before transition of $\Phi_{3,4}$).

(b) Node voltages for switch two in states four and five (after transition of $\Phi_{3,4}$).

Figure 4.6: For implementing switch two a simple PMOS transistor can be used.

- For the last two states the switch is opened, in order to be able to push the capacitance's top plate down to V_{SS} by switch one. As already mentioned in section 4.2.1 this node is high impedance in phase 4, which comes from the needed non-overlapping control signals.

4.2.3 Switch Three (S3)

The third switch is needed in order to connect the flying capacitance's bottom plate to V_{SS}. When closed, it enables the charging of the flying capacitance in parallel phase. One terminal is tied constantly to V_{SS}, whereas the other terminal of the switch changes its voltage from V_{SS} to $-V_{DD}$, when the flying capacitance is pushed down in potential by switch one. As the nodes reach voltages below substrate, which is at V_{SS}, a simple NMOS transistor is not sufficient as its usage would lead to a forward biased diode from bulk, that is equal to the substrate, to the negative terminal.

Therefore two other possibilities can be considered.

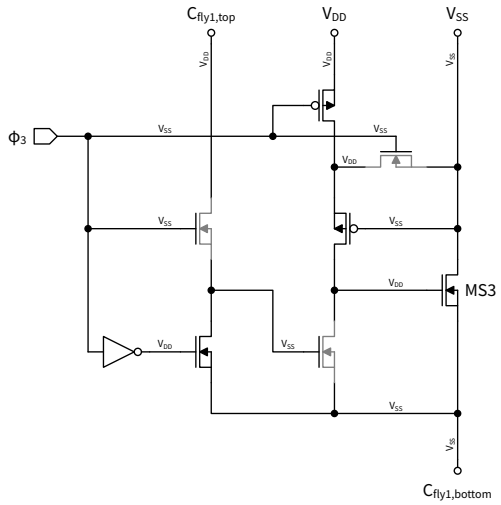
- The first one would be the use of a PMOS transistor, as its bulk is not inherently connected to any specific node and it can be placed according to one's needs. However using a PMOS transistor would require negative gate voltages (about $-V_{DD}$) in the parallel phase, where these are not directly available.

- Thus the second possibility is to use a triple-well NMOS, that is available in the used process. With this device the bulk can be set to negative voltages in order to avoid forward biased diodes. In this way the gate driving is simplified as there are only voltages needed that are actually available in the respective phases.

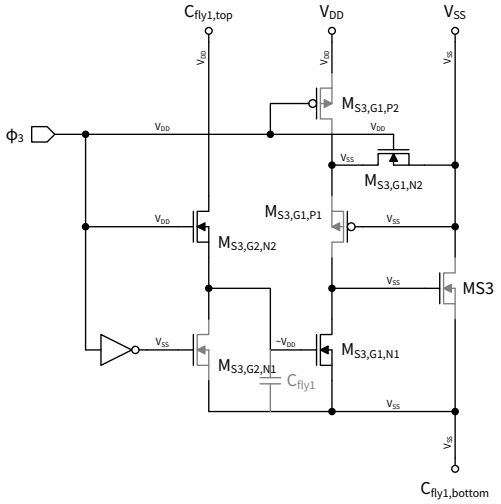
Figure 4.7 shows the implementation of switch three, including its gate driving circuit. Here a similar approach, which was suggested by [2], was used (summarised in section **??**). The general idea is to use voltages that are already available in the specific phases. The advantage comes along with not needing to separately create additional voltages.

Basically there are three important states the circuit for switch three can be in.

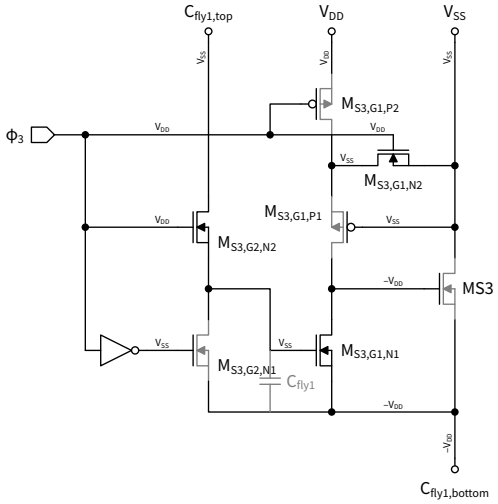
- In the first three state states (before the transition of $\Phi_{3,4}$) the switch is conducting and therefore needs its gate to be set to V_{DD}. This is done by the two PMOS transistors $M_{S3,G1,P1}$ and $M_{S3,G1,P2}$. The reason for using two transistors in series is to not exceed save operating area as the maximum voltage difference between V_{DD} and the gate of M_{S3} can reach up to two times V_{DD}. Transistor $M_{S3,G1,N2}$ is used for defining the node voltage in between the two PMOS transistors better and is turned on and off exactly vice-versa.
- The fourth state (after transition of $\Phi_{3,4}$ and before transition of $\Phi_{4,5}$) is defined in opening the switch by pulling its gate to the bottom plate of the flying capacitance. This is done by transistor $M_{S3,G1,N1}$ whose gate is driven up the node of the top plate of the flying capacitance. By using this topology the gate-source voltage of $M_{S3,G1,N1}$ is exactly the capacitance's voltage. This is also shown in Figure 4.7b.
- Therefore in the fifth state (after the transition of $\Phi_{4,5}$) when the flying capacitance is pushed down by switch one, the gates of transistors M_{S3} and $M_{S3,G1,N1}$ are also pulled down accordingly. In this way the concept is fulfilled, that the operating region of the transistors in not changed from state four to state five.



(a) Node voltages for switch three in states one to three (before transition of $\Phi_{3,4}$).



(b) Node voltages for switch three in state four (after transition of $\Phi_{3,4}$, before transition of $\Phi_{4,5}$).



(c) Node voltages for switch three in state five (after transition of $\Phi_{4,5}$).

Figure 4.7: Circuit for switch three.

4.2.4 Switch Four (S4)

The fourth switch is used for connecting the first capacitance's bottom plate with the second capacitance's top plate in series phase. Due to the selection of three phases (see section 3.2) one triple-well NMOS can be used. For two phases only an additional transistor in series would have to be used. Again a similar principle as in subsection 4.2.3 is applied, by using the first flying capacitance to define the gate-source voltage of switch four. Furthermore the node voltages have to go below substrate which makes a standard NMOS not applicable.

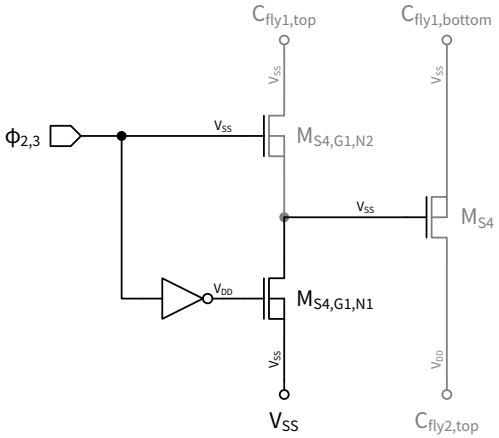
Figure 4.8 shows the circuit for switch four. Basically the already mentioned triple-well NMOS is used which is driven by two other NMOS transistors.

- For states one and two the switch is in off state as its gate is pulled to negative supply voltage (V_{SS}) by $M_{S4,G1,N1}$. This needs be done in parallel phase.
- In state three and four $M_{S4,G1,N2}$ is conducting and therefore pulling the gate's voltage to about $V_{DD} - V_{TH}$. Therefore M_{S4} is turned on and conducting current.
- In fifth state the first flying capacitance's top plate is pushed down by switch one, therefore also pushing the switch's terminals down by the voltage, that is on the capacitance. In this concept again the flying capacitance is put between gate and source terminal of the switch, therefore keeping it enabled during being pushed down.

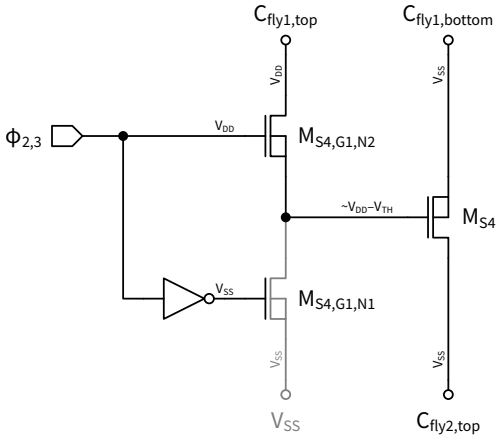
4.2.5 Switch Five (S5)

Switch five is responsible for connecting the second flying capacitance's top plate to V_{DD} in parallel phase. However there are two possible design approaches.

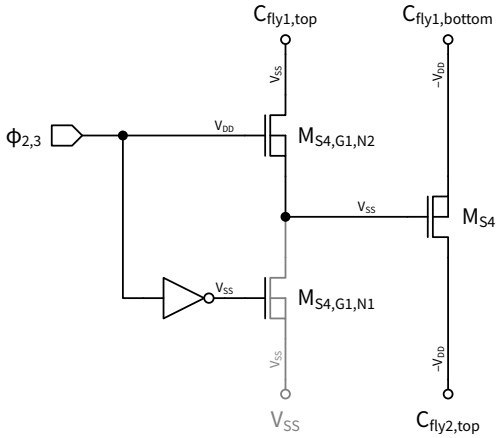
- When using standard PMOS devices it is necessary to use two switches in series in order to stand the maximum voltage drop of two times V_{DD} in series phase. This can be seen in Figure 4.9a. There is an additional NMOS introduced in order to keep the high impedance node between



(a) Node voltages for switch four in states one and two (before transition of $\Phi_{2,3}$).

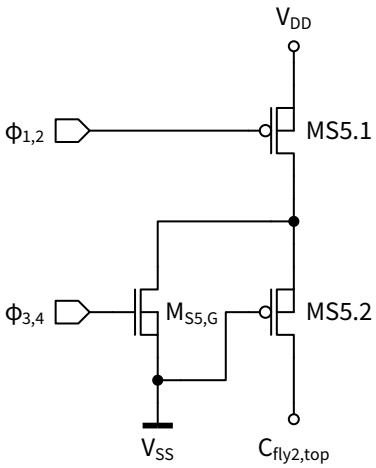


(b) Node voltages for switch four in state three (after transition of $\Phi_{2,3}$, before transition of $\Phi_{3,4}$).

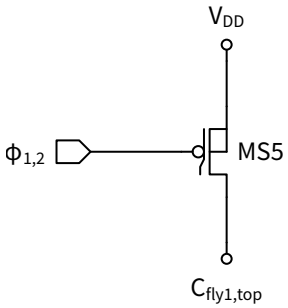


(c) Node voltages for switch four in state four and five (after transition of $\Phi_{3,4}$).

Figure 4.8: Circuit for switch four.



(a) Circuit for switch five using two stacked PMOS devices.



(b) Circuit for switch five using a single DeMOS PMOS devices.

Figure 4.9: Circuitry for switch five.

the transistors on a well defined potential. This simplifies staying in SOA. The disadvantage comes in the series connection of the switches, which leads to a much higher area consumption compared to a single transistor. Furthermore it also demands the use of two transition signals.

- The second approach includes the use of a drain-extended MOSFET (DeMOS) (see Figure 4.9b), which was already described in section 2.3 and in [4], [5]. This device is designed for standing higher drain-source voltages leading to only needing a single transistor and a single transition signal. Therefore this switch is simplified. However as both nodes have connections to the outside ESD measures have to be considered. [20] explains the impacts of bipolar turn-on, impact ionisation and charge modulation under ESD conditions. Due to the extended drain region also the R_{ON} is increasing which again leads to higher area demand.

In order to determine which solution is better some simple simulations are done. A small voltage of about 10 mV is applied on both switches, whereas the transistors are set to their respective maximum gate-source voltages. These can therefore be considered as closed and conducting. By taking the

settled direct current (DC) current, each switches' on-resistance is calculated. In order to reasonably compare the two approaches, their performance is compared with respect to area (A) consumption. The calculation of respective widths is shown in equations 4.1 and 4.2, where obviously the shortest possible channel length is used. The factor of one half at the PMOS width comes from the fact of using two transistors in series. The NMOS is negligible in size and is therefore not considered in these calculations.

$$W_{PMOS} = \frac{A}{2 \cdot L_{PMOS,min}} \tag{4.1}$$

$$W_{DeMOS} = \frac{A}{L_{DeMOS,min}} \tag{4.2}$$

Figure 4.10 shows the results of this comparison. It is visible that for same area the stacked PMOS approach leads to about half the on-resistance compared to the DeMOS. For this reason the switch is implemented as shown in Figure 4.9a by the use of two PMOS in series.

4.2.6 Switch Six (S6)

Switch six connects the second flying capacitance's bottom plate to V_{SS} in parallel phase. Basically there are again different possibilities to implement this switch. In general DeMOS devices could be used, but based on the results from section 4.2.5 these are not discussed further due to their worse performance. However there still remains the possibility to use either two NMOS or two PMOS devices in series. In order to determine the applicability the gate voltages are looked at.

- Using NMOS devices requires gate voltages of V_{DD} on both gates in parallel phase and voltages of $-V_{DD}$ and $-2 \cdot V_{DD}$ in series phase. The advantage is that all node voltages are available in their respective phases, taking the external capacitance's top or bottom plates. Nevertheless the high voltage swing on the gate increases the switching effort, as there are voltages up to $3 \cdot V_{DD}$ that need to be switched. This even worsens the problem at first glance.

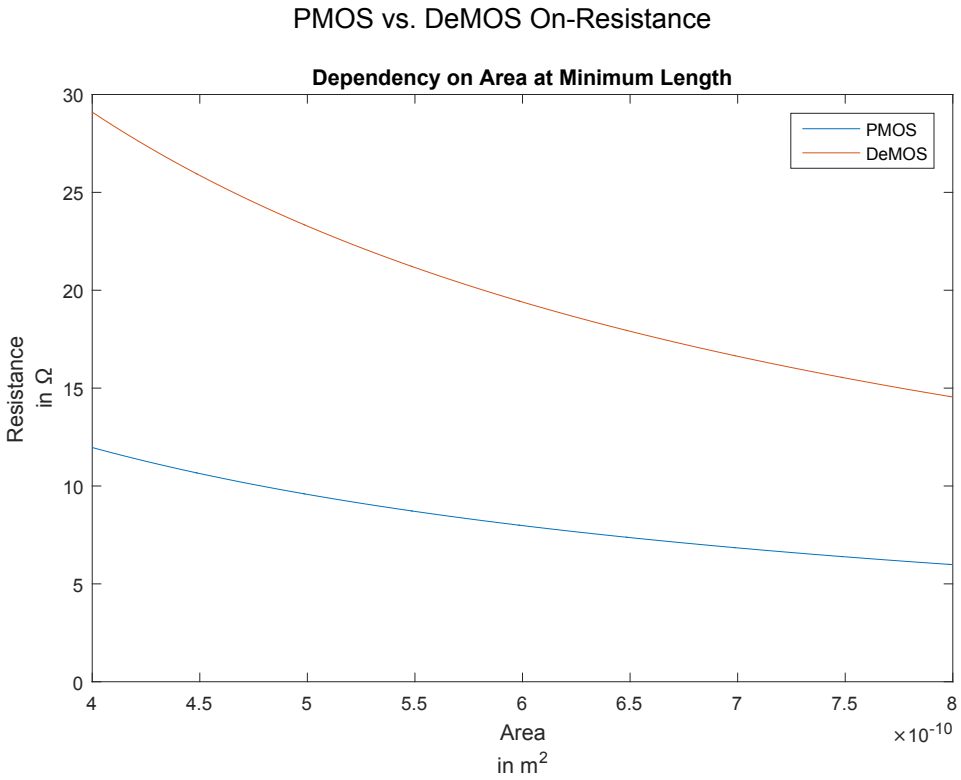


Figure 4.10: Comparison of on-resistance of PMOS and DeMOS with respect to area consumption at minimum channel length.

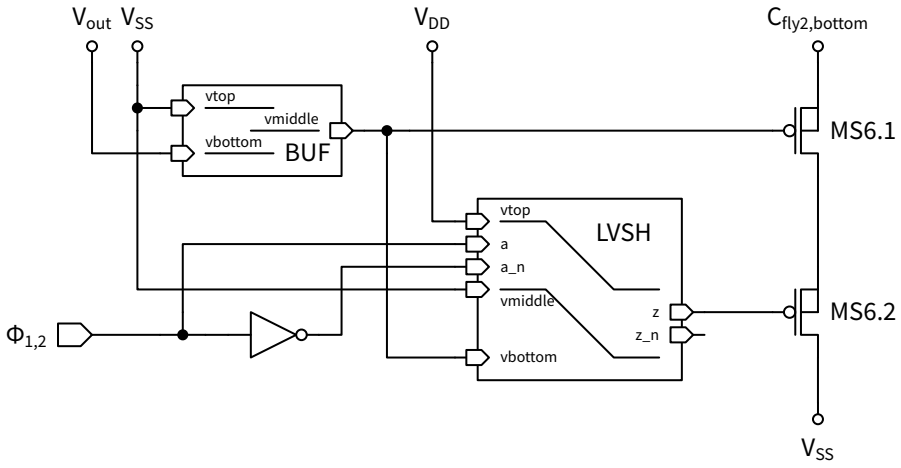


Figure 4.11: Circuit for switch six including voltage buffer and level shifter.

- The alternative is using PMOS devices. In this case one gate voltage can stay constant at $-V_{DD}$, whereas the other gate has to be switched between V_{SS} and $-V_{DD}$, obviously reducing gate voltage swing. The disadvantage with this implementation lies in the fact, that in parallel phase no well-defined $-V_{DD}$ potential is available. Therefore an additional block is required, which is capable of creating $-V_{DD}$ from V_{SS} and $-2 \cdot V_{DD}$ inputs.

Due to less switching effort the second approach with two PMOS is implemented. Therefore a voltage buffer for $-V_{DD}$ (see section 4.3) and a level shifter (see section 4.4) are needed. Figure 4.11 describes the used circuit. As already mentioned one gate is on $-V_{DD}$ constantly, whereas the other one is driven by the level shifter and the transition signal $\phi_{1,2}$.

4.2.7 Switch Seven (S7)

Switch seven - the last described switch - connects the flying capacitance to the output capacitance. In this case the use of two NMOS suits best. It is not possible to use a DeMOS NMOS since there is no triple-well DeMOS NMOS available in this technology. Therefore again a voltage buffer and two level shifters are needed as one gate driving voltage has to be shifted by $2 \cdot V_{DD}$.

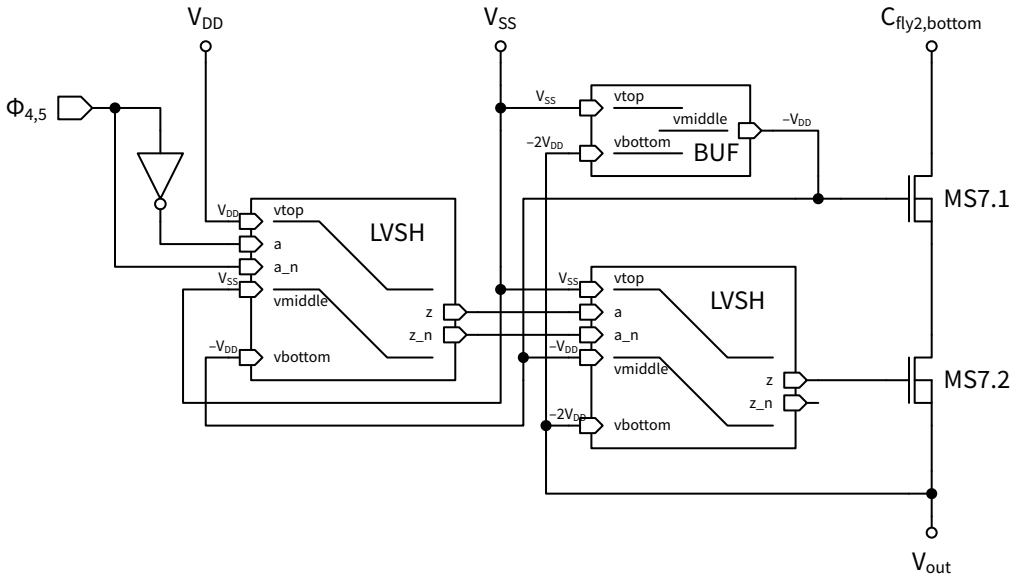


Figure 4.12: Circuit for switch seven including voltage buffer and two level shifters.

These are basically the same blocks, that are already used in section 4.2.6 and described in sections 4.3 and 4.4.

Figure 4.12 shows the used blocks. The transition signal $\phi_{4,5}$ is shifted down by V_{DD} two times. The voltage of $-V_{\mathrm{DD}}$ can be created with the same block, that is already used for switch six.

4.3 Complementary Source Follower

A complementary source follower is used for generating $-V_{\mathrm{DD}}$ voltage for parallel phase. The general principle is shown in Figure 4.13. Basically there are two branches, where current is flowing. In one branch N_1 and P_1 are diode connected each, therefore defining their respective gate-source voltages. These voltages are mirrored to the second branch. If a load is applied to the output, the output node voltage is pulled down. This increases the gate-source voltage of N_2 and decreases V_{GS} of P_2, and is therefore

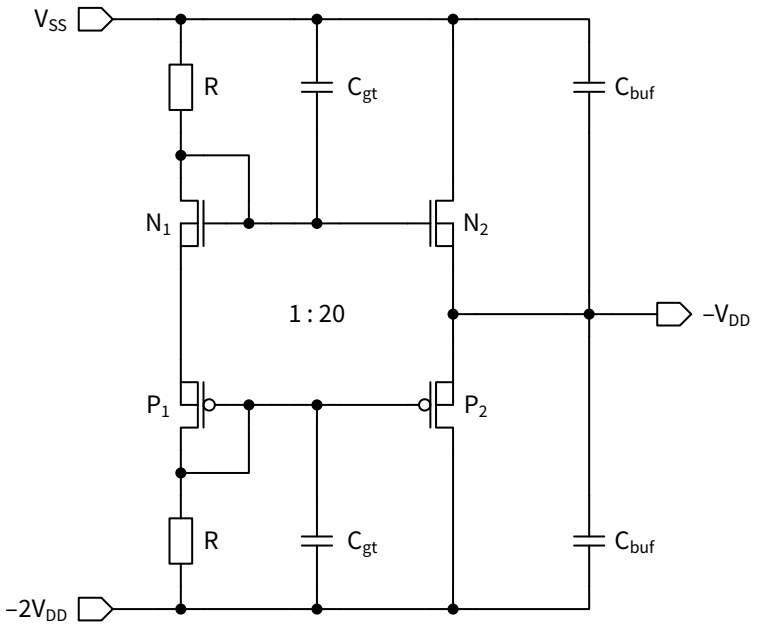


Figure 4.13: Complementary source follower used as voltage buffer for $-V_{\mathrm{DD}}$.

counteracting the voltage decrease by allowing more current to flow into that node.

By the $\frac{W}{L}$ ratios between first and second branch and the current consumption the strength of the buffer can be defined. However it has to be paid attention that SOA is not exceeded, which would be the case if the applied load is too high. Therefore buffer capacitances (C_{buf}) are added in order to withstand higher transients. The gate capacitances (C_{gt}) are needed to reduce the influence of the gate-source capacitance on the gate potential when the output node is changing.

However increasing the ratio between first and second branch also leads to higher static power dissipation. However an idea could be to define the gate-source voltages of all transistors in a way, that it is about threshold voltage. In this way the ratio could be increased, while having less static current flowing through the branches. By pulling or pushing the output node the transistors are forcing higher currents, due to higher gate-source voltage. However this would require more area, as the current that can be

forced is smaller the smaller gate-source voltage is.

4.4 Level Shifter

Along with a voltage buffer also a level shifting circuit is needed in order to drive one PMOS's gate between V_{SS} and $-V_{DD}$. Again considering SOA a conventional level shifter is not sufficient. Therefore a level shifter with cascodes is needed. The design that is used in this project is generally taken from [21].

Figure 4.14 shows the used level shifting circuit. The voltage level of the input signal is ranging in between *vtop* and *vmiddle* and is translated to an output signal from *vmiddle* to *vbottom*. There is an NMOS and a PMOS cross-coupled pair, which flip at a change of the input signal. In order to block higher frequencies capacitances are added at each input. Furthermore two inverter stages, that are increasing in size, are introduced to the output in order to get a well-defined output, that is decoupled from flipping branches.

A problem in the suggested circuit from [21] comes up if slow transients are applied to the input signals *a* and *a_n*. However the level shifter does not flip completely over, but there is a static current flowing through either one of the branches, that are formed by P_1, P_3 and N_5. If the resistors are not present ($R = 0\,\Omega$), the current only causes a voltage drop of about 0.7V over N_5, which was determined by simulation. This voltage drop is not sufficient for enabling N_6, which then causes the transistor N_5 to stay on. Basically the level shifter does not flip over as expected. Obviously the same is true for the opposite direction with transistors P_2, P_4, N_4 and N_6, which do not turn N_5 on.

Figure 4.15a shows this fact for no resistance ($R = 0\,\Omega$), as it is visible, that current is constantly flowing through either one of the branches. Additionally it is also visible that, the output is inverted to the expected behaviour as the stage can not flip.

In order to circumvent this problem the series resistances are used to generate a higher gate-source voltage at N_6. By switching on N_6 sufficiently,

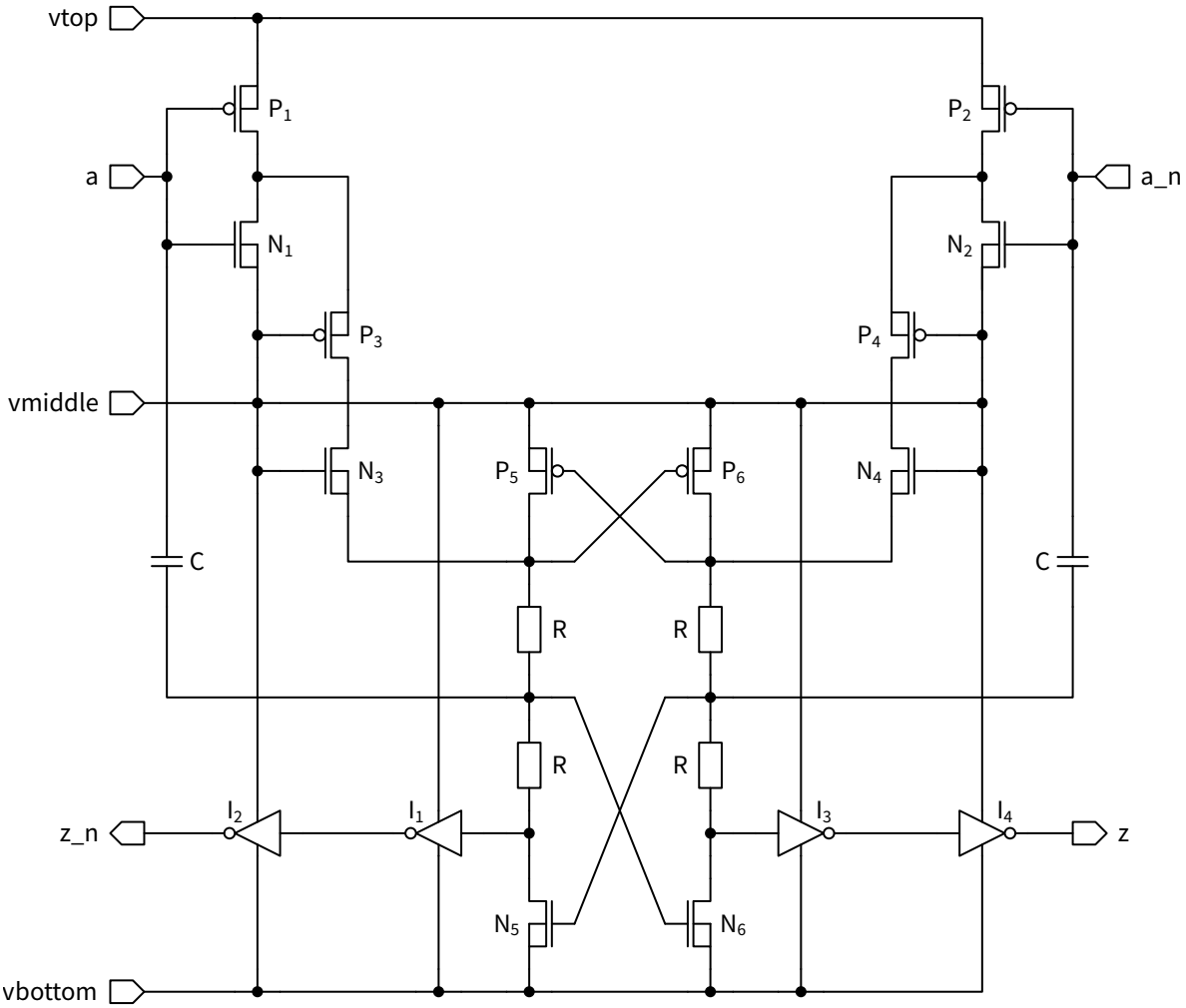
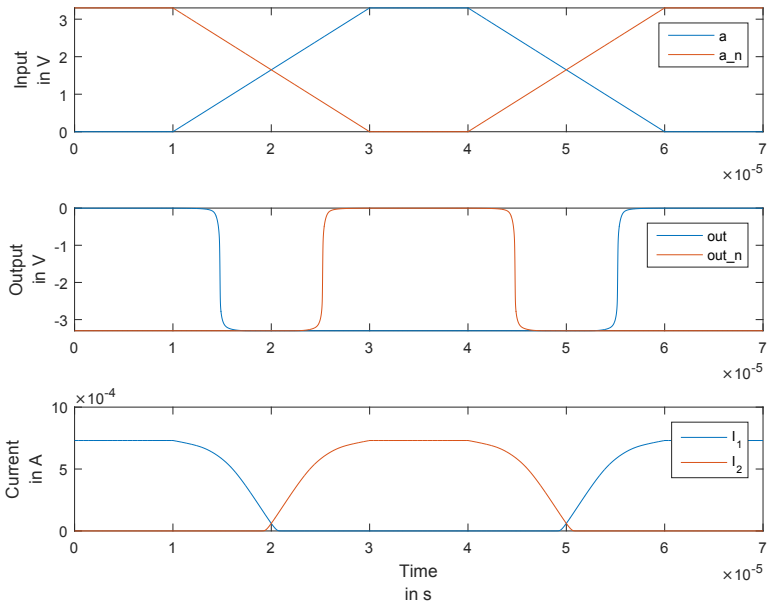
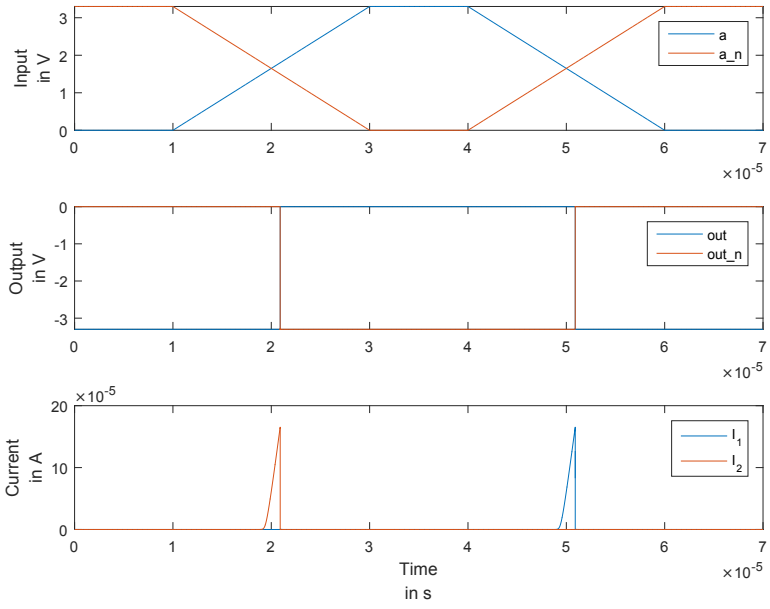


Figure 4.14: Level shifter for shifting transition signal down by V_{DD}.



(a) Level shifter with $R = 0\,\Omega$.



(b) Level shifter with $R = 3\,\mathrm{k}\Omega$.

Figure 4.15: Simulations for level shifter.

N_5 is turned off and the circuit flips and does not consume any static current, as it was happening before. This can be seen in Figure 4.15b, where a resistance of about 3 kΩ was used. In this case the outputs settle properly and current is only flowing during switching.

4.5 Externals

This section deals with modelling external components such as the used external capacitances or bond wires. This is done in order to get more accurate simulation results.

4.5.1 Modelling External Capacitances

In order to correctly model the capacitance the real capacitance values depending on the DC voltage need to be known. These can be acquired from the manufacturer's datasheet. As a simulation program with integrated circuit emphasis (SPICE) simulator is used, the external capacitances can therefore be modelled by a charge based model or a capacitance based model.

However as explained in section 2.8 it is better to use the charge based model, as it includes charge conservation. Therefore the charge has to be defined by static capacitance and voltage over the capacitance. However most manufacturer's datasheets only specify a piecewise linear (PWL) function for dynamic capacitance.

The problem lies in the fact, that in order to get static capacitance, dynamic capacitance has to be integrated. Nevertheless integrating PWL functions, leads to piecewise quadratic functions, whose edges have to be adjusted by the constant introduced by integration so that the function is continuous. One problem lies in SPICE syntax, which does not allow to call functions recursively. In this way the problem becomes too complex. Therefore a better solution consists in curve fitting by using a polynomial function, to model the PWL function. Integrating the resulting polynomial function represents less effort, leading to sufficiently accurate results. Furthermore

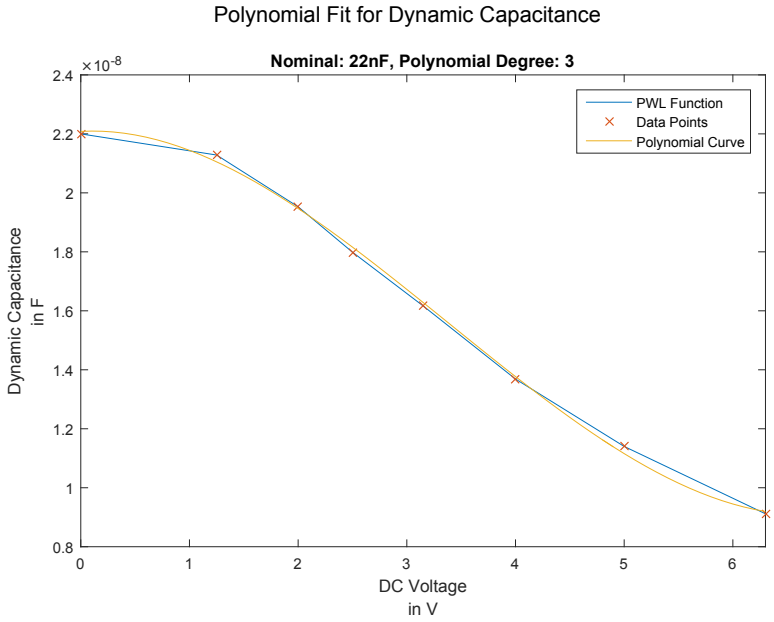
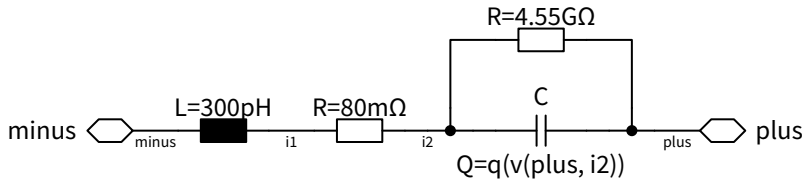


Figure 4.16: Data points, PWL function and polynomial curve with degree 3.

these functions do not have non-differentiable points, which would be the case when using the previously mentioned piecewise functions.

Figure 4.16 shows the data points and PWL function and the polynomially fitted curve. The polynomial degree was swept and finally the best result was selected by visible inspection. In this case it turns out, that a polynomial curve with degree 3 suits very well. Of course this could also be done by an error function.

The implemented model for the capacitance is depictured in Figure 4.17. It consists of a resistance in parallel and in series to the capacitance and an inductance. The values are taken from the corresponding datasheet. The charge based model is implemented by the use of SPICE functions. The first function *p(i)*, is simply used as an array for the polynomial values. *q2(v)* represents the integral of the polynomial curve for dynamic capacitance. However in order for proper assignment of signs and directions an additional function *q(v)* is used. The absolute value of voltage is passed to *q2(v)* leading to a symmetrical behaviour, independent of voltage direction.




```
.func p(i) = 'i <= 0 ? 2.21e-08 : i <= 1 ? 2.09e-10 : i <= 2 ? -9.44e-10 : 9.31e-11'
.func q2(v) = 'p(0)*v + p(1)/2*v**2 + p(2)/3*v**3 + p(3)/4*v**4'
.func q(v) = 'sign(v)*q2(abs(v))'
```

Figure 4.17: Model for the external flying capacitances using charge based capacitance model implemented by SPICE functions.

The sign is afterwards appended accordingly. The function $q(v)$ receives the voltage across the capacitance.

These SPICE functions are directly defined in the specific subcircuit. This has the advantage that the functions are only visible within the subcircuit's scope. Therefore more subcircuits with different parameters can be used in one simulation without them interfering each other.

4.5.2 Modelling Bond Wires

Another important part when using external components is to consider the influence of the bond wires within the package. In this case especially external inductances may have non-negligible effect on the charge pump's performance. Therefore simple models are used to design these parasitics. Basically the bond wire inductance and capacitance are modelled based on a bond wire length. Some basic rules of thumb and typical values can be found in [22] and [23]. The inductance can be assumed to be about $1\,\mathrm{nH\,mm^{-1}}$, whereas the capacitance is assumed to be in a range of about $40\,\mathrm{fF\,mm^{-1}}$.

Figure 4.18 shows the modelled parasitics for the bond wire and PCB. The inductance is split into two equal parts. At the medium node the bond wire capacitance is attached. Furthermore also the inductance of the PCB is assumed to be about 2 mm size. For this assumption to hold true, it is

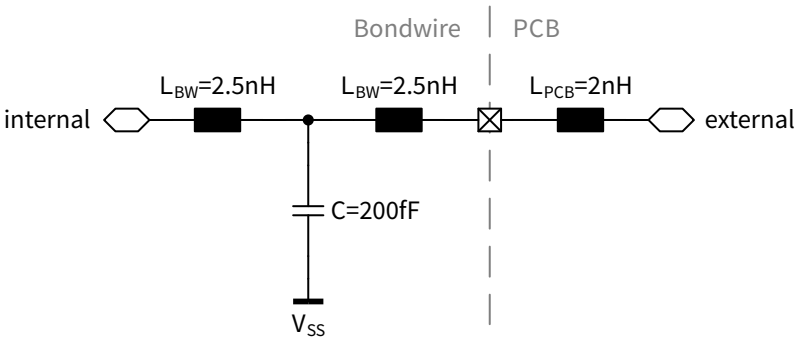


Figure 4.18: Model for bond wires and printed circuit board (PCB) parasitics.

therefore important to keep the flying capacitances as close to the IC pins as possible.

5 Verification

This chapter deals with the verification of the implemented charge pump, showing and comparing the simulation results from chapter 3 (Concept) and chapter 4 (Design). Furthermore additional aspects of optimisation are mentioned.

5.1 Output Resistance

In this section the resulting equivalent output resistance of the charge pump will be investigated. The results will be compared to the results from section 3.3, adapted to the actually used values for the flying capacitances.

To start, a desired output resistance is set by $R_{out} < 65\,\Omega$. From the knowledge of subsection 3.3.3, that the frequency should be set near the crossing of fast switching limit resistance and slow switching limit resistance, this leads to the constraint that $R_{\mathrm{SSL}} \approx R_{\mathrm{FSL}}$. In this way equation 5.1 can be used, assuming the approximation in equation 2.5 holds true.

$$R_{\mathrm{SSL}} = R_{\mathrm{FSL}} = \frac{R_{out}}{\sqrt{2}} = \frac{65\,\Omega}{\sqrt{2}} = 46\,\Omega \tag{5.1}$$

Using these definitions for the fast and slow switching limits also the frequency can be caluclated for known values of the flying capacitances. These are set to be $C_{\mathrm{fly}} = C_{\mathrm{fly1}} = C_{\mathrm{fly2}} = 22\,\mathrm{nF}$ in effective capacitance value. By solving equation 3.4 with respect to f_{sw}, equation 5.2 is given.

$$f_{\mathrm{sw}} = \frac{2}{C_{\mathrm{fly}}} \cdot \frac{1}{R_{\mathrm{SSL}}} = \frac{2}{22\,\mathrm{nF}} \cdot \frac{1}{46\,\Omega} = 1.98\,\mathrm{MHz} \approx 2\,\mathrm{MHz} \tag{5.2}$$

Therefore a switching frequency of about 2 MHz is selected. For the following simulation the on-resistance of the switches was set to reach a fast switching limit resistance of 46 Ω. Further details concerning the sizing of the switches is given in section 5.2. The flying capacitances and the switching frequency are set as described before.

Averaging over the output voltage gives a value of $V_{out,avg} = -6.175\,\mathrm{V}$. The load current is set to $I_{out,load,avg} = -6\,\mathrm{mA}$. However also the current that is needed for supplying the level shifter and the complementary source follower from the negative domain needs to be included in these calculations. It is in average at about $I_{out,sup,avg} = -385\,\mu\mathrm{A}$. Using this information the effective output resistance can be calculated using equation 5.3.

$$R_{out,eff} = \frac{V_{out,ideal} - V_{out,avg}}{I_{out,load,avg} + I_{out,sup,avg}} = \frac{-6.6\,\mathrm{V} - (-6.175\,\mathrm{V})}{-6\,\mathrm{mA} + (-385\,\mu\mathrm{A})} = 66.6\,\Omega \quad (5.3)$$

This result shows that the previously defined output resistance fits the simulated resistance very well. With the shown approach the charge pump's behaviour in terms of output voltage can be determined with little effort, by achieving good estimates. However in this section only the total on-resistance of the switches was set, without any information on the individual switch sizes, showing that only the total on-resistance is important for determining the output resistance. Nevertheless the sizing of the switches is discussed in section 5.2.

5.2 Area Consumption and Optimisation

For the previous simulation the behaviour of the circuit was shown for a given fast switching limit resistance. However the question remains how the switches should be sized each. This section discusses two different design approaches: In Design 1 all switches are set to be approximately equal in terms of on-resistance. Design 2 will focus on minimising the number of unit transistors used and therefore also minimising the area. Both designs

are set to be equal in output voltage and on-resistance and are compared in terms of area consumption.

The sum of all unit transistors is denoted as N, whereas n_1 to n_7 represents the number of unit transistors used for each switch.

$$N = n_1 + n_2 + n_3 + n_4 + n_5 + n_6 + n_7 \tag{5.4}$$

5.2.1 Design 1

The first design approach is based on sizing the switches in a way that all on-resistances are equal. Assuming an amount of $n_1 = n_3 = n_4 = n_{NMOS}$ unit transistors for a single NMOS transistor, also the other amounts can be calculated accordingly. For the single PMOS transistor a factor of about 2.5 can be assumed leading to $n_2 = n_{PMOS} = 2.5 \cdot n_{NMOS}$. For the switches where two transistors are used in series these values need to be quadrupled compared to using a single transistor, giving: $n_5 = n_6 = 4 \cdot n_{PMOS}$ and $n_7 = 4 \cdot n_{NMOS}$.

Determinded from simulation, a value of about $n_{NMOS} = 39$ fits best in order to reach a fast switching limit resistance of about $46\,\Omega$. The used values are shown in table 5.1, these slightly differ from the calculations as the goal was to set the respective on-resistances as equal as possible.

5.2.2 Design 2

In Design 1 the switches one to seven were designed to be approximately equal in terms of on-resistance. However this does not have to be the best design approach. This section presents a way to optimise the switches in terms of area resulting in the same fast switching limit resistance and therefore the same performance.

The approach is based on finding the minimum of a multidimensional cost function. In this case the resulting area, respectively the total amount of

unit size transistors can be directly used as cost function which has to be as small as possible.

$$A = A_{unit} \cdot N \tag{5.5}$$

However it is important to distinguish the number of unit transistors $\boldsymbol{n} = \begin{pmatrix} n_1 & n_2 & \cdots & n_7 \end{pmatrix}^T$ and the actual equivalent number of unit transistors for resistance calculation $\boldsymbol{x} = \begin{pmatrix} x_1 & x_2 & \cdots & x_7 \end{pmatrix}^T$. Therefore the vector $\boldsymbol{w} = \begin{pmatrix} w_1 & w_2 & \cdots & w_7 \end{pmatrix}^T$ is introduced for weighting $\boldsymbol{x}$. In this way $\boldsymbol{n}$ can be expressed by the Hadamard product as $\boldsymbol{n} = \boldsymbol{w} \circ \boldsymbol{x}$. To give an example, for switch one only one transistor is used which leads to $n_1 = x_1$. Switch five needs two transistors in series. In order to get the equivalent resistance for using a single transistor the number of unit transistors has to be quadrupled, therefore leading to $n_5 = 4 \cdot x_5$. N can therefore also be expressed with respect to $\boldsymbol{x}$ as in equation 5.6.

$$N(\boldsymbol{x}) = w_1 \cdot x_1 + w_2 \cdot x_2 + w_3 \cdot x_3 + w_4 \cdot x_4 + w_5 \cdot x_5 + w_6 \cdot x_6 + w_7 \cdot x_7 \tag{5.6}$$

Nevertheless there is one constraint that has to be considered. This is the given, respectively wanted fast switching limit resistance. It can be expressed by equation 5.7, whereas $\boldsymbol{x}$ is the equivalent number of transistors for assuming using a single transistor, $\boldsymbol{R_{unit}}$ represents the resistance of a unit transistor. $\boldsymbol{R_{unit}}$ mainly depends on the used type of transistor (NMOS or PMOS).

$$\frac{R_{FSL}}{2} = \frac{R_{unit,1}}{x_1} + \frac{R_{unit,2}}{x_2} + \frac{R_{unit,3}}{x_3} + \frac{R_{unit,4}}{x_4} + \frac{R_{unit,5}}{x_5} + \frac{R_{unit,6}}{x_6} + \frac{R_{unit,7}}{x_7} \tag{5.7}$$

Rearranging equation 5.7 by x_7 and inserting it into equation 5.6 gives the final cost function (equation 5.8) that has to be minimised. For reasons of distinguishability $x_{1,\cdots,6}$ will be denoted as $\boldsymbol{\theta}$.

$$
\begin{aligned}
N(\boldsymbol{\theta}) &= w_1 \cdot \theta_1 + w_2 \cdot \theta_2 + w_3 \cdot \theta_3 + w_4 \cdot \theta_4 + w_5 \cdot \theta_5 + w_6 \cdot \theta_6 + \\
&+ w_7 \cdot \left(\frac{R_{unit,7}}{\frac{R_{FSL}}{2} - \frac{R_{unit,1}}{\theta_1} - \frac{R_{unit,2}}{\theta_2} - \frac{R_{unit,3}}{\theta_3} - \frac{R_{unit,4}}{\theta_4} - \frac{R_{unit,5}}{\theta_5} - \frac{R_{unit,6}}{\theta_6}} \right) = \\
&= \boldsymbol{w}_{1,\cdots,6}^T \cdot \boldsymbol{\theta} + w_7 \cdot \left(\frac{R_{unit,7}}{\frac{R_{FSL}}{2} - \sum_{i=1}^{6} \frac{R_{unit,i}}{\theta_i}} \right)
\end{aligned}
\tag{5.8}
$$

For finding the minimum of $N(\boldsymbol{\theta})$ an algorithm for gradient descent is used. First a starting vector $\boldsymbol{\theta}^{(0)}$ is initialised. In every iteration each θ_j can then be updated as described in equation 5.9 by descending on the negative gradient. The factor η is the learning rate and needs to specified accordingly [24].

$$
\theta_j := \theta_j - \eta \cdot \frac{\partial N(\boldsymbol{\theta})}{\partial \theta_j} = \theta_j - \eta \cdot \left(w_j - w_7 \cdot \left(\frac{R_{unit,j} \cdot R_{unit,7}}{\theta_j^2 \left(\frac{R_{FSL}}{2} - \sum_{i=1}^{6} \frac{R_{unit,i}}{\theta_i} \right)^2} \right) \right)
\tag{5.9}
$$

The algorithm is stopped when the change from one iteration to the other is smaller than a specified ϵ.

In order to compare results with the previous dimensioning (all transistors with same resistances), the same fast switching limit resistance is set as constraint ($R_{\mathrm{FSL}} = 46\,\Omega$). The unit size transistor on-resistances are set according to the device type and are determined beforehand by simulation ($R_{N,unit} = 127\,\Omega$ and $R_{P,unit} = 326\,\Omega$), with maximum gate-source voltage and $V_{\mathrm{DS}} = 10\,\mathrm{mV}$.

$$
\boldsymbol{R_{unit}} = \begin{pmatrix} R_{N,unit} & R_{P,unit} & R_{N,unit} & R_{N,unit} & R_{P,unit} & R_{P,unit} & R_{N,unit} \end{pmatrix}^T
\tag{5.10}
$$

The weighting vector $\boldsymbol{w}$ has a factor of 1 for single transistors and 4 for two transistors in series. As already explained above, the area consumption increases quadratically for connections in series.

$$\boldsymbol{w} = \begin{pmatrix} 1 & 1 & 1 & 1 & 4 & 4 & 4 \end{pmatrix}^T \tag{5.11}$$

From the resulting $\boldsymbol{\theta} = \begin{pmatrix} 71.9 & 114.8 & 71.9 & 71.9 & 57.6 & 57.6 \end{pmatrix}^T$ the number of unit transistors can be determined. By using equation 5.7 the remaining $n_7 = 35.9$ can be calculated. All values have to be rounded up to the next integer values. It is visible that between the NMOS and the PMOS topologies there is always a ratio of about 1.6. Furthermore the ratio between the switches containing one device and the switches containing two devices in series is a factor of one half.

Table 5.1 compares the results for using the two different design approaches. Design 1 concentrates on using equal on-resistances, whereas design 2 uses the optimum number of unit transistors in terms of area. The postfixes c and m indicate whether the values were calculated (c) or measured (m). Additionally the total resistance (for calculated and measured values) and the total amount of unit transistors N are shown.

In general the fast switching limit resistance is nearly equal, however the second design uses about 19.3 % less unit transistors and therefore less area.

The given and calculated values from table 5.1 are valid for a fast switching limit resistance of about 46 Ω and a switching frequency of about 2 MHz. However the ratio between the different switches should remain the same even for different values of fast switching limit resistance. Of course this is only valid supposing the topology (used switch devices) remains the same.

5.2.3 Charging Losses

However in the previous optimisation charging losses on the gate capacitances are neglected, assuming that the switches are controlled by ideal

General			Design 1				Design 2			
S	$R_{unit,i}$	w_i	x_i	n_i	$R_{ON,i,c}$	$R_{ON,i,m}$	x_i	n_i	$R_{ON,i,c}$	$R_{ON,i,m}$
i	Ω	–	–	–	Ω	Ω	–	–	Ω	Ω
1	127	1	39	39	3.26	3.25	72	72	1.76	1.76
2	326	1	99	99	3.29	3.30	115	115	2.83	2.84
3	127	1	39	39	3.26	3.16	72	72	1.76	1.71
4	127	1	39	39	3.26	3.21	72	72	1.76	1.73
5	326	4	99	396	3.29	3.30	58	232	5.62	5.65
6	326	4	99	396	3.29	3.42	58	232	5.62	5.83
7	127	4	39	156	3.26	3.20	36	144	3.53	3.47
$N \mid \frac{R_{FSL,c/m}}{2}$				**1164**	22.91	22.84		**939**	22.88	22.99
$V_{out,avg}$			−6.175 V				−6.164 V			

Table 5.1: Comparison of the two different design approaches. Design 1 was designed to have all switches sized equally in terms of on-resistance, whereas design 2 is minimising the number of transistors respectively the area.

sources. To give an example: optimisation suggested to choose the switches five and six equal in terms of on-resistance and area. On the one side switch five is supplied and controlled by the positive voltage domain. On the other side switch six needs to be controlled by negative domain. The charging loss is basically the same for both switches, as they are equal in size, but one time energy comes from the supply, whereas the other time energy comes from the output capacitance.

Nevertheless with the shown approach this fact can also be considered by adjusting the weights in the cost function (equation 5.6) accordingly. By increasing the weight of one switch the number of unit transistors for this switch is punished more and therefore likely to decrease. However this leads to the other switches getting bigger.

5.3 Corner Simulations

In order to estimate the circuit's behaviour for different process corners and temperatures. Simulations were done for fast, slow process corners as well

		Temperature		
		−50 °C	27 °C	125 °C
corner	**slow**	−6.20 V	−6.15 V	−6.07 V
	nominal	−6.21 V	−6.17 V	−6.11 V
	fast	−6.21 V	−6.18 V	−6.14 V

Table 5.2: Comparison of the resulting output voltages for different temperature and process corners and nominal values.

as for the minimum and maximum operating temperatures of −50 °C and 125 °C. Table 5.2 shows the resulting output voltages in comparison to the nominal values.

The maximum deviation from the nominal values occurs at slow process corner and a temperature of 125°. The deviation is in a range of about 100 mV respectively 1.6 %.

5.4 Ripple on Output and Flying Capacitances

The ripple on the output of the SC DC-DC converter is mainly defined by the effective output capacitance and does not depend on the charge pump topology. An estimation for the ripple of the output is made in equation 5.12, where only the output current in the series phase of the charge pump is considered. This leads to a maximum voltage difference ΔV of about 1.5 mV. Nevertheless the simulations in Figure 5.1 show a ripple of about 2 mV. This comes from the fact that even in parallel phase the output current is present, whereas the flying capacitances are able to charge the output capacitance first, but afterwards the discharging by the load current is dominating.

$$\Delta V = \frac{\Delta Q}{C} = \frac{I_{out} \cdot \frac{1}{2 \cdot f_{\mathrm{SW}}}}{C} = \frac{6.375\,\mathrm{mA} \cdot \frac{1}{2 \cdot 2\,\mathrm{MHz}}}{1\,\mu\mathrm{F}} = 1.5\,\mathrm{mV} \tag{5.12}$$

Figure 5.1 shows the voltage on the output and on the flying capacitances for the already started-up circuit. Subfigure 5.1a shows the voltages for Design 1, where all switches are equal in resistance. It is visible that both

flying capacitances are charged equally, as also the resulting simplified RC networks are equal in capacitance and resistance values.

Subfigure 5.1b shows the simulation of Design 2 which is optimised in area. Obviously in this case the second flying capacitance is charged less compared to the other, as also the corresponding switches' resistance is greater in value. Nevertheless this is compensated by smaller switch resistances and therefore better behaviour of the first flying capacitance.

5.5 Simulation with Bond Wire and External Parasitics

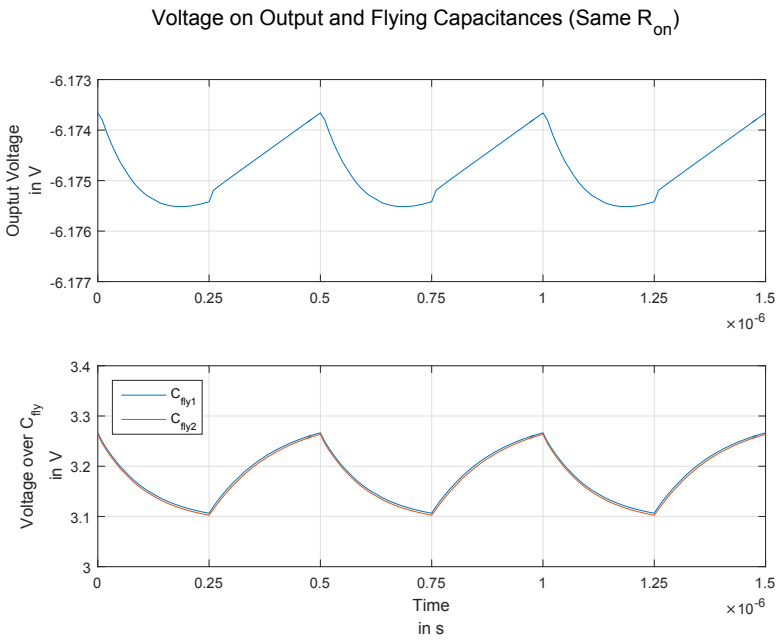
The previous simulations were done for the assumption of having no parasitics coming from the external capacitances. However this is not true in fact. Therefore simulations are made with the circuits from section 4.5.2, that should model the bond wires.

From simulation with the given parasitic model an average output voltage of about $-6.193\,\mathrm{V}$ is reached. It is important to note that for this simulation Design 2 with the same dimensioning was used. However a better behaviour is reached than without any parasitics. In this case two effects come into account.

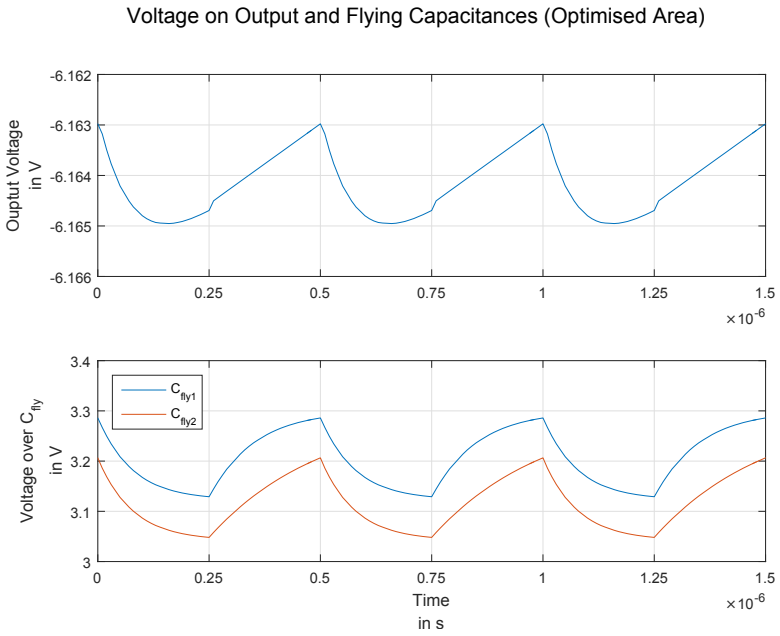
5.5.1 Linear Charging of Capacitance

The first effect comes into account when applying the voltage step for charging the capacitance. When using a voltage step half of the energy is lost during charging of the capacitance, also leading to a high peak current at the start of the voltage pulse. If a current source is used the losses can be neglected. In this case the voltage on the capacitance is increasing linearly and not exponentially.

The added parasitic inductance can also be seen to be similar to a current source, leading to a more linear charging of the capacitance and therefore



(a) Voltage ripple on output and flying capacitances for Design 1, with same on-resistances.



(b) Voltage ripple on output and flying capacitances for Design 2, with optimised area.

Figure 5.1: Voltage ripple on output and flying capacitances for both discussed designs.

having less energy losses. This could also be approximated by a stepwise voltage increase as this is proposed in [25].

5.5.2 Resonant Switched Capacitor Converter

The second effect is based on the fact, that when charging the capacitance the parasitic inductance stores energy, leading to a small overshoot in voltage over the capacitance.

Figure 5.2 shows results of a simplification of the given topology. In this case an RC circuit and and RLC circuit are simulated, whereas the values for R and C are equal in both cases. Solving both resulting differential equations (RC: first order, RLC: second order) with all initial conditions set to zero it is visible, that in the beginning the voltage over the capacitance is higher for the RC topology, but after some time the voltage in the RLC topology is higher. This comes from the fact that the inductance tries to keep the current the same, therefore charging the capacitances faster after some time.

Therefore better results are achieved by using parasitic models containing inductances in this case. However this may not hold true all the time. As it is visible in Figure 5.2 this is only the case if the period is sufficiently high, meaning that a higher switching frequency may decrease this effect. Furthermore for different inductance values the charging also differs. A more detailed explanation can be found in [26].

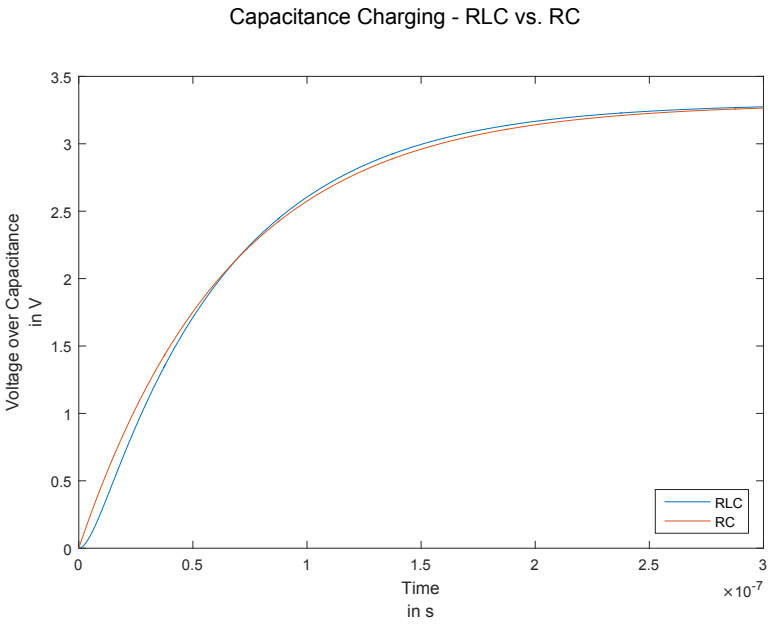


Figure 5.2: Comparison of charging C by RC and RLC topology.

6 Conclusion

To conclude, this thesis described the development of an SC DC-DC converter from concept to verification.

Conceptually the topology (section 3.1), phases (section 3.2), performance limits (section 3.3) and external device (section 3.4) influence was discussed and considered. This basically led to a series-parallel converter having four phases, seven switches and two flying capacitances. The impact of slow switching limit and fast switching limit was investigated as well.

In design the actual implementation of all switches using CMOS devices was explained. However some due to the creating of voltages below substrate, triple-well NMOS devices had to be used. Some switches were rather trivial to implement (Switch One (S1), Switch Two (S2) and Switch Five (S5)), whereas others used an approach of using voltages that are available in the respective phases (Switch Three (S3) and Switch Four (S4)) and yet others needed additional blocks such as levelshifters (section 4.4) and voltage dividers (section 4.3) (Switch Six (S6) and Switch Seven (S7)).

In verification the conceptual calculations and expectations were compared to the simulation results. Furthermore an optimisation method in terms of area (section 5.2) was proposed that saved about 19 % of area compared to a standard approach, while maintaining same performance. Additionally the influence of process and temperature corners (section 5.3) was examined and also external parasitics (section 5.5) were included in the simulations.

In summary, it can be stated that with the shown approaches in this thesis, the performance of the SC DC-DC converter that was defined in conceptual phase was estimated quite accurate. The simulated results met the calculations very well. In addition also area consumption was minimised. Generally, the same concepts that were described, can also be applied to

other SC DC-DC converters with different topology and different specifications.

Appendix

List of Figures

List of Figures

List of Tables

Acronyms

BCD Bipolar-CMOS-DMOS. iv, v, 2

C capacitance. 2, 8, 9, 13–34, 37, 39–41, 43, 46, 48, 50, 51, 54–59, 63–70, 73–76
CMOS complementary metal-oxide-semiconductor. iv, v, 2, 11, 35, 70, 76, 80
C_{avg} average effective capacitance. 30–33
C_D dynamic capacitance. 15–17, 29–32, 54, 55
C_{fly} flying capacitance. 2, 13, 26, 27, 30–33, 37, 39–41, 43, 46, 48, 56–59, 66, 67, 70, 74, 75
C_{GS} gate-source capacitance. 14
C_{out} output capacitance. 26, 30, 32, 48, 75
C_S static capacitance. 15–17, 54

DC direct current. iv, v, 1, 3, 4, 6, 16–19, 22, 25, 26, 29, 30, 32–34, 46, 54, 65, 70, 71, 73, 77, 79, 80
DeMOS drain-extended MOSFET. iv, v, 6, 7, 15, 45–48, 73, 74

E energy. 16, 17
ESD electrostatic discharge. 29, 45

f frequency. 32
FET field-effect-transistor. 4–7, 14, 15, 45, 76, 77, 81
FSL fast switching limit. 9–11, 22, 24–28, 30, 32, 58–64, 70, 73, 77
f_{sw} switching frequency. 2, 8, 10, 22, 24–28, 30–32, 58, 59, 63, 65, 68, 73

GND ground. 19

I current. 17, 25, 32, 76
IC integrated circuit. 1, 2, 29, 57
I_{out} output current. 32

LDD lightly-doped drain. 7

MOS metal-oxide-semiconductor. iv, v, 2, 4–7, 11, 14, 15, 35, 45, 70, 76, 77, 80, 81
MOSFET metal-oxide-semiconductor field-effect-transistor. 4–7, 14, 15, 45, 76, 77, 81

NMOS n-channel MOSFET. iv, v, 4, 6, 7, 11, 12, 14, 37–41, 43, 46, 48, 51, 60, 61, 63, 70, 73

OPAMP operational amplifier. 13

PCB printed circuit board. 56, 57, 74
PMOS p-channel MOSFET. 6, 7, 11, 38–41, 43, 45–48, 51, 60, 61, 63, 74
PWL piecewise linear. 54, 55, 74

Q charge. 15–17, 23–26, 29, 54, 65

R resistance. 22–27, 30–34, 51, 55, 58–64, 73, 77
$\mathbf{R_{FSL}}$ fast switching limit resistance. 26, 58–64
$\mathbf{R_{load}}$ load resistance. 31, 32
$\mathbf{R_{ON}}$ on-resistance. 2, 6, 8, 9, 14, 18, 22, 24–28, 45–47, 59, 60, 62–64, 67, 74, 75
$\mathbf{R_{out}}$ output resistance. 31–34, 73
RS-flip-flop reset-set flip-flop. 35, 36, 73
$\mathbf{R_{SSL}}$ slow switching limit resistance. 24, 26, 31–34, 58

SC Switched-Capacitor. iv, v, 1–4, 6, 7, 18–20, 22, 25, 26, 32, 35, 38, 65, 70, 71, 73, 77, 79, 80
SC DC-DC Switched-Capacitor DC-DC. iv, v, 1, 3, 4, 6, 18, 19, 22, 25, 26, 32, 65, 70, 71, 73, 80
SOA save operating area. 6, 13, 14, 20, 37, 41, 45, 50, 51
SPICE simulation program with integrated circuit emphasis. 54–56, 74
SSL slow switching limit. 8–11, 17, 18, 22–28, 30–34, 58, 70, 73, 77

t time. 17

V voltage. 1, 3–6, 13, 15–21, 25–27, 29–34, 37–41, 43, 46, 48–52, 54, 65, 66, 74, 75, 78
$\mathbf{V_{BS}}$ bulk-source voltage. 11

V_{DD} positive supply voltage. 1, 3–6, 13, 15, 18–21, 30, 32, 33, 37–41, 43, 46, 48–52, 74
V_{DS} drain-source voltage. 6, 37, 45, 62
V_{GS} gate-source voltage. 6, 41, 43, 45, 49–51, 62
V_{in} input voltage. 26
V_{out} output voltage. 26, 31, 32
V_{SS} negative supply voltage. 13, 14, 21, 37–40, 43, 46, 48, 51
V_{TH} threshold voltage. 11, 43, 50

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