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Integrated Filterless Class-D Audio Amplifiers

Investigations on Circuit Design, Electromagnetic Compatibility and Power Efficiency

DISSERTATION

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Contents

Frequently used terms

Terms and abbreviations frequently used throughout this thesis are explained below. The terms are sorted according to their first occurrence.

Term	Explanation
Class-AD	Topology of fully differential Class-D amplifiers, which need dedicated output filtering. Adjective: AD-modulated;
Class-BD	Commonly used topology of filterless Class-D amplifiers. Adjective: BD-modulated;
THD+N	Total harmonic distortion and noise (chapter 2.2.1)
PSRR	Power supply rejection ratio (chapter 2.2.1)
Rated Power	Output power, at which THD+N increases above 10 %.
PWM	Pulse width modulator (chapter 2.2.2)
D	Duty-cycle of a rectangular signal. $D = t_{high}/T_{PWM}$ with signal period T_{PWM} and on-time t_{high}.
f_r	Fundamental frequency of the PWM reference signal. Determines the switching rate of the power-stage. $f_r = 1/T_{PWM}$
DAC	Digital to analog converter.
ADC	Analog to digital converter.
$\Delta\Sigma$	The Delta-Sigma principle of oversampling and noise-shaping, as used in $\Delta\Sigma$ converters.
H	Symbol frequently used relating to the loop-filter in a negative feedback system.
IC	Integrated circuit.
CMOS	Complementary metal oxide semiconductor: Technology to implement ICs using P-channel and N-channel metal oxide semiconductor field effect transistors (MOSFET).
DMOS	Double-diffused MOSFET.
PCB	Printed circuit board.

Term	Explanation
R_{on}	Channel resistance of a MOSFET operated in the linear region.
V_{DD}	Positive supply voltage.
EMI	Electromagnetic interference: Disturbance in an electronic device due to electromagnetic emission.
Slew-rate	The change of voltage dV/dt.
t_{rise}	The rise time needed by a trapezoidal signal to transition from the low level to the high level.
DM	Differential mode signal. In the case of voltage the abbreviation V_{DM} is used.
CM	Common mode signal. In the case of voltage the abbreviation V_{CM} is used.
Speaker	Loudspeaker, an electroacoustic transducer. In this work only electrodynamic loudspeakers are considered.
150 Ω method	150 Ω direct coupling method. A setup for conducted emission measurement at IC level defined in IEC61967-4.
IF	Intermediate frequency used in superheterodyne receivers.
SSM	Spread-spectrum modulation: A method of spectral shaping to reduce EMI.
Δf	Peak frequency deviation of a carrier when using SSM.
f_m	Modulation frequency of a periodic SSM. Also repetition rate of the modulation profile.
LFSR	Linear feedback shift register. In this work only LFSRs that create a maximum length sequence are used.
FSR	Full scale range: Maximum amplitude a digital system can represent.

1. Motivation and background of this work

Class-D amplifiers are well known for their high power efficiency. In the 1960s companies such as Sinclair Radionics introduced Class-D amplifiers for audio power amplification [1]. In those days, cooling requirements at peak power determined the system costs. The Class-D topology offered an ideal possibility to reduce losses and generated heat. At first, customers felt critical towards the new technology. But within the last decades, Class-D amplifiers have become a standard topology for audio power amplification. They are used in a variety of applications, ranging from home entertainment systems, automotive audio, to professional sound equipment.

More recently, mobile audio equipment has become very popular. Devices such as tablets, smart-phones and notebooks try to offer excellent listening experience to the costumer. However, these devices are constrained by a limited energy storage. Again, Class-D amplifiers have become a versatile solution for audio amplification in these devices, due to their high power efficiency.

However, the Class-D amplifiers used in mobile devices show significant differences to the previously used amplifiers. Class-Ds were traditionally used in applications with higher output power. In many mobile devices, often output power below 1 W is needed. Due to space requirements, traditional Class-D amplifiers with inductor based output filtering cannot be used. Instead so-called filterless amplifiers have been developed which are typically integrated on a small silicon die.

When decreasing the output power, small parasitic effects become more important. Efficiency measurement setups such as described in [2, 3, 4, 5, 6], which have been used for the traditional high-power Class-D amplifiers, introduce significant errors when measuring low-power amplifiers for mobile devices. Therefore chapter 3.1 of this thesis shows a modified

efficiency measurement setup for low-power Class-D amplifiers. Additionally, not only the power efficiency at peak power is important. In [7] it is shown that audio amplifiers are operated at less then 10 % of their nominal output power for most of the time. To maximize battery lifetime, the efficiency over the whole output range is of concern. To optimize the power efficiency, a comprehensive analysis of the created losses is needed. Previously published loss analyses such as [8, 9, 10, 11] are targeted towards high-power amplifiers with inductive output filtering. They cannot be directly applied to low-power, filterless amplifiers. In chapter 3.3, these previously published loss analyses are combined and adapted for filterless amplifiers. The result is an efficiency model which can help to create an optimal filterless power-stage design.

Mobile devices become increasingly complex. The functional integrity of all sub-subsystems and their electromagnetic interaction is of significant importance for customer satisfaction. Moreover, the electromagnetic compliance of an electronic system to legal emission limits such as FCC or European Union regulations is required to bring a product to the market. Unfortunately, as will be shown in chapter 4.1, Class-D amplifiers are a major source of electromagnetic emission due to their switching power-stage. In previous works and datasheets of integrated Class-D amplifiers, several different emission measurement setups are used. Conducted measurements [12, 13, 14] and radiated measurements [15, 16, 17, 18] according to system-level standards can be found. Some works also show measurement results of non-standardized setups [19, 20, 21]. None of these measurement setups allows a fair comparison of different integrated amplifiers. The results obtained by setups based on system-level standards heavily depend on the used circuit board, board components, device housing and other factors. The non-standardized setups are often ill-defined and will not lead to repeatable results. Moreover, electromagnetic emission need to be considered already during design of integrated Class-D amplifiers, to avoid design iterations. Simulation tools are needed to predict emission measurement results before production of the microchip. The system-level measurement setups are difficult to model for simulation and often require 3-D simulation. This is not compatible with the standard design flow of integrated circuits. In chapter 4.2 a new measurement setup for Class-D amplifiers at IC-level is proposed. It is based on IEC61967-4 and allows an easy measurement setup, repeatable results, and is ideally suited to compare different Class-D ICs. It is shown how the setup can be modeled for simulation. The modeling approach is based on related work [22, 23,

24], but features a sophisticated post-processing algorithm. This approach is compatible with the standard design flow of integrated circuits. Thanks to the post processing, the simulation results can be directly compared to measurements with standard-compliant measurement equipment.

The stringent space requirements in mobile devices demand for amplifiers with minimum external component count. Especially, commonly used external measures to reduce electromagnetic emission are no longer accepted. Therefore new circuit-level measures are needed, to reduce or avoid the creation of these emission inside the integrated amplifier. So-called spread-spectrum modulation is extensively examined in chapter 5.1. Related research work [19, 20, 17, 13] has mainly focused on emission reduction using pseudo-random spread-spectrum modulation. In this work, also periodic spread-spectrum modulation is examined and it is compared to pseudo-random modulation. For the first time it is also shown that the method can be optimized for a certain verification setup. The implementation of the method to analog and digitally controlled Class-D amplifiers is demonstrated with several prototypes. In contrast to previous works, also the impact of this method on audio performance is investigated. Additionally, circuit level measures for the power-stage design are discussed, and a power stage with adaptive dead-time, adaptive driver strength and slew-rate control emission reduction is presented. The measurement setups and modeling approaches derived in chapter 3 and 4 have proven to be a prerequisite to investigate and develop these circuit level measures.

Ever shrinking technology complicates the design of highly linear analog Class-D amplifiers. An upcoming trend is to implement certain blocks of the amplifier with digital circuitry. Moreover, Class-D amplifiers have long been used for the power amplification of analog signals. In mobile devices, the signal sources typically have a digital nature. Digital-input Class-D amplifiers are thus needed. The first implementations consisted of a digital to analog converter and an analog input Class-D amplifier combined in one IC [25, 26]. More recent works perform digital to analog conversion and power amplification inside the same circuit. Unfortunately, the presented integrated implementations either cannot compete with the audio performance of high-fidelity analog amplifiers [27]; use high switching frequencies above 1 MHz [28] which compromises efficiency and increases electromagnetic emission problems; or rely on analog to digital converters with very demanding specifications [29]. Chapter 5.3 describes circuit blocks and system-level approaches to implement digitally

enhanced Class-D amplifiers.

This work is thus organized as follows: The Class-D amplifiers covered in this work are fully integrated audio amplifiers targeted towards mobile audio applications. They are designed for an input signal band of 20 Hz-20 kHz and are loaded with an electrodynamic loudspeaker. Typically, less than 10 W of output power is required. Chapter 2 introduces filterless Class-D amplifiers. The operation principle is explained and the basic building blocks are reviewed. It will be shown, that a good power-stage design is the key to developing a competitive Class-D amplifier. Consequently chapter 3 and 4 cover power efficiency and electromagnetic emission of filterless amplifiers, which are both largely determined by the power-stage. Finally, chapter 5 covers system and circuit level measures to reduce emission and add digital functionality to the amplifier.

2. Class-D amplifiers

In this chapter, the fundamental properties and operation principles of integrated filterless Class-D amplifiers will be reviewed. The basic terms and definitions necessary to understand this work will be defined and the background for the research presented in this work will be outlined.

2.1. Operation principle

In well-known Class-A or Class-AB amplifiers the amplifying devices (typically transistors) are operated in their linear gain region. Class-D amplifiers are switched mode amplifiers. In these amplifiers, the amplifying devices are operated as switches. This characteristic leads to very different linearity behavior, power-efficiency and spectral characteristics compared to linear amplifiers.

Generic Class-D amplifiers typically consist of two main building blocks as shown in Fig. 2.1. A first block, hereafter called modulator, processes the input signal. A second block, hereafter called power-stage, contains the switching devices driving the load. The modulator can be realized in several topologies, but its main objective is to encode the input signal into two-level control signals for the switches in the power-stage. These switches in the power stage either carry the load current in their ON state, or have very high resistance in their OFF state. In either case, the current-voltage overlap is very small. Thus, in the ideal case no losses are generated, leading to the very high power efficiency of Class-D amplifiers [30, 31]. In reality, several loss mechanisms are present in the power-stage as will be analyzed in chapter 3, reducing the efficiency. Still, efficiency is often higher than 90 % at full output power.

In contrast to linear amplifiers, the output signal not only contains the spectral content related to the input signal. Additionally, spectral content related to the operation of the switches is present. In many applications,

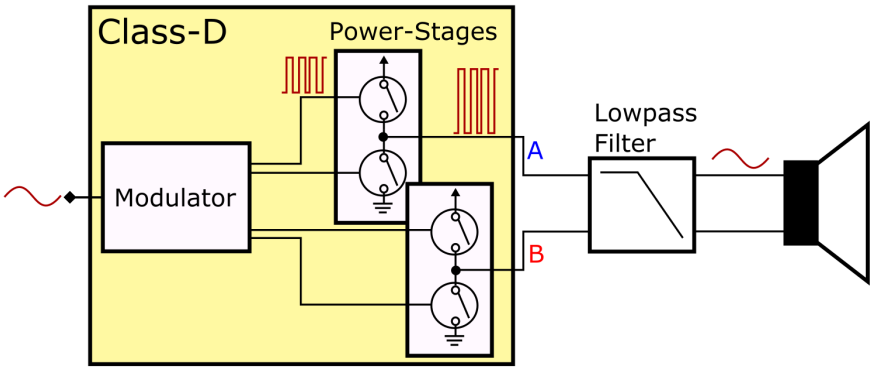


Figure 2.1.: Building blocks of a generic Class-D audio amplifier

Class-D amplifiers are therefore used as baseband amplifiers. They process only a band-limited low-frequency input signal. The switches in the power-stage are operated at a much higher rate. In this way the spectral content of the input signal and the additional content generated by the switching operation does not overlap in frequency domain. The amplified low-frequency input signal can be easily recovered using low-pass filtering as shown in Fig. 2.1. To achieve high efficiency, this filter should be practically lossless for the frequency band of interest.

Audio signals are inherently low-frequency band limited due to the hearing range of the human ear. The upper range of the human reception is generally agreed to be about 20 kHz [32]. Class-D amplifiers have thus become a widespread topology for audio-amplification. The main motivation to use Class-D amplifiers for audio amplification has always been power efficiency. The first audio Class-D amplifiers appeared in the early 1960s [1]. These early designs mainly targeted higher output power, were cooling requirements were a major cost factor. Nowadays, with the widespread use of mobile audio applications, battery lifetime has become the main driver to use Class-D amplifiers.

Early Class-D designs sometimes used a half-bridge power-stage. Thus one terminal of the speaker was connected to the amplifier, the other to a biasing voltage. In most modern Class-D amplifier designs, two power-stages are used, forming a full-bride stage, as shown in Fig. 2.1. In this case the amplifier has two outputs and the speaker is connected as a bridge-tied load between these outputs. Compared to a half-bridge power-stage, the voltage swing at the load is doubled for a given supply voltage. This

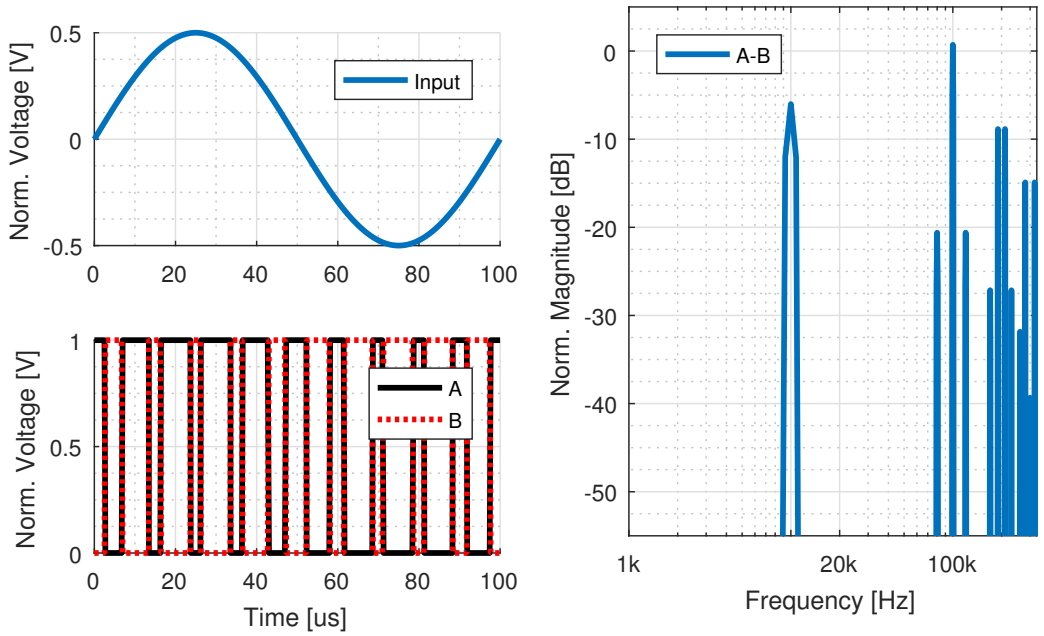


Figure 2.2.: Input and output waveforms of a Class-AD amplifier and according spectrum of the differential output voltage.

increases the possible output power by four.

Fig. 2.2 shows a plot of a Class-D amplifier's input and output voltage signals. The amplifier has a full-bridge power-stage where both sides of the load are driven and output filtering is used (Fig. 2.1). This is a typical configuration in many applications and often called Class-AD [33]. The shown amplifier is excited with a 10 kHz input signal and the modulator controls the power switches with a switching rate of 100 kHz. The according spectrum of the differential voltage at the output of the amplifier is shown in the right of Fig. 2.2. In the audible region, the output spectrum ideally consists of the amplified input signal. Above the audible region, the spectrum contains harmonics of the switching signals and intermodulation products with the input signal. The switches are operated at a frequency a decade above the audible region. Therefore, the generated spectral switching components do not fall into the audible region.

As shown in the block diagram of Fig. 2.1, the signal content above the audible region can be removed using a low-pass filter. Another reason to use a low-pass filter is power efficiency. As shown in Fig. 2.2, the output signal resembles a square-wave signal. Applying such a signal to an unknown load can result in large ripple current. The purpose of an output filter

is to average out the ripple current. The used filter should be practically lossless in the audible region for power efficiency. Traditionally, second order inductive-capacitive filters are used for this purpose [30, 31]. Such inductively filtered Class-AD amplifiers have become a commonly used solution for audio power amplification in home entertainment systems, automotive audio and similar fields.

Unfortunately, the low-pass filter has several disadvantages. The resonance behavior of the inductive-capacitive filter is strongly influenced by the used speaker. Non-linearity of the filter will distort the amplified signals. To avoid excessive distortion, the inductor's saturation current rating has to exceed the maximum load current. This leads to large and expensive inductors. These inductors need a lot of circuit board space and increases the costs. For cost-driven, space constrained electronic applications, such inductive filtering is not applicable.

2.2. Filterless Class-D amplifiers

By considering the characteristics of the applied load, so called filterless Class-D amplifiers have been developed. The electrodynamic loudspeaker load is a complex electro-mechanical device. The electrical impedance is typically formed by several parallel and series resonances of the parasitic components in the speaker assembly [32]. Nevertheless, the impedance is dominated by two characteristics [32, 34, 35]: Across the audible region, the impedance is dominated by resistive behavior, above the audible region inductive behavior can be observed. Thus, the speaker shows a low-pass characteristic.

From a pure signal processing point of view, the low-pass filter is therefore not needed. The speaker represents a high impedance for signals above the audible region. It will not efficiently convert these signals into sound pressure. Moreover, the human ear would not hear these signals. Unfortunately, the inductance of the speaker is not sufficient to average out the square-wave voltage signal. Large ripple current would still flow through the speaker. To reduce the ripple current, modified Class-D topologies have been invented [36, 37]. These modified topologies do not need output filtering for proper operation and are frequently called *filterless Class-D* amplifiers. To my knowledge, the most widely used filterless topology is the so-called Class-BD [36] topology.

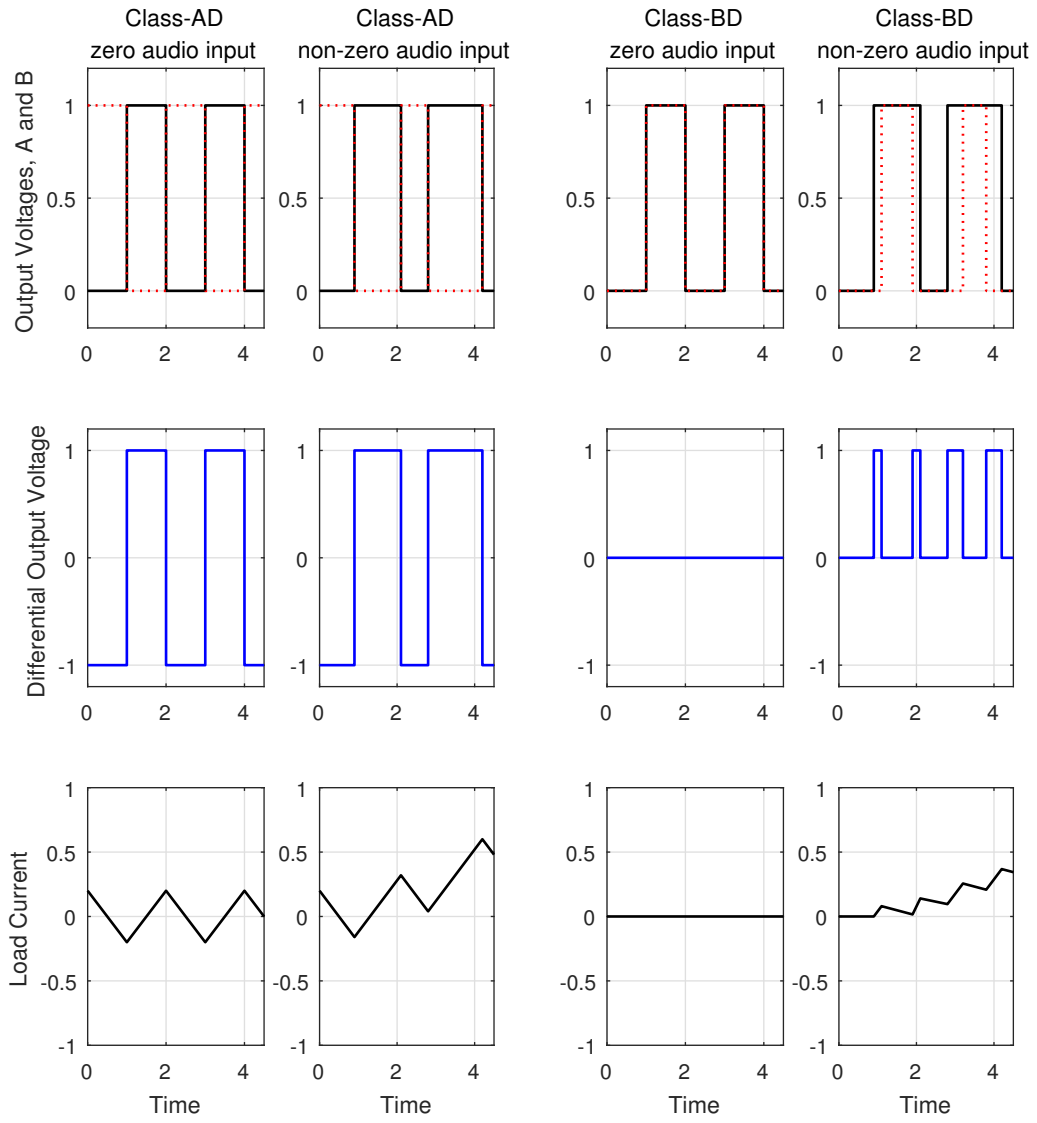


Figure 2.3.: Comparison of Class-AD and Class-BD waveforms. From top to bottom: output waveforms, differential voltage seen by the load and load current.

Fig. 2.3 illustrates the voltage waveforms for the traditional Class-AD and the filterless Class-BD scheme. The figure shows the two output signals, the according differential mode voltage driving the speaker and the resulting current in the speaker. In the Class-AD scheme, the two output channels are exactly 180° out of phase. Whereas in the filterless Class-BD scheme, the output signals are in phase, but the duty-cycle of the signals is different. The Class-BD scheme excites the speaker with a differential voltage only when needed, thereby significantly reducing the ripple current. As can be seen, the differential voltage in the Class-BD scheme is a tri-level signal (-1,0,1). Additionally, the differential voltage has a fundamental frequency twice the switching rate of each output channel, which further reduces ripple current.

Using the Class-BD switching scheme, high power efficiency can be achieved without chunky inductive filters. Thus, this topology is currently dominating the audio power amplification in the mobile market. Unfortunately, Class-D amplifiers can create electromagnetic emission, due to the switched-mode nature of the power-stage. These emission can lead to electromagnetic interference (EMI) in other circuits inside the same device or in other devices. In chapter 4 it will be shown, that filterless amplifiers are especially empowered to create EMI.

2.2.1. Performance measures for filterless amplifiers

Manufacturers of mobile devices use filterless Class-D amplifiers to provide good listening experience to the customer, without sacrificing battery lifetime. Power efficiency and audio performance measures are thus the most important performance criteria.

The listening experience of the audiophile end-customer depends on many factors concerning the complete audio-chain. Not only the electrical properties of the audio chain, but also factors such as the position of the speakers relative to the user, and psychoacoustic phenomena influence the listening experience [32]. Moreover, the human ear is very sensitive to identify periodic signals even when they are buried in noise floor. The repeated claim of enthusiasts and journalists, that measured electrical parameters do not necessarily correlate with the listening experience is thus not surprising. Nevertheless, manufacturers of amplifiers need performance measures to compare different amplifier topologies and to stand out

against competitors on the market. Ideally, these performance measures are standardized and can be expressed in hard numbers. IEC60268-3 [38] is the most widely accepted standard to characterize audio amplifiers. Additionally, several companies have worked out guidelines [2, 3, 4] that focus on measuring Class-D audio amplifiers. The reported measurement conditions and results shown in filterless Class-D datasheets [16, 26, 39] and scientific publications are typically based on IEC60268-3 and can be regarded as the de-facto industry standard.

In the following, the most important audio performance measures used in scientific publications and commercial datasheets are shortly explained. As the amplifier is the last electronic component before the speaker, the amplifier should ideally not generate any audible artefacts. This involves noise added by the amplifier, distortion caused by non-linarity in the amplification, as well as spectral components arising from the switching power-stage. *Total harmonic distorion plus noise (THD+N)* has undeniably become the most prominent audio performance figure in datasheets and scientific publications of Class-D amplifiers. THD+N is measured by applying a very pure sinusoidal input signal to the amplifier. First, the rms voltage V_S of the generated output signal is measured. Then, using a notch-filter [2, 40] the amplified input signal is removed from the measured signal, and the resulting rms voltage V_{HDN} is calculated. V_{HDN} contains harmonic components generated due to non-linearity, noise and possibly additional unwanted components. The industry standard bandwidth used for rms calculation is 20 kHz [16, 26, 39, 4]. The bandwidth is often [2, 39] realized by applying a low-pass filter according to the AES17 [41] standard. Finally THD+N is calculated as follows:

$$THD + N = \frac{V_{HDN}}{V_S} \qquad [\%\ or\ dB] \tag{2.1}$$

THD+N can be misleading as a single number. Thus, typically two graphs are shown in datasheets:
THD+N vs. Amplitude (or Output Power), shows THD+N at different input amplitudes. In this measurement the amplitude of the input signal is swept at a fixed frequency.
THD+N vs. Frequency, shows THD+N at different input frequencies. In this measurement the frequency of the input signal is swept at a fixed amplitude [41].
A sample measurement is shown in Fig. 2.4. On the left side, THD+N

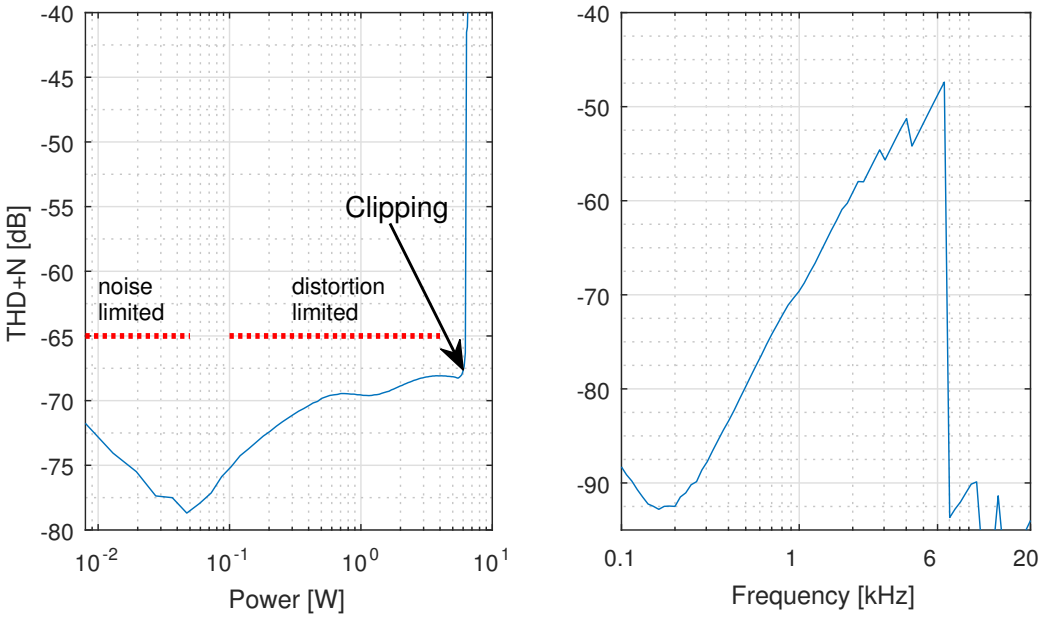


Figure 2.4.: THD+N measurement of a filterless Class-D amplifier. Left: THD+N vs. Output Power; Right: THD vs. Frequency

is measured for a 1 kHz input signal and the amplitude of the signal is swept. It can be seen that THD+N is limited by noise for low input amplitudes and limited by distortion for higher inputs. The clipping behavior of the amplifier can be observed clearly. On the right, THD+N is measured at a constant input signal amplitude. THD+N drops sharply, closely after 6 kHz. One can conclude from this behavior, that the amplifier is dominated by harmonic distortion of third order, which falls out of the measurement bandwidth (20 kHz) at this point.

Another frequently used audio performance measure is the output noise. It describes the output signal, when the input signal to the amplifier is reduced to zero [38]. Often output noise is measured with a weighting filter. Typically A-weighting is used as defined in IEC60268-1 [42].

Power supply perturbation should not couple to the output of the amplifier where it could distract the listener. Therefore, power-supply rejection is especially important for Class-D amplifiers operated in a noisy environment. The measurements are carried out by superimposing a small sinusoidal [43, 38, 4] signal on the supply voltage. For amplifiers targeted towards mobile devices, typically a 200 mV pp to 400 mV pp signal with a frequency of 217 Hz is used [27, 39, 44, 45, 18]. This signal resembles

the noise generated by GSM bursts in cell-phones. Two different cases are measured [46, 44, 43]. In the first case, the input signal to the amplifier is reduced to zero. Then the resulting output signal is measured. The *power supply rejection ratio* (PSRR, sometimes KSVR [4]) is calculated as ratio of supply ripple amplitude V_{SR} to output signal amplitude V_O:

$$PSRR = \frac{V_{SR}}{V_O} \qquad [dB] \tag{2.2}$$

Typical values for state of the art amplifiers are in the range of 70 dB to 100 dB [45].
In the second case, the measurement is repeated with a sinusoidal input signal applied to the amplifier. Due to non-linearity of the amplifier, intermodulation of the supply ripple and the input signal will occur. The measurement is typically carried out with a 1 kHz input signal [43, 44]. The output signal will then show intermodulation signals at 1 kHz$\pm$217 Hz. *PS-IMD to noise* gives the amplitude ratio of these intermodulation signals to the applied supply noise. *PS-IMD to signal* gives the amplitude ratio of the intermodulation signals to the 1 kHz output signal component. PS-IMD is a measure that depends on good power supply rejection and linearity of the amplifier.

The power efficiency does not directly affect the listening experience, but determines cooling requirements and energy consumption. It is a measure that shows how much of the power drawn from the supply is actually transferred to the speaker. Fig 2.5 shows the efficiency of two commercial audio amplifier ICs. The first amplifier is a Class-D [47], the second a Class-AB [48] amplifier. Both amplifiers, from the same manufacturer, are fully differential, operate at a supply voltage of 5 V, drive up to 1.2 W into a 8 Ω speaker, with a peak THD+N of about 0.02 %. The Class-D amplifier clearly shows better performance. It has a high power efficiency over a large output range. This is especially important, as audio signals have high dynamics. The average output power is often less than 10 % of the peak output power [7]. For mobile applications, where energy efficiency is important, the power efficiency at lower levels is therefore of special interest.

Unfortunately, measuring the power efficiency of integrated, filterless amplifiers for mobile applications is a cumbersome task. Efficiency measurements will be covered in detail in chapter 3.1. Another performance parameter, the rated output power can be derived from efficiency measure-

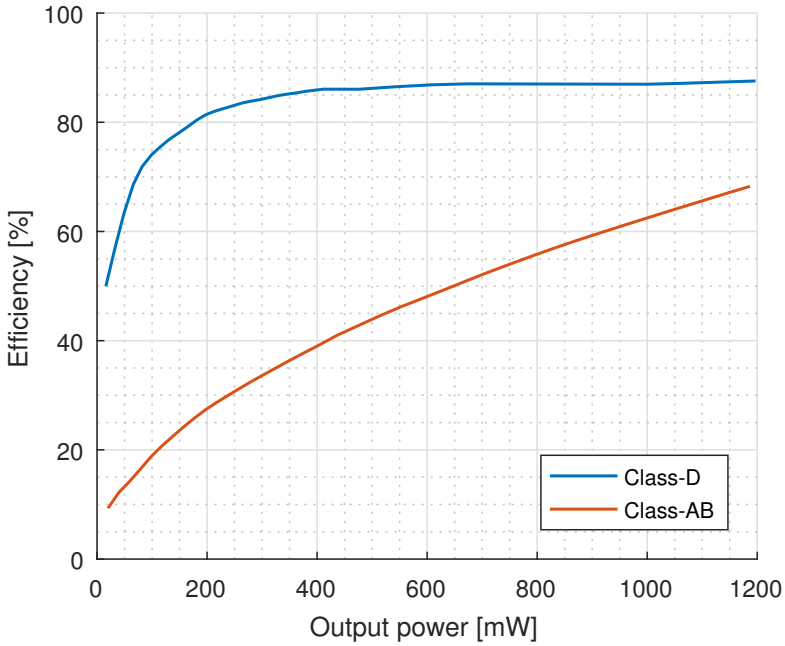


Figure 2.5.: Power efficiency of two 1.2 W audio amplifiers

ments. The rated power is a single figure. It states the output power when the amplifier starts clipping (e.g. THD+N increases above 1 or 10 %).

2.2.2. Modulator design

The modulator encodes the input signal into control-signals for the switching power-stage. The input signal can either be an analog or digital signal. Currently, the majority of Class-D amplifiers have an analog input. But digital input Class-D amplifiers are gaining increased interest.

Three main types of modulators can be identified, which all have different properties. In the following these types will be shortly analyzed, considering analog input modulators.

Pulse width modulators

Fig. 2.6 shows a simple pulse width modulator (PWM). The analog input signal $x(t)$ is compared to a reference signal $r(t)$ using a comparator. In this way, a rectangular output signal $y(t)$ is generated, which can be used

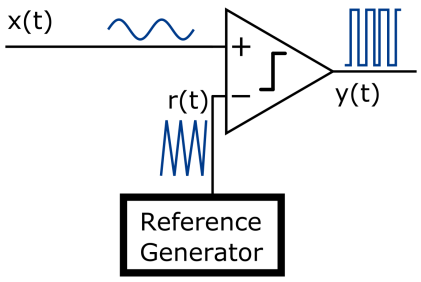


Figure 2.6.: Block diagram of a PWM modulator.

to control the power-stage. The rectangular output signal has a fixed fundamental frequency, but varying duty-cycle. The fundamental frequency of the rectangular signal is determined by the reference signal. The duty-cycle represents the instantaneous value of the analog input signal. The input information is thus encoded in the width of each rectangular pulse. For PWMs build in analog manner, the generated duty-cycle is an analog quantity. The rectangular output signal is therefore inherently analog, even though it only has two levels. In this way, the modulator can theoretically generate output signals with infinite resolution.

However, the input signal bandwidth is limited. In contrast to sampled data systems, the maximum input signal rate is not determined by the Nyquist criterion. For proper operation, the slew-rate of the input signal $x(t)$ must be smaller than the slew-rate of the reference signal $r(t)$ [49]:

$$\left|\frac{\partial\, x\,(t)}{\partial\, t}\right| < \left|\frac{\partial\, r\,(t)}{\partial\, t}\right| \tag{2.3}$$

An extensive review of different reference signals and the resulting spectral properties of the modulator can be found in [49]. In Class-D amplifiers, often triangular reference signals are used. The resulting output signal has been calculated in several works. Black [50] has calculated the output signal is for sinusoidal input signals, using double-fourier series. A more general analysis is presented by Song and Sarwate [51] for arbitrary signals. Given an input signal $x(t)$, and a triangular reference signal $r(t)$ with frequency f_r, the PWM generates an output signal $y(t)$ [51]:

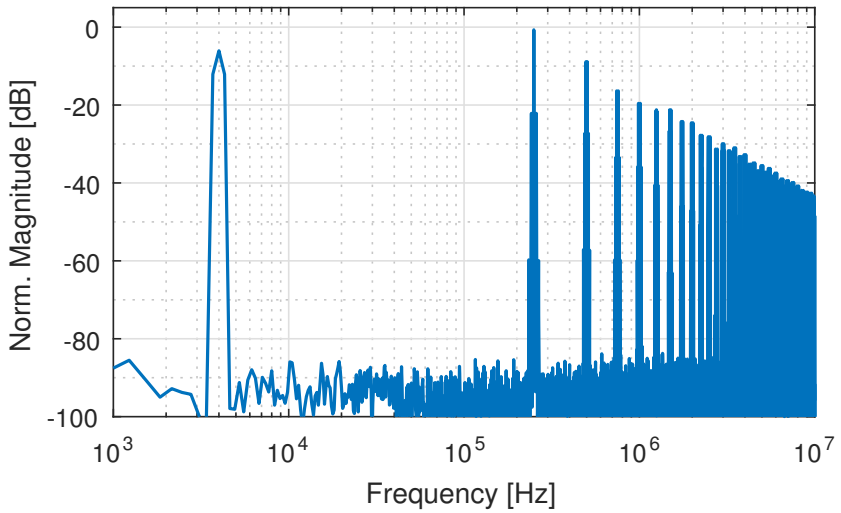


Figure 2.7.: Output spectrum of a PWM-based Class-D amplifier. The magnitude is normalized to the supply voltage level.

$$
\begin{aligned}
y(t) &= x(t) \\
&+ \sum_{k=1}^{\infty} \frac{2(-1)^k}{k\pi} \left[\sin\left(2\pi\, k\, f_r\, t + k\, \pi \frac{x(t)+1}{2}\right) \right. \\
&\left. - \sin\left(2\pi\, k\, f_r\, t - k\, \pi \frac{x(t)+1}{2}\right) \right]
\end{aligned}
\tag{2.4}
$$

The output signal $y(t)$ consists of the input signal $x(t)$. Additionally, harmonics of the rectangular carrier signal are present, each being phase modulated by the input signal. These carrier harmonics are unwanted in most applications. If the harmonics fall into the audible region, they will distract the listener. Therefore, the reference signal typically has a fundamental frequency of 100 kHz to 500 kHz. In this way, the harmonics and their sidebands (due to phase modulation) fall outside the audible region. The frequency of the reference signal also determines the switching rate of the power-stage. Higher switching rates increase the losses in the power stage, as will be explained in detail in chapter 3. Additionally, the energy of the carrier harmonics are concentrated around multiples of f_R and cause electromagnetic emission which can lead to EMI. EMI will be extensively covered in chapter 4.

Fig. 2.7 shows the output spectrum of a PWM-based Class-D amplifier

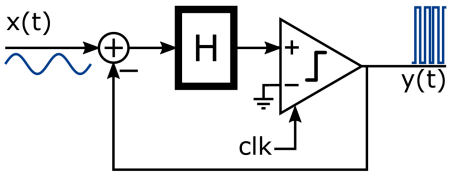


Figure 2.8.: Block diagram of a ΔΣ PDM modulator.

with a 4 kHz sinusoidal input signal. The reference signal has a frequency of 250 kHz. As predicted by eq. (2.4), the PWM is linear in the audible range. No harmonics of the input signal are generated and the modulator perfectly encodes the input signal. $THD + N$ is limited by the noisefloor. Thermal noise is inevitable in analog modulators and is the ultimate performance limit. In real modulators, non-linearity is introduced due to non-ideal circuit implementations. In practical circuits, linearity is affected by the reference signal [52]. A curvature in the reference signal slope leads to non-linear signal encoding. However, compared to the errors introduced in the power-stage, the effect is negligible in many practical circuits.

Pulse density modulators

Pulse density modulation (PDM) also encodes the input signal into a rectangular signal. In contrast to PWM, the input signal is represented by the average value over several output pulse periods. The principle is extensively used in ΔΣ modulators. ΔΣ PDM can be used in Class-D amplifiers to directly control the power-switches.

Fig 2.8 shows a generic block diagram of a ΔΣ modulator. The loop filter H can either be a continuous or discrete time filter. This loop filter integrates the difference between the input signal $x(t)$ and the rectangular output signal $y(t)$. The integrated difference is quantized by a clocked comparator. In filtered Class-D amplifiers two level comparators (1 bit) are used [30, 53]. Filterless Class-D amplifiers can represent three output levels, thus 1.5 bit modulators can be utilized [54, 55]. The well known design techniques [56] for ΔΣ modulators can be used to implement the modulator.

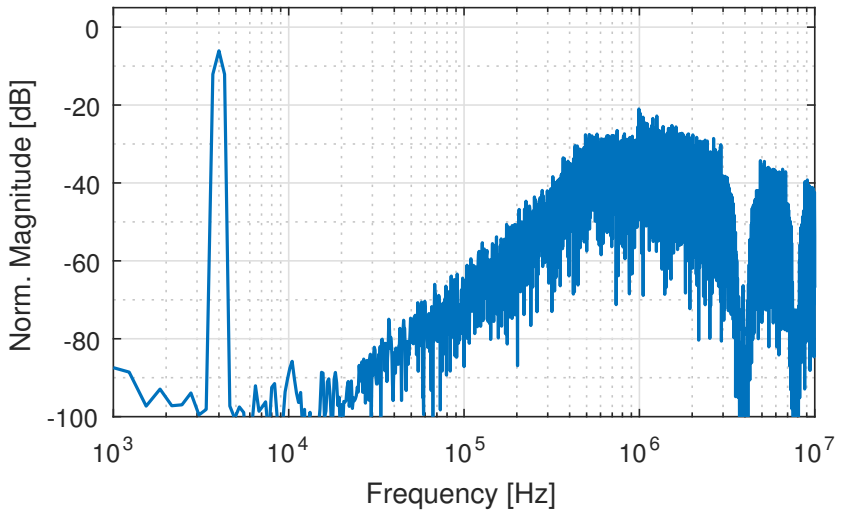


Figure 2.9.: Output spectrum of a PDM-based Class-D amplifier. The magnitude is normalized to the supply voltage level.

The output signal of PDM is quantized in value and time. It is thus a digital signal. Due to the digital nature of the output signal, the resolution is limited by quantization noise. Large oversampling ratios are needed to achieve good noise performance. The comparators in previously published works are thus clocked at rates of 1.2 MHz to 8 MHz [57, 54, 55, 53, 58]. This results in significantly higher switching rates of the power-stage compared to PWM. Modulators with 1.5 bit quantizer and techniques such as dynamic hysteresis in the comparator [59] have been utilized to reduce the switching rates. Still, switching rates with PDM are naturally higher than with PWM, for the same noise performance. PDM is thus inferior in terms of power efficiency.

PDM inherently needs feedback from the output signal $y(t)$. PDM therefore creates lower distortion, in contrast to PWM. This is because non-ideal circuit behavior is suppressed by the feedback. Unfortunately, PDM is generally not stable up to 100 % of the input signal range. The rated output power of PDM-based amplifiers is thus typically lower than with PWM.

Fig. 2.9 shows the output spectrum of PDM-based Class-D amplifier with a 4 kHz sinusoidal input signal. A second order loop-filter is used and the comparator is clocked at 3.9 MHz. The typical noise-shaped spectrum of $\Delta\Sigma$ modulation is clearly visible. In contrast to PWM, the switching rate of the power-stage is not constant. The switching harmonics cannot be clearly identified, but an average switching rate in the order of 1 MHz can

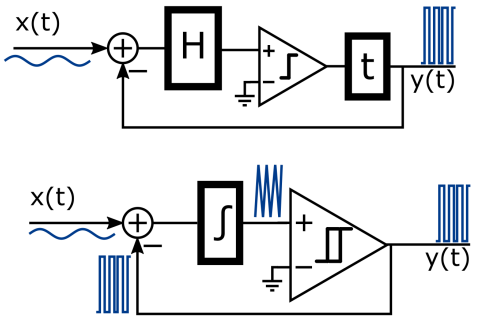


Figure 2.10.: Block diagram of self oscillating modulators.

be estimated.

Self oscillating modulators

Self oscillating modulators do not need a reference signal, nor a digital clock signal. Fig. 2.10 shows two possible realizations. Similar to PDM, self oscillating modulators inherently need feedback. Without input signal, the modulator oscillates, creating a rectangular output signal with 50 % duty-cycle. The 360° phase shift needed for oscillation is generated either by phase shift in the loop filter H and delay t in the forward path, or by using a hysteresis window in the comparator [60]. Applying an input signal to the modulator changes the duty-cycle and the frequency of the output signal. The duty-cycle of the output signal is modified to compensate the input signal within one oscillation cycle, leading to fast response to input signals. Non-linear control theory, such as sliding mode theory can be applied to analyze and design these circuits [61, 62]. Several published works have shown excellent performance figures [63, 64]. Moreover, these modulators can be implemented with very few circuit components allowing low cost and low power implementations [65, 66].

Unfortunately, these modulators have several disadvantages. The oscillation frequency is a function of the input signal amplitude. Fig. 2.11 shows the output spectrum of a self oscillating Class-D amplifier. As can be seen, the broadened harmonics of the switching signal indicate a non-constant switching rate. The oscillation frequency is typically [67, 68, 69] proportional to $1 - M^2$, where M is the modulation index (the ratio of instantaneous input signal amplitude to maximum signal amplitude).

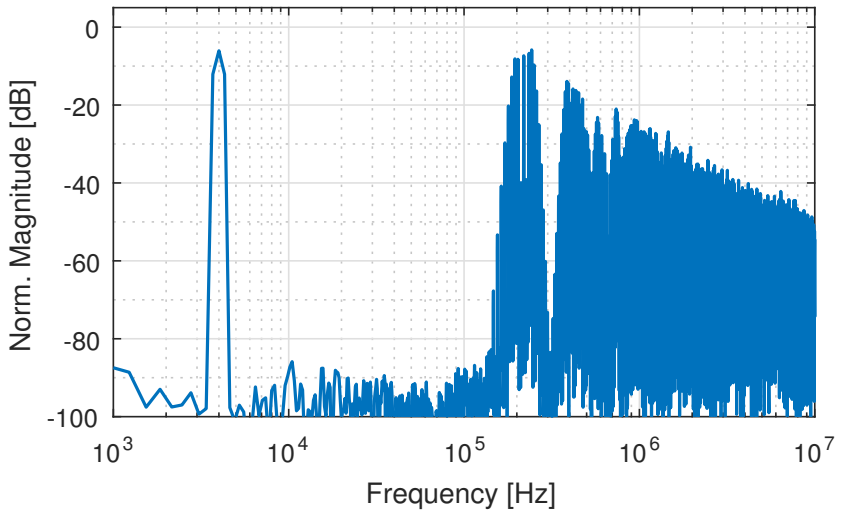


Figure 2.11.: Output spectrum of a self-oscillating Class-D amplifier. The magnitude is normalized to the supply voltage level.

The output signal frequency thus decreases with increasing input signal amplitude. For large input signals, the switching rate of the power-stage might fall into the audible range. For signals close to the maximum amplitude, oscillation can even stop. Several techniques have been invented to reduce the frequency variation. For hysteretic loops, variable hysteresis windows [70] or additional comparators in the feedback loop [71] can be used. For non-hysteretic loops, appropriate phase response of the loop filter can help to stabilize the frequency, as in [72, 69]. Some of these methods significantly add to the system complexity, and finally, none of the methods allows operation up to full-scale signal range.
The oscillation frequency also depends on parasitic delay in the feedback loop, supply voltage and other factors, which are difficult to control. This leads to difficulties in stereo applications. Two independent modulators will always have slightly different oscillation frequencies f_1 and f_2. Even small parasitic coupling can create beating tones in the modulator outputs at $f_1 \pm f_2$. Therefore, the self-oscillating frequencies of two nearby modulators have to be offset by at least 20 kHz to avoid audible artifacts. Unfortunately, self-oscillating frequency is a also a function of the input signal. It is thus difficult to avoid or even predict possible audible artifacts.
A similar problem arises for filterless amplifiers. Filterless amplifiers require at least three output levels, with one level being zero. This cannot be realized with a self-oscillating modulator. A common approach [73, 69] is to use two independent modulators, each driving one side of the speaker.

In this case, the modulators have to be synchronized exactly to avoid large ripple current. This is done by coupling the two modulators [73]. In audio amplifiers the coupling is typically done resistively [69, 74, 75]. However, published works [74] have shown, that the modulator coupling degrades THD+N. This observation is in line with extensive system-level simulation carried out in this project.

The dominant modulator architecture in filterless Class-D amplifiers is clearly PWM. PWM allows lower switching rates than PDM leading to higher power-efficiency. PWM enables stable operation up to the full-scale signal range, thereby delivering the largest *rated power* for a given supply voltage. PWM can be easily used in stereo applications. Synchronization between different amplifiers can by done by sharing the reference signal. Unfortunately, with PWM, the energy of the switching harmonics is concentrated in an narrow bandwidth. This can lead to increased EMI problems. But, as will be shown in chapter 5.1, spectrum shaping methods can be used to overcome this issue.

2.2.3. Power-stage design

The power-stage is controlled by the modulator and amplifies the modulator signal to the full supply voltage. Fig. 2.12 shows a typical power-stage as used in various works [76, 77, 28, 18, 27, 44]. It consists of two large transistors operated as switches with appropriate driving circuitry. State of art designs use MOSFET transistors to realize these switches. The switching transistors form a push-pull stage and connect the output node either to the positive or negative supply voltage. The driving circuit is used to quickly turn the transistors ON or OFF.

Most integrated Class-D designs of the last years were implemented in some kind of CMOS [77, 76, 78, 28, 79] or BCD [80, 81] technology. Fig. 2.13 shows the technology nodes used in publications of the last years. The design of Class-D amplifiers involves high precision signal processing in the modulator combined with a certain voltage handling capability in the power-stage. Hence the 180 nm to 130 nm nodes are currently most widely used. They offer a good compromise for analog design and power capability.

In these technologies, two realizations are commonly used for the switching transistors. For output powers above 10 W, typically NMOS transistors

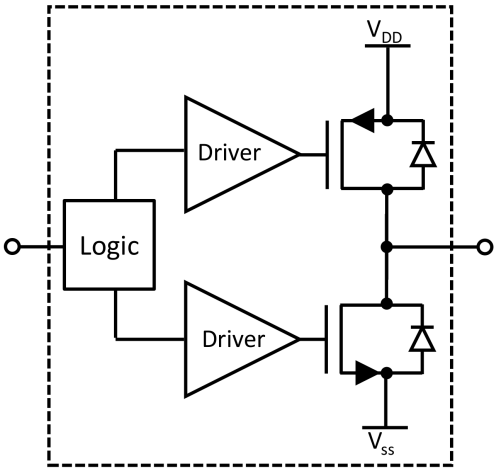


Figure 2.12.: Simplified block diagram of a Class-D power-stage.

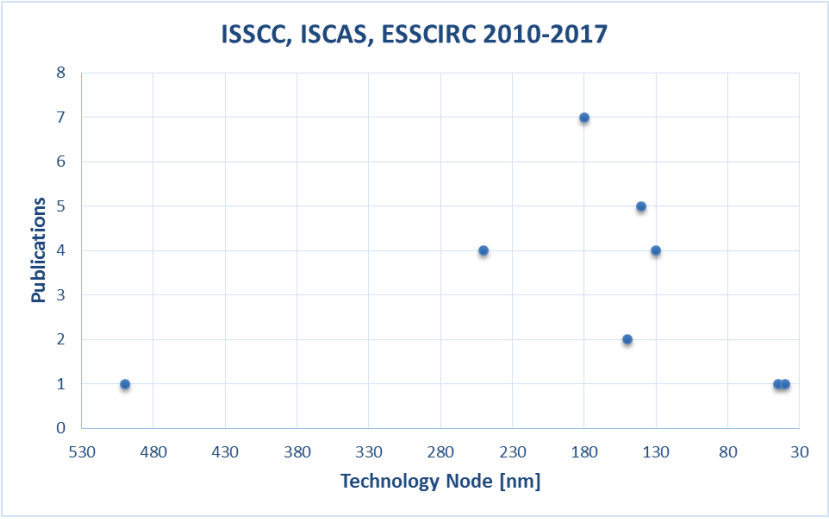


Figure 2.13.: Class-D designs in circuit design conferences.

are used for both switches (e.g. in [82, 11, 83]). For lower powers, often the transistor connected to the positive supply voltage (hereafter called high-side) is a PMOS transistor (e.g. in [77, 76, 28]).

The NMOS only topology is mainly used when supply voltages above 5 V are needed. In state of art CMOS technologies, transistors that can withstand such voltages are often implemented as double-diffused MOSFETs (DMOS). P-channel DMOS transistors are either not available in some technologies, or have a significantly higher resistance in the linear region compared to N-channel DMOS transistors. Using only N-DMOS for the switching transistors is beneficial to reduce silicon area. Unfortunately, the source node of the high-side NMOS is connected to the output node. Controlling the high-side transistor thus requires a driving circuit which is referenced to the output node. As a consequence, to turn the high-side NMOS ON requires a voltage larger than the positive supply voltage. The commonly used solution to generate this voltage, is using an external bootstrap capacitor and to implement a floating high-side driver [83, 84, 15, 16]. Internal charge-pumps are rarely used, due to large energy demand of the gate driving circuit. Additionally, level-shifters (such as described in [85] or [86]) are needed to transfer control-signals from the low-side driver to the high-side driver.

For lower supply voltages, often a P-channel, non double-diffused transistor is used in the high-side. An increase in chip area is accepted, as in turn two external capacitors for bootstrapping and accordingly two package pins can be saved. Moreover, the driver design is simplified, as the high-side driver can be referenced to a fixed potential.

In some designs, cascoded switching transistors are used in the power-stage for higher voltage capability [87]. In this way, a power-stages can be build, which can withstand larger voltages than the break-down voltage of the individual transistors. Such power-stages result from constrained technology choice, but will typically lead to lower power efficiency. These power-stages will not be considered in this work.

The power-stage design is the major engineering challenge in Class-D amplifier design. To achieve highest power efficiency and amplification quality, close-to-ideal switches are needed. Thus, the switching transistors would need zero ON resistance and infinite OFF resistance. Moreover, the transition between theses states should happen without delay and at infinite speed. By using real transistors, non-idealities are introduced, which lead to power-losses and errors in the signal amplification. Additional

requirements, such as electromagnetic compatibility further complicate the design process.

The selection and sizing of the switching transistors largely determines power efficiency. The switching transistors should have a very low ON resistance. Therefore wide transistors are used, which often dominate the chip area needed by the amplifier. Unfortunately wider transistors have larger parasitic capacitance. Such parasitic capacitance causes capacitive losses during switching, which in turn reduces power efficiency. Chapter 3.3 examines how to make the best trade-off in transistor-sizing for optimal power efficiency.

The driver design is another challenge. It was explained above, that full-bridge configurations are used in most integrated Class-D amplifiers. The speaker is connected as a bridge tied load and therefore, each power-stage has to handle hard and soft switching transitions [84]. The circuit concepts for the driving circuits are in part similar to those used in power-stages of DC-DC converters. The drivers need to incorporate some kind of non-overlap circuitry, often implemented using a certain dead-time. This ensures that the switching transistors are not activated at the same time. If both are ON at the same time, a large current would flow from the supply through the transistors' channel. The drivers are used to quickly charge or discharge the gates of the switching transistors to turn them ON or OFF. As will be discussed in chapter 3, stronger drivers allow faster switching, which is beneficial for power efficiency. On the other hand, chapter 4 shows that faster voltage transitions on the output node increase the electromagnetic noise generated and can lead to EMI.

In contrast to DC-DC converters, the power-stage amplifies a high fidelity signal, which encodes audio content. To ensure good audio performance, the power-stage needs to satisfy some additional requirements. The control-signals generated by the modulator need to be amplified without introducing errors. In practical power-stages, several error sources can be identified. The finite ON resistance of the switching transistors introduces a voltage drop, that reduces the output voltage. This voltage drop is a function of the load current. This leads to a signal dependent amplitude modulation of the output signal [52]. Power-supply perturbations will directly couple to the output. Such perturbations can create unwanted tones or intermodulation products with the audio content. The most severe errors are typically signal dependent delays in the power-stage. Such delays modify the duty-cycle of the modulator signal. Ideally, the delay

from the control input of the power stage to a level change at the output should be constant. Unfortunately, the delay is strongly influenced by the magnitude and direction of the load current. This leads to signal dependent modification of the duty-cycle, which generates distortion. Especially the dead-time creates a signal-dependent uncertainty of the switching delay. It was thus identified as one of the most severe mechanisms of signal distortion [88]. To minimize the influence of signal dependent delay, typically strong driving circuits, very short dead-time and high slew-rate in the voltage transitions is implemented. The slew-rate of the voltage transition on the output node typically has a magnitude in the order of 1 V/ns (measurement of several commercial devices [15, 16, 39] and values from scientific works [89, 90]).

It can be concluded, that the power-stage mainly determines power efficiency of the amplifier. Additionally, the large switching transistors determine the layout of the microchip and often dominate the die size. The switching behavior of the power-stage can lead to EMI. Finally, the power-stage is the main contributer of audio signal distortion. A good power-stage design is considered the prerequisite for a successful Class-D amplifier implementation. In this work, a large focus was therefore put on the power-stage design. Chapter 3 and chapter 4 cover analyses and develop methods that help to implement the power-stage.

2.2.4. Error-correction methods

Without correcting power-stage errors, acceptable performance can be achieved only with very careful power-stage design [85, 84]. But THD+N is typically limited to $-60\,\mathrm{dB}$ to $-70\,\mathrm{dB}$. Unfortunately, the power-stage is very sensitive to supply perturbations. To improve linearity and PSRR, error correction methods based on negative feedback are used.

In global feedback approaches, the modulator and the power-stage are embedded into a control loop. For PDM and self-oscillating modulators, the necessary feedback is taken from the output of the power-stage. For PWM, negative feedback and a loop-filter H are added as shown in Fig. 2.14. The error-signal e is processed by the loop filter H to generated a pre-distorted input signal x' for the PWM, thereby correcting errors in y. H should have high gain in the audible region to suppress audible errors introduced in the power-stage. For Class-D amplifiers with full-bridge

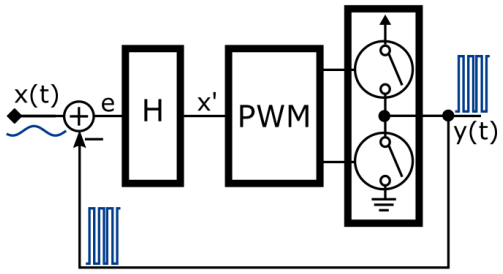


Figure 2.14.: Block diagram of a PWM based Class-D amplifier with global feedback.

power-stage, the global feedback can be realized in two ways: Either a fully differential loop-filter processing the differential output signal can be used. Or two independent, single-ended loopfilters can be implemented, forming a pseudo-differential filter [91]. The first is typically preferred for integrated amplifiers due to better noise performance, the second is used in discrete implementations due to lack of high-performance differential analog components.

The loop-filter is commonly designed by linearizing the PWM and power-stage and modeling it with a constant gain K_{PWM} [92, 93]. Linear feedback theory is then applied to implement a stable feedback loop. For proper operation, the feedback loop has to satisfy the slew-rate criterion for PWM (eq. (2.3)). This limits the largest possible unity-gain frequency f_{UG} of the loop-gain $H\ K_{PWM}$. For first-order loop filters, it was shown [92] that f_{UG} has to satisfy (in the case of filterless, differential, BD modulation):

$$f_{UG} < \frac{2\ f_r}{\pi} \tag{2.5}$$

This restriction is sometimes called *Ripple-Stability*, but is not a stability criterion in the classical sense. If not satisfied, very fast switching rates can occur which are no longer bound by the reference signal frequency f_r. This limits the possible bandwidth available for filter design. Faster PWM is therefore beneficial to design high gain filters.

Unfortunately, closing a negative feedback loop around a PWM intrinsically creates distortion [94, 95, 96, 91]. This is caused by residual switching ripple in x'. This ripple is folded down into the signal band in the PWM process and generates distortion. Different kinds of distortion are generated by differential and pseudo-differential loop-filters [91]. The

differential implementation especially generates high-order distortion. The distortion increases, with increasing input signal amplitude, and increasing input signal frequency.

The loop-filter should preferably have a lot of attenuation at the switching frequency [94, 95], to reduce the residual ripple in x'. High reference signal frequency in the PWM is therefore very beneficial. This allows to design loop-filters with high audio band gain and high attenuation at the switching frequency. Thus, amplifiers with good THD+N figures that were reported in the last years (e.g. [76, 28, 44]), typically have high switching frequency, above 500 kHz. Nevertheless, lower switching frequency is often preferred for efficiency and EMI, limiting THD+N to around -80 dB [91]. Several methods were proposed to reduce this intrinsic distortion, such as reference signal distortion [94] or adapted filter design [95]. In [94] it is also proposed to insert a sample-and-hold block between H and the PWM to reduce the intrinsic distortion. In [44] an analog implementation of this idea was presented, which achieves excellent linearity. Another promising approach is presented in [45], using a novel, less sensitive PWM modulator. Thus, to build a highly linear amplifier, negative feedback only is not sufficient. It has to be combined with measures to reduce the intrinsic distortion.

Instead of global feedback, local feedback can be used. In these approaches, only the power-stage is incorporated in a feedback loop, thereby avoiding the intrinsic feedback distortion. This idea is especially interesting for mixed-mode Class-D amplifiers, where the modulator is implemented in the digital domain. Negative feedback from the output is used to detect errors and then the switching edges are modified to alter the duty-cycle of the PWM signal. Either the direct PWM approach is used [97, 98, 27], or the PEDEC [99] algorithm is utilized. However, presented prototypes generally cannot compete with amplifiers using global feedback. Imperfections in the input PWM signal are not corrected. For filterless Class-D amplifiers, an independent feedback loop for each power-stage is needed, which can lead to non-symmetry.

3. Power efficiency: Measurement, analysis and simulation

The energy efficiency of a Class-D amplifier is mainly determined by the loss mechanisms present in the amplifier's power-stage. The design and implementation of the power-stage therefore determines one of the main performance parameters. In this chapter, the measurement of power efficiency is examined in detail. The difficulties in correctly measuring this parameter are outlined. Then a modified measurement setup is proposed for more accurate measurement of filterless Class-D amplifiers. In the second part of this chapter, the different loss mechanisms present in a power-stage are analyzed. Several previous loss analyses are combined and modified to form an analytic efficiency model for filterless, BD-modulated amplifiers. This proposed model is based on physical implementation parameters and helps to optimize the design of a power-stage.

3.1. Measuring the efficiency of low-power, filterless amplifiers

The power efficiency η is defined as the ratio of power drawn from the supply P_{SUP} to real power delivered the load P_{OUT} [2, 4, 43]:

$$\eta = \frac{P_{OUT}}{P_{SUP}} \tag{3.1}$$

The typical efficiency measurement setup [2, 4, 6, 43] can be seen on Fig. 3.1. The measurement results are intended to help with the calculation of cooling requirements or battery lifetime. It is therefore desirable to carry

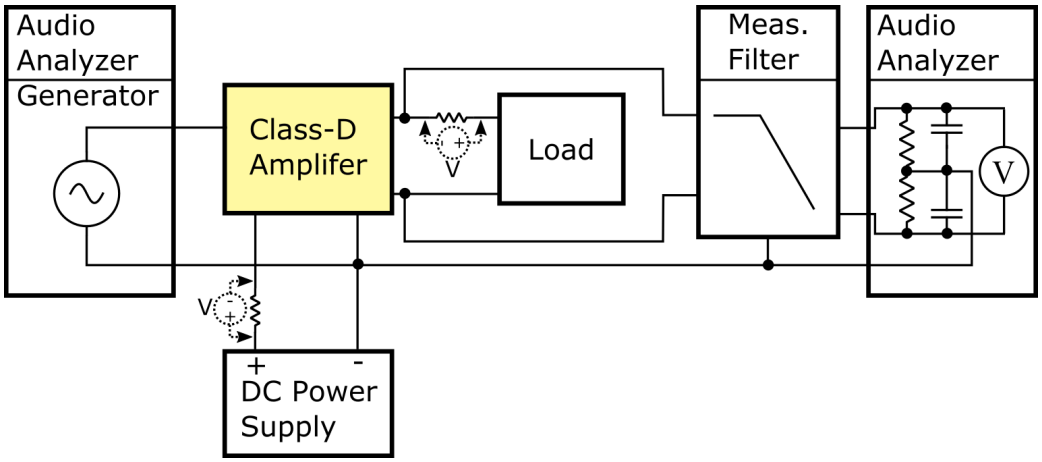


Figure 3.1.: Efficiency measurement setup for Class-D audio amplifiers, proposed in [2, 4, 43].

out the measurement with a realistic test signal as input for the audio amplifier. Unfortunately, audio content is very diverse and typically has high dynamics [38, 100, 101]. Several research groups (e.g. [102, 100, 101]) have analyzed the frequency content and amplitude distribution of different audio signals to derive their characteristics. In that way, several proposals for test signals that represent standard audio content exist. The IEC60268-1 [42] standard defines a test signal basically consisting of filtered pink noise. In [100] an efficiency-test signal suitable for circuit simulators is proposed. It consists of a sum of 24 square-wave signals of different fundamental frequency. The authors of [101] propose a test signal consisting of a distorted sinusoidal signal, which has similar spectral characteristic and amplitude distribution as a large music library. Nevertheless, the de-facto industry standard [2, 43] is to use a sinusoidal input signal with a frequency of 1 kHz. The amplitude of the sinusoidal signal is typically increased from a low value until the amplifier starts clipping. This is indicated by sharply increasing THD+N. The average real input power and average real output power are measured. The power-efficiency is calculated for each input amplitude.

Next, correct loading of the amplifier should be discussed. The IEC60268-3 [38] standard specifies to measure amplifiers with a purely resistive load, if not specified differently by the manufacturer. This is also recommended for traditional, filtered Class-D amplifiers by manufacturers of measurement equipment [2]. However, for correct and realistic circuit operation, a filterless Class-D amplifier has to be loaded with an electrodynamic loud-

speaker. To allow repeatable and comparable results, speaker-dummies are generally used. Such dummy loads consist of a resistor in series with an inductor [43]. A typical electrodynamic loudspeaker with 8 Ω rated impedance is often modeled by an 8 Ω resistor and an 33 µH to 68 µH inductor [16, 26, 39]. In this work, a series combination of 22 µH + 8 Ω + 22 µH was used for all measurements. The construction details will be explained later. The impedance of this dummy load was compared to several electrodynamic loudspeakers with 6 Ω to 8 Ω rated impedance. Fig. 3.2 shows the measurement results. In the audible region, the impedance of the speakers shows one or more resonances, but is generally dominated by resistive behavior below 1 kHz. At the upper edge of the audible region, all speakers start to show an inductive behavior. Above the audible region, all speakers show a parallel-resonant impedance peak. The parallel-resonant impedance peak of the dummy load is caused by the resonance frequency of the used inductors. It occurs between the resonances of the 0.5 W and 10 W speaker. The resonance of the dummy load shows a lower damping, but the characteristics of the simple load model fit remarkable well to typical speakers of lower power.

Integrated Class-D amplifiers generally need a DC power supply. The average supply power can be calculated easily by multiplication of the average supply current with the supply voltage. The average supply current is measured with a shunt resistor or a current probe [43].

As explained above, Class-D amplifiers with a build in output filter, are typically measured with a purely resistive load. In this case, the output power can be easily determined by measuring the root-mean-square (rms) voltage across the load. This measurement is done using an audio analyzer [2, 3, 4]. Still, a portion of the identified real power, might result from signals outside the audible region. It is thus questionable, if such a power measurement is valid to calculate an efficiency figure. Measurement equipment manufacturers therefore recommend to limit the measurement bandwidth [2, 3]. In practice [2, 39, 81], often a very sharp 20 kHz low-pass filter as defined in the AES17 [41] standard is used. In this way, only the real output power in the audible region is considered. The situation is more complicated for filterless amplifiers, which need an inductive-resistive load. The measurement results in scientific publications (e.g. [18, 27, 44]) typically do not state, how the output power is measured. In some measurement guidelines [4, 5] the authors recommend to measure the rms current and rms voltage at the load. The authors claim, that the power can than be calculated by multiplying these figures. However, in this definition

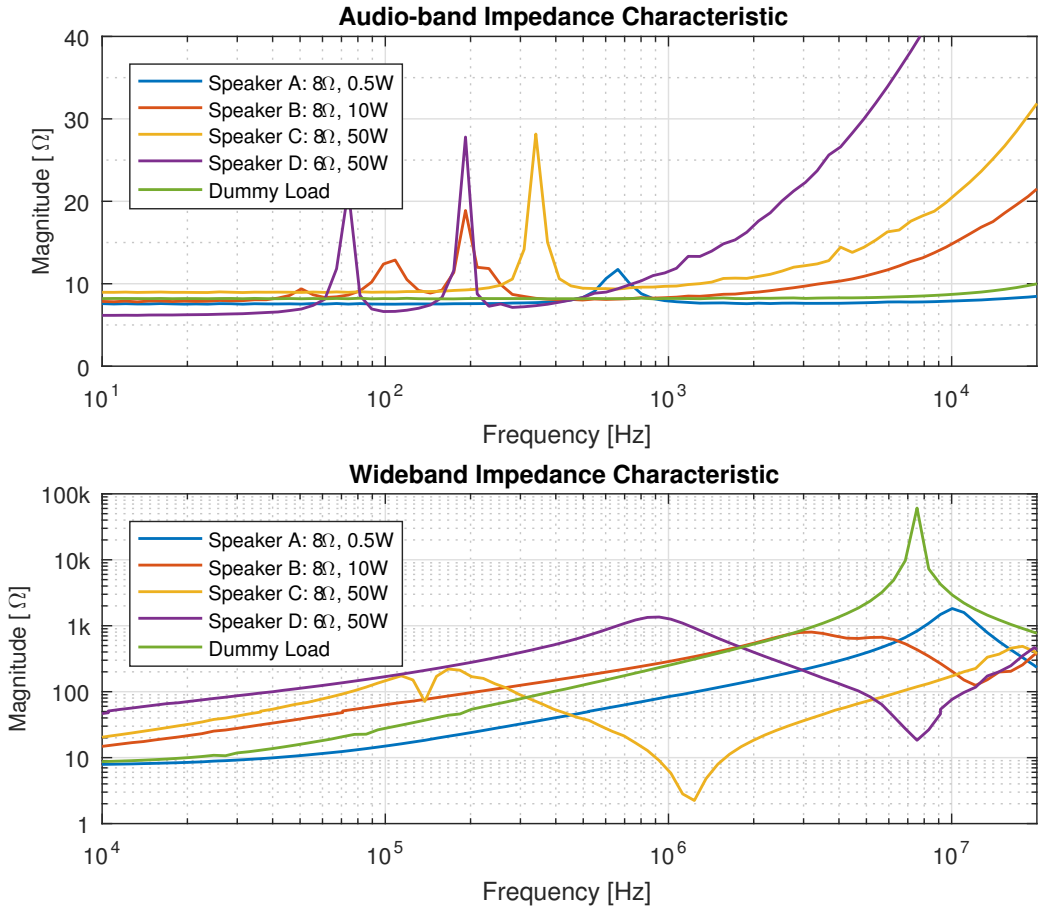


Figure 3.2.: Impedance characteristics of several loudspeakers and the used dummy load.

the phase-relation of current and voltage is not considered and apparent power will be calculated.

Another thing to mention is the measurement filter. The available analyzers on the market [2, 3] cannot directly measure the Class-D output signal. The switching waveform at the output of Class-D amplifiers can have a very high slew-rate. This high slew-rate cannot be handled correctly by the input stages of the measurement equipment [2, 6]. Therefore, low-pass measurement filters are used to protect the audio analyzers from signals with high slew-rate. Due to the high dynamics of the Class-D signals, only passive filters are recommended [2, 3, 4, 6]. Single-stage RC filters [3, 4], multi-stage RC filters [6] and multi-stage LCR filters [2] are proposed in literature. The energy needed by these filters, was generally neglected in the past, where Class-D amplifiers were mainly used for high power applications. However, nowadays filterless Class-D amplifiers are also used in mobile applications, where the needed output power is often below 1 W [31]. When characterizing the efficiency of such a device, the measurement filter should be considered. As a simple example, lets assume a filterless Class-BD amplifier supplied by 5 V is driven with a 1 kHz sinusoidal input signal. The input signal has an amplitude of one tenth of the full input range. The amplifier will create appr. 15 mW of average output power at an 8 Ω speaker in this case. In [4] a first order RC-low-pass filter is recommended for efficiency measurements. It consists of a 1000 Ω resistor and a 5.6 nF capacitor connect in series between each output of the Class-D amplifier and ground. This filter would consume appr. 12.5 mW of average output power. In this case, a significant error is introduced into the measured supply power due to the measurement filter. Numeric compensation of the generated error is difficult, as the efficiency is measured with an AC input signal. The resistance of the filter cannot be increased arbitrarily (and capacitance decreased), as the filter is loaded with the input resistance of the audio analyzer. Industry standard audio analyzers have an input impedance of 100 kΩ [103, 3] and the filter resistance should be significantly smaller.

Accordingly, in the state of the art measurement setups, the measurement of output power leads to two difficulties when measuring low-power, filterless amplifiers: Capacitive loading due to measurement setup creates losses that can be in the same order as the measured output power. The calculated efficiency will thus appear lower than it actually is. Secondly, real output power measurement with non-resistive load is either not considered in standards [38] or it is proposed to measure apparent power

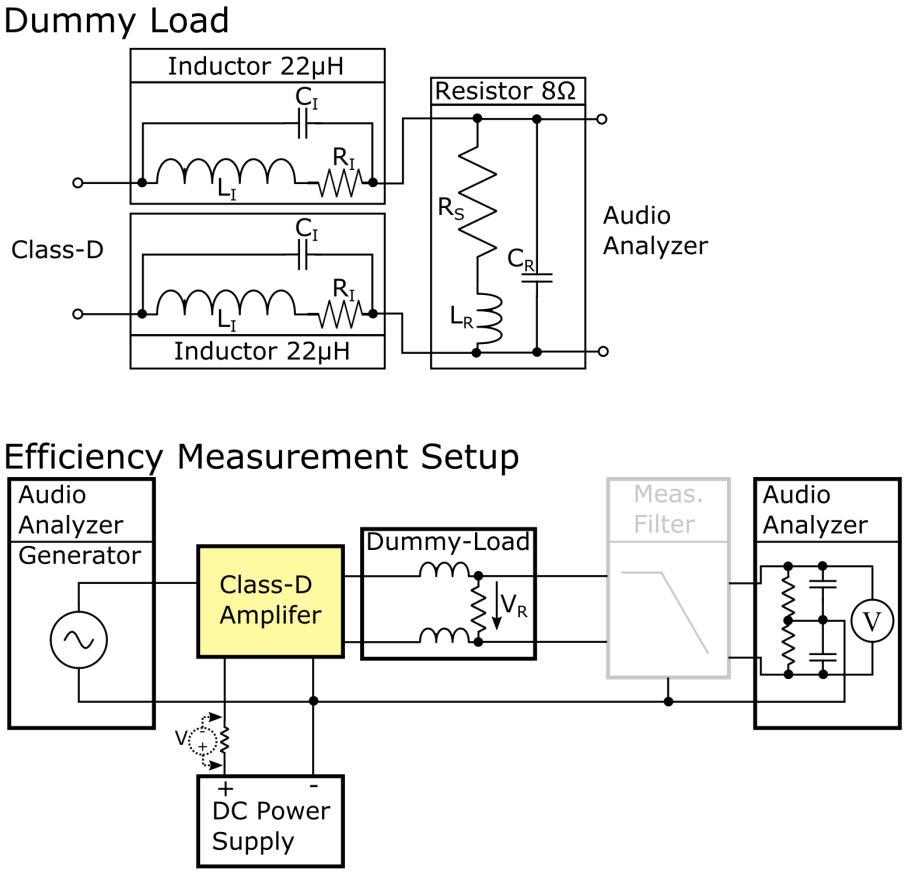


Figure 3.3.: Proposed dummy load and efficiency measurement setup for low-power, filterless Class-D audio amplifiers. The shown measurement filter can be omitted for many audio analyzers.

in some guidelines [4].
In this work a modified output power measurement setup is proposed. It is intended for low-power, filterless Class-D amplifiers and allows lower capacitive loading of the amplifier. First, the dummy load is build as shown in the top of Fig. 3.3. As stated above, it consists of a series combination of two inductors and a resistor. The most important parasitic components of the load are sketched. The resistor should be a low inductive component with well defined resistance R_S. It should have an appropriate power rating for the intended amplifier, to avoid self-heating during measurement. A parallel combination of low-tolerance, thick-film resistors with appropriate cooling is recommended. Constructed in this way, the resistor of the dummy load can be used as a shunt for load current measurement.
The inductors should have a saturation current at least twice the expected load current. This is necessary to avoid excessive non-linearity, which can distort the output signal. The self resonance of the inductor should be at least an order of frequency above the Class-D switching frequency. In this way, high-frequency components in the load current are filtered by the inductor. The dummy load can even be used to imitate a certain family of speakers. The inductors' self resonance frequency and the DC resistance can be chosen to resemble the resonant impedance peak and damping of a certain speaker (Fig. 3.2). However, the DC resistance should be sufficiently small to avoid heating of the coil. Shielded inductors are recommended to reduce magnetic coupling between the two inductors. Moreover, the inductors are ideally selected by hand for best matching and the layout of the load should be very symmetric. The complete setup for real output power measurement is shown in the bottom of Fig. 3.3. The rms voltage V_R across the load resistor is measured using an audio analyzer. Then the real output power is calculated by:

$$P_{OUT} = \left[\frac{V_R}{R_S}\right]^2 (2R_I + R_S) \tag{3.2}$$

R_I is the real part of the inductors' impedance. In the audible range it is equal to the inductor's DC resistance (for properly chosen inductors). Fig. 3.3 also shows a measurement filter. This filter can be omitted for most modern audio analyzer. The inductors of the dummy load will provide sufficient low-pass filtering of the measured differential signal. Unfortunately, the measured signal also has a high frequency common-mode component. Conversion of this common mode component to differential mode signal is greatly avoided by the symmetric layout of the load. In

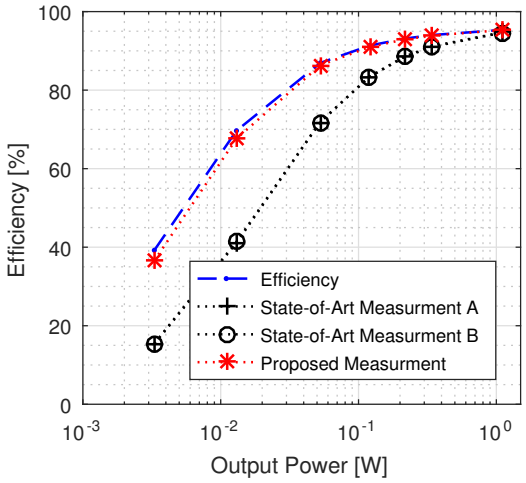


Figure 3.4.: Simulation of different efficiency measurement setups for a 1.5 W filterless Class-D amplifier.

addition, the common-mode rejection of modern analyzers is in most cases sufficient to achieve an accurate rms reading.

In comparison to previous measurement methods [2, 4, 6, 43], the Class-D amplifier is thus not loaded with a measurement filter. Moreover, the amplifier is loaded only with a single measurement instrument. In this way capacitive loading is reduced and accurate measurement results for low output powers are possible. Finally, the setup allows to measure real output power even for resisitive-inductive loads.

To demonstrate the benefits of this new output power measurement setup, a simulation was carried out. The simulation in *LTSpice*® incorporates a 1.5 W filterless Class-D amplifier. The modulator is implemented as a behavioral model, the power stage is a transistor-level model using level one spice models. The amplifier is loaded with a model of the speaker dummy (top of Fig. 3.3) and excited with a sinusoidal input signal at 1 kHz. In simulation, the correct efficiency can be determined easily without having to consider measurement equipment. The simulation was than extended with a model of the state of art measurement setup [3, 4, 6, 2, 43] (Fig. 3.1). The measurement filter and the input impedance of the audio analyzer were modeled [103, 3]. In case A, the measurement filter proposed in [4] was used. In case B, a model of a commercially available filter [104] was used. The manufacturer of this filter does not provide the schematic, but the design was reverse-engineered in [105]. Finally, the efficiency

was simulated with a model of the proposed setup (Fig. 3.3). Figure 3.4 shows simulation results. The correct efficiency calculated from node voltages and branch currents (without the measurement setup modeled) is compared to results which would be derived with the measurement setups. As can be seen, the two state of art setups lead to very similar results. Both underestimate the efficiency. Especially at low output powers, the loading due to the measurement equipment and filters shows significant impact. The deviation to the correct efficiency value is appr. 28 % at 13 mW output power. Using the proposed output power measurement setup, the derived efficiency value is much closer to the correct value. A minor deviation of appr. 2 % at 13 mW output power is still visible. This deviation results from the loading effect due to the input capacitance of the audio analyzer. The input capacitance of an industry standard analyzer is 190 pF to 200 pF [103, 3].

The commercially available measurement filter [104] (setup B) is widely used in the industry. It is clearly not suited for efficiency measurements of low-power, filterless amplifiers. Still, it is frequently used, e.g. in the datasheet of [39]. For power-efficiency measurements at output power levels below 1 W, the modified measurement setup proposed in this work should be used. The proposed setup needs only a single measurement device and can be used down to several mW.

3.2. Analysis of loss contributors

A typical, filterless Class-D amplifier is shown in Fig. 3.5. Designs like this are used in many implementations for mobile applications [77, 28, 18]. All different blocks are implemented on the same silicon die. The amplifier features two power-stages. Each power-stage consists of a PMOS and NMOS transistor in push-pull configuration with appropriate driving circuit. As discussed in chapter 2.2.3, the drivers incorporate a certain non-overlap, such that PMOS and NMOS transistors are never ON at the same time. The amplifier is used to drive an electrodyanimc loudspeaker, which can be considered a resistive-inductive load. The inductance of the speaker will limit the rate of change of the load current. Thus, the inductance will keep the current flowing even during switching transition of the output nodes.

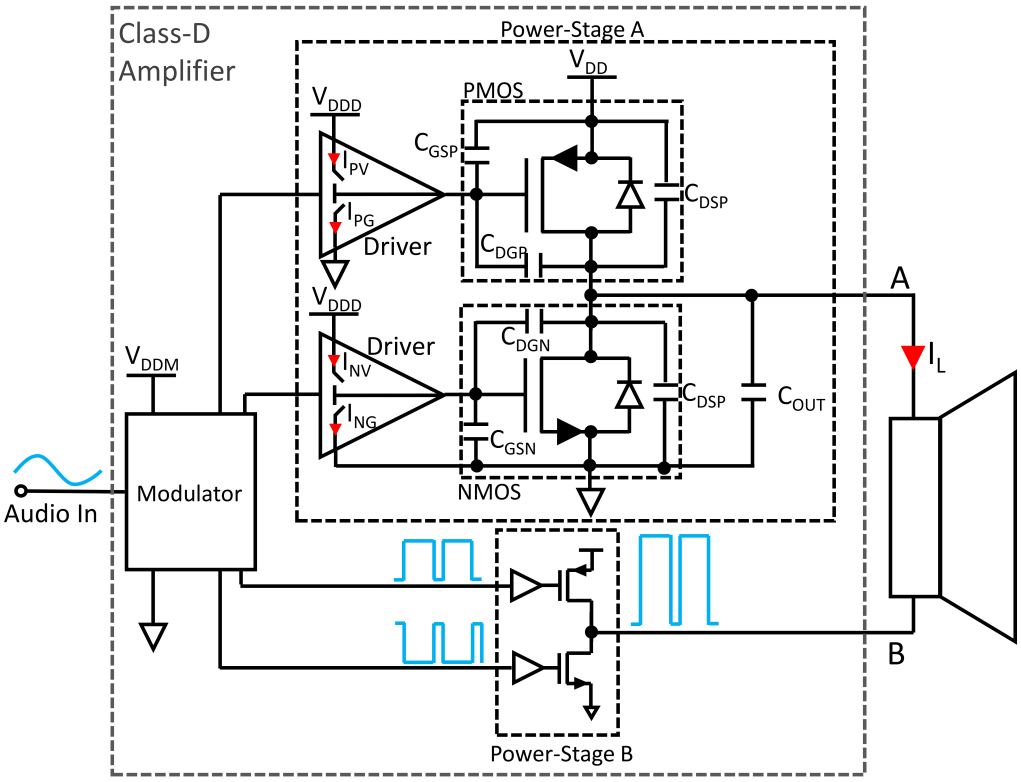


Figure 3.5.: Filterless Class-D topology with a PMOS/NMOS power-stage.

Several parasitic components are associated to the switching transistors, as indicated in Fig. 3.5. These parasitic components are responsible for several different loss mechanisms that reduce the power efficiency of Class-D amplifiers. The loss mechanisms might be dominant at different output powers. The most prominent mechanisms in filterless Class-D amplifiers are discussed below.

- Shoot-through current
  If both switches of an output-driver are activated at the same time, a high current will flow from V_{DD} to ground through the transistors. This shoot-through current should be avoided by design using dead-time. Additionally, the sizing of the driver circuits must be done carefully. Otherwise a transistor which was OFF can be switched ON unintentionally during a switching transition. This can happen due to displacement current conducted by the transistors gate-drain capacitance [8, 85].
- R_{on} Losses
  Even when turned ON, the used switching-transistors have a non-zero resistance. This resistance is mainly made up of channel resistance, but also contains resistance in metal traces and bond-wire resistance. This so-called R_{on}, causes a resistive loss. Using wider switching transistors, and higher driver voltage will yield a lower R_{on} and reduce these losses.
- Switching Losses
  When switching the output node up or down, all the capacitors associated with the output node need to be charged. If this charge is drawn from the supply voltage, capacitive losses are generated.
  The transistors cannot be switched ON and OFF at infinite speed. Thus, current can flow through the transistor's channel while it is not completely ON. This leads to resistive losses at the switching transitions. Finally, due to dead-time, the inductive load can force current trough the body diode of the transistors. This leads to diode losses.
  The capacitive losses can be reduced by narrower switching transistors. The diode losses consist of conduction losses in forward operation and losses due to reverse-recovery. Typically they are technology dependent. Stronger driver circuits can help to reduce the resistive losses due to faster switching, but will increase EMI problems in turn [106].
- Driver Losses

The switching transistors are periodically turned ON and OFF. This is achieved by charging and discharging the parasitic capacitance associated with the transistors' gate. Using narrower transistors and lower driver voltage reduces these losses.

- Signal processing quiescent current
  The modulator block needs energy to perform the PWM generation and signal processing. These losses are prominent for very low output power.

From the above analysis, it can be concluded, that switching-transistors with low R_{on} and low parasitic capacitance should be used for lowest losses. Building a high-efficiency Class-D amplifier thus starts with selecting an appropriate technology for implementation of the power-stage. For the power-stage design, the technology with lowest *Ron* and capacitance per area is favorable.

The design of an integrated Class-D amplifier typically allows a large degree of freedom to choose the different parameters, such as transistor width, driver voltage, driver strength and similar. Considering all the loss mechanisms, it is apparent, that increasing the overall power efficiency is a multidimensional optimization problem. This is especially true when not only the efficiency at peak power, but also the efficiency at lower output power is to be considered. Moreover, the impact of parameter selection is not only limited to efficiency. For instance, the targeted PWM frequency and rise/fall-times of the voltage transitions have a main impact on EMI. Slower rise/fall times will help to avoid radiated emission issues [106]. But slower transitions also increase the switching losses. Lower PWM frequency is beneficial for EMI and efficiency. Unfortunately lower PWM frequency severly limits the the audio performance of global feedback loops. Additionally, several methods are proposed by research groups to improve efficiency, such as *switching frequency regulation* [11], or *dynamic power stage activation* [27]. However, whether a certain method is effective and how to implement it, often depends on the technology used and on system level considerations. This complicates parameter selection. It is thus a difficult task to choose the optimum parameters for best power efficiency, especially when system-level cross-correlations have to be considered.

3.3. An analytic efficiency model

Accurate simulation of the efficiency can be done at transistor level, but requires significant computation time. This is because the frequency of the PWM signal is at least an order of magnitude higher than the test signal applied to the amplifier. Hence, a long simulation with a high temporal resolution has to be carried out. This issue is well known from over-sampled data systems [107], where behavioral transient models are used to estimate the circuit performance [107, 56]. These behavioral transient models allow early design decisions and design optimization. In the ideal case, transistor-level simulation are then only needed for verification.

A similar approach of an abstracted model of the power-stage was developed in the course of this work. The main intention of the model is to predict power-efficiency measurement results in a fast and flexible way. The computational effort is very small compared to transistor-level simulations. It thus allows parameter sweeps in a fast way. Early design decisions can be made easily, and the best parameter trade-off for the design can be found. Once the optimum design parameters are found, transistor level implementation can be started.

The proposed model determines the losses for a given input signal and then calculates the efficiency. Loss analyses have been carried out previously for Class-D amplifiers [8, 11, 9]. The analysis of Nyboe [8] covers many parasitic effects but is targeted towards higher-power amplifiers with inductive output filtering. The work of Yamauchi et al. [9] is largely based on [8], but focuses on the core losses in the inductive output filter. The work of Ma et al. [11] is targeted towards piezo-electric speakers, and the loss analysis neglects resistive switching losses. The proposed model in this work calculates the losses based on these previous works [8, 11, 9]. But the results of these works are combined and modified, to account for the properties of low-power, filterless amplifiers: Small parasitic effects become more important, as no lossy output filter is present; lower supply voltages are used (often below 5 V [77, 28, 18] in the mobile market); no ripple current is present at idle. The derived loss expressions are then applied to the operation principle of BD-modulated amplifiers. In this way a new analytic efficiency model for Class-BD amplifiers is generated. The proposed model can be used to calculate the efficiency of the amplifier when excited with an arbitrary input signal. The losses are thereby

calculated from a small number of physical parameters of the switching transistors and driving circuitry.

3.3.1. Derivation of the model

The proposed efficiency model approximates an arbitrary output signal by a stairstep representation. Each stairstep has a width of one PWM period $T_{PWM} = 1/f_r$, for which the losses are calculated. The calculation is based on the average instantaneous load current I_L, which is the average load current in each PWM cycle. This approximation does not consider ripple current. The simplification is made, because in filterless Class-BD amplifiers, there is no ripple current at idle, additionally there is no inductive output filter which could create losses due to ripple current. Finally, the separately calculated losses of each PWM period are summed together to determine the losses for the complete output signal.

The different losses are calculated for a power-stage consisting of PMOS and NMOS switching transistors as shown in Fig. 3.5. The capacitive and resistive switching losses are calculated based on [8, 11]. The work of Nyboe [8] gives a detailed analysis of the resistive losses in Class-D power-stages. The analysis can be combined ideally with the ideas of Ma et al. [11] to model the capacitive switching losses. Nyboe's and Ma's original analyses consider a single, NMOS only, power-stage in a classic filtered Class-D amplifier. In this work, these analyses were adapted for PMOS/NMOS stages. The derived results were then extended for two power-stages with a bridge-tied load, as used in filterless BD modulated amplifiers. The derivation is shown in appendix A.1 and allows to calculate the capacitive and resistive switching losses for each PWM period, if the following data is available: the load current I_L; the values of the parasitic capacitances; the current which can be sinked and sourced by the driver circuits; the used dead-time in the drivers; as well as the threshold voltages of the switching transistors.

The R_{on} losses are calculated based on the work of Yamauchi et al. [9], the derivation is shown in appendix A.1. The driver losses in each PWM cycle are calculated as suggested by Ma et al. [11] (appendix A.1).

Finally, an efficiency estimation can be carried out. In efficiency measurements, sinusoidal test-signals are used. State of the art filterless Class-D amplifiers typically have high linearity, with THD+N in excess of $-60\,\mathrm{dB}$

[15, 39]. Therefore, the load current will have the same shape as the sinusoidal test-signal. Hence, an integer number of periods (e.g. $N =$ seven periods) of the sinusoidal test signal is analyzed with the model. The losses in each PWM period are calculated and summed up for the complete signal. In this way the total loss E_T is derived. The total energy delivered to the load is easily calculated:

$$E_L = \left(I_A \sqrt{2}\right)^2 R_L \frac{N}{f_{TS}} \tag{3.3}$$

Where f_{TS} is the frequency of the sinusoidal test signal, I_A is the amplitude of the generated load current and R_L is the real part of the load-impedance. Finally the efficiency can be calculated to

$$\eta = \frac{E_L}{E_T + E_L} \tag{3.4}$$

The amplitude of the generated load current I_A can be swept to determine a complete efficiency curve. This model was implemented in *Matlab*® and allows to create a complete efficiency curve within seconds. The model helps in very fast efficiency prediction of a filterless Class-D amplifier at different power levels.

3.3.2. Application of the model in the design process

The benefits of using this efficiency model are demonstrated at the design of an integrated power-stage. The model helps in fast decision making for the different trade-offs, before implementing the power-stage. A filterless Class-D amplifier was designed by the author in 180 nm CMOS technology. The power-stage is implemented as part of the Class-D amplifier. It is composed of PMOS high-side switches and NMOS low-side switches. Inverter based drivers are used. It has a supply voltage of 5 V and it is intended to drive up to 1.5 W into 8 Ω speakers.

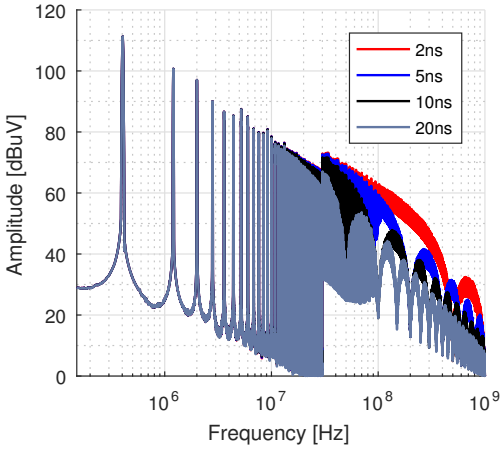
Using transistor models provided by the foundry, first a couple of simple simulations need to be carried out to extract the parameters. For this purpose, unit transistors are used, thus transistors of minimum length and a certain width (e.g. 100 µm). For such a transistor, the different parasitic capacitances, threshold voltage, R_{on} and gate charge can be extracted in short time. The actual parameters of the transistors used in the power-stage can than be derived easily by scaling the extracted parameters. This

is a practical approach as the power-stage often consist of multiple unit transistor connected in parallel.

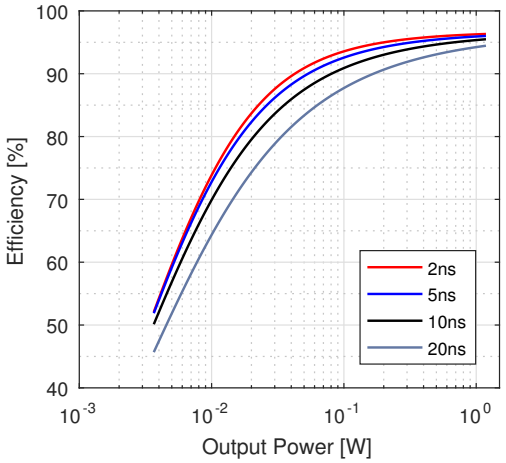
Fig. 3.6 shows some examples of the parameter sweeps and analyses performed in the design. First, the trade-off between EMI and efficiency was considered. Fig. 3.6a shows an EMI-simulation of a PWM signal for varying rise/fall times. The simulation setup will be explained in detail in chapter 4.3. Slower switching clearly reduces the generated high-frequency noise. In Fig. 3.6b the according penalty on efficiency is estimated using the analytic efficiency model. Fig. 3.6c visualizes the relation of R_{on} on efficiency. Lower R_{on} increases the peak efficiency. On the other hand, wider transistors are needed to lower the R_{on}. This increases the parasitic capacitances and reduces efficiency at lower power. Fig. 3.6d shows the relation of the different loss mechanisms at varying input signal amplitudes. For each amplitude, the loss contributions are shown as a fraction of the total input power. In the used technology and for the selected rise/fall times, the switching losses and driver losses dominate at very low power. At higher power, the R_{on} losses become dominant. Depending on the intended application, the amplifier can now be optimized for certain efficiency targets.

The model's results were directly used for the transistor-level implementation of the power-stage. Transistor level simulations was only needed for verification. Fig. 3.7 shows a photograph of the fabricated silicon die. The Class-D amplifier operates at a switching frequency of 400 kHz. The power-stage has an area of 0.57 mm^2, the low-side switches have a total R_{on} of 200 mΩ, the high-side switches have an R_{on} of 280 mΩ. Fig. 3.8 shows power efficiency measurements. The estimated efficiency values by the model and transistor-level simulations are indicated. The transistor-level simulations are done at post-layout stage. Parasitics of the package and circuit board were considered for the model and simulation. The measurements are carried out with the measurement setup proposed above.

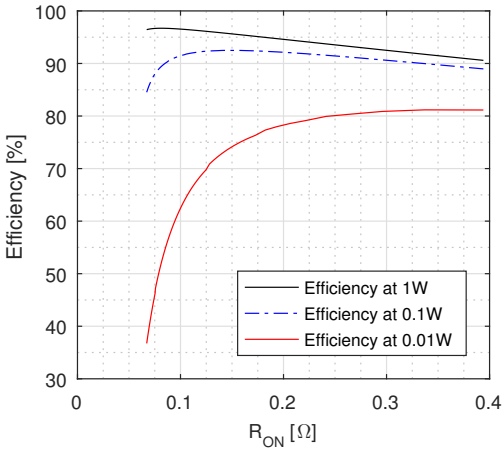
The transistor parameters needed for the analytic model are extracted from the simulation models provided by the foundry. In the ideal case, the model results should thus perfectly match the transistor-level simulation. Above 100 mW of output power, the deviation between model and transistor-level simulation is below 0.5 %. Below 10 mW, the deviation increases towards 3.5 %.



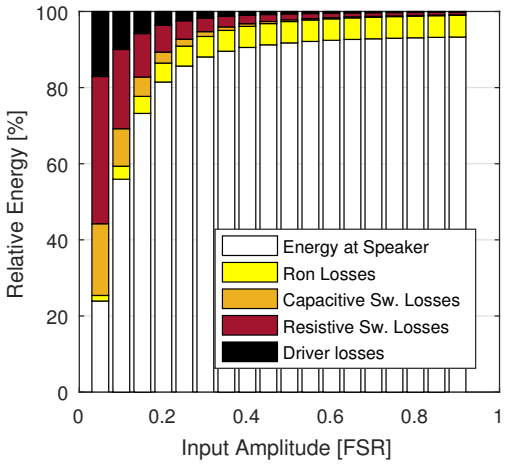
(a)Simulation of conducted emissions for different rise/fall times of a PWM signal. A high-level model of the power stage is analyzed with the emission simulation presented in chapter 4.3.



(b)Power efficiency for different rise/fall times of the power-stage.



(c)Power efficiency for varying R_{on} ($R_{onP} = R_{onN}$).



(d)Relative distribution of the different loss contributers

Figure 3.6.: Design parameter sweeps.

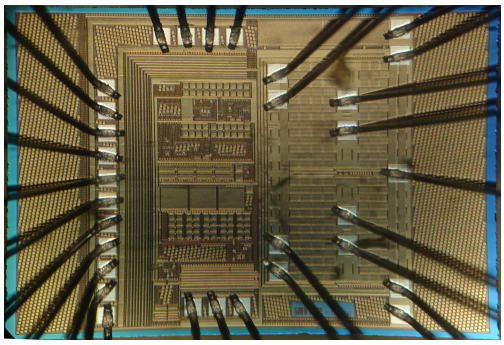


Figure 3.7.: Chip photograph of the Class-D amplifier prototype.

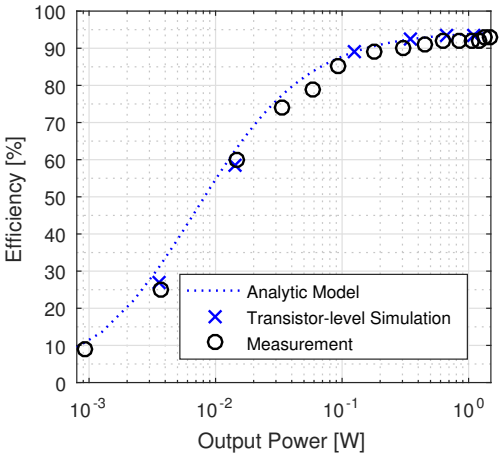


Figure 3.8.: Estimated, simulated and measured power efficiency of the integrated prototype.

The transistor-level simulation show some deviation to the measurement results. Above 100 mW, the simulation overestimates the measured efficiency by 1.5 %. A plausible reason for this deviation is diode loss. The body-diode is not characterized in the transistor models provided by the foundry.

3.4. Conclusion

In this chapter a new measurement setup to determine real output power of low-power, filterless amplifiers is found. In contrast to industry standard measurement setups [2, 104], the new setup is more accurate, because it reduces capacitive loading. Simulation results were conducted to compare previous setups with the setup proposed in this work. The impact of the measurement equipment on the efficiency result could be reduced from more than 25 %, using previous setups to 2 % using the proposed setup. Hence the new measurement setup is suitable to characterize the efficiency of low-power, filterless amplifiers below 1 W.

The work further shows that optimizing the power efficiency is difficult, due to cross-correlation of the different parameters. Transistor-level simulation are not suitable for optimizing due to long computation time.

Behavioral models for power-stage efficiency of filterless Class-BD amplifiers could not be found during extensive literature research. Hence an efficiency model to estimate the power-efficiency was developed in this work. The model is based on previously published loss analyses for filtered amplifiers. These previously published analyses are combined and modified to develop a novel efficiency model for filterless Class-BDs. The model is based on physical implementation parameters, and allows fast parameter sweeps. The benefits of this model were demonstrated at the design of an integrated power-stage. The model needs less than 1 second to estimate an efficiency curve on the author's notebook (Intel Core i7-4600U processor). Transistor level simulation at post-layout stage took about 5 days for a single power-level on dedicated simulation hardware (Intel Xeon E3-1240 processor, simulation running with a single thread). This significant reduction in simulation time is achieved with an error of less then 0.5 % above 100 mW output power, compared to post-layout simulation. With this model early design decisions can be made, optimization of the power-stage parameters can be carried out and different implementation variants can be investigated before transistor-level simulation. The model will thus help to reduce design time.

4. Emission measurement and simulation

Electromagnetic compatibility (EMC) has become an increasingly important topic in the development of electronic devices. In order to bring a product to the market, it has to comply to legal EMC regulations. These regulations are specific to individual countries, but are mostly based on the American FCC or the European EN regulations for consumer products. These regulations have two aims: Electronic devices should operate without malfunction in the vicinity of other devices, or when exposed to static discharge. Thus they should have a certain level of immunity. On the other hand the devices should not cause electromagnetic interference. Thus they should not create excessive emission which can couple to other devices.

In this chapter, it will be shown that Class-D audio-amplifiers can be a potent source of electromagnetic noise. Then, a new measurement setup to quantify the generated noise of filterless Class-D amplifier is proposed. Finally, a simulation approach is presented. Using this approach, the generated noise can be evaluated during design phase of the integrated circuit. In this way costly and time-consuming design iterations can be avoided.

4.1. Class-D amplifiers as emission sources

Chapter 2.1 has shown that the switched mode nature of Class-D powerstages creates electric signals high above the audible region. These signals will be referred to as high-frequency noise. The created noise can couple to other blocks on the same circuit board, via conducted, capacitive or inductive coupling. Moreover, this noise can create radiated emission that will conflict with the legal regulations.

Fully integrated amplifiers incorporate all functional blocks on the same silicon die. This die is contained in a appropriate package. State-of-the-art packages have become very small, with an area of only a couple of mm^2. This small area significantly reduces direct noise coupling from the amplifier to the other components on the same circuit board. However, the amplifier can act as a noise source. The coupling of this noise to the environment is accomplished outside the chip-package, either via PCB traces or cable harnesses.

Therefore, two main effects will be relevant for the emission created by integrated Class-Ds. First, the current drawn from the power supply is not constant. The switching activity causes large current gradients dI/dt at the supply pins. These current variations can be considered high frequency current noise. Second, the voltage at the outputs of the Class-D shows a rapid switching activity. Thus, large voltage gradients dV_{out}/dt at the output pins are present, which can be considered high frequency voltage noise.

The varying supply current can cause significant electromagnetic interference. Some of the coupling mechanism are: The impedance of the supply network will convert the current noise to voltage noise. Thus, the voltage along the supply bus will no longer be constant. The created voltage noise will impact all circuits on the same supply bus. The effect, is not only limited to the positive power supply, but also to the negative supply bus, where it is frequently called ground-bounce. Next, the current flows in a loop, from the power source, via the positive supply bus to the amplifier and back to the power source via a ground bus. The variation of the current in this loop will create a high-frequency magnetic field. Via near-field coupling, this field can disturb other circuits by interacting with nearby PCB traces. Moreover, the current loop will act as a loop antenna and create radiated emission.

A way to reduce the created interference is to have a low impedance supply network. Ideally this network forms a loop with very small area to reduce its ability act as an antenna. A common way [108] to achieve this is to add supply decoupling capacitors between the supply and ground pins of the amplifier. In this way, the supply network becomes locally low-impedance for high frequency noise and a short return path is provided for the high frequency currents. Most manufacturers of integrated Class-Ds request a certain minimum value of decoupling capacitor in their datasheets. It should be noted, that the value only affects the supply network impedance

at low frequencies [108]. For higher frequencies, the parasitic inductance in series with the capacitor has to be taken into account. This inductance consists of the circuit board traces, bond-wires of the IC and series inductance inside the capacitor. It is therefore recommended [108], to place multiple decoupling capacitors of small size as close as possible to the supply pins, to reduce the inductance.
The decoupling capacitors have low requirements on linearity and temperature stability. Thus they are cheap and several microfarad of capacitance can be fit into tiny surface mount packages. Therefore these capacitors are commonly accepted by device manufacturers, because they do not significantly increase costs and board space.
The impact on the supply network can be further reduced at certain frequencies. One possibility is to artificially increase the supply impedance between the amplifier and other circuitry. This can be achieved by decoupling the amplifier and its supply capacitor with a ferrite bead or inductor from the supply bus. Thereby, the high frequency current noise is forced to flow though the decoupling capacitor. Another possibility is to use Kelvin contact decoupling as proposed in [109]. The authors use additional supply and ground pads for their microchip to connect a floating decoupling capacitor. In this way, they divert the high frequency currents away from the supply bus using the bond-wire inductance of the microchip.

The output nodes of the amplifier are switched between the supply voltage and ground voltage. The output voltage can be regarded a rectangular (trapezoidal, due to finite transition speed) signal. Such a signal can be expressed as a Fourier expansion. The harmonic content of a rectangular signal with period T, amplitude H and duty-cycle D is given by [108]:

$$R(t) = \sum_{n=1}^{\infty} A_n \cos\left(\frac{2\pi n t}{T}\right) \tag{4.1}$$

$$A_n = 2\ H\ D\ \frac{sin(n\pi\ D)}{n\pi\ D}\ \frac{sin\left(\frac{n\pi t_{rise}}{T}\right)}{\frac{n\pi t_{rise}}{T}} \tag{4.2}$$

The rise time t_{rise} is the time needed for the voltage to transition from ground to supply potential. Equation (4.2) assumes that the rise time equals the fall time. The spectrum contains an infinite number of components, starting at the fundamental switching frequency. Fig. 4.1 shows a

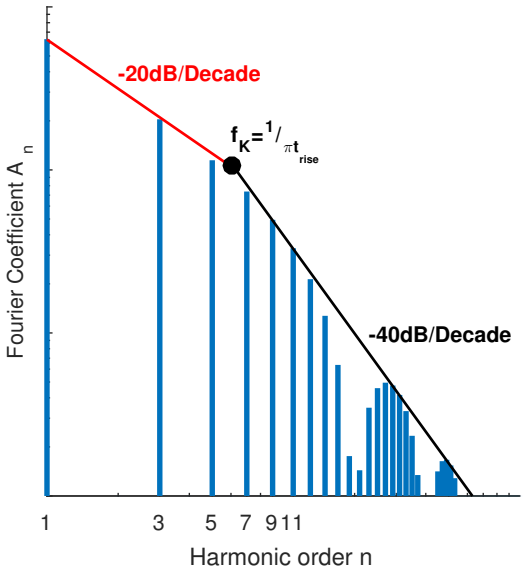


Figure 4.1.: Fourier coefficients of a trapezoidal signal with $D = 0.5$.

plot of the Fourier coefficients A_n for $D = 0.5$. Initially the coefficients decrease with 20 dB/Decade. At a certain point K, the coefficients start to fall with 40 dB/Decade. This point is at the frequency $f_K = 1/(\pi t_{rise})$ [108]. Slower switching transitions will reduce the generated high-frequency noise, as K shifts to lower frequency. Hence, the generated noise at higher frequency is mainly determined by the dV_{out}/dt. Slower switching is thus beneficial to reduce EMI. But as shown in chapter 3, this will increase the switching losses. Having a lower switching rate would also be beneficial, as this shifts the complete harmonic spectrum to lower frequency. But this will lead to lower audio-performance as explained in chapter 2. The generated high-frequency content of the output waveform is thus a compromise between efficiency and audio performance.

The actual spectrum of the output voltage slightly differs from eq. (4.1), due to the presence of dI/dt. The output current is rather constant due to the inductive load. But it is directed towards the positive or negative supply at each switching transition. This dI/dt in the supply lines can cause ringing due to parasitic inductance. Additionally, if the body diode of the switching transistors was conducting during the transition, the dI/dt in the body diode can lead to high dV_{out}/dt [110].

The generated noise can couple capacitively from the speaker lines to the surrounding environment. Additionally, the speaker lines can act as

electric antennas. In this way the voltage noise creates radiated emission. For Class-D amplifiers with two power-stages and a bridge tied load, the effects of common-mode (CM) voltage V_{CM} and differential mode (DM) voltage V_{DM} can be considered separately. Based on the voltage at the amplifier's output nodes V_A and V_B they can be derived as:

$$V_{CM} = \frac{V_A + V_B}{2} \tag{4.3}$$

$$V_{DM} = V_A - V_B \tag{4.4}$$

V_{DM} is present in opposite phase on the speaker lines. It excites the speaker and creates currents in opposite direction on the lines. V_{CM} is present with the same phase on the speaker lines. It does not transfer power to the speaker and creates a common-mode current on the speaker lines.

Typically, the speaker lines are close to each other. On the PCB, parallel traces are used. In a cable harness, often twisted pair cables can be found. Such speaker lines significantly reduce the EMI generated from V_{DM}. The capacitively coupled DM voltage noise from one speaker line is greatly compensated by the coupling form the second line. Radiation is completely inhibited in the best case, as the created electric fields cancel out in the far field. Unfortunately, the situation is different for the CM voltage. The capacitively coupled noise from each speaker line has the same phase. Thereby it is not canceled out. Moreover, the speaker lines can be seen as a single monopole antenna for V_{CM} that will created radiated emission.

In the course of this research, the created CM voltages of traditional filtered and filterless Class-D amplifiers have been analyzed [111]. Class-D amplifiers that need an output filter typically use so-called AD modulation as explained in chapter 2.1. Fig. 4.2 shows the output waveforms of such an amplifier and the created CM voltage. The waveforms are shown for zero and non-zero audio output. Ideally, the two outputs switch exactly in opposite phase and no CM voltage is created. In reality, the voltage transitions will happen at slightly different points in time and with different slew-rate due to circuit mismatch. Thereby short CM spurs will occur.

Two filterless modulation schemes were analyzed. First, Fig. 4.3 shows the popular BD modulation. At zero audio output, no differential voltage is created. Therefore no output filter is needed. However, the waveform

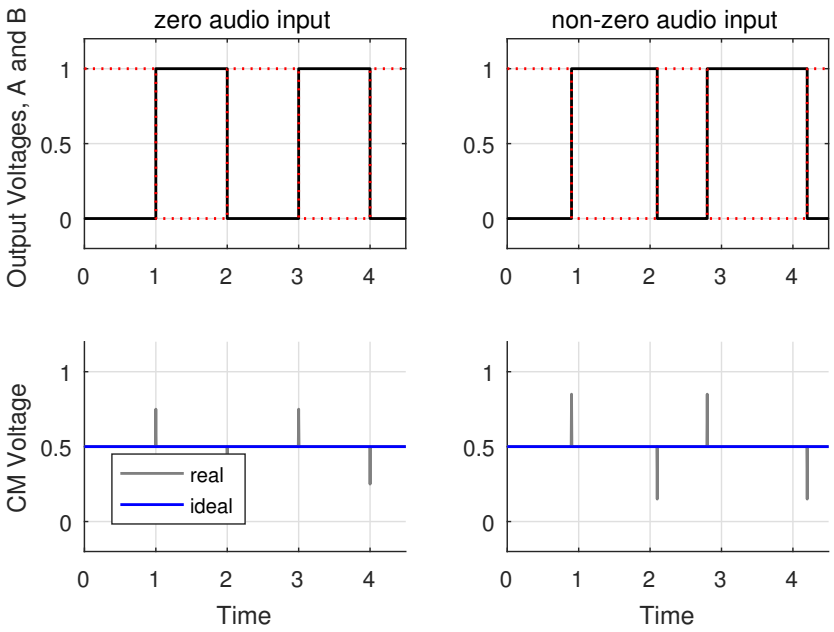


Figure 4.2.: Output waveforms of the AD modulation for filtered amplifiers, and generated CM voltage.

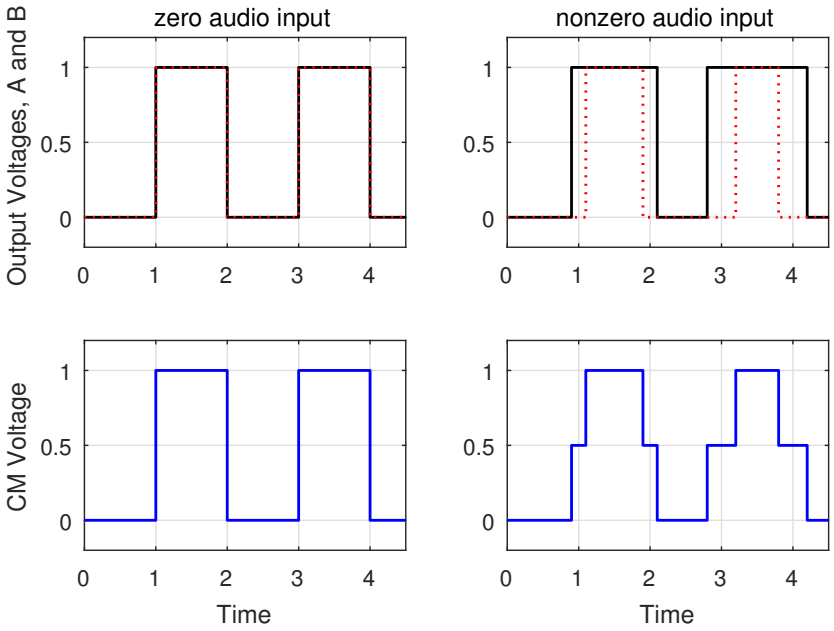


Figure 4.3.: Output waveforms of the BD modulation for filterless amplifiers, and generated CM voltage.

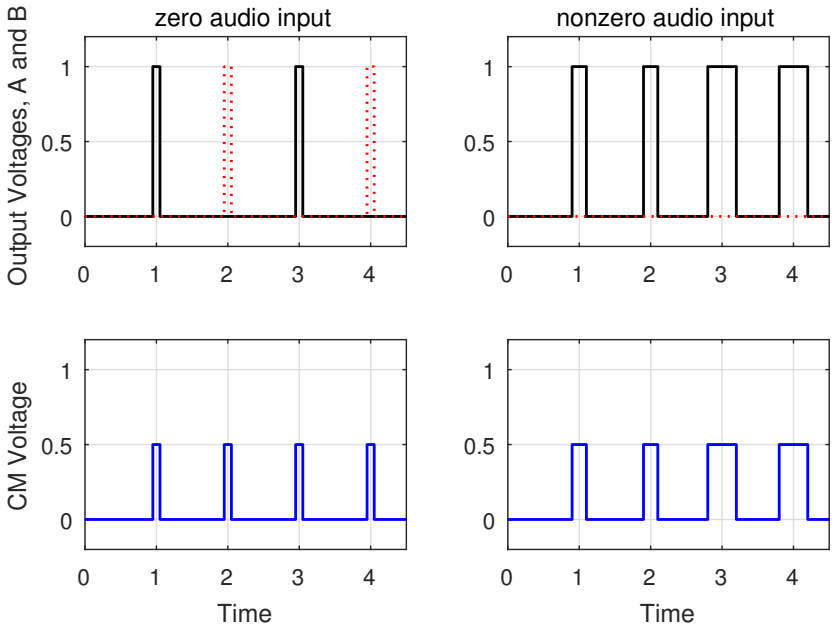


Figure 4.4.: Output waveforms of ternary modulation [37, 112] for filterless amplifiers, and generated CM voltage.

contains a large common-mode component. The common-mode voltage is inherently created by the modulation scheme. At zero audio output the CM voltage is a rectangular signal with a high level equal to the supply voltage. V_{CM} has a fundamental frequency equal to the switching frequency of the outputs. Next, Fig. 4.4 shows another filterless modulation scheme. In the following it will be called ternary modulation and was proposed in [37, 112]. At zero audio output, only short differential pulses are created. This does not lead to significant ripple current in the speaker, enabling filterless operation. The scheme permits only one output to have a high potential at a time. This reduces the CM voltage amplitude by half compared to BD modulation. In contrast, the fundamental frequency of the V_{CM} is doubled for the same switching frequency.
In [113], a filterless modulation scheme was proposed, which significantly reduces CM voltage on the speaker lines. Unfortunately, the scheme has many drawbacks. It needs six power-switches instead of the four typically used in other schemes. This increases the silicon area and the idle current consumption by up to 50 %. These switches are required to operate with a small amount of negative deadtime. Such switching overlap causes shoot-trough current. Thus, significant challenges in the integrated implementation have to be faced to make the design robust

against process, supply and temperature variations. Moreover, the power-stage needs a constant biasing. This causes an additional quiescent current, similar to a Class-AB amplifier. Thus the scheme cannot compete with other schemes in terms of power efficiency and production costs. To the author's knowledge, there is currently no commercial nor further scientific implementation of this scheme to an integrated, filterless, audio Class-D available. The scheme is thus not considered in this work.

The common-mode voltage created by the traditional filtered amplifiers is a result of non-idle circuit implementation. In contrast, the filterless amplifiers inherently create a common-mode signal. This is a direct result of the filterless operation, which requires a zero differential signal at idle. The situation is further worsened: The common-mode voltage in filterless amplifiers is not attenuated by an output filter. It is directly applied to the speaker lines. One can thus conclude, that filterless Class-D amplifiers are prone to creating EMI. A way to reduce the created interference is to place the amplifier as close to the speaker as possible. In this way, the created radiated emission are reduced, because the electrical length of the speaker lines is shorter. Moreover, the speaker lines should be kept away from sensitive circuitry to minimize capacitive coupling. Some amplifier manufacturers [114] recommend to use ferrite-bead based output filters. However, in the mobile market, stringent space requirements often disqualify such filters. It is thus plausible to conclude, that filterless Class-D amplifiers can be a potent source of electromagnetic interference. In many applications, the generated common-mode voltage on the output pins is the main origin of this created interference.

4.2. Emission measurement of integrated Class-D amplifiers

Manufacturers of electronic devices are anxious to fulfill legal emission regulations and to ensure the functional integrity of the different components used in their systems. It is natural, that device manufacturers are very interested in using the components which create the lowest emission. This will help to reduce costs and space needed for filtering and decoupling measures. Moreover it helps to pass the legal emission limits without design iterations.

In the ideal case, all datasheets of Class-D amplifier ICs would list measurement results, which quantify the ability of an IC to act as an emission source. The results should be comparable, as it already is for audio performance or power efficiency. In that way, the system manufacturers could compare the different ICs. Such a measured *emission ability* could be the third important performance parameter to select a Class-D amplifier for a certain application.

Currently, datasheets sometimes show emission measurement results. In [15] radiated emission measurments according to FCC Class-B [115] are plotted for the IC. The datasheet [16] of another manufacturer shows radiated emission measurements according to EN55022 [116]. In the datasheet of [39] it says "..the device has shown to be below the compliance limits of FCC", suggesting emission measurements according to FCC Class-B have been carried out. It should be clarified, that these measurement setups are defined to characterize complete electronic systems. In these measurements, the electronic device is placed in a certain distance to an antenna. Then the radiated emission of the device are measured at the antenna. It can only be reckoned, that the presented measurements are carried out with the IC soldered to a certain PCB and with some kind of housing. From chapter 4.1 it is clear, that: Whether the Class-D amplifier's noise is radiated into the environment mainly depends on system-level measures. Thus, the presented measurements cannot be used to compare different ICs. The measurements show, that the IC can be used to build a system, that can pass FCC or EN emission limits with appropriate filtering, decoupling measures and housing.

Some datasheets also show different measurements. [117] shows a graph named "Wideband Output Spectrum". The graph obviously shows some kind of conducted spectrum measurement without further explanation. A variety of different methods to quantify EMI of integrated Class-D amplifiers can be found in scientific publications [19, 20, 21, 12, 13, 18]. The shown results range from spectrum plots not stating any measurement standard; to conducted measurement setups on the supply lines according to system-level standards (EN55022); radiated emission measurements according to EN55022 and even magnetic field measurements above the chip package. All of the reported measurements may have their justification, but do not allow comparison between different works.

4.2.1. An IC-level emission measurement setup

Electromagnetic emission measurement setups at IC-level have been developed in the last years. Several of these measurement setups have been standardized in the IEC61967 standard. These setups define operation conditions and standardized measurement environments for the characterization of IC. The setups thereby model a realistic operation environment for the tested IC, and try to minimize external factors influencing the measurement result. In this way, measured results are comparable and repeatable among different ICs. Especially in the automotive industry, it has become a standard procedure to evaluate the emission of IC in this way [118].

Yet, to the author's knowledge, there are currently no guidelines or examples on how to apply IC-level measurements to Class-D audio amplifiers. In the course of this research, a new proposal for a measurement setup was worked out. The proposed IC-level measurement setup is ideally suited to compare integrated Class-D amplifiers. It allows to quantify the ability of different Class-D to act as noise sources.

The proposed measurement setup is based on the 150 Ω direct coupling method defined in the IEC61967-4 standard. The 150 Ω method assumes that an IC will not create EMI by its own, but will act as a noise source. The generated noise at the pins of an IC will couple to the environment via board traces and cable harnesses. This assumption is perfectly in line with the analysis of section 4.1 for integrated Class-D amplifiers. The 150 Ω setup therefore measures the conducted voltage noise at the output pins of the IC. In order to imitate a typical antenna impedance of a cable harness, the voltage noise is measured with a network having a 150 Ω input impedance in the measurement bandwidth. Hence the name of the measurement setup. The measurement has to be carried out with an EMI test-receiver according to CISPR16-1-1 [119]. These test-receivers have well defined spectral characteristics. EMI-test receivers apply a certain weighting to the measured signal and are also used in system-level emission measurements.

Fig. 4.5 shows an exemplary application of the 150 Ω method to an IC. An impedance matching network is connected to an output pin of the IC. The network consists of a series capacitor to block DC and low-frequency signals. At higher frequencies, the resistors dominate the network impedance. Together with the 50 Ω input impedance of the test-receiver, the network

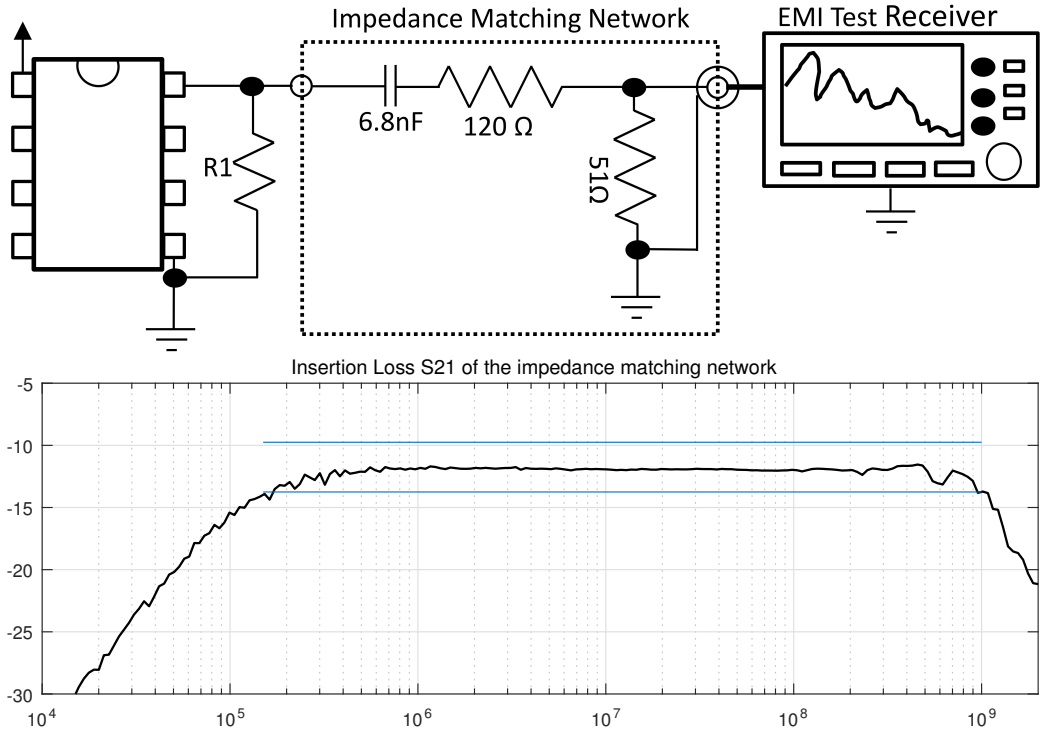


Figure 4.5.: 150 Ω direct coupling measurement according to IEC61967-4. Resistor R1 is an optional pull-up or pull-down depending on application. Below the insertion loss of a typical impedance matching network is shown.

has an input impedance of about 150 Ω from 150 kHz to 1 GHz. The IEC61967-4 standard gives exact guidelines on how to construct this network. Additionally, tolerances for the impedance and the input-output voltage relation are specified. Fig. 4.5 also shows the measured insertion loss $S21$ in a 50 Ω system and the tolerance boarders specified in the standard.

In amendment 1 of IEC61967-4 [120] a 150 Ω network for differential data-lines is defined. It is intended to measure the common-mode noise on symmetric data-lines. Fig. 4.6 shows the proposed measurement setup. The common-mode voltage noise is sensed at the output nodes. The network has an input impedance of approximately 150 Ω for high-frequency common-mode noise. The standard exactly specifies the accuracy and matching requirements of the different components to ensure reproducible results.

It was already outlined that the common-mode output noise on the speaker lines will have the dominant impact on the total EMI. Therefore the setup for differential data lines is the bases for the new Class-D measurement setup. The output pins of the Class-D amplifier are sensed with the impedance matching network to measure the generated common-mode noise. Filterless amplifiers need a load similar to a loudspeaker for proper operation. The standard [120] says "The resistor R4 represents a termination resistor which may be needed to operate the DUT properly". In our work [121, 111] we propose to use a dummy speaker load as used for efficiency measurements to imitate a realistic load. The connection of the matching network to the output pin must be realized with wiring that has a line impedance of 150 Ω. This avoids reflections. Alternatively, unmatched, but very short wiring can be used. It should be significantly shorter than the wavelength of signals at the upper border of the measurement bandwidth.

Fig. 4.7 shows a picture of the proposed measurement applied to an integrated filterless Class-D amplifier. The IC is soldered to a printed-circuit board containing the 150 Ω network. The standard demands, that a solid ground-plane is placed below the impedance matching network. Thus, at least a two layer circuit board is needed. The connection of the IC to the network should have a common-mode characteristic impedance of 150 Ω to avoid reflections. The connection is made with two parallel traces. It is modeled as an edge coupled microstrip-line. In this way, width and

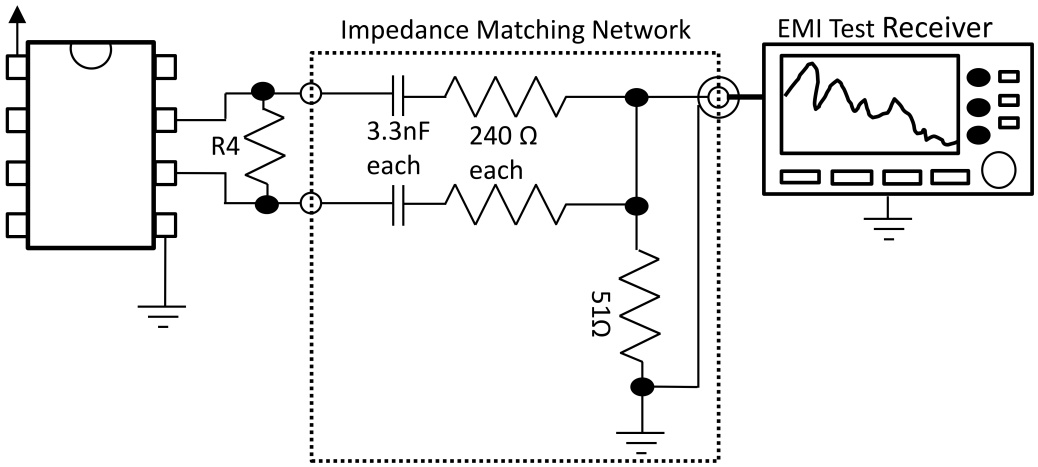


Figure 4.6.: 150 Ω direct coupling measurement on differential data lines according to IEC61967-4-1. Resistor R4 is an optional termination resistor.

spacing of the traces for a given impedance can be calculated using formulas from IPC-2141A [122]. In the measurement shown in the picture, the needed width and spacing of the copper traces could not be implemented. This is due to pin-spacing of the IC package and large current density in the traces. The calculated common-mode characteristic impedance of the used traces is only 50 Ω. However, the spacing from package to network is 8 mm, which is is smaller than 1/20 of the wavelength at the upper boarder of the measurement bandwidth (1 GHz). Thus, reflections will not significantly impact the measurement results. A dummy load as proposed in section 3.1 is applied to the speaker with a short cable. The inductance of the speaker cable can be neglected, as it is series with the large load inductance.

IEC-61967-1 [123] demands that emission measurements are carried out at typical operation conditions. This means that Class-D measurements should be carried out at room temperature, with an appropriate load and input signal. In the case of Class-D amplifiers, the created emission may significantly depend on the audio signal. The emission may be very different at zero input signal and at full scale input signal. One could thus use a test-signal that imitates typical audio content. This has as well been proposed for efficiency measurements [100, 101]. Still, efficiency measurements are generally carried out with a 1 kHz sinusoidal input signal for simplicity. For emission measurement, it is also recommended to use a 1 kHz sinusoidal input signal to keep the measurement setup

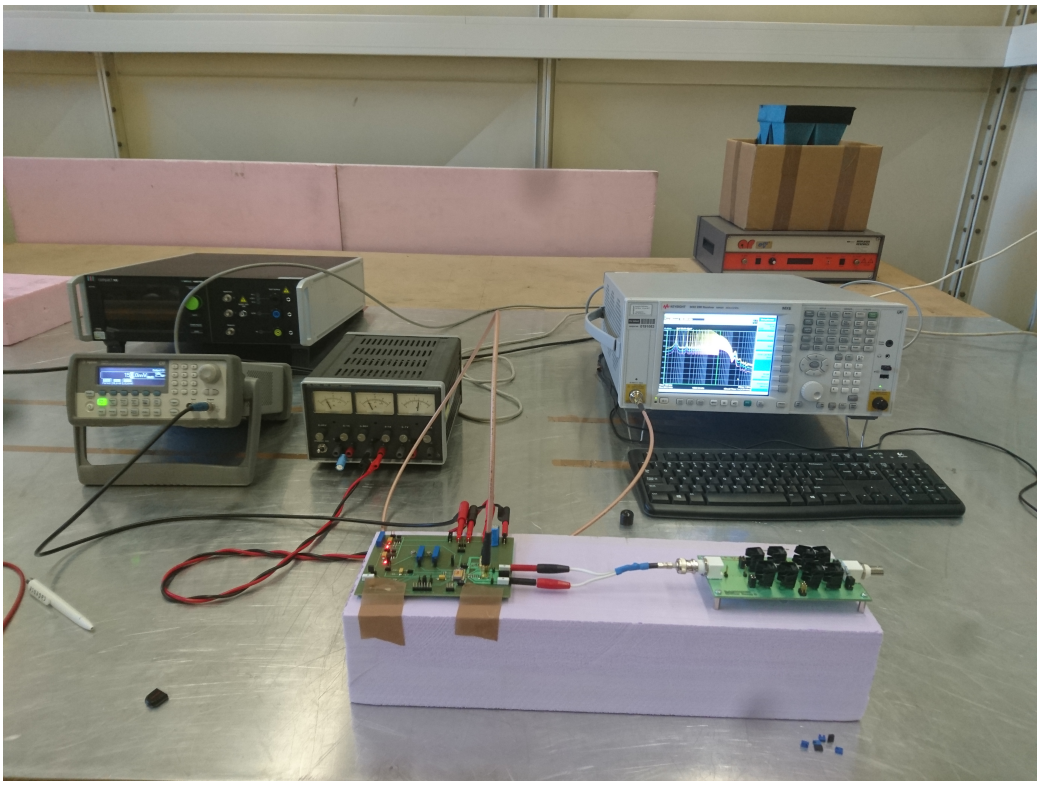


Figure 4.7.: Photograph of the proposed measurement setup applied to an integrated amplifier.

simple. The amplitude of the signal is adjusted to be close to the input full scale of the amplifier. Additionally, a second measurement at zero input signal can be carried out for completeness. Class-D amplifiers often need a supply decoupling capacitor for proper operation. IEC-61967-1 specifies to use a decoupling capacitor according to the IC datasheet.

The proposed measurement method is easy to apply, as only conducted noise is measured. Therefore, complicated and error-prone radiated emission measurements are avoided. It is simple, as only a couple of passive components are involved. This allows high reproducibility. The matching network can be calibrated and verified easily by measuring the insertion loss. The measurement is suitable for a wide frequency range of 150 kHz to 1 GHz. This covers the frequency ranges typically tested for legal compliance according to EN/FCC regulations. The measurement allows comparison of integrated Class-D amplifiers, nearly independent of the used PCB, device housing, and other factors. The proposed measurement setup gives valuable insight into noise created by Class-D amplifier ICs and can help system designers to select the optimal Class-D IC for their application.

Exemplary IC-Level measurements

In the course of this research traditional filtered and filterless Class-D amplifiers have been compared with the above proposed measurement setup [111]. Several commercial amplifiers were measured. These devices were all selected to drive up to 8.5 W into an 8 Ω speaker. For the traditional filtered amplifier, the output filter was removed. This results in larger ripple current in the load, but leads to more comparable measurement results with the filterless amplifiers.

Fig 4.8 shows the measured common-mode voltage noise on the output pins of the amplifiers. Three devices were measured:
An AD-modulated and filtered amplifier with a switching frequency of 300 kHz;
A filterless amplifier with BD modulation and a switching frequency of 400 kHz;
And a filterless amplifier with ternary modulation [37, 112] and a switching frequency of 300 kHz. The measurement is carried out as described above. The amplifiers are excited with a sinusoidal input signal and drive about 8 W into the load. This load is the speaker dummy already described

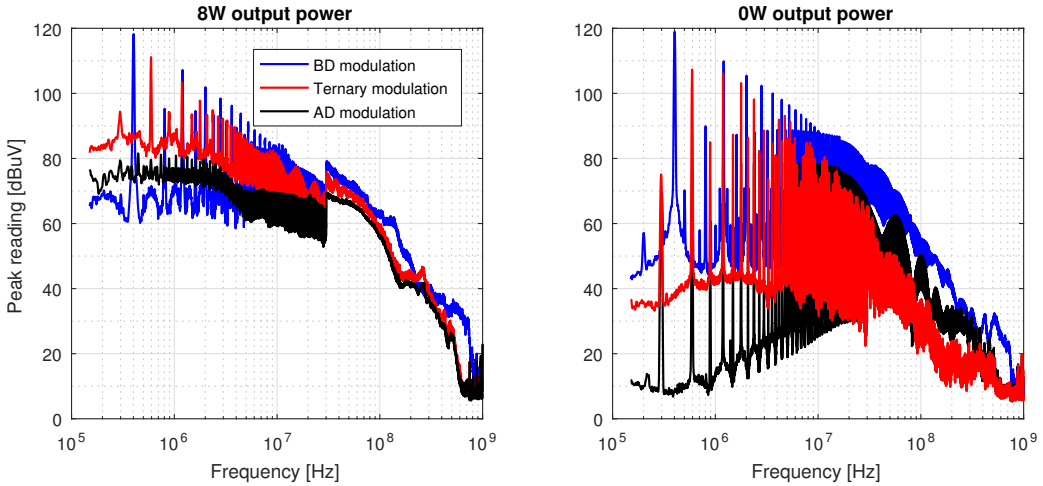


Figure 4.8.: Measurment of the CM output voltage of three commercial Class-D amplifiers.

in chapter 3.1. The right side of Fig. 4.8 shows the measurement result with zero audio input. The created emission below 30 MHz largely depend on the used modulation scheme. Obviously, the two filterless amplifiers create significantly larger common-mode voltage noise, which is 30 dB to 40 dB larger at the first switching harmonic. This is in line with the graphical analysis of the modulation schemes from chapter 4.1. In addition, these amplifiers are used without output filtering. Thus, one can conclude that filterless amplifiers have a higher risk to create EMI. Above 100 MHz the situation is different. Additionally to the modulation scheme, also the transition speed influences the generated noise (comp. to eq. (4.1)). Hence at higher frequencies, the implementation of the power-stage impacts the generated emission.

4.3. Simulation of EMC measurements

EMC measurements can only be carried out after IC manufacturing. Unfortunately, manufacturing is the last step in the design process of integrated circuits. Therefore, unexpected high emission discovered during these measurements, will lead to a costly and time consuming design iteration. Circuit designers therefore need tools to evaluate the EMC performance already before production.

In the last section, a simple and reliable emission measurement setup for filterless Class-D amplifiers was proposed. It is ideally suited to compare different ICs. It can be used to benchmark one's own IC to a competitor on the market. In this section, a simulation model of this emission measurement setup is derived. Using this versatile model, the designer of an integrated Class-D amplifier can simulate the conducted emission of his circuit. The tool can be used to compare the emission of a design to competitors on the market, without having to fabricate the microchip. Moreover, circuit level measures to reduce the emission can be evaluated in a fast and inexpensive way.

In literature, two common ways of modeling emission measurements can be found: In the works of Mrad et al. [124][125, 126] or Onikienko, Pilinsky, and Rodionova [14][127] frequency domain approaches for simulation are presented. The idea is to measure the parasitic components on the circuit board and build an equivalent impedance model of the measurement setup. The Class-D amplifier output is modeled with an AC source. Then a frequency domain analysis is carried out. The amplifier is thereby replaced by the AC voltage source that represents the spectrum of its output voltage or current. The advantage of this method is that frequency domain analysis significantly reduce computation time. The disadvantage is that the designer needs to create a simplified AC model of the amplifier. A designer, experienced with EMI topics is needed, otherwise relevant properties of the amplifier may not be modeled. Moreover, the frequency domain analysis is not suited for circuits with slowly varying transient behavior.

In the works of Li et al. [128] or Adami et al. [12], transient approaches are presented. Thus the measurement setup and the amplifier are modeled with electric components. The simulation is done in transient domain using Spice-like simulators. This approach requires larger computation effort, but is feasible on modern computer hardware. The big advantage of these methods is that integrated circuits are designed and verified in Spice-like environments. Thus, the method is highly compatible to the standard design flow of integrated circuits.

The modeling of IC-level emission measurements according to IEC61967-4 for transient simulations was already shown in [22]. However, the simulated results could not be directly matched to measurement results. The reason is that not only the the measurement setup, but also the behavior of the measurement equipment must be taken into account. In order

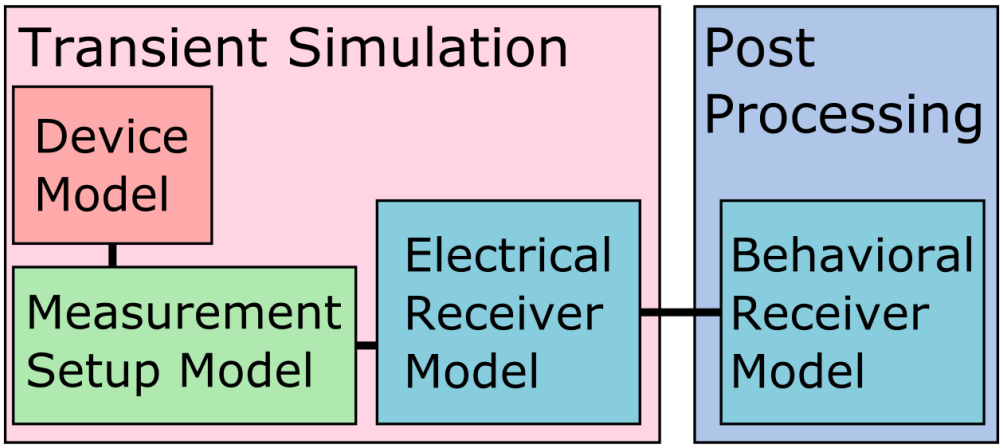


Figure 4.9.: Modeling approach for the IC-level measurement.

to estimate the measured emission already during design phase, accurate models of the Class-D amplifier, the measurement setup and the measurement equipment are needed.

The approach used in this work is shown in Fig. 4.9. At first, a time-domain simulation is carried out. The simulation contains a model of the integrated circuit, a model of the measurement setup as suggest in [22], and an electrical model of the EMI test-receiver. Once the transient signals are obtained, a post processing is applied. In the post processing, the signals are evaluated and weighted to imitate the behavior of the measurement receiver.

A big advantage of this separation is, that the time-domain simulation can be carried out at various abstraction levels. For instance, at the beginning of the product development, system level simulations at a high level of abstraction (e.g. using *Matlab Simulink* or similar) could be conducted for early design decisions. At a later stage in the design process, more accurate emission estimations can be conducted with transient, transistor level simulations. In this way, specified emission targets can be verified throughout the different design stages. In the following, the proposed approach is described for simulations at transistor level.

A similar approach of transient simulation and post-processing is presented in [23]. However, the presented approach is intended for system level measurements. The post processing differs from the behavior of

standard compliant measurement equipment. Hence the acquired simulation results will differ from measurement results. In this work, the transient simulation of an IC-level measurement is proposed. To analyze the simulation output, an extensive model of the measurement equipment was implemented. The model allows a standard-conform spectral representation of the results. The most widely used weighting detectors are modeled. This post processing model was published [129] and allows to directly compare the simulation results to measurement values.

4.3.1. Modeling of of the integrated amplifier, modeling of the measurement setup and transient simulation

The emission of Class-D amplifiers is mainly created by the switching power-stage. The implementation of this power-stage is a classic analog circuit design task. Analog design flows are based on schematic entry and Spice-like transistor-level simulation. Fig. 4.10 shows an overview of the proposed simulation model. The schematic representation of the power-stage is combined with several other schematic blocks. These other blocks model the environment of the silicon die and the measurement setup. During the design process, the additional blocks can simply be added to already existing simulation test-benches. Thereby the created emission can be simulated with little additional effort for the circuit designer. The approach is thus highly compatible to the standard analog design flow.

The schematic representation of the power-stage is composed of device models provided by the foundry. These device models are typically very accurate models describing all behavior frequently needed for circuit design. However, not all physical behavior can be modeled easily, and most models are a trade-off between accuracy and computation time. Physical behavior needed for accurate emission simulation, is sometimes not included in device models from foundries, as it is of minor relevance for circuit design. For instance, the behavior of transistors' body-diode is sometimes not accurately modeled. Especially, the reverse recovery behavior of this diode can be a main source of EMI in Class-D amplifiers [83]. A critical examination of the models provided by the foundry is thus necessary.

In this work, the silicon die is wirebond to the leadframe and packaged. The leadframe is soldered to the printed circuit board and evaluated

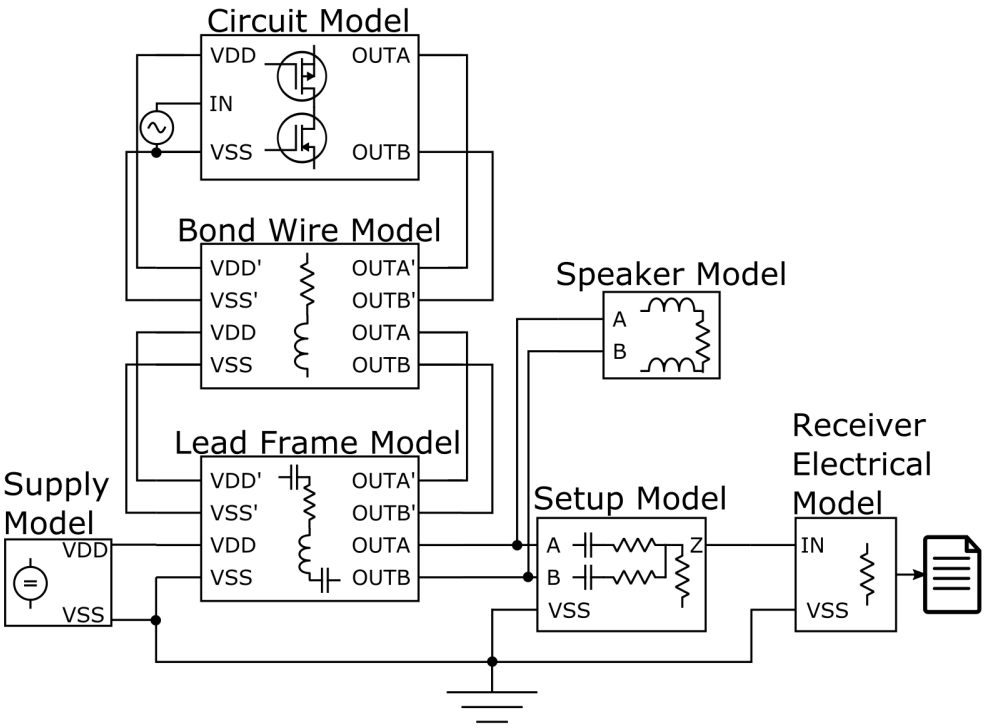


Figure 4.10.: Transistor-level transient simulation of the measurement setup

with the proposed 150 Ω measurement setup. All these additional blocks need to be modeled as lumped-element circuits for transient simulation. Lumped element modeling is one way of modeling an electric system. Dedicated electric devices and physical electric transmission paths are thereby modeled using resistors, capacitors, inductors and mutual coupling to other inductors. A prerequisite is that the modeled physical objects are significantly smaller than the wavelengths of the signals to be simulated. Larger objects have to be divided into a several small objects to generate distributed element models. Inside the package of the microchip, all objects are typically electrically small for the emission measurement bandwidth. Outside the package, most board traces of the measurement setup are either controlled impedance lines, or also have very small dimensions. In the first case, a transmission line model can be used, which is a distributed element model.

The complexity of the model closely relates to the bandwidth of the considered signal. Models that have to be accurate over a large bandwidth need more and more components. Naturally, this will increase the computation time for simulation. When building the lumped-element blocks, some experience is needed to add only the elements, which will play a dominant role, to save simulation time. However, many of the needed blocks are reused for each integrated design. Thus, they have to be created only once by an experienced EMC expert. During the design, they can then be added to the simulation similar to IP-blocks.

The supply network, is typically dominated by the decoupling capacitors. On-chip decoupling is considered in the circuit model. External decoupling capacitors can be modeled with an electrical lumped-element model as proposed in [130]. The element values can be found in capacitor datasheets.

The speaker (speaker-dummy) can be measured and characterized for modeling. Fig. 3.3 in chapter 3.1 shows the used model for the speaker-dummy. The electrical characteristics of the measurement setup are defined in the standard and are simple to model [22].

The parasitics of the leadframe are often characterized and modeled by the lead-frame manufacturer. The bondwires are individual to each packaging variant, and have to be re-modeled for each design. They might not be determined at the beginning of design process. But towards tape-out of the microchip, the properties (material, diameter) and physical location should be roughly known. At this stage, the bondwires can be modeled

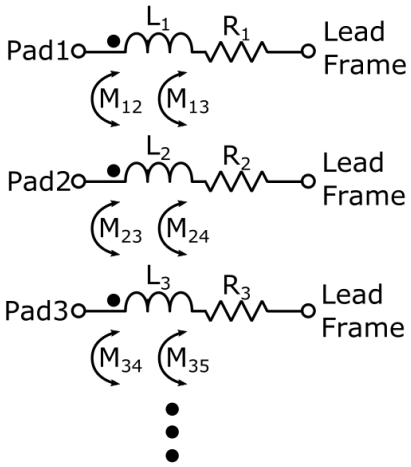


Figure 4.11.: Model of the bond-wires. Three bond-wires are shown. Resistance, self inductance and mutual inductance to the adjacent and first non-adjacent wire is considered.

as lumped element blocks. One way to model the bond wires is shown in figure 4.11. The model includes the resistance of the bond-wire, its self inductance and also mutual inductance to the adjacent and first, non-adjacent wires. The resistance can be calculated from the length, diameter and material of the wire. The self inductance can be estimated from the formula in [131] for straight conductors. If the angle between the bond-wires is close to zero for the used leadframe, the mutual inductance can be modeled by parallel straight, round conductors. The value can then be estimated by the formula in [131].

The electrical model of the EMI test receiver represents the receiver input impedance. It also realizes the data transfer from the transient simulation to the post-processing. The input impedance of 50 Ω [119] is modeled with an ideal resistor. The data transfer needs to be discussed in more detail. State-of-art transient simulators use variable step solvers. The simulation works with fine timesteps in periods where the circuit shows large dynamics, and coarse timesteps otherwise. In this way, computation effort and memory requirements to store the transient data is reduced. Unfortunately, signal processing on such non-equidistant sampled data is difficult.

The post processing in this work is intended to analyze emission in the range of 150 kHz-1 GHz. It needs uniformly sampled data at a sample

rate above the Nyquiste rate. A common approach, also used in [24], is to apply resampling, before signal processing of the simulation data. The transient simulation data is first upsampled to the highest frequency (smallest timestep) present in the simulation output. Then, the signal is downsampled to the target sample rate for signal processing. The advantage of this method is, that the transient simulation is not affected and can be run at full speed. The method also has some disadvantages. First, the memory needed to store the upsampled signal can be enormous. Especially in switching circuits, the smallest timesteps can be in the fs range. In this case the upsampling involves significant algorithmic and computational effort. Additionally, to avoid aliasing and imaging artifacts, appropriate filtering is needed in the resampling process. Such artifacts can lead to erroneous components in the simulated emission spectra. Due to to the large emission measurement bandwidth (150 kHz-1 GHz), the emission spectrum can have a dynamic range of more than 100 dB [132]. Thus, the required filters have very demanding specifications. Finally, resampling introduces numerical errors. In [24] this resampling approach is used, but the actual implementation is not explained. The *Cadence* design environment allows to directly export uniformly sampled simulation data. However, it is not documented how or if aliasing is avoided.

In this work, a different approach was considered. The variable step solver is used, but certain equidistant timesteps are enforced. The simulation output is saved only at these timesteps. In this way uniformly sampled data is generated. Resampling is not needed, which reduces memory consumption and computation time of the post-processing. Moreover, numerical errors are reduced, because the transient circuit simulator directly calculates the needed values. Care must be taken, that only relevant signals are saved, because the memory consumption is larger than before. Additionally, aliasing needs to be considered.
The model is implemented using a *VerilogA* block. VerilogA blocks can be directly added to analog transistor-level simulations in the *Cadence Spectre*® circuit simulator. The voltage current relation at the input port is implemented using Ohm's low to model the receiver input impedance. The block incorporates a low-pass filter and saves the low-passed data to a file at a specified sampling rate. In this way, the VerilogA block implicitly forces the required timesteps. The sampling rate is 4 GHz. To reduce aliasing, signal components above 3 GHz need to be attenuated by the low-pass filter. The filter specifications are very relaxed. A high stopband attenuation is not needed, because in many practical circuits, signals below

1 GHz have a much larger amplitude than signals above 3 GHz. Therefore a cascade of three first order low-pass filters was implemented which have a total attenuation of 15 dB at 3 GHz and 36 dB at 4 GHz. The block can simply be added to a schematic driven simulation. It generates a file of uniformly sampled output output values, ready for post-processing.

As in the measurement, two simulations should be carried out. First an input signal is applied to the power-stage, creating a 1 kHz output signal with an amplitude close to the full scale of the amplifier. Then, the simulation is carried out with a zero input signal. If the power-stage is to be simulated alone, then a PWM input signal is needed. It is recommended to generate this signal in advance, for instance by using the system-level model of the designed Class-D amplifier. For the first simulation, a PWM signal encoding a sinusoid is needed. For the second simulation at zero input signal, the offset voltages of the modulator can be considered. The PWM input signal then contains a small DC component. The generated PWM waveform can then be written into a file from which it is read during transient simulation. Spice-like simulators often offer a voltage source that can generate piece-wise linear voltages. Such source are very well suited to generate the control-signals for the power-stage.

4.3.2. Modeling of the measurement equipment

The post-processing models the measurement equipment behavior. We published the model already in [129], in the following it be shortly summarized.

Emission measurements are carried out using an EMI test-receiver according to CISPR16-1-1 [119]. Traditionally, these receivers were implemented as superheterodyne receiver. A simplified block diagram is shown in Fig. 4.12. The receiver consists of a mixer with a tuneable oscillator. The mixer transfers the input signal to an intermediate frequency (IF). Then a bandpass-filter is used to select a certain measurement bandwidth. Finally, an envelope detector and a weighting detector are used to quantify the signal. Several weighting detectors are defined in CISPR16-1-1, which evaluate the signal for a certain measurement time. The measurement time is called dwell-time and depends on the internal cycling-time of the measured device and the settling time of the used weighting detector. This measurement time has to cover at least several operation cycles of the

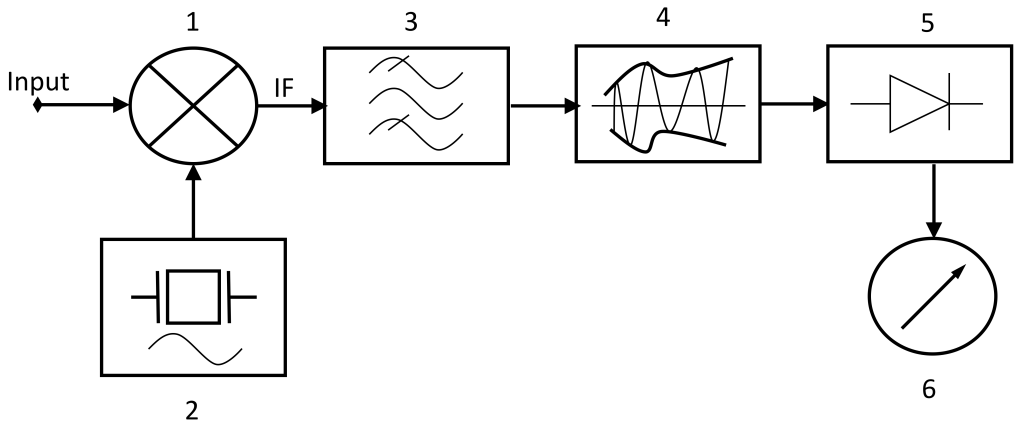


Figure 4.12.: Simplified block diagram of an EMI test-receiver: 1 Mixer; 2 Tuneable oscillator; 3 IF bandpass filter; 4 Envelope detector; 5 Weighting detectors; 6 Meter.

measured device. For instance, a Class-D amplifier which is excited with a 1 kHz input signal should be measured with a dwell-time of several ms.

To measure a large frequency range, a measurement sweep is executed. Thereby the local oscillator's frequency is step wise increased. At each frequency step, the measurement is carried out for the needed dwell time. In civil applications, often CISPR Band-B and Band-C/D are measured. The settings of the EMI receiver in these frequency bands are listed in table 4.1. The property *Resolution-bandwidth (RBW)* characterizes the 6 dB-bandwidth of the bandpass-filter. When performing a measurement sweep, a *frequency-step-size* of approximately $\frac{RBW}{2}$ has to be used. To measure from 150 kHz-1 GHz, approximately 23000 measurements have to be performed. This can take several hours depending on the used dwell time.

Table 4.1.: Setup of the EMI test-receiver

	Band-B	Band-C/D
Frequency range	150 kHz - 30 MHz	30 MHz -1 GHz
Resolution-bandwith	9 kHz	120 kHz

It can be concluded, that an EMI test-receiver scans the spectrum of a signal in stepwise manner. The spectral characteristics are very well de-

fined. At each frequency step, the spectral content is analyzed for a certain time. The amplitude change at each spectral point over time is evaluated using a weighting detector. This behavior cannot be modeled using a simple Fourier transform of a transient signal. Nevertheless, it seems to be common practice among circuit designers to evaluate emission using a single Fourier analysis [22, 19, 12, 124, 133]. This can lead to significant deviations between emission estimates and standard-conform measurements. Not only absolute deviations are likely. Also relative emission differences between two circuit modes may come out different between simulation and measurement. This is especially problematic for designers trying to implement circuit level emission reduction methods. A certain reduction seen in simulation may turn out to be non-measurable. More sophisticated simulation models are needed for correct emission estimates during design time. Unfortunately, modeling the superheterodyne receiver can be a cumbersome task.

In order to reduce measurement time, so called time-domain receivers have been developed [134, 135]. They use a sampling analog to digital converter in combination with a post processing based on Joint-Time-Frequency algorithms (e.g. Short-Time-Fourier-Transform). These receivers measure the complete signal in time domain. Thereby the post processing can evaluate all frequency points in parallel. In theory, this reduces the total measurement time from several hours to the time needed for a single frequency step. The used post-processing algorithms are implemented to imitate the behavior of the traditional, superheterodyne receivers and ideally provide the same measurement reading.

In many cases, only some milliseconds of simulation output is available to verify integrated designs. Therefore, in this work, a model of an EMI test-receiver was implemented which is based on such a time-domain structure. The time-domain structure is ideally suited, as the simulation generates a high resolution transient signal. The model only needs to implement the digital signal-processing algorithm used in the receivers. A similar approach was already published in [23], but cannot be considered a standard-conform implementation. The work of [24] describes a more conform model, but implements only a single weighting filter. In this work, a post-processing algorithm of this simulation data was implemented using the Short-Time-Fourier-Transform (STFT) and the most commonly used weighting filters are modeled. The accuracy of the model has been shown in several publications [121, 129] and extensive test-setups used in this project. The model is implemented having a simple usage in mind.

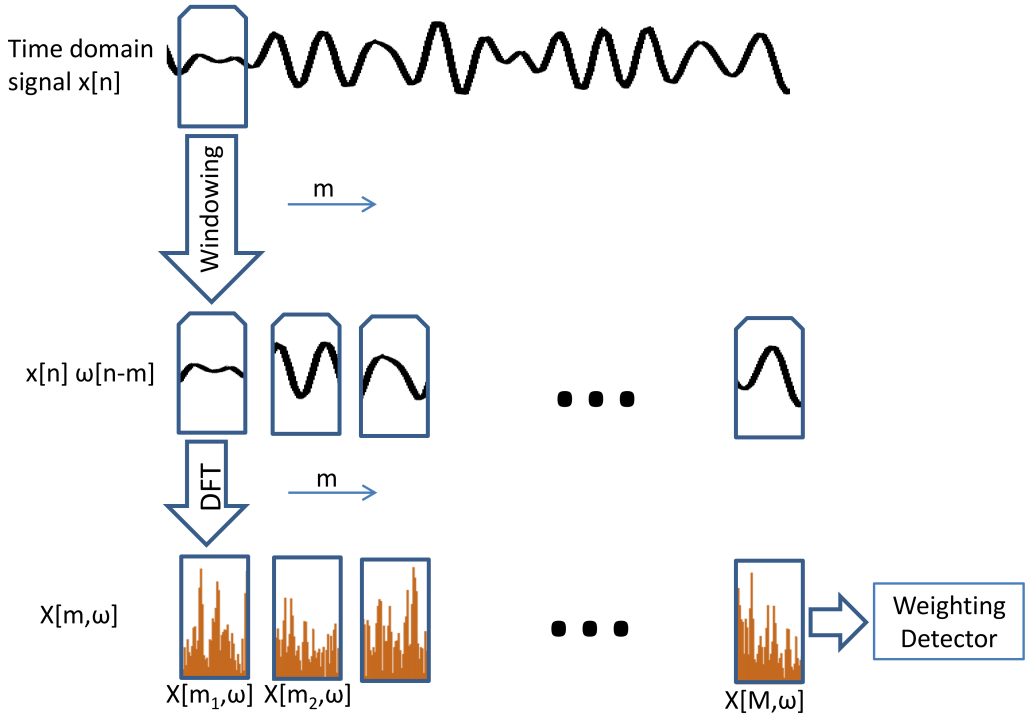


Figure 4.13.: Implementation of the STFT algorithm.

Ideally, the circuit designer should be able to use the model without being an EMC expert. The results of the model can be directly compared to measurement results with a standard-compliant measurement receiver. The implemented model can also be used to turn an oscilloscope into an EMI test-receiver for pre-complince measurements as demonstrated in my work of [129].

The time discrete STFT is defined in eq. (4.5) and the implementation is shown graphically in Fig. 4.13.

$$X(m,\omega) = \sum_{n=-\infty}^{\infty} x[n]\ \omega[n-m]\ e^{-j\,\omega\,n} \tag{4.5}$$

The input signal $x[n]$ is the uniformly sampled output of the transient simulation. First, $x[n]$ is multiplied with an appropriate window function $\omega[n]$ and then Fourier transformed. The window function is non-zero only for a short period of time and is moved along the input signal with a temporal offset of m. The resulting $X(m,\omega)$ then shows the spectra of the signal for different points in time m. In contrast to a single Fourier

transform, the STFT algorithm can thus be used to analyze non-stationary signals. The individual Fourier transforms are implemented using a discrete transform based on a Fast-Fourier algorithm.

The detailed implementation of the algorithm can be found in our published work [129]. The main consideration concerns the used window function. The window function must be chosen such that, its impulse responses equals the frequency response of the superheterodyne receiver's IF bandpass filter. In that way, the STFT will lead to the same spectral representation.

Finally, several weighting detectors are implemented. The detectors evaluate $X(m,\omega)$ for constant ω. Thereby the amplitude change over time at each spectral point is evaluated. The most commonly used weighing detectors in legal compliance measurements are peak, average and quasi-peak detector. The peak detector holds the maximum value observed during dwell time. The average detector shows the mean value over time. The quasi-peak detector has a fast charging constant and slow discharging constant. It evaluates the interference capability of a signal [136]. All detectors will show the same measurement reading for so-called narrowband signals. These are signals with a fundamental frequency above RBW of the bandpass filter. Narrowband signals will show a line spectrum. For broadband signals, the detectors will show different reading. Broadband signals have a fundamental frequency lower than RBW and will show a continuous spectrum. For such signals the peak detector will show the largest reading, the average detector will have the lowest reading.

The peak detector is implemented as proposed in [24]:

$$V_P(\omega) = MAX_{n=0}^{M}\left[X(n,\omega)\right] \tag{4.6}$$

To get correct results, obviously the simulation output $x[n]$ needs to contain all generated disturbances (the dwell-time needs to be large enough).

The average detector is implemented as:

$$V_{AV}(\omega) = \frac{1}{M}\sum_{n=0}^{M} X(n,\omega) \tag{4.7}$$

For pulsed disturbances, the result depends on whether i or $i+1$ pulses are evaluated. It is recommended to simulate the device for at least five

periods of the generated pulses. In this case, the deviation reduces below 2 dB.

The quasi-peak detector is difficult to model. In the CISPR16-1-1 standard, it is defined to have a fast charging constant and slow discharging constant. The standard also defines, that the output of the detector shall be displayed on a critically damped mechanic meter to give a smooth reading. Unfortunately, the definition of the different time constants implies a dwell time of at least 1 s. Clearly, this is an unfeasible long time for transistor-level simulation. In [129] we have thus published an algorithm to estimate the quasi-peak reading from the calculated peak and average readings. A detailed explanation of the algorithm is shown in appendix A.2. The estimation method allows accurate results for a large group of practical signals, and is the first published algorithm to estimate a quasi-peak reading from only some milliseconds of simulation time.

4.3.3. Comparison of measured and simulated results

In the course of this project, a filterless Class-D amplifier in 180 nm CMOS technology was designed by the author. The amplifiers's power stage is intended to drive up to 1.5 W into an 8 Ω speaker. The emission simulation approach derived above was used to estimate the emission measurement result during design-time.

Fig. 4.14 shows the simulated and measured results. The shown simulations were conducted at post-layout stage including extracted parasitics. On the left side, the results with output power of about 1 W are shown. The right side shows the results at idle. The first row shows the peak-detector reading, which gives the highest common-mode voltage observed during dwell time. With a sinusoidal input signal (left), the simulation and measurement show good agreement for the peak measurement. The spiky emission at lower frequencies are predicted very well, with a maximum deviation of 4 dB below 30 MHz. The broadband noise-floor below 10 MHz is lower in simulation. This is because the power-stage control signals are generated using a system-level model in *Matlab*®. The signals do not incorporate flicker and thermal noise typically present in real modulators. The resonances at 160 MHz and 500 MHz are nicely estimated, but the measurements show higher damping of the resonances. The maximum deviation is 5 dB and 6 dB, respectively. A plausible reason could be, that

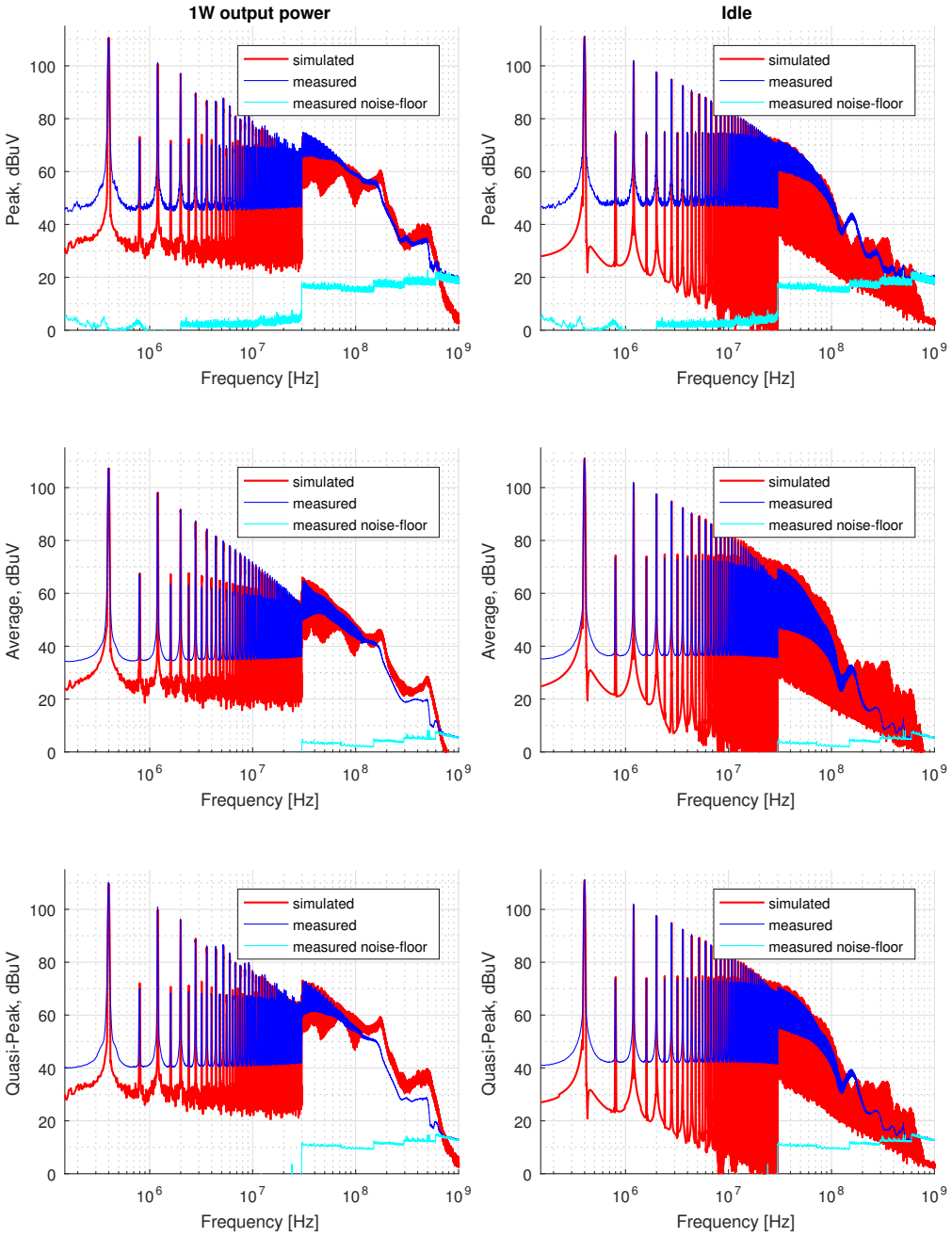


Figure 4.14.: Simulated and measured conducted, common-mode output noise.

the simulation model does not include the skin-effect of conductors. The skin depth in gold at 160 MHz is only 6 µm. This leads to higher resistivity of conductors and higher damping of resonances. Above 100 MHz the emission are overestimated by 3 dB to 6 dB, but generally good agreement is achieved.

In idle operation (right), good agreement is again achieved below 30 MHz, with a maximum deviation of 2 dB. Above 100 MHz the deviation is larger, a difference up to 12 dB can be observed. This could result from differences between simulated and measured rise and fall times when switching without load current. From the difference between peak and average results of the idle measurement, one can conclude that, the rise and fall times vary over time. This behavior is not explained by transistor-level simulation. Nevertheless, it should be noted, that the largest peak-reading deviation (at about 350 MHz) is only 40 µV.

The deviation of the average and quasi-peak results at 1 W, directly results from the behavior at idle. As explained above, the readings are weighted over time. The deviation at idle therefore also impacts the readings with sinusoidal input signal.

Several additional simulations were carried out, mainly to verify the simulation setup and to investigate the influence of the different components in the simulation model. Fig. 4.15 shows the results. The full simulation setup is shown in black, the modified setup in red. Only CISPR band C and D are shown (above 30 MHz), because no differences could be observed for lower frequencies. At first, the mutual inductance between bond-wires was removed. This shifts the resonance at about 160 MHz to higher frequencies (by about 10 MHz). However, the effect is negligible in this case, considering the absolute deviation from the measurement.
The impedance matching network is connected to the microchip with very short (8 mm) microstrip lines. The inductance of these lines is included in the model. In the second simulation, this inductance was removed. As can be seen, this shifts the resonance at 500 MHz towards higher frequencies by about 200 MHz.
In the third case, the models of the leadframe and the bondwires were removed. This changes the complete result above 10 MHz.
Finally, the external supply network model was replaced with an ideal voltage source. Again, the resonance at 160 MHz is affected.

One can thus conclude, that the resonance at 160 MHz mainly results from the bond-wire inductance and the external decoupling capacitor. The

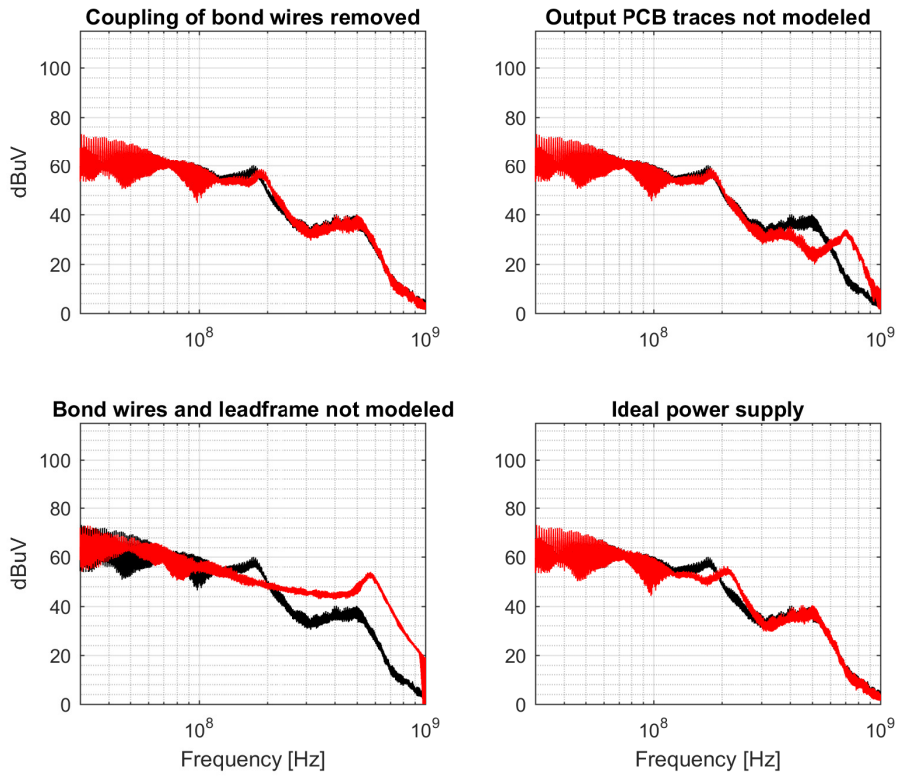


Figure 4.15.: Variations of the simulation model. The full model is shown in black, the modified model in red.

resonance at 500 MHz is determined by the inductance and capacitance at the output of the amplifier. Thus, the simulation setup can also be used to find the root cause of emission issues.

4.4. Conclusion

This chapter outlined, that integrated Class-D amplifiers can be a major source of electromagnetic emission. With theoretical considerations and measurement results, this work proved that filterless amplifiers are especially empowered to create EMI. The findings were published in a peer-reviewed conference [111] and will raise the awareness on emission issues caused by filterless amplifiers.

No suitable emission measurement setup could be found in literature, which allows to compare integrated Class-D amplifiers. Hence a new IC-level measurement for the comparison of integrated Class-Ds is proposed by the author. This new setup allows simple and repeatable conducted measurements to quantify the *emission ability* of an amplifier. Thereby the emission of filterless amplifiers can be compared at IC-level for the first time. The versatility of this measurement setup has been demonstrated in several of our peer-reviewed publications [121, 111, 137, 138].

This work also derives how to model this measurement setup for simulation. The modeling approach developed in this work is very flexible and can be used to verify emission specifications at any stage in the design process. Especially, it is compatible to the standard design flow of analog integrated circuits and can be directly used in schematic driven simulation. In comparison to previous work, not only the electrical properties of the measurement setup are modeled, also the behavior of the measurement equipment is considered. This work clearly outlines that a simple FFT is not sufficient to analyze the emission. Accordingly we derived a sophisticated model of an EMI test-receiver, such that simulation results can be directly compared to measurement results. A comparison between simulation and measurement has been carried out, with a Class-D amplifier designed by the author. The deviation between simulation and peak measurement was less than 4 dB up to 100 MHz. Hence, this simulation approach allows to verify emission targets before IC production.
We published the EMI test-receiver model in one of the most respected conferences on EMC [129]. The publication had a special focus on the implementation details, such that other research groups could profit from this approach. The publication also includes the first algorithm to estimate the quasi-peak result from only some milliseconds of simulation output. In the meantime since publication, the model has contributed to several projects of other researchers [139, 140, 141, 142].

Above 100 MHz the emission simulation was less accurate. The analysis of several simulation variants has shown, that external components and their parasitics strongly affect the created emission at high frequencies. On one hand, this shows that PCB level decisions not only determine emission distribution, but also how much voltage noise is generated inside the microchip. On the other hand it is an indication that IC-level measurements according to IEC61967, are impacted by unwanted parasitic resonances. The claim of IEC61967-4 [143], that IC-level measurements

"... guarantee a high degree of repeatability and correlation ..." should be approached with caution at frequencies above 100 MHz.

5. System and circuit level design techniques

5.1. Spread-spectrum emission reduction

Class-D amplifiers can be a major source of EMI. The situation is especially critical for PWM based Class-D amplifiers. In such amplifiers, the switching rate is constant. The energy of the generated high frequency noise is concentrated around multiples of the switching rate. This leads to spiky emission with large amplitude.

A well known technique to reduce the interference created by clocked electronic circuits is spread-spectrum modulation (SSM) [144]. Clocked circuits, such as synchronous digital blocks typically create spiky emission at their clock frequency and multiples of it. SSM utilizes variable frequency clocks instead of fixed frequency clocks. By using SSM, the generated emission energy is distributed over a larger bandwidth thanks to a variable clock frequency. Thereby, the overall amplitude of the emission peaks is reduced. As an example, in digital communication [145] the digital clock is frequency modulated using a certain modulation patter, to reduce the amplitude of the generated emission. Fig 5.1 illustrates the principle.

Quantifying the achieved amplitude reduction is not straightforward. SSM generates rather broadband emission. When measuring the emissions of clocked circuit with SSM, the used measurement device has to be considered. Emission measurements are typically done in frequency domain. The frequency resolution of the measurement device is important when measuring devices with SSM. The frequency resolution determines how much energy of the emission is accumulated to one point in the measured spectrum. Moreover, the response of the measurement device to broadband signals has to be considered. Several quantification setups can be found in the literature [146, 147, 148, 19] and in datasheets [16]

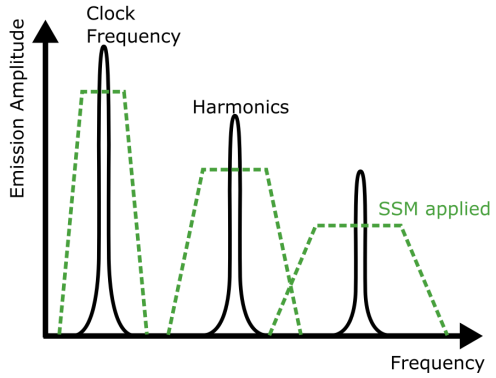


Figure 5.1.: Frequency domain representation of a clocked circuit's emission, with and without SSM.

of devices using SSM. All of them use different (and often unstated) frequency resolution, and various measurement devices. In many research works, this impact of the measurement equipment is not even considered. Comparison of the methods is thus impossible, and presented results often do not allow any prediction how the methods will perform in legal compliance measurements.

SSM methods are implemented to reduce EMI and to pass legal emission limits. Legal emission measurements are carried out using EMI test-receivers, which comply to CISPR16-1-1. Emission reduction achieved with SSM, should therefore be evaluated using such a test-receiver. As covered in chapter 4, these receivers have well defined frequency resolution (comp. table 4.1). Moreover, the response to broadband signals, is clearly specified by weighting filters. In this sense, the term *emission reduction* in this work emphasizes: an amplitude reduction of emission when measured with a standard-compliant test-receiver.

SSM can be applied to PWM based applications to reduce the amplitude of the spiky emission. Various implementations [146, 147, 148, 149] have been reported in the past. For Class-D amplifiers, a frequency modulated reference signal is used instead of a fixed frequency one [19, 20, 13]. Thereby, the resulting PWM signal is frequency modulated with a certain modulation pattern, leading to a variable switching rate of the power stage. In this work, SSM methods for Class-D amplifiers are divided into two groups. In periodic spread-spectrum methods, a dedicated periodic modulation pattern is used. In randomized spread-spectrum methods, a (pseudo-) random modulation pattern is used. Randomized SSM has been

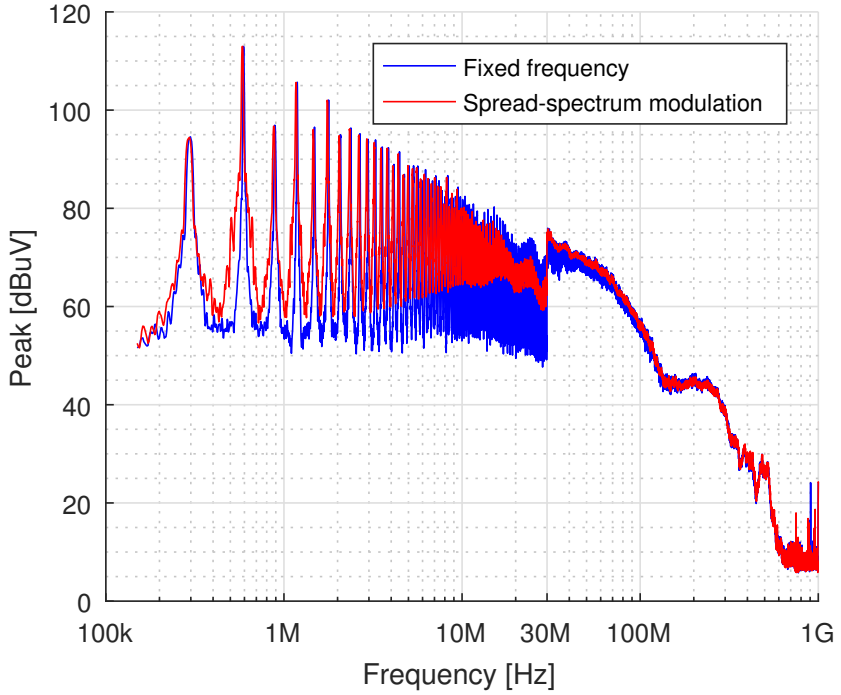


Figure 5.2.: Conducted emission of a commercial Class-D amplifier with optional SSM.

used in Class-D amplifiers by several other research groups [19, 20, 17, 13]. But the presented emission reduction results cannot be compared due to varying verification setups. Randomized SSM has also been used in commercial Class-D amplifiers [16]. But the emission reduction is unsatisfactory, when measured with a standard compliant test-receiver (Fig. 5.2). The published methods often comment on emission reduction, not taking into account impacts on the audio performance. Moreover, a comparison with the rarely used periodic SSM is lacking.
In this chapter, it will be shown, that periodic and randomized SSM can be used for Class-D amplifiers. The advantages and disadvantages of the methods are examined and compared for the first time. Moreover, implementation guidelines for both methods are discussed. Another novelty of this work is that all used methods are strictly targeted towards and analyzed for best performance in legal compliance measurements. Furthermore, the derived analyses in this work allow to optimize a method for a certain measurement setup. The obtained results have already been published [121, 137, 150, 138, 151]. The results were verified with system-level simulations and several discrete Class-D amplifier prototypes. Thereby not only emission reduction, but also audio performance is considered.

Finally, another rarely used technique is studied. Common-mode modulation is a promising approach where spectral shaping is achieved without varying the clock frequency. Even though, the technique is not novel [87], this work presents the theoretical background of the technique for the first time. Using the derived theory, an optimized parameter choice for implementation is discussed.

5.1.1. Periodic spread-spectrum methods

In periodic spread-spectrum methods, a well defined, continuously repeating modulation pattern is used to modulate the frequency of a clock circuit [152]. Thereby the frequency of the clock is varied with a certain modulation pattern $p(t)$. For simplicity of explanation, first a sinusoidal clock generator is considered. In the absence of modulation, it generates a sinusoidal carrier signal with frequency of f_c and amplitude A_c. When frequency modulation is applied, the modulated signal $x(t)$ of can be calculated using well know formulas from telecommunication theory:

$$x(t) = A_c \cos\left[2\pi fc + \int_0^t p\left(\tau\right) d\tau\right] \tag{5.1}$$

Various modulation patterns can be used. In the simplest case, the pattern is a cosine, with a frequency f_m and amplitude Δf. The amplitude Δf of the modulating pattern is called the peak frequency deviation. It is expressed in Hz and defines the maximum excursion of the clock frequency from the base frequency f_c. In this case of so called single tone modulation, eq. (5.1) simplifies to:

$$x(t) = A_c \cos\left[2\pi fc + \int_0^t \Delta f \cos\left(2\pi f_m \tau\right) d\tau\right] \tag{5.2}$$

leading to:

$$x(t) = A_c \cos\left(2\pi f_c t - m_f \sin\left(2\pi f_m t\right)\right) \tag{5.3}$$

$$m_f = \frac{\Delta f}{f_m} \tag{5.4}$$

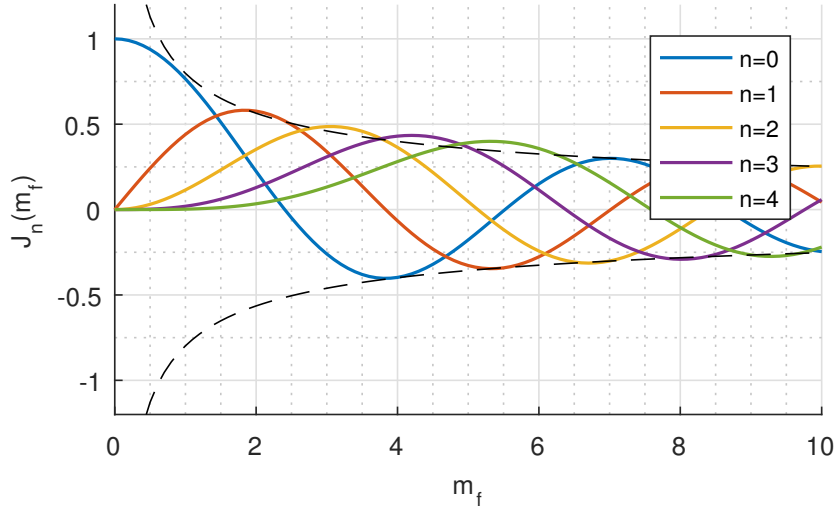


Figure 5.3.: Besselfunctions of the first kind $J_n(m_f)$ for $n = 0;1;2;3;4$, the black, dashed line shows the envelope $\sqrt{\frac{2}{\pi m_f}}$.

A Fourier expansion of this expression using Bessel-functions of the first kind can be conducted. In this way, the spectrum of the generated signal can be interpreted:

$$\begin{aligned} x(t) = A_c\{ & J_0(m_f)\cos(2\pi f_c t) \\ & + J_1(m_f)\left[\cos\left(2\pi\left(f_c + f_m\right)t\right) - \cos\left(2\pi\left(f_c - f_m\right)t\right)\right] \\ & + J_2(m_f)\left[\cos\left(2\pi\left(f_c + 2f_m\right)t\right) - \cos\left(2\pi\left(f_c - 2f_m\right)t\right)\right] \\ & + J_3(m_f)\left[\cos\left(2\pi\left(f_c + 3f_m\right)t\right) - \cos\left(2\pi\left(f_c - 3f_m\right)t\right)\right] \\ & + \ldots \end{aligned} \tag{5.5}$$

The SSM oscillator signal contains an infinite number of cosinusoidal components. The components are offset form the base frequency f_c by multiples of the modulating frequency f_m. Each component is weighted by the according Bessel-function J_n of the first kind, evaluated at the modulation index m_f. Fig. 5.3 shows the first four Bessel-functions. Each function has an amplitude smaller than one, and the functions have an envelope that decreases with $\sqrt{(2/(\pi m_f))}$. Thus, all resulting components have an amplitude smaller than the amplitude of an unmodulated clock. With increasing m_f the amplitude of all generated components decreases. This means, that the energy of the carrier signal is shifted to sidebands

using periodic SSM. Most of the energy will still be concentrated in a certain bandwidth B_{SSM} which can be estimated by Carsons's rule:

$$B_{SSM} = 2(\Delta f + f_m) \tag{5.6}$$

In many applications, not sinusoidal oscillators, but oscillators with rectangular (trapezoidal) output signal are of interest. The effect of SSM on such signals can be studied if the signal is described as Fourier expansion. In this way, the signal is represented as a sum of sinusoidal waves, thus by the fundamental and its harmonics. It can be shown [153] that by applying SSM, each individual harmonic is frequency modulated, as described above. However, the effective frequency deviation Δf_n increases linearly with the harmonic order n: $\Delta f_n = n\Delta f$. Thus, in higher harmonics of the clock signal, the energy is spread to a larger bandwidth. For high order harmonics, the individual B_{SSM} will eventually start to overlap.

In many cases, a non-sinusoidal modulation pattern is used. An extensive review of different patterns can be found in [153]. In several practical works, triangular or sawtooth patterns are employed [154, 145]. The shape of the pattern mainly influences the energy distribution inside the spread bandwidth. Some patterns show a slightly non-uniform distribution of the energy. But, most patterns have a similar performance. This is plausible, when examining eq. (5.1). The modulated signal depends on the integral of the modulation pattern. Therefore, the fundamental frequency present in the modulating pattern largely determines the modulation outcome. The spreading effect is thus mainly determined by the fundamental frequency f_m of the pattern and the peak frequency deviation Δf_n [154].

Using a dedicated periodic pattern, the resulting spread waveform can be very well predicted by eq. (5.5). The amplitude and location of the sidebands can be controlled by choosing the frequency of the pattern and its amplitude. Such periodic SSM can be optimized for lowest measurement results with an EMI test-receiver. This was clearly demonstrated in our already published works [121, 137].

For lowest measurement results, the behavior of the receiver's weighting detectors should be examined. First, the case is considered, where multiple sidebands of the spread waveform fall inside the measurement bandwidth. The bandwidth is determined by the receiver's IF bandpass filter. In this case, the output of the receiver's envelope detector will be a signal with varying amplitude. The varying amplitude results from different phase

relation of the sideband components inside the measurement bandwidth. Most of the time, the sidebands will have a different phase angle, leading to a small signal at the receiver. But if the dwell-time of the receiver is long enough, all of the components will eventually be in phase, resulting in a large signal at the receiver. Accordingly, the measurement result will depend on the used weighting detector. The peak detector will show a much larger result then the average detector. In the extreme case, most of the sidebands of the spread signal fall into the measurement bandwidth. All of them will contribute to the peak reading, and no amplitude reduction will be visible in the measurement. In contrast, the average detector result will show a certain amplitude reduction. This behavior has led to the frequently heard misbelief, that SSM cannot reduce peak readings.

In order to improve a peak detector result, the SSM should be implemented, such that only one sideband falls into the measurement bandwidth. For most Class-D amplifiers, the largest emission will be generated in CISPR Band-B (150 kHz-30 MHz). In CISPR Band-B, the measurement bandwidth is 9 kHz. Therefore, the fundamental frequency of the modulation profile should be chosen larger than 9 kHz. In this way the created sidebands are spaced apart by more than 9 kHz. This will lead to reduced emission measurement results for all weighting detectors. Above CISPR Band-B (above 30 MHz), the measurement bandwidth is 120 kHz. A modulation frequency larger than 120 kHz is not feasible in most Class-D designs. Emission reduction with SSM is thus limited to CISPR Band-B.

A large frequency deviation Δf can be chosen. This reduces the amplitude of the individual sideband components (eq. (5.5)) and increases the resulting bandwidth to which the energy is spread (eq. (5.6)). The amplitude reduction can be easily estimated by considering the envelope of the Bessel-funtions. For a given deviation and modulation frequency, all generated signal components are bound by the envelope. However, as stated above, the spreading effect increases with the harmonic order of the emission. For high order harmonics of the emission, the spread emission will start to overlap. When this happens, the reduction will decrease. Lower frequency deviation will push the beginning of overlap to higher frequency.

The possible frequency deviation is often limited by system-level requirements. It cannot be increased arbitrarily. If only the average detector reading is of concern, a smaller modulation frequency can be used. The individual sidebands will then be closer to each other, and SSM will have

smaller effect on the peak reading. But in turn the modulation index (eq. (5.4)) is increased which reduces the amplitude of the individual components. Significant reduction of the average reading can be achieved, as demonstrated in our work [137].

The implementation of periodic SSM to PWM is as follows: A frequency modulated reference signal is needed. However, the frequency modulated reference signal should not lead to distortion. Therefore, the frequency can only change in stepwise manner at discrete points in time. Fig. 5.4 illustrates the principle applied to a triangular reference signal. As can be seen, the slope of the reference signal is varied at discrete times. In this way any curvature in the slope is avoided which would lead to signal distortion. In this case, the frequency modulation is a stepwise approximation of a continuous modulation. In [152] it was shown, that modulation patterns which are stepwise approximations of continuous patterns have very similar spectral characteristics, when fine grain steps are used. This observation is plausible considering the integral in eq. (5.1).

There are several ways to generate the reference signal for PWM: for instance by using a relaxation oscillator [155], or by integration of a square-wave signal [85]. To implement SSM, relaxation oscillator with adjustable current sources [112, 19, 20] have been proposed to in many works. Fig. 5.4 shows a simplified diagram of a SSM reference generator based on a relaxation oscillator. In contrast to a standard relaxation oscillator, a variable current source is used to generate the working current. In the schematic, several binary weighted current sources are used. They act as a current steering DAC to modify the working current of the oscillator. A small number (e.g. 16 or 32) of different current values is sufficient [152] to achieve SSM. The specifications for DAC design are thus quite relaxed. The modulation profile is generated with a clocked counter, resulting in saw-tooth frequency modulation. The counter is directly clocked by the oscillator reducing implementation effort. In this way, the slope of the reference signal is modified after each reference signal period.

Above, it was explained how to choose the parameters Δf and f_m of the periodic SSM for best emission reduction. This translates directly into the maximum current variation of the DAC and resolution of the used counter. Still, the design of Class-D amplifiers restricts the possible parameter choice, as pointed out in our published works [121, 138]. When global feedback is used, the instantaneous frequency of the reference signal has to fulfill ripple-stability (eq. (2.5)). Otherwise uncontrolled switching

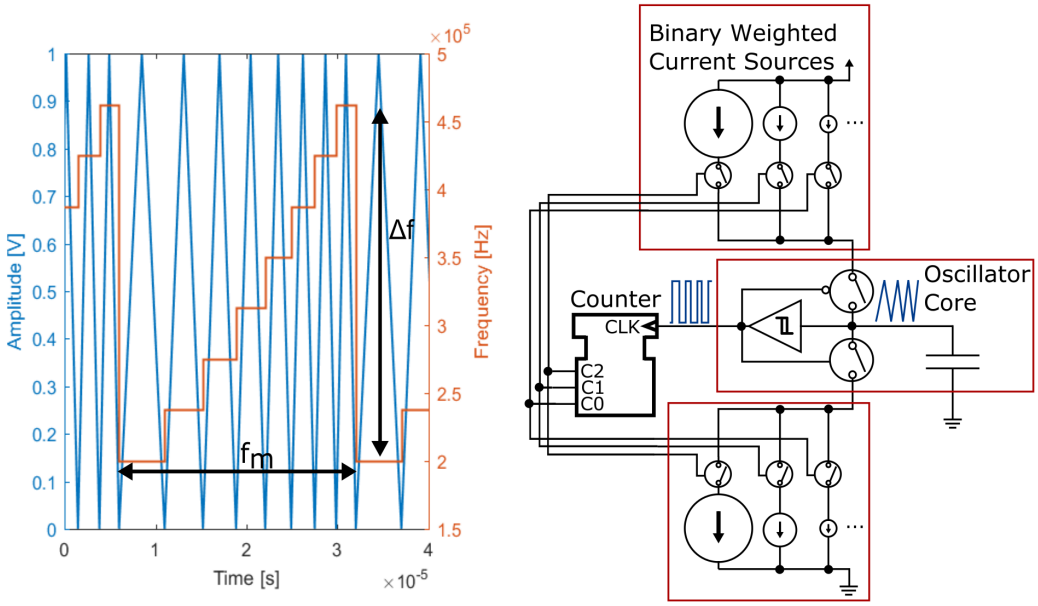


Figure 5.4.: Left: Frequency modulated reference signal using a sawtooth modulation profile.
Right: Simplified schematic of a reference signal generator with SSM.

of the power-stage can occur. Higher switching frequency increases the switching losses. Thus, the maximum possible frequency deviation Δf from the base frequency is limited.

When SSM is applied to audio amplifiers, also the audio performance has to be considered. The impact of a variable reference frequency on the audio-band spectrum is difficult to determine. PWM is generally a highly non-linear process. It is linear only for baseband signals as shown by the mathematical models [50, 51]. But these models cannot be used with variable reference signal. Moreover, in Class-D amplifiers several other non-linear effects are present. Hence, SSM impact on the amplified signal has been studied with several SSM-Class-D prototypes in this project [121, 150, 138]. The results were compared to system-level simulation. In the following the observations and drawn conclusions will be presented.

Extensive system level simulation and measurement of several prototypes developed by the author have clearly shown, that PWM with periodic SSM generates tones in the output spectrum. The tones appear at the modulation frequency f_m and multiples of it ($m\ f_m$). When the PWM processes an input signal, additional intermodulation tones are generated. They appear at $n\ f_{sig} \pm m\ f_m$. However, in filterless, BD-modulated amplifiers, the tone at the modulation frequency (and its harmonics) is not critical. This tone appears with the same phase on both amplifier outputs and is thus suppressed by the symmetrical load-connection. Moreover, all even-order intermodulation products ($2n\ f_{sig} \pm m\ f_m$) are canceled. The remaining tones (odd order intermodulation) can degrade the audio performance. These tones are especially problematic for low frequency, low amplitude input signals. In this case THD+N can deteriorate due to these intermodulation tones. For large input signals and higher signal frequency, the additional tones are often below the intrinsic distortion of the amplifier having a much smaller effect on THD+N.

Unfortunately, global feedback does not properly suppress these tones. A certain attenuation of the tones is visible, but the attenuation is significantly smaller than expected by the open loop gain of the system. It is assumed that a mechanism similar to the intrinsic feedback distortion is causing this behavior. A general observation was that lower modulation frequency creates less degradation of THD+N. This is plausible, because the intermodulation tones are generated at lower frequency. Loop-gain typically increases at lower frequency. Another plausible observation was, that smaller frequency deviation improves audio performance. In some

Class-D designs, a lower modulation frequency and moderate deviation is sufficient to reduce the generated tones below the intrinsic distortion, as demonstrated in one of our publications [137]. Another option is choosing the modulation frequency larger than 40 kHz. In this case, any intermodulation tones of the first kind will fall outside the audible range, not affecting THD+N. This was demonstrated in our work of [121].

It can be concluded, that emission reduction and audio performance leads to opposing demands on the SSM parameter choice. Large frequency deviation spreads the emission to a larger band, but increases audible tones. For a given deviation, modulation frequency above 40 kHz can improve audio performance, but in turn increases the amplitude of individual sidebands in the spread emission. Modulation frequency can be reduced to low frequencies where the amplifier has high loop gain (e.g. 500 Hz). But in this case, the peak detector measurement will not show much reduction any more.

Fortunately, the emission reduction for the different detectors can be simulated using the model of an EMI test-receiver (chapter 4.3). In [121] the author demonstrated, that the reduction predicted by the model shows good agreement with measurement results. As SSM will only be effective up to 30 MHz, a transistor-level model of the amplifier is not needed. A less accurate system-level model of the amplifier is often sufficient to simulate the emission reduction at the first few harmonics. The system-level model can also be used to study the effect on THD+N. In this way, the impact of a certain modulation pattern can be verified in a fast and inexpensive way. And an optimal trade-off of the parameters can be found.

In the following, this approach is demonstrated for a Class-D amplifier example. A filterless, Class-D amplifier with global, differential feedback is considered. The well known second order loop-filter with a single operational-amplifier [156, 46, 45] is used and the nominal frequency of the reference signal is 300 kHz. Fig. 5.5 shows a bode plot of the amplifiers open-loop gain. The finite gain of the single operational-amplifier is considered in the transfer function. Fig. 5.6 shows the system-level model of the amplifier, implemented in *Matlab Simulink®*. A simplified model of a power-stage is used, which models signal dependent delay of the power-stage. Simulation is carried out with a 1 kHz input signal. The emission are simulated with a high-level model of the 150 kHz direct coupling method. Post processing is used to emulate the EMI test-receiver (as discussed in chap. 4.3), and to calculate THD+N.

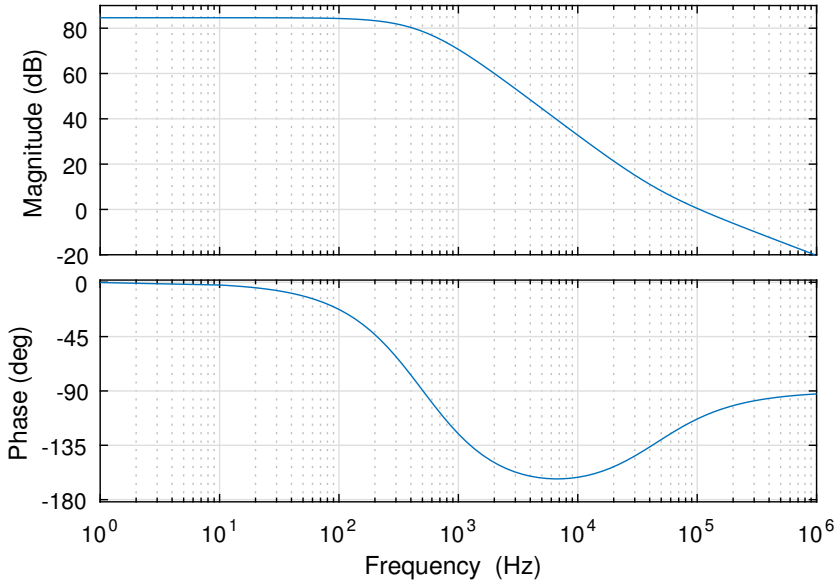


Figure 5.5.: Open loop-gain of the filterless Class-D amplifier used to demonstrate periodic SSM.

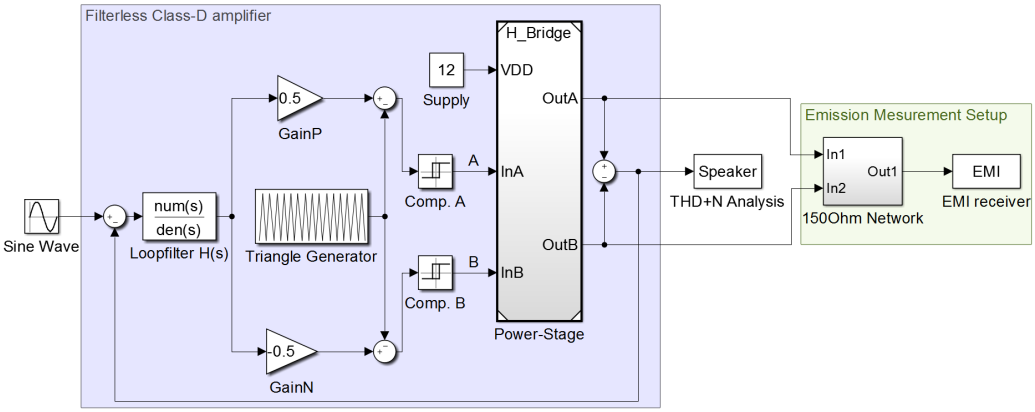


Figure 5.6.: System-level model of the filterless Class-D amplifier. SSM is achieved by assigning a pre-calculated waveform to the triangle generator.

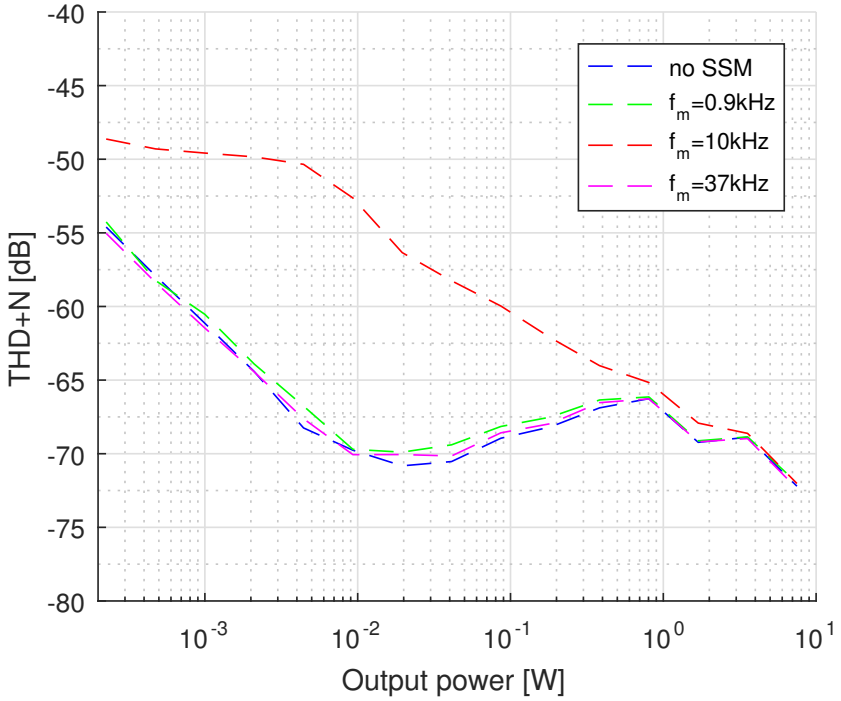


Figure 5.7.: Simulated THD+N for three different SSM settings.

In the following figures, three periodic SSM settings are compared. In all cases a triangular modulation profile is used with a deviation of ± 60 kHz. Each setting has a different modulation frequency, of 0.9 kHz, 10 kHz and 38 kHz. Fig. 5.7, shows the simulated THD+N for the different settings. Output power is calculated considering an 8 Ω speaker.

Fig. 5.8, shows the simulated conducted common-mode emission for the different settings. The achieved reduction at the first harmonic for peak/average is 1.5 dB/17.2 dB, 7.7 dB/7.9 dB, 4.5 dB/4.4 dB respectively. As predicted, with f_m =0.9 kHz, lowest reduction in the peak measurement, but highest reduction in the average measurement is achieved. With f_m =37 kHz, the generated sidebands are clearly visible. The spread bandwidth increases with the harmonic order and starts to overlap from the seventh harmonic upwards.

A rapid prototype of the amplifier was built by the author [138]. Off-the-shelf discrete components were used. But the components were selected to resemble the performance and switching characteristics of an integrated amplifier. Fig. 5.9 shows a picture of the prototype. It is capable of driving up to 8.5 W into an 8 Ω speaker. The reference signal for the PWM is

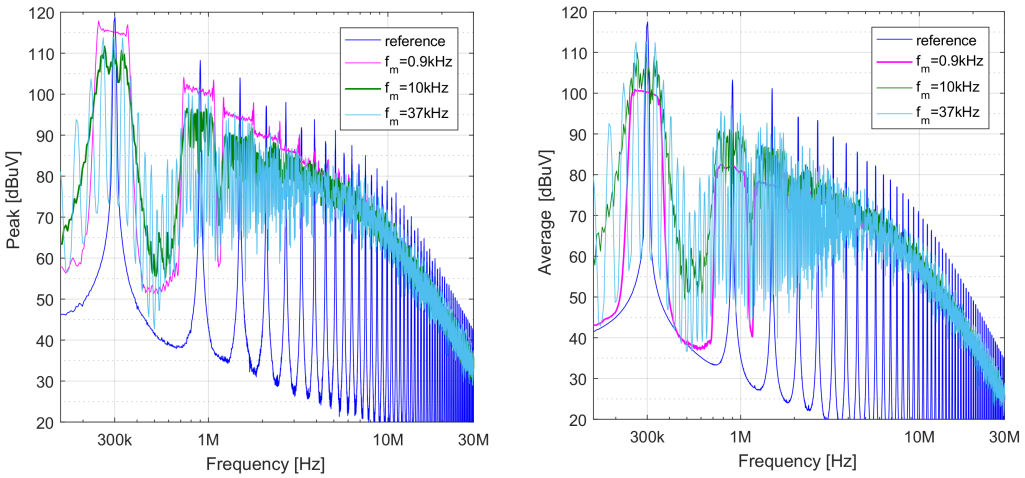


Figure 5.8.: Simulated conducted common-mode emission. Left: peak detector; Right: average detector;

generated using Matlab. The signal is programmed into an arbitrary waveform generator that emulates the relaxation oscillator.

Fig. 5.10 shows measured THD+N. The periodic SSM generates intermodulation tones in the output. The tones are sufficiently suppressed for the f_m =0.9 kHz setting, or do not fall into the audible range for the f_m =37 kHz setting. Fig. 5.11 shows the spectrum for the f_m =10 kHz setting. The intermodulation tones around the modulation frequency are clearly visible and degrade THD+N. The measured output noise (with zero input signal) was 45 µVrms in all settings and not affected by SSM. The measurement results show good agreement to simulated results. Apart form the hump in the measured THD+N at around 20 mW, the THD+N characteristic is estimated correctly. Hence the effect of SSM on THD+N can be analyzed in simulation before building a prototype.

Fig. 5.12, shows the measured conducted common-mode emission of the prototype. The achieved reduction closely matches the simulation result, with a deviation of less than 1 dB at the first harmonic. The absolute values of the emission are different above 10 MHz, because the simulation does not accurately model the slew-rate of voltage transitions. Nevertheless, it is shown that SSM can be analyzed very well with the EMI test-receiver model presented in chapter 4.3. It is thus not necessary to build a prototype for reviewing different SSM methods.

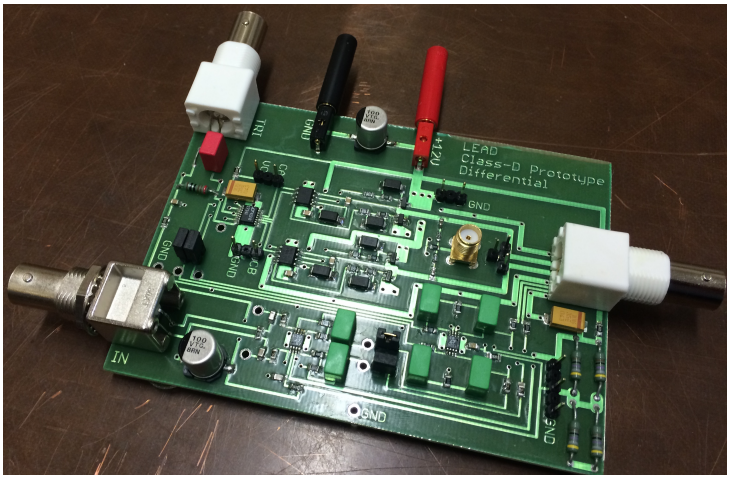


Figure 5.9.: Picture of the rapid prototyping board.

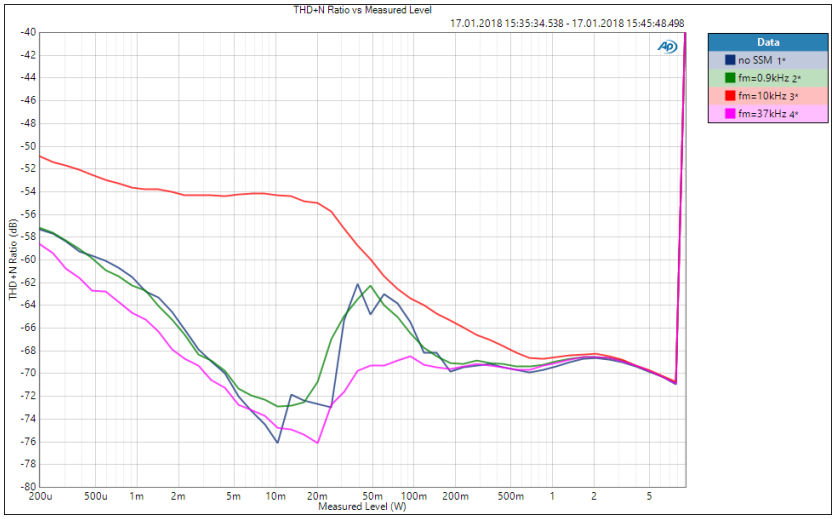


Figure 5.10.: Measured THD+N for three different SSM settings.

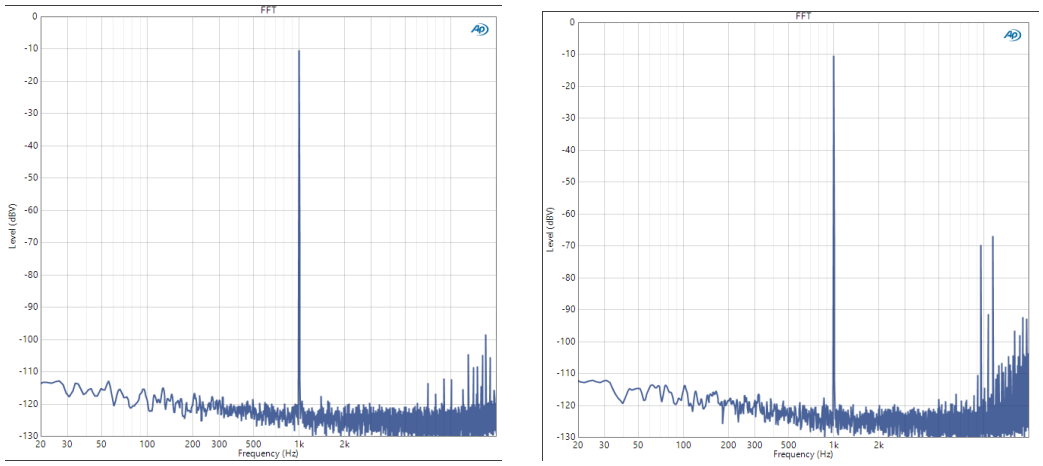


Figure 5.11.: Measured audio-band spectrum.
Left: without SSM; Right: SSM with f_m =10 kHz. THD+N is dominated by the generated intermodulation components.

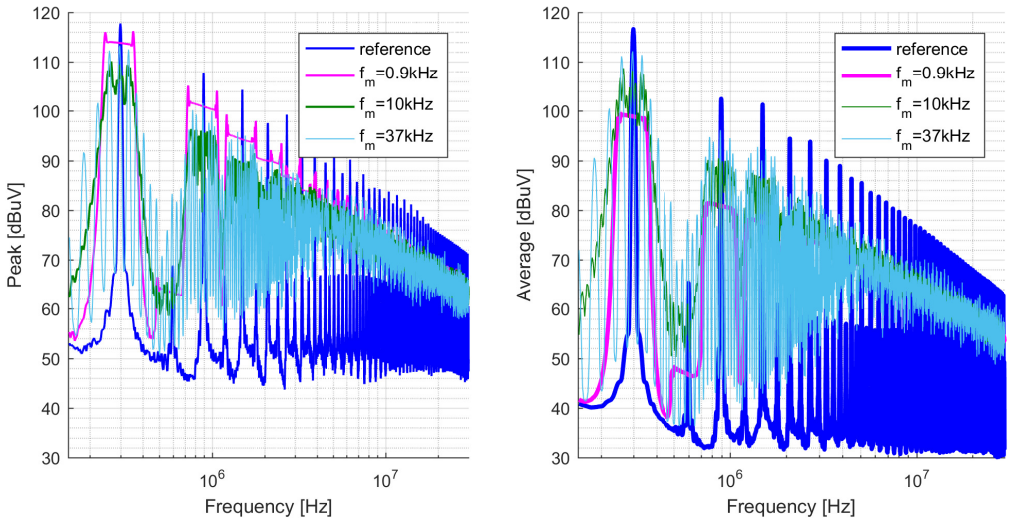


Figure 5.12.: Measured conducted common-mode emission with periodic SSM.

5.1.2. Randomized spread-spectrum methods

Periodic SSM can create audible tones in the output spectrum. The tones are created by the periodic modulation pattern. Such tones can potentially be avoided, by using a modulation pattern which does not show periodic content. A completely random sequence would be an option. But real randomness is hard to achieve, typically pseudo-random modulation patterns are used. Pseudo-random patterns seem random, but have a finite length after which they start to repeat. Thus, a periodicity will still be present in the modulation. However, by choosing a long pseudo-random sequence, the periodicity can fall below the audible range. Randomized SSM can be implemented with the relaxation oscillator used before. But in this case, the counter is replaced by a random number generator. In this way, the switching frequency will change chaotically.

The resulting spectra will look significantly different than the theoretical continuous, single tone modulation treated above. Equation (5.1) is still valid. But derivation of the spectrum is highly complicated due to non-linearity involved. Published works on randomized SSM are thus often based on experimental approaches [19, 20]. In this work, a simple analytic explanation is presented. It allows a informed decision how to choose the implementation parameters for best emission reduction.

The methods used to explain frequency-shift-keying (FSK) in telecommunication lead to an intuitive explanation. In FSK, each symbol of a message to transmit is assigned to a certain frequency. In the simplest case, only two symbols are used. The first symbol is assigned frequency f_1 and the second f_2. The upper part of Fig. 5.13 shows a sample transmission. The transmitter switches between frequency f_1 and f_2 to transmit the message. The message can be considered a superposition of sine-bursts. Each sine-burst has a duration of T_p. Due to linearity of the Fourier transform, the spectrum can be estimated as a superposition of the individual burst spectra. A sine burst has a sinc-shaped spectrum. The spectrum is thus a superposition of two sinc-shapes (lower part of Fig. 5.13). The energy of each burst is largely concentrated in the main lobe. This main lobe is centered at the sine-wave frequency present in the individual burst. In this example, the first lobe is at f_1 and the second at f_2. The zeros of the sinc-shapes are located at $1/T_p$ below and above the center frequency of the main lobe. The energy of each sine-burst is thus mainly concentrated in a bandwidth of $2/T_p$. It is important to note, that the transmitted power

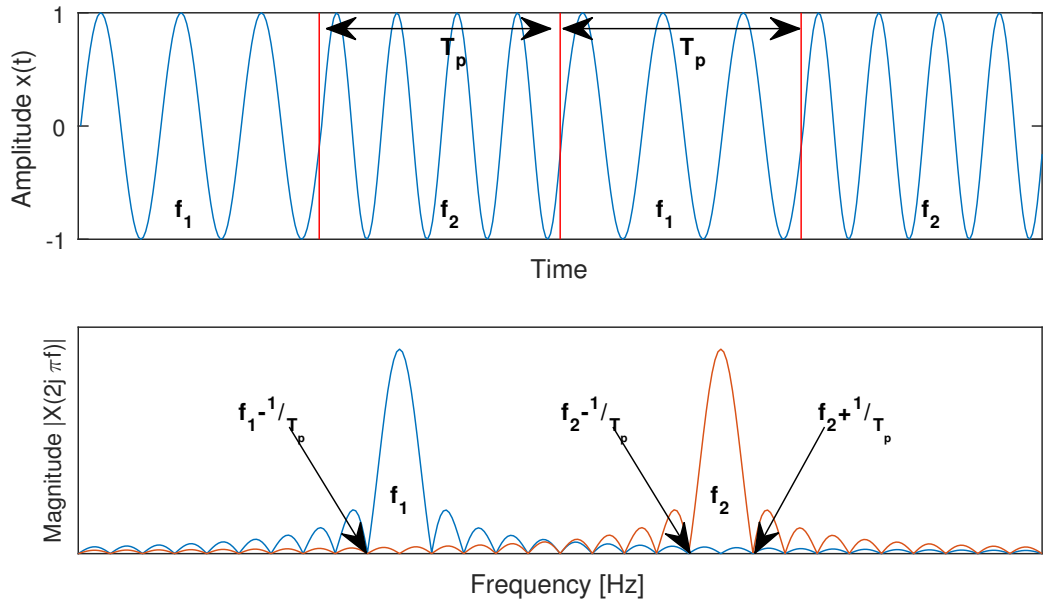


Figure 5.13.: Frequency Shift Keying
Top: Transmitted message; Bottom: Simplified resulting spectrum.

is concentrated around f_1 while f_1 is transmitted and around f_2 otherwise. The instantaneous power at f_1 is thus a time varying quantity. However, the majority of the transmitted power is spread to a bandwidth of $2/T_p$.[1]

In telecommunications, often multiple symbols are used, which are assigned to multiple frequencies (MFSK). The frequencies are offset from each other by f_{step}. This will result in a spectrum with many sinc-shapes. The main lobes will be spaced by f_{step}. Fig. 5.14 illustrates the principle with four different frequencies. The MFSK case is very well suited to describe randomized SSM. The previously mentioned relaxation oscillator is capable of generating M different frequencies in a range of $\pm\Delta f$ around a center frequency f_c. It will thus generate a spectrum of M sinc-shapes. The individual sincs will be offset by $f_{step} = \Delta f / M$.

In the case of randomized SSM, therefore the offset f_{step} of the different frequencies, and the rate of change $1/T_p$ will determine the generated

[1]The described explanation is a simplified view on a waveform with randomly changing frequency. The spectrum of the waveform should be evaluated based on the Fourier transform of the waveform's autocorrelation function (which is the power spectral density), as suggested in [157]. The power spectral density for FSK is derived in [158]. However, for the design of randomized SSM, this simplified view is sufficient to understand the impact of the different parameters.

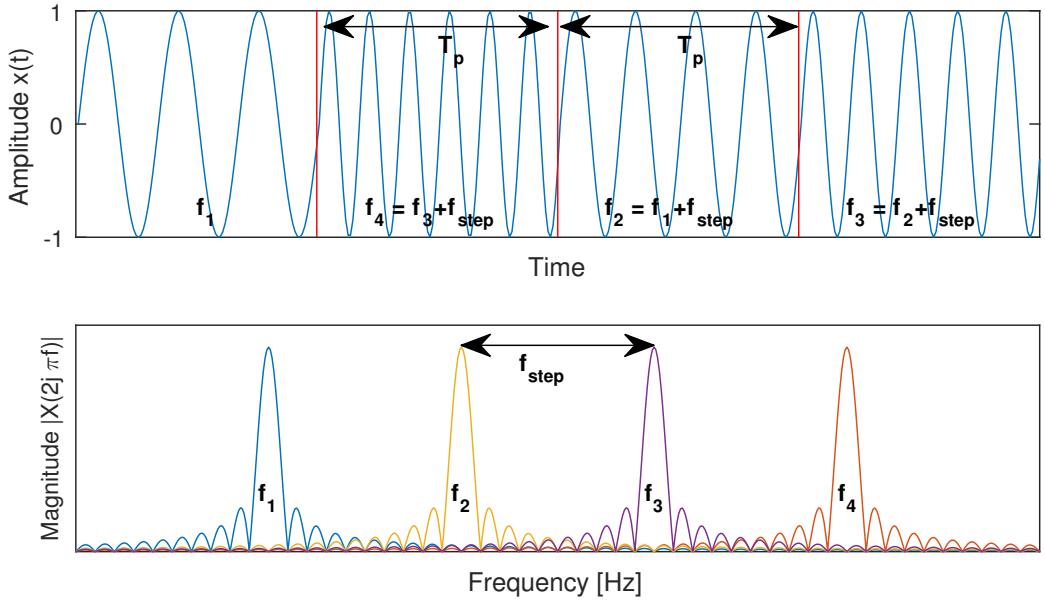


Figure 5.14.: Multiple Frequency Shift Keying
Top: Transmitted message; Bottom: Simplified resulting spectrum.

spectrum. It should be mentioned, that this spectrum is not fundamentally different from periodic SSM. If the frequency step f_{step} decreases, the main lobes will move closer to each other. If T_p is decreased (the frequencies change with a higher rate), the main lobes will become broader. In the case of very small frequency steps and very fast change between the frequencies, the individual sinc-spectra will start to overlap. Constructive and destructive interference will occur. For infinite-decimal small T_p and f_{step} the modulation will approach continuous, analog frequency modulation. On the other hand, periodic SSM in the last section is implemented with step-wise approximation of continuous frequency modulation. It could also be analyzed as a superposition of bursts. However, due to the fine-grain frequency steps used, the individual burst-spectra largely overlap. In this case, considering the continuous single tone modulation approach leads to a more intuitive explanation.

The pseudo-random random number generator is often [19, 20, 17, 13] implemented using a linear feedback shift register (LFSR). Fig. 5.15 shows a realization of the shift register using $N = 8$ D-flip-flops. The LFSR is initialized with a start value (seed). The outputs of the LFSR (P[0] to P[7]) are combined together and fed back to the input by using a feedback function. In each clock cycle, a new random value P[7:0] is generated. A

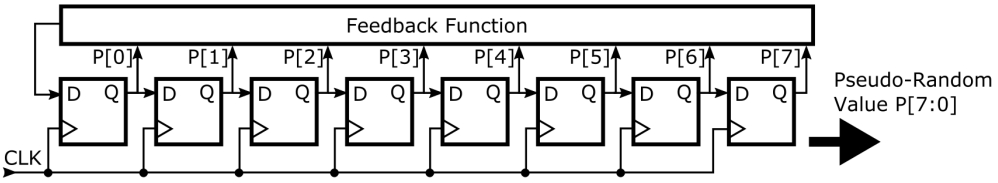


Figure 5.15.: Schematic of a 8-bit LFSR.

maximum length sequence generator can be implemented by choosing a proper feedback function, that has to be a primitive polynomial [159]. In this case, no output value appears twice in the sequence, and the generated pseudo-random sequence starts to repeat only after $2^N - 1$ cycles. The LFSR replaces the counter in the schematic drawing of 5.4, to implement a randomized SSM. The random values generated by the LSFR control the binary weighted current sources of the reference generator. As in the periodic case, the binary weighted current sources act as a DAC to generate a pseudo-randomly varying working current. The clock for the LSFR is provided by the reference generator. The pseudo-random generator is thereby synchronized to the reference generator, such that the frequency changes only at the correct points in time.

A very long pseudo-random sequence is needed to push its repetition rate below the audible range. In the following, two implementations of the pseudo-random number generator will be analyzed. In [13] it is proposed to prolong the repetition rate by using a clock divider in front of the LFSR. In this way, the LFSR is operated at a lower speed. Fig. 5.16 shows the principle. In our work of [150], a cascade of two LFSRs is proposed (fig. 5.16) to increase the sequence length. In this case, the second LFSR initializes the first with a new seed, whenever the pseudo-random sequence starts to repeat. A much longer sequence is generated without slowing down the LFSR.

For the analysis of these two implementations, a simplification is made: Even though, the LFSR is clocked with a variable frequency, a fixed clock frequency of f_{ave} is assumed. This is the average output frequency of the relaxation oscillator. For moderate frequency deviation Δf, this simplification will not have an impact on the analysis.
Using a clock divider, the operation speed of the LFSR can be reduced. The authors of [13] propose to use an eight bit clock divider for their Class-D amplifier. The LFSR will generate a new value with a rate of app.

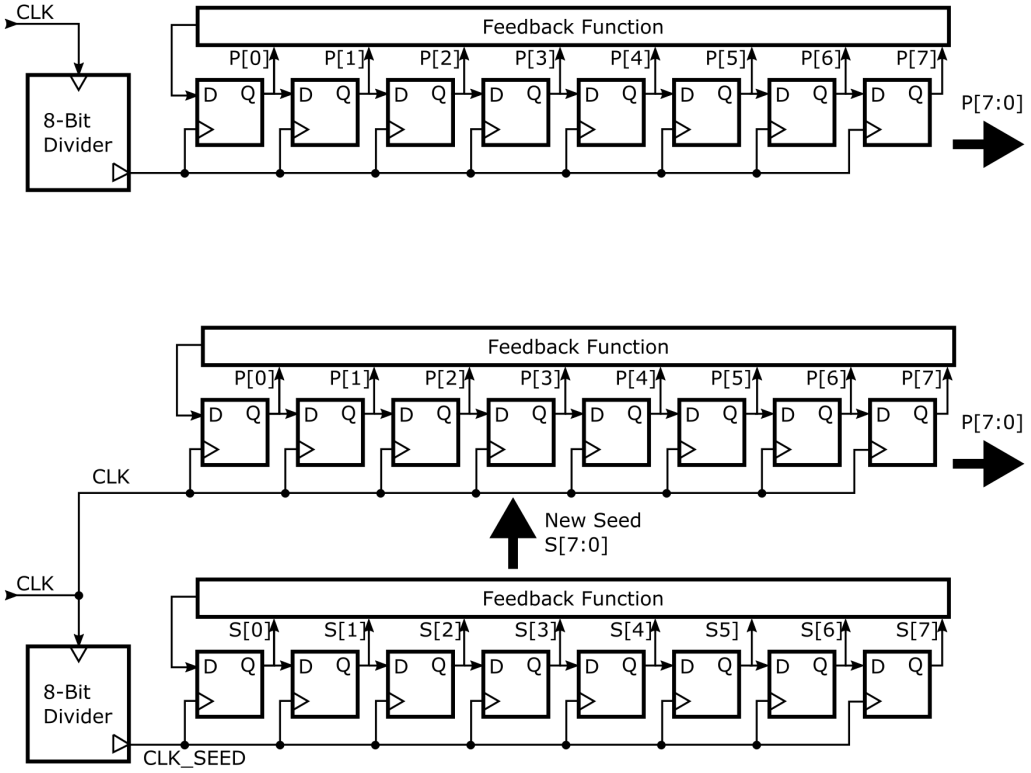


Figure 5.16.: Pseudo-random number generators. Top: A clock-divider is used to slow down number generation [13]; Bottom: Cascaded LFSR, a second LFSR is used to re-seed the main LFSR [150];

$256/f_{ave}$. The relaxation oscillator will thus output the same frequency for $T_p = 256/f_{ave}$. From the observation above, it can be concluded, that the energy of the generated emission is spread to a bandwidth of $2/T_p = f_{ave}/128$. In the case of [13] this results in a bandwidth of app. 1.7 kHz (f_{ave} =215 kHz [13]). Thus, during each frequency step, the energy of the emission is mainly concentrated in a narrow 1.7 kHz bandwidth. The emission of this Class-D are generated in CISPR Band-B. In this frequency range, the test-receiver uses a measurement bandwidth of 9 kHz. Hence no emission reduction with the peak detector will be observed.
With the average detector, an emission reduction will be measured. But this reduction is not caused from interference energy being spread to a larger bandwidth. The reduction with average detector is achieved, because a narrowband 1.7 kHz emission is changing its frequency. It is present only for a short time within the measurement bandwidth.

The situation is different with the cascaded LFSRs. In this case, random number generation is not slowed down. A new value is generated with a period of $1/f_{ave}$. Thereby, the oscillator changes its frequency much faster and the emission of the individual frequency steps is spread to much wider bandwidth. The theoretical zeros of the sinc's main lobe would span a bandwidth of 430 kHz (as before, f_{ave} =215 kHz). The individual sinc-shapes largely overlap creating a rather continuous energy distribution over a large bandwidth. This time, all weighting detectors will show an emission reduction, as the energy inside the 9 kHz measurement bandwidth is actually reduced.

The prototype from the last section was used again to demonstrate the findings. As before, the nominal frequency of the reference signal is 300 kHz, and the maximum deviation is ±60 kHz. The two SSM methods described above were tested. In the first case, random modulation was implemented with an 8-Bit LFSR and 8-bit clock divider. In the second case, a cascaded LFSR consisting of two 8-Bit LFSRs was used. Both methods generate a pseudo-random profile with a repetition rate of app. 4 Hz. Unfortunately, the memory of the used arbitrary waveform generator was not large enough to store the complete sequence. Thus, only a part of the sequence was used and the resulting sequence repeated with 60 Hz. Still, in the audio measurements, this restriction showed no impact. Fig. 5.17 shows measured THD+N. The cascaded LFSR solution shows significantly worse performance. Fig. 5.18 shows the spectrum of this setting. The in-band noise is significantly increased, leading to higher THD+N. However, this noise increases with input signal. The measured idle noise was 45 µVrms

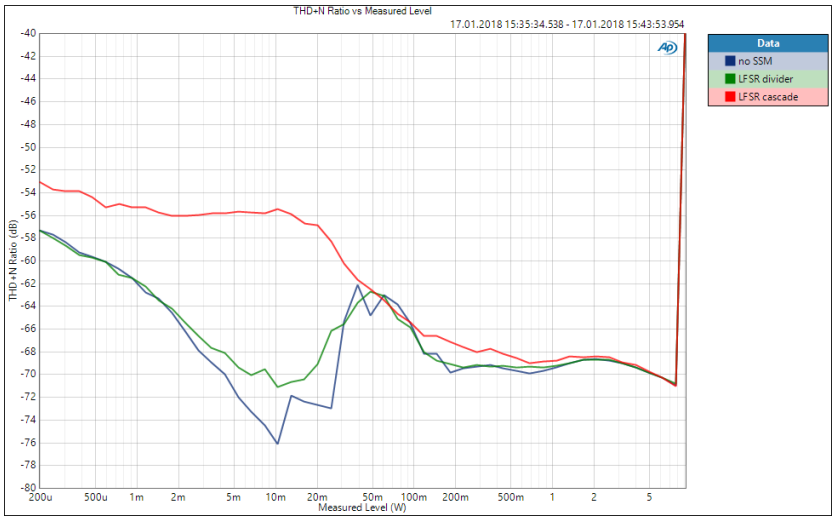


Figure 5.17.: Measured THD+N for randomized SSM.

in all settings and not affected by SSM. The in-band noise is thus linked to the input signal, with periodic SSM.

Fig. 5.19, shows the measured conducted common-mode emission of the prototype. The slow-running LFSR with divider does not spread the emission, thus no peak reduction is achieved. Moreover, the peak spectrum is significantly worsened, due to large emission filling the whole spectrum. Unfortunately, the restricted memory of the waveform generator shows some impact here. It can be seen, that some frequency steps of the LFSR with divider are not generated. In the correct case, the individual peaks would have a flat top. It can be concluded, that the method described in [13] is inadequate to spread the emission. As explained above, the average result is improved, because the emission are constantly moving. When measuring this method, a very long dwell-time of the test-receiver has to be used. Otherwise the test-receiver would *miss* some of the generated emission. As predicted, the fast running cascaded LFSR actually spreads the emission, leading also to peak reduction (3.6 dB at the first harmonic). For the same frequency deviation, randomized SSM achieves a lower reduction than periodic SSM. This is because in randomized SSM the energy is spread to a rather continuous spectrum. In periodic SSM, the energy can be spread to discrete sidebands. In this way, energy can be more effectively moved out of the receiver's bandwidth.

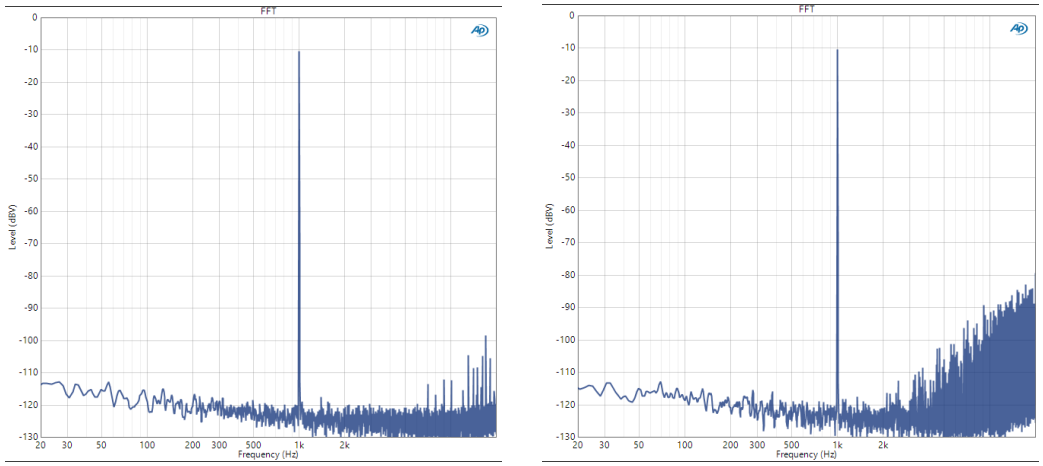


Figure 5.18.: Measured audio-band spectrum.
Left: without SSM; Right: SSM with cascaded LFSRs. THD+N is degraded by increased in-band noise.

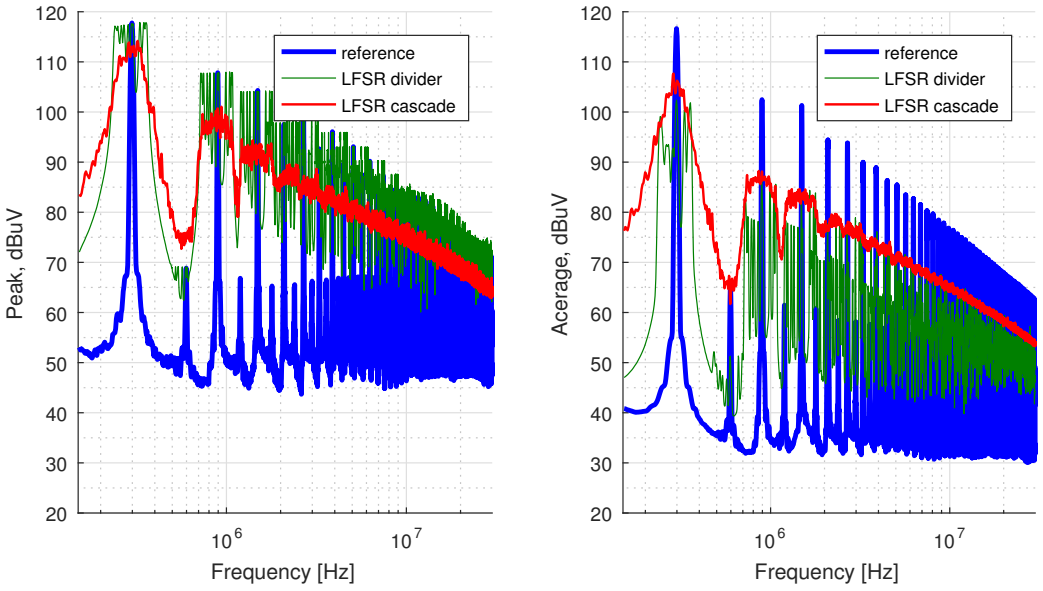


Figure 5.19.: Measured conducted common-mode emission with randomized SSM.

5.1.3. Common-mode modulation

The common-mode voltage noise on the outputs of a filterless Class-D amplifier is a direct result of the filterless operation. For filterless operation, the differential signal at the speaker needs to be a three level signal (-1,0,1). The differential zero-level is generated when both outputs have the same voltage. There are two ways to generate such a zero differential signal. In case Φ, both outputs are at the negative supply voltage. In case Ψ, both outputs are the positive supply voltage. In both cases, the differential voltage, which excites the speaker is zero. However, the common-mode voltage is equal to the negative supply voltage in case Φ, and equal to the positive supply voltage in case Ψ.

The generated common mode voltage can be modified by swapping the zero-representation [87]. Fig. 5.20 shows the principle idea. At time 2, the zero-representation is swapped. In the swapped case, the common-mode voltage is inverted. The figure clearly shows, that the differential signal seen by the speaker is not modified. The swapping should happen while the differential signal is zero, to avoid artifacts in the differential signal. This can be achieved easily, if swapping is synchronized to the reference signal in the modulator. This idea allows to modify the common-mode emission, without affecting the differential audio signal.

The circuit to swap the common-mode voltage is depicted in Fig. 5.20 [87]. It is inserted between modulator and power-stage. The circuit swaps and inverts the control signals, when requested by the control input S. In the work of [87], the swapping circuit is used to modulate the CM signal. A complicated sigma-delta loop with a specially shaped noise-transfer function is used. Thereby the emission in a certain AM-radio band is reduced. In this work, the idea is analyzed in more depth and a theoretical explanation of the resulting spectrum is derived. It will be shown, that the generated common-mode emission have a very predictable spectrum. No complicated sigma-delta loop is needed, to shape the spectrum. The control signal can be generated in a much simpler way, to achieve certain spectral shaping.

The inversion of the common-mode signal can be seen as 180° phase shift. Hence, the control input S of the presented circuit allows to modulate the common-mode signal's phase by $\pm\ 180^\circ$. In telecommunications, such a modulation is called *binary phase shift keying* (BPSK). The spectrum

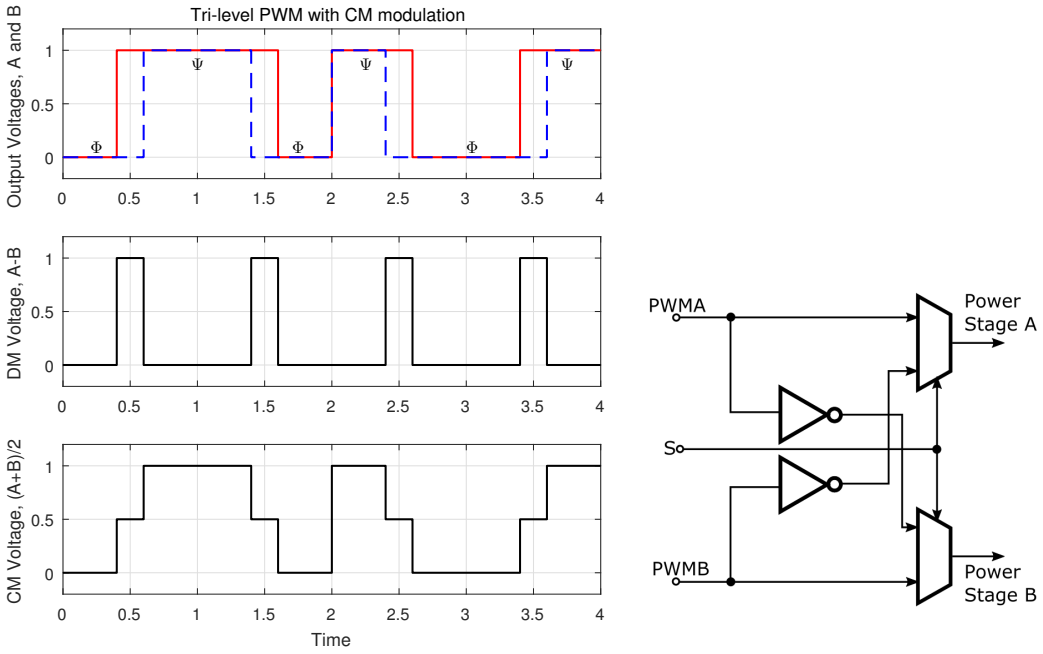


Figure 5.20.: Common-mode swapping
Left: Output voltage waveforms with common-mode swapping. At time 2, the zero representation is swapped.
Right: Circuit to change the zero representation.

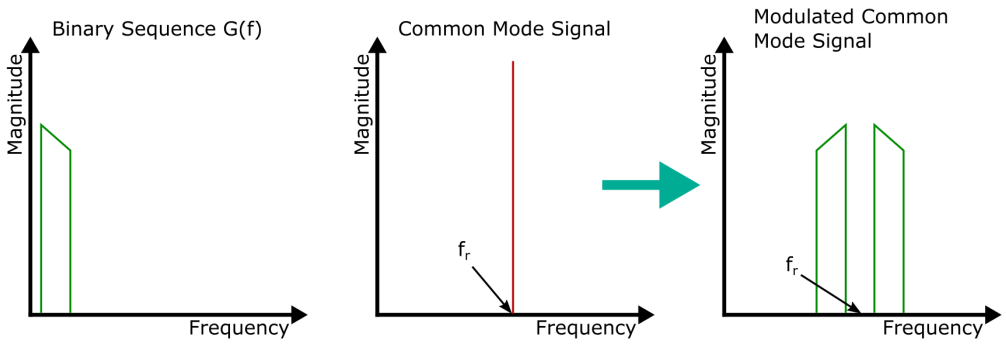


Figure 5.21.: Spectral representation of common-mode modulation.

of a BPSK signal is identical to *double-sided suppressed-carrier amplitude modulation* [158]. It is thus a linear modulation.

Let f_r be the switching frequency of the amplifier. A binary sequence $g[t]$ is applied to the control input S of the swap-circuit. $G(f)$ represents the spectrum of the sequence. The resulting spectrum of the common-mode voltage will then show no carrier signal at f_r, instead $G(f \pm f_r)$ will be disposed symmetrically on either side of f_r. The energy of the common-mode signal is distributed equally to these sidebands. Fig. 5.21 illustrates the principle. In contrast to frequency modulation, only two side-bands are generated.

Knowing this relation, the common-mode spectrum can be tailored to fulfill certain specifications. For instance the carrier can be suppressed completely, if $g[t]$ has no DC-component ($G(f = 0) = 0$). For best reduction with the peak detector, the binary modulating sequence $g(t)$ should have a line spectrum (similar to Fig. 5.23):

$$g(t) = \frac{1}{N} \sum_{n=1}^{N} \sin(2\pi f_x t) \tag{5.7}$$

The energy of the common-mode signal will be distributed to discrete lines, where each line is spaced by f_x apart. Best peak reduction is achieved, if f_x is chosen to be larger than 9 kHz. Such a binary sequence can be generated easily using a short LFSR.

In our work of [151], we have presented a digitally modulated Class-D amplifier (Fig. 5.22). The hardware overhead to implement CM-modulation

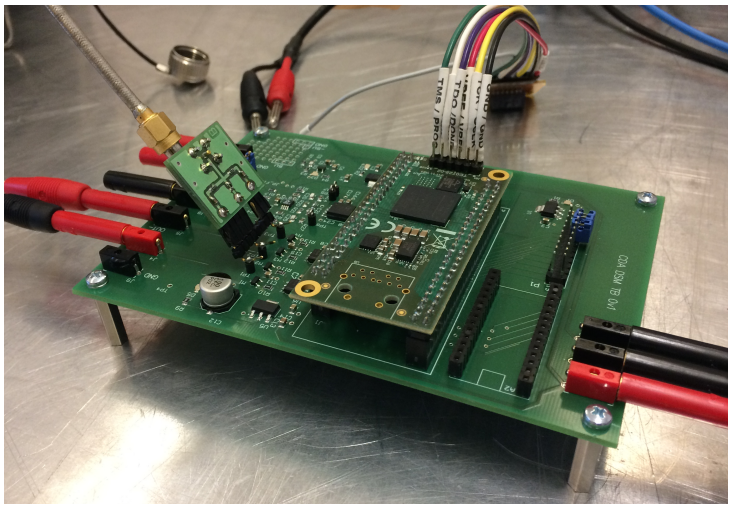


Figure 5.22.: Digitally modulated Class-D amplifier prototype, with CM modulation

is only a couple of digital gates, thus negligible. The prototype uses a 5 V supply voltage. It it operates at 390 kHz and can output up to 1.5 W to an 8 Ω speaker. The binary sequence $g(t)$ was generated using a 5-bit LFSR, which is clocked by the PWM's oscillator. The LFSR generates a pseudo-random sequence with a repetition rate of 12.6 kHz. Fig. 5.23 shows the spectrum of $g(t)$. It has a line spectrum to achieve good peak reduction. The spectrum has a sinc-shaped envelope, which results from the digital nature of the sequence. The resulting peak conducted common-mode emission are shown on the left side of Fig. 5.23. At the first harmonic an impressive reduction of 14.2 dB is achieved. The DC component of $g(t)$ is close to zero, hence the CM carrier is largely suppressed.

However, having a closer look at this technique reveals one significant drawback. Whenever the zero-representation is swapped, an additional switching transition of the power-stages is needed (at time 2 in Fig. 5.20). Each CM swapping thus introduces switching losses. As the switching losses depend on the load current, the impact on efficiency is hard to determine. Moreover, when a chaotic sequence is used, the event of swapping in relation to the load current is impossible to predict. However, an estimation can be made (appendix A.3). If the LFSR is clocked with the same rate as the PWM, the switching losses will increase by 25 % (appendix A.3). The LFSR can be slowed down by a factor K using a clock divider, to reduce losses. In this case, the switching losses will increase by app. $25/K$% (independent of LFSR length). However, in this case the

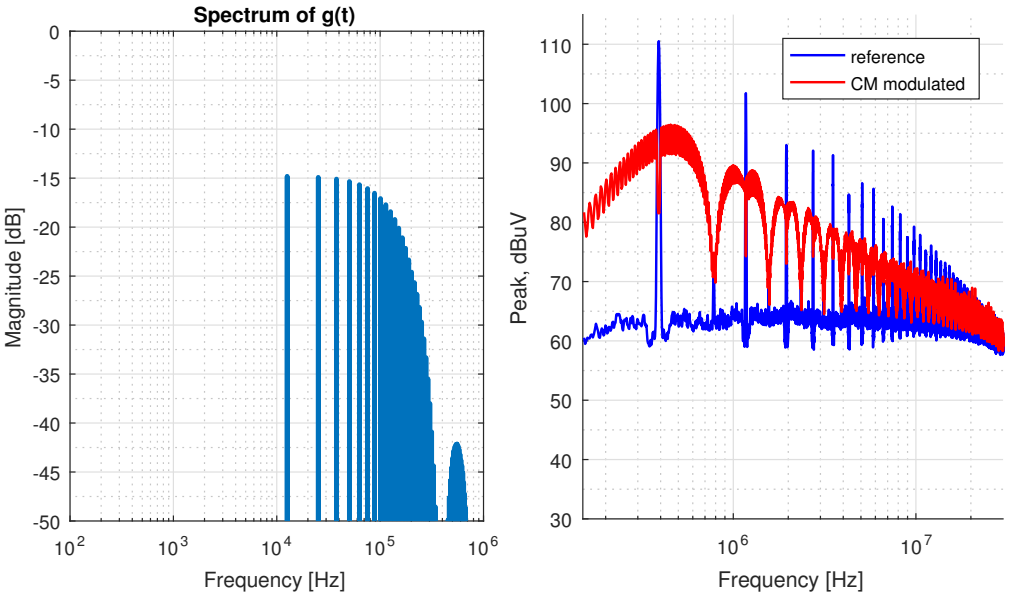


Figure 5.23.: Spectrum of the modulating sequence $g(t)$ and measured peak common-mode emission with CM modulation.

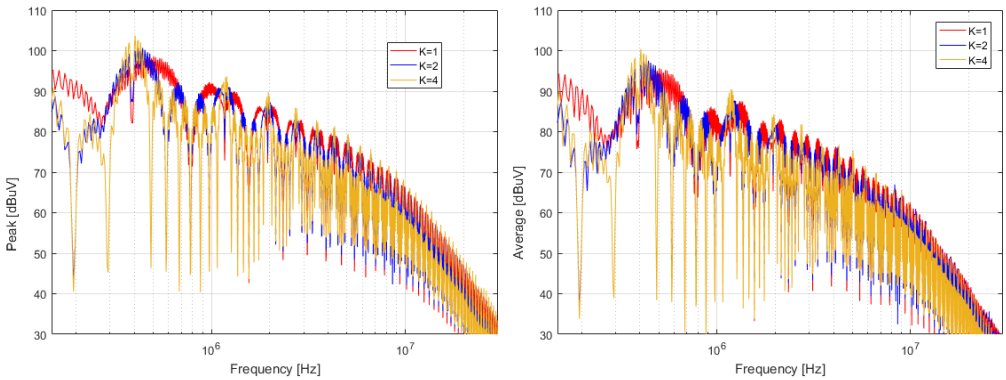


Figure 5.24.: Simulated common-mode emission with CM modulation. The binary modulating sequence has a line spectrum. Different clock dividers (division ratio K) are used, the repetition rate of the modulating sequence is kept constant by decreasing the length of the LFSR. Left: peak results; Right average results

spectrum of the generated bit-stream becomes narrower. This is because the zeros of the sinc-shaped envelope are located at multiples of $1/(T_{clk})$, where T_{clk} is the clock period of the LFSR. Longer clock period, leads to smaller bandwidth of the modulating sequence. The behavior is demonstrated with simulation results in Fig. 5.24. The simulation demonstrates the relation between emission spreading and switching losses.

5.1.4. Conclusion

This section presented spread-spectrum methods for Class-D audio amplifiers. A novelty of this work is that all SSM methods were strictly analyzed with standard compliant measurement equipment. In contrast to many previous works, the results in this work are therefore repeatable and comparable. Moreover, the emission reduction achieved at IC level, will also be measured in compliance tests at system level. The presented methods can therefore be used to actually pass legal emission limits.
Previous works used randomized SSM in Class-D amplifiers. Randomized SSM is also considered in this work and a novel implementation of a pseudo-random sequence generator was published by our research group [150]. Additionally, periodic SSM was investigated in depth. To study the emission reduction, adequate, yet intuitive theoretical models for both methods were derived in this work. These theoretical explanations can be directly used to determine the implementation parameters for each method. In particular, the derived simple explanations allow to optimize the methods for a certain measurement setup, as we demonstrated in several published works [121, 137]. The works prove that SSM can reduce the emission of Class-D amplifiers by up to 10 dB and 20 dB, for peak and average respectively.
Another novelty of this work is the investigation concerning SSM and audio performance. The impact of SSM on THD+N was studied using system-level models and prototypes developed developed in the course of this work. In this way, the effect of randomized and periodic SSM could be investigated in depth. Certain guidelines how to improve the audio performance were found [121]. It was shown that proper parameter choice for SSM can minimize degradation of THD+N. But, in turn emission increase. Hence SSM leads to a trade-off between emission reduction and audio performance.
Emission reduction and audio performance of periodic and randomized

SSM have been compared in this work for the first time. We published the results of this comparison in the largest conference on EMC in the Asian area [138] and the publication was awarded the *Best Student Paper Award*.

In contrast to SSM, CM modulation does not affect the audio performance. It affects only the common-mode component of the output signal. The idea was published previously. But to the author's knowledge, the resulting spectral properties of the modulation have not been explainde before. In this work the theoretical backgrund of the modulation was derived and the impact on power-efficiency was investigated for the first time. The modulated spectrum resembles amplitude modulation. This linear modulation allows a flexible way of shaping the common-mode component and requires very little hardware overhead, as we have shown in [151]. Optimized for peak measurements, an emission reduction of 14 dB is demonstrated with measurement results in this work. Unfortunately, the technique impacts the power efficiency. Hence the method leads to a trade-off between emission spreading and power efficiency.

The emission of PWM have larger amplitude, compared to other modulators and are concentrated in narrow bands. Using the spectrum shaping methods proposed in this section, this disadvantage can be overcome, as shown in our publications [121, 137, 150, 138]. Moreover, with the theoretical framework derived in this work, the distribution of the emission now becomes predictable and controllable.

5.2. Slew-rate control for Class-D amplifiers

Spectrum shaping techniques for Class-D amplifiers are only effective up to 30 MHz. Slew-rate control [106, 160] can help to reduce the emission at higher frequency. Thereby the transition speed at the output node (dV_{out}/dt) is slowed down. This increases rise an fall time of the voltage transitions. In turn high order harmonics of the switching signal (compare to eq. (4.1) in chapter 4.1) are reduced. Hence the method reduces the energy of the generated emission.

The concept of slew-rate control is widely used in digital communication [154]. Unfortunately, the method impacts power efficiency. Chapter 3 clearly shows that slower switching transitions lead to higher resistive

switching losses. Nevertheless, a certain reduction of the slew-rate may be feasible. The efficiency modeling approach presented in chapter 3.3 can be used to determine the slowest acceptable transition speed for a given efficiency specification. Then the according emission reduction can be determined before fabrication using simulation (compare to chapter 4.3).

Slew-rate control is realized by modified driver structures for the switching transistors. Drivers based on switches or drivers based on current sources can be both be used for slew-rate control [110]. In many Class-D designs, drivers based on switches are preferred due to smaller area on the silicon die. Additionally, the power-stage of a Class-D has to fulfill several requirements (compare to chapter 2.2.3). Shoot-through current needs to be avoided by non-overlap. However, to large dead time of the switching transistors leads to distortion. The initial delay, from the input of the power-stage until the output transition starts, should be small. The delay determines the minimum pulse length that can be generated at the output node. It adds unwanted phase-shift to the error correction loop. Moreover, it is a load current dependent quantity and thus contributes to distortion. A smaller delay will reduce its impact on distortion.

Slew-rate control has been implemented to Class-D amplifiers before. The power-stage in [87] uses large feedback capacitors between gate and drain of the switching transistors. The capacitors prolong the Miller plateau during switching transitions and reduce the slew-rate. However, the capacitors increase the capacitive switching losses and need a lot of area on the silicon die. In [90] an inverter based gate driver is used. The transition speed is reduced by adding source resistors to the gate drivers. This method effectively reduces high-frequency emission, but increases the initial delay.

In this work, a power-stage with reduced slew-rate and short initial delay is proposed. We published the work already in [161]. The power-stage incorporates a variable driver strength. The driver current can be modulated during switching transitions, to have a short initial delay combined with a moderate slew-rate. The driver dynamically adjusts the needed non-overlap at each switching transition. Thereby dead time is strongly reduced, while taking into account the varying load current. The proposed power-stage is shown in Fig. 5.25. The circuit is intended for supply voltage larger than 10 V and hence consists of two large NMOS switching transistors. The high-side driver is supplied with an external bootstrap capacitor. The driver blocks consist of several drivers in parallel, each

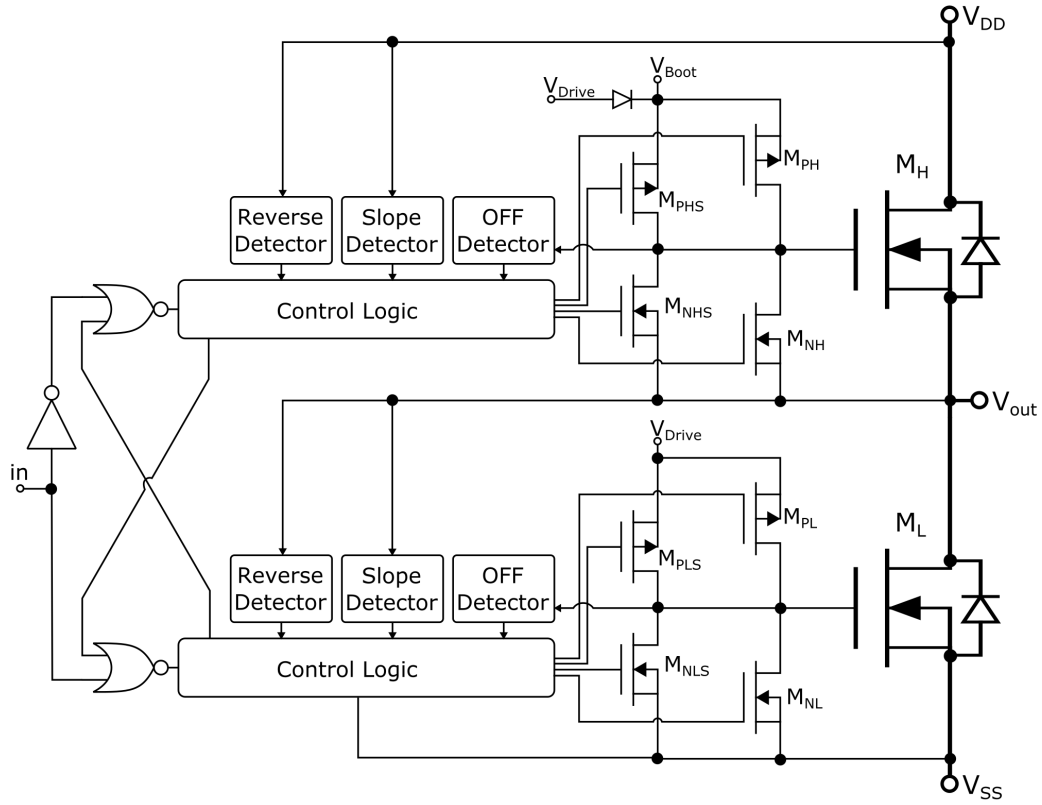


Figure 5.25.: Proposed, slew-rate controlled power-stage.

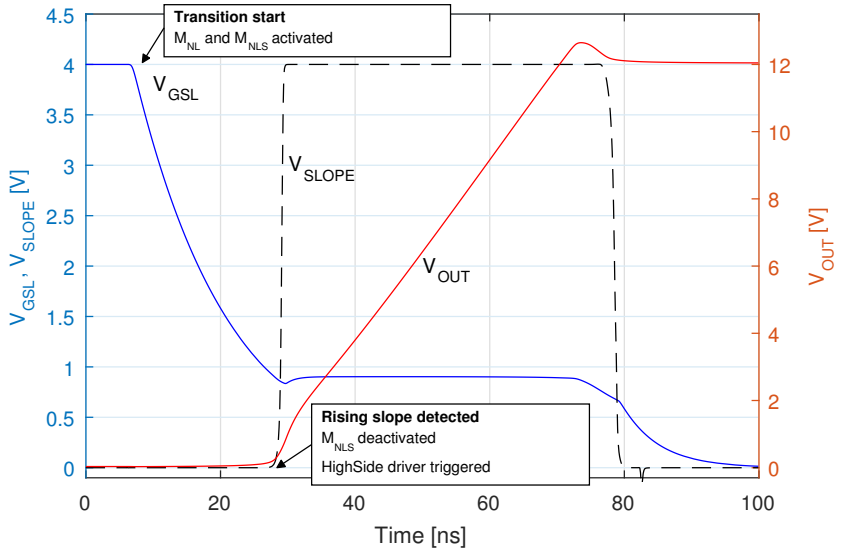


Figure 5.26.: Simulated waveforms during turn-off controlled switching.

with different strength. Three detectors are used to monitor the switching transition. The shown reverse detector indicates, when the body diode of a switching transistor starts to conduct. The circuit presented in [83] is used for this purpose. The off detector monitors the gate voltage of the switching transistor. It signals when the gate voltage of the switching transistor is below its threshold voltage. Finally, the slope detector indicates when the actual voltage transition at the output node starts. The control logic then activates the different drivers as needed during the different phases of the switching transition. Non-overlap between the drivers is implemented with a few logic gates. The control logic decides for the non-overlap dynamically.

In Class-D amplifiers with full-bridge power-stage, two switching scenarios can be identified. In turn-off controlled transitions, the output voltage automatically transitions to the opposite supply rail, when switching OFF the first switch. In turn-on controlled transitions, the load current continuous flowing trough the body diode of a switching transistor. Only when turning ON the opposite switch, the voltage transition starts.

For turn-off controlled transitions the slope detector is used to monitor the switching transition. It enables a short initial delay and a reduced slew-rate of the switching transition. The simulated waveforms for an upward transition are shown in Fig. 5.26. Initially, the low-side switch M_L

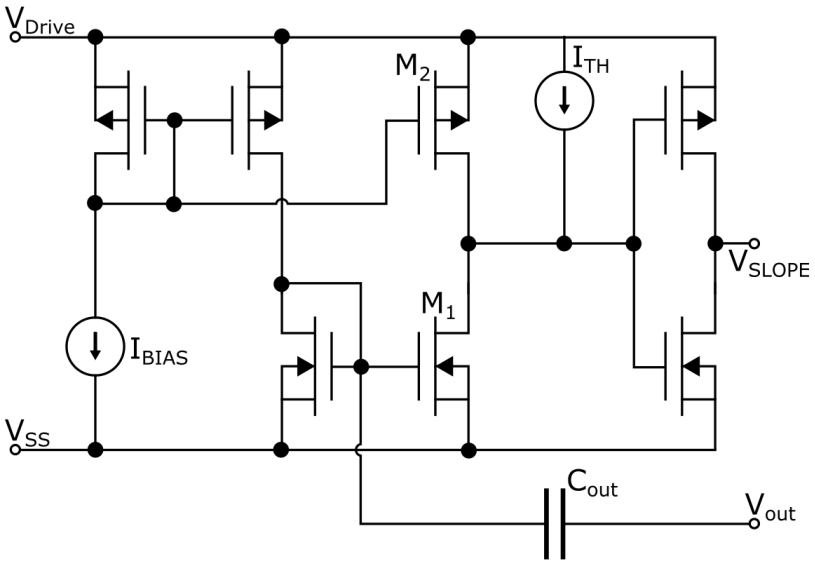


Figure 5.27.: Slope detection circuit.

is ON. The speaker current flows from the load into the power-stage to V_{SS}. At the start of transition, the control logic activates both pull-down drivers M_{NLS} and M_{NL}. Hence the gate of M_L is discharged with a large current, for short initial delay. When M_L enters the saturation region, the output voltage V_{out} starts to rise. The slope detector triggers at this rising voltage. At this trigger signal, the control logic deactivates one of the drivers, M_{NLS}. During the transition, the slew-rate is thus only controlled by the weaker driver M_{NL}. Additionally, the control logic signals to switch ON the high-side driver. The high-side driver's pull-up M_{PH} is activated. This pull-up M_{PH} is sized according to [89], it is slightly weaker than M_{NLS}. It precharges M_H close to its threshold voltage, but cannot switch M_H ON, due to displacement current in its gate-drain capacitance. Hence, no shoot-through current occurs. Once the output voltage has reached V_{DD} potential, M_H turns on completely. Additionally, a stronger pull-up M_{PHS} is activated, to quickly charge the gate of M_H. With this control algorithm, the driver current at the initial discharge phase is decoupled from the current during voltage transition. This allows to have a small initial delay but a limited slew-rate and the dead time is reduced to a minimum.

Fig. 5.27 shows the circuit of the slope detector. The capacitor C_{out} is connected to the output node. Voltage changes (dV_{out}/dt) at the output

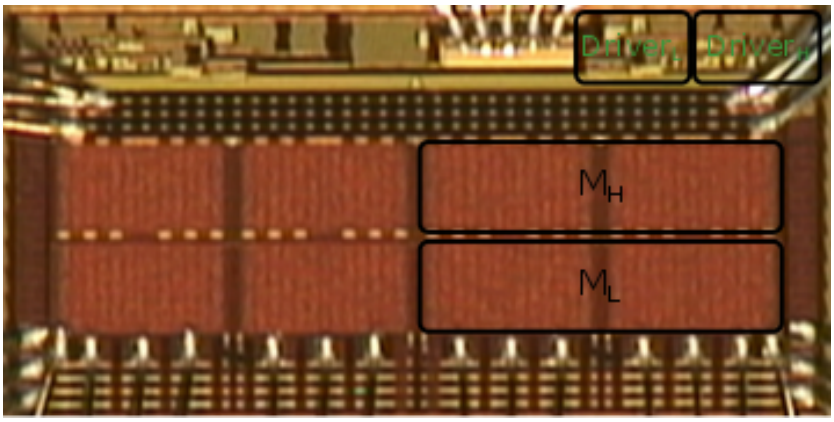


Figure 5.28.: Photograph of the implemented power-stage.

node generate a proportional displacement current through C_{out}. This proportional current is mirrored to M_1 where it is converted to a voltage by the parallel output resistance of M_1 and M_2. The current source I_{TH} provides a threshold for detection. The circuit triggers for rising output voltage with a slew-rate larger than I_{TH}/C_{out}. The circuit can be build of low-voltage transistors, which helps to build a high-speed circuit. Only the capacitor C_{out} has to withstand the output voltage. The detector must be fast enough to generate the signal for the control logic in time. But average power-consumption can be reduced, as the circuit can be switched off most of the time. It is needed only during switching transitions.

At very small load currents, the voltage gradient might be too small to trigger the slope detector. For this case, the off detector is used as a backup solution. The off detector monitors the gate voltage of M_L. The off detector triggers the control logic, when the output voltage has not started to rise up, even though the gate voltage is already below the threshold voltage.

For turn-on controlled transitions, the switching concept presented in [83] is employed. The reverse detector is used to detect the start of diode conduction. The control logic then triggers the high side driver and activates the according pull-ups. Again, the off-detector serves as a backup. It triggers the logic, if diode conduction is not detected due to light load current.

The proposed concept was implemented in a Class-D power-stage by the author. A 180 nm CMOS technology was used. The technology provides laterally diffused DMOS transistors which were used for the switching

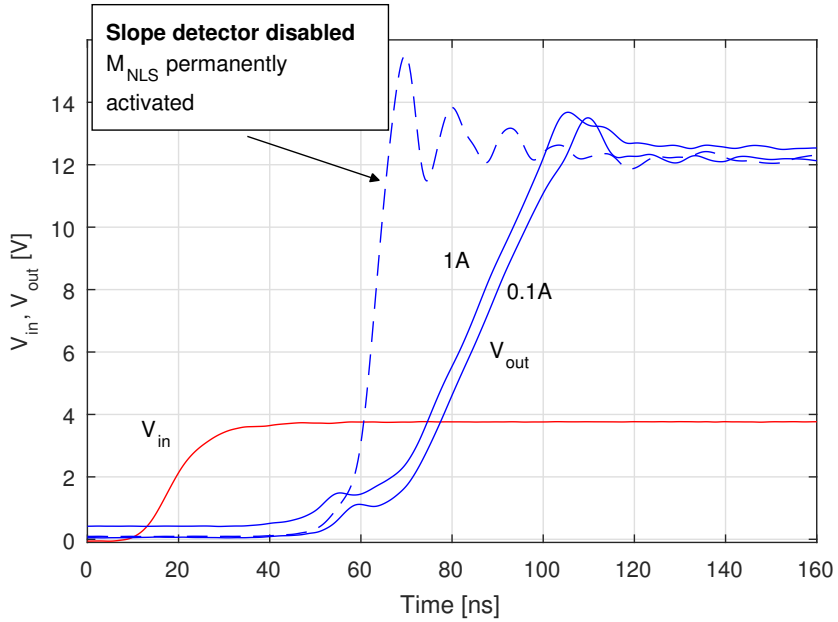


Figure 5.29.: Measured waveforms during turn-off controlled switching.

transistors. The supply voltage for the power-stage is 12 V to 15 V. It is designed to output up to 10 W into 8 Ω speakers. Above, the slope detector was described in detail. In this implementation a 270 fF sense capacitor is used. The detector consumes 30 µA. Fig. 5.28 shows a photograph of the fabricated silicon die.

Fig. 5.29 shows the measured waveforms of the turn-off controlled transition. The solid lines show the input and output voltage waveforms of the power-stage. The waveforms are shown for 1 A and 0.1 A of load current. A small glitch can be seen, where the control logic deactivates the strong driver M_{NLS}. In a third measurement, the slope detector was disabled. In this case, the driver current is not reduced at the start of transition. The dashed line shows the resulting output voltage for 0.1 A of load current. A large voltage gradient occurs, excessive ringing can be seen. Hence, the proposed power-stage reliably reduces the slew-rate, without increasing the initial delay. The initial switching delay of this implemented circuit is 35 ns to 40 ns. Without using the strong driver M_{NLS} at the beginning, it would be approximately 120 ns to 140 ns (predicted by simulation).

The reduction of high-frequency energy was verified with an emission measurement using the 150 Ω direct coupling method. Only a single power-stage was measured, to see the effect of slew-rate control. The stage

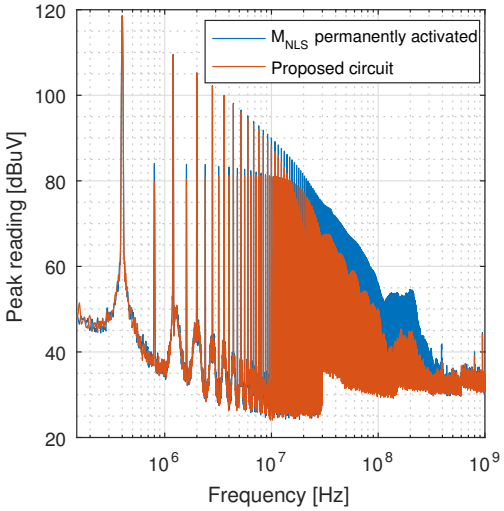


Figure 5.30.: Measured waveforms during turn-off controlled switching.

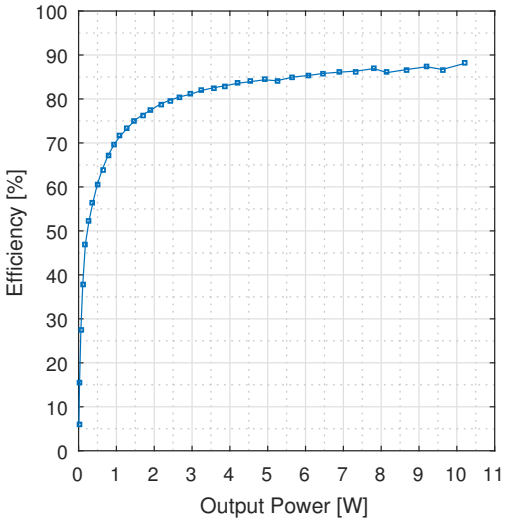


Figure 5.31.: Measured power-efficiency with the speaker dummy and a switching rate of 300 kHz.

was loaded with the speaker dummy. Fig. 5.30 shows the measured results. Additionally, the result with non-controlled slew-rate (slope detector deactivated) is shown. Above 30 MHz, reduction constantly larger than 5 dB is visible, with a maximum of 18 dB at 120 MHz. Fig. 5.31 shows the measured efficiency using two power-stages in a Class-BD configuration.

5.2.1. Conclusion

Slew-rate control is a well known method to reduce emission in power-stages. Previous implementations of slew-rate control in Class-D power-stages have increased the switching delay, or needed large feedback capacitors. In this work a new implementation of a slew-rate controlled Class-D power-stage is proposed. It allows to control the slew-rate of the output voltage independent from the initial switching delay. A detector circuit is developed which is used to determine the start of a switching transition. This detector does not need high-voltage transistors and can thus be used in many technologies. The detector circuit is also used to dynamically decide for the needed dead-time in turn-off controlled transitions. Hence a new and robust way to reduce dead-time in Class-D power-stages has been found. The feasibility of the concept was demonstrated with an integrated prototype designed by the author. The results were published

in a well-respected circuit design conference [161]. Measurement results of the prototype showed emission reduction of up to 18 dB compared to non-controlled slew rate. However, a trade-off between emission reduction and power efficiency has to be made. Fortunately, this trade-off can be carried out before production, using the simulation tools presented in this work.

5.3. Digitally enhanced amplifiers

Audio sources have become almost entirely digital. Hence, there is a growing demand for audio amplifiers with digital input but high-fidelity performance and good power efficiency. Class-D amplifiers with a digital input are thus needed. Additionally, analog integrated design becomes increasingly difficult with still ongoing shrinking of technology. Hence, in recent research, digital input Class-D amplifiers and analog input, mixed-signal amplifiers get a lot of attention. Digital input Class-D amplifiers perform digital to analog conversion and power amplification in one circuit, such as [27, 162]. In analog input mixed-signal amplifiers, certain blocks (such as PWM and loop-filter in [28]) are implemented in the digital domain. In most cases, these digitally enhanced amplifiers are based on PWM [25, 27, 162, 28, 29], due to the better noise and efficiency performance compared to other modulators. Hence, this section focuses on Class-D amplifiers with digital PWM.

5.3.1. Digital pulse width modulator with SSM

Similar to analog PWM, a digital PWM can be implemented by comparing a digital input signal $x[m]$ to a reference signal $r[n]$. This reference signal can be generated using a clocked counter that outputs a digital sawtooth or triangular signal. In contrast to analog PWM, the digital reference signal is quantized in amplitude and time. It can be regarded a stair-step approximation of the analog reference signal, with N_S different steps. Using a clocked synchronous counter, the number of different steps N_S is limited by the clock frequency f_{clk}:

$$N_S = \frac{f_{clk}}{k f_r} \qquad k = \text{ 1 for sawtooth, 2 for triangle} \tag{5.8}$$

For a given repetition rate f_r of the reference signal, the reference signal is quantized into N_S steps. Accordingly the output signal of the PWM can only take N_S different duty-cycle values. Hence digital PWM is limited by quantization noise. The PWM resolution is limited by the digital clock, such that the counter is typically clocked with the fastest clock available in the electronic system.

In analog PWM, SSM is implemented by varying the frequency of the reference signal. The same can be done in digital PWM. Following eq. (5.8), this can be done in two ways. The digital clock frequency f_{clk} can be modulated, or the number of counter steps N_S can be varied. Modulating the digital clock is possible by using SSM clock sources [163] or SSM phase locked-loops [164]. However, this method affects all blocks, which use the same clock. The varying clock impacts timing constraints of digital blocks and might deteriorate the noise performance of mixed-signal blocks. Moreover, the achieved spreading effect is limited due to the digital clock division caused by the counter. Nevertheless, the idea might be used in certain applications and can lead to a reduction of EMI. This was demonstrated in our published work of [151], using a rapid prototype with digital PWM (Fig. 5.33).

Modifying the number of counter steps N_S allows to implement a more flexible SSM approach, without affecting other circuit blocks of an electronic system. Thereby, the upper and lower bounds of the counter are modified, either periodically or pseudorandomly. Following eq. (5.8) the repetition rate of the reference signal is modulated. The idea was proposed in [149] for PWM in digitally modulated DC-DC converters. The authors used pseudo-random modulation profiles. However, the work did not consider one drawback of the method. When N_S is changed, also the mapping from a digital input value to a resulting duty-cycle is modified. This might be acceptable for a DC-DC converter. With a pseudorandom modulation profile, that has an average close to zero, the average output voltage of the converter will not change. For a Class-D amplifier the audio performance will suffer significantly from this behavior. The constantly changing transfer characteristic of the digital PWM will introduce errors to the audio signal.

A modified version of this method makes it suitable for Class-D amplifiers. The proposed modification is covered in detail in our published work [165]: The generated error in the duty-cycle is deterministic. A correction circuitry can be used to suppress the error. The correction is explained with

the following example: In a digital PWM, a counter is used to generate a reference signal with N_{S0} steps. The PWM processes an input signal $x[m]$, which can range from 0 to N_{S0}. The PWM maps the input signal to a duty-cycle D according to:

$$D = \frac{x[m]}{N_{S0}} \tag{5.9}$$

If the counter is modified to have N_{Sx} steps, then a erroneous duty-cycle will be generated:

$$D_{err} = \frac{x[m]}{N_{Sx}} \tag{5.10}$$

This error can be suppressed by multiplying the input value with a correction factor. The new input value $x'[m] = x[m]\ (N_{Sx}/N_{S0})$ will lead to the correct duty-cycle:

$$\frac{x'[m]}{N_{Sx}} = \frac{x[m]\ N_{Sx}}{N_{Sx}\ N_{S0}} = \frac{x[m]}{N_{S0}} = D \tag{5.11}$$

In the case of digital PWM with SSM, N_{S0} is the average number of counter steps. N_{Sx} is the actual size of the counter during SSM operation. The input value $x[m]$ needs to be scaled with a factor N_{Sx}/N_{S0} to correct for the introduced errors. The correction circuitry can be implemented either with a look-up table, or a multiplication and division. Both methods were compared in terms of implementation effort and power consumption. The comparison was done for a digital implementation in 180 nm CMOS technology and a supply voltage of 1.8 V. The digital PWM was based on a 7-bit up-down counter running at 100 MHz. It turned out, that using a multiplier is favorable over the look-up table based solution. The division can be implemented as a shift-operation if N_{S0} is a multiple of two. Thus only a multiplier is needed, which outperforms the look-up table in in terms of area and power-consumption in this case. The comparison is described in detail in our published work [165].

The proposed method was than demonstrated using a mixed-signal Class-D amplifier prototype, built in the course of this work. The rapid-prototype is an analog input Class-D amplifier with digital PWM. An FPGA was used to implement the digital PWM. The digital PWM uses a 7-bit up-down counter to generate the reference signal. It is clocked with 100 MHz and incorporates periodic SSM. As described above, SSM was implemented by changing the number of counter steps. The synchronous counter starts

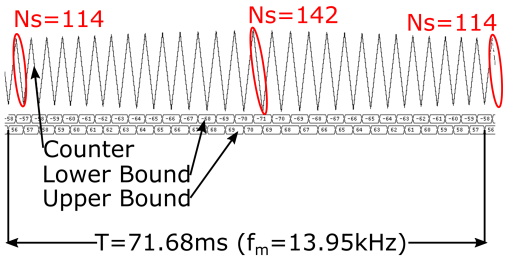


Figure 5.32.: VHDL simulation of the implemented SSM reference generator.

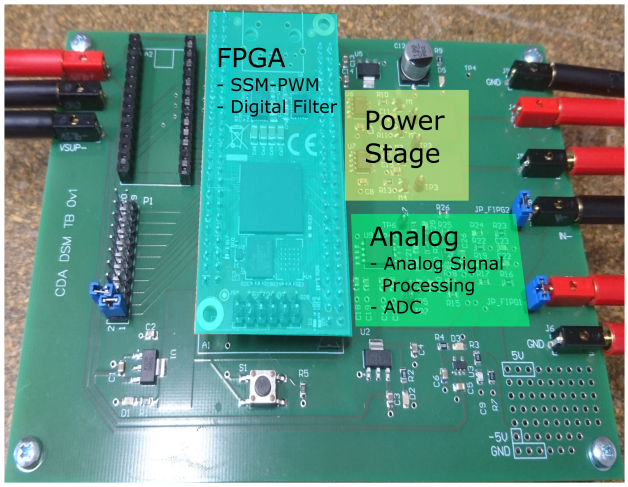


Figure 5.33.: Picture of the digitally modulated Class-D amplifier prototype.

from a lower-bound and then counts up to an upper bound. When it reaches the upper bound, it counts down again to the lower bound. Thereby a digital, triangular reference signal is generated. By shifting the upper and lower bounds, the number of steps N_S are modified to change the counter's repetition rate. Fig. 5.32 shows a VHDL simulation of the counter. Changing the bounds, periodic SSM with a triangular modulation profile is achieved. The digital PWM is used to drive an external discrete power-stage. The switching rate is 390 kHz$\pm$43 kHz. Figure. 5.33 shows a picture of the prototype. The prototype also incorporates a mixed-signal, global feedback-loop, similar to the one proposed in [28]. The feedback-loop uses an analog to digital converter to measure the output signal. A digital high-order loop-filter is implemented to reduce distortion and to perform quantization noise shaping. The prototype is loaded with the speaker dummy. Fig. 5.34 shows the measured conducted common-mode emission of the prototype. The performance of the correction circuitry was evaluated by measuring the THD+N (Fig. 5.35). Without correction, THD+N increases by more than 20 dB. The global-feedback loop is unable to suppress the generated duty-cycle variations. Moreover, the amplifier starts to saturate much earlier. This is because the transfer characteristic of the PWM is not constant, such that the loop filter easily saturates the PWM.

With the error-correction method derived in this work, the penalty on audio performance is nearly canceled. The peak THD+N is improved by 20 dB. The remaining penalty in THD+N compared to the unmodulated case is about 3 dB. It is caused by intermodulation tones, as extensively discussed in the last section. Furthermore, the proposed method restores the complete operation range of the amplifier.

5.3.2. High performance digital PWM

Digital PWM introduces quantization noise. Noise and distortion can be addressed by implementing a mixed-signal global feedback loop as proposed in [28]. However, such a feedback loop needs an analog to digital converter. In this case, the performance limit is shifted to this ADC. Moreover, in some applications a completely digital high performance PWM is needed.

To build a digital PWM with 16 bit resolution, a reference signal with

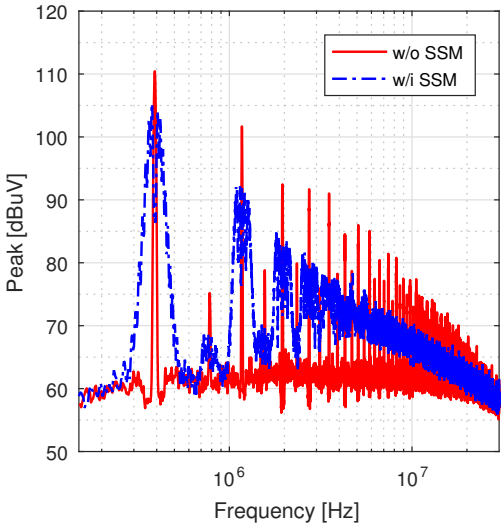


Figure 5.34.: Measured conducted common-mode emission of the digitally modulated prototype.

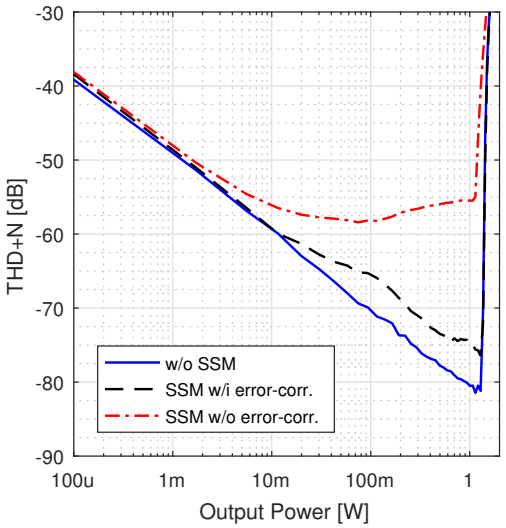


Figure 5.35.: Measured THD+N for a 1 kHz signal.

$N_S = 2^{16}$ steps is needed in the simplest case. If the PWM is intended to operate at 400 kHz, the reference signal needs $N_S = 2^{16}$ and f_r =400 kHz. According to eq. (5.8) a counter with a digital clock of 52.4 GHz has to be implemented. Such a high clock rate is unfeasible. A common solution to lower the clock speed, is to apply noise-shaping as used in $\Delta\Sigma$ converters [166, 33, 27]. Thereby, the input signal is first noise-shaped to a lower resolution and then applied to a low resolution PWM (e.g. 7 Bit). The resulting quantization noise is thereby shaped outside the audible region. Fig. 5.36a shows the principle. Good audio-band resolution can be achieved with this method. However, the filter $H(z)$ in the noise-shaper should be designed carefully. [167] shows that quantization noise shaped close to f_r will be fold to the audible region in the PWM thereby increasing in-band noise.

Noise shaping helps to implement a high resolution digital PWM. However, the input signal to the PWM is quantized in time. This leads to distortion [33] in the PWM encoding. In contrast to analog PWM, digital PWM is thus not linear for the baseband signal. Moreover, in most implementations, the input signal is sampled at a lower rate than the reference signal. This significantly reduces power consumption and implementation effort. In several implementations [27, 29], the input signal $x[m]$ is sam-

pled at a rate of f_r. One new input value is provided per period of the reference signal. For this case, the distortion generated in the baseband can be calculated as proposed in [51] or [49]. For digital BD-modulation with triangular reference signal, the amplitude of generated odd-order harmonics relative to the input signal is:

$$HD_n = 20\log_{10}\left(\frac{4\ J_n\left(n\ \pi\ f_{sig}\ A\ \frac{1}{2f_r}\right)}{n\ \pi\ f_{sig}\ A\ \frac{1}{f_r}}\sin\left(\left(\frac{f_{sig}}{f_r}+1\right)\ \frac{n\ \pi}{2}\right)\right) \quad [dBc] \tag{5.12}$$

with the order of the harmonic n, the Bessel function of the first kind J_n, the input signal frequency f_{sig} and amplitude $A\epsilon\,[0;1]$.

In some publications, this distortion is tolerated. For example in [27] a noise-shapped PWM with a reference signal frequency f_r of approximately 400 kHz is used. For a typical datasheet measurement with an input signal of 1 kHz and amplitude 0.8 FS, the third harmonic is acceptably small at -110 dBc below the fundamental (eq. (5.12)). However, at 6 kHz the third harmonic has already grown to -79 dBc (which is not shown in the publication). Hence measures to reduce the distortion at higher input frequency are needed. One possibility is to use pre-distortion [168, 169]. Thereby, the input signal $x[m]$ is modified to improve linearity. However, these methods have to be implemented before noise-shaping. Hence they have to operate on data with high resolution and typically involve significant computational complexity. Another possibility is proposed in [170]. The digital PWM can be used as a quantizer in the noise-shaper (Fig. 5.36b). In this way, distortion induced in the PWM is suppressed by the open-loop gain of the noise-shaper. However, in this case the noise-shaper has the be clocked at the same high rate as the PWM, leading to high power consumption. In order to reduce the clock speed of the noise-shaper, a decimation filter can be inserted into the feedback path as suggested in [171]. However, the authors in [171] use a multi-tap FIR decimator and admit that loop stability is very difficult to achieve. Moreover, the FIR decimator now has to operate at the high clock speed of the PWM. Hence it will consume a lot of power.

In this work a feasible solution is proposed. The PWM is integrated into the noise-shaping loop for minimum baseband distortion. As proposed in [171] a decimation filter is used in the feedback path to reduce power consumption. But a simple, single stage CIC [172] decimator is proposed. This simple decimation filter adds only very small delay to the feedback

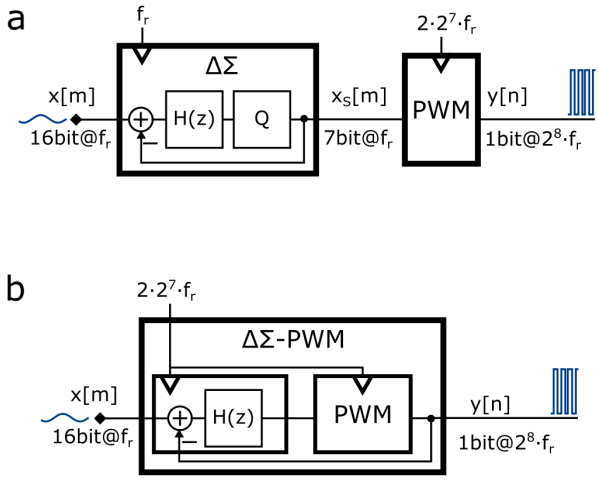


Figure 5.36.: Different implementations of a noise shaped digital PWM.

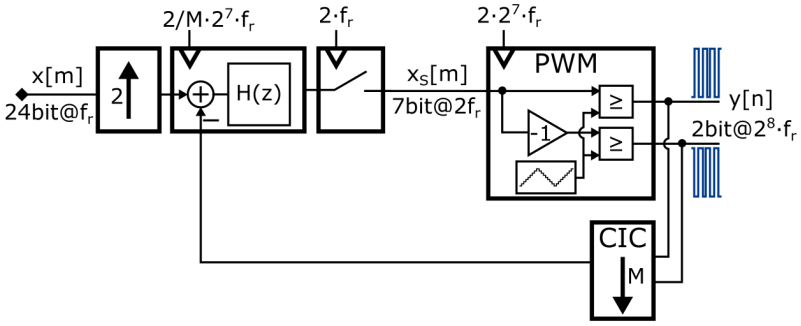


Figure 5.37.: Proposed high-performance digital PWM. BD-modulation is implemented.

loop, to ensure stability. Moreover, the decimator needs only a single accumulator with small bit-width running at the high clock frequency. This keeps power consumption low. To further reduce the delay in the loop, a new input value $x_S[m]$ is generated at each rising and falling slope of the reference signal. We thus generate a PWM signal using two signal samples per reference period. It helps to achieve a stable noise-shaping loop even for high input amplitudes. Additionally, applying two samples per reference period cancels even order distortion [51] of the PWM. Moreover it cancels the intrinsic distortion of the negative feedback loop [94].

The proposed circuit is implemented in 180 nm CMOS technology. A

synchronous design with thin-oxide transistors is used to realize a high-performance BD-modulated PWM. Fig. 5.37 shows a detailed block diagram. The digital PWM uses a triangular reference signal with 128 steps. The reference signal is generated using a clock of f_{clk} =100 MHz. This results in f_r =390.625 kHz. A fifth order loop filter is used for noise-shaping. The filter was designed using the well known *Schreier Toolbox* [56] for $\Delta\Sigma$ converters. The implementation uses two's complement number representation with standard carry-ripple-adders. The loop-filter's coefficients are quantized to fractions of two, such that all multiplications are implemented using shift operations. At the onset of instability, the filter order is reduced to recover stability. The filter has a moderate out-of-band gain to reduce noise foldback by PWM [167]. The noise-shaper is clocked at one eight (12.5 MHz) of the PWM rate which significantly reduces power consumption. The output of the filter is sampled with $2f_r$ and provided to the PWM. The input signal is interpolated from f_r to $2fr$ using a polyphase FIR interpolator. The output of the PWM is fed back to the loop-filter using the proposed, simple CIC decimation filter.

Fig. 5.38 shows simulation results of the proposed high performance PWM. As can be seen, the harmonic distortion is worst at around 6.5 kHz, but THD+N is still below -95 dB, thanks to the feedback. If the PWM was not incorporated in the feedback loop (as in [27]), THD+N would rise up to -74 dB. Fig. 5.39 shows the output spectrum. Dither is currently not added to the noise-shaper, but could be used to mask the sub-harmonic spurs. The required power is estimated by the synthesis tool using appropriate toggle values for each net. The toggle values are generated by simulation using a 24 bit, 1 kHz input signal. The circuit consumes 760 µW at a supply voltage of 1.8 V. Comparison to related work is difficult, as the power consumption of the PWM block alone is typically not stated. Related digitally modulated Class-D amplifiers [27, 28] have a total quiescent power consumption of 7 mW to 10 mW.

5.3.3. Mixed-signal error correction

The previous section describes a digital PWM that enables good noise performance and high linearity. When the generated PWM signal is applied to a power-stage, a high power digital to analog conversion is performed. In this way, a digital input Class-D amplifier is realized. Unfortunately, a real power-stage will introduce distortion to the audio signal and couple power

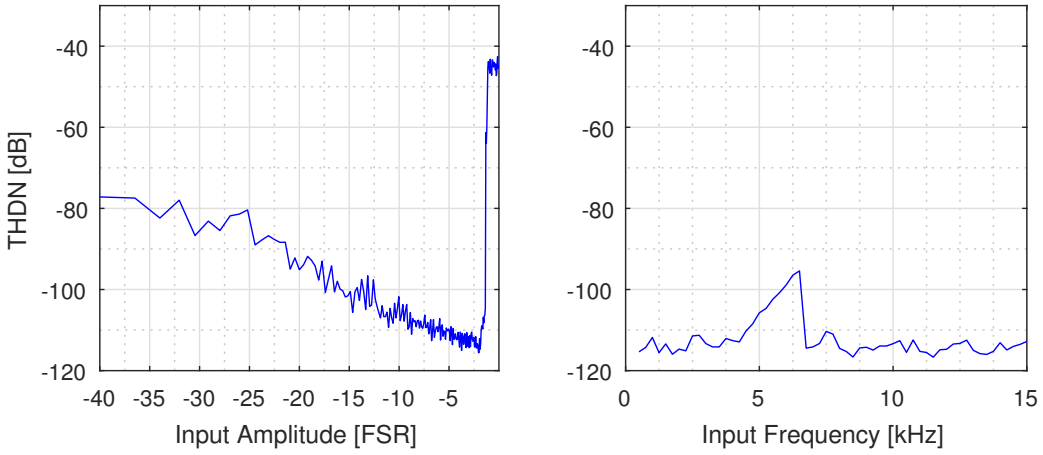


Figure 5.38.: Simulated THD+N: Left: THD+N vs. amplitude at 1 kHz; Right: THD+N vs. frequency at 0.8 FSR

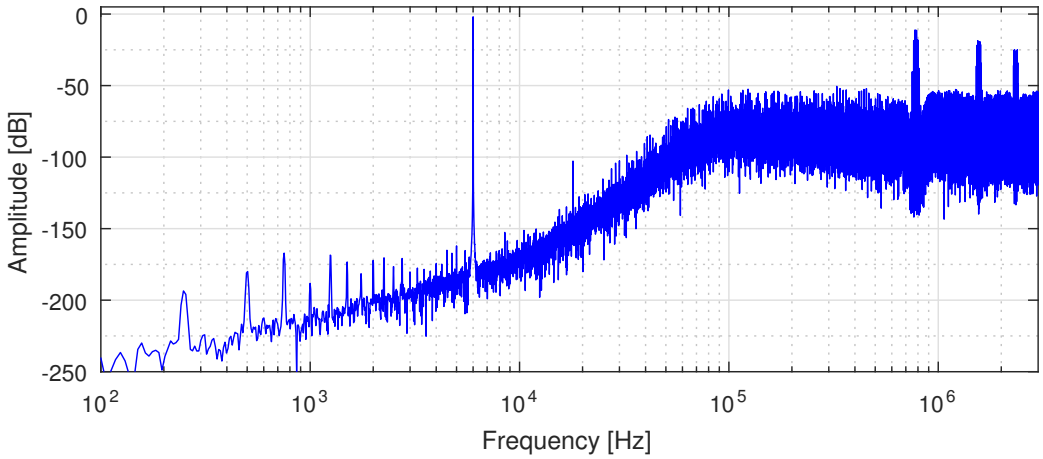


Figure 5.39.: Spectrum of a 6 kHz, 0.8 FSR differential output signal (frequency resolution 6 Hz)

supply perturbations to the output. Hence, error correction is needed. In [27] a completely analog, local feedback loop is employed to suppress the power-stage errors. However, the shown implementation cannot compete with analog Class-D amplifiers in terms of audio performance. Good audio performance is achieved in [28]. A mixed-signal, global feedback loop is proposed, where an ADC is employed in the feedback path to digitize the output signal. As mentioned before, the ADC is the limiting circuit in this case. The ADC has very demanding linearity and noise requirements, as shown in a similar publication [29]. Moreover, the proposed amplifier uses very high switching frequency (above 2 MHz) to achieve good linearity. Accordingly, the efficiency is rather low and the circuit might create EMI issues.

In this a work a new mixed-signal solution is presented. The circuit is shown in Fig. 5.40. The audio signal is provided to the circuit via a digital connection, for instance a I2S interface could be used. The high performance digital PWM proposed above is used. The PWM generates a close-to-ideal pulse width modulated signal. The PWM output signals are applied to a full-bridge power stage driving the speaker. In the power stage, errors are induced into the audio signal, due to supply variations, dead-time, on-resistance of the power switches and similar effects. To achieve high-fidelity audio performance, these errors are corrected with a mixed signal error correction loop. For this purpose, the close-to-ideal PWM signals of the PWM block are compared to the actual output of the power stage. The difference of these signals is the introduced error. An ADC is used to measure the error signal. The measured error signal is applied to the loop-filter of the noise-shaped PWM, such that the error is compensated.

The error induced in the power-stage mainly occurs at the switching edges, for a very short time. On average, the introduced error is small. For a typical output-stage design, the error in the audible range is smaller than 1 % of the output signal. We thus propose a method to reduce the linearity and noise requirements of the ADC. The small error-signal is amplified before the ADC and the amplified error is digitized. Finally the output of the ADC is accordingly downscaled before feeding it to loop filter.

The ADC is implemented as a $\Delta\Sigma$ converter. Good anti-aliasing is needed, because the error signal has a very impulsive characteristic. Therefore a continuous time design is chosen. The ADC is clocked at the same frequency as the noise-shaper in the PWM. The output signal of the ADC

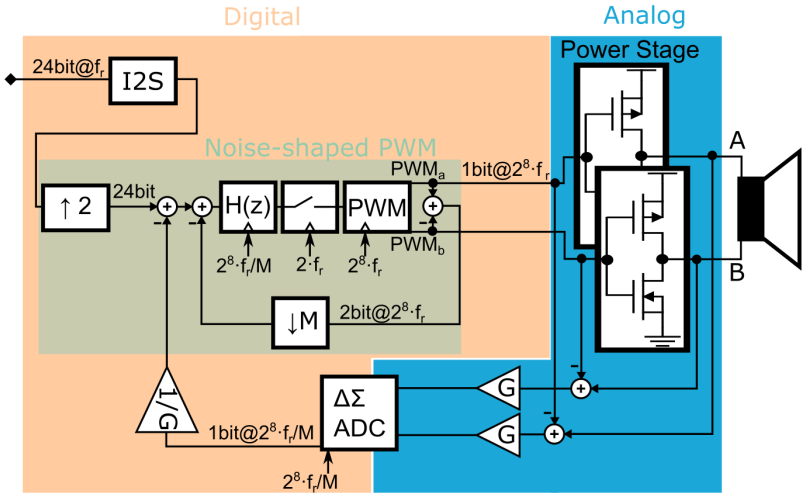


Figure 5.40.: Proposed digital input Class-D amplifier.

is fed-back into the loop-filter of the noise-shaped PWM. The digital loop-filter realizes low-pass filtering of the oversampled ADC signal, to recover the baseband error signal. The noise performance of the complete amplifier is dominated by the ADC, as in previous works [29, 28]. Yet, in our system the ADC processes an amplified version of the error-signal, which helps to significantly relax the ADC requirements. Filterless PWM signals have a strongly varying common-mode component. The subtraction of the output signal from the ideal signal also largely eliminates the common-mode variation at the ADC input. This relaxes the design requirements for the opamp in the first integrator of the $\Delta\Sigma$.

The proposed amplifier was implemented by the research team to evaluate its feasibility. The design was done in 180 nm triple-well CMOS technology. The supply voltage is 5 V for the power-stage, and 1.8 V for the digital circuits. The power-stage is build of complementary MOS-transistors and is designed to drive 8 Ω speakers. An I2S interface is used for the digital input and the previously described noise-shaped PWM is employed, it is clocked at 100 MHz. The ADC is implemented as a single-bit design and uses a non-return to zero feedback DAC.

The error compensation relies on precisely measuring the error between the ideal and real PWM signals. Due to device mismatch in the fabrication a certain gain error in the measured signal will occur. In the digital domain, the measured value is downscaled by a fixed factor, leading to

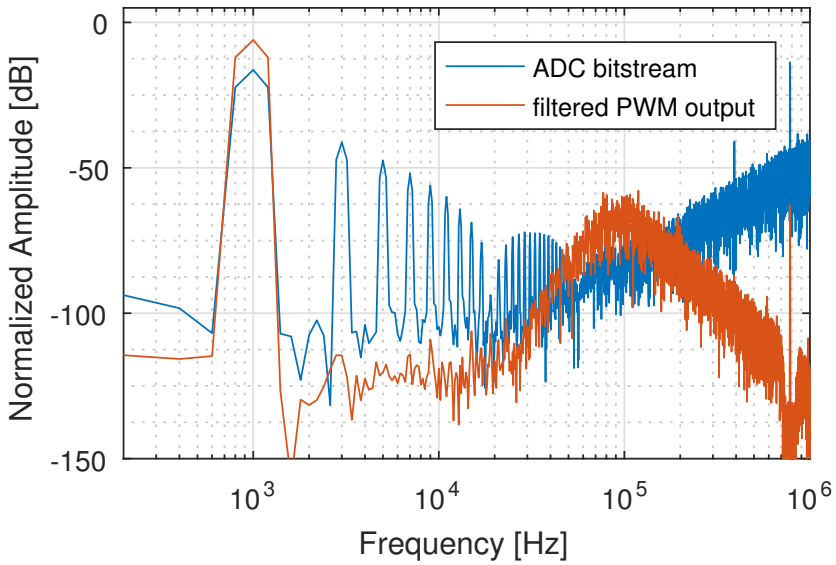


Figure 5.41.: Spectrum of output signal (low-pass filtered) and spectrum of the ADC-bitstream. Simulated with a jittered clock and transient noise.

a slightly deviated feedback value. This will reduce the effective error-suppression. The error correction is thus limited by device matching. In order to reduce the matching requirements, a power-up calibration routine is implemented. At start-up, the error-correction circuitry is characterized with a well-known PWM signal. In this way, offset, positive gain and negative gain of the error-detection ADC are measured. Finally, the factor for digital downscaling is appropriately adapted. The calibration needs app. 65 ms at each power-up.

The complete amplifier is simulated with a mixed-mode simulation. The simulation incorporates transient noise and clock jitter. Fig. 5.41 shows the spectrum of the output signal, with a sinusoidal input signal of amplitude 0.5 FSR. The according error signal at the output of the ADC is also shown. Both spectra are normalized to the same scale. The ADC output shows a higher noise-floor than the Class-D output. The ADC processes the amplified power-stage error, hence it has lower noise-requirements! The simulated THD+N at 1 kHz input signal is -96 dB (-100 dBA) and -91.5 dB (-95 dBA), at amplitude 0.8 FSR and 0.5 FSR respectively. The simulated quiescent current of the circuit (using a digital input of zero) is 0.95 mA for the digital part, 0.75 mA for the ADC and 0.6 mA for the power-stage. The simulations show a peak efficiency of 95 %, not considering package parasitics.

Table 5.1.: Performance Comparison

Parameter	Condition	Typical Value					
		This work*	[27]	[45]	[28]	[76]	[77]
Modulator		digital	digital	analog	digital	analog	analog
THD+N [dB]	best, 1 kHz	−96	−76.5	−91.5	−90	−103.5	−88
Switching [kHz]		390	384	320	2133	650	200
Supply [V]	Power-Stage	5	2.5 to 5.5	1.2 to 4	2.5 to 5.5	3 to 5.5	2.5 to 5.5
Load [Ω]		8	4	8	8	4	8
Power [W]	THD+N<1 %	1.2	2.7	0.85	1.5	3.1	1.02
I_Q [mA]		2.3		3.1	2.8	1.45	2.4
Efficiency [%]	peak	>90	90	94	80	89.5	92
Process		180 nm CMOS	140 nm CMOS	65 nm CMOS	55 nm CMOS	153 nm CMOS	500 nm CMOS

*Simulation results only!

These simulation results are very promising when compared to recent works in literature. Table 5.1 shows the key-figures of several analog and mixed-signal Class-D amplifiers. The table contains only two digitally modulated amplifiers, because high-performance digital amplifiers are still rarely found. The work of [27] uses similar switching frequency, but THD+N is worse. [28] achieves similar THD+N, but needs much higher switching frequency which leads to lower efficiency. The best analog implementations are still hard to beat in terms of THD+N, but would need an additional DAC when used with a digital audio source.

5.3.4. Conclusion

In this chapter, SSM for digital PWM is investigated. The method used in previous work degrades the THD+N and leads to early overload. Therefore an error-correction circuitry to restore audio performance is developed in this work. This proposed error-correction can be implemented with little hardware overhead. The feasibility of the error-correction was demonstrated with a prototype built by the research team. Measurement results show that THD+N is recovered by 20 dB. The detailed implementation was published in a peer-reviewed journal [165]. The new method now enables to implement SSM in PWM without affecting linearity.

Digital PWM is suffering from non-linearity. In this work, a highly-linear digital PWM is proposed. The main novelty of this digital PWM is the application of a simple, yet effective feedback decimator to reduce power-consumption. Digital implementation of the proposed idea was carried out by the research team and simulation results showed the feasibility of the concept. The simulation results prove that linearity in excess of 16 bit at 1 kHz is easily achieved. The proposed feedback decimator effectively

reduces power consumption. The estimated power consumption of the implemented design is below 1 mW. The achieved linearity and power consumption will thus allow to implement very competitive digital Class-D amplifiers.

Analog errors induced in the power-stage degrade the performance of digital Class-D amplifiers. In this work, we presents a novel, mixed-signal error-correction approach. This new approach achieves high linearity, with THD+N in excess of 90 dB, using low switching frequency below 500 kHz. Due to the low switching frequency, high efficiency, better than 90 % is achieved. The requirements towards the analog circuitry are relaxed compared to previous work [28, 29], which makes this design a good candidate for smaller technology nodes. Hence the proposed design is another step towards high resolution, high linearity digital audio amplifiers.

The highly-linear digital PWM and mixed-signal error-correction were picked up by *Graz University of Technology* as a service invention of our research group and patent-application is ongoing.

6. Conclusion

In chapter 3.1 a new measurement setup to determine real output power of low-power, filterless amplifiers is found. In contrast to industry standard measurement setups [2, 104], the new setup is more accurate, because it reduces capacitive loading. Simulation results were conducted to compare previous setups with the setup proposed in this work. The impact of the measurement equipment on the efficiency result could be reduced from more than 25 %, using previous setups to 2 % using the proposed setup. Hence the new measurement setup is suitable to characterize the efficiency of low-power, filterless amplifiers below 1 W.

Transistor-level simulation are not suitable for optimizing the power-stage due to long computation time. Behavioral models for power-stage efficiency of filterless Class-BD amplifiers could not be found during extensive literature research. Hence an efficiency model to estimate the power-efficiency was developed in this work. The model is based on previously published loss analyses for filtered amplifiers. These previously published analyses are combined and modified to develop a novel efficiency model for filterless Class-BDs. The model is based on physical implementation parameters, and allows fast parameter sweeps. The benefits of this model were demonstrated at the design of an integrated power-stage. The model needs less than 1 second to estimate an efficiency curve on the author's notebook (Intel Core i7-4600U processor). Transistor level simulation at post-layout stage took about 5 days for a single power-level on dedicated simulation hardware (Intel Xeon E3-1240 processor, simulation running with a single thread). This significant reduction in simulation time is achieved with an error of less then 0.5 % above 100 mW output power, compared to post-layout simulation. With this model early design decisions can be made, optimization of the power-stage parameters can be carried out and different implementation variants can be investigated before transistor-level simulation. The model will thus help to reduce design time.

Chapter 4 outlined, that integrated Class-D amplifiers can be a major source of electromagnetic emission. With theoretical considerations and measurement results, this work proved that filterless amplifiers are especially empowered to create EMI. The findings were published in a peer-reviewed conference [111] and will raise the awareness on emission issues caused by filterless amplifiers.

Power-efficiency and THD+N are well accepted performance parameters for Class-D amplifiers. A main objective of this work is to show, that the emission generated by Class-D amplifiers should be evaluated and treated as a third performance parameter. Unfortunately, no suitable emission measurement setup could be found in literature, which allows to compare the emission of integrated Class-D amplifiers. Hence in chapter 4.2, a new IC-level measurement for the comparison of integrated Class-Ds is proposed by the author. This new setup allows simple and repeatable conducted measurements to quantify the *emission ability* of an amplifier. Thereby the emission of filterless amplifiers can be compared at IC-level for the first time. The versatility of this measurement setup has been demonstrated in several of our peer-reviewed publications [121, 111, 137]. This setup can be used by IC manufacturers to compare their Class-D to competitors on the market. The measured *emission ability* of the amplifier can then be used to represent this third performance parameter in future datasheets. Such an information will help IC manufacturers to stand out of the crowd and help device manufacturers to select the right amplifier for their system.

When thinking of the emission as a performance parameter, it has to be considered already during the design phase. Chapter 4.3 derives how to model the proposed measurement setup for simulation. The developed model allows to predict the emission before IC production and is compatible with standard analog design flows. In comparison to previous work, not only the electrical properties of the measurement setup are modeled, also the behavior of the measurement equipment is considered. We derived a sophisticated model of an EMI test-receiver, such that simulation results can be directly compared to measurement results. A comparison between simulation and measurement has been carried out, with a Class-D amplifier designed by the author. The deviation between simulation and peak measurement was less than 4 dB up to 100 MHz. Hence, this new simulation approach allows to verify emission targets before IC production. As a consequence, a virtual IC design can now be benchmarked to an actual competitor on the market. Therefore, the simulation model

is a versatile tool for circuit design and can be considered another step forward towards first-time-right integrated circuit development.
We published the EMI test-receiver model in one of the most respected conferences on EMC [129]. The publication had a special focus on the implementation details, such that other research groups could profit from this approach. The publication also includes the first algorithm to estimate the quasi-peak result from only some milliseconds of simulation output. In the meantime since publication, the model has contributed to several projects of other researchers [139, 140, 141, 142].

Due to increasing miniaturization of electronic components, device manufacturers try to reduce external component count of ICs. Traditional measures to reduce EMI are no longer accepted. The developed simulation approaches were thus used to investigate circuit level measures to lower the emission. Chapter 5.1 covers spread-spectrum methods for Class-D audio amplifiers. A novelty of this work is that all SSM methods were strictly analyzed with standard compliant measurement equipment. The results in this work are therefore repeatable and comparable. Moreover, the emission reduction achieved at IC level, will also be measured in compliance tests at system level.
Previous works used randomized SSM in Class-D amplifiers. Randomized SSM is also considered in this work and a novel implementation of a pseudo-random sequence generator was published by our research group [150]. Additionally, periodic SSM was investigated in depth. To study the emission reduction, adequate, yet intuitive theoretical models for both methods were derived in this work. These theoretical explanations can be directly used to determine the implementation parameters for each method. In particular, the derived simple explanations allow to optimize the methods for a certain measurement setup, as we demonstrated in several published works [121, 137].
Another novelty of this work is the investigation concerning SSM and audio performance. The impact of SSM on THD+N was studied using system-level models and prototypes developed in the course of this work. In this way, the effect of randomized and periodic SSM could be investigated in depth. Guidelines how to improve the audio performance were found [121].
Emission reduction and audio performance of periodic and randomized SSM have been compared in this work for the first time. We published the results of this comparison in the largest conference on EMC in the Asian area [138] and the publication was awarded the *Best Student Paper*

Award.

Another spectrum shaping method was investigated in chapter 5.1.3. The idea of CM modulation was published previously. But to the author's knowledge, the resulting spectral properties of the modulation have not been explained before. In this work the theoretical backgrund of the modulation was derived and the impact on power-efficiency was investigated for the first time. The found theory was used to develop a lightweight implementation of CM modulation that requires very little hardware overhead. The implementation was published in a conference with special focus on EMC at IC level [151]. Optimized for peak measurements, an emission reduction of 14 dB is demonstrated with measurement results in this work.

The emission of PWM have larger amplitude, compared to other modulators and are concentrated in narrow bands. Using the spectrum shaping methods proposed in chapter 5.1, this disadvantage can be overcome, as shown in our publications [121, 137, 150, 138]. Moreover, with the theoretical background derived in this work, the distribution of the emission now becomes predictable and controllable.

Slew-rate control is a well known method to reduce emission in power-stages. Previous implementations of slew-rate control in Class-D power-stages have increased the switching delay, or needed large feedback capacitors. In chapter 5.2 a new implementation of a slew-rate controlled Class-D power-stage is proposed. It allows to control the slew-rate of the output voltage independent from the initial switching delay. A detector circuit is developed which is used to determine the start of a switching transition. This detector does not need high-voltage transistors and can thus be used in many technologies. The detector circuit is also used to dynamically decide for the needed dead-time in turn-off controlled transitions. Hence a new and robust way to reduce dead-time in Class-D power-stages has been found. The feasibility of the concept was demonstrated with an integrated prototype designed by the author. The results were published in a well-respected circuit design conference [161]. Measurement results of the prototype showed emission reduction of up to 18 dB compared to non-controlled slew rate. However, a trade-off between emission reduction and power efficiency has to be made. Fortunately, this trade-off can be carried out before production, using the simulation tools presented in this work.

The last part of this thesis covers digital Class-D implementations. Ever shrinking technology and digital audio sources make digital Class-D amplifiers attractive. In chapter 5.3.1 SSM for digital PWM is investigated. The method used in previous work degrades the THD+N and leads to early overload. Therefore an error-correction circuitry to restore audio performance is developed in this work. This proposed error-correction can be implemented with little hardware overhead. The feasibility of the error-correction was demonstrated with a prototype built by the research team. Measurement results show that THD+N is recovered by 20 dB. The detailed implementation was published in a peer-reviewed journal [165]. The new method now enables to implement SSM in PWM without affecting linearity.

Digital PWM is suffering from non-linearity. In this work, a highly-linear digital PWM is proposed. The main novelty of this digital PWM is the application of a simple, yet effective feedback decimator to reduce power-consumption. Digital implementation of the proposed idea was carried out by the research team and simulation results showed the feasibility of the concept. The simulation results prove that linearity in excess of 16 bit at 1 kHz is easily achieved. The proposed feedback decimator effectively reduces power consumption. The estimated power consumption of the implemented design is below 1 mW. Additionally, we proposes a novel error-correction approach for power-stage induced errors. This new mixed-signal approach achieves high linearity, with THD+N in excess of 90 dB, using low switching frequency below 500 kHz. Due to the low switching frequency, high efficiency, better than 90 % is achieved. The requirements towards the analog circuitry are relaxed compared to previous work [28, 29], which makes this design a good candidate for smaller technology nodes. Hence this solution is a promising approach for future digital amplifiers. The highly-linear digital PWM and mixed-signal error-correction were picked up by *Graz University of Technology* as a service invention of our research group and patent-application is ongoing.

Appendix A.

APPENDIX

A.1. Power-stage loss calculation

In the following the calculation of the power-stage losses is outlined. Previous works [8, 11, 9] were combined and modified to suit filterless Class-BD power-stages. The analysis is shortly sketched and explained for the power-stage given in Fig. A.1. The final expression of the presented losses is shown. The derivation of the results is not shown but can be understood easily using the given references [8, 11, 9].

A detailed analysis of the resistive losses can be found in the work of Nyboe [8]. The underlying observation in Nyboe's analysis is: During a transition, the inductive load tries to keep the current steady. This load current either flows through the channel of one switching transistor or into a parasitic capacitance. Only the first case creates losses. In the first case also the current needed to charge the parasitic capacitors flows through the transistor channel. This even increases the resistive losses. This analysis can be combined ideally with the ideas of Ma et al. [11] to model capacitive switching losses.

Nyboe makes several approximations to simplify the analysis [8], which are recapitulated in the following: The switching transistors are assumed to have large transconductance. Thus, they can conduct an arbitrary current at a gate-source voltage close to the threshold voltage. This approximation implies that the driver current stays constant during the transition, independent of whether current-source drivers [110] or inverter-based drivers [18] are used. The load current I_L is considered constant during the switching transition. This is the case for a fast switching power-stage driving an inductive load. The parasitic capacitances associated to the

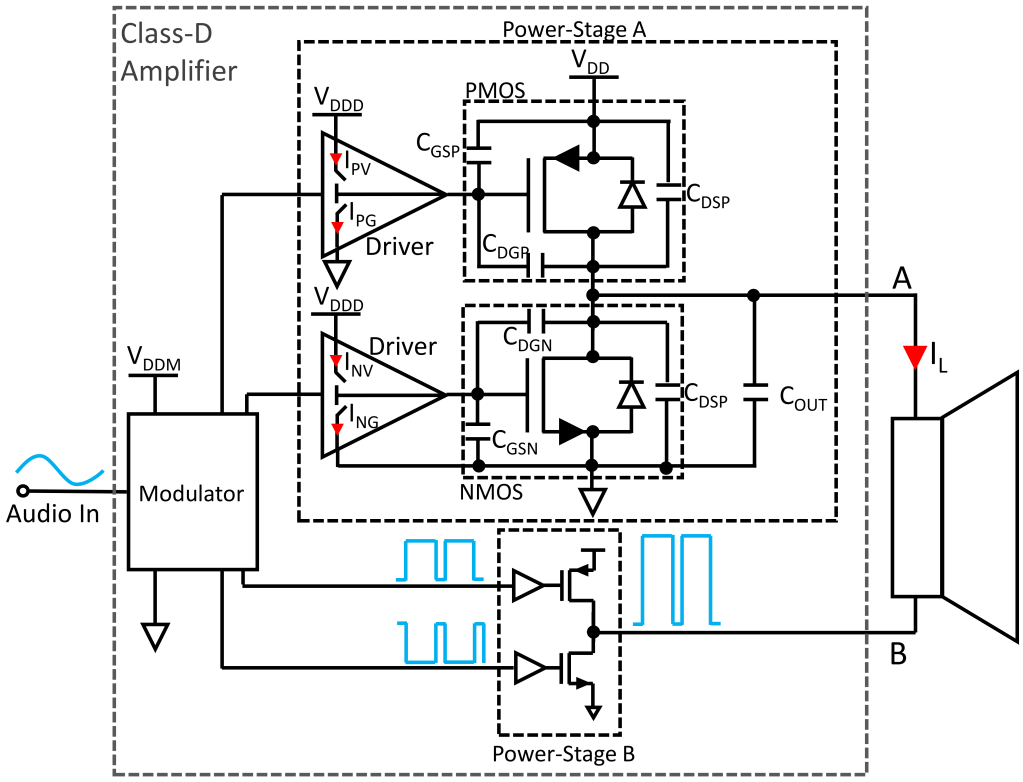


Figure A.1.: Filterless Class-D topology with a PMOS/NMOS power-stage.

output nodes (Fig.A.1) are modeled with linear capacitors. The drivers are modeled with a constant dead-time t_d. The effective dead-time t_{deff} where both power switches are actually OFF is shorter. This is because t_d also incorporates the time needed to discharge the gate of the first switching transistor below its threshold voltage V_{TH} and additionally the time to charge the gate of the second transistor to its threshold voltage.

In the following Nyboe's analysis is carried out for a power-stage with PMOS/NMOS switching transistors driving an inductive load. The load current I_L is typically shown as absolute value $|I_L|$ to help interpretation of the findings. The body diode of the power transistors is assumed to have zero forward voltage drop and no channel capacitance. It is assumed lossless. This simplification has several reasons. Often, the characteristics of this diode are not provided and characterized by the foundry, which makes modeling difficult. Next, the diode is only activated during dead-time. In Class-D amplifiers dead-time is a main source of signal distortion, therefore it is typically kept very short. Combined with the moderate switching frequencies of typically below 1 MHz, the diode loss is not a dominant loss source. However, the diode behavior could be added to the analysis if needed.

As indicated in Fig. A.1, the driver currents are named as follows: I_{NV} indicates the current which can be sourced by the NMOS' driver from supply to switch the transistor ON. I_{NG} indicates the current which can be sinked to ground to shut it OFF. Accordingly, I_{PG} indicates the current which can be sinked by the PMOS' diver to ground to switch the transitor ON. I_{PV} indicates the current which can be sourced from supply to shut it OFF.

For rising transitions of one power-stage (e.g. stage A) 4 different switching scenarios are identified by Nyboe:

- **A:** Hard switching, $I_L > 0$
  This case occurs if the speaker current flows out of the power-stage into the speaker. To switch up, the NMOS transistor is shut OFF first. During effective dead-time of the drivers, both transistors are OFF. In this time, the load current keeps flowing through the body diode of the NMOS. Then the PMOS is switched ON, taking over the load current. Thereby the output node is pulled upwards. Not considering diode loss, the resistive loss E_{RA} can be derived based on Nyboe's analysis and the capacitive loss E_{CA} based on the idea

of Ma et al. to:

$$E_{RA} = (|I_L| + I_B)\,\frac{V_{DD}}{2}\,t_{riseP} \tag{A.1}$$

$$E_{CA} = \frac{(C_{DSN} + C_{PAR} + C_{DGN} + C_{DGP})\;V_{DD}^2}{2} \tag{A.2}$$

$$I_B = I_{PG}\left(1 + \frac{C_{DSP} + C_{DGN} + C_{DSN} + C_{PAR}}{C_{DGP}}\right) \tag{A.3}$$

$$t_{riseP} = \frac{V_{DD}\;C_{DGP}}{I_{PG}} \tag{A.4}$$

The value t_{riseP} depicts the voltage rise time. The displacement current I_B flows into the parasitic capacitors and separates scenario B and C below.

- **B:** Partial soft switching, $-I_B < I_L < 0$
  In this case, a small load current flows from the speaker into the power-stage. First the NMOS transistor is shut OFF. The load current now starts charging the parasitic capacitance of the output node. However the current is too small, such that the output voltage will not reach the supply voltage within the effective dead-time t_{deff}. The calculation of the effective dead-time is shown for a driver with constant current, but can be adapted easily for a different driver topology. At the end of the effective dead-time the output node has reached V_1. Then the PMOS turns ON, taking over the load current and pulling the output node completely to supply potential.

$$E_{RB} = (|I_L| + I_B)\;\frac{V_{DD} - V_1}{2}\,t_{finish} \tag{A.5}$$

$$E_{CB} = \frac{(C_{DSN} + C_{PAR} + C_{DGN} + C_{DGP})\,(V_{DD} - V_1)^2}{2} \tag{A.6}$$

$$V_1 = \frac{|I_L|}{C_{out}}\,t_{deff} \tag{A.7}$$

$$C_{out} = C_{DGP} + C_{DSP} + C_{DGN} + C_{DSN} + C_{PAR} \tag{A.8}$$

$$t_{deff} = t_d - t_{offN} - t_{onP} \tag{A.9}$$

$$t_{offN} = (C_{GSN} + C_{DGN})\;(V_{DD} - V_{THN})\,/\,I_{NG} \tag{A.10}$$

$$t_{onP} = (C_{GSP} + C_{DGP})\;V_{THP}/\left(I_{PG} - \frac{|I_L|\;C_{DGP}}{C_{out}}\right) \tag{A.11}$$

$$t_{finish} = \frac{(V_{DD} - V_1)\;C_{DGP}}{I_{PG}} \tag{A.12}$$

- **C:** Soft switching, $-I_C < I_L < -I_B$
  with $I_C = I_{NG}\left(1 + \frac{C_{DSP}+C_{DPN}+C_{DSN}+C_{PAR}}{C_{DGN}}\right)$
  In this case a larger load current flows from the speaker into the power-stage. During dead-time the load current charges the parasitic capacitance of the output node to supply voltage, where it is clamped by the body diode of the PMOS. Then the PMOS turns ON at vary low drain voltage. This scenario is loss-less, not taking into account diode losses.
- **D:** $I_L < -I_C$
  In this case a large load current flows from the speaker into the power-stage. The NMOS cannot be switched OFF completely. This is because the large load current charges the output node and the output voltage ramps up quickly towards the power supply. This voltage gradient causes displacement current through C_{GDN} opposing the current I_{NG} provided by the driver circuit. When the output voltage reaches the supply voltage, the load current starts flowing through the body diode of the PMOS. The diode clamps the output voltage to the supply potential. The displacement current becomes zero such that the NMOS turns OFF. Then the PMOS is switched ON at vary low drain voltage.

$$E_{RD} = (|I_L| - I_B)\,\frac{V_{DD}}{2}\,t_{riseN} \tag{A.13}$$

$$E_{CD} = 0 \tag{A.14}$$

$$t_{riseN} = \frac{V_{DD}\,C_{DGN}}{I_{NG}} \tag{A.15}$$

An equivalent analysis can be conducted for the falling transition. Similar scenarios and expressions will be found. In the following the scenarios of the falling transition will be named scenario A_f, B_f, C_f, and D_f.

This analysis can be extended for two power-stages with a bridge-tied load, as used in filterless amplifiers. In filterless, BD-modulated amplifiers, each output has a rising and a falling transition in each PWM cycle. For a non-zero load current, there is always a rising transition of type A in one power-stage followed by a type B, C or D transition in the opposite power-stage. Then there is a type A_f falling transition followed by a type B_f, C_f or D_f transition in the opposite power-stage. Thus, for each PWM period the capacitive and resistive switching losses can be calculated if the following data is available: the load current I_L; the values of the parasitic

capacitances associated to the output node, namely C_{DSN}, C_{DSP}, C_{GDN}, C_{GDP}, C_{PAR}; the current which can be sinked and sourced by the driver circuits, namely I_{NV}, I_{NG}, I_{PG} and I_{PV}; the used dead-time in the drivers and additionally, C_{GSN}, C_{GSP} as well as the threshold voltages V_{THN}, V_{THN} for effective dead-time calculation.

The R_{on} losses are calculated based on the work of Yamauchi [9]: Each PWM period is separated into three states: The output node is either connected to ground via R_{onN} of the NMOS, connected to supply via R_{onP} of the PMOS, or it is in switching transition. The time spent in switching transition t_{sw} depends on the load current magnitude and direction. It is estimated as the mean rise-time of scenario A and D. This assumption is reasonable for many Class-D designs: Dead-time is typically reduced to a minimum, rise and fall times are matched to improve amplifier linearity. Moreover, the transition time is often less than 1 % of the PWM period. A small inaccuracy in the switching time estimation will not lead to a large error:

$$t_{sw} = \frac{t_{riseN} + t_{riseP}}{2} \tag{A.16}$$

To calculate the time spent in the different states, the duty-cycle D needs to be calculated first. It can be derived, using the maximum possible load current I_{max}:

$$I_{max} = \frac{V_{DD}}{R_{onP} + R_L + R_{onN}} \tag{A.17}$$

$$D = \frac{I_{max} + I_L}{2\ I_{max}} \tag{A.18}$$

Here R_L is the real part of the load-impedance. The duty-cycle of the opposite output-bridge is $(1 - D)$. Knowing the duty-cycle, the time t_N in which the NMOS is ON and t_P in which the PMOS is ON, can be calculated. The gate charge time, and the gate discharge time is much smaller than t_P and t_N such that R_{on} can be modeled with a constant term [9]. Finally the R_{on} loss of one output-stage can be derived.

$$t_P = D\,(T_{PWM} - 2\ t_{sw}) \tag{A.19}$$

$$t_N = (1 - D)\,(T_{PWM} - 2\ t_{sw}) \tag{A.20}$$

$$E_{Ron} = R_{onN}\ {I_L}^2\ t_N + R_{onP}\ {I_L}^2\ t_P \tag{A.21}$$

The driver losses in each PWM cycle can be calculated as suggested in [11], using the driver supply voltage V_{DDD} and the PWM frequency f_r:

$$P_{Driver} = 2 \left(Q_{gtN} + Q_{gtP} \right) f_r V_{DDD} \tag{A.22}$$

$$Q_{gtN} = \int_0^{V_{DDD}} C_{gN}(U)\, dU \tag{A.23}$$

$$Q_{gtP} = \int_0^{V_{DDD}} C_{gP}(U)\, dU \tag{A.24}$$

The total gate charge Q_{gt} (eg. (A.22)) at zero drain-source voltage is used for more accurate calculation, as the gate capacitance C_g is non-linear. This charge can be derived easily from transistor models provided by the foundry.

A.2. Quasi-peak estimation

The quasi-peak detector evaluates the interference capability of a disturbance. Disturbances with a high repetition rate generate a higher detector reading than disturbances that occur very seldom. In the superheterodyne receiver (CISPR-16-1-1), this detector is implemented with a short charging time T_c and a fast discharging time T_d. The value is then displayed on a critically damped mechanic meter with a certain mechanic time constant. For a time-domain receiver, this detector can be implemented digitally using an IIR filter [173]. But due to the large time constants in the detector, a dwell-time of at least 1 s is needed to for an accurate result.

In the work of [174], an alternative method to estimate the quasi-peak reading is presented. The method shows acceptably accurate results. But it is limited to a certain group of signals. It requires significant knowledge about the measured signal and several separate simulations would be needed. For the ease of use, a different way of estimating the quasi-peak result was developed [129].

The test-receiver model is intended to evaluate signals, which could conflict with legal emission limits. A reasonable assumption is that such signals are dominated by periodically pulsed or continuous content. This assumption holds true for the emission of many practical circuits, such as digital output drivers, charge-pumps, DC-DC converters and similar switched mode circuits.

For narrowband, continuous signals all weighting detectors will generate the same reading. In this case, the quasi-peak reading V_{QP} equals the peak detector reading V_P.

For pulsed disturbances the peak detector will generate the largest reading, the average detector (V_{AV}) the lowest reading. The quasi-peak detector reading will be in the middle, bound by the other two other readings [119]. In this case, a relation between the detector readings can be calculated [175, 136]. The relation depends on the repetition rate f_{rep} of the pulsed disturbance:

$$V_{AV} = \frac{f_{rep}}{B_{imp}} \, V_P \tag{A.25}$$

$$V_{QP} = P(\alpha) \, V_P \tag{A.26}$$

$$\alpha = \frac{\pi \, T_c \, B_6}{4 \, T_d \, f_{rep}} \tag{A.27}$$

B_{imp} is the effective impulse bandwidth of the pre-detector circuit in the superheterodyne receiver. It is determined by the IF bandpass filter, which has a 6 dB bandwidth of B_6. Historically, the bandpass has been implemented as a pair of coupled, tuned transformers. For this case, the standard states $B_{imp} = 1.05 B_6$. In amendment A.7 of the standard, a measurement procedure to determine B_{imp} for arbitrary IF filters is given. This measurement procedure was used to evaluate the B_{imp} for the simulation model.

The time constants of the quasi-peak detector T_c and T_d are explicitly stated in the standard. The pulse response curve $P(\alpha)$ of the quasi-peak detector, is a function of f_{rep}. $P(\alpha)$ is given in [175] and also shown in the standard. $P(\alpha)$ has a much lower slope than f_{rep}/B_{imp}. Thus, slowly pulsed disturbances are weighted more severe with the quasi-peak detector than with the average detector.

Such a relation can not be derived for broadband random noise (e.g. white noise). However, the signals of interest (which have a large amplitude), will be dominated by periodically pulsed or continuous components. For such signals the quasi-peak reading can be estimated. The receiver model is capable of calculating V_P and V_{AV} exactly, if the dwell time is long enough. Whenever a difference between V_P and V_{AV} is observed, V_{QP} can be derived from eqs. (A.25),(A.26) and the constants given in the standard. In this way, all three detector readings are obtained from a single simulation.

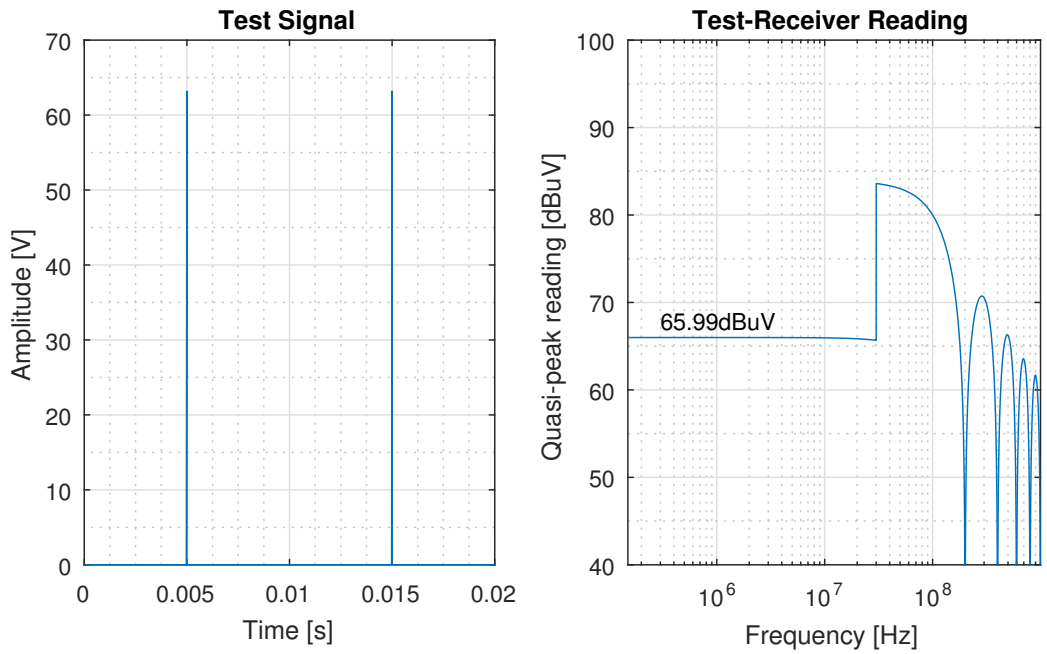


Figure A.2.: Test signal for quasi-peak detector in CISPR Band-B and result of the estimation.

The proposed quasi-peak estimation is valid for narrow-band signals or broadband signals consisting of a single periodically pulsed disturbance. The test-pulses in the CISPR-16-1-1 standard consist of such signals. Fig. A.2 shows the test pulse signal to evaluate the quasi-peak detector in CISPR Band-B. The expected result is a flat spectrum up to 30 MHz of 66 dB µV. A deviation of 1.5 dB µV is allowed. The implemented estimation algorithm performs within the tolerance limits defined in the standard.

However, for superposition of several pulses of different repetition rate, the quasi-peak result will be slightly overestimated. The same is true for a superposition of a continuous and a pulsed disturbance. This can be shown experimentally by comparing the model to a real receiver, where the detector is actually implemented using the correct charging and discharging constants. The deviation is largest in Band-B/C. The worst case occurs, if a very large, slowly pulsed disturbance is superimposed on a very small continuous sinusoidal signal. The error can be up to 12 dB for disturbances pulsed at 100 Hz. Still, in the course of this work, the observed deviations to commercial receivers where in the range of 0 dB to 4 dB for practical signals. The estimated result will always be bound

by the peak reading. Moreover, the standard allows an accuracy of $\pm 2\,\mathrm{dB}$ for narrowband signals and $\pm 1.5\,\mathrm{dB}$ for broadband signals. Therefore the algorithm can be used for a fast estimate of the quasi-peak reading. Additionally, the algorithm will always give a reading on the safe side, thus equal or slightly higher than the real value. The reason is the lower slope of $P(\alpha)$ compared to f_{rep}/B_{imp}.

A.3. Switching losses due to common-mode modulation

Whenever the CM voltage is swapped, the power-stage has to perform an additional switching transition. The method proposed in chaper 5.1.3 uses a LFSR to generate the modulation sequence. The LFSR generates a binary, maximum length sequence. Whenever the sequence changes from 1 to 0 or vice verse, the CM voltage is swapped.

An M bit LFSR clocked at f_{clk} generates pseudo-random binary values. With a properly chosen feedback function the values have a period of $(2^M - 1)/f_{clk}$. In the generated sequence, there are several runs of consecutive 1s or consecutive 0s. There is only one run of consecutive 1s with length M; one run of 0s with length $M-1$; two runs of 1s with length $M-2$; two runs of 0s with length $M-2$ and so forth. In total, there are 2^{M-1} runs [159]. Hence, the LFSR triggers 2^{M-1} additional switching transitions in each LFSR period. On average

$$f_{clk}\,\frac{2^{M-1}}{2^M-1}$$

additional switching transitions are triggered.

The power-stage driven by a PWM has two switching transitions in each PWM period. Hence without CM modulation the transitions rate is $2f_r$. The LFSR is clocked with the same rate as the PWM, to synchronize the swapping to the PWM signal. With CM modulation the transition rate increases on average to

$$f_r\left(2+\frac{2^{M-1}}{2^M-1}\right)$$

The relative increase is

$$\frac{f_r\left(2+\frac{2^{M-1}}{2^M-1}\right)}{2f_r} = 1 + \frac{2^{M-2}}{2^M-1}$$

For $2^M \gg 1$, the transition rate increases on average by 1.25. A valid assumption is that the switching losses thereby increase by approximately 25 %. The losses can be reduced if the LFSR is clocked at a lower rate. The lower clock rate has to be related to the PWM rate for synchronization. In the simplest way, a clock divider can be used to generate a divided clock f_r/K. This leads to a relative increase of the transition rate by

$$1 + \frac{2^{M-2}}{K\,(2^M-1)}$$

Hence the average switching losses increase by approximately $\frac{25}{K}$%.

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