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Relationship between electrical characteristics of NTC ceramics and the surface to volume ratio

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Kurzfassung

In der Firma EPCOS OHG, einem Mitglied der TDK Gruppe werden NTCR (Negative Temperature Coefficient Resistors) für Temperatursensoren auf Basis von Nickel-Mangan-Spinellen hergestellt. NTCR's können aus der gleichen Materialzusammensetzung sowohl mit Vielschichttechnologie als Chips als auch mit Presstechnologie als Scheiben produziert werden. Bei Chips, die nach dem Sintern aus größeren Substraten geschnitten werden, beobachtet man im Vergleich mit Scheiben einen abweichenden Verlauf der Kennlinie im Bereich niedriger Temperaturen.

Ziel dieser Masterarbeit war es die Ursache dieser Abweichung näher zu untersuchen und eine Beziehung zwischen der Bauteilgröße und den elektrischen Eigenschaften herzustellen. Nach der Analyse des Produktionsprozesses stellte sich heraus, dass es während der Sinterung im Verlauf der Abkühlphase zu einer Änderung der chemischen Zusammensetzung in der Randschicht der Chips kommt. Durch Variation der Abkühlrate konnte man die Auswirkung der NiO Ausscheidungen und deren Verteilung im Substrat zeigen, welche einen wesentlichen Einflussfaktor auf die elektrischen Eigenschaften haben. Auch die Größe in der die Chips gesintert werden wirkt sich auf die elektrischen Eigenschaften eines NTCR's aus.

Abstract

In the company of EPCOS OHG, a TDK group company, NTCR or Negative Temperature Coefficient Resistors are produced on $NiMn_2O_4$ spinel ceramic. In the production NTCR's are produced as discs or chips. NTCR's can be produced from the same material composition as chips with multilayer technology and discs with moulding technique. In the production of the NTCR chips a different course of the characteristic curve in the negative temperature range occurred in contrast to the discs.

Thus, the scope of the work is to investigate the relation between the component size and the electrical properties and to identify the root causes for the differences in the characteristics of discs and chips.

After analysing the production process, it could be shown that there is a change of the chemical composition in the surface area during the cooling of the material after sintering of the chips. This supports the hypothesis that the reversal of the decomposition reaction of the spinel phase, which occurs during the cooling of the material after sintering, is the root cause for the changes in the electrical properties. The size in which components are sintered also affects the electrical properties of an NTCR.

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1 Scope of the Work

NTCR or Negative Temperature Coefficient Resistors are resistors with a negative temperature coefficient this means that the resistance decreases with increasing temperature. They can be used as temperature sensors in household electronics, air conditioning and automotive applications in a temperature range from – 50 to 1000 °C. Another field of application is inrush-current limitation in power supply circuits. Such devices are regularly used in automotive applications. NTCR's are also used in medical devices and for temperature measurements of gases in fire detectors. [1]

The most prevalent forms are discs and chips. Discs are made by pressing of spray-dried ceramic granulates into required shape with diameters between 3 and 8 mm and subsequent sintering and metallization. Chips are cut from larger, already sintered and metallized ceramic wafers. The wafer sizes usually are 32 x 32 mm² or 16 x 16 mm² and the chip size ranges from 1 x 0,5 mm² to 3,2 x 1,6 mm². [1] [2] [3]

At the company TDK, NTCR's with the same composition are produced as chips and discs. It can be seen from Figure 1 that the different designs show deviations in electrical properties. In Figure 1, one can see the resistance deviation from a master curve of chips and discs made of the same material composition and same processing conditions. It is particularly noticeable, that at low temperatures the resistance deviations of chips are larger than that of discs even exceeding the tolerance range. [4] [3]

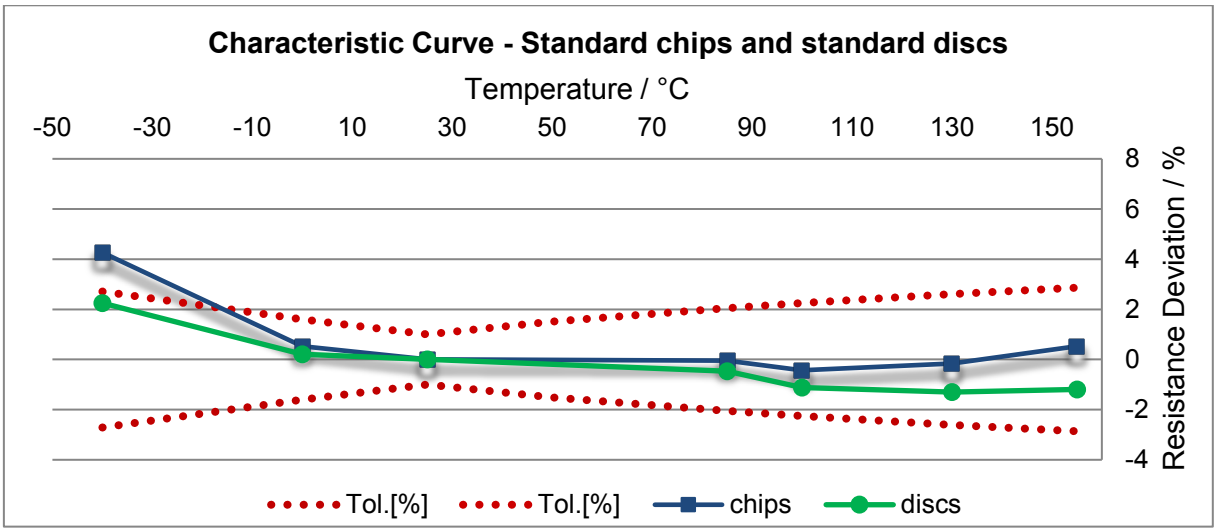

Figure 1: Resistance deviation of chips and disc made of the same material composition

Thus, the scope of the work is to investigate the relation between the component size and the electrical properties and to identify the root causes for the differences in the characteristics of discs and chips. This should be the basis to suggest strategies to improve quality.

The framework of this thesis is to produce different sizes of the above mentioned material composition of NTC chips. The used materials are produced at the company TDK in Deutschlandsberg by tape-casting process and are taken directly out from the production line. The only differences from the commercial chips are the dimensions, the width and the length of the NTC ceramic. The different types of the ceramic sizes are trimmed for one thing as green bodies, then again as sintered bodies. Comparison was made between eleven different component sizes. For each sample, the electrical and morphological properties are compared with each other.

2 Fundamentals and State of the Art

2.1 Fundamentals of NTC Ceramics

A thermistor is a thermally sensitive semiconductor if the temperature of the device is changing it will cause a substantial change in the electrical resistance. The resistance of NTC-thermistors decreases with increasing temperature, therefore they are called Negative Temperature Coefficient resistors, short NTC. They are generally manufactured from polycrystalline mixed oxides with semi-conducting properties, such as manganese, iron, cobalt, nickel, copper and zinc. [5] Areas of applications are temperature sensors for scanning thresholds, to trigger switching pulses and electrical thermometers. [6] Usually NTC's are based on spinels (AB_2O_4), alternatively they are perovskites (ABO_3) or pyrochlores ($A_2B_2O_7$). [4]

The unique characteristics of NTC's are

- the high negative temperature coefficient α (around -0,02 to -0,06 K^{-1})
  The coefficient of resistance is about ten times greater than coefficient of resistance of metals and about five times greater than coefficient of resistance of silicon temperature sensors.
- the ability to create high resistance (R = 1 Ω to 100 MΩ)
- a very high sensitivity to temperature changes (between -2 %/K to -6 %/K)
- the low effort in external circuitry but still highly accurate for temperature measurement (± 0,1 to 20 % - tolerances based on R_{25})
- a relatively low price (<< € 1, because the manufacturing process is easy to organize and control - no semiconductor technology)
- the very compact design (e.g. 0,4 mm cross-section dimension)
- and also a low resistance drift at high temperatures (in the temperature range of 100 °C to 200 °C, in exceptional cases up to 600 °C). [1] [5] [7] [8] [4]

The resistance value decreases with the rise of temperature. This is shown in the two opposing arrows in Figure 2. The $-T$ means that the resistance is negatively dependent on the temperature. [9]

Figure 3 shows the characteristic curve of NTC thermistors. One can see two resistance curves with different nominal resistances. They have the disadvantage of an aggressively nonlinear characteristic. The change is most rapid at low temperatures, thus the measurement resolution will be high. At higher temperature the resistance changes are relatively low, which leads to a poor resolution.

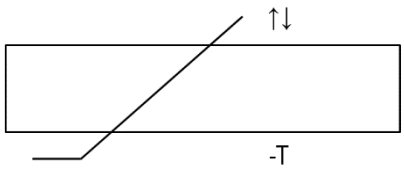

Figure 2: Circuit symbol for NTC with constant current supply [9]

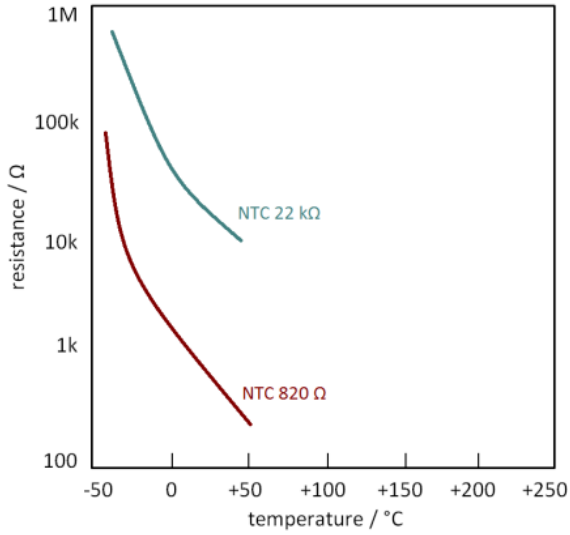

Figure 3: Characteristic curve of two types of NTC-resistors according to DIN 44070 [9]

2.2 The dependence of the resistance on temperature

Equation (1) gives a rough idea of how the resistance (without self-heating) changes depending on the temperature. All thermistors demonstrate an exponential drop of their resistance with increasing temperature [10] Examples for the dependency of the resistance on temperature are shown in Figure 4. The characteristic curve shows the standardized resistance curve of a thermistor with the B-value as a parameter.

$$R_T = R_R * e^{B*(\frac{1}{T}-\frac{1}{T_R})} \tag{1}$$

$$B \sim \frac{E_A}{k} \tag{2}$$

$\boldsymbol{R_T}$ … $NTC\ resistance\ in\ \Omega\ at\ temperature\ in\ K$
$\boldsymbol{R_R}$ … $NTC\ resistance\ in\ \Omega\ at\ rated\ temperature\ T_R\ in\ K\ (is\ usually\ marked\ as\ R_{25}\ at\ T_{25}\ = 298{,}15\ K)$
$\boldsymbol{T}$ … $Temperature\ in\ K$
$\boldsymbol{T_R}$ … $Rated\ temperature\ in\ K$
$\boldsymbol{B}$ … $B\ value, material - specific\ constant\ of\ thermistor\ (determine\ the\ trend\ from\ the\ R-T\ curve)$
$\boldsymbol{e}$ … $Euler\ number\ (e = 2.71828)$
$\boldsymbol{E_A}$ … $activation\ energy\ (E_A \approx k * B)$
$\boldsymbol{k}$ … $Boltzmann\ constant\ (k = 1{,}38066 * 10^{-23} J * K^{-1})$

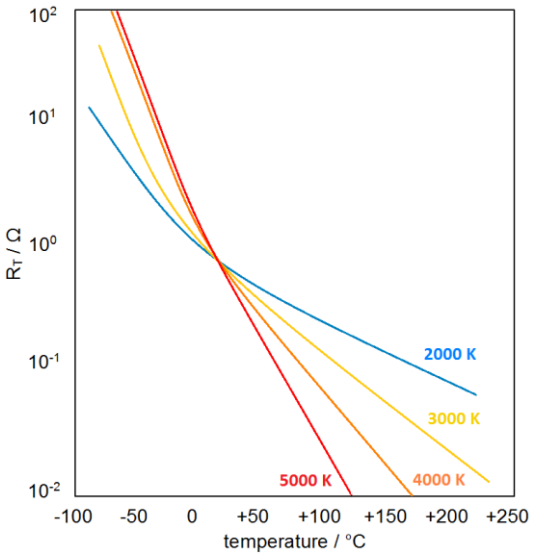

Figure 4: R_T of NTC - thermistors based on R_{25} from four different B-values as a function of temperature [11]

The characteristic curve is almost exponential and specified by nominal resistance (R_{25}) und B-value. In a first approximation the B-value can be connected to the activation energy for the charge transport (see Equation (2)).

For practical applications a more accurate approach of the real characteristic curve is essential. The R/T – curve can be described for instance with the Steinhart-Hart equation (Equation 3).

$$\frac{1}{T} = a + b(lnR_T) + c(lnR_T)^3 \tag{3}$$

$\boldsymbol{T}$ … $Temperature\ as\ a\ function\ from\ the\ measured\ resistance\ in\ K$
$\boldsymbol{a}, \boldsymbol{b}, \boldsymbol{c}$ … $Steinhart - Hart\ coefficients\ (are\ specified\ on\ the\ thermistors\ data\ sheets)$

The advantage is to determine the characteristic curve with three different coefficients.

$\boldsymbol{a} = -(lnR_\infty)$
$\boldsymbol{b} = \frac{1}{B}$
$\boldsymbol{c} = is\ fitted\ to\ the\ measured\ R(T) - curve$

Therefore thermistors can be produced with an uncertainty of only 10 mK. [12] [8]

2.3 B-value

The B-Value describes the steepness of the R-T characteristic of the resistor and can be calculated by the measurement of two pairs of values, for example R_{25} at 25 °C and R_{100} at 100 °C represented in formula (4).

$$B = \frac{ln\left(\frac{R_1}{R_2}\right)}{\left(\frac{1}{T_1} - \frac{1}{T_2}\right)} \tag{4}$$

R_1 and R_2 are the resistances at the temperatures T_1 and T_2. Most common the resistance R_1 is measured at 25 °C (298,15 K) and R_2 at 100 °C (373,15 K) . Typical B-values are between 1500 K and 6000 K. [12] The B-value can be seen as characteristic constant of the material.

A thermistor with fixed dimensions and resistivity is connected to the material-specific constant (B-Value) and the electrical resistance (R) by formula (5). According to formula (5) the temperature dependence of resistivity has an exponential form at high temperatures.

$$R(T) = A * \exp\left(\frac{B}{T}\right) \tag{5}$$

The parameters A and B are very sensitive to the degree of impurity concentration in the crystal. [13] The relative change in resistance referred to the change in temperature is defined by the sensitivity coefficient (α). The sensitivity coefficient gives a differentiation of formula (5). With the formula (6) we can see, that the sensitivity decrease with rise of temperatures. [4]

$$\alpha = \frac{1}{R_T} * \frac{dR_T}{dT} * 100\% \tag{6}$$

$$\alpha = \left(-\frac{B}{T^2}\right) * 100\% \tag{7}$$

The sensitivity coefficient is negative and between -2 %/K to -6 %/K (to compare with metals: +0,4 %/K). The unit is defined in percent per degree of temperature. If B-value is given the temperature coefficient can be calculated by formula (7). The size of α is dependent on the type of material and the temperature of the resistor. One can see, the higher the temperature, the lower the sensitivity and the larger the B-value, the higher the sensitivity coefficient. α is not suitable to develop a NTC or for calculating a resistance value, based on the intense change of the coefficient with the temperature. [8]

2.4 Conduction mechanism of semiconductor

The electrical conductivity reacts differently in metals, semiconductors and isolators to temperature, impurities, electric field and light. All the factors can change the conductivity in an extremely wide range. For metals the conductivity is between 10^6 – 10^4 $\Omega^{-1}cm^{-1}$, for semiconductors is within 10^2 – 10^{-10} mΩ/cm and for insulators it lies between 10^{-14} - 10^{-16} mΩ/cm. [13] In contrast of conductors (metals) the electronic conductivity of semiconductors (ceramics) increases with increasing temperature and at a temperature of 0 K semiconductors behave like isolators. Semiconductors are unique in their electronic properties caused by their band structure. [14] [15].

In the case of covalent semiconductors (e.g. Si, Ge) the big differences between solid states bodies in terms of the electrical conductivity can be explained with the energy – band model. [4] In ionic semiconductors the electron-lattice-interaction is very strong and the bands are badly narrow (ionic crystals have a great ability for polarization), this slows down the motion of electrons. That's the reason why the conductivity for ionic semiconductors is better described with the small polaron model. [4] The mobility of the charge carrier and its temperature dependency can be described with two different conduction mechanisms – the band theory and the polaron hopping process. [1]

2.5 The band theory

The band theory is a very convenient and pictorial way to describe the properties of semiconductors, because only the motion of one electron in the lattice is considered. There is no interaction among single electrons or between electrons and lattice points. [16] [13] In the case of perfect band conduction there are no activation energies and the temperature dependency of the mobility is given by prefactor. [17]

Based on this theory, semiconductors are solids with a band gap of a maximum of 3 eV. Generally ionic crystals have a big band gap and therefore they have a marginal conductivity. Semiconductive mixed oxides behave differently, due to the fact that they do not have filled up d-shells. This is particular important for the conductivity. [6]

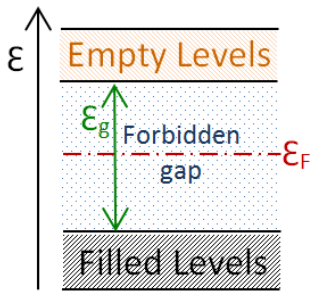

Figure 5: Band structure of semiconductor

Figure 5 shows the band structure of semiconductors. If the lower band is filled and the upper band with the higher energy is empty, the material represents semiconductor (or isolator) characteristics. The filled band is called valence band and the empty band is called conduction band. The band gap (ε_g) demonstrates the average energy between these two bands. ε_F is the Fermi Energy and lies in the middle of the forbidden gab, if the Fermi levels of electrons and holes are equal. The Fermi level can be defined as an energy level and depends of the relative density of holes and electrons and it is measured in eV. [16]

The band theory is used for example in Si or Ge. Si has four valence electrons and is coordinated to four other Si atoms, all bonds are covalent bonds. It has a stable crystalline structure. Each partner provides one valence electron for one double bond. There are no free electrons and therefore there is no electrical current flow (at a temperature of 0 K). [18] [19]

The Figure 6 shows an intrinsic conduction of a pure crystal semiconductor. With increasing temperature (thermal energy input) the atoms and thus the entire crystal begin to vibrate. This leads to a break of the individual bindings. An electron which dropped out from an atomic bond can move freely in the crystal, so called delocalized charge carriers and leaves a hole behind. This process is called generation of an electron hole pair. The holes are called positive charge carriers and do contribute to a variation of conductivity and can be defined as moveable positive charge carriers. Through recombination of an electron with a hole the neutral state is recreated, because the unsaturated bonding can capture the free electrons. With rising temperature, the numbers of jumping electrons significantly increase whereby the conductivity increases. The lifetime of their charge carries amounts a few microseconds and is critical for the quality of the crystal structure. There are preferred directions of charge carrier mobility, under the influence of an electric field e.g. the holes migrate towards the negative pole (cathode). [19] [20] [6]

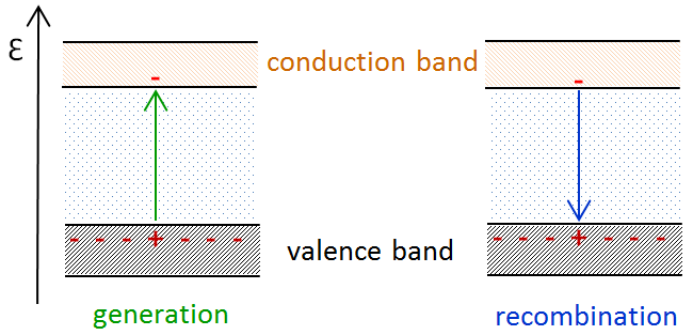

Figure 6: Band model of intrinsic semiconductor. Left side: generation of electron hole pair; Due to the removal of the electrons from the valence band holes are created. Right side: recombination of an electron with a hole.

In an intrinsic semiconductor the electron density and the hole density are the same size. The intrinsic conduction is an unaffected conductivity of a pure crystalline semiconductor and it is defined by crystal temperature and the material caused generation energy for the breakage of the bond. [19]

If dopants or impurities are added to the intrinsic semiconductor an extrinsic semiconductor is created and may easily change by introducing impurities within the raw materials or introduce during the production process. In a doped semiconductor also known as extrinsic semiconductor there is a higher number of holes or electrons than in a pure semiconductor (intrinsic semiconductor). This addition is known as doping and thereby the concentration of carriers (electrons and holes) increases. The conductivity increases the higher the level of doping. Usually it is between 10^{12} and 10^{19} foreign atoms per cm^3. [8] At higher temperatures semiconductors become non-sensitive to impurities. The temperature depends on the material and on the number of foreign atoms. [13] If the temperature increases the intrinsic conductivity of the semiconductors will increase as well and this limits the operating temperature. The extrinsic conductivity is technologically more significant, thereby specific semiconductive properties can be precisely selected. [21] Between the concentration of doping and the conductivity of the semiconductor is a strong non-linear dependency. That's an indication that the charge transport in semiconductors cannot be described with the band theory. [22]

Two types of impurities are used for doping: donor and acceptor dopants. Depending on the doping in semiconductors we are talking about n-type doping, that is a semiconductor which is doped with a donor impurity (electron-conductivity) and p-type doping, doped with an acceptor impurity (hole-conductivity). If the electron - conductivity is dominated, these are designated as n-type semiconductor (surplus of electrons in the conduction band, e.g. for Si, elements of the main group 5) and if the hole – conductivity is dominated they are described

as p-type semiconductor (surplus of holes in the valence band, e.g. for Si, elements of the main group 3). [13] [14] [23]

Depending on the type of conductivity, doping elements are selected near the valence band edge or near the conduction band edge. In consequence both procedures already take place at room temperature, because the energy demand for transferring an electron or an hole is hence very low (circa 0,5 to 1,5 eV). A small energy gap permits an increase for the electrons in the band above already at room temperature. [24]

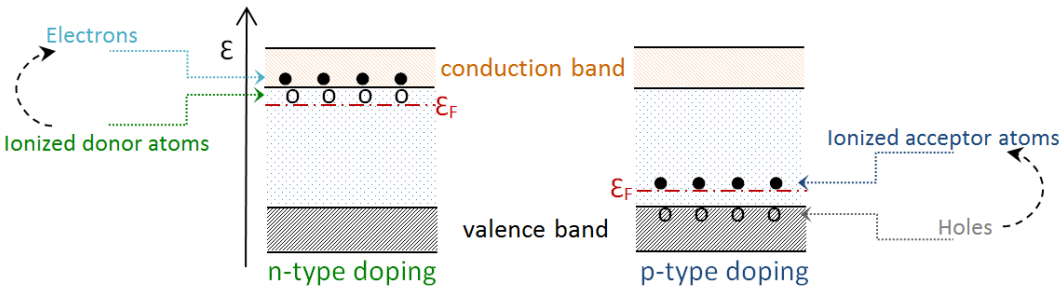

Figure 7: Band structure of doped semiconductors; on the left side occupation with electrons (●) of the conduction band at the bottom, on the right side occupation with holes (o) of the valence band at the upper edge.

In Figure 7 the n-type semiconductor has its donor level close under the conduction band edge. In the process, the electrons are delivered to the conduction band and simultaneously the donor defects are positively charged. That causes the so–called n-type conduction, there is an excess of electrons $(n_0 > p_0)$ (refer to Figure 5, left part). The p-type semiconductor has its acceptor level close above the valence band edge. Within this process electrons are brought up to acceptor level, thus one gets holes in the valence band and the acceptor defects are negatively charged. This results in p-type conduction $(p_0 > n_0)$. See chart 6 on the right hand side, this example shows when the electron moves to the acceptor level it leaves a hole behind and the electron density in the conduction band remains unchanged. n_0 and p_0 are the densities at equilibrium, therefore at equilibrium is $n_0 = n$ and $p_0 = p$. [25] [20] [8] [16]

The conduction mechanisms in NTC thermistors are very complex. Either intrinsic or extrinsic conduction can occur. Ceramics with intrinsic disorder have an intrinsic ionic conductivity. This occurs at high temperatures, when the point defects increase. [26]

If all existing impurities are ionized among the conventional semiconductors to the technical relevant temperature, we talk about impurity depletion. This is a defined value, because the density of the impurities can be precisely specified. See formula (8) and (9), following rules

shall apply for p-type conductivity or for n- type conductivity. If a semiconductor contains acceptors and donators the formula (10) is considered. The conductivity is dominated by impurities with higher concentration.

$$p = N_A^- = N_A \tag{8}$$

$$n = N_D^- = N_D \tag{9}$$

$$p + N_D^+ = n + N_A^- \tag{10}$$

$\boldsymbol{p}$ … $density\ of\ the\ holes$
$\boldsymbol{n}$ … $free\ electron\ density$
$\boldsymbol{N_A^-}$ … $ionized\ acceptor\ density$
$\boldsymbol{N_A}$ … $acceptor\ density$
$\boldsymbol{N_D^+}$ … $ionized\ donator\ density$
$\boldsymbol{N_D}$ … $donator\ density$

If not all existing impurities are ionized there is impurity reserve, this happen at low temperature (T ≤ 70 K) only. [19]

The sensible use of semiconductors require a defined conductivity. This possibility is only available in case of impurity depletion. The chart 8 clearly shows the influence of the temperature with the charge carrier density. [19]

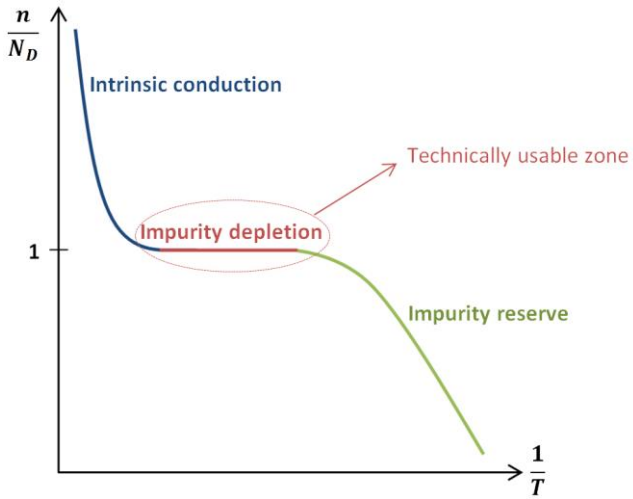

Figure 8: Correlation between the charge carrier concentration and the temperature in the valence band of an n-type semiconductor

The temperature relation of conductivity for semiconductor is given by the density of the holes and electrons (n, p) as well with the mobility of the hole and electrons (μ_n, μ_p). By

variation of the temperature the charge carrier concentration can be changed, thus the conductivity values can differ by orders of magnitude. [27] The electrical conductivity for semiconductors is calculated by formula (8). [28]

$$\sigma = e\,(n\mu_n + p\mu_p) \tag{8}$$

$\boldsymbol{\sigma}$ … $electrical\ conductivity\ in\ \Omega^{-1}cm^{-1}$
$\boldsymbol{e}$ … $elementary\ charge\ (e = 1{,}602 * 10^{-19}As)$
$\boldsymbol{n}$ … $free - electron\ density\ in\ cm^{-3}$
$\boldsymbol{p}$ … $density\ of\ the\ holes\ (p - holes)$
$\boldsymbol{\mu_n}$ … $mobility\ of\ the\ electrons\ in\ cm^2V^{-1}s^{-1}$
$\boldsymbol{\mu_p}$ … $mobility\ of\ the\ holes\ in\ cm^2V^{-1}s^{-1}$

Electrical conductivity in nonmetallic solids is brought by the movement of electrons or ions, mostly the two movements happen at once. [29] The electronic conductivity also increases with the number of charge carriers and their mobility. [30] [6] The mobility of the ions is considerably smaller than that of electrons due to their size and their incorporation into their structure, they cannot be delocalized. That is why the ions move almost exclusively with polaron hopping. [1]

In reverse the charge carrier concentration in metals change only marginally by temperature. The temperature relation of conductivity in metals depends only on the charge carrier mobility.

The following Figure 9 shows the influence of the mobility from electrons (μ_n) and holes (μ_p) in a doped semiconductor (e.g. silicon) at 250 K and 300 K. The mobility of electrons is higher than the mobility of holes. The larger the number of dopants is, the smaller the mobility of the charge carriers. The higher the temperature is, the smaller the mobility.

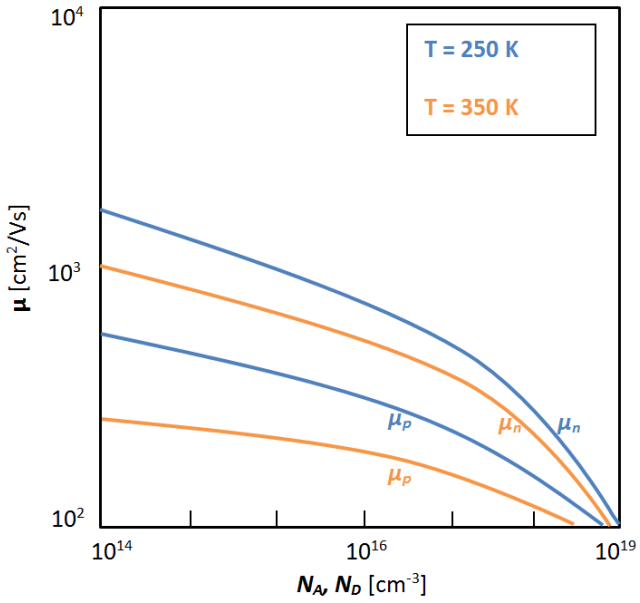

Figure 9: The mobility of electrons (μ_n) and holes (μ_p) for two different temperatures in a doped semiconductor.

The mobility is determined from the drift velocity by charge carrier in an electric field (Coulomb force). [27] It is influenced by the distances between the atoms in the crystal lattice, by the quality of the crystal structure, by the density of the impurities and by the strength of temperature-dependent lattice vibration. [19]

Electrons and holes are able to occur in solids delocalized. Their mobility is defined by the interaction with the lattice vibrations (phonons) or defects e.g. dislocations, grain boundaries, ionized impurities. [1]

The conductivity is proportional to the self-diffusion coefficient. The connection between the diffusions coefficient and the electrical conductivity or rather the mobility of the charge carriers is given by the Einstein relationship (see formula (9)). [31]

$$\mu = \frac{\sigma}{ne} = \frac{eD}{kT} \tag{9}$$

$\boldsymbol{\mu}$ … $mobility\ of\ the\ charge\ carriers\ cm^2V^{-1}s^{-1}$
$\boldsymbol{\sigma}$ … $electrical\ conductivity\ \Omega^{-1}cm^{-1}$
$\boldsymbol{e}$ … $elementary\ charge\ (e = 1{,}602 * 10^{-19}As)$
$\boldsymbol{n}$ … $free - electron\ density\ in\ cm^{-3}$
$\boldsymbol{D}$ … $diffusion\ coefficient\ cm^2s^{-1}$
$\boldsymbol{T}$ … $temperature\ in\ K$
$\boldsymbol{k}$ … $Boltzmann\ constant\ (k = 1{,}38066 * 10^{-23}J * K^{-1})$

The temperature dependence of the conductivity of semiconductors follows the general relation (see formula (10)).

$$\sigma(T) = \sigma_{\infty} * \exp\left(-\frac{E_a}{kT}\right) \quad (10)$$

$\boldsymbol{\sigma}$ … $electrical\ conductivity\ \Omega^{-1}cm^{-1}$
$\boldsymbol{\sigma_{\infty}}$ … $conductivity\ at\ infinfinite\ temperature$
$\boldsymbol{E_a}$ … $activation\ energy$
$\boldsymbol{T}$ … $temperature\ in\ K$
$\boldsymbol{k}$ … $Boltzmann\ constant\ (k = 1{,}38066 * 10^{-23} J * K^{-1})$

The activation energy refers to energy which is necessary for the excitation of the charge carriers to the conduction band. [4]

The limitations of the band theory of semiconductors are the following: The band theory is the theory of a single electron and shows no attention to the other electrons, apart from the Pauli principle. It also ignores the energy replacement among the electrons, between electron and lattice and disregards the trend of electrons to keep those far away from each other. [13] Because of the strong electron-lattice-interaction and the localized mobility of the ions in the ionic semiconductors, the band theory fails. It's more accurate to describe the conduction mechanism of semiconductor with a picture based on localized valences (polaron model), because the charge carriers localize their own environment. [4] The different structures of the ceramics do not support the polaron model. [22]

2.6 The Polaron Model

The concept of polaron was introduced in 1933 by Lev Landau. It is a system, which consists of a charge carrier an electron or a hole and a polarized surrounding area a so called phonon cloud which is described as polaron (see Figure 10). Shown at Figure nine, the negatively charged polaron induced a polarization at every point of the lattice (deflection of ions from their neutral position) in fact different charged ions are deflected in opposite direction. [32] It can therefore be concluded that a charge polaron displaces the atoms form their equilibrium position. [33]

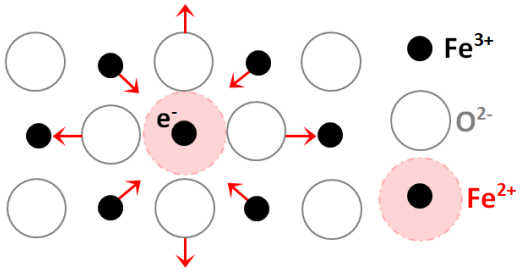

Figure 10:An electron surrounded by a deformed area of the lattice (phonon cloud). e.g. distortion created by the reduction of Fe^{3+} to Fe^{2+}(the same metal ion in two different valence states)

By the reason of coulomb interaction between conduction electrons and lattice ions there is a strong electron – phonon interaction. Caused by that the electron is constantly surrounded by local structural distortion. The polaronic effects, of particle's self-created field are important for semiconductors. [33]

The quasiparticles are responsible for the transport of electrical current. A positive charged polaron is formed by removal of one single electron and can be seen as hole and a negative charged polaron can be seen as electron (see Figure 11). The energy of the polaron lies within the range of the band gab. [34]

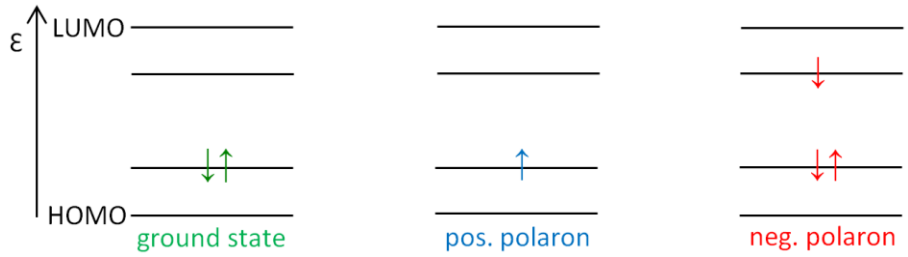

Figure 11:Occupation in the ground state and positive and negative excited state

Polarons are quasiparticle with surround polarization cloud and carry the polarization area along at charge transport. Caused by the movement of whole polaron, a greater amount of energy is necessary for its transport. The mass of the quasiparticle is significantly bigger than the effective mass of a free electron hence the polaron mobility is very low.

The polaron is allocated to a radius (r_P = deformation area) and a distinction is made between small and large polarons (also known as Fröhlich-Polaronen). [6] Small polarons occur when $r_P \leq a$ (a = lattice constant) and large polarons are termed when $r_P \geq a$. [35]

In case of small polarons the interaction between electron and lattice is strong and these are more stable, than large polarons. A higher interaction is synonymous with a higher inertia and therefore both differ in the terms of their mobility as well. [6]

The transport of the charge carriers takes place by two different mechanisms. [19]

1. By an electric field, generated by the charge of the electrons and holes originate a field - strength dependent electricity (field current).
2. Due to inhomogeneous charge distribution the transport of the electrons and holes takes place with the aim of equal distribution of charge carriers (diffusion current). The reason for this is thermal energy.

The motion of the small polaron process shows a positive dependence in temperature (see formula 11). This means that the mobility increase exponentially with the increase of temperature. [1] [22]

$$\mu = \left[\frac{(1-c)|q|a^2 v_0}{kT}\right] * \exp\left(-\frac{W_H}{kT}\right) \tag{11}$$

$\boldsymbol{\mu}$ … $mobility\ of\ the\ quasiparticle\ in\ cm^2V^{-1}s^{-1}\ (between\ 10^{-8}\ and\ 10^{-6}\ at\ T > 300\ K)$
$\boldsymbol{1-c}$ … $number\ of\ unfilled\ sites$
$\boldsymbol{a}$ … $hopping\ distance$
$\boldsymbol{v_0}$ … $vibration\ frequency$
$\boldsymbol{W_H}$ … $hopping\ energy\ (between\ 0{,}1\ and\ 0{,}5\ eV)$
$\boldsymbol{a}$ … $hopping\ distance$
$\boldsymbol{q}$ … $elementary\ charge\ (1{,}602 * 10^{-19}C)$
$\boldsymbol{T}$ … $temperature\ in\ K$
$\boldsymbol{k}$ … $Boltzmann\ constant\ (k = 1{,}38066 * 10^{-23}J * K^{-1})$

The energy $\boldsymbol{W_H}$ needed for this is taken from the thermal lattice vibration and at the same time it is the activation energy of the polaron hops.

It must be noted that in formula (11) no parameters are specified, which describes the ceramics itself (e.g. grain size, structure).

Two types of movement can be carried out: motion of polarons through the whole crystal on the lattice sites or localized movement around lattice defects (see Figure 12).

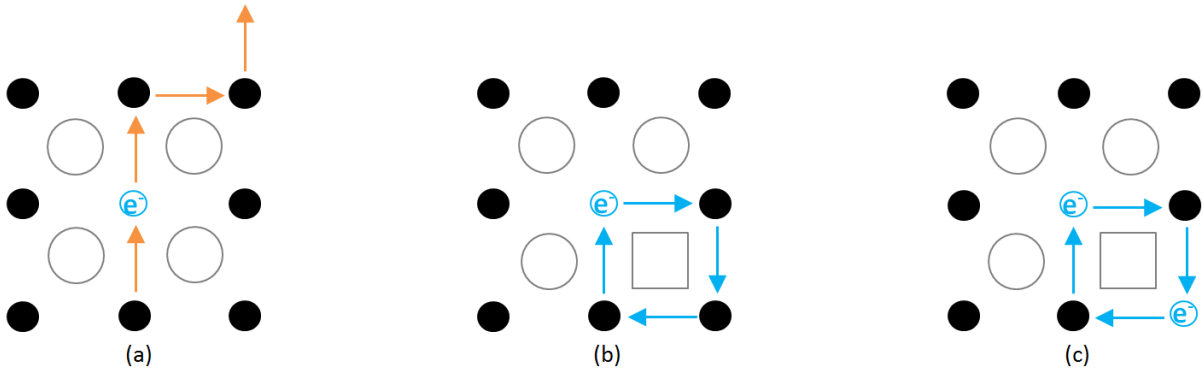

Figure 12: Schematic layout for the movement of polarons (a) free movement on lattice sites; (b) and (c) localized movement around lattice defects.

Unlike the small polarons the mobility of the large polaron shows a negative dependence of temperature (shown in formula 12) and their interaction between the electron and the lattice is low. The mass of the large polarons is only increased lightly and the mobility is not reduced strongly, thus the band theory is a good approximation for the mobility, because the

polarization effect is only weak defined. For instance in semiconductors like InSb are being discussed about large polarons. [17]

The formula (12) states that the mobility decreases if the temperature increases.

$$\mu \propto T^{-\frac{1}{2}} \tag{12}$$

In that case the values varying between 10^{-4} and 10^{-2} $m^2*V^{-1}s^{-1}$ at T > 500 K and the activation energy is relatively small (about 0,1 eV). [1]

At large polarons the deformation extends over several lattice constants and at small polarons only on immediate surrounding. But in both cases there is a decrease in potential energy on the position of the electron, because of deformation in the lattice. Is the reduction sufficiently large this result into localized electrons or holes.

2.7 The Spinel Structure

Semiconductors consist of crystallites which can occur in crystalline structure or spinel. Very often NTC sensors have a spinel structure and then these show valence conduction effects. Normal and invers spinel are created during the sintering process. [22] [5]

The general formula of normal spinel is: A^{2+} B_2^{3+} O_4^{2-}(A^{2+} and B_2^{3+} mean bivalent to trivalent metal atoms). For example a frequently – used thermistor is e. g. Ni^{2+} Mn_2^{3+} O_4^{2-}.

The spinel structure is characterized by a face centered cubic oxygen sublattice (space group Fd3m). The unit cell contains eight formula units AB_2O_4, total of 56 ions (32 O^{2-}, 8 A^{2+} and 16 B^{3+} ions) in a closed packing. In Figure 13 half of the unit cell of the spinel structure can be seen. [15] [36] In a so called “normal” spinel oxide ions create the base lattice and B^{3+} (the smaller metal ions) are on the octahedral interstices and A^{2+} occupies the tetrahedral interstices. Consequently the metal ions are surrounded by oxygen ions either octahedrally or tetrahedrally. The spinel structure has 64 tetrahedral and 32 octahedral interstices, therefore only half of the octahedral (16 out of the 32) and one eighth of tetrahedral sites (8 out of 64) are occupied. [37] [6]

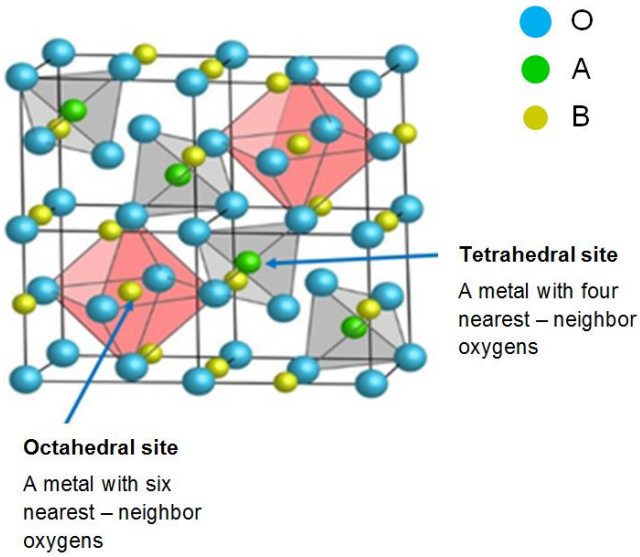

Figure 13: Half of the crystal structure of the normal spinel (AB_2O_4) indicating the tetrahedral and octahedral sites. [38]

In an inverse spinel $B[AB]O_4$ half of the B cations (eight ions) are placed in tetrahedral sites and the remaining half B cations must be placed in the octahedral sites together with the A cations (eight ions). In reality only a few spinels have exactly the normal or invers structure. The distribution of the cations depends on a large number of parameters e.g. temperature, size of cations or d-electron configuration. [39]

Thermistors are manufactured almost exclusively from transition metal oxides with almost an ionic bonding. In this case the valence electrons from the metal atoms move to the neighboring oxygen atoms. Consequently a lattice of positively charged metal ions and negatively charged oxygen ions is created. The ions of these transition metals have the ability to take different valance states, in that way charge transfer is possible.

In nickel manganite is a mixed valence compound. Considering Mn_3O_4 as a normal spinel with Mn^{2+} on tetrahedral sites and Mn^{3+} on octahedral sites one can assume that the incorporation of Ni^{2+} which preferentially occupies octahedral sites leads to a charge compensation by Mn^{4+} ions. The ratio between Mn^{3+} and Mn^{4+} determines the conductivity of the compound. The higher the nickel content the higher is the Mn^{4+} content.

The charge hopping takes place in the spinel structure between ions in octahedral interstices. Because in the spinel structure the B-B bond is the shortest bond length and is represented by $\frac{\sqrt{2a_0}}{4}$ whereas A-A bond = $\frac{\sqrt{3a_0}}{4}$ and A-B bond = $\frac{\sqrt{11a_0}}{8}$. In this case the charge hopping occurs only between ions in octahedral positions, because the hopping distances for ions in octahedral sites are shorter. In addition the octahedral sites share edges, while at

tetrahedral sites are not in contact with each other. Consequently the bond length has an important role in the electrical conductivity.

In this mechanism the hopping process takes place only between atoms which occupy the equivalent crystallographic sites. An ion with different valence states, which is present in a spinel $NiMn_2O_4$ is manganese with Mn^{2+} / Mn^{3+} / Mn^{4+}. Mixed valences of Mn^{3+} / Mn^{4+} ions are on equivalent lattice position at octahedral sites inside the normal spinel (Mn^{2+} is at tetrahedral sites). Consequently in normal spinel conductivity only occurs by the hopping of manganese electrons or holes at octahedral sites. The conductivity depends essentially on the ratio and the distribution of Mn^{3+} and Mn^{4+} on the B sites. In Figure 14 the hopping process between neighbouring Mn^{3+} and Mn^{4+} ions is shown.

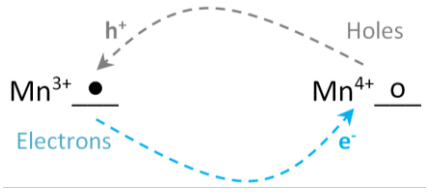

Figure 14: Hopping between neighbouring Mn^{3+} and Mn^{4+} ions

The crystal field theory is very useful to understand the structure of spinels. If a transition metal (e.g. Mn) is surrounded by six negative ions (e.g. oxygen), the d orbitals are no longer degenerated. They are split into two energy levels (t_{2g} – lower energy and e_g – upper energy). This effect occurs in elements with orbital distribution d^9, d^7 and d^4. This behavior results the repulsion between the d electrons and the surrounding negative ions and therefore it is responsible for distortion of the surrounding metal ions.

Mn^{3+} (d^4) in octahedral sites show a Jahn-Teller distortion. This is the reason for the tetragonal symmetry of this spinel. Typical NTC materials have a Mn:Ni ratio between 2:1 and 5:1. If the manganese ratio increases the Mn^{3+} content increase as well and so tetragonal distortion occurs.

Contrary to normal spinel, in invers spinel ($B[AB]O_4$) A and B ions are located on octahedral sites. Hence at the same time these have a variety of different valences. This influences the resistance because of the different polaron concentration. [22] [6] [4] [37] [36]

With a mixture of different suitable oxides it is possible to vary conductivity within orders of magnitude. These oxides can have different conductibility's depending on their sites in normal or invers spinels. Another possibility is introducing dopants e.g. Fe, Cu, Co with high charge carriers concentrations, which reduces the activation energy and means at the same

time a strong increases the conductivity. A third alternative would be a deviation of stoichiometry from transition-metal oxides in the lattice. These can be generated with different settings for sintering process (e.g. a change of sintering temperature, dwell time, oxygen partial pressure or cooling rate). The conductivity can also be influenced by altering or by variation of the Ni:Mn ratio. [22] [36]

2.8 Phase diagram of the NiO-Mn-O system

Figure 15 shows the phase diagram for the system Ni-Mn-O in the temperature range 500 – 1200 °C (created by Wickham) [40]. The information at image 14 are important to produce a single phase product for the system.

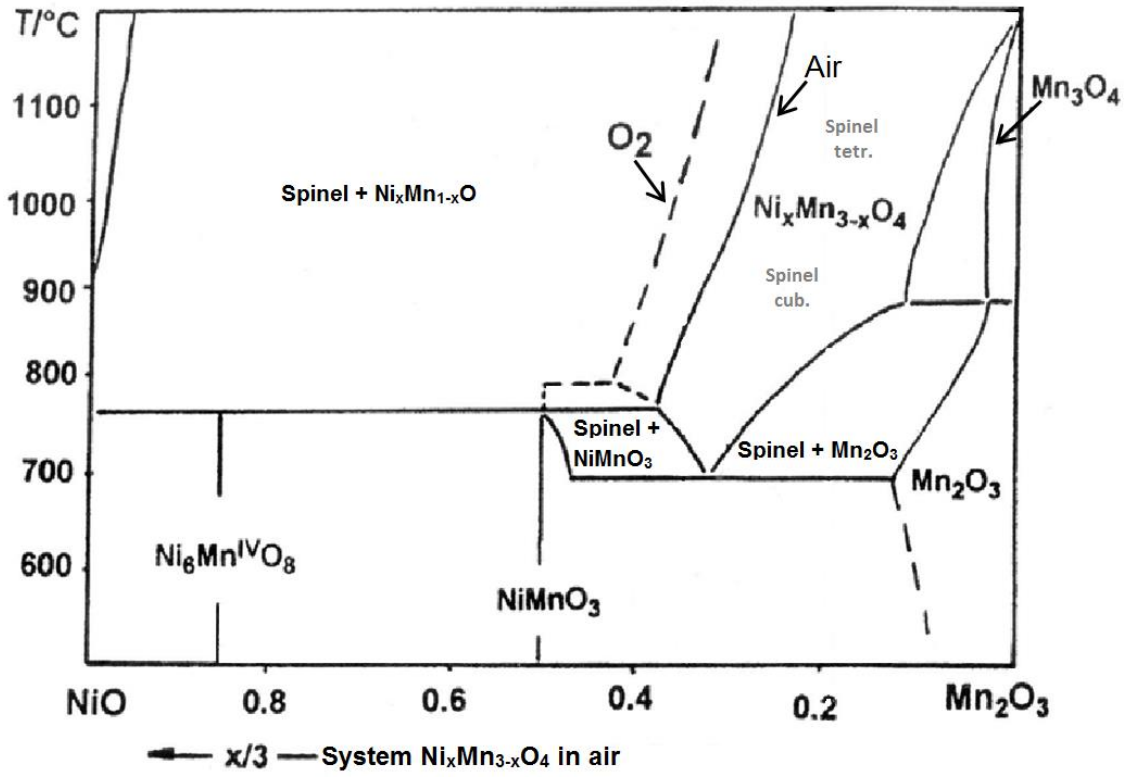

Figure 15: Phase diagram for the system Ni-Mn-O, adapted from Wickham [40]

The solid lines correspond to oxygen partial pressure of 0,21 atm (air) and the dashed lines to 1 atm. According to this phase diagram $NiMn_2O_4$ (R=0,3) is stable in air between 730 °C und 960 °C. The composition of investigated NTC's are around R = 0,3. At sintering temperature about 1200 °C it leads to the two phase area, where nickel oxide precipitations are built along with the spinel phase. [37] [4]

Below 730 °C $NiMn_2O_4$ dissociate to

$$2\ NiMn_2O_4 + {}^1/_2\ O_2 \leftrightarrow Mn_2O_3 + 2\ NiMnO_3$$

Above 960 °C it dissociate to

$$NiMn_2O_4 \leftrightarrow x\ NiO + (3-x)/3\ Ni_{(3-3x)/(3-x)}Mn_{6/(3-x)}O_4 + x/6\ O_2$$

The lower decomposition temperature correlates with the Mn^{2+} concentration on place A in the spinel structure and it oxidizes to Mn^{3+} with oxygen absorption. The upper decomposition temperature is in connection with the Mn^{4+} concentration on place B, which reduces to Mn^{+3} accompanied by oxygen release. In oxygen, both reactions are deferred to higher temperatures (dashed line in Fig. 15). [37] [29]

The largest field on the left side named *Spinel + $Ni_xMn_{1-x}O$* is a two phase region with a spinel and $Ni_xMn_{1-x}O$ (rock salt structure). On the right side next to this region there can be found a single phase region, the spinel. At lower temperature and a composition rich in Manganese there are two phase regions e.g. Spinel + Mn_2O_3 and Spinel + $NiMnO_3$. [40] [29] [4]

NiO precipitations are forming out of the spinel phase. This happens at sintering temperatures, always when two phase regions are built. According to: [41]

$$(3-y)Mn_{3-x}Ni_xO_4 \rightarrow (3-x)Mn_{3-4}N_yO_4 + 3(x-y)NiO + \frac{1}{2}(x-y)O_2$$

Most NTC's are produced as single-phase spinel. To do this, you need exact knowledge about the phase diagram as a function of oxygen partial pressure and temperature. Therefore at constant oxygen partial pressure in the cooling phase oxidation of the spinel occurs and leads to changes in the valence proportion and formation of new phases. This can be avoided with higher cooling rates (kinetic suppression) or readjustment of the pressure during the cooling phase, to keep the oxygen pressure in the sintered body constant (thermodynamically suppression). [1]

2.9 Processing of NTC Ceramics

NTC's are traditionally manufactured from powders by mixed oxide route. The raw materials are weight in a specific ratio than milled, dried and calcined. In most cases a calcination process follows (900 – 1200 K). After another milling and drying process, the NTC powder is ready for the forming processes. Following the molded green bodies run through a thermal process (maximum temperature: 1250 – 1600 K). A classification of the whole processing can be made in four main steps. [1]

1. Powder Synthesis
2. Forming
3. Thermal Processing
4. Finalizing

2.9.1 Powder Synthesis

The first step in the process chain is powder synthesis. Mostly powder mixtures are produced from oxides, carbonates, hydroxides and spray dried salts. Usually, metal oxides from manganese, iron, cobalt, nickel, copper and zinc are applied for thermistors. The incoming raw materials must be tested for purity, particle size and specific surface to ensure sufficient quality of the final products. Afterwards, the raw materials are weighed and mixed together in a specific ratio according to the ceramic formulation. By making use of a mill (e.g. ball mills, attrition mills) two operations can be combined, namely mixing and grinding. The objective is to get a homogeneous mixture and particle size distribution. For the major fraction of products mixing and grinding will be performed wet in ball mills as powder suspension in deionized water. Subsequently, the composition will be dried and calcined. The raw material mixture is calcined, to get a chemical homogeneous and compressed oxide mixture. In the calcination furnace the chemical reactions takes place. After calcination the powder must be milled again to crush agglomerates and to achieve powder with narrow particle size distribution and enhance sinter activity. Typical particle size distribution of a ceramic powder is characterized by D_{10}, D_{50}, and D_{90}. The characteristic parameters of size distributions are for D_{10} = 0,78 µm, for D_{50} = 1,94 µm and for D_{90} = 4,25 µm. The D_{50} is the median diameter and the grain size where 50% of the particles are smaller than this value. Similarly, the D_{10} and D_{90} can be defined. With the subsequent characterization of the finished ceramic powders e.g. specific surface area, powder density, moisture content, check of composition via RFA and crystal structure with XRD, the first production step ends. [15] [42] [1] [43] [44]

2.9.2 Forming

The second step in the process chain is forming of disc and substrates. For disc production binders are added to the milled slurry, which is spray dried to form granulates. For substrates production ceramic tapes are produced from dried powder, for which a different kind of slurry is necessary. In the forming operation the sample gets its final form, only the dimensions are changing during the sintering processes. These dimensional changes must be considered during forming, so that the components after sintering get the appropriate size as close as possible. The shrinkage is influenced by the composition of the powders, organic content and the molding process parameters. The linear shrinkage lies between 15 to 25 % and is not necessarily isotropic. [15] [42] [1] [43]

For the forming process it is necessary to add organic binders, plasticizers and surfactants, which facilitate workability. The choice of the proper additives is very complex and is determined by forming processes and powder properties (specific surface area, wettability, dispersibility). The two most frequently used forming methods for NTC's are pressing of discs and tape casting for multilayer designs. In certain situations, extrusion for rod-shaped NTC's, slip casting and injection molding is also used for forming. [15] [42] [1]

Tape casting

Extremely thin, flat multilayer ceramic components can be manufactured by using tape casting (doctor-blade-process). For this forming process the dried ceramic powder is processed to slurry (ceramic powder, organic binder, other additives and water). On the basis of slurry with a relative high concentration of binder and plasticizers, ceramic tapes are casted. The process how to get square chips (substrates) is as follows: The slurry is evacuated and sieved to remove incorporated air bubbles and coarse agglomerates. The quantity, type and combination of additives determine the castability and homogenization behaviour as well as the drying process and compression process of slurry. The particle size of the ceramic powder for tape casting lies within 1 – 5 µm. The finer the particle size, the smoother the surface of the tape. [44] [15] [42] [1] [45]

At the beginning of the process the slurry is spread over a portable carrier tape. The thickness of the layer depends on the setting of the doctor blade. The preferred thickness of the tape lies between 20 and 100 µm and the width is approx. 30 cm. The necessary strength of the tape is determined by binders. The valid casting viscosity is between 0,8 und 5 Pa*s and is determined mainly by the content of the solvent and temperature. After controlled evaporation of solvant, the coherent and flexible ceramic tape is removed and the

carrier tape is automatically rewinded. Suitable carrier tapes are e.g. polyester films, celluloseacetate films and PTFE films. After the removal from the carrier tape, the dried flexible and rubbery ceramic tape with a smooth surface is forwarded to the next working steps. In Figure 16 a scheme of the tape casting production is schematically discribed. [44] [15] [42] [1]

After the tape casting process the green tape is cut in square green sheets. In order to achieve the desired thickness of the green body, a certain number of tapes are laminated. After that the laminated square green bodies are cut into single components of appropriate sizes. Compared with other pressing techniques, green bodies from laminated tapes have a more uniform packing density. [44] [15] [42]

Pressing

The process of pressing is suitable for the production of discs with a certain aspect ratio and dimensional precision. The production of a proper granulate starts again with a slurry containing binder, surfactants and water. In ceramic processing, spray drying is the well-established technique to create uniform, spherical and homogenous granules from such a slurry. In the spraying tower the slurry is dispersed into very fine droplets by nozzle or centrifugal atomizer. While the droplets fall down, the solvent evaporates in a warm airflow. A sketch of a spray dryer can be seen in Figure 17. The size of the so formed granulate depends on the size of the spray tower and the dispersing technique and is between 20 and 200 µm. [15] [42] [1] [43] [45]

To get a simply shaped disc form, granulate is axially pressed. Spray dried granulate contains organic additive to improve the characteristics for axial pressing (e.g. friction reduction, high green strength). The additive content is usually between 3 - 4 % by weight. A free-flowing granulate with homogenous density is a prerequisite. The flow behaviour is strongly influenced by humidity. The granulate density should be about 45 – 55 Vol. %. [15] [42] [1] [43]

Customary to the operation, the counter and the lower die are located in a steel template. After filling the granulates into the pressing mould, the counter die is closed. The filling quantity of the pressing mould is measured either volumetrically or weight controlled. By moving the die towards each other, the granulates are crushed and compressed into shapes. The maximum pressure for axial dry presses lies between 200 – 1000 bar. Finally, the green body is removed from the pressing mould. Pressing should eliminate large pores. The processing steps for axial compression can be seen in Figure 18. [15] [42] [1] [43] [45]

2.9.3 Thermal Processing

After the forming process, the green bodies have to undergo thermal processing. The thermal processing for ceramic components usually consists of debindering and sintering. In our case these two steps are combined in continuously operated pusher type furnace.

Debindering

The debindering process is a critical and a time-consuming step in ceramic process line. Especially in the case of forming processes such as tape casting, extrusion and injection moulding the binder content is relatively high, as the binder is responsible for the plasticity of the ceramic moulding compound. During debindering the removal of binder takes place to facilitate the sintering process. At best, the binder completely disappears without deformation, creating new cracks and pores or destruction of the moulded padding. Binder removal can be accomplished by thermal decomposition, by dissolution or by extraction. [46] [47]

In ceramics, the process of thermal debindering is most commonly used, because of the easy implementing process. During these process the binder is removed at temperatures up to 600 °C. The binder systems consist of various different additives that differ in their volatility and chemical decomposition. The composition of the binder determines the decomposition temperature and the decomposition products also called as chemical factor. The elimination of the binder is controlled by heat transfer into the moulded compound and mass transport of the decomposition products out of the moulded compound also called as physical factor. The greatest disadvantage is a very long process time, up to several days. During the heating up process a significant increase in pressure might occur. This can cause the destruction of the moulded padding. To avoid this slow heating rates are used (< 1°C/min). [46] [47]

In the dissolution or extraction process the binder will be removed with the help of organic solvents, e.g. hexane or with extracting agent, e.g. CO_2. The advantage of this method is the reduction of process times down to a few hours. The disadvantages are the costs, toxicity, security and the disposal of the substances. [46]

Consequently, the objective of the debindering process is the reduction of process times and in parallel the avoidance of any kind of defects, which could occur during debindering. [46]

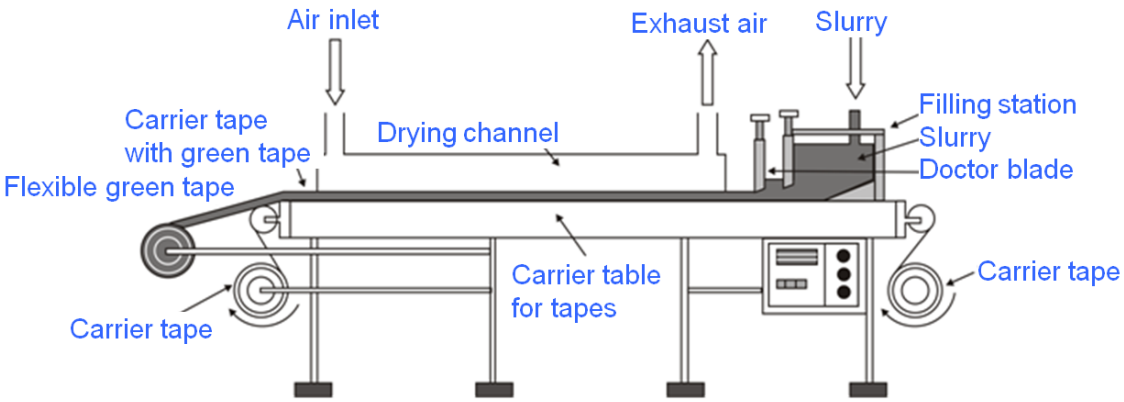

Figure 16: Layout of a continuous tape casting process (training material which has been kindly provided by TDK)

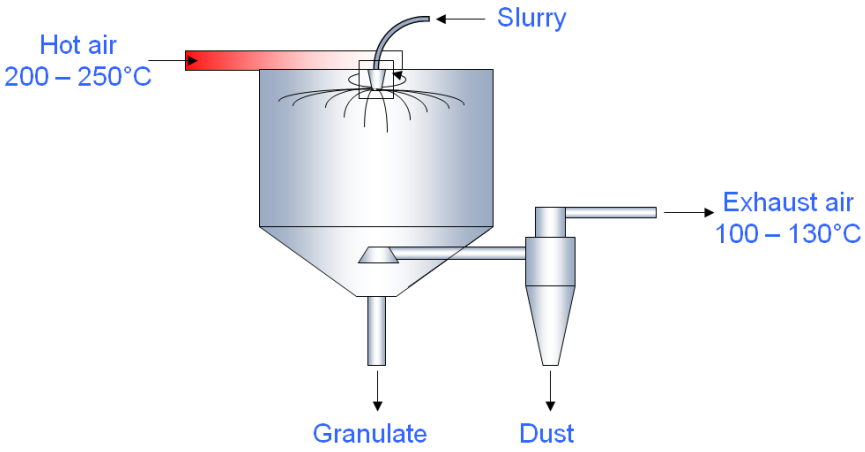

Figure 17: Spray dryer for spraying slurry into a warm drying medium (training material which has been kindly provided by TDK)

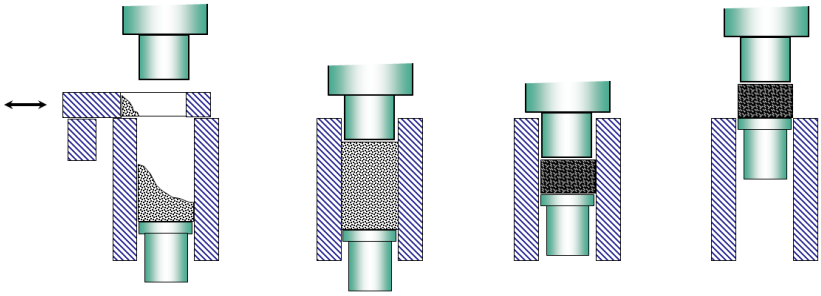

Figure 18: Steps of an axial compression (from left to right): Filling, prepressing, pressing and ejection motion (training material which has been kindly provided by TDK)

Sintering

Under the influence of temperature during sintering the molded green bodies get their final microstructure and mechanical strength as well as all other desired electrical properties e.g. resistivity and B-value. The typical average grain size for NTC ceramics is between 4 and 30 µm. In many cases, the formation of the spinel phase is completed during sintering. [1] [48]

The sintering temperature of ceramics is approximately 70 % of melting temperature. This relation is only a clue, due to the fact that the sintering activity of ceramics depend on the respective powder properties and powder granulation. Generally speaking, caused by the high melting point of ceramics, the sintering temperature is high as well. The simplest way to determine the sintering temperature is to carry out a dilatometry test. [1] [15]

It is essential to keep the sintering temperature low, because of energy savings and as a result to reduce cost. This can be realized with materials with good sintering activity, small particle sizes of ceramic powder or by the addition of flux material. Flux materials accelerate the sintering process. [1] [15]

The driving force for the merge of powder particles, the compressibility of ceramic (reduction of porosity) and the grain growth is always the reduction of the surface free energy of powder particles. The surface energy of a powder is greater than the energy of boundary surface of a dense body. During the sintering process the ceramic is shrinking and finally results in a microstructure with smaller surface or interface area (larger grains) and a lower surface energy due to the change from solid-air-interface (powder) to solid-solid interface in the ceramic. In Figure 19, we can see the structural changes during the sintering process. In the initial stage the grains are rearranged, in the intermediate stage the grains do not move anymore and the porosity decreases. In the last stage, the final stage, the grains are growing and the internal porosity closes. [48] [43]

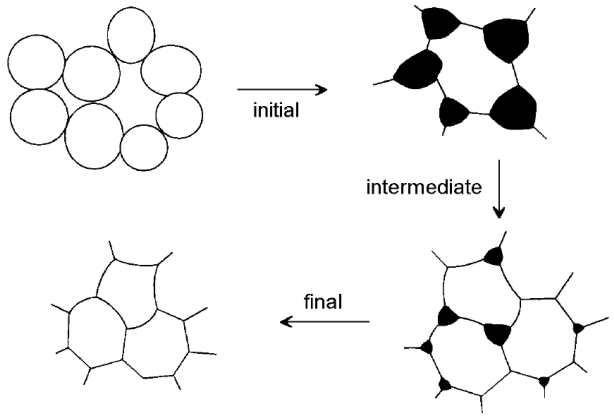

Figure 19: Microstructural changes during sintering [43]

The sintering process depends to a major extent on the composition of the ceramic powder and the implementation of the process. Sinter additives have to be added before forming and improve the sintering rate and control the development of the structure. After the complete sintering process all microscopic and macroscopic procedures can be recorded (e.g. rearrangement of the particles, grain growth, phases, strength, elastic modulus) except for the geometry which can be analysed before and after the sintering process (shrinkage). [43] [15]

Additional, a distinction is made between solid state sintering and fluid phase sintering. In the case of solid state sintering there is melt or liquid phase when maximum sintering temperature is reached. This appears only when the ceramic is very pure. [15] The densification is achieved by rearrangement of particles and the change of their form and size.

If liquid phases are involved during the sintering process, one speaks of fluid phase sintering and there the distinction is made between unwanted and deployed purposeful liquid phase. Unwanted liquid phases occur through impurities, inhomogeneous distribution and segregation of compounds at grain boundaries, which leads to a local exceeding of the melting temperature. This has the effect of formation of new phases, grain- and pore growth hence in the ceramic the strength is reduced. [1] [15] [48]

Fluid phase sintering with selected fluid phases have to wet homogeneously the solid phase and have to dissolve the solid sufficiently to avoid any disturbance during the sintering process. But even fluid phases are accumulating somewhere in the ceramic, dilatation can occur. Thereby the fluid phases diffuse in the grain boundaries and thus push the grains apart. At those places mostly pores are created and this leads to reduction of the strength. The driving force of this process is also the reduction of the interfacial energy, but it has been significantly influenced through liquid phases. At the beginning of this sintering process there is a rearrangement of particles, but it leads to a greater compaction and the reaction velocity is much higher. [1] [15] [48]

After the sintering process follows the metallization process. A layer of conductive material will be deposited on a ceramic substrate to interconnect electronic components. One way of doing this is to coat the ceramic with a metal paste through screen printing and finally the electrode is burned-in. This process is called thick-film metallization. Other options are thin-film metallization, direct bonding and cofiring. This is achieved by screen printing of conductive paste on ceramic green sheets before firing. Thin-film and thick-film metallization will be discussed separately in the next chapter. [1] [49] [50] [51]

2.9.4 Finalizing

To attach the electrode on the ceramic, a layer of metal is applied on it. One opportunity for coating is the thin-film metallization. A ceramic substrate is metallized with a thin film of metal. This requires that the ceramic substrate surface is flat and smooth and for this reason the substrates have to be polished before. Thin films on ceramic surfaces are deposited with e.g. electrochemical deposition, vacuum deposition and sputtering of metals in nm range. These processes are more expensive and the technical realization is harder than thick-film metallization. It is also difficult to sputter a thick metal film, because stress in the deposited film leads to poor adhesion. The typical metal thickness is ~ 2 µm. [52] [53] [54]

A more frequently used method for metallization of ceramic is the screen printing method, because it is suitable for mass fabrication of chips and the costs are low. Screen printing is the process by which a thick film in µm range is applied on ceramic surfaces by a screen mesh. First of all this process has to specify the desired screen mesh. The screen mesh consists of a wire mesh stretched over a screen frame with certain tension. The mesh consists of various wire diameters and mesh counts. The mesh count designates the number of wires per unit length. The finer the wire diameter and the higher the mesh count, the finer the achievable print resolution. Fine wires have less durability of the wire mesh. The mesh count is limited by the particle size of the paste. The screen is an important factor in determining the thickness of the metallization during the screen printing process. For example a thick film paste can be printed with mesh counts of 200 to 400+ and a thin film paste with a mesh count of 80. The wire diameters of 0,9 to 1,1 mils are typically used. After the right wire diameter and mesh count are chosen, the desired screen mesh can be produced and the metallization process can begin. With this method, production of films with thicknesses ranging from 1 to 30 µm and lines widths of > 50 µm is possible. An alternative to screen printing is to use a stencil. A stencil is similar to a screen, but there is no mesh to deal with. [49] [55] [52] [54]

Thick film electrodes are applied on unpolished and sintered ceramic substrates. A printable electrode paste is composed of a desired metal, a glass frit and a solvent. Examples for desired metals are Ag, Au, Pd, and Cu. The glass frit e.g. PbO, Bi_2O_3, ZnO is required for bonding to the ceramic and the required solvent is responsible for the flowability of the paste. A polished substrate would not have the necessary roughness for the grip of the glass frit (glass particles). After the printing process the paste is dried for volatilize the solvent and then fired below the melting point of each metal ingredient, to achieve densification of the film and adherence to the substrate (chemical-bond). During the firing process the metal fuse on the surface of the substrate to form the conductor tracks and the glass frit melts into the substrate (frit-bond). In Figure 20 the two types of bonding are shown. [52] [49] [51] [54]

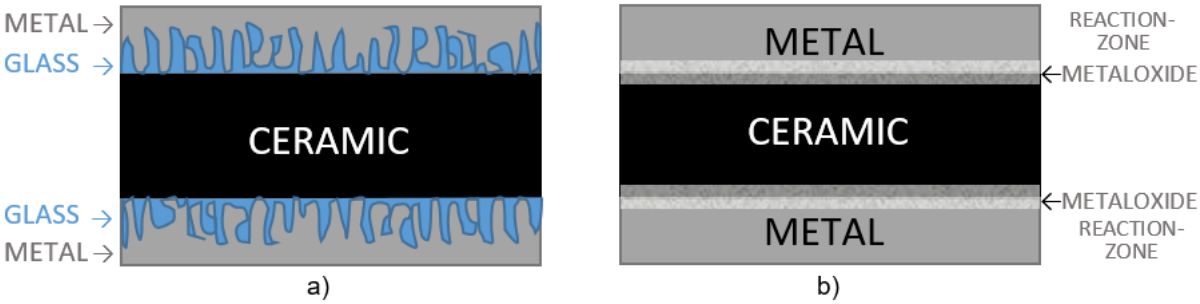

Figure 20: Schema of frit-bond type (a) and chemical-bond type (b)

At best the conductor particles fuse to achieve a smooth solid metal surface for component mounting or wire bonding. The glass interconnects with the ceramic to realise adhesion strength of the electrode. Therefore it is crucial to choose the ideal temperature settings for the furnace. [52] [49] [51] [49] [54]

3 Experimental Methods

The following chapter describes all the experimental methods which are used for the master thesis.

3.1 Six Sigma Tools

The execution of the diploma thesis is based on *Six Sigma paradigms*. *Six Sigma* is a quality management tool and the main objective is the improvement of products and processes. The name for that tool is derived from the objective of process optimization. *Six Sigma* means that a process always has to have a range of tolerance of exactly 12 σ (± 6 σ). Figure 21 shows the normal distribution (Gauss distribution) and one can see that σ is a dimension of the scattering range of the normal distribution. [56]

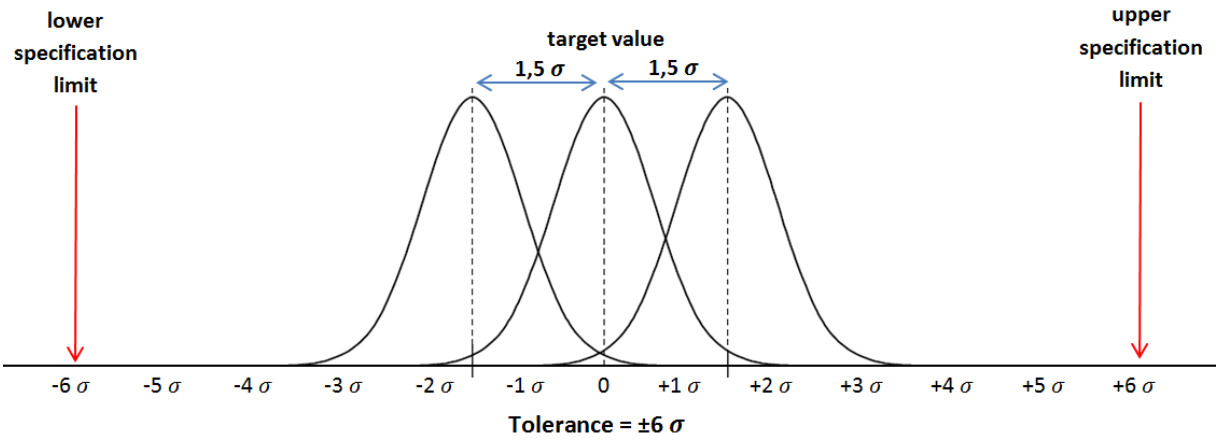

Figure 21: Six Sigma process (by definition of Motorola) [56]

For companies the most important fact is to produce goods and services at low costs, less time and high quality and realize gains.

The improvement of the projects takes place in accordance with a project structure plan, which is called DMAIC method. DMAIC stands for: Define, Measure, Analyze, Improve and Control. The first step is the define phase. This phase includes a detailed description of the initial situation. Within the measurement phase the data should be collected and analyzed. In the analyze phase the cause and effect relation are derived and expressed. During the improvement phase solutions need to be designed and also implemented. Finally, in the control phase, improvements must be achieved and assured in the long run. [56]

3.1.1 Design of Experiments

The design of experiments (DoE) is a part of the analyze phase within the Six Sigma Roadmap and it is a statistics-based method of planning and evaluation of experiments. The main goal is to discover correlations between the influencing parameters (inputs) and results (outputs) with the smallest possible test effort, because resources are limited. For research it is necessary to get reliable and exact results.

During the experiment the influencing parameters are changed specifically and the variations in these changes are measured simultaneously. As a consequence, the relation between inputs and outputs can be precisely ascertained.

3.1.2 Measurement System Analysis

Under the international standards and guidelines from the automobile manufacture it is required to analyse spreading and evaluation for any kind of measurement system. Here it is fundamentally important to distinguish between coincidence and systematical deviation of measured data, to test the suitability for the measurement tasks before starting the series production. [57]

A critical point during performing measurements is the knowledge of the measurement process. The Measurement System Analysis (MSA) determines the ability of the measurement system and finds out and estimates the process error. Such errors might be caused by diverse disturbances, for example by random errors, human interferences, bad manufacturing methods and measuring device mistakes. MSA is a statistical method for evaluating the process of measurement. Decisions are made on the basis of data, facts and Figures, not on the foundation of assumptions. [56] [58]

3.2 Process Flow Chart

The process flow chart in this master thesis defines the processes for the NTC chip production. It shows the flow of every single process during NTC chips manufacturing in order to describe the influencing value during the process easily. This can be seen in Figure 22.

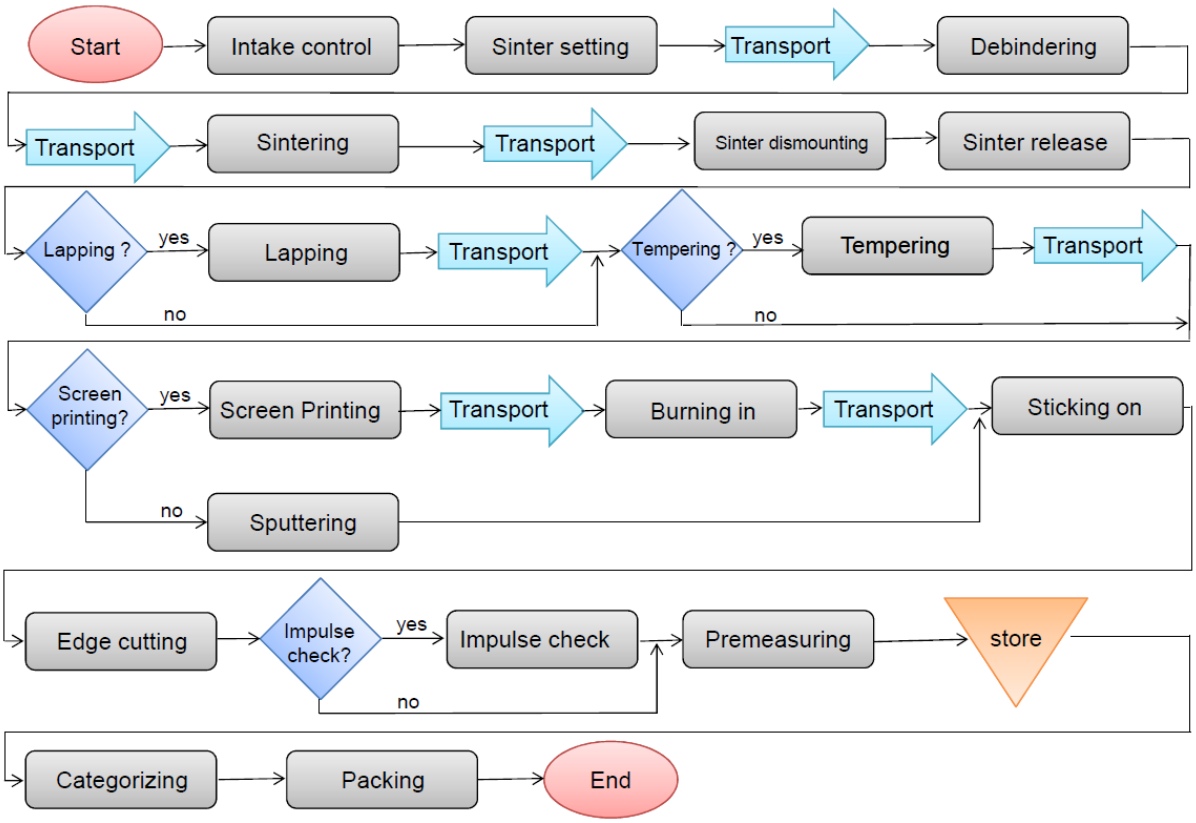

Figure 22: Process Flow Chart

3.3 Sample Taking

For the evaluation of the relationship between electrical characteristics of NTC ceramics and the surface-volume ratio eleven different sizes of NTC chips from the same material assembly have been produced.

For the first type of samples chips are taken out directly from the production line at the company TDK in Deutschlandsberg. In mass production they are produced exactly in the same way. Dried tapes from tape casting process are cut as 90 x 90 mm square shaped ceramic plates. 14 sheets of the square green tapes are stacked, laminated and pressed together. Subsequently, green bodies with a size of 32x32 mm^2 and 16x16 mm^2 and with a thickness of 0,6 mm are cut out from the square shaped ceramic plate.

After the lamination and cutting process, the 32x32 mm^2 and 16x16 mm^2 substrates are debindered and sintered under standard conditions. Subsequently the substrates are metallized and cut in three different chip sizes: 1x2, 2x2 and 3x3 mm^2. These chips are labelled as *standard chips*. Afterwards the chips are examined electrically and morphologically. In Figure 23, one can see the production steps of standard chips, starting from green bodies and ending in cut metallized chips.

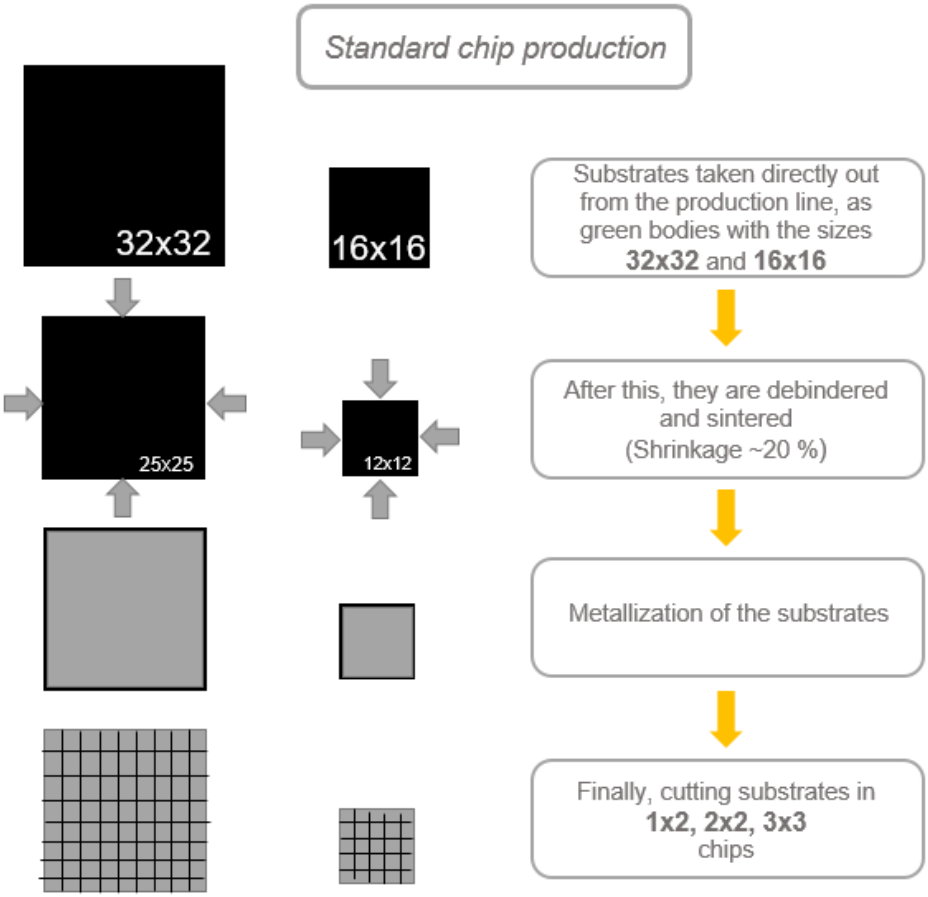

Figure 23: Standard chip production

As a second type of samples, chips with a different production sequence have been produced. These chips are labelled as *non – standard chips*. For these samples after the lamination process, green bodies with a size of 40x40, 12x12, 10x10, 8x8, 5x5, 3x3, 2x2, 1x2, 1x3 mm^2 and a thickness of 0,6 mm are cut out of the laminated plate.

This cut specimens are decarbonized and sintered under standard - conditions. Subsequently the samples 40x40, 12x12, 10x10, 8x8, 5x5, 3x3, 2x2, 1x2, 1x3 mm^2 are metallized with an AG paste via screen printing using a special designed metallization device. After a burn-in process the chips are fit for electrical examinations. In Figure 24 the production steps for the non-standard chips, starting from green bodies and ending in metallized chips are shown.

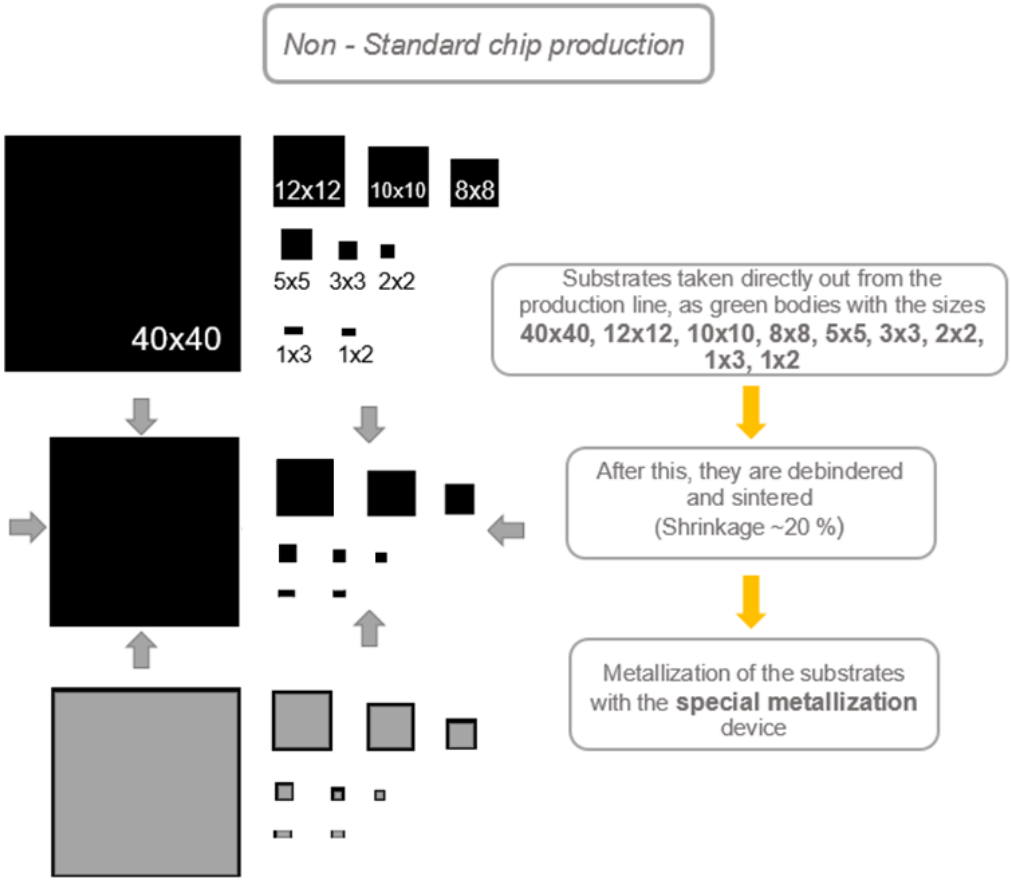

Figure 24: Non-standard chip production

Four of the finished chips which are metallized with the special metallization device can be seen in Figure 25. The shown pictures are taken with a light microscope (Leica, WILD M3C, asset number 28747).

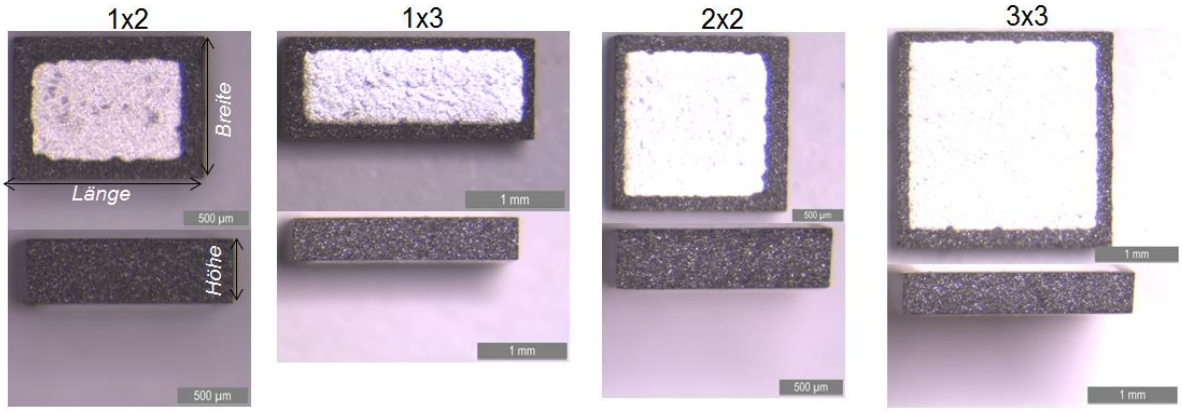

Figure 25: Metallized NTC non-standard chips in four different sizes: 3x3, 2x2, 1x3, 1x2 mm^2

These four sizes 3x3, 2x2, 1x2, 1x3 mm^2 are chosen for the Sinter DoE. All other sizes, 40x40, 32x32, 16x16, 12x12, 10x10, 8x8 and 5x5 mm^2 are only sintered with the standard sintering parameters for this NTC ceramic. For the sinter process the AMI III sintering furnace is used with the asset number 34907. In the last step the non-standard chips 40x40, 12x12, 10x10 and 8x8 mm^2 are cut into 1x2 mm^2 chips for further electrical investigations.

3.3.1 Metallization

For the metallization special screens mesh and an associated metallization device has been created due to the specific sizes of the ceramic chips. The metallization device is designed for four different component sizes of 80 items each.

After forming, cutting, debindering and sintering of each chip the metallization process can begin. For this purpose each individual chip has to be placed by hand into cavity of the metallization device. The chip orientation is audited and the alignment of the screen to the chip is verified under a microscope. By applying pressure with a scraper, an Ag film over the surface of the ceramic chip is applied through the openings of a screen made of mesh. Both sides of the chips are printed and dried separately.

After the first side is printed, the chips are dried and inspected. If no problems are found, e.g. blisters or wrinkles, they are turned by hand to print the other side. Finally all chips are burned in at 750 °C.

Figure 26 shows the chips and the device for the metallization process. The device is suitable to metallize NTC Chips in four different sizes: 1x2, 1x3, 2x2, 3x3 mm^3.

Figure 26: Cut substrates in the size of 32x32 mm^2 compared with 2x2 mm^2 chips on the left side - special metallization device in the middle and on the right side for metallization of 3x3, 2x2, 1x3 and 1x2 mm^2 non-standard chips

3.4 Measurement System Analysis

The objective of Measurement System Analysis (MSA) in this diploma thesis is to check the ability of measurement systems for a given measuring task. All of the measuring devices which are used in this diploma thesis are calibrated in agreement with DIN ISO standard specification. For the following measurement equipment's a MSA was performed: Caliper gauge, micrometer gauge and laboratory balance. For all other measuring instruments a MSA was performed by the laboratory employees of the company TDK. The MSA has been analyzed by software Minitab with the *Gage R&R ANOVA Method*. With this software, technicians are able to interpret a MSA in fast and simply way. [59] [57]

Based on the analysis of variance (ANOVA) the observed dispersion of measurement will be separated from the initiator usage. A distinction is made between the variations of samples, operator, interaction between samples and operator and kind of measurement. The advantages of this method are the comprehensive and precise analysis and the possibility to determine the interactions between sample and operator. The result of ANOVA is a statistical verification of the influences as well as a detection of the scatter. [59] [57]

The *Two-Way ANOVA Table With Interactions* (Fig. 27) shows the significance of the independent variables to the dependent variable. The p-value indicates whether the difference between dedicated classes occur by chance alone or not. The higher the p-value the less likely is the significant influence of the classes. [59] The systematic error of measurement is significant when the p-value is lower than 0,05. There is no interaction when the p-value is bigger than 0,05. [57]

The results of the data from Minitab show the *Two-Way ANOVA Table With Interaction*, as Figure 27 implies.

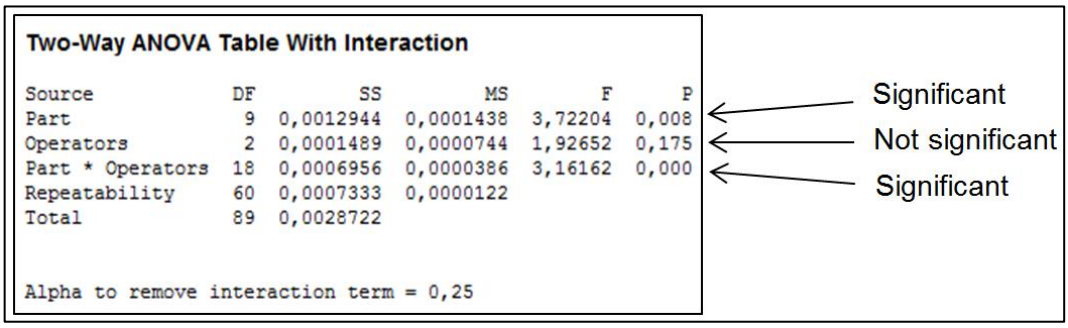

Figure 27: Results of Two-Way ANOVA Table from Minitab

The second part of the data from Minitab shows the results of *Gage R&R*, as can be seen in Figure 28. This analysis is used to identify if a measurement system is suitable for its intended purpose. [60] [58] The following limit values can be used for the evaluation of the test set. [60]

%R&R < 10%:	The measuring system is capable
10% ≤ %R&R ≥ 30%:	The measuring system is limited capable
%R&R > 30%:	The measuring system is inapplicable

R&R stands for repeatability and reproducibility and is presented by the code *%R&R*. Repeatability is an indicator for the scatter results, if the same specimen are measured several times with the same measurement system. Reproducibility is an indicator about the influence of the operator, if the same part is measured with the same measurement system from various operators. *%R&R* is an ascertained total dispersion from the repeatability and reproducibility. [56]

The results of analysis of *GageR&R* from Minitab are split into two parts. The first part handles the variances of repeatability and reproducibility. The variance from the measurement system is calculated by adding the two variances together (*Total Gage R&R*). The *Total Variation* is calculated by adding the variance of the parts (*Part to Part*). The second part is used for the analyses of standard deviations. The standard deviations are not added, unlike the variances. The resolution is the smallest change of a value that a measured system can clearly distinguish the results from the spread. The spread (*Study Var*) of the *Standard Deviation* is multiplied by six, caused by the six sigma concept. The *%Study Variation* (*%SV*) presents the ratio of each variation component related to the total variation. The first value of the column *%SV* is the *%R&R* relating to the total deviation. The *%R&R* has to be smaller than 10% to call a measuring system capable. In the last row of *GageR&R*

is denoted the *Number of Distinct Categories* (ndc), which should be recognized by the measurement system. For measurement system five or more clearly distinguishable categories are recommended.

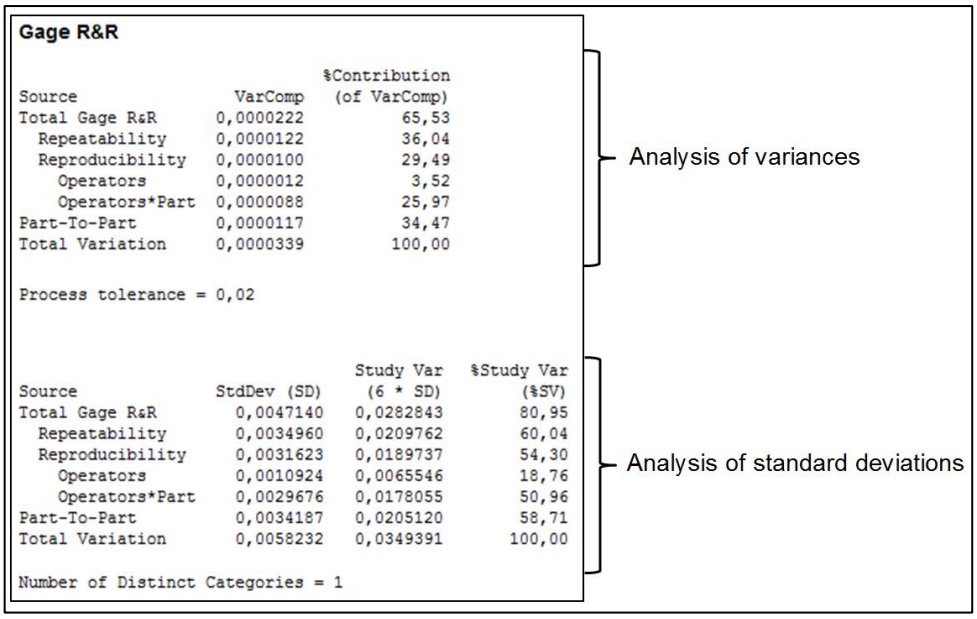

Figure 28: Results of GageR&R from Minitab

In addition to the numerical results, the graphical results should be kept in mind, which were generated from Minitab as standard and state an overview of the measurement system analysis as shown in Figure 29. The first window on the left side will show the individual scattering components and is designated as *Components of Variation*. The second represent the spans for each operator and each part and is called *R Chart by operator*. The last window on the left side presents the average value for each operator and is specified as *Xbar Chart by operator*. The first window on the right side displays all recorded measurements and is known as *Length by Part*. The second is called *Mass by Operator* and all recorded measurements are assigned to the operators, the average of each operator is aligning. The third window assigns the average values of each operator on each part and is called *Part * Operator Interaction*.

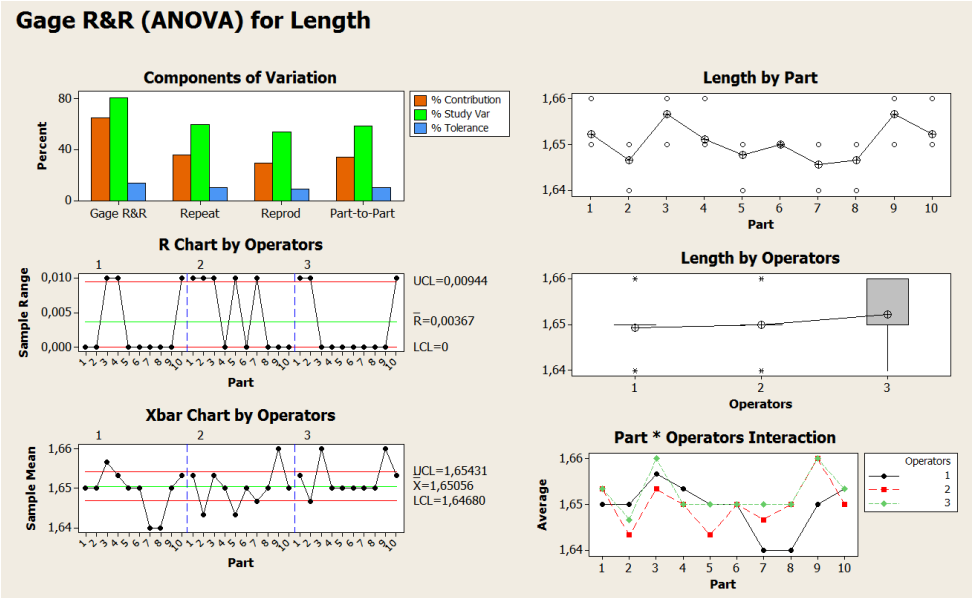

Figure 29: Graphical summary of the Gage R&R (ANOVA)

3.4.1 Calliper Gauge

In the first instance, the length and width of ten different ceramics substrates are measured sequentially with a measuring device to evaluate the measurement capability. Afterwards the same samples are measured randomly two times. The same procedure for measuring the lengths and widths of all samples is used by three different operators. Subsequently an analysis of variance (ANOVA) evaluates the repeatability and the reproducibility (R&R) of the test set.

Length Measurement

The results of *Two-Way ANOVA Table with Interaction* for the length measurement of the executed ANOVA with a Caliper gauge (Mitutoyo Absolute Coolant Proof IP 67, model number 500-716-20, ME-03382, EPCOS calibration date 03. 02. 2017) can be seen in Figure 30. The p-value for the *Part* is 0,008 and for the term *Part*Operator* it is zero. The phrase *Part*Operator* characterizes the cooperation between the parts and the operator. Both terms are below the boundary of 0,05 of the confidence interval. This indicates that those two terms have a significant effect on the capability of the caliper gauge and are affected by the measurement. The p-value for the *Operator* is 0,175, which means that the measuring person has no significant effect and thereby no influence on the measurement.

Figure 31 illustrates the analytic results of the repeatability and reproducibility study (*Gage R&R*). According to the results of the caliper gauge length measurement the *%R&R* relating to the total deviation is 80,95%. The value is very high because the parts that were used for the measurements are not representative for the total deviation.

It requires that a measurement system can be subdivided into five categories. The measurement system can distinguish just one category and consequently the calliper gauge is incapable to measure the length. The resolving capacity of the calliper gauge length measurement is 2,83 x 10^{-2} mm.

The graphical illustration of the ANOVA is visible in Figure 32.

Two-Way ANOVA Table With Interaction

Source	DF	SS	MS	F	P
Part	9	0,0012944	0,0001438	3,72204	0,008
Operators	2	0,0001489	0,0000744	1,92652	0,175
Part * Operators	18	0,0006956	0,0000386	3,16162	0,000
Repeatability	60	0,0007333	0,0000122		
Total	89	0,0028722			

Alpha to remove interaction term = 0,25

Figure 30: Minitab excerpt of the Two-Way ANOVA for length measurement with interaction between operator and parts

Gage R&R

Source	VarComp	%Contribution (of VarComp)
Total Gage R&R	0,0000222	65,53
Repeatability	0,0000122	36,04
Reproducibility	0,0000100	29,49
Operators	0,0000012	3,52
Operators*Part	0,0000088	25,97
Part-To-Part	0,0000117	34,47
Total Variation	0,0000339	100,00

Process tolerance = 0,02

Source	StdDev (SD)	Study Var (6 * SD)	%Study Var (%SV)
Total Gage R&R	0,0047140	0,0282843	80,95
Repeatability	0,0034960	0,0209762	60,04
Reproducibility	0,0031623	0,0189737	54,30
Operators	0,0010924	0,0065546	18,76
Operators*Part	0,0029676	0,0178055	50,96
Part-To-Part	0,0034187	0,0205120	58,71
Total Variation	0,0058232	0,0349391	100,00

Number of Distinct Categories = 1

Figure 31: Minitab excerpt of the gage R&R for the caliper gauge length measurement (ANOVA – Method)

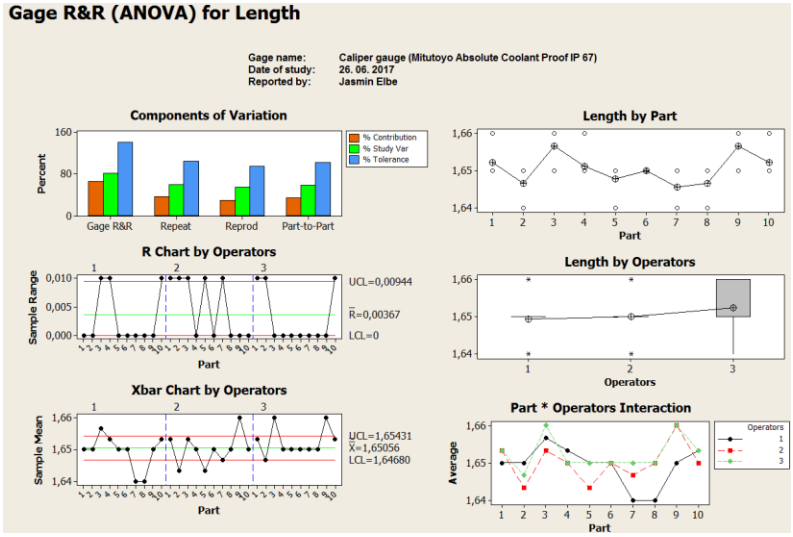

Figure 32: Graphical summary of the Gage R&R for the caliper gauge for the length

Width Measurement

The widths of ten different ceramic substrates are measured with the caliper gauge as well (Mitutoyo Absolute Coolant Proof IP 67). The measurement data are shown in Figure 33, 34 and 35. The ANOVA evaluation shows that the interaction between *Part* and *Part*Operator* has a significant influence on the measurement, whereas the *Operators* have no significant influence.

The *Gage R&R* provides the analysis of the measurement capability. The repeatability and reproducibility is 73,62%. The number of distinct categories is one and the resolution is 3,25 x 10-2 mm. The results for the width are almost equal to the length. Therefore, the caliper gauge cannot be used to measure the width.

Two-Way ANOVA Table With Interaction

Source	DF	SS	MS	F	P
Part	9	0,0024178	0,0002686	5,83378	0,001
Operators	2	0,0002156	0,0001078	2,34048	0,125
Part * Operators	18	0,0008289	0,0000460	2,59028	0,003
Repeatability	60	0,0010667	0,0000178		
Total	89	0,0045289			

Alpha to remove interaction term = 0,25

Figure 33: Minitab excerpt of the Two-Way ANOVA for width measurement with interaction between operator and parts

Gage R&R

Source	VarComp	%Contribution (of VarComp)
Total Gage R&R	0,0000293	54,19
Repeatability	0,0000178	32,93
Reproducibility	0,0000115	21,27
Operators	0,0000021	3,81
Operators*Part	0,0000094	17,45
Part-To-Part	0,0000247	45,81
Total Variation	0,0000540	100,00

Source	StdDev (SD)	Study Var (6 * SD)	%Study Var (%SV)
Total Gage R&R	0,0054092	0,0324551	73,62
Repeatability	0,0042164	0,0252982	57,38
Reproducibility	0,0033884	0,0203306	46,11
Operators	0,0014344	0,0086066	19,52
Operators*Part	0,0030698	0,0184190	41,78
Part-To-Part	0,0049732	0,0298391	67,68
Total Variation	0,0073479	0,0440875	100,00

Number of Distinct Categories = 1

Figure 34: Minitab excerpt of the gage R&R for the caliper gauge width measurement (ANOVA – Method)

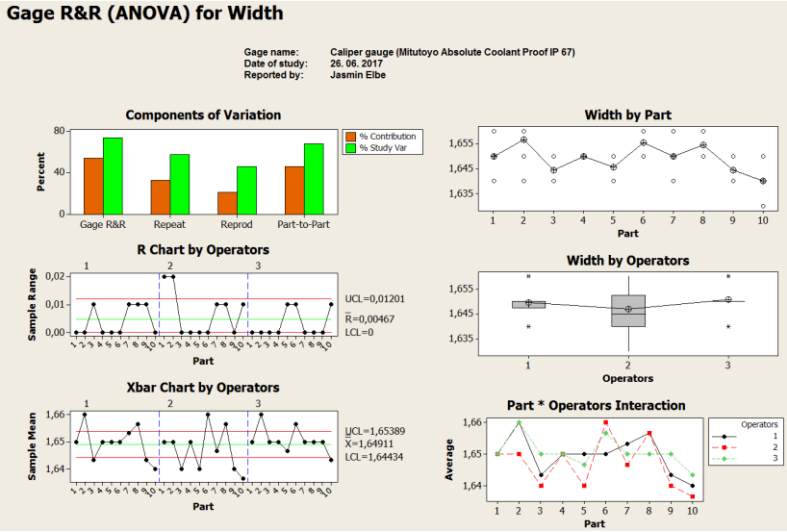

Figure 35: Graphical summary of the Gage R&R for the caliper gauge for the width

3.4.2 Micrometer Gauge

The *Two-Way ANOVA Table with Interaction* for the micrometer gauge (Mitutoyo Digimatic; ME-03412, EPCOS calibration Date: 31. 01. 2018) can be seen in Figure 36.

The p-value for the term *Part* is zero, for the term *Part*Operator* it is 0,001 and for the term *Operator* it is also 0,001. All terms are below the boundary of 0,05 of the confidence interval. This indicates that all terms have a significant effect on the capability of the micrometer gauge and therefore have a direct influence on the measurement.

Figure 37 illustrates the analytic results of the repeatability and reproducibility study (*Gage R&R*). According to the results of the micrometer gauge measurement the *%R&R* relating to the total deviation is 33,00%. The value is too high because the parts that were used for the measurements are not representative for the total deviation. The *%R&R* has to be smaller than 30% to call a measurement system limited capable. The number of distinct categories is four, recommended for measurement systems are five or more clear distinguishable categories. The resolution is 9,93 x 10-3 mm and exceeds the caliper gauge by one decimal power.

The graphical illustration of the ANOVA is visible in Figure 38.

Two-Way ANOVA Table With Interaction

Source	DF	SS	MS	F	P
Part	9	0,0012280	0,0001364	68,1600	0,000
Operators	1	0,0000542	0,0000542	27,0500	0,001
Part * Operators	9	0,0000180	0,0000020	4,0037	0,001
Repeatability	40	0,0000200	0,0000005		
Total	59	0,0013202			

Alpha to remove interaction term = 0,25

Figure 36: Minitab excerpt of the Two-Way ANOVA for micrometer gauge with interaction between operator and parts

Gage R&R

Source	VarComp	%Contribution (of VarComp)
Total Gage R&R	0,0000027	10,89
Repeatability	0,0000005	1,99
Reproducibility	0,0000022	8,90
Operators	0,0000017	6,91
Operators*Part	0,0000005	1,99
Part-To-Part	0,0000224	89,11
Total Variation	0,0000251	100,00

Source	StdDev (SD)	Study Var (6 * SD)	%Study Var (%SV)
Total Gage R&R	0,0016550	0,0099298	33,00
Repeatability	0,0007071	0,0042426	14,10
Reproducibility	0,0014963	0,0089778	29,84
Operators	0,0013184	0,0079106	26,29
Operators*Part	0,0007075	0,0042453	14,11
Part-To-Part	0,0047336	0,0284019	94,40
Total Variation	0,0050146	0,0300876	100,00

Number of Distinct Categories = 4

Figure 37: Minitab excerpt of the gage R&R for the micrometer gauge (ANOVA – Method)

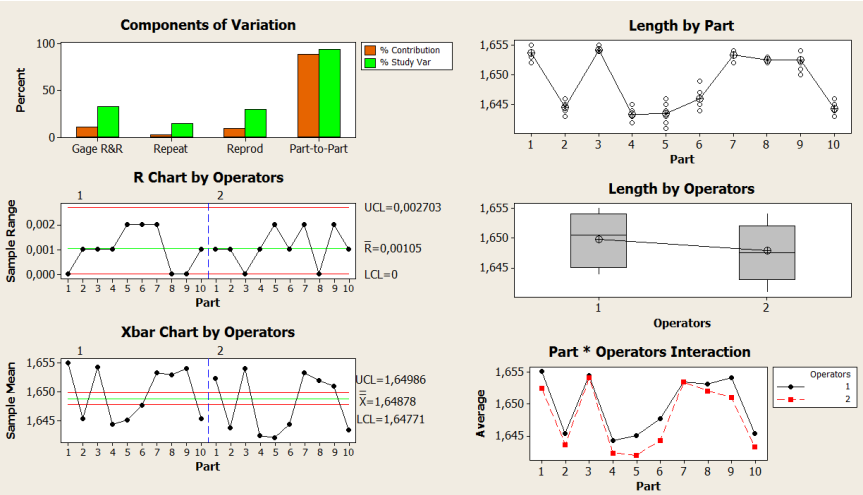

Figure 38: Graphical summary of the Gage R&R for the micrometer calliper

3.4.3 Laboratory Balance

The suitability of the measurement device for the weight had to be determined. Therefore ten different ceramic substrates are measured sequentially with a measuring device. Afterwards the same samples are measured randomly two times and all samples have been measured by two operators.

The *Two-Way ANOVA with Interaction* for the Laboratory Balance (Sartorius Lab Instruments, MSA225P-1CE-DI, ME-03398) can be seen in Figure 39. It shows that the connection between part and operator has no significant effect for the measurement. The *Part* and the *Operator* have a significant effect, as the p-value is smaller than 0,05.

The *Gage R&R* can be seen in Figure 40. The number of distinct categories is three and the resolution is 1,04 x 10^{-4} g. The *%R&R* relating to the total deviation is 39,92%. The parts we have used for the measurement are not representative for the total deviation. That is the reason why the value is above the limit. The *%R&R* relating to the tolerance is 5,20% and therefore the Laboratory Balance is measurable for the ceramic substrates.

In Figure 41 the graphical illustration of the *Gage R&R* for the Laboratory Balance is visible.

Two-Way ANOVA Table With Interaction

Source	DF	SS	MS	F	P
Part	9	0,0000001	0,0000000	64,0243	0,000
Operators	1	0,0000000	0,0000000	7,3835	0,024
Part * Operators	9	0,0000000	0,0000000	0,5115	0,857
Repeatability	40	0,0000000	0,0000000		
Total	59	0,0000001			

Alpha to remove interaction term = 0,25

Figure 39: Minitab excerpt of the Two-Way ANOVA for laboratory balance with interaction between operator and parts

Gage R&R

Source	VarComp	%Contribution (of VarComp)
Total Gage R&R	0,0000000	15,93
Repeatability	0,0000000	14,42
Reproducibility	0,0000000	1,51
Operators	0,0000000	1,51
Part-To-Part	0,0000000	84,07
Total Variation	0,0000000	100,00

Process tolerance = 0,002

Source	StdDev (SD)	Study Var (6 * SD)	%Study Var (%SV)	%Tolerance (SV/Toler)
Total Gage R&R	0,0000173	0,0001039	39,92	5,20
Repeatability	0,0000165	0,0000989	37,98	4,94
Reproducibility	0,0000053	0,0000320	12,30	1,60
Operators	0,0000053	0,0000320	12,30	1,60
Part-To-Part	0,0000398	0,0002387	91,69	11,94
Total Variation	0,0000434	0,0002604	100,00	13,02

Number of Distinct Categories = 3

Figure 40: Minitab excerpt of the *gage R&R* for the laboratory balance (ANOVA – Method)

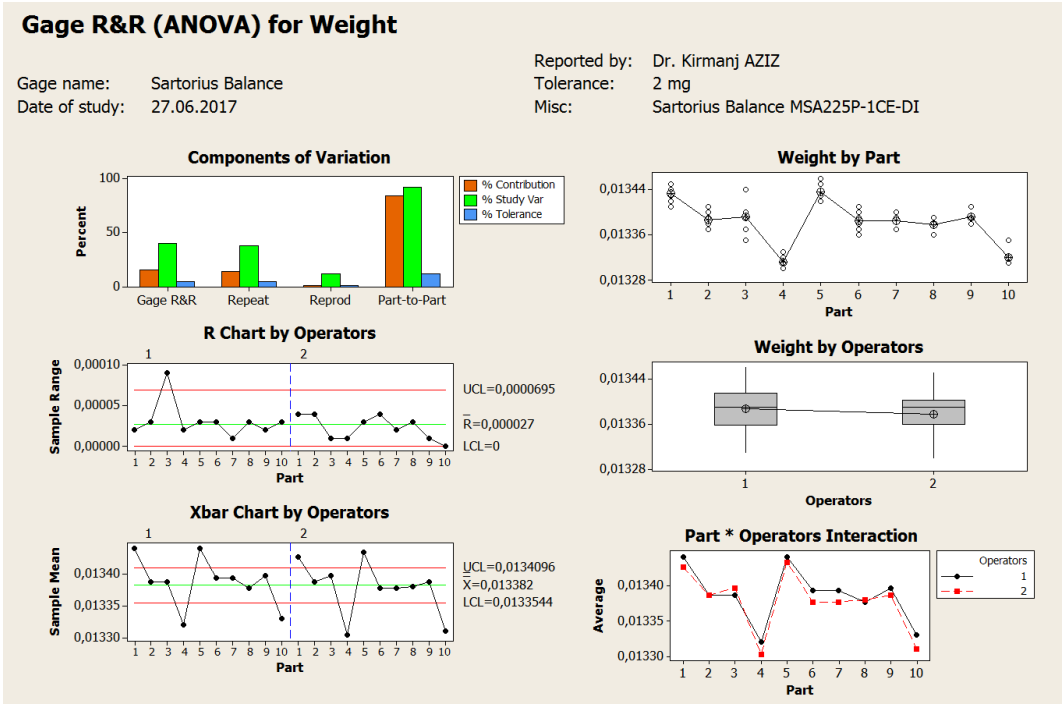

Figure 41: Graphical summary of the *Gage R&R* for the laboratory balance

3.5 Density Measurement

The knowledge of volume and weight of a ceramic are not expressive to compare the characteristics of different materials or designs. The density of a material for example is a comparable value. For determining the density of ceramics, a variety of methods can be applied. During the master thesis, the density is determined by geometric measurements or with a Helium-Pycnometer. [48]

3.5.1 Geometric density

The total density (ρ) is the ratio of weight (m) of a body to the total volume (V) of a substance with all its pores. The specimens to be characterized are rectangular and square green and sintered bodies. Due to the simple geometry, the density can be calculated by geometric measurements according to formula (12). [48]

$$\rho = \frac{m}{V} \tag{12}$$

$\boldsymbol{\rho}$ … $Density\ in\ g/cm^3$
$\boldsymbol{m}$ … $Mass\ in\ g$
$\boldsymbol{V}$ …$Volume\ in\ cm^3$

For this purpose, the mass of the green and sintered bodies (m) is weighted with the Laboratory Balance (Sartorius Lab Instruments, ME-03398). The height (h) and length (a) are measured with a micrometer caliper (Mitutoyo Digimatic; ME-03412).

3.5.2 He-Pycnometer

The measurement with the He – pycnometer is performed on a defined sample quantity. The sample quantity is introduced into the measuring cell of the pycnometer. Subsequently the measuring cell is filled with a specific pressure with helium and via a second cell (expansion cell) omitted. The filling pressure, the pressure after the expansion, the volume of the cell and the known amount of sample are used to calculate the density. For this purpose the He-Pycnometer – AccuPyc II 1340 V1.09 is utilized.

3.6 Morphological examinations

The microstructure of ceramics is determined by the manufacturing processes (e.g. composition and form of the raw materials, moulding, thermal treatment). The properties of the ceramics depend on the composition e.g. of raw material type, quantity, particle size and

purity. It is therefore necessary to carry out structure analysis, because this brings an essential contribution in optimizing ceramic materials. In the microstructure a wide range of investigation opportunities are possible, for example type and quantity of the phases and pores as well as their size, form, orientation and distribution. At atomic level (nm range) examinations of interstitials, dislocations and grain boundaries are possible. Suitable tools for characterizing the microstructure are microscopes. [15] [48] For the microstructure tests during the master thesis light microscope and scanning electron microscope are used.

3.6.1 Light optical microscope

With the light optical microscope resolution up to 0,3 µm can be achieved. [15] All samples have to be embedded, grinded and polished. Therefore examinations of fracture surfaces are not suitable. Microstructures become visible by etching with acids. [61] The samples were investigated by the reflected light microscope Olympus BX51M (asset number 87139).

The surfaces of the samples were investigated with Stereo Microscope Leica, WILD M3C (asset number 28747).

3.6.2 Scanning electron microscope

The scanning electron microscope (SEM) is one of the most important instruments for the investigation of bulk specimens. During the measurement, an electron beam is scanning a raster over a section of the sample. With the SEM, a resolution up to 2 nm can be achieved. [48] The spatial resolution is limited by the diameter of the electron beam.

Ceramics need to be coated with a thin, conductive layer to avoid local electrical charges and magnetization of the specimen. The samples are coated with carbon by physical vapor deposition. This procedure is not necessary in the case of NTC ceramics. All the samples are investigated with the Zeiss Merlin VP (asset number 87139).

For information about the topography of a sample, secondary electrons (SE) are used. They are produced form primary electrons (PE) of the electron probe and are known as SE 1. They resign from a depth of around 5 - 50 nm and their withdrawal probability depends on the surface quality. Their work function is ≤ 50 eV and the detector is fixed sideward of the specimen. [15] [62] [63]

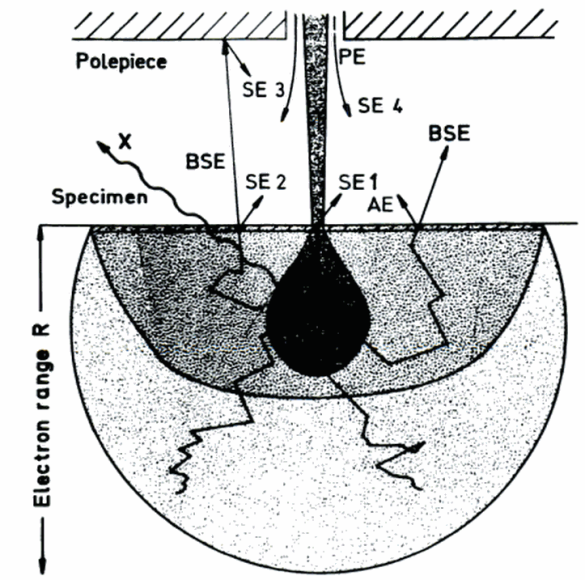

Figure 42: Scanning electron microscope – interaction volume

For information about the atomic number of elements, backscattered electrons (BSE) are used. The brighter the local position in the picture, the higher the atomic number. Consequently the intensity of the BSE depends on the electron density. Their work function is ≥ 50 eV and they come from a depth of around 50 – 100 nm. For this purpose, an EDX detector is used, because with an EDX detector the element composition can be analysed. To emit X-rays (specific energy for the corresponding element) the electrons of the specimen are stimulated by an electron beam.

The BSE can produce secondary electrons, too. They are designated as SE 2 or SE 3. The SE 2 resign in a surface layer of a large diameter (0,1 – 1 µm at 10 – 20 kV).

The SE 3 are produced when BSE is striking parts of the specimen chamber. A further group of SE is SE 4. They diffuse from the column to the specimen chamber. A good SE detector should not record SE 3 and SE 4. In Figure 42 all electron-specimen interactions are shown. The dark grey volume resigns X-rays and the medium grey volume BSE. The medium grey volume covers an information depth of about half of the electron range. [15] [62] [63]

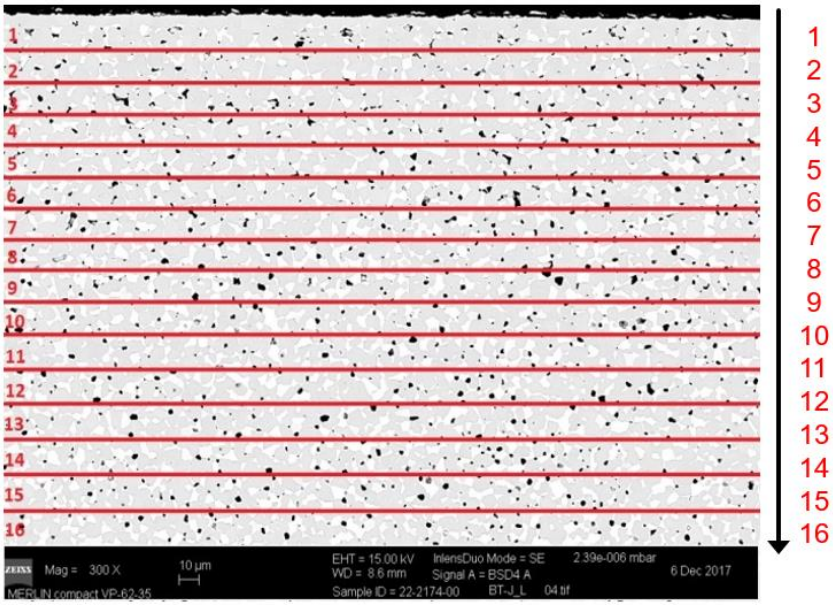

Figure 43: Example for a picture with BSE for the determination of NiO precipitation

The measurement of precipitations is performed with scanning electron microscope in backscattered mode. The content/ratio of precipitations is evaluated with the software Analyze. Therfore the pictures are subdivided into 16 regions with a width of 10 µm. In Figure 43 you can see the lines within the NiO precipitations are determined. Along the black arrow NiO precipitations are examined over the entire sample cross section, from the length and from the width of the specimen. In Figure 44 the selected sections are shown (red box) for the specimen 1x2 mm^2. Inside the red boxes the distribution of precipitations has been investigated. Along the black arrows the 16 subdivided regions of 10 µm are analysed, as demonstrated in Figure 43 and 44. For the sample cross-section a resolution of 150x and for the length and width of 300x was chosen.

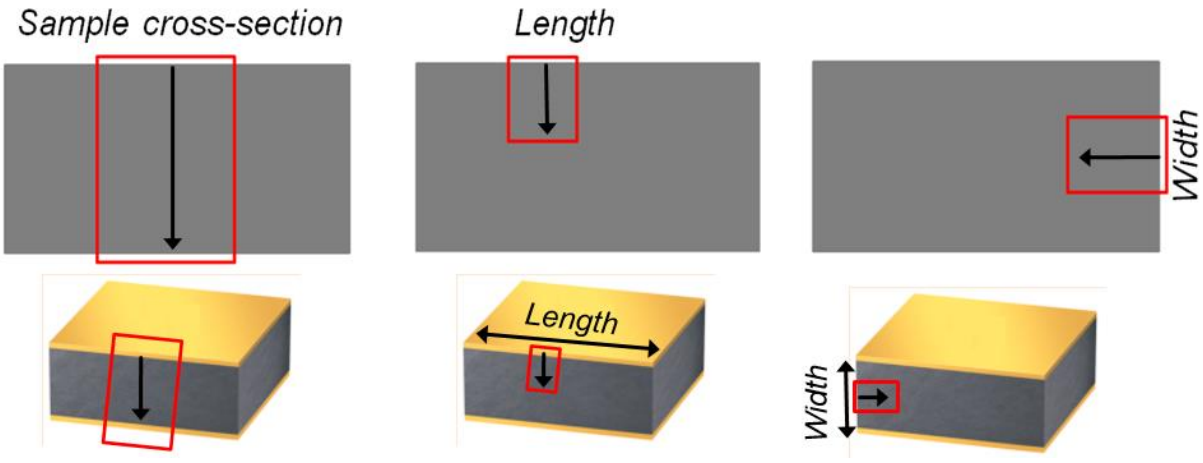

Figure 44: Selected sections for analyse the distribution of precipitations

3.7 Electrical Tests

For the measurement of the electrical properties, ceramic samples must be metalized. For standard chips the different sizes are cut out of substrates after metallisation, for non-standard chips the substrates are cut in different sizes before metallisation. After the metallization process, the samples are clamped in a special sample holder for the electrical measurements. The sample holders are immersed into heated oil baths and the resistances are measured with a special configuration of current and voltage. For the measurement a Keithley 2002 measurement device is used.

3.7.1 B-Value calculation

For the B-value calculation according to section 2.3 the resistances were measured at 25 °C and 100 °C.

3.7.2 Recording the characteristic curve

Characteristic curves can be calculated and formed by setting the value of temperature range and resistance tolerance (max. spread of resistance at temperature in %). For the characteristic curve the resistance was measured at -40 °C, 0 °C, 25 °C, 85 °C, 100 °C, 130 °C and 150 °C. The measured values are standardized to the resistance value at 25 °C and the deviation from the characteristic curve (standard performance curve) is plotted in a diagram. The maximum permissible deviation from the resistance marks the tolerance band (blue and red line in Figure 45). In Figure 45 an example of the tolerance band for a characteristic curve is shown. Throughout the total resistance-temperature profile, a deviation must be expected. The width of the tolerance band is not the same for all temperatures. For resistance at 25 °C (R_{25}) a resistance tolerance of ± 1% can be specified and for all other temperatures a resistance tolerance of max. ± 3% is tolerated.

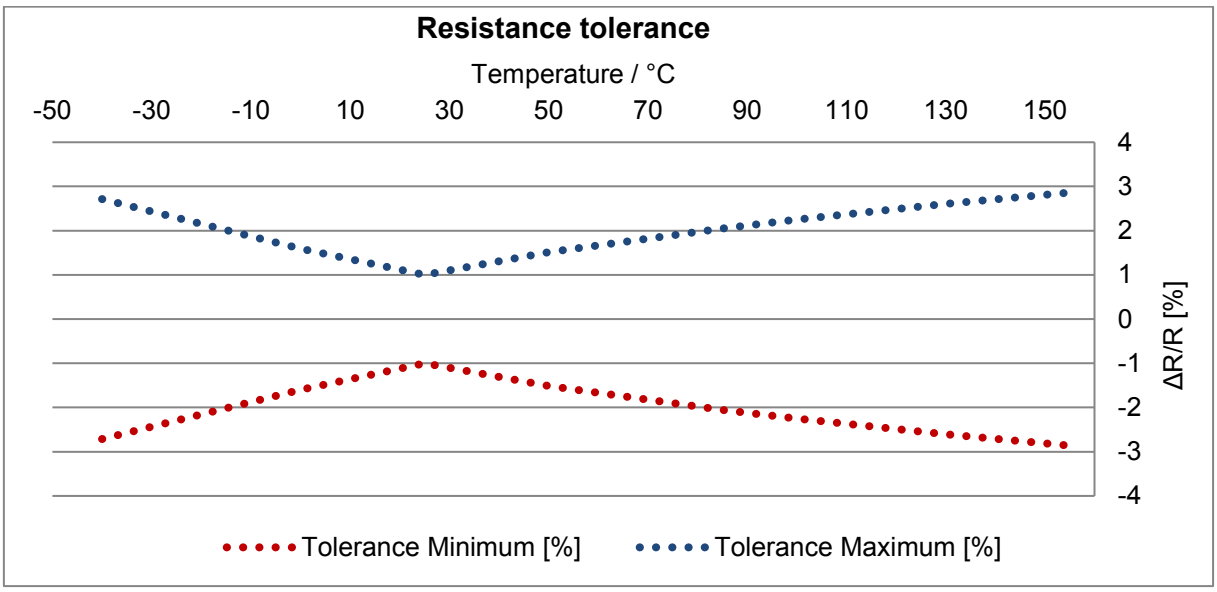

Figure 45: Characteristic curve with tolerance band

4 Results and Discussion

In the following chapter properties of a NTC ceramic like density, B-value, characteristic curve and microstructure are discussed. The variables are the size and the sinter properties of the samples. Each type of NTC was labelled with a sample ID. For the naming of all the substrates, the geometry of the green body is used. The production of the chips is divided into two groups: chips produced under standard conditions, labelled as *standard chips* and chips produced under non-standard conditions, labelled as *non-standard chips*. The *standard chips* are taken directly out from the production line of the company TDK in Deutschlandsberg, they are produced exactly in the same way as in mass production. The non-standard chips are made from substrates which are directly taken out of the production line as well, but they are cut to final size before debindering.

It is assumed that non-standard chips exhibit similar electrical properties as NTC discs. Regarding a possible electrical change and in particular the transformation of the characteristic curve, non-standard chips were evaluated in comparison to standard chips to verify this hypothesis.

4.1 Calculated Density of non-standard chips

Following section describes the density of green and sintered bodies, as well as the influence of the different chip sizes of NTC non-standard chips.

In Figure 46 the geometric density of green and sintered bodies in g*cm^{-3} is plotted against different sizes of chips. In general it can be said that the sintered bodies have a higher density than the green bodies and the smaller the sintered bodies are, the higher the density as can be seen in Figure 46.

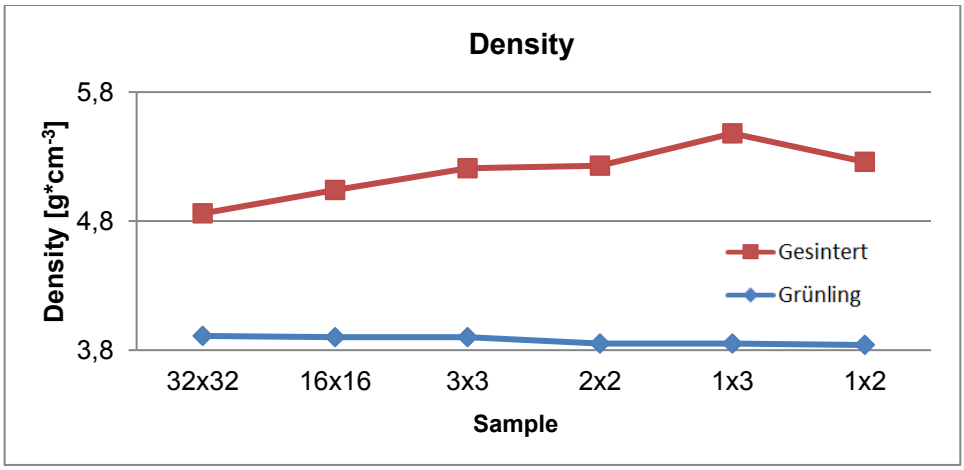

Figure 46: Calculated geometric density of green and sintered bodies

In table 1 the geometric density and the density measured with a He-pycnometer of green bodies are compared for the non-standard chip sizes 1x2, 2x2 and 3x3 mm^2. A small deviation between both methods is noticeable. The density measured with He-pycnometer is slightly higher than the geometric density. The reason could be a small portion of accessible porosity that is filled with Helium resulting in a higher density value.

Table 1: Density of green bodies

Sample	**1x2 mm^2**	**2x2 mm^2**	**3x3 mm^2**
Geometric density [g/mc^3]	3,84 ± 0,18	3,85 ± 0,13	3,90 ± 0,06
He-Pycnometer [g/mc^3]	3,9191 ± 0,0004	3,9158 ± 0,0006	3,9181 ± 0,0003

4.2 Evaluation of the electrical properties

The section “evaluation of the electrical properties” gives an overview of the measured resistance and the calculated B-value. The variables between the samples are the sizes of the green bodies and chips which are taken directly out of the production line and cut to final size before debindering. All other parameters (e.g. sintering) are equal.

4.2.1 Characteristic curve

This section describes the characteristic curves for NTC *standard chips* and *non-standard chips* compared to the nominal characteristic curve.

Standard chips

Standard chip are chips which are directly taken from the production line. More detailed description for chips labelled as *standard chips* can be found in chapter 3.3. In Figure 47 the percentage deviation of standard chips from the nominal characteristic curve is plotted over the temperature in °C. These chips are cut out from standard substrates which have the size of 32x32 mm^2. The sizes of the chips which are cut out are 1x2 mm^2, 2x2 mm^2 and 3x3 mm^2. As shown in Figure 47, the deviations of all those chips lie within the area of the tolerance range, except for the at –40 C. Between the chip sizes, 1x2 mm^2, 2x2 mm^2 and 3x3 mm^2 in Figure 47 no significant difference in the deviations can be noticed.

In Figure 48, the percentage deviation from the nominal characteristic curve over the temperature in °C is plotted, for chips cut out from standard substrate with a size of 16x16 mm^2. The sizes of the cut out chips are 1x2 mm^2, 2x2 mm^2 and 3x3 mm^2 as well. In Figure 48 can be discerned, that the deviations from those chips lie within the area of the tolerance

range, except for the values at –40°C. Again the deviations at -40 C are out of the tolerance range. Between the chip sizes 1x2 mm^2, 2x2 mm^2 and 3x3 mm^2 in Figure 48, no significant difference in the deviations can be noticed.

The only difference between the plotted curves in Figure 47 and 48 is the geometric size of the initial substrates, namely 32x32 mm^2 and 16x16 mm^2. The sinter parameters as well as the production conditions are identical. The characteristic curves of chips cut out of these two substrates can be regarded as equal. Thus there is no major difference in the electrical properties of chips if substrates are sintered in substrate sizes 32x32 mm^2 or 16x16 mm^2. In both figures (47 and 48) can be seen that the deviation of the measured standardized values at -40 °C, the course of the characteristic curve from the chips are outside the tolerance range.

In Figure 49 the percentage deviation for standard chips and disc from the nominal characteristic curve is plotted over the temperature in °C. The chips are produced by tape casting and cut out as a 1x2 mm^2 chips from a standard substrate with a size of 32x32 mm^2 and the discs are produced by pressing of granulates. As Figure 49 illustrates all deviations from discs lie within the required area of the tolerance range and the deviations from chips lie within the area of the tolerance range except the values at -40 °C.

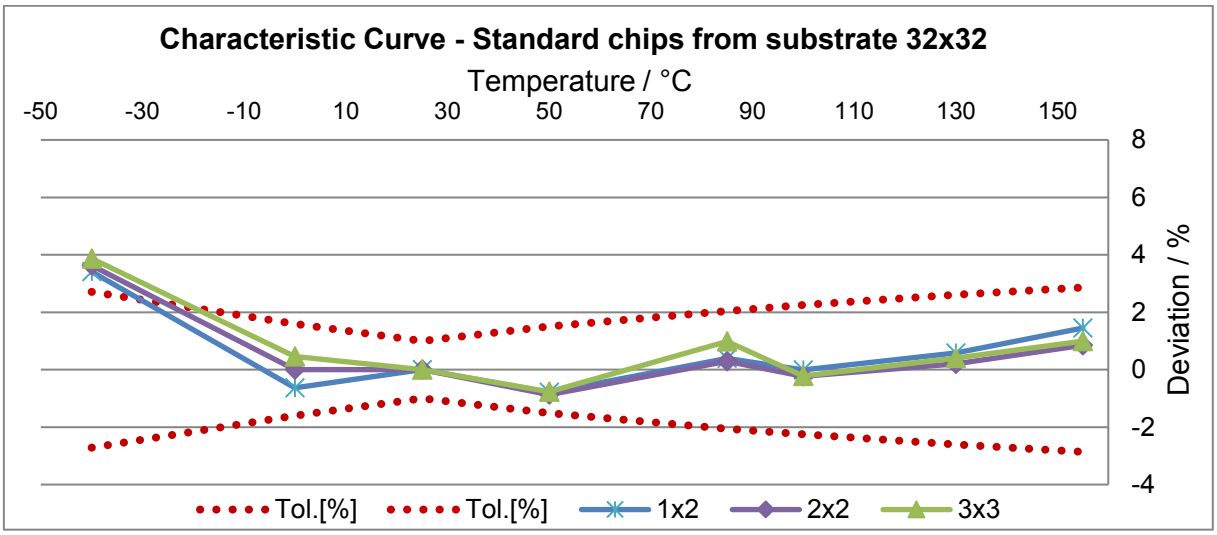

Figure 47: Characteristic curves of standard chips: 1x2, 2x2, 3x3 mm^2 cut from standard substrate 32x32 mm^2

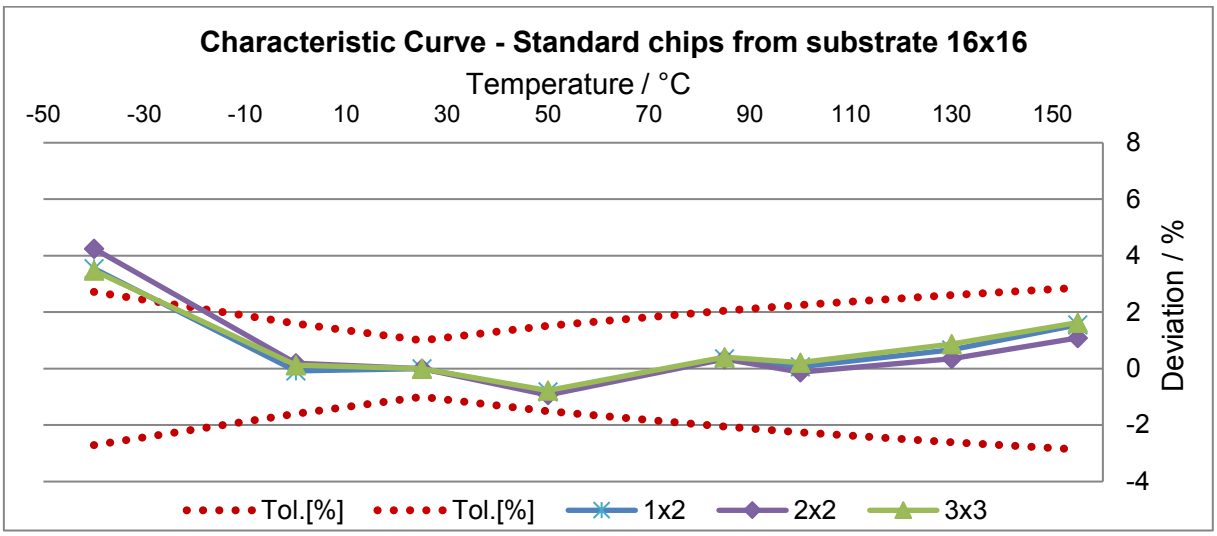

Figure 48: Characteristic curves of standard chips: 1x2, 2x2, 3x3 mm² cut from standard substrate 16x16 mm²

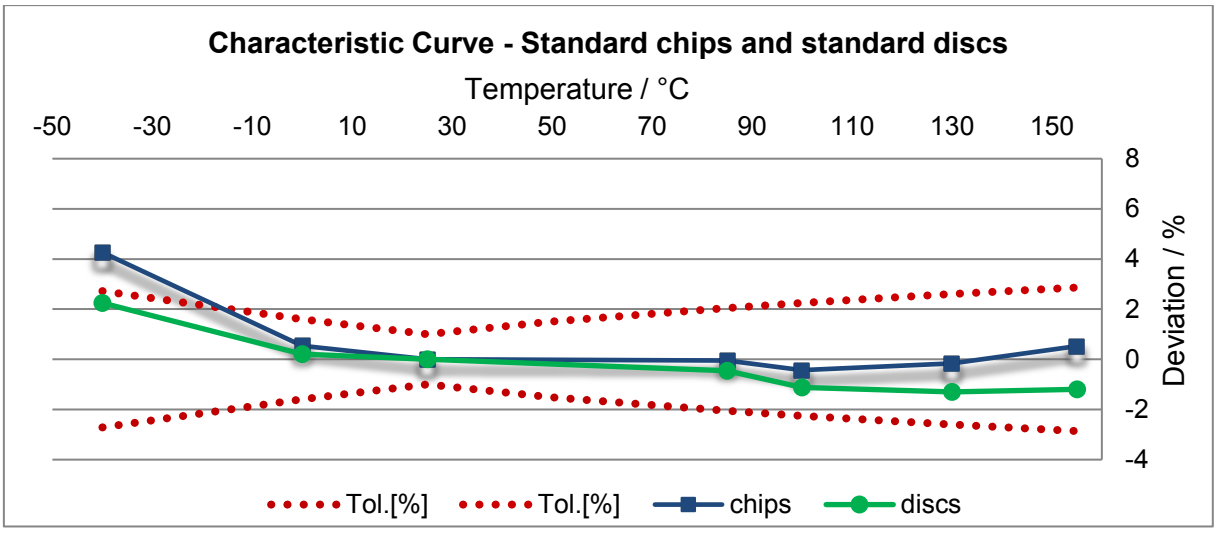

Figure 49: Characteristic curves of NTC standard chips and standard discs

Non-standard chips

The special feature of *non-standard chips* is the fact that the substrates were taken from the production line and cut to chip size before debindering. Because of this change of procedure they had to be metallized with the special metallization device. More detailed description for chips labelled as *non-standard chips* can be found in chapter 3.3.

In Figure 50 the percentage deviation for non-standard chips from the nominal curve is plotted over the temperature in °C. The sizes of the chips are: 1x2, 1x3, 2x2 and 3x3 mm². As shown in Figure 50, the deviations from all those chips lie outside the tolerance range apart from the measurement values at 25 °C, 0 °C and –40 °C. Between the chip sizes 1x2 mm², 1x3 mm², 2x2 mm² and 3x3 mm² a difference in the deviations can be noticed.

The comparison between standard chips (Figure 47, 48 or 49) and non-standard chips (Figure 50) shows a significant difference. The deviations of the non-standard produced chips are larger, especially towards higher temperatures. It also indicates a clear tendency: the smaller the chip, the higher the deviation. This trend becomes much more apparent when we look at Figure 51.

In Figure 51 the percentage deviation from the nominal characteristic curve is plotted over the temperature in °C for all standard chips as well as non-standard chips which are produced during the master thesis. The sizes of the chips which are evaluated are for standard chips: 32x32 mm^2 and 16x16 mm^2 and for non-standard chips: 40x40, 12x12, 10x10, 8x8, 5x5, 3x3, 2x2, 1x2, 1x3 mm^2. The dotted lines show all chips, which are not within the area of the tolerance band. These are standard chips: 32x32 and 16x16 and non-standard chips: 40x40, 3x3, 2x2, 1x2, 1x3 mm^2. The continuous lines represent chips, which are within the area of the tolerance band. These are the non-standard chips: 12x12, 10x10, 8x8 and 5x5 mm^2.

With non-standard chips 12x12, 10x10, 8x8 and 5x5 mm^2 the expected changes in characteristic curves can be achieved. Here the deviations from 12x12, 10x10, 8x8 and 5x5 mm^2 non-standard chips lies within the area of the tolerance range.

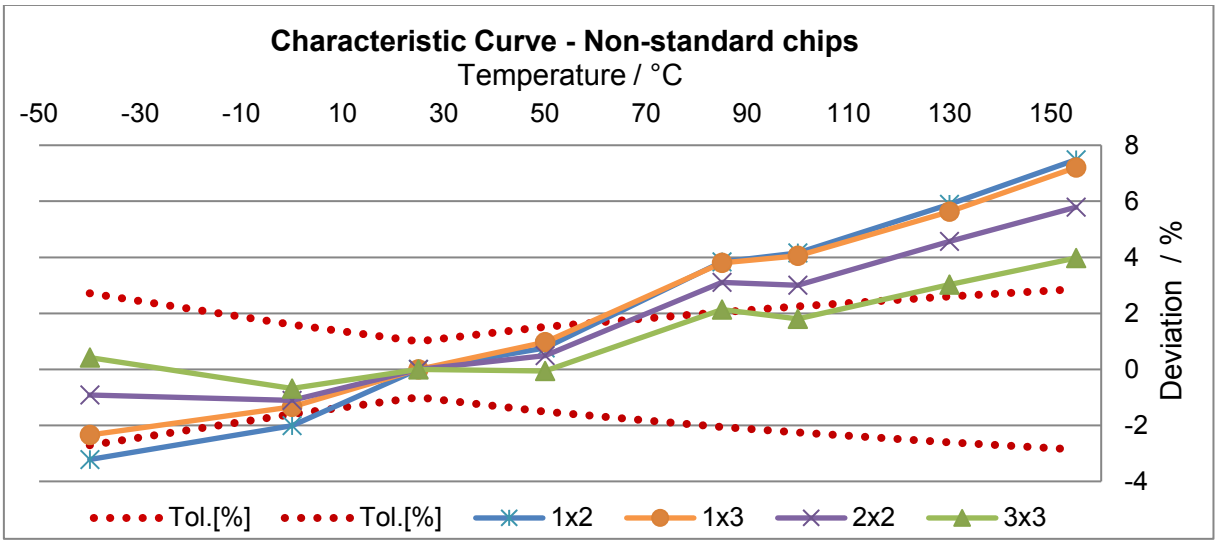

Figure 50: Characteristic curve of non-standard chips: 1x2, 1x3, 2x2, 3x3 mm^2

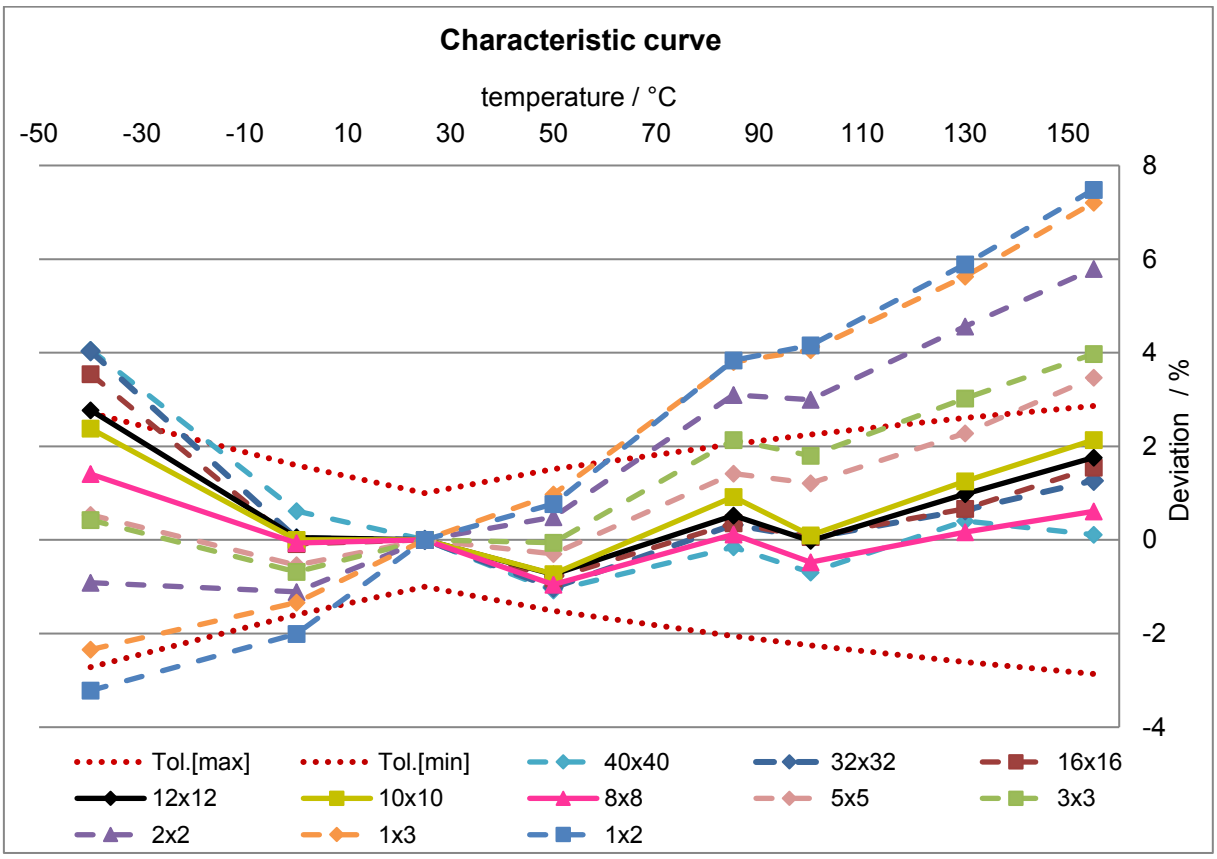

Figure 51: Characteristic curves of standard chips: 32x32 and 16x16 and non-standard chips: 40x40, 12x12, 10x10, 8x8, 5x5, 3x3, 2x2, 1x2, 1x3 mm^2

4.3 B-value

In Figure 52 the B-values in K of standard and non-standard chips are plotted against different sizes of chips. The blue curve in Figure 52 represents the results from the standard substrate 32x32 mm^2 and its chips in the sizes 3x3, 2x2 and 1x2 mm^2. The green curve in Figure 52 represents the results from the substrate 16x16 and its chips in the sizes 3x3, 2x2 and 1x2 mm^2. As Figure 52 shows, there is no significant difference whether the substrates are sintered with a size of 32x32 mm^2 or 16x16 mm^2. The sizes of the chips which have been cut out from the substrate 32x32 mm^2 and 16x16 mm^2 have no influence of the B-value either.

The green curve in Figure 52 represents the non-standard chips. The sizes of the chips are 3x3, 2x2 and 1x2 mm^2. As can be seen in Figure 52 the B-values decreases significantly, the smaller the non-standard chips are. There also is a significant difference between the B-values of standard and non-standard chips. The smallest B-value of all samples has the 1x2 mm^2 non-standard chip, it amounts to 3494 ± 0,1 K.

In Figure 53 the B-values in K of standard and non-standard chips are plotted against different sizes of chips: 32x32, 16x16, 12x12, 8x8, 5x5, 3x3, 2x2, 1x3 and 1x2 mm^2. As can be seen in Figure 53, there is no significant difference between the B-values of the standard chips 32x32 mm^2 and. This trend continues until chip geometry 10x10 mm^2, afterwards the B-value drops continuously. The smaller the sintered chip is, the lower the B-value. In Figure 53 the drop of the value can be clearly seen.

In Figure 54 the B-values in K of 1x2 mm^2 chips are plotted against different sizes of chips. The 1x2 chips are cut out of standard chips: 32x32 mm^2 and 16x16 mm^2 and non-standard chips: 40x40, 12x12, 10x10, 8x8 mm^2 and the non-standard chip 1x2 (without cutting). In Figure 54 it is easy to see that there is no significant difference between chips from standard substrates: 32x32 mm^2 and 16x16 mm^2 and non-standard substrates: 40x40, 12x12, 10x10, 8x8 mm^2. Only for the non-standard as fired chip 1x2 mm^2 chip a drop-off the B-value is apparent and a significant difference can be observed.

In Figure 55 the standard deviation test for the B-value of 1x2 mm^2 chips is shown. The plotted sizes of chips in Figure 55 are: standard chips: 32x32 mm^2 and 16x16 mm^2 and non-standard chips: 40x40, 12x12, 10x10, 8x8 mm^2 and the non-standard chip 1x2 (without cutting). In Figure 55 it is clearly identifiable that there are no significant differences in B-values between chip geometries 40x40 to 8x8 mm^2, only 1x2 mm^2 is significantly different.

Due to the B-values and the deviations of characteristic curve from standard and non-standard chips, investigations of the microstructure are carried out. The evaluation can be seen in chapter 4.5.

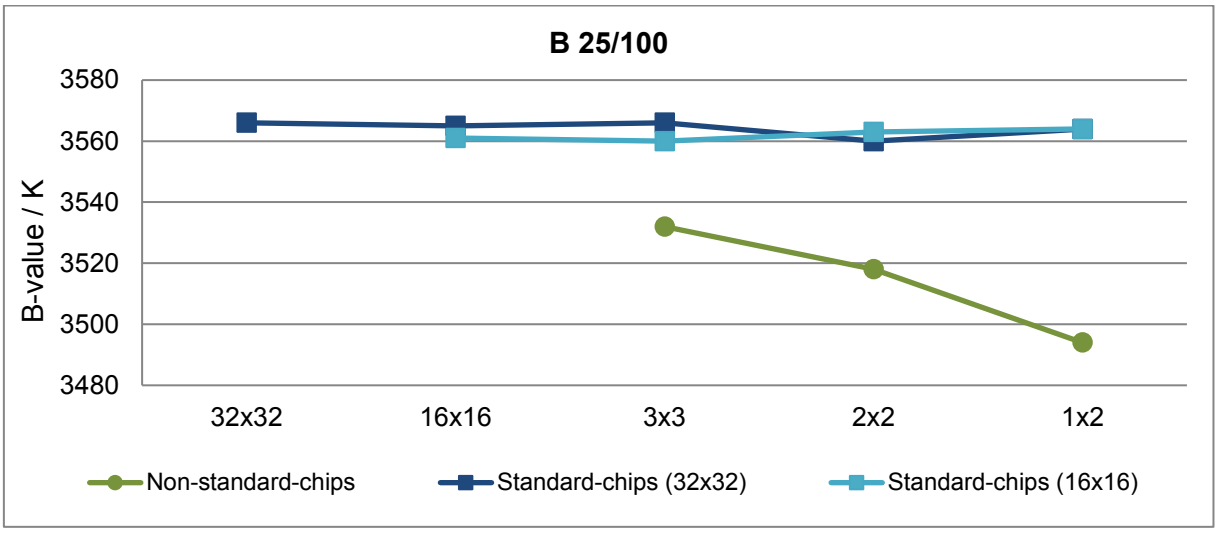

Figure 52: B-value of standard chips: 32x32 mm^2 (16x16, 3x3, 2x2 and 1x2) and 16x16 mm^2 (3x3, 2x2, and 1x2) and non-standard chips: 3x3, 2x2, and 1x2 mm^2

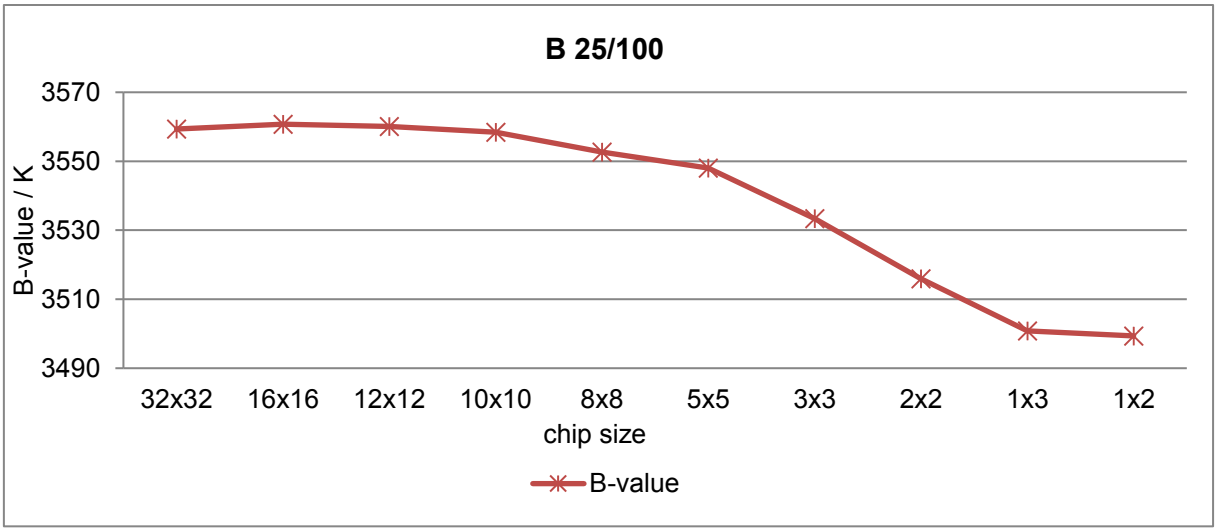

Figure 53: B-value of standard chips: 32x32 mm^2, 16x16 mm^2 and non-standard chips: 12x12, 8x8, 5x5, 3x3, 2x2, 1x3 and 1x2 mm^2

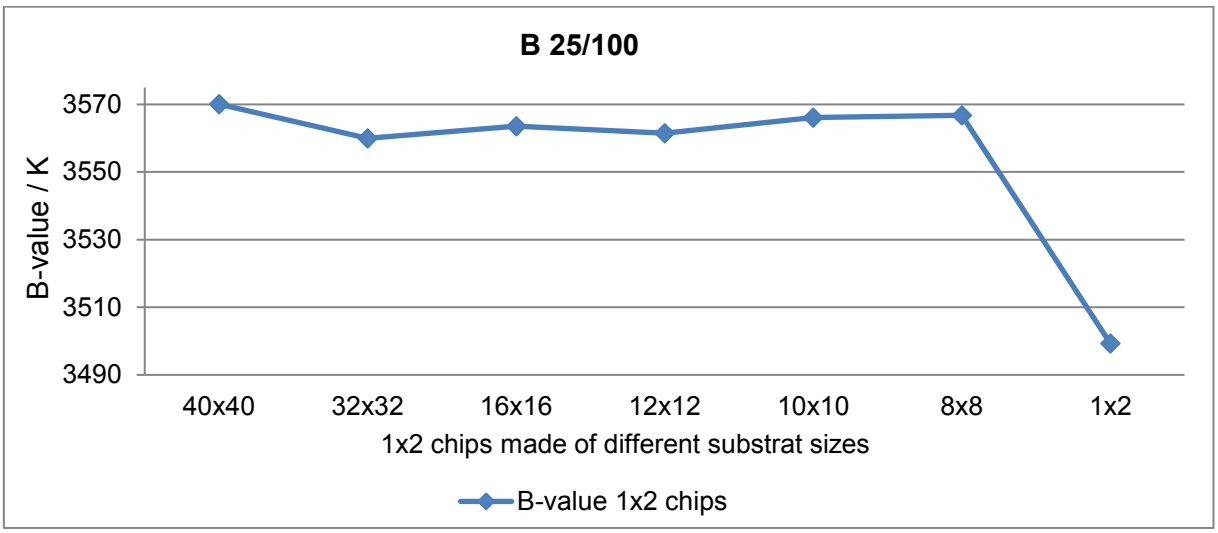

Figure 54: B-value of 1x2 mm² chips of standard substrates: 32x32 mm² and 16x16 mm² and non-standard substrates: 40x40, 12x12, 10x10, 8x8 mm² and the non-standard chip 1x2 mm² (without cutting).

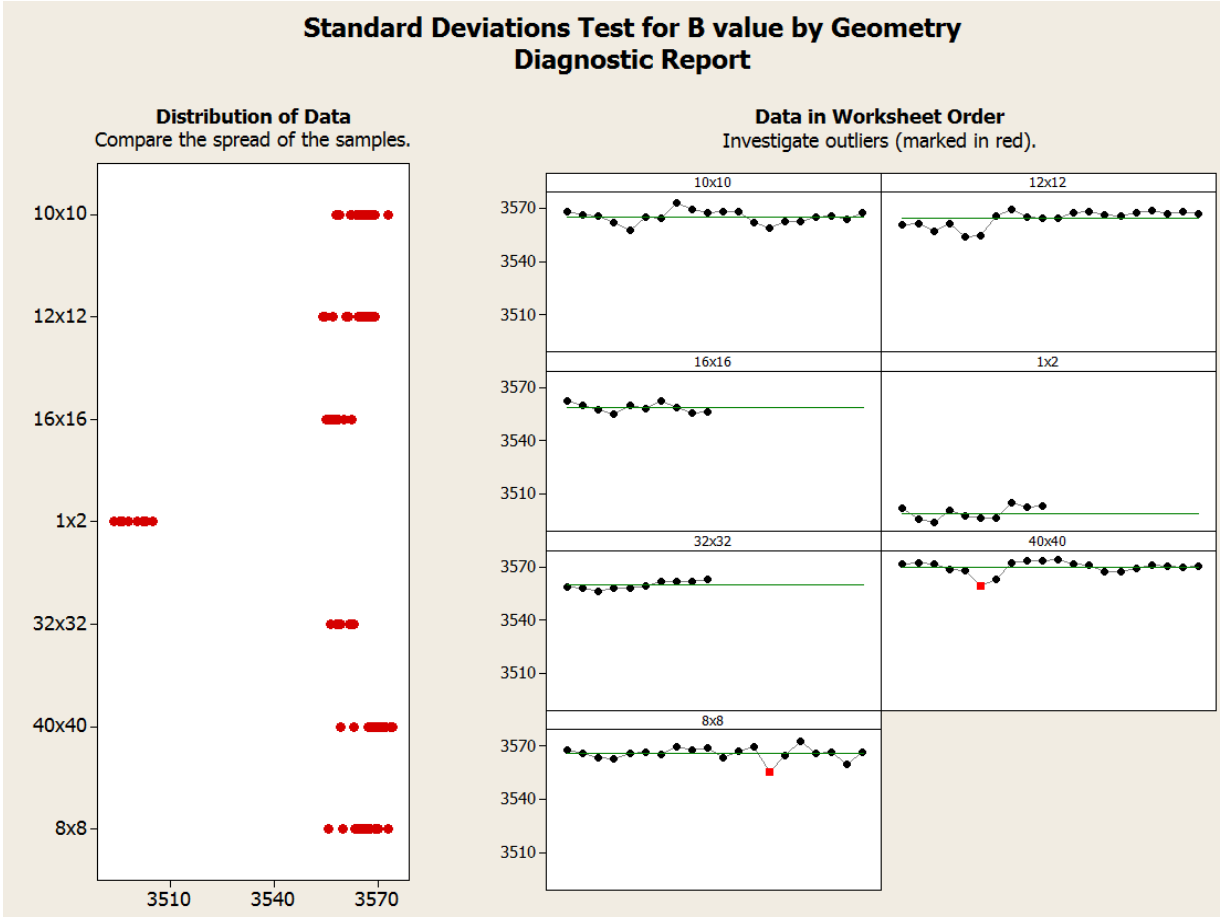

Figure 55: Standard deviation test for B-value by geometry of 1x2 standard substrates: 32x32 mm² and 16x16 mm² and non-standard substrates: 40x40, 12x12, 10x10, 8x8 mm² and the non-standard chip 1x2 mm² (without cutting).

4.4 Evaluation of the microstructure

This section gives an overview of microstructural features of the samples. Precipitations and porosity distribution was determined quantitatively. All samples consist of the same material and are sintered with the same sinter parameters. The specimens only differ by their size and they are inspected before being metallized.

4.4.1 Phase analysis

Rich areas of Ni are detected with the EDX analysis. Ni-rich phases in the ceramic can be seen in Figure 56 as light grey areas. The black areas are pores and the dark grey areas represent the spinel phases. Table 2 contains the composition of different areas. The typical spinel composition was detected in Spectra Nr. 1, 2 and 6. Ni-rich areas are detected in Spectra Nr. 4, 3 and 5.

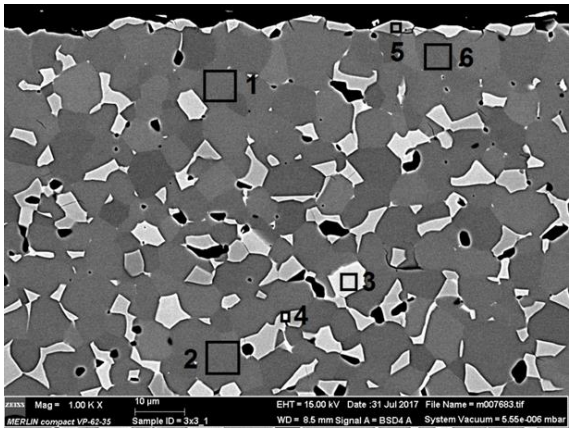

Figure 56: Microstructure of ceramics with EDX analysis (area indicated by numbered square).

Table 2: EDX spectrum of selected areas in Fig. 56

Spectrum Nr.	O [% w/w]	Mn [% w/w]	Co[% w/w]	Ni [% w/w]	Zr [% w/w]
1	23,66	38,65	16,45	21,24	0,47
2	20,8	40,61	13,56	14,21	
3	17,85	5,57	11,13	65,45	
4	21,19	22,87	13,08	42,85	
5	17,9	2,79	9,1	70,21	10,82
6	23,7	35,78	17,49	23,04	

4.4.2 Distribution of NiO Precipitations

This chapter describes the existence of Ni-rich precipitations and their distribution over the entire sample cross section as well as the length and the width of the specimen.

For these investigations, all samples are cut into 1x2 mm^2 specimen, except the sample 1x2 mm^2, that sample has not to be cut. After polishing SEM images were taken as described in section 3.6.2 (cf. Fig. 43 and 44).

Figure 57 represents SEM pictures in BSE mode from the edge of the specimen to the center, along the length from four different sample sizes: 1x2, 5x5, 8x8 and 40x40 mm^2, which are used to determine the fraction of NiO precipitations in the ceramics. In Figure 58 the analysis of precipitation distribution in % is plotted over 16 subdivided regions along the length of 5 different sintered chip sizes. The sizes of the chips are: 40x40, 32x32, 8x8, 5x5 and 1x2 mm^2. As demonstrated in Figure 58, there is no significant difference between the varied sintered chip sizes. All chips have an increase of precipitations from the edge of the specimen, between 8 and 20 % to the center of the specimen, between 20 to 24 %. Obviously the ceramic decomposes during sintering, because according to the phase diagram (Figure 15) at this temperature a spinel phase with higher manganese content coexists with NiO. This decomposition reaction is accompanied by a loss of oxygen (see Equ. yy). During cooling of the ceramic this decomposition should be reversed, but due to the densification during sintering the necessary oxygen from the atmosphere can only diffuse slowly into the ceramic. This explains that the NiO precipitations near the surface of the specimens are reduced but in the center still the equilibrium situation at sintering temperature is maintained. This partial reversal of the decomposition also changes the composition of the spinel phase and by that the electrical properties of the spinel phase. Along the length of the specimens this is equal for all sizes, so there should be no size dependent differences in the electrical properties

In Figure 59 one can see SEM pictures in BSE mode from the edge of the specimen to the centre along the width from four different sample sizes: 1x2, 5x5, 8x8 and 40x40 mm^2, which are used to determine the fraction of NiO precipitations in ceramics. In Figure 60 the analysis of precipitation distribution in % is plotted over 16 subdivided regions along the width of 5 different sintered chip sizes. The sizes of the chips are: 40x40, 32x32, 8x8, 5x5 and 1x2 mm^2. As one can see in Figure 60, there is no significant difference between the varied sintered chip sizes: 40x40, 32x32, 8x8, 5x5 mm^2 except the chip size: 1x2 mm^2. At the chip size 1x2 one can see that also from the sides the oxygen can access the ceramic and a reversal of the decomposition reaction takes place resulting in a reduced amount of NiO precipitations. The specimens from 40x40, 32x32, 8x8, 5x5 mm^2 samples have a constant

precipitation distribution from the edge of the specimen to the center of the specimen (from 20 to 24 %) because they are cut from larger samples and the sides, which are in contact with the atmosphere are removed.

As mentioned above, in such regions with reduced amount of NiO precipitations, sometimes called “sintered skin”, the spinel phase has a different composition than the spinel phase in the center. The manganese content of the spinel phase is lower in the region with lower amount of NiO precipitions. Thus the 1x2 mm^2 non-standard chip has a smaller B-value and the R/T characteristic differs significantly from the standard chip.

In Figure 61, one can see schematically a non-standard 1x2 mm^2 chip on the left side and a standard 1x2 mm^2 chip cut out of a larger substrate after sintering on the right side. It demonstrates the differences of the distribution of precipitations between standard and non-standard chips. The region of higher amount of NiO precipitations in the ceramic is shaded light grey and the region of lower amount of NiO precipitations in the ceramic is shaded dark grey. Chips that are cut before sintering have an additional region of lower amount of NiO precipitations (and consequently a spinel phase with lower manganese content) at the sides, which is responsible for the differences in the electrical characteristic.

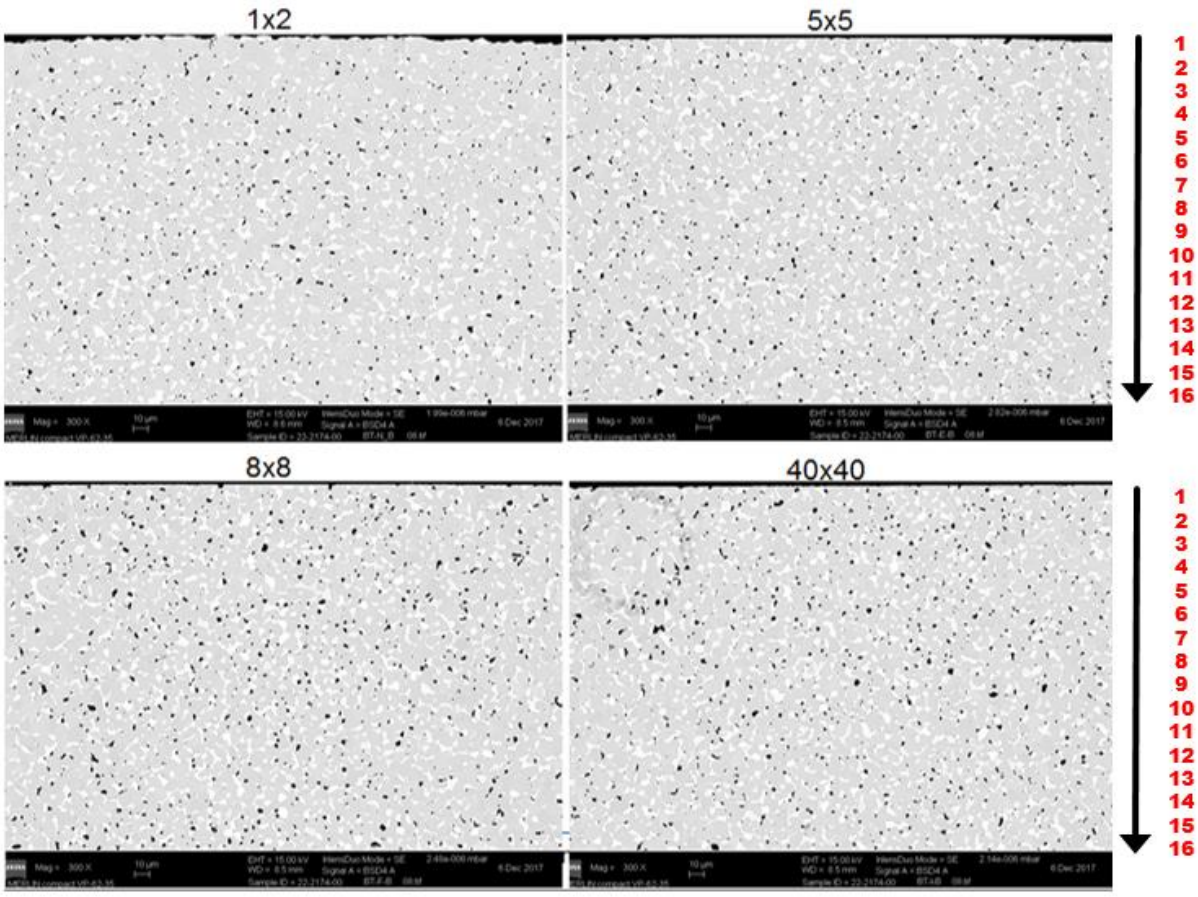

Figure 57: SEM pictures in BSE mode for the length in four different sinter geometries from 1x2 mm^2 chips cut out off: 40x40, 8x8 and 5x5 mm^2 substrates and 1x2 mm^2 non-standard chip

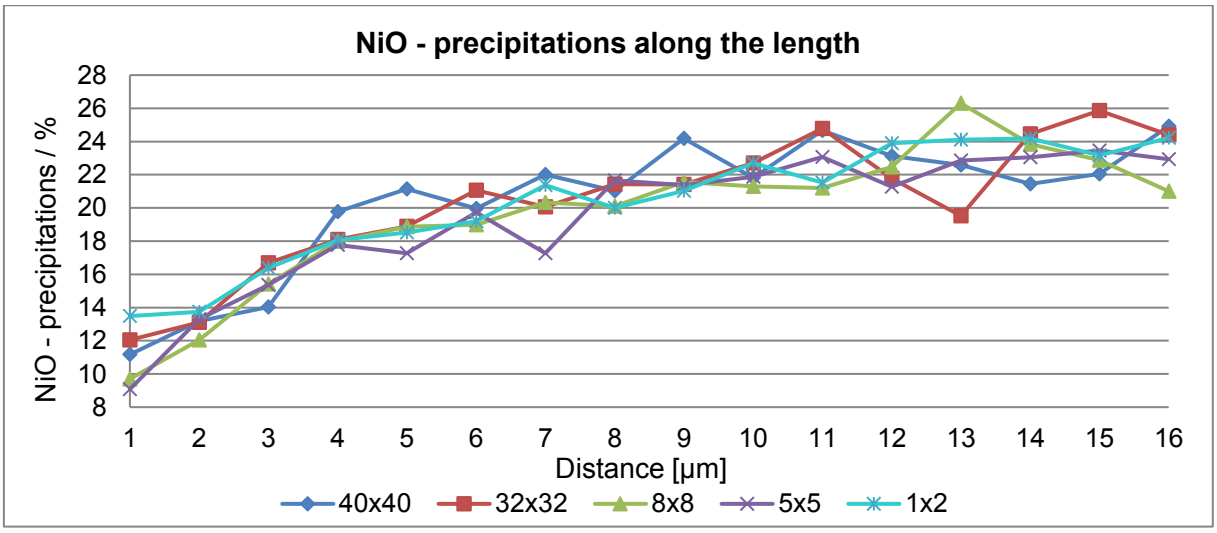

Figure 58: Precipitation distribution along the length from 1x2 mm^2 chips cut out of: 40x40, 32x32, 8x8, 5x5 mm^2 substrates and 1x2 mm^2 non-standard chips

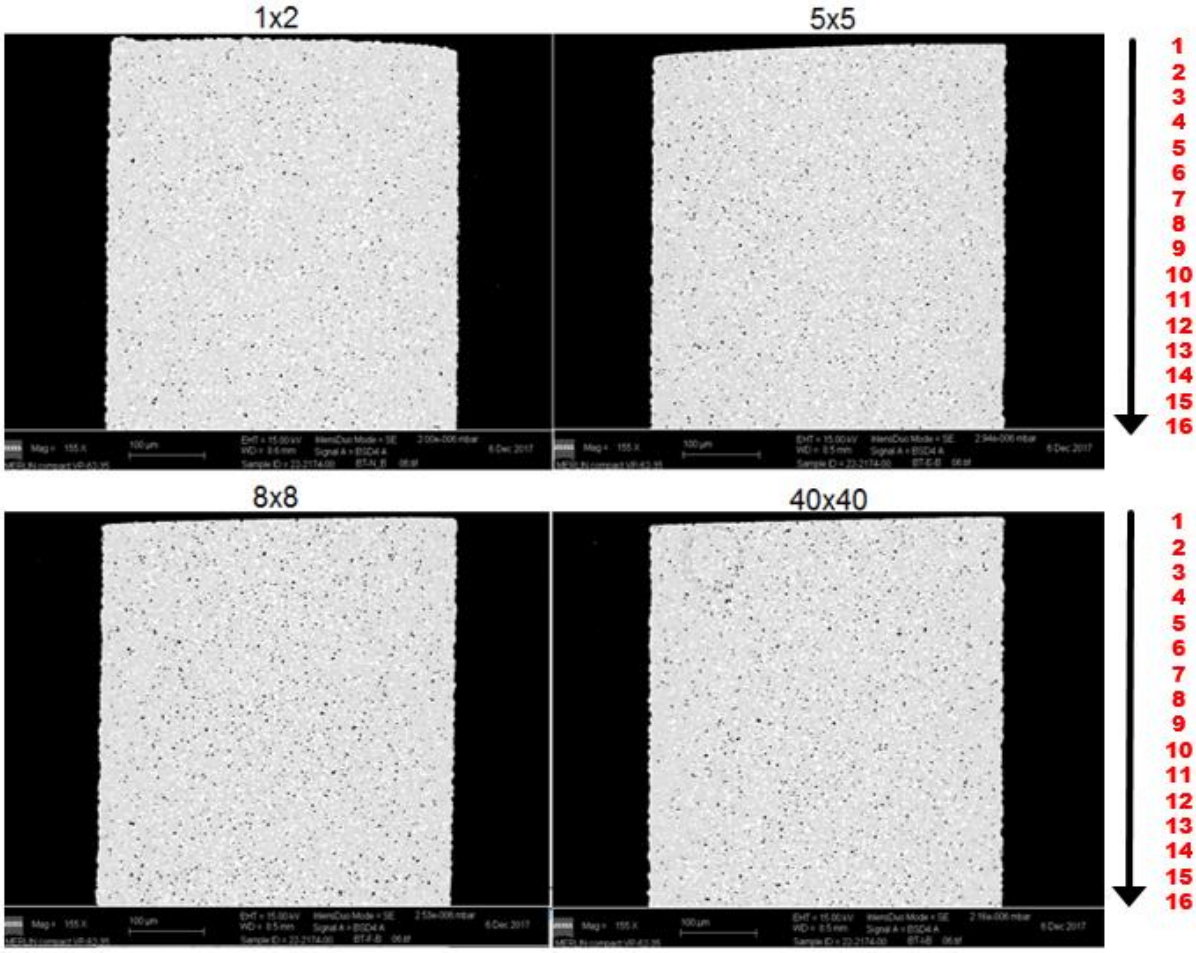

Figure 59: SEM pictures in BSE mode for the width in four different sinter geometries: from 1x2 mm^2 chips cut out from: 40x40, 8x8 and 5x5 mm^2 substrates and 1x2 mm^2 non-standard chip

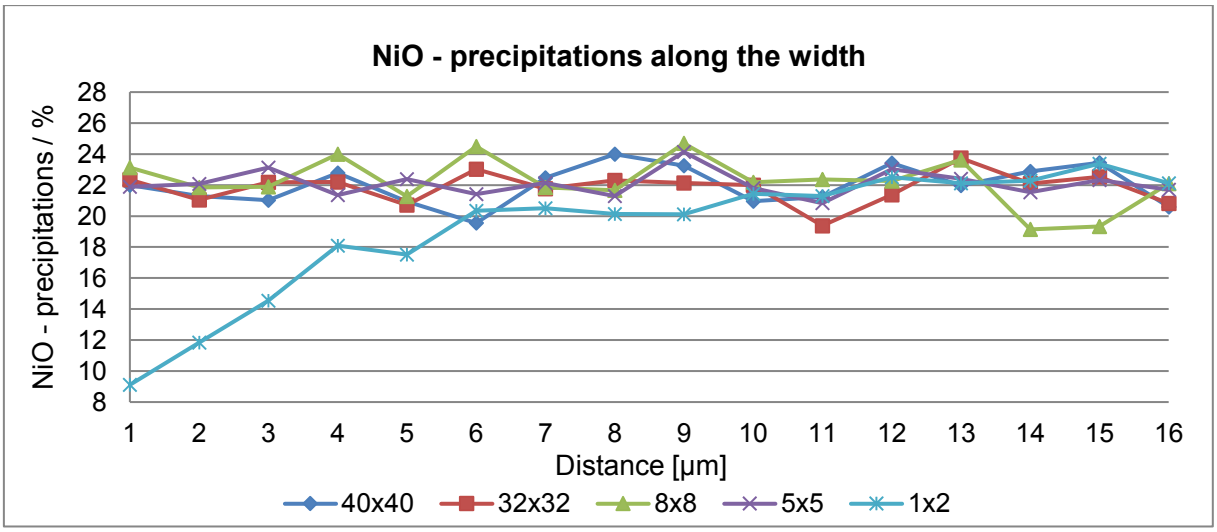

Figure 60: Precipitation distribution along the width from 1x2 mm^2 chips cut out from: 40x40, 32x32, 8x8 and 5x5 mm^2 substrates and 1x2 mm^2 non-standard chip

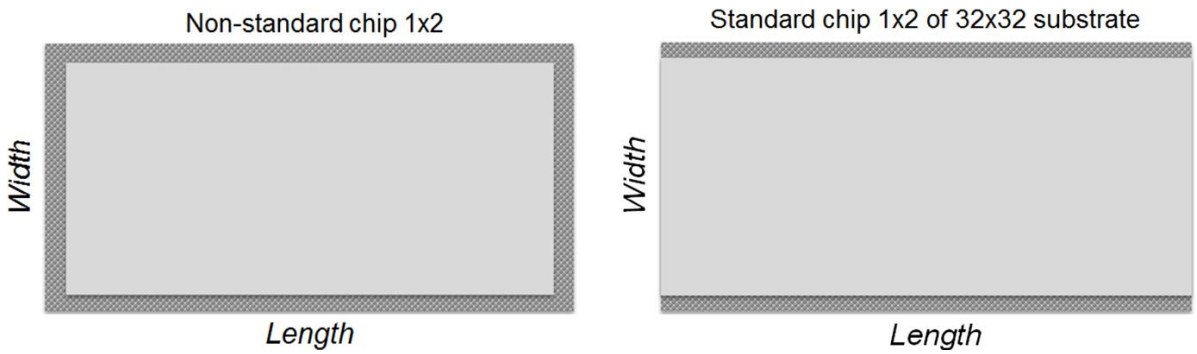

Figure 61: Comparison of NiO precipitation non-standard 1x2 mm^2 chip and standard chip 1x2 mm^2 chip cut out of a larger substrate after sintering. The region of higher amount of NiO precipitations is shaded light grey and the region of lower amount of NiO precipitations is shaded dark grey.

4.5 Design of Experiments: Evaluation of Sintering Parameter

This section gives an overview of the Design of Experiments (DoE) applied on sintering parameters. The relevant process parameters for sintering can be found in the process mapping (see Fig. 62). For the carried out DoE the factors *Maximum Temperature* and *Dwell time* are examined. The variables between the samples are the different sizes of non-standard chips: 1x2, 1x3, 2x2 and 3x3 mm^2. The detailed DoE plan is listed in table 3.

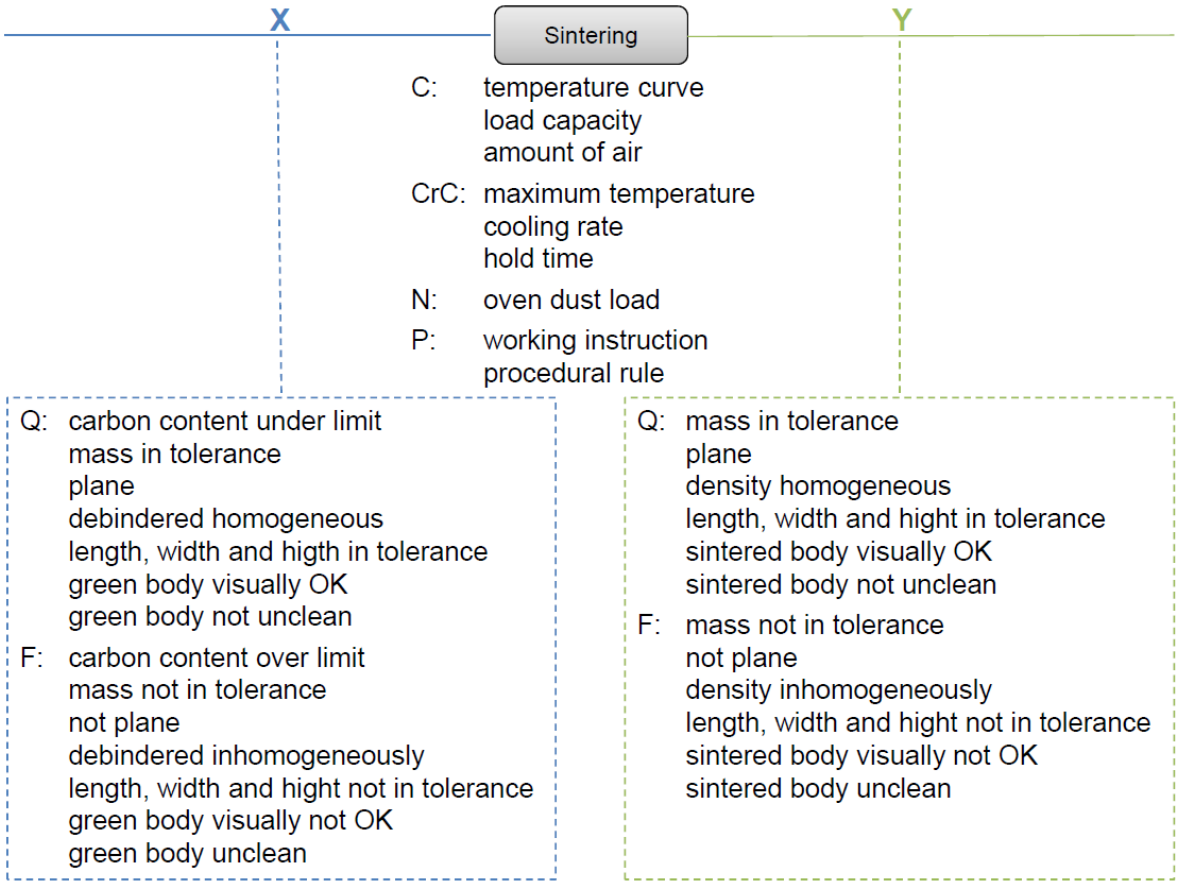

Figure 62: Process Mapping
X: Input parameters of the first process step, e.g. the product- or quality characteristics.
Y: Output parameters of the last process step, e.g. the product- or quality characteristics.
C: Controllable factors, which are changeable during the process.
CrC: Critical controllable factors, these factors have particular wide influence on the process outcome.
N: The disturbance value N (Noise) has bad influence especially on the spreading of the product characteristics.
P: The procedure parameters influence the values of the whole process.
Q: Desired results according to quality standards.
F: Undesired and faulty but possible process results.

The standard sinter parameters are chosen as center point (Maximum Temperature 1195 °C, Dwell time 120 min and Cooling rate 0,74 K/min). 1240 °C and 360 min is the highest temperature and longest dwell time, respectively 1140 °C and 30 min is the lowest temperature and shortest dwell time. To start with these sintering parameters are selected. Later the temperature 1240 °C and dwell time 30 min and the temperature 1140 °C and dwell time 360 min were added. For every test point ten samples were evaluated. The results were analyzed with Excel and Minitab. For the purpose of this thesis, R_{25}, R_{100}, B-value and characteristic curves have been evaluated. The Excel evaluations can be seen in Figure 63, 64 and 65.

In Figure 63 the resistivity values for R_{25} and R_{100} in Ω of 1x2, 1x3, 2x2 and 3x3 mm^2 non-standard chip are plotted against the different sintering trails. As can be seen in Figure 63 there is no significant difference of R_{25} and R_{100} for 1x2 as well for 1x3, 2x2 and 3x3 mm^2 non-standard chip between the variable sintering trails.

In Figure 64 the B-values in K for 1x2, 1x3, 2x2 and 3x3 non-standard chip are plotted against the different sintering trails. As can be seen in Figure 64 there is no significant difference of B-value for 1x2 as well for 1x3, 2x2 and 3x3 non-standard chip between the variable sintering trails.

In Figure 65 the percentage deviation for non-standard chips from the standard performance curve is plotted over the temperature in °C. The sizes of the chips are: 1x2, 1x3, 2x2 and 3x3 mm^2. As shown in Figure 65, the deviations from all those chips lie out of the tolerance range except for the values at 25 °C, 0 °C and –25 °C. Between the chip sizes, 1x2, 1x3, 2x2 and 3x3 mm^2 a difference in the deviations can be detected. But there is no significant difference between the diverse sintering trails.

Summarizing, it can be said that in the Figures 63 and 65 the changes for T_{max} and dwell time have no significant effect on R_{25} and R_{100}. Figure 64 shows small changes in B-value. There are also no significant changes in the deviations from the nominal characteristic curves due to the changes of sinter parameters. More detailed analysis of the *Sinter DoE* is carried out with Minitab.

Table 3: Central Composite Designed DoE

DoE Nr.	Maximum Temperature [°C]	Dwell time [min]	Size [mm]
1	1195	120	1x2
2	1195	120	1x3
3	1195	120	2x2
4	1195	120	3x3
5	1240	360	1x2
6	1240	360	1x3
7	1240	360	2x2
8	1240	360	3x3
9	1140	30	1x2
10	1140	30	1x3
11	1140	30	2x2
12	1140	30	3x3
13	1140	360	1x2
14	1140	360	1x3
15	1140	360	2x2
16	1140	360	3x3
17	1240	30	1x2
18	1240	30	1x3
19	1240	30	2x2
20	1240	30	3x3
21*	1240	120	1x2
22*	1240	120	1x3
23*	1240	120	2x2
24*	1240	120	3x3
25*	1140	120	1x2
26*	1140	120	1x3
27*	1140	120	2x2
28*	1140	120	3x3
29*	1195	360	1x2
30*	1195	360	1x3
31*	1195	360	2x2
32*	1195	360	3x3
33*	1195	30	1x2
34*	1195	30	1x3
35*	1195	30	2x2
36*	1195	30	3x3

*This sintering process was not performed

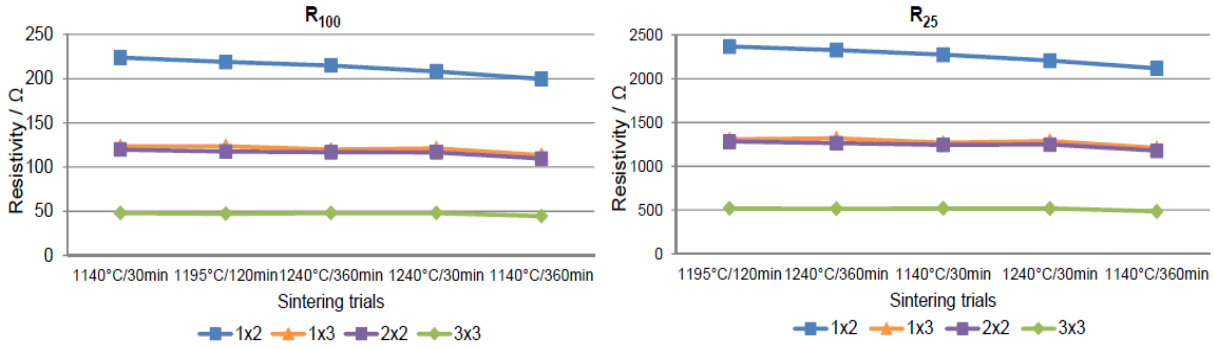

Figure 63: Evaluation R_{25} and R_{100} Sinter DoE

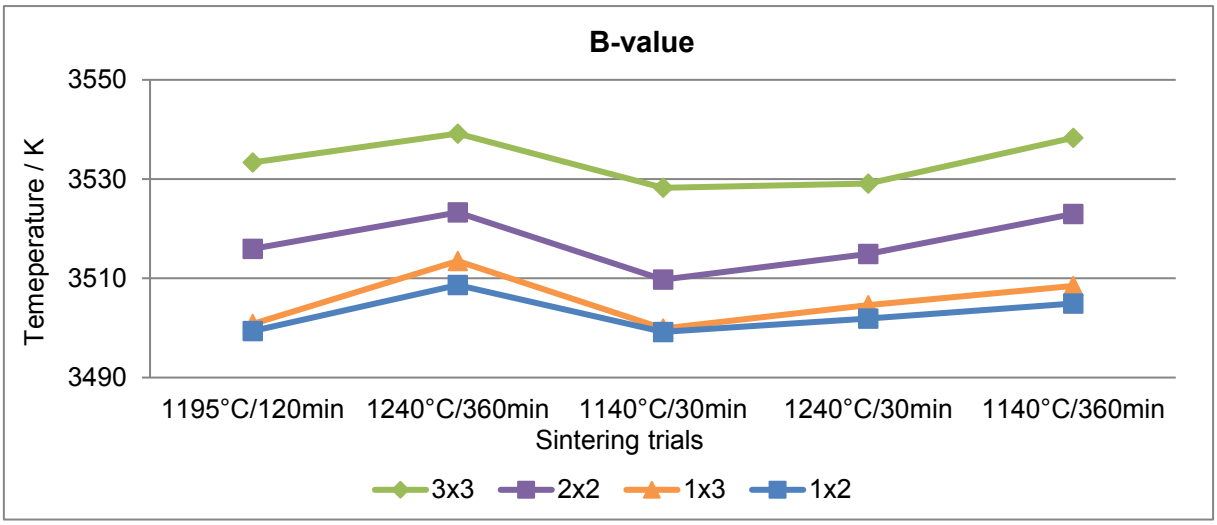

Figure 64: Evaluation B-value Sinter DoE

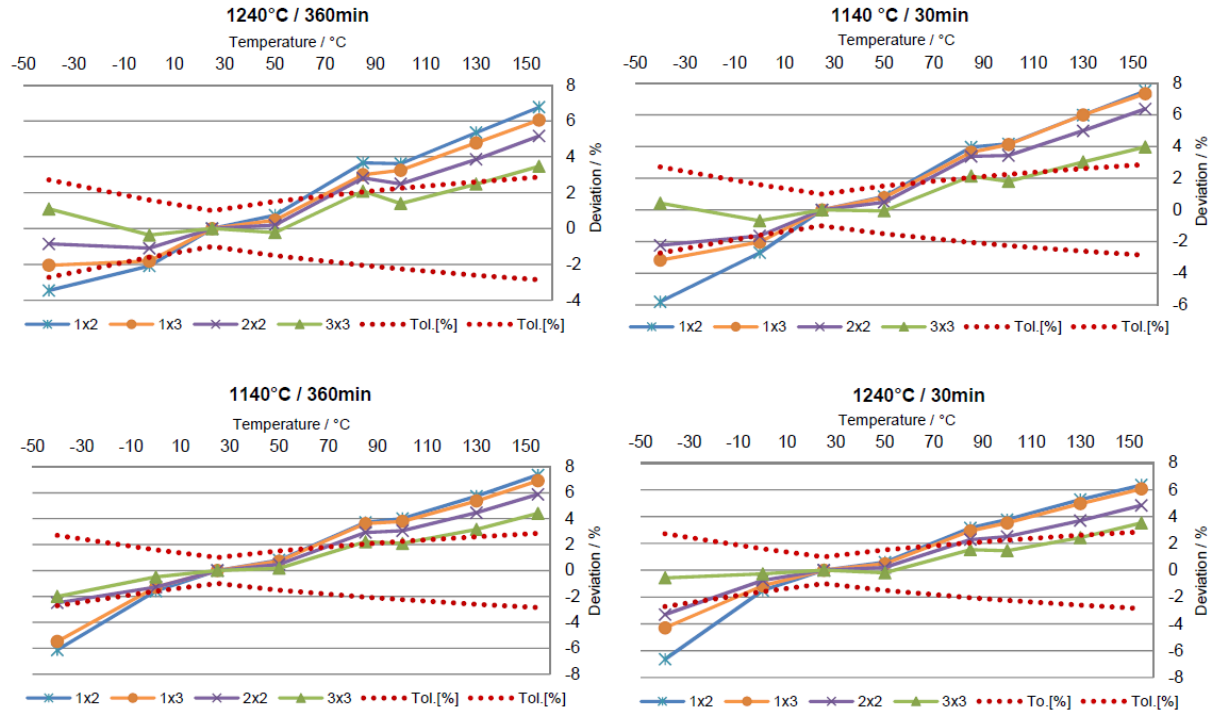

Figure 65: Evaluation characteristic curves Sinter DoE (cooling rate 0,74 K/min)

4.5.1 Sinter DoE for 3x3 2x2, 1x3 and 1x2 non-standard chip

The estimated coefficients and effects for the 3x3 geometry are shown in table 4, 5 and 6. The p-value of the regression for T_{max}, dwell time and T_{max} * dwell time is above 0,05 for the R_{25} and R_{100}, thus T_{max}, dwell time and T_{max} * dwell time have no significant influence. The p-value of the regression for the constant is below 0,05 and therefore is has a significant influence on the constant. The value R-Sq for R_{25} and R_{100} is 90,9 %, this indicates that the regression is good (see table 4 and 5).

The p-value of the regression for T_{max} and T_{max} * dwell time is above 0,05 for the B-value and based on that it has no significant influence on T_{max} and T_{max} * dwell time. The p-value for the constant and the dwell time is below 0,05 and therefore is has a significant influence on the constant. The value R-Sq for B-value is 99,9 %, this means that the regression is very good (see table 6).

The evaluation with Minitab demonstrates that the B-value depends on dwell time. The contour plots for the dependence of B-value and dwell time can be seen in Figure 66. The formula 12 shows the calculation for the B-value. For a desired B-value of 3560 K the dwell time has to be set to 1100 min.

$$B - value_{3x3} = 0{,}03 * dwell\ time + 352767 \quad (12)$$

Table 4: Estimate Coefficients and Effects for non-standard chips 3x3 mm² R_{25}

	Coef	**T**	**p**
Constant	526,814	125,62	0,005
T_{max}	-0,033885	1,60	0,356
Dwell time	-1,15265	-2,17	0,275
T_{max} * Dwell time	0,000918449	1,67	0,344

Table 5: Estimate Coefficients and Effects for non-standard chips 3x3 mm² R_{100}

	Coef	**T**	**p**
Constant	50,2619	119,24	0,005
T_{max}	-0,0015952	1,57	0,360
Dwell time	-0,100924	-2,33	0,259
T_{max} * Dwell time	$7{,}95737*10^{-5}$	1,48	0,377

Table 6: Estimate Coefficients and Effects for non-standard chips 3x3 mm^2 B-value

	Coef	T	p
Constant	3517,66	26270,59	0,000
T_{max}	0,00841488	2,81	0,217
Dwell time	0,0302723	33,55	0,019
T_{max} * Dwell time	$2,56496*10^{-7}$	0,01	0,991

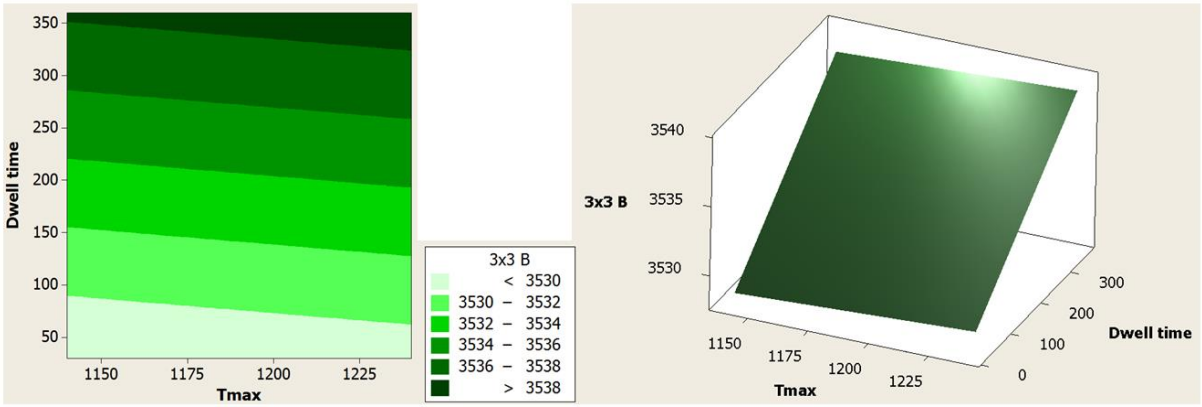

Figure 66: Contour plot (left side) and surface plot (right side) for B-value of 3x3 mm^2 non-standard chips

The p-values of the regression for the non-standard chip 2x2, 1x3 and 1x2 are all above 0,05 and therefore T_{max}, dwell time and T_{max} * dwell time have no significant influence on the sintering process. This means that, the changes of dwell time and T_{max} have no influence on electrical properties (see table 7 – 15). That is the reason why the asterisked sintering processes were not performed, see table 3.

Table 7: Estimate Coefficients and Effects for R_{25} non-standard chips 2x2 mm^2

	Coef	T	p
Constant	1305,21	64,60	0,010
T_{max}	-0,039993	1,04	0,486
Dwell time	-3,06068	-0,57	0,669
T_{max} * Dwell time	0,00250937	0,96	0,512

Table 8: Estimate Coefficients and Effects for R_{100} non-standard chips 2x2 mm^2

	Coef	T	p
Constant	127,580	62,67	0,010
T_{max}	-0,0081127	0,96	0,514
Dwell time	-0,301015	-0,76	0,588
T_{max} * Dwell time	0,000244976	0,98	0,508

Table 9: Estimate Coefficients and Effects for 2x2 mm^2 B-value

	Coef	T	p
Constant	3444,30	4911,85	0,000
T_{max}	0,0560383	1,71	0,337
Dwell time	0,207610	6,74	0,094
T_{max} * Dwell time	$-1{,}4699*10^{-4}$	-1,51	0,371

Table 10: Estimate Coefficients and Effects for 1x3 mm^2 R_{25}

	Coef	T	p
Constant	1149,67	87,41	0,007
T_{max}	0,115255	1,99	0,296
Dwell time	-3,31635	-0,44	0,743
T_{max} * Dwell time	0,00274995	1,39	0,398

Table 11: Estimate Coefficients and Effects for R_{100} non-standard chips 1x3 mm^2

	Coef	T	p
Constant	113,200	77,21	0,008
T_{max}	0,0070023	1,66	0,346
Dwell time	-0,315466	-0,58	0,665
T_{max} * Dwell time	0,000259939	1,23	0,434

Table 12: Estimate Coefficients and Effects for B-value non-standard chips 1x3 mm^2

	Coef	T	p
Constant	3444,33	1508,81	0,000
T_{max}	0,0470312	0,94	0,521
Dwell time	0,016205	1,68	0,342
T_{max} * Dwell time	$8{,}598*10^{-5}$	0,03	0,983

Table 13: Estimate Coefficients and Effects for R_{25} non-standard chips 1x2 mm^2

	Coef	T	p
Constant	3366,16	41,49	0,015
T_{max}	-0,92252	0,58	0,666
Dwell time	-9,97337	-0,14	0,913
T_{max} * Dwell time	0,00833849	1,13	0,461

Table 14: Estimate Coefficients and Effects for R_{100} non-standard chips 1x2 mm^2

	Coef	T	p
Constant	321,966	39,72	0,016
T_{max}	-0,090365	0,53	0,692
Dwell time	-0,942928	-0,20	0,875
T_{max} * Dwell time	0,000786309	1,08	0,475

Table 15: Estimate Coefficients and Effects for B-value non-standard chips 1x2 mm^2

	Coef	T	p
Constant	3468,04	2025,92	0,000
T_{max}	0,0261283	0,83	0,560
Dwell time	-0,016748	1,61	0,353
T_{max} * Dwell time	$2{,}9947*10^{-4}$	0,13	0,919

4.6 Influence of the Cooling rate

In the following chapter, properties of sintered NTC ceramics like electric properties microstructure and Ni precipitations are discussed. The factors *Maximum Temperature* and *Dwell time* show no significant connection to the results and therefore they are not investigated in the following chapter (see section 4.4.1). The variables in this series of experiments are different sizes of non-standard chips: 1x2, 1x3, 2x2 and 3x3 mm^2 and the investigation of the influence of different cooling rates: 0,74, 2,00, 3,05, 5,37, and 10 K/min on the electrical behavior.

4.6.1 Electrical Properties

This section gives an overview of all investigated samples in regards to B-value, R_{25}, R_{100} and characteristic curve. The differences between those NTC chips are the sample size and the cooling rate during the sintering process.

In Figure 67 the B-values in K for 1x2, 1x3, 2x2 and 3x3 mm^2 non-standard chip are plotted against the different cooling rates during the sintering process. As can be seen in Figure 67 there is a significant difference of B-value from 1x2 as well as 1x3, 2x2 and 3x3 mm^2 non-standard chips between the variable cooling rates during the sintering process. Based on this it can be derived that the faster the cooling rate is, the higher the B-value. Additionally it can be said that the bigger the sample geometry is, the higher the B-value. The largest NTC chips sintered with fastest cooling rate have the highest B-value. The smallest chips with the slowest cooling rate have the lowest B-value. Summarized the cooling rate has a major influence on the B-value.

In Figure 68 the resistance R_{25} in Ω from 1x2, 1x3, 2x2 and 3x3 mm^2 non-standard chip are plotted against the different cooling rates during the sintering trails. As can be seen in Figure 68 there is a significant difference of R_{25} from 1x2 as well as 1x3, 2x2 and 3x3 mm^2 non-standard chips between the variable cooling rates during sintering trails.

In Figure 69 the resistance R_{100} in Ω from 1x2, 1x3, 2x2 and 3x3 mm^2 non-standard chips are plotted against the different cooling rates during the sintering trails. Here also a significant difference of R_{100} from 1x2 as well as 1x3, 2x2 and 3x3 mm^2 non-standard chips between the variable cooling rates during sintering trails is visible.

To sum up the smaller the chips the larger the influence of cooling rate, shown by the evaluation of R_{25} and R_{100} in Figure 68 and 69. The smallest non-standard chip 1x2 mm^2, shows the maximum variation in resistance (R_{25}, R_{100}) of all measured samples. Thus the

faster the cooling rate, the higher the resistance values. The largest non-standard chip 3x3 mm^2 shows the lowest resistance values with the slowest cooling rate.

In Figure 70 the boxplot of B-values of all investigated samples can be seen. The connection lines connect the mean values between the different cooling rates. It is evident that there is a significant difference in B-value between the different cooling rates. Also the chip sizes have an influence on the B-values.

In Figure 71 the percentage deviation for non-standard chips from the characeristic curve is plotted over the temperature in °C. The sizes of the chips are: 1x2, 1x3, 2x2 and 3x3 mm^2 and the different cooling rates are: 10, 5,37, 3,05 and 2 K/min. As shown in Figure 71, the deviations from the tolerance range of those chips depend on the cooling rate and on the chip sizes. A rotation of the curve around the standardized R_{25} value can be observed. At a cooling rate of 2 K/min all curves are within the tolerance band. This finding again supports the hypothesis that the reversal of the decomposition reaction of the spinel phase is the root cause for the changes in the electrical properties.

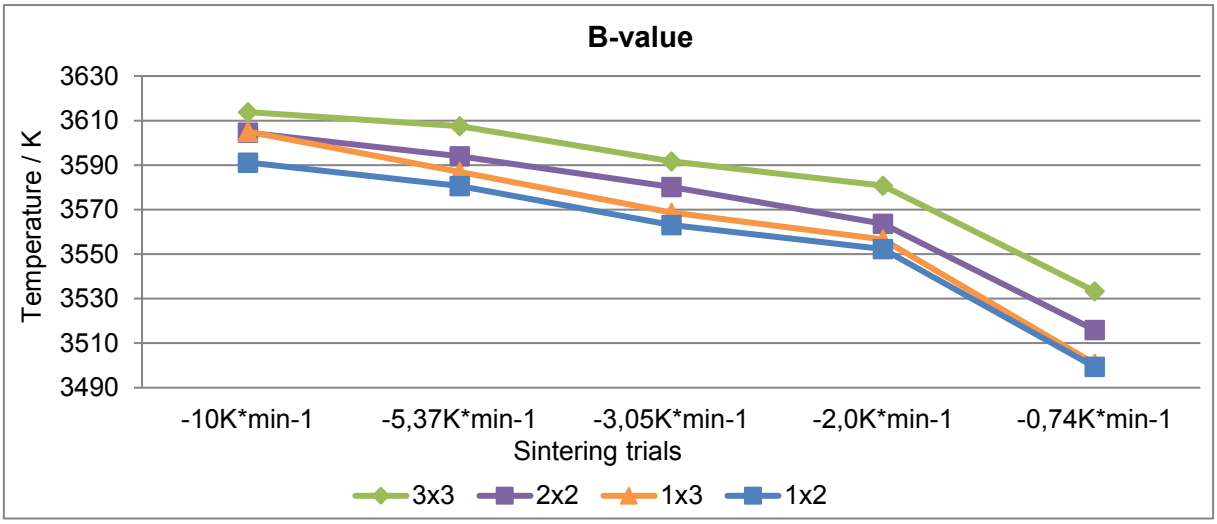

Figure 67: Evaluation of B-value with different cooling rates

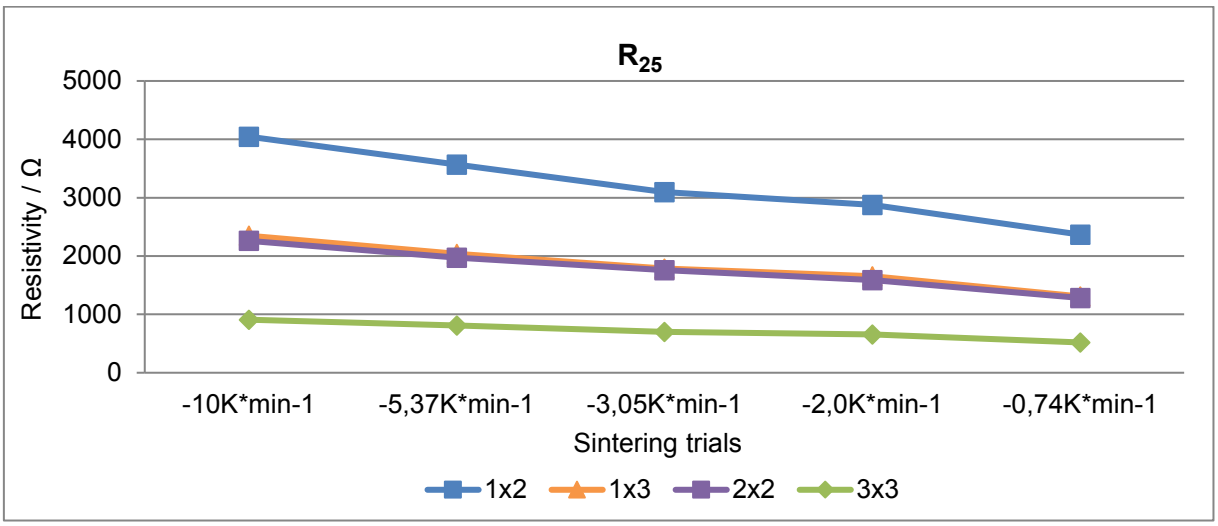

Figure 68: Evaluation of R_{25} with different cooling rates

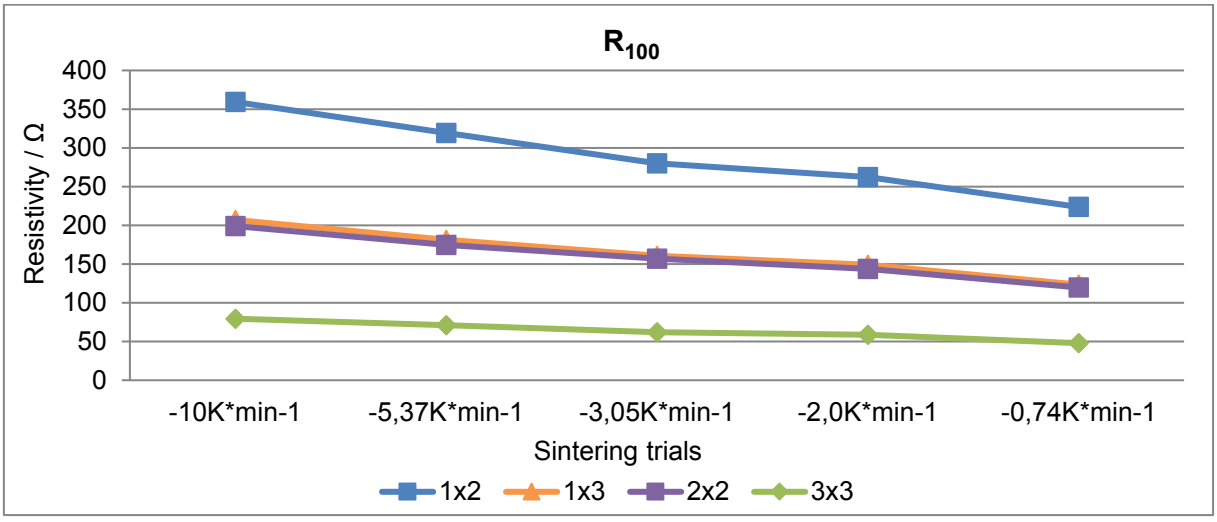

Figure 69: Evaluation of R_{100} with different cooling rates

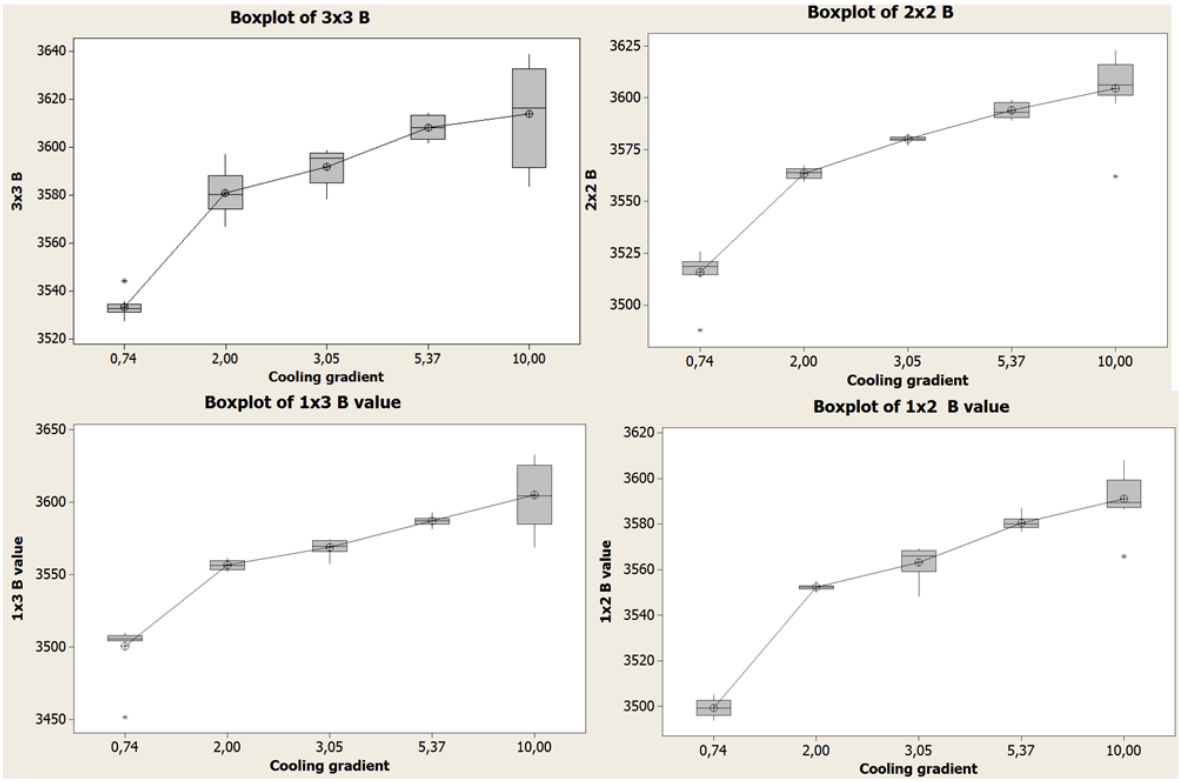

Figure 70: Influence of cooling rate on different non-standard chips: 1x2, 1x3, 2x2 and 3x3 mm^2

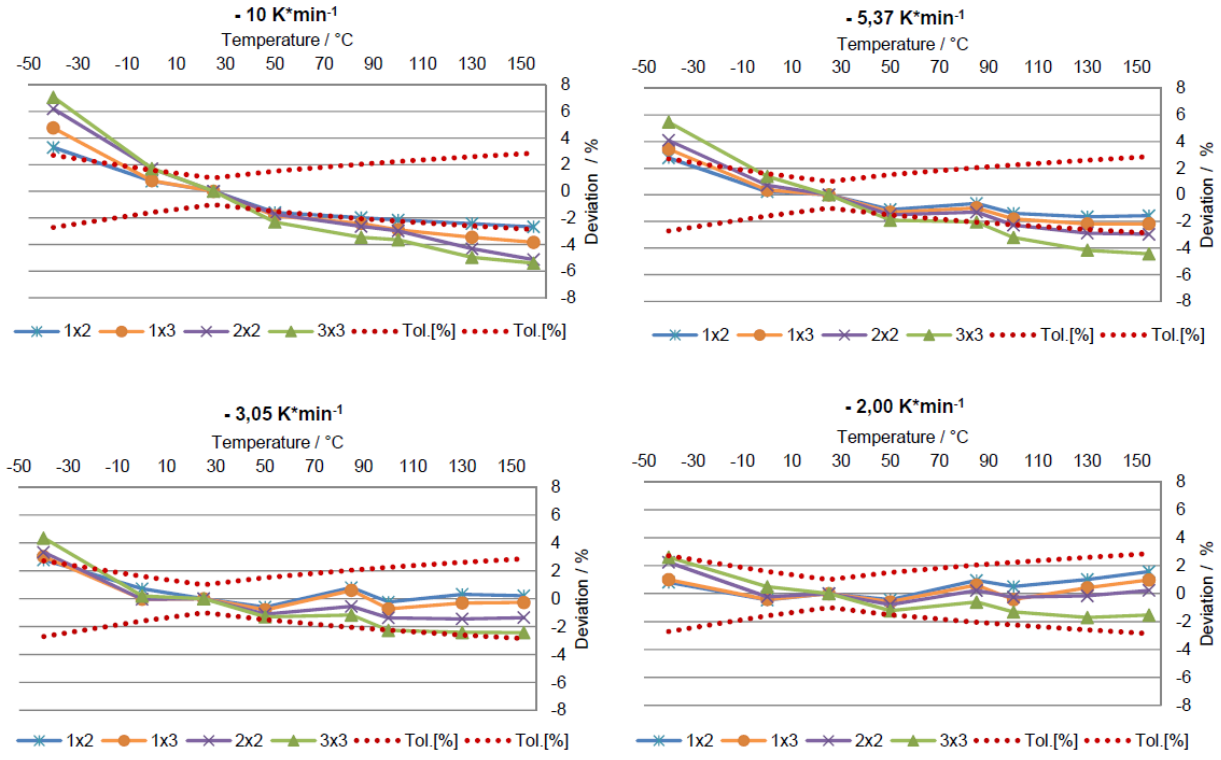

Figure 71: Characteristic curves of different cooling rates: 10, 5,37, 3,05 and 2 K/min

4.6.2 NiO Precipitation Distribution

The following section takes a closer look at the amount and distribution of NiO precipitiations of the samples processed at different cooling rates.

Figure 72 represents SEM pictures in BSE mode for 1x2 mm^2 non-standard chips from the edge of the sample to the middle along the length processed with four different cooling rates: 10, 5, 3, 2 K/min^{-1}. These pictures are used to determine the fraction of NiO precipitations in ceramics. In Figure 73 the analysis of precipitation distribution in % is plotted over 16 subdivided regions along the length of the chips, of five different cooling rates: 10, 5, 3, 2, 0,74 K/min^{-1}. All chips show an increase of NiO precipitations from the edge of the sample, between 8 and 32 % to the middle of the sample, between 32 to 36 %.

Figure 74 represents SEM pictures in BSE mode from 1x2 mm^2 non-standard chips from the edge of the sample to the middle, along the width of four different cooling rates: 10, 5, 3, 2 K/min^{-1}. These pictures are used to determine the fraction of NiO precipitations in the ceramics. In Figure 75 the analysis of precipitation distribution in % is plotted over 16 subdivided regions along the width of the chips of five different cooling rates: 10, 5, 3, 2, 0,74 K/min^{-1}. As demonstrated in Figure 75, again there is a significant difference between the five different cooling rates. All chips show an increase of precipitations from the edge of the sample, between 8 and 28 % to the middle of the sample, between 20 to 28 %. So the precipitations increase along the width of the sample from the edge until the middle of the chips.

When comparing the Figure 73 and 75 one can see, that the fraction of NiO precipitations in ceramics are larger along the length than along the width. The samples with the lowest cooling range (0,74 K/min) show the lowest NiO precipitations. The precipitations rise from 8 % at the edge of the sample up to 24 % at about the middle of the sample. With increasing cooling range the precipitations are continuously rising. The sample with the highest cooling rate shows the highest NiO precipitations. This sample has a distribution of precipitation from 13 % up to 36 %. In all cases the profile of the fraction of NiO precipitations is similar to a diffusion profile. Also the flattening of the profiles (fast cooling corresponds to high amount of NiO precipitations, slow cooling corresponds to low amount of NiO precipitations) fits to a diffusion process indicating the role of oxygen diffusion after sintering. The effect of the process variation of cooling rate on the electrical properties and the results of the distribution of NiO precipitations again indicate that the reversal of the decomposition reaction during cooling of ceramics is responsible for the difference between the electrical characteristics of chips cut from larger wafers and small discs. Furthermore it could be shown that adjusting

the cooling rate is an effective means to yield identical electrical characteristics for both components.

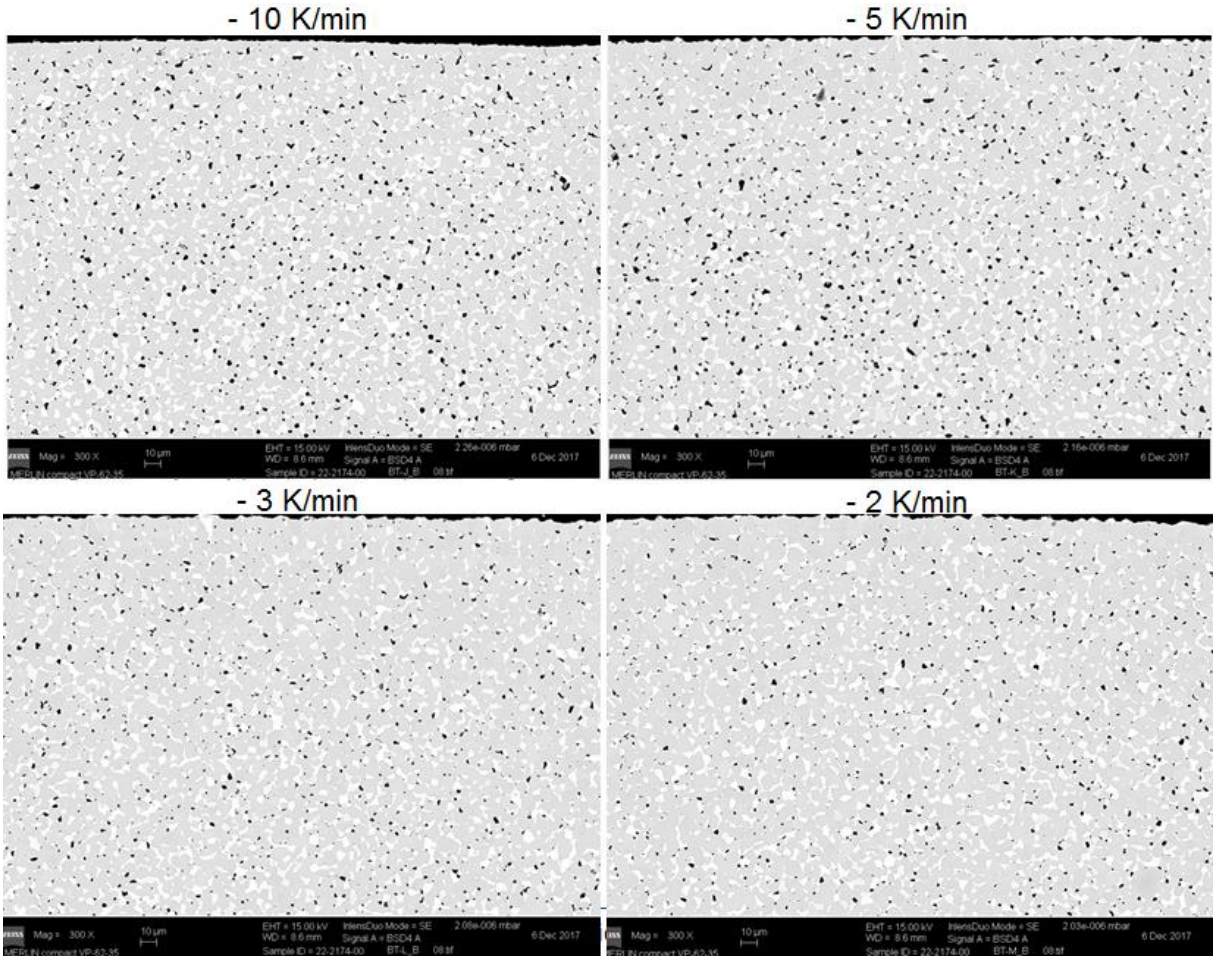

Figure 72: SEM pictures in BSE mode for the length of four different cooling rates

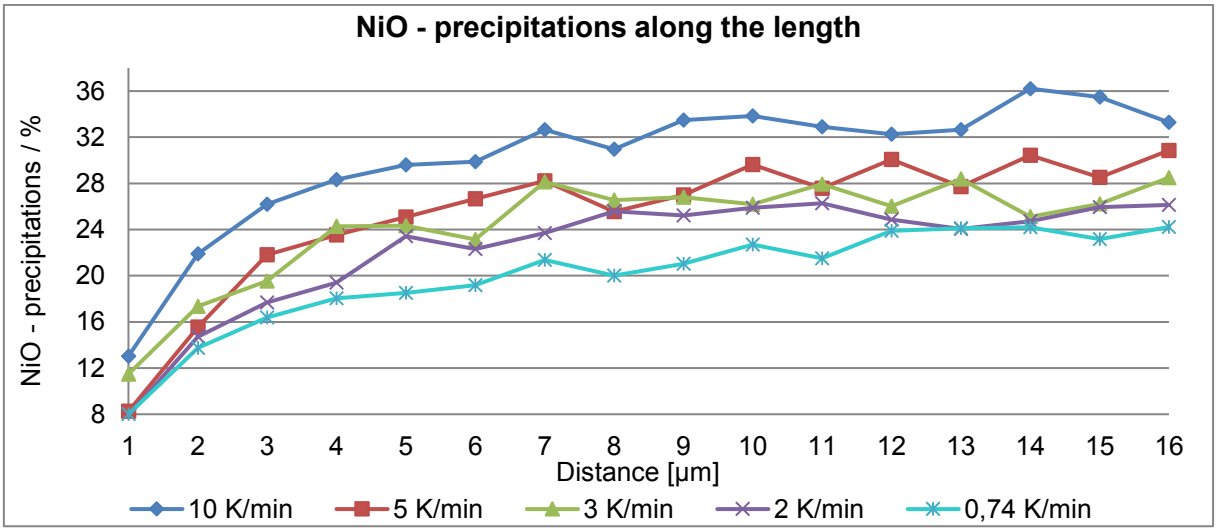

Figure 73: Precipitation distribution of NiO along the length

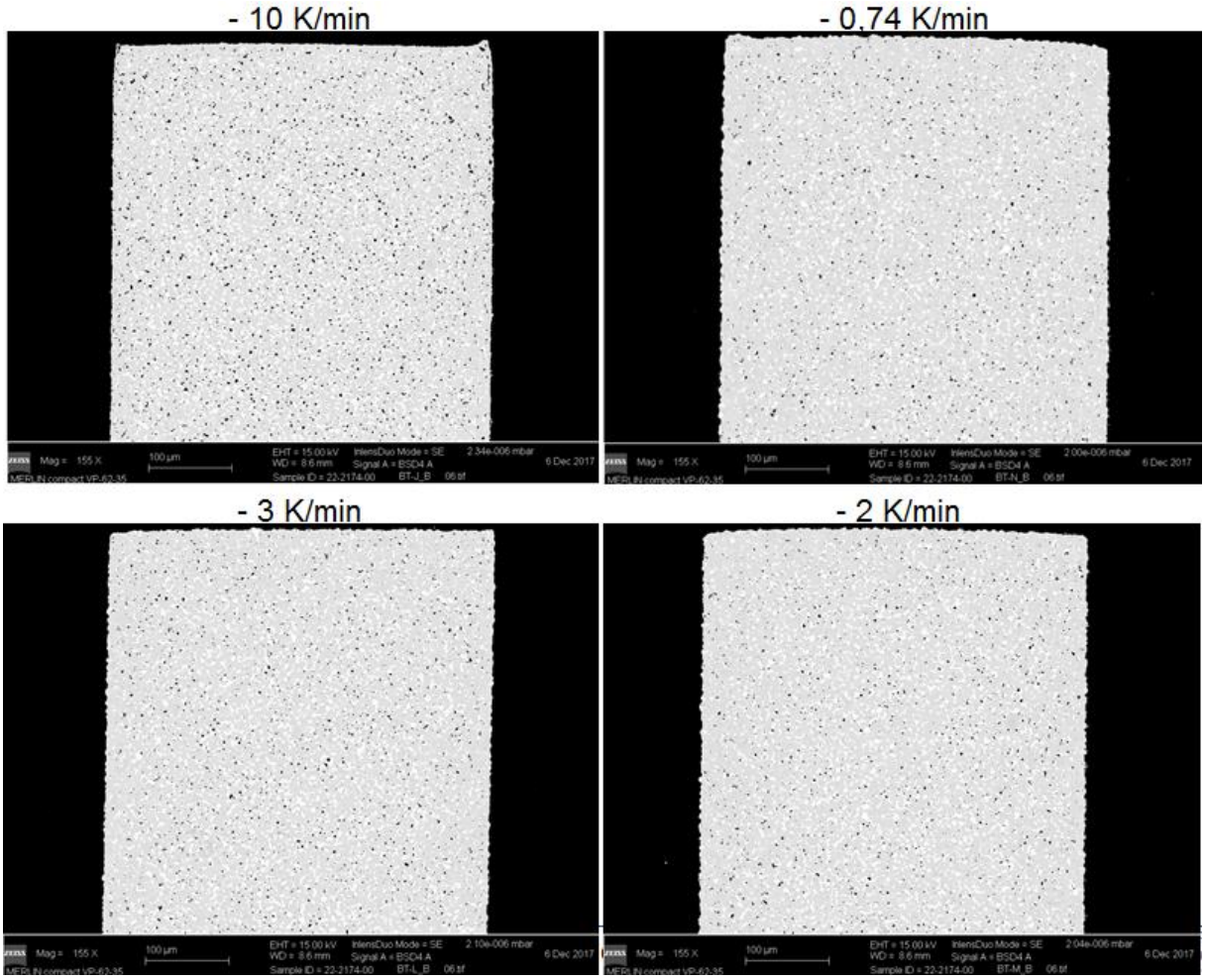

Figure 74: SEM pictures in BSE mode for the width of four different cooling rates

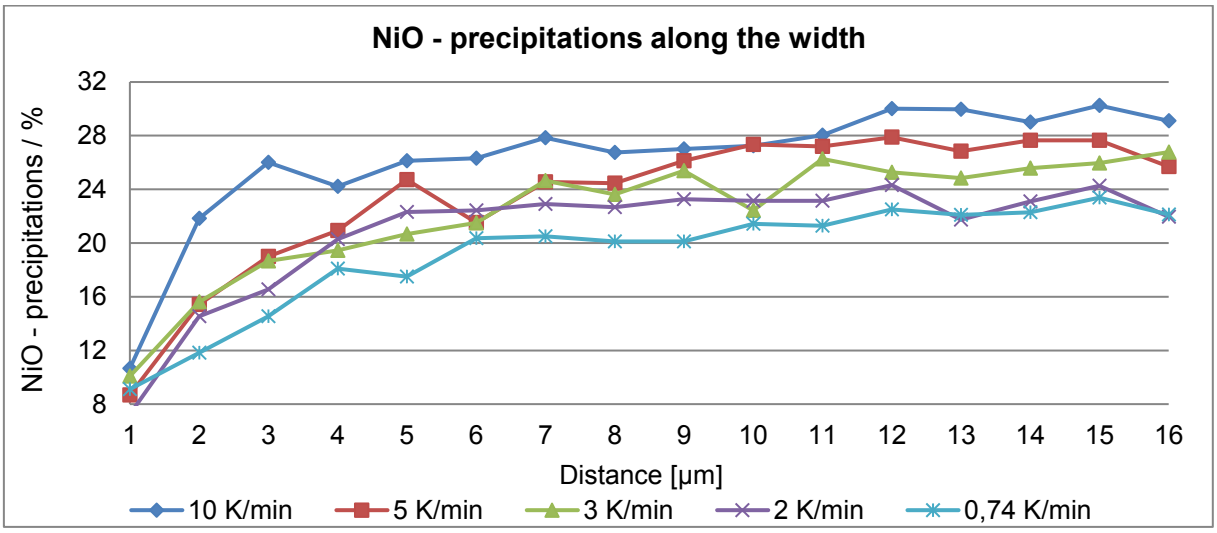

Figure 75: Precipitation distribution of NiO along the width

5 Summary

The goal of current diploma thesis was to investigate the relation between the component sizes and the electrical properties of NTC chips and its influencing factors in order to clarify observed differences in the characteristic curves between chip thermistors and disc thermistors. If one compares the characteristic curve between chips of 1x2 mm^2 size and discs of 2,8 mm diameter of the same material composition and same processing conditions it can be seen that at -40°C the resistance deviations of the 1x2 mm^2 standard chips are larger than that of the discs even exceeding the tolerance range. The electrical properties have been investigated for eleven different sizes of NTC chips from the same material assembly.

In this thesis a distinction is made between two different types of NTC chips which are labelled as standard chips and non-standard chips. The standard chips with the sizes 1x2 mm^2, 2x2 mm^2 and 3x3 mm^2 are cut out from sintered and metallized wafers with the size 32x32 mm^2 and 16x16 mm^2. The non-standard chips with the sizes 1x2 mm^2, 1x3 mm^2, 2x2 mm^2, 3x3 mm^2, 5x5 mm^2, 8x8 mm^2, 10x10 mm^2, 12x12 mm^2 and 40x40 mm^2 are cut to final chip size before debindering and sintering. A more detailed description for the distinction of the specimen and the sample taking can be found in chapter 3.3.

For the investigation of the electrical properties of the standard and non-standard NTC chips the resistance R_T at -40 °C, 0 °C, 25 °C, 50 °C, 100 °C, 130 °C and 150 °C was determined. Subsequently the percentage deviation of the resistance from the nominal characteristic curve was plotted over the temperature and the B-value was calculated from the measurement of R_{25} at 25 °C and R_{100} at 100 °C.

If one compares the characteristic curve between the standard chips 1x2 mm^2, 2x2 mm^2 and 3x3 mm^2 cut out from 32x32 mm^2 and 16x16 mm^2 substrates they can be regarded as equal as can be seen in Figure 47 and 48. In both figures it can be seen that the deviation of the measured standardized values at -40 °C are outside the tolerance range.

However if we compare the characteristic curve between the non-standard chips 1x2 mm^2, 1x3 mm^2, 2x2 mm^2 and 3x3 mm^2 a difference in the deviations between chip sizes from the nominal curve can be noticed (see Figure 50). Further a fundamental difference arises if one compares the characteristic curve from the standard chips, which are cut out form 32x32 mm^2 and 16x16 mm^2 and the non-standard chips with the size 1x2 mm^2, 1x3 mm^2, 2x2 mm^2 and 3x3 mm^2. The non-standard chips with sizes 5x5 mm^2, 8x8 mm^2, 10x10 mm^2, 12x12

mm^2 lie within the area of the tolerance range like the NTC discs which are produced from the same material composition (see Figure 51).

If one compares the B-value between the standard chips 1x2 mm^2, 2x2 mm^2 and 3x3 mm^2 cut out from 32x32 mm^2 and 16x16 mm^2 substrates no significant difference between chips from standard substrates can be seen (see Figure 52). However if we compare the B-value between the non-standard chips 1x2 mm^2, 2x2 mm^2 and 3x3 mm^2 a significant difference can be seen between those chip sizes. The smaller the chip sizes, the lower the B-value (see Figure 53). However this trend is noticeable from a chip size 1x2 mm^2 to 8x8 mm^2. The specimen with the sizes 10x10 mm^2, 12x12 mm^2, 16x16 mm^2 and 32x32 mm^2 show no significant difference between the B-values.

The evaluation of the microstructure revealed that the distribution of nickel oxide precipitations in the ceramics is different between standard chips and non-standard chips. After sintering samples have a so called sintered skin. In the sintered skin a small fraction of NiO precipitations are visible. The amount of NiO precipitations increase from the edge to the center of the sample. The occurrence of this gradient in nickel oxide precipitations can be explained with the phase diagram for the system Ni-Mn-O described in chapter 2.8. The phase diagram shows that sintering samples with the composition of the specimen under investigation above 1000 °C leads to a two phase area representing a decomposition of the spinel phase to NiO under release of oxygen yielding the coexistence of NiO and a spinel phase with a higher manganese content than the starting composition. For dissolving the NiO precipitates in a back reaction during cooling oxygen would be needed. In a state of closed porosity the oxygen can enter the material only by diffusion in bulk and along grain boundaries. That is why only in a thin surface layer, the above mentioned sintered skin, this back reaction takes place.

Precipitations at the surface of a sample are far less than in the middle of a sample, as can be seen in Figure 58. Standard chips with the sizes 1x2 mm^2, 2x2 mm^2 and 3x3 mm^2 which are cut out from sintered and metallized wafers with the size 32x32 mm^2 and 16x16 mm^2 exhibit this sintered skin only on top and bottom surfaces but not on the sides. In contrast non-standard chips additionally exhibit this sintered skin also on the sides. This means that these regions with lower NiO precipitations consist of a spinel phase with different composition (lower manganese content) than the center of the sample. The conductivity as well as the B-value of NTC chips made of nickel manganite depends on the ratio and the distribution of Mn^{3+} and Mn^{4+}, which is mainly a function of composition that is nickel-manganese-ratio. This existence of two regions, side region and center with different chemical composition and hence different electrical resistance and B-value which is equivalent to the situation in disc thermistors is the root cause for the differences in the

characteristic curve observed between standard chips and non-standard chips and consequently between standard chips and discs. Due to the surface to volume ratio this effect is most pronounced at non-standard chips with the size 1x2 mm².

As an outcome after the process analysis according to Six Sigma standards, the percentage deviation of standard chips from the nominal characteristic curve should be influenced by variation of the sintering parameters *Maximum Temperature, Dwell time*, and *Cooling rate* . The final conclusion of different settings during sintering process are that *Maximum Temperature* and *Dwell time* have no significant influence on electrical properties, as can be seen in Figure 63. On the other hand it was possible to improve the electrical properties by changing the *Cooling rate*, as can be seen in Figure 67, 68 and 69.

The samples with the lowest cooling range show the lowest NiO precipitations and with increasing the cooling rate the NiO precipitations are continuously rising, as can be seen in Figure 73. The B-values for the lowest cooling range and the smallest non-standard chip size 1x2 mm^2 lie around 3500 K and for the highest cooling range with the same chips it is around 3590 K as can be seen in Figure 67. As an outcome of the different settings of the cooling range it was possible to change the B-value and the electric resistance value and hence to induce a rotation of the characteristic curve around the standardized R_{25} value. The deviations from the tolerance range of those chips depend on the cooling rate and on the chip sizes. At a cooling rate of 2 K/min the non-standard chips with chip size 1x2 mm^2, 1x3 mm^2, 2x2 mm^2 and 3x3 mm^2 are within the tolerance band. This finding again supports the hypothesis that the reversal of the decomposition reaction of the spinel phase, which occurs during the cooling of the material after sintering, is the root cause for the changes in the electrical properties.

As summary analysis for this thesis can be given that the deviations from the tolerance range of non-standard chips depend on the cooling rate and on the chip sizes. Through modification of the cooling rate a rotation of the curve around the standardized R_{25} value can be expected and the amount of the NiO precipitations changes. The cause for this is the decomposition of the spinel phase during sintering and the reduction of the NiO precipitations in the surface regions in the back reaction during cooling. Non-standard chips with sizes 8x8 mm^2, 10x10 mm^2, 12x12 mm^2 achieve the characteristic curve of discs with the standard sinter parameters

For the future it could be useful to change the sinter conditions and using more or less oxygen during sinter process to change the microstructure and the NiO precipitations of the NTC ceramics.

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