Paul Stampfer, BSc

Characterization and modeling of semiconductor devices at cryogenic temperatures

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Univ.-Prof. Ph.D. Peter Hadley

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AFFIDAVIT

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Finally, Lena, love of my life, thank you for being my partner and best friend. Thank you for your support, patience, and love.

Dankbarkeit ist das Gedächtnis
des Herzens.

Jean-Baptiste Massillon (1663 – 1742)

Abstract

Ion traps are amongst the most promising candidates towards the realization of a fully fault-tolerant many qubit quantum computer. The PIEDMONS project aims at the design, production and experimentation of such ion traps, as well as finding first applications.

Ion traps of the project are most likely operated at cryogenic temperatures. In this thesis the behavior of semiconductor devices at cryogenic conditions is analyzed in order to develop electronic circuitry that operates at cryogenic temperatures. Therefore, devices from a 130 nanometer CMOS technology were characterized and modeled at cryogenic temperatures down to 15 K. Fundamental physical parameters were extracted and the temperature dependence analyzed. Several device parameter allow even for a higher performance at cryogenic temperatures. The following effects could be confirmed at cryogenic temperatures: an increase in the transistor mobility, increase in the transistor threshold voltage, the decrease of the transistor subthreshold slope and it's deviation from the predicted linear behavior for temperatures below about 50 K, a quasi temperature independent capacitance of CMOS capacitor structures, an increase of the resistance of poly-silicon resistors, and an decrease of the resistance of salicided poly-silicon resistors.
Additionally, self heating effects on transistors were quantified, and a negligible temperature rise on single transistors could be confirmed for applied powers below the mW - regime.
Finally, a Python model was developed to compute the current-voltage characteristics of NMOS transistors down to cryogenic temperatures. This physic based model relies on the charge sheet and fully depletion approximation. Good agreement between the developed model and measurements is found.

Contents

1. Introduction

This thesis is part of the PIEDMONS project which is funded by the European Union's Horizon 2020 research and innovation programme. **PIEDMONS** is an acronym standing for: **P**ortable **I**on **E**ntangling **D**evices for **M**obile-**O**riented **N**ext-generation **S**emiconductor-technologies. A central part of the project is the development of miniaturized, thus portable, ion traps, which are among the most promising candidates for the realization of a quantum computer [1]. As stated on the project website [2], "The project aims at designing, implementing, experimenting and finding first applications for the basic building blocks of future quantum computers". However, research includes also other possible applications of ion traps like GPS-free positioning, portable atomic clocks, quantum cryptography and security.

A computer working on the principles of quantum mechanics is superior to it's classical opponent in solving certain mathematical problems. Among the most famous examples for this supremacy, is a quantum computer algorithm for the factorization of integer numbers develop by Shor [3]. As opposed to the bit of a classical computer, the basic logical unit of the quantum computer is the qubit, which is a two-level quantum mechanical system. There are various ways for the realization of such a quantum mechanical system, such as trapped ions [4], electron spin in semiconductors [5] and quantum dots in silicon [6], to name a few. In ion traps, ions are confined using combined electrostatic and radio-frequency electric fields, and the two qubit level correspond to two energetic (electronic or motional) different states of the trapped ion. The manipulation and initialization of the ion's quantum states is done via the interaction with electromagnetic waves (laser or microwave). Currently, the maximum number of ions the can be trapped and controlled is around 50 [7], which is already going towards the direction of a noisy intermediate-scale quantum (NISQ) technology that is able to outperform classical computers in certain tasks [8].

However, there is still a long way to the thousands or millions of qubits needed for a fully fault-tolerant trapped-ion quantum computer capable of executing complex algorithms, as for example factoring a 200 digital number in fault tolerant way would require around 100000 qubits [9].

Current research in the field of quantum computing includes trapping ions in traps fabricated in scalable complementary metal-oxide-semiconductor (CMOS) processes [10] [11]. This allows for a high level of integration.

Ion traps of the PIEDMONS project will be most likely operated at cryogenic temperatures. The purpose of this thesis is to develop models that accurately describe the behavior of semiconductor devices at cryogenic conditions. This allows the integration of semiconductor circuitry into the cryogenic regime, which would have promising advantages [12]. Additionally, electric circuitry and the ion traps could be co-integrated on the same substrate, which would be beneficial for further miniaturization of quantum computers.

Apart from its possible application in the field of quantum computing there are other fields where electronic devices are operated at cryogenic conditions, such as space science and satellite communication [13] or high precision measurements due to improved noise performance. Additionally, at cryogenic temperatures physical phenomena can be studied, that only occur or are magnified at such low temperatures [14].

In general it is known that many parameter for electronics operated at cryogenic temperatures improve, such as the subthreshold swing [15] or mobility [16]. There are many recent publications in the field of cryoelectronics (e.g. [17] [18] [19]) indicating that a lot of research activity in that field is currently going on.

2. Fundamentals and background

In this chapter fundamentals relations of semiconductors and semiconductor devices will be introduced. Most of this relations can be found in standard textbooks on semiconductor physics, like the book by Sze [20] or Tsividis [21]. At first, the relevant temperature dependent properties of bulk silicon are introduced and secondly cryogenic effects altering the characteristics of MOSFETs will be discussed.

2.1. Bulk semiconductors

2.1.1. Temperature-dependence of the bandgap

The band gap E_g is a very important material-specific property of great theoretical and practical interest. E_g of silicon is known to slightly decrease with higher temperatures T. The temperature dependence is governed by two mechanisms [22]:

- temperature dependent lattice dilatation
- temperature dependent electron lattice interaction,

both leading to an increase of the bandgap at lower temperatures [23].

In all computations presented in this thesis an empirical relation by Varshni [22] is used to describe the temperature dependence of the bandgap:

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T + \beta}, \tag{2.1}$$

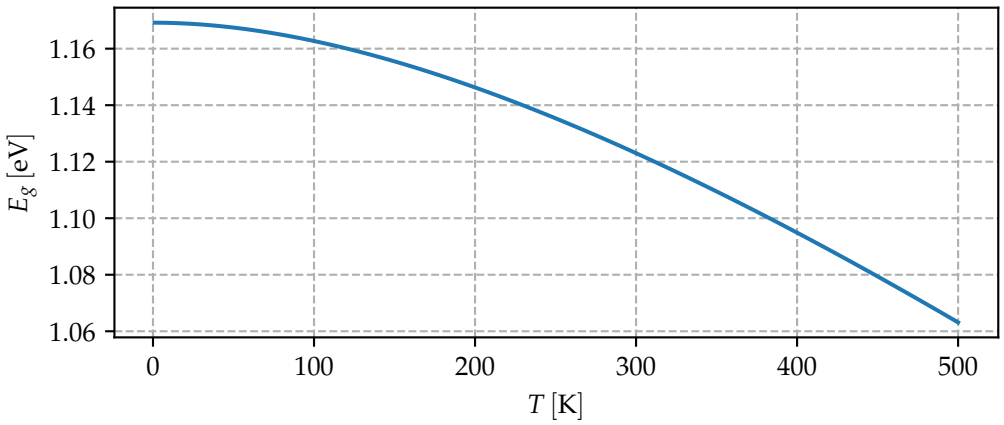


Figure 2.1.: Bandgap energy E_g of Silicon as a function of temperature T, modeled according to eq. 2.1 with the parameters given in 2.2.

where the values for $E_g(0)$, α and β are taken from reference [24]:

$$\begin{aligned} E_g(0) &= 1.1692\,\mathrm{eV} \\ \alpha &= 4.9\,\mathrm{eV\,K^{-1}} \\ \beta &= 655\,\mathrm{K}. \end{aligned} \tag{2.2}$$

2.1.2. Temperature dependence of the effective density of states

As will be introduced in section 2.1.3 the effective densities of states in the conduction and valence band (N_c and N_v) can be used to calculate the charge carrier densities of electrons and holes in a semiconductor. N_c and N_v can be calculated via [20]:

$$N_c = 2\left(\frac{m_n k_\mathrm{B} T}{2\pi\hbar^2}\right)^{3/2}, \tag{2.3}$$

and

$$N_v = 2\left(\frac{m_p k_\mathrm{B} T}{2\pi\hbar^2}\right)^{3/2}. \tag{2.4}$$

In eq. 2.3 and eq. 2.4 m_n, m_p, T, $\hbar$ are the electron density-of-states effective-mass, hole density-of-states effective-mass, temperature and reduced Plancks constant, respectively. m_n and m_p are also temperature dependent primarily due to the following three mechanism [25]:

- change of lattice spacing
- change of the Fermi distribution function in a non-parabolic band
- change of the band curvature due to the interaction between electrons (holes) and lattice vibrations.

In all computations in this thesis the following empirical relations for the temperature dependence of m_n and m_p are used [26]:

$$m_n = -1.084 \times 10^{-9} T^3 + 7.580 \times 10^{-7} T^2 + 2.862 \times 10^{-4} T + 1.057 \quad (2.5)$$

and

$$m_p = 1.872 \times 10^{-11} T^4 - 1.969 \times 10^{-8} T^3 + 5.857 \times 10^{-6} T^2 + 2.712 \times 10^{-4} T + 0.584. \quad (2.6)$$

A plot of the temperature dependence of m_n, m_p, N_c and N_c can seen in fig. 2.2 and fig. 2.3.

2.1.3. Charge carriers in intrinsic and extrinsic semiconductors

For an intrinsic semiconductor with a bandgap energy E_g, at a temperature T, the law of mass action (eq. 2.7, valid for intrinsic and extrinsic semiconductors) can be used to calculate the intrinsic carrier concentration n_i [27]:

$$np = N_c N_v \exp\left(\frac{-E_g}{k_\mathrm{B} T}\right) = n_i^2, \quad (2.7)$$

$$n_i = \sqrt{N_c N_v} \exp\left(\frac{-E_g}{2k_\mathrm{B} T}\right), \quad (2.8)$$

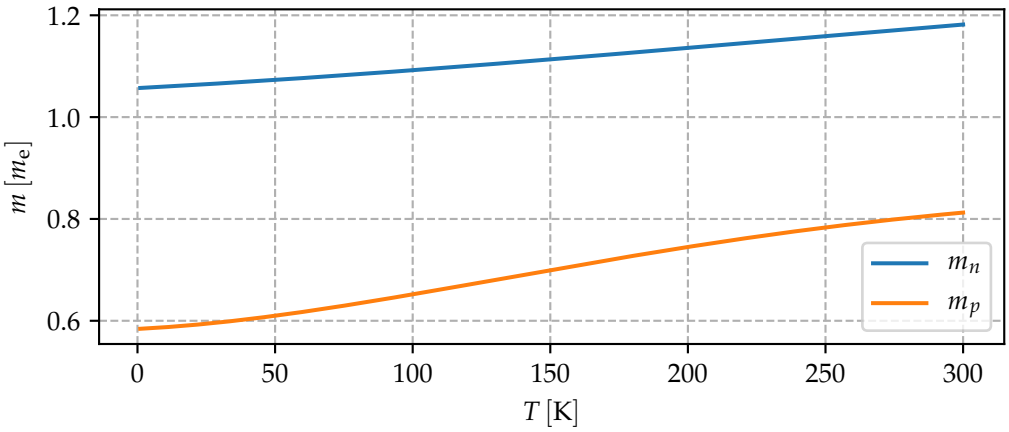


Figure 2.2.: Electron density-of-states effective-mass m_n and hole density-of-states effective-mass m_p as a function of temperature T in units of the electron mass m_e. Temperature dependence is given by eq. 2.5 and eq. 2.6 and is taken from reference [26].

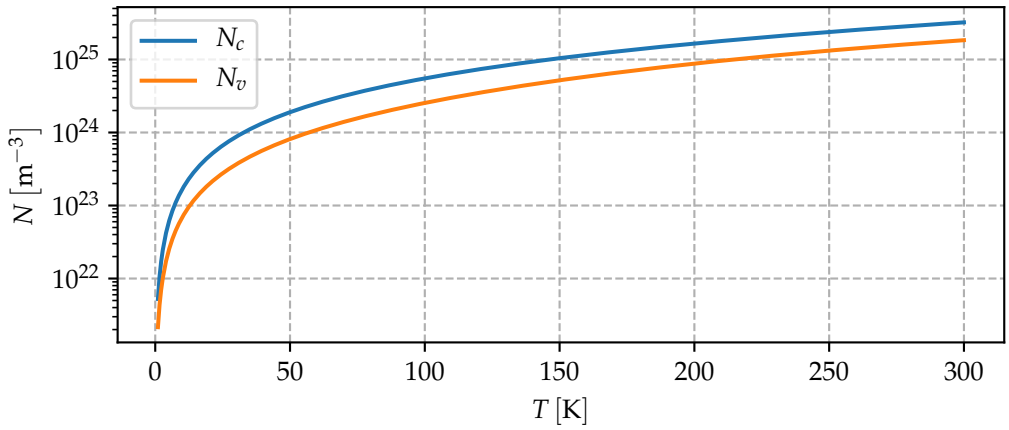


Figure 2.3.: Effective densities of states in the conduction and valence band (N_c and N_v) as a function of temperature T.

where n and p are the electron and hole concentration, N_c (N_v) the effective density of states in the conduction (valence) band and k_B the Boltzmann constant. The temperature dependence of N_c and N_v is presented section

2.1.2. Due to its exponential dependence on temperature n_i covers a high range of values as a function of temperature, i.e. $n_i \approx 1 \times 10^{-130}\,\mathrm{cm}^{-3}$ at $T = 20\,\mathrm{K}$,while $n_i \approx 1 \times 10^{10}\,\mathrm{cm}^{-3}$ at $T = 300\,\mathrm{K}$ [26].

In doped semiconductors the electron and hole concentrations are typically calculated using the Boltzmann approximation [20]:

$$n = N_c \exp\left(\frac{E_c - E_f}{k_\mathrm{B}T}\right) = n_i \exp\left(\frac{E_f - E_i}{k_\mathrm{B}T}\right), \tag{2.9}$$

$$p = N_v \exp\left(\frac{E_f - E_v}{k_\mathrm{B}T}\right) = n_i \exp\left(\frac{E_i - E_f}{k_\mathrm{B}T}\right), \tag{2.10}$$

where E_f, E_c and E_v are the Fermi energy, the conduction band energy and the valence band energy respectively. This approximation, valid for non-degenerate semiconductors, can be verified down to the milli-Kelvin regime [19]. The very right hand side of eq. 2.9 and eq. 2.10 , follows if the intrinsic energy level E_i is introduced as the Fermi energy of the undoped semiconductor (derivation see A.1):

$$E_i = \frac{E_c + E_v}{2} + \frac{k_\mathrm{B}T}{2} \ln\left(\frac{N_v}{N_c}\right). \tag{2.11}$$

If the number of donors is N_D and the number of acceptors is N_A the Fermi energy can be computed via the charge neutrality condition:

$$n + N_A^- = p + N_D^+, \tag{2.12}$$

where the number of ionized dopands (N_A^- , N_D^+) can be calculated with [20]:

$$\begin{aligned} N_A^- &= \frac{N_A}{1 + g_A \exp\left((E_A - E_f)/(k_\mathrm{B}T)\right)} \\ N_D^+ &= \frac{N_D}{1 + g_D \exp\left((E_f - E_D)/(k_\mathrm{B}T)\right)}. \end{aligned} \tag{2.13}$$

In eq. 2.13 E_A (E_D) and g_A (g_D) are the acceptor (donor) energies and the acceptor (donor) site degeneracy factors. For silicon g_A is 4 due to fourfold hole degeneracy (heavy/light valence band and spin up/down) and g_D is 2 (spin up/down) [28]. The effect of incomplete ionization (eq. 2.13) is often neglected at room temperature, via assuming $N_A^- \approx N_A$ and $N_D^+ \approx N_D$. However, at

cryogenic temperatures incomplete ionization needs to be considered, as E_f even drops below (above) E_A (E_D) for an n(p)-doped semiconductor, see fig. 2.4.

2.1.4. Fermi energy as a function of temperature

The Fermi energy is determined via the implicit equation 2.12.

In fig. 2.5 it is shown graphically how the Fermi energy is determined at three different temperatures. In these plots one can recognize that incomplete ionization does not need to be considered at room temperature, but at lower temperatures this effect significantly effects the solution of the Fermi energy. The Fermi energy as a function of temperature and different doping concentrations can be seen in fig. 2.4.

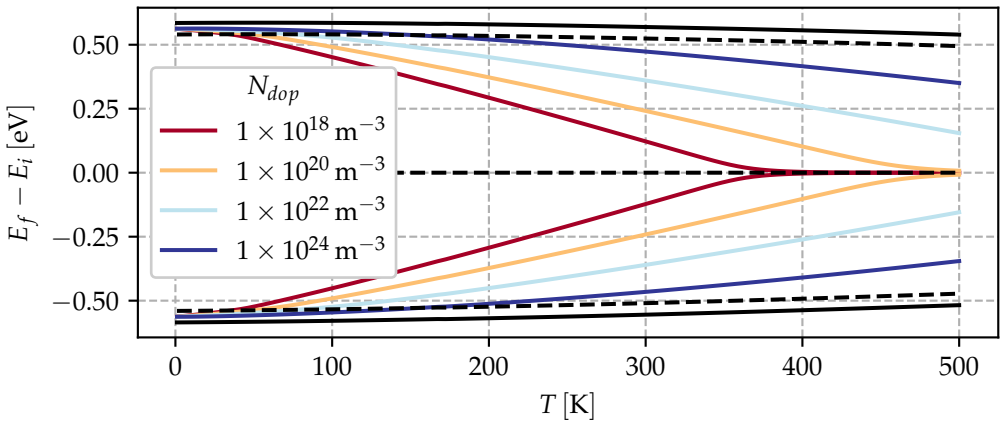
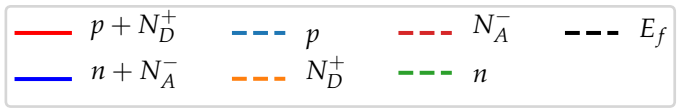
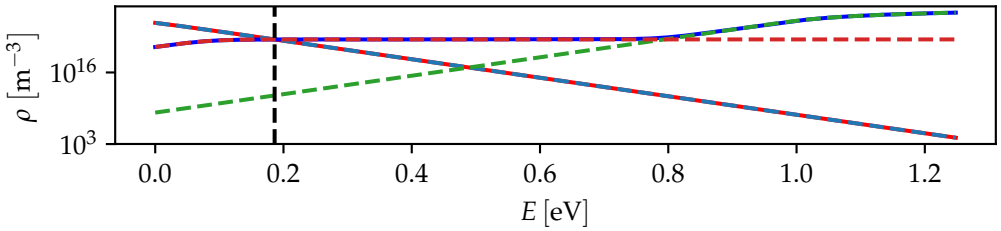


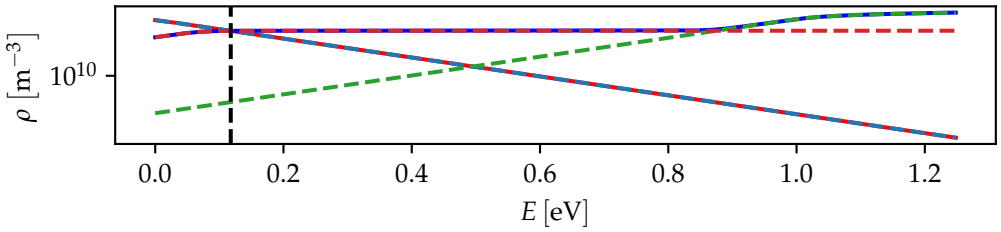
Figure 2.4.: Fermi energy E_f as a function of temperature T and doping concentration N_{dop}. For each value of N_{dop} eq. 2.12 is solved twice: one time for $N_A = N_{dop}$ and $N_D = 0$, the other time for $N_A = 0$ and $N_D = N_{dop}$. The top/bottom solid black lines are E_c/E_v and the top/bottom black dashed lines are E_D/E_A.



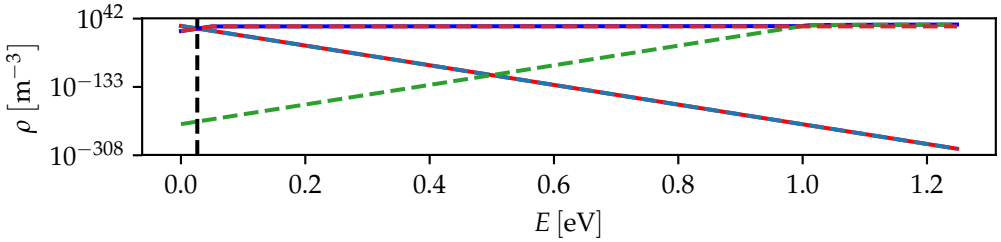
(a) Legend



(b) 300 Kelvin



(c) 100 Kelvin



(d) 20 Kelvin

Figure 2.5.: Graphical calculation of the Fermi energy E_f for a silicon bulk semiconductor with $N_A = 1 \times 10^{16}\,\mathrm{cm}^{-3}$ and $N_D = 0$ at three different temperatures. Charge carrier densities ρ are calculated using Fermi-Dirac integrals and are plotted as a function of the Fermi energy

2.2. MOS transistor modeling

Fundamental relations describing the physics in a MOS transistor are presented in this chapter. Many state of the art compact models, such as BSIM [29] or EKV [30], rely on equations presented in this section. Relations in this section refer to a NMOS transistor, however they can be easily converted to describe the physics in a PMOS transistor as well.

2.2.1. General relations

The MOS transistor in inversion can be described by eq. 2.14 together with eq. 2.17 [21]. These two coupled equations are the charge balance equation and the potential balance equation.

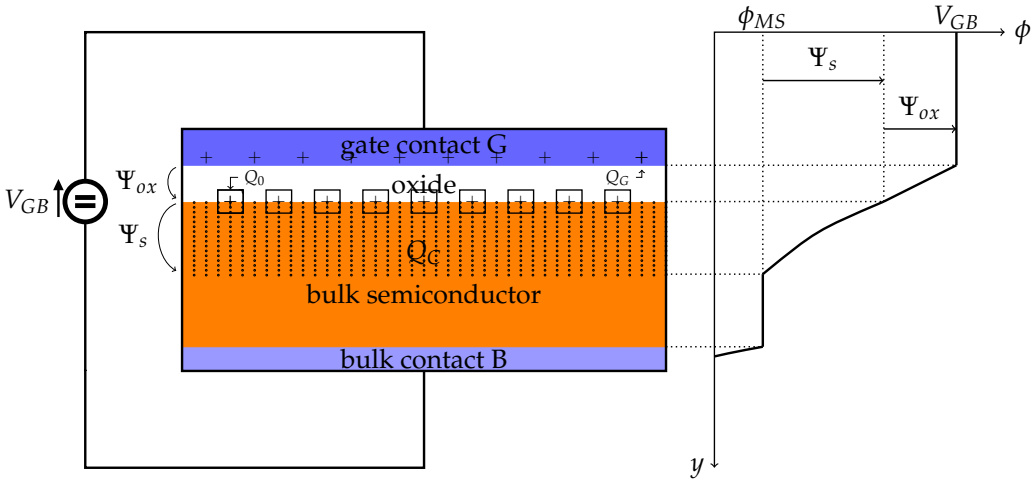


Figure 2.6.: Sketch of a MOS capacitor with a voltage source applied voltage source, redrawn from [21].Q_G,Q_0,Q_C are the charges on the gate, the interface charges and the charges in the semiconductor under the oxide, respectively. The right side shows the potential distribution, where ϕ_{MS}, Ψ_s, Ψ_{ox} and V_{GB} are the semiconductor-metal work function, the surface potential, the potential drop across the oxide and the gate to bulk voltage, respectively.

The simplified structure consists of the bulk semiconductor, an isolating oxide and a metallic gate on top. Additionally a voltage source is connected to the gate and bulk contacts to apply an external gate to bulk bias V_{GB}. The right hand side of fig. 2.6 sketches the potential ϕ as a function of the vertical coordinate y.

Going through a loop all appearing potentials must cancel each other out, thus:

$$V_{GB} = \psi_{\text{ox}} + \psi_s + \phi_{ms}, \tag{2.14}$$

where ψ_{ox}, ψ_s, ϕ_{ms} are the oxide potential, the surface potential and the metal-semiconductor work function, respectively. The surface potential ψ_s is defined as the potential drop from the semiconductor-oxide surface to the bulk region of the semiconductor that is not effected by the voltage applied to the gate and the oxide potential is the potential drop across the oxide. ψ_s can be linked to the intrinsic energy at the surface $E_{i,s}$:

$$\psi_s = \frac{E_{i,b} - E_{i,s}}{e}, \tag{2.15}$$

and in general the potential $\Psi(y)$ is linked to the intrinsic energy at the vertical distance y from the interface via:

$$\Psi(y) = \frac{E_{i,b} - E_i(y)}{e}. \tag{2.16}$$

It should be noted that a definition according to eq. 2.15 and eq. 2.16 is not always used, in literature definitions of the surface potential with respect to the intrinsic energy E_i can also be found (compare for example definition of ψ_s in reference [20] with its definition in reference [19]).

Additionally, in order to maintain charge neutrality the sum of all appearing charges in equilibrium must be zero:

$$Q_G + Q_0 + Q_C = 0, \tag{2.17}$$

where Q_G, Q_0 and Q_C are the charges on the gate, the interface charges and the charges in the semiconductor under the oxide, respectively. The interface charges are drawn in a rectangles in fig. 2.6.

The potential $\Psi(y)$ allows the computation of charge carrier density along the y-axis (see appendix A.2):

$$\begin{aligned} n(y) &= n_0 \exp\left(\frac{\Psi(y)}{\phi_t}\right) \\ p(y) &= p_0 \exp\left(\frac{-\Psi(y)}{\phi_t}\right) \end{aligned} \tag{2.18}$$

where the Fermi potential ϕ_f is defined as :

$$\phi_f = \frac{E_i - E_f}{q}, \tag{2.19}$$

and the thermal potential ϕ_t is computed with:

$$\phi_t = \frac{k_\mathrm{B} T}{q}. \tag{2.20}$$

The total charge density ρ at position y can be written as

$$\rho(y) = q[n_0 \exp\left(\frac{\Psi(y)}{\phi_t}\right) + p_0 \exp\left(\frac{-\Psi(y)}{\phi_t}\right) + N_A^- + N_D^+], \tag{2.21}$$

Combining eq. 2.18 and 2.21 Poisson equation can be written as:

$$\frac{\partial^2 \Psi(y)}{\partial y^2} = -\frac{\rho(y)}{\epsilon_S} = f(\Psi(y)), \tag{2.22}$$

which allows, for a given ψ_s, N_A, N_D and T the numerical computation of $\Psi(y)$, $n(y)$, $p(y)$ and $\rho(y)$. Solving eq. (2.22) for $|\overrightarrow{E}| := \mathcal{E} = -|\nabla\Psi|$, and considering that $Q_C = -\epsilon_{si}|\overrightarrow{E}_{surface}| = -\epsilon_{si}\mathcal{E}_s$, where ϵ_{si} is the permittivity of silicon and $\mathcal{E}_s$ is the electric field evaluated at the semiconductor - isolator interface an analytic result for Q_C can be received:

$$Q_C = f(\psi_s), \tag{2.23}$$

where the rather lengthy function f as well as a short derivation of this relationship can be found in A.3. The total charge in the semiconductor can be

furthermore split into the mobile inversion charge Q_I and the immobile ionized acceptor charge Q_B

$$Q_C = Q_I + Q_B. \tag{2.24}$$

Especially Q_I is of special interest when deriving formulas for the drain to source current of the device. Very common and accurate approximations to analytically calculate this mobile charge are presented in the next subsection 2.2.3.

2.2.2. Drain to source voltage

When a drain to source voltage V_{DS} is applied and an inversion layer is present, electrons can be transported along the channel. This creates a non-equilibrium situation for the electrons, that can be incorporated in the formalism presented in section 2.2.1, via the introduction of the channel voltage V_{ch} [31] [19]. The channel voltage has a value of V_{DS} right at the drain side of the transistor and drops to V_S at the source side of the transistor and is thus a function of the horizontal position x. V_{ch} shifts the potential Ψ in the calculation of the electron concentration n such that eq. 2.18, needs to be modified [32]:

$$\begin{aligned} n(y,x) &= n_0 \exp\left(\frac{\Psi(y) - V_{ch}(x)}{\phi_t}\right) \\ p(y) &= p_0 \exp\left(\frac{-\Psi(y)}{\phi_t}\right). \end{aligned} \tag{2.25}$$

In eq. 2.25 the computation for n now also depends on the horizontal position x, and thus solving Poisson equation just yields a solution at this particular horizontal position. It should be noted that the computation for $p(y)$ stays the same even in the presence of a drain to source voltage.

2.2.3. Charge sheet and depletion approximation

In order to calculate the mobile charge Q_I, an expression for Q_B is derived, and then Q_I is calculated using eq. (2.24). In the depletion approximation it is assumed that Q_B is uniform till the depth x_p and then decreases sharply

to zero. If additionally it is assumed that Q_I is within a sheet of negligible thickness (charge sheet approximation,originally introduced by Brews [33]), one can show that also the potential drop across this sheet approaches zero [20]. In this case the full potential ψ_s must drop across the depletion length x_p, and an expression for $Q_B(\psi_s)$ can be derived (similar to the abrupt junction approximation for diodes, see A.4):

$$Q_B = -\sqrt{2q\epsilon_S N_A \psi_S}. \tag{2.26}$$

2.2.4. Transistor current

The transistor current is typically described via the two transport mechanism drift and diffusion. These equations can be derived from the Boltzmann transport equation and read [34]:

$$\begin{aligned} \overrightarrow{j_n} &= qn\mu_n \nabla \overrightarrow{E} + qD_n \nabla n \\ \overrightarrow{j_p} &= qp\mu_p \nabla \overrightarrow{E} - qD_p \nabla p, \end{aligned} \tag{2.27}$$

where $\overrightarrow{j_n}$ ($\overrightarrow{j_p}$), μ_n (μ_p), D_n (D_p) are the electron (hole) current density, mobility and diffusion constant, respectively.

Within the charge sheet approximation and just considering inversion charges to contribute to the current, eq. 2.27 can be written as [21]:

$$I_{DS} = -\frac{\mu}{L} Q_I \frac{d\psi_S}{dx} + \frac{\mu}{L} \phi_t \frac{dQ_I}{dx}. \tag{2.28}$$

2.3. Cryogenic transistor effects

2.3.1. Incomplete ionization

Incomplete ionization of dopant atoms in a bulk semiconductor can be described with eq. 2.13. This formula can also be used to describe incomplete ionization in a MOSFET within the charge sheet approximation by replacing the Fermi

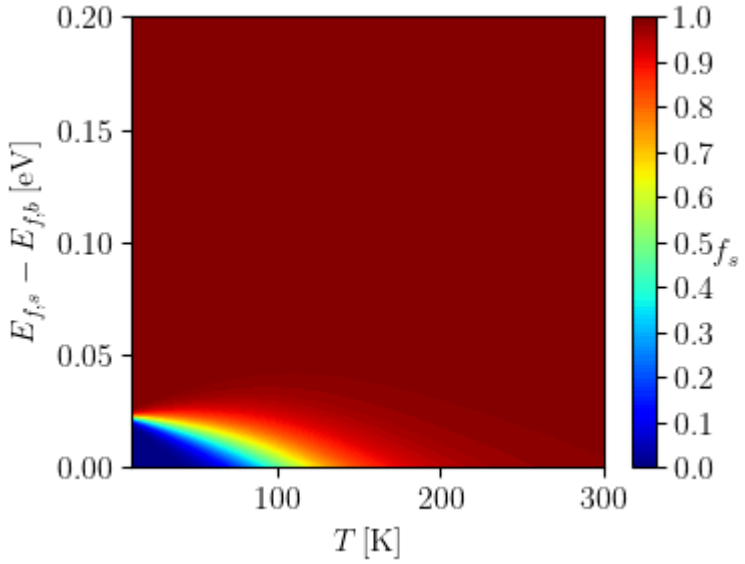


Figure 2.7.: Incomplete ionization: ionization factor f_s as a function temperature T and Fermi energy. $E_{f,b}$ denotes the Fermi energy in the bulk region of the mosfet, $E_{f,s}$ is the Fermi energy at the channel. The plot is made for a bulk doping concentration of $N_A = 1 \times 10^{16}\,\mathrm{cm}^{-3}$.

energy E_f with the (quasi) Fermi energy at the channel interface $E_{f,s}$. It has to be considered, that $E_{f,s}$ is also a function of the applied external voltages. For electrons in an n-MOS (p-type bulk) it can be written as:

$$N_A^- = N_A f_s \tag{2.29}$$

$$f_s = \frac{1}{1 + g_A \exp\left((E_A - E_{f,s})/(k_\mathrm{B}T)\right)}, \tag{2.30}$$

where f_s is the ionization factor.

Incomplete ionization is therefore governed by two external factors: the external biases ("field-assisted ionization") and the temperature ("temperature assisted ionization"). Fig. 2.7 shows the dependence of f_s on the difference between the Fermi energy in the bulk and at the surface $E_{f,s} - E_{f,b}$ and on temperature.

It should be considered that $E_{f,b}$ is a function of temperature. In normal operation the transistor is driven towards inversion and thus $E_{f,s} > E_{f,b}$. The line at $E_{f,s} = E_{f,b}$ shows the incomplete ionization of the bulk silicon. In this example, freeze out in the bulk starts appearing at about 100 K. Furthermore it can be seen, that for most temperatures and Fermi energies all of the dopants are ionized, making complete ionization a valid assumption. However, in the sub-threshold regime at low temperatures incomplete ionization starts playing a role, which can degrade the subthreshold slope [19].

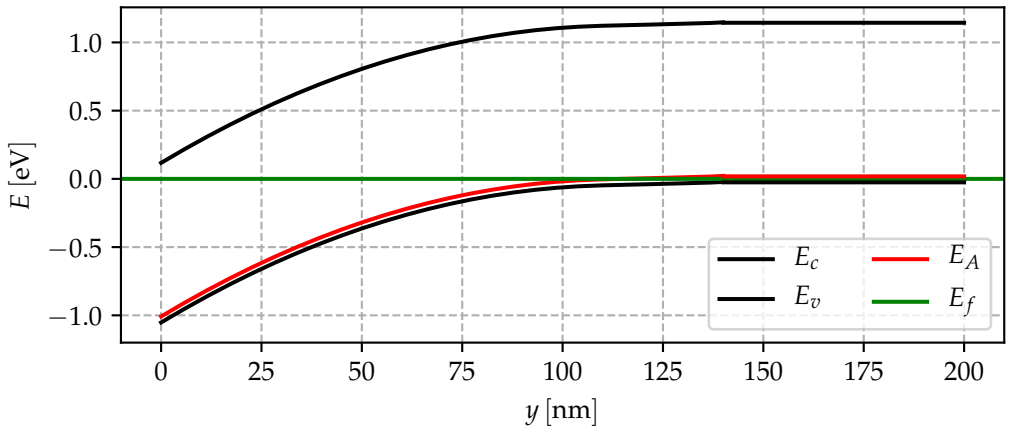


Figure 2.8.: Band diagram for a NMOS transistor as a function of the vertical position y. Temperature, bulk doping concentration and gate voltage are: $T = 30\,\mathrm{K}$, $N_A = 1 \times 10^{23}\,\mathrm{m}^{-3}$, $V_G = 0.2\,\mathrm{V}$. The Fermi energy E_f is used as reference energy and is set to 0. The band bending is calculated via numerically solving Poisson equation (eq.2.22).

In fig. 2.8 the band diagram for a NMOS transistor with an applied gate voltage of 0.2 V is shown. It can be seen that in the bulk region of the transistor the Fermi energy E_f is below the acceptor energy level E_A and thus the ionization factor f_s, as introduced in eq. 2.30, becomes very small: $f_s << 1$. The acceptor atoms in the bulk region therefore "freeze out". However, as the bands are bent towards the semiconductor oxide interface but the Fermi energy stays constants, f_s approaches 1 for small values of y. Out of the plot shown in fig. 2.8 it can be seen that in the region $y \lessapprox 100\,\mathrm{nm}$ all of the dopants are ionized, since f_s has an exponential dependence on the distance $E_A - E_f$. In that region ionization can be considered complete.

2.3.2. Mobility

Effective mobility at moderate transverse electric fields

The mobility μ of charge carriers (appearing in the MOSFET current equations, eq. 2.27 and eq. 2.28) is a strong function of temperature [35]. Different scattering mechanism affect the mobility, according to reference [36] they can be listed as follows:

- lattice scattering
- ionized impurity scattering
- surface scattering
- carrier-to-carrier scattering
- neutral-impurity scattering

The total mobility can be determined with Mathiessen's rule, via the inverse of the sum of all scattering rates of the above mentioned mechanisms [14]. However, this results in very complicated formulas that are unsuitable for compact modeling [36]. Therefore, different empirical laws for the temperature dependency of the mobility have been proposed. Emani et al. suggest an empirical model for the dependence of the mobility on the gate voltage (and thus transverse electric field) valid in the temperature range from 4.2 K to 300 K [37] [38]:

$$\mu = \mu_m \frac{[\theta(V_G - V_t)]^{n-2}}{1 + [\theta(V_G - V_t)]^{n-1}}, \tag{2.31}$$

where μ_m is proportional to the maximum mobility μ_{max}, θ is the mobility attenuation factor, V_t is the threshold voltage, and, n is an exponent coefficient. It should be noted that the parameters n, μ_{max} and θ as well as V_t are temperature dependent [37]. The relationship between μ_m and μ_{max} can be written as follows [37]:

$$\mu_{max} = \mu_m \frac{(n-2)^{\frac{n-2}{n-1}}}{n-1}. \tag{2.32}$$

A plot showing the mobility modeled with eq. 2.32 can be seen in fig. 2.9.

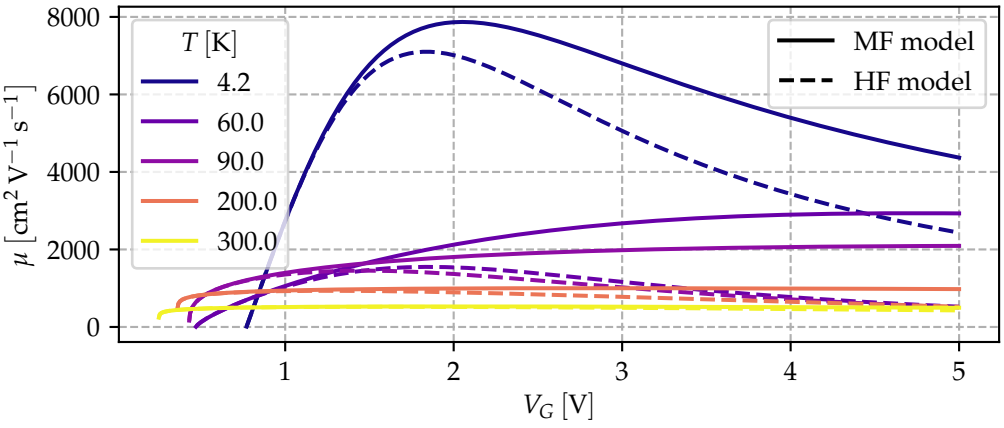


Figure 2.9.: Plots of the mobility μ as a function of the gate voltage V_G for different temperatures T. MF and HF refer to moderate electric field model and high electric field model and the mobilities are computed via eq. 2.32 and eq. 2.33 respectively. A table showing the used parameters can be found in the appendix 6.1.

Effective mobility at high transverse electric fields

At large gate overdrives and thus large vertical electric fields it is found that the transconductance can even become negative [39], for n-MOS [40] as well as p-MOS devices [41] [42].

This negative transconductance can be empirically modeled by introducing a second attenuation factor θ_2 and modifying eq. 2.32 [43]:

$$\mu = \mu_m \frac{[\theta(V_G - V_t)]^{n-2}}{1 + [\theta(V_G - V_t)]^{n-1} + [\theta_2(V_G - V_t)]^n}. \tag{2.33}$$

The reason for this negative transconductance at high fields and cryogenic temperatures can be explained by the dependence of different scattering mechanism on the electric field as well as on temperature [44] : at room temperature the mobility at low electric fields is dominated by phonon scattering and the mobility at high electric fields is dominated by surface roughness scattering whilst at cryogenic temperatures Coulomb scattering dominates phonon scattering for low electric fields and the dependence of surface scattering on the electric

field is much more pronounced. This is illustrated in fig. 2.10. In fig. 2.9 it can be seen that with the additional parameter θ_2 the mobility decreases at higher rates after the maximum.

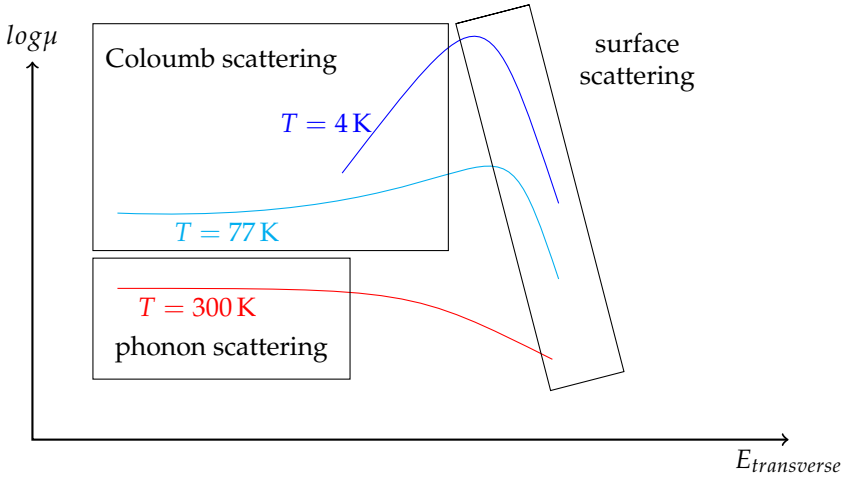


Figure 2.10.: Sketch of the main scattering mechanism affecting the mobility μ as a function of the transverse electric field $E_{transverse}$ for three different temperatures T. Redrawn as found in [44].

A detailed discussion and analysis on the above mentioned scattering effects can be found in the following references: [45] [46] [47].

2.3.3. Threshold voltage

The extraction method and definition of the MOSFET threshold voltage V_t is not uniquely defined [48] [49] [50]. One common way is to define the threshold voltage as the value of the gate voltage required to apply for the surface electron (hole) density to become equal to the hole (electron) concentration in the neutral bulk. For a NMOS transistor this condition reads:

$$n_{surface} = p_{bulk} = N_A. \tag{2.34}$$

It should be noted that strictly the threshold condition should be $n_{surface} = N_A^-$ but N_A^- can be very low at cryogenic temperatures (see fig. 2.7 at $E_{f,s} - E_{f,b} =$

0) and therefore a definition according to equation 2.34 is more meaningful [51], but still the effect of incomplete ionization can be incorporated in the resulting formula for V_t.

The threshold voltage V_t corresponds to the gate voltage that needs to be applied to satisfy eq. 2.34. Within the charge sheet approximation a formula for V_t can be derived (the derivation can be found in the appendix 6.41) [51]:

$$V_t = \phi_f^0 + \phi_m - (\chi + \frac{E_c - E_i}{e}) + \frac{\sqrt{2eN_A\epsilon_{si}}}{C_{ox}}\sqrt{\phi_f^0 + \phi_f^*}, \tag{2.35}$$

where ϕ_f (introduced in eq. 2.19) refers to the bulk Fermi potential, ϕ_f^0 is the bulk Fermi potential excluding incomplete ionization, ϕ_f^* is the bulk Fermi potential including incomplete ionization. Additionally, χ is the electron affinity of the semiconductor material and ϕ_m the metal work function. ϕ_f^0 and ϕ_f^* can be calculated via the following relation (derivation of ϕ_f^0 and ϕ_f^* and definition of factor A see appendix A.5):

$$\begin{aligned} \phi_f^0 &= \phi_t \log \frac{N_A}{n_i} \\ \phi_f^* &= \phi_t * \log \frac{-1 + \sqrt{1 + 4AN_A/n_i}}{2A}. \end{aligned} \tag{2.36}$$

Plots for $e\phi_f = E_i - E_f$ as a function of temperature for different doping concentrations were already presented in fig. 2.4, a plot showing a comparison between ϕ_f and ϕ_f^* can be found in the appendix 6.4.

A plot showing V_t as a function of temperature for three different doping concentrations can be seen in fig. 2.11. In these plots a n^+ poly silicon gate was assumed, such that the metal work function ϕ_m equals the silicon electron affinity χ. It can be seen that the doping concentration has a big impact on the value of V_t, mainly due to its influence in ϕ_f^0 and ϕ_f^* (compare fig. 2.4). Additionally the change of threshold voltage ($\Delta V_t = V_t(T) - V_t(T = 300\,\mathrm{K})$) as a function of temperature for three different doping concentrations is shown in fig. 2.12. It can be noted that just at very low temperatures differences in ΔV_t for the three doping concentrations become significant.

In many compact models the temperature dependence of the threshold voltage is modeled just by a linear term, which is quite accurate down to temperatures

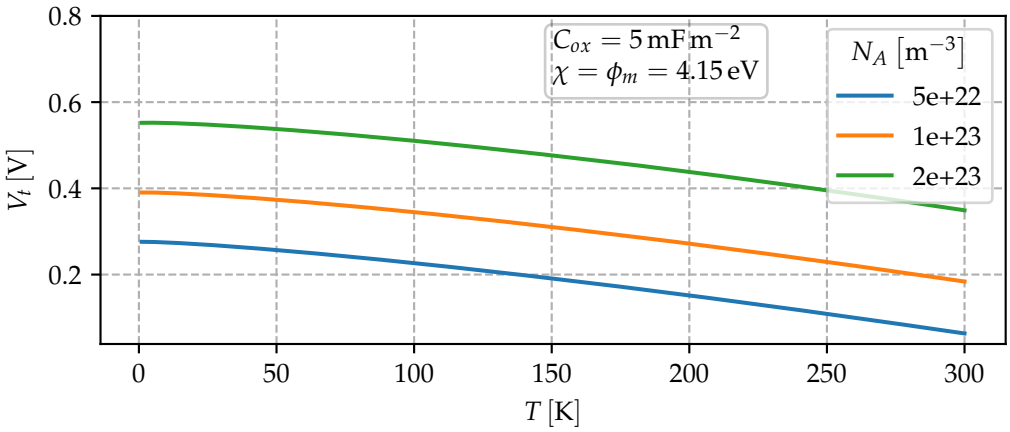


Figure 2.11.: Temperature dependence of the threshold voltage V_t for three different doping concentrations N_A.

of about 50 K, however for lower temperatures deviations from this linear behavior start appearing [52] as can also be seen in fig. 2.11.

2.3.4. Subthreshold swing

The subthreshold swing S is related to the switching characteristics of a transistor and describes how fast it is turned off/on by the gate voltage. It is defined as the inverse of the derivative of the subthreshold drain to source current $I_{DS,sub}$ with respect to the applied gate bias V_{GS} [20]:

$$S = \left(\frac{\partial log I_{DS,sub}}{\partial V_{GS}} \right)^{-1} = \log(10) \frac{m k_B T}{e}, \tag{2.37}$$

where the factor $m \geq 1$ accounts for the depletion and interface traps capacitance and has an upper bound of roughly 2 when not accounting for interface traps [19]. Fig. 2.13 shows a typical transfer characteristic of a MOSFET. In the subthreshold region I_D has an exponential dependence on V_G, thus a straight line on logarithmic scale. The inverse of this slope is defined as the subthreshold slope.

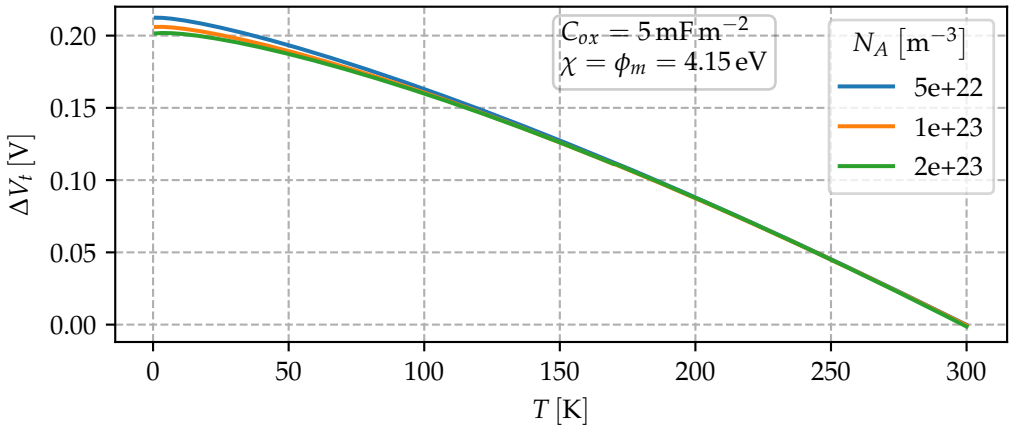


Figure 2.12.: $\Delta V_t = V_t(T) - V_t(T = 300\,\mathrm{K})$ as a function of temperature for three different doping concentrations N_A.

Eq. 2.37 with $m = 1$ is known as Boltzmann thermal limit, which corresponds to $S \approx 200\,\mu\mathrm{V/K/dec}$. However, there is a nonlinear deviation from this limit, which according to recent publication by Bohuslavskyi et al. [17] can be assigned to a source to drain diffusion current in the subthreshold regime.

A common way to model deviations from the predicted linear behavior of S is to make m a temperature dependent quantity [53]. Typically S starts to deviate from the linear temperature behavior at temperatures below 50 K , as for example measured in reference [17].

2.3.5. Interface traps

Interface trap charges Q_{it} can be introduced in eq. 2.17 as additionally appearing charges. They are associated with a voltage $V_{it} = \frac{-Q_{it}}{C_{ox}}$. The sign of Q_{it} can be positive or negative, where trap energy levels below mid-gap have donor-like characteristics and trap energy levels above the mid-gap have acceptor-like characteristics [54]. Their occupation status depends on the Fermi-level at the silicon-oxide interface and therefore on the surface potential ψ_s [55].

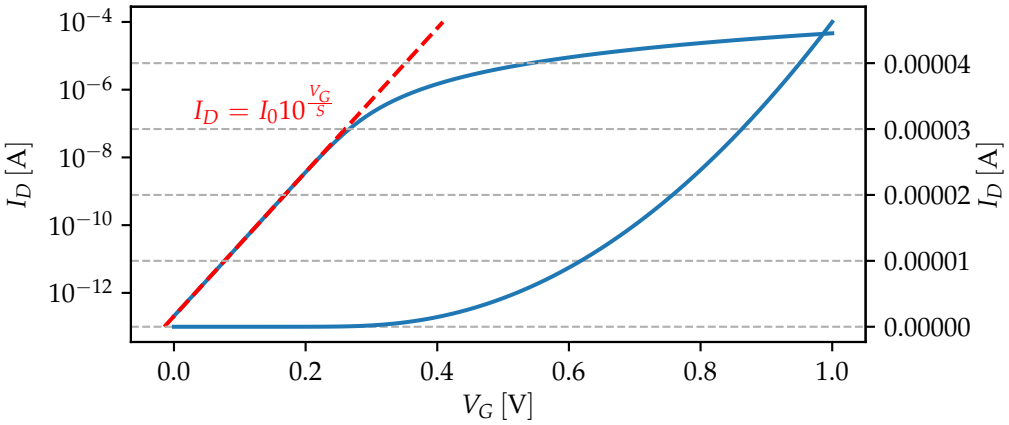


Figure 2.13.: Plot of a typical MOSFET transfer characteristic (drain current I_D versus gate voltage V_G) on linear and logarithmic scale. In the subthreshold region I_D has an exponential dependence on V_G. The subthreshold slope S corresponds to the inverse of the linear slope of I_D versus V_G on logarithmic scale.

Q_{it} can be calculated for a given interface trap density D_{it} and trap degeneracy factor g_{it} via:

$$Q_{it} = -e \int_{E_v}^{E_c} D_{it}(E) f_{it}(E, E_f) dE, \tag{2.38}$$

where $f_{it}(E)$ is an occupation factor of the form:

$$f_{it}(E, E_f) = \frac{1}{1 + g_{it} \exp\left(E - E_f\right)/(k_B T)}. \tag{2.39}$$

For a continuous interface trap density the integral, eq. 2.38 can typically not be solved analytically, however for discrete levels D_{it} reduces to a sum of delta functions and eq. 2.38 reduces to the following summation [19] :

$$Q_{it} = -e \sum_{j=1}^{N} N_{it,j} f_{it}(E_j, E_f), \tag{2.40}$$

where $N_{it,j}$, N and E_j are the number of interface states at the jth trap level, the total number of different trap energies and the energy of the jth trap level.

It should be noted, that f_{it} also depends on temperature, and for a incorporation of interface traps with eq. 2.40 including just one trap (N=1) it can be shown to influence the subthreshold slope via the following relation [19]:

$$S = \log(10)\frac{mk_{\mathrm{B}}T}{e} + \frac{eN_{it}}{C_{ox}}\frac{g_t \log(10)}{(1+g_t)^2}. \tag{2.41}$$

2.4. Self heating

High power densities (dissipated power per unit area) can be present in (sub-) micron CMOS circuits because of a high density of active devices. In recent literature there are many publications in the field of self heating in silicon on insulator (SOI) technologies [56] [57], where the problem is even more critical due to the low thermal conductivity of the additional insulating layer.

Driving a current I through an electronic device will heat it up according to Joule's first law, where the power P that is converted from electrical to thermal energy is calculated via :

$$P = VI = I^2R = V^2/R, \tag{2.42}$$

where V and R are the voltage drop across the device and the resistance of the device, respectively. This dissipated power leads to a local increase of temperature that is commonly simplified via [58] [59]:

$$T = T_{amb} + PR_{th}, \tag{2.43}$$

where R_{th} is the thermal resistance and T_{amb} is the ambient temperature.

2.4.1. Simplified radial model

Heat conduction phenomena can be described with Fourier's law [60]:

$$\dot{q} = -K\nabla T, \tag{2.44}$$

where $\dot{q}$ is the heat flux ([$\mathrm{W\,m^{-2}}$]), K the thermal conductivity ([$\mathrm{W\,m^{-1}\,K^{-1}}$]), ∇ the nabla operator for spatial derivatives, and T the temperature.

The steady state solution of a point source distributing heat in an isotropic, semi-infinite medium can be written as:

$$\dot{q} = \frac{P}{2\pi r^2}, \tag{2.45}$$

where P is the power and r is the radial distance to the source. It is assumed that the emitted power per half sphere is a constant, which directly leads to eq. 2.45. Considering now only the radial component in eq. 2.44, it can be written as:

$$\frac{P}{2\pi r^2} = -K\frac{\partial}{\partial r}T(r), \tag{2.46}$$

where it was used that the radial component of ∇ is $\nabla_r = \frac{\partial}{\partial r}$.

Assuming a temperature independent thermal conductivity, the differential equation 2.46 is easily solved via integration, a particular solution can be obtained if the additional constraint $T(r_1) \stackrel{!}{=} T_0$ is required:

$$T(r) = \frac{P}{2\pi K}\left(\frac{1}{r} - \frac{1}{r_1}\right) + T_0. \tag{2.47}$$

In fig. 2.14 a plot of such a temperature distribution is shown. It should be noted that the chosen parameter for the thermal conductivity K corresponds to the literature value for K of silicon at around 30 K [61]. Since the temperatures in the given example just vary within around 0.3 K, the assumption of a temperature independent thermal conductivity can be justified.

The temperature right at the heat source drops rapidly towards the temperature T_0. The radical temperature drop can be explained with the very high thermal conductivity of silicon at those temperatures (K at 30 K is around 35 times higher than at room temperature [61]). This very high thermal conductivity leads to very efficient transport of thermal energy into the semiconductor.

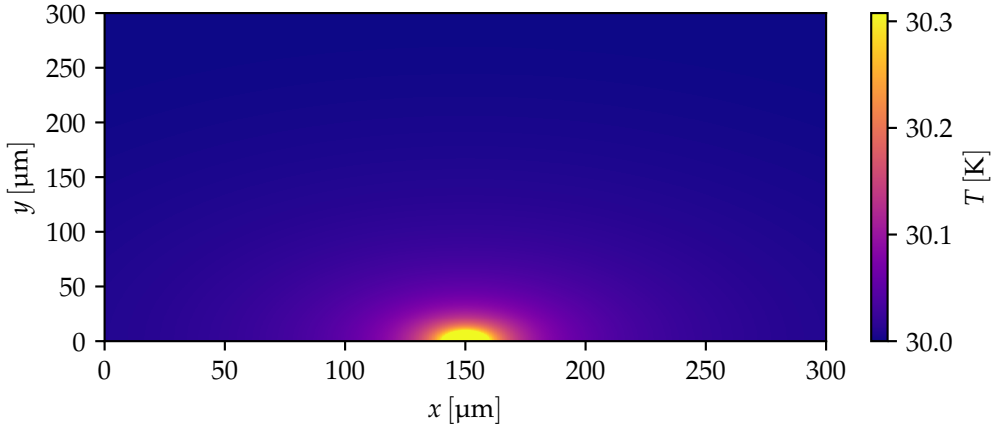


Figure 2.14.: Radial temperature profile $T(r = \sqrt{(x-x_0)^2 + (y-y_0)^2})$ as a function of vertical and horizontal position x and y. A (half) spherical heat source is assumed with a radius r_{source} of 10 µm, such that $T(r < r_{source}) = T(r_{source})$ and $T(r > r_{source})$ is given by eq. 2.47. The used parameters are: $P = 100\,\mathrm{mW}$, $K = 5000\,\mathrm{W\,m^{-2}}$, $r_1 = 300\,\mu\mathrm{m}$ and $T_0 = 30\,\mathrm{K}$ and the heat source is placed at $x_0 = 150\,\mu\mathrm{m}$ and $y_0 = 0\,\mu\mathrm{m}$.

3. Experimental setup

In this section the used measurement setup and devices are presented. Measurements were performed in the laboratory at KAI, Villach, either at the needle prober 3.1 or at the cryogenic probe station 3.2.

3.1. Needle prober

The needle prober from Süss MicoTech was used to perform measurements at room temperature only. Electrical characterizations were done with a Keysight B1500A semiconductor device parameter analyzer.

3.2. Cryogenic probe station

The cryogenic setup consists of a LakeShore CRX-6.5K probe station. The cryostat is a close-cycle type and the covered temperature range is 6.5 K to 675 K , where any temperature within that range can be set with the LakeShore model 336 cryogenic temperature controller. The used compressed and expanded medium in the cryostat is liquid helium and in normal operation the probe chamber is evacuated to high vacuum. The system is equipped with a vision system consisting of a high sensitivity color CCD camera and a monitor. 4 probe arms are installed to the station, allowing to electronically bias up to four terminals of the device under test.

Communication to all of the used devices (measurement devices, temperature controller) is done via an in house built LabView software. This software establishes proper connections to all devices, offers a graphical live output of the measurement results and enables storing the measured data.

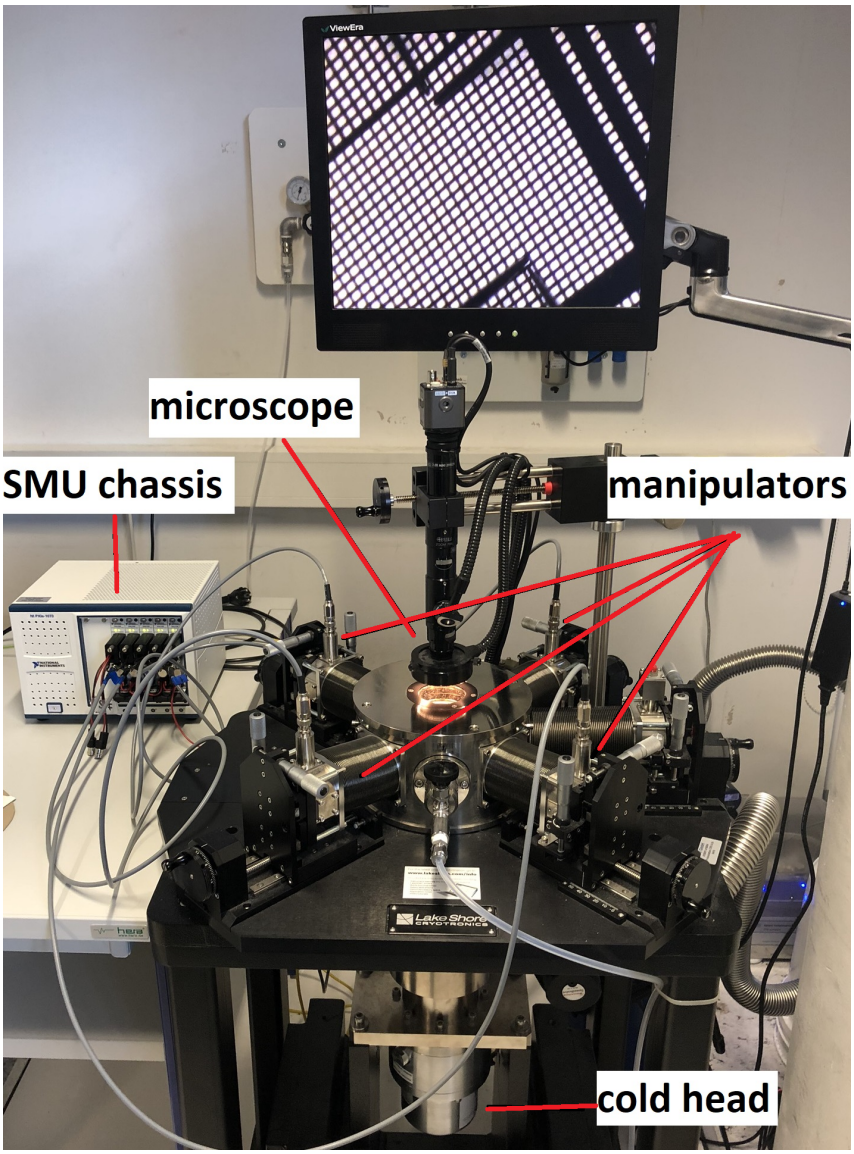


Figure 3.1.: Cryogenic measurement station. The source-measurement-unit (SMU) -chassis contains 5 high precision SMUs that are connected to the 4 manipulators and to a chuck connector on the backside of the cryostat. With the 4 manipulators probe arms in the probing area can be controlled and devices can be electrically contacted with needles mounted to these probe arms. The screen shows an image of the loaded sample recorded with the microscope. The cold head at the bottom of the station is a 2-stage Gifford-McMahon cryocooler.

3.2.1. Current-voltage measurements

Current-voltage measurements at the cryogenic probe station are performed with 4 National Instrument (NI) source measurement units (PXIe 4135 - Precision SMU).

3.2.2. Capacitance-voltage measurements

Capacitance-voltage characteristics are recorded using the Agilent 4292A Precision Impedance Analyzer. The outputs of the measurement device are extended with the Keysight 16048H Extension Cable. The covered frequency range is 40 Hz to 110×10^6 Hz and impedances are measured using the Four-Terminal Pair configuration with the Auto-Balancing-Bridge method [62].

4. Measurement techniques and results

Experimental results of the measurements are presented in this section. Temperature dependent measurements are colored in accordance to the colorbar given in fig. 4.1.

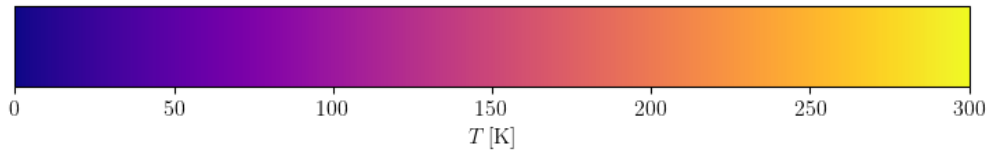


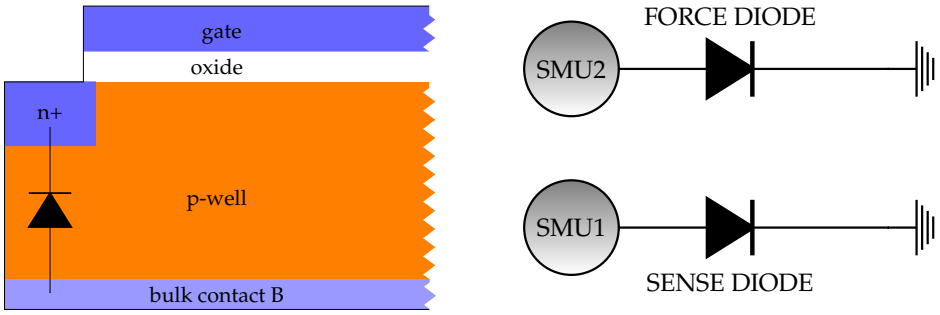
Figure 4.1.: Colorbar for temperature dependent measurements.

4.1. Self-heating

4.1.1. Measurement method

The temperature rise due to self heating was measured with the body diodes of two neighboring transistors. The body diode, as sketched in fig. 4.2a, is an intrinsic p-n-junction of the MOSFET between the source/drain contact (n (p) doped) and the body contact (p (n) doped).

The measurement idea is, that the forward bias current of the diode at a given voltage is a strong function of temperature, and thus the diode can be calibrated as a thermometer. One could also take a reverse bias current, but the diodes



(a) Schematic drawing of the body diode.

(b) SMU2 is forcing a large current and thus a large power dissipation in body diode 2 (FORCE DIODE) whilst SMU1 is powering diode 1 (SENSE DIODE) which acts as a self self.

that were used in this measurement were simply too small to get a measurable current in reverse bias conditions.

At the same time a diode can be used as a two terminal device where a lot of power can be dissipated. Thus the measurement consisted of the following steps:

- identification of two appropriate body diodes
- calibration of the sensor diode as a thermometer: characterizing the diode as a function of temperature
- dissipation of power in the force diode and at the same time measuring the temperature with the sensor diode.

Fig. 4.3 shows the measured characteristics of the diode for different temperatures. A reference voltage of $V_{sense} = 1\,\mathrm{V}$ was chosen and plots of the measured currents for this bias can be found in fig. 4.4.

4.1.2. Measurement results

The thermometer diode was calibrated as described in section 4.1.1. The force diode was swept very slowly from 0 V to a forward bias of 4 V, where the integration time for each point was 100 power-line-cycles or equivalently 2 s. The measurement was performed for four different chuck temperatures

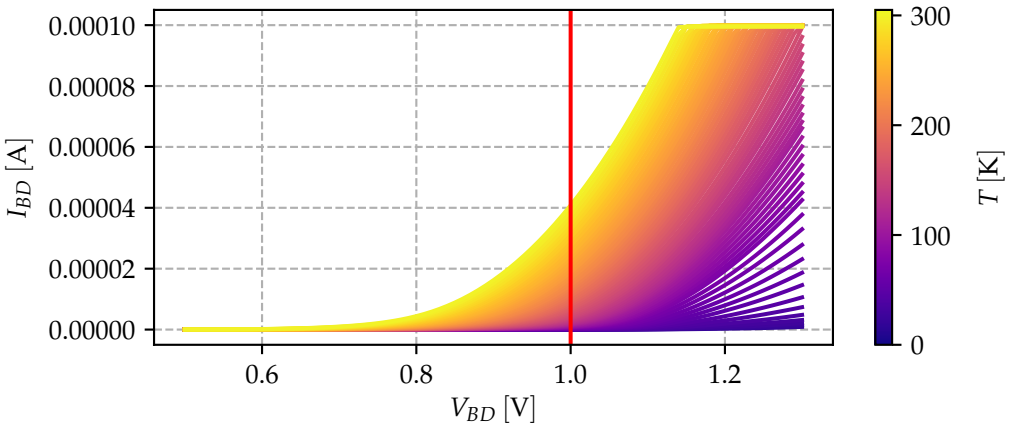


Figure 4.3.: Body diode thermometer: drain to bulk current I_{DB} as a function of the drain to bulk voltage V_{DB} for different temperatures. The vertical red line shows the chosen reference voltage. A plot of measurements along this line can be found in fig. 4.4.

(T_{amb}) in the range of 20 K to 50 K. Results of the sensed temperature as a function of the applied power can be seen in fig. 4.5, the temperature raise ($\Delta T = T_{sense} - T_{amb}$) can be seen in fig. 4.6. The measurements indicate that the self heating effects are quite similar for the different ambient temperatures. One can see that the local temperature rise is very high for powers in the mW-regime, going up to about 200 K for powers of about 400 mW.

Additionally it should be noted that the measurement error in temperature δT is approximated to be $\delta T \approx 5\,\mathrm{K}$ as ΔT does not perfectly approach 0 for very low applied powers P and does not depend on the applied power till $P \approx 1 \times 10^{-4}\,\mathrm{W}$.

Table 4.1 shows a summary of measured self heating effects in n- as well as p-MOSFETs. Measurement results and data presented in this table show good agreement. The main take-away from this measurements is, that as long as the applied power stays below the mW - regime, self heating effects can be neglected, but once the applied powers are beyond that level, the device heats up very quickly, effecting many of the semiconductor properties as described in section 2.

Table 4.1.: Self heating measurements results found in literature. Table taken from [63]. P_{appl} : applied power ; T_{amb} : ambient temperature ; ΔT[K] : temperature raise due to self heating ; R_{th} : thermal resistance.

Type	P_{appl} [mW]	T_{amb} [K]	ΔT[K]	R_{th}[K W^{-1}]	Reference
n-MOSFET	15	4.2	40	2667	[64]
n-MOSFET	30	20	24	800	[65]
		80	10	333	
		200	9	300	
p-MOSFET	46 – 60	20	24	522 – 400	[66]
		80	12	261 – 200	
		200	11	239 – 183	
n-MOSFET	120	4.2	37	308	[67]
	57		32	561	
	32		29	906	
	14		25	1786	
n-MOSFET	40	10	4.6	115	[68]
	30		3.4	113	
	15		1.7	113	

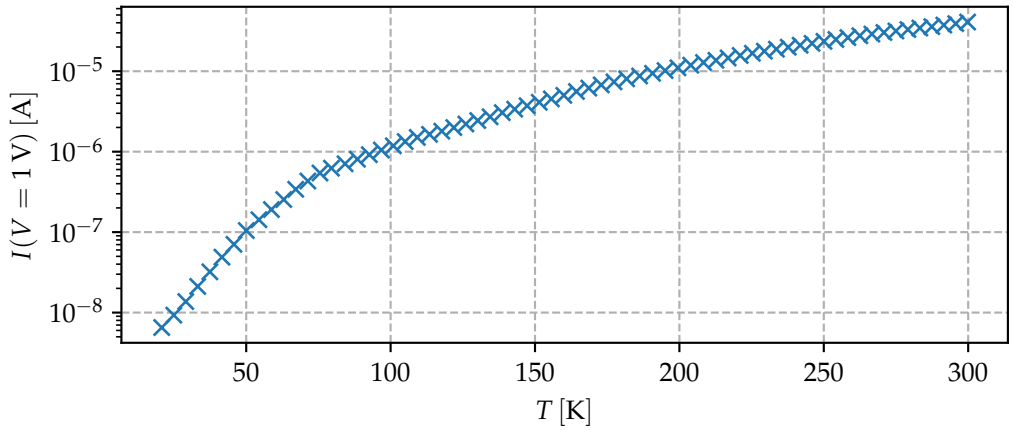


Figure 4.4.: Body diode thermometer: drain to bulk current I_{DB} at $V_{DB} = 1\,\mathrm{V}$ as a function of temperature T.

Table 4.2.: Thermal conductivity K of silicon at different temperatures T, taken from ref. [61]. The column $T_{sense,model}$ refers to the expected sensored temperature according to the simplified model presented in sec. 2.4.1.

T_{amb} [K]	$K\left[\mathrm{W\,cm^{-1}\,K^{-1}}\right]\mathrm{at}T_{amb}$	$T_{sense,model}$ [mK]
20	49.8	3
30	48.1	3
40	35.3	5
50	26.8	6

4.1.3. Comparison to simplified radial model

The thermal conductivity of silicon at the measured ambient temperatures can be seen in tab. 4.2. Assuming an applied power of $P = 100\,\mathrm{mW}$ (which according to the results presented in fig. 4.5 leads to a significant increase in temperature), and assuming a wafer thickness of $r_1 \approx 300\,\mu\mathrm{m}$ the expected temperature at a distance r can be calculated.

The force and sense diodes had a spacial separation of around $r \approx 230\,\mu\mathrm{m}$, thus one can calculate the expected sensored temperature according to this simple model. The results of such a calculation are presented in tab. 4.2. The order of

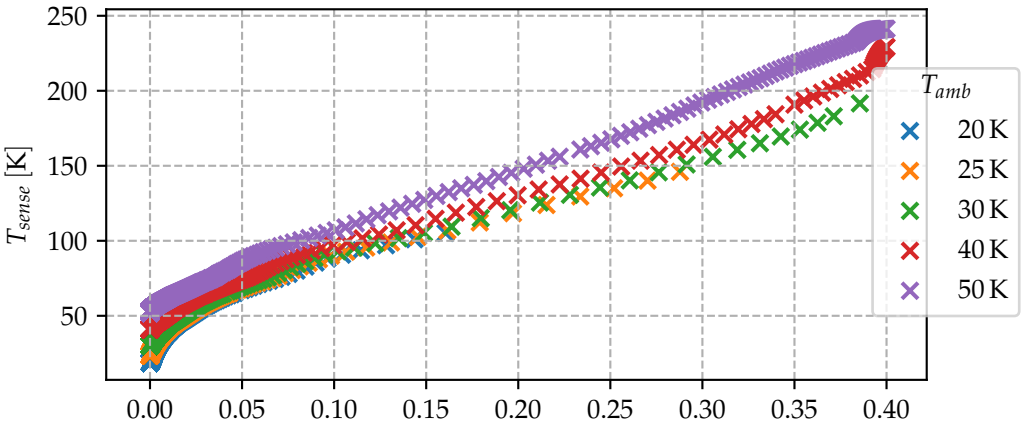


Figure 4.5.: Measured temperature T_{sense} as a function of the dissipated power P for different chuck temperatures T_{amb}.

magnitude is by far smaller then the measured temperatures, indicating that this simplified model is not sufficient to describe the temperature distribution. What is assumed, for example, is that the chip is thermally perfectly coupled to the chuck which in practice is not true. If the thermal resistance of the sample-chuck interface is very high, the applied power could heat up the whole sample, as in the sample the heat is distributed very homogeneously. Thus the recorded temperature raise probably belongs to heating of the whole chip rather than to some local (intersample) temperature change.

To further investigate and verify this assumption any of the following measurements could be performed:

- Sensing the temperature at different points: Relying on the same measurement principle as presented in this section, power could be applied in one body diode and measured at two (or more) other body diodes. In this way the radial temperature distribution could be analyzed.
- Pyrometry: Via the optical access window into the cryostat contactless temperature measurement of the sample surface could be performed using a pyrometer.
- Time dependent temperature measurements: Local heating and global heating of the whole chip can be expected to happen on different time

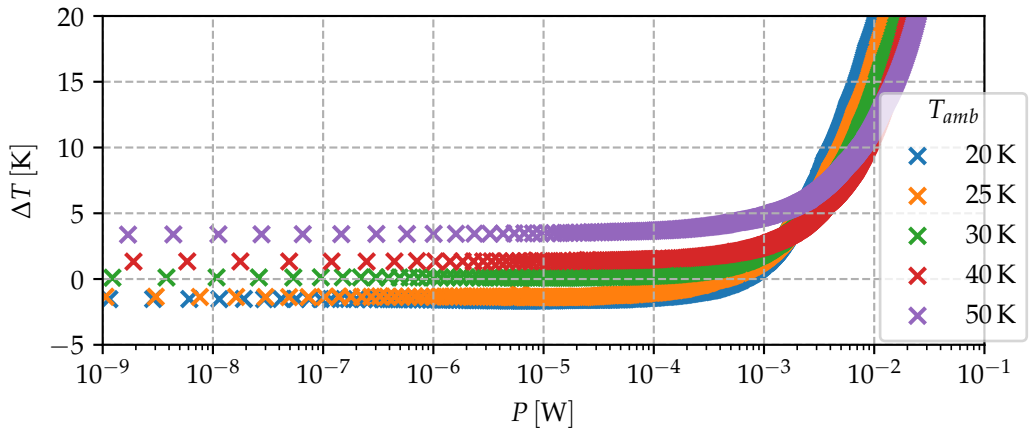


Figure 4.6.: Measured temperature raise $\Delta T = T_{sense} - T_{amb}$ as a function of the dissipated power P for different chuck temperatures T_{amb}.

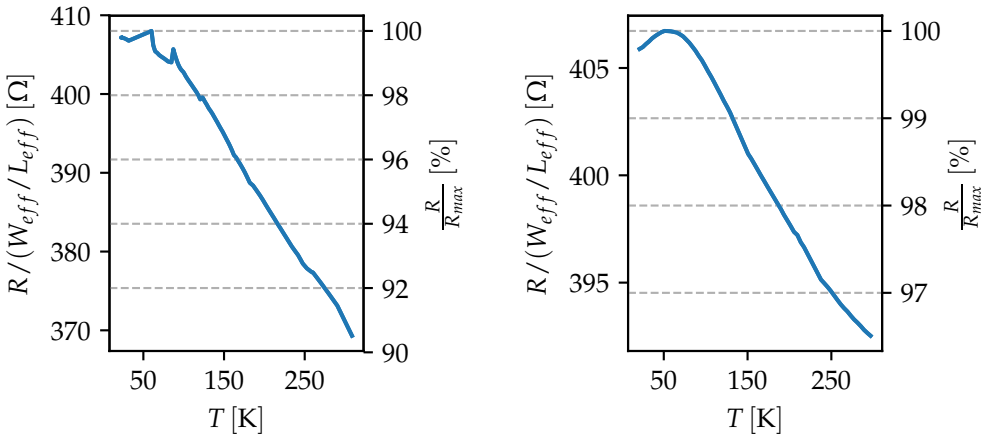
scales. Extracted time constants τ of the heating process could be used to estimate the thermal resistance R of the chuck sample interface, since $\tau = R \cdot C$, and values of the thermal conductivity C at different temperatures can be found in literatur.

4.2. Temperature dependence of resistors

The temperature dependence of poly-silicon (poly) resistors has been measured. The resistance of poly resistors is known to hardly change with temperature, as for example reported in [69].

Measurement results for a n-poly- and a p-poly-resistor can be seen in fig. 4.7. The resistances show a weak temperature dependence in both cases, variations are smaller than 10 %. The curves show a maximum at about 70 K.

Additionally, poly resistors produced with a self-aligned silicide process (salicide) were measured. This process lowers the sheet resistance and is applied in CMOS technologies at source drain contacts or also at the polysilicon gate. Results of the resistivity of salicided poly resistors can be seen in fig. 4.8. Unlike the results presented in fig. 4.7, these one show a strong temperature dependence.



(a) n-poly resistor

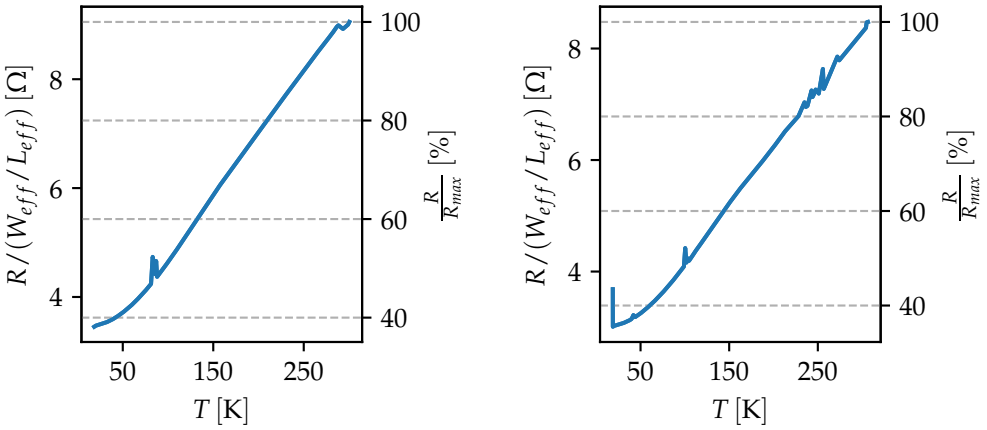
(b) p-poly resistor

Figure 4.7.: Resistance R of poly resistors as a function of temperature T. The right axis shows the ratio of the measured resistance to maximal measured resistance.

The resistivity is reduced by a factor of roughly 3, which is in good agreement with results reported in [70], where similar measurements have been performed. They report a linear temperature dependence of the resistivity for temperatures higher than 75 K and a saturation to a constant resistivity for temperatures below 50 K. It can be noted that the silicided structures behave comparable to a metal in terms of resistivity. The linear dependence of the resistivity is typical for electron- phonon scattering whilst the saturation towards a temperature independent value can be assigned to impurities and crystallographic defects [71].

4.3. Temperature dependence of capacitors

Capacitance versus voltage measurements were performed on a CMOS capacitor structure, consisting of a n-well and a n-type poly gate separated by an oxide with a nominal thickness of about 6 nm. The applied voltage was varied to drive the capacitor from inversion (highly negative voltages) to accumulation (highly positive voltages). As can be seen in fig. 4.9f the value of the oxide capacitance (the capacitance approaches the oxide capacitance in accumulation)



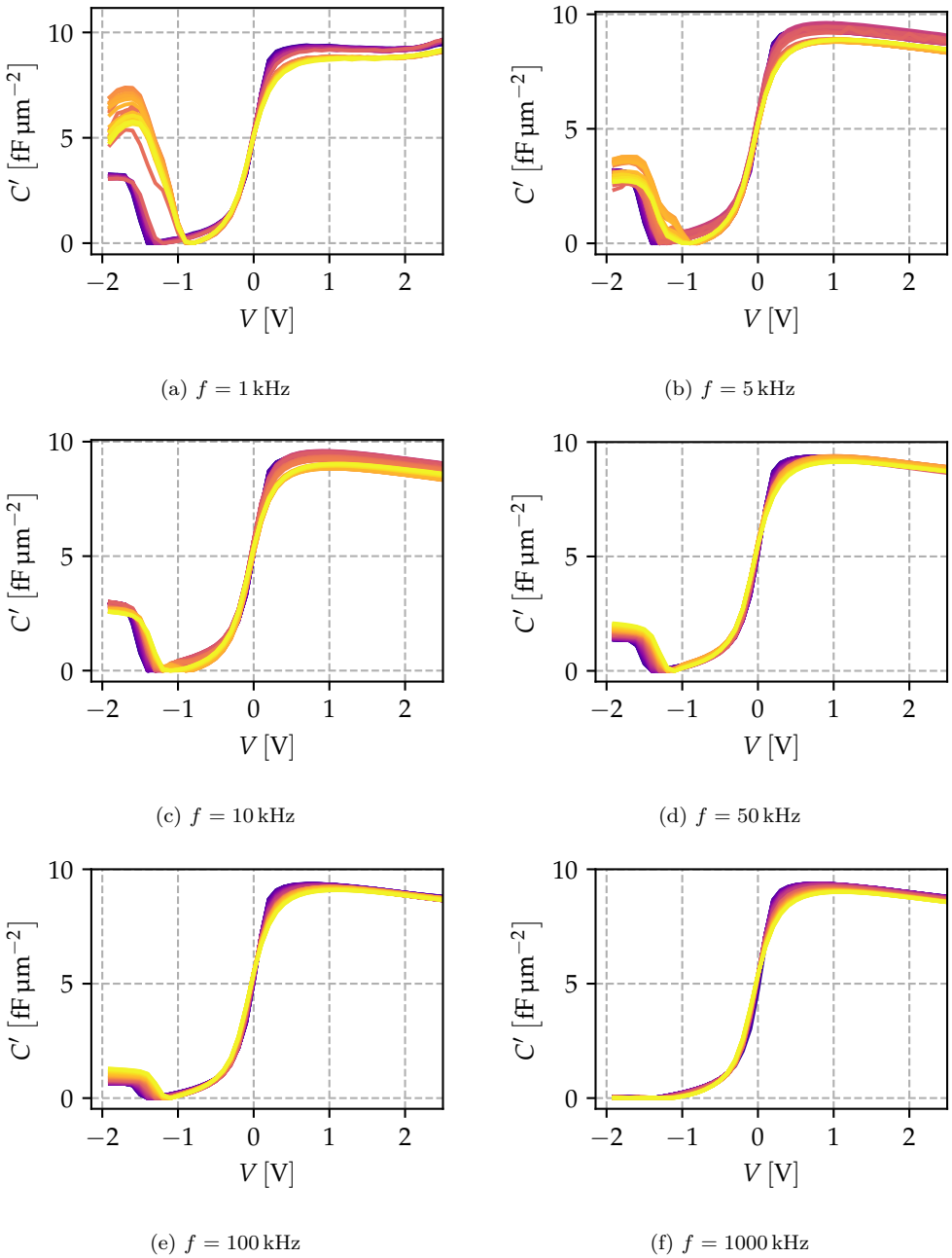
(a) n-poly resistor salicided

(b) p-poly resistor salicided

Figure 4.8.: Resistance R of salicided poly resistors as a function of temperature T. The right axis shows the ratio of the measured resitance to maximal measured resistance.

just slightly varies with temperature. This observation is in agreement with recent literature [72] [73]. However, depending on the doping concentration of the poly gate/n-well also freeze out effects can occur, leading to a sharp decrease of the accumulation and depletion capacitance at the freeze out temperature [36].

For lower frequencies the inversion branch starts appearing. This frequency dependent effect can be explained with the ability of the electrons to follow the applied ac signal [20], and according to the measurements it does not seem to be dependent on temperature. Measurements at lower frequencies than those presented in fig. 4.9 resulted in unreasonable measurement curves and errors from the impedance analyzer and are thus not presented here. Already the measurement at 1 kHz shows some of these effects.



(a) $f = 1\,\mathrm{kHz}$

(b) $f = 5\,\mathrm{kHz}$

(c) $f = 10\,\mathrm{kHz}$

(d) $f = 50\,\mathrm{kHz}$

(e) $f = 100\,\mathrm{kHz}$

(f) $f = 1000\,\mathrm{kHz}$

Figure 4.9.: Measured capacitance per unit area C' as a function of the voltage V for different frequencies f and temperatures.

4.4. Charge pumping measurement

4.4.1. Measurement method

The charge pumping technique for MOS devices [74] allows the determination of the trap density C_{it} in the Si-SiO_2 interface. In the following a n-MOS transistor with electrons as main charge carriers is assumed, however the considerations can easily be inverted for the case of a p-MOS transistor.

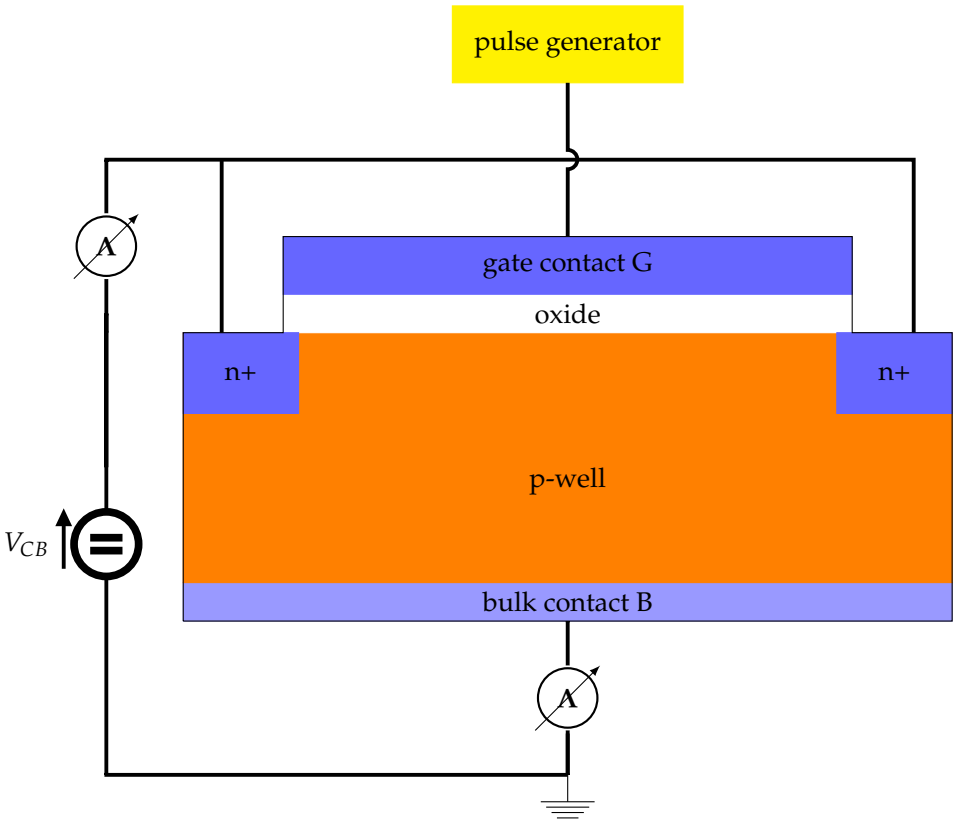


Figure 4.10.: Sketch of a charge pumping measurement setup for a n-MOS transistor.

As sketched in fig. 4.10, the source and drain contact of the transistor are electrically shortened and an optional bias voltage V_{CB} can be applied. The

amplitude of the pulsed signal on the gate must be sufficiently high to drive the transistor in inversion and accumulation. Different signal forms for the gate bias are possible (e.g. square, triangular, trapezoidal or sinusoidal [75]).

This way an inversion channel is periodically built and closed in the transistor with the frequency given by the external gate bias. During inversion, most electrons remain free in the conduction band, whilst some are captured at trap states at the semiconductor-dielectric interface. When switching the gate bias, going to accumulation, the electrons in the conduction band flow back to the source/drain terminals, whereas for the trapped electrons it takes a longer time to escape from their trapping potential. In case the frequency is high enough, incoming holes recombine with these trapped electrons before they can escape, leading to a charge pumping current I_{CP}^{max}, which is given by [76]:

$$I_{CP}^{max} = A_{G,eff} f q N_{CP}, \tag{4.1}$$

where $A_{G,eff}$ is the effective gate area, f is the frequency of the gate bias signal and N_{CP} is the number of charges per unit area. Additionally, a so called geometric charge pumping current I_{Geo} [77] might additionally be present leading to a total measured bulk current I_B:

$$I_B = I_{CP}^{max} + I_{Geo}. \tag{4.2}$$

The origin of this current is that also some of the free electrons in the channel might not be "evacuated" quickly enough and also recombine with incoming holes. However, in many cases, this additional current is negligible in comparison to I_{CP}^{max} [78], leading to $I_B \approx I_{CP}^{max}$. Thus, via measuring I_{CP}^{max} the number of interface charges per unit area can be estimated.

4.4.2. Measurement results

Charge pumping measurements were carried out to estimate the number of interface traps in the characterized devices, which is an important model parameter.

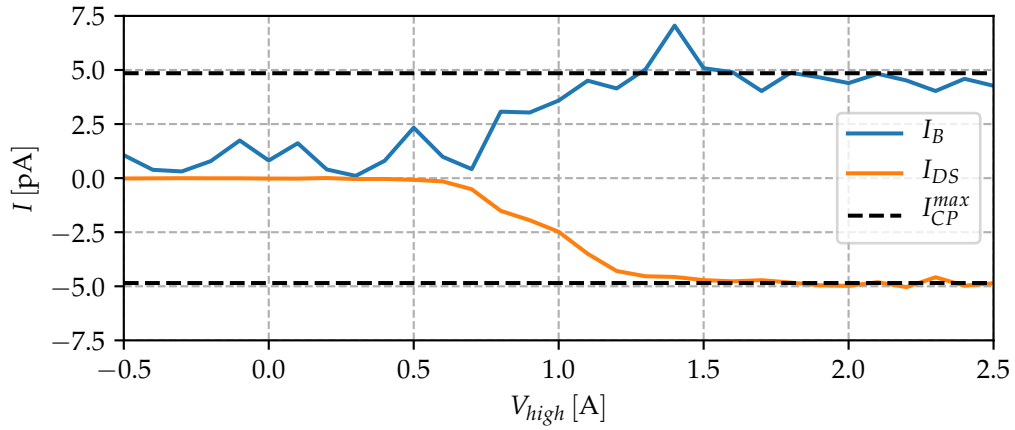


Figure 4.11.: Charge pumping measurement at room temperature. A bulk current I_B and a drain to source current I_{DS} appear due to recombination with trapped charges. The maximal charge pumping current I_{CP}^{max} is estimated via averaging over I_{DS} values for high level voltages $V_{high} > 1.5\,\mathrm{V}$.

Table 4.3.: Charge pumping: Measurement and device parameters.

parameter	W/L	$V_{G,high}$	$V_{G,low}$	f
value	$5/5\,\mu\mathrm{m}$	$-0.5\,\mathrm{V}$ to $2.5\,\mathrm{V}$	$-2.5\,\mathrm{V}$	$10\,\mathrm{kHz}$
parameter	$\frac{dV_G}{dt}$	V_{DS} / V_B	T	DC
value	$10\,\mu\mathrm{V\,s^{-1}}$	$0/0\,\mathrm{V}$	$300\,\mathrm{K}$	$50\,\%$

The measurement result for one transistor (parameter according to tab. 4.3) can be seen in fig. 4.11. The value of I_{CP}^{max} is extracted and the number of interface traps per unit area can be approximated to be:

$$I_{CP}^{max} \approx 4.85\,\mathrm{pA} \Rightarrow N_{CP} \approx 6.055 \times 10^{9}\,\mathrm{cm^{-2}}. \tag{4.3}$$

4.5. Split CV measurement

4.5.1. Measurement method

The Split-CV measurement setup was firstly introduced by Koomen in 1973 [79], it allows the experimental determination of the transistor mobile inversion charge Q_i, which can then be used to calculated the effective mobility μ_{eff}. Q_i is determined via measuring the gate to channel capacitance, a typical measurement setup can be seen in fig. 4.13. Having measured the gate to channel capacitance C_{GC}, the inversion charge can be calculated via [80]:

$$Q_i = \int_{-\infty}^{V_G} \frac{C_{GC}}{WL} dV_G. \tag{4.4}$$

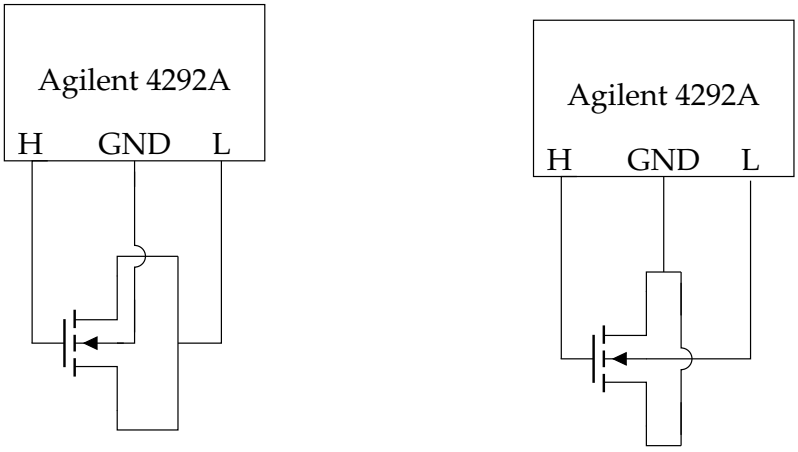
The effective mobility can then be extracted as a function of the gate voltage, if additionally the transitor transfer characteristic ($I_D(V_G)$ for a fixed V_D) is measured:

$$\mu_{eff} = \frac{LI_D}{WV_DQ_i} \tag{4.5}$$

In eq. 4.5 $\frac{I_D}{V_D}$ can also be replaced with the drain transconductance $g_D = \frac{dI_D}{dV_D}$ [80].

4.5.2. Measurement results

The measurement results from the split-CV measurement can be seen in fig. 4.15. The threshold voltage shifts towards higher (absolute) values for both transistors. For high gate voltage overdrives, the inversion channel is fully built and therefore C'_{GC} approaches the value of the nominal oxide capacitance per unit area. The oxide capacitance per unit area is about half of the value of the capacitance per unit area measured in section 4.3 due to the fact, that the oxide thickness is twice as big.



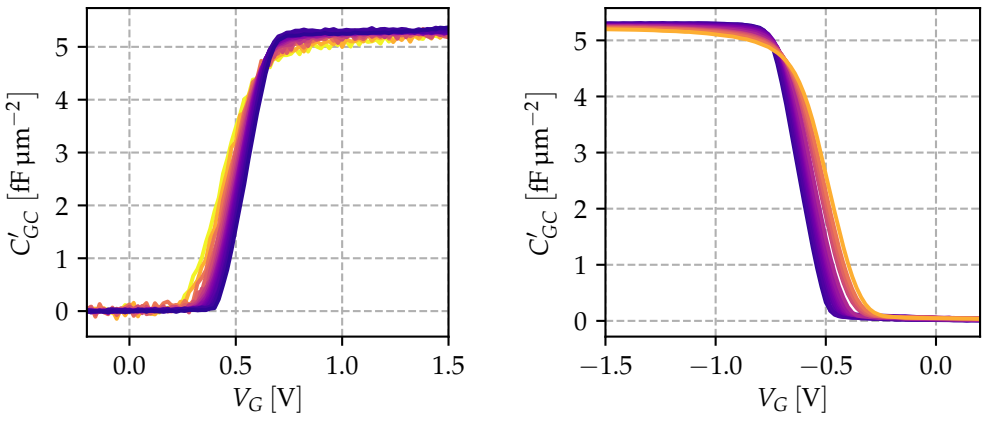
(a) Setup to measure the gate to channel capacity C_{GC}

(b) Setup to measure the gate to bulk capacity C_{GB}

Figure 4.12.: Setup for the split CV measurement with the Agilent 4292A impediance analyzer.

Additionally, transfer characteristics were recorded for different drain biases and temperatures. Results for a drain voltage of $V_D = 20\,\mathrm{mV}$ can be seen in fig. 4.14. The data for the NMOS transistor show a negative transconductance at low temperatures, due to increased influence of surface scattering at low temperatures as described in section 2.3.2.

Combining the measurements presented in fig. 4.13 and fig. 4.14, the mobility was calculated with eq. 4.5. Results for the NMOS as well as the PMOS transistor can be found in fig. 4.15. μ_{eff} as a function of the gate voltage (and thus vertical electric field) has a maximum at gate voltages of around 1.3 V, which shifts slightly with a change in temperature. For high gate voltages the mobility decreases. This decrease becomes more pronounced the lower the temperatures. For the lowest temperature curve of the NMOS transistor (fig. 4.15a), the maximum mobility has a value of around $2000\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ whereas the mobility at $V_G = 3\,\mathrm{V}$ is around $800\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$, which is a relative decrease of around 60 %. This high decrease in mobility at high fields for low temperatures leads to the negative transconductances recorded at theses temperatures (as can be seen in fig. 4.14a). When rearranging eq. 4.5 one can see that the drain



(a) NMOS transistor

(b) PMOS transistor

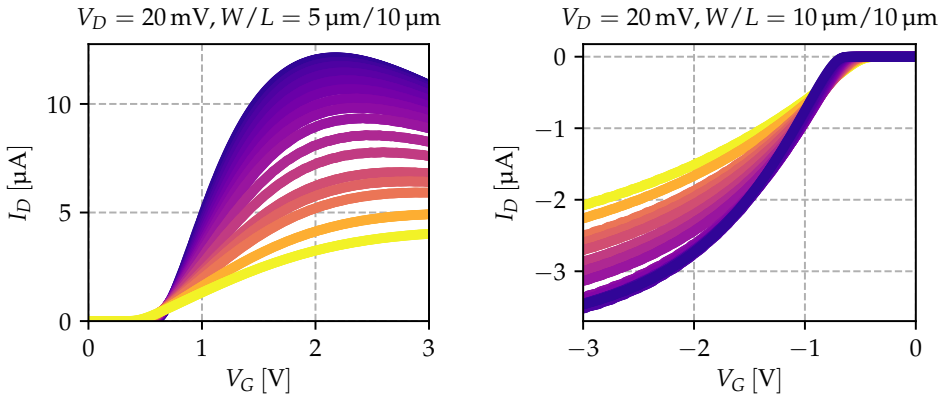
Figure 4.13.: Split-CV measurement: gate to channel capacitance per unit area C'_{GC} as a function of the gate voltage V_G , swept over temperature.

current I_D is proportional to u_{eff} and Q_i. In fig. 4.13a it can be seen that C'_{GC} approaches a constant value for V_G larger than around 0.8 V. Consequently, for these gate voltages Q_i becomes a linear function of V_G. Increasing the gate voltage thus leads to more charge in a linear relationship, but at the same time the mobility decreases. If this decrease overcompensates the increase in charge, the drain current can be smaller for higher gate voltages, leading to a negative transconductance.

4.5.3. Mobility model parameter extraction

The high transverse electric field mobility model introduced in section 2.3.2 (eq. 2.33) is used to reproduce the measured data. The model equation was put to Python code, and the set of parameters were extracted using the scipy [81] curve_fit function. Results of the fits can be seen in fig. 4.16 and a table showing the extracted parameter at the different temperatures is also provided in tab. 4.4.

The authors in ref. [37] state, that the model parameter n starts at values of around 2 at room temperature and approaches 3 in the cryogenic regime, which



(a) NMOS transistor

(b) PMOS transistor

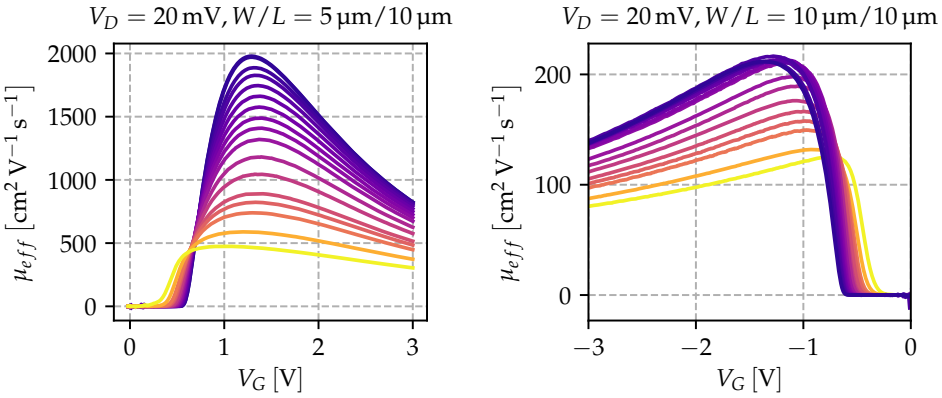
Figure 4.14.: Transfer characteristics of the NMOS and PMOS transistor at different temperatures.

is indeed also the case for the extracted values via fitting. Additionally, also the changes over temperature of the other three parameters, namely μ_{max}, V_t, θ, θ_2 appear continuous and with physical meaning. The lower the temperature: μ_{max} rises with an exponential trend, as reported in [37], V_t rises approximately linearly, and the two attenuation factors θ and θ_2 rise as well, as reported in [43].

With the given model it is indeed possible to reproduce the measured data with great accuracy. The temperature dependence of the extracted parameters agrees with the physical phenomena described in section 2.3 (e.g. rise of μ_{max} and V_t) and also the trends for the other parameters agree with the trends found in literature. It can be concluded, that a special parameter extraction methodology is not needed, as the parameters can be extracted as well with a simple fitting method. This is supported by the fact, that the extracted parameters change with temperature continuously. Finally, the same procedure was applied to the data for the PMOS transistor. A comparison of measurement data and fits can be found in fig. 4.17 and the extracted parameters can be found in the appendix 6.2.

Table 4.4.: Extracted parameter of the high electric field mobility model for different temperatures T. The extracted parameters correspond to the fits for the NMOS transistor presented in fig. 4.16.The parameter are introduced in section 2.3.2.

T [K]	μ_{max} $\left[\mathrm{cm^2\,V^{-1}\,s^{-1}}\right]$	n	V_t [V]	θ	θ_2
300	490	2.13	0.49	0.22	0.32
250	634	2.25	0.49	0.32	0.38
200	823	2.34	0.51	0.37	0.44
180	942	2.37	0.52	0.39	0.47
160	1042	2.38	0.52	0.39	0.49
140	1256	2.45	0.54	0.43	0.54
120	1453	2.48	0.55	0.46	0.57
100	1660	2.51	0.56	0.48	0.61
90	1801	2.52	0.57	0.47	0.63
80	1910	2.55	0.57	0.51	0.65
70	2042	2.56	0.58	0.52	0.66
60	2159	2.57	0.58	0.54	0.68
50	2237	2.61	0.59	0.63	0.70
40	2322	2.63	0.59	0.69	0.72
30	2351	2.66	0.60	0.79	0.73
20	2461	2.70	0.60	0.95	0.76
17	2470	2.68	0.60	0.95	0.76



(a) NMOS transistor

(b) PMOS transistor

Figure 4.15.: Effective mobility μ_{eff} versus gate voltage V_G, extracted with the split-CV method.

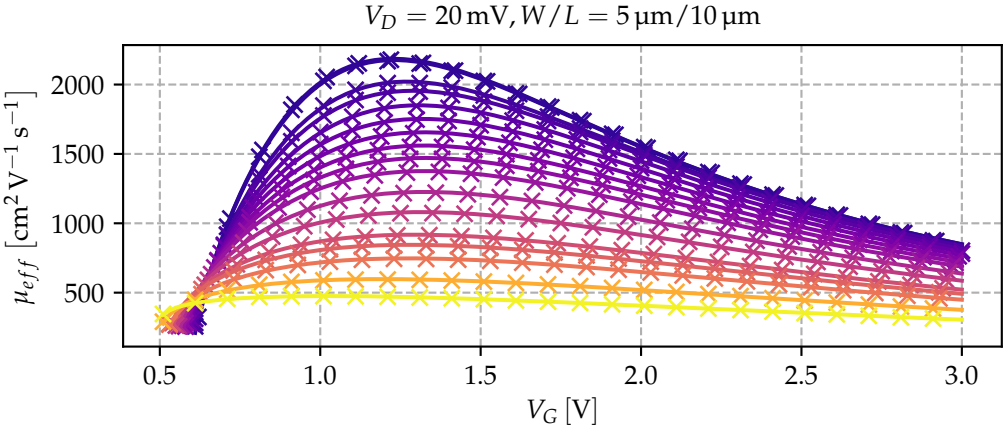


Figure 4.16.: Measured and modeled (solid line) mobility μ_{eff} of the NMOS transistor as a function of the gate voltage V_G for different temperatures. The mobility is modeled using the high electric field model, eq. 2.33. Just every 10th measurement point is shown to increase the readability. The extracted parameters corresponding to the curves presented in this plot can be found in tab. 4.4.

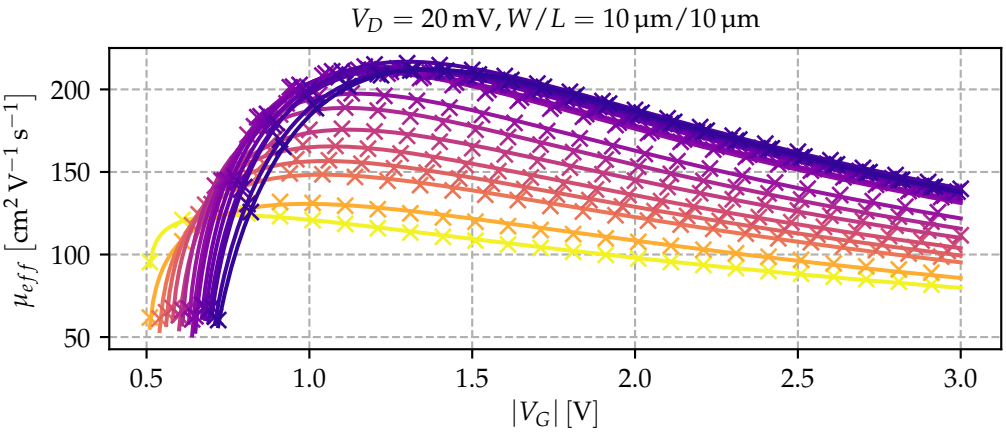


Figure 4.17.: Measured and modeled (solid line) mobility μ_{eff} of the PMOS transistor as a function of the gate voltage V_G for different temperatures. The mobility is modeled using the high electric field model, eq. 2.33. Just every 10th measurement point is shown to increase the readability. The extracted parameter corresponding to the curves presented in this plot can be found in tab. 6.2.

4.6. Digital transistors

Digital transistors with different width to length ratios were characterized at various temperatures. In this section extracted values for the threshold voltage V_t and the low-field mobility μ_0 for four different digital transistors are presented. However, modeling approaches for the measured current voltage characteristics are just performed on the analog transistors presented in the next section 4.7.

The index "hvt" refers to high threshold devices, where the threshold voltage is adjusted via additional "threshold voltage adjust implants". The low-field mobility μ_0 and the threshold voltage V_t of large digital transistors with a width to length ration (W / L) of 1.28 µm / 1.20 µm are extracted using the "Current-to-square-root-of-the-Transconductance Ratio"-method described by G. Ghibaudo in 1988 [82]. This method, valid in strong inversion in the linear region only, allows to determine μ_0 and V_t relying on a combined exploitation of a MOSFET transfer and transconductance characteristics. Figures showing the measured transfer characteristics can be seen in the appendix B.2. The applied drain voltage was $V_D = 50\,\mathrm{mV}$.

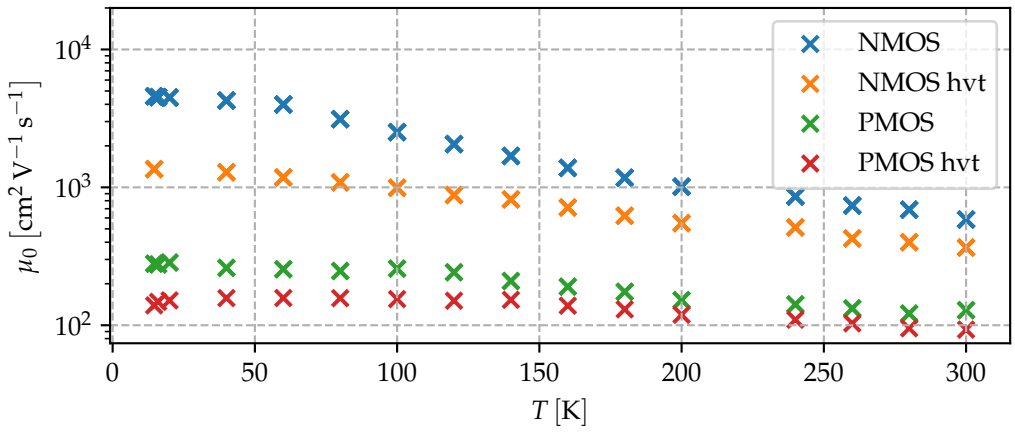


Figure 4.18.: Extracted low field mobility μ_0 versus temperature T for four different digital transistors.

As can be seen in fig. 4.19 the threshold voltage in the "hvt" devices is indeed

higher, than in the normal devices. The shift of the threshold voltage with temperature is comparable for all of the four transistors as indicated in fig. 4.20. According to fig. 4.18 it can be seen that the threshold voltage adjust implants tend to lower the low field mobility.

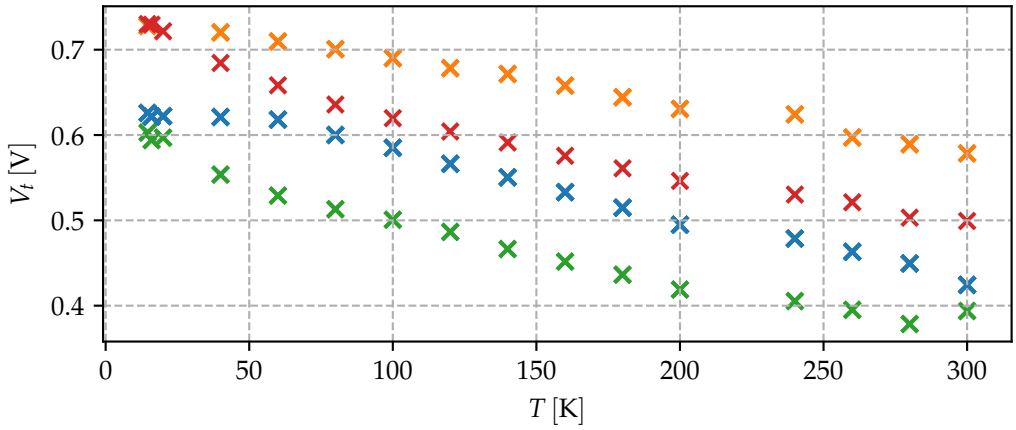


Figure 4.19.: Extracted threshold voltage V_t versus temperature T for four different digital transistors.Legend as in fig. 4.18

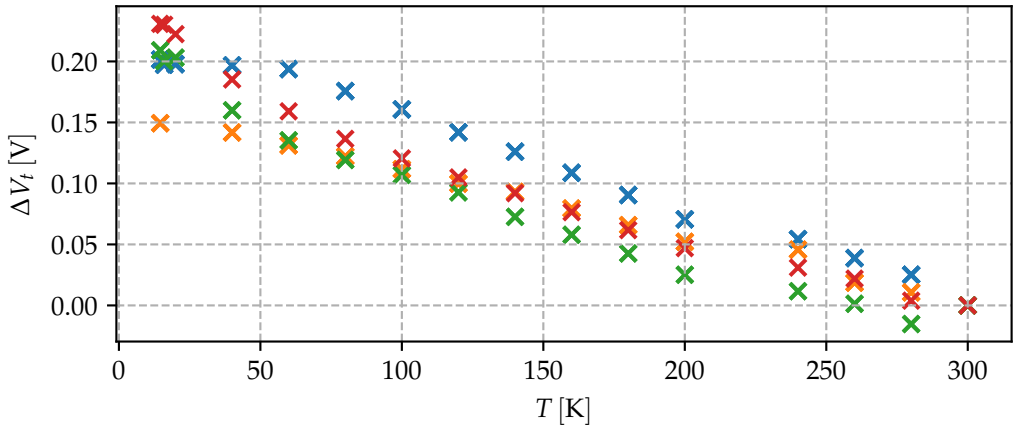


Figure 4.20.: Extracted $\Delta V_t = V_t(T) - V_t(T = 300\,\mathrm{K})$ versus temperature T for four different digital transistors.Legend as in fig. 4.18

Fig. 4.21 shows a comparison of the measured NMOS transistors with the

threshold voltage model presented in section 2.3.3. As can be seen, the additional implants in the "hvt" device has not just an impact on the value of the threshold voltage, but also on it's temperature dependence.

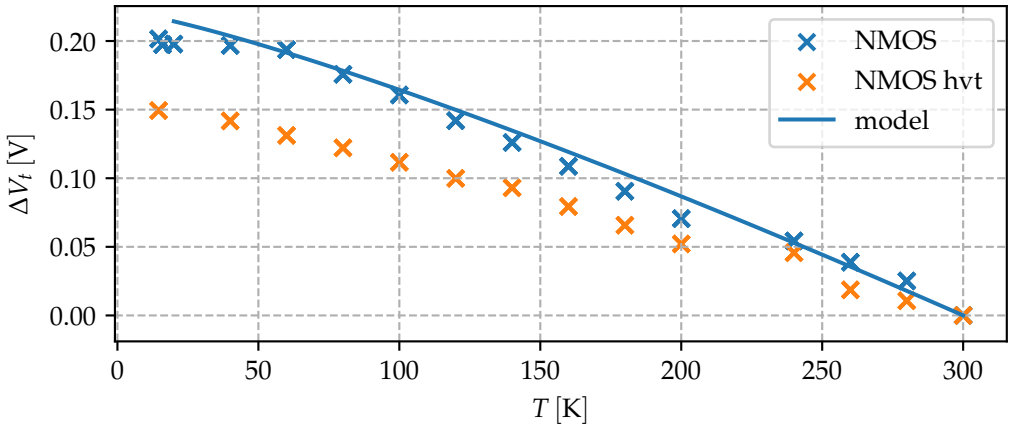


Figure 4.21.: Extracted $\Delta V_t = V_t(T) - V_t(T = 300\,\mathrm{K})$ versus temperature T for two digital NMOS transistors. Comparison to the threshold voltage model presented in section 2.3.3. The parameters used are: $C_{ox} = 10\,\mathrm{mF\,m^{-2}}$, $N_A = 1 \times 10^{22}\,\mathrm{m^{-3}}$.

4.7. Analog transistors

Analog transistor with various widths and lengths were characterized at different biasing conditions. Figures showing the measured transfer can be seen in the appendix B.3. Modeling approaches for these transistors are presented in section 5.
In this section extracted values for threshold voltage, mobility and subthreshold slope of two analog N- and P- MOS transistors with $W/L = 10\,\mu m/0.36\,\mu m$ and $W/L = 10\,\mu m/0.8\,\mu m$ are presented exemplarily. The threshold voltage is extracted using the "Current-to-square-root-of-the-Transconductance Ratio"-method and the "Linear Extrapolation" - method as described in ref. [83]. All of the transistors parameter are extracted using transfer characteristics with an applied drain voltage of $V_D = 20\,mV$, at different temperatures.

4.7.1. Threshold voltage

As pointed out in reference [83], different extraction methods and definitions can lead to different values of the extracted threshold voltage. This can be seen in fig. 4.24 and fig. 4.22: the two different extraction methods lead to different values of the threshold voltage. However, as can be confirmed in fig. 4.25 and fig. 4.23, the temperature dependence is similar in the extracted values for both methods.

In fig. 4.24 and fig. 4.22 it can be seen that the threshold voltage has a dependency on the transistor length L: the shorter transistors have lower threshold voltages. In general the dependence of the threshold voltage as a function of the channel length can be of any form (there can be a maximum in V_t versus L, such that there are regions where V_t is increasing with larger L, and also regions where V_t is decreasing with larger L, as for example shown in ref. [84]), depending on technology details.

It should be noted that in the threshold voltage model introduced in section 2.3.3 size dependent effects are not included and thus this length dependent shift in threshold voltage can not be reproduced with this model.

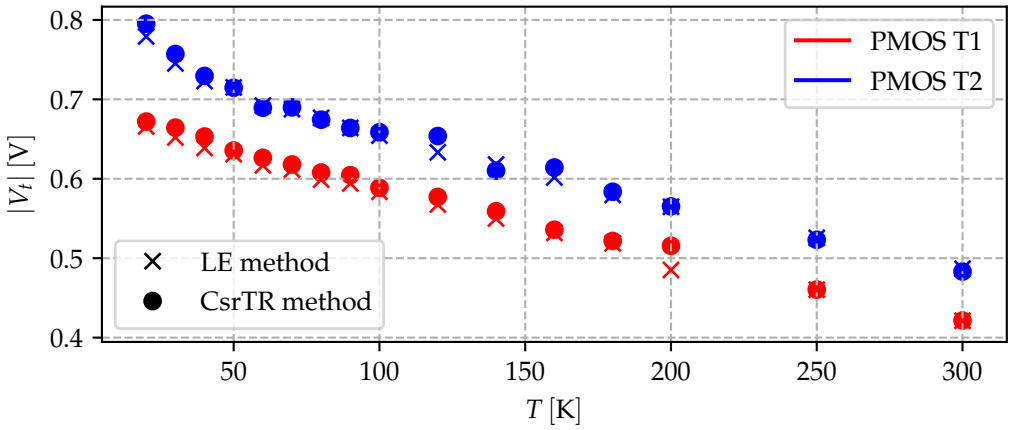


Figure 4.22.: Extracted threshold voltage V_t versus temperature T for two PMOS transistor (see tab. 6.3). V_t is extracted according to two different methods as described in [83]: CsrTR: "Current-to-square-root-of-the-Transconductance Ratio" - method, LE: Linear Extrapolation - method.

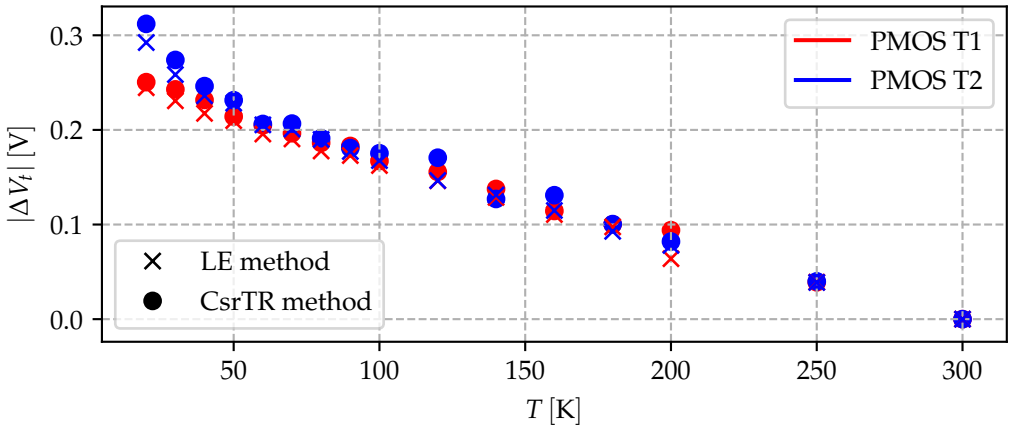


Figure 4.23.: Extracted $\Delta V_t = V_t(T) - V_t(T = 300\,\mathrm{K})$ versus temperature T for two PMOS transistor (see tab. 6.3). Legend as presented in fig. 4.24.

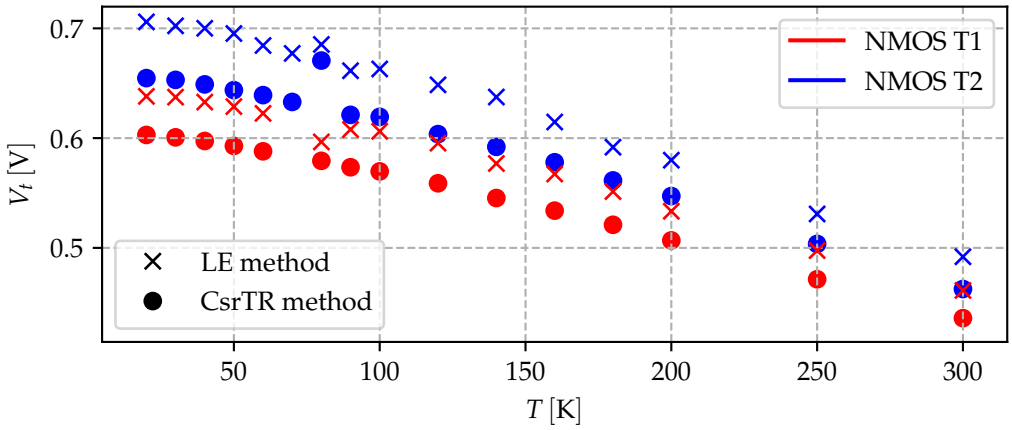


Figure 4.24.: Extracted threshold voltage V_t versus temperature T for two NMOS transistor (see tab. 6.3). V_t is extracted according to two different methods as described in [83]: CsrTR: "Current-to-square-root-of-the-Transconductance Ratio" - method, LE: Linear Extrapolation - method.

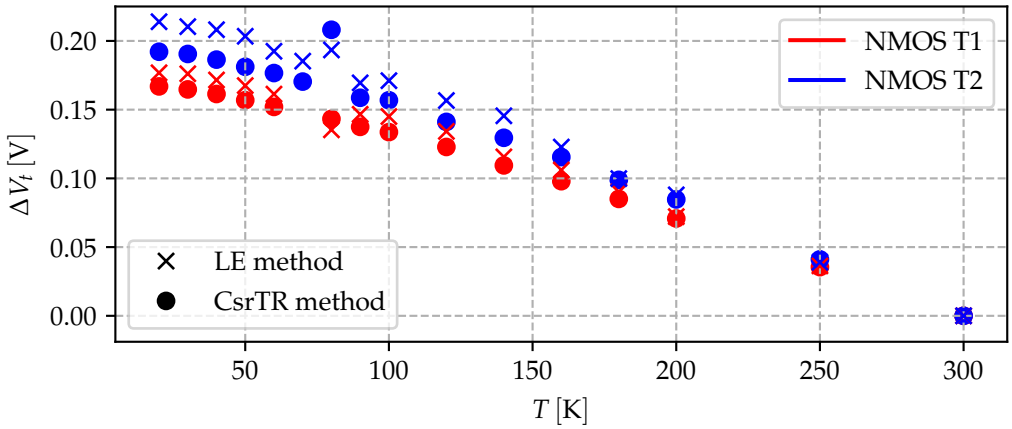


Figure 4.25.: Extracted $\Delta V_t = V_t(T) - V_t(T = 300\,\mathrm{K})$ versus temperature T for two NMOS transistor (see tab. 6.3). Legend as presented in fig. 4.24.

4.7.2. Mobility

The low field mobility μ_0 (often also referred to as "free carrier mobility" [85]) was extracted using the "CsrTR"- method. μ_0 in doped silicon is expected to have a bell-shaped trend as a function of temperature because of a change of the dominant scattering mechanism [86]. The maximum in mobility (as a function of temperature) was recently reported for a 28 nm FDSOI CMOS technology to be at around 10 K for NMOS transistors and around 80 K for PMOS transistors [18]. Measurement results as presented in fig. 4.26 and fig. 4.27 are comparable to those presented in the above cited reference, as also a maximum for the hole mobility is measured at around 70 K. The stated maximum at 10 K in the NMOS low field mobility can not be seen in fig. 4.27 as the values were just extracted to temperatures of 20 K. However, the curve shows the tendency towards a maximum, that could be located at around that temperature.

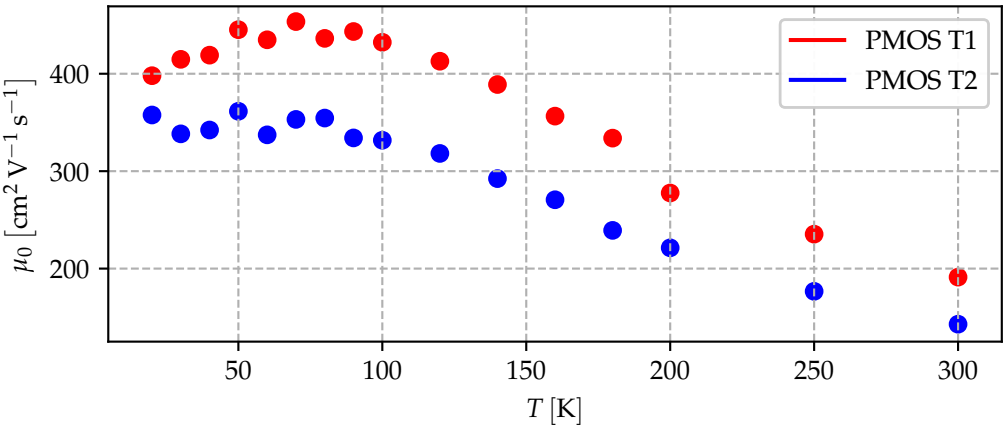


Figure 4.26.: Extracted low field mobility μ_0 versus temperature T for two PMOS transistor (see tab. 6.3).

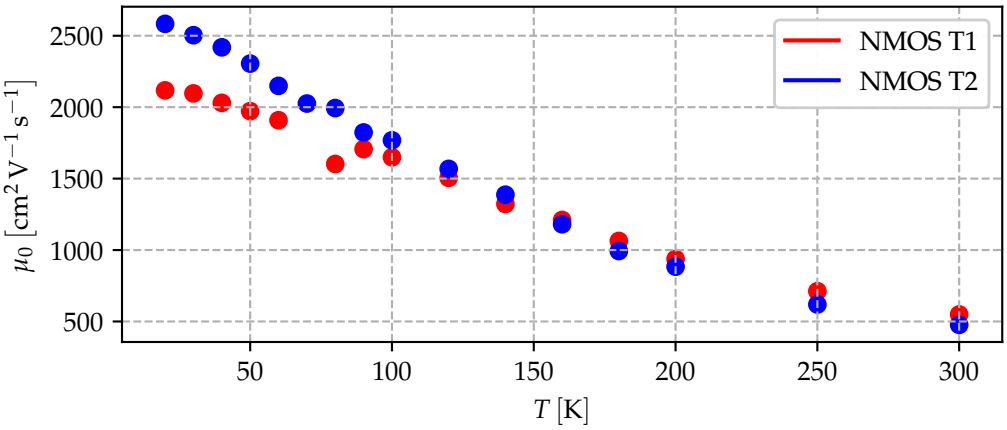


Figure 4.27.: Extracted low field mobility μ_0 versus temperature T for two NMOS transistor (see tab. 6.3).

4.7.3. Subthreshold slope

The subthreshold swing was extracted via performing linear fits in the subthreshold region of the measured transfer characteristics. As can be seen in fig. 4.28 and fig. 4.29 the subthreshold slope seems to be independent on the transistor size. In these figures also Boltzmann thermal limit is shown, multiplied with a slope factor m of 1.18 (see section 2.3.4 for details). It can be seen that the extracted values follow this theoretical line till temperatures of about 100 K and start to deviate for temperatures below. This deviations from S at low temperatures as well as the extracted value for m agree with measurements presented in recent literature [87] [88].

Bohuslavskyi et al. demonstrated recently that band tail states lead to a saturation of the subthreshold slope at low temperatures [17]. Beckers et al. were able to model the subthreshold slope as a function of temperature using Fermi Dirac statistics and band tail states [89].

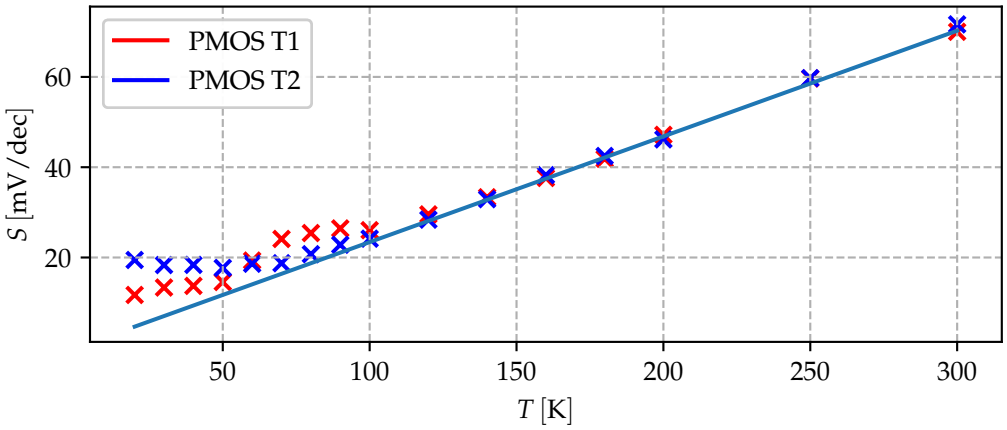


Figure 4.28.: Extracted subthreshold slope S versus temperature T for two PMOS transistor. Solid line: Boltzmann thermal limit (see eq. 2.37) multiplied with $m = 1.18$.

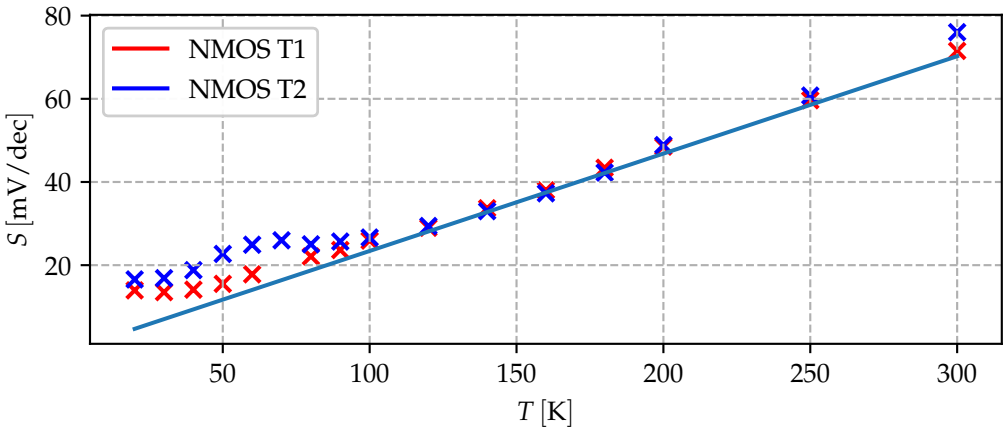


Figure 4.29.: Extracted subthreshold slope S versus temperature T for two NMOS transistor. Solid line: Boltzmann thermal limit (see eq. 2.37) multiplied with $m = 1.18$.

5. Transistor modeling

In this chapter two main approaches to model the measured data of the analog transistors are presented.

5.1. Simplified EKV model

The simplified EKV model [90] [91] is, as the name suggests, a simplified version of the charge-based Enz–Krummenacher–Vittoz (EKV) - model [92]. The model is just valid in saturation and is "simple" in the sense, that it just has four (or even just three in the case of the long channel model) parameters: the slope factor n, the specific current per square $I_{spec\square}$, the threshold voltage V_{T0} and the velocity saturation parameter L_{sat}. The latter is introduced to describe short channel effects, and can thus be set to zero for large transistors.

The different region of operation (weak, moderate and strong inversion) within this model can be distinguished with the introduction of the inversion coefficient IC, which is defined as [92]:

$$IC = \frac{I_D}{I_{spec\square} W/L}, \tag{5.1}$$

where I_D, W and L are the drain current in saturation and the width and length of the MOS device. The value of IC is related to the region of operation via [90] [91]:

$$\begin{aligned} IC &\leqslant 0.1 : \text{weak inversion} \\ 0.1 \leqslant IC &\leqslant 10 : \text{moderate inversion} \\ 10 &\leqslant IC : \text{strong inversion.} \end{aligned} \tag{5.2}$$

5.1.1. Long-channel simplified EKV model

In the long channel simplified EKV model the gate voltage V_G is computed, given the above introduced parameters n, $I_{spec\square}$ and V_{T0} and a value of IC via:

$$V_G = n\phi_t(\log\sqrt{4IC+1} - 1 + \sqrt{4IC+1} - (1+\log 2) + \frac{V_S}{\phi_T}) + V_{T0}. \quad (5.3)$$

5.1.2. Short-channel simplified EKV model

In the short channel simplified EKV model the additional velocity saturation parameter L_{sat} is introduced. IC is related to the normalized inversion charge at the source q_s via [90] [91]:

$$IC = \frac{4(q_s^2 + q_s)}{2 + \lambda_c + \sqrt{4(1+\lambda_c) + (\lambda_c(1+2q_s))^2}}, \quad (5.4)$$

where λ_c is related to the velocity saturation parameter L_{sat} via:

$$\lambda_c = \frac{L_{sat}}{L}. \quad (5.5)$$

For a given set of parameters one can calculate the gate voltage V_G for a given drain current I_D (and thus IC) and source voltage V_S via implicitly solving eq. 5.4 for q_s and then computing V_G via [18]:

$$V_G = n\phi_t(\log q_s + 2q_s + V_S/\phi_t) + V_{T0}. \quad (5.6)$$

It should be noted that the short-channel simplified EKV model is numerically more expensive than its long-channel counterpart, not only because of the additional parameter L_{sat}, but also because for computing V_G given I_D an implicit equation (eq. 5.4) needs to be solved, whilst in the long channel model this calculation can be performed explicitly (eq. 5.3).

5.1.3. Fitting results

The equations as presented in the previous subsections were put into python code, and the introduced parameters were fitted to match the measured curves as best as possible. Fitting is done using the scipy [81] curve_fit function.

Wide transistor

In this section results from fitting performed on a large and wide ($W = L = 10\,\mu m$, NMOS T3 according to tab. 6.3) NMOS transistor are presented. It should be once more noted that the simplified EKV model just works in saturation and therefore fitting approaches are just made for drain to source voltages $V_D \geq 0.4\,V$, as can be seen in the output characteristic in the appendix (fig. 6.12), this voltage level is high enough to ensure being in the saturation regime for the whole temperature range.

Results for this fits for various temperatures in the range 17 K to 300 K can be seen in fig. 5.2 for two different drain biases. The measured drain current I_D as a function of the gate voltage V_G is independent of the drain voltage V_D in the saturation regime, which can be also seen in fig. 5.2. The modeled curves can reproduce the measurement with great accuracy even down to 17 K. The extracted parameters for the plots presented in fig. 5.2 are shown in tab. 5.1, an extended table with additional temperatures can be found in appendix 6.4.

Although the transistor is wide and large, both models (the short channel as well as the long channel simplified EKV model) were fitted to test whether fitting with the additional parameter L_{sat} influences the results on the other parameters. As can be seen in tab. 5.1 for both models the extracted parameter are the same with great accuracy, and the extracted value for L_{sat} tends to be very small. The very small values of L_{sat} do not visibly change the model curves, as both models are overlying for the whole temperature range in fig. 5.2.

Fig. 5.1 shows a plot of the extracted parameters over temperature.

The same procedure was applied to fit measured data from PMOS transistors. A comparison between fits and measurement data is shown in fig. 5.3 and the extracted parameters can be found in the appendix 6.5. Also for the long channel

Table 5.1.: Fitted parameter of the simplified EKV model, on a NMOS transistor with $W = L = 10\,\mu m$. The applied drain voltage was $V_D = 1\,V$, and plots of the fits can be seen in fig. 5.2b. The long channel model has no parameter L_{sat}. A table showing fitting results at additional temperatures can be found in the appendix 6.4.

T	model type	$I_{spec\square}$ [nA]	n [1]	V_{T0} [V]	L_{sat} [nm]
17	long	189.293	7.116	0.600	NAN
	short	189.293	7.116	0.600	2.6E-14
50	long	203.911	2.737	0.581	NAN
	short	203.910	2.737	0.581	1.5E-07
100	long	277.114	1.760	0.553	NAN
	short	277.114	1.760	0.553	8.0E-05
160	long	315.362	1.393	0.517	NAN
	short	314.591	1.392	0.517	1.0E-01
200	long	338.677	1.276	0.492	NAN
	short	338.550	1.276	0.492	9.9E-02
250	long	371.814	1.215	0.461	NAN
	short	371.813	1.215	0.461	1.0E-07
300	long	408.290	1.191	0.430	NAN
	short	408.361	1.192	0.430	9.6E-02

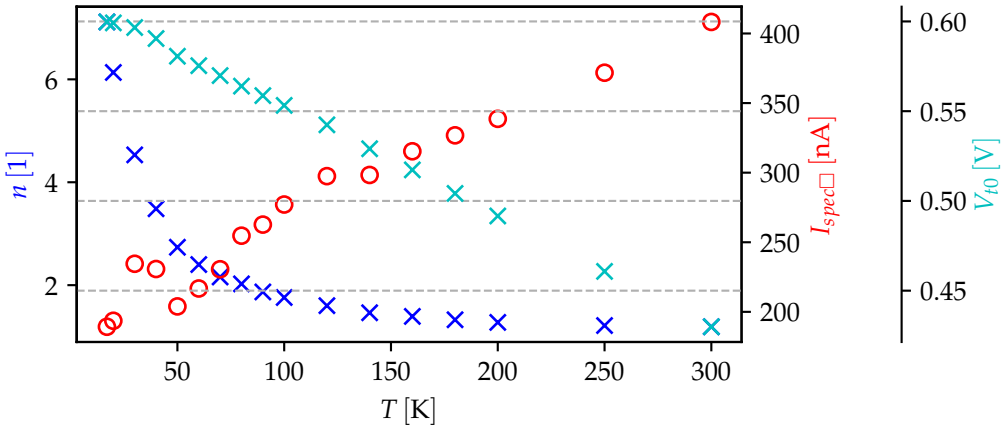
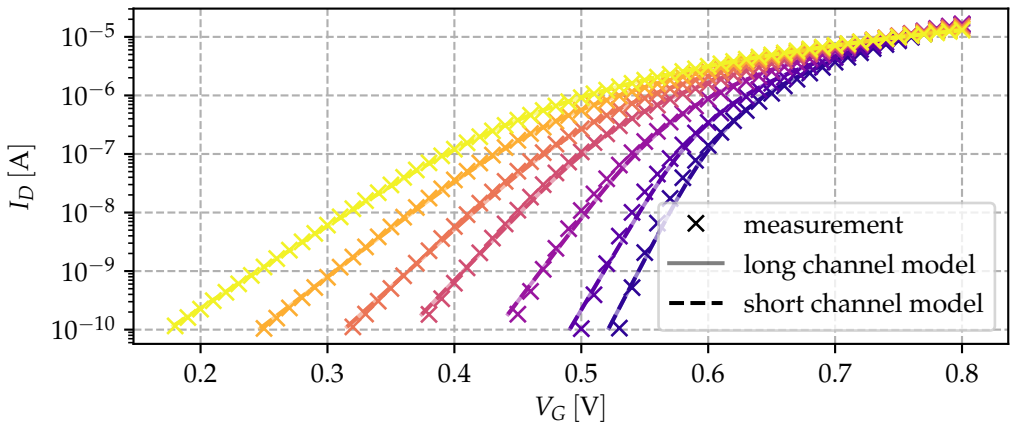
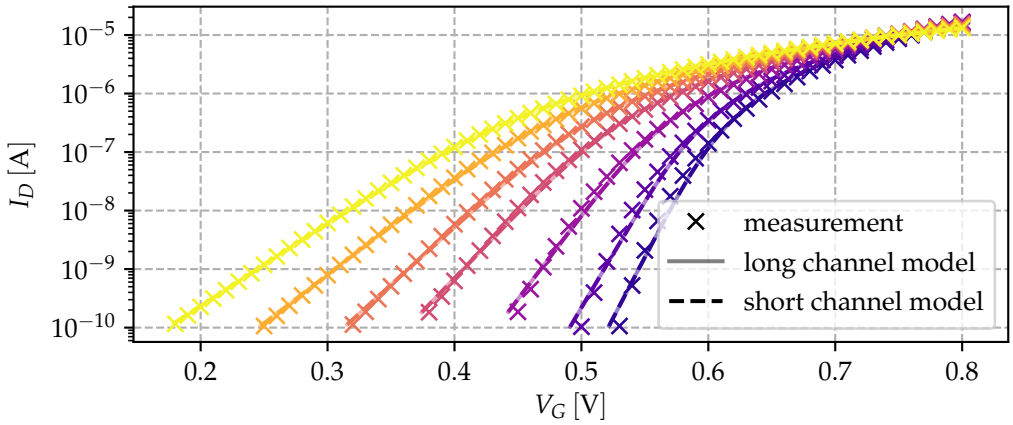


Figure 5.1.: Plot of the extracted parameter of the long channel simplified EKV model for a long NMOS transistor. Data of this plot can be found in the appendix 6.4.

PMOS transistor the measured data can be reproduced with the simplified EKV model with great accuracy.



(a) $V_D = 0.4\,\mathrm{V}$



(b) $V_D = 1.0\,\mathrm{V}$

Figure 5.2.: Simplified EKV model versus measurement data for a NMOS transistor biased with two different drain voltages V_D in accumulation.The temperatures according to the lines from left to right are: 17 K,50 K,100 K,160 K,200 K,250 K and 300 K. Transistor length and width are $W = L = 10\,\mu\mathrm{m}$. Source and bulk voltage were kept at zero volts: $V_S = V_B = 0\,\mathrm{V}$.

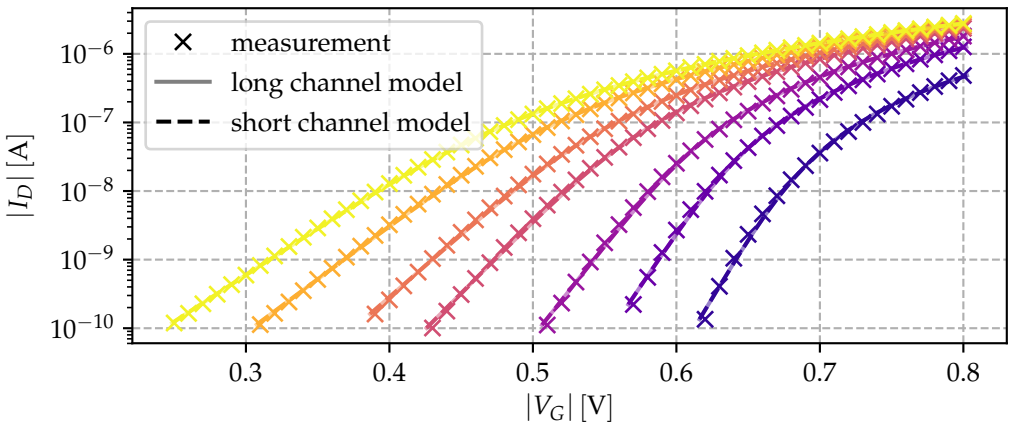


Figure 5.3.: Simplified EKV model versus measurement data for a PMOS transistor biased with a drain voltage of $V_D = -1\,\mathrm{V}$.The temperatures according to the lines from left to right are: 20 K,60 K,100 K,160 K,200 K,250 K and 300 K. Transistor length and width are $W = L = 10\,\mu\mathrm{m}$. Source and bulk voltage were kept at zero volts: $V_S = V_B = 0\,\mathrm{V}$.

Short transistor

In this subsection fitting results for a short transistor ($W = 10\,\mu m$, $L = 0.36\,\mu m$, NMOS T1 according to tab. 6.3) are presented. When performing fitting it turned out, that the parameter of the short and and long transistor model were not fitted to the same value, but instead a tradeoff mainly between the $I_{spec\square}$ and L_{sat} parameter can be seen. A table showing this fitting results can be found in the appendix 6.6.

However, for fitting this short transistor with the simplified EKV model a different approach was chosen. The fit with the short channel model is made for n and V_{t0} but with a fixed value of $I_{spec\square}$ that was extracted on the long channel transitor in the previous section. This approach was chosen, since $I_{spec\square}$ is considered a parameter independent of dimensions [90]. Plots showing measured and modeled curves are presented in fig. 5.4 and a plot of the fitted parameter over temperature can be seen in fig. 5.5.

Plots and data for a short PMOS transistor can be found in the appendix 6.8, 6.16 and 6.17.

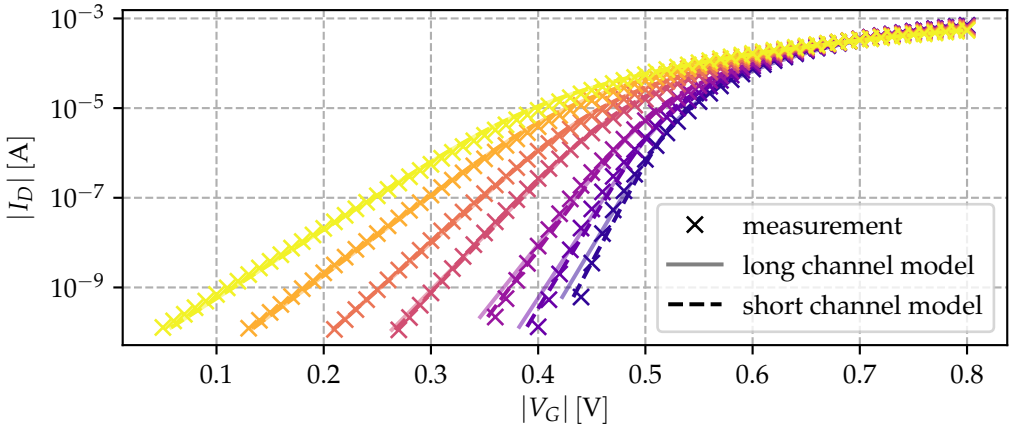


Figure 5.4.: Simplified EKV model versus measurement data for a NMOS transistor biased with a drain voltage of $V_D = 1\,V$.The temperatures according to the lines from left to right are: 17 K,60 K,100 K,160 K,200 K,250 K and 300 K. Transistor length and width are $W = 10\,\mu m$, $L = 0.36\,\mu m$. Source and bulk voltage were kept at zero volts: $V_S = V_B = 0\,V$.

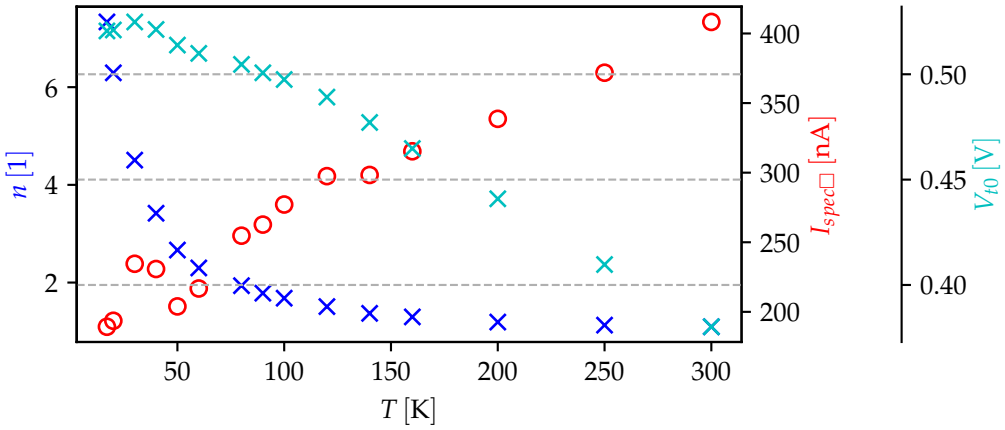


Figure 5.5.: Plot of the extracted parameter of the short channel simplified EKV model for a short NMOS transistor. Data of this plot can be found in the appendix 6.4.

5.1.4. Discussion

In this section it was shown that the simplified EKV model is indeed capable of modeling measured transfer characteristics even down to cryogenic temperatures. However, it should be noted that the authors of the model suggest a parameter extraction methodology [90] instead of fitting the parameters to the measured curves. This extraction methodology requires biasing the MOSFETs to higher gate voltages than it was done in the measurement presented in this thesis. It can be seen that the simpler long channel model is sufficient to model the measured curves, as the extracted value for the parameter L_{sat} are very small, and both model fit to the data very well.

The main purpose of introducing the simplified EKV model in this thesis, is to show, that there is indeed the possibility to model transfer characteristics even at cryogenic conditions. However, the main drawback of this model is it's restriction to the saturation regime.

5.2. Physics based developed model

General transistor relations and cryogenic effects, as described in chapter 2 were put into Python code. The repository ("pm-mos-model") can be freely downloaded on github[1].

This section describes the parameter of the Python model and how quantities are computed and consists of the following subsections : Bulk Boltzmann model, Bulk Fermi-Dirac model, QV Boltzmann model, QV Fermi-Dirac model and IV model.

All of the introduced parameters refer to silicon as the bulk material and a NMOS transistor, however they can be easily changed to model different materials as well as a PMOS transistor.

5.2.1. Bulk Boltzmann model

In this subsection parameters and formulas of the bulk python class are presented. Three main parameter should be set by the user of the code: the doping concentrations N_A and N_D and the temperature T. The set of other parameters (E_g, g_A, g_D, E_A, E_D, N_c, N_v, χ) is initialized with default values for a silicon bulk semiconductor with Phosphorus atoms as donors and Boron atoms as acceptors.

Bandgap, valence and conduction band

The temperature dependence of the bandgap E_g is modeled as described in section 2.1.1. The conduction band E_c is set with reference to the valence band E_v:

$$E_c = E_v + E_g \tag{5.7}$$

[1] `https://github.com/michi7x7/pm-mos-model`

Electron affinity

The electron affinity χ relates to the semiconductor work function ϕ_s via [20]:

$$\phi_s = \chi + \frac{E_c - E_i}{e} + \phi_f. \tag{5.8}$$

The default value of χ is set to:

$$\chi = 4.05\,\mathrm{eV}, \tag{5.9}$$

which is taken from reference [20].

Effective density of states

The temperature dependence of effective density of states (N_c and N_v) is modeled as described in section 2.1.2.

Donor and acceptor energy level

The donor and acceptor energy levels (E_D and E_A) describe the energy that is needed to ionize an dopant atom. Usually these energies lie within the bandgap and their energies are given as energetic distance to the conduction (valence) band E_c (E_v). For silicon, assuming Phosphorus atoms as donors and Boron atoms as acceptors, the following default values are taken for computations [93]:

$$\text{Phosphorus: } E_D = E_c - 45\,\mathrm{meV}, \tag{5.10}$$

$$\text{Boron: } E_A = E_v + 44\,\mathrm{meV}. \tag{5.11}$$

This energetic distances to the conduction (valence) band are assumed temperature independent.

Donor- and acceptor-site degeneracy factor

The donor- and acceptor-site degeneracy factor (g_D and g_A) are per default set to:

$$\begin{aligned} g_D &= 2 \\ g_A &= 4. \end{aligned} \tag{5.12}$$

These values are standard values for silicon [28]. It should be noted that setting g_D and g_A to zero corresponds to assuming always complete ionization as in this case $N_D = N_D^+$ and $N_A = N_A^-$ (see eq. 2.13). Thus initiating an instance of the bulk class with $g_D = g_A = 0$ allows for computing properties with the assumption of complete ionization.

Calculation of the bulk Fermi level

The introduction of the constants and parameters in the previous subsections allows the computation of the Fermi energy in the bulk $E_{f,b}$ of the transistor, requiring charge neutrality (see eq. 2.12). In the bulk Boltzmann model this computation is performed using Boltzmann statistics, as described in section 2.1.3.

5.2.2. Bulk Fermi-Dirac model

In the Fermi-Dirac Bulk model charge carriers are computed using Fermi Dirac integrals [20]:

$$n = \int_{E_c}^{\infty} f(E) D_c(E) dE, \tag{5.13}$$

where $f(E)$ is the Fermi function:

$$f(E) = \frac{1}{1 + \exp\left(\frac{E - E_f}{k_\mathrm{B} T}\right)}, \tag{5.14}$$

and $D_c(E)$ the density of states in the conduction band. $D_c(E)$ is linked to the effective density of states in the conduction band N_c via:

$$D_c(E) = \frac{2}{\sqrt{\pi}} \frac{N_c}{(k_\mathrm{B} T)^{3/2}} \sqrt{E - E_c}. \tag{5.15}$$

Analogously the concentration of holes is computed via [20]:

$$p = \int_{-\infty}^{E_v} (1 - f(E)) D_v(E) dE, \tag{5.16}$$

where the density of states in the valence band $D_c(E)$ is linked to the effective density of states in the valence band N_v via:

$$D_v(E) = \frac{2}{\sqrt{\pi}} \frac{N_v}{(k_\mathrm{B}T)^{3/2}} \sqrt{E_v - E}. \tag{5.17}$$

The integrals in eq. 5.13 and eq. 5.16 can not be solved analytically. The Fermi level is computed as described in section 2.1.3, via the charge neutrality condition.

5.2.3. QV Boltzmann model

The QV-model allows the computation of the surface potential ψ_s, the mobile charge in the channel Q_I, the immobile bulk charge Q_B, the semiconductor charge Q_C and the interface trap charge Q_{it}. These quantities were introduced in section 2.2.1.

It should be noted, that all of the energies and potentials in the python model are linked to the Fermi energy E_f. In this convention the surface potential ψ_s is defined as:

$$\psi_s = \frac{E_f - E_{i,s}}{e}, \tag{5.18}$$

and the intrinsic energy in the bulk $E_{i,b}$ is linked to a bulk potential ψ_b:

$$\psi_b = \frac{E_f - E_{i,b}}{e}. \tag{5.19}$$

This convention is adopted from reference [19].

In the QV- model additional parameters are introduced: C_{ox}, N_{it}, ψ_t, g_t, Q_0, ϕ_m.

Interface traps

Interface traps are included in the python model via the three parameters N_{it}, ψ_t and g_{it}. Each of them can be a list with N entries. The implementation allows to set discrete trap levels with an energy $E_{t,j}$, linked to the potential $\psi_{t,j}$ via:

$$\psi_{t,j} = \frac{E_{t,j} - E_i}{e}. \tag{5.20}$$

The number of traps at each of this level with energy E_j is $N_{it,j}$. The occupation factor, given in eq. 2.39, can be written in terms of the surface potential ψ_s and the trap potential $\psi_{t,j}$:

$$f_{it}(\psi_{t,j}, \psi_s) = \frac{1}{1 + g_{it} \exp\left((\psi_{t,j} - (\psi_s - V_{ch}))/(\phi_t)\right)}, \tag{5.21}$$

where the channel voltage V_{ch} describes the non equilibrium shift for the electron potential in the presence of a drain to source voltage V_{DS} as described in section 2.2.2.

Finally, the interface trap voltage V_{it} can be written as:

$$V_{it}(\psi_s) = \frac{-q}{C_{ox}} \sum_{j=1}^{N} N_{it,j} f_{it}(\psi_{t,j}, \psi_s). \tag{5.22}$$

A plot of V_{it} versus ψ_s for three different temperatures can be seen in fig. 5.6. The temperature enters V_{it} via ϕ_t in the occupation factor in eq. 5.21, the lower the temperature the lower ϕ_t and thus the sharper the switching from zero to full occupation.

Electric field at the surface

The electric field at the semiconductor oxide interface $\mathcal{E}_s$ can be computed via solving Poisson equation (see eq. 2.22). Assuming $N_A >> N_D$ the Poisson equation can be written in terms of the surface potential as:

$$\frac{\partial^2 \psi(y)}{\partial y^2} = \frac{e}{\epsilon_{si}} \left(n_i \exp\left(\frac{\psi - V_{ch}}{\phi_t}\right) - n_i \exp\left(\frac{-\psi}{\phi_t}\right) - N_A^- \right), \tag{5.23}$$

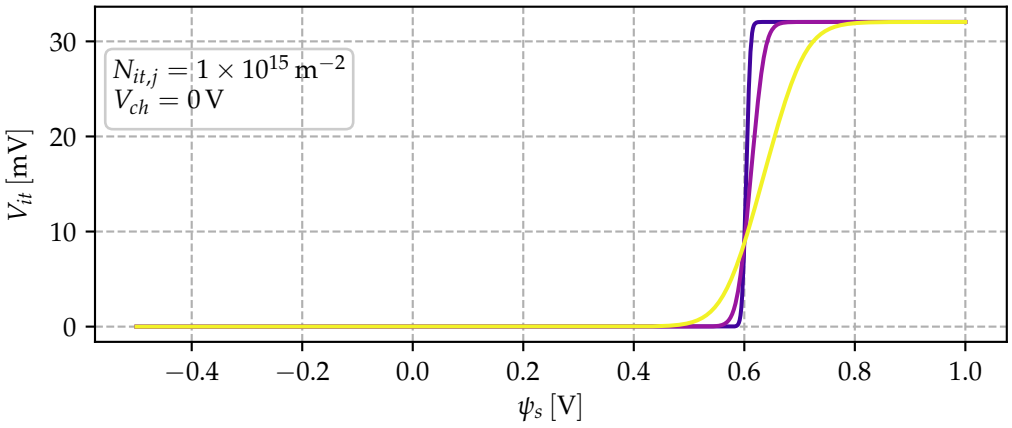


Figure 5.6.: Plot of V_{it} versus ψ_s for three different temperatures: 30 K, 100 K, 300 K. Five arbitrary trap potentials $\psi_{it,j}$ were chosen: $\psi_{it} = [0.58\,\mathrm{eV} - 2\phi_t, 0.58\,\mathrm{eV} - 1\phi_t, 0.58\,\mathrm{eV}, 0.58\,\mathrm{eV} + 1\phi_t, 0.58\,\mathrm{eV} + 2\phi_t]$.

where the potential ψ is defined with reference to E_i:

$$\psi(y) = \frac{E_f - E_i(y)}{e}. \tag{5.24}$$

An analytic solution to eq. 5.23 can be found right at the surface $y = 0$ [19]:

$$\mathcal{E}_s^2 = \frac{2en_i\phi_t}{\epsilon_{si}}\left(\exp\left(\frac{\psi_s - V_{ch}}{\phi_t}\right) - \exp\left(\frac{\psi_b - V_{ch}}{\phi_t}\right) + \exp\left(\frac{-\psi_s}{\phi_t}\right) - \exp\left(\frac{-\psi_b}{\phi_t}\right)\right) + \frac{2eN_A}{\epsilon_{si}}\left(\psi_s - \psi_b - \phi_t \log\left(\frac{1 + g_A \exp\frac{\psi_A - \psi_b}{\phi_t}}{1 + g_A \exp\frac{\psi_A - (\psi_s - \psi_b)}{\phi_t}}\right)\right) \tag{5.25}$$

The solution can be obtained in the same manner as eq. 2.22 is solved (shown in the appendix A.3), the only difference is the inclusion of incomplete ionization, which leads to the last term containing the logarithm. This term becomes 0 in the case of complete ionization since then $g_A = 0$. Apart from that term and the fact that N_D was assumed to be neglectable small compared to N_A, the two solutions (eq. 5.25 and eq. 6.11) are identical, if the different definitions of the surface potential are considered (compare definition of ψ_s eq. 5.18 with

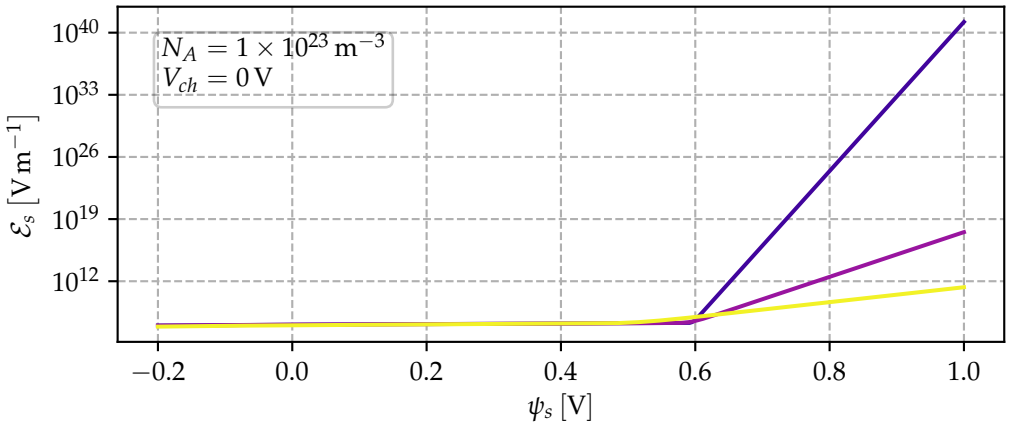


Figure 5.7.: Plot of $\mathcal{E}_s$ versus ψ_s for three different temperatures: 30 K, 100 K, 300 K.

definition eq. 2.15). A plot of $\mathcal{E}_s$versus ψ_s for three different temperatures can be seen in fig. 5.7.

Potential loop equation

The potential loop equation, as introduced in section 2.2.1, is solved to link the gate to bulk voltage V_{GB} to a surface potential ψ_s. This equation (eq. 2.14), considering that $\psi_{ox} = (\epsilon_{si}\mathcal{E}_s + Q_0)/C_{ox}$ and considering the interface trap voltage ψ_{it}, can be written as :

$$V_{GB} = (\psi_s - \psi_b) + \phi_{ms} + \epsilon_{si}\mathcal{E}_s(\psi_s)/C_{ox} + Q_0/C_{ox} + V_{it}(\psi_s). \tag{5.26}$$

Eq. 5.26 is solved implicitly for a given value of V_{GB} and V_{ch} to get ψ_s. Fig. 5.8 shows a plot of ψ_s versus the gate voltage V_G. For each of the shown temperatures ψ_s is one time computed with interface traps and one time without. As can be seen in the figure, interface traps slightly influence the surface potential.

Furthermore, being able to calculate $\psi_s(V_{GB}, V_{ch})$ allows the calculation of the semiconductor charge Q_C, the immobile, fixed charge Q_B and the mobile inversion charge Q_I as presented in the next subsection.

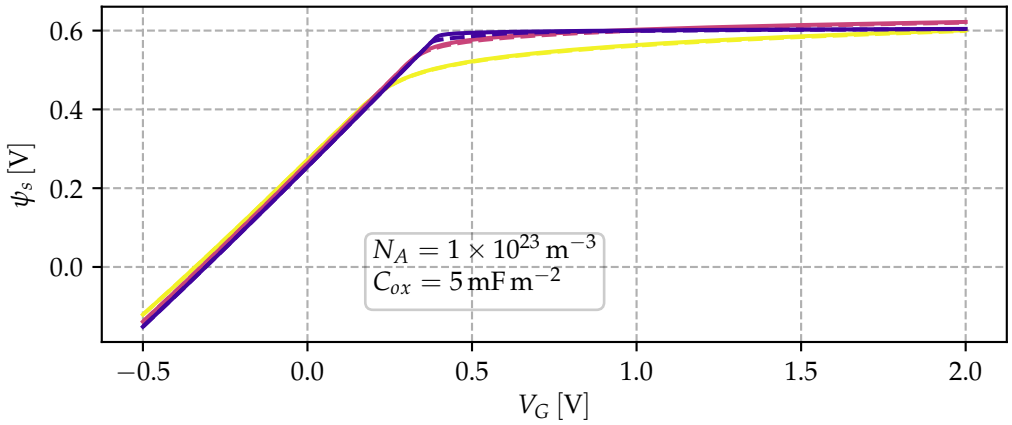


Figure 5.8.: Plot of ψ_s versus V_G for three different temperatures: 30 K, 100 K, 300 K. For each temperature two lines are plotted. Solid lines: no interface traps, dashed lines: interface traps with the parameters given in fig. 5.6.

Computing charges

Q_C can be computed with the help of the electric field at the semiconductor oxide interface $\mathcal{E}_s$:

$$Q_C = \frac{\epsilon_{si}\mathcal{E}_s}{C_{ox}}, \tag{5.27}$$

where $\mathcal{E}_s$ is given in eq. 5.25. Q_B is computed using the charge sheet and depletion approximation (derivation see appendix A.8):

$$Q_B = -\epsilon_{si}\sqrt{\frac{2eN_A(\psi_s-\psi_b)}{\epsilon_{si}} - \frac{2eN_A\phi_t}{\epsilon_{si}}\phi_t \log\left(\frac{1+g_A\exp\frac{\psi_A-\psi_b}{\phi_t}}{1+g_A\exp\frac{\psi_A-(\psi_s-\psi_b)}{\phi_t}}\right)}, \tag{5.28}$$

and finally Q_I is computed via eq. 2.24:

$$Q_I = Q_C - Q_B. \tag{5.29}$$

Plots of the charges Q_I, Q_C and Q_B can be found in fig. 5.9, 5.10 and 5.11, respectively.

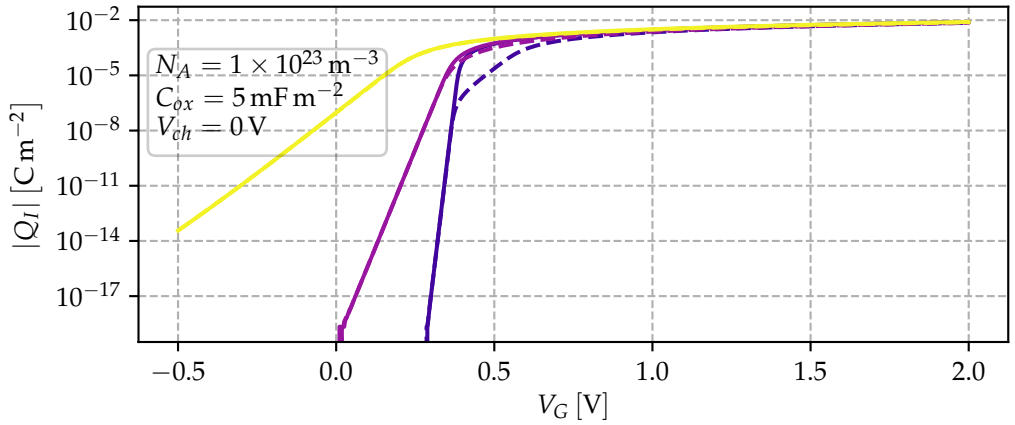


Figure 5.9.: Plot of Q_I versus V_G for three different temperatures: 30 K, 100 K, 300 K. For each temperature two lines are plotted. Solid lines: no interface traps, dashed lines: interface traps with the parameters given in fig. 5.6.

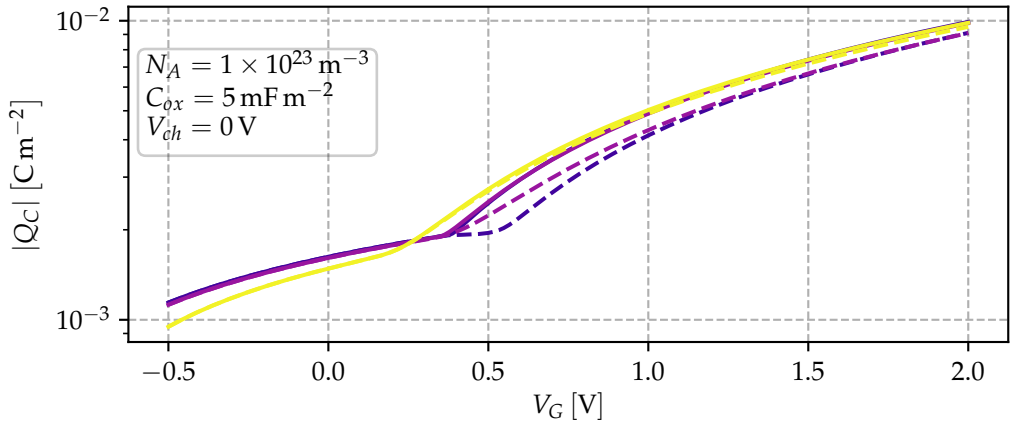


Figure 5.10.: Plot of Q_C versus V_G for three different temperatures: 30 K, 100 K, 300 K. For each temperature two lines are plotted. Solid lines: no interface traps, dashed lines: interface traps with the parameters given in fig. 5.6.

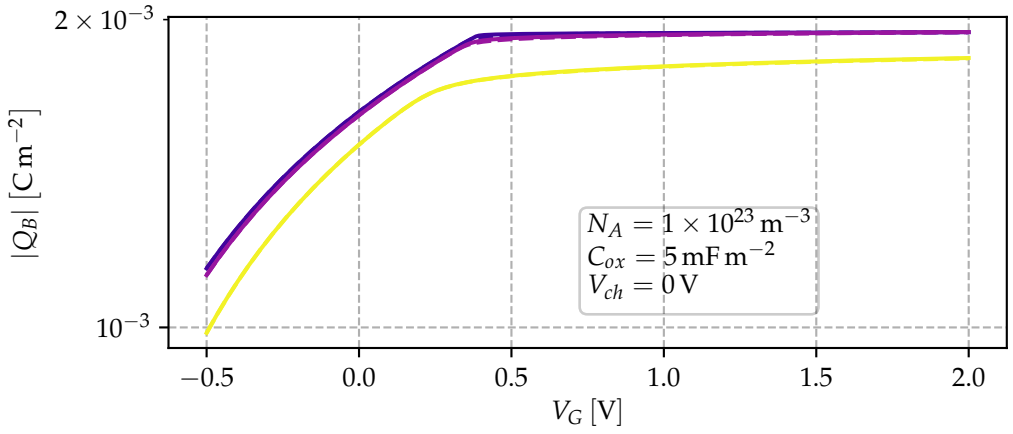


Figure 5.11.: Plot of Q_I versus V_G for three different temperatures: 30 K, 100 K, 300 K. For each temperature two lines are plotted. Solid lines: no interface traps, dashed lines: interface traps with the parameters given in fig. 5.6.

5.2.4. QV Fermi-Dirac model

Using Fermi-Dirac integrals to calculate charge carrier concentrations n and p affects the calculation of $\mathcal{E}_s$, any other quantity is calculated as presented in the previous section.

If the charge carriers are computed with Fermi-Dirac integrals Poisson equation can be written as ($N_A >> N_D$ is assumed):

$$\frac{\partial^2\psi(y)}{\partial y^2} = \frac{e}{\epsilon_{si}}\left(-\int_{E_c}^{\infty}\frac{1}{1+\exp\left(\frac{E-e\psi-E_i}{k_B T}\right)}D_c(E)dE+ \int_{-\infty}^{E_v}\left(1-\frac{1}{1+\exp\left(\frac{E-e\psi-E_i}{k_B T}\right)}\right)D_v(E)dE - N_A^-\right). \quad (5.30)$$

An expression for the electric field at the surface can be derived (derivation

can be found in the appendix A.7):

$$\mathcal{E}_s^2 = \frac{2e}{\epsilon_{si}} \int_{\psi_b}^{\psi_s} \left(- \int_{E_c}^{\infty} \frac{1}{1 + \exp\left(\frac{E - e\psi - E_i}{k_\mathrm{B}T}\right)} D_c(E)dE + \right. \\ \left. \int_{-\infty}^{E_v} \left(1 - \frac{1}{1 + \exp\left(\frac{E - e\psi - E_i}{k_\mathrm{B}T}\right)} \right) D_v(E)dE - N_A^- \right) d\psi \quad (5.31)$$

5.2.5. Threshold voltage

The threshold voltage is calculated as presented in sec. 2.3.3 (eq. 2.35 combined with eq. 2.36).

5.2.6. IV model

The IV- model allows the computation of a drain to source current I_{DS} in the transistor. Additional parameter that need to be introduced are: the low field mobility μ_0, the mobility attenuation factor θ and the metal work function ϕ_m. Also length L and width W of the transistor need to be specified.

An expression for I_{DS} starting from drift and diffusion transport equation is given in eq. 2.28. This expression for I_{DS} can be written in an integral form in terms of the channel voltage V_{ch} [92]:

$$I_{DS} = -\frac{\mu_0}{1 + \theta V_G} \frac{W}{L} \int_{V_{SB}}^{V_{DB}} Q_I(V_{ch}) dV_{ch}, \quad (5.32)$$

where a simple model for the mobility μ is used:

$$\mu = \frac{\mu_0}{1 + \theta V_{GB}}. \quad (5.33)$$

This simple mobility model can easily be extended to some more sophisticated approach, as for example presented in sec. 2.3.2, but this has the cost of introducing additional parameters.

5.2.7. Fitting results

In this subsection current voltage characteristics generated with the developed Python model are compared to real measurement data. Since the model works for the NMOS transistor only and does not incorporated width and length dependencies, a long and wide NMOS transistor is chosen to be compared to. The NMOS transistor has an aspect ratio of $W/L = 10\,\mu m/10\,\mu m$ (analog NMOS T3, according to tab. 6.3).

The following parameters are fitted to a given transfer (with $V_D = 20\,mV$): ϕ_{ms} (corresponds to fitting V_t), u_0 and θ. At first no interface traps are implemented. The temperature dependence of the extracted parameters can be seen in fig. 5.16 and fig. 5.15. The fitted values for the threshold voltage have a similar temperature dependence as values extracted with the "CsrTR"- method. The negative values for θ at lower temperatures can be explained with the rise of the mobility as a function of the gate voltage in this regime, this is further illustrated in fig. 5.17, where the mobility is plotted as a function of the gate voltage for different temperatures. It should be considered that the mobility in the Python model is computed with eq. 5.33.

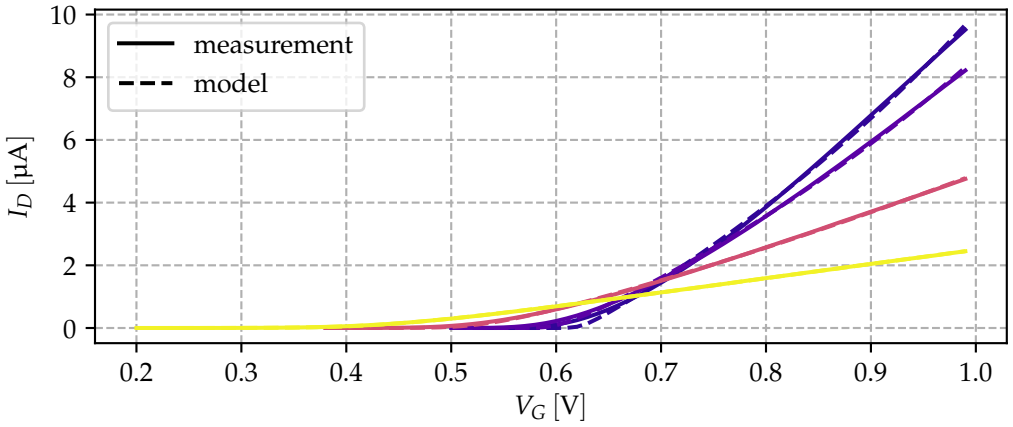


Figure 5.12.: Modeled and measured transfer characteristics of NMOS T6 at 4 different temperatures: 20 K, 50 K, 160 K, 300 K. The interface trap density N_{it} was set to 0.

Fig. 5.12 shows a comparison between the measured and modeled transfer

characteristics at 4 temperatures on a linear scale. Good agreement between measured and modeled data can be seen. However, as can be seen in fig. 5.13, where the same plot is shown on a log scale, there are significant deviations especially in the subthreshold regime: the modeled curves tend towards steeper subthreshold slopes than it was actually measured at low temperatures. This is in agreement with the results presented in sec. 4.7.3, since also there the measurements show a deviation from the predicted linear dependency.

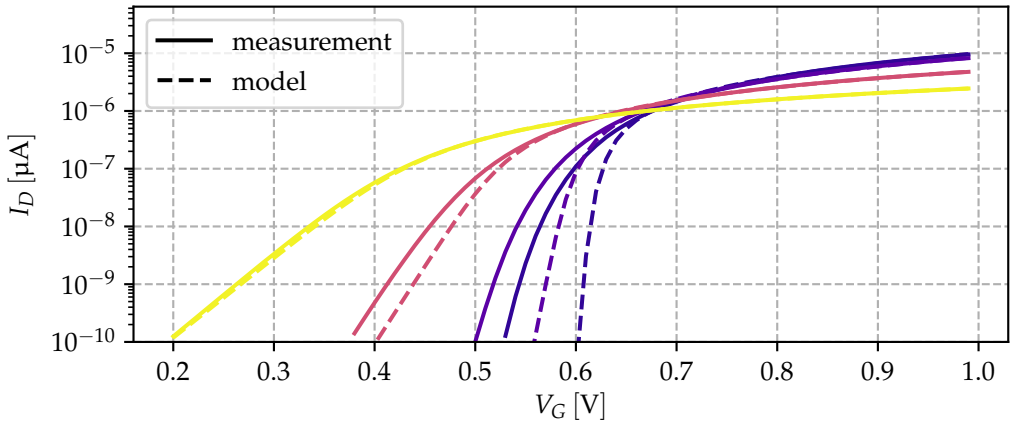


Figure 5.13.: Modeled and measured transfer characteristics of NMOS T3 on logarithmic scale at 4 different temperatures: 20 K, 50 K, 160 K, 300 K. The interface trap density N_{it} was set to 0.

The deviation in the subthreshold regime can be modeled using interface traps, as introduced in section 5.2.3 [89]. Figure 5.14 shows a measurement-model comparison at a temperature of 50 K. It can be seen that the inclusion of interface traps indeed allow for a better modeling in the subthreshold regime. It should be noted that exemplarily a single interface trap is placed to show how it impacts the subthreshold slope. To be more accurate either discrete interface traps at many different energetic levels or even a continuous distribution of interface traps should be considered. However, both of the above mentioned approaches lead to unreasonably high values of the interface trap density N_{it} [15]. This is already evident in the single trap approach presented in fig. 5.14: the extracted value of the interface trap density N_{it}, is by far larger than the one that was estimated out of the charge pumping measurement in section 4.4

(see eq. 4.3).

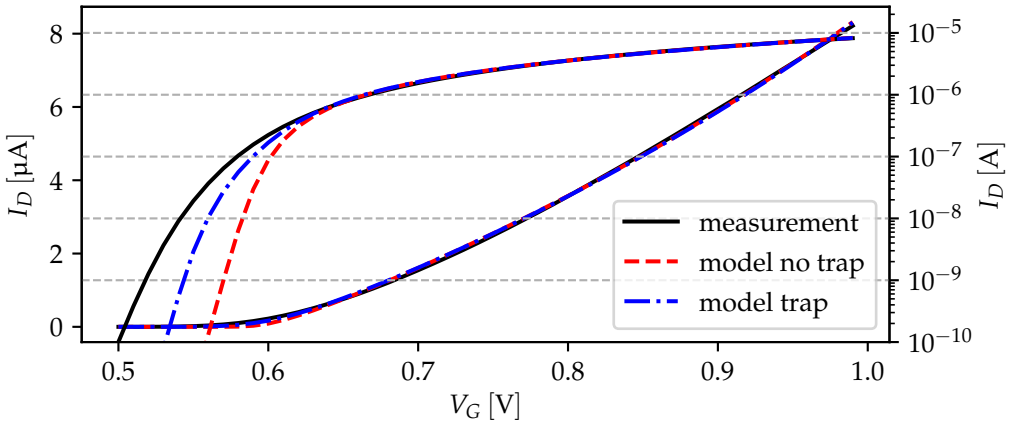


Figure 5.14.: Modeled and measured transfer characteristics of NMOS T3 at 50 K on logarithmic and linear scale. The trap model includes a single trap level with the parameters: $N_{it} = 1 \times 10^{11}\,\mathrm{cm}^{-2}$ and $\psi_t = 0.575\,\mathrm{eV}$.

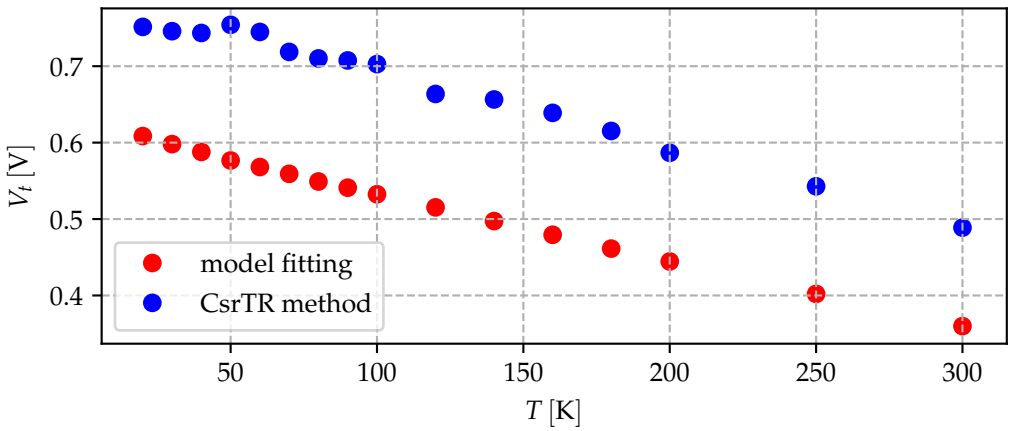


Figure 5.15.: Fitted and extracted threshold voltage V_t versus temperature T. "CsrTR"-method, see section 4.7.2.

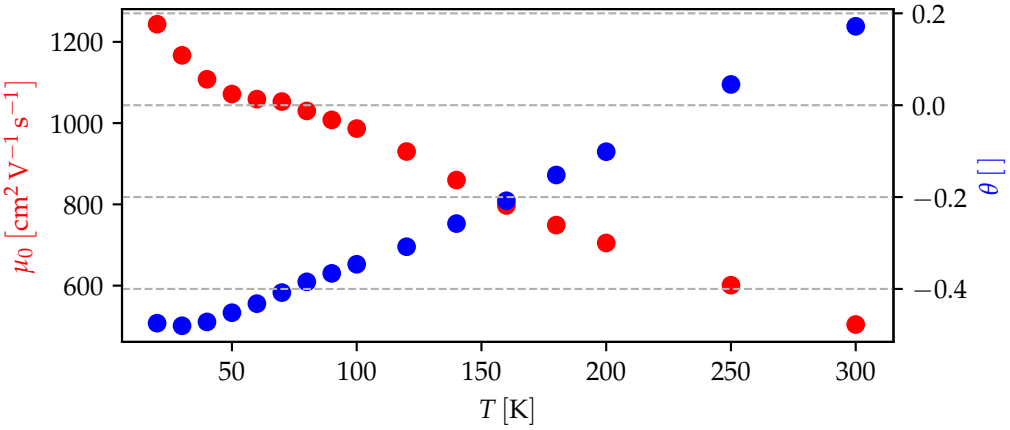


Figure 5.16.: Fitted values for the low field mobility μ_0 and mobility reduction factor θ versus temperature T.

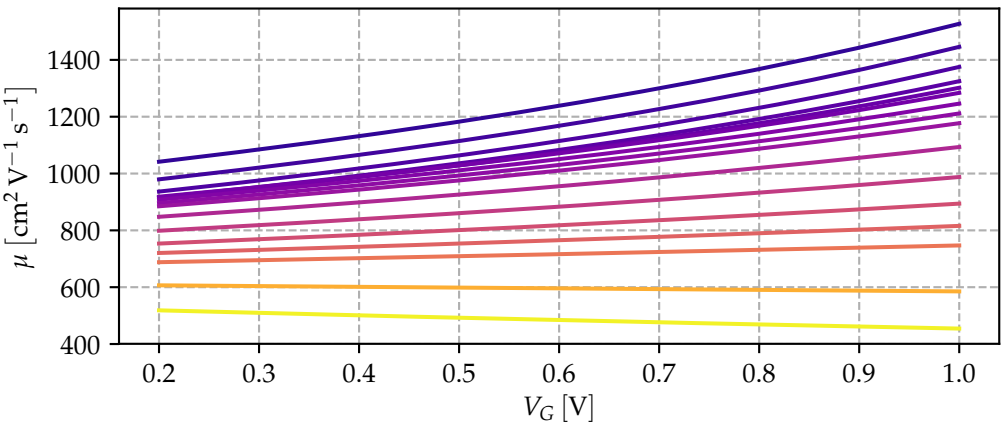


Figure 5.17.: Mobility as a function of the gate voltage, modeled with eq. 5.33. The parameters and temperatures are given in fig. 5.16.

6. Conclusion and Outlook

6.1. Conclusion

Many properties of silicon change as a function of temperature. In this work a review was made on the relevant properties of silicon that effect the macroscopic features of semiconductor devices. Additionally, general relations regarding the physics in a MOS transistor were reviewed and a study on different cryogenic transistor effects was presented.

Semiconductor devices from a 130 nm CMOS process were characterized at various biasing conditions down to cryogenic temperatures. The results of these measurements are presented in this thesis. Agreeing with literature and recent publications the following effects could be confirmed at cryogenic temperatures: an increase in the transistor mobility (section 4.6 and 4.7.2), increase in the transistor threshold voltage (section 4.6 and 4.7.1), the decrease of the transistor subthreshold slope and it's deviation from the predicted linear behavior for temperatures below about 50 K (section 4.7.3), a quasi temperature independent capacitance of CMOS capacitor structures (section 4.3), an increase of the resistance of poly-silicon resistors, and an decrease of the resistance of salicided poly-silicon resistors (section 4.2).

A Python model incorporating the above mentioned cryogenic effects was developed (section 5.2). The Python code is freely available as an online resource. A comparison between the developed model and real measurement results is made and a possible explanation for the mismatch in the subthreshold regime at cryogenic temperatures was given.

6.2. Outlook

Within this work a first step towards the implementation of a cryogenic circuit was made. Possible further items of action might be:

- Performing AC transistor measurements: The transistors were only characterized in DC mode. However, also temperature dependent AC characterizations might be of interest, in order to design the cryogenic circuit.
- Noise measurements and modeling: In order to fully simulate an electronic circuit models for noise are needed. It would be very interesting to characterize semiconductor devices in terms of their noise behavior down to cryogenic temperatures. Models for this noise need to be developed and implemented.
- Modeling of short transistor effects: The presented data could be analyzed in terms of the variation of certain parameters with respect to the transistor size. Effects such as effective lengths and widths or velocity saturation could be modeled.
- Using the presented model in a circuit simulator: The Python code of the transistor model needs to be converted to some resource that can be used by standard simulators, e.g. VERILOG-A.
- Design of the electronic circuitry: Circuitry needed to deliver the required electronic signals must be developed.

Once the concept of the circuit is proven to work at the cryogenic conditions, it will also be of great interest to cointegrate the circuit with the ion traps of the PIEDMONS project. Electronic circuitry and the trap on the same substrate might have many benefits, and could be the next step towards a scalable quantum computer realized with ion traps.

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List of Figures

Appendix

A. Derivation of formulas

In this section some formulas appearing in the chapter 2 are derived. The derivations can be found in standard books on semiconductor devices and are shown here for completeness and as a quick look-up resource.

A.1. Derivation of eq. 2.11

For an intrinsic semiconductor $n = p$ and thus using the Boltzmann approximation:

$$N_c \exp\left(\frac{E_f - E_c}{k_\mathrm{B}T}\right) = N_v \exp\left(\frac{E_f - E_v}{k_\mathrm{B}T}\right) \tag{6.1}$$

$$\Rightarrow \frac{N_v}{N_c} = \exp\left(\frac{E_f - E_c - E_v + E_f}{k_\mathrm{B}T}\right) = \exp\left(\frac{-E_c - E_v}{k_\mathrm{B}T}\right), \tag{6.2}$$

solving this equation for E_f and considering that for the intrinsic semiconductor $E_f = E_i$ yields the result:

$$E_f \overset{\text{intrinsic case}}{=} E_i = \frac{E_c + E_v}{2} + \frac{k_\mathrm{B}T}{2} \ln \frac{N_v}{N_c}. \tag{6.3}$$

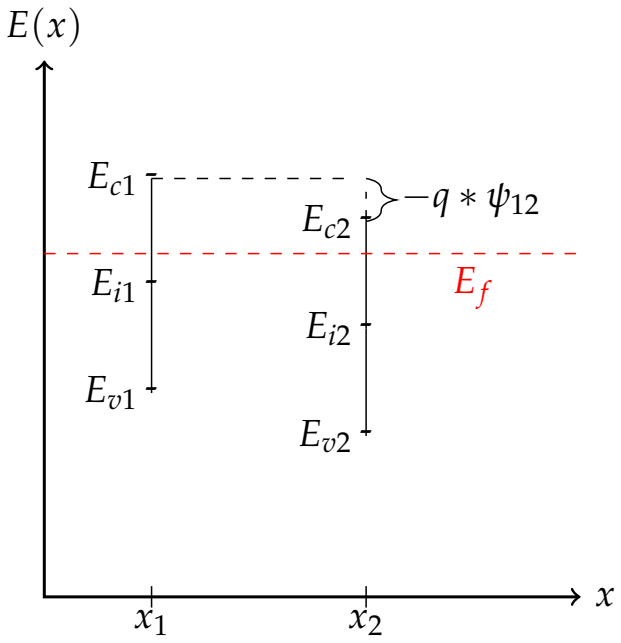

Figure 6.1.: Sketch of the band diagram $E(x)$ of two points x_1, x_2 with a potential difference Ψ_{12} in a n-doped semiconductor. The Fermi energy is constant throughout the semiconductor, the potential difference causes a shift in E_c , E_v and E_i.

A.2. Derivation of eq. 2.18

To show that this equation holds it is sufficient to show that if there is a potential difference ψ_{12} between two points (labeled 1 and 2) in a doped or undoped semiconductor in equilibrium the following relation applies [21]:

$$\frac{n_1}{n_2} = \exp \frac{\psi_{12}}{\phi_t}. \tag{6.4}$$

The potential difference shifts E_c , E_v and E_i, whereas E_f stays constant with position. For the shift in energies:

$$\Delta E_c = \Delta E_v = \Delta E_i = -q\Psi_{12}, \tag{6.5}$$

this is illustrate in fig. 6.1.

Now using eq. 2.9 and considering that the intrinsic doping level is the same at the two positions:

$$\begin{aligned} n_1 &= n_i \exp\left(\frac{E_f - E_{i1}}{k_\mathrm{B}T}\right) \\ n_2 &= n_i \exp\left(\frac{E_f - E_{i2}}{k_\mathrm{B}T}\right). \end{aligned} \tag{6.6}$$

If n_1 is now related to n_2:

$$\frac{n_1}{n_2} = \exp\left(\frac{E_{i2} - E_{i1}}{k_\mathrm{B}T}\right) = \exp\left(\frac{q\Psi_{12}}{k_\mathrm{B}T}\right) = \exp\left(\frac{\Psi_{12}}{\phi_t}\right), \tag{6.7}$$

the desired relation is derived.

The charge carriers in doped semiconductors can thus be calculated as follow:

$$n = n_i \exp\left(-\phi_f\right), \tag{6.8}$$

and

$$p = n_i \exp\left(\phi_f\right), \tag{6.9}$$

where the Fermi potential is given by eq. 2.19.

A.3. Derivation of eq. 2.23

This derivation assumes complete ionization, however also analytical solutions to eq. 2.23 including incomplete ionization can be derived. A common way to analytically solve eq. 2.22 ([21], [19])is to multiply both sides with $2\frac{\partial\psi}{\partial y}$ and identifying the left side of the equation with $\frac{\partial}{\partial y}(\frac{\partial\psi}{\partial y})^2$:

$$\frac{\partial}{\partial y}(\frac{\partial\psi}{\partial y})^2 = \frac{\partial}{\partial y}\mathcal{E}^2 = \frac{\partial}{\partial y}\frac{2q}{\epsilon_{si}}[p_0 \exp\left(-\psi(y)/\phi_t\right) - N_A + N_D - n_0 \exp\left(\psi(y)/\phi_t\right)], \tag{6.10}$$

which can be solved (assuming that the electric field deep in the bulk vanishes) analytically:

$$\mathcal{E}_s = \mathcal{E}(y=0) = sgn(\psi_s)\sqrt{\frac{2q}{\epsilon_{si}}}\sqrt{p_0\phi_t(\exp(-\psi_s/\phi_t)-1)+(N_A-N_D)\psi_s+n_0\phi_t(\exp(\psi_s/\phi_t)-1)} \tag{6.11}$$

A.4. Derivation of eq. 2.26

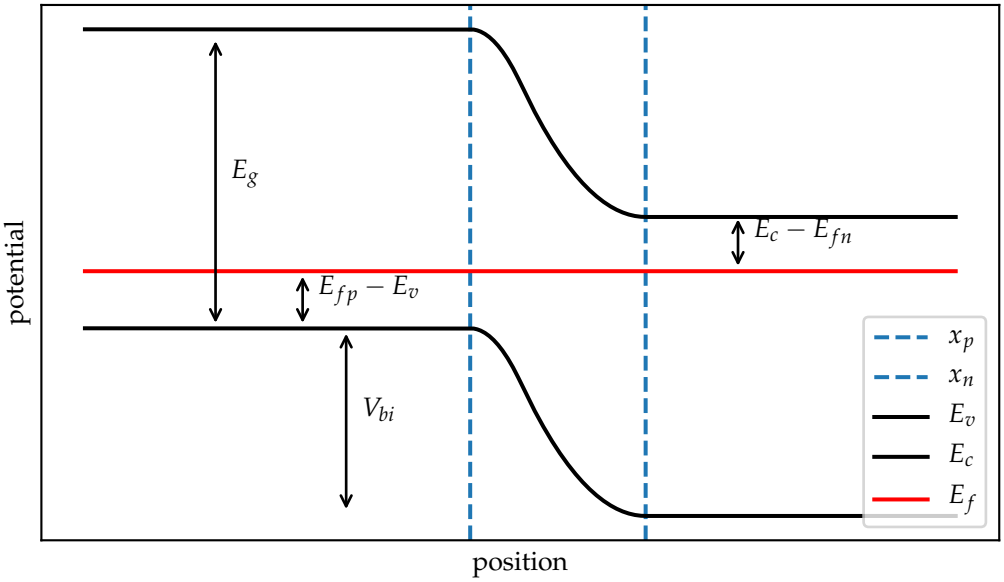

Figure 6.2.: Abrupt pn-junction: derivation of the built in voltage

Considering an abrupt p-n junction of a semiconductor with a band gap E_G, n-doping concentration of N_D, p-doping concentration of N_A and effective density of states in the valence/conduction band E_v/E_c, the built in potential V_{bi} can be calculated according to fig. 6.2. In this figure E_{fn}, E_{fp} are the distances of the Fermi energies to the conduction/valence band in the n/p doped regions and x_p and x_n denote the distances of the depleted regions in

the n and p side. From this figure one can obtain:

$$qV_{bi} = E_g - k_\mathrm{B}T[\log \frac{N_c}{N_{D,n} - N_{A,n}} + \log \frac{N_v}{N_{A,p} - N_{D,p}}], \tag{6.12}$$

where the relation $E_{fp} - E_v = k_\mathrm{B}T * \log \frac{N_v}{N_A}$ and $E_c - E_{fn} = k_\mathrm{B}T * \log \frac{N_c}{N_D}$, which follow from the Boltzmann approximation, where used. Combining eq. 6.12 with eq. 2.8 and applying some algebra finally yields:

$$qV_{bi} = k_\mathrm{B}T \log \frac{N_D N_A}{n_i^2}, \tag{6.13}$$

where $N_{D,n} = N_D >> N_{A,n}$ and $N_{A,p} = N_A >> N_{D,p}$ was assumed.

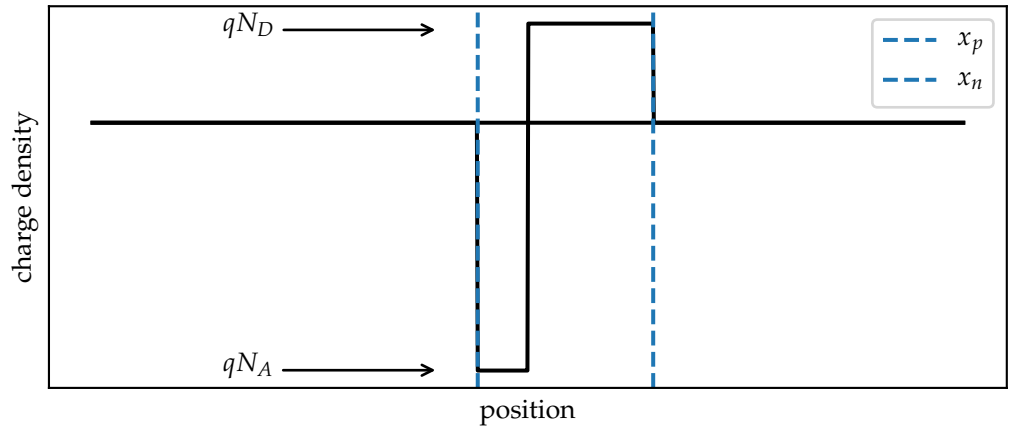

Figure 6.3.: Abrupt pn-junction: charge density versus position

The charge density versus position relation can be qualitatively seen in fig. 6.3. It is assumed constant till x_p/x_n and then jumps abruptly to zero. The charge density can be integrated twice to get the potential:

$$V(x) = \begin{cases} \frac{-qN_A}{2\epsilon} x_p^2, & x < x_p \\ \frac{qN_A}{\epsilon}(\frac{x^2}{2} + x x_p), & -x_p < x < 0 \\ \frac{-qN_D}{\epsilon}(\frac{x^2}{2} - x x_n), & 0 < x < x_n \\ \frac{qN_D}{2\epsilon} x_n^2, & x_n < x \end{cases} \tag{6.14}$$

V_{bi} can now be calculated:

$$V_{bi} = \frac{qN_A x_p^2}{2\epsilon} + \frac{qN_D x_n^2}{2\epsilon}. \tag{6.15}$$

Combining eq. 6.12 and eq. 6.15 allows the calculation of x_n and x_p, where W is introduced as total depletion length ($W = x_n + x_p$):

$$x_p = \frac{N_D W}{N_A + N_D} \tag{6.16}$$

$$x_n = \frac{N_A W}{N_A + N_D} \tag{6.17}$$

$$W = \sqrt{\frac{2\epsilon(N_D + N_A)V_{bi}}{qN_A N_D}}. \tag{6.18}$$

In the limit of a very heavily one sided p-n junction (e.g $N_D >> N_A$) eq. 6.18 reduces to:

$$W = \sqrt{\frac{2\epsilon V_{bi}}{qN_A}}. \tag{6.19}$$

In this limit $x_p \approx W$ and $x_n \approx 0$, and the charge on the p side Q_p can be calculated according to fig. 6.3:

$$Q_p = -qN_A x_p \approx \sqrt{2q\epsilon_S N_A \psi_S}. \tag{6.20}$$

A.5. Derivation of eq. 2.36

Derivation of $\phi_f^{'}$

The Fermi potential is defined as:

$$\phi_f = \frac{E_i - E_f}{q}. \tag{6.21}$$

Assuming a p-doped semiconductor (bulk of the NMOS transistor) E_f can be calculated via :

$$p \stackrel{!}{=} N_A. \tag{6.22}$$

p can be calculated using Boltzmann statistics:

$$\begin{aligned} p = N_v \exp\left((E_v - E_f)/(k_\mathrm{B}T)\right) = N_v \exp\left((E_v - E_i + E_i - E_f)/(k_\mathrm{B}T)\right) \\ = n_i \exp\left((E_i - E_f/(k_\mathrm{B}T)\right), \end{aligned} \tag{6.23}$$

where an artificial $0 = E_i - E_i$ was introduced to use:

$$n_i = N_v * \exp\left((E_v - E_i)/(k_\mathrm{B}T)\right). \tag{6.24}$$

Considering eq. 6.22 and eq. 6.23 yields:

$$n_i \exp\left(E_i - E_f\right)/(k_\mathrm{B}T) = N_A, \tag{6.25}$$

which is easily solved for $E_i - E_f$:

$$E_i - E_f = k_\mathrm{B}T \log \frac{N_A}{n_i}. \tag{6.26}$$

Inserting eq. 6.26 into eq. 6.21 yields the final result:

$$\phi_f^0 = \phi_t \log \frac{N_A}{n_i} \tag{6.27}$$

Derivation of ϕ_f^*

For computing ϕ_f^* incomplete ionization is considered, thus eq. 6.22 is modified to:

$$p \stackrel{!}{=} N_A^- = \frac{N_A}{1 + g_A \exp\left(E_A - E_f\right)/(k_\mathrm{B}T)}. \tag{6.28}$$

Introducing $A = g_A \exp\left((E_A - E_i)/(k_\mathrm{B}T)\right)$ equation 6.28 can be written as:

$$n_i \exp\left((E_i - E_f)/(k_\mathrm{B}T)\right) = \frac{N_A}{1 + A \exp\left((E_i - E_f)/(k_\mathrm{B}T)\right)} \tag{6.29}$$

Considering $\phi_f^* = \frac{E_i - E_f}{q}$ this can be identified as a quadratic equation in the variable $\exp\left(\phi_f^*/\phi_t\right)$:

$$(1 + A \exp\left(\phi_f^*/\phi_t\right)) \exp\left(\phi_f^*/\phi_t\right) = N_A/n_i. \tag{6.30}$$

Mathematical solutions to this equation are:

$$\exp\left(\phi_f^*/\phi_t\right) = \frac{-1 \pm \sqrt{1 + 4AN_A/n_i}}{2A}. \tag{6.31}$$

Requiring a positive solution, the upper sign (+) is taken. Solving for ϕ_f^* yields:

$$\phi_f^* = \phi_t * \log \frac{-1 + \sqrt{1 + 4AN_A/n_i}}{2A}. \tag{6.32}$$

Equation 6.33 can be rewritten to better see the difference between ϕ_f^0 and ϕ_f^*:

$$\phi_f^* = \underbrace{\phi_t \log \frac{N_A}{n_i}}_{\phi_f^0} - \phi_t \log \frac{1 + \sqrt{1 + 4AN_A/n_i}}{2}. \tag{6.33}$$

A plot of the two functions ϕ_f^0 and ϕ_f^* can be seen in fig. 6.4.

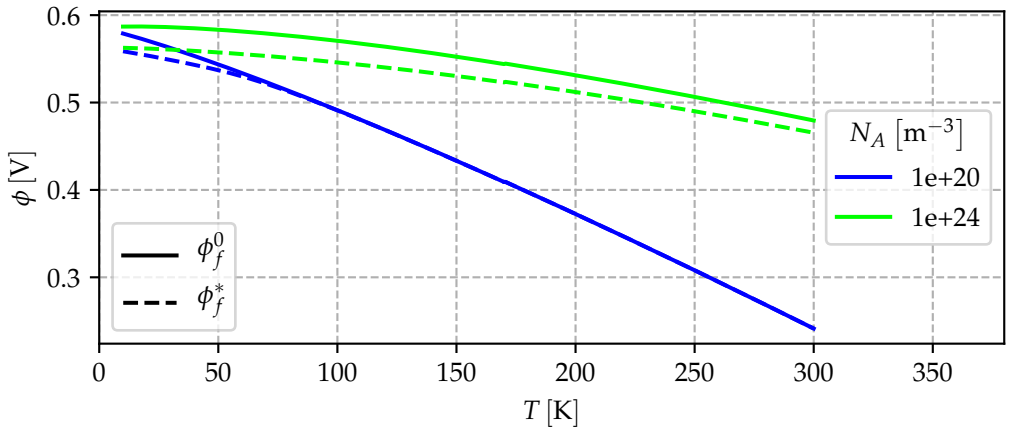

Figure 6.4.: Fermi potential with (ϕ_f^0) and without (ϕ_f^*) incomplete ionization plotted as a function of temperature for two different doping concentrations N_A.

A.6. Derivation of eq. 2.35

The derivation of the expression for the threshold voltage V_t follows the procedure presented in ref. [51], the expression for V_t is derived right at the source end of the transistor ($V_{ch} = 0$, $V_{SB} = 0$). This derivation assumes zero interface charges $Q_0 = 0$ and neglects interface trap charges Q_{it}.

An expression for the gate voltage is given by eq. 2.14. In this expression the oxide potential ψ_{ox} can be expressed as $\psi_{ox} = \epsilon_{si}\mathcal{E}_s/C_{ox}$ (where $\mathcal{E}_s$ is the vertical electrical field at the surface) yielding:

$$V_{GB} = \psi_s + \phi_{ms} + \epsilon_{si}\mathcal{E}_s(\psi_s)/C_{ox}. \tag{6.34}$$

To further proceed it is useful to recall how the charge carrier densities can be calculated as a function of the Fermi potential ϕ_f, given by eq. 6.8. The relation between N_A and ϕ_f^0 is then given by:

$$N_A = n_i \exp\left(\phi_f^0/\phi_t\right) \tag{6.35}$$

and the concentration of electrons right at the interface is given by:

$$n_s = n_i \exp\left((\psi_s - \phi_f^*)/\phi_t\right). \tag{6.36}$$

Now requiring that $n_s \stackrel{!}{=} N_A$ yields for ψ_s:

$$\psi_s = \phi_f^0 + \phi_f^*. \tag{6.37}$$

The metal semiconductor work function ϕ_{ms} is given by the following expression:

$$\phi_{ms} = \phi_m - \phi_s. \tag{6.38}$$

ϕ_m can be assumed temperature independent [51] and ϕ_s is calculated via:

$$\phi_s = \chi + \frac{E_c - E_i}{e} + \phi_f^*. \tag{6.39}$$

$\mathcal{E}_s$ in eq. 6.34 can be calculated from solving the Poisson-Boltzmann equation [19]. Right at the threshold condition ($\psi_s = \phi_f^0 + \phi_f^*$, as derived in equation 6.37) $\mathcal{E}_s$ can be calculated as follows [51]:

$$\mathcal{E}_s = \frac{\phi_t}{\sqrt{\epsilon_{si}\phi_t/(2eN_A)}}\sqrt{\frac{\phi_f^0 + \phi_f^*}{\phi_t} + \log f_\theta + \log\left(1 + A\exp\left(-\phi_f^*/\phi_t\right)\right)} \quad (6.40)$$

The electric field in eq. 6.40 is computed including the effect of incomplete ionization, however the two terms belonging to this effect (the logarithmic terms in the square root of eq. 6.40) can be neglected tolerating a $\approx 1\,\%$ error.

Putting all of the just derived relevant terms back into eq. 6.34, a formula for the threshold voltage is derived:

$$V_t = \phi_f^0 + \phi_m - (\chi + \frac{E_c - E_i}{e}) + \frac{\sqrt{2eN_A\epsilon_{si}}}{C_{ox}}\sqrt{\phi_f^0 + \phi_f^*}. \quad (6.41)$$

Rewriting n_i, E_i, N_c and N_v as a function of temperature, an expression for V_t can be derived, where all analytical temperature dependencies are explicitly shown:

$$\begin{aligned} V_t = {} & \frac{k_\mathrm{B}T}{e}\log\frac{N_A}{4\left(\frac{k_\mathrm{B}T}{2\pi\hbar^2}\right)^3(m_n m_p)^{3/2}} + \phi_m - \chi + \frac{k_\mathrm{B}T}{2e}\log\left(\left(\frac{m_p}{m_n}\right)^{3/2}\right) \\ & + \frac{\sqrt{2eN_A\epsilon_{si}}}{C_{ox}}\cdot \\ & \sqrt{\frac{E_g}{e} + \frac{2k_\mathrm{B}T}{e}\log\frac{N_A}{\sqrt{4\left(\frac{k_\mathrm{B}T}{2\pi\hbar^2}\right)^3(m_n m_p)^{3/2}}} - \frac{k_\mathrm{B}T}{e}\log\frac{1 + \sqrt{1 + 4g_A\exp\left(\frac{E_A - E_i + E_g}{2k_\mathrm{B}T}\right)\frac{N_A}{4\left(\frac{k_\mathrm{B}T}{2\pi\hbar^2}\right)^3(m_n m_p)^{3/2}}}}{2}}. \end{aligned} \quad (6.42)$$

A.7. Derivation of eq. 5.31

The derivation is the same as the one presented in sec. A.3, just with a different definition of the potential ψ. In eq. 5.31 a formula for $g(\psi(y))$ is stated such

that $\frac{\partial^2}{\partial^2 y}\psi(y) = g(\psi(y))$. Both sides of this equation are multiplied with $2\frac{\partial\psi}{\partial y}$ and the left side can be identified as:

$$2y\frac{\partial^2}{\partial^2 y}\psi(y) = \frac{\partial}{\partial y}\left(\frac{\partial\psi(y)}{\partial y}\right)^2 = \frac{\partial}{\partial y}\mathcal{E}(y)^2 = 2\frac{\partial\psi}{\partial y}g(\psi(y)). \tag{6.43}$$

Thus $\mathcal{E}_s^2$ can be calculated via integrating from $y = -\infty$ to $y = y_s$:

$$\mathcal{E}_s^2 = \int_{y=-\infty}^{y=y_s}\frac{\partial}{\partial y}\mathcal{E}(y)^2 dy = \int_{y=-\infty}^{y=y_s} 2\frac{\partial\psi}{\partial y}g(\psi(y))dy, \tag{6.44}$$

which can be transformed to:

$$\mathcal{E}_s^2 = \int_{\psi=\psi_b}^{\psi=\psi_s}\frac{\partial}{\partial y}\mathcal{E}(\psi)^2 d\psi = \int_{\psi=\psi_b}^{\psi=\psi_s} 2g(\psi)d\psi, \tag{6.45}$$

where the variable y was substituted with the variable ψ.

A.8. Derivation of eq. 5.28

The charge sheet approximation assumes that the inversion layer is a sheet of negligible thickness, and thus the potential drop across this layer approaches 0 [21]. Additionally, it is assumed that the region below the interface is depleted, and thus just the fixed acceptor ions remain when writing Poisson equation:

$$\frac{\partial^2}{\partial^2 y}\psi(y) = \frac{e}{\epsilon_{si}}N_A^- = \frac{e}{\epsilon_{si}}\frac{N_A}{1 + g_A\exp\left(\frac{\psi_A-\psi-V_{ch}}{\phi_t}\right)} \tag{6.46}$$

As shown in derivation A.7 this can equation can be rewritten to calculate the electric field at the surface $\mathcal{E}_{cs}$, where the under-script cs refers to charge sheet:

$$\mathcal{E}_{cs}^2 = \int_{\psi=\psi_b}^{\psi=\psi_s}\frac{2e}{\epsilon_{si}}\frac{N_A}{1 + g_A\exp\left(\frac{\psi_A-\psi-V_{ch}}{\phi_t}\right)}d\psi. \tag{6.47}$$

This integral can be solved analytically, which yields:

$$\mathcal{E}_{cs}^2 = \frac{2eN_A}{\epsilon_{si}}\left(\psi_s - \psi_b - \phi_t\log\left(\frac{1 + g_A\exp\frac{\psi_A-\psi_b}{\phi_t}}{1 + g_A\exp\frac{\psi_A-(\psi_s-\psi_b)}{\phi_t}}\right)\right). \tag{6.48}$$

Finally, the fixed charge Q_B is related to this electric field via:

$$Q_B = -\epsilon_{si}\mathcal{E}_{cs}. \tag{6.49}$$

Plugging the square root of eq. 6.48 into eq. 6.49 yields the final result.

B. Measurement results

B.1. Mobility model parameter

Parameters for the mobility model presented in section 2.3.2 are given in tab. 6.1 and tab. 6.2.

Table 6.1.: Mobility model parameter for different temperatures taken to create the plots presented in fig. 2.9. Values for the moderate field model are taken from [37]. The values for θ_2 are estimated out of plots presented in [43]. The parameter are introduced in section 2.3.2.

T [K]	V_t [V]	μ_{max} $\left[\mathrm{cm^2\,V^{-1}\,s^{-1}}\right]$	n	θ	θ_2
4.1	0.77	7870	3.0	0.78	
	0.77	7870	3.0	0.78	0.5
60	0.47	2935	2.75	0.20	
	0.47	2935	2.75	0.20	0.48
90	0.43	2094	2.30	0.08	
	0.43	2094	2.30	0.08	0.4
200	0.36	1001	2.1	0.05	
	0.36	1001	2.1	0.05	0.22
300	0.25	530	2.1	0.07	
	0.25	530	2.1	0.07	0.1

Table 6.2.: Extracted parameter of the high electric field mobility model for different temperatures T. The extracted parameters correspond to the fits for the PMOS transistor presented in fig. 4.17.The parameter are introduced in section 2.3.2.

T [K]	μ_{max} $\left[\mathrm{cm^2\,V^{-1}\,s^{-1}}\right]$	n	V_t [V]	θ	θ_2
300	124	2.09	0.51	0.43	2.88×10^{-5}
250	131	2.23	0.50	0.63	4.74×10^{-5}
200	148	2.27	0.53	0.71	6.26×10^{-6}
180	157	2.28	0.55	0.74	1.37×10^{-5}
160	166	2.29	0.57	0.78	5.09×10^{-5}
140	176	2.33	0.59	0.83	4.50×10^{-5}
120	189	2.34	0.60	0.87	2.76×10^{-5}
100	197	2.36	0.62	0.89	1.52×10^{-4}
90	210	2.39	0.63	0.92	9.00×10^{-5}
80	212	2.40	0.64	0.92	5.17×10^{-6}
70	214	2.40	0.66	0.91	5.22×10^{-5}
60	213	2.41	0.67	0.91	1.77×10^{-4}
50	213	2.44	0.68	0.92	3.59×10^{-7}
40	217	2.46	0.68	0.94	1.43×10^{-4}
30	212	2.50	0.69	0.97	1.40×10^{-4}
20	212	2.54	0.69	1.00	2.40×10^{-4}

B.2. Digital transistors

In this subsection transfer characteristics of 4 digital transistors, that were used to extract the parameters in section 4.6 are presented. The applied drain voltage was $V_D = 50\,\mathrm{mV}$. The aspect ration of all measured transistors is given by: $W/L = 1.28\,\mu\mathrm{m}/1.20\,\mu\mathrm{m}$. The lines are colored according to the colorbar given in fig. 4.1.

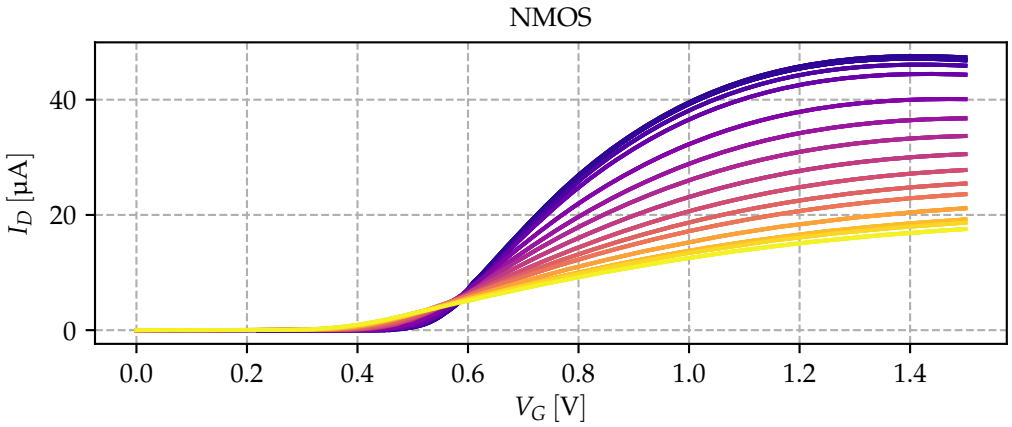

Figure 6.5.: Transfer characteristics for a logic NMOS transistor at different temperatures.

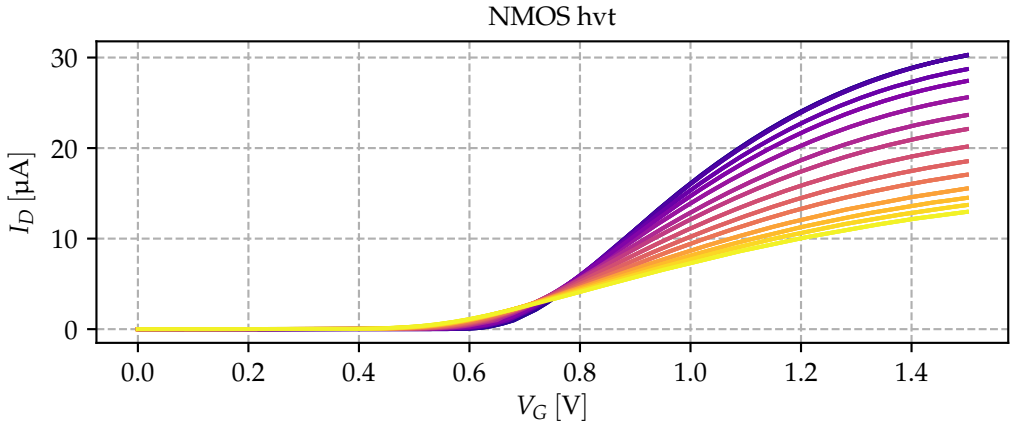

Figure 6.6.: Transfer characteristics for a logic NMOS transistor with an additional "threshold voltage adjust implant" at different temperatures.

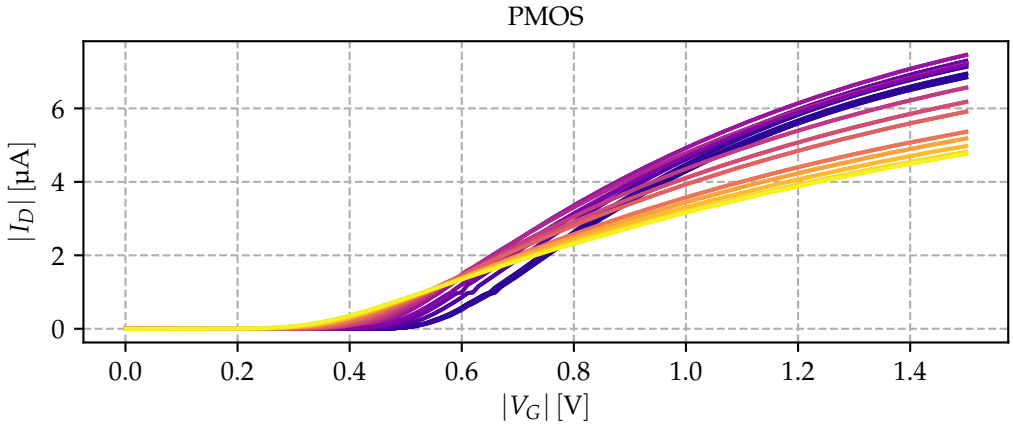

Figure 6.7.: Transfer characteristics for a logic PMOS transistor at different temperatures.

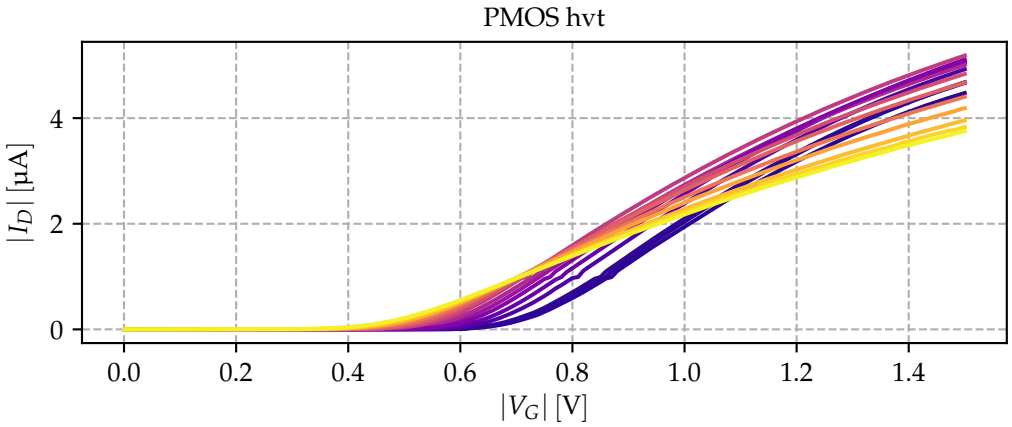

Figure 6.8.: Transfer characteristics for a logic PMOS transistor with an additional "threshold voltage adjust implant" at different temperatures.

B.3. Analog transistors

In this subsection transfer characteristics of analog transistors, that were used to extract the parameters in section 4.7 are presented. Widths, lengths and drain biases of the measured transistor are given in tab. 6.3.

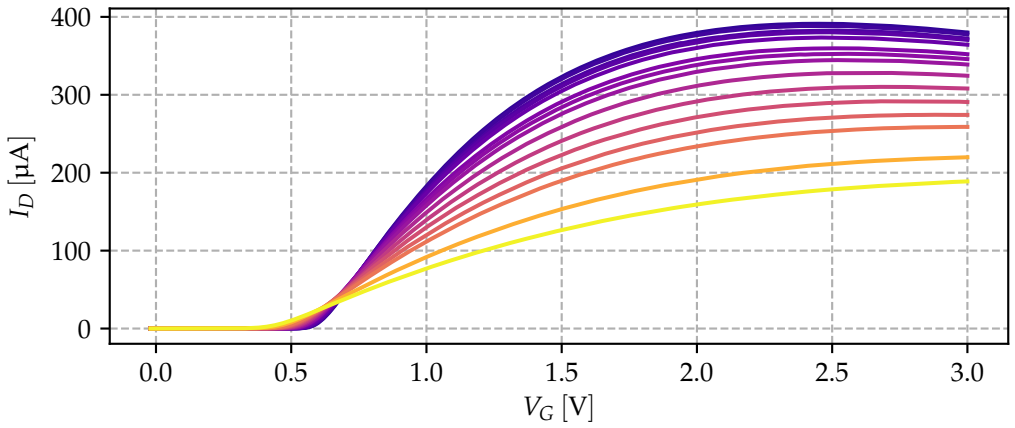

Figure 6.9.: Transfer characteristics for NMOS T1 at different temperatures. Details see tab. 6.3.

Table 6.3.: Widths, lengths and drain biases of the measured analog transistors.

Name	W[µm]	L[µm]	V_D[mV]
NMOS T1	10	0.36	20
NMOS T2	10	0.8	20
NMOS T3	10	10	20
PMOS T1	10	0.36	20
PMOS T2	10	0.8	20
PMOS T3	10	10	20

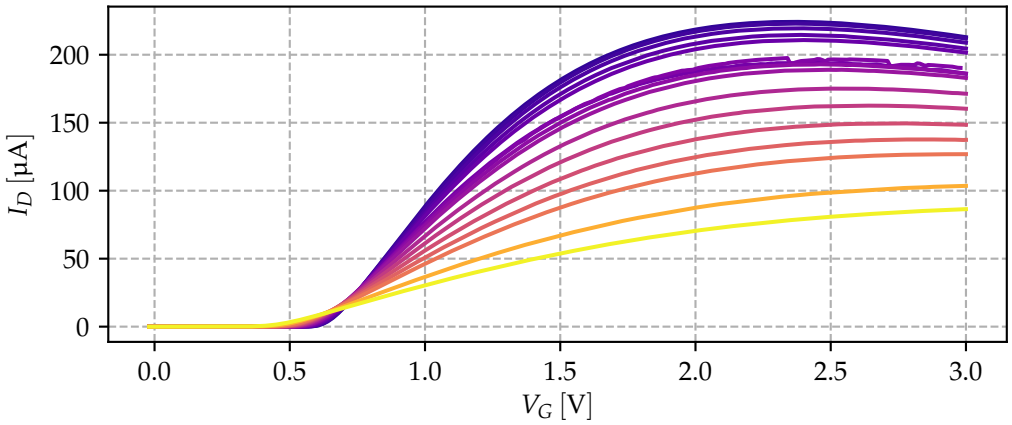

Figure 6.10.: Transfer characteristics for NMOS T2 at different temperatures. Details see tab. 6.3.

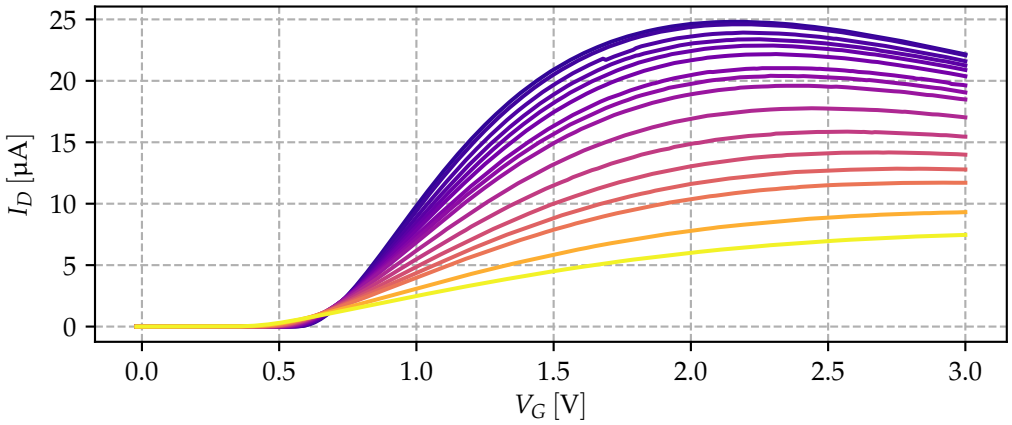

Figure 6.11.: Transfer characteristics for NMOS T3 at different temperatures. Details see tab. 6.3.

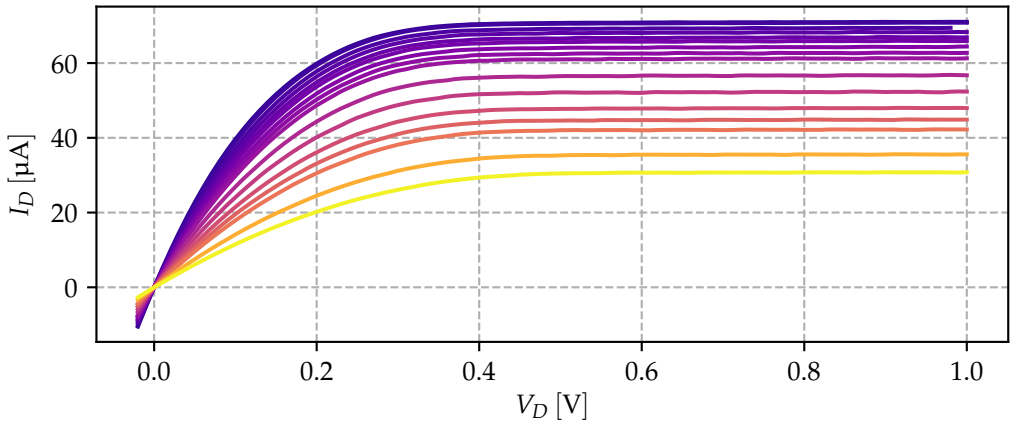

Figure 6.12.: Output characteristics for NMOS T3 at different temperatures. Width and length of measured transistor see tab. 6.3. The applied gate bias was: $V_G = 1.0\,\mathrm{V}$.

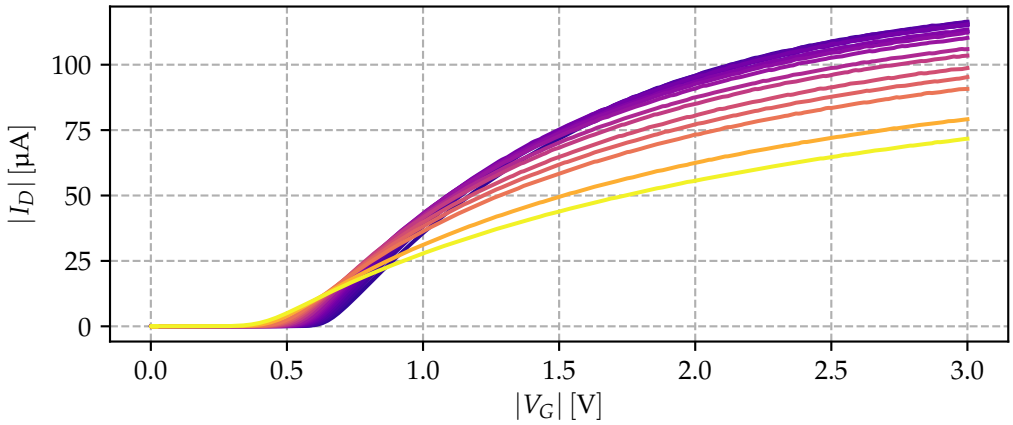

Figure 6.13.: Transfer characteristics for PMOS T1 at different temperatures. Details see tab. 6.3.

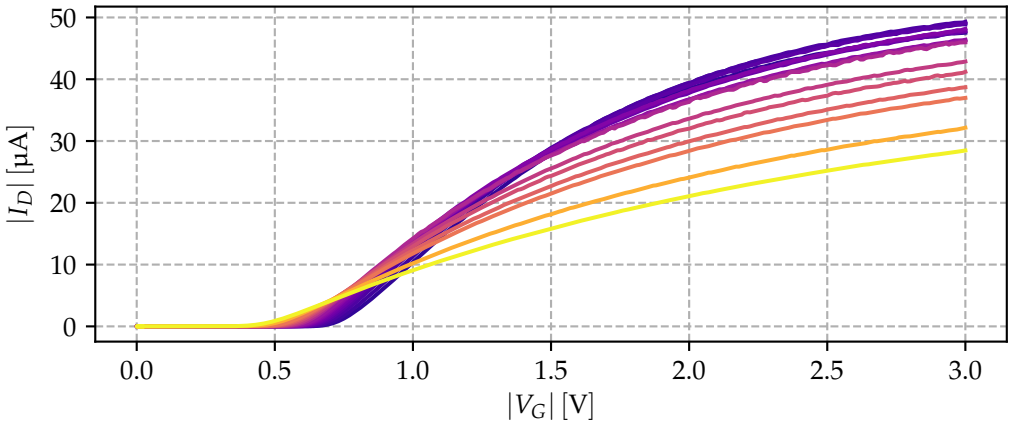

Figure 6.14.: Transfer characteristics for PMOS T2 at different temperatures. Details see tab. 6.3.

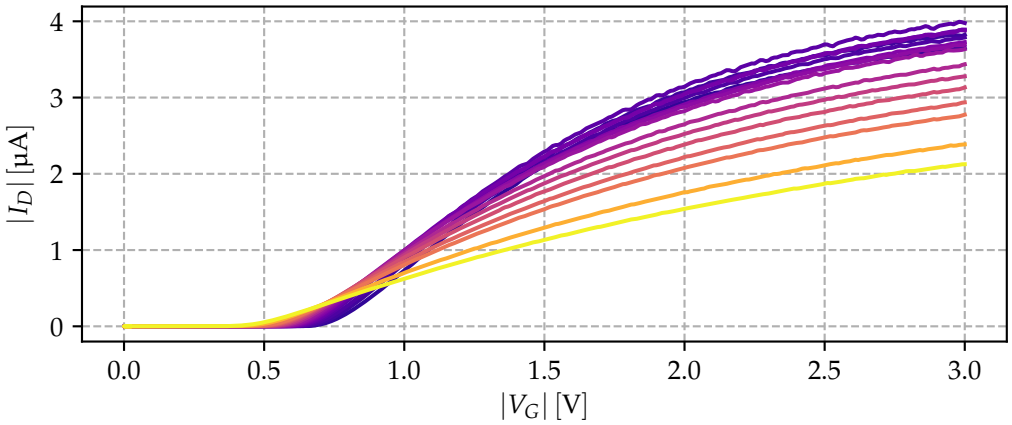

Figure 6.15.: Transfer characteristics for PMOS T3 at different temperatures. Details see tab. 6.3.

B.4. Simplified EKV model parameter

In this subsection extracted parameter for the simplified EKV model, introduced in section 5.1, are presented.

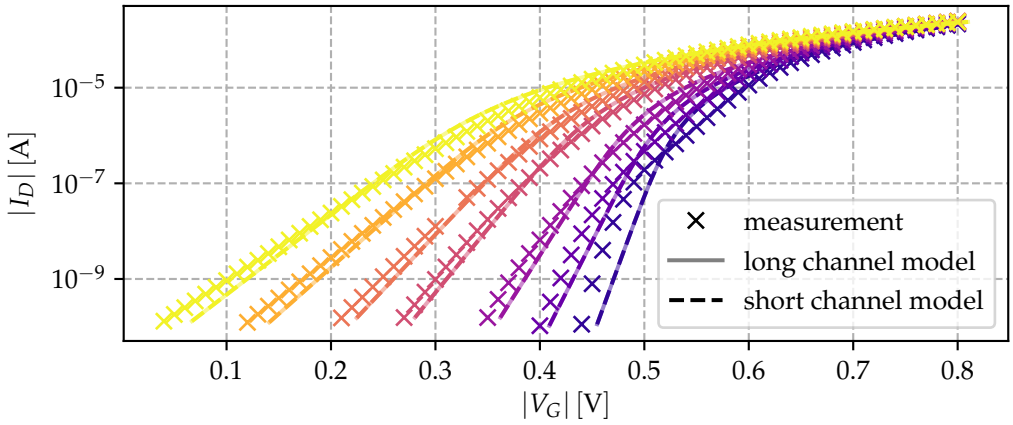

Figure 6.16.: Simplified EKV model versus measurement data for a PMOS transistor biased with a drain voltage of $V_D = -1\,\mathrm{V}$.The temperatures according to the lines from left to right are: 20 K,60 K,100 K,160 K,200 K,250 K and 300 K. Transistor length and width are $W = 10\,\mu\mathrm{m}$, $L = 0.36\,\mu\mathrm{m}$. Source and bulk voltage were kept at zero volts: $V_S = V_B = 0\,\mathrm{V}$.

Table 6.4.: Fitted parameter of the simplified EKV model, on a NMOS transistor with $W = L = 10\,\mu m$. Plots of the fits can be seen in fig. 5.2b.

T	model type	$I_{spec\square}$ [nA]	n [1]	V_{T0} [V]	L_{sat} [nm]
17	long	189.293	7.116	0.600	NAN
	short	189.293	7.116	0.600	2.6E-14
20	long	193.590	6.134	0.599	NAN
	short	193.367	6.131	0.599	5.1E-01
30	long	234.541	4.532	0.597	NAN
	short	234.483	4.532	0.597	4.2E-07
40	long	230.778	3.485	0.590	NAN
	short	230.688	3.485	0.590	7.1E-01
50	long	203.911	2.737	0.581	NAN
	short	203.910	2.737	0.581	1.5E-07
60	long	216.779	2.401	0.575	NAN
	short	216.779	2.401	0.575	9.6E-13
70	long	230.610	2.159	0.570	NAN
	short	230.610	2.159	0.570	3.2E-06
80	long	254.726	2.025	0.564	NAN
	short	254.726	2.025	0.564	1.1E-04
90	long	262.690	1.868	0.559	NAN
	short	262.690	1.868	0.559	2.8E-04
100	long	277.114	1.760	0.553	NAN
	short	277.114	1.760	0.553	8.0E-05
120	long	297.502	1.602	0.542	NAN
	short	297.001	1.601	0.542	3.4E+00
140	long	298.354	1.464	0.529	NAN
	short	298.302	1.463	0.529	6.8E-02
160	long	315.362	1.393	0.517	NAN
	short	314.591	1.392	0.517	1.0E-01
200	long	338.677	1.276	0.492	NAN
	short	338.550	1.276	0.492	9.9E-02
250	long	371.814	1.215	0.461	NAN
	short	371.813	1.215	0.461	1.0E-07
300	long	408.290	1.191	0.430	NAN
	short	408.361	1.192	0.430	9.6E-02

Table 6.5.: Fitted parameter of the simplified EKV model, on a PMOS transistor with $W = L = 10\,\mu m$. Plots of the fits can be seen in fig. 5.3.

T	model type	$I_{spec\square}$ [nA]	n [1]	V_{T0} [V]	L_{sat} [nm]
20	long	21.760	7.211	0.679	NAN
	short	21.761	7.211	0.679	4.505E-01
30	long	27.313	4.906	0.670	NAN
	short	27.320	4.907	0.670	1.692E+00
40	long	32.682	3.834	0.659	NAN
	short	33.404	3.862	0.659	5.129E+00
60	long	41.343	2.688	0.639	NAN
	short	41.346	2.688	0.639	1.295E+00
70	long	42.294	2.319	0.630	NAN
	short	42.296	2.319	0.630	1.150E+00
80	long	47.792	2.157	0.623	NAN
	short	47.779	2.157	0.623	2.672E-02
90	long	55.257	2.038	0.617	NAN
	short	55.257	2.038	0.617	1.241E-07
100	long	58.295	1.895	0.609	NAN
	short	58.297	1.895	0.609	2.718E-01
120	long	68.657	1.741	0.595	NAN
	short	68.654	1.741	0.595	2.021E-02
140	long	74.160	1.595	0.580	NAN
	short	74.159	1.595	0.580	1.613E-07
160	long	79.411	1.495	0.563	NAN
	short	79.412	1.495	0.563	1.073E-01
180	long	85.181	1.429	0.549	NAN
	short	85.190	1.429	0.549	2.445E+00
200	long	89.618	1.369	0.536	NAN
	short	89.625	1.369	0.536	1.859E+00
250	long	101.234	1.292	0.497	NAN
	short	101.234	1.292	0.497	5.538E-03
300	long	112.876	1.232	0.467	NAN
	short	112.877	1.232	0.467	9.908E-02

Table 6.6.: Fitted parameter of the simplified EKV model, on a NMOS transistor with $W = 10\,\mu m$ and $L = 0.36\,\mu m$. The applied drain voltage was $V_D = 1\,V$.

T	model type	$I_{spec\square}$ [nA]	n [1]	V_{T0} [V]	L_{sat} [nm]
17	long	106.134	5.852	0.509	NAN
	short	218.718	6.803	0.523	4.301E+01
20	long	106.574	4.987	0.509	NAN
	short	221.225	5.806	0.523	4.352E+01
30	long	107.238	3.361	0.507	NAN
	short	196.466	3.786	0.519	3.794E+01
40	long	114.458	2.640	0.505	NAN
	short	188.144	2.897	0.514	3.379E+01
50	long	125.460	2.230	0.502	NAN
	short	208.013	2.437	0.513	3.635E+01
60	long	146.190	2.001	0.500	NAN
	short	199.801	2.104	0.506	2.899E+01
80	long	165.785	1.667	0.492	NAN
	short	238.287	1.765	0.500	3.303E+01
90	long	185.429	1.582	0.490	NAN
	short	265.698	1.670	0.498	3.506E+01
100	long	203.271	1.514	0.488	NAN
	short	287.733	1.591	0.496	3.616E+01
120	long	224.279	1.378	0.479	NAN
	short	298.150	1.431	0.486	3.317E+01
140	long	260.640	1.314	0.472	NAN
	short	341.551	1.355	0.479	3.598E+01
160	long	293.450	1.269	0.462	NAN
	short	376.304	1.303	0.468	3.641E+01
200	long	355.062	1.207	0.443	NAN
	short	456.503	1.235	0.451	4.160E+01
250	long	427.335	1.171	0.418	NAN
	short	567.201	1.196	0.428	5.145E+01
300	long	491.709	1.147	0.393	NAN
	short	669.795	1.171	0.405	6.049E+01

Table 6.7.: Fitted parameter of the simplified EKV model, on a NMOS transistor with $W = 10\,\mu m$ and $L = 0.36\,\mu m$. Extraction strategy as described in section 5.1.3.

T	model type	$I_{spec\square}$ [nA]	n [1]	V_{T0} [V]	L_{sat} [nm]
17	long	189.293	7.335	0.521	NAN
	short	189.293	6.558	0.520	3.652E+01
20	long	193.590	6.293	0.521	NAN
	short	193.590	5.614	0.520	3.743E+01
30	long	234.541	4.506	0.525	NAN
	short	234.541	3.945	0.522	4.672E+01
40	long	230.778	3.419	0.521	NAN
	short	230.778	3.036	0.519	4.377E+01
50	long	203.911	2.665	0.514	NAN
	short	203.911	2.426	0.512	3.538E+01
60	long	216.779	2.299	0.510	NAN
	short	216.779	2.141	0.508	3.327E+01
80	long	254.726	1.936	0.505	NAN
	short	254.726	1.790	0.502	3.671E+01
90	long	262.690	1.783	0.501	NAN
	short	262.690	1.666	0.498	3.439E+01
100	long	277.114	1.680	0.498	NAN
	short	277.114	1.579	0.495	3.384E+01
120	long	297.502	1.508	0.489	NAN
	short	297.502	1.431	0.486	3.303E+01
140	long	298.354	1.370	0.477	NAN
	short	298.354	1.324	0.475	2.576E+01
160	long	315.362	1.297	0.465	NAN
	short	315.362	1.267	0.463	2.145E+01
200	long	338.677	1.191	0.441	NAN
	short	338.677	1.191	0.441	1.000E-01
250	long	371.814	1.128	0.410	NAN
	short	371.814	1.128	0.410	9.197E-14
300	long	408.290	1.095	0.380	NAN
	short	408.290	1.095	0.380	2.615E-17

Table 6.8.: Fitted parameter of the simplified EKV model, on a PMOS transistor with $W = 10\,\mu m$ and $L = 0.36\,\mu m$. The applied drain voltage was $V_D = 1\,V$. Extraction strategy as described in section 5.1.3.

T	model type	$I_{spec\square}$ [nA]	n [1]	V_{T0} [V]	L_{sat} [nm]
17	long	189.293	7.335	0.521	NAN
	short	189.293	6.558	0.520	3.652E+01
20	long	193.590	6.293	0.521	NAN
	short	193.590	5.614	0.520	3.743E+01
30	long	234.541	4.506	0.525	NAN
	short	234.541	3.945	0.522	4.672E+01
40	long	230.778	3.419	0.521	NAN
	short	230.778	3.036	0.519	4.377E+01
50	long	203.911	2.665	0.514	NAN
	short	203.911	2.426	0.512	3.538E+01
60	long	216.779	2.299	0.510	NAN
	short	216.779	2.141	0.508	3.327E+01
80	long	254.726	1.936	0.505	NAN
	short	254.726	1.790	0.502	3.671E+01
90	long	262.690	1.783	0.501	NAN
	short	262.690	1.666	0.498	3.439E+01
100	long	277.114	1.680	0.498	NAN
	short	277.114	1.579	0.495	3.384E+01
120	long	297.502	1.508	0.489	NAN
	short	297.502	1.431	0.486	3.303E+01
140	long	298.354	1.370	0.477	NAN
	short	298.354	1.324	0.475	2.576E+01
160	long	315.362	1.297	0.465	NAN
	short	315.362	1.267	0.463	2.145E+01
200	long	338.677	1.191	0.441	NAN
	short	338.677	1.191	0.441	1.000E-01
250	long	371.814	1.128	0.410	NAN
	short	371.814	1.128	0.410	9.197E-14
300	long	408.290	1.095	0.380	NAN
	short	408.290	1.095	0.380	2.615E-17

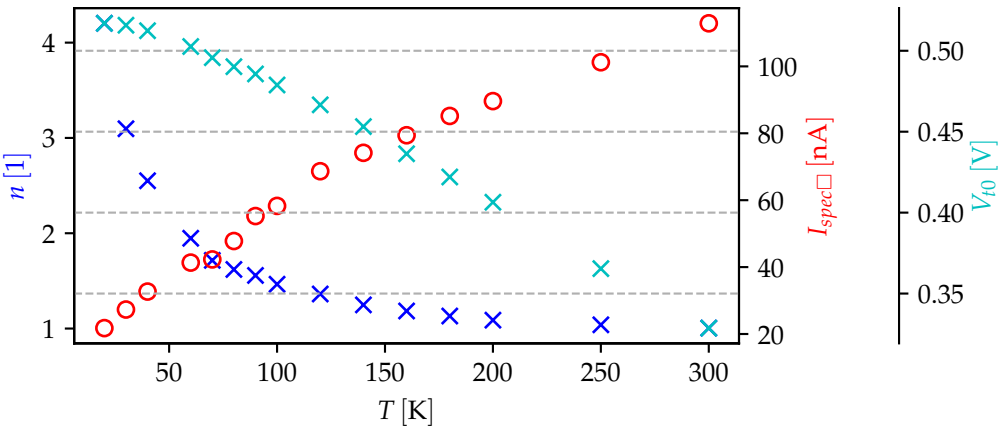

Figure 6.17.: Plot of the extracted parameter of the short channel simplified EKV model for a short PMOS transistor. Data of this plot can be found in the appendix 6.4.