Norbert Sailer, BSc

A Floating Differential Digital to Analog Converter for an Integrated Electrochemical Measurement System

Master's Thesis

to achieve the university degree of

Master of Science

Master's degree program: Electrical Engineering

submitted to

Graz University of Technology

Supervisor

Ass.-Prof. Dipl-Ing. Dr.techn. Mario Auer

Institute of Electronics
Head: Univ.-Prof. Dipl-Ing. Dr.techn. Bernd Deutschmann

Dipl-Ing. Markus Haberler
Infineon Technologies Austria AG

Graz, April 2020

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Acknowledgement

I would like to express my very great appreciation to Mario Auer for introducing me to the beauty of analog chip design. I am particularly grateful for the assistance given by my colleagues at Infineon Technologies Austria AG. I would like to thank my family for their unconditional support and love. Furthermore I would like to thank my friends for helping me become the person I am today.

Abstract

During the last decade, the number of wearable devices increased steadily [1]. Apparently, consumers are willing to use such devices for acquiring health and fitness parameters in order to improve their wellbeing. Electrochemical measurement procedures can be used to monitor additional physiological indicators in sweat or saliva and for biosensing in liquids. These applications require cheap, integrated and low-power electrochemical measurement systems.

This master's thesis addresses the design of a floating differential digital to analog converter (FD-DAC) for such a system, integrated in standard complementary metal-oxide semiconductor (CMOS) technology, capable of efficiently exploiting the limited supply voltage. Digital to analog converter (DAC) performance metrics, design trade-offs and various DAC architectures are discussed. Three different concepts for the implementation of a FD-DAC are proposed. The design process of the most suitable concept, based on two interpolated 8-bit resistor string (R-string) DACs, is described.

Post-layout simulations of the implemented 16-bit FD-DAC show the transient sinusoidal electrochemical impedance spectroscopy (EIS) waveform with a signal frequency of 10 kHz and an amplitude of 80 mV, while consuming 132 µW from a 3 V supply at a sample rate of 100 kS/s. The DAC's common-mode (CM) voltage is variable, thus the differential output voltage signal can float in the range from 0.2 V to 2.5 V.

Kurzfassung

Während des letzten Jahrzehnts nahm die Anzahl von Wearables stetig zu [1]. Offenbar sind die Verbraucher bereit solche Geräte zur Erfassung von Gesundheits- und Fitnessparametern zu verwenden, um ihr Wohlbefinden zu verbessern. Elektrochemische Messverfahren können zur Überwachung zusätzlicher physiologischer Indikatoren in Schweiß oder Speichel und zur Messung von Bioindikatoren in Flüssigkeiten verwendet werden. Voraussetzung dafür sind billige, integrierte und stromsparende elektrochemische Messsysteme.

Diese Masterarbeit befasst sich mit dem Entwurf eines floatenden Digital-Analog-Umsetzers (DAU) für ein solches integriertes System in komplementärer Metall-Oxid-Halbleiter (CMOS) Standardtechnologie. Das System ist in der Lage, die begrenzte Versorgungsspannung effizient auszunutzen. DAU Leistungsmetriken, Design Trade-offs und verschiedene DAU Architekturen werden besprochen. Es werden drei verschiedene Konzepte für die Implementierung eines schwebenden differentiellen DAUs vorgestellt. Der Entwurfsprozess des am besten geeigneten Konzepts, basierend auf zwei interpolierten 8-Bit Widerstandsleitern, wird beschrieben.

Post-Layout-Simulationen des implementierten 16-Bit DAUs zeigen den transienten Sinuskurvenverlauf einer elektrochemischen Impedanzspektroskopie (EIS) mit einer Signalfrequenz von 10 kHz und einer Amplitude von 80 mV. Der Leistungsverbrauch beträgt 132 µW aus einer 3 V Versorgung und einer Abtastrate von 100 kS/s. Die Gleichtaktspannung des DAUs ist variabel, dadurch kann sich das differentielle Ausgangsspannungssignal in einem Spannungsbereich von 0.2 V bis 2.5 V bewegen.

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1. Introduction

1.1. Motivation

A survey published by Accenture [1] in 2018 found out that the use of wearable devices by consumers has risen from 9 percent in 2014 to 33 percent in 2018. This trend is ongoing. In [2] the compound annual growth rate (CAGR) of wearables is predicted to be roughly 27 percent during the period from 2019 to 2027. It seems that consumers are willing to use such devices in order to improve their wellbeing. Commercially available wearables use non-invasive measurement techniques to acquire health and fitness parameters. For example, optical measurement methods are used to monitor physiological indicators such as heart rate [3] and blood oxygen levels [4]. Electrochemical measuring procedures can be used to analyze sweat [5] or saliva [6]. Research is currently carried out in the field of food safety [7] and diagnostics [8], [9]. This thesis aims to enable the transition from expensive and large electrochemical laboratory gauges to cheap and small integrated circuits (ICs) manufactured in standard complementary metal-oxide semiconductor (CMOS) technology.

1.2. Electrochemical Measurements

1.2.1. Electrochemical Measurement Methods

The underlying fundamental processes of electrochemistry are reduction-oxidation (redox) reactions, where electrons are transferred between chemical species. Oxidation is the loss of electrons, whereas reduction is the gain of electrons [10]. A common electrochemical measurement technique

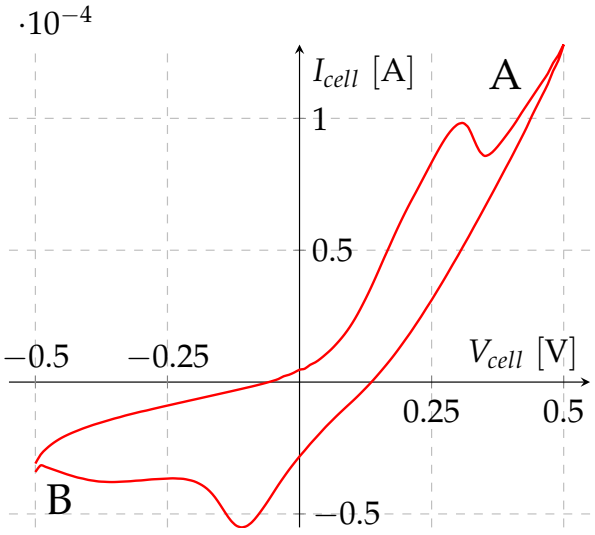
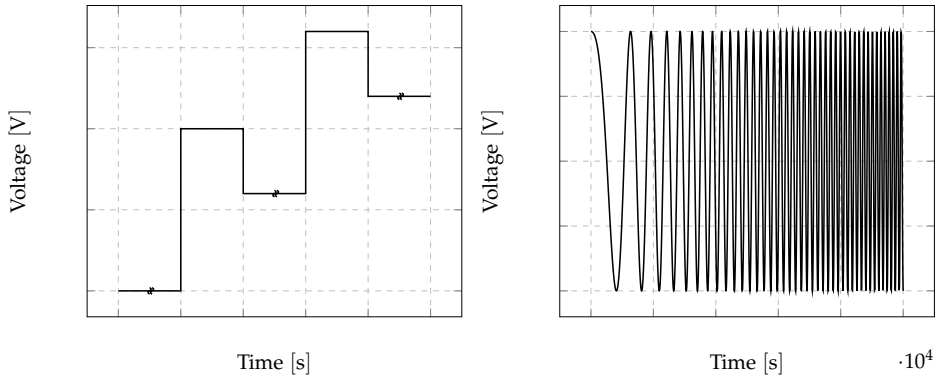


Figure 1.1.: Voltammogram of a cyclic voltammetry (CV) of orange juice with a scan rate of 60 mV/s. The voltage V_{cell} is swept from 0.5 V to −0.5 V and back to 0.5 V while the corresponding current, I_{cell}, trough the electrochemical cell was measured. Data provided by [14].

is called voltammetry [11]. In this method, a varying voltage, V_{cell}, is applied across an analyte. Due to redox reactions a current, I_{cell}, flows through the electrochemical cell. Information about the analyte is obtained by measuring I_{cell}. The plot of I_{cell} as a function of V_{cell} is called a voltammogram [12]. Figure 1.1 shows the voltammogram of a cyclic voltammetry (CV) of orange juice. V_{cell} was varied from 0.5 V to −0.5 V with a scan rate of 60 mV/s. As the potential is scanned negatively, from a higher potential at point A to a lower potential at point B, a reduction process takes place. Oxidation occurs when the potential is scanned positively, from a lower potential at point B to a higher potential at point A. Properties of chemical species can be assessed by the amplitude of the peak currents and their separation. CV was used in [13] to monitor sulphur dioxide levels during winemaking, a preservative to prevent undesirable reactions.

Another voltammetric method is the differential pulse voltammetry (DPV), where a staircase signal is applied to the electrochemical sensor [15]. An example waveform of a DPV is plotted in Figure 1.2a. I_{cell} is sampled



(a) Differential pulse voltammetry (DPV). (b) Electrochemical impedance spectroscopy (EIS).

Figure 1.2.: Typical excitation waveforms of electroanalytical methods.

immediately before the voltage pulse. As with the CV, the interpretation of the voltammogram allows to draw a conclusion about the analyte's electrochemical properties. An application of a DPV is the determination of antioxidant activity of red wines [16].

The frequency dependent behavior of an analyte can be measured with an electrochemical impedance spectroscopy (EIS) [17]. A sinusoidal signal is superimposed on a dc voltage. The sine's frequency can either be swept as shown in Figure 1.2b, or a single-frequency measurement is repeated for different frequencies. The result is represented graphically in a Nyquist plot. Applications for EIS measurements are reviewed in [18].

1.2.2. Architecture of Electrochemical Measurement Systems

Figure 1.3 shows the setup of an electrochemical measurement system according to [15], called potentiostat. This instrument consists of three controlled electrodes: the working electrode (WE), the reference electrode (RE) and the counter electrode (CE), respectively. A digital to analog converter (DAC) determines the voltage V_{cell} between the WE-RE pair, which is applied by two operational amplifiers (op-amps). In order to control this potential difference reasonably well, no current is allowed to pass through the RE. The reaction of interest takes places at the WE. The

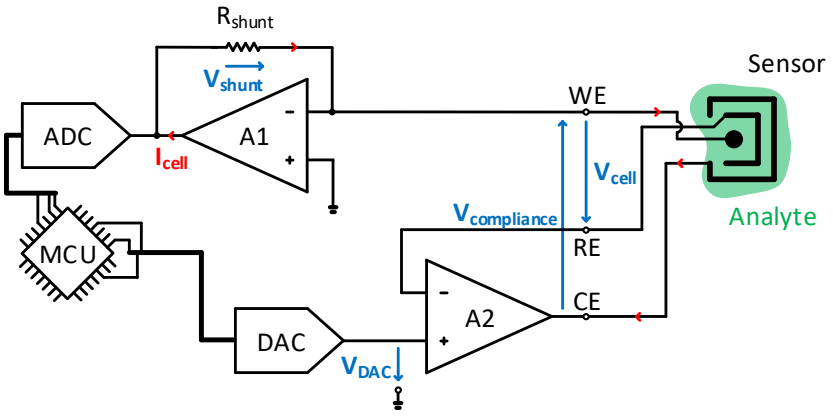
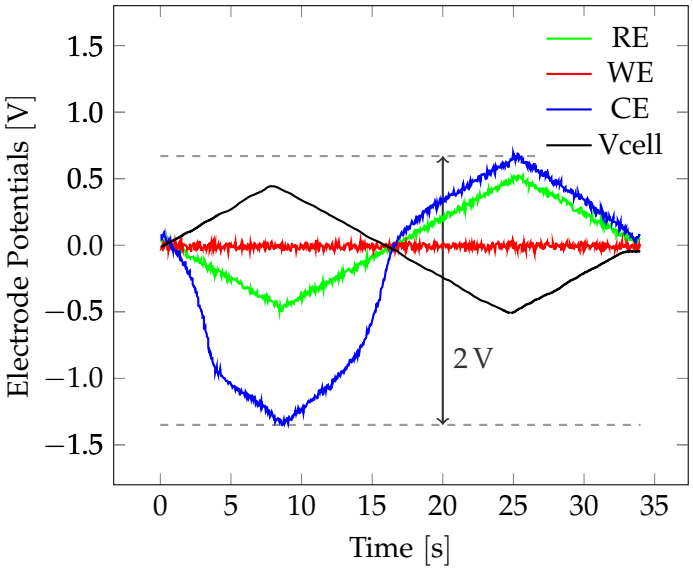


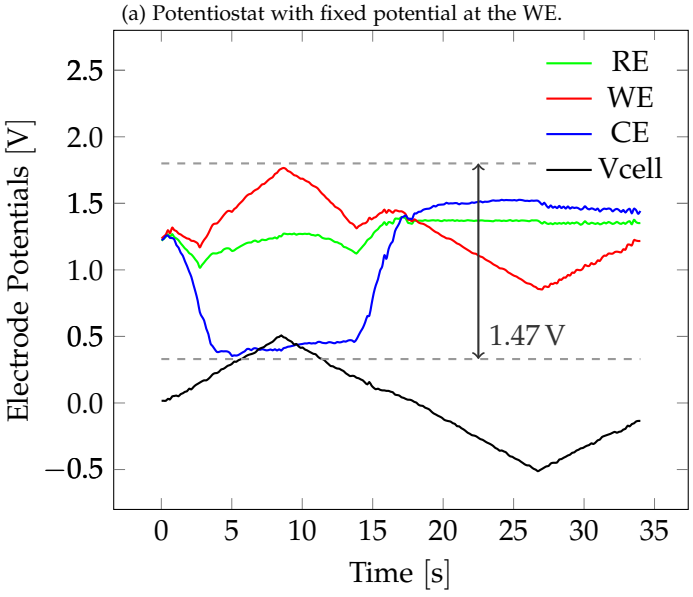
Figure 1.3.: Block diagram of an electrochemical measurement system consisting of an analog to digital converter (ADC), a single-ended digital to analog converter (DAC), two operational amplifiers (op-amps) in three electrode potentiostat configuration, a microcontroller unit (MCU) and a sensor covered with an analyte. The DAC determines the voltage V_{cell} between the working electrode (WE)-reference electrode (RE) pair, which is applied by two op-amps. A negative feedback adjusts the potential at the counter electrode (CE) in a way that I_{cell} can flow trough the sensor and the analyte. A transimpedance amplifier ($A1$ and R_{shunt}) converts I_{cell} into a voltage which is measured with an ADC. The whole test sequence and data processing is controlled by the MCU.

RE is a high impedance node. The potential at the CE is adjusted by a negative feedback loop in a way that I_{cell} can flow through the sensor and the analyte so as to balance the reaction at the WE. A transimpedance amplifier ($A1$ and R_{shunt}) converts I_{cell} into a voltage. This voltage is measured with an analog to digital converter (ADC). The whole test sequence and data processing is controlled by a microcontroller unit (MCU).

The compliance voltage, $V_{compliance}$, is the maximum potential difference a potentiostat can apply between the CE and the WE [19]. It determines the minimum supply voltage V_{DD} of the system and restricts the types of sensors that can be used. Commercial laboratory equipment keeps either the WE or the CE at a constant potential. This case is depicted in



(a) Potentiostat with fixed potential at the WE.



(b) Dynamic output voltage range exploitation as proposed in [14].

Figure 1.4.: Comparison of the electrode potentials of the cyclic voltammetry (CV) of Figure 1.1. The commercially available potentiostat keeps its working electrode (WE) at 0 V, whereas the dynamic voltage positioning proposed in [14] adjusts the electrode potentials more efficiently. Data provided by [14].

Figure 1.3, where the WE is set to 0 V. Figure 1.4a shows the electrode potentials during the CV performed in Figure 1.1. The $V_{compliance}$ needed is 2 V. In contrast, [14] could reduce the compliance voltage for the same measurement to 1.47 V by dynamically positioning the electrodes within the supply voltage range. Thus, enabling the measurement system to work with lower supply voltages. Figure 1.4b shows the electrode potentials during the CV performed in Figure 1.1 with dynamic output voltage range exploitation. However, this approach requires a differential DAC. In Figure 1.5, the block diagram of an electrochemical measurement system, capable of dynamic output voltage range exploitation, is redrawn. In order to fully benefit from this concept, the DAC has to be differential and floating. Only then two output voltages within the supply voltage range can be generated. The scope of this thesis is to design such a data converter as part of an electrochemical measurement system IC.

This thesis is structured as follows. Chapter 2 provides an overview of DAC performance metrics and converter architectures. Detailed specifications and a discussion about different concepts of the data converter can be found in Chapter 3. Design considerations for resistor string (R-string) DACs are covered in Chapter 4. Chapter 5 explains the design and the implementation of the DAC. The simulation results are analyzed in Chapter 6. Chapter 7 concludes this thesis by summarizing the design procedure.

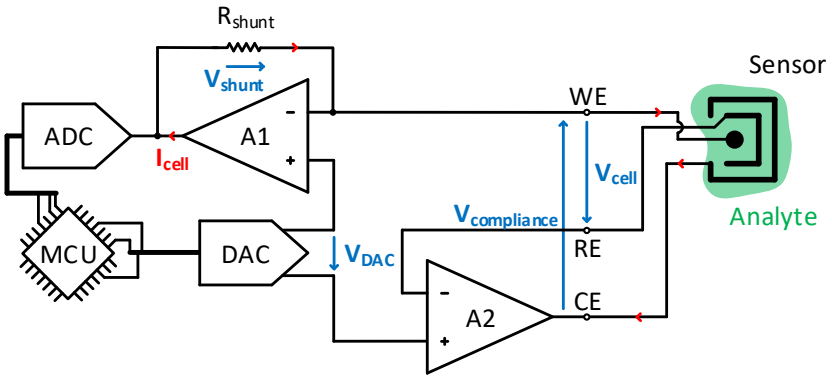


Figure 1.5.: Block diagram of an electrochemical measurement system consisting of an analog to digital converter (ADC), a differential digital to analog converter (DAC), two operational amplifiers (op-amps) in three electrode potentiostat configuration, a microcontroller unit (MCU) and a sensor covered with an analyte. The DAC determines the voltage V_{cell} between the working electrode (WE)-reference electrode (RE) pair, which is applied by two op-amps. A negative feedback adjusts the potential at the counter electrode (CE) in a way that I_{cell} can flow trough the sensor and the analyte. A transimpedance amplifier ($A1$ and R_{shunt}) converts I_{cell} into a voltage which is measured with an ADC. The whole test sequence and data processing is controlled by the MCU.

2. Digital to Analog Converters

Data converters are used as an interface between the analog and the digital domain. This chapter focuses on the digital to analog converter. Performance metrics and basic conversion principles are discussed.

2.1. DAC Basics

Figure 2.1 shows the block diagram of a mixed-signal processing system composed of a digital control circuit, an analog signal conditioning circuit and a sensor. In order to apply an analog voltage to the sensor, a DAC is used that transforms the digital information of the MCU to the analog domain of the sensor front-end. The block diagram of an N-bit DAC with a voltage output is depicted in Figure 2.2. D_{in}, the N-bit digital input signal, is decoded by a clocked decoder, thereby generating control signals for setting the corresponding switch positions for the digital to analog conversion. Conversion principles will be discussed in Section 2.3. The generated analog voltage V'_{out} is a fraction k of the reference voltage V_{ref}

$$\begin{aligned} V'_{out} &= k \cdot V_{ref} \,, \\ k &\in \left[0; \frac{2^N - 1}{2^N}\right] . \end{aligned} \tag{2.1}$$

The sample rate f_s of a DAC is equivalent to the frequency of the decoder's clock signal CLK. It has to be at least two times the signal bandwidth f_b in order to satisfy the Nyquist criterion. A reconstruction filter (RCF) removes the unwanted high frequency contents of the output signal V'_{out}. V_{out} is the filtered and buffered output voltage. A DAC with a resolution

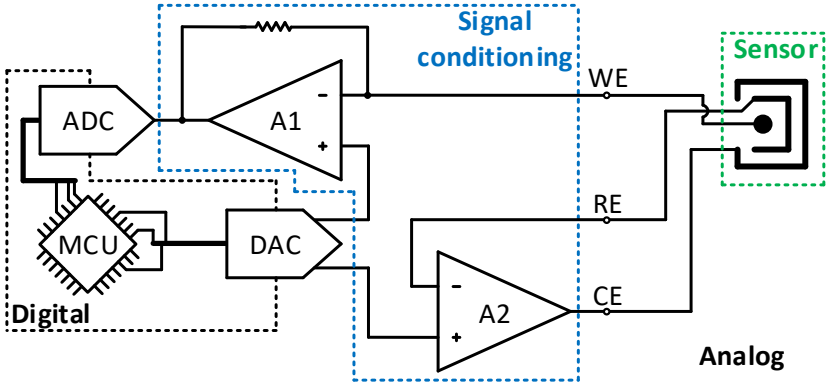


Figure 2.1.: Block diagram of a mixed-signal processing system. The analog to digital converter (ADC) and the digital to analog converter (DAC) interface the digital microcontroller unit (MCU) and control the signal conditioning circuitry which drives the sensor.

of N bit can generate 2^N states. Changing the input code by one least significant bit (LSB), increases or decreases the output voltage by

$$V_{LSB} = \frac{V_{ref}}{2^N} . \tag{2.2}$$

According to [20], the maximum analog output voltage V_{FS} is the difference between the analog output voltage for the smallest and largest digital input code and can be expressed as

$$V_{FS} = \frac{2^N - 1}{2^N} \cdot V_{ref} . \tag{2.3}$$

To work properly, DACs require a precise and stable reference voltage. Bandgap circuits [21] are capable of this task.

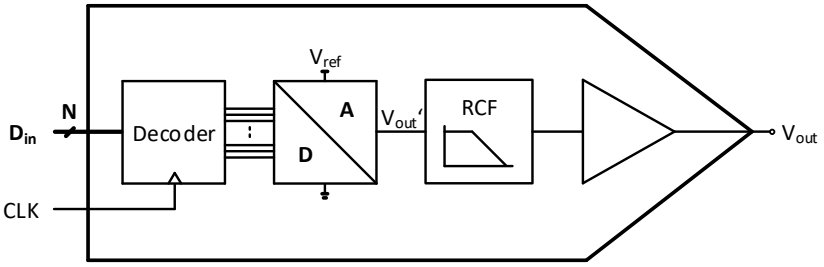


Figure 2.2.: Block diagram of a digital to analog converter (DAC). The N-bit digital input signal, D_{in}, is converted to an analog output voltage, V_{out}. D_{in} is decoded by a clocked decoder, thereby generating control signals for setting the corresponding switch positions for the digital to analog conversion. The generated analog voltage V'_{out} is a fraction of the reference voltage V_{ref}. A reconstruction filter (RCF) removes the unwanted high frequency contents of the output signal V'_{out}. V_{out} is the filtered and buffered output voltage.

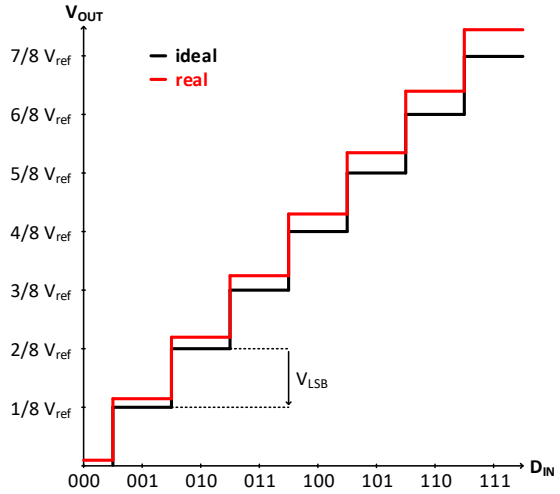
2.2. DAC Performance Metrics

To characterize DAC implementations, performance metrics are used. For explanation of these metrics, an ideal transfer characteristic of a 3-bit DAC is compared to an assumed transfer characteristic of a real 3-bit DAC in Figure 2.3a. Each digital input code, D_{in}, is assigned to an analog output voltage, V_{out}. This plot is used to derive static nonlinearties. The gain and offset error are depicted in Figure 2.3b. Reference [22] defines the offset error to be the output for a digital input code consisting of only zeros. The gain error is the deviation in slope of the actual DAC transfer characteristic from the ideal, when the offset error has been reduced to zero.

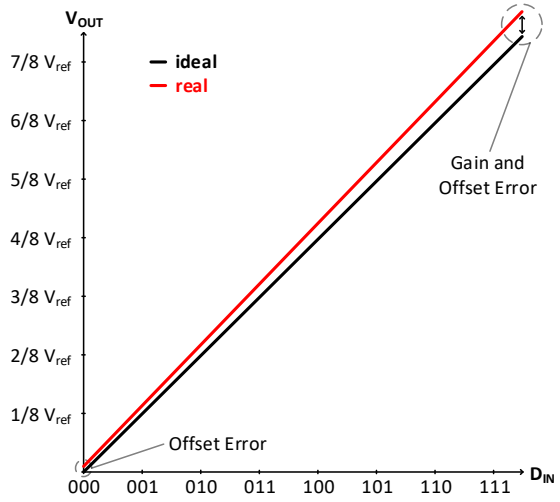
The differential nonlinearity (DNL) is defined as the difference between the actual step size and the ideal step size:

$$DNL_j = \left(V_j - V_{j-1}\right) - V_{LSB}\,. \tag{2.4}$$

Graphically, the DNL can be represented as shown in Figure 2.4a. The integral nonlinearity (INL) is defined as the difference between the actual



(a) Ideal and assumed real transfer characteristic of a 3-bit DAC.



(b) Gain and offset error of the transfer characteristic of the 3-bit DAC shown above in Figure 2.3a.

Figure 2.3.: Transfer characteristic of a 3-bit digital to analog converter (DAC). Each digital input code, D_{in}, is assigned to an analog output voltage, V_{out}.

analog output voltage and the ideal analog output voltage for the same digital input code:

$$INL_j = V_j - V_{j_{ideal}} \,. \tag{2.5}$$

Figure 2.4b illustrates this nonlinearity.

The ideal and real time domain output of a DAC is plotted in Figure 2.5. After a propagation delay the output voltage of the real DAC starts to rise. The slope is limited by the slew rate and settles after an overshoot.

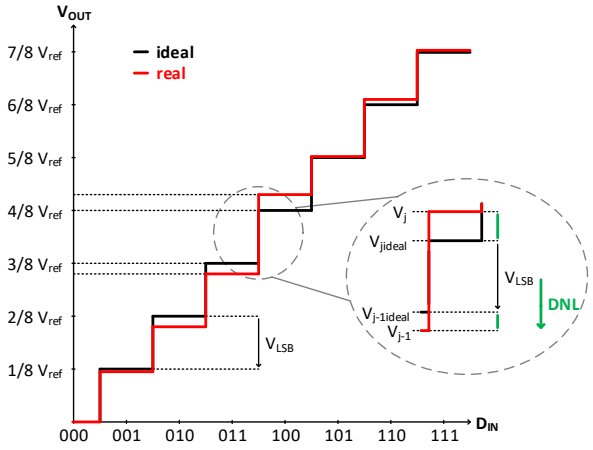
2.3. DAC Architectures

A rough overview of basic digital to analog conversion principles is depicted in Figure 2.6. The classification done by [20] was used as a basis. Reference [22] distinguishes two main types of data converters: Nyquist-rate and oversampling (OS) converters. The latter ones operate at much higher sample rates f_s than the signal's Nyquist-rate $2 \cdot f_b$ (up to 512 times faster). Speed is traded for a higher signal-to-noise ratio (SNR) [23]. In contrast, Nyquist-rate converters have a one-to-one correspondence between input and output samples.

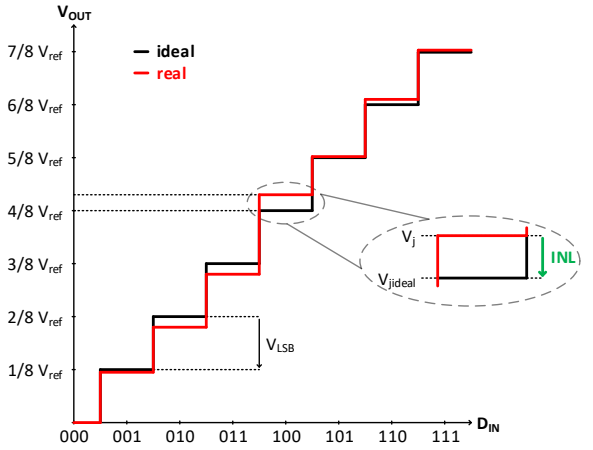
The simplest conversion principle is voltage division, where a voltage reference is divided by a series connection of equal resistors R. Figure 2.7 shows the schematic of a 3-bit R-string DAC. By closing the j-th switch the output voltage, V'_{out}, can be calculated:

$$\begin{aligned} V'_{out} &= \frac{j}{8} \cdot V_{ref} \,, \\ j &\in [0;7] \,. \end{aligned} \tag{2.6}$$

To achieve a resolution of N-bit, 2^N resistors are required. For high resolutions, the number of resistors increases considerably. The DAC depicted in Figure 2.8 uses an R-2R resistor network in order to divide a current into binary weighted partial currents. This topology achieves high resolutions



(a) Illustration of the DNL in a 3-bit DAC.



(b) Illustration of the INL in a 3-bit DAC.

Figure 2.4.: Nonlinearities of a digital to analog converter (DAC). The differential nonlinearity (DNL) is defined as the difference between the actual step size and the ideal step size: $DNL_j = (V_j - V_{j-1}) - V_{LSB}$. The integral nonlinearity (INL) is defined as the difference between the actual analog output voltage and the ideal analog output voltage for the same digital input code: $INL_j = V_j - V_{j_{ideal}}$.

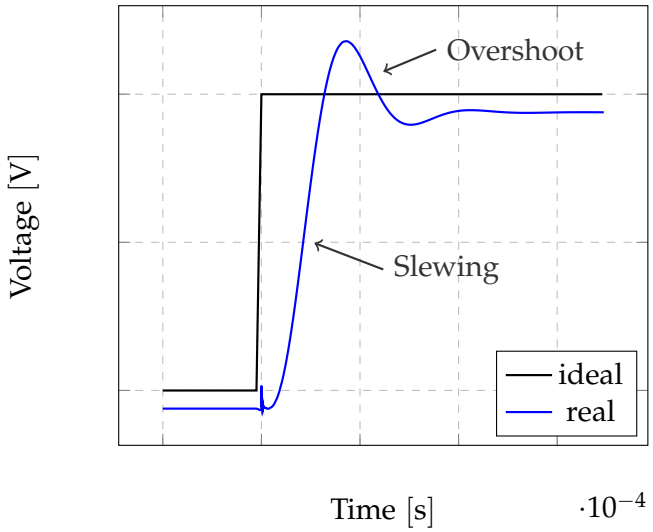


Figure 2.5.: Ideal and real time domain output of a digital to analog converter (DAC). The real response settles after slewing and an overshoot.

with less unit elements. A transimpedance amplifier converts the current I_R into an output voltage given by

$$V'_{out} = -I_R \cdot R = -\frac{j}{8}\frac{V_{ref}}{R} \cdot R = -\frac{j}{8} \cdot V_{ref} \,, \qquad j \in [0;7] \,. \tag{2.7}$$

The switches are controlled by a binary coding scheme as explained in Table 2.1, where 0 means that the switch is opened and 1 that it is closed.

Another conversion scheme works in the current domain. Figure 2.9 shows the schematic of a 3-bit current steering DAC. A reference current I_{ref}, which is derived from a reference voltage and a resistor, is replicated by multiple, binary or unary scaled, current sources. Same as the R-2R

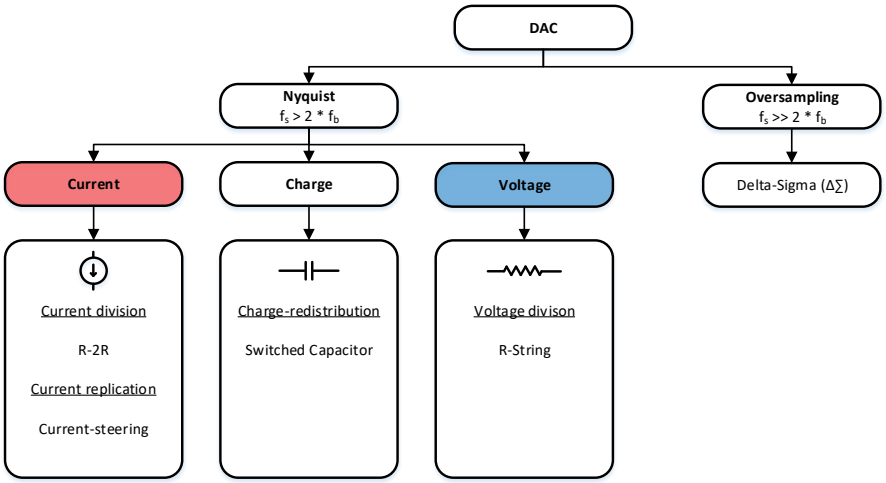


Figure 2.6.: Classification of digital to analog converters (DACs). Two main types can be distinguished: Nyquist-rate and oversampling converters. Nyquist DAC architectures can further be separated in their domain of operation, that is current, charge and voltage. Multiples or fractions of a reference voltage or current can be generated by replication or division.

Table 2.1.: Conversion of a decimal to a 3-bit binary number.

Decimal Number	Binary Number		
j	S_3	S_2	S_1
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

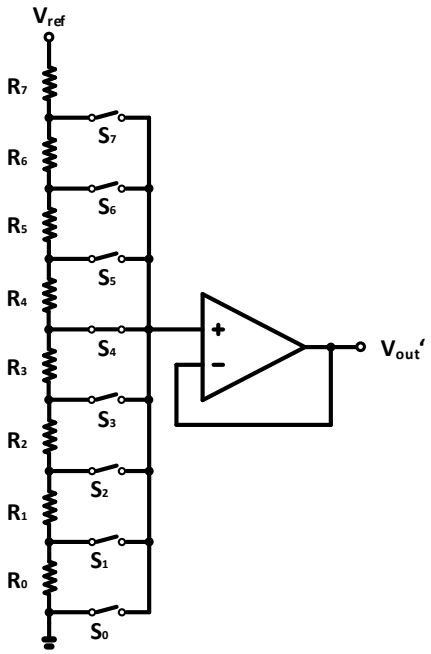


Figure 2.7.: Schematic of a 3-bit resistor string (R-string) digital to analog converter (DAC). A fraction of the reference voltage V_{ref} is generated by closing one of the switches. A buffer avoids loading of the R-string.

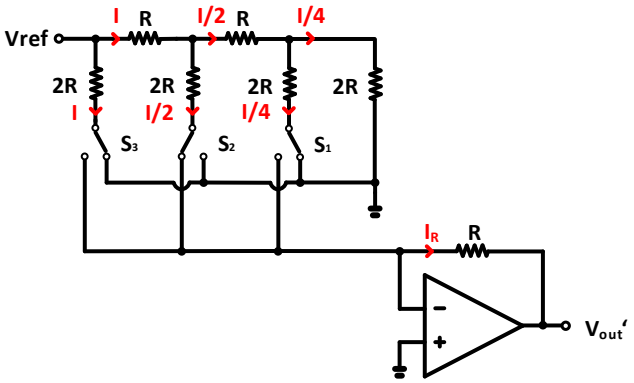


Figure 2.8.: Schematic of a 3-bit R-2R digital to analog converter (DAC). A resistor network divides a current into binary weighted partial currents. I_R depends on the switch positions and is converted to an output voltage by a transimpedance amplifier.

architecture, the current is converted into an output voltage:

$$V'_{out} = -I_R \cdot R = -jI_{ref} \cdot R = -j\frac{V_{ref}}{8R} \cdot R = \frac{j}{8} \cdot V_{ref}\,, \quad j \in [0;7]\,. \tag{2.8}$$

Switched capacitor (SC) circuits transfer charges between capacitors. Figure 2.10 shows a 3-bit charge-redistribution DAC. During the reset phase all capacitors are discharged. Next, the input capacitors are either charged to V_{ref} or left discharged, depending on the switch position in the sample phase. During the next phase, the total stored charge Q is transferred to the output capacitor:

$$V'_{out} = \frac{Q}{8C} = \frac{jCV_{ref}}{8C} = \frac{j}{8} \cdot V_{ref}\,, \quad j \in [0;7]\,. \tag{2.9}$$

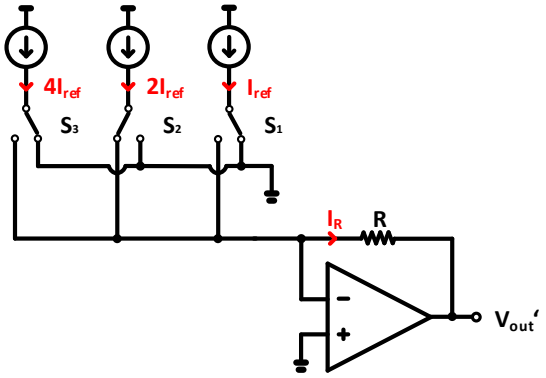


Figure 2.9.: Schematic of a 3-bit current-steering digital to analog converter (DAC). A reference current I_{ref} is replicated by multiple, binary or unary scaled, current sources. I_R depends on the switch positions and is converted to an output voltage by a transimpedance amplifier.

The unit elements, resistors, transistors and capacitors, of the DAC architectures mentioned so far determine the precision of the converter. OS DACs relax the accuracy requirements of the analog components by increasing the sample rate to values much higher than the Nyquist-rate and by applying noise shaping. Figure 2.11 shows the block diagram of a delta-sigma ($\Delta\Sigma$) DAC. The sample rate of the input data, f_{in}, is increased to f'_{in} by the interpolation filter (IF). Noise is then shifted out of the signal's bandwidth by the noise-shaping loop (NL), increasing the SNR. Usually, multi-bit DACs are used for $\Delta\Sigma$ converters [23].

Figure 2.12 compares the previously mentioned DAC architectures regarding speed and resolution. Clearly, a trade-off between those two performance metrics exists. DACs from [24]–[28] were used for the comparison.

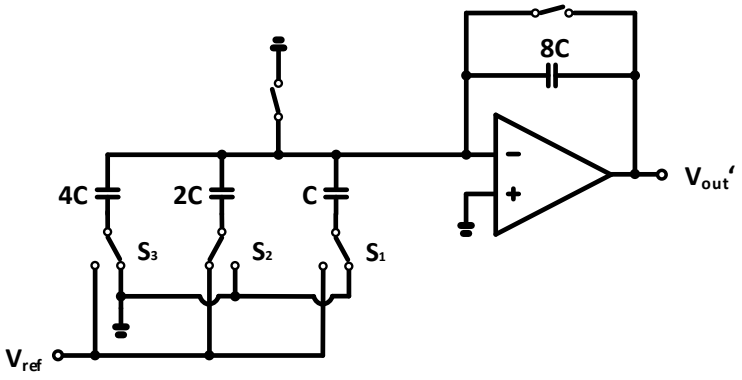


Figure 2.10.: Schematic of a 3-bit charge-redistribution digital to analog converter (DAC). The input capacitors are either charged to the reference voltage V_{ref} or left discharged, depending on the switch position in the sample phase. During the next phase, the total stored charge is transferred to the output capacitor.

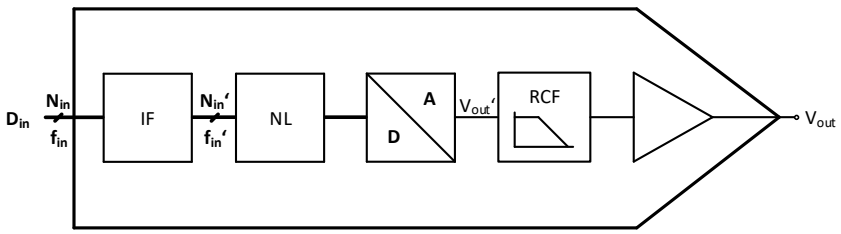


Figure 2.11.: Block diagram of a delta-sigma ($\Delta\Sigma$) digital to analog converter (DAC). The sample rate of the input data, f_{in} is increased by the interpolation filter (IF). Noise is then shifted out of the signal's bandwidth by the noise-shaping loop (NL) increasing the signal-to-noise ratio (SNR). The digital to analog conversion can be implemented by the principles discussed in Section 2.3. A reconstruction filter (RCF) removes the unwanted high frequency contents of the output signal V'_{out}. V_{out} is the filtered and buffered output voltage.

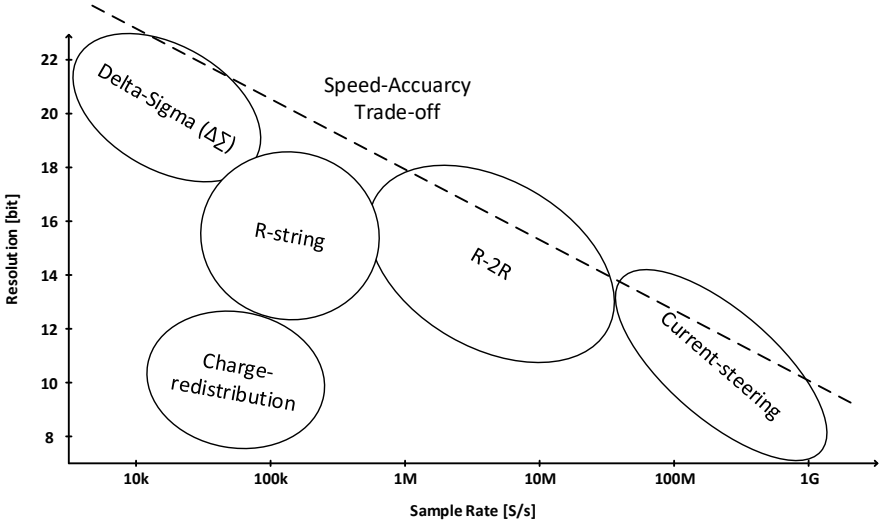


Figure 2.12.: Comparison of different digital to analog converter (DAC) types regarding speed and resolution. A trade-off between speed and accuracy is indicated by the dashed line.

3. Concept Considerations

A floating differential digital to analog converter (FD-DAC) is required for the application in the electrochemical measurement system as discussed in Section 1.2.2. In the first part of this chapter, the design specifications of the digital to analog converter are summarized. Based on these requirements three possible implementation options of a FD-DAC are discussed.

3.1. Application Related DAC Specifications

As discussed in Chapter 1, the DAC has to be differential. In addition, the two output voltages have to be shifted between 200 mV and 2.5 V for a power supply of 3 V. Power consumption should be low, as the integrated measurement system is battery powered or supplied by harvested energy [29]. The electrochemical sensors require the output signal to have a full-scale range of 800 mV and a step size of 100 µV. According to Equation 3.1, the DAC requires a resolution of 13 bit. Steep edges are required for the DPV, whereas the EIS needs an RCF for sinusoidal voltage characteristics. The maximum required signal output frequency is 10 kHz. Since many applications require single-ended voltages, the converter has to be able to provide output voltages referred to the system's ground as well. Table 3.1 summarizes all specifications of the DAC.

$$N = \log_2\left(\frac{V_{FS}}{V_{LSB}}\right) = \log_2\left(\frac{800\,\mathrm{mV}}{100\,\mu\mathrm{V}}\right) = 13bit \tag{3.1}$$

Table 3.1.: Specifications of the floating differential digital to analog converter (FD-DAC).

Parameter		Value	Unit
Supply voltage	V_{DD}	3	V
Temperature range		$-20 \leftrightarrow +80$	°C
Floating range		$0.2 \leftrightarrow 2.5$	V
Full-scale	V_{FS}	800	mV
LSB	V_{LSB}	100	µV
Resolution	N	13	bit
Sample rate	f_s	> 20	kS/s
Slew rate	SR	5	$\mathrm{mV\,\mu s^{-1}}$

3.2. Concept 1 - Voltage Domain Voltage Adding

Figure 3.1 depicts the first considered concept. It is based on adding two single-ended voltages V_{out} and V_{pos}, to generate a differential voltage V_{cell}. The positioning voltage V_{pos} determines the offset, V_{out} the amplitude. Any DAC architecture with a voltage output can be used to implement this concept.

To superimpose the two voltages, two possibilities are considered, where V_{sum} is the output voltage of the summing block. In the first, a non-inverting summing amplifier as shown in Figure 3.2a controls V_{sum} as follows:

$$V_{sum} = \frac{V_{out} + V_{pos}}{2} \cdot \left(1 + \frac{R_f}{R}\right) . \tag{3.2}$$

If $R_f = R$ the gain of the summing amplifier is one. The second possibility makes use of a differential difference amplifier (DDA), introduced by [30]. In contrast to the op-amp, the difference between two differential voltage inputs is set to zero by negative feedback. The DDA converts the voltage differences into currents which are then subtracted, converted back into the voltage domain and amplified. Figure 3.2b shows a DDA based adder circuit where

$$V_{sum} = V_{out} + V_{pos} . \tag{3.3}$$

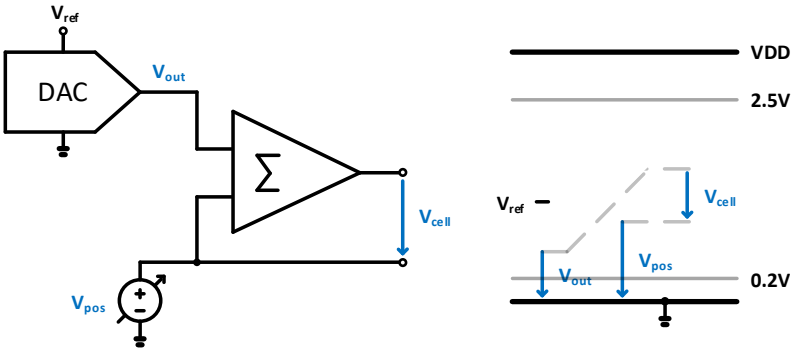


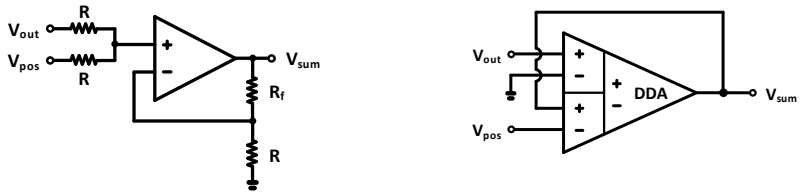
Figure 3.1.: Digital to analog converter (DAC) concept 1: Voltage domain voltage adding. A voltage summing block generates a differential voltage V_{cell} by adding the two single-ended voltages V_{out} and V_{pos}. Two possible implementations of the voltage adder are depicted in Figure 3.2.

A low-voltage rail-to-rail CMOS version of a DDA was implemented by [31].

The design of a DDA is more complex than the design of an op-amp, whereas the non-inverting summing amplifier is loading the DAC. Concept 1 is simple and versatile. By bypassing the summing amplifier two independent single-ended voltages can be generated.

3.3. Concept 2 - Current Domain

A FD-DAC can be implemented as a fully differential current-steering DAC, where the output common-mode voltage level $V_{CM_{out}}$ is controlled by V_{pos}. Figure 3.3 shows the circuit. As already concluded in Chapter 2 (Figure 2.12), current-steering DACs are used for high-speed applications, implying a high power consumption. Assuming 10 nA as the LSB current



(a) Non-inverting summing amplifier.

(b) Differential difference amplifier (DDA) based adder.

Figure 3.2.: Implementations of a voltage summing block. The output voltage V_{sum} of the voltage adder circuits is $V_{sum} = V_{out} + V_{pos}$. This is the case if the feedback resistor R_f of the non-inverting summing amplifier is equal to R.

for a 13-bit current steering DAC would give a total current of

$$I_t = 10\,\text{nA} \cdot 2^{13} = 81.92\,\mu\text{A}\,. \tag{3.4}$$

A low-power implementation of a fully differential current-steering DAC for 13-bit is not possible.

3.4. Concept 3 - Current Domain Resistor String

Concept 3 is a modified R-string DAC. Instead of a reference voltage V_{ref}, a reference current

$$I_{ref} = \frac{V_{ref}}{R} \tag{3.5}$$

is injected into the top of the resistor ladder. If the total resistance of the R-string matches R, the voltage across the resistors is equal to V_{ref}. The absolute voltage levels referred to ground (V_{posp} and V_{posm}) can be set by V_{pos} and the arrangement as a feedback system as shown in Figure 3.4. An advantage of this topology is that the negative feedback reduces the output resistance of the R-string DAC. The two high impedance nodes might make it difficult to compensate this system.

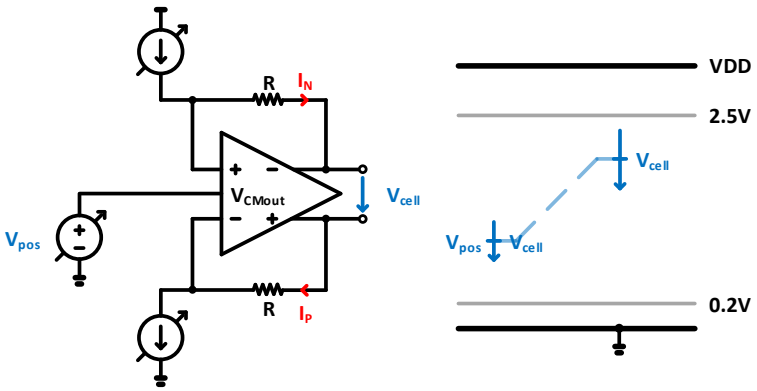


Figure 3.3.: Digital to analog converter (DAC) concept 2: Fully-differential current-steering architecture. The amplitude of the fully-differential output signal is set by the currents I_N and I_P and the output common-mode voltage level $V_{CM_{out}}$ is equal to V_{pos}.

An optimized version of concept 3 was chosen for the implementation of the FD-DAC, as it best fulfills the requirements and allows easy integration with the rest of the integrated electrochemical measurement system. As can be seen from Figure 3.5 the R-string DAC was taken out of the feedback-loop and decoupled by two op-amps (A1 and A2), as switching in the feedback path might cause disturbances. In this implementation, two identical 8-bit R-strings can be either interpolated as one 16-bit DAC or used as two independent 8-bit DACs. In both, the low and the high-resolution mode, single-ended, differential, dc (steep edges) or ac (sinusoidal) output voltages can be generated. This configurability is implemented by switches and an analog multiplexer (ANA MUX).

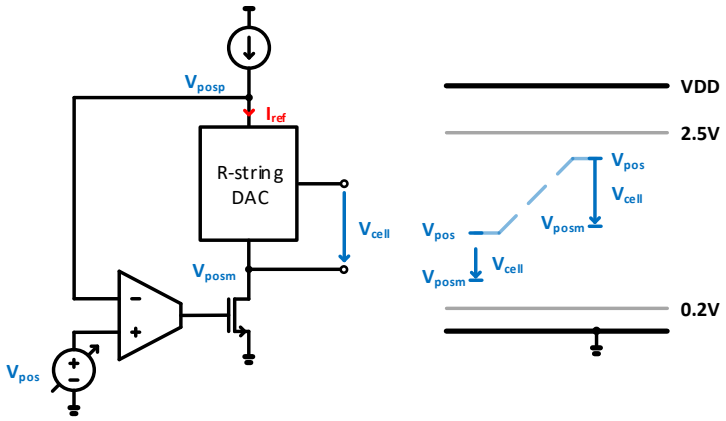


Figure 3.4.: Digital to analog converter (DAC) concept 3: Current domain resistor string (R-string) architecture. The voltage at the top of the R-string V_{posp} is set to V_{pos} by a negative feedback loop. The voltage drop across the R-string is determined by the reference current I_{ref} and the total resistance of the R-string.

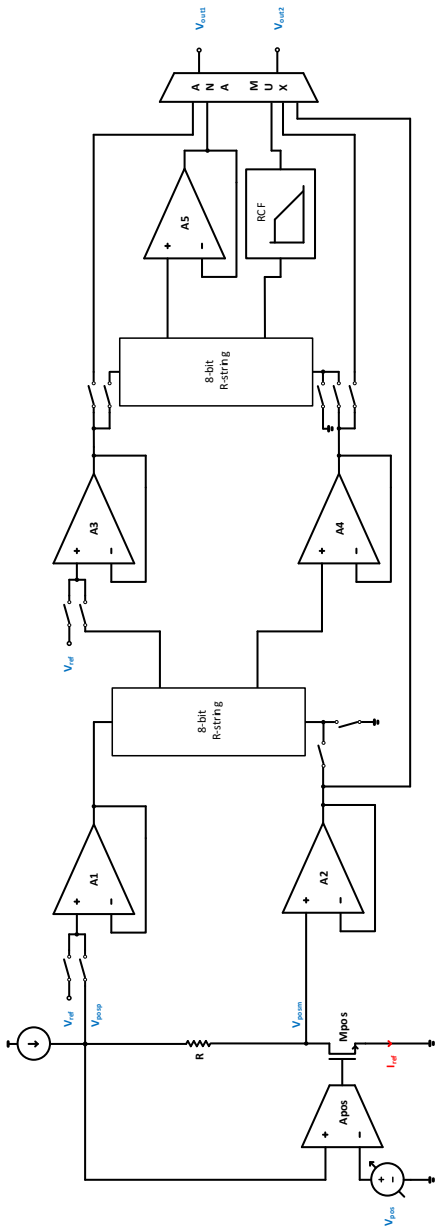


Figure 3.5: Final concept of the floating differential digital to analog converter (FD-DAC). Amplifier A_{pos}, transistor M_{pos} and the reference current source generate a floating reference voltage for the FD-DAC. The two identical 8-bit resistor strings (R-strings) can be either interpolated as one 16-bit digital to analog converter (DAC) or used as two independent 8-bit DACs. In both, the low and the high-resolution mode, single-ended, differential, dc (steep edges) or ac (sinusoidal) output voltages can be generated. This configurability is implemented by switches and an analog multiplexer (ANA MUX).

4. Design Considerations for R-string DACs

The FD-DAC implemented for the electrochemical measurement system is based on R-string DACs. A detailed analysis of this architecture is done in this Chapter.

4.1. Number of Devices

An N-bit R-string DAC, as drawn in Figure 2.7, requires 2^N resistors and switches. As can be seen from the logarithmic plot in Figure 4.1, 1 024 devices are needed for a 10-bit, and 65 536 devices for a 16-bit implementation. This number can be reduced by interpolation. Figure 4.2 shows, that a DAC can be decomposed into a coarse and a fine R-string. Hence, by interpolation the LSB voltage of the coarse string is subdivided by the fine resistor ladder. The total DAC resolution N is the sum of the individual resolutions, that is

$$N = N_c + N_f \,, \tag{4.1}$$

where N_c and N_f are the resolutions of the coarse and the fine DAC ladders. For example, a 16-bit DAC can be composed of two 8-bit DACs. The minimum number of resistors can be achieved by choosing

$$N_c = N_f = \frac{N}{2} \,, \tag{4.2}$$

thus reducing the required number of resistors from 2^N to $2 \cdot 2^{\frac{N}{2}}$. For a resolution of 16-bit this leads to a reduction by a factor of about 100 (from 65 536 to 512) as plotted in Figure 4.1.

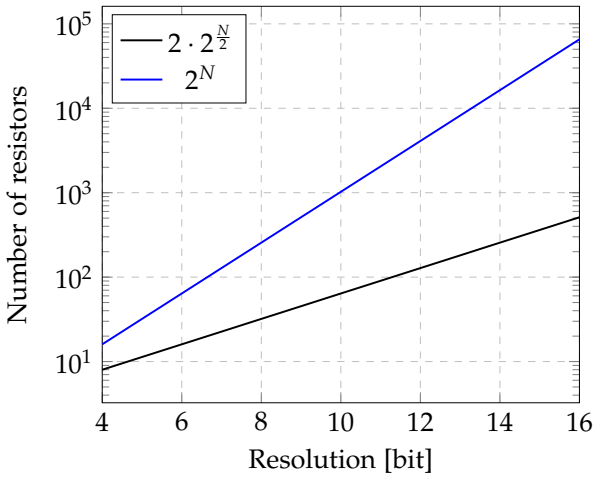


Figure 4.1.: Number of resistors needed for a N-bit resistor string (R-string) digital to analog converter (DAC). The standard architecture depicted in Figure 2.7 requires 2^N resistors. This number can be reduced to $2 \cdot 2^{\frac{N}{2}}$ by interpolating according to Equation 4.2.

Interpolation has the disadvantage that the coarse R-string is loaded by the fine string, decreasing the total resistance, R_t, from

$$R_t = 2^{N_c} R_c \tag{4.3}$$

to

$$R_t' = \left(2^{N_c} - 1\right) R_c + \left(R_c \parallel 2^{N_f} R_f\right) . \tag{4.4}$$

This increases the current and hence, the voltage drop across each resistor, except for the interpolated one. The schematic of Figure 4.3 was used to simulate the loading effect. Simulation results are plotted in Figure 4.4, where Vc are the ideal results and Vc_{int} the deteriorated results due to interpolation. The larger the ratio of the total resistance of the fine R-string ($2^{N_f} R_f$) to the unit resistance of the coarse string (Rc), the smaller the error. This is undesirable, since it leads to an increased R_{out}, as will be further discussed in Section 4.4. Furthermore the two R-strings are coupled. Feedback of the switching operations might decrease the performance of the rest of the circuit. To avoid this, a decoupling stage is necessary.

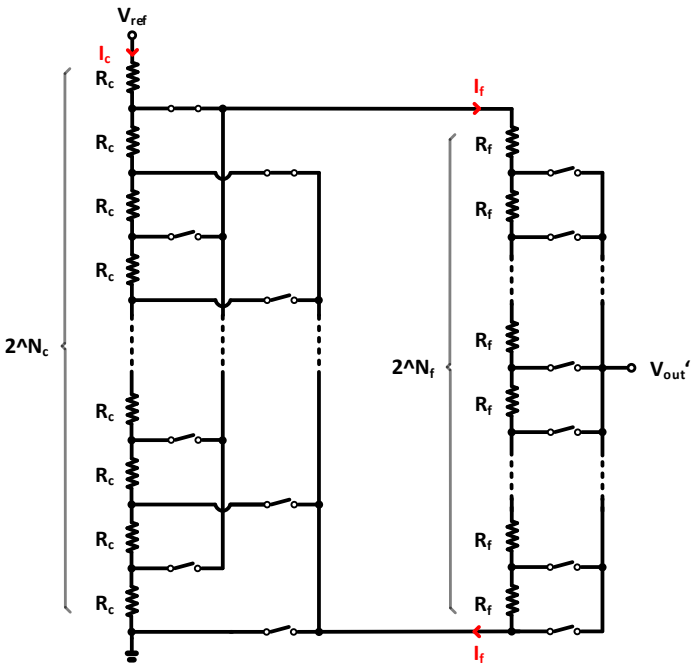


Figure 4.2.: Basic principle of interpolation. The voltage across one of the unit resistors R_c of the coarse resistor string (R-string) is subdivided by the fine resistor ladder. The total digital to analog converter (DAC) resolution is the sum of the individual resolutions of the R-strings $N_c + N_f$. Without a decoupling stage, the coarse R-string is loaded by the current I_f trough the fine R-string, changing the node potentials of the coarse resister ladder compared to an implementation without interpolation.

Reference [27] used two op-amps as shown in Figure 4.5a. The amplifiers have to be sufficiently fast and their offsets affect the linearity of the converter, as will be discussed in Section 4.3. Input and output common-mode ranges of the op-amps limit the voltage range of the DAC. The use of source followers is suggested by [32] in order to increase the speed. An up and a down shift, or vice versa, are necessary to reach the original voltage level. The mismatch in the gate source voltages of the n-type metal-oxide-semiconductor (NMOS) and the p-type metal-oxide-semiconductor (PMOS) transistors affects the linearity of the converter. Lu and others [33] used two source followers of the same type to avoid offset errors at the expense of increased complexity. Figure 4.5b depicts a decoupling scheme proposed by [34]. A compensation current, I_{compp}, is injected into the top of the fine R-string. If the current I_{compn}, drawn by the current sink, is equal to I_{compp}, I_{L1} and I_{L2} are zero. Hence, no loading of the coarse string happens. The difference in $I_{compp} - I_{compn}$, due to mismatch of current mirrors and the finite output resistance of the current source and sink, determines the loading of the coarse resistor ladder and thus the linearity of the DAC. Only low speeds can be achieved as the output resistance is high.

4.2. Types of Resistors

Poly or diffusion resistors are commonly used for R-string DACs [35]–[37]. A comparison of their performance regarding voltage and temperature stability shows that poly resistors are superior for the application in R-string DACs. This is simulated in Figure 4.6. The reason is the voltage and temperature dependency of the width of the depletion region between the diffused material and the substrate.

The mismatch of two resistors R and R', caused by random process fluctuations, is defined as

$$\frac{\Delta R}{R_m} = \frac{R - R'}{\frac{(R+R')}{2}}, \tag{4.5}$$

where ΔR is the difference in resistance between the two resistors and R_m their mean value. Figure 4.7 shows the top view of an integrated resistor

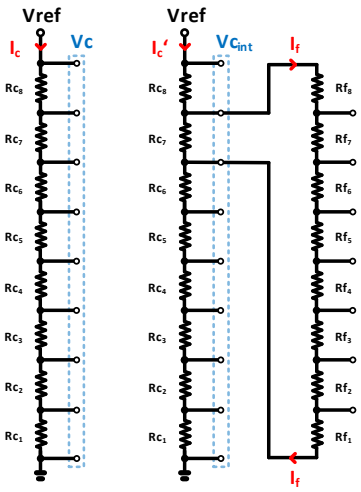


Figure 4.3.: Schematic for simulating the loading effect caused by interpolation. The node potentials of an unloaded resistor string (R-string) Vc are compared to the coarse resistors ladder's node potentials Vc_{int} of an interpolated R-string.

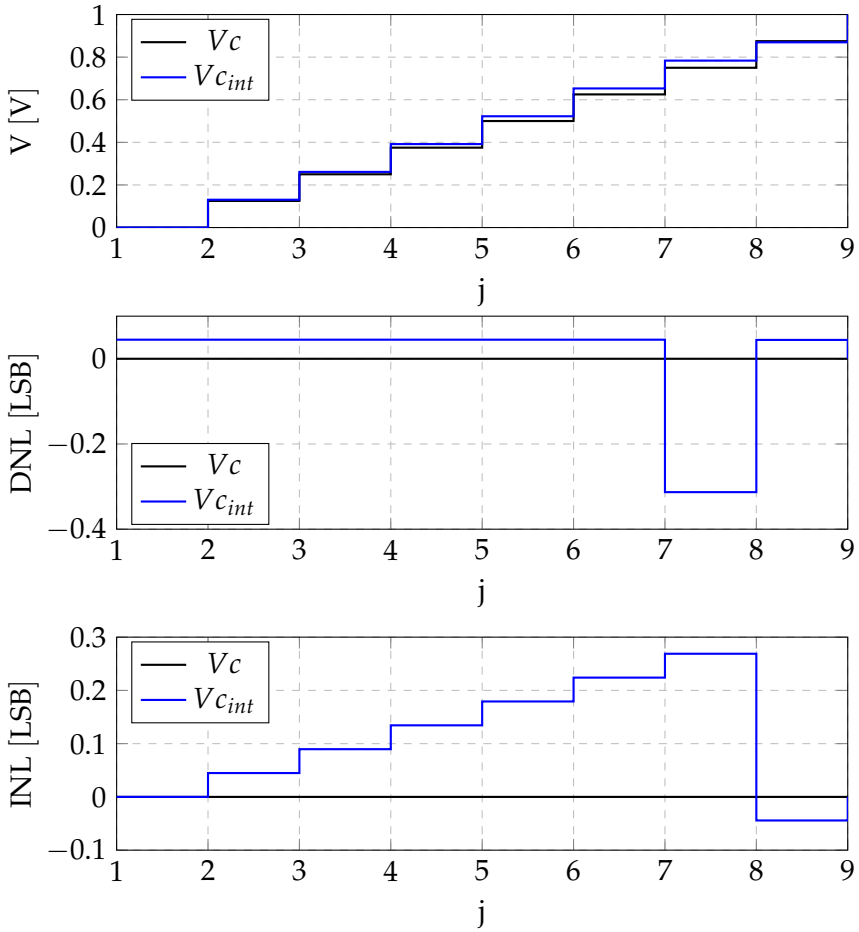
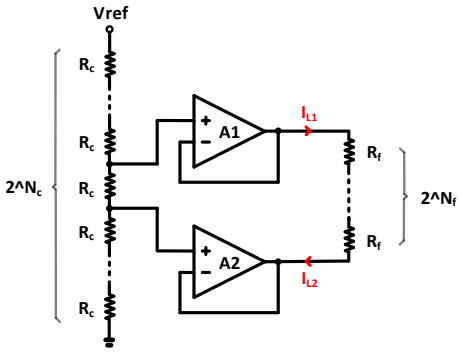
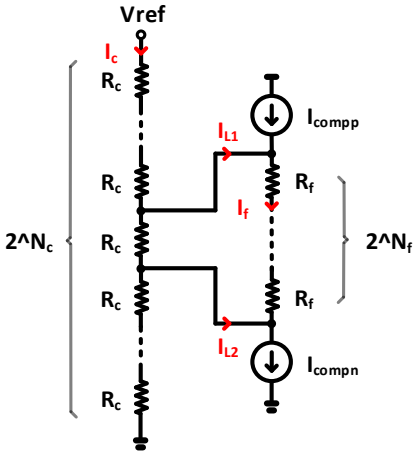


Figure 4.4.: Simulation results of the loading effect caused by interpolation of the circuit depicted in Figure 4.3. The node potentials of an unloaded resistor string (R-string) Vc are compared to the coarse resistors ladder's node potentials Vc_{int} of an interpolated R-string. Top: Node voltages as a function of the tap position. Middle: Differential nonlinearity (DNL) as a function of the tap position. Bottom: Integral nonlinearity (INL) as a function of the tap position.



(a) Decoupling with operational amplifiers (op-amps): No current flows into the high impedance inputs of the op-amps, hence the coarse R-string is not loaded.



(b) Decoupling with compensation currents: If the currents of the compensation current source, I_{compp}, and compensation current sink, I_{compn}, are equal ($I_{compp} = I_{compn}$), the coarse R-string is not loaded ($I_{L1} = I_{L2} = 0$).

Figure 4.5.: Decoupling schemes for interpolated resistor string (R-string) digital to analog converters (DACs) avoiding the loading effect.

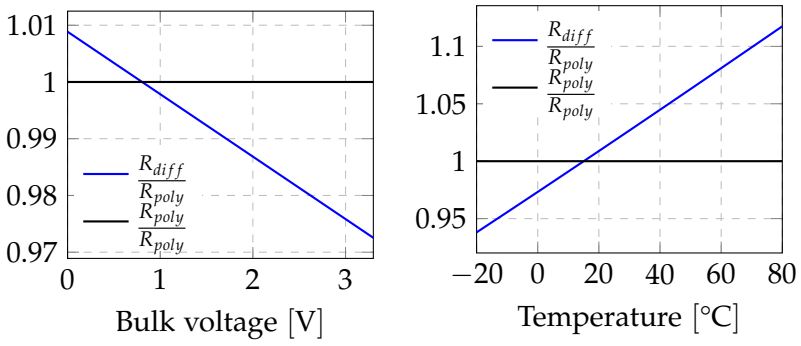


Figure 4.6.: Performance comparison of a poly resistor R_{poly} with a diffusion resistor R_{diff}. Left: Normalized resistance as a function of the bulk voltage. Right: Normalized resistance as a function of the temperature. The performance of diffusion resistors is worse than the performance of poly resistors due to the voltage and temperature dependency of the width of the depletion region between the diffused material and the substrate.

with width W and length L. Process variations change the dimensions to W' and L', that is a reduction by $\Delta e = W - W' = L - L'$ for the depicted case. Neglecting the contact resistance, the resistance of an integrated resistor is calculated as

$$R = R_{\square} \frac{L}{W}, \tag{4.6}$$

where $R_{\square}$ is the sheet resistance in $\Omega/\square$ and W and L the dimensions of the resistor in µm. Combining Equation 4.5 and 4.6 gives

$$\frac{\Delta R}{R_m} = \frac{R - R'}{\frac{(R+R')}{2}} = \frac{R_{\square}\frac{L}{W} - R_{\square}\frac{L-2\Delta e}{W-2\Delta e}}{\frac{R_{\square}\frac{L}{W} + R_{\square}\frac{L-2\Delta e}{W-2\Delta e}}{2}}. \tag{4.7}$$

Pelgrom and others [38] measured that the standard deviation (σ) of the mismatch is inversely proportional to the square root of the area:

$$\sigma\left(\frac{\Delta R}{R_m}\right) = \frac{A_R}{\sqrt{WL}}. \tag{4.8}$$

A_R is a technology dependent parameter. Usually, L is significantly larger for resistors than W, therefore W determines the matching. The plot in

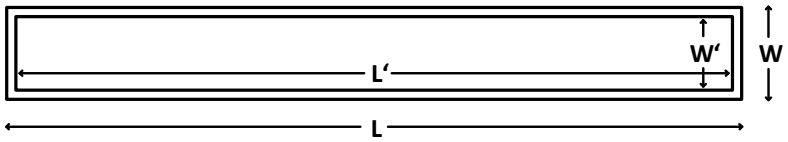


Figure 4.7.: Top view of an integrated resistor with width W and length L. Random process fluctuations cause a change in dimensions to W' and L'.

Figure 4.8 confirms the relationship between resistor width and mismatch. Equation 4.7 was plotted with a L to W ratio of 10, Δe was kept constant at 0.1.

4.3. Nonlinearities

In Section 2.2 DAC nonlinearities were already defined. In R-string DACs, these errors mainly result from mismatch in the resistors compromising the ladder [39]. Using Equation 2.4 and taking only resistor mismatch into account, the DNL of an R-string DAC was derived:

$$
\begin{aligned}
DNL_j &= \left(V_j - V_{j-1}\right) - V_{LSB} = \\
&= V_{ref}\frac{jR + \sum_{n=0}^{j}\Delta R_n}{2^N R + \sum_{n=0}^{2^N}\Delta R_n} - V_{ref}\frac{(j-1)\,R + \sum_{n=0}^{j-1}\Delta R_n}{2^N R + \sum_{n=0}^{2^N}\Delta R_n} - V_{ref}\frac{1}{2^N} = \\
&= V_{ref}\frac{R + \Delta R_j}{2^N R + \sum_{n=0}^{2^N}\Delta R_n} - V_{ref}\frac{1}{2^N} = \\
&\underset{2^N R \gg \sum_{n=0}^{2^N}\Delta R_n}{=} V_{ref}\frac{R + \Delta R_j}{2^N R} - V_{ref}\frac{1}{2^N} = \\
&= V_{ref}\frac{R}{2^N R} + V_{ref}\frac{\Delta R_j}{2^N R} - V_{ref}\frac{1}{2^N} = V_{ref}\frac{\Delta R_j}{2^N R} = V_{LSB}\frac{\Delta R_j}{R}\,.
\end{aligned}
\tag{4.9}
$$

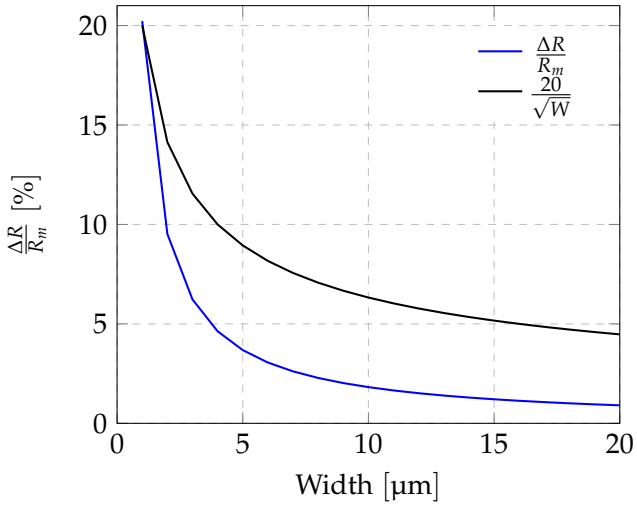
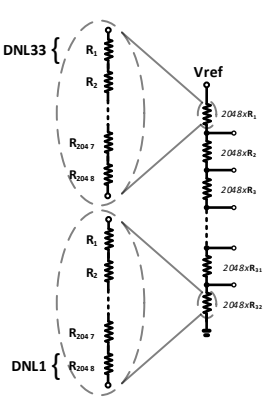
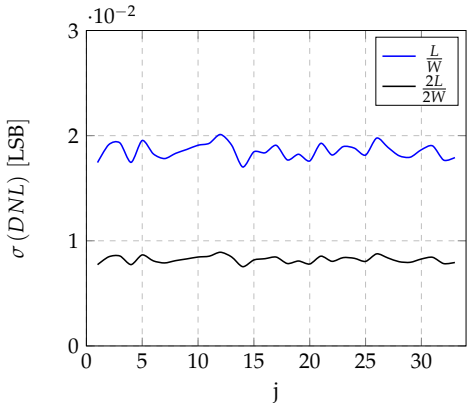


Figure 4.8.: Mismatch of two integrated resistors as a function of the resistor's width according to Equation 4.7. The L to W ratio was set to 10, Δe was kept constant at 0.1. A fitting parameter was used to highlight the $\frac{1}{\sqrt{W}}$ relationship between W and the mismatch.

Other sources of nonlinearity errors are the loading effect or offsets of op-amps. Equation 4.9 indicates that the DNL is determined by the matching of the unit resistors and thus should remain approximately constant along the R-string. This result was verified by a Monte Carlo simulation (MC simulation) with 300 runs of a 16-bit R-string with two different areas of the unit resistors. As expected, Figure 4.9b shows a nearly constant DNL profile. Furthermore, the DNL error for the unit elements with four times the area is lower by a factor of two.



(a) Schematic illustrating where the DNL was measured.



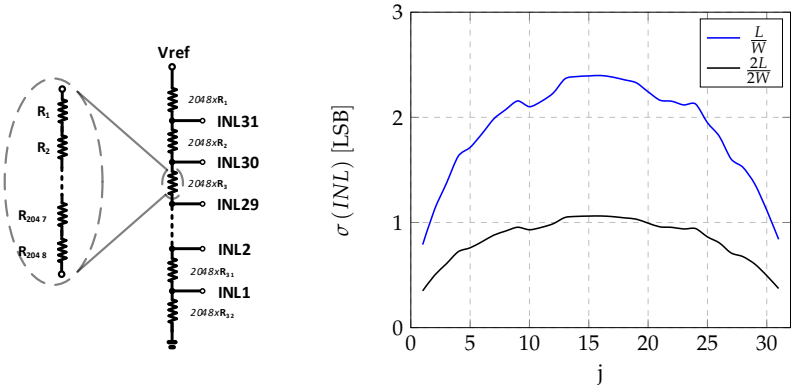
(b) DNL profile for two different areas of the unit resistors.

Figure 4.9.: Differential nonlinearity (DNL) of a 16-bit R-string. The DNL is determined by the matching of the unit resistors and remains approximately constant along the R-string.

Equation 2.5 was used to describe the INL of an R-string:

$$
\begin{aligned}
INL_j = V_j - V_{j_{ideal}} &= V_{ref}\frac{jR + \sum_{n=0}^{j}\Delta R_n}{2^N R + \sum_{n=0}^{2^N}\Delta R_n} - V_{ref}\frac{jR}{2^N R} = \\
&= V_{ref}\frac{jR}{2^N R + \sum_{n=0}^{2^N}\Delta R_n} + V_{ref}\frac{\sum_{n=0}^{j}\Delta R_n}{2^N R + \sum_{n=0}^{2^N}\Delta R_n} - V_{ref}\frac{jR}{2^N R} = \\
&\underset{2^N R \gg \sum_{n=0}^{2^N}\Delta R_n}{=} V_{ref}\frac{jR}{2^N} + V_{ref}\frac{\sum_{n=0}^{j}\Delta R_n}{2^N R} - V_{ref}\frac{jR}{2^N R} = \frac{V_{ref}}{2^N}\frac{\sum_{n=0}^{j}\Delta R_n}{R} = \\
&= V_{LSB}\frac{\sum_{n=0}^{j}\Delta R_n}{R}\,.
\end{aligned}
\tag{4.10}
$$

Again only the resistor mismatch was taken into account. The derived equation is a general valid expression. It requires that the mismatch is



(a) Schematic illustrating where the INL was measured.

(b) INL profile for two different areas of the unit resistors.

Figure 4.10.: Integral nonlinearity (INL) of a 16-bit resistor string (R-string). The INL is determined by the matching of the unit resistors and reaches its maximum at the midpoint of the R-string

known and its sum is zero. Reference [40] analyzed where to expect the worst INL of an R-string. The authors concluded, that the maximum occurs at the midpoint and that the nonlinearity error is related to he mismatch and to the number of resistors. These findings were replicated by a MC simulation. Figure 4.10b shows that the maximum occurs in the middle of the R-string and scales inversely proportional to the area. Comparing the absolute values of the DNL and INL for the same unit resistor area, the INL (2 LSB) is roughly 100 times larger than the DNL (0.02 LSB). The integral nonlinearity thus determines the area of the unit resistors in R-strings.

4.4. Speed

Neglecting the on-resistances of the switches, the output resistance, R_{out}, of a 3-bit R-string DAC, normalized to the unit resistance R, is plotted as a function of the tap position j in Figure 4.11b. R_{out} is the parallel connection

of all resistors above and below the closed switch:

$$\frac{R_{out}}{R} = \frac{j\,(2^N - j)}{2^N} \underset{N=3}{=} \frac{j\,(8 - j)}{8}\,. \tag{4.11}$$

The curve has a parabolic shape with its maximum at the middle tap. The maximum is one fourth of the resistor ladder's total resistance. Each node of the circuit is associated with a parasitic capacitance as depicted in Figure 4.11a. C_{on} and C_{off} are the parasitic capacitances associated with the on and off states of the switches and C_L is the load capacitance at the output node. The equivalent circuit of an R-string DAC can be approximated by an RC network [41]. Like in any other passive RC network, the time constant

$$\tau = R_{out} \cdot C_{out} \tag{4.12}$$

determines the settling of the output voltage, where C_{out} is the total capacitance at the output node.

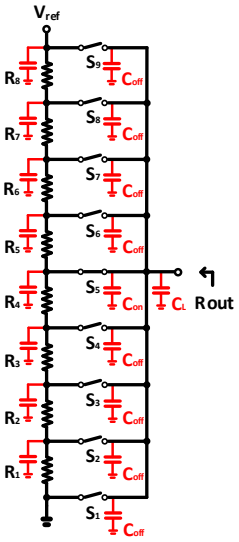
4.5. Power consumption

The total power consumption P of an R-string DAC is composed of a static part P_S and a dynamic part P_D. Figure 4.12 illustrates a simplified schematic of an R-string DAC for a basic power analysis. Leakage currents, through currents during logic transitions, dynamic currents supplied by the V_{ref} source and the power consumption of the decoder were neglected. The current flowing through the resistor ladder with 2^N devices and a reference voltage V_{ref} is

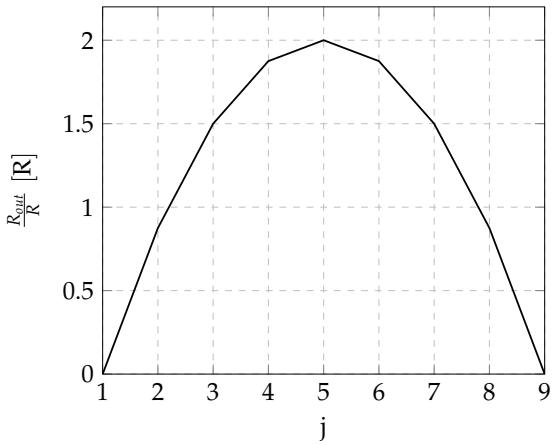
$$I_R = \frac{V_{ref}}{2^N R}\,. \tag{4.13}$$

P_S, the static power consumption, thus is

$$P_S = \frac{(V_{ref})^2}{2^N R}\,. \tag{4.14}$$



(a) Schematic of a 3-bit R-string DAC.



(b) R_{out} normalized to the unit resistance R of a 3-bit R-string as a function of the tap position.

Figure 4.11.: Output resistance R_{out} of a resistor string (R-string) digital to analog converter (DAC). R_{out} is the parallel connection of all resistors above and below the closed switch. The maximum R_{out} occurs at the middle of the R-string. C_{on} and C_{off} are the parasitic capacitances associated with the on and off states of the switches and C_L is the load capacitance at the output node.

Parasitic capacitances and the gates of the metal-oxide-semiconductor field-effect transistors (MOSFETs) have to be charged and discharged during the switching operation of the control signals of the decoder. The current needed for changing the voltage across a capacitor C_1 by V_{DD} is

$$I_{D1} = C_1 \frac{dV_{DD}}{dt} . \tag{4.15}$$

$$P_{D1} = C_1 (V_{DD})^2 f \tag{4.16}$$

Equation 4.16 describes the dynamic power consumption due to the charge and discharge process of capacitor C_1 depending on the switching frequency f of the clock signal CLK. For calculating the total power consumption P, the total capacitance C of the circuit, which is $C = \sum_{n=0}^{2^N-1} C_n$, has to be taken into account:

$$P = \frac{(V_{ref})^2}{2^N R} + C(V_{DD})^2 f . \tag{4.17}$$

4.6. Switch Resistance

Switches in CMOS technology are realized by MOSFETs. The on-resistance, R_{on}, of a MOSFET is

$$R_{on} = \frac{L}{W \mu C_{OX} (V_{GS} - V_{TH})} , \tag{4.18}$$

where W and L are the dimensions in µm, μ the electron or hole mobility in $\mathrm{cm}^2/(\mathrm{V} \cdot \mathrm{sec})$, V_{GS} the gate source voltage in V and V_{TH} the threshold voltage in V. Figure 4.13b shows the voltage dependency of R_{on} of three different switch implementations. NMOS and PMOS transistors are only suitable for signal voltages close to ground or the supply voltage. The transmission gate (TG), a parallel connection of an NMOS and a PMOS, shows an almost constant characteristic.

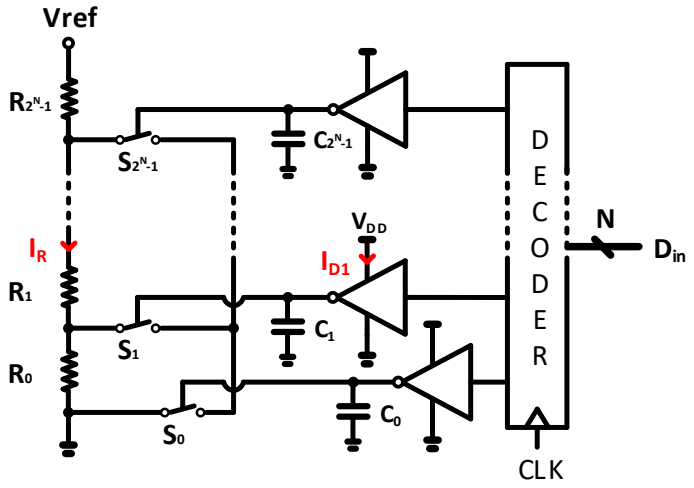
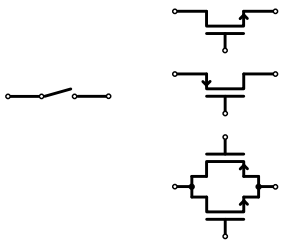
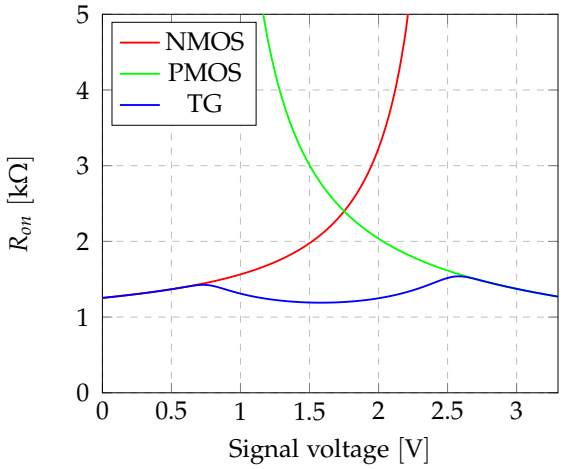


Figure 4.12.: Simplified schematic for analyzing the power consumption P of a resistor string (R-string) digital to analog converter (DAC). P is composed of a static part P_S and a dynamic part P_D. The product of the reference voltage, V_{ref}, and the current trough the R-string, I_R, determines P_S. D_{in}, the N-bit digital input signal, is decoded by a clocked (CLK) decoder. Charging and discharging the capacitor C_1 between 0 V and the supply voltage V_{DD} with a frequency f requires a power of $P_{D_1} = C_1(V_{DD})^2 f$.



(a) CMOS switch implementations.



(b) R_{on} as a function of the signal voltage of different CMOS switch implementations.

Figure 4.13.: Complementary metal-oxide semiconductor (CMOS) switches can be implemented by a single n-type metal-oxide-semiconductor (NMOS) or p-type metal-oxide-semiconductor (PMOS) transistor or a parallel connection of an NMOS and a PMOS transistor (Transmission gate (TG)). The on-resistance, R_{on}, of the TG is almost constant over the whole signal voltage range, whereas single transistor switches are only suitable for signal voltages close to ground or the supply voltage.

Table 4.1.: Comparison of the three N-bit decoder architectures regarding the complexity, the number of buffers (# Buffers), the number of switches (# Switches) and the resistance between the analog input and the analog output, R_{dec}, depicted in Figure 4.14.

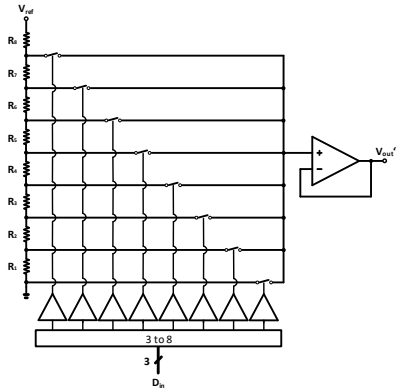
Decoder type	Complexity	# Buffers	# Switches	R_{dec}
N to 2^N	Medium	2^N	2^N	R_{on}
Tree	Low	$2 \cdot N$	$\approx 2^{N+1}$	$N \cdot R_{on}$
Matrix[1]	High	$2 \cdot \sqrt{2^N}$	$2^N + \sqrt{2^N}$	$2 \cdot R_{on}$

[1] Quadratic allocation was assumend, that is $R = C = \frac{N}{2}$ and $x = y = \sqrt{N}$.

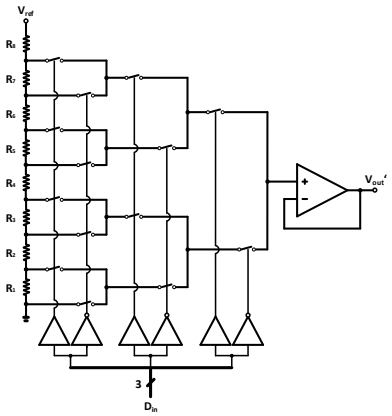
4.7. Decoder Architectures

Until now, the decoder used for processing the digital data signals was depicted as an N to 2^N decoder. Alternative architectures were developed as can be seen in Figure 4.14 [22]. Table 4.1 compares three N-bit decoder architectures regarding the complexity, the number of buffers (# Buffers), the number of switches (# Switches) and the resistance between the analog input and the analog output R_{dec}. The simplest implementation is the tree decoder. Additional digital circuit is not needed as the arrangement of the switches decodes the digital input signal. The series connection of the on-resistances of the switches limit the speed. R_{dec} can be reduced, and thus the speed increased by controlling each switch independently (N to 2^N decoder) at the expense of additional silicon area. A more efficient decoding scheme folds the R-string into a matrix arrangement while the output voltage is generated by selecting the respective row and column, similar to digital memory.

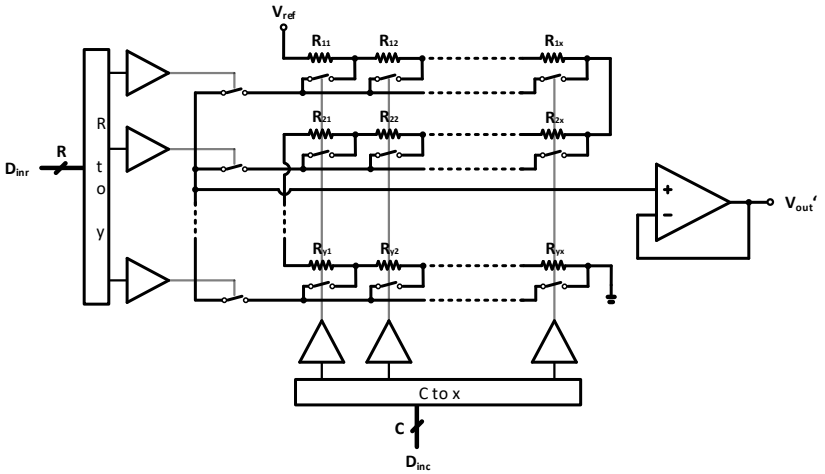
The analysis so far has shown a design trade-off between accuracy, speed, power dissipation and area consumption. Razavi illustrated this problem in the ”analog design octagon” [42].



(a) Schematic of an N to 2^N decoder for a 3-bit R-string DAC.



(b) Schematic of a 3-bit tree decoder.



(c) Schematic of an N-bit matrix decoder. The R-string is folded into a matrix arrangement. A row and a column decoder select the output voltage, similar to digital memory.

Figure 4.14.: Different decoder architectures for resistor string (R-string) digital to analog converters (DACs).

5. Design and Implementation of the DAC

The previous discussion of design considerations for R-string DACs is used in the following section to optimize the design of the two 8-bit R-string DACs for the FD-DAC. Furthermore the implementation of the remaining building blocks, the op-amps, the RCF and the control logic are discussed in detail in this chapter. Figure 5.1 shows the schematic of the designed 16-bit FD-DAC.

5.1. R-string DAC

Each of the two identical 8-bit R-string DACs is composed of 256 unit resistors with a nominal resistance of 3 kΩ. This gives a total resistance of

$$R_t = 256 \cdot (3\,\mathrm{k\Omega} \pm 10\,\%) = 768\,\mathrm{k\Omega} \pm 10\,\%\,, \tag{5.1}$$

including process variations. A bandgap circuit, providing 1.2 V, is used as a voltage reference. This gives $V_{FS} \approx 1.2\,\mathrm{V}$ and a LSB voltage of 18.3 µV in the 16-bit mode and a LSB voltage of 4.68 mV in the 8-bit mode. Solving Equation 4.13 for $V_{ref} = 1.2\,\mathrm{V}$ and $2^N R = 691.2\,\mathrm{k\Omega}$ yields 1.74 µA, the maximum current trough the resistor ladder. Not only the power consumption, but also the speed are determined by the resistance as explained in Section 4.4. The maximum R_{out} value neglecting the switches on-resistance is equal to

$$R_{out_{max}} = \frac{844.8\,\mathrm{k\Omega}}{4} = 211.2\,\mathrm{k\Omega}\,. \tag{5.2}$$

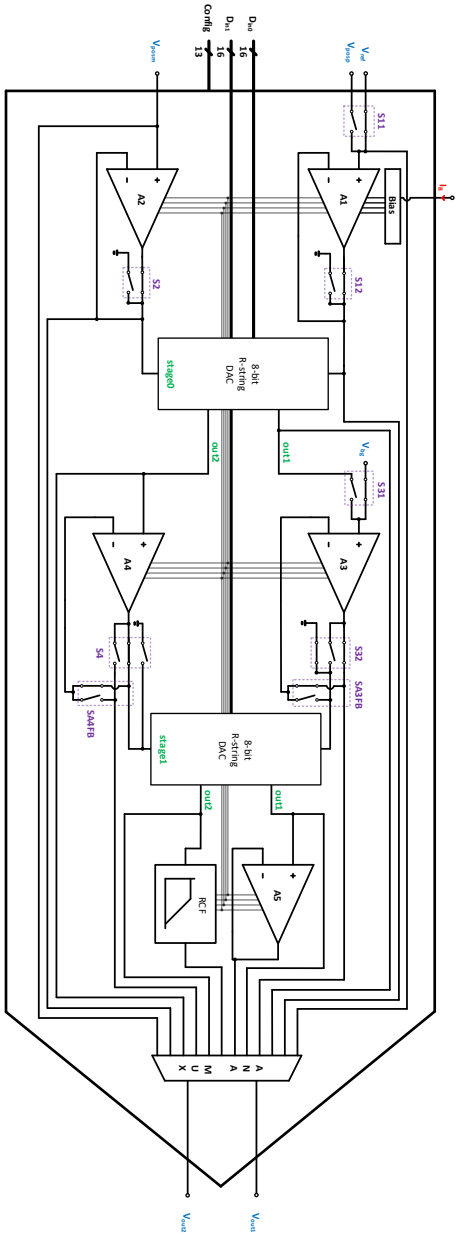


Figure 5.1.: Schematic of the designed 16-bit floating differential digital to analog converter (FD-DAC). Two 8-bit resistor string (R-string) digital to analog converters (DACs), decoupled by operational amplifiers (op-amps), can generate single-ended or differential output voltage signals, both ac or dc. The configuration can be selected by switches and an analog multiplexer (ANA MUX).

The area of a unit resistor was chosen in order to restrict the standard deviation of the INL to

$$\sigma\left(INL\right) = 3.4LSB\,. \tag{5.3}$$

Figure 5.3 depicts the implemented 8-bit R-string DAC. Two 8-bit tree decoder, controlled by 16 digital data signals, select the voltages for the two outputs. TGs were used as switches to allow the DAC to float between the supply rails. The worst case R_{on} of the switches is 4 kΩ, increasing the maximum $R_{out_{max}}$ by

$$\Delta R_{out} = 8 \cdot 4\,\mathrm{k\Omega} = 32\,\mathrm{k\Omega} \tag{5.4}$$

to $R_{outS_{max}} = 243.2\,\mathrm{k\Omega}$. In order to determine the speed of the R-string DAC (see Section 4.4), given by

$$\tau = R_{outS_{max}} \cdot C_{out}\,, \tag{5.5}$$

a partial test layout was created to estimate the capacitance C_{out} of the R-string. With the help of a layout extraction tool, a capacitance of $C_{out} \approx 160\,\mathrm{fF}$ was simulated, neglecting the input capacitance of the output buffer. Equation 5.5 gives a τ of 40 ns. However, the settling time of the R-string DAC's output voltage is much larger due capacitive coupling between the digital control wires and the R-string, and the settling behavior of the op-amp. Figure 5.2 shows the time response of output $out1$ of the extracted final layout of the R-string DAC for the worst case scenario, which is in the middle of the R-string under slow process corner conditions. The time constant $\tau = 906\,\mathrm{ns}$, which is significantly smaller than the reciprocal of the minimum sample rate

$$\frac{1}{f_s} = \frac{1}{20\,\mathrm{kHz}} = 50\,\mu\mathrm{s}\,. \tag{5.6}$$

The total capacitance C_R of all R-string nodes combined is $C_R = 5\,\mathrm{pF}$. Small through currents of digital CMOS logic can be achieved by short rise t_r and fall times t_f of the signal. Buffers with a high driving strength were used for the signals from the MCU to the input of the TG buffers, whereas t_r and t_f of the output of the TG buffers were kept as short as

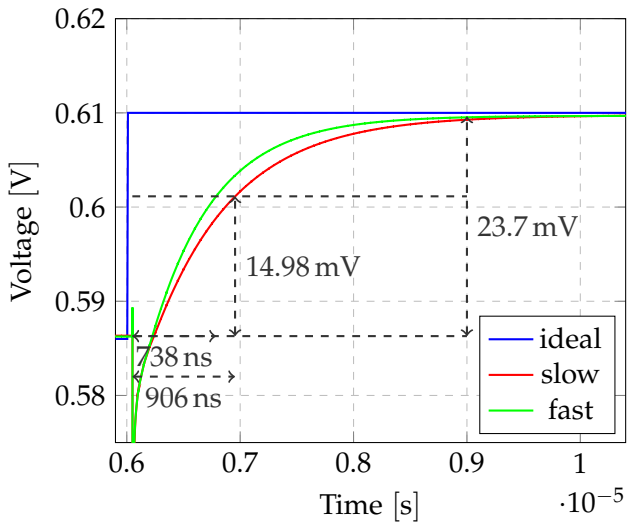


Figure 5.2.: Time response of the output *out*1 at the midpoint of the resistor string (R-string). The time constant τ, which is the time needed to reach 63.2% of the final value, was measured for the slow (906 ns) and the fast corner (738 ns).

needed. Capacitive coupling into the R-string can be reduced. A certain charge

$$Q = I \cdot t \tag{5.7}$$

is needed during a charging process, where t is in the order of ns. This is too fast for the on-chip supply voltage regulator to react. Furthermore the voltage drop across the bond wire might be too large, provided that the external supply is fast enough. Decoupling capacitors were dimensioned for an acceptable power supply voltage drop ΔV, according to

$$C = \frac{Q}{\Delta V}\,. \tag{5.8}$$

The maximum charge needed is during the transition of the digital input code from 10000000 to 01111111.

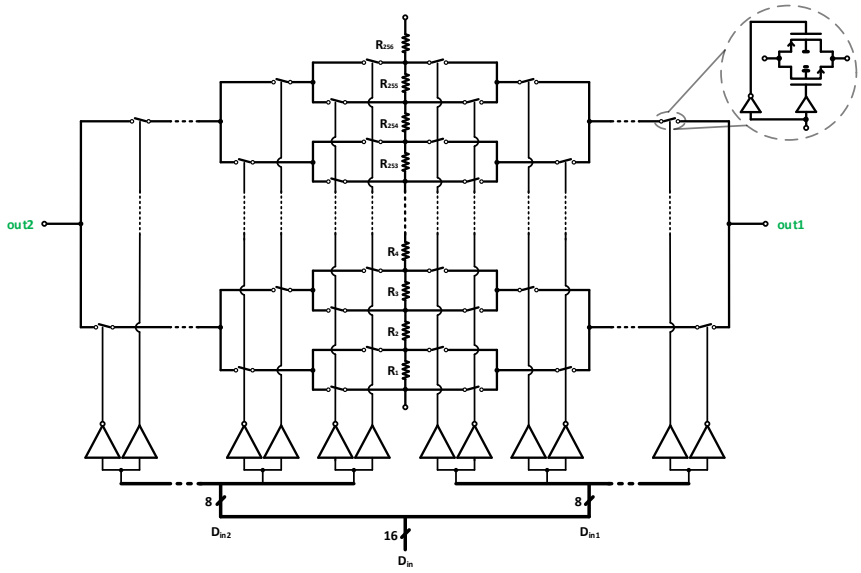


Figure 5.3.: Implementation of the 8-bit resistor string (R-string) digital to analog converter (DAC). The R-string consists of 256 unit resistors and 1020 switches are needed for the two tree decoders. Transmission gates (TGs) were used as switches. The two outputs are each independently controlled by eight digital signals.

5.2. Op-amp

Op-amps in unity-gain configuration were used to decouple the R-strings from the rest of the circuit. The input and output common-mode (CM) voltage specification of the op-amps ranges from 0.2 V to 2.5 V. A folded cascode (FC) with a PMOS input differential pair operated in weak inversion was designed to avoid a rail-to-rail architecture. The output stage was implemented as a common source amplifier. Either an NMOS or a PMOS transistor is used as the active device, depending on whether current has to be sourced (A1, A3) or sinked (A2, A4). Reference [43] introduced a low-power fast-settling CMOS op-amp employing hybrid cascode compensation. The authors concluded that less power is needed for the same bandwidth compared to the conventional Miller compensation scheme [44]. Figure 5.4 shows the structure of the two-stage amplifier. Two compensation capacitors (C_{C1} and C_{C2}) are connected between the output node of the second stage and the two low-impedance nodes of the cascodes of the first stage. The dc voltage gain, A_v, is the product of the individual gains A_{v_S} of the two stages given by

$$\begin{aligned} A_v &= A_{v_{S1}} \cdot A_{v_{S2}} = g_{m_{S1}} R_{out_{S1}} \cdot g_{m_{S2}} R_{out_{S2}} = \\ &= g_{m2} \left(r_{o5} g_{m7} r_{o7} \parallel \left[\left(r_{o3} \parallel r_{o11} \right) g_{m9} r_{o9} \right] \right) \cdot g_{m13} \left(r_{o12} \parallel r_{o13} \right) , \end{aligned} \tag{5.9}$$

where g_m is the small-signal transconductance of the transistors, $R_{out_{Sx}}$ is the total output resistance of stage x and r_o is the small-signal output resistance of the transistors. An analysis of the open loop transfer function of a hybrid cascode compensated FC op-amp was done by [45]. The first stage pole, located at

$$p_1 \approx -\frac{1}{R_{out_{S1}} A_{v_{S2}} \left(C_{C1} + C_{C2} \right)} , \tag{5.10}$$

gives the bandwidth (BW) of the amplifier. The gain-bandwidth product (GBW)

$$GBW \approx A_v \cdot BW = \frac{g_{m2}}{2\pi \left(C_{C1} + C_{C2} \right)} \tag{5.11}$$

is limited by the transconductance of the differential pair and the value of the compensation capacitors. To relax the RCF's performance requirements

oversampling is used. The MCU is capable of providing 100 kS/s. A GBW of 1 MHz is a reasonable trade-off between gain and power. The maximum capacitive load C_L at the DAC output is expected to be 1.5 pF. One third of C_L is a good starting point for the value of the total compensation capacitance $C_{C1} + C_{C2}$. Solving Equation 5.11 for g_{m2} yields:

$$g_{m2} \approx GBW \cdot 2\pi \left(C_{C1} + C_{C2}\right) = 1\,\text{MHz} \cdot 2\pi\, 500\,\text{fF} = 3.14\,\mu\text{S}\,. \tag{5.12}$$

The lower limit of the bias current I_{B1} of the differential pair is set by a chosen $\frac{g_m}{I_D}$ ratio of 20 to

$$I_D = \frac{g_{m2}}{20} = \frac{3.14\,\mu\text{S}}{20} = 160\,\text{nA}\,. \tag{5.13}$$

This leads to a bias current of

$$I_{B1} = 2 \cdot I_D = 2 \cdot 160\,\text{nA} = 320\,\text{nA}\,. \tag{5.14}$$

A certain amount of current is needed fo fulfill the internal slew rate (SR) requirement:

$$I_{B1} = SR_{int} \cdot \left(C_{C1} + C_{C2}\right) = 5\,\text{mV}\,\mu\text{s}^{-1} \cdot 500\,\text{fF} = 2.5\,\text{nA}\,. \tag{5.15}$$

Similarly, the quiescent current of the output stage has to be larger than

$$I_{B2} = SR_{ext} \cdot \left(C_{C1} + C_{C2} + C_R\right) = 5\,\text{mV}\,\mu\text{s}^{-1} \cdot 5.5\,\text{pF} = 27.5\,\text{nA}\,. \tag{5.16}$$

Both, I_{B1} and I_{B2} from Equation 5.15 and Equation 5.16, are smaller than the bias current required for achieving GBW (Equation 5.14). I_{B1} and I_{B2} was set to 500 nA by the bias circuit depicted in Figure 5.5. The cascode voltages V_{b2} and V_{b3} are generated by this circuit as well. Reference [45] continued the analysis of the open loop transfer function by calculating the higher frequency poles p and zeros z to

$$p_2 \approx -\frac{g_{m7} g_{m9} \left(C_{C1} + C_{C2}\right)}{C_{C1} C_{C2} \left(g_{m7} + g_{m9}\right)}\,, \tag{5.17}$$

$$p_{3,4} \approx -\frac{g_{m9} C_{C1} \left(C_{C2} + C_L\right) + g_{m7} C_{C2} \left(C_{C1} + C_L\right)}{2 C_L C_{C1} C_{C2}} \pm j \frac{g_{m13} \left(g_{m7} + g_{m9}\right)}{C_B C_L}\,, \tag{5.18}$$

$$z_1 \approx -\frac{g_{m7}}{C_{C1}} \tag{5.19}$$

and

$$z_{2,3} \approx \pm\frac{g_{m9}g_{m13}}{C_B C_C}\,. \tag{5.20}$$

C_B and C_C are the capacitances at nodes B and C:

$$C_B \approx C_{db7} + C_{dg7} + C_{db9} + C_{dg9} + C_{gs13}\,, \tag{5.21}$$

$$C_C \approx C_{db3} + C_{gs9} + C_{sb9} + C_{db11}\,, \tag{5.22}$$

where C_{db} is the drain-bulk capacitance, C_{dg} is the drain-gate capacitance, C_{gs} is the gate-source capacitance and C_{sb} is the source-bulk capacitance of a transistor. The cascode transistors M_6 to M_9 were designed for the same g_m. Furthermore, $C_{C1} = C_{C2} = 200\,\text{fF}$ canceling the first zero z_1 by the second pole p_2. M_{13}, the input transistor of the second stage, was sized to sink or source the quiescent current of 0.5 µA plus the maximum load current of the R-string of 1.74 µA, that is 2.24 µA. One bias circuit generates the bias voltages V_b for all amplifiers (A1 to A5 and RCF). Figure 5.6 shows the schematics for characterizing the designed op-amp under two different load conditions, test case 1 (TC1) and test case 2 (TC2). The simulated frequency responses of the extracted layouts under all corner conditions are plotted in Figures 5.7, 5.8, 5.9 and 5.10. Table 5.1 summarizes the simulated op-amp characteristics, where PM is the phase margin and V_{os} the offset voltage of the amplifier.

5.3. Reconstruction Filter

Active continuous-time (CT) RCFs can be implemented as active RC filters [46] or transconductance-capacitance (gm-C) filters [47]. The latter architecture is based on operational transconductance amplifiers (OTAs) and is used for high-frequency applications. Due to the poor linearity of the transconductor, for example a differential pair, a compensation circuit would be necessary to achieve an approximate constant cutoff frequency.

Table 5.1.: Simulated operational amplifier (op-amp) characteristics of the extracted layout under all corner and load conditions.

Parameter	Value		Unit
	Min.	Max.	
A_v	78	130	dB
PM	51	67	deg
GBW	1.6	2.7	MHz
$\sigma\left(V_{os}\right)$	1.8		mV

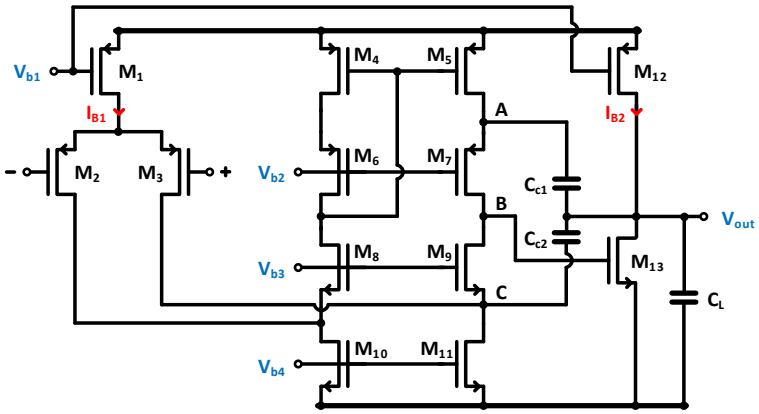


Figure 5.4.: Two-stage folded cascode (FC) operational amplifier (op-amp) employing hybrid cascode compensation [43]. A FC with a PMOS input differential pair was used as a first stage. The second stage was implemented as a common source amplifier. Two compensation capacitors (C_{C1} and C_{C2}) are connected between the output node of the second stage and the two low-impedance nodes of the cascodes of the first stage.

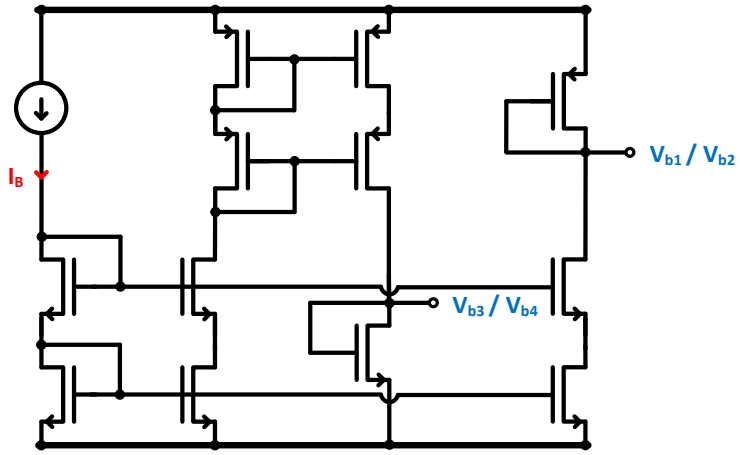
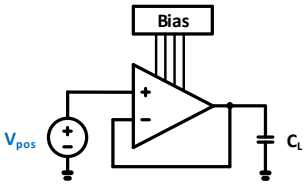
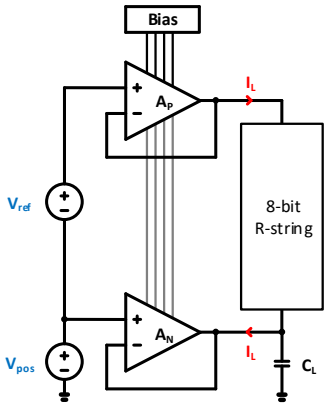


Figure 5.5.: Schematic of the bias circuit of the operational amplifier (op-amp) in Figure 5.4. The bias current I_B flowing trough a diode connected metal-oxide-semiconductor field-effect transistor (MOSFET) generates a bias voltage V_b.



(a) Test bench for test case 1 (TC1): Capacitive load C_L.



(b) Test bench for test case 2 (TC2): Capacitive load C_L and load current I_L due to the resistor string (R-string).

Figure 5.6.: Test benches for the operational amplifier (op-amp) in Figure 5.4. The op-amp has to be stable under different load conditions. Amplifier A_P uses a p-type metal-oxide-semiconductor (PMOS) as the active transistor in the output stage, whereas amplifier A_N uses an n-type metal-oxide-semiconductor (NMOS).

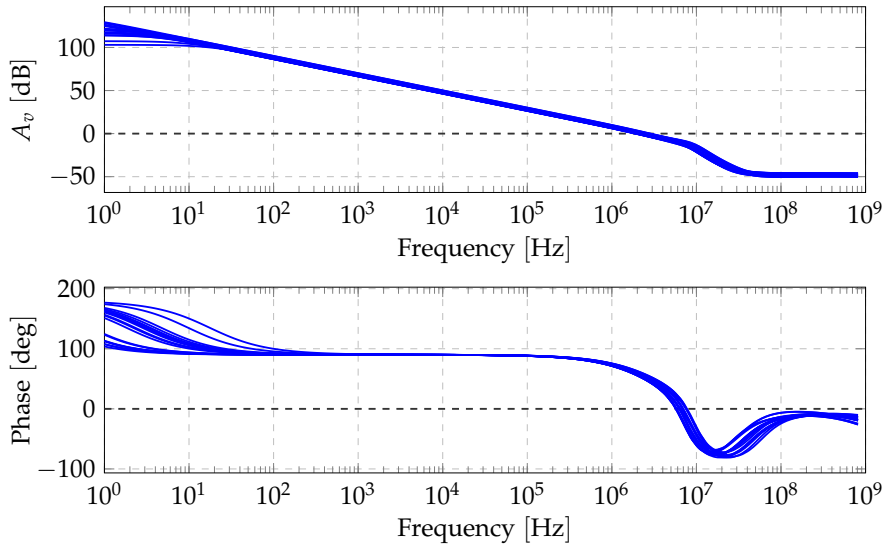


Figure 5.7.: Frequency response (top: magnitude, bottom: phase) of the operational amplifier (op-amp) with an n-type metal-oxide-semiconductor (NMOS) common source output stage in test case 1 (TC1) configuration (see Figure 5.6a). The simulation results of the extracted layout under all corner conditions show, that the op-amp is stable with a minimum phase margin of 51 degrees.

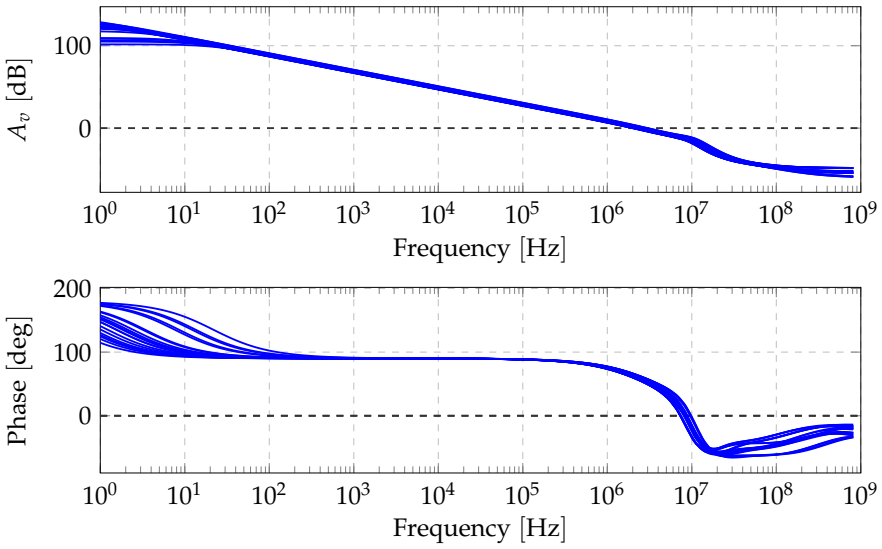


Figure 5.8.: Frequency response (top: magnitude, bottom: phase) of the operational amplifier (op-amp) with a p-type metal-oxide-semiconductor (PMOS) common source output stage in test case 1 (TC1) configuration (see Figure 5.6a). The simulation results of the extracted layout under all corner conditions show, that the op-amp is stable with a minimum phase margin of 51 degrees.

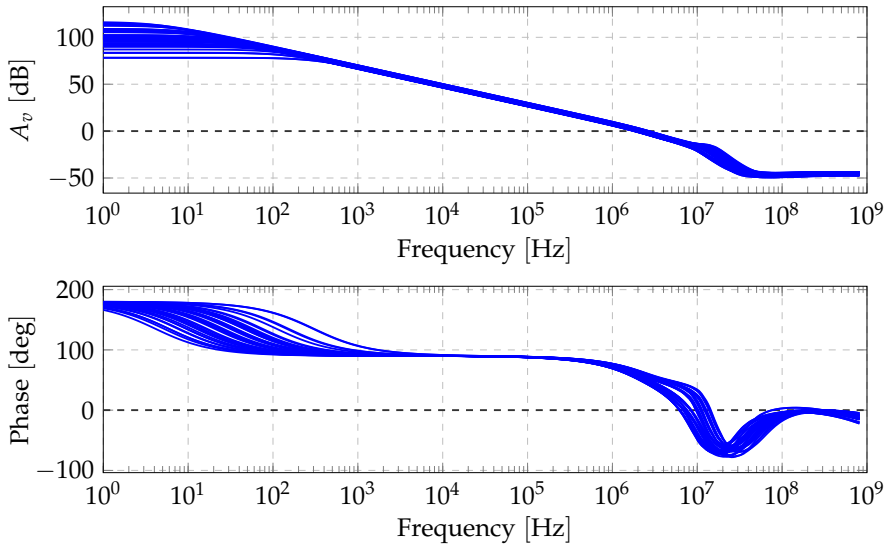


Figure 5.9.: Frequency response (top: magnitude, bottom: phase) of the operational amplifier (op-amp) with an n-type metal-oxide-semiconductor (NMOS) common source output stage in test case 2 (TC2) configuration (see Figure 5.6b). The simulation results of the extracted layout under all corner conditions show, that the op-amp is stable with a minimum phase margin of 54 degrees.

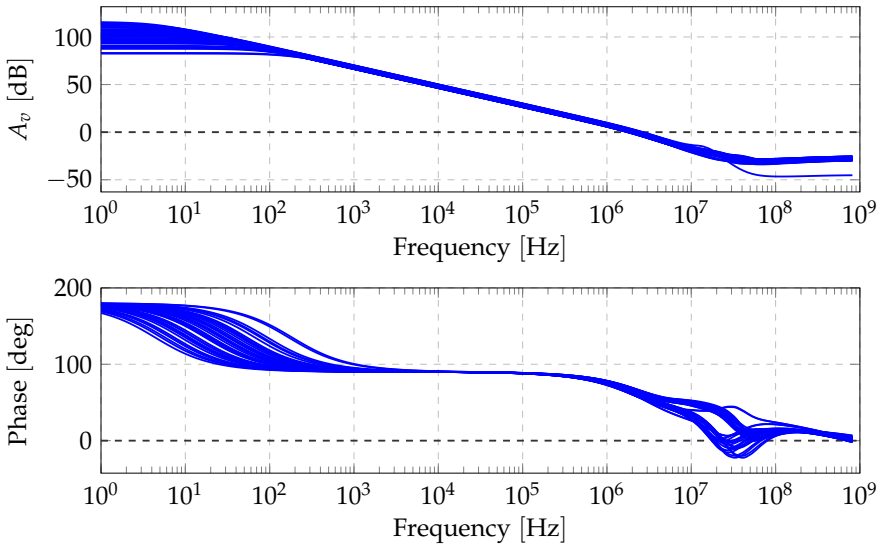


Figure 5.10.: Frequency response (top: magnitude, bottom: phase) of the operational amplifier (op-amp) with a p-type metal-oxide-semiconductor (PMOS) common source output stage in test case 2 (TC2) configuration (see Figure 5.6b). The simulation results of the extracted layout under all corner conditions show, that the op-amp is stable with a minimum phase margin of 60 degrees.

Thus, an active RC filter was chosen for this work. Reusing the existing op-amp, a second-order low-pass unity-gain Sallen-Key filter was designed. The schematic is shown in Figure 5.11 and the ideal transfer function is given by:

$$H(s) = \frac{1}{(j2\pi f)^2 (R_1 R_2 C_1 C_2) + j2\pi f (R_1 C_1 + R_2 C_1) + 1}. \tag{5.23}$$

The process dependent cutoff frequency, defined as the $-3\,\mathrm{dB}$ point, is

$$f_c = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}. \tag{5.24}$$

Bessel filters have an optimized transient response: The phase response is linear (falling and rising edges look similar) and neither overshoot nor ringing occur [48]. This comes at the expense of a flat roll-off. Reference [49] provides equations for calculating the filter's component values:

$$R_1 = mR, \tag{5.25}$$

$$R_2 = R, \tag{5.26}$$

$$C_1 = C \tag{5.27}$$

and

$$C_2 = nC, \tag{5.28}$$

where $m = 0.42$ and $n = 1.5$ for a Bessel type filter. An additional passive low-pass (R_3 and C_3) was added in series with the filter's output, improving the high-frequency response of the filter. A6 in Figure 5.11 buffers the output of the R-string DAC. The FC op-amp was reused but with a reduced GBW. Table 5.2 summarizes the component values for a nominal cutoff frequency of 30 kHz. The simulated frequency responses under all corner conditions are plotted in Figure 5.12. f_c varies between 16.5 kHz and 27.7 kHz.

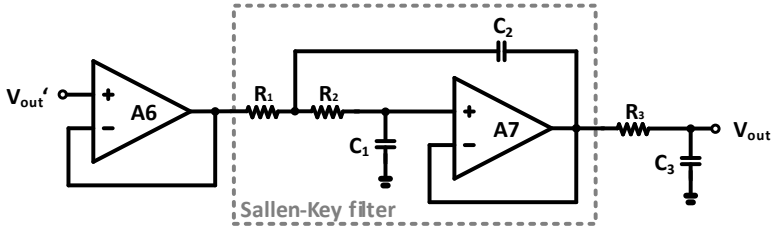


Figure 5.11.: Schematic of the reconstruction filter (RCF) composed of an input buffer A6, a second-order low-pass unity-gain Sallen-Key filter and an additional passive low-pass at the output. The cutoff frequency is determined by the absolute values of the resistors and capacitors.

Table 5.2.: Component values of the reconstruction filter (RCF) for $f_c = 30\,\text{kHz}$.

Parameter	Value	Unit
R_1	4.81	MΩ
R_2	2.405	MΩ
C_1	1	pF
C_2	1.499	pF
R_3	200	kΩ
C_3	1	pF

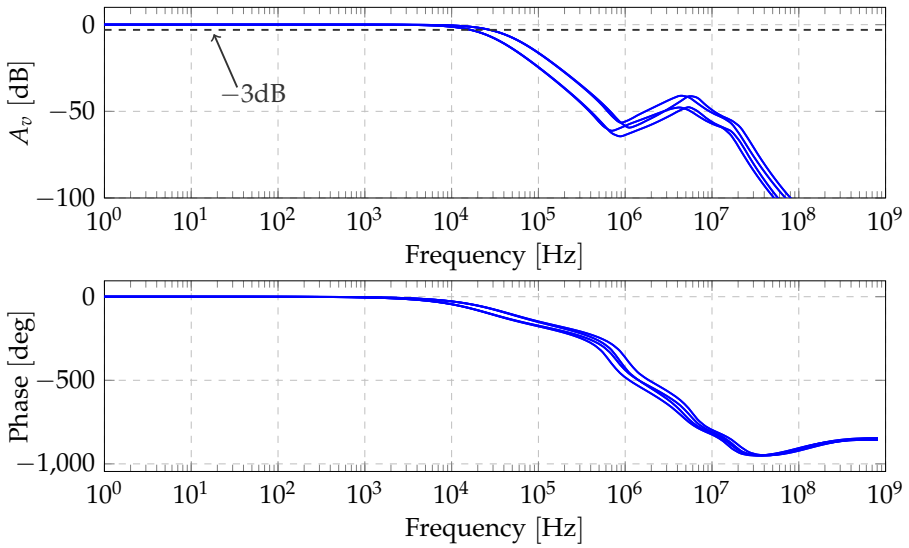


Figure 5.12.: Frequency response (top: magnitude, bottom: phase) of the reconstruction filter (RCF) in Figure 5.11. The simulation results of the extracted layout under all corner conditions show, that the −3 dB cutoff frequency varies between 16.5 kHz and 27.7 kHz.

5.4. Control Logic

The 13 configuration bits of the FD-DAC are set by the MCU. 3 bits are used for choosing one of the eight modes of operation listed in Table 5.3, where a 1 means that switches are closed and op-amps are enabled. A decoder generates the signals which are required for setting the correct switch positions and turning on or off the amplifiers required. All op-amp input and output signals can be multiplexed to either one of the two DAC outputs. This enables the measurement of the amplifier's offset voltages. Most critically are the offsets of A3 and A4. V_{LSB} of the coarse stage (stage0) is

$$V_{LSB_{stage0}} = \frac{V_{ref}}{2^8} = \frac{1.2\,\mathrm{V}}{256} = 4.68\,\mathrm{mV}\,. \tag{5.29}$$

As the offsets of all op-amps (A1 to A7) are uncorrelated and the offset magnitudes lie within $\pm 5.4\,\mathrm{mV}$ with a probability of 99.7 %, the voltage across the R-string of the fine stage (stage1) might be zero. Offset errors can be compensated by changing V_{LSB} of the coarse stage, though at the expense of a lower resolution. This can be done by the firmware of the electrochemical measurement system's MCU. The process dependent attenuation by the RCF of the output signal can be compensated by firmware as well. Two 4 to 12 decoders control the ANA MUX. The remaining two configuration bits are enable signals.

Figure 5.13 shows the layout of the FD-DAC. All building blocks were placed between the two identical 8-bit R-string DACs. Empty space was filled with power supply decoupling capacitors.

Table 5.3.: Modes of operation of the floating differential digital to analog converter (FD-DAC) shown in Figure 5.1. A 1 means that the corresponding switch is closed and the operational amplifier (op-amp) is enabled. In both, the low (8-bit) and the high-resolution (16-bit) mode, single-ended, differential (FD), dc (steep edges) or ac (sinusoidal) output voltages can be generated.

Mode of operation	Config$<2:0>$			Description	A1 A3 S12	$\overline{\text{S11}}$ A3 S2	A4	A5	RCF	S31	S32 SA3FB	S4 SA4FB
1	0	0	0	Reset	0	0	0	0	0	0	1	0
2	0	0	1	FD, dc, 8-bit	1	1	0	0	0	0	1	0
3	0	1	0	FD, dc, 16-bit	1	1	1	1	0	0	0	1
4	0	1	1	FD, ac, 16-bit	1	1	1	0	1	0	0	1
5	1	0	0	single-ended, dc, 8-bit	1	0	0	0	0	0	1	0
6	1	0	1	single-ended, dc, 8-bit, 2 channels	1	1	1	1	0	1	0	0
7	1	1	0	single-ended, dc, 16-bit	1	1	1	1	0	0	0	1
8	1	1	1	single-ended, ac, 16-bit	1	1	1	0	1	0	0	1

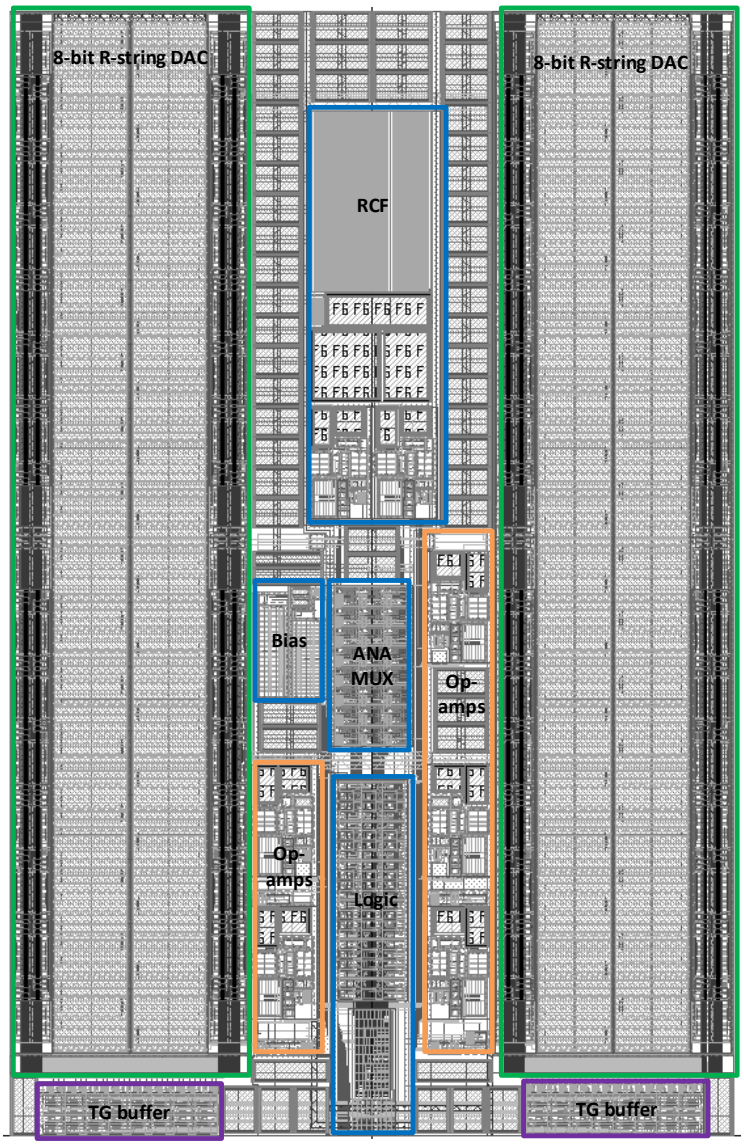


Figure 5.13.: Layout of the floating differential digital to analog converter (FD-DAC). All building blocks, the reconstruction filter (RCF), the bias circuit (Bias), the analog multiplexer (ANA MUX), the operational amplifiers (op-amps), the control logic and the transmission gate (TG) buffers, were placed between the two identical 8-bit resistor string (R-string) digital to analog converters (DACs).

6. Simulation and Characterization

The individual building blocks of the FD-DAC were already characterized in Chapter 5. In this chapter, the performance of the FD-DAC is verified. The first section explains the test bench used for the verification. Based on the requirements defined in Section 3.1 a DPV and an EIS waveform were generated by the FD-DAC, to demonstrate the overall functionality of the implementation. Finally, the total power consumption of the FD-DAC is determined.

6.1. Test bench

The test bench depicted in Figure 6.1 was used to characterize the FD-DAC. Ideal sources generate the reference voltage, V_{ref}, the positioning voltage, V_{pos}, and the bias current, I_{bias}. Furthermore, the configuration bits were set by ideal voltage sources. V_{DAC}, the ideal output waveform of the FD-DAC, was generated by a MATLAB® script and exported to a text file for test bench integration. An example code for generating a DPV signal and the corresponding plot are attached in Appendix A. In order to control the two interpolated R-string DACs, a Verilog-A module was programmed. It splits the information of an analog input signal into four analog signals, one for each output of the two interleaved DAC stages. Four ADCs, clocked at the sample rate f_s, then convert the modified V_{DAC} voltages into digital control signals. The Verilog-A code of the "Analog Control" module and the waveforms of the analog signals are attached in Appendix B.

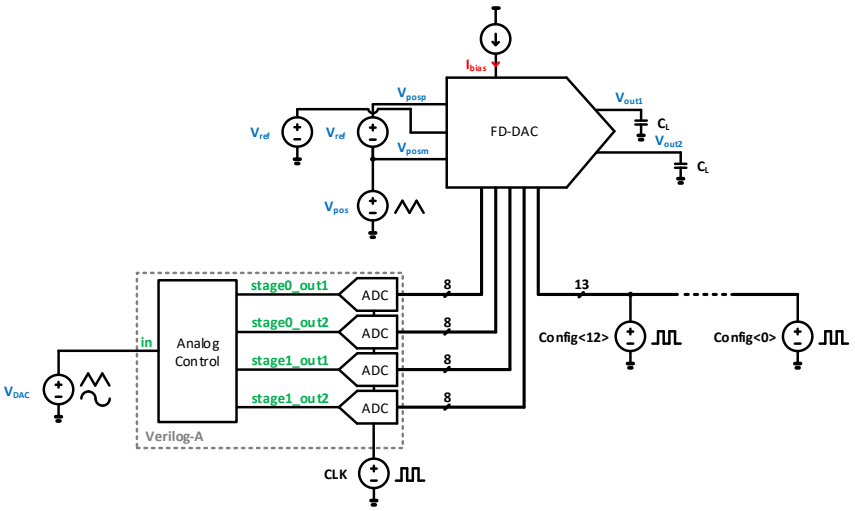


Figure 6.1.: Test bench for characterizing the floating differential digital to analog converter (FD-DAC). The ideal output waveform of the FD-DAC, V_{DAC}, is converted into digital signals by a Verilog-A module controlling the FD-DAC. The configuration bits, the bias voltages and the bias current are set by ideal sources.

6.2. Differential Pulse Voltammetry

For generating a DPV waveform, the FD-DAC was set to operation mode 3, which is the 16-bit dc floating differential mode. The test bench was configured as follows: $V_{ref} = 1.2\,\mathrm{V}$, $C_L = 1.5\,\mathrm{pF}$ and V_{pos} increases linearly from 0.2 V to 1.3 V. Rather extreme parameters for the DPV were chosen compared to [16] in order to verify the FD-DAC. The width of the pulses is 100 µs and the amplitude is 100 mV. The slope (scan rate) of the DPV is $100\,\mathrm{V\,s^{-1}}$. An input sample rate of 100 kS/s is provided by the ADCs. Figure 6.2 shows the simulation results of the extracted FD-DAC under nominal conditions. The FD-DAC is enabled after 300 µs. V_{out1} and V_{out2}, the generated output voltages, coincide with the ideal voltages DPV and V_{posm} and float in a range from 0.2 V to 2.5 V.

6.3. Electrochemical Impedance Spectroscopy

The FD-DAC's dc mode was successfully simulated in the previous section. An EIS waveform is used to verify the ac mode. The FD-DAC was set to operation mode 4, that is the 16-bit ac floating differential mode. The test bench was configured as follows: $V_{ref} = 1.2\,\mathrm{V}$, $C_L = 1.5\,\mathrm{pF}$ and V_{pos} decreases linearly from 1.3 V to 0.2 V. Three simulation runs under slow process conditions were performed. Sinusoidal signals with an amplitude of 80 mV, a frequency of 10 kHz and offsets of 0.1 V, 0.6 V and 1.1 V were generated at a sample rate of 100 kS/s. Figures 6.3 to 6.5 show that the FD-DAC is capable of generating sinusoidal signals with a frequency of 10 kHz in the floating range from 0.2 V to 2.5 V.

6.4. Power Consumption

Speed and SR requirements were verified by generating an EIS and a DPV waveform. The power consumption of the FD-DAC during those simulations without a capacitive load ($C_L = 0$) is analyzed in this section. As stated in Section 4.5, the total power consumption P is composed of a

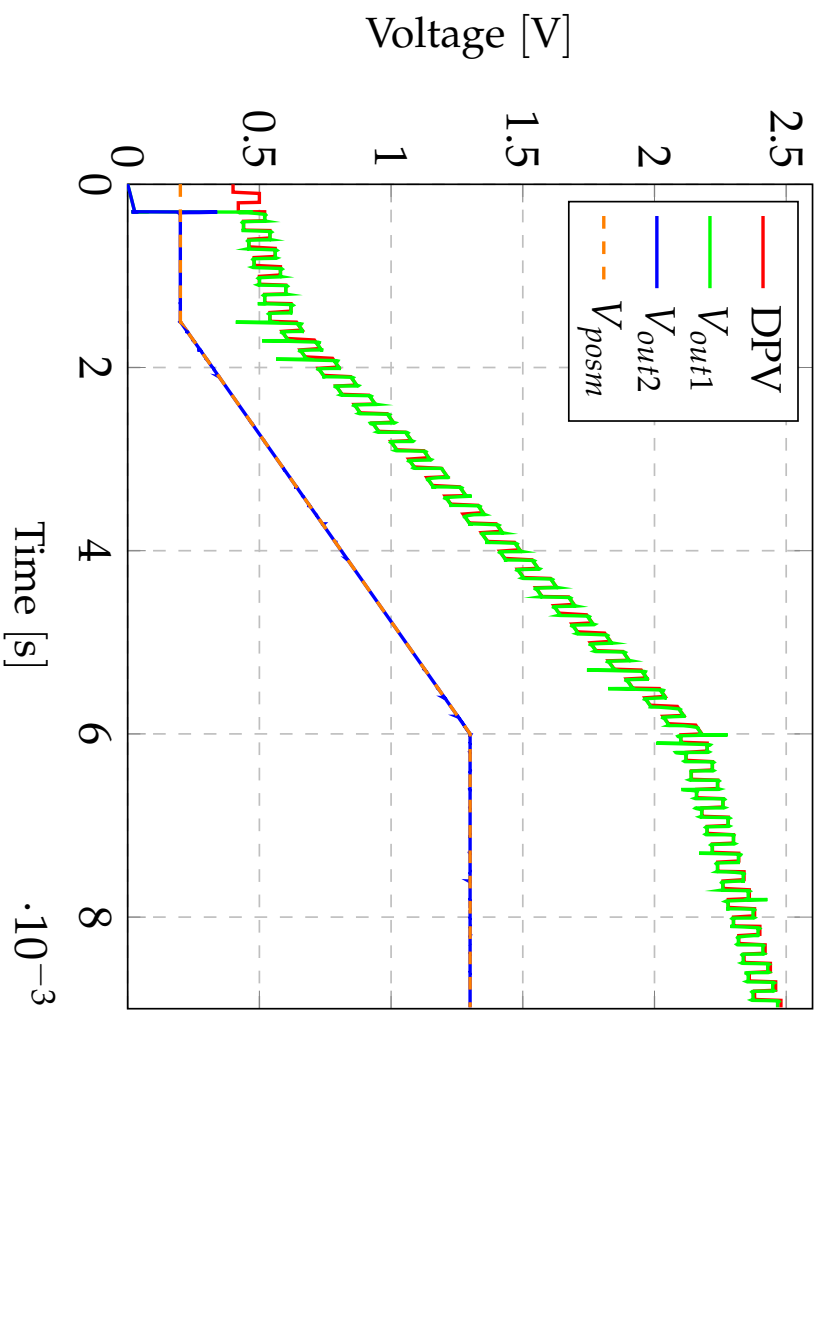


Figure 6.2.: Simulation results of a differential pulse voltammetry (DPV). The width of the pulses is 100 µs, the amplitude 100 mV and the slope (scan rate) of the DPV is 100 V s^{-1}. V_{out1} and V_{out2}, the generated output voltages, coincide with the ideal voltages DPV and V_{posm}.

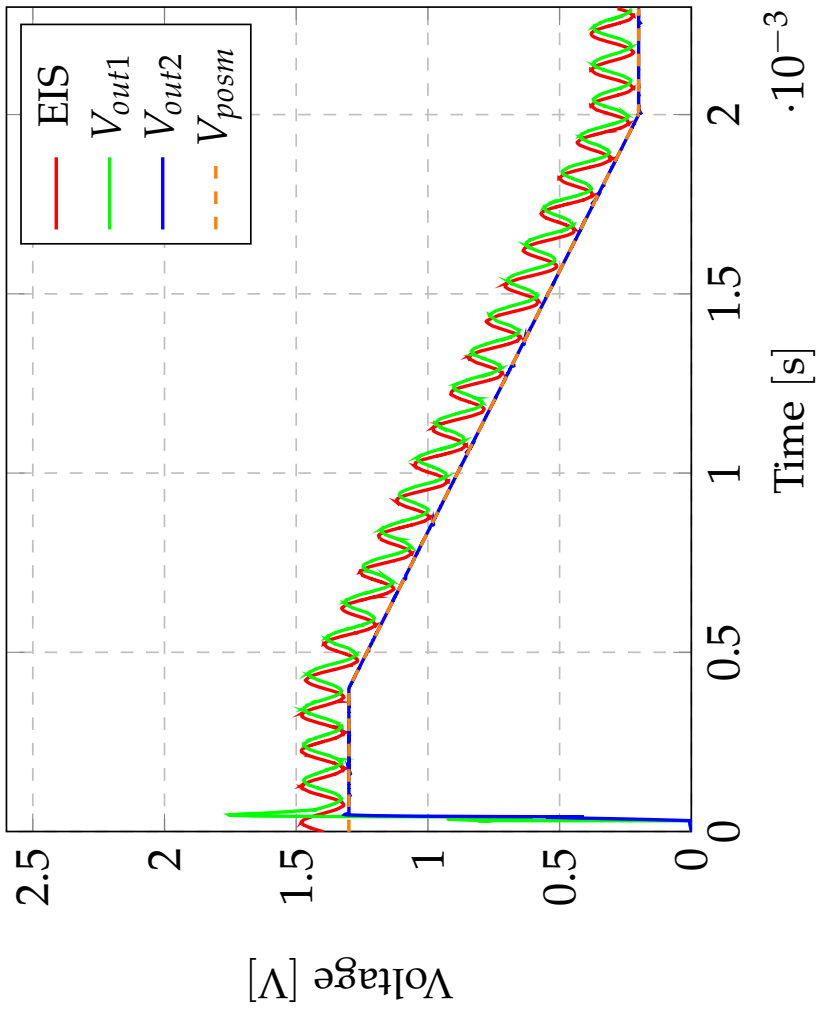


Figure 6.3.: Simulation result 1 of an electrochemical impedance spectroscopy (EIS) waveform. The frequency of the sine is 10 kHz, the amplitude 80 mV and the dc offset voltage 100 mV. V_{out1} and V_{out2}, the generated output voltages, coincide with the ideal voltages EIS and V_{posm}.

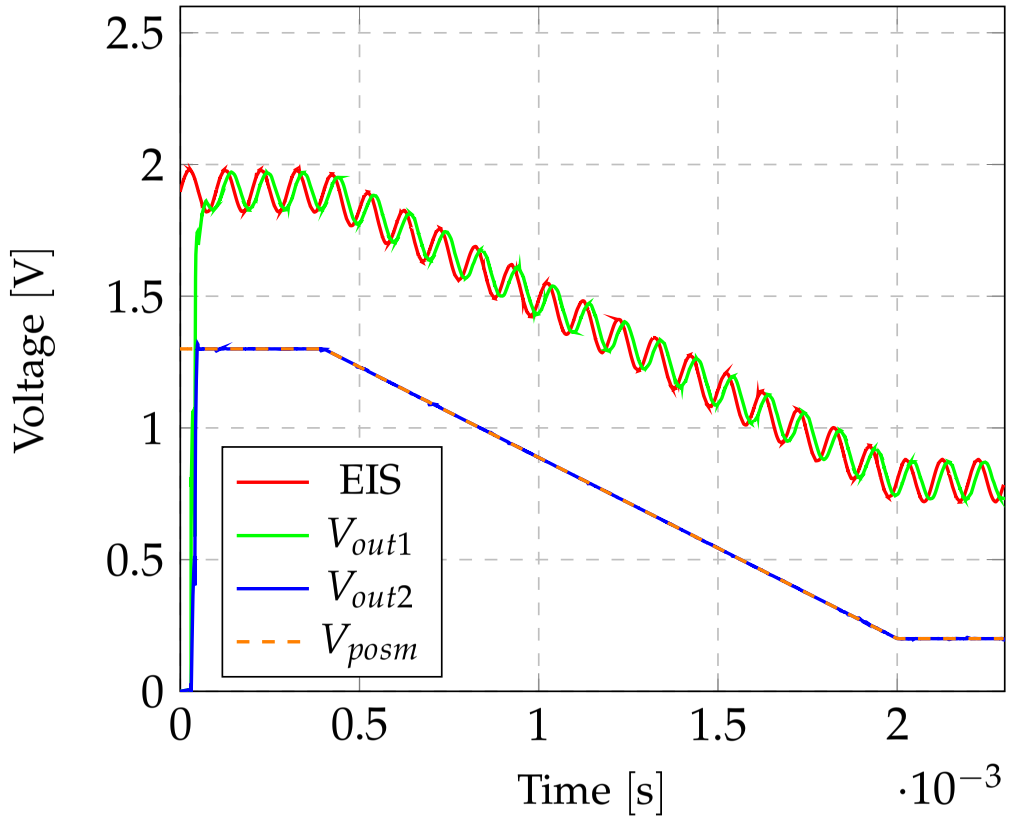


Figure 6.4.: Simulation result 2 of an electrochemical impedance spectroscopy (EIS) waveform. The frequency of the sine is 10 kHz, the amplitude 80 mV and the dc offset voltage 600 mV. V_{out1} and V_{out2}, the generated output voltages, coincide with the ideal voltages EIS and V_{posm}.

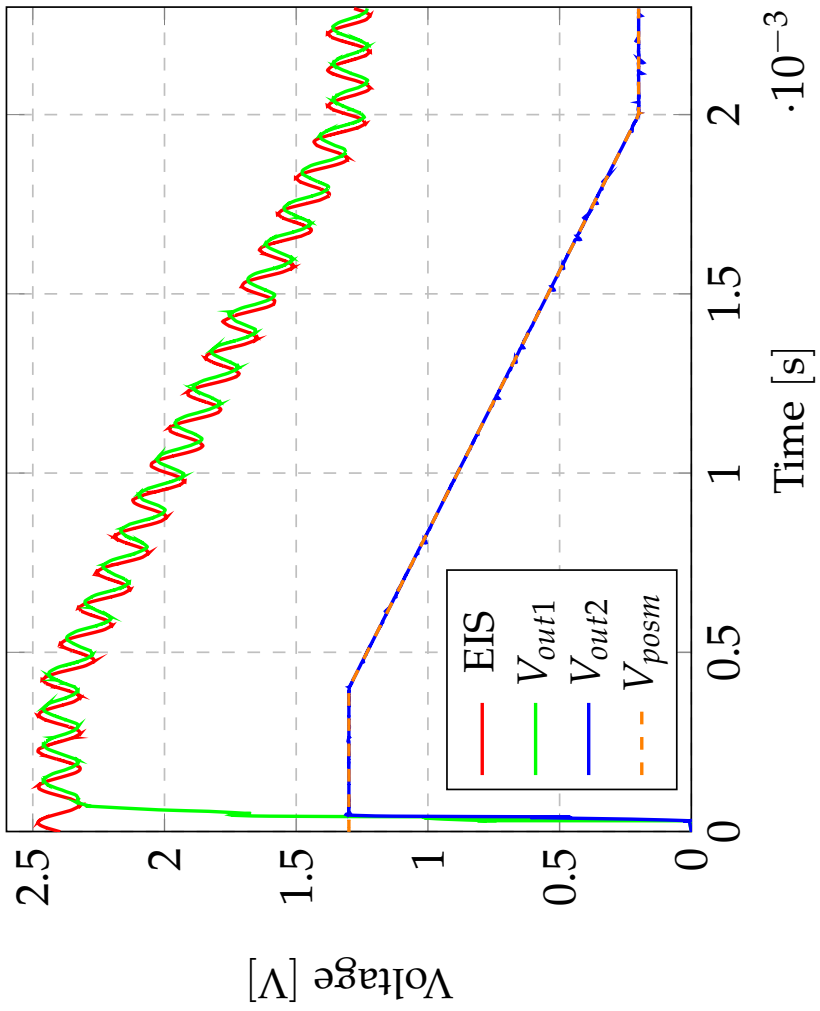


Figure 6.5.: Simulation result 3 of an electrochemical impedance spectroscopy (EIS) waveform. The frequency of the sine is 10 kHz, the amplitude 80 mV and the dc offset voltage 1.1 V. V_{out1} and V_{out2}, the generated output voltages, coincide with the ideal voltages EIS and V_{posm}.

static part P_S and a dynamic part P_D. Two supply voltages are used for the FD-DAC. The analog part is supplied by $V_{DD_{ANA}}$ and the digital part is supplied by $V_{DD_{DIG}}$. Thus the total power consumption is equal to

$$P = P_S + P_D = P_{S_{ANA}} + P_{S_{DIG}} + P_{D_{ANA}} + P_{D_{DIG}} \,. \tag{6.1}$$

The static power consumption P_S is composed of

$$P_S = V_{DD_{ANA}} \cdot I_{S_{ANA}} + V_{DD_{DIG}} \cdot I_{S_{DIG}} \,, \tag{6.2}$$

where I_S are the static currents drawn from the respective supplies. The power-dissipation capacitance, C_D, defined in [50], models the dynamic power consumption including through currents and switching currents.

$$C_D = \frac{I_D}{V_{DD} \cdot f_s} \tag{6.3}$$

Equation 6.3 calculates C_D, where I_D is the root mean square (RMS) value of the dynamic supply current:

$$I_D = \sqrt{\frac{1}{T} \int_0^T i(t)^2 dt} - (I_{S_{ANA}} + I_{S_{DIG}}) \,. \tag{6.4}$$

The current i in Equation 6.4 is the total current consumed by the FD-DAC. P_D is calculated as:

$$P_D = C_D \left(V_{DD}\right)^2 f_s \,. \tag{6.5}$$

Table 6.1 summarizes all simulated and calculated values under nominal conditions for $V_{DD_{ANA}} = 3\,\text{V}$, $V_{DD_{DIG}} = 1.5\,\text{V}$ and $f_s = 100\,\text{kHz}$. $I_{D_{ANA}}$ and $I_{D_{DIG}}$ are the RMS values of the analog and digital supply currents. The maximum power consumption during an EIS is 131.91 µW. This value can be reduced to 18.18 µW when generating only one static output voltage in the low-resolution mode.

The transient behavior of the FD-DAC was simulated in this chapter. Both, DPV and EIS waveforms, were generated meeting the specifications under all operating conditions.

Table 6.1.: Simulated power consumption of the extracted floating differential digital to analog converter (FD-DAC) for an analog supply voltage $V_{DD_{ANA}} = 3\,\mathrm{V}$, a digital supply voltage $V_{DD_{DIG}} = 1.5\,\mathrm{V}$ and a sample rate $f_s = 100\,\mathrm{kHz}$. $I_{D_{ANA}}$ and $I_{D_{DIG}}$ are the RMS values of the analog and digital supply currents according to Equation 6.4. $C_{D_{ANA}}$ and $C_{D_{DIG}}$ are the power dissipation capacitances of the analog and digital supply defined by Equation 6.3. The total power consumption P is composed of a static part P_S and a dynamic part P_D.

Mode of operation	$I_{D_{ANA}}$ µA	$C_{D_{ANA}}$ pF	$I_{D_{DIG}}$ µA	$C_{D_{DIG}}$ pF	$P_{D_{ANA}}$ µW	$P_{D_{DIG}}$ µW	$P_{S_{ANA}}$ µW	$P_{S_{DIG}}$ nW	P µW
5: single-ended, dc, 8-bit	12.89	42.97	1.55	10.33	38.67	2.32	18.17	10.5	59.16
4: FD, ac, 16-bit	30.76	102.53	4.42	29.47	92.28	6.63	33	10.5	131.91

7. Conclusion

This thesis covered the design of a FD-DAC for an integrated electrochemical measurement system. Dynamic output voltage range exploitation allows the system to work with lower supply voltages than conventional architectures, thus enabling the integration with standard CMOS technologies and the use in wearables and mobile applications. However, this approach requires a floating and differential DAC. In addition to the measurement system's performance, commonly used electrochemical measurement techniques define the specifications of the FD-DAC. After discussing DAC performance metrics and architectures three different concepts, with focus on low power consumption, were proposed. A versatile 16-bit FD-DAC, based on two interpolated 8-bit R-string DACs, was chosen for the implementation, as it best fulfills the requirements and allows easy integration with the rest of the electrochemical measurement system. As the FD-DAC is based on R-string DACs, design considerations and design trade-offs for such an architecture were analyzed in detail.

Two-stage, hybrid compensated op-amps were used to avoid loading of the R-strings and coupling into other parts of the system. An FC OTA was used as the first stage of the op-amps. The second stage was implemented by a common source stage, with either an NMOS or a PMOS active transistor. In that way, building blocks could be reused, decreasing the design effort. Oversampling was used to relax the RCF's performance requirements. Reusing the existing op-amp, an active RC Sallen-Key low-pass filter was designed to remove the unwanted high frequency contents of the DAC's output signal. Switches and an analog multiplexer were used to implement eight modes of operation for the FD-DAC. In both, the low (8-bit) and the high-resolution mode (16-bit), single-ended, differential, dc (steep edges) or ac (sinusoidal) output voltages can be generated. The full scale range is 1.2 V. At a supply voltage of 3 V, the FD-DAC outputs can float from

0.2 V to 2.5 V. Simulation results of a DPV and an EIS waveform verified the transient behavior of the FD-DAC, under all process corners and temperatures from −20 °C to 80 °C. The simulated power consumption during an EIS, generating a sine with a frequency of 10 kHz, an amplitude of 80 mV and a sample rate of 100 kS/s is 132 µW. When generating only one single-ended output voltage in the low-resolution mode, the power consumption can be reduced to 18 µW. The simulation results show that the implemented FD-DAC is suitable for the application in low-voltage and low-power electrochemical measurement systems.

Appendix

Appendix A.

Waveform Generator

Listing A.1: Matlab code for generating a differential pulse voltammetry (DPV) waveform as plotted in Figure A.1. The offset, the pulse width, the pulse height and the slope (scan rate) of the DPV signal can be chosen.

```
% DPV waveform generator

n = 240;

step_v_r = 100e-3;
step_v_f = 80e-3;
step_t = 100e-6;
step_t_delta = 1e-9;

v_offset = 200e-3;

waveform = zeros(2*n, 2);

if v_offset > 0
  waveform(1,2) = v_offset;
end

for i = 2:3:2*n-1
  if i < n
    waveform(i,1) = waveform(i-1,1) + step_t - step_t_delta
        ;
    waveform(i,2) = waveform(i-1,2);
    if mod(i,2)
      waveform(i+1,1) = waveform(i-1,1) + step_t;
      waveform(i+1,2) = waveform(i-1,2) - step_v_f;
    else
```

```
        waveform(i+1,1) = waveform(i-1,1) + step_t;
        waveform(i+1,2) = waveform(i-1,2) + step_v_r;
    end
  waveform(i+2,1) = waveform(i-1,1) + step_t + step_t_delta
      ;
  waveform(i+2,2) = waveform(i+1,2);
end

fileID = fopen('waveform.txt','w');

for i = 1:1:2*n
  fprintf(fileID,'%10.9f %c',waveform(i,1));
  fprintf(fileID,'%10.9f \n',waveform(i,2));
end

fclose(fileID);

plot(waveform(:,1),waveform(:,2));
title('Waveform');
xlabel('Time')
ylabel('Input voltage')
grid on
```

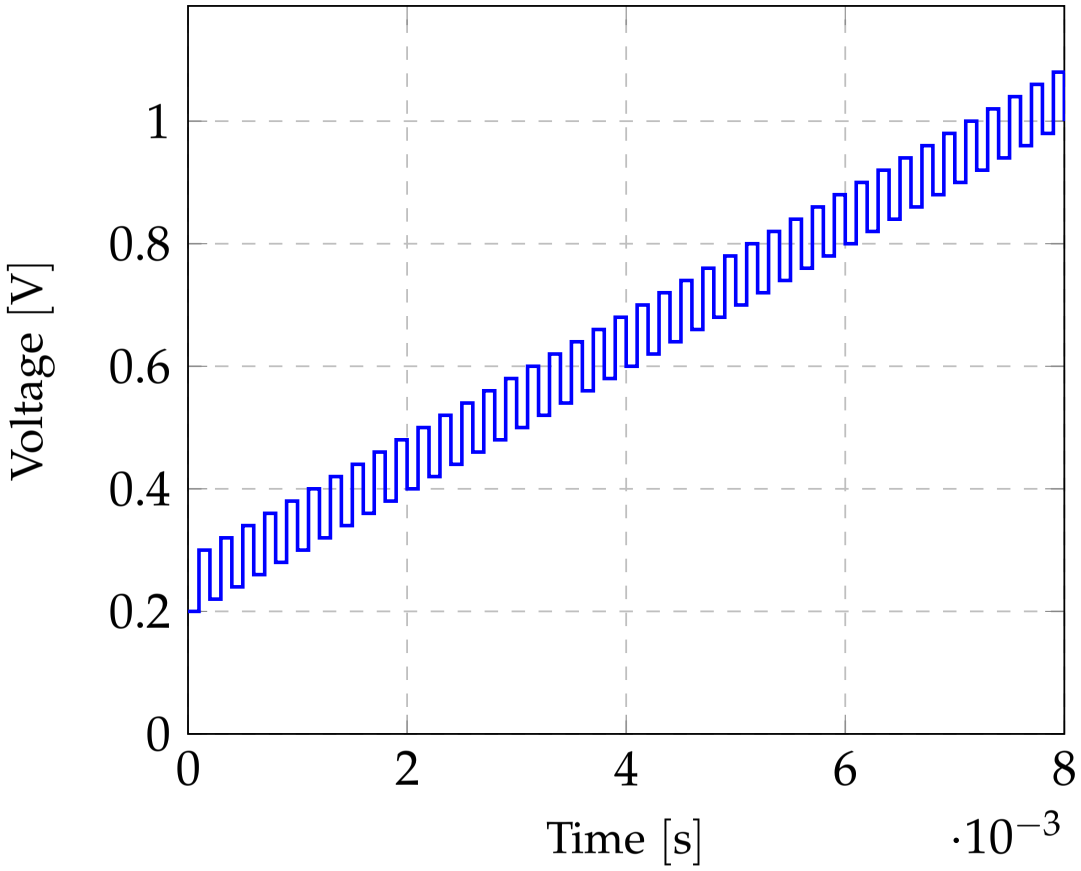


Figure A.1.: Typical differential pulse voltammetry (DPV) waveform generated by the Matlab code in Listing A.1. The width of the pulses is 100 µs and the amplitude is 100 mV. The slope (scan rate) of the DPV is 100 V s^{-1}.

Appendix B.

Verilog-A Control Block

Listing B.1: Verilog-A code of the "Analog Control" module used in the test bench depicted in Figure 6.1. The information of an analog input signal is split into four analog signals to control two interleaved digital to analog converter (DAC) stages. Figure B.1 shows the corresponding waveforms.

```
`include "discipline.h"
`include "constants.h"

//-------------------------------------------------------------------
//
// dac_control_veriloga
//
//
// parameters:
//
// v_stage_1_ref  = reference voltage [V]
//
//
// Modifies an analog input signal in order to control an
// interpolated DAC.
//
//-------------------------------------------------------------------

module dac_control_veriloga(in_stage_1, out_stage_0_1,
    out_stage_0_2,out_stage_1);
input in_stage_1;
output out_stage_0_1, out_stage_0_2, out_stage_1;
electrical in_stage_1, out_stage_0_1, out_stage_0_2,
    out_stage_1;
parameter real v_stage_1_ref = 1;
```

```
integer a = 0;
real b = 0;
integer c = 0;

analog begin

  if (V(in_stage_1) > v_stage_1_ref) begin
    a = floor(V(in_stage_1) / v_stage_1_ref);
    b = V(in_stage_1) % v_stage_1_ref;
    if (b > 0) begin
      a = a + 1;
    end else begin
      a = a;
    end
    if ((a - c) > 0) begin
      V(out_stage_0_1) <+ a * v_stage_1_ref;
      V(out_stage_0_2) <+ (a - 1) * v_stage_1_ref;
      V(out_stage_1) <+ V(in_stage_1) - ((a - 1) *
          v_stage_1_ref);
    end else begin
      V(out_stage_0_1) <+ a * v_stage_1_ref;
      V(out_stage_0_2) <+ (a - 1) * v_stage_1_ref;
      V(out_stage_1) <+ V(in_stage_1) + ((a - 1) *
          v_stage_1_ref);
      c = a;
    end
  end else begin
    V(out_stage_0_1) <+ v_stage_1_ref;
    V(out_stage_0_2) <+ 0;
    V(out_stage_1) <+ V(in_stage_1);
    c = 0;
  end
end

endmodule
```

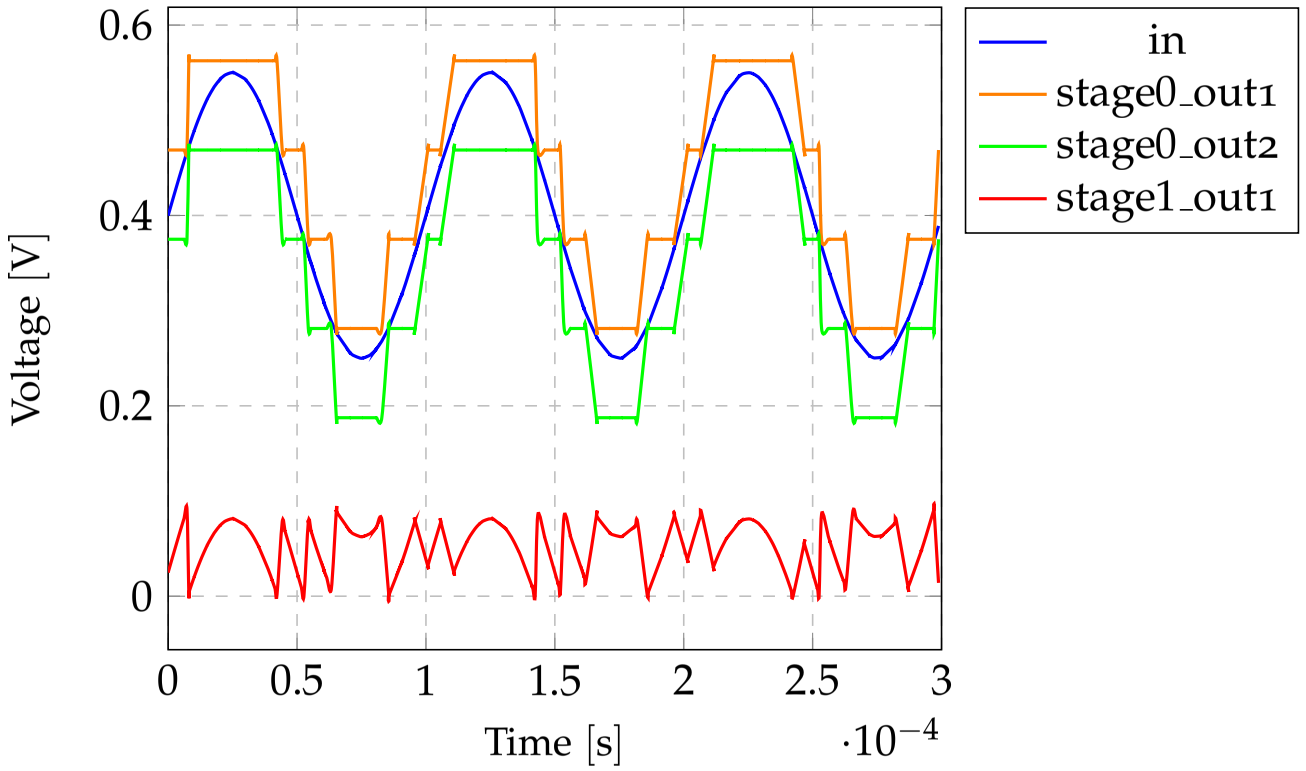


Figure B.1.: Waveforms of the "Analog Control" module generated by the Verilog-A code in Listing B.1. Stage 0 generates a constant reference voltage ($stage0\_out1 - stage0\_out2$) for stage 1. Signal $stage1\_out1$ generates the shape of the input signal *in*.

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