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Proof of Concept for Power-Line Communication in Battery Stacks

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Abstract

Electric mobility is advancing steadily, and the rising number of hybrid and electric vehicles is increasing the demand for range and reliability. In order to achieve long ranges continuously and to guarantee them over the entire service life of a vehicle, great attention has to be paid to the management of battery cells. This is where battery management systems come into play. They monitor and manage the charge states of all cells and even disconnect the battery in the event of a fault in order to prevent danger to the passengers, the car and its surroundings. Monitoring the large number of cells in decentralised systems requires a communication link between the individual management modules and the host controller. Additionally, the high voltages of several hundred volts require isolated communication interfaces. The needed real-time monitoring of cell voltages, currents and temperatures require high data rates. Hence, power-line communication is an interesting alternative where the path through the battery cells via power connectors can be used as a communication channel without the need for further isolation and cabling. In this master thesis a demonstrator for a proof-of-concept was developed, which shows that this communication via lithium-ion cells is actually possible.

Keywords: Power line communication, battery management, electric vehicles, lithium-ion battery

Kurzfassung

Die Elektromobilität schreitet stetig voran und mit der steigenden Anzahl an Hybrid- und Elektro-Fahrzeugen steigt auch der Anspruch an deren Reichweite. Um hohe Reichweiten auch kontinuierlich zu erreichen und über die gesamte Lebensdauer eines Fahrzeugs zu garantieren, muss großes Augenmerk auf das Management der Akku-Zellen gelegt werden. Hier kommen Batterie-Management-Systeme ins Spiel, die den Zustand aller Zellen überwachen, verwalten und im Fehlerfall die Batterie abtrennen um Schäden oder sogar möglichen Bränden vorzubeugen. Die Überwachung der großen Zahl an Zellen erfordert bei dezentralen Systemen eine Kommunikation der einzelnen Module mit einem Host. Spannungen von mehreren hundert Volt erfordern isolierte Kommunikationsschnittstellen, die Überwachung von Zellspannungen, Strömen und Temperaturen in Echtzeit benötigt hohe Datenraten. Hier stellt die "Power-Line Kommunikation" eine interessante Alternative dar, bei welcher der Pfad durch die Batterie-Zellen und Hochstromverbinder als Kommunikationskanal verwendet wird, ohne weitere Isolation und Verkabelung zu benötigen. In dieser Masterarbeit wurde ein Demonstrator für ein "Proof-of-Concept" entwickelt, der zeigt, dass diese Kommunikation über Lithium-Ionen Zellen tatsächlich möglich ist, mit welchen Einschränkungen zu rechnen ist und welche Probleme dabei auftreten.

Schlagwörter: Powerline-Kommunikation, Batteriemanagement, Elektrofahrzeuge, Lithium-Ionen Batterie

Contents

3 Introduction

3.1 Motivation

As hybrids and electrical cars are slowly replacing the combustion engine, reducing battery cost and increasing range, as well as battery lifetime are in the main focus of the industry. On the other hand, due to the dangers of mishandling lithium-ion cells, safety is also a huge concern in building electric cars.

Traction batteries usually consist of multiple stacked Li-Ion cells to increase the pack voltage and parallel cells to give the wanted energy storage capacity. To achieve these goals, each cell or module has to be monitored to assure its use in the best conditions for efficiency and range, while staying in the safe range. The battery management unit has to communicate with the individual cell circuits over a safe communication channel to perform the needed state-of-charge (SOC) and state-of-health (SOH) estimations and the balancing of the cells. In this work, a proof of concept for an alternative communication channel over the pre-existing power-line is shown.

The power-line channel in electric cars provides a harsh environment for communication due to its properties optimized for power transmission, its many noise sources, which degrade the communication quality hugely, and also the needed robustness of the communication against thorough EMC testing.

3.2 Power Line Communication

Every existing electronic device needs to be supplied with power to work. The conductors that feed the sufficient supply-voltage to the device and carry the resulting current are called power-lines.

Usually, communication with other devices is done over a separate channel, e.g. wireless transmission, optical transmission or dedicated communication wires, but Power-Line-Communication (PLC) offers an alternative to this "usual" approach by re-purposing the power-line as a communication channel. The advantages of PLC can be:

- Reduced wiring effort and cost
- No additional peripherals (connectors, antennas,...)

On the contrary, in PLC systems a lot of issues have to be taken care of:

- Radiated and conducted electromagnetic emissions due to high frequency signals on unprotected wires

- Susceptibility to electromagnetic interference
- Difficult to nearly-impossible channel characterization
- Changing channel characteristics due to load changes, geometry changes,...

The communication over the power-line is usually done by modulating a carrier signal onto the power line with a high frequency. The power line can use DC as well as AC transmission (50 Hz in Europe). The used carrier frequencies in state-of-the-art systems vary from the lower kHz range up to 100 MHz, the used modulations range from simple amplitude and frequency modulations up to complex modulation schemes like orthogonal frequency-division multiplexing (OFDM).

4 Related Work

4.1 Literature

While research in the area of PLC in buildings is already well advanced, at the time this document is written only very little work has been published on the topic of power-line communication in Li-Ion batteries. Most of the published papers and books come from the "Karlsruhe Institute of Technology" where the properties of the battery communication channel were examined during the "IntLiIon" project. Ouannes, Nickel, and Dostert proposed a a high-frequency model for a prismatic battery cell and simulated the channel transfer characteristics. The research results of Opalko were published in "Powerline-Kommunikation für Batteriemanagement-Systeme in Elektro- und Hybridfahrzeugen," where the author specialized in the coupling of the PLC signal into the system via "Rogowski" coils, disturbance investigations and measurements on real battery modules.

4.2 State of the Art for PLC

The use of power-line communication is widely spread from low-speed communications in high-voltage power grids to high speed communications, but it can generally be divided into two categories [23]:

- Narrow-Band communication
  Frequencies from 3 - 500 kHz
- Wide-Band communication
  Frequencies from 1.8 - 86 MHz

For in-house power line communication, current state of the art are the IEEE Standard 1901[7], which was published in 2010 and reused many features from the Homeplug AV specification and the ITU-T standard "G.hn". Available devices provide speeds of more than 1 Gbit/s, but the communication for battery management purposes has no use for excessively high data rates, instead - robustness is needed. The Homeplug Alliance developed the "Green PHY" Standard[2] to be used in smart grid applications, which shows promising properties for use in traction batteries.

HomePlug GreenPHY 1.1 Key Attributes[2]

- Used frequencies: 2 MHz to 30 MHz
- OFDM modulation
- QPSK subcarrier modulation
- 1155 sub-carriers
- 24.414 kHz sub-carrier spacing

- Robust OFDM repeat coding

By using only a simple QPSK modulation for each sub-carrier instead of higher order modulations, the specifications for the analog front-end and the analog/digital conversion can be relaxed and with the repeat coding, high PHY rates are traded for redundancy. This can be achieved by spreading copies of the data over multiple sub-carriers in the whole spectrum, which results in less packet loss even when multiple sub-carriers are lost. These modifications reduce the complexity of the devices and increase the robustness of the communication, which are properties that are very much desired in automotive uses, especially for the application in battery systems, where high demands regarding safety and electromagnetic compatibility are required.

4.3 Battery-Management Communication Interfaces

The need for a communication link between battery-management components in a distributed system is obvious, but the implementation of such a link can be done in a multitude of ways.

4.3.1 Wired Connection

Typically, one would simply use a wired communication, which is cheap and reliable. But in the case of a high-voltage battery pack, this assumption is not valid. Due to the high-voltage, isolation of every component is needed and due to the dangers to human personnel, the mounting of the cable harness in said high-voltage environment is complicated and expensive. Additionally, the huge amount of mechanical connectors makes them susceptible to defects.

4.3.2 Optical Connection

An alternative approach would be to bring the isolation directly into the physical layer: An optical communication link between the components would already provide all the needed isolation with no additional effort needed. Of course, this also comes with disadvantages: The optical media (e.g. fiberglass) is expensive and the photo-emitters degrade significantly over the long term use in an automotive environment.

4.3.3 Wireless Connection

On the other hand, one could completely take the physical connection of components out of the equation. By using a wireless link between system components, there would be no need for any connectors, wires or isolation. These benefits come with some drawbacks: The system should not be influenced from wireless communication from the outside or disturb communication around the car, which means excessive measurements of battery packs, simulation and re-measurements are necessary to optimize shielding and the placement of the transceivers.

4.3.4 Power-Line Communication

In a combination of wireless and wired communication, power-line communication offers some advantages to the other methods. By using wireless modulation techniques on the existing power-line circuit, the need for additional connectors and wires is completely eliminated. Still, some extra hardware is needed for the power-line transceivers and the electromagnetic disturbances and noise degrade the performance of PLC significantly.

4.3.5 State of the Art

Currently, on the market for battery-management systems, most isolated communication interfaces are based on capacitor or transformer isolated wired buses, while some wireless and optical systems are in development or in prototype-state. Although some papers on the subject of PLC for battery management have been published, no product or even a prototype based on this technology exists as this thesis is written.

5 Theory

For a first start, the "IEEE Standard for Broadband over Power Line Networks: Medium Access Control and Physical Layer Specifications"[7] provides a good introduction into the topic "Power Line Communication". Even though the writers created the standard mainly in respect to "in-house" communication over mains networks, many assumptions and descriptions also fit very well to the use of PLC in battery stacks.

The IEEE Standard 1901-2010[7] describes the power line medium in 3 major ways:

- *Pre-existent medium*
  The use of an already existing medium is different to common wired communication technologies, which mostly define their own media. This also means that the technology which is communicating on the power line has to be able to adapt to the changing topology of the medium, which includes switching of different loads, changing sizes of the network and other problems of a shared medium.

- *Adverse medium*
  As the main use of power lines is the transportation of power from source to sink, power lines are designed to transport power as lossless as possible and provide probably the worst possible conditions for communication. Characterization of the communication channel is in most cases not possible due to the infinite possibilities of changes on the medium.

- *Open medium*
  Similar to IEEE 802.11 (WiFi) frequency bands, the power line is an open and unlicensed medium, which also means it is susceptible to noise on every frequency.

The performance of a communication system does always depend on the properties of the communication channel, which is why the properties of the medium have to be examined thoroughly. "IEEE Standard for Broadband over Power Line Networks: Medium Access Control and Physical Layer Specifications" also describes the differences of power-line media to wired media.

Excerpt from IEEE 1901:

> *The PHYs used in IEEE 1901 are fundamentally different from those of traditional wired media. IEEE 1901 PHYs:*
>
> - *Use a medium that has neither absolute nor readily observable boundaries*
> - *Are unprotected from other signals that may be sharing the medium*
> - *Communicate over a medium significantly less reliable than traditional wired PHYs*
> - *Operate in networks with dynamic topologies (a user throwing a switch may enable or disable branches of the network)*
> - *Lack full connectivity, and therefore, the assumption normally made that every station STA can hear every other STA is invalid (i.e., STAs may be "hidden" from each other)*

- *Have time-varying and asymmetric propagation properties*
- *May experience interference from other power line networks operating in overlapping areas"*

While this description was written in hindsight to PLC on 50 and 60 Hz AC power lines, it is also quite accurate for DC networks and shows the challenges a PLC system has to overcome to provide reliable communication.

5.1 The Traction Battery

As the ultimate goal of this work is to find out if a power-line communication is a feasible approach to realize communication in a battery system in an automotive environment, the battery in electrical cars (i.e. traction battery) has to be considered. It is one of the biggest cost-factors in electric vehicles (EV) and to achieve the maximum possible performance in respect to driving range, battery lifetime and safety, the management of the battery and its individual cells is necessary.

This work is based on the power-train of battery electric vehicles (BEV), where the traction battery is responsible for the following functions[15]:

- Supplying power to the drive train
- Supplying power to accessories (e.g. heating, air condition, entertainment,..)
- Recovering of brake energy
- Charging

Fig. 5.1 shows a simplified example of a battery stack with i cells in series and j cells in parallel. The cells are monitored by cell sensor circuits (CSC), which monitor various cell-parameters to provide information on the state of health (SOH) and state of charge (SOC).
The battery management unit (BMU) communicates with the CSCs, measures the current through the battery stack and controls the main relay switches, which can separate the battery stack from the vehicle. For additional safety reasons a main fuse protects the system against over-current. HV+ and HV- mark the positive and negative high voltage battery connectors.
In a typical BEV, the most relevant connections are to:

- a DC/AC converter that supplies the engine (also called inverter)
- a charging circuit for AC and/or DC charging
- a DC/DC converter for the on-board supply

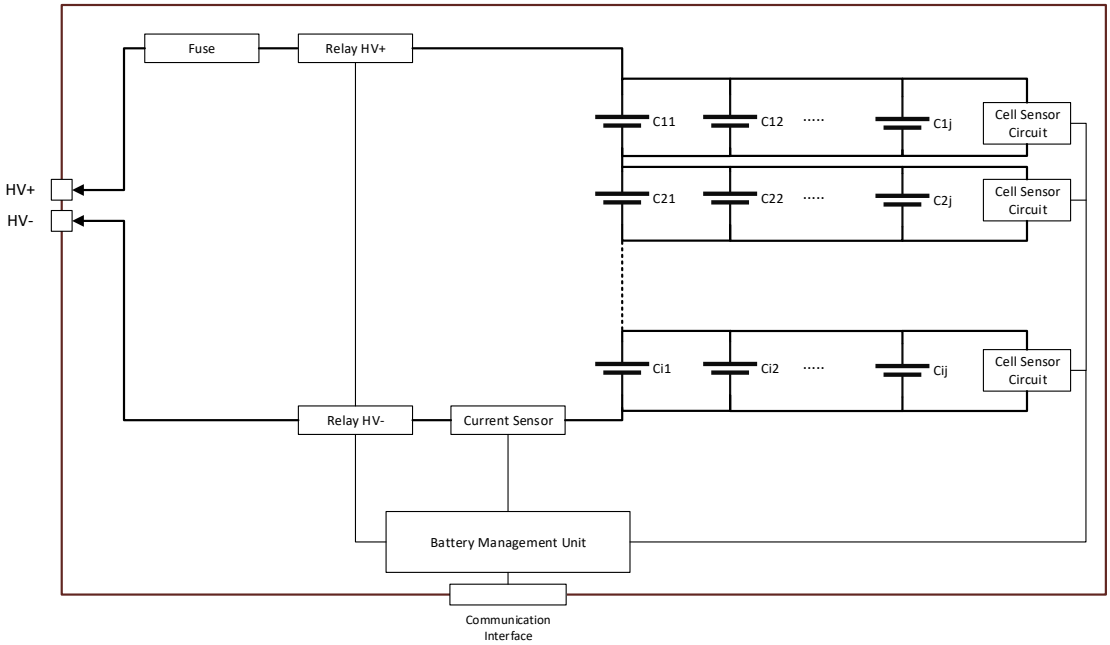

Figure 5.1: A complete battery stack with battery management, main relay and fuse

5.1.1 Example Values

An example battery stack could be:

- 18650 cells
- 96 cells in series / 74 cells in parallel
- Cell capacitance: 3.4 Ah at 3.7 V nominal voltage
- Used cell voltage range: 4.2 V to 3 V
- Total stack capacitance: 89.4 kWh
- Full charged stack voltage: 403.2 V

Note: As no concrete information is published by car manufacturers about their battery architecture, this example values are based on an unofficial tear-down of a "Tesla Model S" and should only show the rough values that are present in state-of-the-art car batteries. Other manufacturers might use bigger prismatic cells, which means that less parallel cells are needed, for smaller batteries, even single cells are used.
A simple calculation shows the amount of current that can flow through a battery. If we assume acceleration and the electric motor demands 100 kW of power (converter efficiency and time dependency disregarded) from a battery at nominal voltage, the needed DC current for this would be:

$$|I_{battery}| = \frac{P_{out}}{N_{cells,series} \cdot V_{cell,nominal}} = \frac{100\,\mathrm{kW}}{96 \cdot 3.7\,\mathrm{V}} = 281.5\,\mathrm{A} \tag{5.1}$$

In high-powered BEVs, the currents flowing out of the battery can exceed 1 kA during acceleration, as quick load changes result in big current spikes.
However, also the currents during charging, especially fast charging systems are to

be considered. An example for "High-Power-Charging" (HPC) with 350 kW and a nearly empty battery with 3 V single cell voltages:

$$|I_{battery}| = \frac{P_{in}}{N_{cells,series} \cdot V_{cell,empty}} = \frac{350\,\mathrm{kW}}{96 \cdot 3\,\mathrm{V}} = 1215A \tag{5.2}$$

5.1.2 The Lithium-Ion Cell

Every Lithium-Ion cell is constructed with a positive electrode (called cathode) and a negative electrode (anode). Between the electrodes, there is an electrolyte and a separator to keep the electrodes from short-circuiting. The anode is usually made of graphite and the cathode material varies depending on the cell chemistry, usually it is comprised of mixed oxides of cobalt, mangan and nickel [18]. The electrolyte carries the Lithium-Ions and can be in fluid, polymer or solid form.

The discussion of different cell chemistries is not in the focus of this thesis and is therefore omitted, but the different geometries of used cells have to be taken into account. The main types of cells currently on the automotive market are

- Cylindrical cells
- Prismatic cells
- Pouch cells

Cylindrical Cells

In cylindrical cells, the anode-separator-cathode-separator stacked material is wrapped multiple times around the positive connector in the middle. The outer electrode of the wrap is connected to the cylindrical enclosure. Different diameters and lengths are possible, the most common sizes are "18650" and "21700". Cylindrical cells can offer advantages in cost due to being easy to manufacture, however their energy-to-space ratio is not perfect due to their round shape.

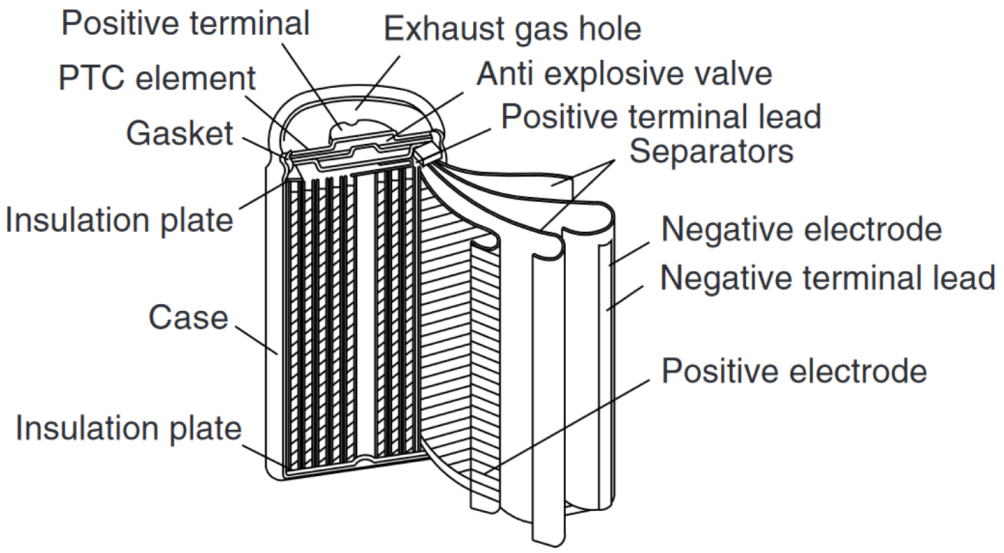

Figure 5.2: The internal structure of cylindrical cells[17]

This work is mainly focused around round LiIon-Cells of the size "18650", which is one of the most popular sizes in consumer electronics. The dimensions of the cell are described by its name: 18 mm in diameter and 65 mm in length. Fig. 5.3 shows an image of the used type of cells in this thesis.

Figure 5.3: A Samsung SDI ICR18650-26J cell

Prismatic Cells

In prismatic cells, the wrapping is very similar to cylindrical cells, except the shape of the wrapping is not circular but rectangular.

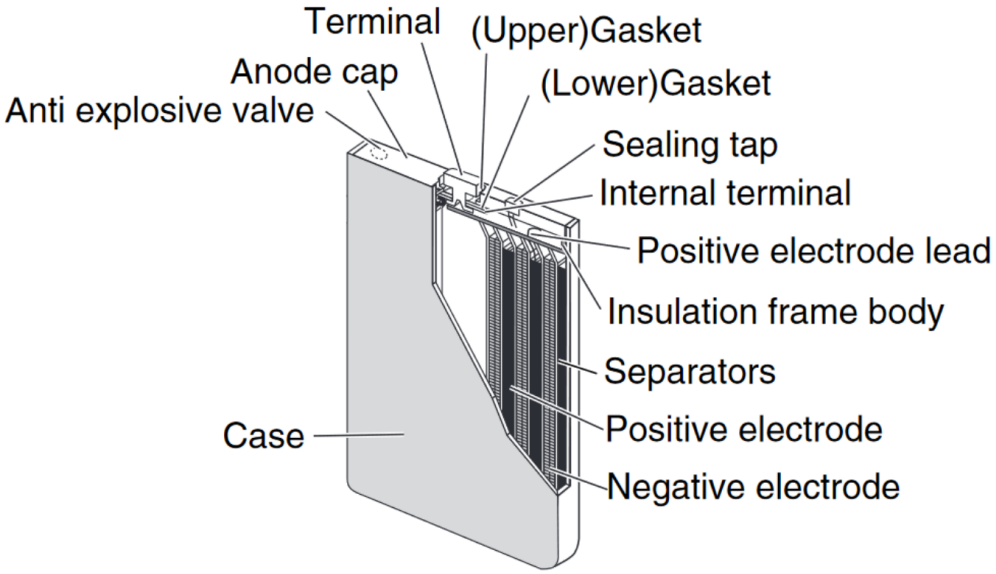

Figure 5.4: The internal structure of prismatic cells[17]

Pouch Cells

Also known as "coffee-bag" cells, the structure of pouch cells differs significantly from the other cells. Instead of wrapping the layers, they are stacked on top of each other. The encasing is usually a thin aluminium foil, which allows good heat conduction and the production in all possible sizes.

Specification of the Used Cell

The used Samsung SDI ICR18650-26J battery cell has the following specification[11]:

- Capacity: 2550 mAh
- Nominal voltage: 3.63 V
- Charge cut-off voltage: 4.2 V
- Discharge cut-off voltage: 2.75 V

For a communication system based on the transmission of radio frequencies (RF), the impedance curves of the elements in the battery stack are of particular interest. Fig. 5.5 shows the impedance plot of an 18650 cell that has been measured with a network analyzer and modelled with an equivalent circuit. The model has been developed by Thomas Landinger (Infineon Munich / Technical University Munich) and was presented at the "2019 IEEE International Symposium on EMC+SIPI" in New Orleans, Louisiana.

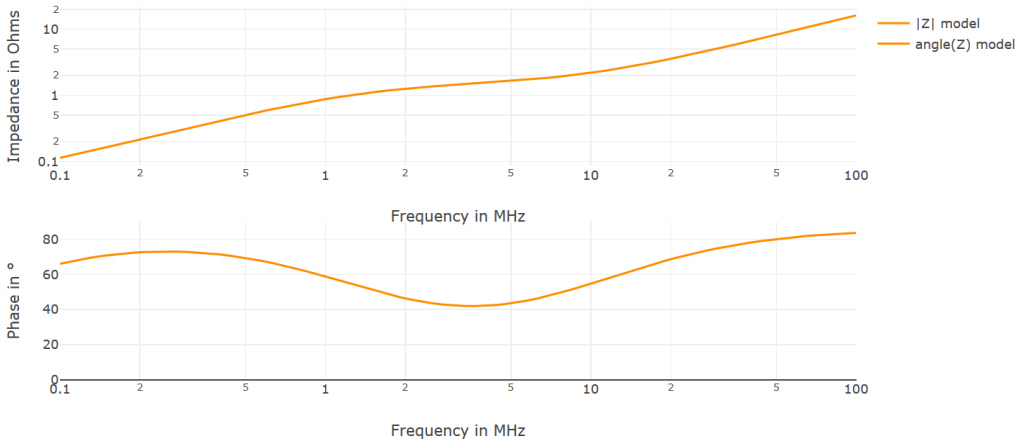

Figure 5.5: Impedance and phase of a 18650 cell.

5.1.3 Dangers of Lithium-Ion Cells

The highest priority in building a vehicle should always be the safety of the passengers and surrounding bystanders. Nevertheless, LiIon battery cells, if mishandled, can produce excessive heat, burn or even explode. To minimize the risks or completely prevent that from happening, great effort is put into the management of the batteries to keep them in a safe operating area. One of the biggest dangers is the growth of dendrites on the electrodes that puncture the separator and short-circuit the cell. When the cells are deep-discharged or overcharged, dendrite growth becomes dangerous. If over- or under-voltage at the battery cell is detected, the BMS should deactivate the car to prevent fire or explosion. The same logic can be applied to the cell temperature. While heating is used to keep the cell warm in colder environments for higher capacity, cooling is needed for big load currents as well as to avoid overheating. If a certain temperature threshold is reached, the car would be switched off. *ISO 26262.2018 - Road vehicles – Functional safety*[9] addresses the development process of such safety-relevant electronic systems and the safety-goals that should be achieved to avoid possible hazards as fire or electric shock that would be caused by the failing of said systems. Most of these safety-goals can be reached by keeping the LiIon cells in their safe-operation area which defines the safe operation limits for temperature, voltage and current.

5.2 Bringing PLC into the Battery Stack

In this work, two different topologies with varying positioning of the PLC "master" are discussed. The "master" is the only element with a wired connection to the outside of the battery or to another control module, while the "slaves" would be battery monitoring circuits with connections only to the cells or modules.

5.2.1 Master Outside the Stack

The first approach was to simply put the "master" device at the HV+ and HV- connections of the stack. In the images Fig. 5.6 and Fig. 5.7 a simplified setup with N cells is show. For simplicity only the n-th cell is shown as a PLC slave. As the power-line is a shared medium and a single carrier modulation is used, the communication can only work one way at a time (half-duplex). This means there are two cases:

Master to Slave Communication

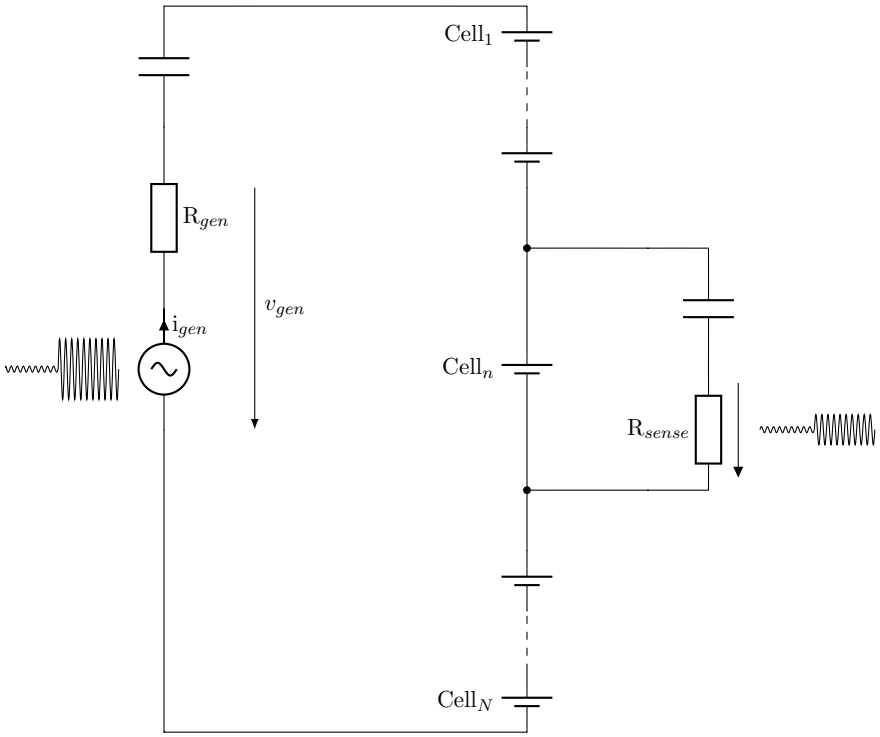

Figure 5.6: Master to slave communication

The master injects the communication signal into the positive and negative poles of the stack, which results in a current flow through the cells. The resulting voltage over the sense resistor then shows the modulated carrier. As the cell impedance is very low, it is preferred to let most of the current flow through the cell and let the sense resistor be significantly bigger than the cell impedance at the used frequency. To remove continuous DC power consumption, the signal generator and receiver are AC coupled with capacitors.
This is very straightforward and the resulting signal strength can be calculated easily

if parasitics are neglected ($R_{sense} >> Z_{cell}$).

$$v_{cell} = i_{gen} \cdot Z_{cell} \tag{5.3}$$

and

$$i_{gen} = \frac{v_{gen}}{R_{gen} + N \cdot Z_{cell}} \tag{5.4}$$

Which gives a simple voltage divider.

$$\frac{v_{gen}}{v_{cell}} = \frac{Z_{cell}}{R_{gen} + N \cdot Z_{cell}} \tag{5.5}$$

However, parasitics have to be considered, as they are very significant. Depending on the used frequency, the connection inductances between the cells, the connection between master and stack as well as the connection between the cells and the power-line receiver degrade the performance of the system by increasing the total impedance and therefore decreasing the current through the loop. Additionally, the current might not flow through the cells but instead through parasitic capacitances.

Slave to Master Communication

If the communication is reversed, the result is a similar voltage divider. However, an issue arises: The low cell impedance requires big currents to achieve significant voltage levels at the cell. In Fig. 5.7, it is shown, how a current is imprinted into the communication loop, but as the impedance of a single cell is significantly lower than that of the whole stack, the biggest part of the current will flow only through the cell. Only a small part will actually flow through the whole system, and the efficiency of this will be very bad. This could be improved in a multi-cell system, where multiple cells are serialized and the total device-count is lower, resulting in a better current transfer.

Topology Issues

This topology has one major disadvantage:
The master is placed directly at HV+ and HV-. This means that the device is directly connected to the HV lines that go to the inverter and other peripherals in a car, which means that they have to be tested against electromagnetic disturbances, for example a "bulk-current injection" (BCI) test. In this test, coils are placed over the wiring harness and rf currents are injected. The ISO Standard ISO 11452-4:2011 specifies currents of up to 100 mA. The BCI test is considered as a component test, where the battery with all of the battery management and communication systems forms a single component. The test would be performed by putting the BCI coils over the high voltage cables that connect the battery to the inverter, DC/DC or other elements. As the current will flow in the path of the least impedance, this could mean that the master will see a big part of the test-current. If one would design a PLC receiver that can still receive and demodulate such a signal, the input stage should not clip, because the BCI disturbance will be added to the PLC signal.

For a receiving circuit with 50 Ω impedance, the received disturbance power would be:

$$P_{bci} = I_{bci}^2 \cdot Z_{receiver} = (100mA)^2 \cdot 50\Omega = 0.5W \approx 27dBm \tag{5.6}$$

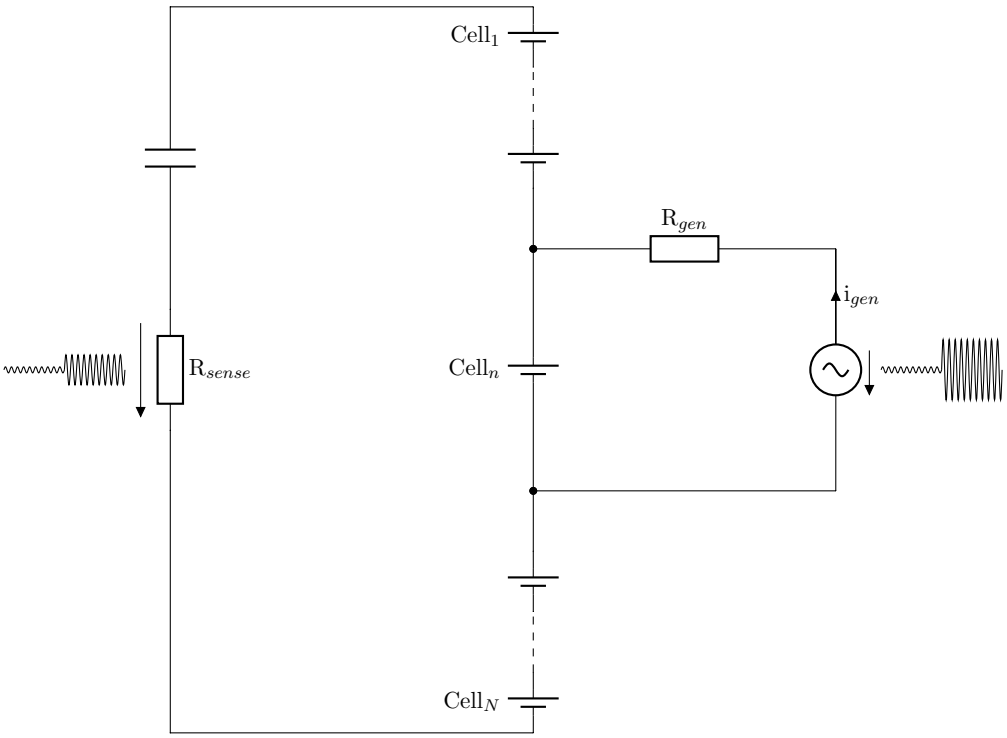

Figure 5.7: Slave to master communication

This high power level brings further problems: The receiver has to be able to dissipate this power while still being able to demodulate the data that is overlapped with this signal and significantly smaller than the disturbance. With frequency hopping or spread spectrum techniques the signal can still be received correctly, but if the input stage starts clipping, the information is lost.

5.2.2 Master Inside the Stack

To overcome the issue regarding BCI testing, a different topology can be used. The master is removed from the outside and instead one of the slaves is used as master, which makes the physical layer of all power-line components equivalent. Fig. 5.8 and Fig. 5.9 show such a topology.

With this topology, the injected BCI current will mostly flow over the loop capacitor instead of the battery stack because of its low rf-impedance. This relaxes the requirements to the communication-system significantly. Not only is the influence of the injected currents reduced, also noise currents from the connected loads will return through the loop capacitor. But it comes with another disadvantage: The communication interface of the master to the "outside" has to be galvanically isolated from the battery stack as one side is supplied by the board supply (a DC/DC converter) and the other side is supplied from the battery. Also, it is very important to ensure that the power-consumption from the cell is similar to the consumption of the slave cell circuits to reduce ageing based on different use. If this cell would age faster then all others, it would degrade the performance of the complete battery stack.

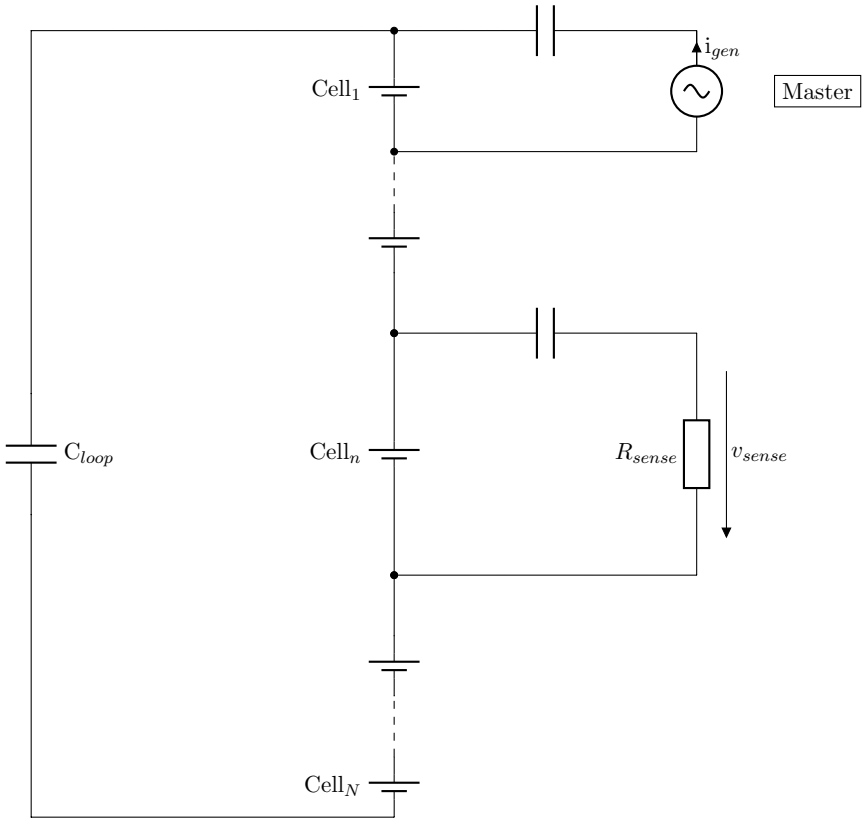

Figure 5.8: Master to slave communication

Comparison to Regular Power-Line

In a comparison between the above topologies and the common in-house power-line, one could see that there is one big difference: While the in-house power-line always uses two wires that are right next to each other (e.g. "L" and "N"), and are connected in "parallel" to each device that is connected to the network, in a battery there is no such connection. Instead of going in parallel to all devices in the system, the communication current flows through all the devices serially and forms a current loop with the dimensions of the battery. The resulting emissions from this loop-current have to be considered before bringing such a system into series production or onto the market.

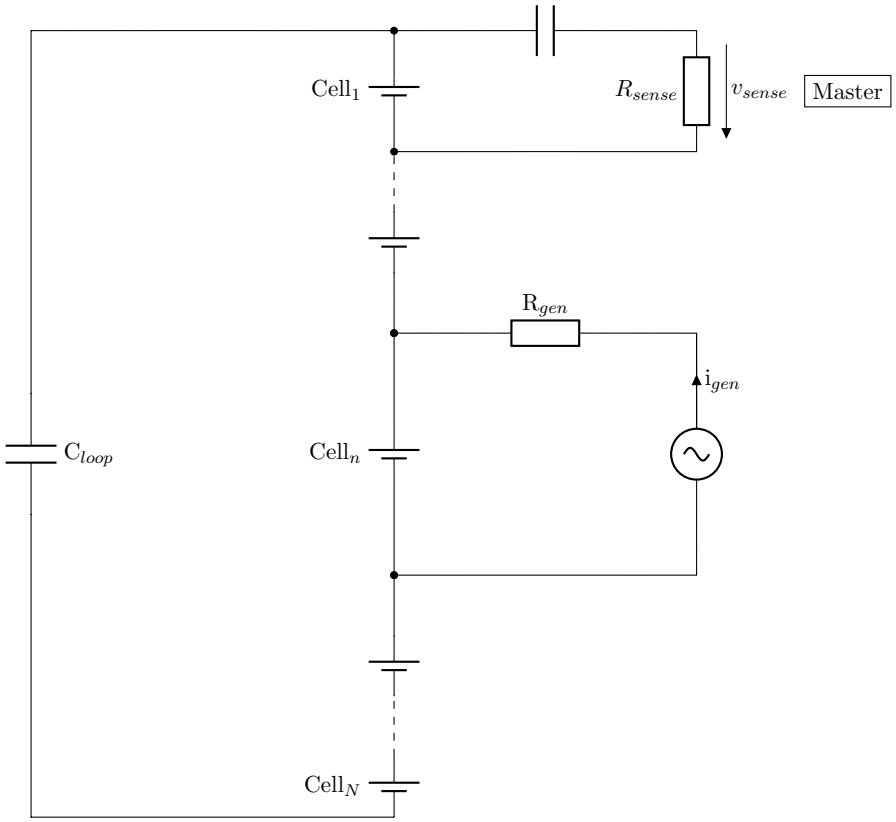

Figure 5.9: Slave to master communication

5.3 Communication Requirements for a Battery-Management-System

As the battery-management system has to detect short-circuits and heat spikes to shut down the car and open the main relays in time, a close-to-real-time communication is needed. Opalko[14] proposes the requirements in Tab. 5.1.

Data rate	2 Mbps
Voltage resolution	14 bit
Temperature resolution	11 bit
Maximum temperature measurement delay	100 ms
Maximum voltage measurement delay	10 ms

Table 5.1: Communication requirements for a battery with 100 cells, by Opalko[14]

The requirements of the time constraints for the voltage measurements are much stricter than the temperature measurements, because any issue with the observed cell will influence the cell voltage immediately. Temperature changes however, are much slower due to the big thermal capacity of the cells. If a cell is heating up due to a dendrite that has grown through the separator, it can take multiple seconds to even detect the increase in temperature.
As the detection of dendrite growth and resulting short-circuits can only be done by observing the cell voltage, the requirements for the maximum delay for the measurement of all cells in the system are much stricter than for the rather slow temperature

sensors. The high data rate is required to achieve these demands for all cells in time and for various other diagnostic data, as well as error detection for reliable communication. This requirement will only increase in the future as more and more sensors are put into the cell-sensor-circuits and cell-impedance measurements are included to provide higher accuracy for state-of-charge and state-of-health estimations.

5.4 Modulation Schemes

Modulation is the process of changing a carrier or base-signal according to a information carrying signal. The information can be either analog or digital, where analog means that the transition is continuous and digital means it changes step-wise. The most important parameters of the carrier signal that can be changed are: Amplitude, Frequency and Phase.

5.4.1 Amplitude Modulation

The amplitude modulation of a carrier with the circular frequency ω_c and the amplitude A_p with the information signal $v(t)$ (where $|v(t)| \leq 1$) can be described as:

$$u(t) = A_p \cdot cos(\omega_c \cdot t) \cdot [1 + v(t)] \tag{5.7}$$

If v(t) is also a cosine signal with $\omega_v < \omega_c$:

$$v(t) = A_v \cdot cos(\omega_v \cdot t) \tag{5.8}$$

Then $u(t)$ can be formulated as:

$$u(t) = A_p \cdot cos(\omega_c \cdot t) + A_p cos(\omega_c \cdot t) \cdot A_v \cdot cos(\omega_v \cdot t) \tag{5.9}$$

With

$$cos(x) \cdot cos(y) = \frac{1}{2} \cdot [sin(x - y) + sin(x + y)] \tag{5.10}$$

the equation can be written as:

$$u(t) = A_p \cdot cos(\omega_c \cdot t) + \frac{A_p \cdot A_v}{2}[sin((\omega_c - \omega_v)t) + sin((\omega_c + \omega_v)t)] \tag{5.11}$$

This means that the spectrum of the modulated signal has no components at the frequency of the modulating signal, however it contains the frequencies of the carrier-signal and two side-bands at both sides of the carrier frequency with a distance of the modulating frequency. In Fig. 5.10 the typical spectrum of such a modulated signal can be seen.

Another important key figure in describing an amplitude-modulating system is the modulation index. It is described as the ratio of the maximum amplitude of the information carrying signal to the amplitude of the unmodulated carrier.

$$m = \frac{max(v(t))}{A_p} \tag{5.12}$$

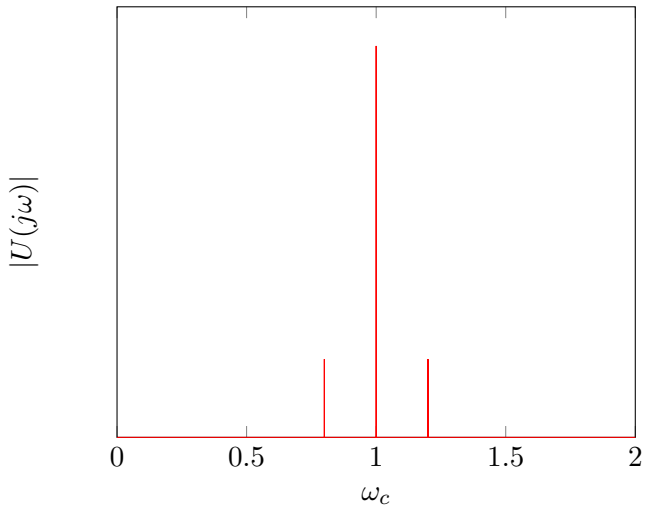

Figure 5.10: Frequency spectrum of an amplitude modulated carrier signal

On-Off-Keying

If the modulation index m is equal to 1, this special case is called "on-off-keying". In other words, the carrier wave is simply switched on and off to produce the modulated signal. This is of course a digital modulation, a digital value of "high" or "one" can be assigned to "the carrier is present" and a logical "low" or "zero" can be assigned if no carrier signal is received.

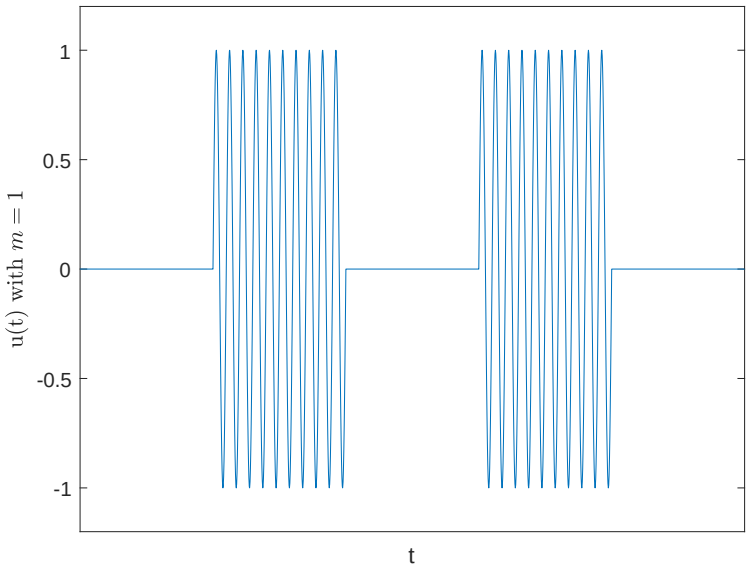

Figure 5.11: A On-Off-keyed carrier

Demodulation

In order to get the information back from the modulated signal, the signal can be processed by coherent or non-coherent demodulation. The coherent demodulation approach would be to multiply the incoming signal with the carrier signal. If the used carrier signal is in-phase with the originally used carrier, the spectrum of the AM signal is shifted into the base-band (additionally to frequencies of $\pm 2\omega_c$), where

it can be low-pass filtered to recover the original signal.
In practice, during the transmission from transmitter to receiver, noise will disturb the incoming signal. As the shown circuit will demodulate all frequencies, it is necessary to bandpass-filter the input to reduce disturbances from out-of-band noise or other transmission signals.

Amplitude modulation is possibly the most easy-to-realize type of modulation; however it comes with a serious drawback in comparison to other modulation types: In-band-noise is directly influencing the amplitude of the incoming signal and cannot be filtered out.

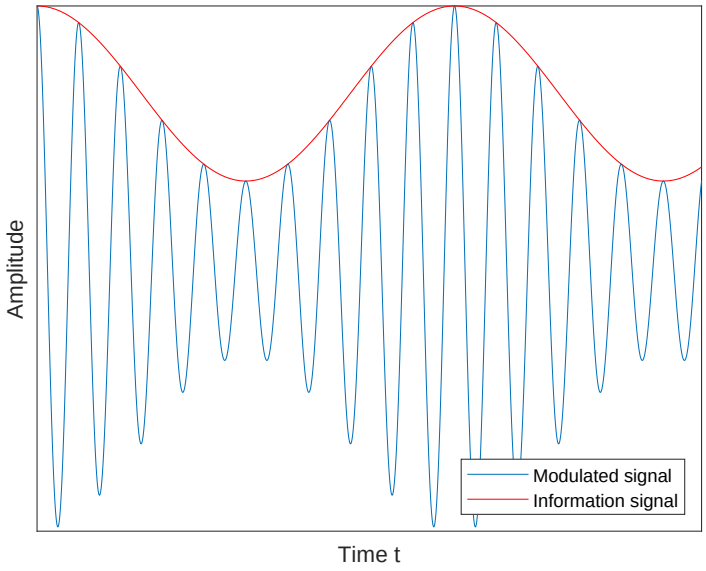

Figure 5.12: AM signal and the modulation signal

Non-coherent demodulation is done by recovering the information from the envelope of a signal. The demodulation used in this work is done by using non-coherent demodulation. One way of doing this, is by rectifying and low-pass filtering the signal, like shown in Fig. 5.12. The positive cycles of the input signal charge the capacitor to the highest voltage in the signal, for all lower voltages the diode blocks discharge currents from the input, and the capacitor is only discharged by the parallel resistor. By carefully choosing capacitance and resistance, the resulting signal will be the ground truth minus the voltage drop across the diode and additional DC, which can be filtered out easily by high-pass filtering if needed.

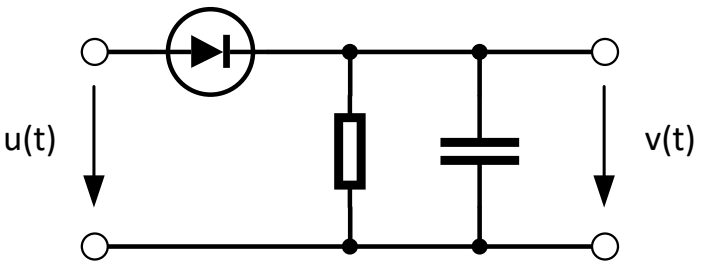

Figure 5.13: Envelope detector demodulation circuit

5.4.2 Frequency Modulation

Another way of imprinting information on a sine shaped carrier is to modulate the frequency of the carrier signal.

$$u(t) = A_p \cdot cos((\omega_c + \omega_i) \cdot t) \tag{5.13}$$

The information that is contained in this resulting signal has no dependence to the amplitude, which means that additive noise does not disturb the signal as long as the frequency can be detected correctly and therefore a massive improvement to AM with bandwidth as a trade-off for robustness. Fig. 5.14 shows a frequency-modulated signal in the time domain. This special case where the carrier is switched between two distinctive frequencies is called "frequency shift keying" (FSK).

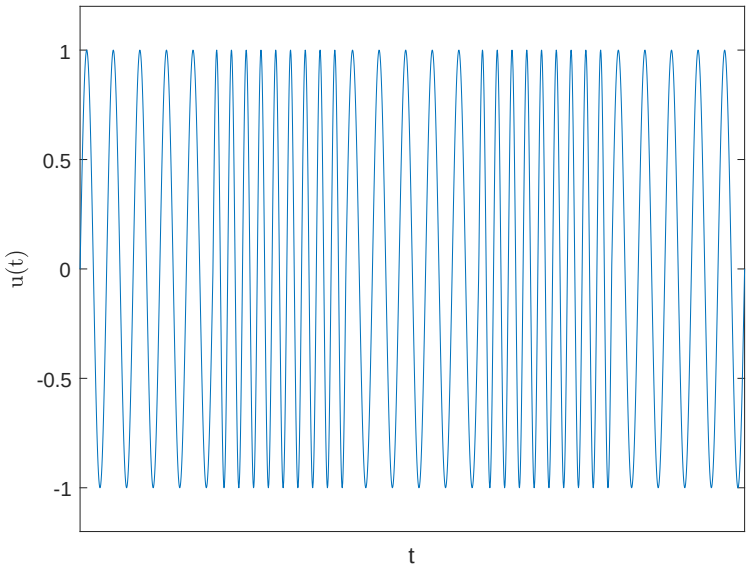

Figure 5.14: Frequency shift keying

The demodulation of frequency-modulated signals can be done by differentiation and detection of the resulting envelope, because the differentiation results in multiplication with $j \cdot \omega$ in the frequency domain, which means the amplitude of the differentiated signal is proportional to the frequency. Then, an envelope detector can be used directly to get the information.

Another way of demodulating a FM signal is by using a "phase-locked loop" (PLL). A phase detector is used to compare the frequency of the modulated signal with a local voltage-controlled oscillator (VCO). It generates a control voltage proportional to the phase difference, which is filtered and fed to the VCO. If the phase difference approaches zero, the PLL is locked in and the control voltage is proportional to the carried information.

5.4.3 Phase Modulation

In phase modulation, the information is applied to the phase of the carrier.

$$u(t) = A_p \cdot cos(\omega_c \cdot t + \phi_i) \tag{5.14}$$

The practical use of analog phase modulation is very limited, as the receiver has

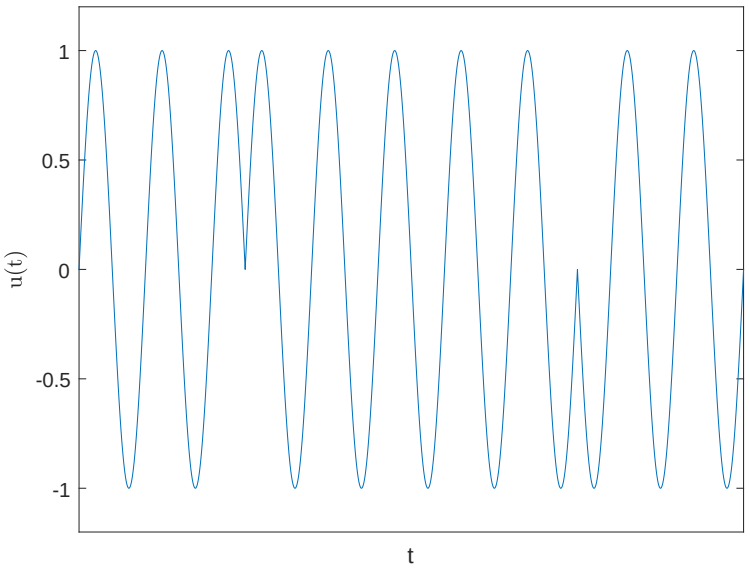

Figure 5.15: Phase shift keying - BPSK

to know the true phase of the used carrier at all times, which would be extremely complex in an analog circuit and phase synchronization would be needed to compensate for drift. However, in digital systems, this can be done easily and is used in phase-shift keying PSK. The easiest form of PSK is binary-PSK (B-PSK), where the phases 0° and 180° are used; also combinations of a higher number of phases are possible (e.g. Quadrature phase shift keying - QPSK with 0°, 90°, 180° and 270°, 8-PSK, 64-PSK, etc.).

5.4.4 Orthogonal Frequency Division Multiplexing

In digital communication systems, orthogonal frequency division multiplexing (OFDM) has been proven to be one of the most useful techniques for high-data rate systems. It is used in WiFi (IEEE802.11), terrestrial television, mobile communications (LTE, 5G), power-line communications and many others.

OFDM is a multi-carrier modulation where each carrier has its own modulation, the complexity of the sub-carrier modulations in most applications is based on the channel characteristics and noise. If the sub-carrier uses a "good" frequency band, a higher order modulation is used (e.g. DOCSIS 3.1 for cable internet uses up to 4096-QAM) and on "bad" channels, more robust modulations are used (e.g. B-PSK).

The main advantage of OFDM in comparison to a simpler multi-carrier carrier system is its spectral efficiency ($\frac{Bitrate}{Bandwidth}$) and reduced effort in filters for each sub-carrier. Where a normal frequency-division-multiplex system needs to have guard-bands around the sub-carrier frequency and sharp filters for each carrier to avoid inter-symbol interference, the orthogonality of sub-carriers can be exploited to eliminate this problems. Said orthogonality of the carriers requires the spacing between the sub-carriers to be $\Delta f = \frac{k}{t_{symbol}}$ where k is a positive integer number (mostly 1 is used). A visualization for this principle is provided in Fig. 5.17. The spectrum of a B-PSK modulated square wave (Fig. 5.16) has its zero crossings at $f_c \pm \frac{k}{Tsymbol}$, by spacing the sub-carriers with the same factor, the peak of each sub-carrier falls into the zero-crossings of all other carriers. This means the sub-carriers are orthogonal

and that there is no interference between them.

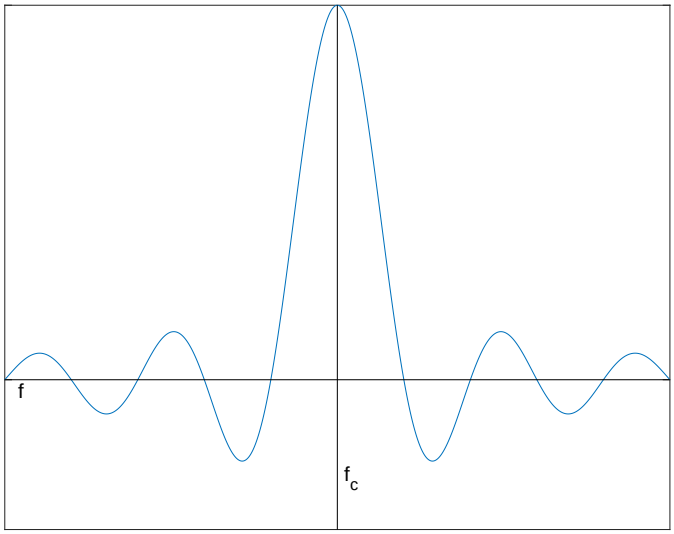

Figure 5.16: The power spectrum of a BPSK modulated square (linear scale)

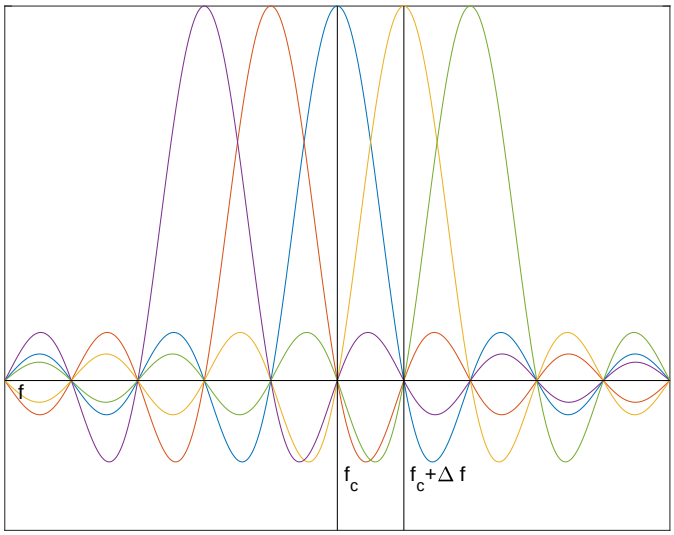

Figure 5.17: The peak of each carrier falls exactly into the zero crossings of all other carriers

The modulation and demodulation of such signals is done completely in the digital domain. The block diagrams in Fig. 5.18 and Fig. 5.19 show the structures of modulator and demodulator respectively.

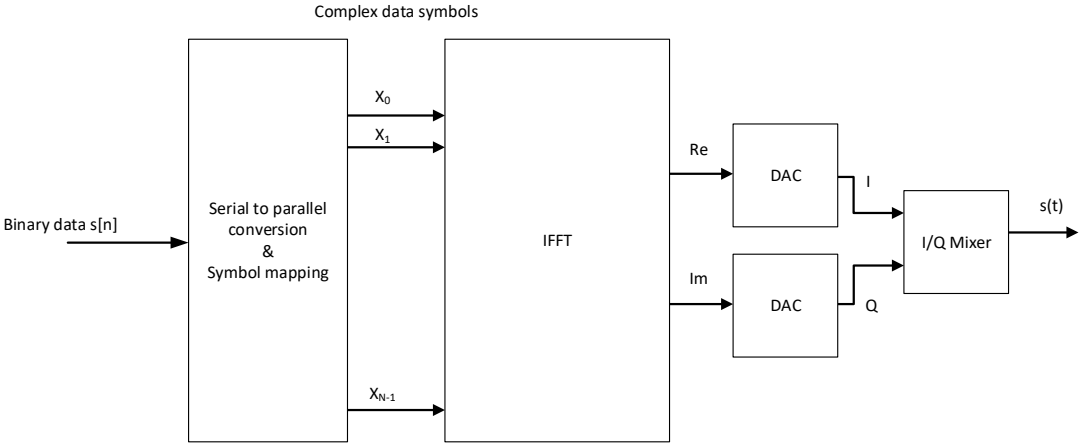

Figure 5.18: The block diagram of an OFDM modulation circuit

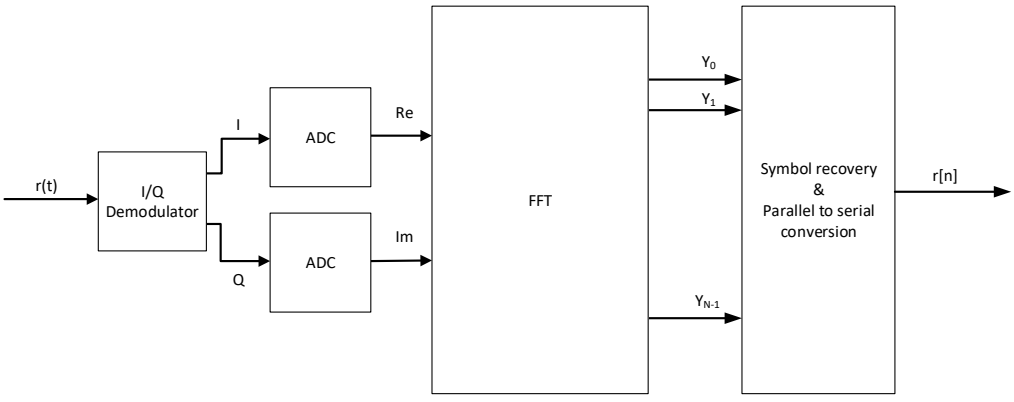

Figure 5.19: The block diagram of an OFDM demodulation circuit

6 Method

6.1 Concept

The constructed demonstrator has the architecture seen in Fig. 6.1. Each slave-cell in use, has its own power-supply circuit which filters the carrier signals and other disturbances on the cell and provides analog and digital supplies for the other blocks. For the receiving chain, the preamplifier first amplifies the PLC signal for the ”demodulation”, which is done by an amplitude detector. Then the signal is fed to a comparator which converts it to the digital domain. The transmit chain is based around an oscillator, which is switched on and off for the OOK modulated signal and then an amplifier which drives the signal into the cell and the battery stack. The microcontroller controls the sent and received data flow and provides interfaces for a display and buttons as well as a simple cell voltage measurement and the internal temperature to provide dummy data.

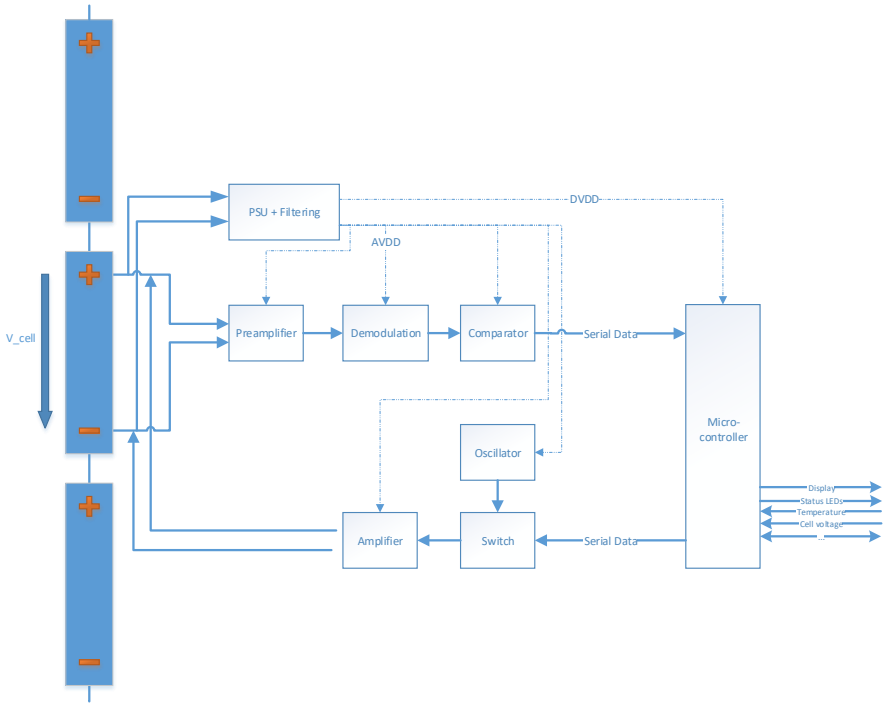

Figure 6.1: The proposed concept for the demonstrator

6.2 PCB Design

The constructed demonstrator was split into blocks similar to the block-diagram in Fig. 6.1.

6.2.1 Top Level Schematic

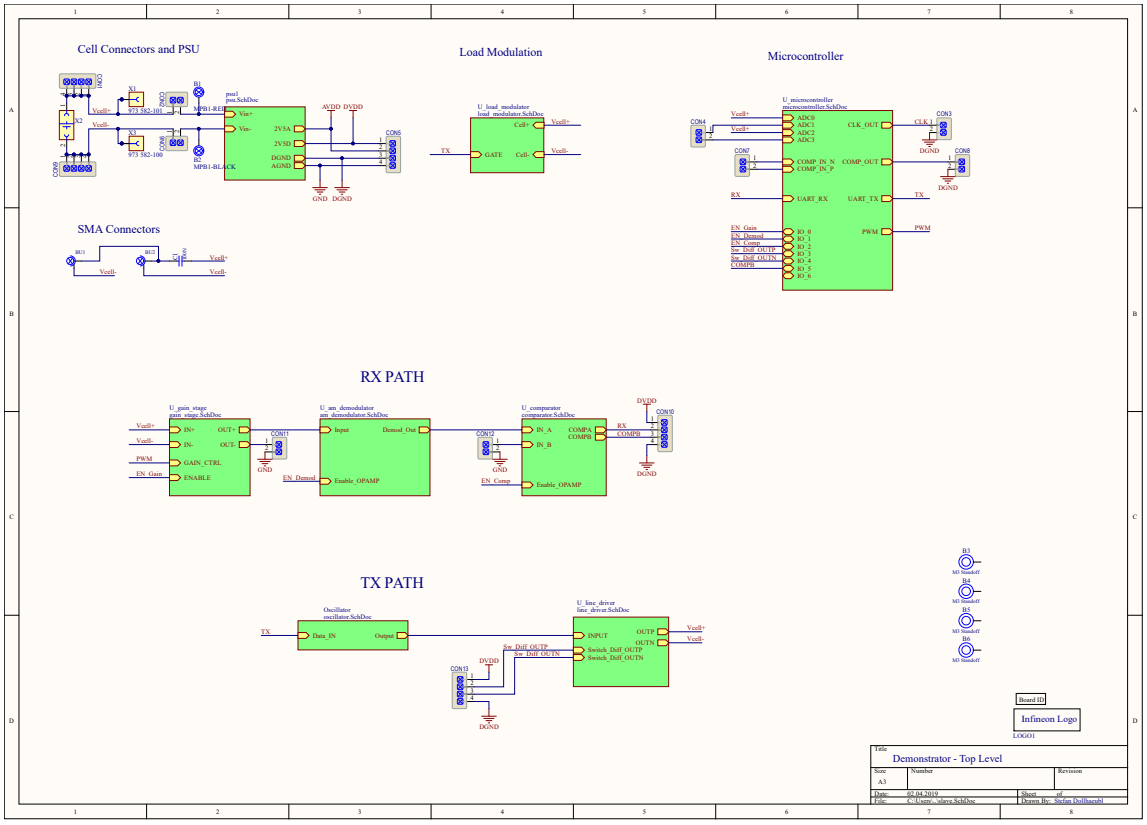

Figure 6.2: Top level schematic

The top level shows the block-based design approach where the transmit and receive chain are completely separated from each other. The microcontroller handles transmit and receive signals, while also offering the possibility to monitor the cell voltage and controls all other peripherals. The power-supply circuit provides one analog and one digital supply rail each with separated grounds. The board provides a 18650 cell holder as well as connectors to directly supply the circuits. To provide an additional communication option, a load modulation circuit was also put on the PCB and for future measurements or prototyping, two SMA connectors where fitted to the board.

6.2.2 Power Supply

The power supply offers an extensive amount of filtering, including a common-mode choke, a big power inductor, various footprints for capacitors and ferrites to decouple the power-supply from the communication signals. For each rail (analog and digital) a dedicated low-drop linear regulator provides a supply voltage of 3.05 V and enough current capabilities for the attached components. The voltage of 3.05V was chosen on one hand to provide a big operating range for various cell voltages and on the

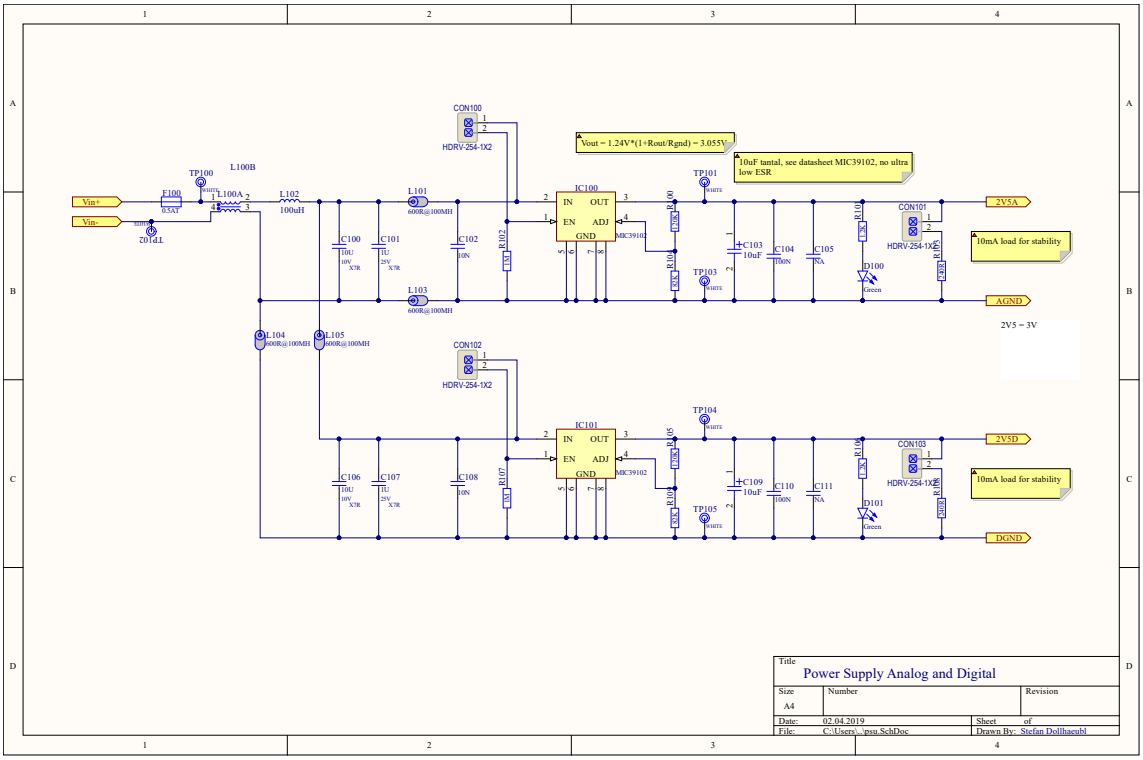

Figure 6.3: Power supply schematic

other hand to provide a safe region of operation for components that are specified for a minimum supply voltage of 3 V.
Note: The naming of the output ports 2V5A and 2V5D is a relict of an older version where the minimum supply voltage was set to 2.5 V.

6.2.3 Preamplifier

As the demodulation circuit works best with big amplitudes, it is needed to amplify the incoming signal in some way. The chosen IC for this signal conditioning is an "Analog Devices AD8330"[5] variable gain amplifier(VGA), which is a differential amplifier with linear adjustable gain from 0 to 50 dB (and additional gain from +20 dB to -30 dB). This makes it a good fit in this application, as the final amplitude of the received signal can not be estimated accurately beforehand. The gain control voltage VDBS can either be set with a potentiometer or from an external source. This device could be used in an automatic gain control (AGC) circuit in the future. The input section offers the possibility for high- and low-pass filtering, another low-pass filter is placed at the output. Via the control interfaces, gain can be controlled linear-in-dB via the VDBS pin and additionally via the magnitude control interface VMAG.

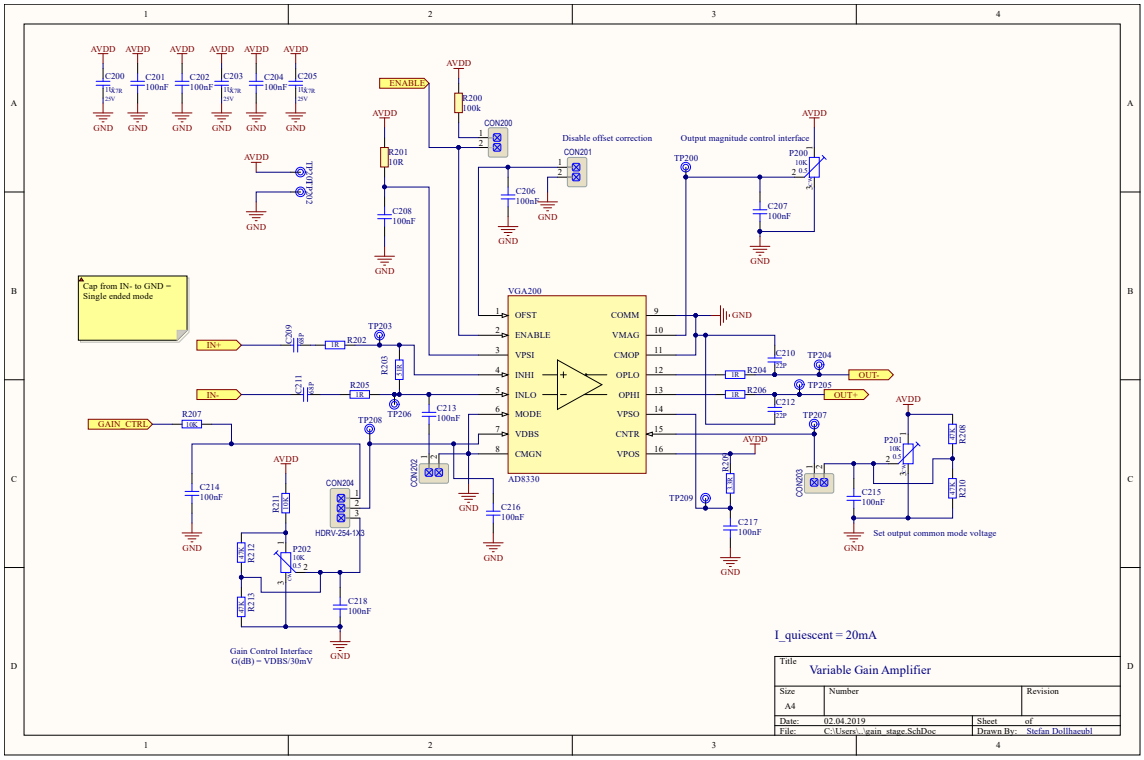

Figure 6.4: Preamplifier schematic

6.2.4 Demodulation

In the demodulation block, the incoming signal is conditioned via an AC coupled active bandpass-filter which should remove out-of-band noise from the signal. It is then decoded using a simple passive diode detector with low-pass filtering afterwards. There is also the option to build an active rectifier for the signals if the performance of the passive detector should prove to be not good enough. However, due to the adjustable input amplitude, this should not be a problem.

If the operational amplifiers have to swing down to true zero volts, a negative charge-pump can supply the negative rail voltage of -0.232 V. For normal operation this should not be needed.

Found Errors or Improvements

The label "-Vbias_demod" should be named "-Vbias", to connect the negative supply of the operational amplifier correctly.
The connection from the output of the operational amplifier IC300B to the filter network around TP303 is wrong, the connection should be to pin 1 of D301/D302, D303 and D304 are unused.

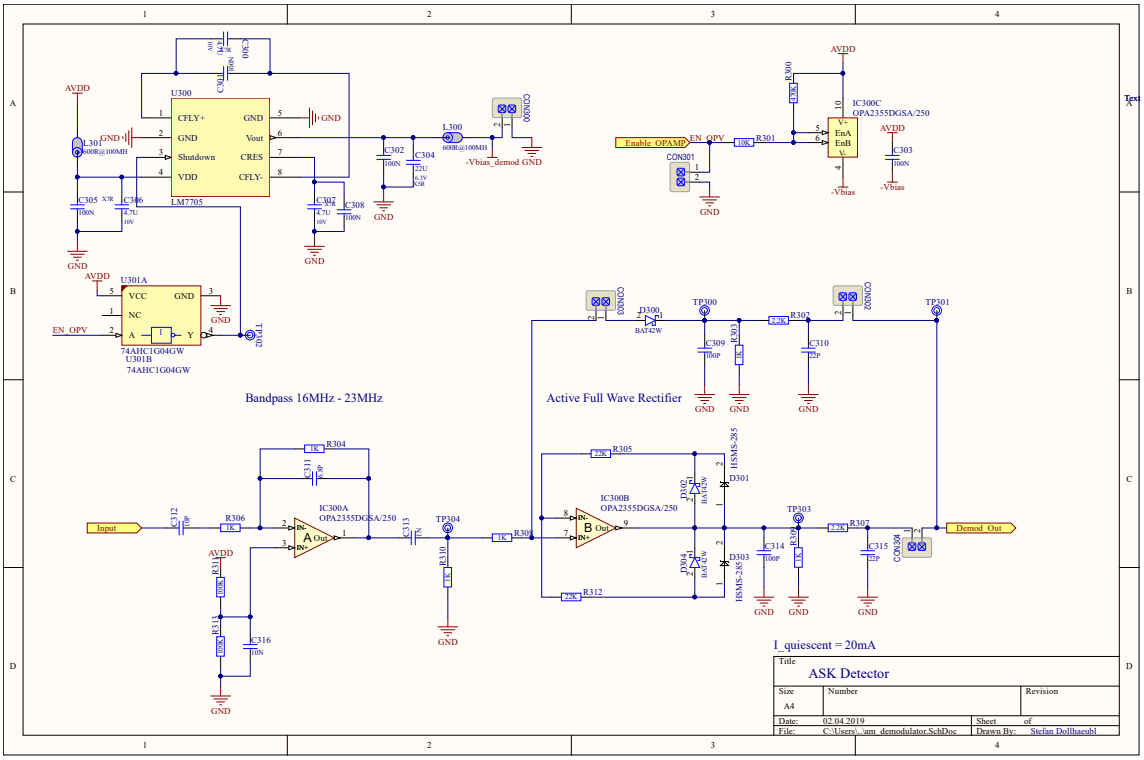

Figure 6.5: Demodulator schematic

6.2.5 Comparator

To convert the analog signal to the digital domain, a comparator with hysteresis ("Texas Instruments TLV3502"[21]) is used. The reference voltage is derived from a voltage reference IC ("Texas Instruments REF2920"[20]) and a resistive divider. To reduce glitches and errors in the signal, a hysteresis can be set. If additional signal conditioning such as offset correction is needed, two additional operational amplifiers can be used in subtraction configuration.

Found Errors or Improvements

The feedback resistors from the comparator outputs to the positive inputs are cross-swapped. In a future revision, the feedback resistors should be connected from INA_P to OUTA as well as INB_P to OUTB.

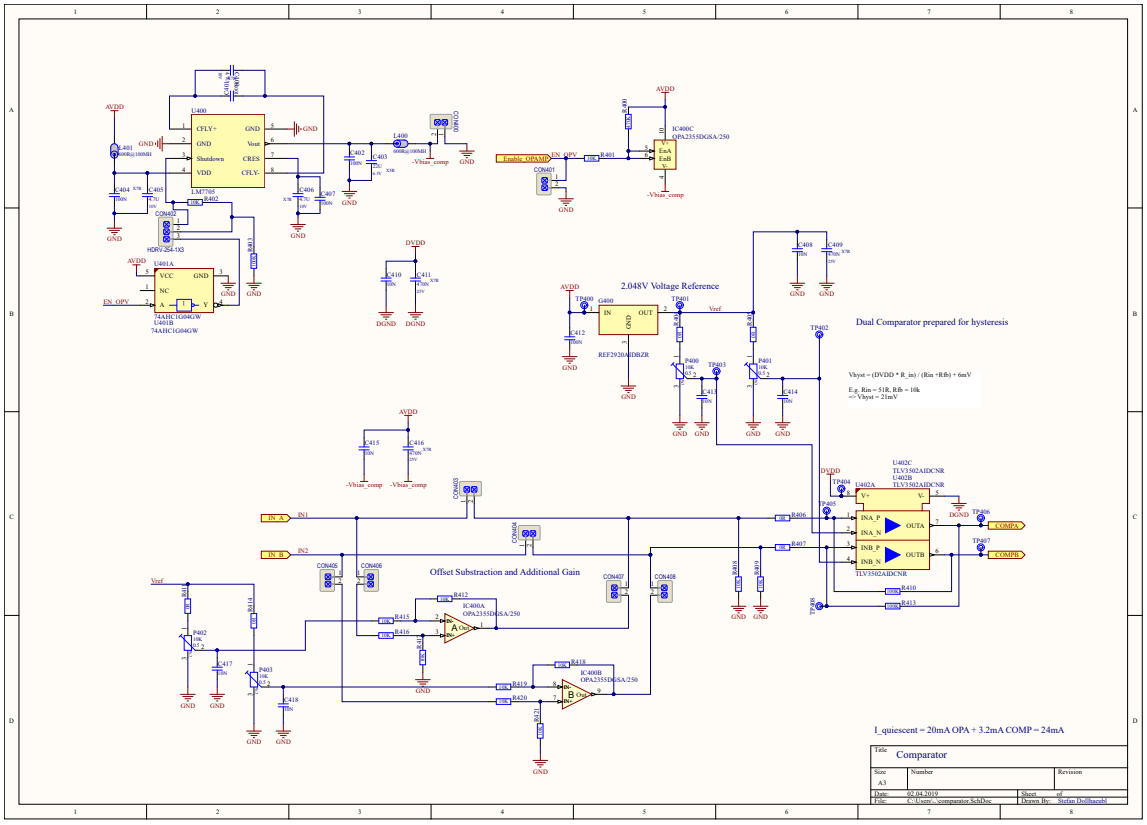

Figure 6.6: Comparator schematic

6.2.6 Oscillator and Switch

A local oscillator is used to generate the carrier frequency for the modulated ASK signal. The oscillator is a simple Hartley-oscillator followed by a voltage follower to buffer the signal. A second voltage follower can also be used as a back-up or additional filter.

The OOK modulation is done by switching the output from a capacitor, which presents a high frequency short circuit to ground, to the output of the buffer.

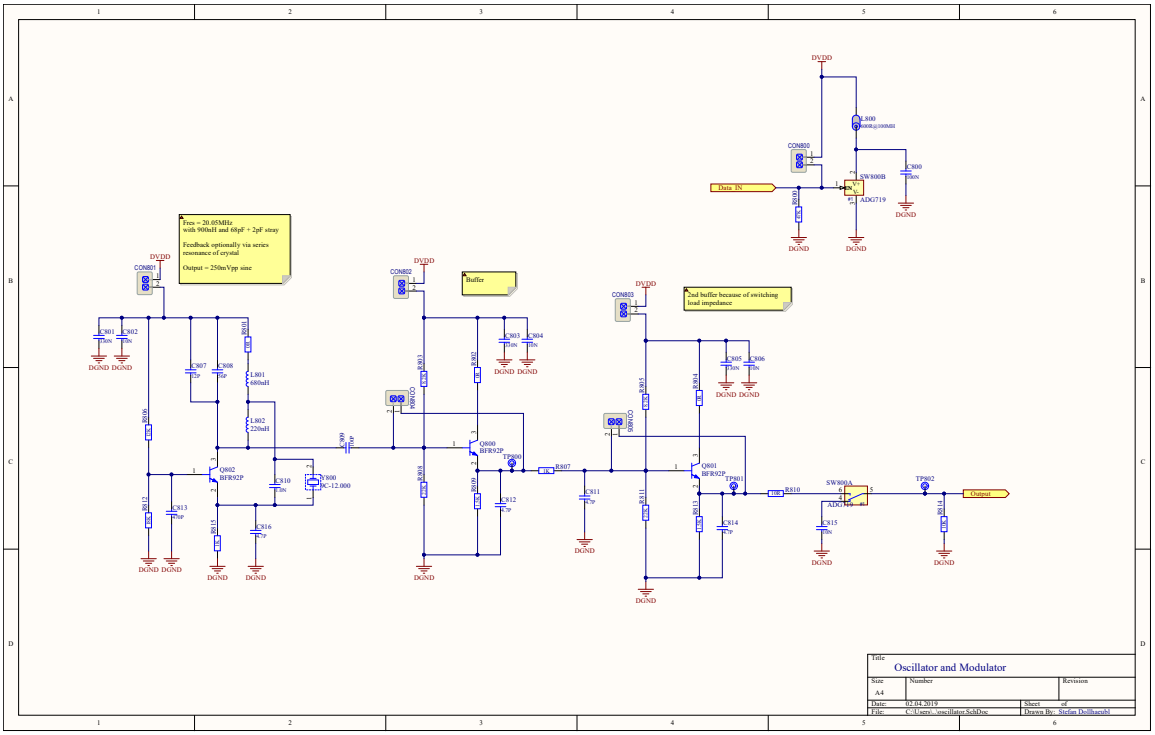

Figure 6.7: Oscillator and modulator schematic

6.2.7 Amplifier

The designed PCB offers two variants for the output amplifier: One is a "Analog Devices AD8132[3]" differential amplifier (pin compatible with AD8138[4]), the other is a push-pull amplifier with a BFR92[12]/BFT92[13] complementary pair. Both can be connected to the battery with "Texas Instruments TS5A21366"[22] analogue switches.

Found Errors or Improvements

The analog switches are supplied by the regulated AVDD voltage (3.05 V), however the battery voltage ranges at least from 2.7 V to 4.2 V, which is out of the usable range for the switches. In a future revision, the devices should be supplied directly by the battery, or alternatively the battery should be AC coupled.

At the outputs of the differential amplifier there should be AC coupling capacitors.

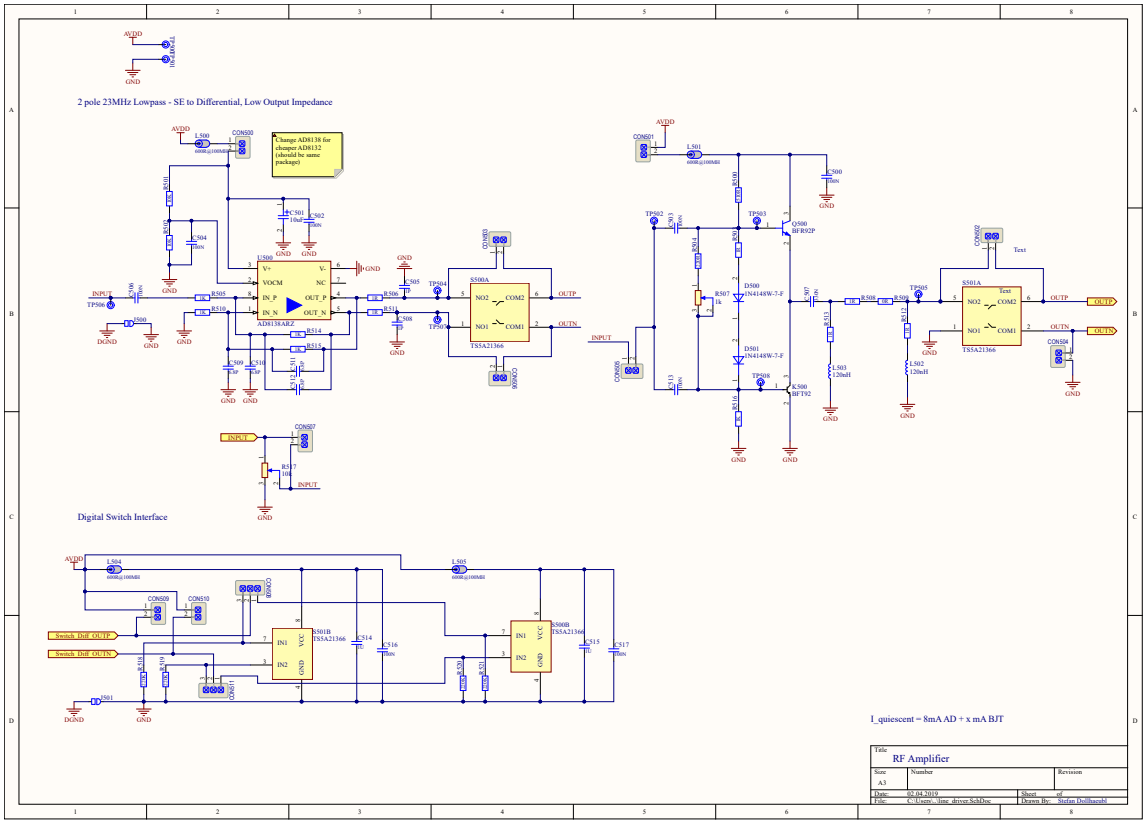

Figure 6.8: Amplifier schematic

6.2.8 Microcontroller

An Infineon XMC1404 Boot Kit[8] was chosen as a microcontroller sub-board for the following reasons:

- Power supply range of 1.8 V to 5.5 V fullfills the needs for low-voltage supply without additional boost regulators
- Reduced complexity of the PCB design as this is not the main goal of this work
- Sufficient computing power for the application while keeping the needed supply current relatively low
- Enough peripherals (Timers, UART, I2C,..) for the application

Additionally, the board was fitted with four push-buttons, a connector for I2C displays, a jumper for master/slave selection and decoupling capacitors. In addition, two ADC pins have resistive dividers to convert voltages greater than the microcontroller supply to the digital domain.

Found Errors or Improvements

The I2C pins SDA and SCL should be fitted with pull-up resistors.
The ADC inputs should not be connected directly to the battery cell, but instead after the power-supply jumpers. This should be done to avoid the back-supplying of the microcontroller over the ADC inputs when the power-supply jumpers are open.

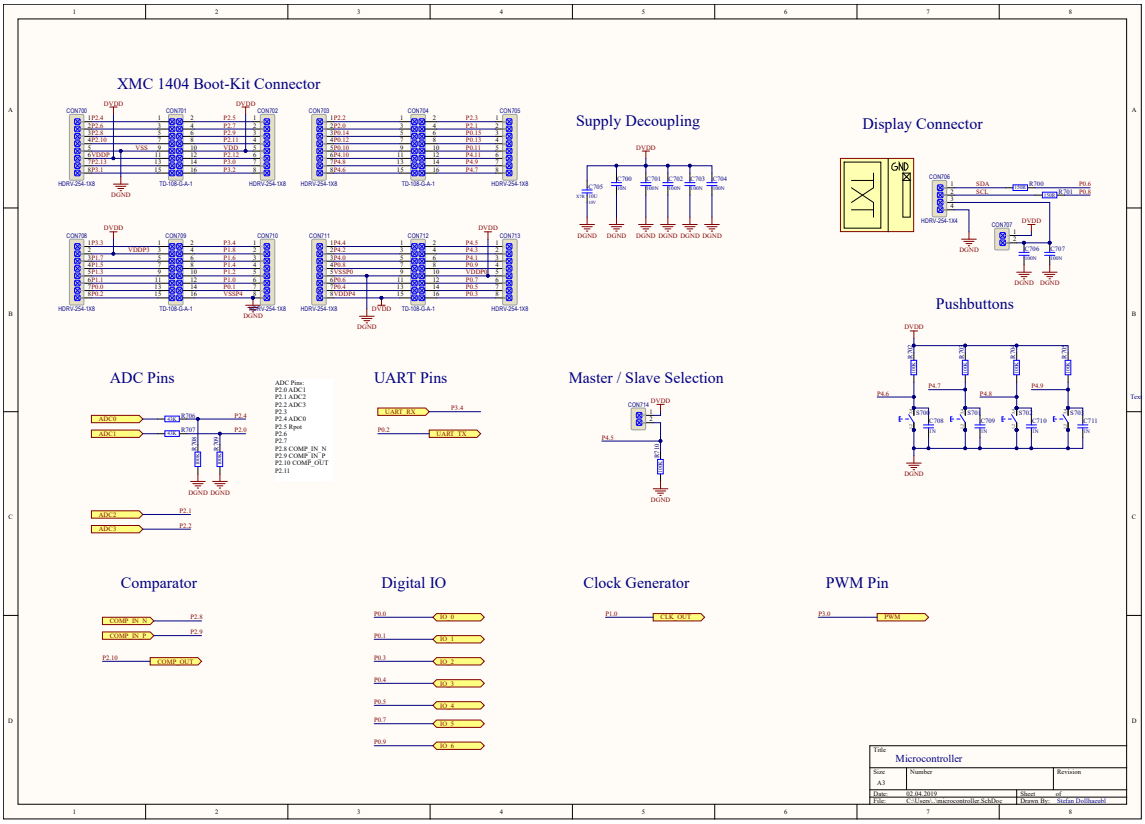

Figure 6.9: Microcontroller schematic

6.2.9 Load Modulator

Another option to imprint the ASK onto the battery cell is to switch a load on and off with the carrier frequency. As the design was developed, this was not a priority, but still the goal was to give as many options as might be necessary. This is the reason why different transistors, loads and jumpers have been placed.

Found Errors or Improvements

The "GATE" input of the load modulator block is connected to a UART transmit output, but instead it should be connected to a PWM pin, that can be gated by the UART block inside the microcontroller, which means the output of the microcontroller is already an on-off-keyed digital signal.
The connection leading to the "GATE" input is very long and in combination with the input capacitance of the MOSFETs, the microcontroller cannot drive the gate voltage fast enough at the required carrier frequency (see Section 7.1.6 for more details). This should be fixed in a future revision by placing a driver or buffer at the gate.

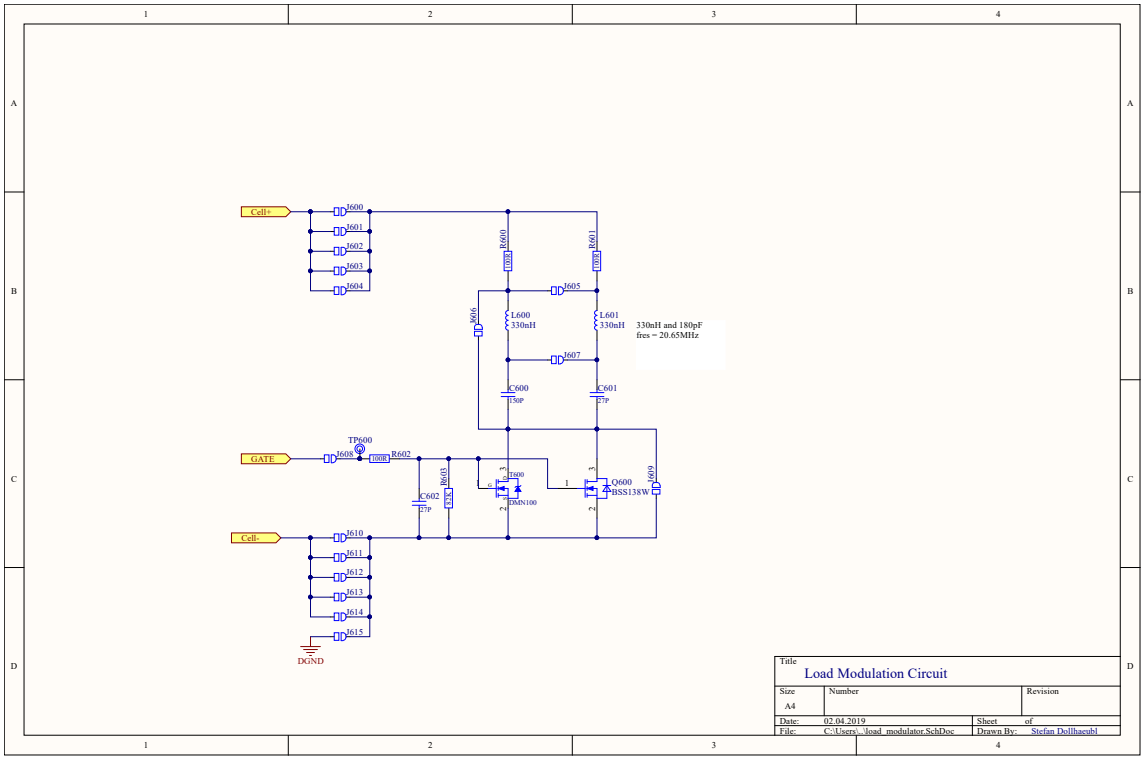

Figure 6.10: Load modulator schematic

6.2.10 Software

To use the demonstrator PCB as a "stand-alone slave" and as pc-connected "master", two variants of the microcontroller software have been developed.
The master should be able to connect to a PC, preferably via a virtual COM-port to transmit and receive UART data from USB and translate it to the power-line communication.
The slave offers the possibility to send out dummy data on its own as well as respond to specific commands.

Features

The master features can be summarized:

- USB-to-UART interface
- USB-UART to PLC-UART translation (for better configurability)

The slave variant is more complex:

- Receive and send PLC-UART commands
- Push data to an SSD1306 display
- Measure the internal temperature of the microcontroller
- Cell voltage measurement
- Potentiometer voltage measurement
- Respond to UART commands with debug and data packets with CRC

Data Request Commands

To show the functionality of the power-line communication, two commands were implemented. They consist of a simple 8-bit address that is sent out by the master and the slave responds to. For systems with multiple slaves, a more complex addressing scheme would have to be implemented.

Adress	Function
0x31	Send out 256 UART frames with data 0x00 to 0xFF
0x32	Respond with measured data and CRC

Table 6.1: Used commands.

Adress	Byte 0	Byte 1	Byte 2:5	Byte 6:9	Byte 10	Byte 11
0x32	Temperature	0x00	Cell Voltage	Pot. voltage	0x00	CRC8(0:10)
-	uint8_t	-	float	float	-	Polynomial 0x07

Table 6.2: Request data command and corresponding data types.

The used CRC is the standard CRC8 with polynomial 0x07 and initial value 0x00 and the used format for the floating point data is IEEE 754 in little endian order.

7 Results

To prepare for the first testing of the developed PCB, a verification plan for the different blocks and also for the complete system was made. First, a single PCB was soldered block-wise and each block tested for functionality. Various measurements were made to verify the behaviour of the demonstrator PCBs blocks, and afterwards, a second PCB was built and tested to prepare for tests on a small battery stack.

7.1 Block Verification

All measurements that verify the functionality of single blocks, have been performed only on one PCB.

7.1.1 Power Supply

The first step in verifying the functionality of the PCB was to check the power-supply. All measurements have been performed with a resistive divider of 120 kΩ and 82 kΩ to give an output voltage of 3.055 V. At the outputs, green LEDs with 2.2 kΩ resistors were placed.

Output Voltage

	Input voltage	Output voltage	Quiescent current
Analog supply	5 V	3.060 V	834 uA
Digital Supply	5 V	3.059 V	833 uA

Table 7.1: Power supply characterisitics

Load Regulation

To show that the supply voltages stay at least bigger than 3 V under load, a load regulation measurement has been done by increasing the load current with a source-measure unit.
The measurement results can be seen in Fig. 7.1. The linear regulators show no significant drop in the output voltage and should be sufficient for the application.

Power Supply Rejection of Communication Signals

The power supply rails should not be influenced even during a communication on the power-line, so the rejection of sine-shaped signals in the range of 1 to 30 MHz has been measured. This was done by injecting an AC signal with an amplitude

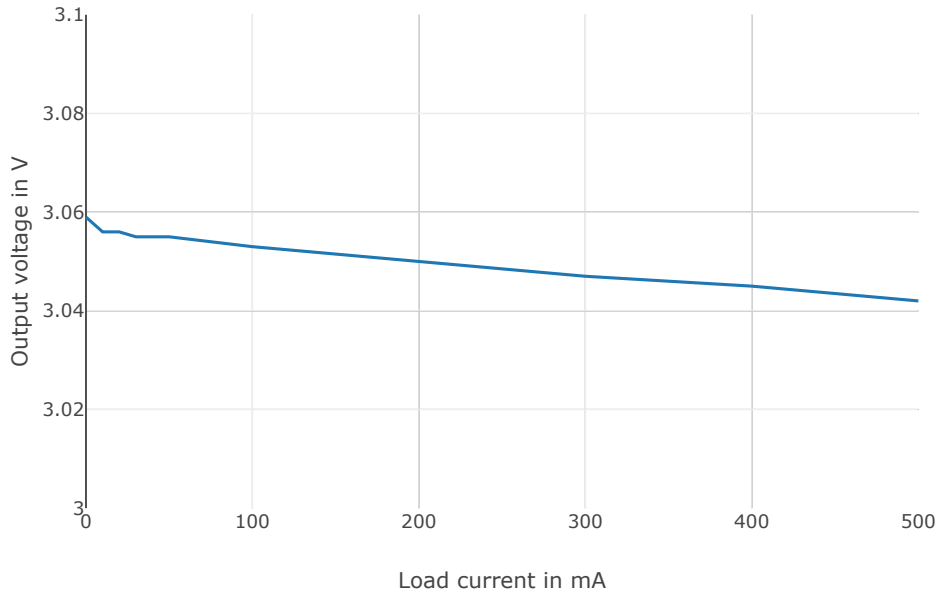

Figure 7.1: Voltage versus load current

of 500mV into the SMA connector BU1 that is connected to the supply voltage via a DC-blocking capacitor. Then the input and output voltage of the regulator are measured and the power-supply rejection ratio is calculated as follows:

$$PSRR = 20 \cdot log_{10} \frac{V_{out}}{V_{in}} \tag{7.1}$$

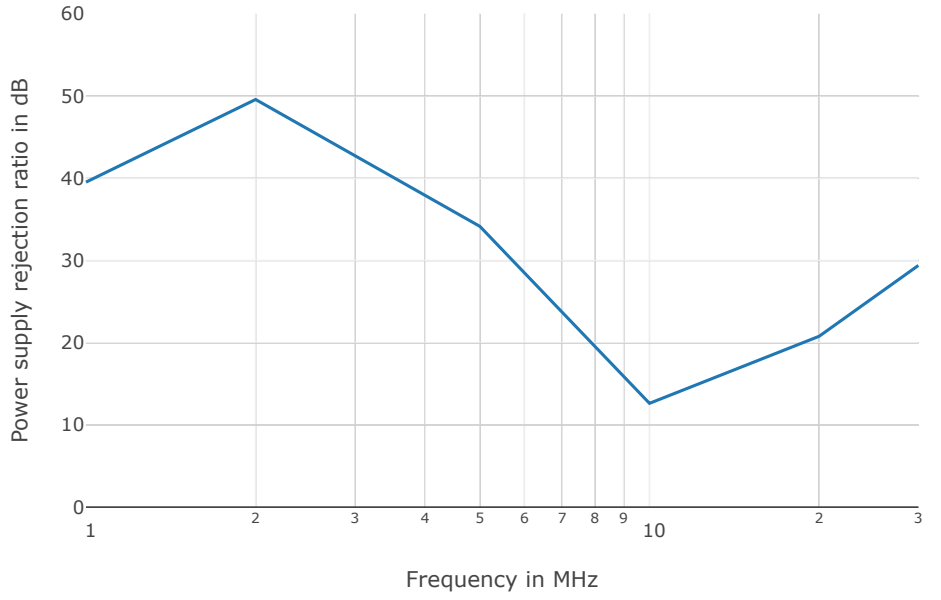

Figure 7.2: Power supply rejection ratio with no additional load

The PSRR behaviour seen in Fig. 7.2 does not look very good, but it is very likely that this is the result of the bad performance of the regulator in no-load conditions. The datasheet specifies a minimum load current of 10 mA, so a 300 Ω resistor was added to the output to try to improve the performance. With this additional load, the performance increases significantly (see Fig. 7.3) and as the real application will

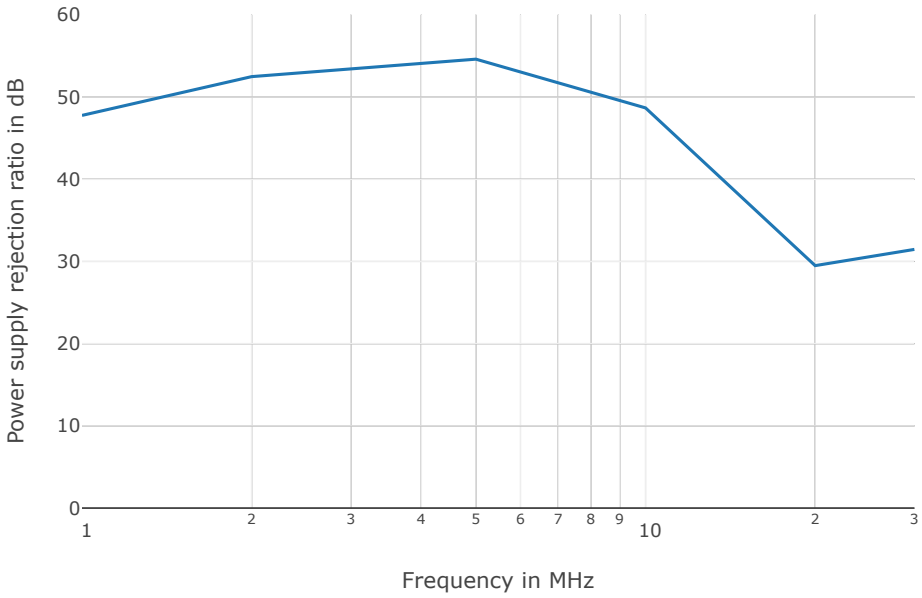

Figure 7.3: Power supply rejection ratio with 300Ω additional load

always load the regulators more than 10 mA, this is accepted as it has not shown to be a problem.

7.1.2 Preamplifier

One of the most important blocks on this demonstrator is the VGA IC. To ensure the functionality of the amplifier, a measurement of the gain with varying control voltage VDBS was done. The output-magnitude-control voltage VMAG was fixed to 0.5 V.

VDBS in V	Vin in mVpp	Vout in Vpp	Gain
1.552	132	0.09	0.68
1.400	133	0.13	0.98
1.300	133	0.19	1.43
1.200	136	0.30	2.21
1.100	140	0.44	3.14
1.000	139	0.66	4.75
0.900	139	0.97	6.98
0.800	142	1.39	9.79
0.700	141	2.00	14.18
0.600	27	0.55	20.37
0.500	27	0.74	27.41
0.400	26	1.03	39.62
0.300	25	1.52	60.80
0.200	29	2.14	73.79

Table 7.2: Measurement results of the gain versus control voltage VDBS

The input voltage has to be decreased for higher gains, or else the output starts clipping.

Fig. 7.4 shows the gain of the variable gain amplifier. In the datasheet of the AD8330 [5] IC it can be seen that this corresponds to the upper end of the gain

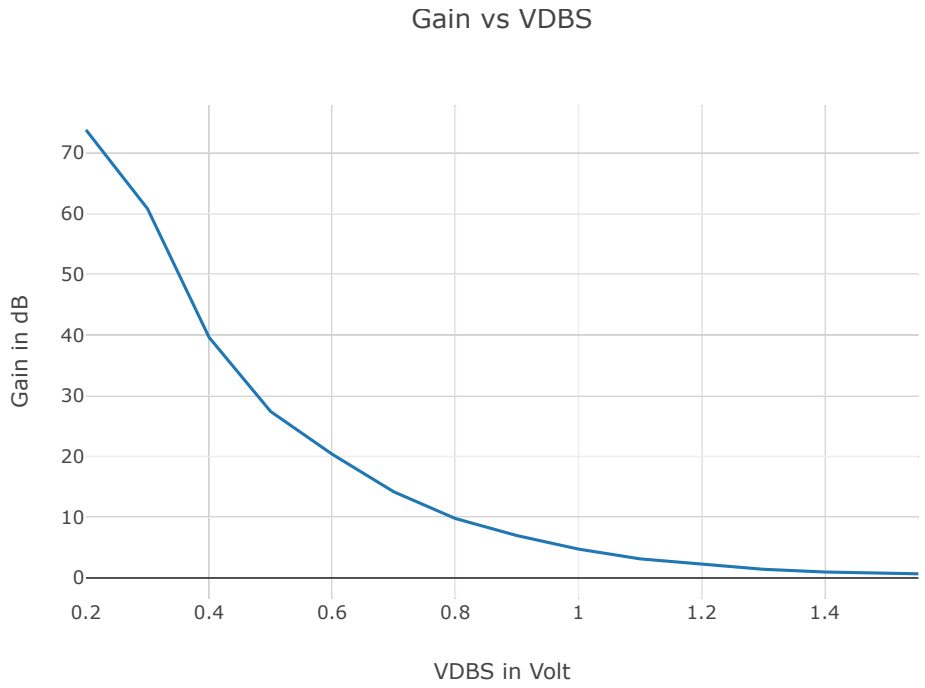

Figure 7.4: Gain versus VDBS voltage

range, where the gain is not a linear-in-dB function of the control voltage, this is only valid for lower gain settings. For this demonstrator the linear interface is not needed because the gain is set only one time initially and then stays at the same level.

7.1.3 ASK Demodulation

The ASK demodulation circuit has been verified with a 20 MHz carrier in "burst" mode with a burst pulse width of 1us, which is equal to an 100 % ASK (On-Off Keying).

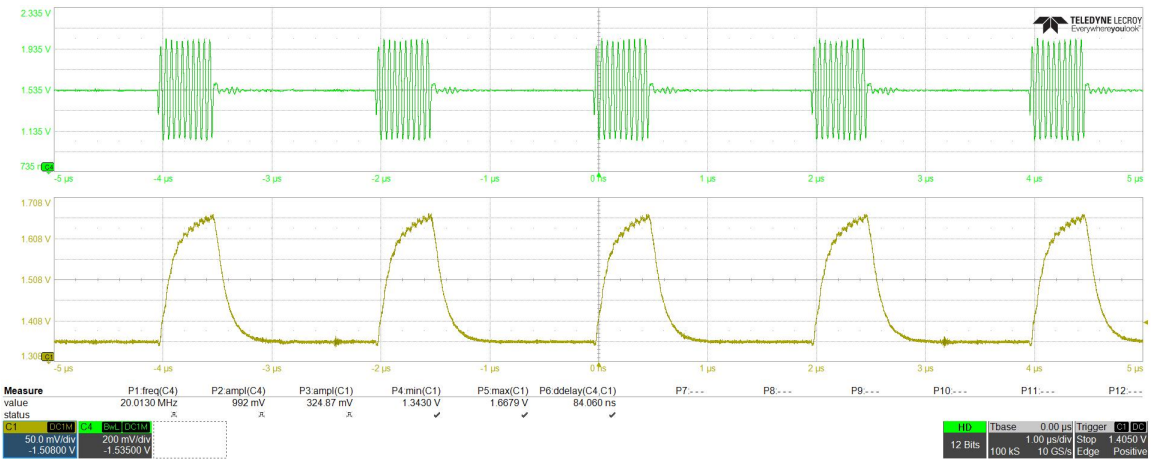

Figure 7.5: Demodulation of a 1Vpp carrier signal

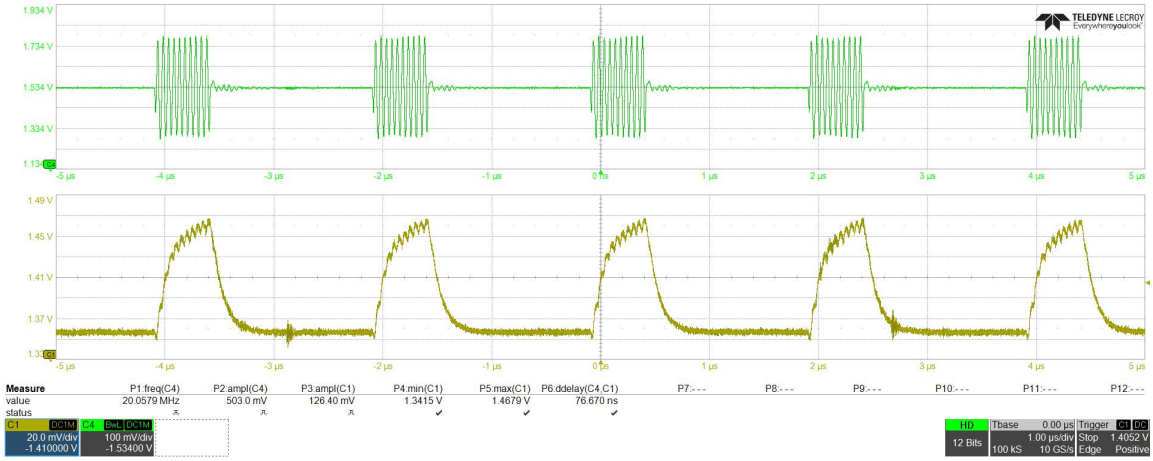

Figure 7.6: Demodulation of a 500mVpp carrier signal

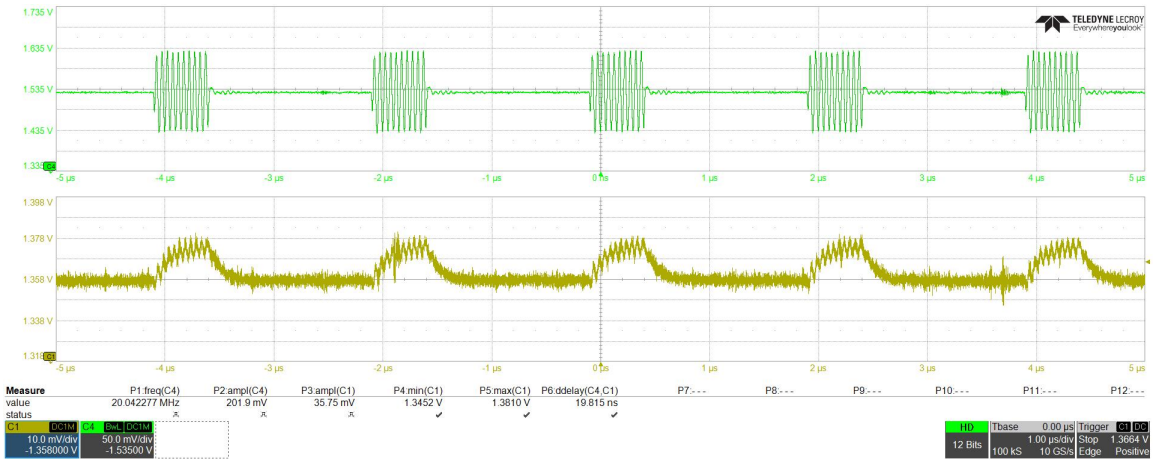

Figure 7.7: Demodulation of a 200mVpp carrier signal

From the signals seen in Fig. 7.5 to Fig. 7.7, it can be said that higher input amplitudes for the demodulation circuit are better, as the rejection of the carrier frequency is better than for lower input amplitudes. As a rule of thumb, it can be said that the input voltage to the diode detector should preferably be greater than 1 Vpp, but at least 500 mVpp to achieve good performance. On the other hand, clipping on the output of the preamplifier should also be avoided, as this will produce harmonics which might degrade the performance.

7.1.4 Oscillator

Hartley oscillator

Fig. 7.8 shows the output of the oscillator with the calculated values for a tank circuit with 900 nH and a capacitance of 68 pF. The resulting oscillation frequency was 21.59 MHz.
The spectrum of the generated sine wave shows a significant amount of harmonics on the signal, which can be improved by adding filters to the buffers at the oscillator output. Note: The spectrum analyzer function of the scope calculates the dBm values for 50 Ω inputs, therefore the absolute values are not correct, but the differences between the peaks are. The -17.83 dB difference between the fundamental and first

harmonic shows that the sine wave is not very pure. After some added filtering, the behaviour was decided to be good enough for the ASK modulation, however for other modulation variants, this might not be sufficient.

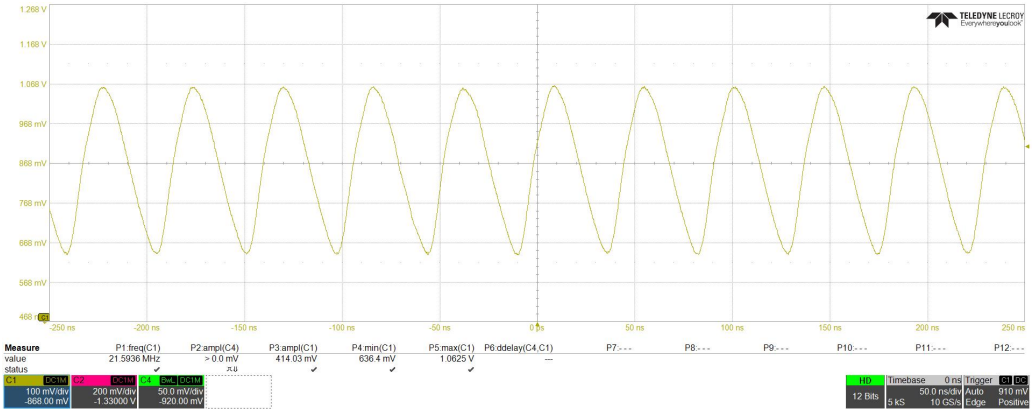

Figure 7.8: Buffered output of the oscillator

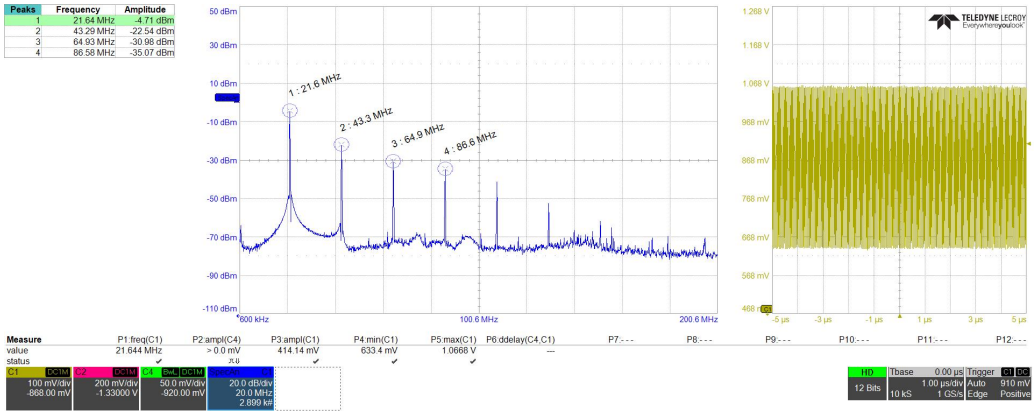

Figure 7.9: Spectrum of the oscillator signal

To improve the frequency accuracy of the oscillator, the parameters of the "tank" components were checked.
By measuring the real tank inductance with an LCR meter, it appears the influence of the PCB increases the total inductance to approximately 1.1 uH, which was corrected by decreasing the capacitance to 54 pF. The resulting oscillation frequency was 20.4 MHz and decided to be "good enough" for further measurements.

Modulator

The modulation is done by using an analog switch for On-Off-Keying. Fig. 7.10 shows the output of the switch with a digital control signal with 300 ns pulse-width. The ringing after switch-off should be filtered by the following amplifier to reduce harmonics, but otherwise the modulator should work for bitrates beyond 3 Mbit/s, which is more than needed for this demonstrator.

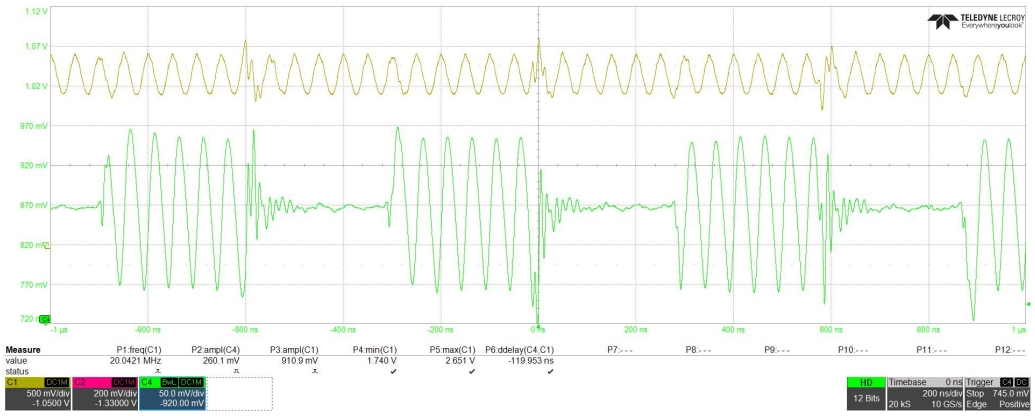

Figure 7.10: Test of the analog switch with a pulse width of 300ns

7.1.5 Power Amplifier

As the power amplifier seems to be working quite well, no extensive measurements have been done on this block, only the functionality of the AD8132[3] IC has been verified by measuring the output and input signals for a standard communication frame. Fig. 7.11 shows the behaviour of the amplifier for an ASK modulated input signal in blue and the differential output voltage in red. The input voltage has an amplitude of 200 mVpp, while the differential output shows approximately 250 mVpp. This measurement has been done with an 18650 cell as a load to show the functionality in a real world scenario.

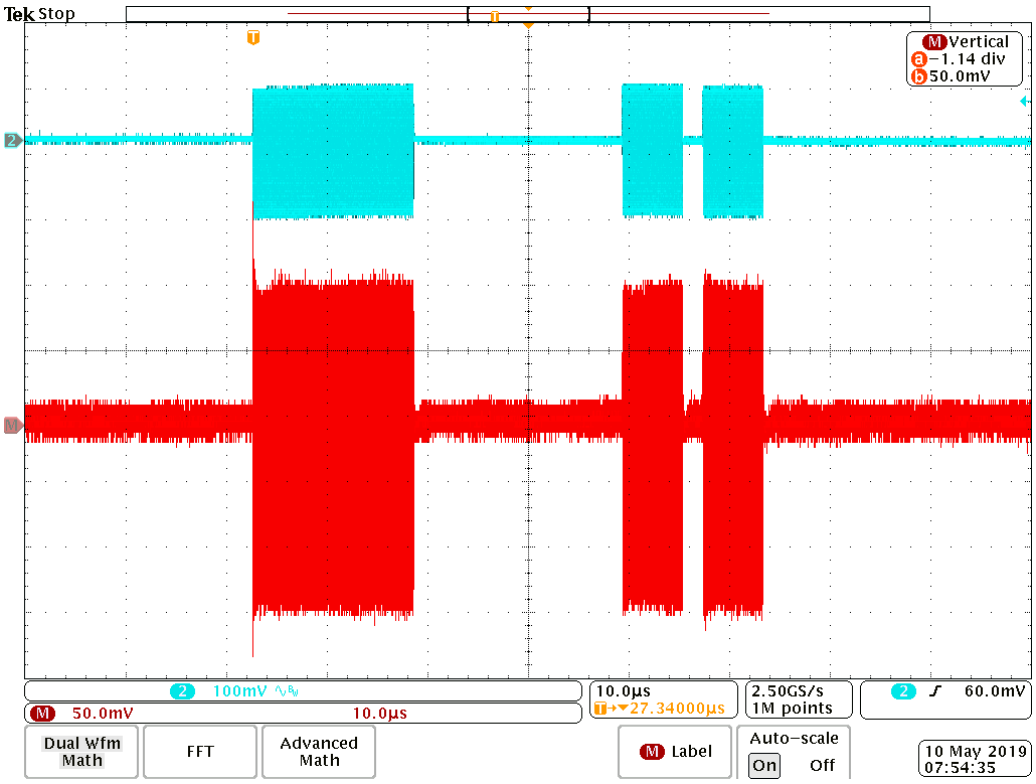

Figure 7.11: Amplification of a standard data frame with an 18650 cell as load

7.1.6 Load Modulation

An alternative approach instead of using a push-pull amplifier to drive the communication current into the cell and stack, is to simply switch a load on the cell with a transistor. The control signal should be off for zero (no communication), and a clock signal with the carrier frequency otherwise.

It should be noted, that this is probably the easiest way to inject a high-frequency signal into the battery stack, however due to the harmonics of the switching signal, the electromagnetic emissions at multiples of the switching frequency would be very high.

The load modulation is done by switching a 20 Ω resistor load with a MOSFET (DMN100). The FET is driven by a 19.1 MHz clock signal from the microcontroller, which is gated by the UART data. When the gate voltage was provided directly from the microcontroller over the long connection across the board, it was obvious that the microcontroller pin could not drive the gate fast enough to switch the FET completely on and off. To improve this, a buffer was placed right next to the FET (74AHC1G125D).

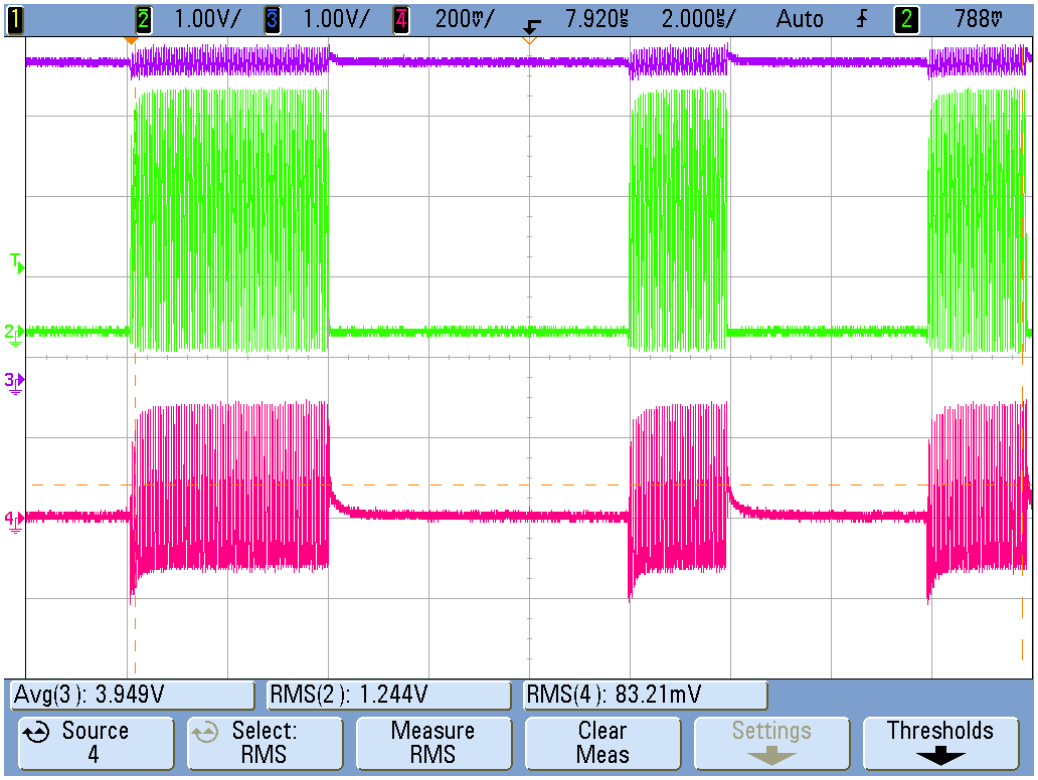

Figure 7.12: Load modulation transmission

Fig. 7.12 shows the DC cell voltage (channel 3, Measured: $V_{cell,dc} = 3.949V$), the AC coupled cell voltage (channel 4) and the voltage drop over the load modulation resistor (channel 2). To improve the accuracy for the AC measurements, Fig. 7.13 shows a zoomed version of the signals (Channel 3 has been replaced by the gate control voltage for the MOSFET). It is necessary to do this, because the used oscilloscope does reduce the horizontal sample resolution due to the limited memory when a wider horizontal range is used.

Figure 7.13: Zoomed into the switching signals

The measured voltage over the load resistor in Fig. 7.13 shows a current flowing through the load of:

$$I_{cell,rms} = \frac{V_{rload,rms}}{R_{load}} = \frac{1.654\,\mathrm{V}}{20\,\Omega} = 82.7\,\mathrm{mA} \tag{7.2}$$

It is assumed that the load is purely resistive.
This means the average load on the cell during the switching activity is 82.7 mA, with $P = I^2 \cdot R$, the power dissipated by the resistor is:

$$P_R = I^2_{cell,rms} \cdot R_{load} = (82.7\,\mathrm{mA})^2 \cdot 20\,\Omega = 136.9\,\mathrm{mW} \tag{7.3}$$

Additionally it can be said by looking at the shape of the current (CH2, Fig. 7.13), that the gate of the transistor is not charged and discharged fast enough to reach a settled state before the control signal changes its state again. There are some ways that this can be improved:

- A stronger gate driver
- A stronger gate driver with additional overdriving (higher voltages to speed up the charging time of the gate capacitance)
- A MOSFET with a smaller gate capacitance (probably resulting in a higher $R_{ds,on}$)

In choosing the third option, the DMN100 MOSFET was changed to a BSS138N which has a substantially smaller gate capacitance (BSS138N: typ. 32 pF vs. DMN100: typ. 150 pF), with the tradeoff of a higher $R_{ds,on}$.

The improvement can be seen by looking at the output voltage of the buffer, which drives the gate of the transistor. Fig. 7.14 shows that with the higher capacitive load, the buffer is not strong enough to drive the gate voltage to the supply voltage or to ground. By exchanging the transistor, this behaviour is improved significantly (see Fig. 7.15).

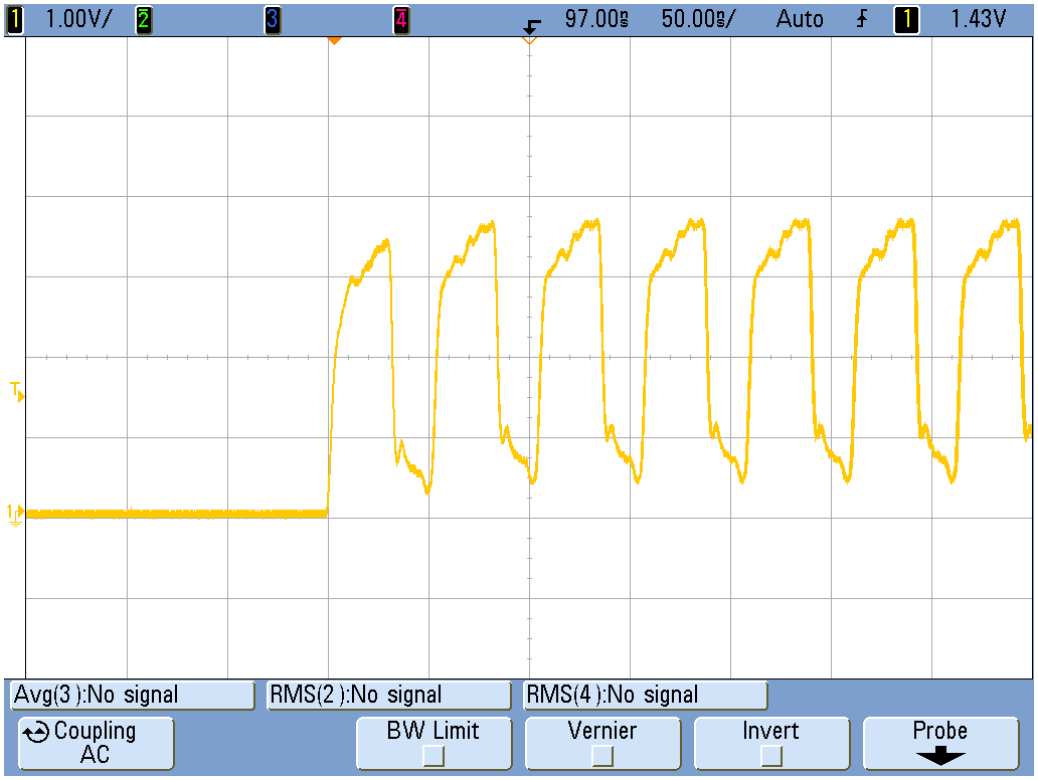

Figure 7.14: Output voltage of the gate driving buffer with a DMN100 transistor

Finally, the cell current in Fig. 7.16 shows a semi-rectangular shape (with some additional ringing due to the parasitic inductances and capacitances).

When using load modulation, it has to be taken into account that only a part of the energy converted from DC to AC is sent out at the carrier frequency, the rest is sent out at harmonic multiples of the fundamental frequency, which could be problematic regarding electromagnetic emission.

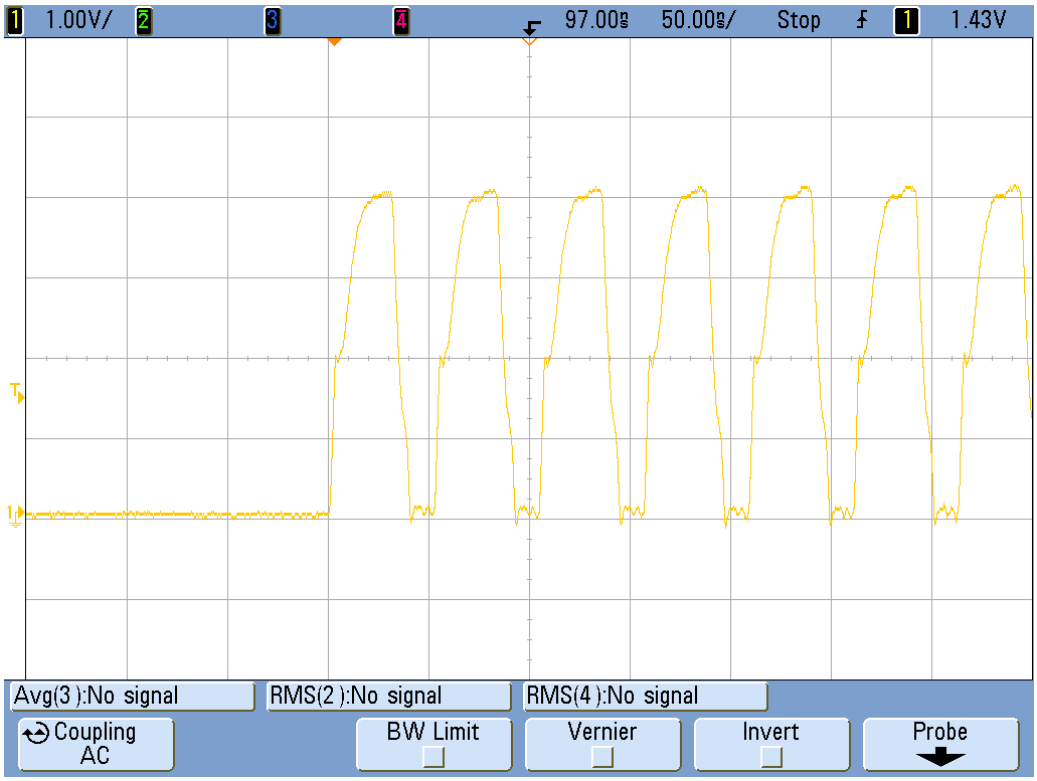

Figure 7.15: Output voltage of the gate driving buffer with a BSS138P transistor

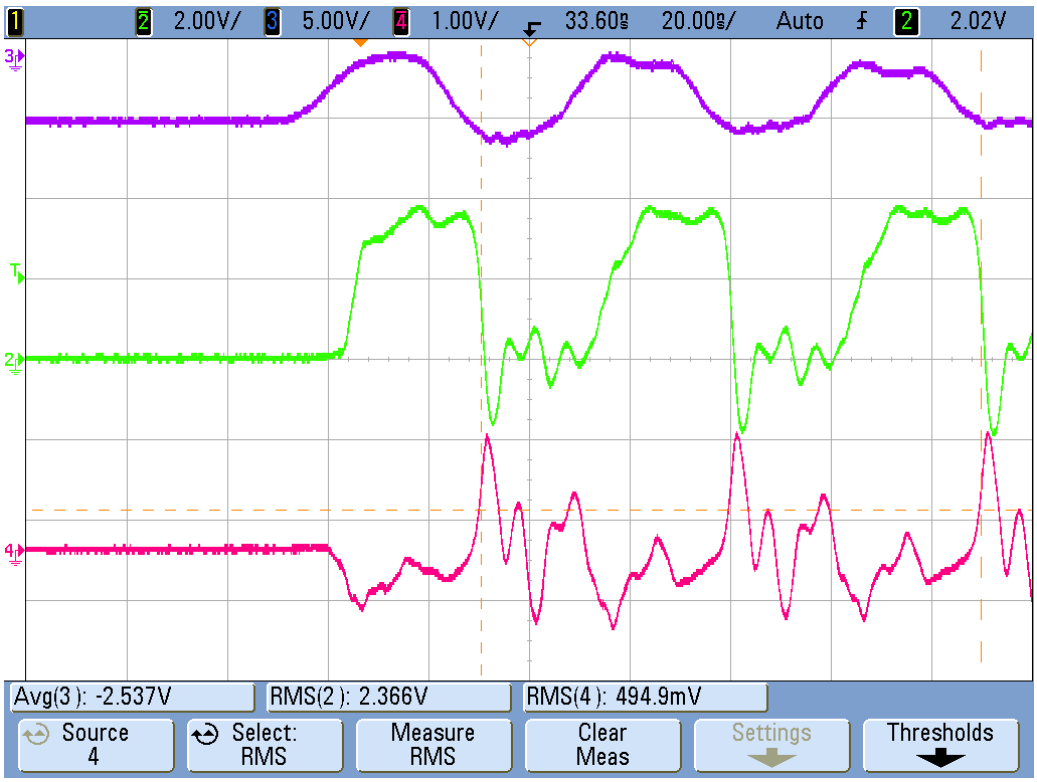

Figure 7.16: Replacing the load modulation transistor with a lower input capacitance transistor

7.1.7 Microcontroller

To show that the microcontroller is working as expected, various functionality tests are performed.

UART Communication

The most important feature is the UART interface of the microcontroller, which is used on the power-line. For the master, it is useful to have an USB-to-PLC bridge, where the data that is transmitted and received can be directly controlled and accessed from a host pc. The XMC board offers a virtual com-port for the debugging interface, which is connected to a communication block in the microcontroller and also the power-line TX and RX pins are connected to a UART interface. Although the demodulated signals could be just inverted and directly fed to the virtual COM UART pins, it is better to use the UART blocks in the microcontroller, as frame timings, filters, etc. can be controlled easily. In Fig. 7.17, a translation from USB-UART (light blue) to the PLC-UART (dark blue) can be seen. The UART data gets inverted, because the modulator takes a logical "high" to switch the sine on and a "low" to disable it, which is why it should be "low" when inactive, so that no signals are transmitted.

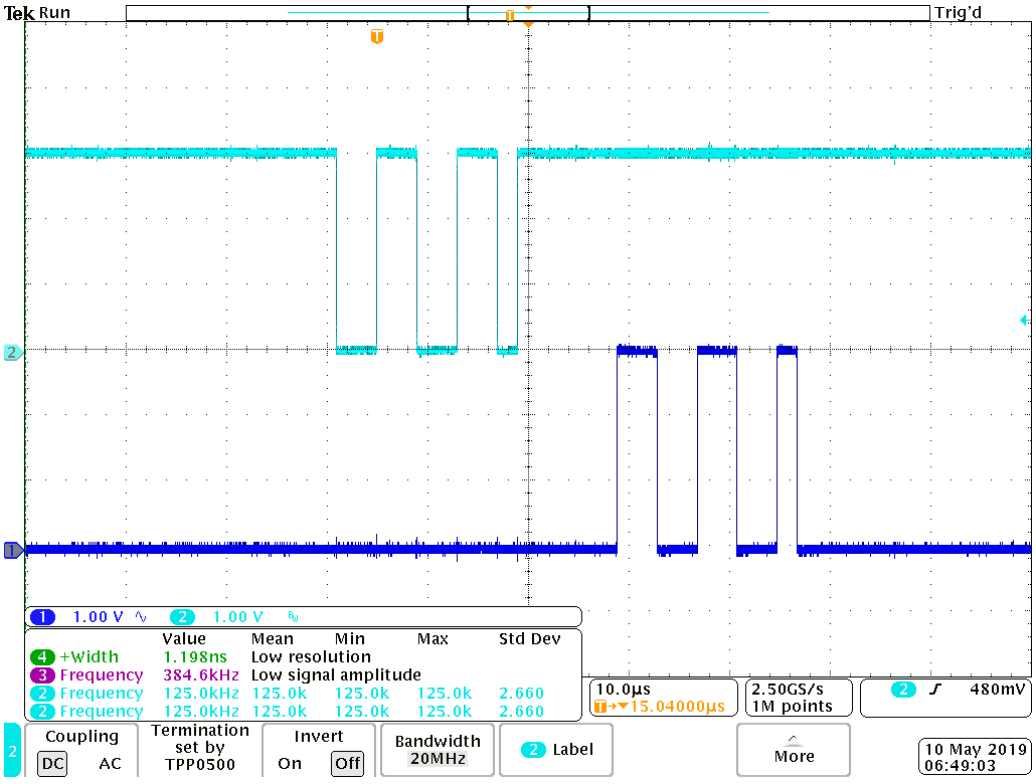

Figure 7.17: Translation of UART data from a host pc to the power-line interface

Cell Voltage Measurement

The voltage of the battery cell (or supply) is measured over a resistive divider of 43 kΩ and 100 kΩ, which gives a ratio of 0.6993 to the internal reference of 5 V.
For a cell voltage of 4.190 V (measured with a calibrated digital multimeter), the measurement of the ADC shows a voltage of 4.17 V (after calculating back from the

reference). Also there is quite some noise on the measurement data, with varying results of up to +-10 mV. For this demonstrator the accuracy of the cell voltage measurement is not really relevant, so this behaviour is accepted.

Miscellaneous

Additionally, the following non-critical functions have been tested successfully:

- Master / Slave selection via jumper
- Buttons for user control
- I2C display with an SSD1306 controller

7.2 System Verification

After the verification of the single blocks, the whole system is tested.

7.2.1 Self-Demodulation

To verify the functionality of the overall-system, the first test is the demodulation of the own generated signal. This can be checked by simply generating a signal on the TX pin at the microcontroller. The generated signal switches the oscillator on (High) and off (Low), which results in the On-Off-Keying modulated signal that is amplified and driving the cell. Then, the signal at the cell is amplified (the gain has to be adjusted so that the demodulator can work properly, 1Vpp should be sufficient), then demodulated and converted to a digital signal by the comparator. For this test, the comparator reference voltage should be set approximately in the middle between the minimum and maximum voltage at the output of the demodulator. As the needed gain to demodulate this signal is very small compared to a real application, noise on the power line plays nearly no role.

See Fig. 7.18 for the demodulation of the self-generated signal. The blue curve shows the input for the cell driving amplifier, purple the output of the diode detector and green the digital comparator signal. The variable gain amplifier is not shown because its signal shape is essentially equal to the blue signal and its amplitude can be adjusted anyway.

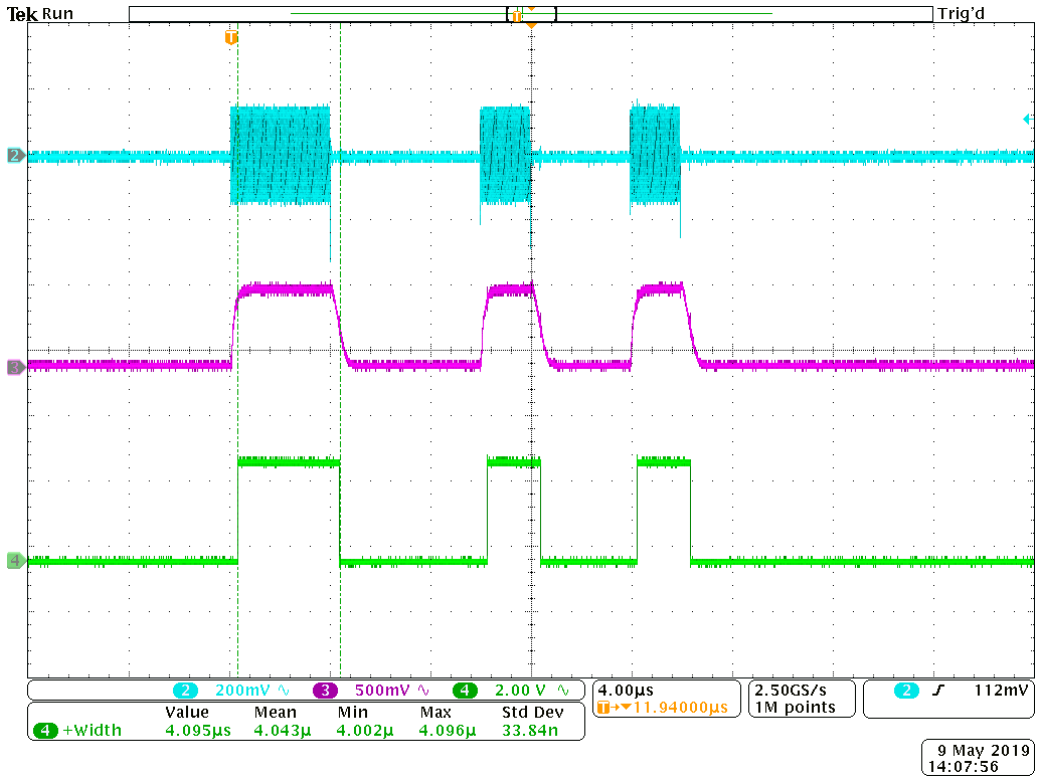

Figure 7.18: Comparison of sent out signal, demodulation and conversion to the digital domain

Fig. 7.18 shows the transmission of the ASCII character "v" (0x76), the frame format is:

- 500 kBaud
- 1 Startbit
- 8 bit payload
- 2 Stopbits

The demodulation works very well under this conditions, because of the high signal to noise ratio due to small gains and low attenuation from transmitter to receiver.

7.2.2 Bi-Directional Communication over a 6 Cell Battery Stack

After the successful start-up of the first PCB, the first test of a real communication over a small battery stack was prepared.

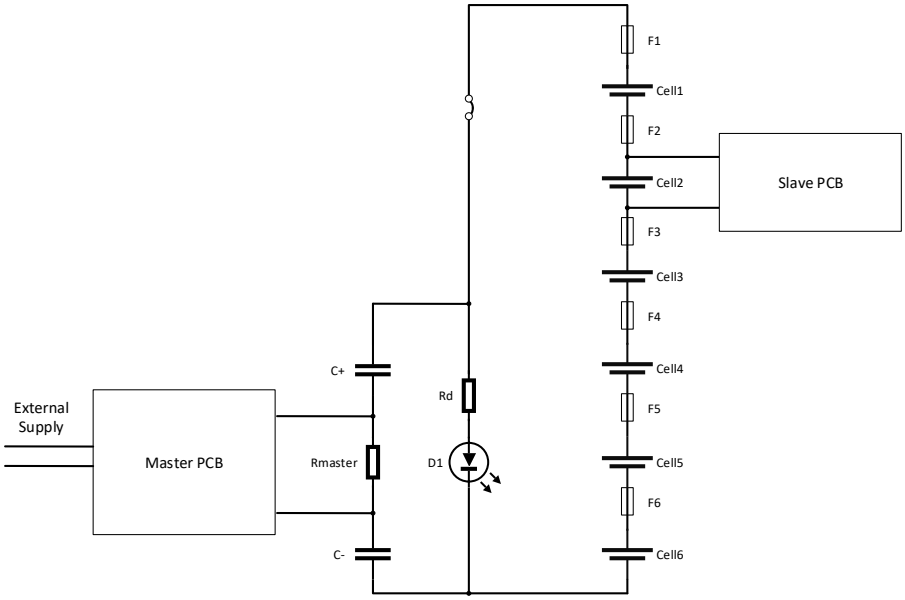

Figure 7.19: Schematic of a small stack with one master and one slave

The stack contains six 18650 Li-ion cells, a master which is connected to a detection resistor of 51 Ω and two DC blocking capacitors, which close the AC current loop. The single slave PCB is placed directly on top of the cell and connected with thin metal plates that fit between the battery holder and the cell poles.

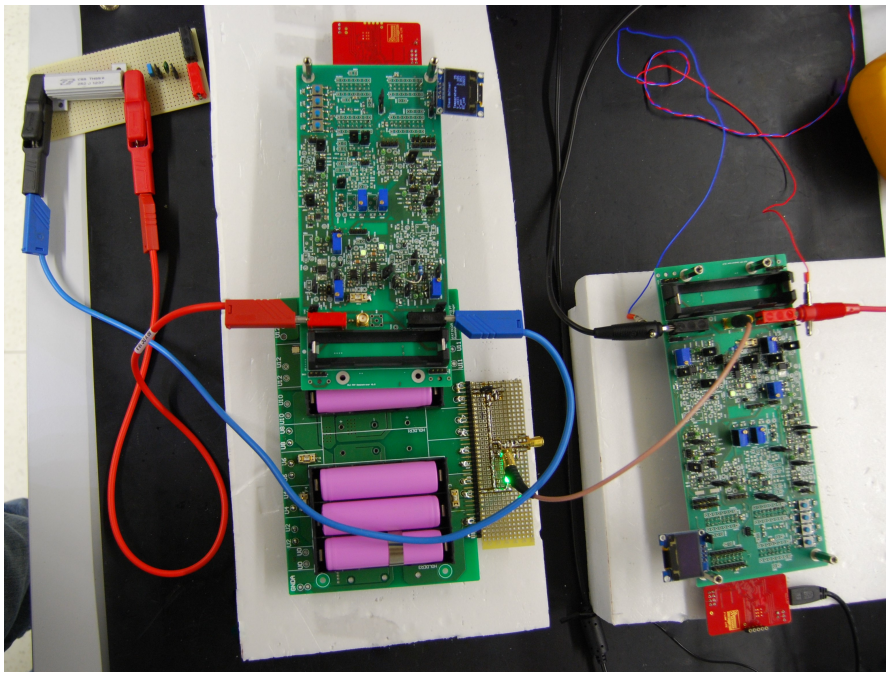

Figure 7.20: A simple setup with the master outside the 6-cell stack and a single slave

For this setup, the signal amplitudes were measured with a spectrum analyzer.

Name	Value	Unit
V_{tx}	12.4	mVrms
V_{rx}	2.8	mVrms
L	-14.8	dB

Table 7.3: Measured values for a transmission from master to slave

Name	Value	Unit
V_{tx}	59.9	mVrms
V_{rx}	20.5	mVrms
L	-9.3	dB

Table 7.4: Measured values for a transmission from slave to master

From this measurement it can be seen, that there is capacitive coupling in between the battery cells. By simple calculation, the damping from master to slave should be 1/6th of the transmitted voltage, or -15.5 dB. As additional losses are also expected, the measured value of -14.8 dB shows that there is additional coupling from the cell to the slave PCB.

Test of packet transmission

In total 1000 packets are requested from the master and the slave responds with 1000 answer packets. If one packet is received wrong, it is counted as an erroneous packet which increases the bit error rate (BER). To show that the communication is working, the potentiometer on the slave is turned and the potentiometer voltage is plotted by the computer that controls the master.

Fig. 7.21 shows that the transmission worked without errors, and the transmission of the potentiometer voltage shows the trend of multiple turns on the potentiometer over the duration of 80 seconds.

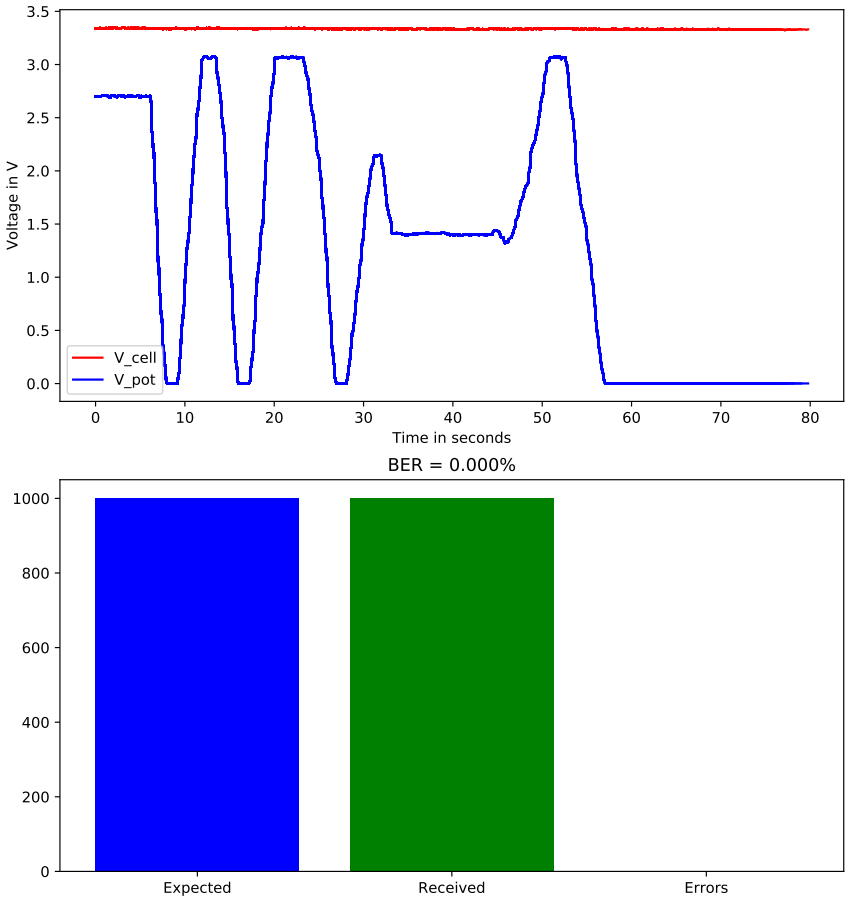

Figure 7.21: Read out slave data at the master: Cell and potentiometer voltage, Packet count and BER

8 Conclusion

8.1 General

In this thesis, possible approaches for bringing power-line communication into an automotive battery stack and the requirements regarding electromagnetic susceptibility were investigated. A demonstrator for experiments on a small-scale lithium-ion battery pack was designed, built and it has been proven that a power-line communication in small packs is possible. However, the high noise levels and required communication robustness call for better modulation methods, as well as forward-error correction and redundancy. On the other hand, this increased complexity reduces the benefits of saving wiring and isolation significantly by the need for additional hardware, extensive characterization and rigorous testing.

8.2 Improvements

The next steps to further advance in the field of PLC in battery stacks would be to develop a robust communication system that can withstand excessive noise from DC/AC and DC/DC converters, as well as the EMC testing. A possible approach could be the implementation of a software-defined-radio (SDR) on an FPGA with a complex modulation format like OFDM with forward error correction and improved addressing. Alternatively, already existing Homeplug GreenPHY chips could be used to setup such a system, but additional effort would be needed to imprint the signals into the cells. A compromise would be the grouping of cells into modules, which reduces the complexity of amplification and also needed data-rate due to decreasing overhead.
The most important step however, would be the testing of such a system in a real car while driving, standing and even charging to prove that a PLC communication can be a true alternative to the conventional wiring.

Glossary

AC Alternating Current
ADC Analog digital converter
AGC Automatic gain control
AM Amplitude modulation
ASK Amplitude shift keying
BCI Bulk current injection
BER Bit error rate
BEV Battery electric vehicle
BMS Battery management systems
BMU Battery management unit
COM Serial communication port
CRC Cyclic redundancy check
CSC Cell sensor circuit
DC Direct Current
EMC Electromagnetic compatibility
EV Electric vehicle
FET Field effect transistor
FM Frequency modulation
FPGA Field programmable gate array, a programmable logic device
FSK Frequency shift keying
I2C Inter-integrated circuit, serial bus for communication between integrated circuits
IC Integrated circuit
LED Light emitting diode
LiIon Lithium-Ion, a battery cell chemistry
MOSFET Metal oxide semiconductor field effect transistor
OFDM Orthogonal frequency division multiplex
OOK On-Off keying
PC Personal computer
PCB Printed circuit board
PHY Physical Layer
PLC Power Line Communication, Transmission of data over the power supply lines
PLL Phase-locked loop
PSK Phase shift keying
PWM Pulse width modulation
QPSK Quadrature phase shift keying
RF Radio frequency
SDR Software defined radio
SOC State of charge

SOH State of health

SPI Serial peripheral interface

STA A station in the communication network

UART Universal asynchronous receiver transmitter, hardware for asynchronous communication between electronic devices

USB Universal serial bus

VCO Voltage controlled oscillator

VGA Variable gain amplifier

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[23] A. M. Tonello and A. Pittolo. “Considerations on narrowband and broadband power line communication for smart grids.” In: *Proc. IEEE Int. Conf. Smart Grid Communications (SmartGridComm).* Nov. 2015, pp. 13–18. DOI: `10.1109/SmartGridComm.2015.7436269`.

Appendix A

Introduction to Homeplug GreenPHY

Homeplug GreenPHY is a standard for power-line communication that was developed by the HomePlug Powerline Alliance, mainly for smart grid applications while remaining compatibility to Homeplug AV and IEEE 1901. The main trade-off that was made in GreenPHY is the reduction of data rates to increase robustness and the complexity (and therefore cost) of devices.

The most important GreenPHY PHY specifications are[1]:

- Bandwidth: 2-30 MHz
- Modulation: OFDM
- Subcarriers: 1155
- Subcarrier Modulation: QPSK
- Forward error correction: 1/2 rate turbo code
- Data rates: 4, 5 or 10 Mbps depending on repeat coding

Currently GreenPHY is used as communication interface between charging stations and electric vehicles, ISO 151118-3[19] specifies the use of Homeplug GreenPHY as physical layer in charging systems. As it is already used in automotive systems and the data rates are sufficient, it is of particular interest in the focus of this thesis.

I2SE PLC-Stamp-1

The devices used in this test are called PLC-Stamp-1[6] and were developed by the I2SE GmbH.

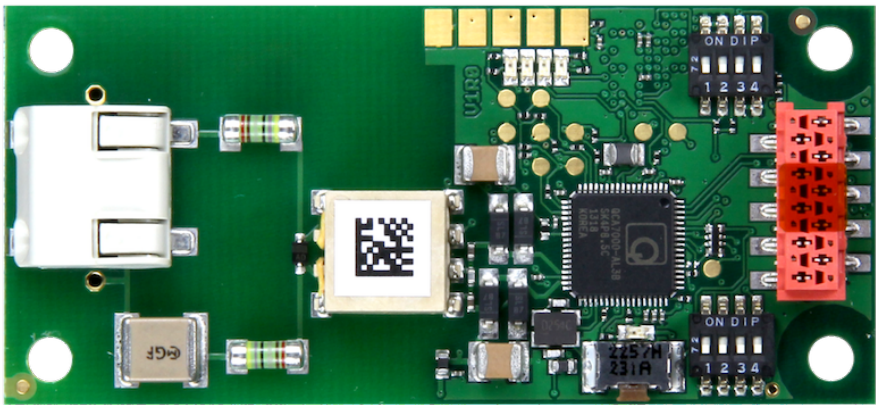

Figure 9.1: I2SE PLC-Stamp-1 ©I2SE GmbH

They provide AC isolation to work with 230 V networks, but can also be used in DC applications. Based on the Qualcomm QCA7000 GreenPHY IC and a dedicated Freescale MK20DX256 microcontroller, they allow the development of stand-alone

devices that can communicate over the DC power-line in traction batteries.

Testing the Modules

Two PLC-Stamp-1 devices are connected directly to each other to test the communication and the "RemoteGPIO" example is flashed.
In figure 9.2 a transmission between two modules is shown. The green signal (channel 2) shows the spi data line on the sending station, the yellow signal (channel 1) shows the power-line signal, where the first block comes from the sender and the second block is sent back from the receiver. The purple signal (channel 4) shows the spi data line on the receiving station.
The signal on the power-line contains two "packets". The first is a request to all listening devices, then after a guard interval a device answers with the requested data. Without demodulating, it cannot be told which packet comes from which device, however the activity on the SPI lines indicates the data direction.

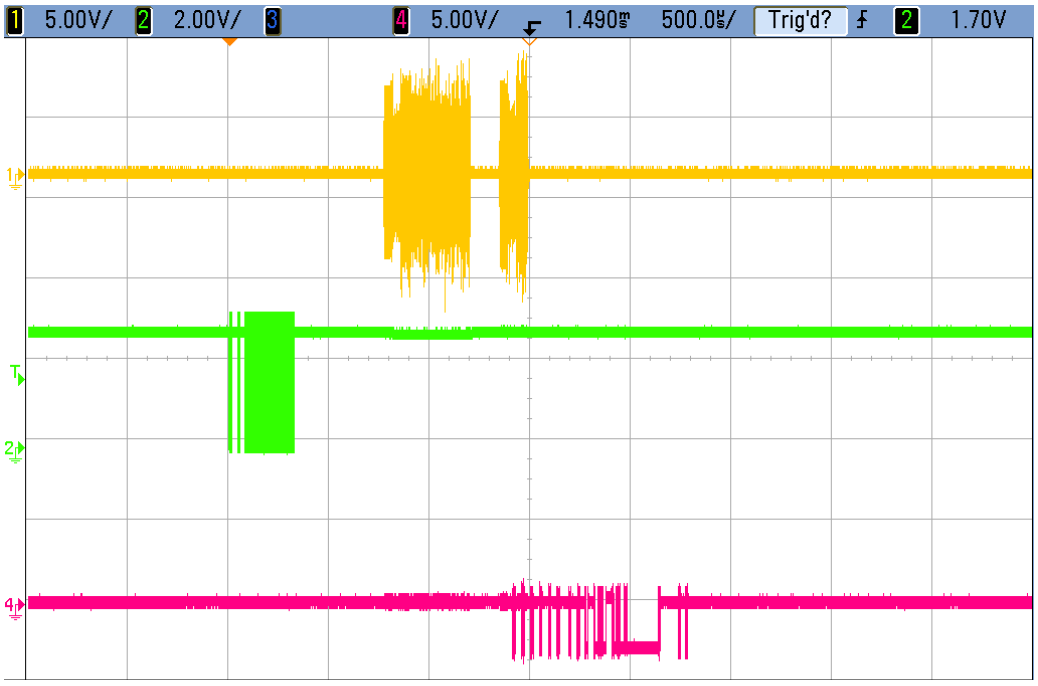

Figure 9.2: A transmission between two GreenPHY stations

Spectrum of the GreenPHY Signal

The averaged spectrum of a GreenPHY communication shows the broad spectrum from 2-28 MHz and the masked bands at various frequencies.

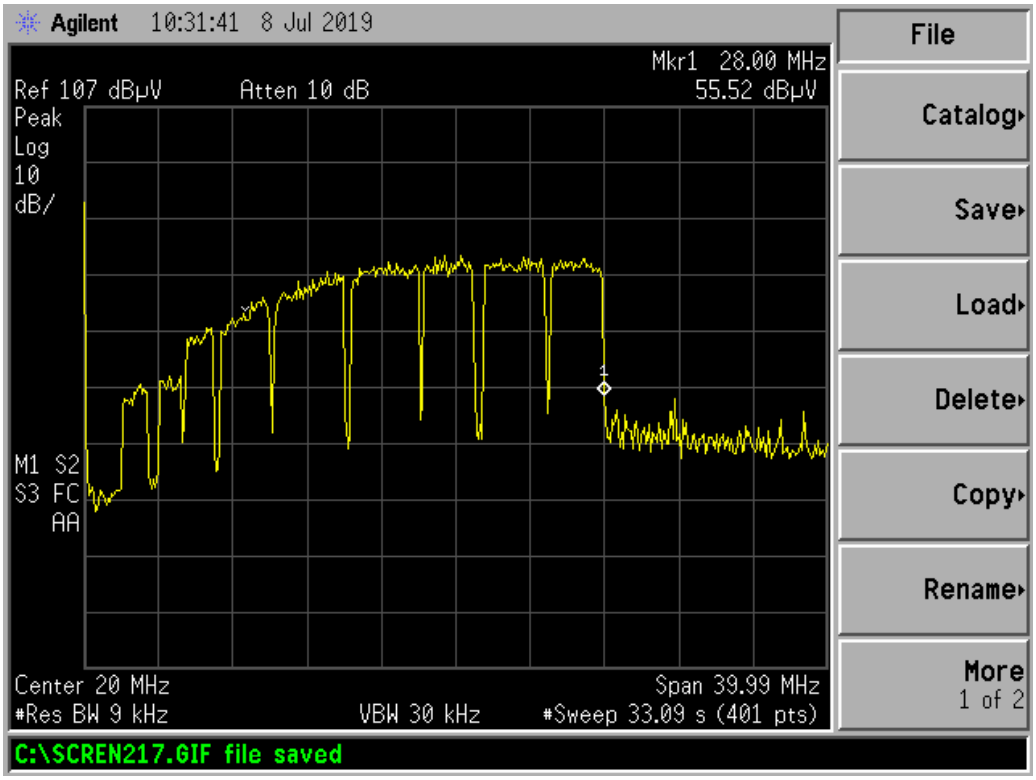

Figure 9.3: The spectrum of a GreenPHY signal

Bringing GreenPHY to the battery

To connect two GreenPHY devices to the battery stack they were modified to be connected directly to the demonstrator PCB. The flashed software is the same "RemoteGPIO" example from above and a signal generator is connected to one of the GPIO pins. The pin-state is monitored from this device and transmitted to the other one. The received signal is shown in Fig. 9.4, which also shows the limits of the simple software. The transmission rate is very slow because the software does not continuously monitor the inputs and uses "Management Message Entries" to communicate. To increase the data rate an Ethernet stack should be implemented and packet-management is needed.

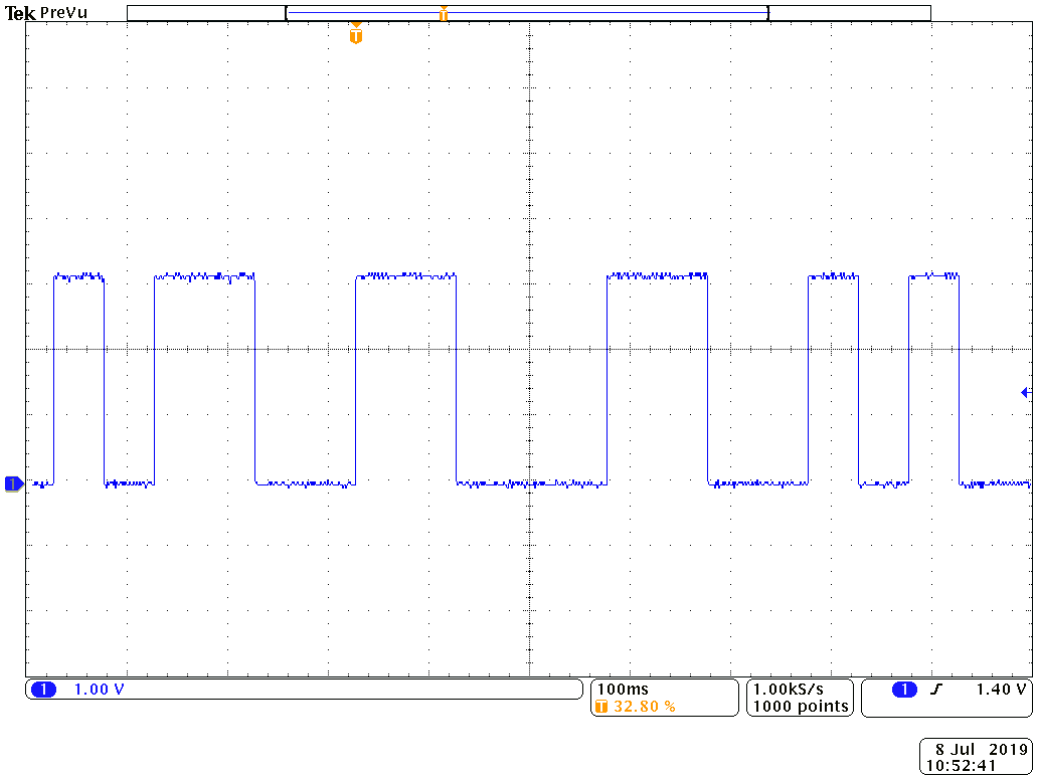

Figure 9.4: Transmitted data over the battery stack