Graz University of Techology

Master Thesis

Optimization of integrated trans-impedance amplifier for high speed and low noise performance

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A thesis submitted in fulfilment of the requirements
for the degree of Master of Science

in the subject of

Electrical Engineering

October 2019

Declaration of Authorship

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"The first principle is that you must not fool yourself and you are the easiest person to fool."

— Richard P. Feynman

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Abstract

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This thesis deals with current to voltage amplifiers, also called transimpedance amplifiers, which feature a high bandwidth, high gain and also extremely low noise. Such amplifiers can be used for characterization of photodiodes, which represent a vital part of today's optical communication systems. On the one hand, a rather simple approach based on inverter based circuits is investigated, on the other hand a more complex circuit called regulated cascode transimpedance amplifier topology is examined. In addition to circuit examples, also noise behaviour of NMOS and PMOS type transistors under different bias conditions is explored. Finally a proof of concept for a fast switching measuring-range extension by a direct modification of the feedback network is shown. With this feature, the amplification of the amplifier can be changed within 5ns, so that the further processing speed of the signal is not affected.

Diese Masterarbeit beschaeftigt sich mit Strom-Spannungs-Verstaerkern, die im Allgemeinen auch als Transimpedanzverstaerker bezeichnet werden. In diesem Zusammenhang werden speziell Verstaerker mit einer grossen Bandbreite, hoher Verstaerkung und sehr niedrigem Rauschen behandelt. Einsatzzweck dieser Verstaerker ist die Verwendung zur Charakterisierung von Photodioden, die heutzutage in der optischen Nachrichtentechnik eine wichtige Rolle spielen. Im Rahmen dieser Arbeit werden sowohl einfache Verstaerker auf Basis von Inverterschaltungen, als auch komplexere Schaltungen, sogenannte Regulated Cascode Transimpedanzverstaerker behandelt.

Zusaetzlich zu den Schaltungen wird auf das Rauschverhalten von NMOS und PMOS Transistoren bei unterschiedlichen Arbeitspunkten eingengangen.

Schlussendlich wird noch ein Nachweis der Machbarkeit fuer eine schnell agierende Messbereichserweiterung durch Veraenderung des Rueckkopplungsnetzwerkes des Transimpedanzverstaerkers durchgefuehrt. Mittels dieser Funktion ist es moeglich, die Verstaerkung des Verstaerkers innerhalb von 5ns zu veraendern, so dass die nachfolgende Auswertung des Ausgangssignals nicht beeintraechtigt wird.

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Abbreviations

TIA	**T**rans**i**mpedance **A**mplifier
FTTH	**F**iber **t**o **t**he **H**ome
FTTD	**F**iber **t**o **t**he **D**esk
MOS	**M**etal-**O**xide-**S**emiconductor
MOSFET	**M**etal-**O**xide-**S**emiconductor **F**ield-**E**ffect **T**ransistor
CMOS	**C**omplementary-**m**etal-**o**xide-**s**emiconductor
IC	**I**ntegrated **C**ircuit
DC	**D**irect **C**urrent
e-h	**e**lectron - **h**ole (pair)
CS	**C**ommon - **S**ource
CG	**C**ommon - **G**ate
MEMS	**M**icroel**e**ctro**m**echanical **S**ystems
SEM	**S**canning **E**lectron **M**icroscopy
AGC	**A**utomatic **G**ain **C**ontrol

Scope

Presented thesis is done with the goal to provide an comprehensive overview over different topologies used for high bandwidth, high gain and low noise transimpedance amplifiers. Main focus is laid on understanding noise behaviour of different circuits. Although the main target of this work are amplifiers for communication applications, proposed circuits can also be used for particle detectors or similar applications.

The first chapter provides a short introduction into the photodiode-amplifier topic. A general overview regarding fiber optics communication is given. The properties of components which directly interact with the transimpedance amplifier, such as photodiode and subsequent toplevel readout circuits are reviewed. This chapter also provides a quick introduction to noise basics and noise behaviour of MOSFET devices.

The second chapter deals with actual topologies for transimpedance amplifiers. The first part is about the behaviour of very basic push-pull inverter based topologies. The most basic one, a single stage push-pull inverter amplifier is used as a reference circuit for all the other designs. In addition to the basic single-stage inverter TIA, a single stage inverter with an added cascode extension is also reviewed. The last part for the inverter based circuit represents a three stage push-pull inverter based transimpedance amplifier. In the second part, two regulated cascode based circuits are investigated. Firstly, a widely spread resistor based version is introduced and secondly a topology which relies on current-mirrors for biasing is introduced.

Chapter 3 especially is about noise behaviour of MOSFET devices. Based on the observations from Chapter 2 the differences between n-channel and p-channel MOSFET, as well as the impact of different bias currents on noise behaviour is discussed.

In Chapter 4 an exceptional approach of a variable gain amplifier is shown. Other than usual transimpedance amplifiers commonly used in actual fibre optic applications the gain is adjusted immediately when the signal approaches the limits of the output swing of the amplifier. Of course, this adjustment has to be done fast, so that the desired evaluation period for subsequent signal processing of 10 ns still holds.

Chapter 5 summarizes all gathered findings and provides a technical discussion. Finally an overview of possible next steps is presented.

Chapter 1

Introduction

As optical transmission systems become more and more popular and technologies like *Fibre to the Home (FTTH)* or even *Fiber to the Desk (FTTD)* are feasible for more and more people, a lot of research has been done to improve the performance and lower the costs of such systems. Remarkable results have been achieved regarding implementation of photodiodes using standard CMOS process nodes and thus lowering the costs drastically. Also the subsequent current to voltage converters/ amplifiers can be designed by using the same CMOS process nodes. As the transmission rates are increasing, faster and more powerful diodes are needed. To characterize the performance of such photodiodes, a photodiode amplifier featuring high gain and bandwidth, as well as low noise is designed in this thesis.

Nevertheless, transimpedance amplifiers are also used in other applications than fiber optics, for instance at particle detectors or in microelectromechanical systems (MEMS). Extremely low noise TIAs are for instance needed at scanning electron microscopes (SEM) as current to voltage converter for their detectors.

1.1 Optical Transmission Systems

A fundamental optical transmission consists of a transmitter-part and a receiver part. A simplified structure diagram of such a system is shown in Figure 1.1. One of the most important parts in such a system is the combination of a photodiode and the

subsequent photodiode amplifier, because it highly influences the performance of the whole transmission.

1.1.1 Photodiodes

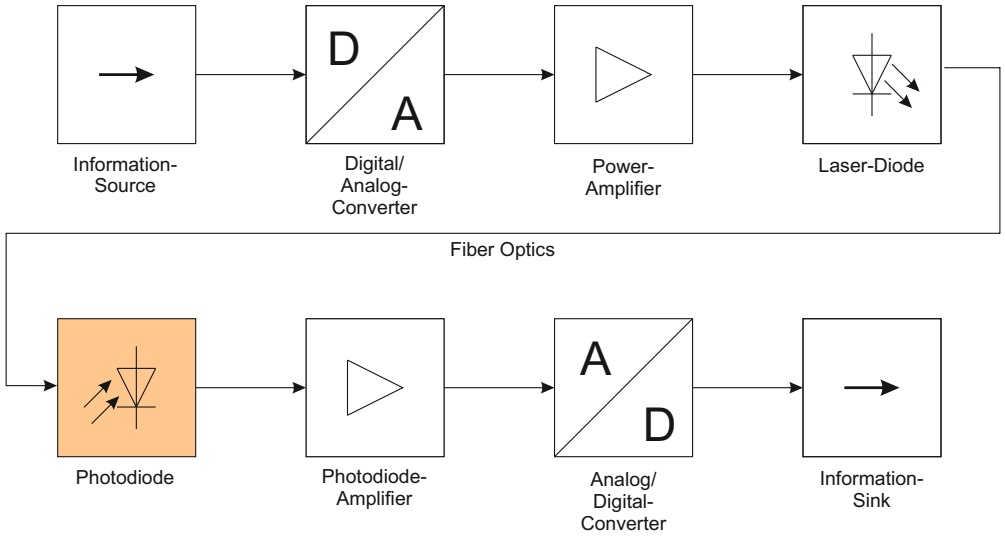

FIGURE 1.1: Structure diagram of an optical transmission system.

Photodiodes are special types of diodes, which are capable of converting impinging photons to electrical currents based on the photovoltaic principle. Photodiodes often consist of a conventional p-n junction and as a consequence thereof a built in electrical field. When photons hit the p-n junction, some electrons get excited and electron-hole pairs (EHP) are generated. Due to the intrinsic electrical field the electron-hole-pairs get separated and induce a current through the terminals. Therefore a photodiode is essentially a current source. Depending on the size of the p-n junction, they are either referred as solar cells, featuring a very big junction area, or smaller devices which are called photodiodes.

For high speed applications so called PIN diodes are used. In contrast to a conventional photodiode, an additional intrinsic semiconductor layer between the p and the n area is used to widen the depletion area thus reducing the capacity and therefore enabling higher frequencies.

To read out the photodiode signal, the generated electron-hole-pairs (EHP) have to be separated by a voltage. In photodiodes the intrinsic field at the space charge region

inside the p-n junction is used. Additionally the electrical field can be increased by applying a reverse bias.

From the semiconductor physics' point of view, photodiodes behave very similar compared to conventional p-n diodes, although the area of the p-n junction in photodiodes, similar to power diodes, is usually designed to be much bigger compared to conventional small-signal diodes. This is to increase the sensitivity of the device.

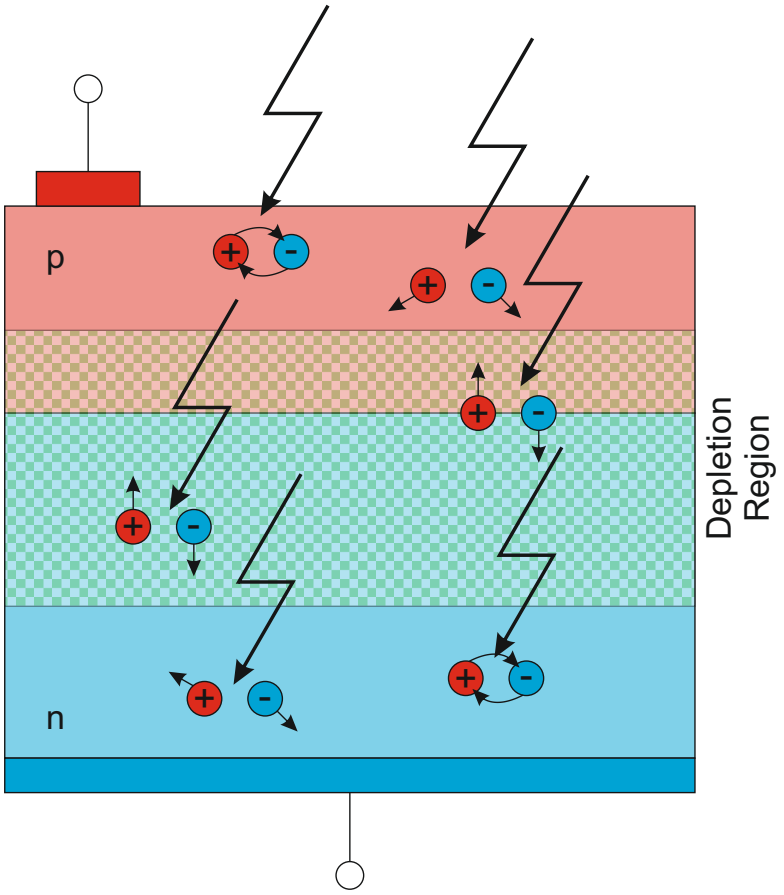

FIGURE 1.2: In a photodiode, photons produce electron-hole pairs. Within the depletion region they get separated and accelerated towards the terminals, whereas the electron-hole pairs occurring outside the depletion region either recombine immediately or travel by diffusion.

1.1.1.1 Biasing Conditions

Photodiodes can be biased in two different regimes. Firstly the photodiode can be operated in forward bias, which is the case for photovoltaic elements. In forward bias the photodiode operates very slowly and therefore this operating regime is not suitable for detecting fast signals, hence it is not further considered in this work.

The second mode of operation is the so-called photoconductive mode, where the diode is either shorted or in reverse bias. The reverse bias leads to an increase of the depletion width and therefore a reduction of the junction capacitance and in addition to an increase of the sensitive volume. Providing reverse bias for the p-n junction also decreases the dark current of the photodiode, whereas the photocurrent stays virtually constant.

If the photodiode is biased in reverse direction, in addition to the electron-hole-pairs generated directly inside the depletion region, also the charge carriers which are generated in the diffusion areas are accelerated towards the p-n junction. Directly at the p-n junction they get sucked off by the intense electrical field and contribute to the reverse current as well. Basically the reverse current i_s is composed of the virtually constant dark current i_0 and an additional photo current i_{ph} as described in Equation (1.1).

$$i_s = i_0 + i_{ph} \tag{1.1}$$

According to literature [1] typical orders of magnitude for the photocurrent are in the region of some tens to hundreds of micro amperes, whereas the dark current is the order of some nano amperes.

1.1.1.2 Equivalent Circuit Diagram

To model behaviour of photodiodes, in this work the equivalent circuit diagram shown in Figure 1.3 is used. The equivalent circuit consists of a current source.

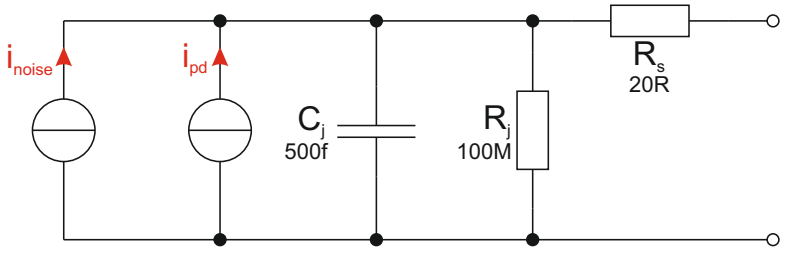

FIGURE 1.3: Equivalent circuit diagram of a photodiode.

In accordance to literature [1] where a high speed photodiode featuring a capacitance of $C_j = 345\,\text{fF}$ using a 180 nm CMOS process is created, the junction capacitance in the model in this work is set to $C_j = 500\,\text{fF}$. The junction resistance is usually very high and therefore modelled by a parallel resistance of $R_j = 100\,\text{M}\Omega$. The noise contribution

of the photodiode is determined by the leakage current i_{leak} and is can be calculated as in Equation (1.2). The so called shot noise of the photodiode is not considered in this thesis.

$$i_{noise} = 2i_{leak}q \tag{1.2}$$

where:

i_{leak}	leakage current
q	charge carrier (electron)

The junction capacitance of a photodiode is proportional to the junction area. Thus big photodiodes feature a high parasitic capacitances which make the photodiode slower. Indeed, a bigger junction area leads to a higher amount of separated electron-hole-pairs and therefore to a higher photodiode current. This leads in turn to a lower necessary gain of the subsequent photodiode amplifier.

1.1.2 Photodiode Amplifiers / Transimpedance Amplifiers

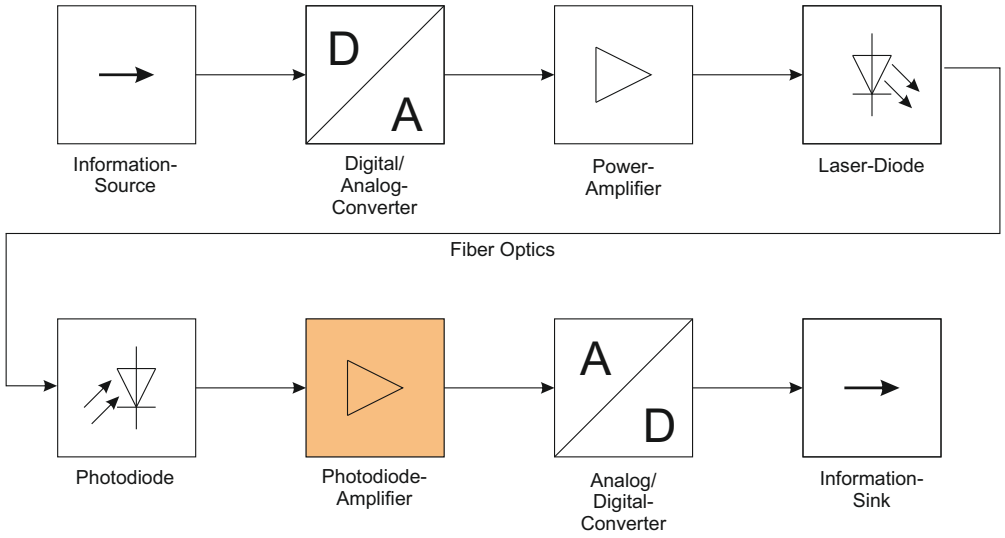

FIGURE 1.4: Structure diagram of an optical transmission system.

Basically transimpedance amplifiers (TIAs) provide a current input and an amplified voltage output. According to Equation (1.3) the relationship between the magnitude of the input signal and the magnitude of the output signal is defined as the transimpedance Z. As the relationship compares a voltage and a current, the unit of the transimpedance

is Ohm [Ω]. Today transimpedance amplifiers play an important role in so-called photodetectors, which are a hybrid component consisting of a photodiode and a subsequent transimpedance amplifier, often located on the same die. Due to the fact that optoelectronics is the main field where transimpedance amplifiers are used, also the term *photodiode* amplifier is used synonymously.

$$Z_{TIA} = \frac{\delta V_{out}}{\delta I_{in}} \ , \qquad dim\left\{Z_{TIA}\right\} = \frac{[V]}{[A]} = [\Omega] \tag{1.3}$$

According to literature [2] transimpedance amplifiers can be either implemented as an open-loop topology, which are e.g. a simple termination resistor, a common-gate TIA or a regulated cascode TIA, or as closed-loop (feedback) topologies namely a common-source amplifier or a CMOS inverter.

According to [3] photodiode amplifiers lead to multidimensional restrictions in the performance of photodiode applications. A well designed photodiode amplifier provides a low-ohmic input, to act as an almost ideal current sink for the photodiode current. The voltage output should also be able to drive the specified load, which is in most cases a combined impedance of resistance and capacitance. The bigger the output capacitor, the lower the output resistance of the amplifier has to be.

1.2 Noise Theory

In electronics, the stochastical and mostly unwanted disturbance of the signal is considered as noise. Every electronic device creates some kind of noise caused by different effects. Noise can mathematically be expressed by random processes. Although the instantaneous amplitude for example cannot be predicted by the help of mathematics, some other properties like the average power for example can. The most common types of noise are thermal noise, shot noise and flicker noise. The different types of noise can usually be distinguished by the shape of their power spectral density.

1.2.1 Noise at Amplifiers

A basic noise model of a photodiode amplifier is shown in Figure 1.5. As noise sources the thermal noise of the feedback resistor, as well as the input current noise and the input voltage noise of the amplifier are shown. The feedback resistor R_F directly contributes to the output noise and its noise contribution v_{nR} is not amplified by the amplifier. The shot noise of the input current is represented by i_{ni}. This shot noise is amplified by the transimpedance Z_T of the amplifier. Similar to the noise of the feedback resistor, the input noise voltage v_{ni} of the amplifier is transferred with unity gain to the output.

As the input signal of a transimpedance amplifier is amplified by the transimpedance gain Z_T, it is obvious, that increasing the transimpedance R_F would lead to an optimized signal-to-noise ratio. On the one hand an increased transimpedance would also increase the contribution of the shot noise at the input, on the other hand increasing transimpedance leads to a reduction of the bandwidth. Therefore a trade-off has to be found.

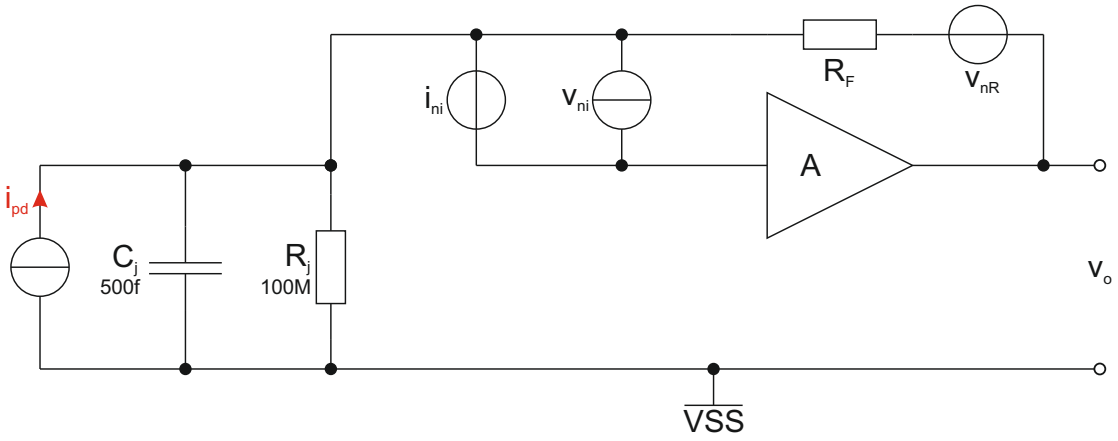

FIGURE 1.5: Noise analysis model of a basic photodiode amplifier.

The noise of the photodiode can be referred to the output by simply multiplying the frequency response of the amplifier to the photodiode noise expression as in Equation (1.4).

$$overline{v_{n_{out}}}^2 = H(j\omega) \cdot i_{n_{in}}^2 \tag{1.4}$$

where:

$v_{n_{out}}^2$	output noise contribution from photodiode
$i_{n_{in}}^2$	input noise from photodiode
$H(j\omega)$	frequency transfer function

1.2.2 Thermal Noise

Thermal noise also often resistor noise is a primarily white noise, which means that the power distribution is constant over the whole range of the frequency spectrum. It is caused by random movement of charge carriers (Equation (1.5)).

$$\overline{u^2} = 4k_B T R \Delta f \tag{1.5}$$

where:

k_B	Boltzmann constant
T	Temperature
R	Ohmic Resistance
Δf	Bandwidth

1.2.3 Shot Noise

Shot noise describes a special type of white noise which can be statistically modelled as a poisson process. The principle of shot noise lies in the corpuscular nature of charge carriers, in semiconductors called electrons and holes. Considering a potential barrier like at a p-n junction, each single charge passes the potential barrier independently of each other, hence the sum of all charge carriers passing the barrier doesn't stay constant over time. The average shot noise current can be written as follows (Equation (1.6)):

$$\overline{i^2} = 2qI\Delta f \frac{1}{1+\omega^2\tau_t^2} \tag{1.6}$$

where:

q	charge carrier
I	Current
Δf	Bandwidth
τ_t	transit (flight) time through the barrier (can be neglected)

1.2.4 Flicker Noise

Flicker Noise features a power spectral density proportional to $\frac{1}{f}$, therefore it is often also called $\frac{1}{f}$-Noise. Generally in MOSFET devices there are traps situated inside the gate oxide. Those traps cause an inhomogenous charge carrier distribution inside the channel and therefore lead to changes of channel resistance. The noise amplitude in dependence of the frequency for MOSFET devices operating in saturation regime is shown in Equation (1.7)

$$S_{I_d(f)} = \frac{(KF)\, I_d}{L^2 C_{ox} f} \tag{1.7}$$

where:

KF	flicker noise coefficient
I_d	drain current
L	channel length
C_{ox}	gate oxide
f	frequency

1/f noise can be reduced by using bigger transistors or by increasing the gate capacitance C_{ox}.

1.2.5 Noise at MOSFET devices

According to [4], the mean-square current-noise of a MOSFET is defined as in expression Equation (1.8).

$$i_n^2 = \left[\frac{8kTg_m\,(1+\eta)}{3} + \frac{(KF)\, I_D}{fC_{ox}L^2}\right]\Delta f \tag{1.8}$$

where:

Δf	bandwidth
η	g_{mbs}/g_m
k	Boltzmann's constant
T	temperature
g_m	small-signal transconductance

The right fraction is equal to the flicker noise expression. The power spectral density of thermal and flicker noise at a MOSFET is shown in Figure 1.6

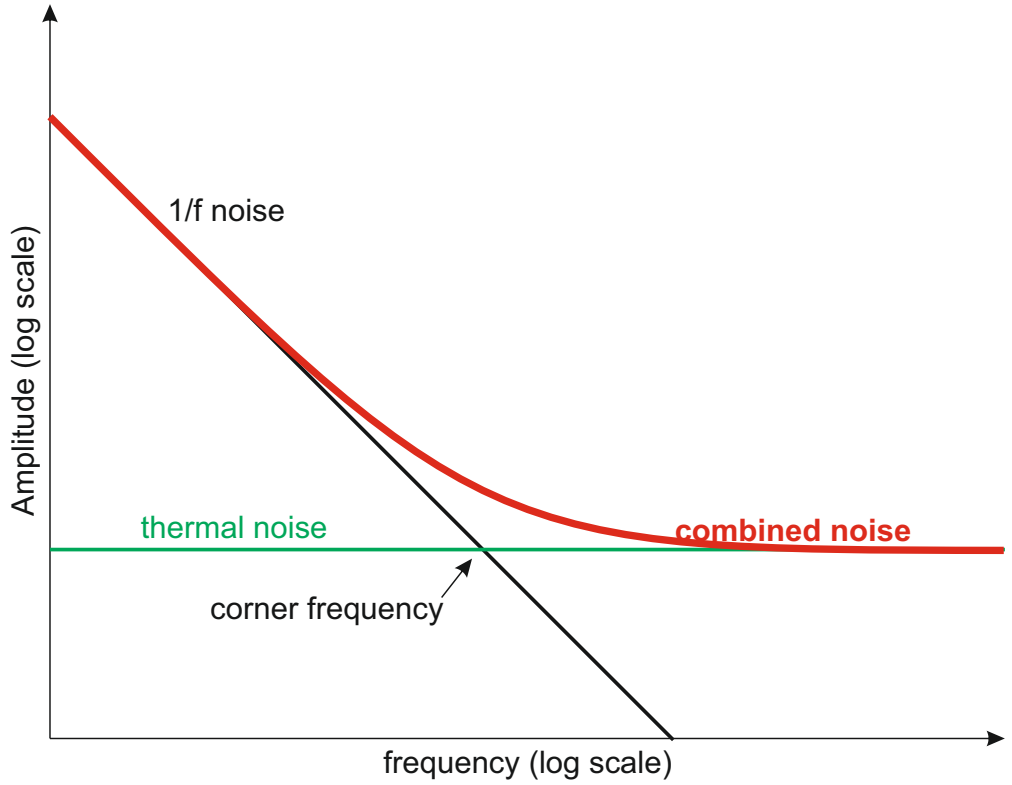

FIGURE 1.6: Power spectral densities of thermal and flicker noise at a MOSFET. The flicker noise dominates the low frequency section whereas the thermal noise dominates at higher frequencies.

1.2.6 Input / Output Referred Noise

Usually noise of an amplifier is measured as a voltage at the output. In addition to the amplified noise level of the input, the noise level at the output consists of the noise by the amplifier itself. If the input signal of the amplifier is considered to be ideal and

without noise, the measured output noise level describes only the noise introduced by the amplifier.

Speaking of *Signal to Noise Ratio (SNR)*, an amplifier with higher gain, producing the same noise level compared to an amplifier with lower gain, is considered to be more low-noise. Thus, noise performance of amplifiers is usually compared by using the input referred noise. Input referred noise is the noise current or voltage that, applied to the input of a noiseless circuit, generates the same output noise as the actual circuit does.

To properly model noise at the input port, two noise sources, a current source and a voltage source have to be considered. With regards to Figure 1.7 it is easy to show, that on the one hand if the source impedance is zero, noise from $\overline{i_{n,in}^2}$ through $\overline{v_{n,in}^2}$is without any effect at the output. The whole noise solely arises from $\overline{v_{n,in}^2}$. On the other hand if an open input is used, $\overline{v_{n,in}^2}$ has no effect on the output noise which is then generated solely by $\overline{i_{n,in}^2}$.

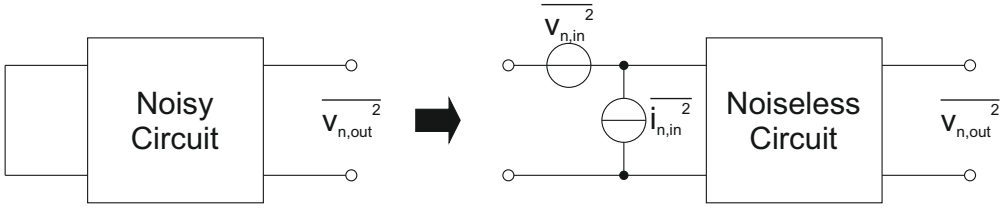

FIGURE 1.7: Conversion between measureable output noise $\overline{v_{n,out}^2}$ and the theoretical, though often used input referred noise sources $\overline{v_{n,in}^2}$ and $\overline{i_{n,in}^2}$.

The input referred noise can also be considered as the output noise divided by the transfer function of the system, or in this case the frequency response of the amplifier.

$$\overline{v_{n,in}^2} = \frac{1}{H(f)}\overline{v_{n,out}^2} \tag{1.9}$$

Therefore, the output noise of a MOSFET can also be referred to the gate by simply dividing Equation (1.8) by g_m^2 which leads to *input referred* noise shown in Equation (1.10).

$$e_n^2 = \frac{i_n^2}{g_m^2} = \left[\frac{8kT\left(1+\eta\right)}{3g_m} + \frac{\left(KF\right)I_D}{2fC_{ox}WLK'}\right]\Delta f \tag{1.10}$$

1.3 Toplevel Readout Circuits

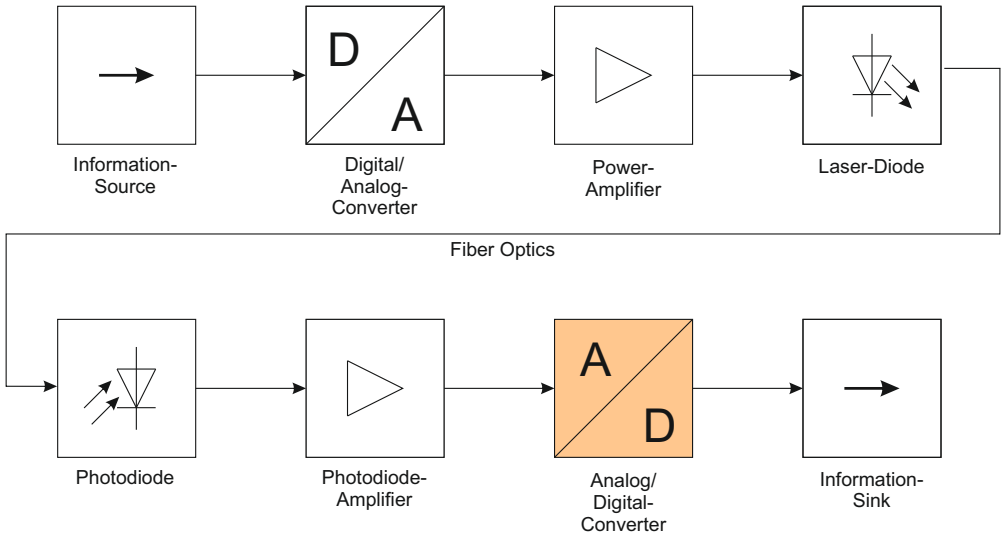

FIGURE 1.8: Structure diagram of an optical transmission system.

From a systematic approach, the impact of the subsequent system on the amplifier has to be considered as well at design level. Usually the top level readout of photodiodes is done by converting analog voltage to digital values. The conversion between time-continuous / continuous current values and time discrete / discrete values is done by a so called analog-to-digital converter.

There are many different types and topologies of analog-to-digital converters but almost every type needs a track-and-hold circuit at the input, to provide freezed signal to the conversion circuit. The flash type ADC does not intrinsically need a track-and-hold circuit at its input, because the conversion is done immediately with high speed. The disadvantage of the flash adc is the fact that it needs a lot of comparators, depending of the number of bits. The high number of comparators hence features a high capacitance which burdens the output of the photodiode amplifier.

Chapter 2

TIA Topologies

Within the scope of this thesis different transimpedance amplifier topologies are investigated. There exist many different architectures for TIAs, each having its specific advantages and disadvantages. Parameters for the selection of an appropriate topology can be for instance bandwidth, gain, noise, stability regarding different input / output capacitances.

After extensive literature research two topology types looked promising to fulfil the specifications of a bandwidth of at least 100 MHz, a gain value of approximately 60 dB and the ability to detect signals featuring an amplitude as low as 10 nA. On the one hand the quite simple inverter based amplifiers, where a one stage solution and a more complex three stage solution is provided, and on the other hand a highly specialized low noise architecture called regulated cascode transimpedance amplifier are investigated.

For all proposed circuits a 180 nm standard CMOS process without any special process options is used. The supply voltage is set to $V_{DD} = 1.8\,\mathrm{V}$ unless otherwise noted.

2.1 Simple Inverter Circuit

According to literature [2] a inverter based transimpedance amplifier is considered to be a shunt-shunt feedback amplifier.

2.1.1 Single Stage Inverter

To get familiar with the properties of inverter based transimpedance amplifiers, a simple, single stage push-pull inverter cell is designed to function as a transimpedance amplifier. The goal is to get the highest possible gain and bandwidth, as well as the lowest noise behaviour. Figure 2.1 shows the proposed single inverter stage TIA with resistive feedback and a load capacitor which represents the input capacitance of a subsequent top level read out circuit like an analog-to-digital converter.

A push-pull inverter features its largest gain when both transistors *M1* and *M2* are operating in their saturation region. By considering the small-signal model the voltage gain can be found as in Equation (2.1)

$$\frac{v_{out}}{v_{in}} = \frac{-\left(g_{m1} + g_{m2}\right)}{g_{ds1} + g_{ds2}} \tag{2.1}$$

In addition to the voltage gain, the output resistance is defined as Equation (2.2)

$$R_{out} = \frac{1}{g_{ds1} + g_{ds2}} \tag{2.2}$$

The input capacitance C_M (Miller capacitance) for a push pull inverter is dominated by gate-drain capacitance of *M1* (Equation (2.5)), whereas the output capacitance consists of the gate-drain capacitance of *M2*, the bulk-drain capacitance of both transistors and the load capacitance C_L located at the output (Equation (2.6)). The frequency behaviour of an inverter based amplifier is defined by a pole and a zero. Usually, the zero in Equation (2.3) is larger than the pole and therefore the corner frequency is solely defined by the pole in Equation (2.4).

$$z = \frac{g_{m1} + g_{m2}}{C_M} \tag{2.3}$$

$$p = \frac{-1}{R_{out}\left(C_{out} + C_M\right)} \tag{2.4}$$

with

$$C_M = C_{gd1} \tag{2.5}$$

$$C_{out} = C_{gd2} + C_{bd1} + C_{bd2} + C_L \tag{2.6}$$

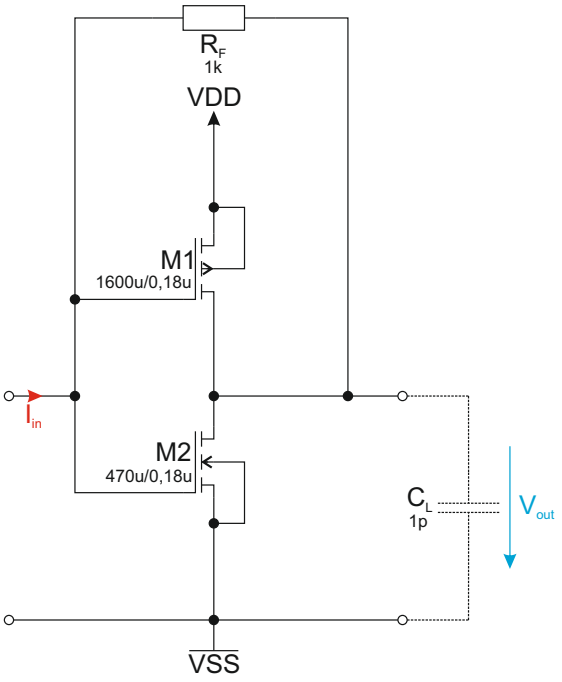

FIGURE 2.1: Schematic of a single stage inverter transimpedance amplifier with feedback resistor R_F and load capacitance C_L.

2.1.1.1 Noise Analysis of a Push-Pull Inverter

According to [4] the equivalent input referred noise of a push-pull inverter can be calculated as in Equation (2.7).e_{n1} and e_{n2} represent noise of respective MOSFETs.

$$e_{eq} = \sqrt{\left(\frac{g_{m1}e_{n1}}{g_{m1}+g_{m2}}\right)^2 + \left(\frac{g_{m2}e_{n2}}{g_{m1}+g_{m2}}\right)^2} \tag{2.7}$$

2.1.1.2 Implementation and Simulation Results

The process used is a XFAB 180 nm standard CMOS process with regards to potential production costs only very basic modules available e.g. no isolated devices, no low noise transistors. The supply voltage is set to $VDD = 1.8\,\mathrm{V}$. Transistor *M1* is a p-type

MOSFET, whereas *M2* is a corresponding n-type MOSFET. The circuit diagram is shown in Figure 2.1. As output load, a capacitor with a capacitance of $C_L = 1\,\text{pF}$ is used.

The dimensioning of a single stage push pull inverter transimpedance amplifier is rather easy. On the one hand, both transistors should operate in saturation region, on the other hand g_m and i_d of both transistors has to be big enough to drive the specified output load capacitance of $C_L = 1\,\text{pF}$. In this design, the bias current is $i_d = 21,67\,\text{mA}$ which is extremely high for a 180 nm process. As a matter of fact, the transistors have to be extremely big as well.

Figure 2.2 shows the open-loop frequency response of a single stage push-pull inverter based TIA. To be able to provide a big enough phase margin with respect to the output capacitance, the sizes of both transistors are chosen. The p-type MOSFET has to be approximately two times bigger compared to the n-type MOSFET because of worse mobility of the holes. The first pole at a frequency of about $f_{p1} = 100\,\text{Hz}$ is defined by the photodiode itself.

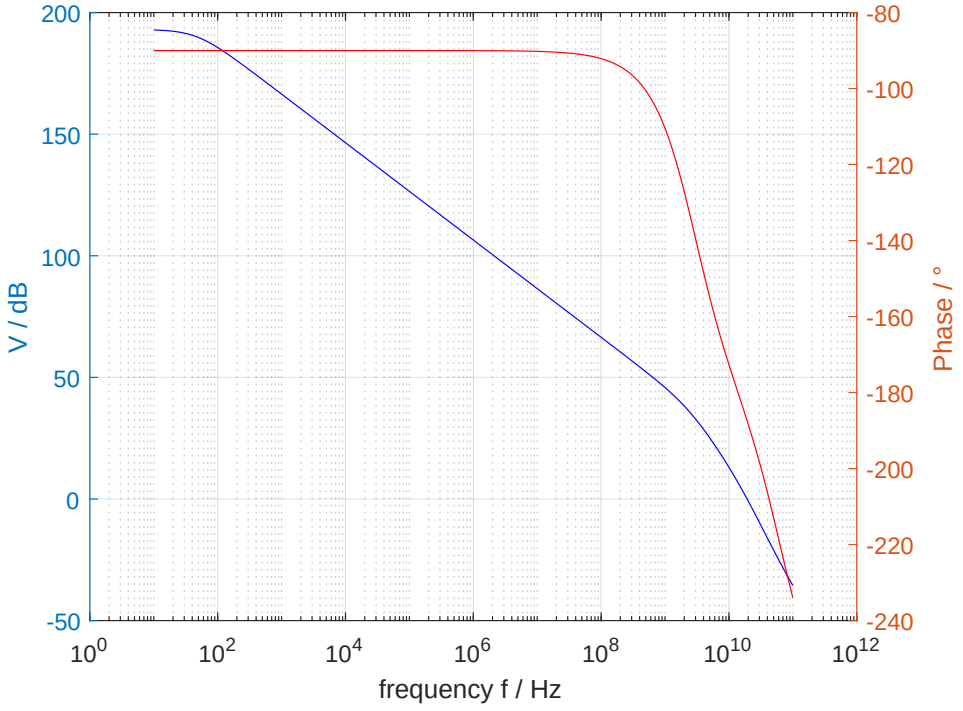

FIGURE 2.2: Open loop Bode diagram of the single stage inverter TIA

Figure 2.3 shows the transient response of the proposed TIA. It can be easily seen, that the voltage at the output follows the input current with just a little amount of

over-/undershoot, which also proofs the stability of the circuit.

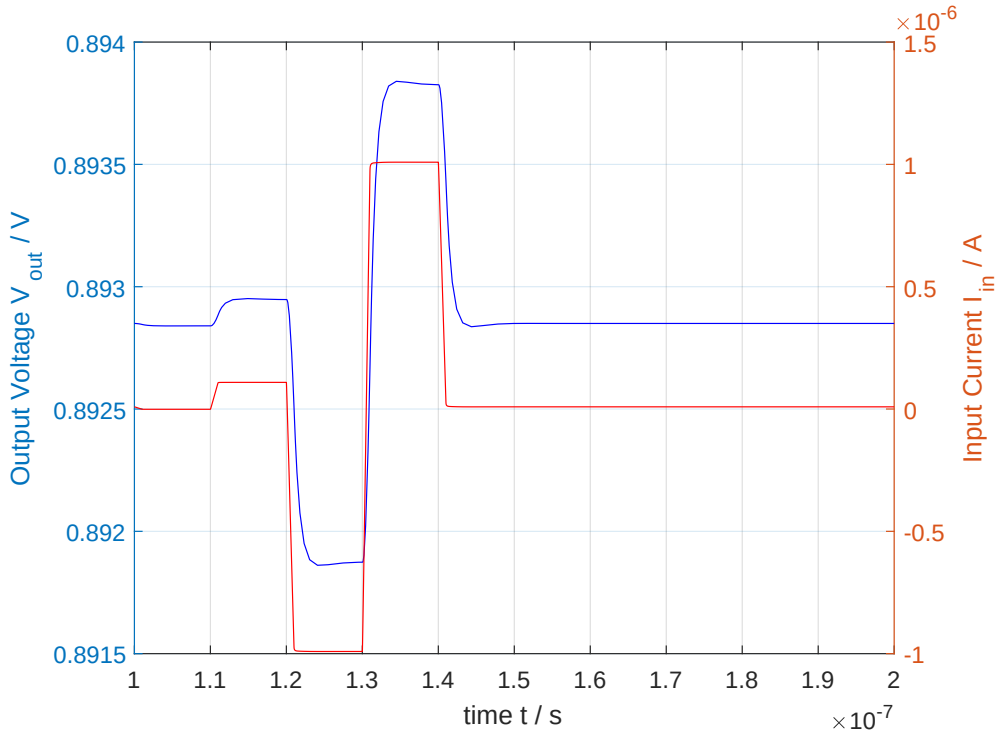

FIGURE 2.3: Transient analysis the proposed single stage push pull inverter transimpedance amplifier. There can be a little overshoot observed at the edges, but it is still considered to be stable.

Figure 2.4 depicts the noise response of the single stage inverter based TIA. The red line shows the equivalent output noise voltage, whereas the blue graph shows the input referred noise current. With respect to the input referred noise current, the distribution of different noise sources: flicker noise at low frequencies and thermal noise at higher frequencies, can be seen quite nicely.

2.1.1.3 Simulated Circuit Performance including Process Corners

Finally the proposed circuit was simulated using corner analysis. All process corners for MOSFETs and resistors are simulated.

For MOSFET devices the *worst speed (ws)*, *worst power (wp)*, *worst one (wo)*, *worst zero (wz)* and *typical mean (tm)* cases are simulated. For resistors the *worst power (wp)*, *worst speed (ws)* and *typical mean (tm)* are simulated. The temperature ranges from $T = 0\,°\mathrm{C}$ to $T = 80\,°\mathrm{C}$. The supply voltage is set to $V_{DD} = 1.8\,\mathrm{V}$.

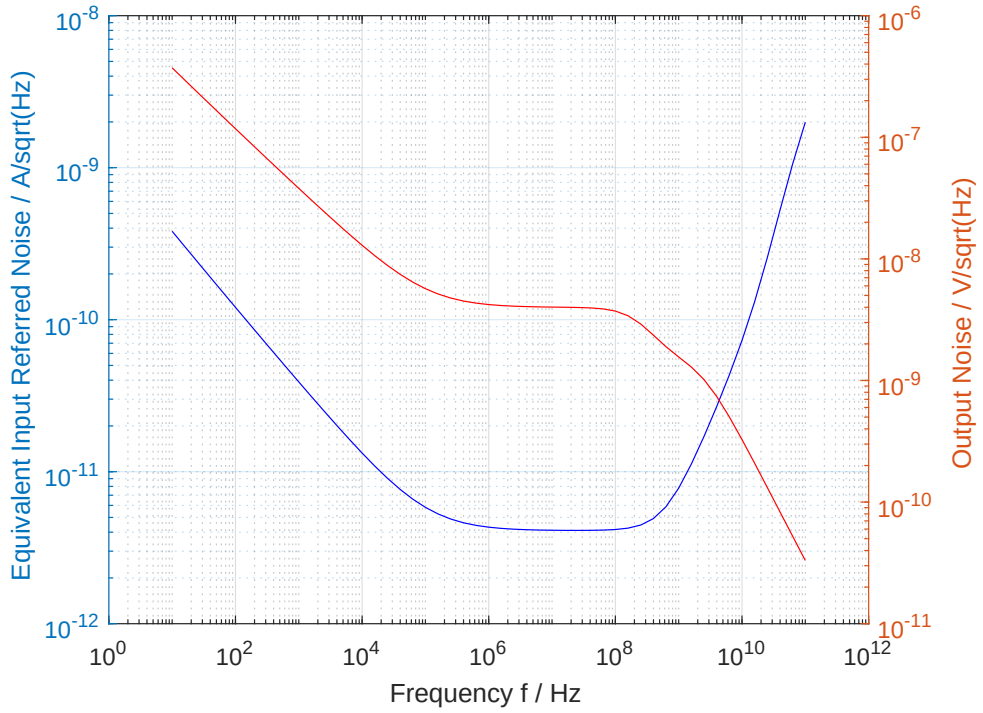

FIGURE 2.4: Noise analysis the proposed single stage push pull inverter transimpedance amplifier. The red line represents the noise voltage at the output, whereas the blue line represents the equivalent input referred noise current.

The results of the performance and some other parameters across these corners are shown in Table 2.1. Regarding the transient response, rise- and fall times are determined only for the typical process corner.

In addition to the overall noise analysis shown in Figure 2.4, a more detailed noise analysis is conducted. Table 2.2 shows the noise contribution at the output for different devices at different frequencies. This analysis is helpful to detect the most severe noise sources in a circuit which is the feedback resistor in this case. The noise contribution of the photodiode is not modelled and simulated. The unit for spot noise is $V/\sqrt{Hz}$, the unit for the integrated noise is V.

TABLE 2.1: Simulated circuit performance of a single stage push-pull inverter transimpedance amplifier, including corner analysis.

Parameter	Symbol	Unit	Min	Typ	Max	Condition/Comment
DC output	V_{outDC}	V	836,2	892,8	961,8	Iin=0 (Closed Loop)
DC input	V_{inDC}	V	836,2	892,8	961,8	Iin=0 (Closed Loop)
Output upper dynamic voltage	$V_{outDR_{hi}}$	V	1,55		1,58	
Output lower dynamic voltage	$V_{outDR_{lo}}$	V	0,2		0,22	
Input upper dynamic current	$I_{inDR_{hi}}$	µA	500		1000	
Input lower dynamic current	$I_{inDR_{lo}}$	µA	-1000		-400	
AC closed loop gain	A_{CL}	dB	57,56		62,53	dB[V/A]
AC closed loop 3dB frequency	f_{3dB}	MHz	150,7	250	322,6	
AC open loop gain	A_{OL}	dB	190		195	dB[V/A]
Phase margin	Φ_M	deg	54		56,2	
Gain bandwidth	GBW	GHzOhm		275		
Rise time	t_R	ns		1,55		10n – 100n
Fall time	t_F	ns		2,35		100n – 10n
Input referred noise 100 MHz	i_{eq}	pA/sqrtHz		4,14		
Integrated input referred noise	$i_{eq_{RMS}}$	nA		66,42		1kHz – 250MHz
Power consumption	P	mW		39		
Estimated Area	A	μm^2		9600		

TABLE 2.2: Noise contribution of different devices at different frequencies at a single stage push-pull inverter based transimpedance amplifier. The unit for spot noise is $V/\sqrt{Hz}$, the unit for the integrated noise is V.

Frequency	device	param	Output Noise Contribution	% of total
100kHz	RF.r1	rn	3,98E-09	49,13
	M2.m1	fn	3,92E-09	47,47
	M1.m1	fn	1,02E-09	3,25
100MHz	RF.r1	rn	3,66E-09	97,1
	M2.m1	id	3,99E-10	1,16
	M1.m1	fn	3,56E-10	0,92
10Hz - 250MHz	RF.r1	rn	5,50E-05	95,13
	M2.m1	id	7,48E-06	1,76
	M2.m1	fn	7,25E-06	1,65

2.1.2 Single Stage Push-Pull Cascoded Inverter Transimpedance Amplifier

In a cascode amplifier topology, the CS-stages at the input get extended by a CG stage. A cascode extension features two advantages over common source amplifiers. At first, a cascode topology reduces the miller capacitance and therefore increases the bandwidth of the amplifier. Secondly, it increases the output impedance and therefore the overall gain of the amplifier [4]. A push-pull inverter stage consists of two complementary CS stages, the one on the upper side implemented with PMOS transistors, the CS stage on the lower side implemented with NMOS transistors.

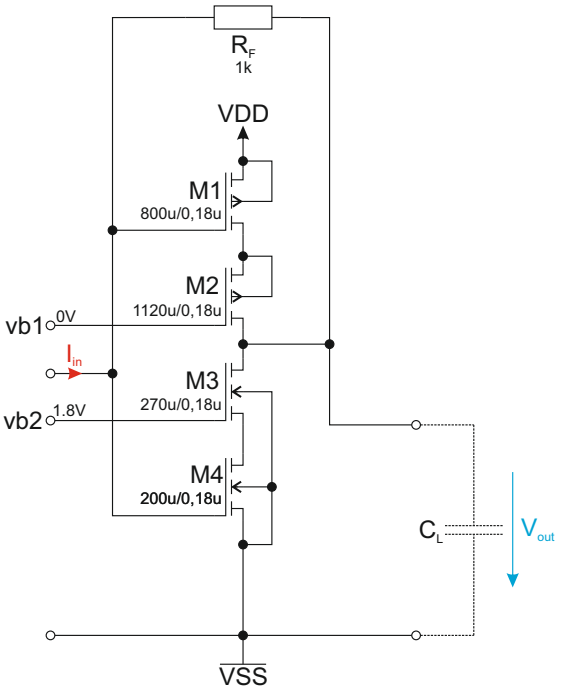

FIGURE 2.5: Schematic of a transimpedance amplifier based on a single stage cascoded push-pull inverter with feedback resistor R_F and load capacitance C_L and a diode load after each stage.

According to [5] the voltage gain of a cascode inverter proposed in Figure 2.5 is shown in equation Equation (2.8). The corresponding bandwidth can be estimated as in Equation (2.9).

$$A_{invC} = (g_{M3} + g_{M4}) \cdot [(g_{M3} r_{dsM3} r_{dsM4}) \,||\, (g_{M2} r_{dsM2} r_{dsM1})] \tag{2.8}$$

$$BW_{invC} \cong \frac{1 + A_{invC}}{2\pi R_F \left(C_j + C_{gsM1,M4} + C_{gdM1} C_{gdM4}\right)} \tag{2.9}$$

Dimensioning of a push pull cascoded inverter is straight forward. Again, major concern is, that all transistors should operate in the saturation regime and that the bias voltages at the output and input are somewhere around $V_{DD}/2$. Transistors *M2* and *M3* are biased to act primarily as switches, and therefore increasing the output resistance just a little bit, while not decreasing the performance of transistors *M1* and *M4*. The parameters for optimum performance are determined by simulation. The results obtained by the simulation are comparable to results shown in [5].

Figure 2.6 shows the Bode plot of the open loop configuration as well as the closed loop configuration. The lowest pole is determined by the photodiode. The gain at the closed loop is mainly set by the feedback resistance of $R_F = 1\,\mathrm{k\Omega}$, similarly to the previously discussed topology.

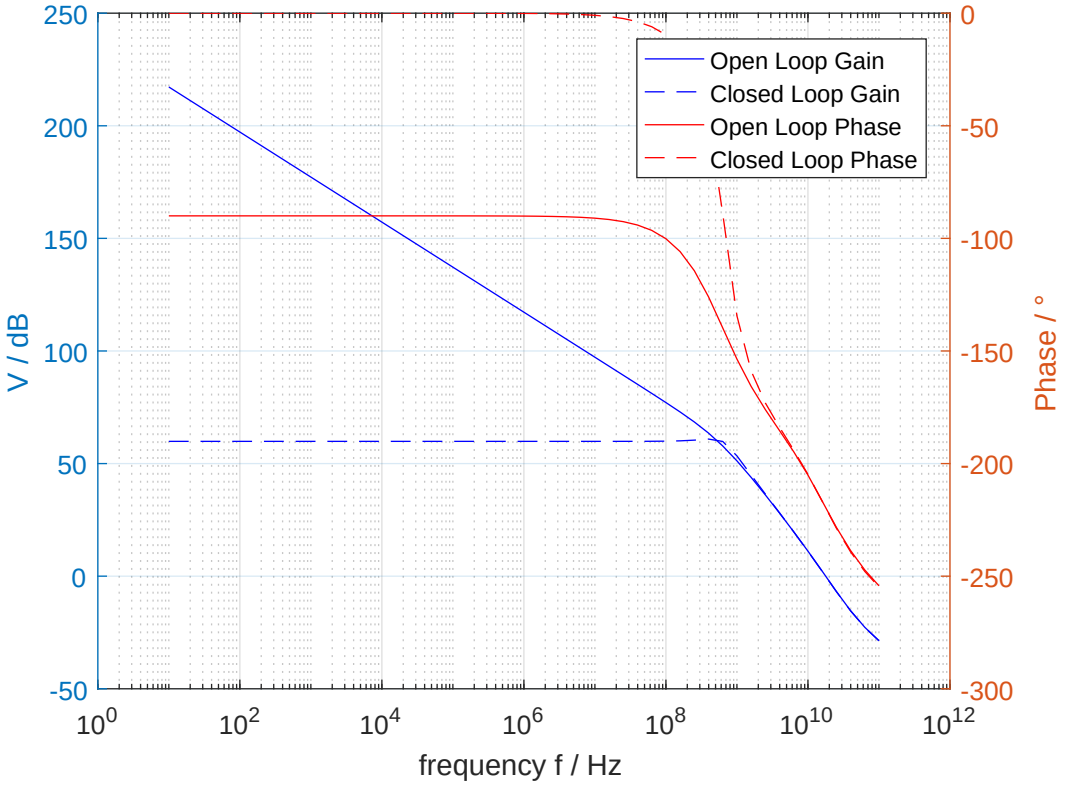

FIGURE 2.6: Bode plot of a single stage inverter amplifier with cascode. The solid line depicts the open loop configuration, whereas the dashed line represents the closed loop configuration with a feedback resistance of $R_F = 1\,\mathrm{k\Omega}$.

Again, transient response approves stability but there is a little amount of over-/undershoot observable which can be seen in Figure 2.7. Nevertheless, this over-/undershoot can be also seen at the input signal, which leads to the conclusion, that this behaviour has to be caused by the photodiode in interaction with the amplifier. The amplifier itself features a phase margin of approximately $\Phi_M = 60\,°$, so it can be considered as stable.

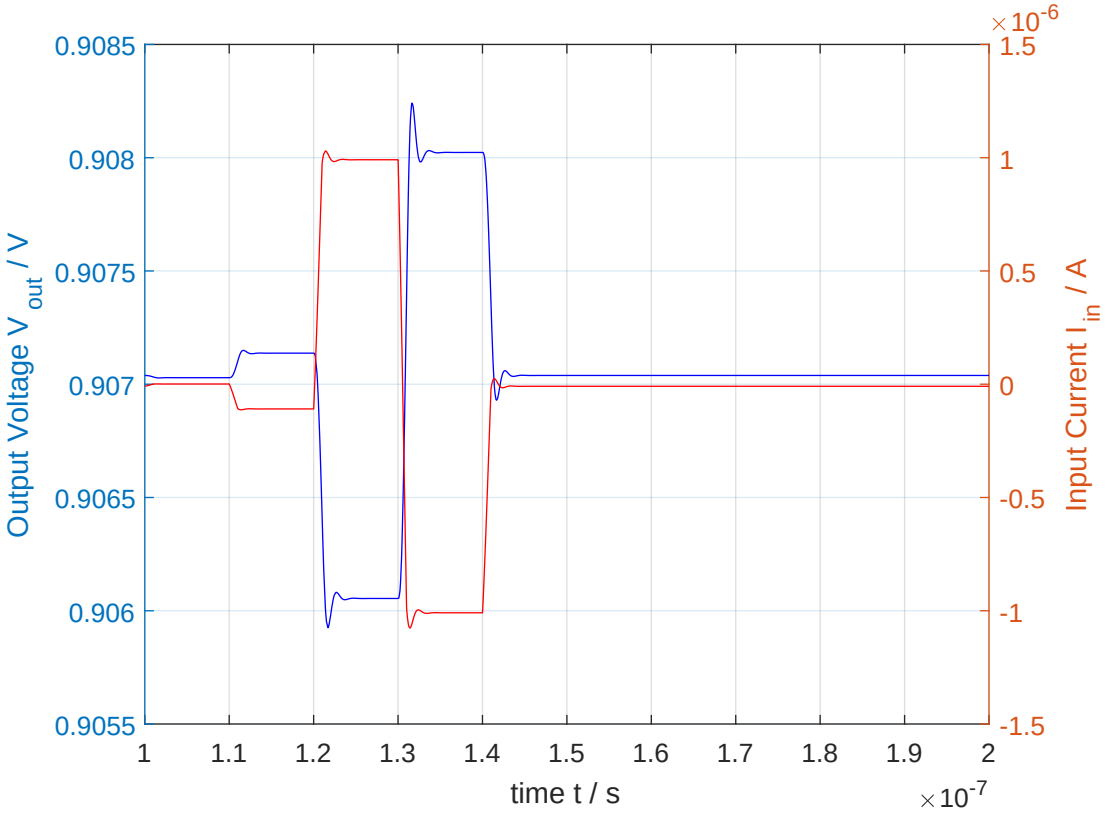

FIGURE 2.7: Transient response of a single stage push pull inverter based transimpedance amplifier with cascode.

The noise behaviour of the cascoded inverter looks similiar to the response of the conventional push-pull inverter transimpedance amplifier. Figure 2.8 shows noise in the same order of magnitude compared to the single stage inverter TIA without cascode. The main advantage of a cascode based inverter TIA is the higher bandwidth and therefore the possibility to use a higher transimpedance, which then leads to a reduction of the influence of transistors on the input referred noise, as their contribution will be attenuated by a higher gain.

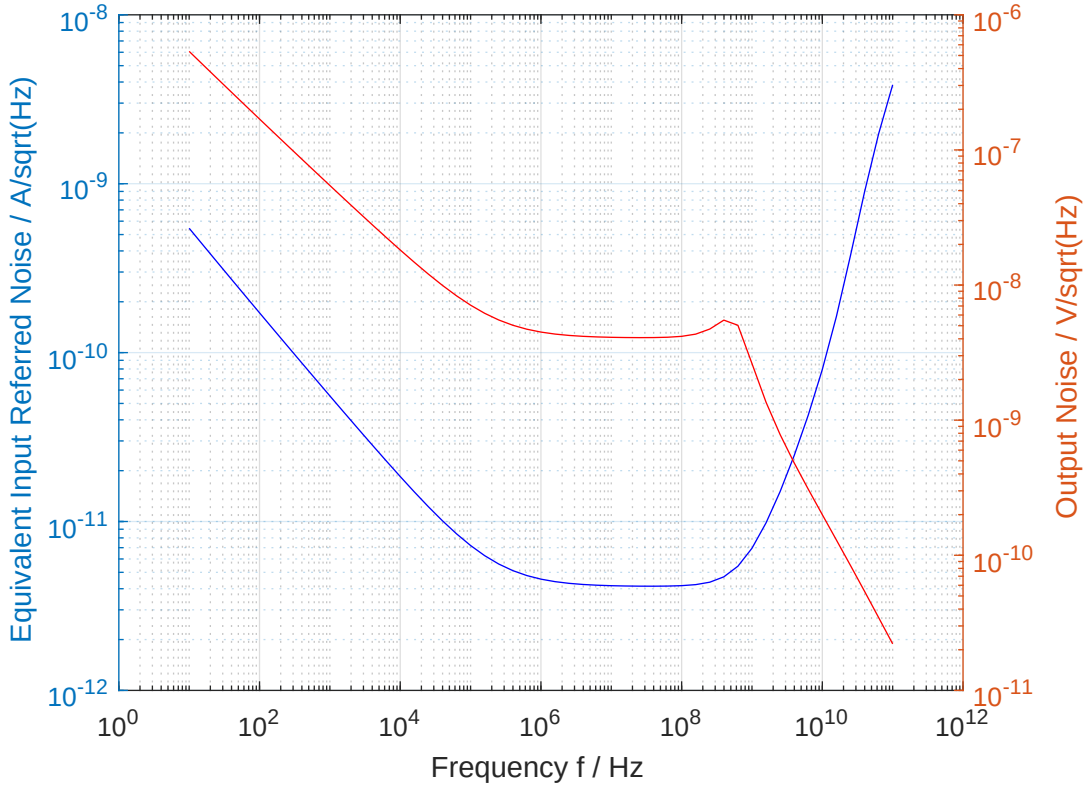

FIGURE 2.8: Noise analysis of a single stage cascoded push-pull inverter based transimpedance amplifier. The blue curve shows input referred current noise, whereas the red curve shows the output noise voltage.

2.1.2.1 Simulated Circuit Performance including Process Corners

Finally the proposed circuit was simulated using corner analysis. All process corners for MOSFETs and resistors are simulated.

For MOSFET devices the *worst speed (ws)*, *worst power (wp)*, *worst one (wo)*, *worst zero (wz)* and *typical mean (tm)* cases are simulated. For resistors the *worst power (wp)*, *worst speed (ws)* and *typical mean (tm)* are simulated. The temperature ranges from $T = 0\,°\mathrm{C}$ to $T = 80\,°\mathrm{C}$. The supply voltage is set to $V_{DD} = 1.8\,\mathrm{V}$.

TThe results of the performance and some other parameters across these corners are shown in Table 2.3.

In addition to the overall noise analysis shown in Figure 2.8, a more detailed noise analysis is conducted. Table 2.4 shows the noise contribution at the output for different devices at different frequencies. This analysis is helpful to detect the most severe noise

sources in the circuit. The noise contribution of the photodiode is not modelled and simulated. The unit for spot noise is $V/\sqrt{Hz}$, the unit for the integrated noise is V.

TABLE 2.3: Simulated circuit performance of a single stage push-pull inverter transimpedance amplifier with integrated cascode circuit, including corner analysis.

Parameter	Symbol	Unit	Min	Typ	Max	Condition/Comment
DC output	V_{outDC}	V	847,9	907	979,7	Iin=0 (Closed Loop)
DC input	V_{inDC}	V	847,9	907	979,7	Iin=0 (Closed Loop)
Output upper dynamic voltage	$V_{outDR_{hi}}$	V	1,4		1,59	
Output lower dynamic voltage	$V_{outDR_{lo}}$	V	0,25		0,39	
Input upper dynamic current	$I_{inDR_{hi}}$	µA	388		1000	
Input lower dynamic current	$I_{inDR_{lo}}$	µA	-1000		-406,8	
AC closed loop gain	A_{CL}	dB	57,62		62,61	dB[V/A]
AC closed loop 3dB frequency	f_{3dB}	MHz	521	791	1016	
AC open loop gain	A_{OL}	dB	216		218	dB[V/A]
Phase margin	Φ_M	deg	58		66	
Gain bandwidth	GBW	GHzOhm		791		
Rise time	t_R	ns		0,41		10n – 100n
Fall time	t_F	ns		0,84		100n – 10n
Input referred noise 100 MHz	i_{eq}	pA/sqrtHz		4,17		
Integrated input referred noise	$i_{eq_{RMS}}$	nA		135,8		1kHz – 791MHz
Power consumption	P	mW		17,49		
Estimated Area	A	μm^2		13900		

TABLE 2.4: Noise contribution of different devices at different frequencies at a single cascoded stage push-pull inverter based transimpedance amplifier. The unit for spot noise is $V/\sqrt{Hz}$, the unit for the integrated noise is V.

Frequency	device	param	Output Noise Contribution	% of total
100kHz	M4.m1	fn	5,63E-09	63,04
	RF.r1	rn	4,04E-09	32,37
	M1.m1	fn	1,48E-09	4,35
100MHz	RF.r1	rn	4,10E-09	96,73
	M4.m1	id	4,59E-10	1,21
	M1.m1	id	4,02E-10	0,93
10 - 791M	RF.r1	rn	1,17E-04	74,64
	M4.m1	id	4,63E-05	11,6
	M1.m1	id	3,96E-05	8,51

2.1.3 Three Stage Push-Pull Inverter Transimpedance Amplifier

Due to the fact that literature for very low noise transimpedance amplifiers based on three stage inverter based amplifiers [2], this topology is also investigated in this thesis. By cascading more inverter stages together, a three stage inverter based TIA is created. The idea of creating more stages is to split the open-loop gain into more stages, although using more than one amplifier stage makes the circuits become more unstable and difficult to use as the second pole has to be more than two times larger than the gain-bandwidth product. Therefore a large safety margin at the design level is required. However transimpedance amplifiers based on three inverter stages are used in circuits where low noise behaviour is required [2] and a tradeoff between gain and bandwidth can be found. As three stage inverter based transimpedance amplifiers do not meet the criteria for either bandwidth or gain for the characterization of photodiodes, the other presented topologies might be preferred.

Based on the approach of [6] a three stage push pull inverter based circuit is designed. The transfer function is written in Equation (2.10)

$$\frac{v_{out}}{v_{in}} = \frac{A}{1+A}\frac{R_F}{1+j\omega C_T \frac{R_F}{1+A}} \tag{2.10}$$

where C_T consists of the capacitance of the photodiode and the inputcapacitance of the amplifier. A is considered to be the intrinsic gain of the amplifier.

Figure 2.9 shows the implemented three stage inverter based transimpedance amplifier. Speaking of a three stage amplifier, there exist at least three poles compromising stability. Therefore stability requires extensive attention at this topology. The first stage is designed to be the biggest regarding transistor dimensions to fulfil the above mentioned stability criteria for cascaded inverters. According to the nomograph method used in [2], the second stage has to be at maximum only half the size of the first stage. Additionally a diode load after each stage limits gain and is of utmost importance to make a three stage inverter based TIA stable. The phase margin can be controlled by the size of the diode load. Another approach to make such a circuit stable would be a single feedback resistor at each stage, which is theoretically proposed in literature [7].

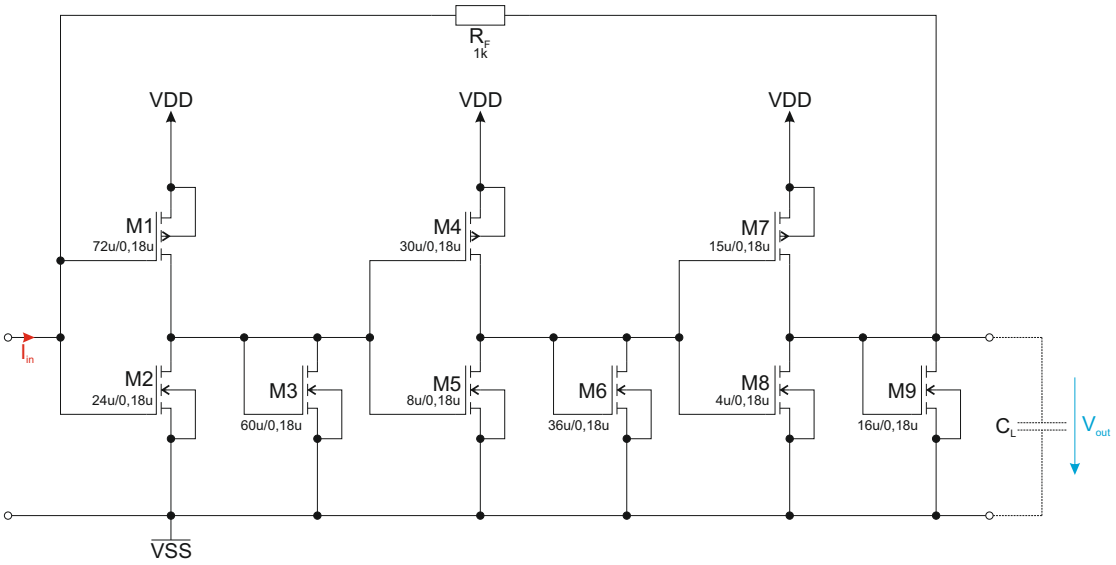

FIGURE 2.9: Schematic of a three stage inverter transimpedance amplifier with feedback resistor R_F and load capacitance C_L and a diode load after each stage. At the first stage a cascode circuit is used to increase the gain, and thus the noise figure of the ciruit.

Figure 2.10 shows the Bode plot of the amplifier in open loop and in closed loop configuration. A phase margin of approximately $\phi_m = 50\,^\circ$ is obtained. The closed-loop gain in this case is not only defined by the feedback resistor $R_f = 1\,\mathrm{k\Omega}$, but also by the load transistor of the last stage, which is important for stability.

Transient response in Figure 2.11 proofes stability of the circuit. As the over-/undershoot is quite low, a phasemargin of $\phi_m = 50\,^\circ$ is sufficient.

Figure 2.12 shows the noise behaviour of the proposed TIA.

2.1.3.1 Simulated Circuit Performance including Process Corners

Finally the proposed circuit was simulated using corner analysis. All process corners for MOSFETS and resistors are simulated. For all other types of devices the option *typical mean (tm)* is used.

For MOSFET devices the *worst speed (ws)*, *worst power (wp)*, *worst one (wo)*, *worst zero (wz)* and *typical mean (tm)* cases are simulated. For resistors the *worst power (wp)*, *worst speed (ws)* and *typical mean (tm)* are simulated. The temperature ranges from $T = 0\,^\circ\mathrm{C}$ to $T = 80\,^\circ\mathrm{C}$. The supply voltage is set to $V_{DD} = 1.8\,\mathrm{V}$.

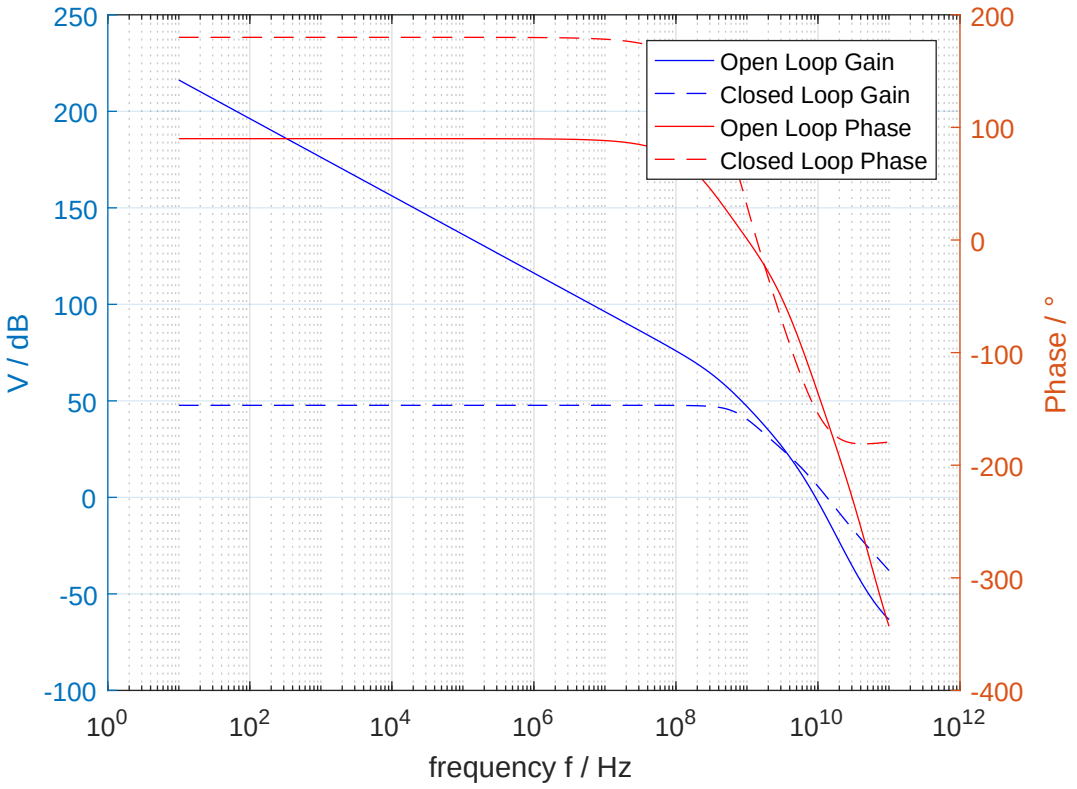

FIGURE 2.10: Bode plot of a three stage inverter amplifier.

The results of the performance and some other parameters across these corners are shown in Table 2.5.

In addition to the overall noise analysis shown in Figure 2.12, a more detailed noise analysis is conducted. Table 2.6 shows the noise contribution at the output for different devices at different frequencies. This analysis is helpful to detect the most severe noise sources in the circuit. The noise contribution of the photodiode is not modelled and simulated. The unit for spot noise is $V/\sqrt{Hz}$, the unit for the integrated noise is V.

2.1.4 Summary of inverter based transimpedance amplifiers

Three different types of inverter based transimpedance amplifiers are reviewed in this thesis. Often inverter based amplifiers TIAs are used for sake of simplicity, but compared to different, more sophisticated topologies they either perform worse, or feature increased bias current or size requirements.

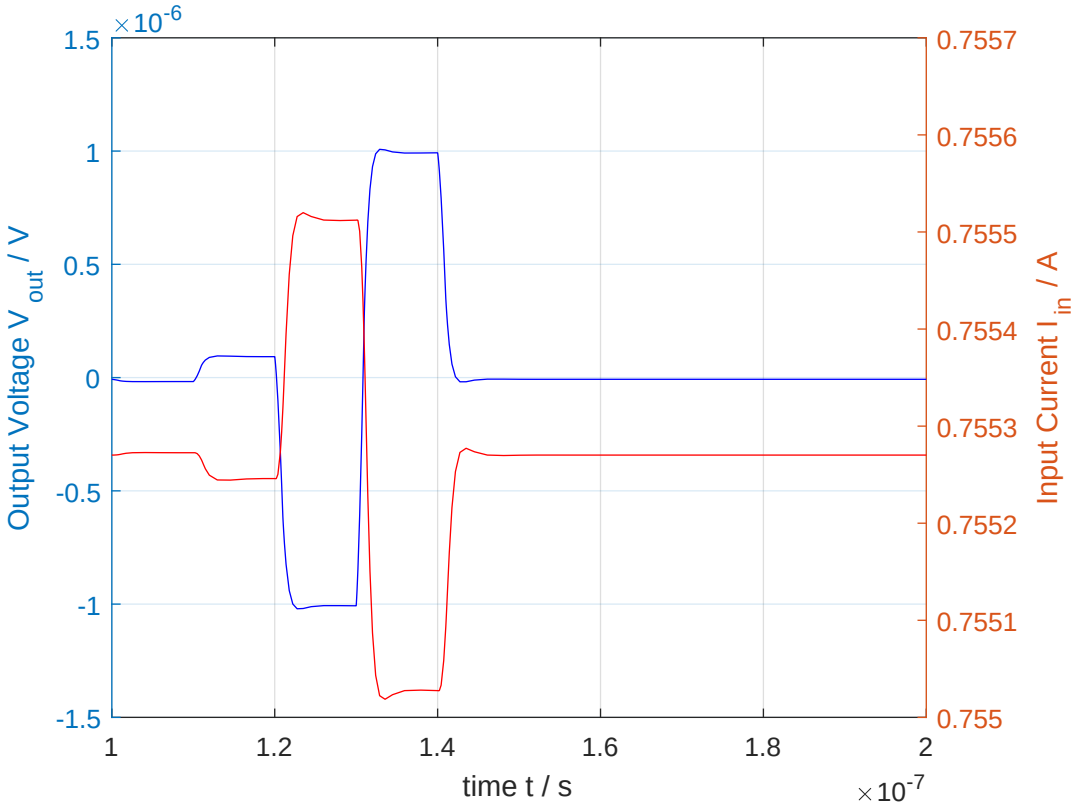

FIGURE 2.11: Transient analysis of a three stage inverter amplifier.

A single stage push-pull inverter TIA is easy to design and provides good overall performance, although it needs to be quite big to drive requested output capacitance. The proposed amplifier can reach a bandwidth of up to 250 MHz by providing a gain of 60 dBΩ. The integrated input referred noise level lies at 66, 42 nA for the specified bandwidth. Most probably because of its simplicity, it is often used in today's circuits.

The cascoded inverter TIA provides even better gain and bandwidth compared to a single stage inverter TIA, but due to the added transistors the output voltage swing is limited. The extended amplifier can reach a bandwidth of up to 791 MHz by providing a gain of 60 dBΩ. The integrated input referred noise level lies at 135, 42 nA for the specified bandwidth.

Due to stability restrictions, a three stage inverter based TIA either provides high bandwidth and low gain or vice versa. For instance, this topology is used for highly specialized applications like current-voltage converters for Everhart-Thornley detectors at scanning electron microscopes, where bandwidth is not a big issue. For photodiode applications

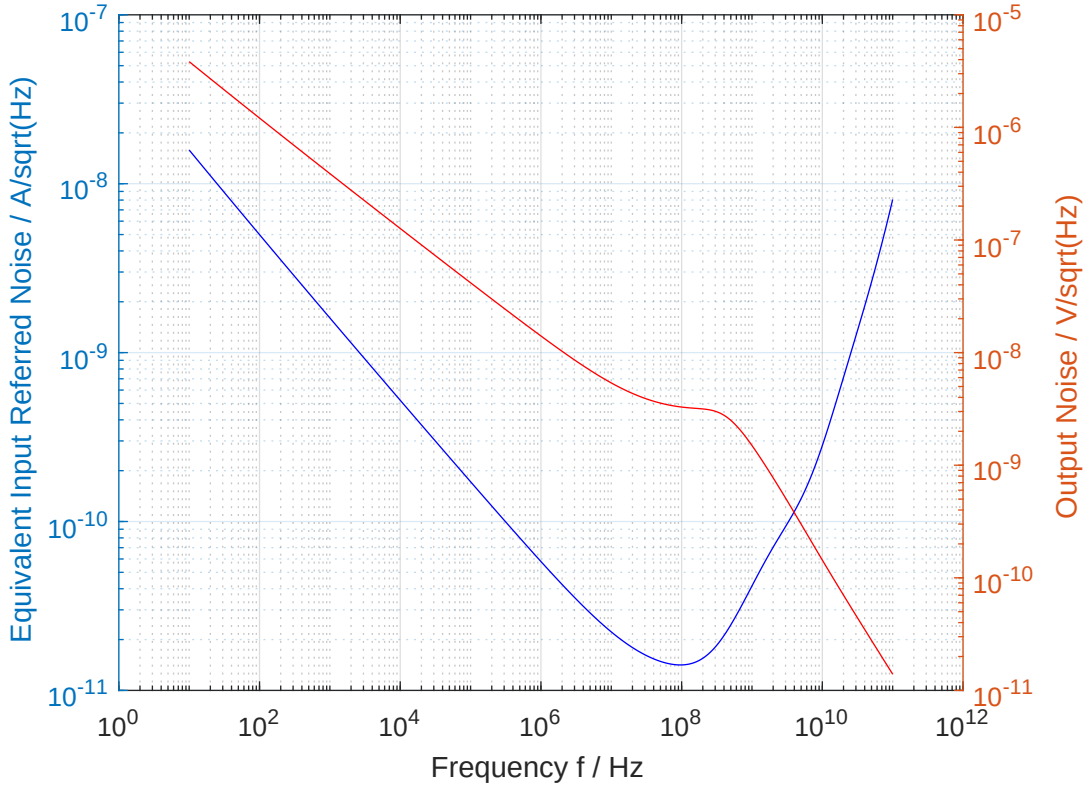

FIGURE 2.12: Noise analysis of a three stage inverter amplifier.

though, high bandwidth and high gain are important requirements to meet. Additionally the stability heavily depends on the input and output configuration. Therefore this topology is not applicable for characterization purposes and hence not considered further.

For the single stage inverter amplifiers the device with the most noise contribution in each single case is the feedback resistor R_F. Although, R_F is equal to all circuits, different values for the integrated noise are determined due to the different bandwidths obtained by the amplifiers.

TABLE 2.5: Simulated circuit performance of a three stage push-pull inverter transimpedance amplifier circuit, including corner analysis.

Parameter	Symbol	Unit	Min	Typ	Max	Condition/Comment
DC output	V_{outDC}	V	738,1	798,4	851,9	Iin=0 (Closed Loop)
DC input	V_{inDC}	V	738,1	798,4	851,9	Iin=0 (Closed Loop)
Output upper dynamic voltage	$V_{outDR_{hi}}$	V	0,85		1,1	
Output lower dynamic voltage	$V_{outDR_{lo}}$	V	0,33		0,45	
Input upper dynamic current	$I_{inDR_{hi}}$	µA	410		470	
Input lower dynamic current	$I_{inDR_{lo}}$	µA	-655		-466	
AC closed loop gain	A_{CL}	dB	35,83	47,69	54,84	dB[V/A]
AC closed loop 3dB frequency	f_{3dB}	MHz	504	602	1570	
AC open loop gain	A_{OL}	dB		215		dB[V/A]
Phase margin	Φ_M	deg	37	50,27	62,56	
Gain bandwidth	GBW	THzOhm		240		
Rise time	t_R	ns		1,53		10n – 100n
Fall time	t_F	ns		0,85		100n – 10n
Input referred noise 100 MHz	i_{eq}	pA/sqrtHz		14,15		
Integrated input referred noise	$i_{eq_{RMS}}$	nA		510		1kHz – 602MHz
Power consumption	P	mW		6,45		
Estimated Area	A	μm^2		5200		

TABLE 2.6: Noise contribution of different devices at different frequencies at a three stage push-pull inverter-based transimpedance amplifier. The unit for spot noise is $V/\sqrt{Hz}$, the unit for the integrated noise is V.

Frequency	device	param	Output Noise Contribution	% of total
100kHz	M9.m1	fn	5,13E-08	41,37
	M8.m1	fn	3,27E-08	16,86
	M6.m1	fn	2,99E-08	14,06
100MHz	M9.m1	id	2,71E-09	21,81
	M9.m1	fn	1,87E-09	16,11
	M7.m1	id	1,75E-09	14,23
10 - 791M	M9.m1	fn	6,76E-05	22,55
	Rpd	rn	6,37E-05	20,04
	M9.m1	id	4,40E-05	9,57

2.2 Regulated Cascode Input Stages

2.2.1 General Description

Regulated cascode transimpedance amplifiers provide high output impedance and high output voltage swings. Another important property of the regulated cascode topology is its virtual ground input, which is very useful for high-speed and low noise amplifiers [8].According to Figure 2.13 the input current is converted to a voltage at transistor *M1* which operates as a common gate circuit. Transistor *M2* acts as a feedback and reduces the input impedance by the factor of its voltage gain [9]. The input resistance is given by Equation (2.11).

$$Z_{in} \cong \frac{1}{g_{m1}\left(1 + g_{m2}R_2\right)} \tag{2.11}$$

According to [10] the transimpedance gain of the amplifier can be specified as in Equation (2.12).

$$Z_T = \frac{R_1 g_{m1} R_3 \left[1 + g_{m2}\left(r_{ds2}||R_2\right)\right]}{1 + g_{m1}R_3\left[1 + g_{m2}\left(r_{ds2}||R_2\right)\right]} \tag{2.12}$$

2.2.2 Conventional Regulated Cascode Input Stage with Resistors

Figure 2.13 shows the schematic diagram for a conventional regulated cascode transimpedance amplifier based on resistors. In comparison to inverter based transimpedance amplifiers, the transistors are about two orders of magniude smaller by still providing similar noise, gain and bandwidth values. Compared to inverter based transimpedance amplifiers, the slower rise and fall times are considerable. Also it has to be mentioned, that the advantage of smaller transistors is overshadowed by the size and the number of resistors used at the regulated cascode.

As the regulated cascode topology is considered to be an open-loop topology with intrinsic feedback, an open-loop analysis is not usefully viable. Therefore the closed-loop Bode diagram is shown in Figure 2.14.

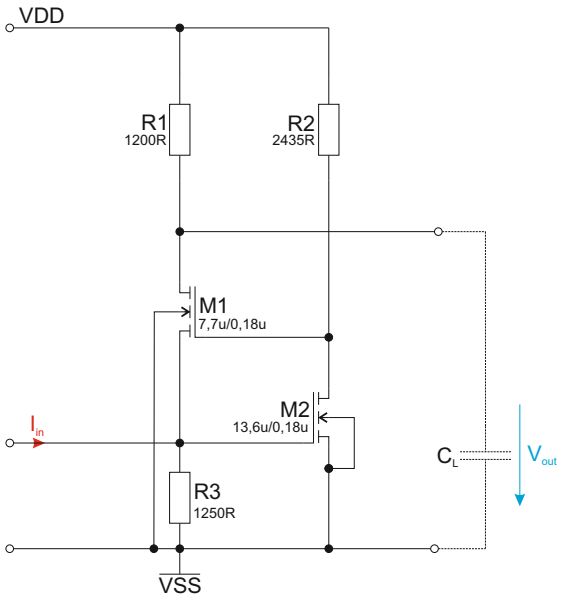

FIGURE 2.13: Circuit diagram of a regulated cascode TIA with resistive biasing.

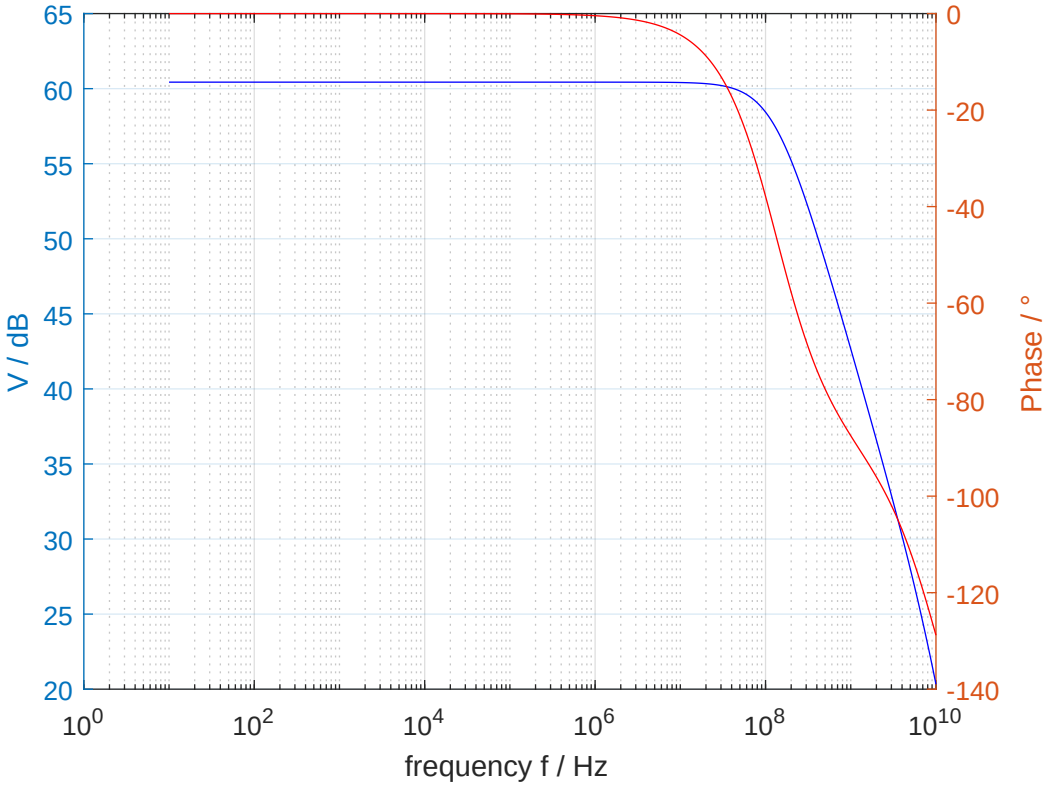

FIGURE 2.14: Bode plot of a regulated cascode TIA with resistors

The transient response in Figure 2.15 approves stability as no over-/undershoot is observable. There is only the typical process corner case shown, but transient analysis is done for all possible process corners.

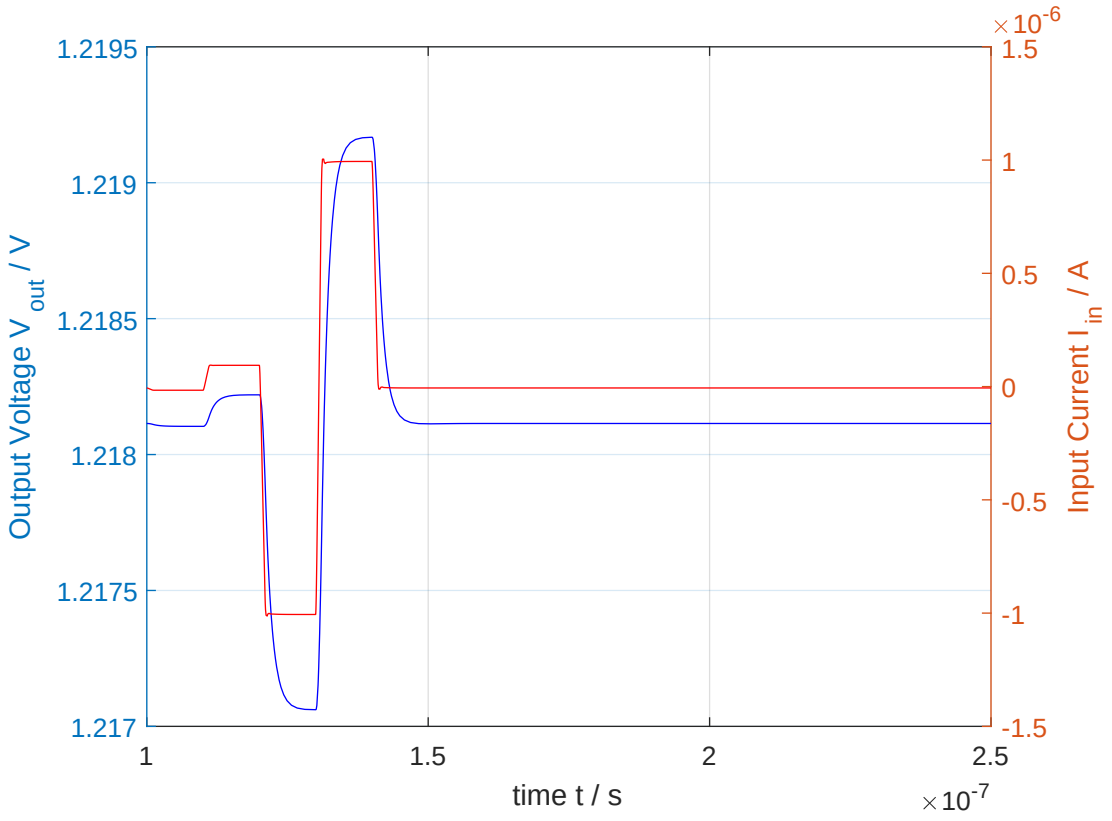

FIGURE 2.15: Transient response of a regulated cascode TIA with resistive biasing.

The noise behaviour of a standard regulated cascode is shown in Figure 2.16. Noise performance of a regulated cascode TIA is comparable to inverter based circuits with much bigger transistors.

2.2.2.1 Simulated Circuit Performance including Process Corners

Finally the proposed circuit was simulated using corner analysis. All process corners for MOSFETs and resistors are simulated. For all other types of devices the option *typical mean (tm)* is used.

For MOSFET devices the *worst speed (ws)*, *worst power (wp)*, *worst one (wo)*, *worst zero (wz)* and *typical mean (tm)* cases are simulated. For resistors the *worst power (wp)*, *worst speed (ws)* and *typical mean (tm)* are simulated. The temperature ranges from $T = 0\,°\text{C}$ to $T = 80\,°\text{C}$. The supply voltage is set to $V_{DD} = 1.8\,\text{V}$.

The results of the performance and some other parameters across these corners are shown in Table 2.7.

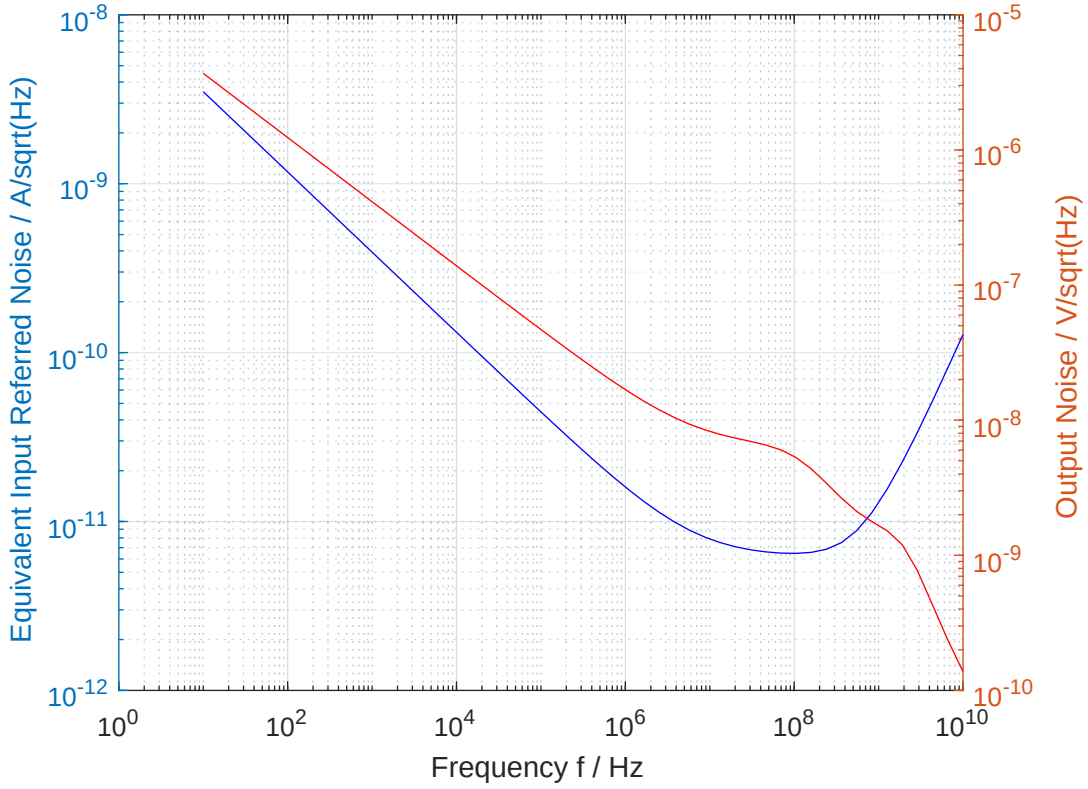

FIGURE 2.16: Noise behaviour of a regulated cascode TIA with resistors.

In addition to the overall noise analysis shown in Figure 2.16, a more detailed noise analysis is conducted. Table 2.8 shows the noise contribution at the output for different devices at different frequencies. This analysis is helpful to detect the most severe noise sources in the circuit. The noise contribution of the photodiode is not modelled and simulated. The unit for spot noise is $V/\sqrt{Hz}$, the unit for the integrated noise is V.

2.2.2.2 PMOS Input Stage

Because of the fact that PMOS transistors are considered to be superior in noise performance compared to NMOS transistors, a circuit complementary to the above mentioned regulated cascode TIA with PMOS input transistors is designed and investigated. Unfortunately the noise analysis shows no significant difference between NMOS and PMOS input transistors.

TABLE 2.7: Simulated circuit performance of a regulated cascode transimpedance amplifier circuit with resistive biasing, including corner analysis.

Parameter	Symbol	Unit	Min	Typ	Max	Condition/Comment
DC output	V_{outDC}	V	1207	1218	1249	Iin=0 (Closed Loop)
DC input	V_{inDC}	V	574,3	606,1	618,1	Iin=0 (Closed Loop)
Output upper dynamic voltage	$V_{outDR_{hi}}$	V	1,75		1,78	
Output lower dynamic voltage	$V_{outDR_{lo}}$	V	0,67		0,75	
Input upper dynamic current	$I_{inDR_{hi}}$	µA	381		960	
Input lower dynamic current	$I_{inDR_{lo}}$	µA	-702		-353	
AC closed loop gain	A_{CL}	dB	57,2		63,5	dB[V/A]
AC closed loop 3dB frequency	f_{3dB}	MHz	95	128	140	
AC open loop gain	A_{OL}	dB				not applicable
Phase margin	Φ_M	deg				not applicable
Gain bandwidth	GBW	GHzOhm		135		
Rise time	t_R	ns		3,5		10n – 100n
Fall time	t_F	ns		3,1		100n – 10n
Input referred noise 100 MHz	i_{eq}	pA/sqrtHz		6,5		
Integrated input referred noise	$i_{eq_{RMS}}$	nA		86,4		1kHz – 128MHz
Power consumption	P	mW		2,9		
Estimated Area	A	μm^2		52000		

TABLE 2.8: Noise contribution of different devices at different frequencies at a resistor based regulated cascode transimpedance amplifier with resistive biasing. The unit for spot noise is $V/\sqrt{Hz}$, the unit for the integrated noise is V.

Frequency	device	param	Output Noise Contribution	% of total
100kHz	M2.m1	fn	4,19E-08	78,17
	M1.m1	fn	2,12E-08	19,98
	R1.r1	rn	4,39E-09	0,85
100MHz	R1.r1	rn	3,48E-09	41,44
	R3.r1	rn	3,04E-09	31,59
	R2.r1	rn	1,80E-09	11,11
10 - 128M	M2.m1	fn	5,25E-05	35,75
	R1.r1	rn	4,41E-05	25,22
	R3.r1	rn	3,85E-05	19,23

2.2.3 Regulated Cascode Input Stage with Current Mirror

As resistor-set bias currents usually lead to big variations in corner analysis, an additional approach of a regulated cascode transimpedance amplifier design is shown in the following section. Two of the three resistors are replaced by current mirrors and a current source, which provide an appropriate bias for the regulated cascode circuit. As the small signal resistance of a current mirror is much bigger compared to the biasing with resistors, also the transistors of the amplifier stage have to be bigger, although the overall size, including biasing transistors and current mirror transistors, of a current mirror based regulated cascode is about 20% less compared to the resistor based approach. Additionally it has to be mentioned, that all transistors used are metal-resistors, which feature the best temperature and process stability. The design of a regulated cascode TIA with current mirrors is shown in Figure 2.17

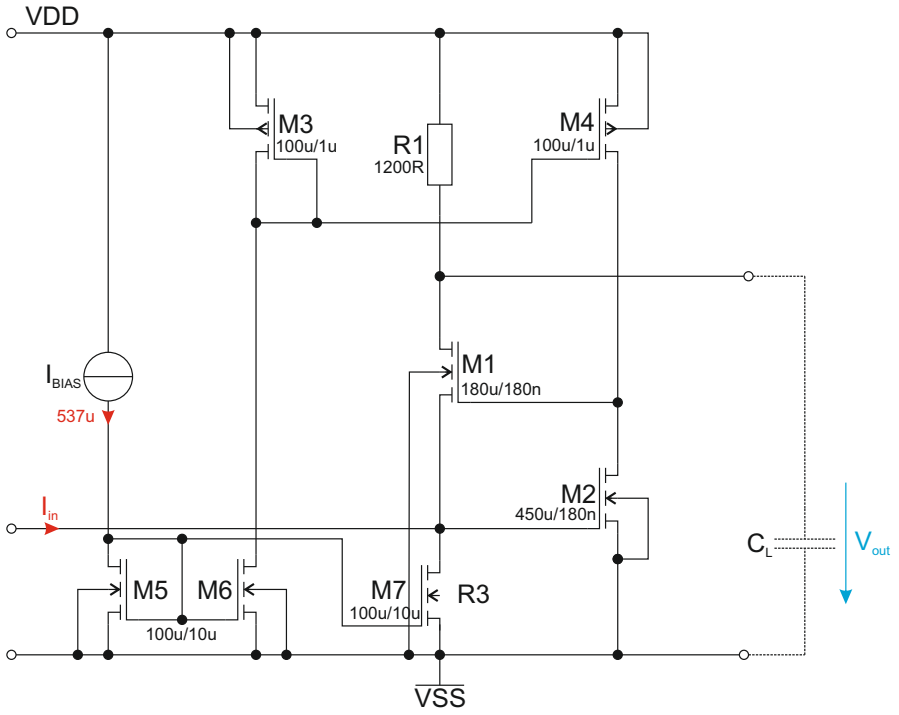

FIGURE 2.17: Schematic diagram of a regulated cascode transimpedance amplifier with current mirrors.

As the regulated cascode topology is considered to be an open-loop topology with intrinsic feedback, an open-loop analysis is not usefully conductable. Therefore the closed-loop Bode diagram is shown in Figure 2.18.

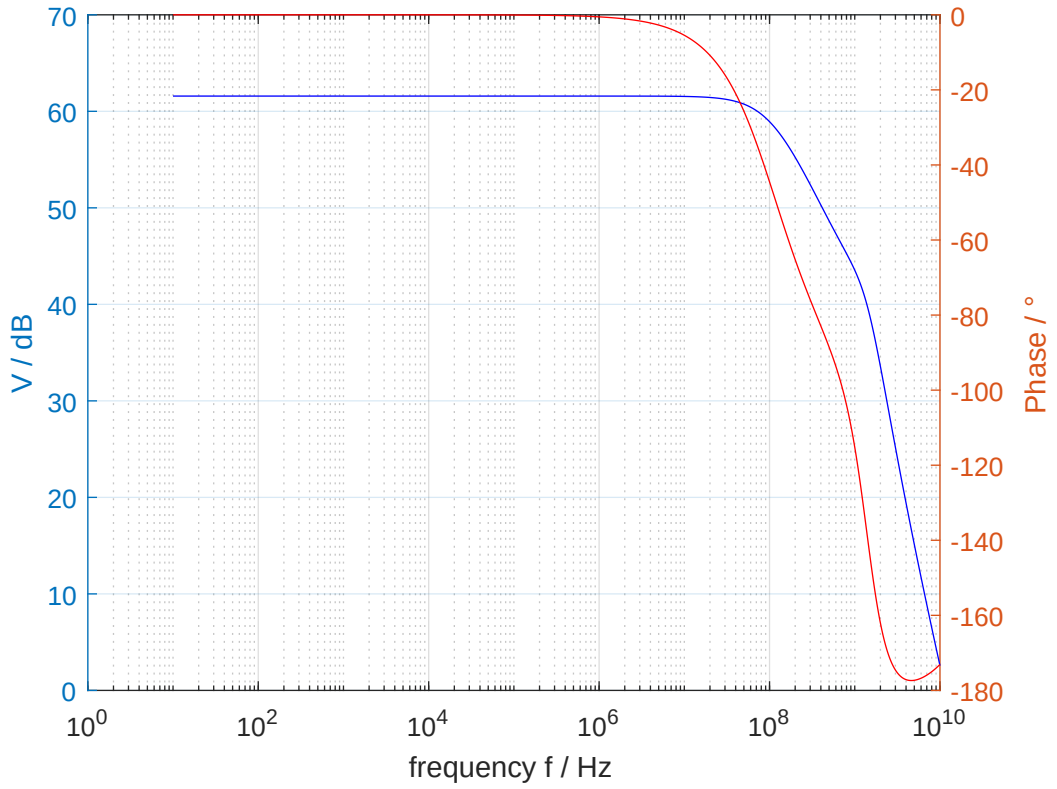

FIGURE 2.18: Closed loop Bode plot of a regulated cascode transimpedance amplifier with current mirrors

The transient response in Figure 2.19 approves stability as no over-/undershoot is observable. There is only the typical process corner case shown, but transient analysis is done for all possible process corners.

The noise behaviour of the proposed TIA is shown in Figure 2.20 which shows a similar order of magnitude compared to the resistor based regultaed cascode stage.

2.2.3.1 Simulated Circuit Performance including Process Corners

Finally the proposed circuit was simulated using corner analysis. All process corners for MOSFETs and resistors are simulated. For all other types of devices the option *typical mean (tm)* is used.

For MOSFET devices the *worst speed (ws)*, *worst power (wp)*, *worst one (wo)*, *worst zero (wz)* and *typical mean (tm)* cases are simulated. For resistors the *worst power (wp)*, *worst speed (ws)* and *typical mean (tm)* are simulated. The temperature ranges from $T = 0\,°\text{C}$ to $T = 80\,°\text{C}$. The supply voltage is set to $V_{DD} = 1.8\,\text{V}$.

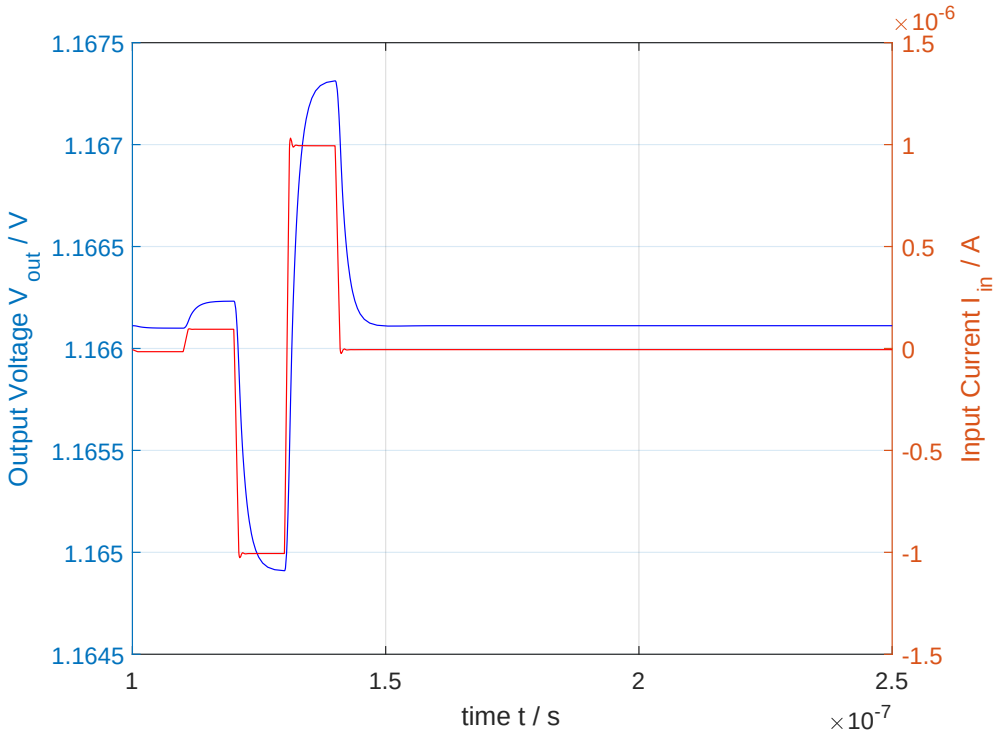

FIGURE 2.19: Transient response of a regulated cascode transimpedance amplifier with current mirrors.

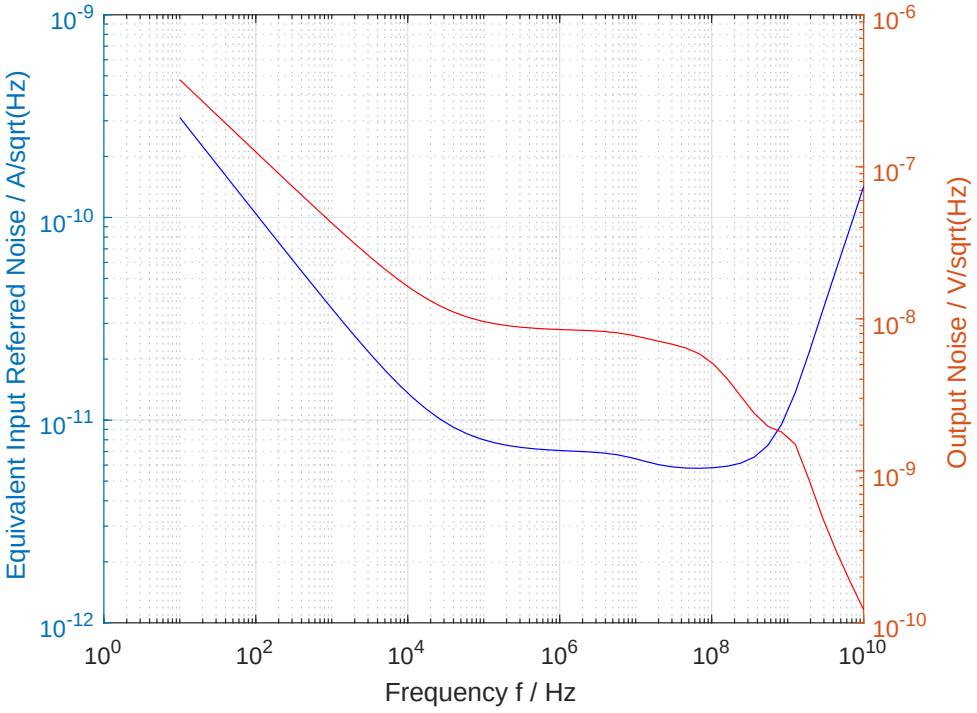

FIGURE 2.20: Noise figure of a regulated cascode transimpedance amplifier with current mirrors.

The results of the performance and some other parameters across these corners are shown in Table 2.9.

In addition to the overall noise analysis shown in Figure 2.20, a more detailed noise analysis is conducted. Table 2.10 shows the noise contribution at the output for different devices at different frequencies. This analysis is helpful to detect the most severe noise sources in the circuit. In this case the most impact on output noise is provided by the lower current mirror MOSFET. The noise contribution of the photodiode is not modelled and simulated. The unit for spot noise is $V/\sqrt{Hz}$, the unit for the integrated noise is V.

TABLE 2.9: Simulated circuit performance of a regulated cascode amplifier circuit with current mirrors, including corner analysis.

Parameter	Symbol	Unit	Min	Typ	Max	Condition/Comment
DC output	V_{outDC}	V	970,9	1166	1306	Iin=0 (Closed Loop)
DC input	V_{inDC}	V	492,5	578,2	638,7	Iin=0 (Closed Loop)
Output upper dynamic voltage	$V_{outDR_{hi}}$	V	1,77		1,78	
Output lower dynamic voltage	$V_{outDR_{lo}}$	V	0,59		0,62	
Input upper dynamic current	$I_{inDR_{hi}}$	µA	234		751	
Input lower dynamic current	$I_{inDR_{lo}}$	µA	-508		-490	
AC closed loop gain	A_{CL}	dB	59,3		64,3	dB[V/A]
AC closed loop 3dB frequency	f_{3dB}	MHz	61,61	112	148	
AC open loop gain	A_{OL}	dB				not applicable
Phase margin	Φ_M	deg				not applicable
Gain bandwidth	GBW	GHzOhm		117,6		
Rise time	t_R	ns		4,1		10n – 100n
Fall time	t_F	ns		3,8		100n – 10n
Input referred noise 100 MHz	i_{eq}	pA/sqrtHz		5,82		
Integrated input referred noise	$i_{eq_{RMS}}$	nA		63,1		1kHz – 112MHz
Power consumption	P	mW		5,8		
Estimated Area	A	μm^2		43700		

2.2.4 Summary of regulated cascode based transimpedance amplifiers

Two different types of inverter based transimpedance amplifiers are reviewed in this thesis. The standard regulated cascode circuit which is biased by resistors shows slightly better performance regarding bandwidth and speed compared to the current mirror based approach. The current mirror version of the regulated cascode transimpedance amplifier uses bigger input transistors, which are also the main reason for the slightly decreased performance. The approach of replacing NMOS input transistors by PMOS transistors to reduce noise failed, as the flicker noise contribution does not play an important role for high bandwidths.

TABLE 2.10: Noise contribution of different devices at different frequencies at a regulated cascode transimpedance amplifier with current mirrors. The unit for spot noise is $V/\sqrt{Hz}$, the unit for the integrated noise is V.

Frequency	device	param	Output Noise Contribution	% of total
100kHz	M14.m1	id	5,17E-09	28,86
	M10.m1	id	4,83E-09	25,25
	R0.r1	rn	4,46E-09	21,5
100MHz	M14.m1	id	3,83E-09	54,78
	R0.r1	rn	3,29E-09	40,39
	M0.m1	id	5,85E-10	1,28
10 - 128M	M14.m1	id	4,83E-05	51,35
	R0.r1	rn	4,16E-05	38,12
	M10.m1	id	1,94E-05	8,3

A regulated cascode TIA with resistive biasing provides good overall performance. The proposed amplifier can reach a bandwidth of up to 128 MHz by providing a gain of 60 dBΩ. The integrated input referred noise level lies at $86,4$ nA for the specified bandwidth.

The regulated cascode TIA biased by current mirrors shows a slightly decreased performance compared to the resistive biased version. The proposed amplifier can reach a bandwidth of up to 112 MHz by providing a gain of 60 dBΩ. The integrated input referred noise level lies at $63,1$ nA for the specified bandwidth.

Chapter 3

Some Comments on Noise of Transimpedance Amplifiers

3.1 Difference between NMOS and PMOS

In Chapter 2 it is attempted to reduce noise of a regulated cascode transimpedance amplifier by changing NMOS input transistors to PMOS.

In fact, as noise is not caused by a single mechanism, several mathematical descriptions are provided for modelling different mechanisms. The white noise part is caused by the resistance of the channel. As the channel is located right below the gate oxide, defects can occur at the silicon-silicon dioxide interface which cause flicker noise.

To directly compare the noise performance of NMOS and PMOS devices, two identical CS-stages, one with a NMOS transistor and the other one with a PMOS transistor are designed. As drain resistance a value of $R_D = 10\,\mathrm{k}\Omega$ is used. At both transistors size is set equally to $W = 20\,\mu\mathrm{m}$ and minimum length of $W = 180\,\mathrm{nm}$.

On the one hand, as it is shown in Figure 3.1, PMOS devices feature about an order of magnitude lower flicker noise than NMOS transistors [11]. On the other hand, for same size transistors NMOS feature a lower channel resistance, thus producing less white noise at higher frequencies.

To obtain similar performance for a PMOS based amplifier compared to a NMOS based amplifier, transistor dimensions at the PMOS based circuit have to be about two to

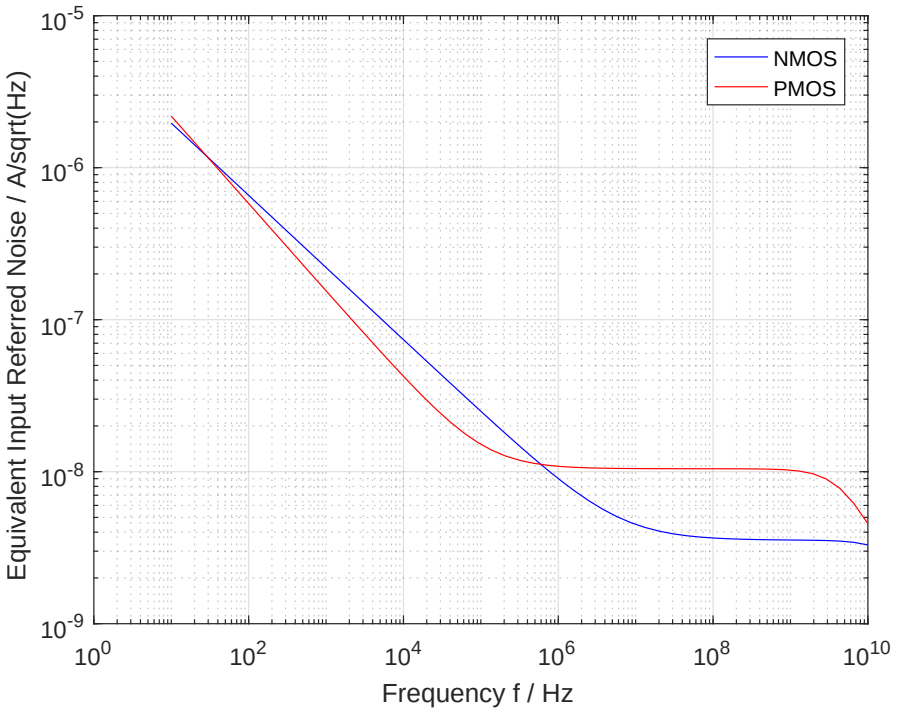

FIGURE 3.1: Comparison of input referred noise behaviour of same sized NMOS and PMOS transistors. The width of both transistors is set to $W = 20\,\mu$m

three times bigger compared to the NMOS version, so that the bias current through the amplifier is similar. To obtain equal current values in both transistors, the width of the PMOS type is set approximately 2.5times as big compared to the NMOS transistors. Considering the difference of noise behaviour for NMOS and PMOS type transistors driving the same current, it is easy to see in Figure 3.2, that the only difference is the magnitude of flicker noise. As the channel resistance has to be equal for both types in this case, both feature an equal magnitude of thermal channel noise.

Even with bigger sized PMOS transistors, at low frequencies noise performance is still better compared to NMOS devices, but the PMOS based regulated cascode transimpedance amplifier does not show perceptible improved noise performance compared to its equivalent NMOS version. The cause for this observation lies in the distorting representation of the noise behaviour by using a logarithmic x-axis. As the corner frequency between flicker noise and thermal channel noise is at least one order of magnitude lower than the bandwidth of the amplifier, the better flicker noise performance of PMOS transistors is negligible when considering the integrated noise over the whole bandwidth.

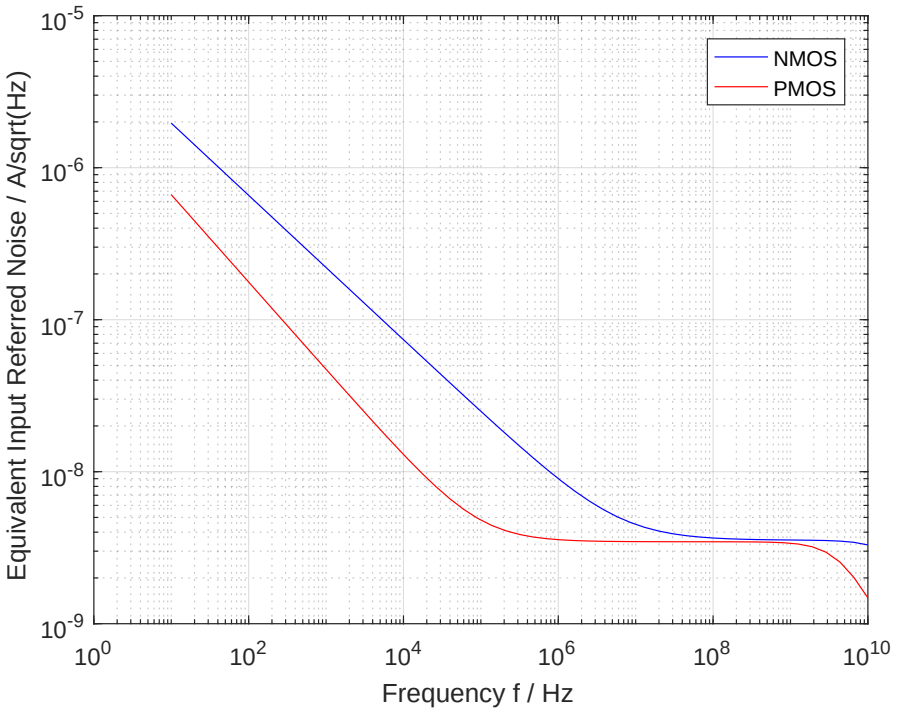

FIGURE 3.2: Comparison of input referred noise behaviour for NMOS and PMOS devices driving the same current.

3.2 Noise behaviour in dependence of bias current

The second approach in reducing noise is by providing higher bias currents. Figure 3.3 shows the dependence of equivalent input noise with respect to transistor with, and as a matter of fact also in dependence on drain current.

3.3 Conclusion

As shown in this chapter, PMOS only provides advantages compared NMOS in the lower frequency regions. For higher bandwidth applications the only methodology beside chosing an appropriate circuit topology for the specific application and increasing the channel length of transistors, is to increase bias currents. By variation of bias currents noise behaviour of MOSFETS can be controlled quite nicely, allthough one has to have in mind, that higher bias currents lead to bigger transistors, which in fact provide higher parasitic devices such as gate-source capacitances. The parasitics however can limit other design properties such as bandwidth. There will be always a tradeoff between

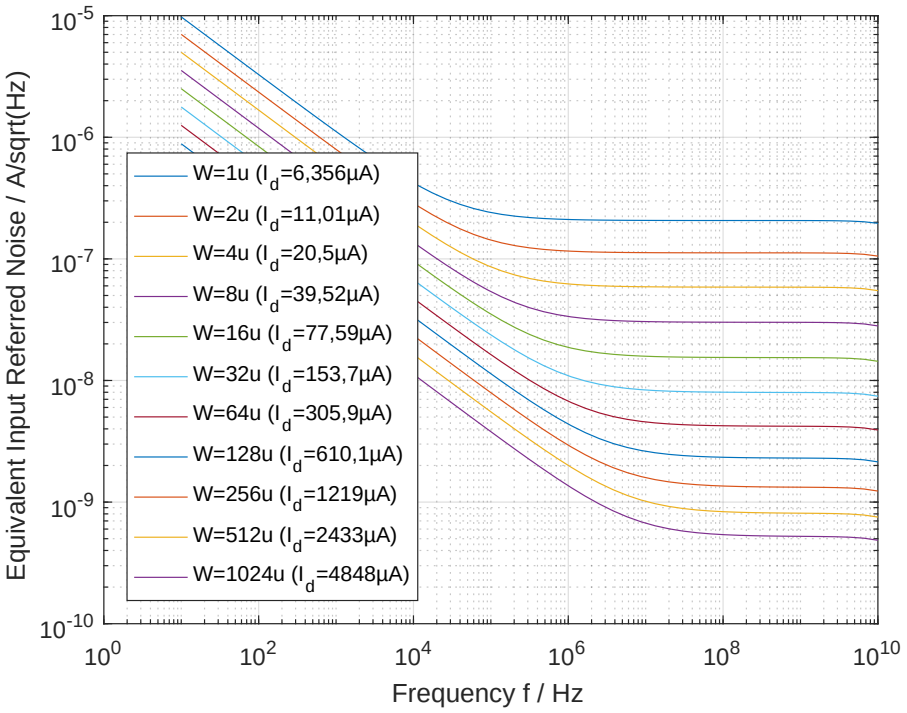

FIGURE 3.3: Comparison of input referred noise behaviour for different sized NMOS transistors and different currents. The gate voltage V_G is kept constant.

gain, bandwidth and noise. In this thesis, the influence of the input capacitance on the overall noise behaviour is not investigated.

Chapter 4

Variable Gain Amplifier

4.1 Adjustable Gain Amplifier

The goal of this approach is to extend the measurement range of previously proposed transimpedance amplifiers. Variable gain amplifiers play an important role in fibre optic communications as they have to deal with very weak signals on the one hand, and at shorter link distances with strong signals on the other hand. The control circuit which adapts the gain at the amplifier corresponding to signal strength is called automatic gain control [12]. Usually an automatic gain control consists of a peak detector and a so called linear-to-dB converter, which is then responsible for providing an appropriate control voltage for the adjustable feedback network at the amplifier [13]. The goal of an amplifier with AGC is to use the full dynamic range of the output. [14] [15]

As this thesis deals with measurement amplifiers, the conventional approach for designing an adjustable gain amplifier is not suitable, since defined gain is immanent for proper measurements and device characterization.The toplevel circuit diagram of the adjustable gain amplifier is shown in Figure 4.2.

This approach uses a comparator at the output of feedback TIA. The comparator ensures, that the gain of the transimpedance amplifier gets reduced, as soon as the output signal of the amplifier reaches its dynamic range limits.

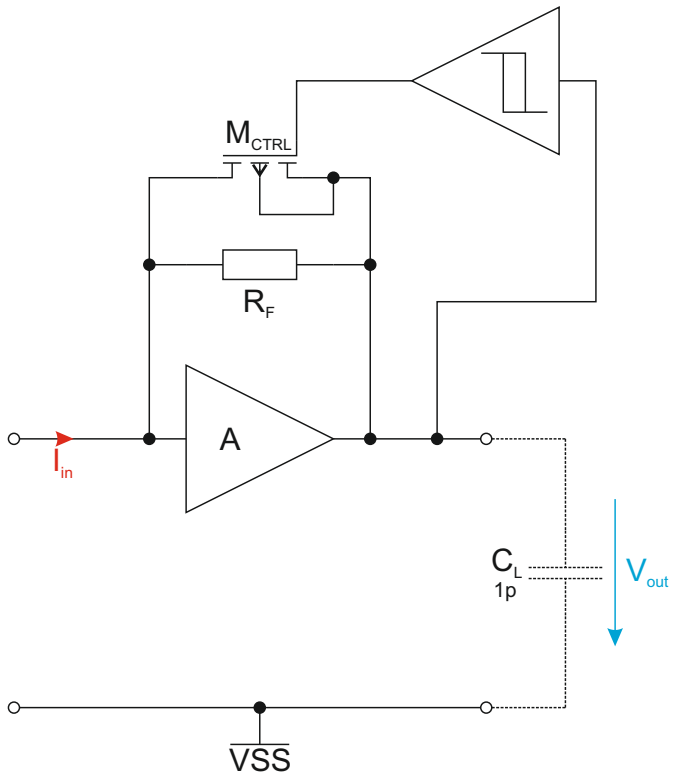

FIGURE 4.1: Toplevel circuit diagram of the proposed adjustable gain amplifier consisting of a conventional transimpedance amplifier, a comparator and an adjustable feedback network.

Figure 4.2 shows the added bypass transistor to the conventional feedback of a single stage push-pull inverter based TIA. The Control input of the bypass transistor V_{CTRL} is connected via a simple inverter to the comparator shown in Figure 4.3.

As supply voltage $V_{DD} = 1.8\,\mathrm{V}$ are used.

The comparator is designed to meet the criteria to provide fast enough switching of the adjustable gain. A small hysteresis is added to the comparator by using a resistive positive feedback.

Figure 4.4 shows the bode plot of the proposed adjustable TIA in open loop and in closed loop configuration with different gain values. The gain difference of the two gain steps has been adjusted to $\Delta A = 10\,\mathrm{dB}$.

In Figure 4.5 the response of the proposed circuit for high swing signals is shown. The settling time in case of a gain jump is less than $t_s \leq 5\,\mathrm{ns}$ and therefore fulfils the speed criteria.

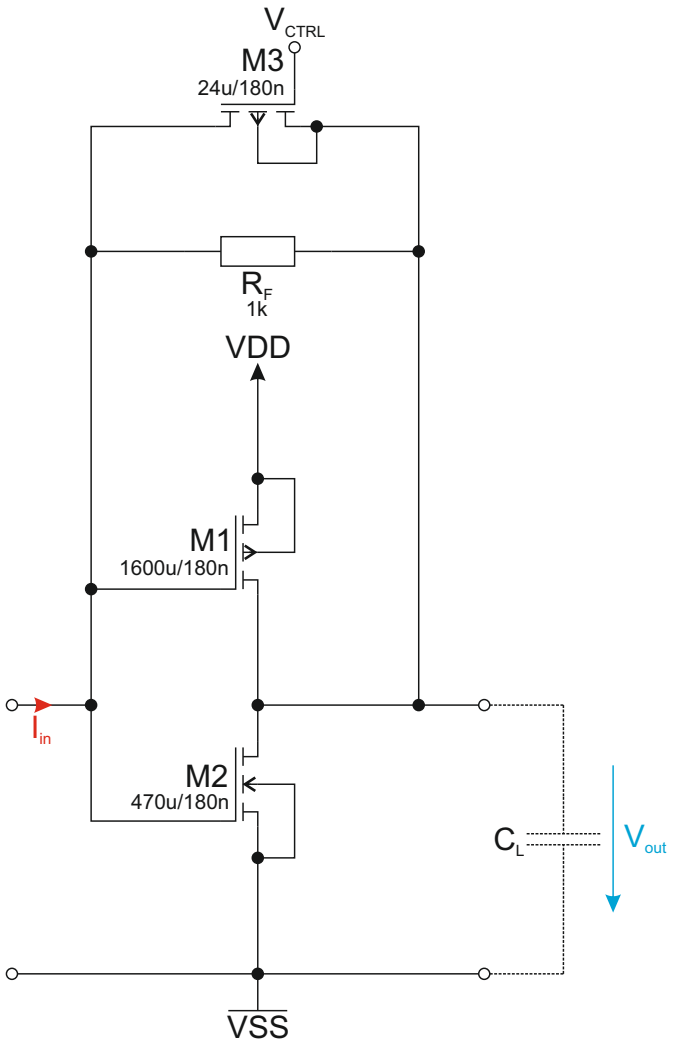

FIGURE 4.2: Dimensioning of 2 step automatic gain TIA.

Figure 4.6 shows noise performance of the TIA for the two different gain values. As the gain of the amplifier is decreased, the input referred noise for the lower gain value is worse.

4.1.1 Conclusion

It is shown, that it is possible to create an adjustable gain amplifier which is capable of changing the gain within one measurement period. The adjustable dynamic range is $\Delta A = 10\,\mathrm{dB}$. Further gain steps could be introduced by inserting more feedback transistors in parallel where each transistor is controlled by an appropriate comparator.

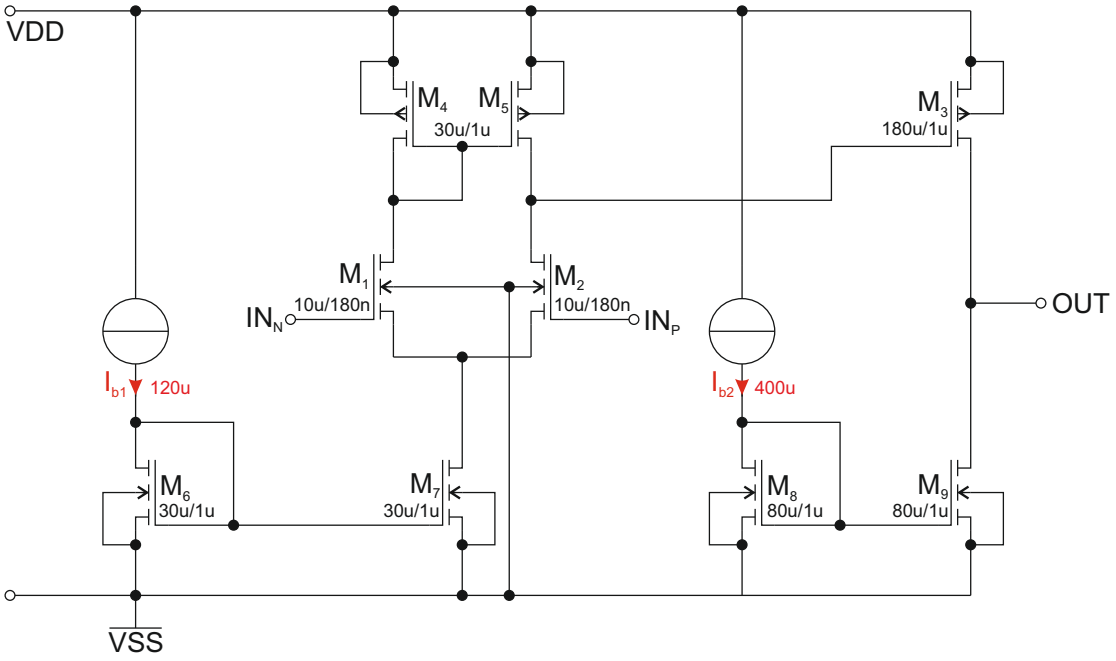

FIGURE 4.3: Dimensioning of a comparator.

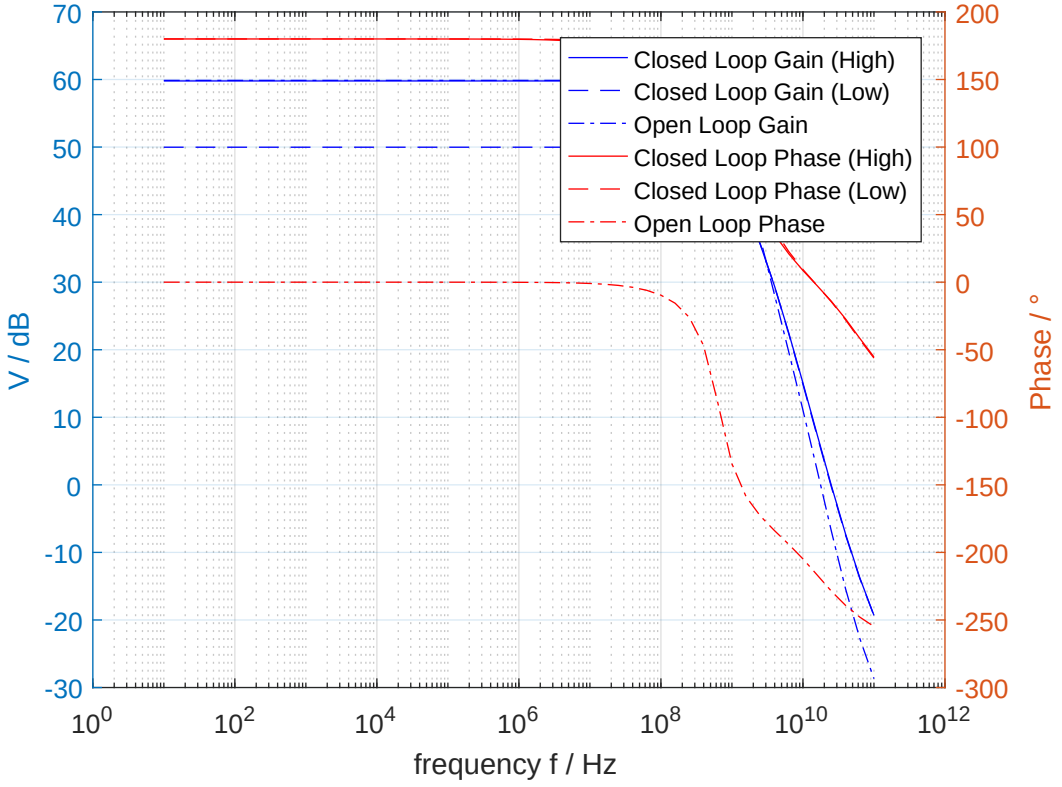

FIGURE 4.4: Bode plot of a 2 step variable gain amplifier

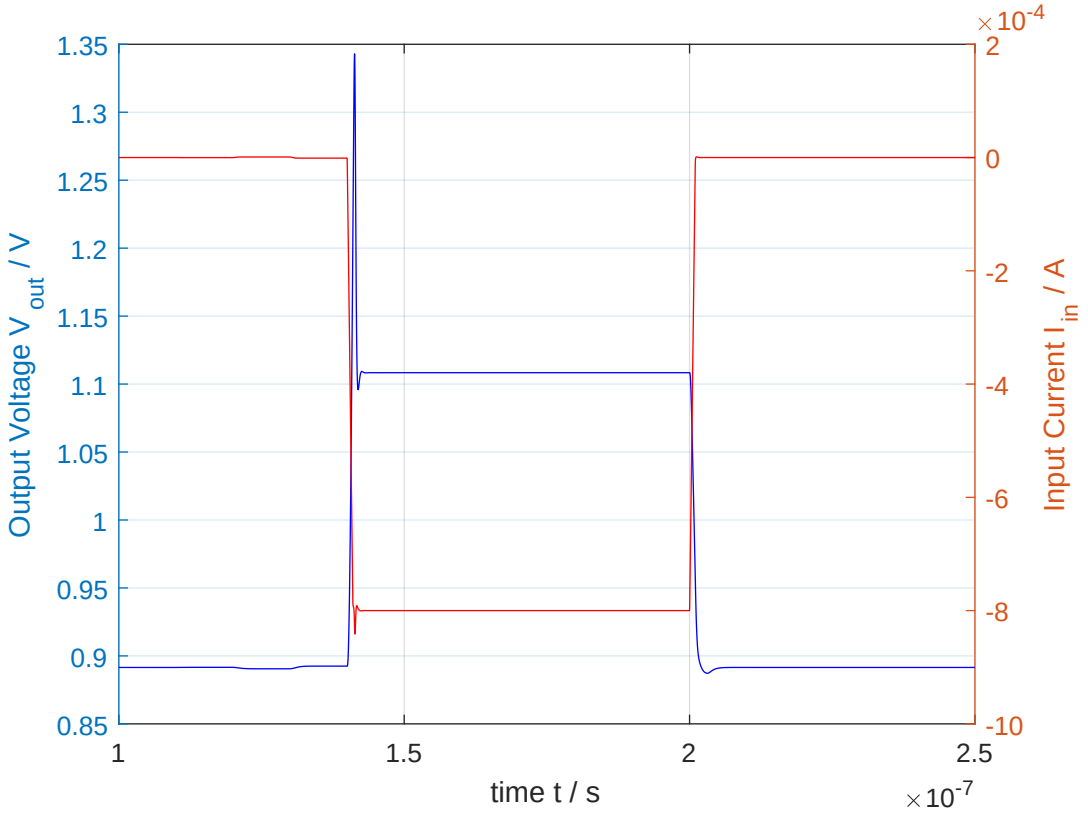

FIGURE 4.5: Transient response a 2 step variable gain amplifier

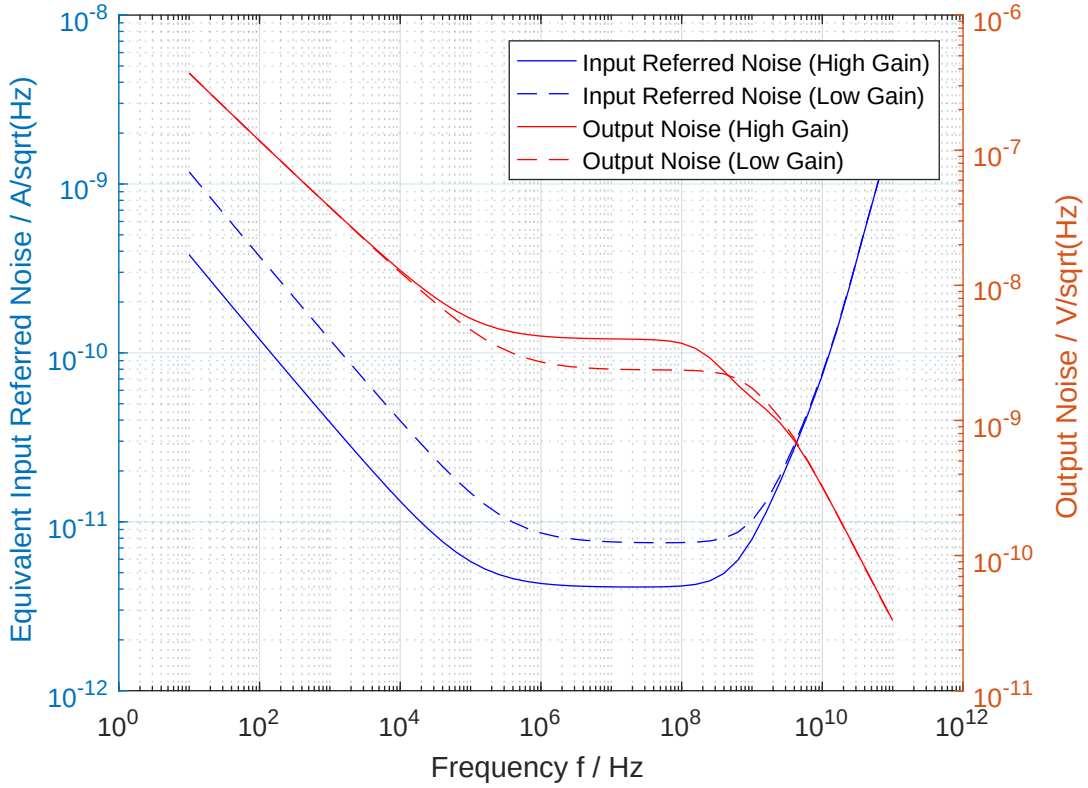

FIGURE 4.6: Noise response of a 2 step variable gain amplifier

Chapter 5

Results, Discussion and Outlook

5.1 Results and Conclusion

Photodiode amplifiers play an important role in a vast number of applications. In particular for the field of fibre optic communications more powerful, thus faster and lower noise transimpedance amplifiers are needed. By dealing with data rates of 400 GBit/s over a single fibre, characterization of photodiodes plays a very important role.

In this thesis five different topologies for photodiode amplifiers are reviewed. Starting with a very basic inverter based topology, the properties of transimpedance amplifiers are investigated. As discussed in Chapter 2 a single stage push-pull inverter transimpedance amplifier can reach a bandwidth of up to 250 MHz by providing a gain of 60 dBΩ. The integrated input referred noise level lies at $66,42$ nA for the specified bandwidth.

The performance of a single stage push-pull inverter transimpedance amplifier can be further improved by extending it with a cascode circuit. The improved amplifier can reach a bandwidth of up to 791 MHz by providing a gain of 60 dBΩ. The integrated input referred noise level lies at $135,42$ nA for the specified bandwidth.

It turned out, that a three stage push-pull inverter transimpedance amplifier is not suitable for the purpose of photodiode characterization, as its stability is highly dependent on input and output configuration.

The disadvantages of all single stage inverter based transimpedance amplifiers is their high power consumption.

A completely different approach represents the regulated cascode topology. A standard regulated cascode transimpedance amplifier with resistive biasing features a bandwidth of 128 MHz and a gain of about 60 dBΩ. The integrated input referred noise level lies at 86, 4 nA for the specified bandwidth.

The current mirror based approach of a regulated cascode transimpedance amplifier does not provide the intended improvement of stability for process variations and as it also features worse performance regarding bandwidth of 128 MHz compared to the standard regulated cascode amplifier it is not further considered.

Chapter 4 shows the feasibility of a controlled gain amplifier for measurement purposes. The actual design is able to switch gain between 50 dBΩ and 60 dBΩ without compromising a further processing in speed, as the settling time lies below 5 ns.

The desired performance for detecting 10 nA pulses with a period of 20 ns is not reached in this thesis, though achieved performance is in accordance with literature research, one has to accept that especially regarding noise, this is the maximum performance achievable with this kind of semiconductor process. By using smaller process nodes, the noise contribution of the transistors can be further decreased. Additionally the performance could be increased by obtaining better $\frac{W}{L}$ ratios, while still keeping parasitic capacitances low. For smaller process nodes also the maximum supply voltage is decreased, but with the controlled gain amplifier approach, the issue of decreasing dynamic ranges can be mitigated.

5.2 Outlook

The semiconductor process chosen for this thesis is a conventional 180 nm silicon based process. Performance of proposed circuits could be dramatically improved by switching to a smaller process node. Also using specialized devices, for instance low noise transistors or isolated transistors which are only available with expensive process options, could further improve performance of the amplifiers.

The basic concept of the controllable gain amplifier can be extended to more gain steps to further increase dynamic range or simply provide finer steps. In this case a control logic would be necessary to provide proper gain to optimize the output swing.

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