Michael Kalcher, Dipl.-Ing., BSc

Fully Integrated Mixed-Signal RF-Domain Transmitter-Induced Self-Interference Cancellation for Advanced Wireless Cellular Mobile Transceivers

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AFFIDAVIT

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Michael Kalcher

Abstract

Mobile cellular data traffic has continuously grown exponentially for the past decade with no end in sight, mainly driven by users' increasing demand for video streaming. This fuels technological advances, e.g. certain aspects of the upcoming 5G standard, since the available RF spectrum for data transmission is restricted by regulations and physical limits.

A key 5G candidate technology to significantly increase spectral efficiency is in-band full duplex, where transmission and reception of signals simultaneously occur on an overlapping band of frequency; the known transmit signal completely blocks the receive unit without any further measures. The technology to enable in-band full duplex is self-interference cancellation (SIC). Furthermore, data throughput in existing 4G cellular systems with multiple aggregated carriers benefits from SIC: The fixed frequency separation of up- and downlink channels and fragmented spectrum allocation for cellular operators creates challenging transmitter-induced self-interference scenarios.

Analysis of the state-of-the-art reveals that most existing SIC systems are either fully digital or analog/RF systems, incapable of simultaneously exploiting the benefits of RF-domain cancellation and digital signal processing. Fundamental investigations led to a novel hybrid SIC solution, a fully integrated RF-domain mixed-signal approach, presented in this work. The cancellation signal is generated digitally, benefiting from the flexibility of digital signal processing. A radio-frequency digital-to-analog converter (RF-DAC), specially designed for this application, is used to directly convert the digital signal into the RF-domain, where it is directly injected into the receiver, canceling the transmitter-induced self-interference and restoring receive performance.

Based on this new SIC topology, an integrated CMOS demonstrator is developed and scientifically investigated. To demonstrate the feasibility of the ap-

proach, the mixed-signal RF-domain SIC system operates from 1.4 to 2.7 GHz covering the mid and high frequency 4G and 5G new radio frequency bands.

Furthermore, a novel quadrature and multiphase local oscillator (LO) generator circuit architecture is introduced, saving power in LO distribution. It is intended to be used as the quadrature LO source for the developed cancellation RF-DAC, but can also be directly employed in other applications. Based on the new topology, two prototype circuits are designed, a differential quadrature and a differential 120° three phase generator. The circuit architecture is scientifically investigated with simulations and measurements.

The proposed SIC method is scientifically evaluated and its feasibility, by means of the developed prototype, is demonstrated with comprehensive post-layout circuit level simulations. The SIC system achieves a cancellation performance better than 25 dB over a variety of analyzed self-interference scenarios, targeting high transmit and receive bandwidths exceeding 100 MHz. Furthermore, the proposed system allows the receiver to recover from saturation up to peak interference powers of −20 dBm. The achieved performance, which can be further enhanced with more sophisticated cancellation signal processing, demonstrates the feasibility of the proposed mixed-signal RF-domain approach.

The developed system and its demonstrated performance, besides being a key component for in-band full duplex, can enhance data throughput in existing 4G. Carrier aggregation scenarios which are limited by transmitter-induced self-interference, can be enabled with the proposed, scientifically analyzed, and implemented approach. The enhancements are especially beneficial where high transmit powers are required, i.e. at enclosed locations or far away from base stations.

Contents

1 Introduction

In recent years, the total global data traffic experienced exponential growth. According to Cisco [1], the total global traffic exceeded 150 EB per month in 2018, where approximately 20 EB per month are attributed to mobile (cellular) traffic. Similarly, Ericsson [2] claims exponential growth for mobile data traffic, reaching 20 EB per month in 2018 and exceeding 100 EB per month by 2022. Cisco, while predicting more conservative 77 EB per month in 2022, also forecasts exponential growth for mobile data traffic. Compound annual growth rates (CAGRs) exceeded 50 % in the past and are expected to further grow.

Increasing (wireless) data traffic is caused mainly by two technologically driven developments: First, cellular communication providers create new business models, e.g. by offering broadband fixed wireless access (FWA) or connectivity for internet of things (IoT) [3], [4]. Second, customers' demand for video streams significantly drives wireless and cellular data traffic. Technology-wise, this growth in data traffic fuels all further development, since all wireless radio communications operate on the limited resource of usable radio-frequency (RF) spectrum.

A key fifth generation (5G) candidate technology to significantly increase spectral efficiency is in-band full duplex (FD), where transmission and reception of signals simultaneously occurs on the same or an overlapping band of frequency [5], [6]. While there are many challenges to be solved to allow practical commercialization of in-band FD, existing cellular systems face spectral inefficiencies: The relatively inflexible frequency separation of transmitted and received signals and fragmented spectra allocated to the individual operators [7] further complicate or completely render efficient spectrum usage impossible. The crucial effect is transmitter (TX) induced self-interference (SI), which desensitizes reception or, in the case of in-band FD, (completely)

masks the received signals. A detailed problem description is provided in Chapter 2.

The key technology to counter these issues, as well as to enable in-band FD, is self-interference cancellation (SIC) [6]. Several SIC systems have been published so far, mostly either being fully digital or entirely analog systems. Fully digital approaches perform calculation of the cancellation signal as well as the cancellation itself in the digital domain, being unable to restore receiver (RX) performance in case of nonlinear operation, e.g. saturation or clipping. Analog/RF domain solutions perform cancellation and generate the required signals in an analog fashion, which makes it impossible to exploit the benefits of digital signal processing (DSP), amidst other drawbacks. Chapter 3 focuses on published and state-of-the-art SIC approaches with an emphasis on integrated circuit design.

A hybrid solution, generating the cancellation signal digitally, converting it to analog and performing the cancellation in the RF domain was presented by Schacherbauer *et al.* in 2000 [8]. Using a discrete prototype composed from off-the-shelve components, Schacherbauer *et al.* demonstrated the principal operation of such a system. Due to the high overhead and some non-optimal design choices, the attractiveness of this system suffered, as well as being a discrete prototype.

This work presents and investigates a novel hybrid SIC solution, a fully integrated RF-domain mixed-signal approach, greatly extending the previous approach. The cancellation signal is generated digitally, exploiting all the benefits of DSP. A specialized radio-frequency digital-to-analog converter (RF-DAC) is used to directly convert the digital signal into the RF domain, where it is directly injected into the RX, canceling the SI and restoring RX performance. Scientific analyses and further considerations on system level of the developed approach are summarized in Chapter 4.

Within this work, to show the presented approach's feasibility, an integrated complementary metal-oxide-semiconductor (CMOS) demonstrator is developed. The system implements the proposed mixed-signal RF domain SIC approach, operating from 1.4 GHz to 2.7 GHz covering the mid and high Long-Term Evolution (LTE) and 5G new radio (5G-NR) frequency bands. Chapter 6 details the integrated circuit design of the dedicated cancellation RF-DAC and the SIC augmented RX.

Furthermore, a novel quadrature and multiphase local oscillator (LO) and/or clock generator circuit architecture is developed. It is intended to be used as the LO source for the developed cancellation RF-DAC, but can also be directly adopted for use in other applications. The circuit architecture is thoroughly detailed and investigated in Chapter 5. Two prototypes are developed, implementing a differential quadrature and a differential 120° three phase generator.

1.1 Thesis Organization

This thesis is structured as follows: Chapter 2 further details the effect and workings of TX induced SI. Chapter 3 provides a comprehensive review of published (circuit design oriented) SIC solutions. System-level considerations and aspects of the developed SIC approach are detailed in Chapter 4. The quadrature and multiphase LO circuit architecture and implementations are covered in Chapter 5. Circuit design and simulation results of the cancellation augmented RX and the cancellation RF-DAC and necessary auxiliary circuitry are detailed in Chapter 6. Finally, Chapter 7 concludes this work and provides an outlook on future research activities.

2 Transmitter-Induced Self-Interference

The phenomenon of transmitter-induced SI or alternatively TX-leakage has drawn the attention of RF engineers mainly due to two rather recent developments in mobile handsets.

First, the demand for cheaper, smaller and more flexible hand-held devices resulted in TX and RX architectures featuring less passive components with each generation. This trend is additionally accelerated by the digitization of as much RF functionality as possible, and the increased spectral flexibility required to support all the latest wireless communication standards [9].

Figure 2.1 shows a conventional direct-conversion transceiver (TRX) setup, providing filtering in the RF domain and in baseband [10]. Modern direct modulation (cf. Figure 2.2) TRXs try to avoid as many passive components as possible, exploiting technology scaling and digital signal processing, and employing filters only when absolutely necessary.

The remaining distinct passive component in a TX-RX shared antenna system, commonly used in modern cellular phones, is the so called duplexer [11]. It decouples the RX from the TX. Such devices function similarly to circulators, but utilize the frequency separation of frequency division duplex (FDD) operation, achieving improved TX-to-RX isolation. Unfortunately, these components are generally fixed in operating frequencies, usually several of them are required for multi-band operation. They account for a big portion of a phone's RF system's cost, while providing only limited TX-to-RX isolation. These factors make manufacturers want to eliminate duplexers from their designs or replace them with cheaper components providing even less isolation. Similarly, systems having no duplexer but dedicated RX and

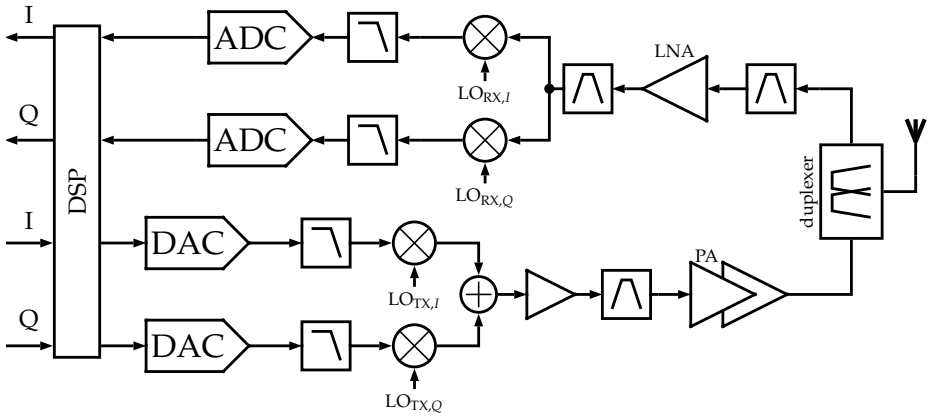


Figure 2.1: Conventional direct-conversion TRX architecture.

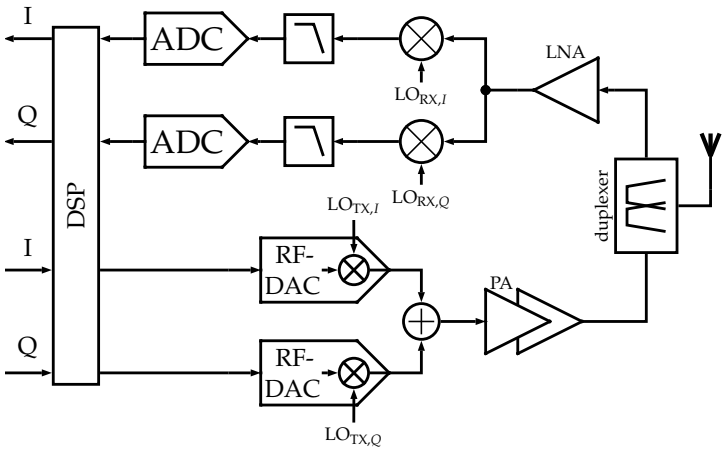


Figure 2.2: Modern digital-intensive direct-modulation TRX architecture.

TX antennas equally suffer from limited TX-to-RX isolation, on top of the space and component overhead of two distinct antennas.

The reduced spectral selectivity in the RX caused by the omission of passive filtering increases the susceptibility to any interfering signals. The TRX's own transmitted signal leaking via the non-ideal isolation of the duplexers is especially critical due to the high transmit power required. This potentially strong interfering signal can drive the RX into non-linear operation regimes,

such as saturation or even clipping, therefore severely degrading the RX's performance.

Second, several technologies and techniques [12], [13] have been proposed to achieve the targets [4], [14], [15] of the upcoming 5G wireless communication standards. One of the candidate technologies is FD [16]–[18], where transmission and reception simultaneously occur in the same or an overlapping band of frequency. Advances in CMOS technology and signal processing enabled researchers to break the general consensus that FD communication is impossible [19, Chapter 14]. This technique potentially allows for doubled spectral performance of wireless communication systems and eases frequency planning.

Obviously, as the TX and RX are operating simultaneously on equal bands of frequency, due to non-ideal isolation, the transmitted signal directly masks the received signal. This is also true for low transmit powers, as there is no frequency separation compared to FDD systems.

Relaxing the requirements on isolation between the TX and RX paths in FDD TRX without adding additional filtering, as well as enabling FD communications, are made possible by utilizing knowledge of the TRX's own transmit signal. The harmful self-interference is canceled and eliminated in the RX.

2.1 Frequency Division Duplex Systems

Modern multi-mode hand held phones support a variety of (legacy) wireless cellular standards and bands, ranging from Global System for Mobile Communications (GSM) to LTE. Many of these bands are operated in FDD, where transmission and reception is occurring simultaneously but on different bands of frequency [20, Chapter 19].

Due to nonideal components a portion of the transmitted signal is leaking into a simultaneously active RX: Either the dedicated RX antenna receives the (attenuated) TX signal, or in the shared antenna case the duplexer, which decouples the RX from the TX, provides only limited isolation, as sketched in Figure 2.3.

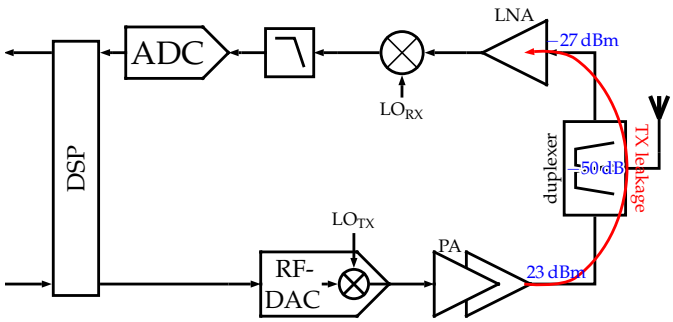


Figure 2.3: Transmitter leakage in modern digital-intensive direct-modulation TRX (simplified architecture).

Even though the TX and RX operate in distinct bands of frequencies, the residual leaked signal can be substantial and heavily impair the RX performance. Also, the duplex spacing, i.e. the frequency separation between the uplink (UL) and downlink (DL) channels, is rather small, generally only $4 \sim 5\,\%$ of the mean UL and DL frequencies, and as low as 10 MHz in the worst case. This phenomenon is further aggravated by the omission of frequency selective components in the RX and TX paths.

Practical high-performance duplexers are usually limited to approximately 50 dB TX-to-RX isolation subject to dynamic variations caused by changes in temperature and especially antenna impedance [21]. To put this figure into context, consider the maximum transmit power of handsets defined by the LTE standard of 23 dBm at the antenna [20], [22]. Assuming 50 dB of attenuation, the resulting leakage signal has a power of -27 dBm (2 µW) at the RX's input. The RX's sensitivity level[1], which varies with band and signal bandwidth, is always below -90 dBm (1 pW) [22]. Comparing this value to leaked signal power reveals a difference greater than six orders of magnitude, which can easily cause non-linear operation of the receiver, e.g. saturation or even clipping effects.

Such a scenario is sketched in Figure 2.4. The RX input signal is the sum of the weak desired signal at frequency f_{RX} and the self-interference portion

[1]The sensitivity level defines minimum signal power level the receiver must be able to correctly receive, essentially specifying the required noise performance.

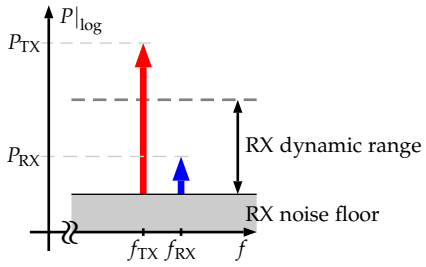


Figure 2.4: RX signal powers in the self-interference case.

at frequency f_{TX}. If the signal power exceeds the RX's dynamic range (DR), non-linear clipping occurs rendering correct signal reception impossible.

In case the TX is operated in back-off, alas below its maximum power, and the received signal power is well above the sensitivity limit, the leaked signal (even when within the RX's DR, cf. Figure 2.4) can still cause performance degradations in the RX due to the low duplex distances and non-idealities in the RX, e.g. non-linearities, spurious tones on the LO etc.

A prominent example is the second-order intermodulation distortion (IMD2) caused by the non-linearities of the RX components [23]. A portion of the leakage is converted to undesired signal components around 0 Hz, i.e. falling into the baseband (BB) of direct conversion RXs. Hence, the received signal is corrupted with these second-order components.

Furthermore, the leaked signal, although centered around the TX frequency, can be directly downconverted into baseband corrupting the actual DL signal [24] by spurious and intermodulation tones on the LO.

This aforementioned effect is further aggravated by carrier aggregation (CA) introduced in LTE. In order to increase data rates, signal bandwidths need to be increased. In the LTE standard, the maximum signal bandwidth per RF carrier is limited to 20 MHz [20], [22]. To increase the effective bandwidth, several such carriers are aggregated to form a virtual signal band that exceeds this 20 MHz limit achieving peak data rates exceeding 1 Gb/s [25]–[27].

The LTE defines three possible CA scenarios [25]–[27] to accommodate the fragmented spectrum of wireless cellular operators [7]:

- **Intra-band CA**: Two or more RF carriers of potentially different bandwidths are combined in the same frequency band, forming either a contiguous signal band as sketched in Figure 2.5a, or a non-contiguous frequency band of virtual higher bandwidth sketched in Figure 2.5b.
- **Inter-band CA**: Two or more carriers are combined in different frequency bands, forming a virtual band as sketched in Figure 2.5c.
- **Any combination**: Currently, the LTE standards allows for combining up to five RF carriers. This can include inter- as well as intra-band and contiguous and non-contiguous CA. Figure 2.5d shows an example.

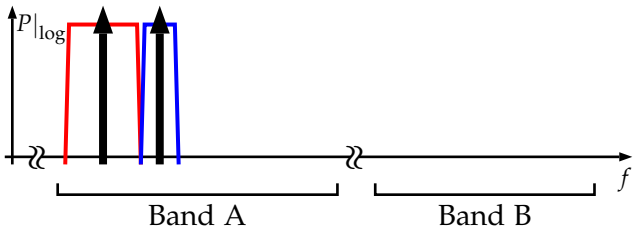
Any of these CA combinations increase the available signal bandwidth ultimately increasing data throughput. From an RF perspective, the intra-band contiguous case is potentially the easiest to handle: If the total continuous bandwidth does not exceed the RX's or TX's analog and signal processing bandwidths, virtually no or little modifications in RF circuitry are required, e.g. progressing from a maximum bandwidth of 20 MHz towards 40 MHz in the case of 2× contiguous CA.

For the non-contiguous and inter-band CA cases most probably several TXs and RXs are required featuring their own LOs as sketched in Figure 2.6 for a 2× DL-CA scenario. Due to non-ideal isolation and crosstalk between these simultaneously active LOs, additional spurious and intermodulation tones are present, some of them falling close to the transmit frequency (or frequencies) [24], [28]–[30]. This phenomenon aggravates the previously mentioned effect of downconverting the leakage signal from the TX into the received baseband.

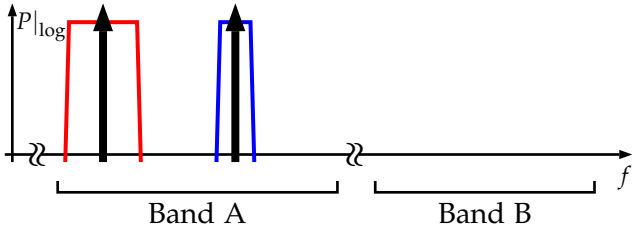
Due to the coupling between the different LO signals, intermodulation spurious tones are generated from the harmonics of the LOs with frequencies

$$f_{\text{spur},mn} = m \cdot f_{\text{RX},1} + n \cdot f_{\text{RX},2} \tag{2.1}$$

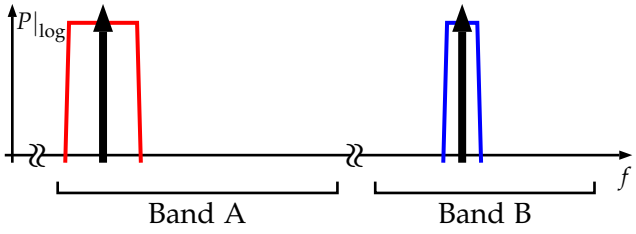
where $m, n \in \mathbb{Z}$ for the case of two simultaneously active RX paths. As an example assume the combination of LTE bands 5 and 7, where the band 5 UL frequency is $f_{\text{TX}} = 832\,\text{MHz}$ and the aggregated DL bands are located at $f_{\text{RX},1} = 877\,\text{MHz}$ and $f_{\text{RX},2} = 2675\,\text{MHz}$ for band 5 and 7 respectively. Due to this coupling mechanism of the RX-LOs, several intermodulation tones are generated: The combination of $m = 4$ and $n = -1$ results in $f_{\text{spur}} = 833\,\text{MHz}$, which is only 1 MHz away from the TX frequency f_{TX}. If this spur



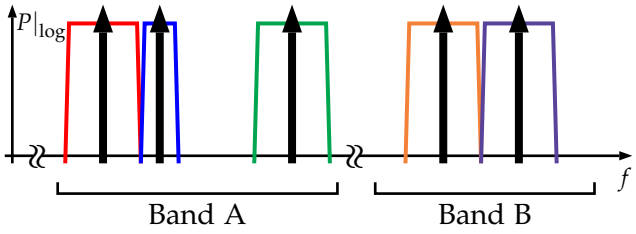
(a) Contiguous intra-band CA.



(b) Non-contiguous intra-band CA.



(c) Interband-band CA.



(d) Combination of different CA modes.

Figure 2.5: Exemplary LTE CA scenarios.

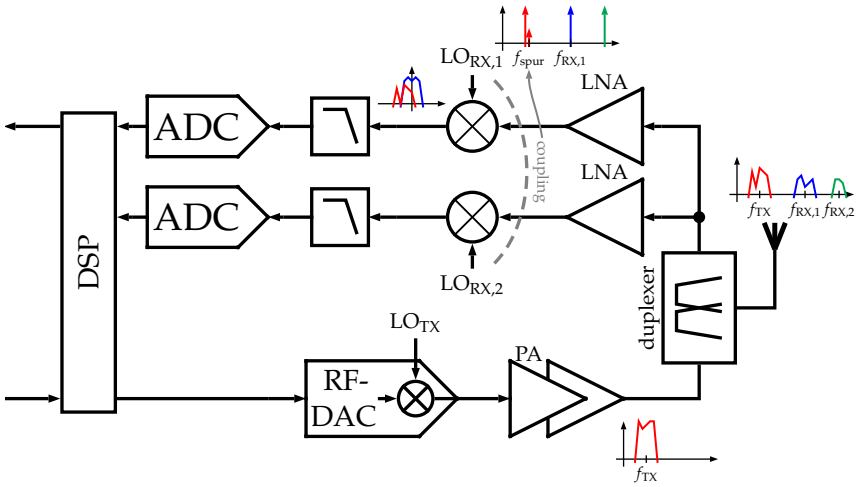


Figure 2.6: Transmitter leakage in LTE CA TRX with two dedicated receive paths for 2× CA in DL (simplified architecture).

is prominent, a substantial portion of the leaked TX signal, centered around f_{TX}, is downconverted into the first RX baseband due to this intermodulation tone, impairing the received signal as sketched in Figure 2.6.

There are yet other transmitter-induced SI effects present in conjunction with CA. First, with several CA combinations a harmonic (e.g. second or third) of the UL signal directly falls into a paired DL band [31]. E.g. the third UL harmonic of band 17 (ranging from 704 MHz to 716 MHz, i.e. the harmonic potentially lies between 2112 MHz and 2148 MHz) directly falls into the associated DL of band 4 ranging from 2110 MHz to 2155 MHz, potentially degrading signal reception.

Second, in non-contiguous CA modes additional intermodulation effects can cause undesired signal components again falling into the RX band [32]. Assuming inter-band CA of bands 1 and 3 with TX frequencies of $f_{TX,1} = 1950\,\text{MHz}$ and $f_{TX,2} = 1750\,\text{MHz}$ respectively, several intermodulation products will appear. One such undesired distortion is the third-order intermodulation (IM3) component at $f_{IM3} = 2 \cdot f_{TX,1} - f_{TX,2} = 2150\,\text{MHz}$. This component directly falls into the RX frequency region from 2110 MHz to 2170 MHz of band 1.

A possibility to overcome these self-interference issues is increasing the effective isolation of the TX to the RX. The readily available TX (baseband) data, which defines the transmitted and therefore interfering signal, can be utilized to recreate the interference. This copy can then be used to cancel out the actual interference seen in the RX effectively increasing the TX-to-RX isolation. A review of published SIC systems for FDD applications is provided in Section 3.1.

2.2 In-Band Full Duplex Systems

In in-band FD systems transmission and reception of signals simultaneously occurs on the same or an overlapping band of frequency [5], [6]. Obviously the strongest interferer is the TRX's own TX without any frequency separation and directly impairing the received signal quality.

Assuming practical transmission powers in the ballpark of 20 dBm and sensitivity levels well below -90 dBm, which is true for Wi-Fi and LTE, the isolation requirement easily exceeds 110 dB [33]. Without sophisticated means of interference cancellation such isolation values are impossible to achieve.

An overview of published SIC approaches and solutions is provided in Section 3.2. The challenge not only lies in the tremendous power difference between RX and TX signals, but also in the composition of the SI signal. There are generally three categories these contributions can be classified into [33]:

- **Linear components**: Linearly weighted attenuated and delayed signal components e.g. from echoes and reflections. These should make up for the most part of the SI.
- **Nonlinear components**: Contrary to the linear SI portions, nonlinearities introduce signal components at frequencies different from the undistorted signal. A prominent example usually is the power amplifier in the TX path, which is a source of harmonics and spectral regrowth, e.g. in the adjacent channel leakage ratio (ACLR) region.
- **TX noise**: Noise from the TX becomes non-negligible due to the high power difference and must also be taken care of.

Obviously all these components must be canceled in a FD system, since all of them potentially fall into the RX bandwidth of interest. Bharadia, McMilin, and Katti [33] provide an overview of the cancellation requirements of FD for Wi-Fi-type systems.

Cancellation of the SI signal is required down to the RX's (thermal) noise floor, in order to achieve the same signal-to-noise ratio (SNR) compared to the non-FD operation. Cancellation of the interference below the noise floor obviously cannot further improve the SNR of the received signal.

As argued above, an isolation and/or cancellation of the linear main component of the TX signal of 110 dB is required. For cellular LTE-systems these numbers are even more stringent with lower sensitivity levels and higher output powers.

Second, the experimentally observed harmonics and spectral regrowth is more than 40 dB below the main linear component [34] for high performance TXs (i.e. 70 dB above the RX noise floor), dominating emissions in the adjacent channels. Similarly, the (thermal) TX noise is at least $60 \sim 70$ dB below the main linear TX component, requiring roughly $40 \sim 50$ dB of cancellation. In contrast to the linear and non-linear interference components, the noise portion obviously cannot be recreated by any algorithm from the baseband data. In order to cancel it a copy must be obtained where it is generated, e.g. at the TX output.

Figure 2.7 sketches these relations. An additional constraint again is the DR of the RX. Any (leakage) signal exceeding this limit results in clipping and other undesired saturation effects in the RX. Assuming a 70 dB dynamic range [35], already 50 dB of isolation and/or cancellation, also accounting for 10 dB peak-to-average power ratio (PAPR) of the TX and SI signal, must be present in front of the RX to avoid saturation.

Although challenging, in-band FD systems offer several benefits, complementing and sustaining the evolution of 5G networks, not exhibited in their non-FD counterparts [6]:

- **Increased link capacity**: Under ideal conditions true FD communication doubles the link capacity, because the available bandwidth can be utilized in both time and frequency.

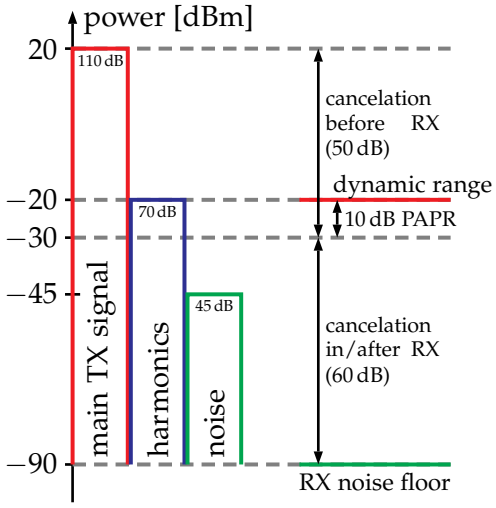


Figure 2.7: SI signal component powers in the FD case.

- **Spectrum virtualization**: True FD is the (extreme) case where both TX and RX bands are completely overlapping. Theoretically, the mechanisms employed in FD systems can isolate any TX and RX frequencies, e.g. partially and non overlapping bands of frequency. Such systems potentially act as software-defined duplexers.
- **Eased CA scenarios**: FD capable systems can isolate any TRX's own TX from any own RX, heavily easing CA configurations. With the reconfigurability of FD systems, various CA can be handled adaptively.
- **Novel relay solutions**: With FD systems employed in base stations and relays, the simultaneous reuse of spectrum is possible for backhaul and access channels.
- **Physical layer network security** [36]: Instead of using the FD communication for enhanced throughput, the received signal can also be masked or jammed with a strong (meaningless) signal. Only the RX with knowledge of that jamming signal can cancel it and recover the desired signal.

Essentially several benefits justify research and development of SIC, although this obviously is a challenging task. Section 3.2 provides an overview over published SIC systems for FD applications.

3 A Review of Self-Interference Cancellation Systems

This chapter provides an overview of published SIC systems, both for FDD and FD applications. SIC systems can be distinguished not only by their targeted tasks. Further differentiation concerns the point(s) of cancellation in the RX and the generation and/or acquisition of the reference and cancellation signals.

Figure 3.1 sketches possible points of cancellation signal injection into an RX lineup:

① at the very RX input
② in the input low-noise amplifier (LNA), e.g. in a specially designed LNA to support signal injection
③ after the input LNA, still in the RF domain
④ in the analog BB or intermediate frequency (IF) domain
⑤ digitally in the digital BB

Additionally, Figure 3.1 highlights potential points to obtain a TX reference signal to generate a cancellation signal:

ⓐ digitally in the digital BB
ⓑ in the analog BB or IF domain
ⓒ at the TX's output
ⓓ at the RX's input

There are essentially three popular choices for SIC systems published:

- First, fully digital systems, where the reference signal is obtained in the digital TX BB, additional signal processing is performed and the cancellation happens in the digital RX BB, e.g. a combination of ⓐ and ⑤ in Figure 3.1.

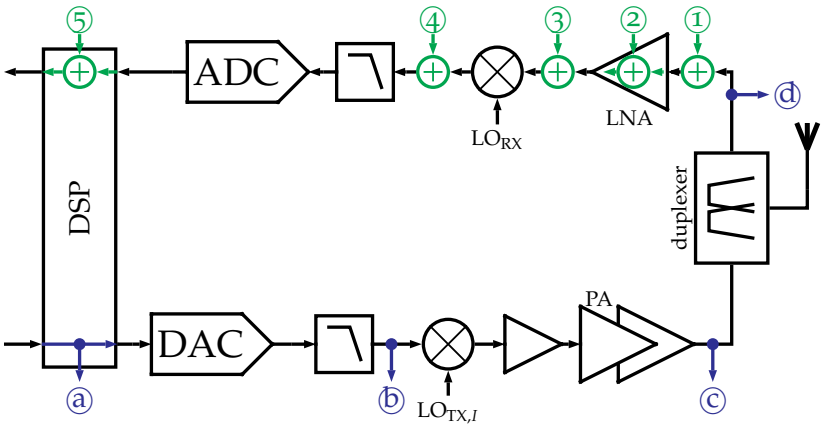


Figure 3.1: Cancellation signal injection possibilities (green) and potential taps to obtain the reference signal (blue) in modern wireless TRX (simplified direct conversion architecture).

- Second, a full RF domain approach, where the reference signal is obtained at the very TX output and canceled in the RX's RF portion, e.g. from ⓒ to ①, ②, or ③.
- And third, a combination of the two approaches, almost always employed in in-band FD systems.

3.1 Self-Interference Cancellation for Frequency Division Duplex Systems

This section reviews published SIC systems for FDD applications, e.g. for (existing) third generation (3G) and fourth generation (4G) TRXs. Solutions battling issues introduced with CA, described in Chapter 2, are also covered in this section.

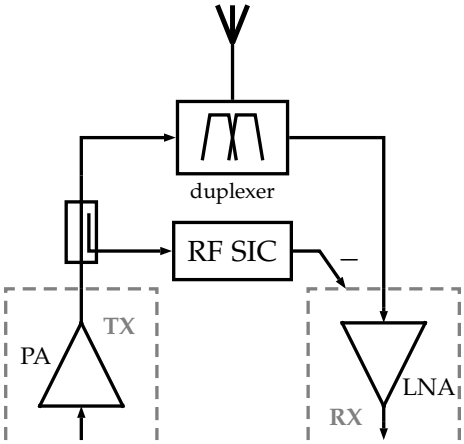


Figure 3.2: Conceptual sketch of TRX systems employing RF domain leakage cancelers.

3.1.1 Analog and RF Domain Self-Interference Cancellation Systems

As briefly mentioned in the introduction of this chapter, and sketched in Figure 3.2, most RF domain SIC systems obtain a copy of the TX signal at the very output, just before the antenna or duplexer/coupler. This reference signal then is used by the SIC circuitry to generate a replica interference signal. The reference signal is accordingly modified, e.g. delayed and frequency shaped, to match the undesired signal at the RX as closely as possible in the frequency region(s) of interest. This interference replica is then subtracted in the RX in the RF domain.

It shall be noted, that RX interference tolerance enhancing methods, e.g. multiple paths or enhanced filtering (e.g. [37]–[39]), are not covered in this section. The reason is that these schemes mainly improve the out-of-band rejection by additional filtering and frequency selective multipath approaches, contrary to "traditional" cancellation scenarios. Similarly, electrical balance duplexers (e.g. [40]–[43]) are not covered in this survey, as they aim at directly providing the duplexing functionality on CMOS.

Research in TX related SIC essentially started in the late '90s with the prospect of extensions to GSM, such as General Packet Radio Service (GPRS) and En-

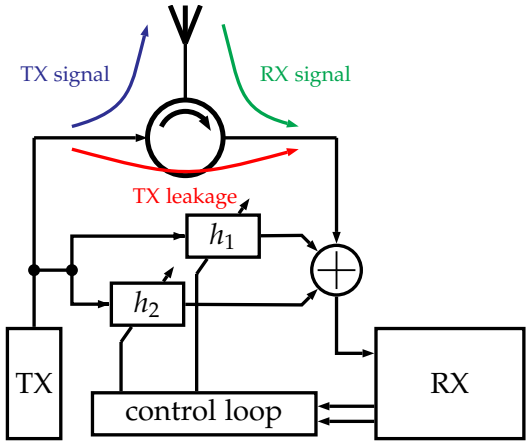


Figure 3.3: Adaptive duplexer structure employing a double loop cancellation structure introduced by Kannangara and Faulkner [44]. The transfer functions h_1 and h_2 are implemented as (programmable) time delays and attenuators.

hanced Data Rates for GSM Evolution (EDGE), as well as Universal Mobile Telecommunications System (UMTS). First, RF domain SIC was seen as a flexible and cost-effective alternative to the poor and insufficient performance of discrete passive duplexers.

Kannangara and Faulkner proposed an adaptive wideband duplexer architecture [44], [45] for code division multiple access (CDMA) and wideband code division multiple access (WCDMA). They employ a wideband circulator with low isolation to couple the antenna and decouple TX from RX. The residual leaked TX signal is canceled with two delayed and attenuated replicas effectively generating two nulls: one at the main TX frequency, to avoid RX overloading and saturation, and another one at the main RX frequency, to remedy the TX-in-RX band noise. The setup is sketched in Figure 3.3.

With their discrete prototype, Kannangara and Faulkner achieve a cancellation of 46 dB (where an additional 20 dB of isolation are attributed to the wideband circulator) for an unspecified signal bandwidth.

This approach was advanced by O'Sullivan *et al.* [46] to improve the isolation of a surface acoustic wave (SAW) duplexer. The authors report an increase of

isolation (i.e. cancellation) of more than 20 dB for 2 MHz wide CDMA signals for their discrete prototype and a single cancellation loop. Furthermore, for two loops, a 20 dB cancellation is reported for more than 4.5 MHz bandwidth. The power consumption is 9.75 mW and 22.4 mW for the single and double loops respectively. The authors report an insertion loss (IL) of 0.24 dB in the RX band.

The original structure was further extended with extensive means of DSP by Eslampanah *et al.* to support CA applications [47]. With their approach, they achieve a cancellation of 30 dB over a 20 MHz bandwidth with LTE signals in simulations.

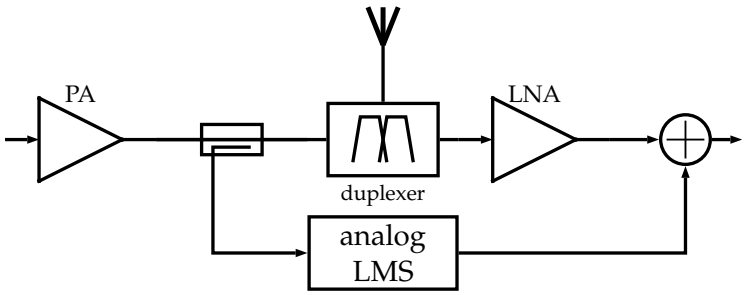
Also for CDMA RXs, Aparin *et al.* introduced a fully integrated leakage canceler featuring an analog least mean squares (LMS) algorithm to dynamically estimate the duplexer's or isolator's leakage transfer function [48]. The implemented system is sketched in Figure 3.4. The system essentially estimates complex coefficients with the analog LMS algorithm by trying to null the signal portion that is correlated with the TX signal.

With this approach, Aparin *et al.* achieve more than 40 dB of cancellation of a single tone at 835 MHz. For a 1.23 MHz bandwidth CDMA signal, employing a SAW duplexer, the cancellation degrades to 14.3 dB, compared to the case of 20.7 dB of leakage suppression, when a linear attenuator is used. Obviously the employed LMS cannot fully cover the complicated TX-to-RX transfer function, which essentially limits the cancellation performance for TX signals with wider bandwidths.

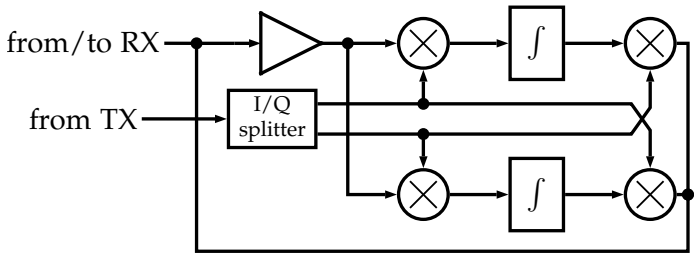
As further disadvantages of this solution the authors list reduced LNA gain and an increased noise figure (NF) from 1.4 dB to 2.7 dB. The maximum power consumption is reported as 16 mA from a 2.7 V supply and varies with operating frequency and TX output power.

A more recent approach was introduced by Kim *et al.* for a WCDMA receiver [49]. A cascoded inductively degenerated differential common source (CS) LNA is extended with leakage cancellation as sketched in Figure 3.5a. The canceler, shown in Figure 3.5b, comprises a quadrature splitter, two variable gain amplifiers (VGAs), and an output summation and buffer circuit.

The quadrature splitter is implemented as a single passive polyphase filter (PPF) stage, since a precise 90° phase shift is not required. The VGAs in the



(a) Overall system employing the adaptive leakage canceler.



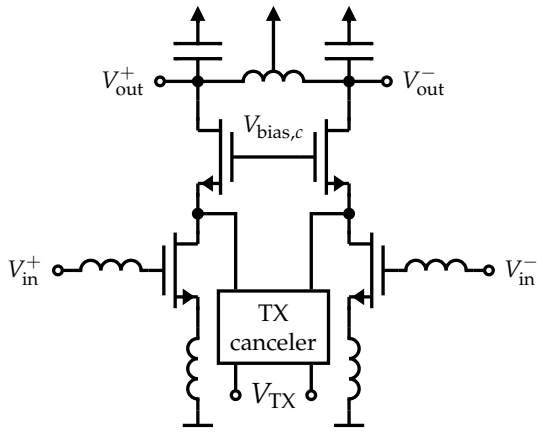
(b) Analog LMS algorithm to dynamically cancel the TX leakage.

Figure 3.4: Adaptive leakage canceler introduced by Aparin *et al.* [48].

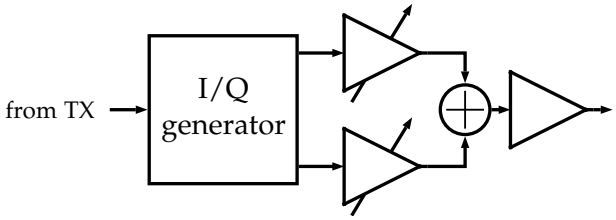
quadrature paths are based on a modified folded Gilbert cell, whose gain can be changed from -1 to $+1$ respectively. The summation is done in the current domain simply by adding the output currents of the VGAs. By varying the gain accordingly, a full 360° phase rotation and amplitude variation can be achieved.

Finally, the buffer of the canceler is a differential pair, whose output drain terminals are directly connected to the LNA's low impedance nodes at the source terminals of the cascode devices. The required phase rotation and amplitude of the cancellation signal are determined by an adaptive LMS algorithm operating in the RX's baseband.

Using an external SAW duplexer for UMTS with 25 dB of passive isolation, Kim *et al.* report a minimum TX leakage rejection of 22.5 dB throughout the whole WCDMA band for 5 MHz signal bandwidths. The NF of their LNA increases from 2.4 dB to 2.84 dB when the cancellation unit is active. The full



(a) Inductively degenerated LNA with leakage cancellation.



(b) Block diagram of the employed leakage canceler.

Figure 3.5: TX leakage cancellation system by Kim *et al.* for WCDMA applications [49].

RX RF system consumes 19.6 mA from an 1.8 V supply, where 10.5 mA are attributed to the leakage canceler.

A principally similar solution of RF domain SIC was published by Zhou *et al.* [50], [51], employing a cancellation signal injection-augmented common gate (CG) LNA. The LNA is based on thermal noise canceling [52], [53], sketched in Figure 3.6.

Transistor M_G is a wideband CG amplifier matched to the 50 Ω input, the matching stage. Transistor M_S is an inverting CS amplifier, sensing the input signal and the noise generated by M_G, the noise canceling stage. If the outputs of the two stages are subtracted, e.g. by differential signaling, the noise cancels and only the input signal remains.

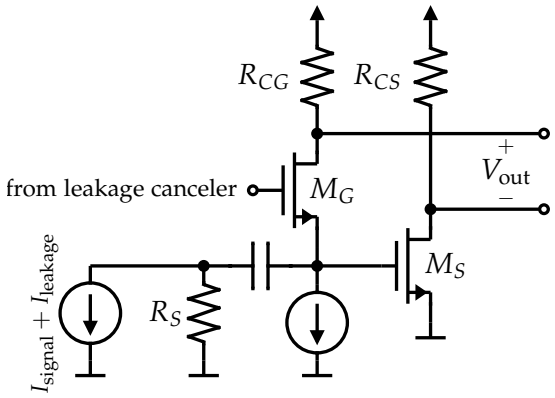


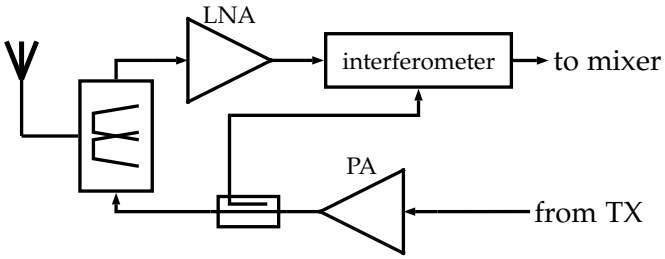
Figure 3.6: Thermal noise canceling LNA [52], [53] augmented with SIC capabilities by Zhou *et al.* [50], [51]. Biasing not fully shown.

For TX leakage cancellation, the canceler's signal is injected onto the CG amplifier's gate, canceling the interfering signal at the input. Additionally, a second point of injection is added at the output of the CS path to further cancel the TX-in-RX-band noise.

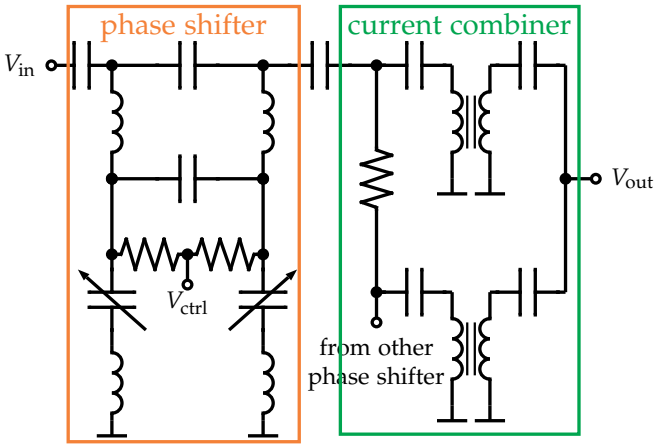
The canceler has two paths, one for the CG and CS paths respectively. Each path is composed from programmable gain amplifiers, operating on quadrature split inputs, similarly to the previous approach by Kim *et al.* as sketched in Figure 3.5b.

Zhou *et al.* built a wideband SIC-RX operating from 0.3 GHz to 1.7 GHz achieving a NF of 4.2 dB without leakage cancellation active. The worst case NF degradation due to leakage cancellation is reported to be 0.8 dB when canceling SI with 2 dBm power (3 dB PAPR). Cancellation of roughly 30 dB or more is achieved with an antenna pair or an attenuator used as TX-to-RX isolating devices.

A passive leakage cancellation method based on the interferometer principle was demonstrated by Li *et al.* for frequencies above 10 GHz [54]. As sketched in Figure 3.7a, the suppression of the undesired leakage signal is achieved in the passive interferometer inserted after the RX-LNA. It consists of two lumped reflective type phase shifters and a transformer based current combiner. The current combiner additionally offers impedance transformation



(a) Cancellation enhanced TRX-system employing the passive interferometer.



(b) Schematic of the passive interferometer.

Figure 3.7: Passive interferometer based TX leakage cancellation system by Li *et al.* [54].

for on-chip loads different from 50 Ω. The full interferometer is sketched in Figure 3.7b.

Their prototype, fabricated in a 65 nm CMOS technology, occupies an area of $0.95 \times 1.05\,\text{mm}^2$ and contains only the passive interferometer. Li *et al.* achieve a cancellation better than 40 dB in the frequency region of $9.5 \sim 11.5$ GHz with optimal manual tuning, although neither signal bandwidth nor type is specified. Furthermore, the measured insertion loss of the interferometer prototype is 15 dB, which requires a high gain LNA in the RX lineup.

Zhang *et al.* presented another passive SI canceler based on a three-input transformer [55]. The transformer based matching network at the RX LNA's

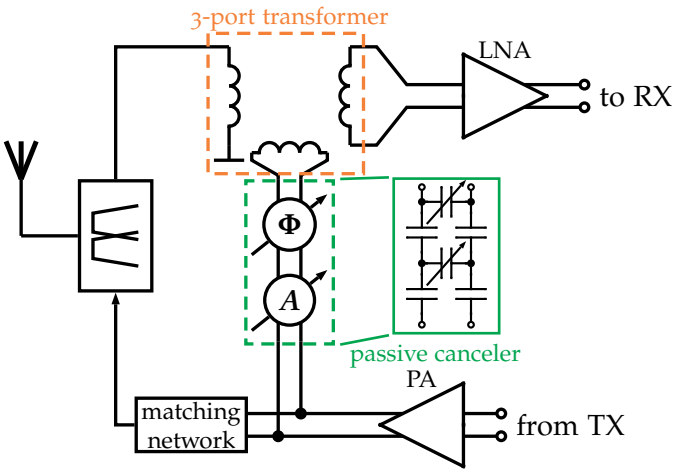


Figure 3.8: Passive leakage canceler based on a three port transformer [55].

input is extended with another port to inject the cancellation signal. The block diagram of the implemented system is shown in Figure 3.8. The canceler itself is a passive circuit providing programmable attenuation and phase shift.

Their prototype, manufactured in a 40 nm CMOS process, occupies a silicon area of $1.6 \times 1.3\,\mathrm{mm}^2$, including a matching network for the power amplifier (PA) (but not the PA itself), the leakage canceler, LNA and testing buffers. The transformer of the SIC system occupies an area of roughly $400 \times 400\,\mu\mathrm{m}^2$.

The peak measured LNA conversion gain is reported as 20.6 dB, including the IL of the employed WCDMA duplexer. The NF is approximately 5 dB over the entire 60 MHz RX band, including ILs of the duplexer ($1.5 \sim 2$ dB) and the transformer based leakage canceler and matching network ($1 \sim 1.5$ dB). The LNA's in-band third order input referred intercept point (IIP_3) is $+3$ dBm.

Zhang *et al.* report an achievable cancellation of 23 dB for continuous wave (CW) signals across the entire TX band of $1.92 \sim 1.98$ GHz when manually optimizing the canceler's settings. For modulated WCDMA signals with 3.84 MHz bandwidth a cancellation better than 20 dB is achieved.

Another passive approach for RF-cancellation is presented by Montanari *et al.* [56], [57]. The proposed method is further combined with a mixed-signal TX-cancellation system, discussed in Section 3.1.3. The proposed RF leakage

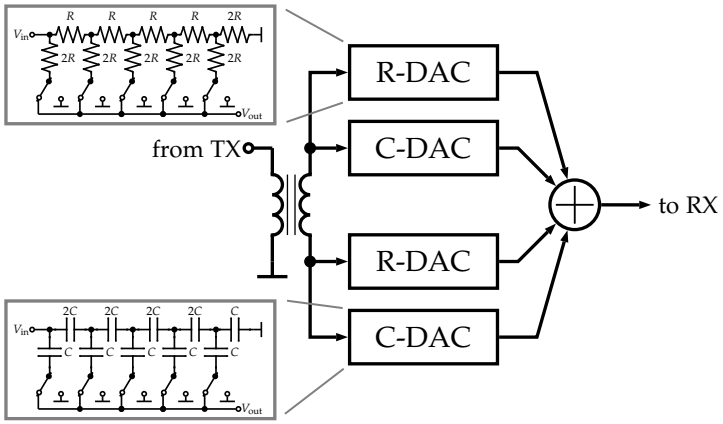


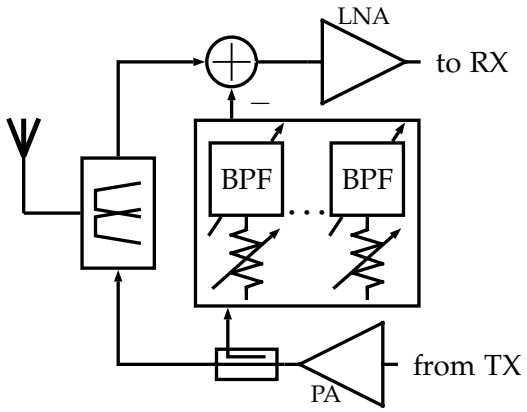
Figure 3.9: Passive leakage canceler presented by Montanari *et al.* [56], [57]. The C- and R-DACs are programmable capacitive and resistive voltage dividers.

canceler gets the differential TX signal, either directly from the TX if available, otherwise by means of a balun. To minimize losses in the canceler, parallel programmable attenuators, one resistive and one capacitive, are placed on both differential phases. The output currents are summed and directly injected at the RX input, as shown in Figure 3.9. The attenuators are implemented as *R*-2*R* and *C*-2*C* networks respectively.

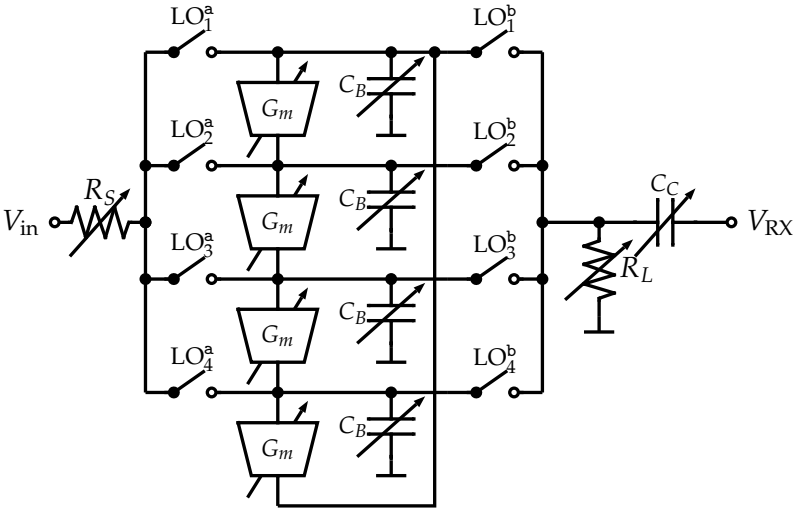
The prototype was manufactured in a 28 nm CMOS technology. The entire RX occupies an area of 0.51 mm^2. The measured NF with the canceler disabled is 4.6 dB at 2 GHz, varying from 4 dB to 5.2 dB versus operating frequency. Activating the RF canceler degrades the NF by $0.4 \sim 0.8$ dB, depending on its programming. For correct canceler settings, the authors report 20 dB cancellation for 15 MHz bandwidth signals. The RX IIP3 is improved by 16 dB reaching 25 dBm until the canceler nonlinearity limits performance.

A different approach to replicate the TX-to-RX leakage signal path was chosen by Zhou *et al.*, where parallel band pass filters (BPFs) are employed to generate the desired transfer function in the leakage canceler [58], [59]. Figure 3.10a shows the overall system with the employed canceler consisting of parallel BPFs.

The cancellation signal is injected capacitively into the RX. The thermal noise canceling CG LNA is similar to their previous SIC implementation [50] pre-



(a) TRX system with leakage canceler.



(b) Implementation of an N-path G_mC second order filter.

Figure 3.10: Leakage canceler based on parallel BPFs by Zhou *et al.* [58], [59]

sented earlier in this section. The reconfigurable BPFs are implemented as high quality-factor N-path G_mC filters [60]–[62] with embedded programmable phase shifting and amplitude control. In Figure 3.10b the second order BPF's implementation is sketched. The filter bandwidth is controlled by changing the value of capacitors C_B, the center frequency by G_m, the attenu-

ation with R_S, and the overall phase shift by the skew of the 25 %-duty cycle LO phases (denoted as a and b in Figure 3.10b) that is driving the filter's switches.

The prototype, manufactured in a 65 nm CMOS technology, occupies an active area of 4.8 mm^2. The measured RX NF ranges from $4.8 \sim 5.8$ dB over the operating frequency range of $0.8 \sim 1.4$ GHz.

For FDD operation, 20 dB cancellation bandwidths of 17 MHz and 24 MHz are achieved, when using one and two parallel BPFs respectively. An LTE-like *LC*-based duplexer, providing 30 dB of isolation, is used for this measurement. The increase in NF is measured as 0.5 dB and 0.6 dB respectively. In this case the *N*-path filters are driven with the TX LO, the frequency offsets of the filters are achieved by varying their respective G_m.

A single canceler's BPF's power consumption is reported as maximally 47 mW for the G_m-cells and additionally 44 mW for the LO at 1.35 GHz.

Another active RF domain cancellation scheme is presented by Tijani and Manstretta [63]. The required phase shift and attenuation of the TX signal is achieved by two parallel programmable transconductance amplifiers. The two amplifiers incorporate the functionality of an *RC-CR* quadrature splitter, as previously discussed. Furthermore, they are designed as slices, that can independently be turned on and off, providing for the required programmability. The system and the SI canceler are shown in Figure 3.11. To further linearize the canceling amplifiers, feedback resistors $R_{f,I}$ and $R_{f,Q}$ are added to feed back a portion of the RX and canceler's output signal.

The system is designed in a 40 nm CMOS technology with a 1.8 V supply. The maximum simulated power consumption of the active canceler is reported as 16.2 mW. In simulations, a 30 dB cancellation bandwidth is achieved when there is no TX-to-RX delay. For a more realistic scenario with 2 ns delay, the 30 dB bandwidth decreases to 10 MHz. The simulated NF degradation is 0.8 dB. For in-band scenarios, the 1 dB-compression point is improved from -25 dBm to 4 dBm with the cancellation active. Similar to out-of-band scenarios, it is improved from 1.7 dBm to 5 dBm in simulations.

A different approach was adopted by Yüksel *et al.* [64], [65], where the interfering TX signal is canceled by destructive interference from the RX. Figure 3.12 essentially depicts the operating principle of the distributed TX,

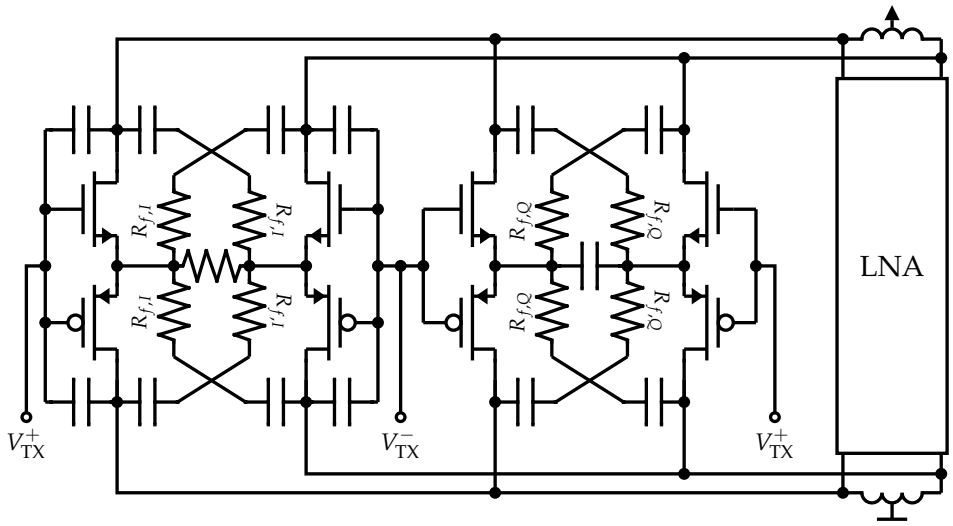


Figure 3.11: Active RF-domain leakage canceler by Tijani and Manstretta [63].

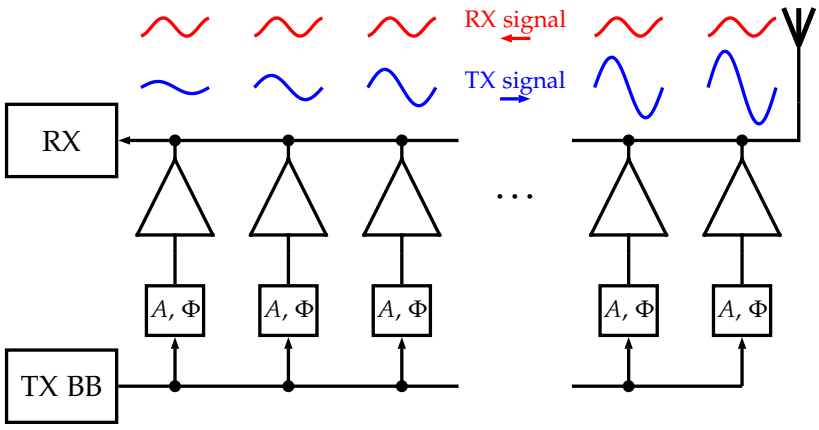


Figure 3.12: Transmission line based duplexing scheme by Yüksel *et al.* [64], [65].

whose output signals add constructively towards the antenna output and cancel destructively to the RX input.

The individual sub-TXs have individual BB signal processing, effectively providing complex weighting factors. This allows for constructive TX signal combination at the antenna output while simultaneously nulling the signal at the RX input.

The artificial transmission line is implemented with lumped elements: inductors and capacitors, which provide an electrical delay. The design of the distributed TX, including the artificial transmission line, heavily influences the operating frequency region, output power and eventually TX efficiency. The number of TX stages N_{st} effectively determines the practicable frequency range $f_{\max}/f_{\min} \approx N_{st}$, while the interstage delay τ_{st} sets the upper frequency limit $f_{\max} \lesssim 1/(2 \cdot \tau_{st})$.

Furthermore, the practical limit of N_{st} is set by the maximum tolerable IL of the transmission line, since the RX signal needs to traverse through it, effectively degrading the RX NF. Also, the area occupied by the transmission line is non-negligible, as each interstage inductor has a value of 2 nH.

Yüksel *et al.* chose $N_{st} = 6$, although the three sub-TX closest to the antenna feature a special high-swing high-power design with increased supply voltage. In order to combat the uncorrelated noise of the sub-TX in the RX frequency band, an adaptive source degeneration of the PAs is included. A passive mixer is used to provide a narrowband degeneration at the RX frequency, effectively suppressing the TX-in-RX band noise.

Their prototype, manufactured in a 65 nm CMOS technology, occupies an area of $2.4 \times 3.0\,\mathrm{mm}^2$. The operating frequency region is reported as $0.3 \sim 1.6$ GHz. The TRX system consumes 2.2 W from a 2.5 V supply, while transmitting 16 dBm at 900 MHz and receiving at 785 MHz. The RX NF is measured as $8 \sim 12$ dB, although a flaw in physical design prevented the prototype to achieve the expected performance.

The prototype achieves a TX-to-RX isolation better than 25 dB over the entire operating frequency range. A change in the voltage standing wave ratio (VSWR) (from 1 : 1 to 1 : 3) results in a drop of isolation by 20 dB and of 5.4 dB in output power. By recalculating the weights of the individual sub-TX, the TX-to-RX isolation can be restored.

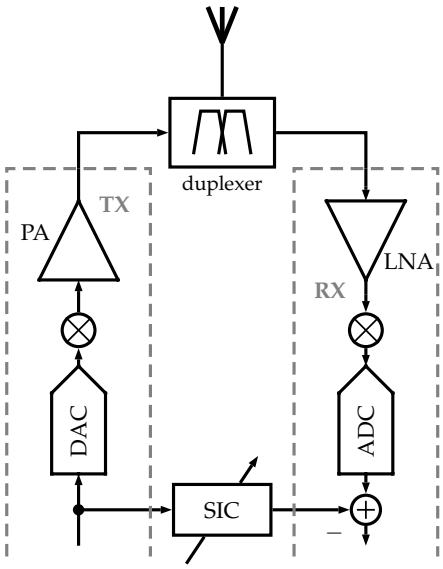


Figure 3.13: Conceptual sketch of TRX systems employing digital-only leakage cancelers.

3.1.2 Digital-Only Self-Interference Cancellation Systems

As introduced in the beginning of this chapter, digital-only SIC operates fully in the digital domain. This includes obtaining the reference signal, which is the data stream provided to the TX. The cancellation of the undesired leakage signal is also done entirely in the digital domain, after the analog-to-digital conversion of the RX as conceptually sketched in Figure 3.13.

This obviously implies that the SI must not degrade the RX's operation, e.g. drive it into saturation or clipping, since digital-only SIC only impacts the signal after all RF and analog signal processing. Therefore, digital-only SIC can only improve reception if, for example, nonlinear artifacts of the leaked TX signal have sufficiently low power and are well covered by the analog linearity the RX offers. These products may directly impair the desired RX signal, e.g. by folding or falling into the RX baseband, where they then may be removed with means of digital SIC.

Advantageous to digital-only SIC is that it fully exploits the benefits of digital signal processing, including adaptive filters [66], which are able to not only

learn the leakage transfer characteristics but can also track changes thereof over time. Furthermore, existing RX designs can be easily augmented with digital-only SIC. No changes to the analog and RF RX hardware are necessary, and no additional analog circuits, e.g. auxiliary LNAs, mixers, or analog-to-digital converters (ADCs), are needed.

Therefore, research into digital-only SIC emerged with feasible and affordable integrated digital signal processing capabilities, which are directly linked to advances in CMOS technology.

First approaches in 2008 to digital-only SIC tackled second order nonlinear effects of TX leakage. Frotzscher and Fettweis published a LMS algorithm [67], [68] to cancel second-order intermodulation (IM2) products of the leaked SI signal in a zero-IF WCDMA RX. In such a system, these nonlinear TX-induced components directly fall onto the desired RX signal. Without any further means (e.g. improved TX-to-RX isolation or cancellation) the reception is heavily impaired by the TX leakage.

In simulations, with a linear SI model for their algorithm, Frotzscher and Fettweis achieve a 2 dB gain in SNR for a 10^{-2} bit error rate (BER).

Similarly, Kahrizi *et al.* also mitigate the TX-induced IM2 distortion products in a WCDMA RX [69]. In addition to a LMS algorithm, an adaptive delay is added to align the TX IM2 products and their digital recreation. In simulations, the authors report that "cancellation" of the IM2 products is achieved.

Yet another LMS-based IM2 cancellation was published by Lederer and Huemer [70]. In addition to the LMS algorithm, an adaptive fractional delay filter [71] is added to improve cancellation. The authors report a measured improvement of the susceptibility of 5 dB of the RX to TX induced IM2 products for equal noise levels when comparing the cancellation algorithm switched on and off.

Similarly, Kiayani *et al.* introduced a digital-only IM2 cancellation system [72], based on a second order Volterra kernel [73]. The parameters of the model are estimated adaptively with a linear least squares (LS) algorithm. The authors specify that correct time alignment of the reference signal and the baseband output of the RX is crucial for correct operation.

The proposed IM2 cancellation system introduces higher complexity and effort compared to the previously presented IM2 cancellation schemes. But the authors report that for 10 MHz LTE signals their system outperforms the others, canceling the TX-induced IM2 products below the RX noise floor.

In 2017 Gebhard *et al.* proposed a nonlinear low-complexity LMS-type algorithm for adaptive TX-induced IM2 cancellation [23], [74]. For 10 MHz LTE signals the authors report cancellation of the IM2 products down to the RX noise floor up to 23 dBm TX signal power with a high performance duplexer in place.

A different approach to IM2 (and other nonlinearities) cancellation is published by Gerzaguet *et al.* [75], [76]. The (nonlinearly distorted) reference signal is passed through an adaptive fractional delay and an adaptive single tap complex gain to recreate the leakage signal. The gain and delay are adapted with a joint LMS-based estimation algorithm. The authors report a signal-to-interference ratio after cancellation of more than 35 dB for their approach for 1.4 MHz bandwidth LTE signals.

Increasing data rates require higher bandwidths in the uplink TX signals required by modern wireless communication standards. All nonlinear components in the TX chain, especially the PA, contribute to spectral regrowth [77]. With increased signal bandwidths, inevitably the frequency range polluted by this intermodulation distortion (IMD) is also vastly increased. With low duplex spacings and high bandwidths, as specified and employed in UMTS and LTE, this TX out-of-band (OOB) emission can directly overlay with the simultaneously active RX band. This undesired IMD products can now also leak through the duplexer into the RX, degrading its performance.

While this effect can be countered by digital pre-distortion (DPD) of the TX [78], [79], effectively linearizing the TX, Omer *et al.* counter this effect with OOB emission SIC [80]. Several IMD products, potentially falling into the RX band, of the reference signal are generated. They are then passed through adaptive linear filters resembling the duplexer and other signal processing components in the leakage path. This closely resembles a bank of Hammerstein filters [81], [82] to recreate the leakage signal.

With recursive least squares (RLS) adaptation, the authors report a 18 dB cancellation of the leaked TX OOB emissions leaving a residual approximately

2 dB above the noise floor in measurements for a 10 MHz High Speed Uplink Packet Access (HSUPA) signal.

A similar approach is chosen by Kiayani *et al.*: They again recreate IMD products falling into the RX band [83]. These distortion components are again weighted and passed through a set of LS adaptive filters. In simulations, they achieve cancellation of the TX OOB emissions below the noise floor for a 5 MHz LTE signal. They also note that for acceptable performance, all necessary polynomial orders in the recreation of the reference IMD products are required.

Another issue related to TX-induced SI is the so called modulated spur problem. In this case, the RX LO exhibits a spurious tone close to the TX frequency. This spur, although with low power compared to the main tone at the RX frequency, downconverts the high power TX leakage directly into the RX baseband, corrupting reception. Spurs can be a result of nonlinearities, e.g. in the frequency synthesizers, or cross-coupling with other simultaneously active clocks or LOs.

First in 2012, Omer *et al.* tackle this modulated spur issue [84]. The approach requires knowledge of the RX, TX, and the spur frequencies. An iterative RLS-based approach is used to estimate the leakage transfer function and the spur downconversion characteristics.

For a 2 MHz bandwidth Evolution-Data Optimized (EVDO) signal the authors report that their approach can restore the RX signal-to-interference-and-noise ratio (SINR) to the original SNR within 1.6 dB for low RX powers. For higher RX powers, starting at 15 dB of SNR, the restored SINR falls short by more than 3 dB compared to the original SNR. The higher power RX signal obviously disturbs the performance of the adaptive algorithms to estimate the TX leakage channel.

Kanumalli *et al.* propose a similar approach for LTE CA RXs [21], [23], [24]. In these systems two or more RX LOs are active. Combinations of these LOs or their harmonics can easily lead to such undesired spurs close to the TX frequency.

With an LMS-based estimation approach, where again all involved frequencies are known, the authors report more than 11.6 dB of cancellation for a 10 MHz LTE signal. For increasing RX signal strengths, again the restored

SINR drops compared to the original RX SNR, although the degradation is confined to 1.1 dB at 24.7 dB RX SNR.

Another challenge tackled by digital-only SIC is related to non-contiguous uplink CA (see Section 2.2). Dabag *et al.* developed a multiple-input single-output cancellation algorithm to battle intermodulation products of multiple TX falling into RX bands [85]–[87]. This algorithm considers only crossmodulation terms of two or more TX signals, as they potentially fall onto RX frequencies. For the different transmitters usually dedicated passive front-end components are used, resulting in different group delays of the individual TX signals before the antenna. The authors account for these different time delays in their cancellation system.

In simulations, perfect cancellation is achieved when correctly estimating the different delays of the TX signals for 5 MHz LTE signals. In measurements, for RLS-based adaptation and 2× uplink CA with 5 MHz TX signals, a cancellation of more than 19 dB is reported for weak RX powers.

Kiayani *et al.* proposed a similar algorithm that also considers I/Q imbalance of the TXs [88]. In simulations, they achieve cancellation of the interfering intermodulation products below the RX noise floor for sufficiently high modeling orders, achieving $15 \sim 20$ dB of suppression in presence of a weak RX signal. In measurements, for two 5 MHz wide quadrature phase shift keying (QPSK) signals, cancellation of roughly 20 dB is achieved without an RX signal present. With a weak LTE downlink signal present, the leakage suppression is reduced to approximately 18 dB.

Yet another similar approach is introduced by Yu and Zhu [89], [90]: Contrary to the previous approaches, only a single crossmodulation term is computed from the two TX baseband signals falling into the RX band. Further nonlinear components are added by introducing the composite envelope of the total TX signal. This approach heavily reduces computation complexity and sampling rate requirements. Moreover, this approach can be generalized to incorporate multiple TX signals [89]. In measurements, for two 5 MHz LTE signals, the authors report up to 25 dB of cancellation without any RX signal present.

Waheed *et al.* approach this issue for the case in which both TX signals have their own PAs additionally introducing different nonlinearities on the two uplink signals [32]. In simulations, for a frequency-flat duplexer, the authors

report a cancellation performance of the interference 10 dB below the noise floor. For realistic duplexer transfer functions, the proposed model fails, as there is no memory included to cope with this frequency selectivity.

3.1.3 Mixed-Signal Self-Interference Cancellation Systems

Mixed-signal SIC solutions are hybrid, combining RF-domain and digital approaches. Essentially, there are two possibilities:

- First, the reference signal and subsequently the cancellation signal are generated in the digital domain and leakage cancellation is performed in the analog/RF domain.
- Second, the reference signal is obtained in the analog/RF domain and the cancellation is performed in the digital domain. Both approaches have been published as presented in this section.

A first approach to mixed-signal SIC was publised by Schacherbauer *et al.* in 2000 [8], [91], [92]. The cancellation signal is generated in the digital baseband of the transmitter and fed to an auxiliary TX. The output of this auxiliary path is coupled into the input of the RX, attempting to cancel the TX leakage signal. The overall system is sketched in Figure 3.14. Furthermore, to avoid degradation of the RX performance due to spurious emissions of the main and auxiliary TXs, additionally two suitably chosen IFs are employed in the RX.

Test signals are injected prior to normal operation in order to estimate the stop-band transfer function of the duplexer, necessary to obtain cancellation. With this knowledge, a finite impulse response (FIR) filter is programmed in advance to generate an appropriate cancellation signal. With a discrete prototype [92] the authors report cancellation of approximately 35 dB for a 5 MHz UMTS signal although the performance degrades when time varying components are included.

A similar approach is taken by Kiayani *et al.*, where again the output of an auxiliary TX chain is subtracted at the RX's input [93], [94]. The system computes the cancellation signal with nonlinear adaptive filters, namely with parallel Hammerstein models [95], [96], whose coefficients are adapted online.

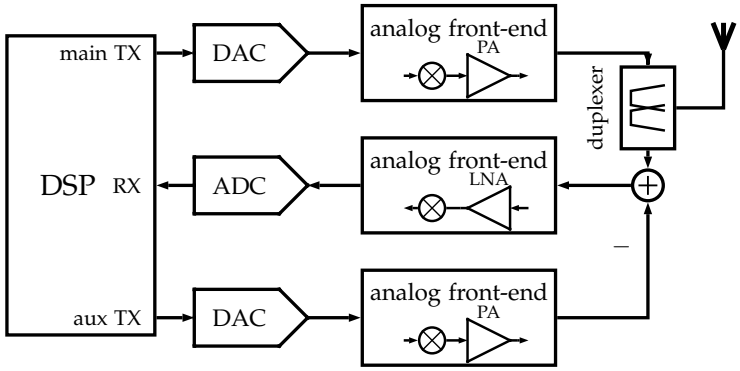


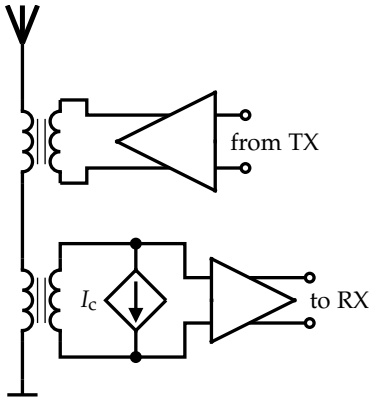
Figure 3.14: Mixed-signal SIC system by Schacherbauer *et al.* [8], [91], [92]

With their discrete prototype, the authors report cancellation of the TX leakage by 23 dB for a 10 MHz LTE signal with a linear canceler only. By means of their non-linear canceler, the suppression of the SI is improved by more than 12 dB.

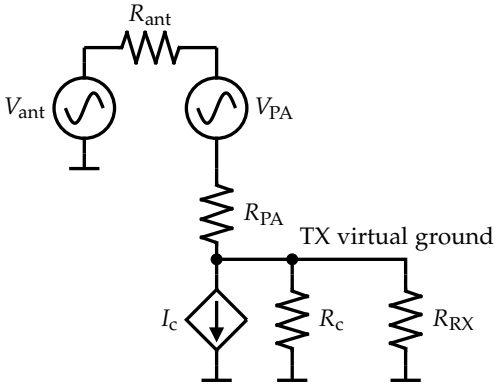
An integrated mixed-signal cancellation solution is presented by Calderin *et al.*, where a dedicated cancellation RF-DAC is integrated with the RX in the entire TRX system [97]–[99]. The principal system block diagram and its equivalent circuit model are shown in Figure 3.15.

This architecture implies that the output impedance of the TX must be sufficiently low in the RX band. It forms a voltage divider with the RX input impedance, resulting in additional IL for the RX. Further, the cancellation RF-DAC's equivalent impedance must be high, as it otherwise shunts the RX signal again, causing RX IL. The cancellation RF-DAC's output is directly fed into the low impedance TX virtual ground node. Albeit this node acts as a virtual ground for the TX in case the cancellation RF-DAC is operated properly, otherwise the TX power divides equally to the antenna and RX impedances.

The TX is implemented as a switched-capacitor power amplifier (SCPA) (or capacitive RF-DAC) [100], providing the required low output impedance in the RX band. The cancellation RF-DAC is implemented as a 10 bit current RF-DAC with DPD. The cancellation RF-DAC's and the TX's LO paths are shared to have their phase noise correlated, additionally resulting in TX phase noise



(a) TRX system overview. I_c signifies cancellation RF-DAC output current.



(b) Equivalent circuit model of the TRX.

Figure 3.15: Integrated mixed-signal leakage canceler by Calderin *et al.*, [97]–[99]

cancellation. The quadrature RF-DACs are driven with 25 % duty cycles to mitigate some of the power penalty of Cartesian digital-to-analog converters (DACs) compared to the polar architecture [9]. It should be noted that, contrary to the SCPA architecture, where the equivalent output impedance is nearly constant and not depended on its input data, the output impedance of the current RF-DAC is inversely proportional to its input code.

The authors report more than 50 dB of cancellation for a 20 MHz wide signal with 2 MHz tone spacing with their integrated prototype manufactured in a 65 nm CMOS technology. Before being passed to the demonstrator, the can-

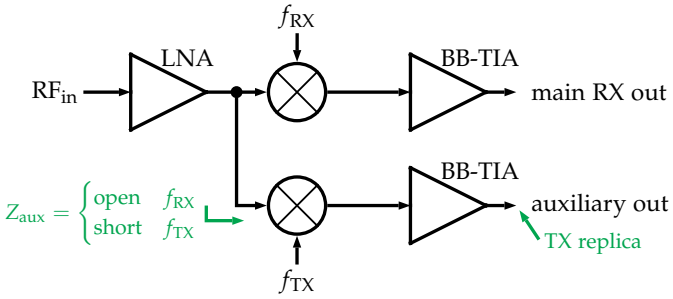


Figure 3.16: Leakage suppression RX by Mirzaei *et al.* [101].

cellation data is adaptively filtered to improve cancellation in real time. The RX NF is degraded by 1.7 dB at 2 dBm TX power and increases to 4.3 dB at an output power of 10.6 dBm.

A very different approach is chosen by Mirzaei *et al.* [101]. The TX leakage (or any interfering signal with known center frequency) is attenuated in the RX. An additional auxiliary RX path is added as sketched in Figure 3.16.

The passive mixer is driven with the TX frequency (or blocker frequency) and acts as an N-path bandpass filter [60]–[62]. This auxiliary RX presents a high impedance further away from the TX frequency towards the main signal path. Contrary at frequencies close to the mixer frequency it acts as low impedance, shunting the leakage signal away from the main RX. Additionally, the output of the auxiliary signal path can be used to further digitally cancel any residual leakage, IM2 correction, or used to linearize and/or predistort the TX in a closed-loop manner. Of course, routing an additional LO signal close to the sensitive RX potentially causes additional undesired spurs and crosstalk. Furthermore, routing the TX-LO into the RX is usually a very power intensive task, as the two blocks are generally placed at a large distance to avoid coupling and crosstalk. Multiple such auxiliary paths operating at different frequencies can be added to the RX.

The prototype, fabricated in a 40 nm CMOS technology, occupies an area of 0.93 mm^2. The NF of the main RX is reported as 1.6 dB with the auxiliary path disabled. Activation thereof degrades the NF by only 0.1 dB. At 0 dBm modulated blocker power at 100 MHz offset, the NF is improved by 11.5 dB,

achieving a value of 13.5 dB with SIC enabled. For the prototype no additional digital cancellation is applied.

Elmaghraby *et al.* propose a similar architecture to tackle the modulated spur issue [29], [102]. An auxiliary RX, including an auxiliary low-gain LNA, is added to capture the TX leakage signal that already traversed the high-order stopband TX-to-RX transfer function of the duplexer. The output of this auxiliary path is digitized and canceled from the main RX signal in the digital domain. Beneficial to other digital SIC approaches on modulated spurs is the heavily reduced complexity of the cancellation DSP. The reference signal, captured after the duplexer, already contains the actual frequency selectivity and delay of the leakage path and thus does not require further system identification and signal processing. The frequency of the problematic spur still needs to be known to align the cancellation signal in the frequency domain.

The authors also mention using the main RX LO for leakage downconversion. This implies less critical LO routing and avoidance of additional crosstalk, spurs, and LO coupling. Of course, a wideband ADC with high sampling rate is required in the auxiliary path to capture the signal at the duplex offset, which can be as high as 400 MHz.

For a proof-of-concept, the authors use a TRX system manufactured in a 28 nm technology capable of 2× CA with two simultaneously active RXs. They set the LO of the first RX to the RX operating frequency and the one of the second RX to the TX frequency, acting as the auxiliary RX. Further a CW spur with known frequency is injected to the LO of the main RX.

The authors report that for 5 MHz bandwidth LTE signal the unwanted modulated spur interference can be canceled below the noise floor in the digital domain with their low complexity adaptive algorithm. Further, the RX's NF, is degraded by the TX signal by 1.1 dB to 4.3 dB without any spur on the LO present. With a spur present but the cancellation off, the leakage dominates the noise floor and the NF rises to 15.6 dB. Activating the cancellation again improves the RX NF to 4.4 dB, which implies a negligible NF degradation of only 0.1 dB and the authors report a cancellation of the modulated spur by 28 dB.

Another similar approach is published by Sadjina *et al.* to counter the modulated spur issue in a 2× CA RX [30], [103], [104]. Again an auxiliary RX

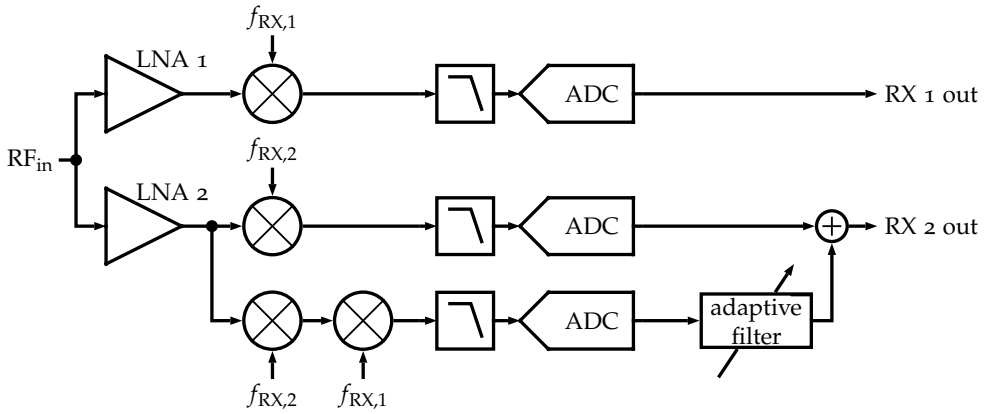


Figure 3.17: *Serial mixing detector* by Sadjina *et al.* [30].

path is added to obtain a reference signal for digital cancellation already incorporating the TX leakage path characteristics. Contrary to the previous approaches, in the auxiliary RX, two passive mixers in series driven by the two main RX-LOs, dubbed *serial mixing*, are used to downconvert the leakage signal as sketched in Figure 3.17. Therefore, for spurs created by the simultaneous operation of the two RXs for CA, no prior knowledge of the specific spur frequency is required.

The auxiliary RX path obviously has an impact on the main RX it is added to, as sketched in Figure 3.17. A trade-off between gain and NF degradation of the main RX and the gain of the auxiliary path exists: high auxiliary gain is beneficial for high SNR values in the auxiliary path easing and improving digital cancellation. High gain in this path obviously also takes more signal current from the main RX, worsening its gain and NF.

The authors implemented this architecture in a demonstrator manufactured in a 28 nm CMOS technology. A power consumption of the auxiliary path of 14.3 mW for a 20 MHz LTE TX signal with -23 dBm at the LNA input. The addition of the proposed auxiliary path degrades the measured RX gain by 1.4 dB and the NF from 3.1 dB to 3.5 dB.

For a 5 MHz LTE TX signal that is provoking the modulated spur issue, a NF of 5.7 dB is measured. Using the proposed auxiliary path and low com-

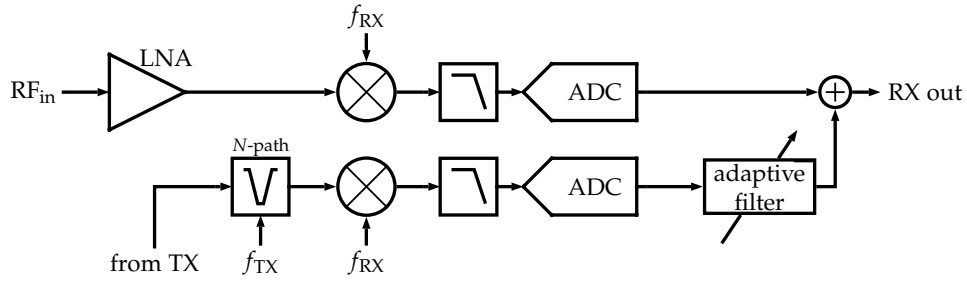


Figure 3.18: TX-in-RX band noise mixed-signal cancellation system by Montanari *et al.* [56], [105].

plexity digital cancellation, the authors report restoration of the NF to 3.4 dB, canceling the undesired interference by 21.8 dB, below the noise floor.

Yet another possibility of mixed-signal SIC is presented by Montanari *et al.*, where an auxiliary RX is connected to the TX's output [56], [105]. This additional signal path captures the TX-in-RX band noise, used to improve the RX's noise performance by digital cancellation. The system is sketched in Figure 3.18. Furthermore, this cancellation scheme is also combined with a RF-domain system, separately discussed in Section 3.1.1.

In order to capture the TX OOB noise with sufficient resolution, a TX band-reject filter, based on an active N-path filter [60], [62], is employed to reduce the DR requirements on all other circuit blocks in the auxiliary RX. This signal then is downconverted with a passive mixer driven with the RX-LO and digitized. The output signal of this auxiliary path then is equalized with an adaptive LMS-based filter and subtracted from the main RX output.

The prototype, manufactured in a 28 nm CMOS technology, occupies an area of 0.12 mm^2 for the auxiliary RX without ADCs and digital algorithm. The main RX's NF is reported as 4.6 dB. When applying a 23 dBm TX signal with -153 dBc/Hz RX band noise density, the NF degrades by 13 dB without cancellation. Activating the mixed-signal cancellation restores the NF within 1 dB of its original value without the TX-in-RX band noise. It shall be noted that the measured scenario does not include any duplexer but simulated a loosely coupled antenna pair with linear attenuators and delay lines.

3.1.4 Conclusion

There are essentially three possible approaches to TX-induced SIC for FDD systems as discussed in the previous sections. All approaches exhibit advantages and disadvantages:

- **Analog/RF SIC**: These approaches generally can either relax RX specifications or improve resilience to the TX interferer due to canceling it at the input or an early stage of the RX chain. If the RX is saturated or even clipping due to the strong TX leakage, cancellation systems injecting the cancellation signal in the RF domain are the only possibility to enable and/or improve reception. Disadvantageous of analog/RF systems is the usually non-negligible degradation of NF, increase in power consumption (valid for active cancellation systems), and increase of silicon area (especially valid for passive cancellation systems). Furthermore, correctly adapting or programming the cancelers' parameters is not trivial and requires further digital processing or complicated analog feedback and control loops.
- **Digital-only cancellation**: Digital-only approaches are very well suited when the TX leakage is not causing saturation or clipping effects in the analog RX circuitry but degrades the reception due to secondary effects such as cross- and intermodulation, spurs on the RX LO, or crossmodulation of multiple TX signals. No modifications in the analog domain of the RX are required; the solutions generally offer great flexibility due to the employed digital signal processing. For decent cancellation performance, generally complicated signal processing algorithms are required which results in a penalty in power consumption and silicon area. Furthermore, these approaches are confined to the more specialized set of secondary effects of SI scenarios discussed in the respective sections.
- **Mixed-signal solutions combining the above approaches**: Mixed-signal solutions try to combine the advantages of the two previously discussed classes of SIC systems. Essentially, the versatility of digital signal processing is combined with some aspects of analog/RF SIC: either obtaining an analog reference signal or canceling the leakage signal in the RF domain.

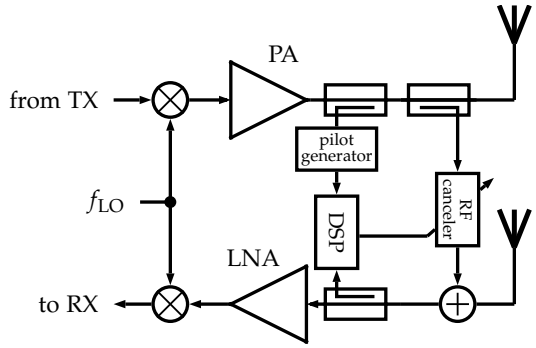


Figure 3.19: *Division-free duplex* system introduced by Chen *et al.* in 1998 [107]. The additional baseband digital SIC is not shown.

3.2 Selected Systems with Self-Interference Cancellation for In-Band Full Duplex

Introduced in Chapter 2.2, in-band FD system simultaneously transmit and receive at equal or overlapping bands of frequency. As previously discussed, the power of the desired RX signal may be weaker by more than 100 dB compared to the TX signal. To uncover this desired signal, a suitable SIC system is required.

One of the first times SIC for wireless FD communications is mentioned, is Kenworthy's already expired patent dating back to 1997 [106]. It describes several possibilities of SIC for wireless TRX.

In one of the first scientific publications, dating back to 1998, dealing with SIC for in-band FD (actually called *division-free duplex* by the authors), Chen *et al.* propose a combined RF-domain and digital cancellation system [107]. The overall system is sketched in Figure 3.19. Additionally to two dedicated antennas, one used by the TX and RX each, a so called RF echo canceler is employed. It is controlled by an adaptive digital controller. Furthermore a dedicated pilot generator allows for training of the echo canceler. Unfortunately there are no details on the implementation of the echo canceler provided.

The prototype solely includes the RF echo canceler. The system is designed for a channel bandwidth of 200 kHz at 1.823 GHz center frequency. For a

transmitted three tone signal, the authors report cancellation of more than 72 dB, where 29 dB are attributed to the dual antennas, 6 dB to RX-IL and 37 dB to the RF echo canceler.

In 1999 Gummalla and Limb employed the approach of Chen *et al.* in a busy tone multiple access [109] ad-hoc network TRX [108], [110], where the busy tone channel was moved into the main transmission frequency band.

Thereafter, research on in-band FD communications quieted until 2009, where Radunovic *et al.* employed a discrete noise canceler [112] for in-band FD for Wi-Fi [111]. Cancellation of 30 dB is reported without further detailing any measurement conditions.

In 2010, Choi *et al.* extend the previous approach and further combine it with digital SIC and an antenna cancellation scheme pictured in Figure 3.20 [17]. The placement of two transmit antennas is exploited to achieve destructive interference at the location of another antenna used by the RX. This is achieved by placing the RX antenna so that its distance to the two TX antennas differs by an odd multiple of half the signal wavelength $\lambda/2$.

As the authors correctly state, the setup is fixed to a dedicated frequency (since frequency directly translates to a certain wavelength) and cancellation degrades with increasing signal bandwidth. Furthermore, the amplitudes at the TX antennas must match to achieve cancellation. The system is also highly sensitive to errors and variations in the aforementioned parameters.

Another issue with antenna cancellation reported by Choi *et al.* is the effect on other receiving nodes. With parameters set ideally for SIC, there are significant nulls present in the far field rendering reception impossible for other nodes in the network depending on their location.

A measured cancellation performance better than 30 dB is reported for the proposed antenna cancellation for a 5 MHz ZigBee signal. When additionally activating the RF canceler with the discrete noise canceler [113], the cancellation performance is reported to improve up to 60 dB. Last, the digital cancellation further improves performance by 10 dB.

Also in 2010, Duarte and Sabharwal presented a different solution of SIC for in-band FD [18], [114]. Again, multiple cancellation approaches are combined: First, dedicated antennas for TX and RX are used to provide some

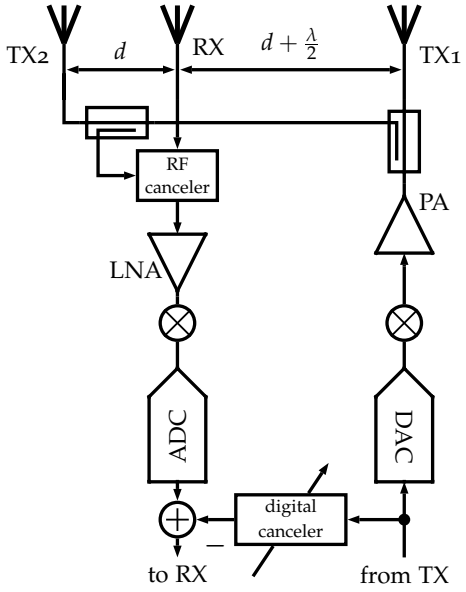


Figure 3.20: In-band FD system by Choi *et al.* employing antenna canceler [17].

passive isolation. Second, a mixed signal cancellation (although called analog by the authors) creates a cancellation signal injected at the RX input with an auxiliary TX. Third, digital cancellation is used to further boost performance. The overall FD system is sketched in Figure 3.21.

The demonstrator consists of readily available discrete components and operates at 2.4 GHz. For a 625 kHz signal bandwidth, the authors report an average cancellation performance of 78 dB and 80 dB for different antenna separations. In the first case, 39 dB of cancellation are attribute to the passive isolation, 33 dB to the mixed-signal cancellation and 6 dB to digital, with a similar but reduced digital contribution in the second case.

A different approach for an in-band FD system is published by Hong *et al.* in 2012, where a passive RF-domain canceler is employed [115], [116]. The canceler uses two fixed delay lines with delays τ_1 and τ_2 and two programmable attenuators in series. The two outputs are summed to generate the cancellation signal with a delay compared to the TX output that is somewhere between τ_1 and τ_2 depending on the attenuator settings. This approach re-

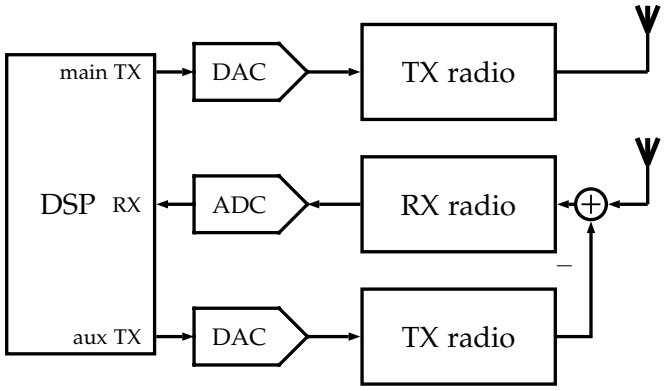


Figure 3.21: In-band FD system by Duarte and Sabharwal employing discrete components [114].

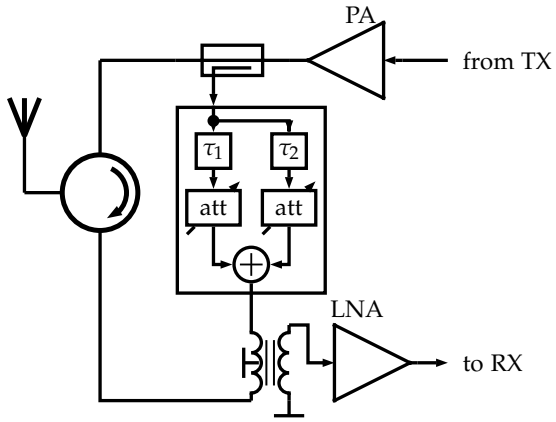


Figure 3.22: In-band FD system by Hong *et al.* [115].

produces the delay of the leakage signal through the circulator decoupling TX and RX. The cancellation signal then is inverted and subtracted at the RX input by means of a transformer. The system is sketched in Figure 3.22.

The fully discrete prototype implements the mentioned delays as microstrip traces on a printed circuit board (PCB). Furthermore, all RF components, such as amplifiers and mixers, are mounted on the same board. Further signal processing and programming of the attenuators is done on an field-

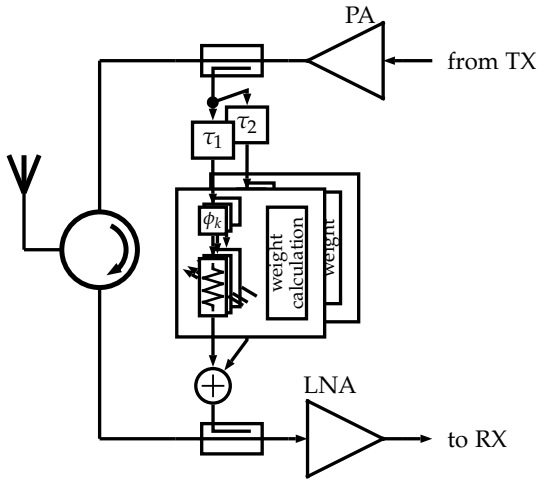


Figure 3.23: RF cancellation system for in-band FD by Choi and Shirani-Mehr [117].

programmable gate array (FPGA). The authors report cancellation of more than 33 dB (more than 46 dB including the circulator) over a 60 MHz bandwidth in the 2.45 GHz industrial, scientific, and medical (ISM) band.

In 2013 Choi and Shirani-Mehr published a similar approach for in-band FD communications [117]–[119]. The RF canceler employs a set of vector modulators, where the reference signal, tapped after the PA in the TX chain, is appropriately delayed and attenuated to match the leakage signal. A special property of this approach is that variations and non-idealities of the delays are compensated. Every delay is composed from a set of individual parallel delay lines, that are weighted accordingly to yield the actual desired phase shift and additionally attenuation.

Furthermore, a LMS-based fully analog algorithm is employed to adapt the individual weights in the delays, and also the delays themselves. The RF cancellation system is sketched in Figure 3.23.

With a discrete prototype, the authors report [118], [119] a RF cancellation performance of more than 56 dB including the circulator for a 20 MHz bandwidth LTE signal at 2.46 GHz carrier frequency. Similarly, for a 1.4 MHz band-

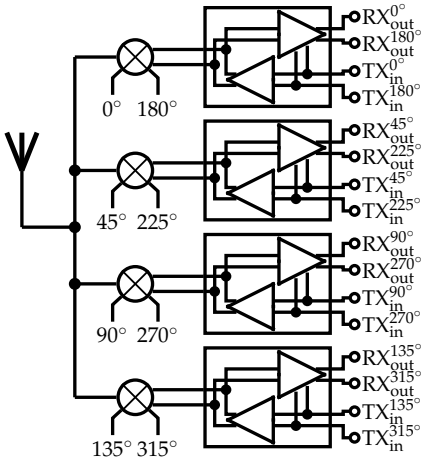


Figure 3.24: Low TX output power in-band FD TRX by Yang *et al.* with TX/RX shared passive mixer [120].

width signal, a cancellation of 79 dB is measured. Further augmenting the approach with a digital nonlinear canceler enhances the cancellation performance to 101.8 dB and 110.9 dB respectively.

For a low power TXs, Yang *et al.* proposed a novel approach suitable exclusively for in-band FD TRXs [120], sharing the up- and downconversion mixer between RX and TX. The general system is sketched in Figure 3.24. The distinct benefit of this approach is that phase noise has no effect on duplex operation, i.e. cancellation of the TX signal.

The mixer obviously must be highly linear to avoid nonlinear distortion of the TX signal as well as cross modulation between the TX and RX signal. For this reason an eight-phase passive CMOS mixer is used offering high linearity. Beneficial for leakage cancellation is the direct connection of the TX output to the RX input in baseband. The cancellation signal also is directly derived in the analog baseband of the TX and canceled in the LNA. A thermal noise canceling LNA [52], [53] is adopted for SIC, similar to the one used by Zhou *et al.* [50] presented in Section 3.1.1, sketched in Figure 3.6.

A major drawback of this solution is the upconversion mixer at the very end of the TX chain. This TX architecture limits the achievable output power. For

moderate to high output powers generally a PA operating in the RF domain is required.

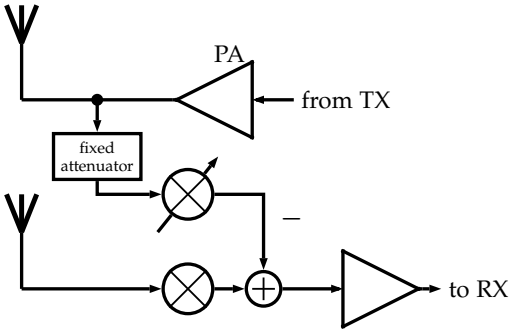
The prototype, fabricated in a 65 nm CMOS technology, occupies an area of 1.5 mm^2 and includes the RF front-end with mixer and RX baseband amplifiers. The TX baseband signal is fed externally to the mixer. The operating frequency range is $0.1 \sim 1.5$ GHz. The maximum achievable TX output power is measured as -7.1 dBm. The authors report a worst case TX-to-RX isolation of 28.3 dB. The reported RX NF ranges from 5 dB to 8 dB, depending on LO frequency. In duplex operation, the NF stays at 5 dB until the TX power reaches -25 dBm. The same test, but the TX signal being injected at the very RF input, yielded a degradation of NF already at -53 dBm, showing the effectiveness of the approach.

A different in-band FD system with SIC based on a passive mixer is published by Broek *et al.* [121]. The reference signal is tapped at the TX output and downconverted with a passive mixer, simultaneously acting as a vector modulator, allowing for programmable attenuation and phase shift. The resulting cancellation signal is canceled in the analog baseband of the passive mixer first RX in front of the baseband amplifier. The system is sketched in Figure 3.25a.

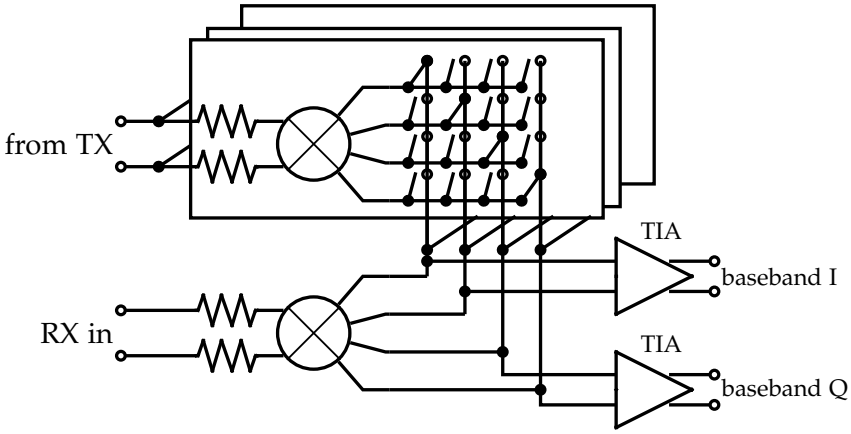
The vector modulator downconverter is sketched in Figure 3.25b. It is a sliced mixer, where each of the outputs can be connected to one of the four baseband virtual ground nodes at the amplifiers' inputs. This way, a set of attenuations and phase shifts can be obtained. Beneficial to this architecture is that solely passive linear components, apart from the mixer switches, are used in the canceler, maintaining linearity.

The prototype, manufactured in a 65 nm CMOS technology, occupies an area of 1.4×1.4 mm^2. The optimum worst case cancellation performance, for a 16.25 MHz bandwidth Wi-Fi like signal at 2.5 GHz, is reported as 27 dB. The RX NF of 6.2 dB is degraded by the canceler to 10.3 dB at maximum amplitude settings and further to 12.3 dB when the canceler is operating at its minimum possible amplitude.

There are many more publications on enabling in-band FD communications, especially lately as SIC and in-band FD heavily gained traction and interest in



(a) TRX system overview.



(b) Vector modulator downconverter.

Figure 3.25: In-band FD system with vector modulator downconverter based SIC by Broek *et al.* [121].

the research community. The presented selection mainly covers contributions focusing on analog and RF domain cancellation.

Most of the in-band FD approaches are also applicable to FDD systems and vice versa. Filtering approaches presented in Section 3.1 do not apply to in-band FD, as TX and RX bands overlap. Similarly, sharing of the LOs or otherwise exploiting the frequency overlap does not apply to FDD systems.

Concluding this section, it is made obvious to the reader that for in-band FD systems a combination of two or more SIC mechanisms are required. As al-

ready detailed in Section 2.2, 100 dB of cancellation or more are necessary. At least a digital cancellation approach is required in addition to the presented approaches, although not specifically focused in this overview.

4 Single-Chip Mixed-Signal RF-Domain Self-Interference Cancellation System and Prototype Architecture

Within this chapter the targets and requirements of the prototype developed in this work as well as several system level aspects are discussed. A mixed-signal RF domain SIC system for modern multi-standard wireless mobile TRX systems is designed and implemented by means of an integrated demonstrator. The main goal is to enhance FDD operation with an option for in-band FD whether suitable.

Judging by the preceding review of existing SIC systems, two key observations can be made:

- The cancellation signal should be injected as early as possible in the RX chain, e.g. at the very input of the RX in the RF domain. This way, desensitization of the analog components due to SI in the RX can be alleviated or even avoided by means of SIC.
- The essential feature for acceptable cancellation performance over a wide range of scenarios, supporting multiple communication standards, and being easily extensible for future applications, is the correct and comprehensive adaptation of the canceler to varying environmental conditions. Generally, the leakage channel from the TX to the RX must be suitably estimated and continuously tracked over time. Hence, the canceler can reproduce the actual SI present at the RX. The most versatile approach to this issue is DSP to estimate and track the leakage channel and to further generate a suitable cancellation signal.

The obvious conclusion from these two observations is to opt for a mixed-signal solution. Injection of the cancellation signal is performed in the RF domain. The synthesis of this cancellation signal, derived from the reference, is done digitally.

Such an approach maintains a maximum of flexibility, since the actual signal processing is entirely done in the digital domain and possibly programmable. Thus a multitude of signals and standards can be supported by properly choosing suitable algorithms on demand. Also, coexistence can be potentially eased, e.g. canceling a Wi-Fi signal from an LTE RX, given the respective digital data are available. Further, such digital intensive solutions heavily benefit from CMOS technology scaling, increasing processing capability while simultaneously decreasing power consumption [122].

Also RF circuitry generally benefits from advances in CMOS manufacturing [123], [124] with increasing transistor transition frequencies and decreasing parasitic capacitances. Further, successful attempts on digitizing RF functionality leverage both signal processing and technology benefits. This includes benefits for both the RX, including high oversampling ratios (OSRs) and clock frequencies for ADCs [35], [125], and the TX, implementing digital intensive and fully digital transmitter architectures [126], [127].

The key component for efficient digital transmitters is the RF-DAC [9], [34], [100], [128]–[130]. It provides the conversion of the digital input data directly into the RF domain. It is clocked with the LO and inherently provides the upconversion mixing. The input signals are sampled either directly with the LO, or with a related frequency, e.g. half or quarter thereof. Such an RF-DAC, adapted to the needs of the developed SIC approach, is a suitable candidate for the proposed mixed-signal SIC system.

The general architecture of the developed mixed-signal SIC system is shown in Figure 4.1. The block diagram looks similar to previous mixed-signal SIC approached discussed in Chapter 3, e.g. the early approach of Schacherbauer *et al.* for FDD [8], [91], [92] or similarly Duarte and Sabharwal's solution for FD applications [18], [114].

The key differences of this work to previous mixed-signal SIC approaches are:

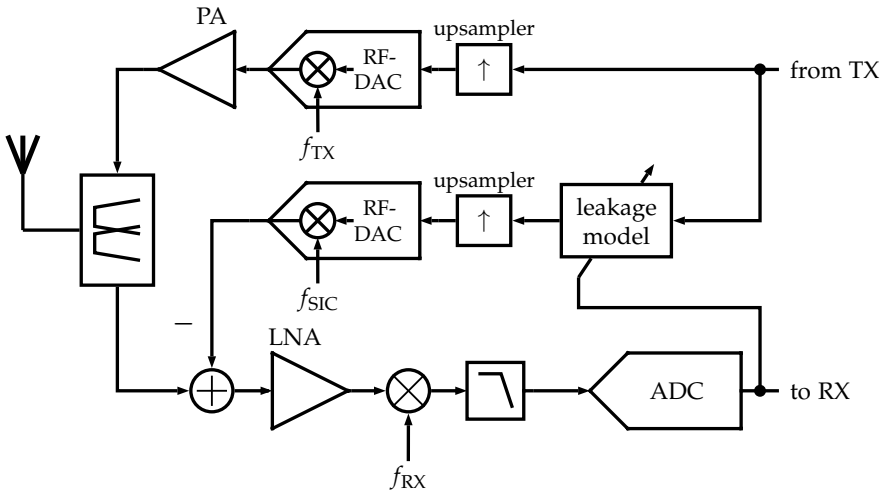


Figure 4.1: Developed mixed-signal SIC system.

- **Single-chip integration**: This work is integrated in a single-chip CMOS TRX system without the need for external components dedicated to SIC. This is key for high performance operation and applicability in future commercial TRX systems.
- **CMOS technology**: This work leverages the benefits of recent advances in CMOS manufacturing. It is implemented in an advanced 28 nm bulk-CMOS technology.
- **Digital intensive circuits**: The SIC system further exploits the gains of DSP and CMOS technology by employing digital intensive and digital-like circuits, such as the RF-DAC.

Although sketched for FDD applications in Figure 4.1, the system can be easily adapted for in-band FD. The duplexer can be replaced by e.g. a circulator and for a FD system, all mixing blocks would share their LO.

4.1 Transceiver Circuit Blocks

Circuit level design aspects of the TRX and developed SIC are covered in Chapter 6.

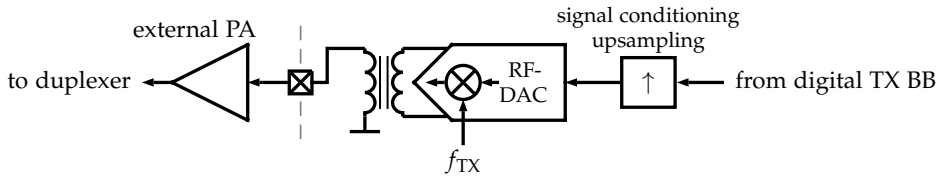


Figure 4.2: Employed TX system in the prototype TRX.

4.1.1 Transmitter

Designing the TX is not part of this work. A readily available commercial TX system [131], based on a quadrature capacitive RF-DAC [9], [34], [100], [130] is integrated in the TRX.

An integrated transformer based matching network, used for differential to single-ended conversion and impedance matching to 50 Ω, is used to drive the external PAs operating in the LTE mid- and high bands ranging from 1.4 GHz up to 2.7 GHz. The essential TX block diagram is shown in Figure 4.2.

The TX system supports LTE, UMTS, GSM, and related standards in time division duplex (TDD) and FDD modes. The maximum peak output power of the system, as required by the standards, is at least 34 dBm at the antenna for 7 dB PAPR. The TX exhibits excellent OOB noise and emission performance, e.g. below −157 dBc/Hz at 80 MHz offset for peak output powers.

This work does not modify the TX, apart from obtaining its (upsampled) input data as the reference signal. Additionally, the (upsampled) input data to the TX may be delayed to account for additional signal processing in the cancellation chain.

4.1.2 Receiver

Similarly to the TX, general development and design of the RX is not part of this work. Again, a commercially available RX subsystem [131] is expanded by means of signal injection for the developed SIC and integrated into the TRX.

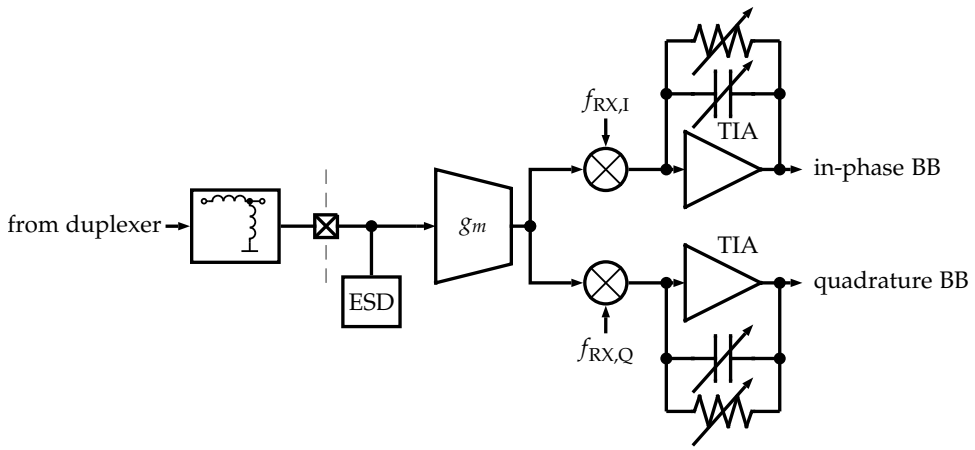


Figure 4.3: Employed RX system in the prototype TRX.

Also the RX system supports LTE, UMTS, GSM, and related standards in TDD and FDD modes. It supports contiguous signal bandwidths exceeding 40 MHz.

The essential architecture of the original RX is shown in Figure 4.3. A low noise transconductance amplifier is externally impedance matched to 50 Ω. The RF output signal is downconverted into the in-phase and quadrature analog baseband signals by a single-balanced passive mixer, driven by 25 % duty cycle LOs. Transimpedance amplifiers (TIAs) properly terminate the mixers with their input impedances and provide (programmable) low pass filtering.

4.2 Mixed-Signal RF-Domain Self-Interference Cancellation

The actual SIC system, sketched in Figure 4.4, consists of three main portions:

- **DSP circuitry** to generate an appropriate cancellation signal and properly precondition it

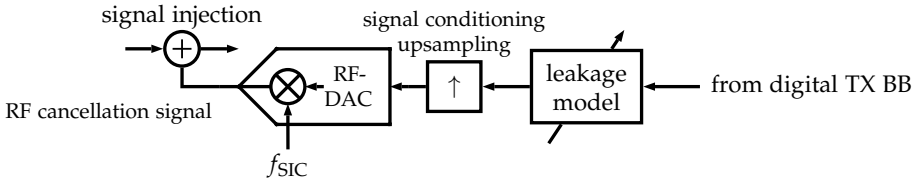


Figure 4.4: Developed SIC portion of the TRX system.

- an **RF-DAC** to convert the digital cancellation signal directly to the RF domain
- **means of injection** of this analog RF signal at the RX input to cancel the actual SI signal

The main focus of this work lies on the design and implementation of the cancellation RF-DAC and the injection of its output signal into the RX. While the signal processing portion is by far not a trivial task, the main challenge posed by this concept lies in the mixed-signal circuit implementation.

There are two key specifications that define the performance and applicability of the proposed SIC system which mainly influence circuit design: first, the maximum peak power of the leakage signal that needs to be canceled, and second, the tolerable noise added by the canceler in the RX band. Further parameters include e.g. canceler linearity. Of course there are many more specifications that influence circuit design, but they are not necessarily specific to SIC, e.g. power consumption, operating frequencies, supply voltages, etc.

In the demonstrator, a suitable duplexer, providing minimally 50 dB of TX-to-RX isolation, is used. For in-band FD applications, a circulator or similar means of passive isolation are adapted to emulate practical scenarios.

4.2.1 Maximum Leakage Power

The maximum leakage power that is to be expected is essentially determined by the maximum transmit antenna power required by the wireless standards the TRX supports. For LTE FDD bands, the specified maximum root mean square (RMS) power at the antenna is 23 dBm [132].

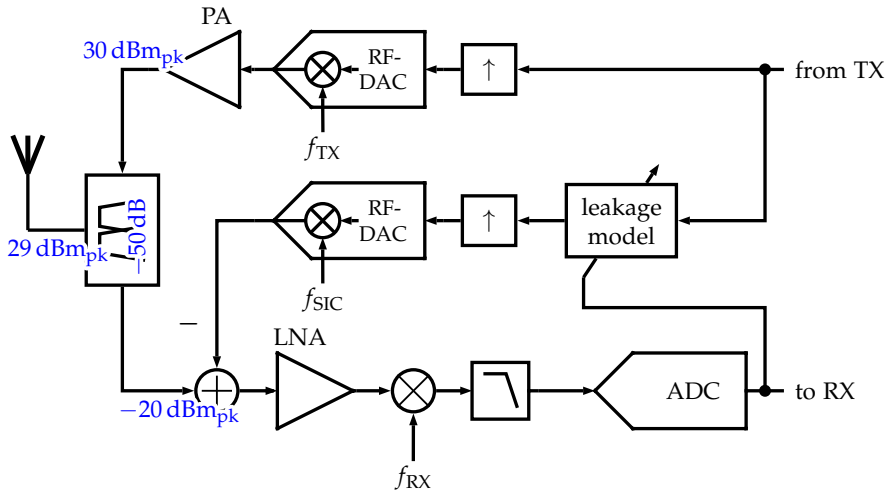


Figure 4.5: SI signal levels in the TRX system.

Assuming TX-to-antenna losses of 1 dB and a reasonable PAPR of 6 dB [133], the expected maximum peak power at the duplexer's TX input is approximately 30 dBm. Assuming further a worst case TX-to-RX isolation of 50 dB, the expected maximum peak leakage power at the RX input is −20 dBm or 10 µW. These relations are sketched in Figure 4.5. At a perfectly matched 50 Ω input, these leakage levels translate to a voltage swing of more than 22 mV.

For comparison, the specified minimum sensitivity level, i.e. the minimum signal power the RX must be able to correctly process, is maximally −90 dBm (or 1 pW) and bandwidth dependent, i.e. lower signal powers for lower bandwidths [132]. Essentially, there can be more than seven decades of power between the SI signal and the desired RX signal.

4.2.2 Canceler Noise in RX-Band

Another function of the duplexer in such a TRX system sketched in Figure 4.1 is the attenuation of TX OOB noise desensitizing the RX. Still, in these otherwise filterless architectures, very low OOB emissions, e.g. spurs, thermal, and phase noise, of the TX is key for high performance FDD operation. Further

coexistence with other radios similarly requires low OOB emissions, e.g. to simultaneously operate cellular and geolocation services [134].

The same, at least for FDD operation, holds true for operating the SIC system. In this case, any noise or other unwanted emissions falling into the RX band directly impair the RX performance by increasing its noise floor.

Assuming that the RX noise floor is dominated by the inevitably present thermal noise of $-174\,\mathrm{dBm/Hz}$ at room temperature, one can calculate how additional noise from the TX and/or canceler impacts the RX. Taking the previously mentioned $-157\,\mathrm{dBc/Hz}$ of the TX at 24 dBm RMS output power results in an OOB noise level of $-133\,\mathrm{dBm/Hz}$ at the duplexer's TX port. Assuming the worst case TX-to-RX attenuation of 50 dB, the TX-in-RX band noise level is at $-183\,\mathrm{dBm/Hz}$. Eventually, this raises the thermal noise floor by approximately 0.5 dB. The calculation for canceler OOB noise into the RX band is analogous.

For lower TX powers, the absolute OOB noise levels can stay the same in terms of absolute power. E.g. for each dB of decrease in TX power, the relative noise (in dBc) can increase by 1 dB. The same holds true also for the canceler.

4.2.3 Canceler Linearity

The linearity of the canceler has an impact on cancellation performance and unwanted harmonic signal components injected into the RX. In order to achieve a certain cancellation performance, the linearity must be at least as good. In other words, all harmonic components must be of lower power compared to the desired cancellation level. Otherwise these nonlinear signal portions stay residual, again degrading the system performance. Furthermore, nonlinear signal components generated in the RX band by the canceler are also highly undesired, as they are experienced again as interference by the RX [135].

Luckily, in the proposed SIC architecture, the linearity requirements can be greatly alleviated. Since the cancellation signal is generated in the digital domain, also digital predistortion mechanisms and algorithms [79], [136], to

linearize the canceler, can be applied. Such measures are generally a great relief for RF-DAC circuit design.

4.2.4 Canceler Resolution

The impact of the canceler's resolution on cancellation performance has been investigated by Schacherbauer [92]. Unfortunately though, the analysis is purely based on the cancellation DAC's SNR, which does not account for sampling frequency. The main result presented by Schacherbauer in terms of achievable cancellation depth is

$$\text{canc}|_{\text{dB}} = 20\ \log_{10}\left(\frac{1}{2\cdot 2^{N_e}}\right) \approx -(B_e+1)\cdot 6.02\,\text{dB} \tag{4.1}$$

where N_e is the effective number of bits, i.e. the (ideally chosen) cancellation signal is $c_{\text{rms}} = V_{\text{LSB}}\cdot 2^{N_e}$ on average and $V_{\text{LSB}} = \frac{V_{\text{FS}}}{2^{N_B}-1}$ the quantization step. This analysis does not account for the sampling frequency, thus potentially heavily overspecifying the converter.

If the assumption of a white quantization noise spectrum is valid, which generally is the case for practical signals used in communications systems [137], the quantization noise spreads equally over the converter's Nyquist bandwidth. Thus, for uniformly distributed quantization noise, the resulting noise density, normalized to the cancellation signal power, can be approximated with

$$N_Q|_{\text{dBc/Hz}} = 10\ \log_{10}\left(\frac{V_{\text{LSB}}^2}{12}\,\frac{1}{\frac{f_{\text{LO}}}{2}}\,\frac{1}{c_{\text{rms}}^2}\right) = 10\ \log_{10}\left(\frac{1}{6\cdot f_{\text{LO}}\cdot\left(2^{N_e}\right)^2}\right) \tag{4.2}$$

Thus, for an ideal converter with an ideally chosen cancellation signal, the quantization noise power in the signal band of interest, i.e. in the TX bandwidth, is the achievable limit of cancellation. For a cancellation bandwidth B_{canc}, the total quantization noise power, normalized to the cancellation signal power, is

$$N_{Q,B}|_{\text{dBc}} = 10\ \log_{10}\left(\frac{B_{\text{canc}}}{6\cdot f_{\text{LO}}\cdot\left(2^{N_e}\right)^2}\right) \tag{4.3}$$

For an LO frequency of 1.4 GHz, which is also the sampling frequency, and a large signal bandwidth of 200 MHz, the achievable cancellation due to quantization noise already exceeds 40 dB for only four bits. With Schacherbauer's result [92], a cancellation of only 30 dB is predicted incorrectly.

For the architecture at hand, the main driver in the resolution specification is rather dominated by the required OOB noise performance discussed in Section 4.2.2. The resolution of the canceler directly influences the quantization noise deposited in the RX band. The expected quantization noise density is given by (4.2). For ten bits of effective resolution at $f_{\mathrm{LO}} = 2\,\mathrm{GHz}$, the quantization noise density is $-164\,\mathrm{dBc/Hz}$, which might be insufficient for the previously mentioned $-157\,\mathrm{dBc/Hz}$ in the RX band. Therefore, resolutions greater than ten bits are required to obviate degradation of RX performance, essentially not posing practical limits on cancellation depth.

4.2.5 Cancellation RF-DAC Local Oscillator and Sampling Frequency

The employed LO frequency of the RF-DAC eventually also determines its sampling frequency. In Figure 4.1, the LO frequency of the cancellation RF-DAC is only indicated as f_{SIC}. Pragmatically, there are two options: the TX LO frequency and the RX LO frequency. Both options offer a distinct set of benefits.

Since the leakage signal, that is to be canceled, is centered around the TX frequency, it seems straightforward to directly use this same LO signal for the cancellation RF-DAC. The TX digital baseband can be readily used with suitable sampling for cancellation signal generation. Further, the cancellation RF-DAC's signal bands are centered around 0 Hz, resulting in low overall signal bandwidths and high effective OSRs, improving the RF-DAC's performance.

Unfortunately, this might not be the optimum choice. Assuming that the cancellation RF-DAC is placed in direct vicinity of the SIC enabled RX on the TRX system, this approach would require the TX LO to be fed to the RF-DAC. This implies routing the TX LO into the RX, which are potentially physically separated to avoid unnecessary crosstalk and coupling effects. Reintroducing

this LO there gives rise to even more SI phenomena. Furthermore, distributing such a noise critical LO signal over longer distances consumes a lot of power that may be better spent elsewhere.

Another undesired effect can be the resampling of the cancellation signal with the RX LO frequency, which implicitly happens due to the passive mixing operation, that is originally sampled with the TX LO. The two LO frequencies are separated by the so called duplex distance, which is specified individually for each band in the wireless communication standards. The impact of this effect greatly depends on the cancellation RF-DAC's output filtering and image suppression, but may not be negligible.

Given the baseband signal $b(t)$ and it's frequency domain representation $B(j\omega)$, the RF-DAC's output signal is

$$x(t) = \int_{-\infty}^{\infty} g(\chi) \left(\mathrm{e}^{j2\pi f_{\mathrm{TX}}(t-\chi)} \int_{-\infty}^{\infty} \sum_{k=-\infty}^{\infty} b\left(\frac{k}{f_{\mathrm{TX}}}\right) \delta\left(\tau - \frac{k}{f_{\mathrm{TX}}}\right) h(t-\chi-\tau) d\tau \right) d\chi \tag{4.4}$$

where $\delta(t)$ is the Dirac delta and $h(t)$ is the impulse response of the reconstruction process (e.g. zero-order hold (ZOH)) and $g(t)$ the impulse response of any filtering applied at the RF-DAC's output. Alternatively, in the frequency domain

$$X(j\omega) = f_{\mathrm{TX}} \cdot G(j\omega) \cdot H(j\omega - j2\pi f_{\mathrm{TX}}) \cdot \sum_{k=-\infty}^{\infty} B(j\omega - k \cdot j2\pi f_{\mathrm{TX}}) \tag{4.5}$$

where $G(j\omega)$ and $H(j\omega)$ are the frequency domain representations of $g(t)$ and $h(t)$ respectively. As expected, the sampling images appear at multiples of the sampling frequency f_{TX} and are weighted by the reconstruction process $H(j\omega)$ and the output filter $G(j\omega)$.

With the passive mixing downconversion, effectively the RF-DAC output is resampled with the RX frequency f_{RX}. The effective output then is

$$r(t) = \mathrm{e}^{-j2\pi f_{\mathrm{RX}}} \sum_{k=-\infty}^{\infty} x\left(\frac{k}{f_{\mathrm{RX}}}\right) \delta\left(t - \frac{k}{f_{\mathrm{RX}}}\right) \tag{4.6}$$

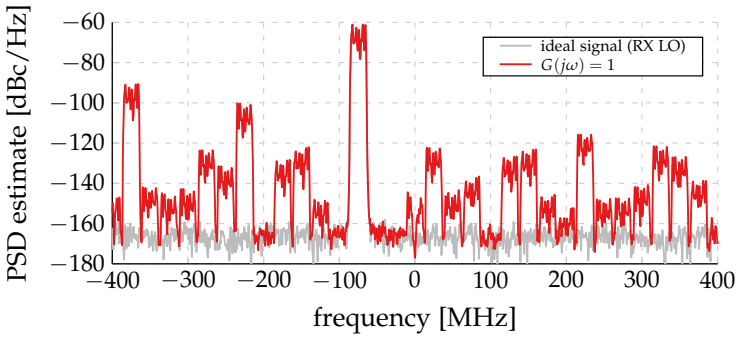
and in the frequency domain

$$\begin{aligned} R(j\omega) &= f_{\mathrm{RX}} \sum_{k=-\infty}^{\infty} X(j\omega - k \cdot j2\pi f_{\mathrm{RX}}) \\ &= f_{\mathrm{RX}} f_{\mathrm{TX}} \sum_{k=-\infty}^{\infty} \Bigg[G(j\omega - k \cdot j2\pi f_{\mathrm{RX}}) H(j\omega - j2\pi(f_{\mathrm{TX}} - k f_{\mathrm{RX}})) \\ &\qquad \sum_{l=-\infty}^{\infty} B(j\omega - l \cdot j2\pi f_{\mathrm{TX}} - j2\pi(f_{\mathrm{TX}} - k f_{\mathrm{RX}})) \Bigg] \end{aligned} \tag{4.7}$$

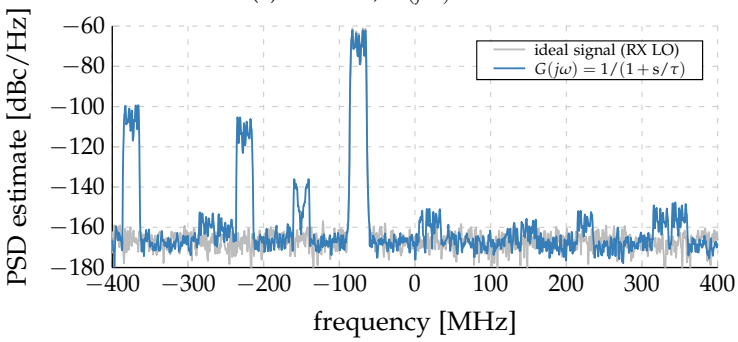
Effectively, as shown in Figure 4.6 for different output filters $G(j\omega)$, images of the cancellation signal are generated by the resampling, some of them directly falling close to 0 Hz in the RX baseband. For the RX, these images are another source of SI. As this effect depends on the duplex distance, specific LO frequencies, and the RX bandwidth, generally this kind of operation is only possible when sufficiently attenuating any sampling images at the cancellation RF-DAC's output.

The obvious solution to this issue, when such images cannot be sufficiently filtered, is using the RX LO for the cancellation RF-DAC. This obviously implies resampling either the TX or the cancellation data with an asynchronous or fractional sample rate converter [138]–[140], which can be a costly operation, but these images can be digitally suppressed. Furthermore, a digital frequency shift by the duplex distance is required to eventually synthesize the signal at the TX frequency as desired, e.g. the leakage signal is centered around $f_{\mathrm{TX}} - f_{\mathrm{RX}}$ in baseband when using the RX LO. This implies very high signal bandwidths for the cancellation RF-DAC, reducing the effective OSR, even though the signal spectrum is sparsely occupied.

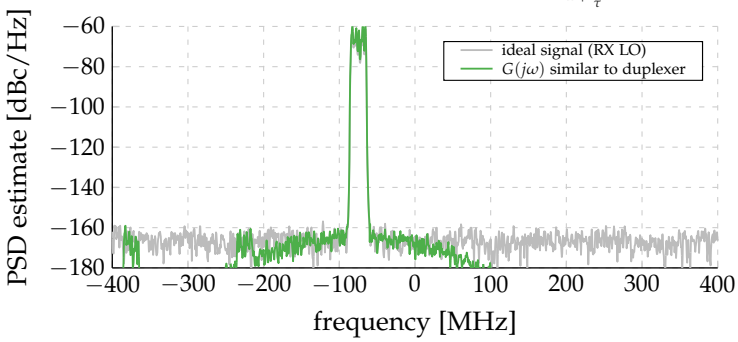
Beneficial to this approach though, apart from avoiding folding of sampling images, is the direct availability of the RX LO for the cancellation RF-DAC. Routing the TX LO signal into the RX is not required, hence avoiding crosstalk and coupling effects and significantly reducing power consumption.



(a) No filter, $G(j\omega) = 1$.



(b) Single pole low pass filter, $G(j\omega) = \frac{1}{1+\frac{s}{\tau}}$.



(c) Duplexer-like band pass filter with a minimum stop band attenuation of 50 dB.

Figure 4.6: Example RX BB spectra when applying different filters $G(j\omega)$. $f_{\mathrm{TX}} = 2\,\mathrm{GHz}$ and $f_{\mathrm{RX}} = 2.075\,\mathrm{GHz}$ with a signal bandwidth of 20 MHz and 13 bit quantization.

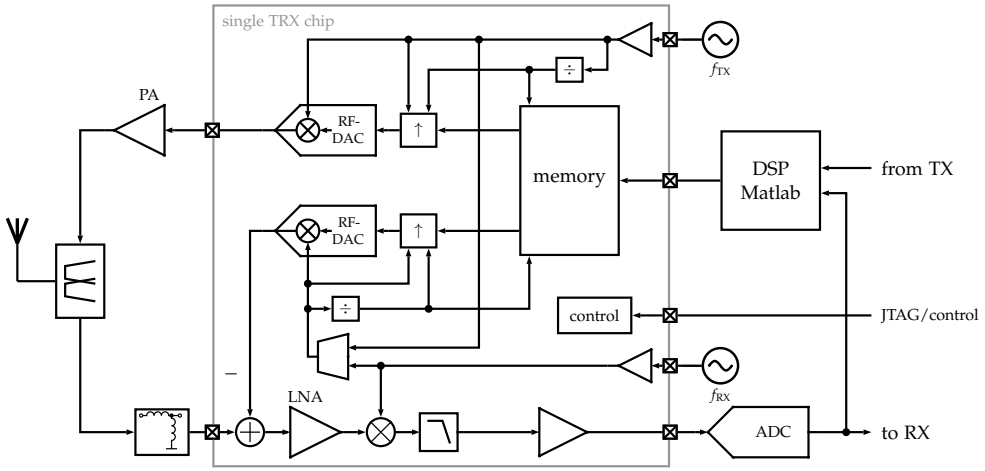


Figure 4.7: Developed mixed-signal SIC prototype demonstrator.

4.3 Integrated Mixed-Signal RF Domain Self-Interference Cancellation Prototype

In order to demonstrate the feasibility of this integrated mixed-signal RF domain SIC approach, a prototype is developed. Previously introduced wireless TRX components are adopted and enhanced with the proposed mixed-signal SIC. Eventually, an integrated, SIC-capable, TRX system is developed.

4.3.1 Prototype Architecture

The general architecture of the demonstrator is sketched in Figure 4.7. Integrated on the same chip are the previously discussed digital TX, the analog and RF portions of the RX, and the mixed-signal RF domain SIC system, including injection into the RX.

For ease of implementation of the demonstrator, to reduce complexity, and to bring the system design and implementation efforts down to a manageable time frame, some obvious simplifications have been applied.

First, a memory based approach is chosen, no high speed real time interfaces are required. Memories are employed for both the TX and SIC RF-DACs, that can be programmed and controlled individually. Synchronously starting the individual data streams to the RF-DACs is enabled by dedicated control registers.

With this approach, unfortunately, no real time digital adaptation can be performed. This drawback can be easily mitigated by applying block level adaptation algorithms, that operate on longer blocks of signals.

Second, on the RX side, only the analog and RF portions are included in the single chip TRX system. The baseband RX signal is digitized externally by an ADC or other measurement equipment. This approach increases flexibility, reduces the complexity of memory controllers, and decreases the required memory size.

On the other hand, several options for performance enhancements and investigations are implemented. This includes two separate LO distribution networks for RX and TX LOs, where one of the two can be fed to the SIC system, chosen programmatically. All sample rate conversions are fully programmable, allowing for different conversion ratios, including fractional ratios. Further, the externalization of PA, matching network, and RX ADC allow for increased flexibility. This is also true for the duplexer, which, since it is external, can be directly replaced by alternative models or even circulators and attenuators and such, allowing for a multitude of testing and analysis options.

Finally, employing a fully software driven DSP approach, e.g. based on numerical computing software such as Matlab, or FPGA based solutions, offer an utmost of flexibility, allowing to fully concentrate on the mixed-signal RF domain circuitry.

4.3.2 Self-Interference Cancellation Specification

Practical specifications for the developed mixed-signal RF domain SIC system are derived from the previous analyses. Some specifications are defined by the system architecture and overall targets for a product-like TRX. The prototype, which is used to demonstrate the feasibility of this SIC approach,

implements a subset of a TRX fully supporting cellular standards, i.e. with reduced operating frequencies, to focus on the analog, RF, and mixed-signal circuitry.

Main specifications for the SIC system include:

- **operating frequency range**: 1.4 GHz $\sim$ 2.7 GHz to cover LTE mid- and high-bands
- **cancelable leakage power**: more than $-20\,\mathrm{dBm_{peak}}$ at the RX input
- **RX noise degradation**: NF degradation less than 3 dB
- **cancellation depth**: better than 20 dB for static scenarios
- **implementation aspects**:
  - usage of an already existing LO in the system, e.g. the TX's or RX's LO
  - no additional on-chip inductors, minimizing the area overhead and newly introduced cross talk

5 Quadrature and Multiphase Local Oscillator Generation

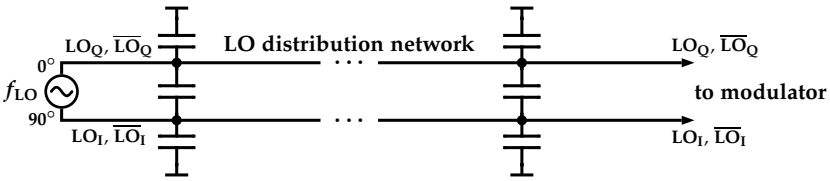
As discussed in Chapter 4, the proposed mixed-signal SIC system's RF-DAC needs LO signals to perform the digital to RF domain conversion. Readily available on the TRX are the TX and RX LOs. Even though the SIC system should be placed closely to the cancellation augmented RXs, a substantial amount of current needs to be spent on distributing either one of the LO signals to the mixed-signal SIC RF-DAC.

In wireless TRX systems, a significant part of the dissipated power is spent on clock and LO distribution. Generally, including the SIC system, quadrature amplitude modulation schemes are employed, which require quadrature (I/Q) LO signals. Silicon area of such integrated TRX system can be up to tens of mm^2 [141], [142], which aggravate the power spent on LO distribution.

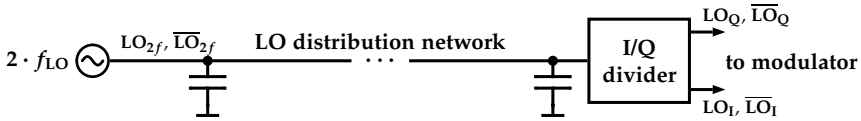
The need for quadrature LOs (two 90° shifted LO signals) further worsens the power consumption of the LO distribution: since I/Q LOs consist of two individual LO phases, the power needed for their distribution is approximately doubled compared to distributing only a single phase at the same frequency, as sketched in Figure 5.1a.

Alternatively, twice the desired output frequency can be distributed (see Figure 5.1b), but this hardly improves the power spent on distributing these signals. Additionally, the LO phase with doubled frequency needs to be divided down into the desired I/Q outputs [143].

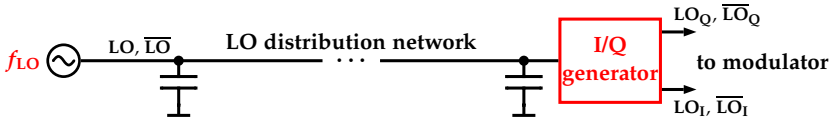
This problem is especially severe when distributing noise critical LO signals as required in wireless TRXs and for SIC. Due to immunity reasons, these signals are usually distributed differentially and special layout considerations, such as shields and guards, are employed, which even further increase capacitive loading and therefore power consumption.



(a) In-phase and quadrature LOs distributed separately.



(b) Single phase LO distribution at doubled frequency with quadrature divider.



(c) Proposed LO distribution at desired output frequency with quadrature generator.

Figure 5.1: I/Q LO distribution scenarios.

To counter the increased power consumption of the I/Q LO distribution, only one LO phase is distributed across the system and quadrature LO phases are generated locally at the same frequency, as shown in Figure 5.1c. Later in this chapter, in Section 5.2, also local multiphase generation based on the proposed circuit architecture is discussed.

Conventional I/Q generators have been published for sinusoidal signals [144], [145] as well as for CMOS trapezoidal LO signals [143], [146]–[150], especially delay-locked loops. These solutions either extensively rely on passive components or employ complicated, thus power hungry, circuit structures. These properties of conventional architectures pose limits to low power consumption and adequate noise performance required for wireless TRXs. Furthermore, some circuits do not allow operation in advanced CMOS technologies due to limitations on supply voltages amongst other things.

In this work, a novel approach to quadrature [151]–[153] and multiphase generation [154], [155] capable of superior noise performance and low power consumption, is developed. The architecture relies on matched delays and linear phase interpolation to generate I/Q outputs at the LO input frequency.

The architecture allows for a low number of devices, which is beneficial for low power consumption and good noise performance. The required circuit blocks can be implemented in a digital manner, which enables low supply voltages. Furthermore, the circuit can benefit from technology scaling.

5.1 Quadrature Generation

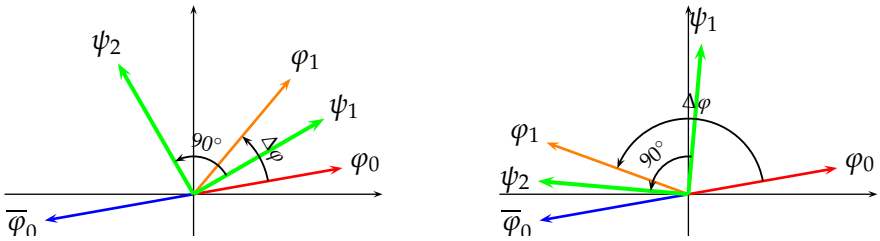
First, the more specialized application of quadrature generation is presented in this section. Measurement results of a fabricated prototype test chip are included. Second, in Section 5.2 the generalization, i.e. multiphase generation, of the circuit architecture is discussed.

5.1.1 Operating Principle

The principal idea of the developed circuit architecture is linear interpolation of two 180° shifted inputs to obtain outputs with the desired 90° phase shift. In wireless TRX and other noise critical applications the LO signals in question are usually distributed differentially. Therefore, both the LO signal as well as its inverse $\overline{\text{LO}}$ are available. Assuming the conventional 50 % duty cycle, the two individual signals inherently exhibit the required 180° phase shift.

Practical direct phase interpolators are unable to linearly interpolate the LO and $\overline{\text{LO}}$ signal, since the input signals to such phase interpolators require overlapping transitions [156]. The presented principle uses additional phase shifts to generate auxiliary signals, enabling the linear phase interpolation of the two 180° shifted input signals LO and $\overline{\text{LO}}$.

The novel operating principle is explained with phases in the phase space. A phase φ is a special representation of a periodic signal $x(t) = x(t - nT)$ with period T ($n \in \mathbb{Z}$). The value of the phase φ is defined as its phase shift compared to a reference phase with a phase shift of 0°. If the reference time signal is $x(t)$, then the phase φ represents the time signal $x\left(t - \frac{\varphi}{360°} \cdot T\right)$, $x(t)$ delayed by $\frac{\varphi}{360°} \cdot T$.



(a) Small $\Delta\varphi$.

(b) Large $\Delta\varphi$.

Figure 5.2: Quadrature phase generation principle with different phase shifts $\Delta\varphi$ of the auxiliary phase φ_1 [151], [152].

To illustrate the essential idea of this new principle, auxiliary phases are introduced step-by-step to obtain the implementable differential quadrature phase generator.

Starting with the two 180° shifted input signals LO and $\overline{\text{LO}}$ in their phase representation φ_0 (corresponding to LO) and $\overline{\varphi}_0$ (corresponding to the $\overline{\text{LO}}$ input) the auxiliary phase φ_1 is generated with a phase shifter so that

$$\varphi_1 = \varphi_0 + \Delta\varphi \tag{5.1}$$

with an arbitrary but fixed phase shift $\Delta\varphi$ from the input φ_0.

Next, the output phases ψ_1 (quadrature LO) and ψ_2 (in-phase LO) are constructed with linear phase interpolation. The phases φ_0 and φ_1 are interpolated to yield

$$\psi_1 = \frac{1}{2}(\varphi_0 + \varphi_1) = \varphi_0 + \frac{\Delta\varphi}{2} \tag{5.2}$$

The phases φ_1 and $\overline{\varphi}_0 = \varphi_0 + 180°$ are interpolated to create

$$\psi_2 = \frac{1}{2}(\varphi_1 + \overline{\varphi}_0) = \varphi_0 + \frac{\Delta\varphi}{2} + 90° \tag{5.3}$$

The phase difference obviously is $\psi_2 - \psi_1 = 90°$ as desired for quadrature LO phases *independently* of the previously chosen phase shift $\Delta\varphi$. The phase relationship is shown in phasor diagrams in Figure 5.2 for different values of $\Delta\varphi$.

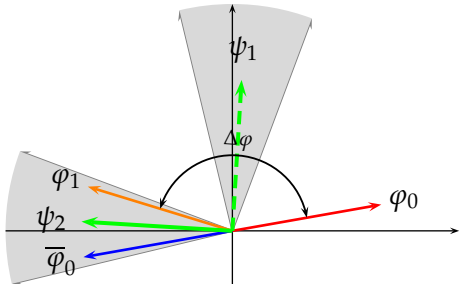


Figure 5.3: Choosing $\Delta\varphi$ to obtain linear phase interpolation of the output ψ_2. The shaded areas indicate the linear interpolation regions of practical phase interpolators [152].

Of course, solely introducing one auxiliary phase φ_1 is not sufficient. The phase differences of the interpolated signals are still too big for simple implementable linear phase interpolation. A simple practical phase interpolator (see Section 5.1.3.2) operates only linearly, if the phase difference of its input phases is sufficiently small.

The phase differences of the interpolated phases φ_0, φ_1, and $\overline{\varphi}_0$ are $\varphi_1 - \varphi_0 = \Delta\varphi$ and $\overline{\varphi}_0 - \varphi_1 = 180° - \Delta\varphi$. They are dependent on the chosen value of the phase shift $\Delta\varphi$ and cannot be made arbitrarily small for both interpolated outputs ψ_1 and ψ_2 simultaneously. If such behavior of independent phase differences is achieved, practical and implementable linear phase interpolators can be employed.

Therefore, the principle is extended to enable implementable linear phase interpolation. First, the phase shift $\Delta\varphi$ is chosen so that the second output ψ_2 can directly be generated with linear phase interpolation as shown in Figure 5.3. The gray shaded sectors in this figure indicate the linear interpolation region for a practical phase interpolator for the desired output.

Second, linear interpolation for the first output ψ_1 requires additional auxiliary phases. These phases, denoted as λ_1^- and λ_1^+, are introduced as shown in Figure 5.4, placed symmetrically around the desired output ψ_1. Linear interpolation of λ_1^- and λ_1^+ will therefore result in the desired output ψ_1.

Placement of the two additional phases as described implies equal phase shifts between the input φ_0 and the first additional auxiliary phase λ_1^-, de-

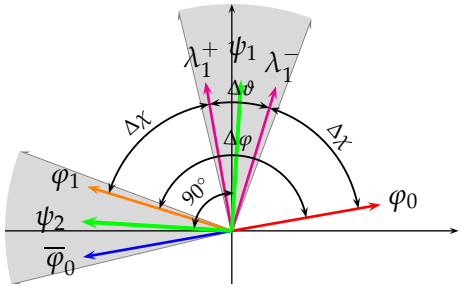


Figure 5.4: Quadrature phase generation principle with additional auxiliary phases to enable operation with real circuit components. The shaded areas indicate the linear interpolation regions of practical phase interpolators [151], [152].

noted as $\Delta\chi$, and the second additional phase λ_1^+ and the original auxiliary phase φ_1: $\lambda_1^- - \varphi_0 = \Delta\chi$ and $\varphi_1 - \lambda_1^+ = \Delta\chi$.

Alternatively, $\lambda_1^- = \varphi_0 + \Delta\chi$ and $\lambda_1^+ = \varphi_1 - \Delta\chi$. Interpolation of the two additional phases for the first output ψ_1 yields

$$\psi_1 = \frac{\lambda_1^- + \lambda_1^+}{2} = \frac{\varphi_0 + \Delta\chi + \varphi_1 - \Delta\chi}{2} = \varphi_0 + \frac{\Delta\varphi}{2} \tag{5.4}$$

which is the same as obtained previously.

The additional phases can be easily obtained by partitioning the original phase shift $\Delta\varphi$ into three parts: first, $\Delta\chi$ to obtain λ_1^-, second $\Delta\vartheta$ to get λ_1^+ and third again $\Delta\chi$ to finally create φ_1. The original phase shift is $\Delta\varphi = \Delta\chi + \Delta\vartheta + \Delta\chi$, where $\Delta\vartheta$ is the residue phase difference of λ_1^- and λ_1^+, i.e. $\Delta\vartheta = \Delta\varphi - 2\,\Delta\chi$. This phase shift determines whether the two additional auxiliary phases can be linearly interpolated.

For a given value of $\Delta\varphi$, $\Delta\vartheta$ is determined by the value of $\Delta\chi$, which needs to be chosen accordingly. Alternatively, for a fixed (suitable) value of $\Delta\vartheta$, the chosen value of $\Delta\chi$ determines $\Delta\varphi$ and therefore whether the second output ψ_2 can be generated by linear interpolation. Of course, $\Delta\vartheta = 0°$ is a valid possibility, which implies that $\lambda_1^+ = \lambda_1^-$ are identical.

With these additional phases, the phase differences of the interpolated phases (φ_1, $\overline{\varphi}_0$ and λ_1^-, λ_1^+) can be made arbitrarily small simultaneously by choosing

appropriate values of the phase shifts $\Delta\varphi$ and $\Delta\chi$ (or alternatively $\Delta\chi$ and $\Delta\vartheta$).

The second output phase ψ_2 is generated by interpolation of φ_1 and $\overline{\varphi}_0$ as before, while the first output phase ψ_1 is obtained by interpolating the additional phases λ_1^+ and λ_1^-

$$\psi_1 = \frac{1}{2}\left(\lambda_1^- + \lambda_1^+\right) = \varphi_0 + \Delta\chi + \frac{1}{2}\Delta\vartheta \tag{5.5}$$

Writing also ψ_2 in terms of $\Delta\chi$ and $\Delta\vartheta$

$$\psi_2 = \frac{1}{2}(\varphi_1 + \overline{\varphi}_0) = \varphi_0 + \Delta\chi + \frac{1}{2}\Delta\vartheta + 90^\circ \tag{5.6}$$

shows that the phase difference again is $\psi_2 - \psi_1 = 90^\circ$ independently of the absolute values of $\Delta\chi$ and $\Delta\vartheta$.

Differential outputs of the presented principle can easily be generated by interchanging the two input phases φ_0 and $\overline{\varphi}_0$. When using the same phase shifts, $\Delta\chi$ and $\Delta\vartheta$, the 180° shifted outputs $\overline{\psi}_1$ and $\overline{\psi}_2$ are obtained.

The block diagram of the differential quadrature phase generator in the phase space is shown in Figure 5.5. Obviously, the differential paths need to be matched as well.

The presented architecture relies on linear phase interpolation and matched phase shifts. Contrary to conventional solutions, no accurately tuned phase shifts are required, which avoids complicated adjustment loops and circuitry. The circuit structure is very simple, comprising only few components, which is beneficial for low noise and low power operation. Additionally, both elements can be implemented digital friendly (see Section 5.1.3), so the architecture potentially benefits from technology scaling and is suitable for low supply voltages.

5.1.2 Non-50 % Duty Cycle of the Input Phases

Generally, the proposed principle can operate with any periodic signal waveform, on which phase shifts and phase interpolation can be performed. The

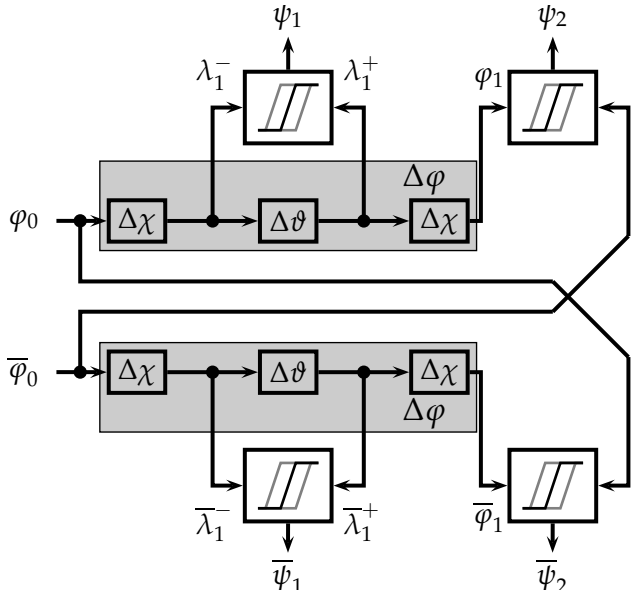
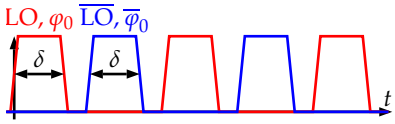


Figure 5.5: Block diagram of the differential I/Q generator in the phase space [151], [152].

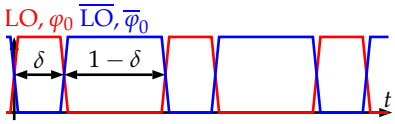
case of CMOS trapezoidal signals is of interest for practical implementations. As mentioned in Section 5.1, the required 180° phase shift of the input phases φ_0 and $\overline{\varphi}_0$ is ensured by the 50 % duty cycle of the corresponding LO and $\overline{\text{LO}}$ signals. Therefore, the sensitivity of the proposed architecture to duty cycle variations is of interest.

Two scenarios can be considered:

- Both input signals have a non-50 % duty cycle δ and the 180° phase shift is still valid for both rising and falling transitions as sketched in Figure 5.6a.
- The LO input signal has a non-50 % duty cycle δ, $\overline{\text{LO}}$ signal is the inverted version of LO, having a duty cycle of $1 - \delta$. The rising and falling edges of the input signals do not exhibit a 180° phase shift, as sketched in Figure 5.6b.



(a) Equal duty cycle on both input signal exhibiting a 180° phase shift.



(b) $\overline{\text{LO}}$ being the inverted version of LO not exhibiting a 180° phase shift.

Figure 5.6: LO and $\overline{\text{LO}}$ input signals for non-50 % duty cycles [152].

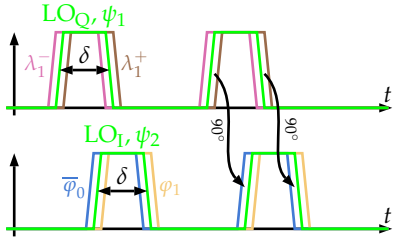


Figure 5.7: Output signals LO_Q (ψ_1) and LO_I (ψ_2) when both input signal exhibit the same duty cycle and a 180° phase shift [152].

5.1.2.1 Non-50 % Duty Cycle δ on LO and $\overline{\text{LO}}$

For the first case, where both input signals, LO and $\overline{\text{LO}}$, have a δ duty cycle, the proposed principle detailed in Section 5.1.1 applies unchanged. A time domain plot is sketched in Figure 5.7. Since no restrictions were posed on the input signals other than the 180° phase shift, which is fulfilled in this case, the output signals have the same shape as the inputs. Therefore, the duty cycle of the outputs follows the duty cycle of the input signals and is δ.

5.1.2.2 Non-50 % Duty Cycle δ on LO and $(1-\delta)$ on $\overline{\text{LO}}$

The second scenario is sketched in Figure 5.8, where the $\overline{\text{LO}}$ signal is the inverted version of the LO input. This case probably is more relevant for

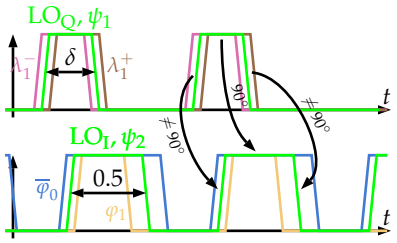


Figure 5.8: Output signals LO_Q (ψ_1) and LO_I (ψ_2) when $\overline{LO}$ being the inverted version of LO not exhibiting a 180° phase shift [152].

implementations, since slight deviations in duty cycles are unavoidable due to device mismatch etc.

The rising and falling transitions are considered individually, rising transitions are indicated with a $^{\lceil}$ superscript while falling edges are denoted with a $^{\rfloor}$ superscript. The input transitions referred to the rising edge of the LO input $\varphi_0^{\lceil}$ are $\varphi_0^{\rfloor} = \overline{\varphi}_0^{\lceil} = \varphi_0^{\lceil} + 360° \cdot \delta$ and $\overline{\varphi}_0^{\rfloor} = \varphi_0^{\lceil} + 360°$.

For simplicity, the outputs are calculated only with one auxiliary phase φ_1 as described in the beginning of Section 5.1.1. The transitions of this phase are $\varphi_1^{\lceil} = \varphi_0^{\lceil} + \Delta\varphi$ and $\varphi_1^{\rfloor} = \varphi_0^{\rfloor} + \Delta\varphi = \varphi_0^{\lceil} + \Delta\varphi + 360° \cdot \delta$. The output phases' transitions are

$$\psi_1^{\lceil} = \frac{1}{2}\left(\varphi_0^{\lceil} + \varphi_1^{\lceil}\right) = \varphi_0^{\lceil} + \frac{1}{2}\Delta\varphi \tag{5.7}$$

$$\psi_1^{\rfloor} = \frac{1}{2}\left(\varphi_0^{\rfloor} + \varphi_1^{\rfloor}\right) = \varphi_0^{\lceil} + \frac{1}{2}\Delta\varphi + 360° \cdot \delta \tag{5.8}$$

$$\psi_2^{\lceil} = \frac{1}{2}\left(\varphi_1^{\lceil} + \overline{\varphi}_0^{\lceil}\right) = \varphi_0^{\lceil} + \frac{1}{2}\Delta\varphi + 180° \cdot \delta \tag{5.9}$$

$$\psi_2^{\rfloor} = \frac{1}{2}\left(\varphi_1^{\rfloor} + \overline{\varphi}_0^{\rfloor}\right) = \varphi_0^{\lceil} + \frac{1}{2}\Delta\varphi + 180° \cdot (1 + \delta) \tag{5.10}$$

Although the transitions themselves do not exhibit the desired 90° phase shift if $\delta \neq 0.5$, the centers of the pulses $\hat{\psi}_i = \frac{1}{2}(\psi_i^{\lceil} + \psi_i^{\rfloor})$ ($i \in \{1, 2\}$) and therefore the first harmonics of the outputs (which are usually of interest in wireless TRX applications) exhibit a 90° phase shift, since

$$\hat{\psi}_1 = \frac{1}{2}\left(\psi_1^{\lceil} + \psi_1^{\rfloor}\right) = \varphi_0^{\lceil} + \frac{1}{2}\Delta\varphi + 180° \cdot \delta \tag{5.11}$$

$$\hat{\psi}_2 = \frac{1}{2}\left(\psi_2^{\lceil} + \psi_2^{\lfloor}\right) = \varphi_0^{\lceil} + \frac{1}{2}\Delta\varphi + 180^\circ \cdot \delta + 90^\circ \tag{5.12}$$

and the phase shift of the centers is $\hat{\psi}_2 - \hat{\psi}_1 = 90^\circ$, which implies that also the first harmonics of the outputs exhibit a perfect 90° phase shift under input duty cycle deviations.

But the non-50 % input duty cycle introduces a mismatch in the outputs duty cycles

$$\delta_1 = \left| \frac{\psi_1^{\lceil} - \psi_1^{\lfloor}}{360^\circ} \right| = \delta \tag{5.13}$$

$$\delta_2 = \left| \frac{\psi_2^{\lceil} - \psi_2^{\lfloor}}{360^\circ} \right| = 0.5 \tag{5.14}$$

which translates to an amplitude imbalance of the first harmonics. Interestingly, the in-phase output ψ_2 exhibits a perfect 50 % duty cycle while the quadrature output follows the input duty cycle.

The afore mentioned relations are also true for the differential architecture introduced in Section 5.1.1, shown in Figure 5.5, where the outputs are again related by inversion.

5.1.3 Circuit Implementation

The block diagram of the implemented circuit is shown in Figure 5.9. The main building blocks are the phase shifters (denoted ΔT and ΔT_f), the phase interpolators and an additional digital control circuitry.

The targeted operating frequency region spans from 1.5 GHz to 2.6 GHz. The targeted quadrature phase imbalance is less than $\pm 5^\circ$, values below this target can be corrected digitally in this system. A phase noise performance better than -155 dBc/Hz (at 100 MHz offset) for generic wireless TRX applications should be achieved, covering the entire operating frequency region and also process, supply voltage, and temperature (PVT) variations. This specification determines the transistor sizing. The circuit is designed in a 28 nm bulk-CMOS technology with a 1.1 V supply voltage.

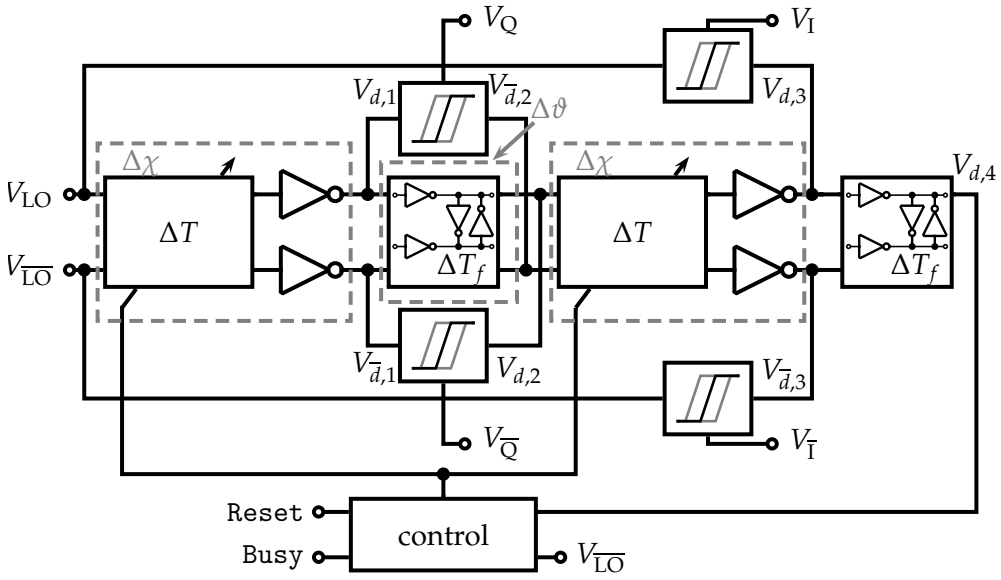


Figure 5.9: Block diagram of the implemented quadrature generation circuit, the phase shifts are annotated in gray [151], [152].

5.1.3.1 Phase Shifters

The phase shifters are implemented as time delays exploiting the inherent CMOS gate delay. The corresponding phase shift is $\Delta\varphi = \Delta T \cdot f_{\mathrm{LO}} \cdot 360°$ (for any delay value ΔT), which is related to the operating frequency f_{LO}.

The small phase shift $\Delta\vartheta$ introduced in Section 5.1.1 is implemented as a non-tunable pseudo differential inverter indicated as ΔT_f in Figure 5.9. The delay provided by this block must be sufficiently small to guarantee overlapping transitions of its input and output signals ($V_{d,1}$, $V_{\overline{d,1}}$ and $V_{d,2}$, $V_{\overline{d,2}}$). This is required to enable the linear phase interpolation to generate the V_{Q} and $V_{\overline{\mathrm{Q}}}$ outputs. Additionally, this block is used to realign the differential paths with the cross-coupled structure.

The second and larger phase shift $\Delta\chi$, implemented as the time delay ΔT, comprises three tunable delay stages shown in Figure 5.10a exploiting the RC-delay. The load capacitance can be varied by digitally setting the NMOS

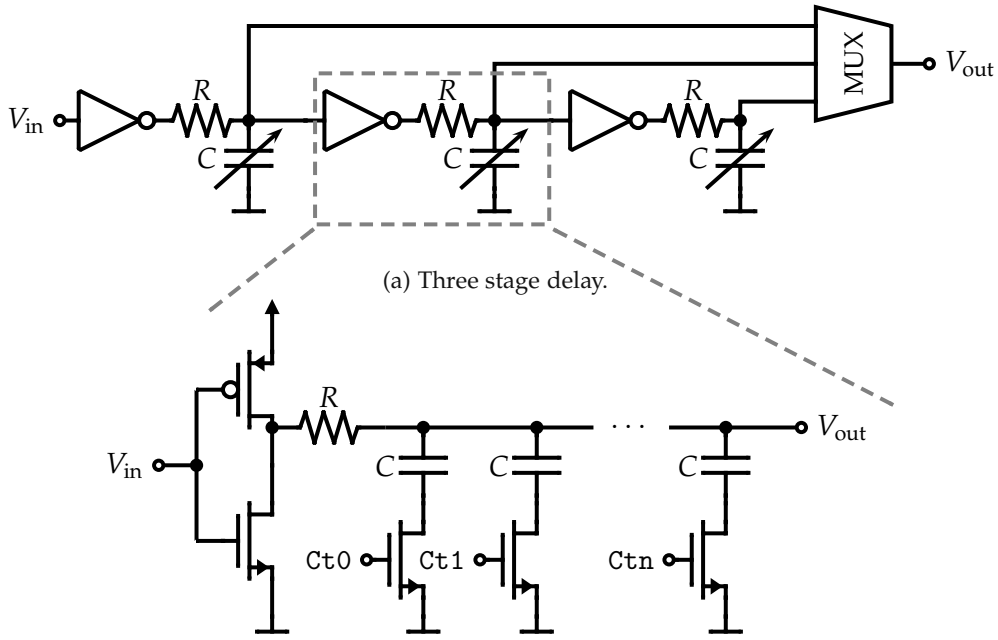


Figure 5.10: Phase shifter exploiting the CMOS gate delay, sketched in single-ended fashion [151], [152].

switches. A single stage is shown in Figure 5.10b. Note that this entire delay element has redundant settings due to the multistage implementation, which result in similar delays and a non-monotonic delay behavior at when switching on and off stages.

The two delay elements ΔT need to match as explained in Section 5.1.1 above. Therefore, also an additional delay ΔT_f is added at the end of the second tunable delay ΔT to ensure equal loading.

Overlapping the transitions of the input signals of the phase interpolators (Section 5.1.3.2), V_{LO} and $V_{d,3}$ for the I as well as $V_{\overline{\mathrm{LO}}}$ and $V_{\overline{d,3}}$ for the $\overline{\mathrm{I}}$ phase interpolators, need to be ensured by correctly adjusting the delays ΔT, providing a suitable phase shift for the input frequency. The input signals to the Q and $\overline{\mathrm{Q}}$ phase interpolators have overlapping transitions if the delay ΔT_f is designed properly.

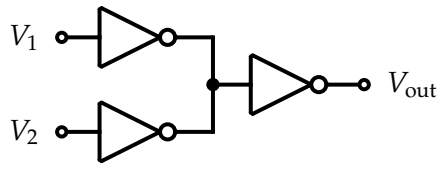


Figure 5.11: Single-ended voltage mode phase interpolator [151]–[153].

The range of one delay element ΔT needs to cover approximately 90° over the desired operating frequency region. Then both delays ΔT provide roughly 180° which guarantees overlapping transitions of V_{LO} and $V_{d,3}$ as well as $V_{\overline{\text{LO}}}$ and $V_{\overline{d,3}}$.

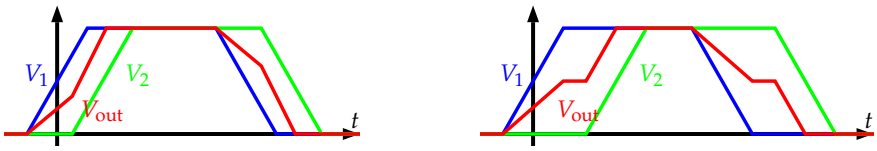
The sizing of the circuit elements was determined, apart from enabling the required achievable delays for the operating frequency range of 1.5 GHz to 2.6 GHz, by the targeted phase noise requirements of -155 dBc/Hz at 100 MHz offset to the carrier over PVT variations.

5.1.3.2 Phase Interpolators

A voltage mode phase interpolator [157] was chosen over current mode implementations [158], shown in Figure 5.11. This phase interpolator comprises two inverters that drive the interpolation node, and an output inverter, that loads this node with its gate capacitance and restores the output signal's rise and fall times.

As already mentioned, for linear operation in terms of phase, the interpolator requires overlapping transitions of the input signals. A simplified sketch is shown in Figure 5.12a.

In the case of non-overlapping transitions, sketched in Figure 5.12b, the two input inverters will just work against each other and the phase information is lost [156]. In this case, the signal at the output will be determined only by the actual transistors' driving strengths and threshold voltages, which is undefined and thus undesired behavior.



(a) Overlapping input transitions. (b) Non-overlapping input transitions.

Figure 5.12: Simplified input and output signals of the phase interpolator. The gate delay is not shown for simplicity [152].

5.1.3.3 Auxiliary Digital Control

Programming the delay elements ΔT introduced in Section 5.1.3.1 to match the input frequency can be performed manually. In this work, a simple auxiliary digital control block is added to perform this task automatically.

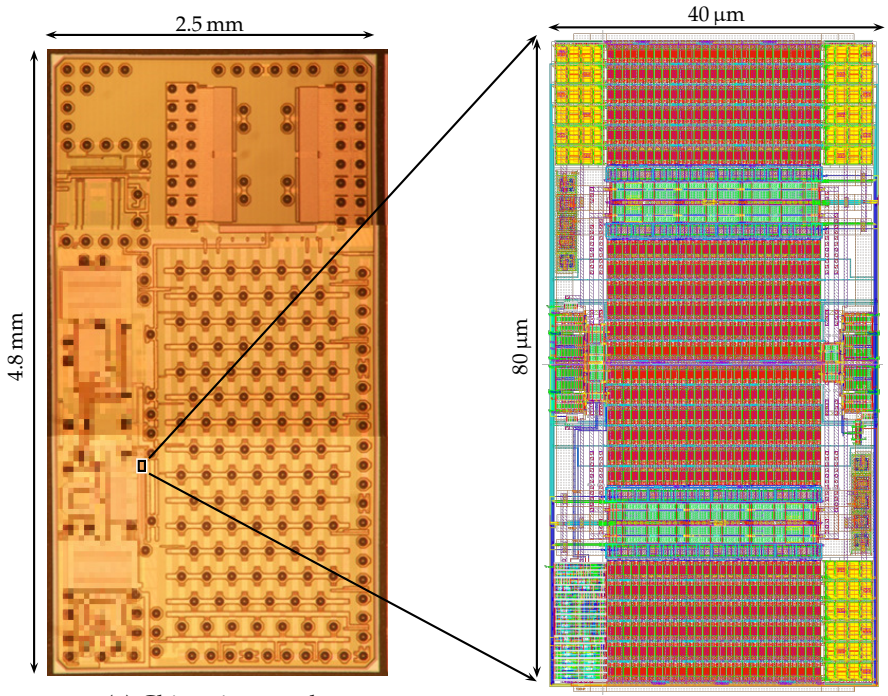
This block is activated upon reset, e.g. triggered on start-up or LO frequency change. It finds suitable values for the delays ΔT which takes several LO cycles and then is switched off.

The control block is composed of a phase detector, that compares the output of the delay line with the (inverted) LO input, several registers and some logic gates to perform the search algorithm. It varies the number of active stages and load capacitance to match the delays to the input frequency.

This closely resembles a digital delay-locked loop: the control loop adjusts the transitions of the delay line output to match the ones of the (inverted) LO input, which eventually is approximately a 180° shift.

As previously noted, this is only done to guarantee linear interpolation for every operating frequency and to counter PVT variations. When the search algorithm finds the optimal settings, the control loop is switched off and the circuit operates in its open-loop configuration.

Due to simplicity, all components of this additional block exclusively comprise standard digital cells. This also holds true for the phase detector, which is composed from registers, trading accuracy for implementation effort.



(a) Chip micrograph.

(b) Physical drawing of the circuit.

Figure 5.13: Micrograph of the entire fabricated test chip and physical drawing of the quadrature generator [151], [152].

5.1.4 Measurement Results

The presented circuit was manufactured in a 28 nm bulk-CMOS technology with 1.1 V supply voltage as part of a wireless TRX system. A chip micrograph of the fabricated prototype and the physical drawing of the presented block are shown in Figure 5.13.

The implemented component occupies an area of 40 µm × 80 µm. The switchable load capacitors occupy roughly 1600 μm^2, i.e. 50 %, of the area, as clearly visible in the physical drawing. The digital control algorithm makes up for less than 3 % of the total area.

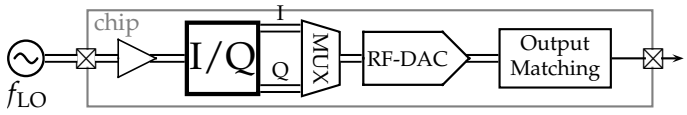


Figure 5.14: Measurement setup of the quadrature phase generator [151], [152].

5.1.4.1 Measurement Setup

The measurement setup is sketched in Figure 5.14. The outputs of the block feed the clock input of an RF-DAC, set to a constant code, acting as an RF output buffer, driving the chip output [100].

Both, the I and Q signals, can be multiplexed to the same clock input of the RF-DAC in order to precisely measure the phase accuracy of the block without suffering from any of the imbalances of the following output chain. The NOR-based multiplexer is a capacitive load of approximately 40 fF per signal for the I/Q generator.

The subsequent stages were designed with approximately 10 dB better phase noise performance than the quadrature generator, thus the noise is dominated by the presented circuit. The quadrature generator consumes 4.4 mW from a 1.1 V supply at 2 GHz operating frequency.

5.1.4.2 I/Q Phase Shift

The I/Q phase shift was measured for ten different samples. The results are shown in Figure 5.15, where the delay was set by the digital control algorithm for each operating frequency, as detailed in Section 5.1.3.3.

The specifications of less than $\pm 5^\circ$ I/Q phase error are met for the entire measured frequency range of 1 GHz up to 3 GHz for all ten samples when automatically setting the delays.

As can be seen in Figure 5.15, there is a systematic phase error visible around 1.6 GHz and 2.2 GHz when having the digital control algorithm adjust the delays. It obviously does not handle the different number of stages optimally, which is indicated by the kinks visible in the I/Q phase shift curves, although the target specification is still met.

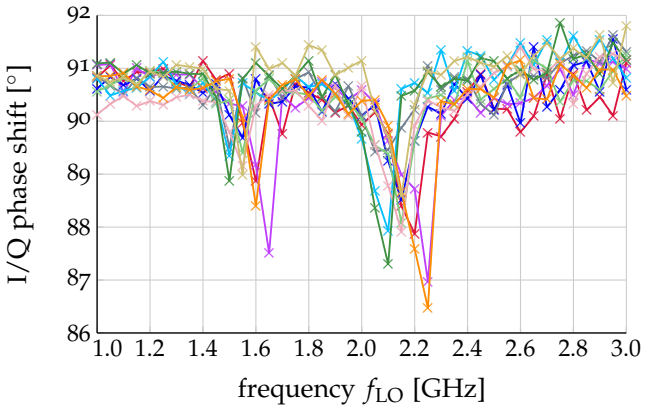


Figure 5.15: I/Q phase shift measured for ten different samples with the delays set by the digital control algorithm [152].

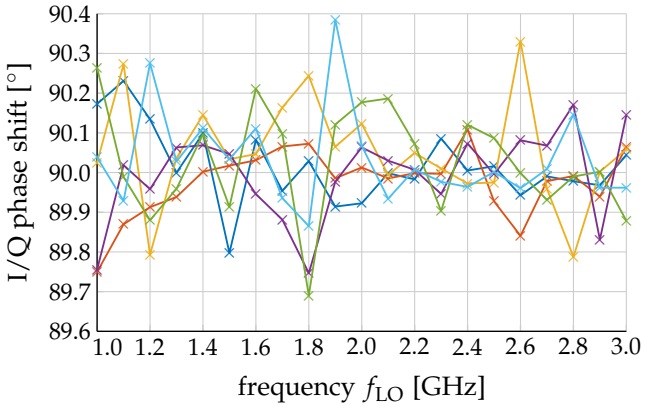


Figure 5.16: I/Q phase shift measured for different samples with optimum delay settings, note the different scale on the y-axis [152].

This is not a drawback of the circuit architecture itself. Several samples were tested for their optimum I/Q phase shift by testing all possible delay settings versus frequency. The optimum achievable I/Q phase shift versus operating frequency is shown in Figure 5.16. Upon setting the optimum delays, the I/Q phase accuracy is better than $\pm 0.4^\circ$ for the entire measured frequency range of 1 GHz up to 3 GHz for all tested samples.

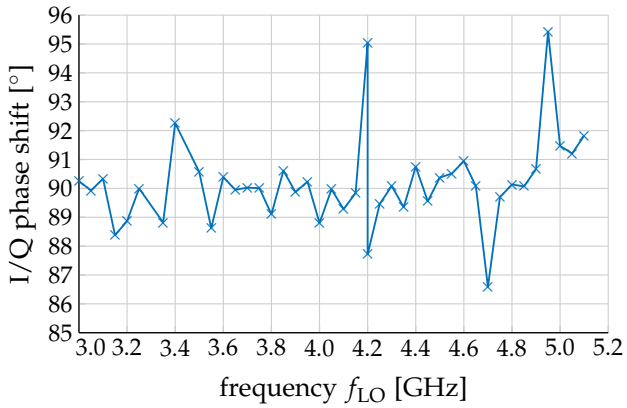


Figure 5.17: I/Q phase shift measured for one sample at operating frequencies higher than 3 GHz [152].

Furthermore, one sample was characterized at higher input frequencies. In particular, the circuit was measured up to 5.1 GHz, i.e., the highest LO frequency the prototype's test platform can support. The resulting I/Q phase shift is shown in Figure 5.17.

Interestingly, the circuit still produces viable I/Q LO signals at frequencies above 3 GHz. At such high operating frequencies, there is no setting of the delay elements to match the delay line to 180°.

In the circuit principle presented in Section 5.1.1 the only restriction posed on the delays is that they are chosen suitably to enable linear interpolation. As explained in Section 5.1.3.1 before, this means that the delay is matched roughly to 180° according to the operating frequency $\Delta\varphi = \Delta T \cdot f_{LO} \cdot 360°$.

For operating frequencies higher than 3 GHz, the delay line does not match 180° but approximately $(2n+1) \cdot 180°$ ($n \in \{0, 1, ...\}$), e.g. $3 \cdot 180° = 540°$. When choosing such a setting, again the transitions of the input signals of the phase interpolators are overlapping and they are working in their linear interpolation region. In other words, the phase wraps around n times.

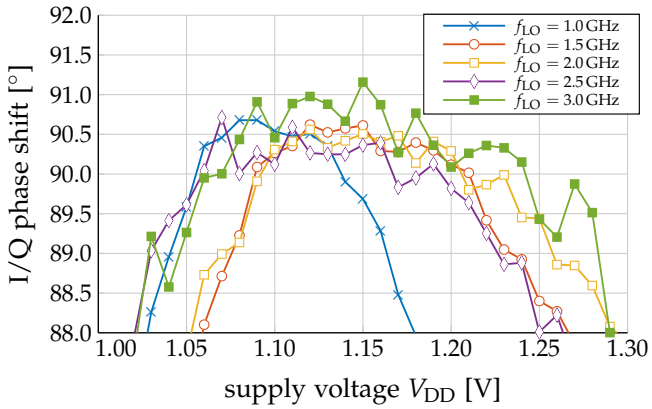


Figure 5.18: I/Q phase shift measured for different supply voltages. The delay was adjusted at the nominal supply voltage of 1.1 V [152].

5.1.4.3 Sensitivity to Supply Voltage

The sensitivity to supply voltage is of special interest, since digital circuit blocks offer little power supply rejection. Figure 5.18 shows the sensitivity of the I/Q phase shift to supply voltage changes. The delays were set with the digital control algorithm at the nominal supply voltage of 1.1 V.

For a maximum deviation $< \pm 1°$, there is always more than 50 mV of tolerable voltage range available. Such a requirement can easily be fulfilled by a very reasonably specified low-dropout regulator or a similar supply voltage regulator.

5.1.4.4 Phase Noise Performance

The phase noise performance at the 2 GHz carrier frequency is shown in Figure 5.19. The phase noise performance at 100 MHz offset is better than -155 dBc/Hz over the entire measured frequency range from 1 GHz to 3 GHz.

The phase noise performance is slightly different on the I and Q outputs, with the in-phase output outperforming the quadrature one. This is explained by the different signals used to create the outputs by interpolation: as shown in the circuit's block diagram in Figure 5.9, for the I output the input LO and a

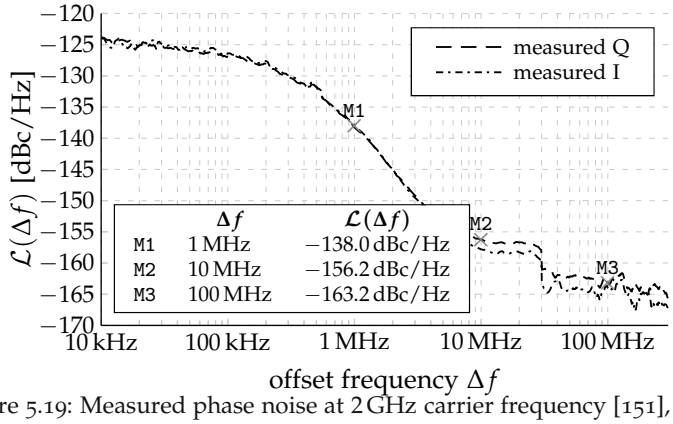


Figure 5.19: Measured phase noise at 2 GHz carrier frequency [151], [152].

delayed signal are interpolated, while for the Q output two delayed signals are combined. The usage of the clean input signal on the in-phase output explains the slightly better noise performance.

5.1.5 Comparison to the State-of-the-Art

Table 5.1 compares the proposed prototype with similar circuits found in literature. The manufactured circuit exhibits superior performance compared to alternate solutions, providing improved tuning range, small area, and very low phase noise at low power consumption. This proves the feasibility of the proposed circuit concept.

Table 5.1: Comparison to State-of-the-Art Solutions

	this work			Elshazly et al. [147]	Yousef et al. [148][a]	Valero et at. [149]	Bhardwaj et al. [150]
operating principle	phase interpolation			delay locked loop	injection-locked ring oscillator	polyphase filter	pumped capacitor & LC tank
frequency range (GHz)	$1.0 \sim 3.0$			$2.0 \sim 7.5$	$4.23 \sim 4.77$	$2.4 \sim 2.5$	$9.9 \sim 14.6$
technology	28 nm			14 nm FinFET	180 nm	250 nm BiCMOS	28 nm
supply voltage (V)	1.1			1.35	n/a	2.5	n/a
area (mm^2)	0.003			0.002	n/a	2	0.04
tuning range (%)	100			116	12[a]	4	38
frequency (GHz)	2			7.0	4.5	2.45	11.75
phase noise (dBc/Hz)	−138.0	−156.2	−163.2	−126.0	−130.9[a]	−128.0	−118.0
at (MHz)	1	10	100	1	1	1	10
power (mW)	4.4			4.4	4.25[a]	12.5	3.1[a]
FoM (dBF)	197.6	195.8	182.8	196.5	197.7[a]	184.8	166.5[a]
FoM_T (dBF)	201.1	199.3	186.3	200.5	198.2[a]	185.0	168.0[a]

[a] simulation results only

In order to enable a rather fair comparison between the different circuits, two figures of merits (FoM) [159] are used incorporating operating frequency f_0, phase noise $\mathcal{L}(\Delta f)$ at the offset frequency Δf, power consumption P as well as the tuning range $f_{\max} - f_{\min}$. The higher the FoM, the better the circuit performance

$$\mathrm{FoM} = 20\ \log_{10}\left(\frac{f_0}{\Delta f}\right) - \mathcal{L}(\Delta f) - 10\ \log_{10}\left(\frac{P}{1\,\mathrm{mW}}\right) \tag{5.15}$$

$$\mathrm{FoM}_T = \mathrm{FoM} + 20\ \log_{10}\left(1 + \frac{f_{\max} - f_{\min}}{f_{\max} + f_{\min}}\right) \tag{5.16}$$

Table 5.1 shows that the manufactured prototype provides state-of-the-art performance. In particular, the proposed circuit achieves the best figures of merit, while featuring an extremely small footprint.

5.2 Generalization and Multiphase Generation

Multiple phase LOs and clocks have manifold applications: In digital circuits ranging from high speed serial link applications, where data streams are processed at a bit rate higher than the clock frequency [160]–[162], in clock multiplication where the individual phases are combined into a high frequency clock [163]–[166], and in microprocessors, where timing constraints can be eased with multiphase clocks [167], [168]. In analog and mixed-signal circuits, multiphase clocks and LOs are used for time interleaved data converters [169], [170], N-path filters [60]–[62], and multiphase mixers [171], [172] and PAs [173].

The novel quadrature generation architecture introduced in Section 5.1 can indeed be generalized. First, the need of 180° spaced input LO phases can be eliminated. Second, the quadrature generation can be extended to support arbitrary n multiphase outputs with phase differences of $\frac{360^\circ}{n}$ ($n \in \mathbb{N}^*$). The implementation benefits of the previously introduced circuit architecture are maintained, as is explained in this section.

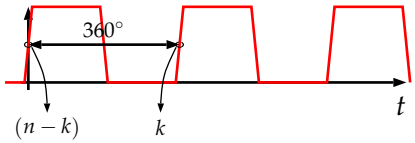


Figure 5.20: Usage of a single input phase with weighted linear phase interpolation for multiphase generation [155].

5.2.1 Operating Principle

Similarly to the quadrature generation principle, the main idea of this new multiphase generator is linear phase interpolation of inputs with precisely known phase differences. In the general case, a single input signal (φ_0 in the phase space) is sufficient, and the precise phase difference is obtained by a full period of this very input phase, i.e. 360° as will be explained below.

Contrary to the quadrature generator, weighted linear phase interpolation is used. The output ψ of such a weighted phase interpolator is

$$\psi = \frac{1}{w_1 + w_2}(w_1 \cdot \varphi_1 + w_2 \cdot \varphi_2) \tag{5.17}$$

for the input phases φ_1 and φ_2 with respective interpolation weights w_1 and w_2. The circuit implementation of such a weighted phase interpolator is discussed in Section 5.2.4.2.

Again, the main idea is to use weighted linear phase interpolation on the input signal and the respective next period of the very same input signal, effectively interpolating between two phases with a perfect 360° phase shift, as sketched in Figure 5.20. With weights $n - k$ and k ($0 \leq k < n$), the k-th output phase is

$$\psi_k = \frac{1}{n}((n-k) \cdot \varphi_0 + k \cdot (\varphi_0 + 360°)) = \varphi_0 + \frac{k}{n} \cdot 360° \tag{5.18}$$

where $\varphi_0 + 360°$ indicates the next period as sketched in Figure 5.20.

Even if this results in the desired outputs already mathematically, a practical phase interpolator, cannot distinguish between periods. For CMOS trapezoidal signals, always the closest signal transitions will be interpolated.

Similarly to the quadrature generation presented in Section 5.1, several requirements are posed on the interpolated signals in order to enable implementable linear phase interpolation.

First, the interpolated phases must be arbitrarily close to the respective desired output phase, i.e. their phase difference must be sufficiently small. For n output phases, a 360° phase shift needs to be tapped at e.g. $\frac{360^\circ}{n}$ intervals as explained below.

Second, absolute values of phase shifts are not available. This is especially true when employing time delays as phase shifts, which is suitable for CMOS implementation. The respective phase shift then varies with the operating frequency as $\Delta\varphi = \Delta T \cdot f_{\mathrm{LO}} \cdot 360^\circ$. As previously shown in Section 5.1.3, the phase shifts can be made programmable, to compensate the operating frequency and PVT variations, but with limited granularity. But still, one can rely on relatively matched time delays and therefore matched phase shifts.

With these limitations in mind, the operating principle is illustrated step-by-step to obtain the general multiphase generation architecture.

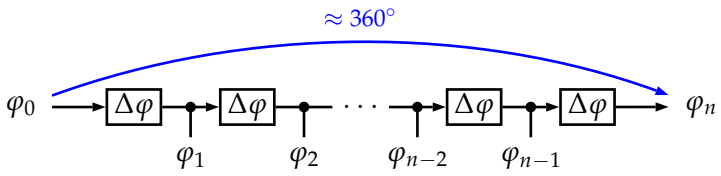
Through a chain of n phase shifters, sketched in Figure 5.21a, with each phase shifter providing $\Delta\varphi \approx \frac{360^\circ}{n}$, a total phase shift of $n \cdot \Delta\varphi \approx 360^\circ$ is obtained. Note that this is not a precise phase shift, but limited by programming granularity and such, as previously explained. In addition to the input phase φ_0, n further auxiliary phases $\varphi_1, ..., \varphi_n$ become available, where the k-th phase is

$$\varphi_k = \varphi_0 + k \cdot \Delta\varphi \tag{5.19}$$

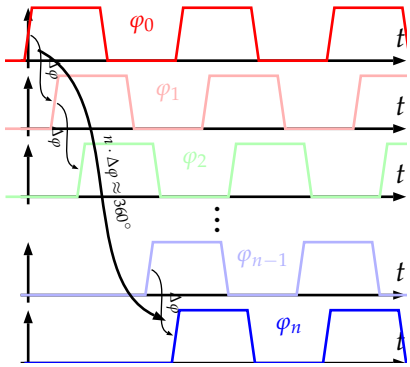
For CMOS trapezoidal signals, respective time domain sketches are shown in Figure 5.21b.

As indicated in Figure 5.21b, φ_0 and φ_n can be made arbitrarily close by choosing $\Delta\varphi$ sufficiently close to $\frac{360^\circ}{n}$. When feeding these two phases to a phase interpolator, it will interpolate φ_n and already the next period of φ_0, since these are the closest transitions, as sketched in Figure 5.21b. This is already close to the initially introduced idea of interpolating φ_0 and $\varphi_0 + 360^\circ$. Weighted linear phase interpolation of these two phases, with arbitrary k, yields

$$\psi = \frac{1}{n}\left((n-k)\,\varphi_n + k\,(\varphi_0 + 360^\circ)\right) = \varphi_0 + \frac{k}{n} \cdot 360^\circ + (n-k) \cdot \Delta\varphi \tag{5.20}$$



(a) Block diagram.



(b) Time domain sketch for CMOS trapezoidals.

Figure 5.21: Chain of phase shifters to provide a phase shift of approximately 360° and n additional auxiliary phases $\varphi_1, ..., \varphi_n$ [155].

Contrary to the ideal case where φ_0 and $\varphi_0 + 360°$ are interpolated, an offset term, that depends on k, is introduced.

Further phase shifters $\Delta\varphi$ can be appended to the existing chain of n phase shifters, sketched in Figure 5.22. Doing so makes further pairs of phases $(\varphi_l, \varphi_{n+l})$ available, that exhibit a $n \cdot \Delta\varphi$ phase difference, similar to the previously discussed pair (φ_0, φ_n) (essentially having $l = 0$).

Linear phase interpolation of the l-th pair, where similarly to the case with $l = 0$ the next period is used for φ_l, with arbitrary $0 \leq k < n$, yields

$$\begin{aligned} \psi_l &= \frac{1}{n}\left((n-k)\,\varphi_{l+n} + k\,(\varphi_l + 360°)\right) \\ &= \frac{1}{n}\left((n-k)(\varphi_0 + (n+l)\,\Delta\varphi) + k\,(\varphi_0 + l\cdot\Delta\varphi + 360°)\right) \end{aligned} \tag{5.21}$$

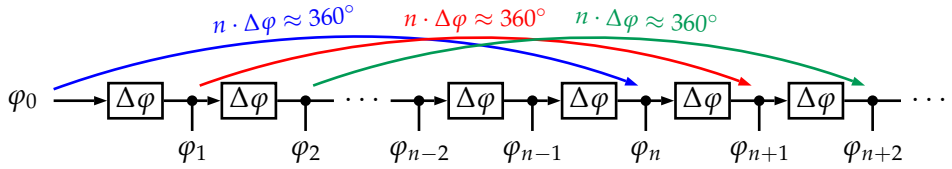


Figure 5.22: Extension of the chain of phase shifters, obtaining more pairs of phases $(\varphi_l, \varphi_{n+l})$ with $n \cdot \Delta\varphi$ phase difference [155].

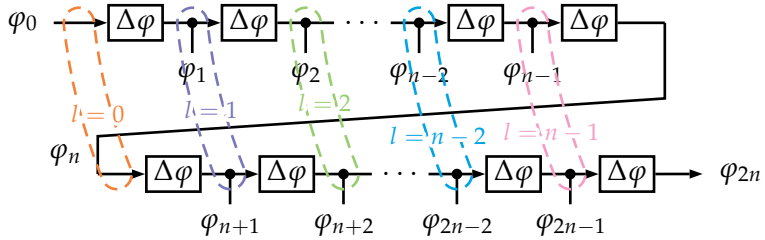


Figure 5.23: Full chain of phase shifters (for $c = 1$), highlighting the interpolated phase pairs [155].

$$= \varphi_0 + \frac{k}{n} \cdot 360° + (n - k + l)\,\Delta\varphi$$

The previously introduced offset term now not only depends on the interpolation weight k, but also on the pair index l. Since k and l exhibit opposite signs, proper choice thereof can cancel any dependency of this offset term on both k and l making it constant for all ψ_l.

This condition is achieved when $c := k - l = \text{const}$, although both $k, l \geq 0$. Furthermore, the interpolation weight $n - k \geq 0$, as negative weights are not implementable. Therefore, the interpolation weights for the l-th phase pair are $k = l + c$ and $(n - k) = n - l - c$. When obtaining all n output phases, $0 \leq c \leq 1$ in order to avoid negative implementation weights. Obviously, for the least amount of circuit components, $c = 1$, sparing the last auxiliary phase φ_{2n}, generating the output phases $\psi_0, \ldots, \psi_{n-1}$ as sketched in Figure 5.23.

For $c = 1$, the l-th output phase then is

$$\psi_l = \frac{1}{n}\left((n - l - 1)\,\varphi_{l+n} + (l + 1)\,(\varphi_l + 360°)\right) \tag{5.22}$$

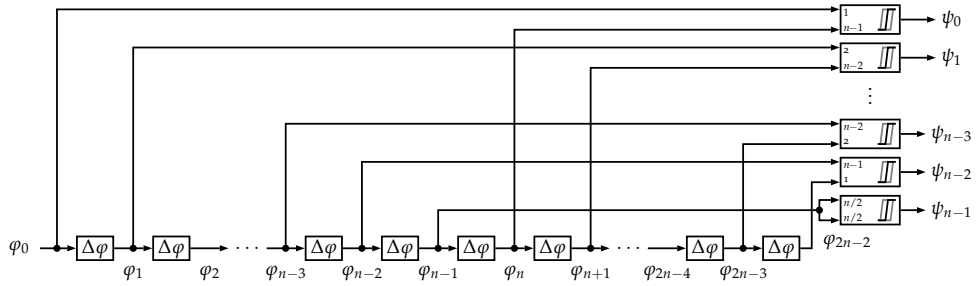


Figure 5.24: Phase space block diagram of the multiphase generator [155].

$$= \frac{1}{n}((n-l-1)\,(\varphi_0 + (n+l)\,\Delta\varphi) + (l+1)\,(\varphi_0 + l\cdot\Delta\varphi + 360^\circ))$$
$$= \varphi_0 + \frac{l+1}{n}\cdot 360^\circ + \Delta\varphi\cdot(n-1)$$

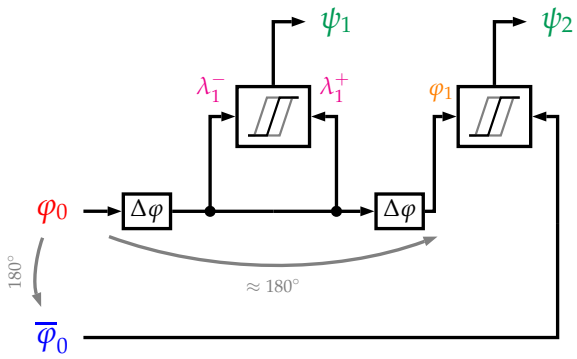
and consecutive output phases ψ_j and ψ_{j+1} exhibit a perfect $\frac{360^\circ}{n}$ phase shift as desired. Note that the last phase shifter generating φ_{2n} in Figure 5.23 is not required, although for implementations, proper loading of the previous phase shifter is essential. The full phase space block diagram of the multiphase generator is shown in Figure 5.24.

Obviously, when n is chosen appropriately, this circuit architecture can generate differential outputs from a single-ended input LO or clock phase, allowing for considerable savings in power spent on LO or clock distribution.

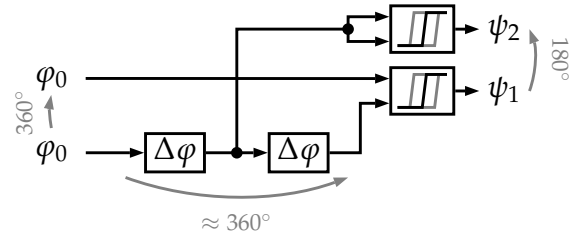
Similarly to the previously presented quadrature generator discussed in Section 5.1, this architecture relies on weighted linear phase interpolation and matched phase shifts. Again, no precise phase shifts are required which avoids complicated adjustment loops and circuitry. Further, all elements can be implemented digital friendly (see Section 5.2.4), benefiting from technology scaling and being suitable for low supply voltages.

5.2.2 Comparison to the Quadrature Phase Generator

This multiphase generation principle is a generalization of the quadrature generator discussed in Section 5.1.1. In order to highlight this fact, phase



(a) Single-ended quadrature generator with $\Delta\vartheta = 0$.



(b) Multiphase generator for $n = 2$.

Figure 5.25: Phase space block diagrams to highlight the relation of the two discussed circuit principles.

space block diagrams of the single-ended quadrature phase generator (with $\Delta\vartheta = 0$) and the multiphase generator for $n = 2$ are sketched in Figure 5.25.

The input phase φ_0 in Figure 5.25b is drawn twice to better highlight the equivalence of the two discussed principles. In the case when a 360° phase difference is interpolated, a single input signal is sufficient. The 360° essentially signify the next period of the very same signal, as discussed in Section 5.2.1.

As can be gathered from the two block diagrams in Figure 5.25, any two phases can be implemented with this circuit principle. Therefore, the total phase shift provided by the two phase shifters $\Delta\varphi$ needs to approximately match the input phase difference. Thanks to the employed linear phase interpolation, exact phase differences in the output signals are achieved.

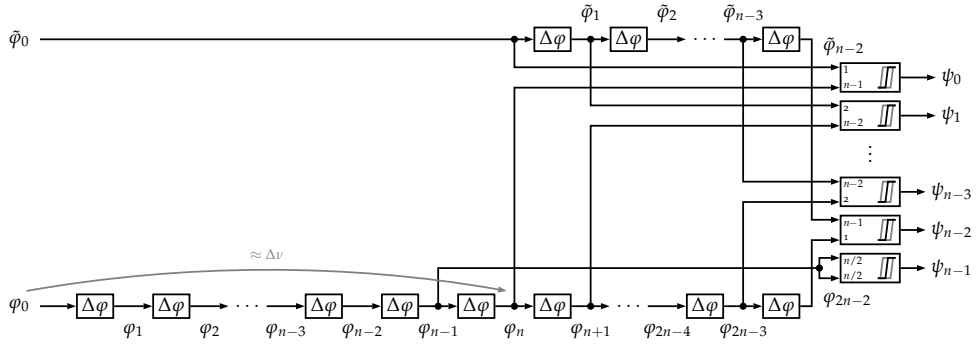


Figure 5.26: Phase space block diagram of the multiphase generator for arbitrary input phases φ_0 and $\tilde{\varphi}_0$ with phase shift $\Delta\nu$.

5.2.3 Arbitrary Multiphase Interpolation

As suspected within the previous section, the presented principle can also be used for multiphase interpolation of two arbitrary input phases φ_0 and $\tilde{\varphi}_0$. The phase difference between the two is not limited to any special case like 360° or 180° and denoted as $\Delta\nu$. Essentially, output phases with phase differences of $\frac{\Delta\nu}{n}$ can be generated by adapting the previously discussed multiphase generation principle. Without loss of generality, it is assumed that φ_0 is leading, i.e. $\tilde{\varphi}_0 - \varphi_0 = \Delta\nu \geq 0$.

The respective modified phase space block diagram is sketched in Figure 5.26. An additional chain of $n-2$ phase shifters, taking the second input $\tilde{\varphi}_0$ as its input, generates further auxiliary phases $\tilde{\varphi}_1, ..., \tilde{\varphi}_{n-2}$, where $\tilde{\varphi}_l = \tilde{\varphi}_0 + k \cdot \Delta\varphi = \varphi_0 + \Delta\nu + k \cdot \Delta\varphi$. Contrary to the previously discussed multiphase generation, the individual phase shifters provide $\Delta\varphi \approx \frac{\Delta\nu}{n}$, such that $n \cdot \Delta\varphi \approx \Delta\nu$, and therefore $\varphi_n \approx \tilde{\varphi}_0$.

The k-th ($0 \leq k < n-1$) output phase then is acquired by weighted linear phase interpolation of φ_{n+k} and $\tilde{\varphi}_k$. The interpolation weights are $(n-k-1)$ and $(k+1)$ respectively. Finally, the output phase $\psi_{n-1} = \varphi_{n-1}$, which needs to be matched to the other outputs with a dummy phase interpolator as sketched in Figure 5.26.

To show the validity of these observations, the k-th output is calculated as

$$\begin{aligned}\psi_k &= \frac{1}{n}((n-k-1)\cdot\varphi_{n+k} + (k+1)\cdot\tilde{\varphi}_k) \\ &= \frac{1}{n}((n-k-1)\cdot(\varphi_0 + (n+k)\cdot\Delta\varphi) + (k+1)\cdot(\varphi_0 + \Delta\nu + k\cdot\Delta\varphi)) \\ &= \frac{1}{n}\left(n\cdot\varphi_0 + \left(n^2-n\right)\cdot\Delta\varphi + (k+1)\cdot\Delta\nu\right) \\ &= \varphi_0 + \frac{k+1}{n}\cdot\Delta\nu + (n-1)\cdot\Delta\varphi\end{aligned} \tag{5.23}$$

given that $\Delta\varphi$ is suitably chosen to allow the linear phase interpolation. The last output ψ_{n-1} (but temporally leading signal) plainly calculates to

$$\psi_{n-1} = \varphi_0 + (n-1)\cdot\Delta\varphi \tag{5.24}$$

It is clearly visible that the phase differences between the individual output phases are

$$\psi_{k+1} - \psi_k = \frac{1}{n}\cdot\Delta\nu \tag{5.25}$$

as expected. Therefore, two individual input phases φ_0 and $\tilde{\varphi}_0$ with phase difference $\Delta\nu$ can be interpolated to generate n output phases. For implementations, cases with $n = 2$ or even $n = 4$ are probably of viable interest.

5.2.4 Circuit Implementation

A multiphase generator is designed implementing the presented novel circuit architecture. It generates three differential output phases spaced 120°, implying $n = 6$ individual single-ended outputs with phase differences of 60° each. Other than employing these six output phases directly in a time interleaved scheme, e.g. a frequency tripler can be realized.

Such a scheme is especially handy e.g. for frequency bands around 3.6 GHz. To reduce power spent on LO distribution, a clock multiplier can be employed. But doubling the frequency results in distributed LOs around 1.8 GHz and by quadrupling, it ends up close to 900 MHz, all of which are occupied by LTE and other sensitive bands. Using such a frequency for distribution

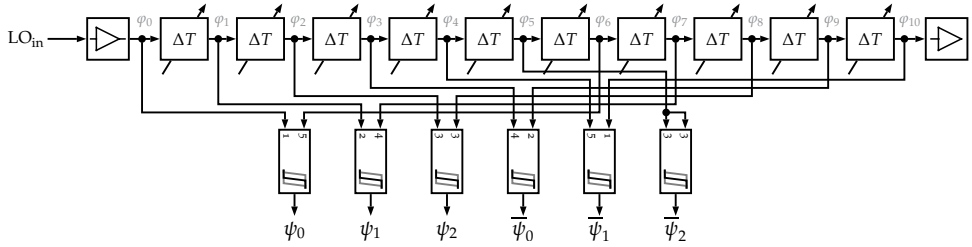


Figure 5.27: Block diagram of the implemented multiphase generator. [155]

will likely result in undesired spurious tones and other crosstalk effects. Using a frequency tripler instead, results in distributed LOs around 1.2 GHz, where no LTE bands are allocated, essentially reducing undesired crosstalk effects in sensitive frequency regions as well as power consumption.

The block diagram of the implemented circuit is shown in Figure 5.27. The main building blocks are the phase shifters and the weighted phase interpolators.

The targeted operating frequency region spans from 1.5 GHz to 2.6 GHz. A phase noise performance better than $-145\,\mathrm{dBc/Hz}$ (at 100 MHz offset) for wireless TRX applications should be achieved, covering the entire operating frequency region and also PVT variations. This specification determines the transistors' sizing. The circuit is designed in a 28 nm bulk-CMOS technology with a 0.95 V supply voltage.

5.2.4.1 Phase Shifters

The phase shifters are implemented as CMOS time delays denoted as ΔT in Figure 5.27, similarly to the quadrature generator discussed in Section 5.1.3.1. Ten phase shifters are employed to obtain the eleven auxiliary phases $\varphi_0, ..., \varphi_{10}$ required to generate six output phases $\psi_0, ..., \psi_2$ and $\overline{\psi}_0, ..., \overline{\psi}_2$ as explained in Section 5.2.1. Furthermore, a dummy load is added at the end of the chain of delays to match the load. Also, a dummy driver is introduced at the input to match rise and fall times.

The individual delay comprises two stages, each exploiting the RC delay. A single stage is sketched in Figure 5.28. A pair of tristate inverters, where only

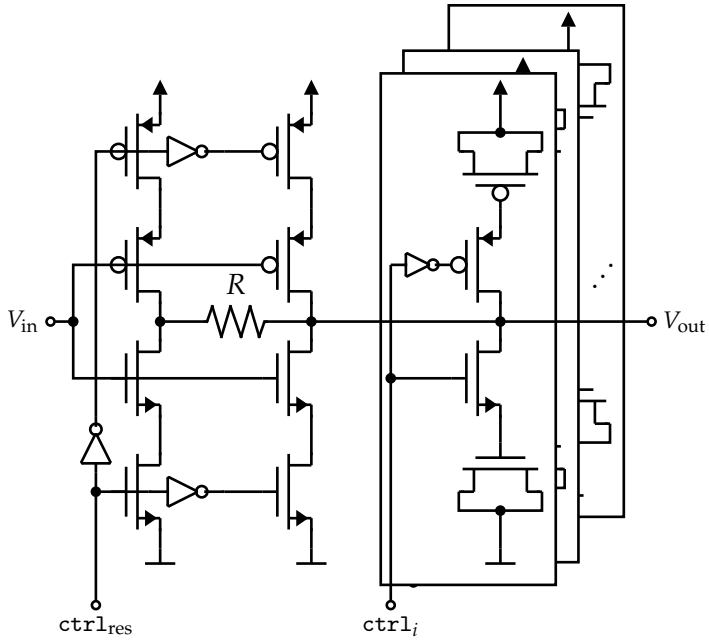
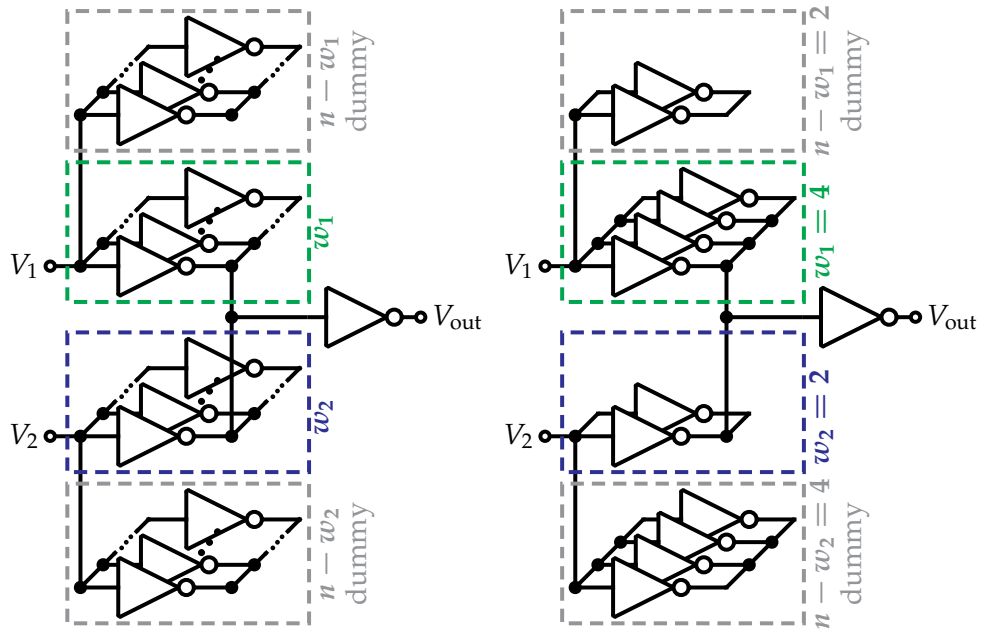


Figure 5.28: Circuit implementation of a delay element's single stage [155].

one is active at any time, drives a programmable set of PMOS and NMOS capacitors. The effective load capacitance is controlled by the capacitance control word $\texttt{ctrl}_{\text{c}}$, which comprises the individual digital signals $\texttt{ctrl}_i$. These control signals enable or disable the capacitors by means of the transistor switches shown in Figure 5.28.

By selecting one or the other driving inverter by means of the digital signal $\texttt{ctrl}_{\text{res}}$, an additional linear resistor R in series to the transistors' resistance can be enabled to further extend the possible delay and enhance the available range of delays.

This programmability is introduced to achieve the desired phase shift $\Delta\varphi \approx \frac{360^\circ}{n}$ or $\Delta T \approx \frac{T_{\text{LO}}}{n}$ over the entire operating frequency region. It further allows to compensate for PVT variations.



(a) General case.

(b) Example for $n = 6$, $w_1 = 4$ and $w_2 = 2$.

Figure 5.29: Single-ended voltage mode weighted phase interpolator with interpolation weights w_1 and w_2 [155].

5.2.4.2 Weighted Phase Interpolators

Similarly to the quadrature phase generator, voltage mode weighted phase interpolators, interpolating input signals V_1 and V_2, are used. They are composed from a set of n unit inverters driving the same output node V_{out}, where $n = w_1 + w_2$ is the sum of the interpolation weights (expressed as integers, i.e. $w_1, w_2 \in \mathbb{N}_0$). This arrangement is sketched in Figure 5.29.

In order to have both inputs equally loaded with n unit inverters, additional dummy inverters are added. This implies $n - w_1$ and $n - w_2$ dummy inverters for the two inputs respectively. This is done to further equalize the load not only at the two interpolator's inputs, but also across all interpolated auxiliary phases, i.e. $\varphi_0, ..., \varphi_{10}$ in Figure 5.27. This setup furthermore ensures equal

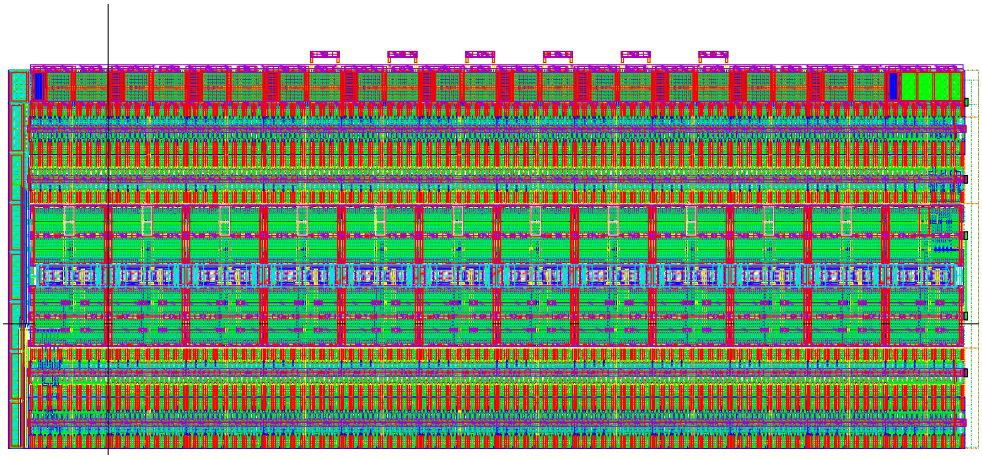


Figure 5.30: Physical drawing of the presented multiphase generator. It occupies an area of 66 µm × 27 µm [155].

driving strength on all interpolated nodes, since always n unit inverters are connected to every output inverter driving $\psi_0, ..., \psi_2$ and $\overline{\psi}_0, ..., \overline{\psi}_2$.

The same considerations regarding overlapping transitions of the interpolator's input signals apply compared to the phase interpolator used with the quadrature generator, discussed in Section 5.1.3.1. In order to meet this condition and achieve linear phase interpolation, the phase shifters are programmable, to allow for the wide range of operating frequencies and compensate for PVT variations.

5.2.5 Simulation Results

The presented circuit, implementing the novel multiphase generation architecture, is designed in a 28 nm bulk-CMOS technology with 0.95 V supply. The physical drawing of the presented block is shown in Figure 5.30. The implemented block occupies an area of 66 µm × 27 µm. All simulations are performed with the post-layout extracted RC-coupled netlists.

The phase shifts versus capacitor settings of the differential output phases are plotted in Figure 5.31a, at $f_{LO} = 2$ GHz for different process corners. The 0°

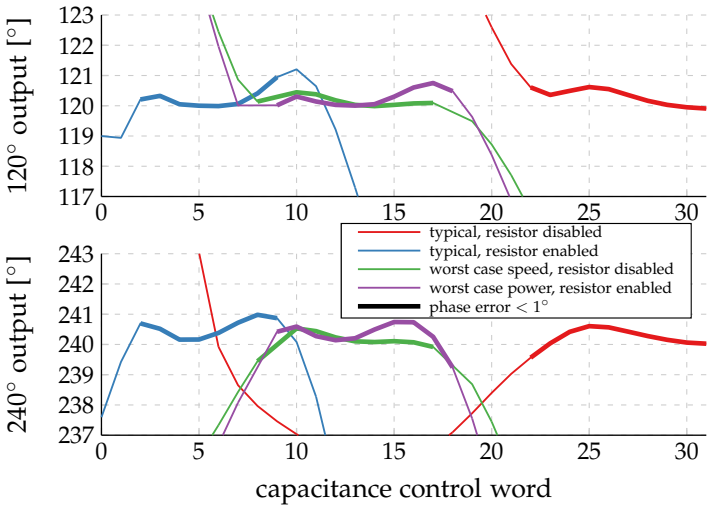
output phase is used as the reference phase. All simulations are performed for different values of the capacitance control word, in order to correctly tune the phase shifters' delay to match operating frequency and PVT variations (see Section 5.2.4.1). The ranges of this control word, where all outputs are within $\pm 1^\circ$ of the target phase shifts simultaneously, are highlighted in the figure. For all cases a rather wide range of several settings is available. Similarly, the additional load resistor is activated and deactivated, as denoted in the plots below.

Figure 5.31b shows the respective power consumption of the circuit for various capacitor settings. Obviously, the load capacitance influences the power consumption plainly by the charge required to charge and discharge the respective nodes. Additionally, the overlap of the interpolators' input signals (or the lack thereof) influences the power consumption. In case of non-overlapping transitions, the phase shift of the outputs deviates from the desired values, since the inverters are driving against each other, sinking a large amount of cross current and the interpolation is not working linearly as required.

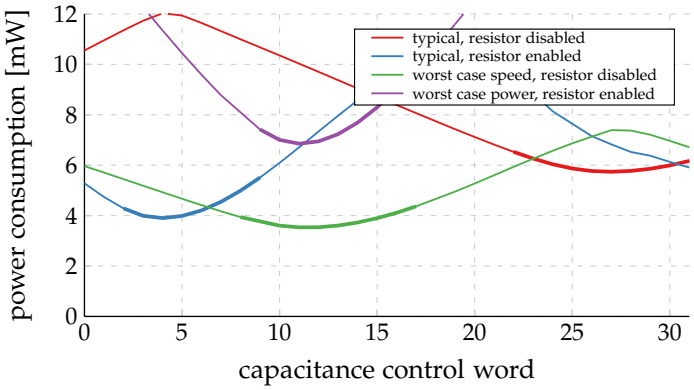
In Figure 5.32, the phase shifts for different operating frequencies f_{LO} are shown. A Monte Carlo simulation is performed with $n = 200$ runs for each simulated point in frequency. Capacitor settings, derived from the ideal mismatch free circuit, are used. A worst case standard deviation of $\sigma = 0.25^\circ$ of the output phases is observed.

Figure 5.33 shows the simulated dependency of the phase shifts on supply voltage. For a variation of $\pm 100\,\mathrm{mV}$ from the nominal value of 0.95 V, the respective deviation of the phase shifts is below $\pm 1^\circ$ in relation to the nominal phase shift at 0.95 V.

The respective phase noise performance at 2 GHz operating frequency, is shown in Figure 5.34 for various process corners. The programming for optimum phase shifts is used to evaluate the phase noise performance. For all cases, a phase noise performance better than $-150\,\mathrm{dBc/Hz}$ at 100 MHz offset frequency can be achieved for meaningful capacitor settings.



(a) Phase shifts. The 0° output phase is used as the reference [155].



(b) Power consumption.

Figure 5.31: Simulated output phase shifts and power consumptions for different process corners at $f_{LO} = 2\,\text{GHz}$ over programming for the post-layout extracted design.

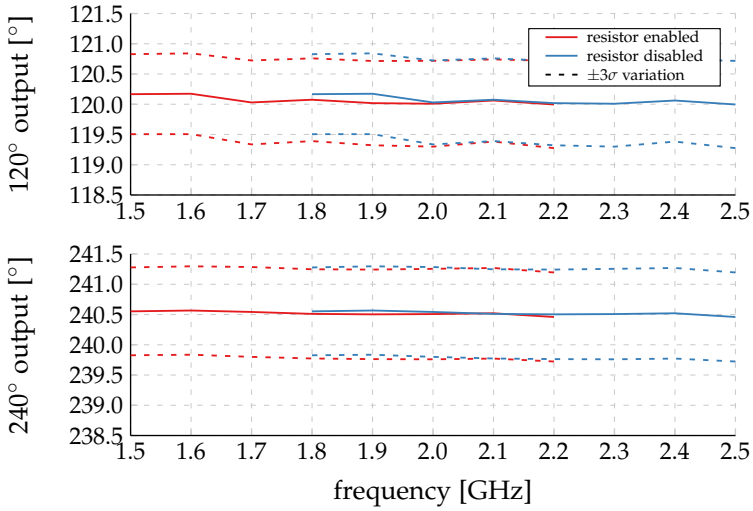


Figure 5.32: Monte Carlo simulated output phase shifts for the post-layout extracted design. For each frequency point $n = 200$ runs are performed. The 0° output phase is used as the reference [155].

5.3 Conclusion

A novel circuit architecture for quadrature and multiphase clock and LO generation has been developed. Within this chapter, the operating principle, circuit design implications, and prototype implementations are discussed.

This principle offers several advantages for implementation in nanometer CMOS technologies:

- open-loop feed-forward operation with low complexity,
- low device count for low noise and power consumption, and
- a digital-like implementation suitable for low supply voltages, technology scaling and portability.

The feasibility of this approach is demonstrated with two demonstrator circuit implementations, a quadrature generator and a multiphase generator, suitable for wireless TRX applications.

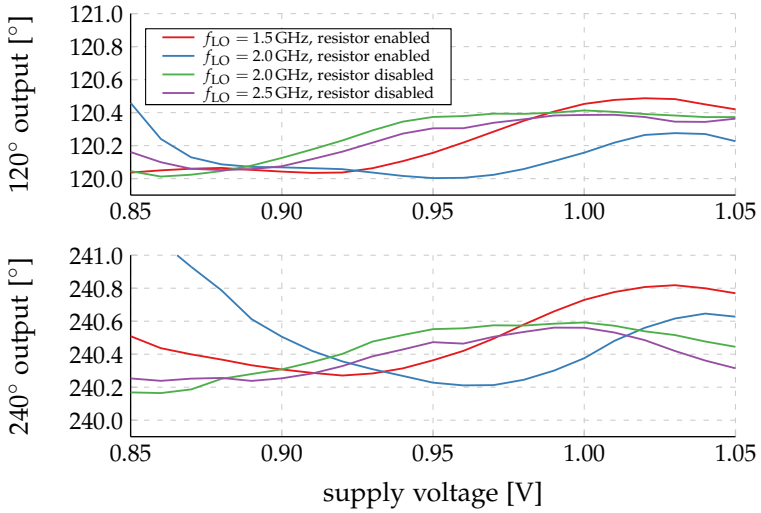


Figure 5.33: Simulated output phase shifts for the post-layout extracted design for several LO frequencies and settings. The supply voltage is varied by $\pm 100\,mV$. The capacitor settings are taken for the nominal value of 0.95 V. The 0° output phase is used as the reference.

A resulting patent application covering the presented multiphase generation approach [154] demonstrates the novelty and its extension to the state-of-the-art. The quadrature generator circuit architecture, discussed in Section 5.1, was first presented in 2016 to the circuit design community [151]. A more detailed journal paper is also submitted [152].

An alternative circuit implementation, adhering to different target specifications, of the same principle demonstrates the versatility and portability of the developed architecture [153]. Finally, the multiphase generator prototype presented in Section 5.2, is presented in 2019 to the circuit and systems community [155].

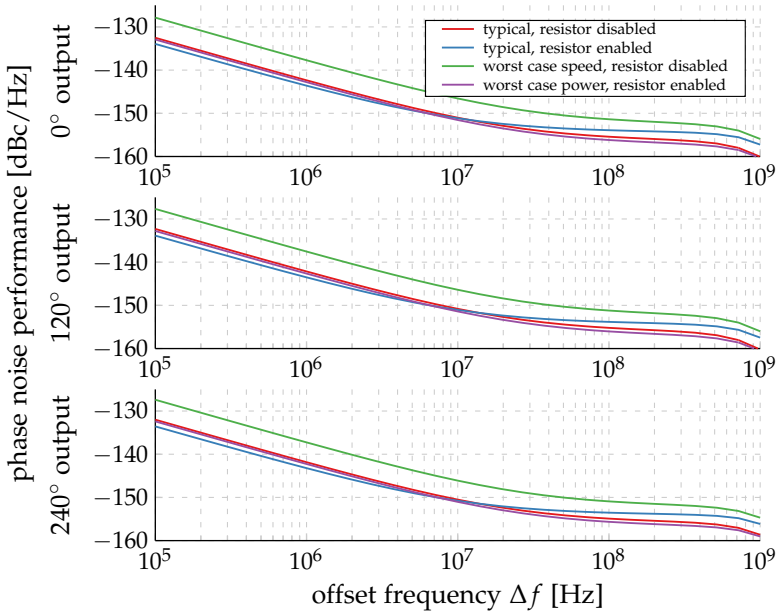


Figure 5.34: Simulated phase noise of the differential outputs for the post-layout extracted design. The respective settings for optimum phase shifts are used [155].

6 Mixed-Signal RF-Domain Self-Interference Cancellation Circuit Design

The circuit level implementation of the mixed-signal RF-domain SIC system discussed in Chapter 4 is detailed in this chapter. Starting with the prototype system's block diagram shown in Figure 4.7, the design includes:

- *Injection-augmented RX*: The available RX is modified in order to allow injection of the cancellation signal generated by cancellation RF-DAC.
- *Cancellation RF-DAC*: The entire cancellation RF-DAC is designed and implemented according to the requirements previously derived and discussed in Chapter 4.

The process of designing these two blocks is a combined effort, as the two directly influence each other. Therefore, the actual choice of the RF-DAC type and architecture are discussed in this chapter. The same holds for the augmentation of the RX.

The available TX subsystem is not modified but solely placed on the TRX system independently. It is used as the source of self-interference and is not further discussed in this chapter. The same holds for the purely digital portions of the signal processing, such as memories and sample rate converters, which are placed as available and thus not further discussed.

The main focus of this chapter is the circuit implementation of the cancellation RF-DAC and all the additionally required blocks, e.g. voltage regulators and biasing circuitry. Furthermore, the modifications of the RX are detailed.

The entire prototype is designed in a 28 nm bulk-CMOS technology using a 0.95 V supply which is derived, on the chip by means of regulators, from a

1.15 V power supply. The already available and reused circuit blocks are also designed and implemented in this very technology.

6.1 A Brief Survey of RF-DACs

Essentially, there are two popular types of RF-DACs available [9] which are briefly discussed in this chapter:

- **Current-mode RF-DAC**: The more *analog* approach, using a set of current sources activated by the digital input code. A current commuting mixer, driven by the LO, is stacked on top to achieve upconversion [174]–[176].
- **Capacitive RF-DAC**: The more *digital* approach, employing a set of parallel capacitors directly switched with the LO. The number of actively switched capacitors is determined by the digital input [100], [177].

There are also further, less popular RF-DAC concepts available, but these are less suitable for general applications and the SIC design at hand.

6.1.1 Current-Mode RF-DACs

The essential circuit of the current mode RF-DAC is shown in Figure 6.1 [9]. A single-ended current DAC generates a baseband current. It comprises a set of current sources, which are activated depending upon the digital input code. The reference current, is mirrored to all the current sources, is programmable in order to digitally adjust the gain and eventually the maximum output current of the RF-DAC.

A current commuting mixer, driven with the LO and its inverse, is stacked on top. This integrated mixer essentially performs the upconversion into the RF domain. Furthermore, a transformer based output matching network is used to perform differential to single-ended conversion and impedance matching. The limited bandwidth also applies a certain amount of bandpass filtering on the RF output. The current-mode RF-DAC is also supplied via the center tap of this matching network, as indicated in Figure 6.1.

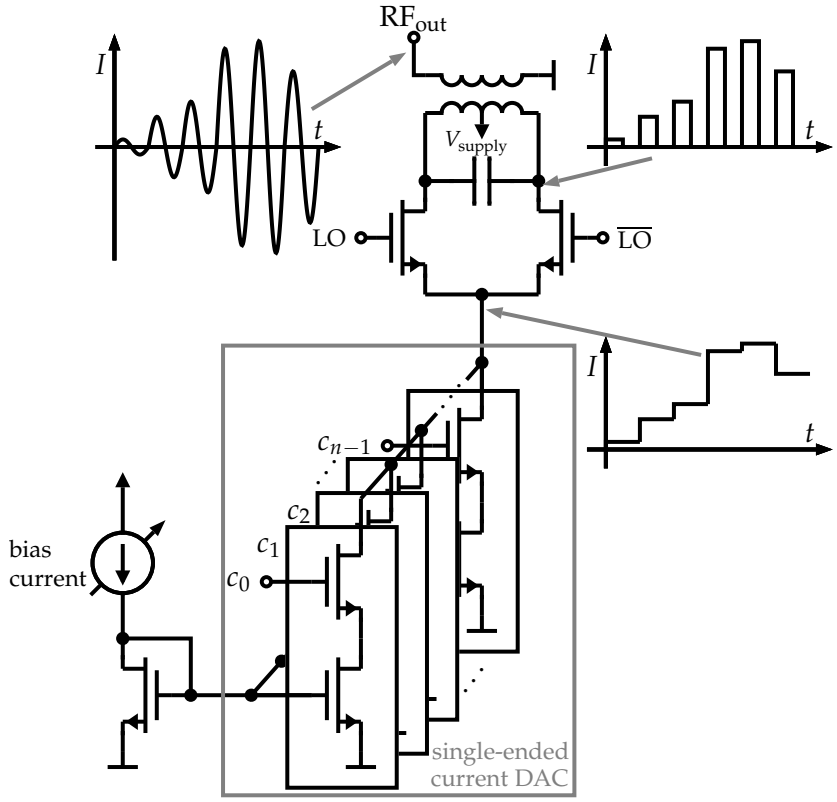


Figure 6.1: Principle circuit implementation of current-mode RF-DACs [9].

The performance of this structure heavily depends on correct bias points, i.e. operating all current source and cascode transistors in saturation. This requirement necessitates a comparably high supply voltage, which becomes more and more problematic with the most advanced CMOS processes.

There are several further considerations related to DAC performance [129]. This includes proper dimensioning of the current source array to control transistor mismatch [178], [179], controlling thermal noise, and reducing integral nonlinearity, which is essentially determined by the DAC's output impedance [180], [181]. There are additional dynamic effects that require compensation which are related to the activation and deactivation of the current sources at LO rate [129], [182].

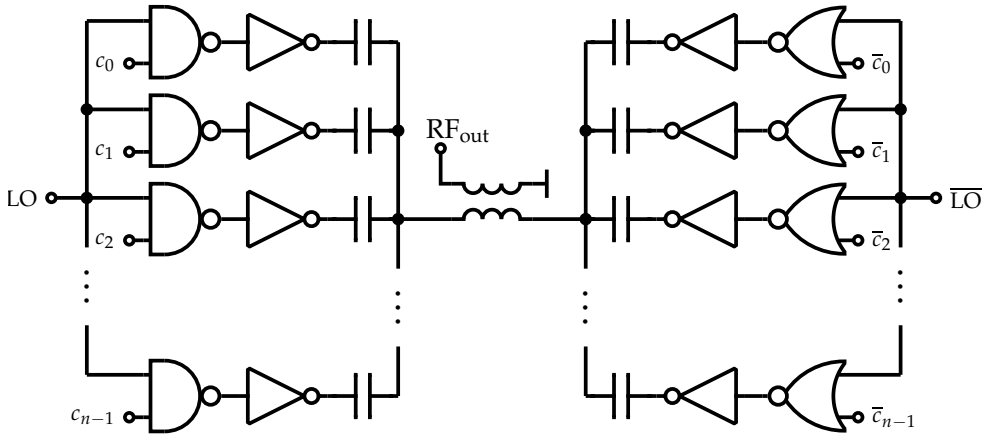


Figure 6.2: Principle circuit implementation of a pseudo-differential capacitive RF-DACs [9], [100].

6.1.2 Capacitive RF-DACs

A more recent alternative to the previously discussed current-mode RF-DAC is its capacitive counterpart [100], [177]. Its principle circuit architecture is shown in Figure 6.2. A set of matched capacitors is driven by the LO signal. In the pseudo-differential case, half of the cells are operated with the inverse LO. The amplitude information, e.g. the digital input code, is digitally mixed with the LO by means of the NAND and NOR gates. Depending on this digital input, the number of actively switching capacitor cells, that contribute to the output, is controlled. This structure essentially is a capacitive voltage divider operated with the LO.

Similar to the current-mode RF-DAC, a transformer based output matching network is added. It provides differential to single-ended conversion, impedance matching, resonates the capacitors, and basic bandpass filtering to suppress higher order harmonics.

This capacitive structure has several benefits over the current-mode RF-DAC. It behaves like a class-D/S/T amplifier enabling high efficiency, which is most important for TXs in battery operated devices. Instead of current sources, capacitors are used as linear matching elements. They do not need voltage headroom for saturation and no biasing circuitry. These capacitors are driven

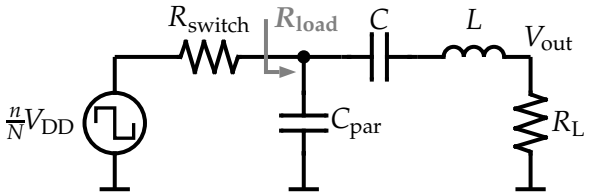


Figure 6.3: Equivalent circuit model of the (single-ended) capacitive RF-DACs [100].

by inverters and very simple logic gates, which are most technology scaling friendly. Furthermore, this circuit structure allows for very low supply voltages well below 1 V.

Although the capacitive RF-DAC offers several obvious advantages, there are some drawbacks. Its sensitivity to the supply voltage is of utmost concern, since it also acts as the DAC's reference voltage. Any disturbances on the supply also directly propagate to the RF-DAC's output due to the limited supply rejection of the inverters. Furthermore, the input code dependent current consumption impacts the supply voltage (over the I(L)R-drop or imperfect supply regulation) which results in nonlinear effects at the DAC's output.

There are further non-ideal effects, mainly related to the imperfect behavior of the driving inverters as switches. This includes different performance and effects of the NMOS and PMOS transistors [100].

The equivalent circuit model of the capacitive RF-DAC is shown in Figure 6.3 [100]. The voltage source driving the circuit is a square wave representing the LO. Furthermore, the amplitude of this source is scaled by $\frac{n}{N}$, where n is the number of actively switching cells and N the total number of cells in the RF-DAC. Effectively it is $\frac{n}{N}V_{\text{DD}}$, where V_{DD} is the supply voltage of the driving inverters.

The first harmonics's output amplitude of the capacitive RF-DAC, neglecting losses, ideally is

$$V_{\text{out}}(n) = \frac{2}{\pi}\frac{n}{N}V_{\text{DD}} \tag{6.1}$$

and subsequently the first harmonic's output power

$$P_{\text{out}}(n) = \frac{2}{\pi^2}\left(\frac{n}{N}\right)^2 \frac{V_{\text{DD}}^2}{R_{\text{load}}} \tag{6.2}$$

where R_{load} is the effective load seen by the RF-DAC.

6.1.3 Conclusion

As discussed in this section, there are two popular choices for RF-DACs available. The current-mode RF-DAC requires rather high supply voltages for high performance operation. The capacitive RF-DAC supports low voltage operation, but due to its digital nature, offers very little power supply rejection.

Essentially all published RF-DACs employed in TX applications are implemented (pseudo) differentially and require some kind of inductive output matching network. This is required for differential to single-ended conversion and for impedance transformation. Many RF components, such as PAs and filters, are single-ended and matched to a 50 Ω impedance, requiring the same for TXs' outputs.

For the application of integrated RF domain SIC, these requirements are not necessarily true. Depending on the RX architecture, a single-ended or differential signal injection and further cancellation RF-DAC outputs are required. Also, the output impedance essentially only depends on the RX and the chosen point of injection. Even mismatched operation of the cancellation system is possible.

And finally, the absence of another bulky on-chip inductor or transformer is always welcome. If the RF-DAC employed in the cancellation system can spare such an output matching network, a very compact solution is possible. It would further reduce any electromagnetic coupling and other unwanted crosstalk effects.

It becomes clear that the actual requirements on the cancellation RF-DAC are determined by the RX and the injection point. One of the presented RF-DAC architectures could be adapted to meet these expectations.

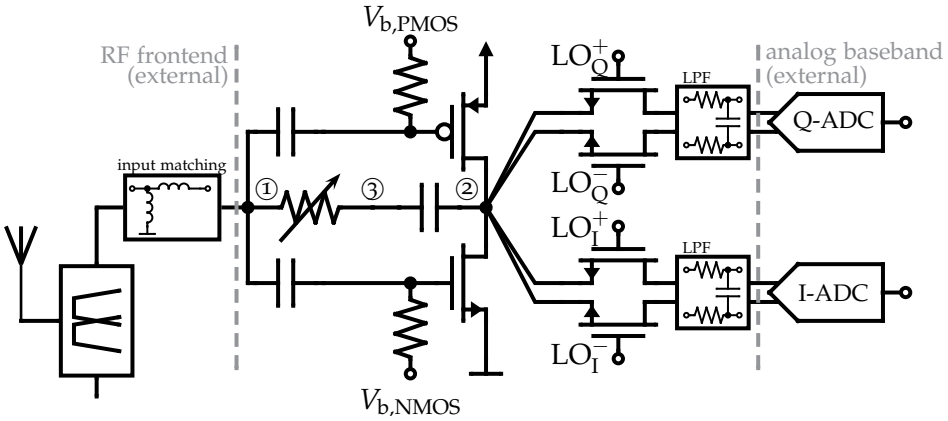


Figure 6.4: RF and analog portions of the adopted RX. Possible on-chip injection nodes are annotated. Bias circuitry omitted.

6.2 Injection-Augmented Receiver Design

In order to decide on a cancellation RF-DAC architecture and the point of signal injection, the adopted RX [104] is briefly discussed. The circuit implementation of the unmodified and previously available RX signal path is shown in Figure 6.4.

6.2.1 Adopted Receiver Design

The RX is single-ended in the RF domain. Single-ended to differential conversion is achieved by a passive CMOS mixer. Therefore, no bulky on-chip inductors or transformers are required. This RX can be implemented very area efficiently.

Matching to 50 Ω is achieved with an external matching network. A push-pull common source LNA is capacitively alternating current (AC) coupled to the input, where also additional electrostatic discharge (ESD) protection circuitry is added. The LNA essentially operates as a low noise transconductance. The bias potential of the NMOS and PMOS are set individually with bias resistors. This way, the bias current through the LNA and its zero output potential can be precisely controlled. These biasing circuits are not shown in Figure 6.4.

Additionally, an AC coupled programmable feedback resistor is included to simplify input matching for different bands of operating frequency.

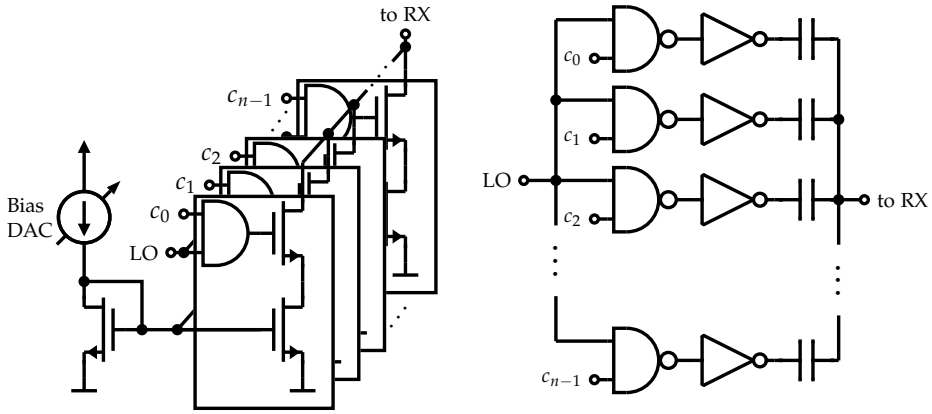
The downconversion mixer is a single-balanced passive mixer [183]–[185] that also performs single-ended to differential conversion. The respective LO phases all have a 25 % duty cycle. This portion of the RX circuit, starting with the output of the LNA, operates in the current domain. Finally an active low pass filter, that also drives the chip output, loads the mixer. For this demonstrator, the ADCs are external, as already discussed in Chapter 4.

6.2.2 Cancellation Signal Injection

Prior to in-depth circuit design, a decision on the type of RF-DAC architecture and the method of cancellation signal injection into the RX must be taken. In order for the circuit to fulfill the system level requirements discussed in Chapter 4, this decision is mainly driven by the circuit level implications of the respective possibilities. This section details the RF-DAC architecture choice and the necessary modifications to the previously available RX.

In order to get to an architecture decision in a reasonable time frame, i.e. to reduce the required simulation run times, initially, the impact of adding an RF-DAC on the RX is evaluated with simplified models. The available RF-DAC choices are assumed to not need any inductive output matching network. The simplified circuits are shown in Figure 6.5. As the RF portion of the RX is single-ended, also single-ended RF-DAC models are used.

From the two simplified models a basic conclusion can immediately be drawn: The current-mode RF-DAC's output can essentially be connected to any node, it will sink current as determined by the digital input code. A requirement is though, that the voltage level seen by RF-DAC does not drop too low, otherwise the current sources will not be in saturation. For the NMOS-only version, all currents drawn must also be supplied though this node. Furthermore, in this configuration, the current-mode RF-DAC can only sink current. A possibility is to build a push-pull current RF-DAC, which has complementary PMOS current sources, feeding current into the injection node. This comes at the cost of increased capacitive loading and NMOS/PMOS mismatch.



(a) Current-mode RF-DAC.

(b) Capacitive RF-DAC.

Figure 6.5: Simplified single-ended current-mode RF-DAC models, omitting any inductive output matching networks.

For the capacitive RF-DAC the behavior is inherently different. First, the output is capacitively coupled, implying that not every node is suitable for injection. Second, depending on the LO polarity, a signal can be added or subtracted from the injection node. Third, due to the capacitive coupling, no current needs being supplied through the injection node.

The three possible injection points with an RF-DAC are annotated in Figure 6.4 as ① to ③. The addition of any type of RF-DAC will essentially capacitively load this node. Representative simulation results, i.e. for nominal PVT values, when adding capacitances to the potential injection nodes, are shown in Figure 6.6. This includes, as an illustrative example, gain and NF at 3 MHz and the required series L_s and parallel L_p inductances for impedance matching to 50 Ω at the RX input for an LO frequency of $f_{\mathrm{LO}} = 2.14\,\mathrm{GHz}$.

The gain is measured from a 50 Ω input port to the analog baseband output of the RX, right at the input of the active low pass filter. The negative logarithmic values in Figure 6.6a denote voltage gain, which are a result of the RX's output being in the current domain.

Reasonable capacitive loads introduced by a directly connected RF-DAC as sketched in Figure 6.5 are well above 1 pF. Generally the parasitics of the

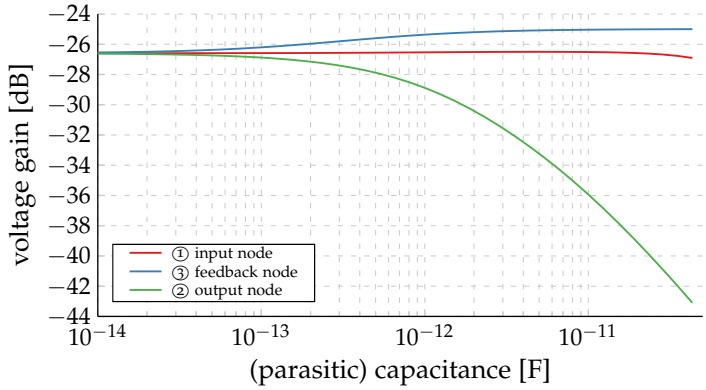
interconnect through such an array of current sources or capacitors amount to values in that range. Assuming a total array capacitance of 1 pF, for a capacitive RF-DAC with 13 bits of physical amplitude resolution, the smallest capacitor would be 0.12 fF, which is already close to being unfeasibly small.

The first option ① is to inject the cancellation signal directly at the RX input. The major drawback of that, independently of the chosen RF-DAC type, is the additional capacitive loading of the input. This (parasitic) capacitance will inevitably form an unwanted shunt capacitor in parallel to the AC coupling capacitors and therefore reduce the effective LNA gain and NF. This is true whether or not the SIC system is activated or not. In Figure 6.6 this effect is not directly visible, because it is compensated by the adapted input matching. In turn, the input matching inductances need to assume impractically small values in the sub-nH region, which eventually reduces the achievable matching network bandwidth, as shown in Figure 6.6c. A qualitatively equal behavior is exhibited for different offset frequencies Δf and LO frequencies f_{LO}.

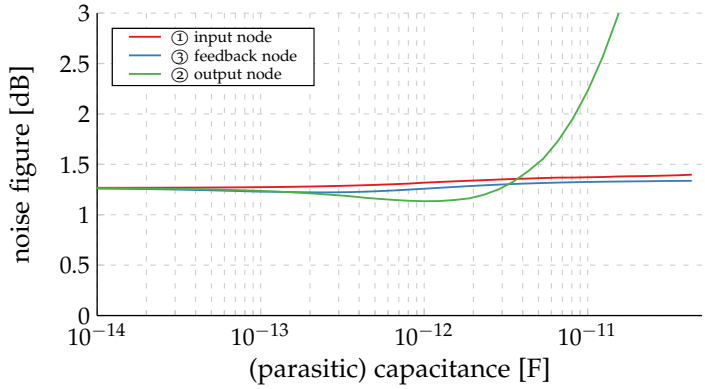
Of course, the least amount of signal power from the canceler is required in this case, since no amplification has yet happened. On the other hand, when injecting a signal at the input node, it will be also amplified by the LNA. This especially holds for any noise generated by the cancellation RF-DAC.

The second option ② is to inject at the LNA's output at the mixer input. Doing so capacitively loads the LNA's output. Depending on the chosen RF-DAC type, the strength of this effect varies also with dimensioning of the RF-DAC components. But already these initial simulations, shown in Figure 6.6, reveal that LNA gain and NF suffer heavily for realizable capacitive loading. Beneficial to this approach would be that the noise requirements on the RF-DAC can be relaxed, since the cancellation signal is injected after the RX input signal has been already amplified. The same behavior is observed also for other LO frequencies f_{LO}.

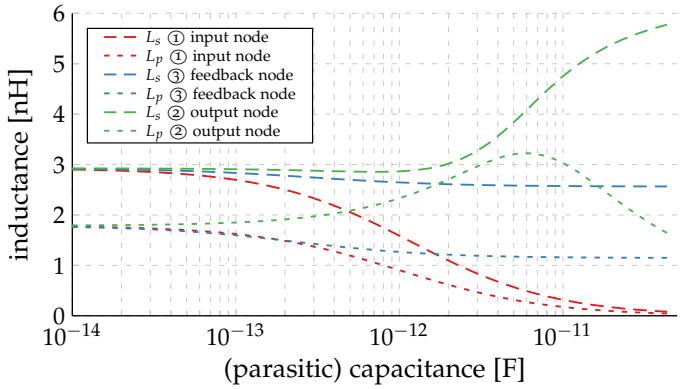
The third and most attractive option ③ is to inject into the feedback network of the LNA. There is virtually no capacitive loading of neither input nor output of the LNA. For (parasitic) capacitive loads in the single picofarad region, the decrease in gain and increase in NF of the LNA is negligible compared to the other options, as seen in Figure 6.6. Also, the input matching hardly



(a) Voltage gain at $\Delta f = 3\,\mathrm{MHz}$.



(b) NF at $\Delta f = 3\,\mathrm{MHz}$.



(c) Input matching inductors.

Figure 6.6: Simulation results for added (parasitic) capacitances at the LNA ① input, ② output, and ③ feedback nodes at $f_{\mathrm{LO}} = 2.14\,\mathrm{GHz}$.

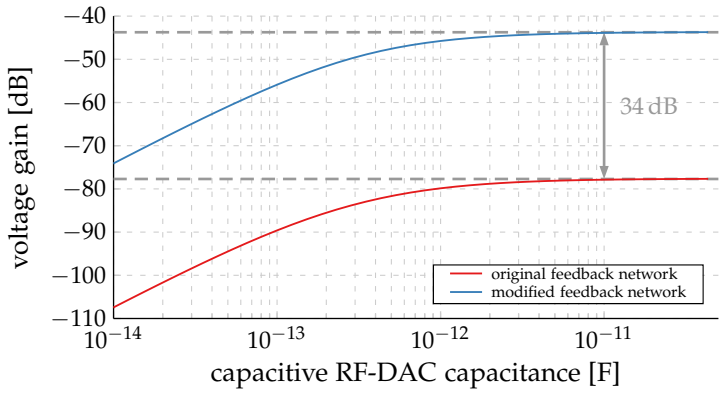


Figure 6.7: Simulated transfer function for the injection node of the LNA at $f_{LO} = 2.14\,\text{GHz}$.

changes compared to the unmodified RX. Equal behavior is also exhibited for different LO frequencies f_{LO}.

Judging by these results, the most obvious solution so far is to inject the cancellation signal into the feedback node. Since the capacitance added there is not too critical, the capacitive RF-DAC is a promising option, as it does not require any change in the LNA's bias potentials.

In Figure 6.7 the transfer function from the point of injection to the RX baseband output is shown, for the (original) LNA's feedback network as sketched in Figure 6.4. This transfer function is similar to the main RX signal characteristics shown in Figure 6.6a.

When comparing these two figures, the difference in the magnitude of the transfer functions is of interest. As explained later, a capacitive RF-DAC is chosen. This DAC has a maximum first harmonic's output amplitude of

$$V_{inj} = \frac{\sqrt{2}}{\pi} V_{DD} \tag{6.3}$$

which, for a 0.95 V supply translates to more than 400 mV.

The maximally expected peak leakage amplitude is 22 mV at the RX input at 50 Ω, as discussed in Section 4.2.1. This difference can be exploited to tolerate less gain from the injection port to the LNA output compared to the main RX

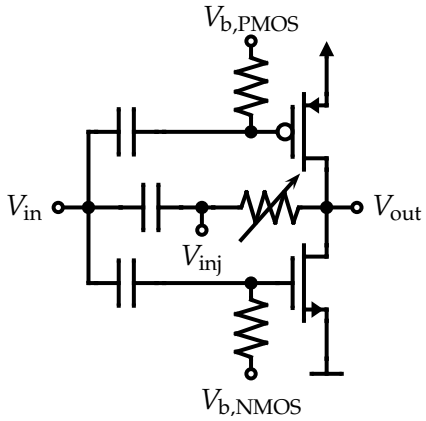


Figure 6.8: LNA with modified feedback network to enable signal injection.

gain. The direct comparison of the two peak amplitude values result in a relaxed gain requirement of the injection path of 25 dB.

While the main LNA gain is approximately at -25 dB (cf. Figure 6.6a), the respective injection gain is -77 dB (see Figure 6.7), with the original LNA circuit as shown in Figure 6.4. Unfortunately, this injection transfer function is 52 dB less, which is well below the tolerable 25 dB.

In order to overcome this issue, the LNA circuit is modified. As shown in Figure 6.8, the elements in the capacitively coupled feedback network are exchanged. Instead of directly connecting the programmable resistor with the RF input, the coupling capacitor is placed there. The benefit of doing so is shown in Figure 6.7. The transfer function of the injected signal is improved by 34 dB to a saturated value of -43 dB, which is only 18 dB less than the main RX transfer function. With this modification, the requirements can be fulfilled, leaving some margin, e.g. for PVT.

Another important aspect is to decouple the value of the cancellation capacitive RF-DAC's total array capacitance from the one that is seen by the LNA. The reason is to gain more flexibility in this RF-DAC parameter, as silicon area and capacitor matching is essentially determined by the DAC cell's capacitors. To achieve this behavior, an additional series capacitor, connected between the RF-DAC output and the injection node in the LNA is added.

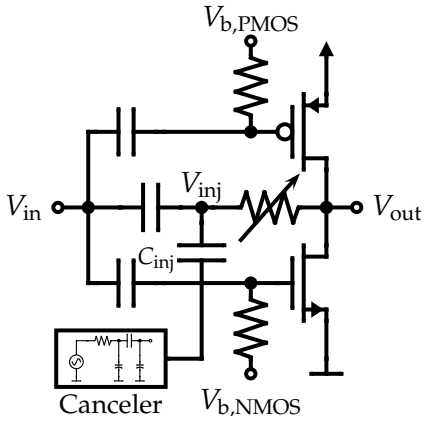


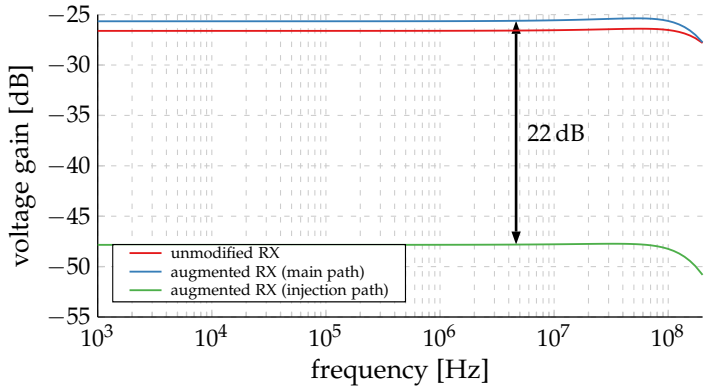
Figure 6.9: LNA with modified feedback network and the additional series injection capacitor C_{inj}.

This arrangement is shown in Figure 6.9. The effective injection capacitance seen by the LNA therefore is determined by this series capacitor, assuming that the RF-DAC's total capacitance is much larger. A series capacitor of $C_{inj} = 600\,\text{fF}$ is chosen, resulting in an injection gain of $-47\,\text{dB}$, which, compared to the $-25\,\text{dB}$ of the main transfer function, still yields a reasonable margin of 3 dB to the requirements.

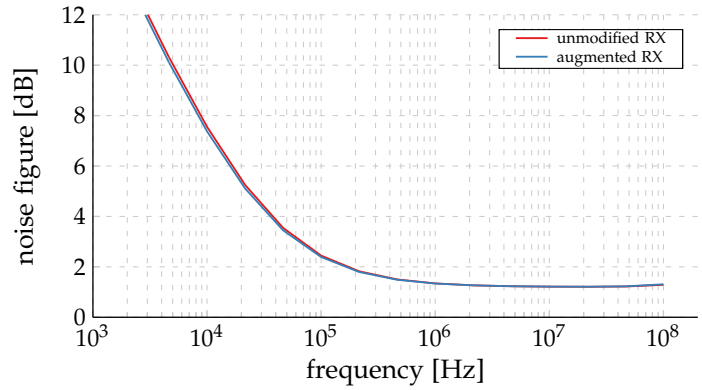
Finally, the transfer functions and NF of the injection augmented RX are shown in Figure 6.10 for an LO frequency of $f_{LO} = 2.14\,\text{GHz}$. Very similar behavior is observed over the entire targeted operating frequency region. A total RF-DAC capacitance of around 3 pF is assumed as a starting point and used for these initial simulations.

6.3 Cancellation RF-DAC Design

This section details the design of the cancellation RF-DAC employed in the RF domain mixed-signal SIC system. As discussed in the preceding sections, a capacitive RF-DAC with a single-ended output, omitting any inductor or transformer based output matching network, is favorable. From these requirements, a key design implication can already be derived: Since there is no



(a) Voltage gain.



(b) NF.

Figure 6.10: Simulation results of the injection augmented LNA at $f_{LO} = 2.14\,\text{GHz}$.

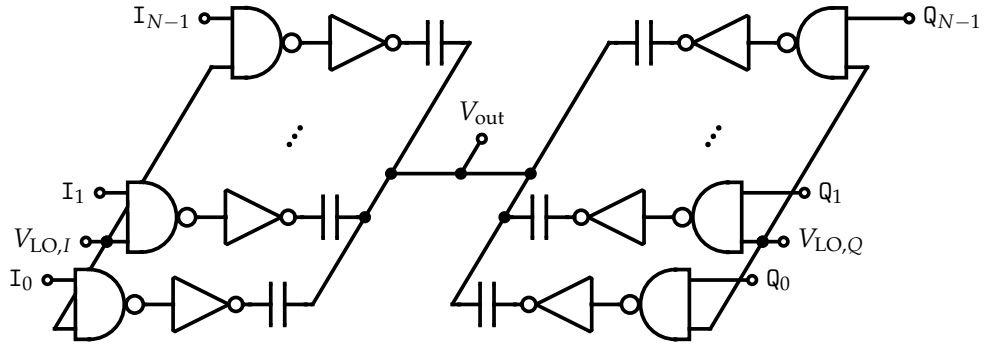


Figure 6.11: Principle capacitive cancellation RF-DAC circuit structure with cells assigned to the in-phase and quadrature components.

obvious differential to single-ended conversion by means of a transformer possible, the entire DAC needs to be single-ended.

There are hardly any RF-DACs published that do not rely on inductive matching networks, relying on impedance matching and/or differential to single-ended conversion. A notable exception is the rather novel concept of charge based RF-DACs [186], where solely the PA employs inductors. Otherwise, published RF-DACs almost always are implemented (pseudo) differentially and their output is matched to 50 Ω. Therefore, a different, single-ended RF-DAC approach, based on the capacitive RF-DAC, is developed in this section.

6.3.1 Cancellation RF-DAC Architecture

The essential circuit topology of the designed RF-DAC is shown in Figure 6.11. As discussed earlier in Section 6.1.2, a set of capacitors, usually arranged in a cell array, is driven with the LO. The number of capacitors actively switched is determined by the digital input code, essentially setting the capacitive voltage division ratio. Further, the cancellation DAC is a quadrature system, where half of all capacitors are assigned to the in-phase signal component $\mathtt{I}_0, ..., \mathtt{I}_{N-1}$ and $V_{\text{LO},I}$, while the other half is associated with the quadrature component $\mathtt{Q}_0, ..., \mathtt{Q}_{N-1}$ and $V_{\text{LO},Q}$.

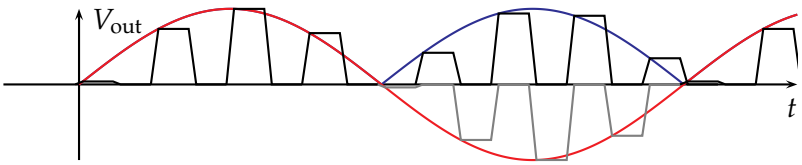


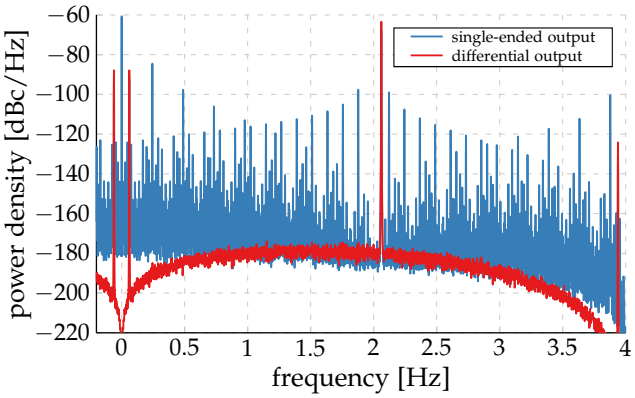
Figure 6.12: Exemplary unloaded output signal of the capacitive RF-DAC for different polarity of the input data. Only a single phase (either in-phase or quadrature) is sketched. The red curve signifies the underlying baseband data, while the blue curve indicates the effective magnitude output by the RF-DAC. Also the theoretical output of a DAC having negative supply voltages is sketched in gray.

6.3.1.1 Four Quadrant Operation

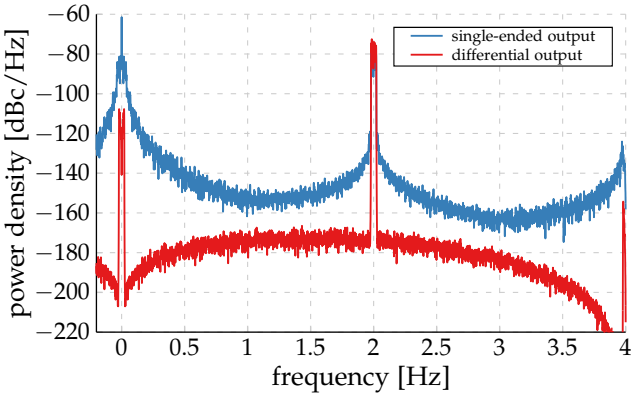
The single-ended nature of the developed RF-DAC presents several challenges. One of them is four quadrant operation, in order to cover the entire complex plane. Even though a signal can be injected with either polarity by means of a capacitive RF-DAC as stated in Section 6.2.2, several issues are encountered. For (pseudo) differential RF-DACs, there is principally no issue. The sign of the underlying input signal can easily be reflected in the RF domain by inverting the respective LO phases accordingly [187].

The exact same method could also be used in a single-ended capacitive RF-DAC. The respective simplified output signal is sketched in Figure 6.12, where also the underlying signed baseband data and the effective output signal are sketched in red and black respectively.

The issue with this approach is a further signal dependent component introduced around direct current (DC). In addition to the desired output in the RF domain, the envelope of the signal is directly present at the output, as indicated in blue in Figure 6.12. Contrary to the portion in the RF domain, whose polarity is determined by the LO phase, this is not true for the component around DC. This part always exhibits the same polarity. Effectively, the absolute value of the DAC's input signal is directly fed to the output, which obviously is a harsh nonlinearity resulting in undesired harmonics, as shown in Figure 6.13 for a single tone and a 40 MHz bandwidth signal. For comparison, the figure further includes an output spectrum of an equivalent differential RF-DAC.



(a) Single tone complex exponential at $f = 61.05\,\mathrm{MHz}$



(b) 40 MHz bandwidth multi tone signal.

Figure 6.13: Single-ended and differential output spectra $f_{\mathrm{LO}} = 2\,\mathrm{GHz}$ for 13 bits quantization.

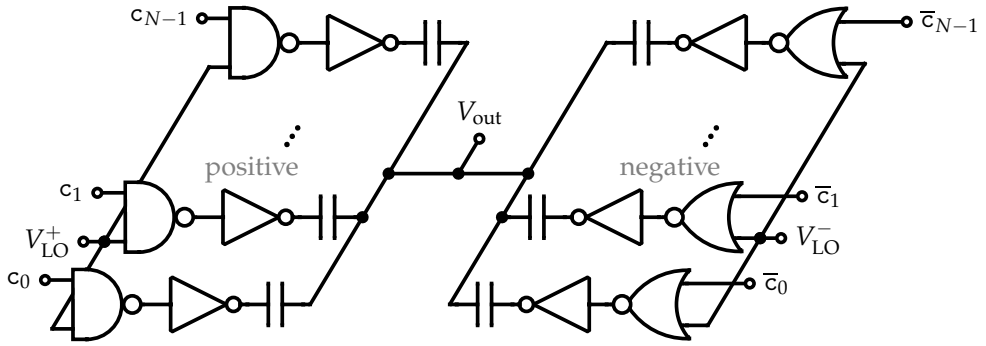


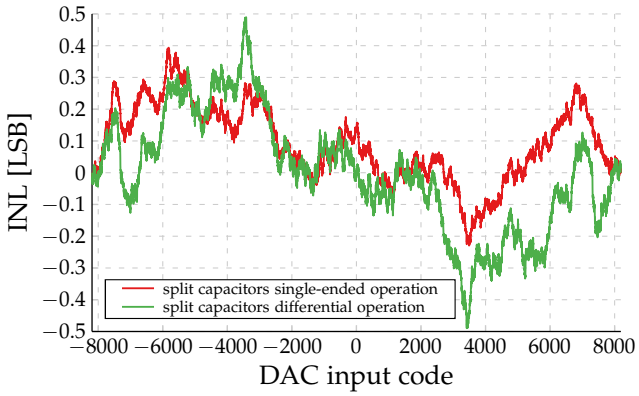
Figure 6.14: Principle capacitive cancellation RF-DAC circuit with split capacitors assigned to positive and negative data polarities. Only a single phase (in-phase or quadrature) is shown.

To overcome this issue, a naive solution is to include a negative supply voltage. The respective output signal pulses are drawn in Figure 6.12 in gray. There are many drawbacks to an additional supply voltage, including its generation and increased circuit complexity.

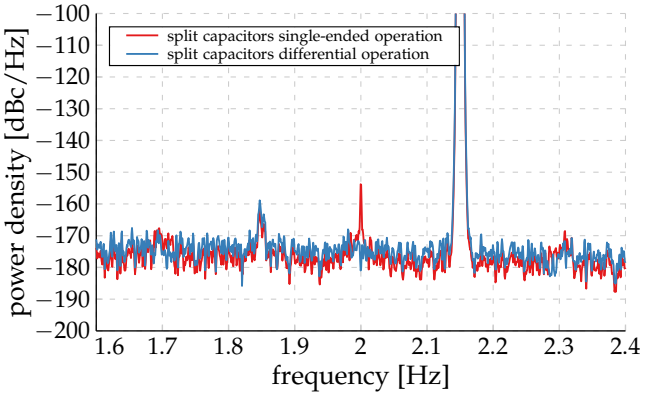
A new approach, circumventing the issues related to four quadrant operation, achieving the same output signal, is sketched in Figure 6.14 for a single phase (either in-phase or quadrature). The AC coupled nature of the capacitive RF-DAC is exploited to mimic the effect of a negative supply voltage: cells that are assigned to the negative polarity switch to ground when active, as opposed to the positive cells which switch to the supply voltage. A drawback of this approach is the reduction of the maximum achievable output voltage by $\frac{1}{2}$.

Unfortunately, having split capacitors, where activation depends upon the input data's polarity, results in unsymmetrical integral nonlinearity (INL) characteristics. In general, such a INL profile has even order components. When operating the cancellation RF-DAC at an offset, e.g. synthesizing a signal centered around the TX frequency but using the RX LO, as suggested in Section 4.2.5, even order INL components will cause undesired signal energy deposited directly back to the RX frequency [188]–[191].

This essentially implies increased noise directly in the RX band, which of course is to be avoided. A representative example INL characteristic and re-



(a) Example INL characteristics.



(b) Resulting output spectrum of a 10 MHz bandwidth signal at 150 MHz offset from the LO.

Figure 6.15: Output spectra of a single-ended split capacitor RF-DAC with polarity dependent activation of cells and the respective pseudo differential operation at $f_{\mathrm{LO}} = 2\,\mathrm{GHz}$ for 13 bits quantization.

sulting output spectrum is shown in Figure 6.15. Note that this behavior in the spectrum can be considered as an increase of the RF-DAC's OOB noise floor, which is also the focus of the figure. This behavior is independent of LO frequencies and signal properties such as bandwidth and PAPR.

A novel way to symmetrize the single-ended DAC's transfer function is presented: The already pseudo differential circuit shown in Figure 6.14 is operated in exactly this way. Independently of the input data's polarity, an equal

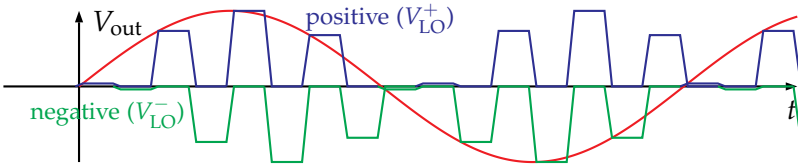


Figure 6.16: Exemplary output signal of the single-ended capacitive RF-DAC with the proposed pseudo differential operation mode. Only a single phase (either in-phase or quadrature) is sketched. The red curve signifies the underlying signed baseband data. The blue and green signals indicate the contribution to the output by the positive and negative cells respectively.

number of cells from both the positive and negative sets are activated. The polarity of the output signal is determined by the order of activation of the respective cells, i.e. for positive input data the positive cells are activated before the negative ones and vice versa as sketched in Figure 6.16.

This mode of operation results in a DC-free output signal, independent of the input data, as shown in Figure 6.16. Furthermore, shown for one example in Figure 6.15, this mode of operation results in an antisymmetric INL characteristic. This symmetry nulls all even order components, which is a clear benefit of this architecture. There is no energy deposited back to the RX frequency when synthesizing a signal centered around the TX frequency. In other words, in the example shown in Figure 6.15b, no increased noise floor around the RX frequency is observed. Additionally, there is no drawback in terms of maximum output amplitude achieved by the RF-DAC compared to the purely single-ended approach.

With this, the proposed single-ended capacitive RF-DAC four quadrant operation is enabled. There is no drawback in maximally achievable output amplitude. Furthermore, no additional auxiliary or negative supply voltages are needed and the INL and DAC transfer characteristics are fully symmetric.

6.3.1.2 Sign Switching

The RF-DAC architecture principally allows for four quadrant operation. Still, a related architectural problem remains: directly switching the polarity of the output signal, dubbed sign switch or sign change. Updates to the input

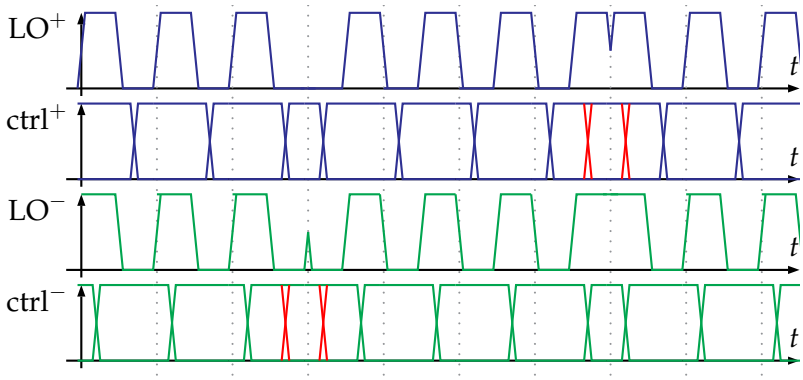


Figure 6.17: LO and control signals for positive and negative cells in the cases of sign changes. The critical control signal transitions are highlighted in red.

data of the RF-DAC, happening e.g. at LO rate, includes amplitude data as well as its polarity, i.e. the sign. Simultaneously changing the amplitude data dependent control signals to the individual capacitor cells and the temporal order of the positive and negative LOs leads to glitches, transitions driven by control signals, and other undesired effects degrading the DAC performance [192].

The critical scenarios are sketched in Figure 6.17 for an RF-DAC implementation as sketched in Figure 6.14. Positive and negative LOs are gated with NAND and NOR gates respectively. When control signals are updated during the respective inactive periods of the LOs, the instant when the DAC output signal changes is only determined by the LO. Thus, the control signals' performance, i.e. phase noise, is relaxed, as the only requirement is to fulfill this timing.

In the case of touching LO transitions, also the control signals need to be correctly updated according to the RF-DAC's input data. But this change obviously needs to happen instantaneously, exactly at the original LO transition. For implementations, such a scenario obviously is unfeasible. The result, when the control signals change while the LO is active, is an erroneous output signal.

In Figure 6.17 the critical control signal transitions are highlighted. Depending on which of the polarities is dominant, either one (or both) of the control

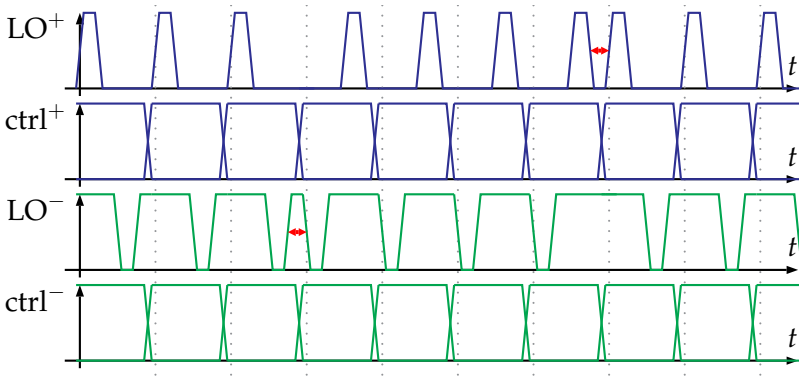


Figure 6.18: 25 % duty cycle LO and control signals for positive and negative cells in the cases of sign changes. There is always a $\frac{T_{LO}}{4}$ window, highlighted, where the data can be updated independently of the polarity of the data.

signal transitions happen. But both of the potential transitions occur while the respective LO is active, resulting in undesired glitches and data driven transitions.

There are possibilities to overcome this limitation. One of them relies on having additional spare capacitor cells that are exclusively used for this sign change operation [193]. Such a solution introduces additional complexity and control signal traces, which potentially break the symmetry of the capacitor cell array. Other solutions with different benefits and drawbacks are summarized in a patent application [192], partially developed throughout this thesis.

An alternative approach is to trade maximum output amplitude of the first harmonic. Essentially, an LO duty cycle lower than 50 % is used to avoid the touching LO transitions, opening up a polarity independent temporal window where the LOs are inactive. For this specific prototype, 25 % duty cycles are used for the LOs, allowing for a $\frac{T_{LO}}{4}$ sign independent period where all control signals can be updated. These scenarios are sketched in Figure 6.18.

A drawback of this approach is the more stringent timing requirement to change the control signals, reduced from $\frac{T_{LO}}{2}$ to $\frac{T_{LO}}{4}$, when designing for the worst case, i.e. during a sign change. Furthermore, the maximum output amplitude of the first harmonic is reduced by $\cos(\pi \cdot d) = \frac{\sqrt{2}}{2}$, where $d =$

0.25 is the duty cycle. For the application of SIC, this is a reasonable trade off to reduce implementation complexity, power consumption, and layout effort.

The maximum possible first harmonic's output amplitude the DAC can achieve with its 25 % duty cycle, ideally, without losses due to parasitics, is

$$V_{\text{out,max}} = \underbrace{\frac{4}{\pi}}_{\substack{\text{Fourier}\\ \text{coefficient}}} \underbrace{\cos\left(\frac{\pi}{4}\right)}_{\substack{25\,\%\text{ duty}\\ \text{cycle}}} \underbrace{\frac{1}{2}}_{\text{I/Q}} V_{\text{DD}} = \frac{\sqrt{2}}{\pi} V_{\text{DD}} \tag{6.4}$$

which is reduced by 6 dB, compared to an ideal 50 % duty cycle single phase RF-DAC implementation [100].

6.3.1.3 Conclusion

To conclude this section, the novel architecture of the capacitive cancellation RF-DAC is summarized: The capacitor cell array is split into two halves, assigned to the in-phase and quadrature components of the signal respectively. As introduced previously in this work, the individual cells are pseudo differential with a single-ended output, as sketched in Figure 6.14. This allows for different signal polarities by exchanging the temporal order of the LOs signals without introducing any unwanted spectral components that compromise the performance of the DAC.

Furthermore, to allow for a simplified implementation, maximum achievable output amplitude is traded-off by using 25 % duty cycle LO signals. Doing so allows for glitch and error free sign changes. Moreover, no additional signal traces or dedicated cells are required, keeping the symmetry and equality of all cells. Alternative approaches to the sign change issue have been developed and resulted in a patent application [192].

The result is a novel capacitive quadrature single-ended RF-DAC architecture, depicted in Figure 6.19. Additionally to the discussed capacitor cell array, a quadrature LO divider or generator with 25 % duty cycle and LO buffers are added. Moreover, a data decoding scheme is required to correctly address the individual cells.

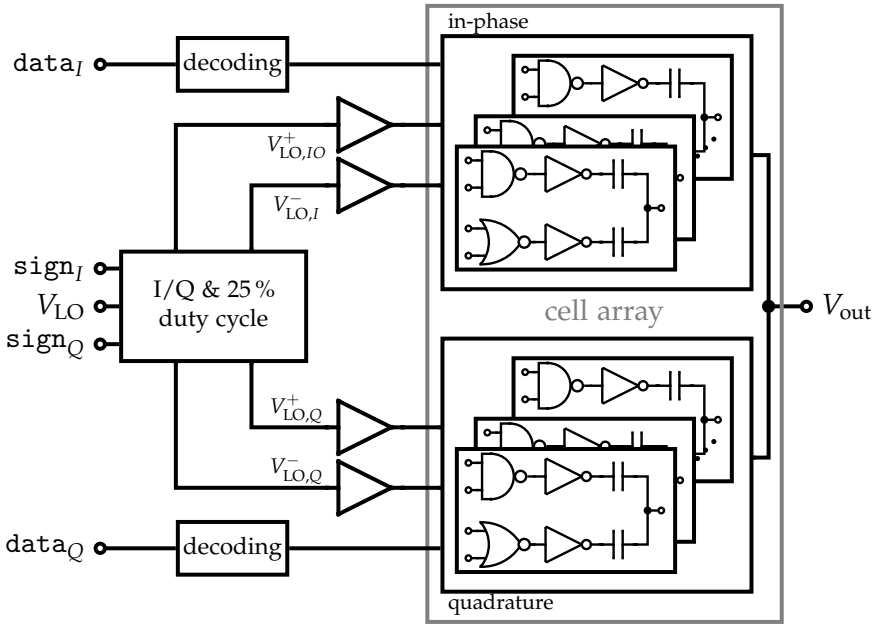


Figure 6.19: Proposed cancellation RF-DAC architecture.

6.3.2 Noise Contributors and Budget

As already discussed in Section 4.2.2, noise performance of the cancellation RF-DAC in the RX band is crucial for system performance. In order to fulfill these requirements, a noise budget for the individual noise sources within the RF-DAC needs to be allocated.

The outcome of this analysis determines circuit design targets, since there are no architectural limitations in terms of noise performance. Essentially, the number of bits, segmentation and individual transistor dimensions are influenced by the required noise performance.

The noise specification of $-157\,\mathrm{dBc/Hz}$ of the main TX is specified at an output power of $-3\,\mathrm{dBm}$ at 80 MHz offset from the carrier [129]. This is essentially the worst case in terms of absolute noise power in the RX band. For the canceler, a point in TX output power needs to be defined, where this noise

performance needs to be matched, e.g. at the TX power level when the canceler is turned on. For simplicity, for the discussed demonstrator, this point was set to 3 dB backoff from the cancellation RF-DAC's full scale.

For powers above this point the specification in dBc/Hz stays constant. For lower powers, this value is allowed to increase by 1 dB per dB of less output powers, resulting in a constant noise floor.

Essentially, there are four contributors to the DAC's output noise:

- **thermal noise** of the RF-DAC components and supply, truly random noise
- **quantization noise** due to the limited resolution of the DAC, deterministic but noise-like behavior for practical signals
- **switching noise** generated through the supply impedance of the RF-DAC, deterministic but also noise-like behavior
- **device mismatch** also generates undesired deterministic signal components, which are treated as pseudo random

6.3.2.1 Thermal Noise

The thermal noise of the DAC is the only truly random noise source. There are two components comprising the thermal noise contribution of the RF-DAC.

First, as the output is directly connected to the supply of the capacitor cell array through the inverters' switches, also any thermal noise on that supply propagates to the output.

Second, the thermal noise of all devices in the RF-DAC, that are driven by the LOs and effectively contribute to the output, is converted to phase noise seen in the output signal. Essentially, steep rise and fall times and low parasitics on all signals traces help reducing the effective phase noise [194]. Finally, all transistor dimensioning and power consumption is determined by the required phase noise performance.

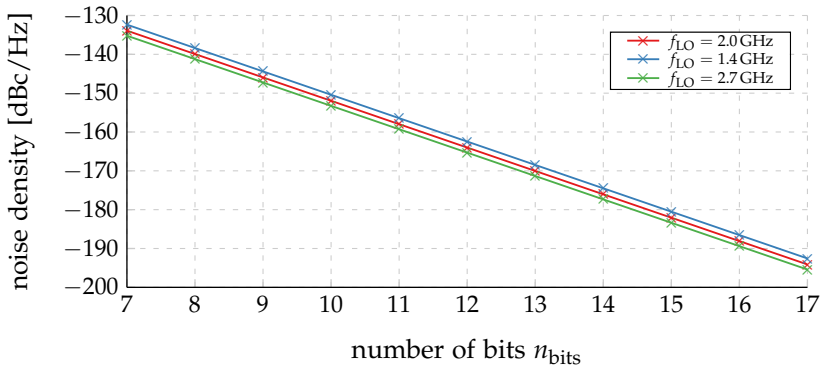


Figure 6.20: Expected quantization noise levels for different LO frequencies. The number of bits n_{bits} excludes the sign information.

6.3.2.2 Quantization Noise

Quantization [195] noise essentially is not a truly random signal but dependent on the input signal of the RF-DAC. For practical input signals, it behaves like a frequency flat noise signal, whose power only depends on the DAC's resolution. The well known quantization noise power formula, for the case of the RF-DAC is

$$N_Q|_{\text{dBc/Hz}} = 10\,\log_{10}\left(\frac{2}{12}\frac{1}{f_{\text{LO}}}\frac{1}{\left(2^{n_{\text{bits}}}\right)^2}\left(\frac{V_{\text{out,max}}}{V_{\text{out,ref}}}\right)^2\right) \tag{6.5}$$

where an additional factor of two is introduced for the quadrature system.

The expected noise performance for various n_{bits} is plotted in Figure 6.20. Realistic values for physical number of bits n_{bits} should not exceed 14 or 15 excluding the sign information. From the figure a performance better than $-168.5\,\text{dBc/Hz}$ for 13 bits can be gathered. This is already more than 10 dB less than the targeted $-157\,\text{dBc/Hz}$ for the entire cancellation RF-DAC, but should also be considered a lower limit on the number of physical bits.

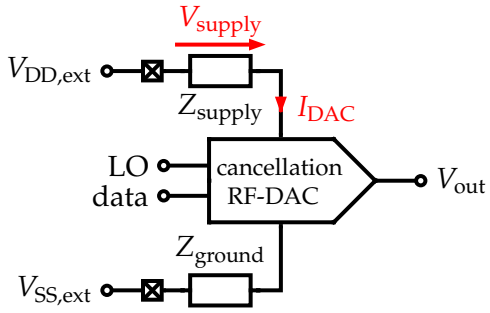


Figure 6.21: Generation of switching noise via the supply impedance in the capacitive cancellation RF-DAC.

6.3.2.3 Switching Noise

Switching noise again is a deterministic undesired signal component as it depends on the DAC's input signal. Mainly the current drawn from the RF-DAC becomes visible in the output voltage via its supply impedance, sketched in Figure 6.21, just like the well known I(L)R-drop. The magnitude and impact of the switching noise is essentially determined by the supply network and regulators, and obviously also by the RF-DAC's current profile. In simulations, the effect of switching noise can be separated, since, for an ideal supply, none of these effects materialize in the output signal [196].

The supply impedance is not only composed from the trace resistances, inductances, and (decoupling) capacitances, but also from the non-ideal impedance presented by supply regulators. Therefore, this is a complicated network that heavily depends on the regulator and the actual physical implementation. Also note that there is an additional impedance on the ground network, but due to the lack of a regulator and judging by prior experience, the dominant portion is on the supply.

6.3.2.4 Device Mismatch and Segmentation

The capacitive RF-DAC relies on intrinsic capacitor matching. Thus, the influence of the capacitor variation has to be accounted for in the DAC performance. Even though the undesired signal components introduced due to

imperfections in the capacitor to capacitor matching are fixed for the individual realizations of the RF-DAC, they can be treated as a pseudo random effect. Essentially, the capacitor mismatch introduces, apart from the low order INL characteristics, high order noise like distortions.

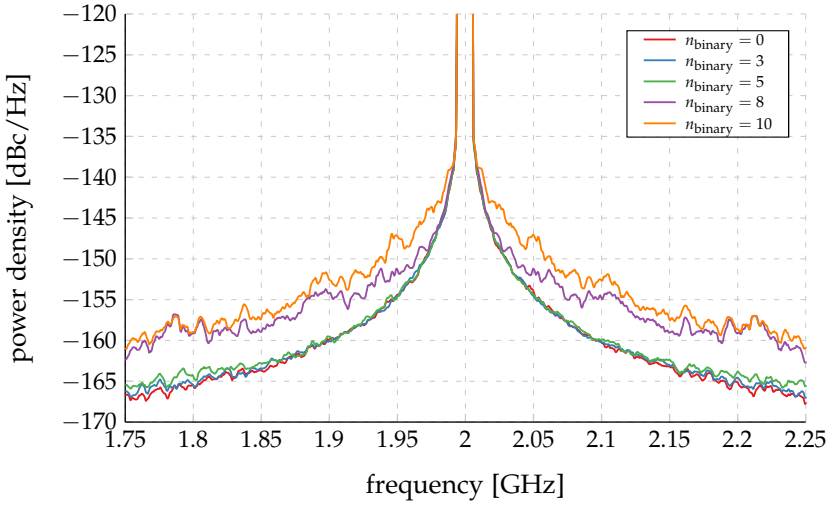
Related to capacitor mismatch is cell array segmentation [179], [197]. In order to further reduce implementation complexity, the DAC is partitioned into two sub-DACs, where one is unary and the other one binary weighted. Essentially, to avoid decoding for and addressing $2^{n_{\text{bits}}}$ cells, only $2^{n_{\text{unary}}}$ are unary weighted, while n_{binary} cells are binary weighted and can directly be addressed. Obviously $n_{\text{unary}} + n_{\text{binary}} = n_{\text{bits}}$.

Applying this topology reduces complexity at the cost of degraded INL and especially differential nonlinearity (DNL) performance [179]. The trade off between complexity and DNL, or n_{unary} and n_{binary}, is essentially determined by the required noise performance and the intrinsic device variations.

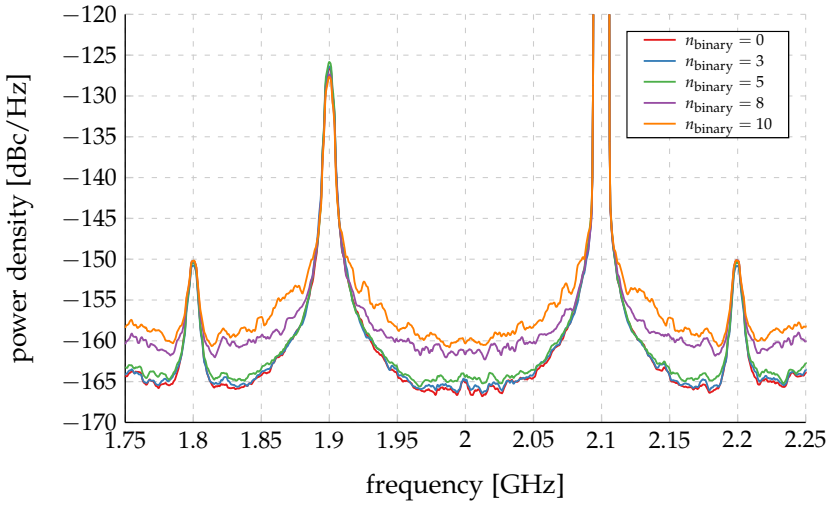
In order to judge the effect of these device variations, model-based Monte Carlo simulations have been performed. The device mismatch depends on the physical area of the capacitors, and eventually on the required capacitor sizes. The targeted value of 3 pF is used for these simulations. Further, the applicable technology parameters for metal capacitor mismatch are employed in the analysis. These simulations also allow for judging the effect of the different options for segmentation, i.e. adequately choosing n_{unary} and n_{binary}.

Figure 6.22 shows representative simulated output spectra for different segmentations with $n_{\text{bits}} = 13$, averaged over 100 runs for each topology. Many more combinations of RX and TX frequencies and signal bandwidths have been analyzed. Note that the spectrum plots focus only on the noise floor, since this is the main concern of these analyses. In Figure 6.23 the respective power densities for various n_{binary} at certain offset frequencies are shown.

Due to the very small total capacitance of only 3 pF, and the resulting high capacitor variation, already quite a degradation in noise performance is exhibited, compared to the ideal quantization noise floor. Also inherently included in these results is the effect of quantization noise. Judging by these simulations, five binary bits are a good compromise between signal performance

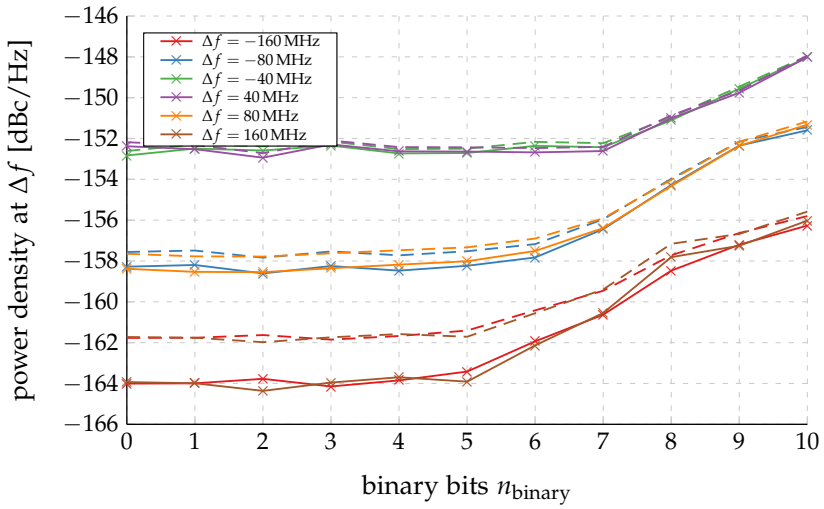


(a) TX LO at $f_{\text{LO}} = 2\,\text{GHz}$, no offset.

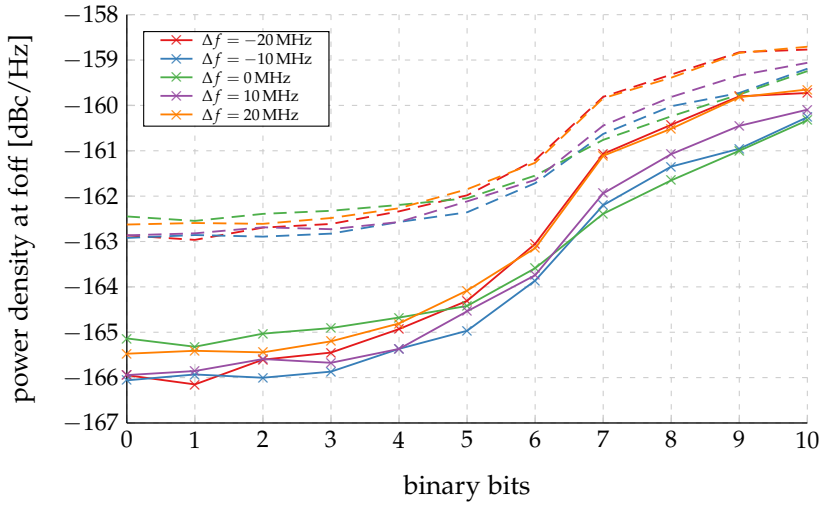


(b) RX LO at $f_{\text{LO}} = 2\,\text{GHz}$, offset equals duplex distance of $f_{\text{TX}} - f_{\text{RX}} = 100\,\text{MHz}$. The mismatch induced I/Q image at 1.9 GHz is 60 dB below the main signal.

Figure 6.22: Simulated output spectra averaged over 100 Monte Carlo runs for various segmentations with a 5 MHz bandwidth signal. Additional smoothing along the frequency axis is applied. The plots are zoomed to the noise floor, which is of interest in these analyses.



(a) TX LO at $f_{\text{LO}} = 2\,\text{GHz}$, no offset.



(b) RX LO at $f_{\text{LO}} = 2\,\text{GHz}$, offset equals duplex distance of $f_{\text{TX}} - f_{\text{RX}} = 100\,\text{MHz}$.

Figure 6.23: Power densities averaged over 100 Monte Carlo runs at different offsets from the respective LOs for various segmentations with a 5 MHz bandwidth signal. The dashed lines indicate the $3 \cdot \sigma$ variation of the power densities.

and circuit complexity, leaving $2^{n_{\text{unary}}} = 256$ unary weighted cells. Especially when using the RX LO, this segmentation appears to be the sweet spot.

6.3.2.5 Noise Budget

Essentially, the total RF-DAC output noise is composed from the previously discussed noise sources.

$$N_{\text{tot}} = N_{\text{th}} + N_{\text{sw}} + N_Q + N_{\text{mm}} \tag{6.6}$$

To achieve the target of $-157\,\text{dBc/Hz}$ at 80 MHz offset, the available noise power is budgeted as follows:

- **Device mismatch**: It is essentially fixed at $-160\,\text{dBc/Hz}$, including quantization noise, due to the very small DAC capacitance, leaving a remaining noise power equivalent to $-160\,\text{dBc/Hz}$ for the other contributors.
- **Switching noise**: The remaining noise contribution is split equally between these two sources, leaving $-163\,\text{dBc/Hz}$ for each of them. This results in supply impedance requirements depending on the DAC's current.
- **Thermal noise**: The residual noise of $-163\,\text{dBc/Hz}$ is again divided: $\frac{3}{4}$ thereof are assigned to phase noise generated by RF-DAC, resulting in a phase noise requirement of $-164.3\,\text{dBc/Hz}$. The remainder, $-169\,\text{dBc/Hz}$, is taken by thermal supply noise.

6.3.3 Circuit Implementation

The capacitive cancellation RF-DAC is, as already mentioned, designed in a 28 nm bulk CMOS technology with a 0.95 V internal supply derived from 1.15 V externally supplied. This section details the circuit level implementation of the discussed DAC, including floorplanning, individual circuit blocks, and physical design.

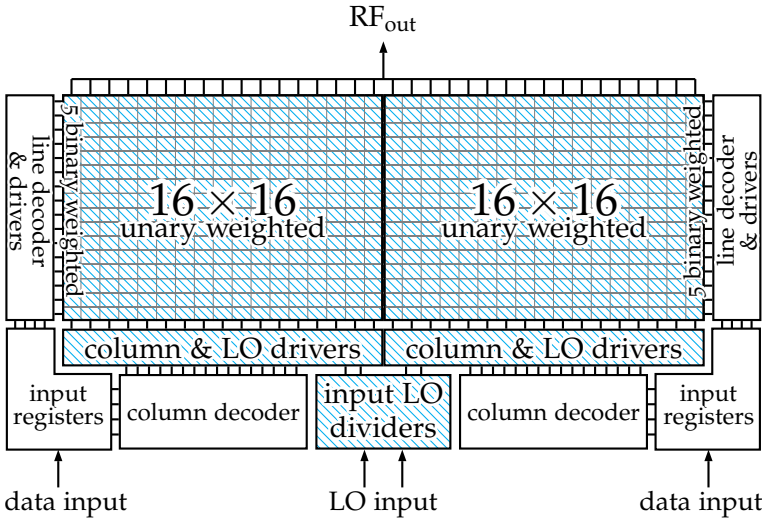


Figure 6.24: Floorplan of the capacitive cancellation RF-DAC. Blocks with noise critical supplies are highlighted.

6.3.3.1 Floorplan

The floorplan of the RF-DAC is shown in Figure 6.24. It consists of two symmetric halves, assigned to the in-phase and quadrature signal components respectively. The RF-DAC is partitioned into the capacitor cell array, an internal LO generation and distribution circuitry, and decoding and control blocks.

6.3.3.2 Capacitor Cell Array

The cell array, which consists of $2^{n_{\text{unary}}} = 256$ unary weighted cells per quadrature phase, is laid out as a 16×16 cell array. This results in 16 lines as well as 16 columns, as sketched in Figure 6.24. The additional $n_{\text{binary}} = 5$ binary weighted capacitor cells are put into a dedicated column at the edges of the array.

There are several signals routed through the cell array as sketched in Figure 6.24. Obviously, this includes the respective LO signals to drive the cells,

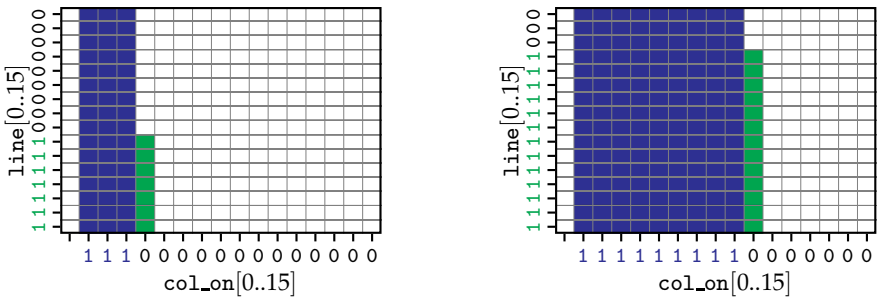


Figure 6.25: Line and column based control signals affecting fully and partially active columns differently in the array. Leftmost column contains the binary weighted cells, which are controlled separately. Only a single phase is shown.

and also the output traces to collect the resulting signal. The LOs are driven individually into the columns of the cell array, allowing some columns to receive an LO signal while others do not. Furthermore, to enable and disable the individual unary weighted cells, there are control signals routed through each column and also all lines.

A certain DAC input code potentially results in several columns being fully active, one column being partially enabled, and the remaining columns being completely off, as sketched in Figure 6.25. The columns fully off are easy to handle: the respective LOs are switched off. Parallel to the LOs, control signals called `col_on`[0..15] are introduced, which are fed into the columns. For fully active columns, these signals are activated, forcing the cells to be sensitive to the LO, i.e. to be active.

To control the number of enabled cells in the partially active column, control signals called `line`[0..15] are routed into the individual lines, perpendicular to the LO signals. The respective `col_on` of that column is inactive, and therefore the active cells are determined by the `line` controls.

Dedicated control signals are routed exclusively to the binary weighted cells, independent of the ones for unary weighted cells.

6.3.3.3 Capacitor Cell

The cells contain the unit capacitors, drivers and the LO gating NAND and NOR gates, as shown before in Figure 6.14. Additionally, a local decoder circuit is needed to generate the actual enabling signal from the `col_on` and `line` controls, as discussed in the previous section. The required logic function is rather simple

$$\texttt{cell\_active} = \texttt{col\_on} \vee \texttt{line} \tag{6.7}$$

The transistor implementation of the cell is shown in Figure 6.26. All gates that are in the signal/LO path are implemented as CMOS gates. Contrary, the logic function of the local decoder is implemented with a modified pass transistor logic that is not connected to any supply rail in the cell array. This is done in order to reduce any currents drawn that are not perfectly proportional to the active number of unary cells as explained later in Section 6.3.4.

The actual LO gates are built as symmetric NAND and NOR gates, to match the rise and fall times of both signal paths. The unused or permanently active devices are tied to the proper potentials by means of a tie circuit. The output driver consists of two staggered inverters which also provide increased isolation in case the cell is switched off.

Finally, the input LO signals are additionally buffered by an inverter. This is done to ensure a constant load on the input LO signal, which is shared amongst all cells in the column. Depending on the number of active cells, the amount of NAND and NOR gates building up conductive channels, and therefore the effective load capacitance on these nodes, varies [198], [199].

Figure 6.27 shows this impact of the number of active cells on the LO phase. The skew of less than a picosecond might seem negligible, but the impact in the output spectrum, close to the signal, is considerable, as shown in Figure 6.28. This effect is aggravates with signal bandwidth, and is especially problematic for low TX-to-RX duplex distances.

In order to avoid this undesired phase modulation of the columns' LO signals, these inverters are placed upfront the actual LO gates. Since the inverters' behavior is not dependent whether cells are active or not, constant loading and therefore code independent delays of the LOs are achieved. Furthermore, the spectral performance is restored as depicted in Figure 6.28 [34].

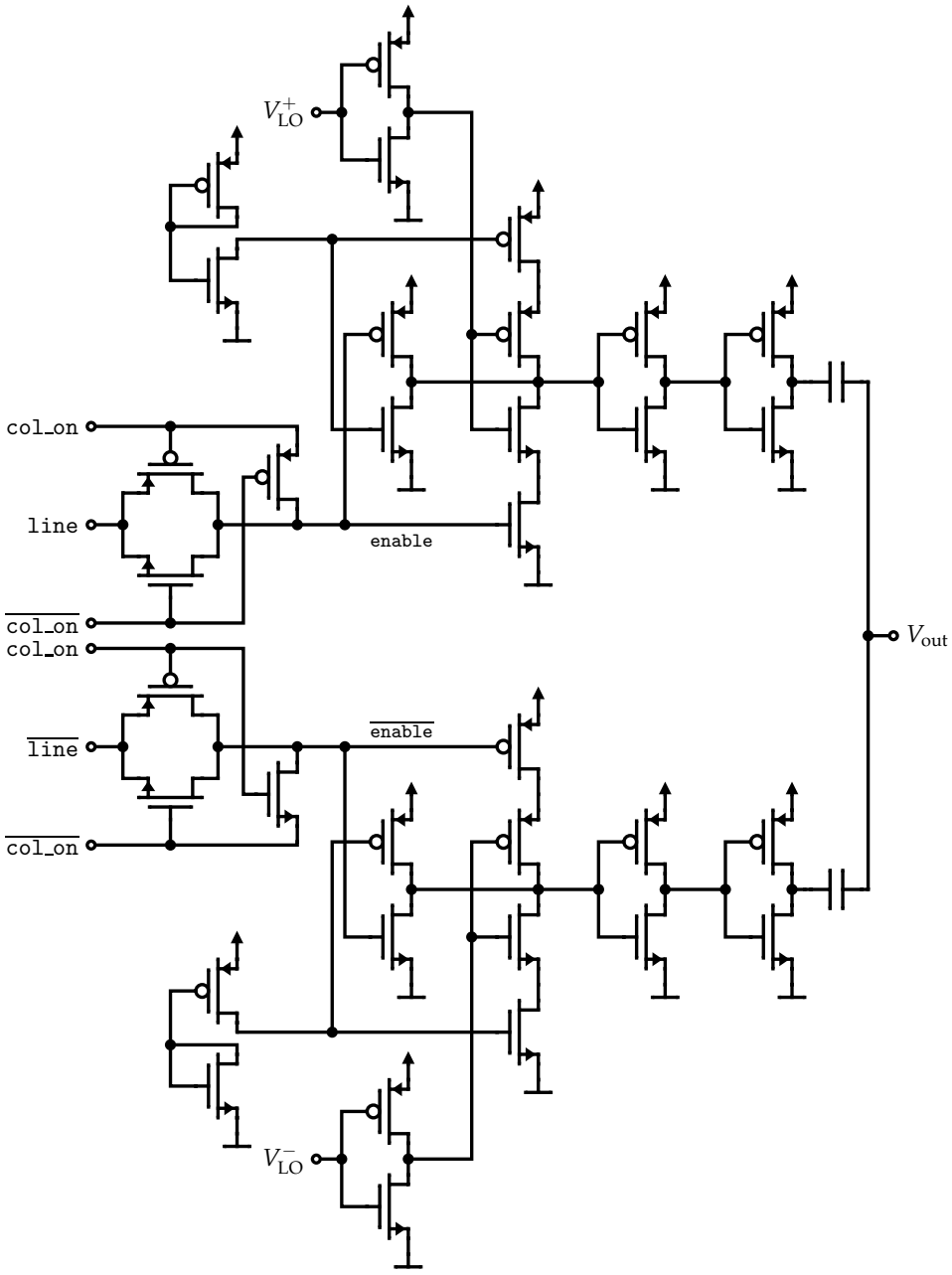


Figure 6.26: Transistor level implementation of the unary capacitor cell.

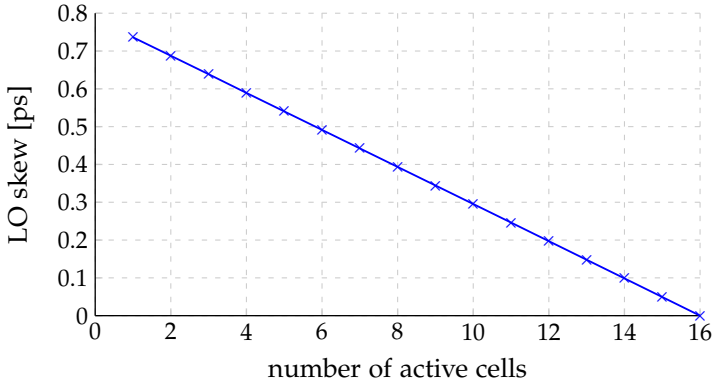


Figure 6.27: Simulated impact on column's LO phase of different number of active cells in a column.

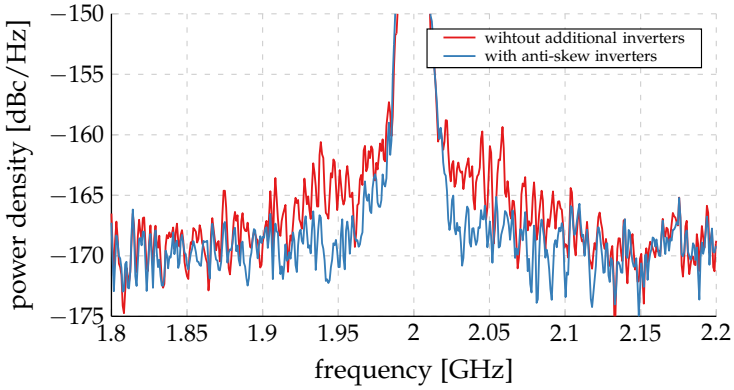


Figure 6.28: Simulated impact on the output spectrum with varying phases on the columns' LOs for a 40 MHz bandwidth signal at $f_{\mathrm{LO}} = 2\,\mathrm{GHz}$.

In addition to the unary weighted cells all having two unit capacitors, two segments of five binary weighted cells are added to the capacitor array for in-phase and quadrature respectively. These segments are essentially two additional columns at the left and right edges of the unary weighted array.

In order to guarantee a perfect temporal alignment with the unary cells, the binary cells are implemented equally. The binary weighted capacitors are essentially geometrically split into two portions. First, the part that is connected

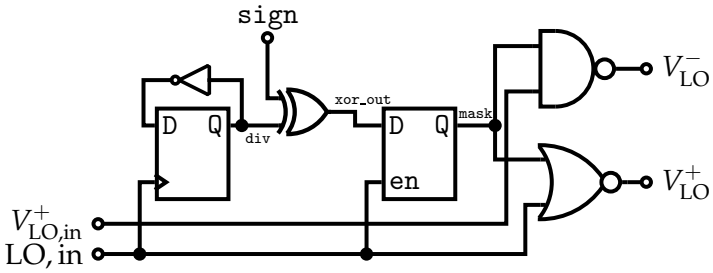


Figure 6.29: Input LO divider and 25 % duty cycle generator.

to the output and contributes to the signal accordingly. Second, the remainder is connected to a fixed potential, e.g. ground, to provide equal loading to the driving inverter and ensure proper temporal alignment [200].

6.3.3.4 Local Oscillator Generation and Distribution

The LO divider and 25 % duty cycle generator is shown in Figure 6.29. It is fed a differential input LO at $2 \cdot f_{LO}$. For the demonstrator an on-chip LO distribution scheme at double the LO frequency was chosen, since it eases the 25 % duty cycle generation.

The divider uses an LO blanking technique [201], [202], where every other LO pulse at $2 \cdot f_{LO}$ is masked, resulting in a 25 % duty cycle LO at f_{LO}. The in-phase and quadrature dividers have their LO inputs swapped. Due to reasons of physical placement in layout, the two phases have split dividers.

The LO divider furthermore also has an input for the sign information fed to the RF-DAC. The polarity of the output signal is determined by the temporal order of the positive and negative cell halves, as discussed in Section 6.3.1.2. In order to swap the precedence of these two LO signals, the blanking signal is inverted depending on the sign information by means of the XOR gate shown in Figure 6.29, providing the desired result. A timing diagram is shown in Figure 6.30.

As obvious from the previous discussion, the positive LO^{+} is active with high potential as it drives NAND gates to generate the positive output pulses.

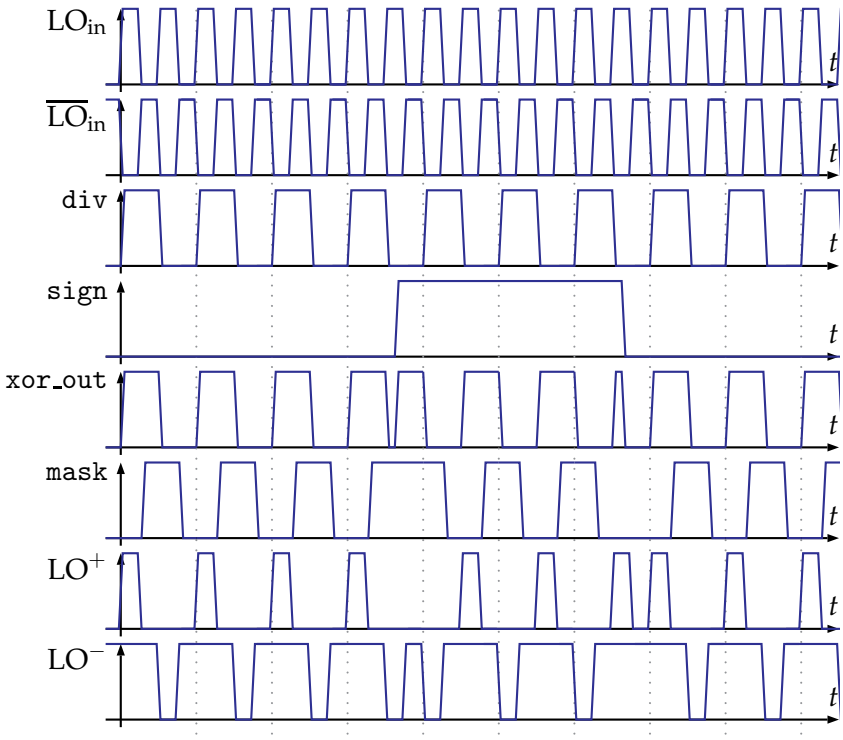


Figure 6.30: Timing diagram of the LO divider and 25 % duty cycle generator.

Contrary, the negative LO^- is active low, driving NOR gates to achieve the negative output.

These LO signals are then distributed along the array horizontally, supplying the individual columns' LO drivers. These drivers are activated on demand, i.e. only when the respective columns actually contribute to the output signal. This way, a considerable amount of power, approximately 0.5 mA per column that is switched off, required by the RF-DAC's LO distribution can be spared. Furthermore, such operation mode is required by the very simple data decoding scheme employed in the cell array, as discussed in Section 6.3.3.2.

The circuit level implementation of the column LO drivers is shown in Figure 6.31. Similarly to the capacitive cells found in the array, a buffer inverter is employed at the LO input. The different number of active LO drivers would

otherwise, depending on the number of columns with active cells, modulate the LO phase of the entire DAC [34]. This results in an undesired amplitude to phase conversion, quantized by the number of cells, resulting in degraded spectral performance. Figure 6.32 shows this effect for the different number of active cells. The effective skew on the LO is quite significant, reaching 6 ps. At $f_{\mathrm{LO}} = 2\,\mathrm{GHz}$, this shift already is more than 4° of phase modulation.

6.3.3.5 Data Path and Decoders

The propagation of amplitude data fed to the RF-DAC is obviously of importance. Due to the high sampling and operating frequencies, which are directly linked to the LO, the design and layout of the involved circuitry is a complicated non-trivial task performed manually. Proper temporal alignment of all control signals and the LOs is of utmost importance. Only the LO signals are designed for the required phase noise performance and symmetry. Therefore, all transitions that propagate to the output of the RF-DAC must be solely triggered by the LOs. Otherwise the phase noise performance cannot be met, and further glitches and other undesired effects may emerge, since the propagation delays of the control signals are not well controlled and generally not matched to the LO other than fulfilling these timing requirements, i.e. changing only when the respective LO signal is inactive.

The essential stages of the data path are sketched in Figure 6.33. The names of the functional blocks generally match the ones as denoted in the floorplan in Figure 6.24.

The first register stage in the data path is used to obtain data from the upsampler already at the LO rate. The clock used for these registers is also derived from the LOs fed to the RF-DAC, and further passed onto the sample rate converter. This clock is shared between the in-phase and quadrature portions of the DAC. All further stages use clocks matching the LO phase, generated in the input LO dividers. E.g. there are both in-phase and quadrature versions of the RF-DAC's digital clock.

The second register stage is used for the clock domain crossing, to synchronize the data stream to the respective phase, either in-phase or quadrature.

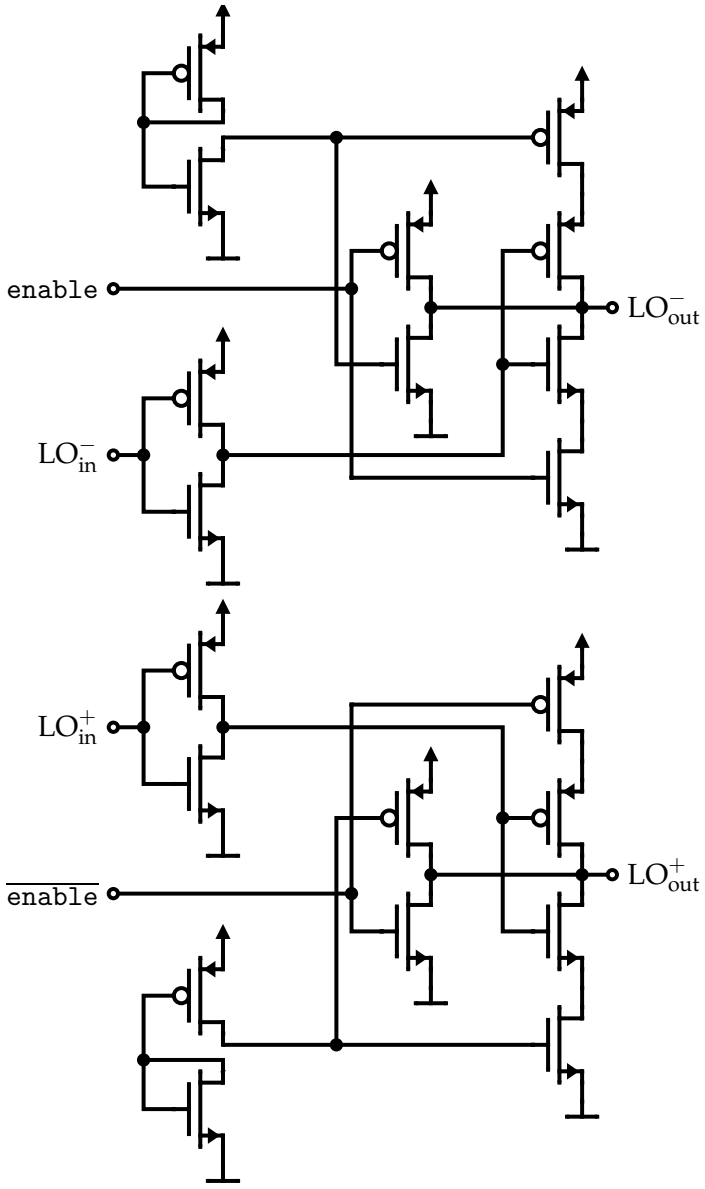


Figure 6.31: Transistor level implementation of the column LO driver.

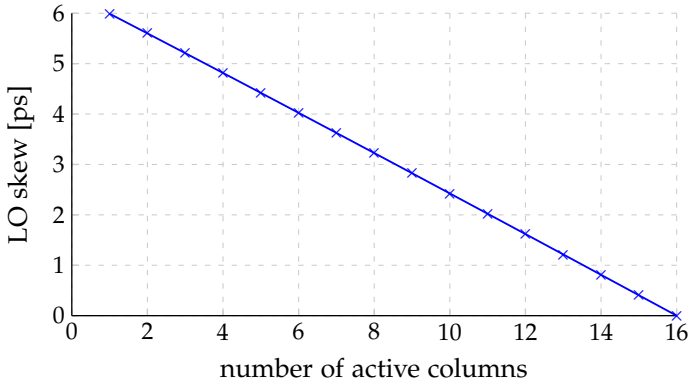


Figure 6.32: Simulated impact on the RF-DAC's LO phase of different number of active column drivers without the additional buffer inverter.

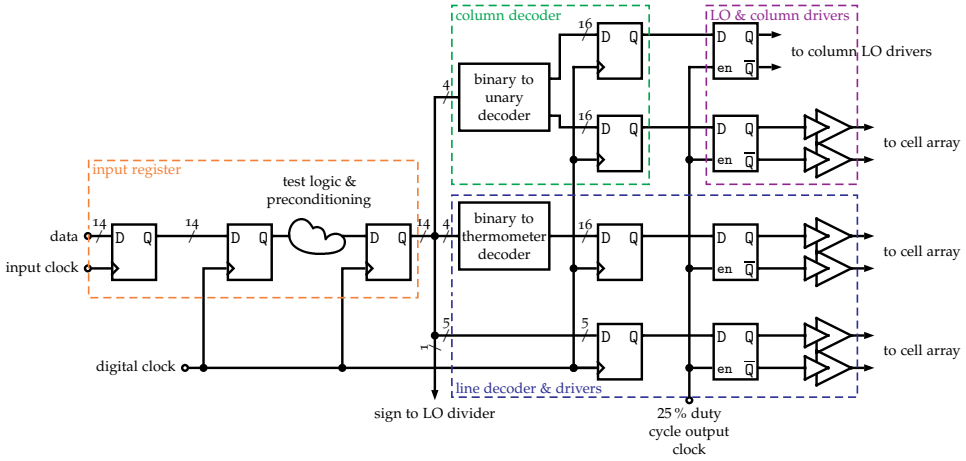


Figure 6.33: Essential stages in the data path of the cancellation RF-DAC, sketched only for one phase.

Preceding test and preconditioning logic and another register stage, the binary encoded data signals are distributed along the outsides of the cell array through the decoders. There the binary data are decoded to the unary weighted or thermometric signals used in the cell array, as explained in Section 6.3.3.2.

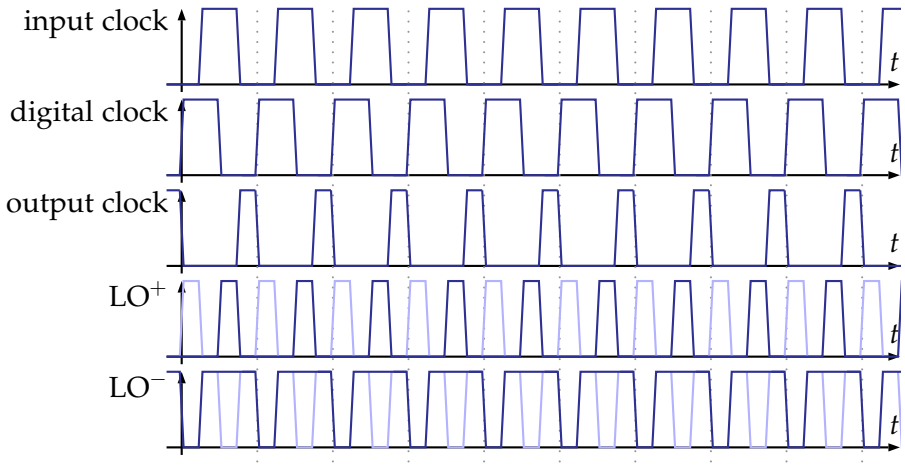


Figure 6.34: Timing diagram of the RF-DAC's clocking scheme.

Finally, these signals are fed to latches, which are enabled with a special 25 % duty cycle clock. These latches are only transparent while the respective LOs fed to the array are inactive and the control signals in the array can change. With the chosen LO scheme discussed in Section 6.3.1.2, this is only the case for $\frac{T_{LO}}{4}$, reflected by the 25 % duty cycle of this very clock.

This scheme is also inherently independent of the polarity of the sign and the temporal order of the LO signals. A timing diagram of the clocking scheme is shown in Figure 6.34.

6.3.4 Supply Concept and Domains

The supply voltage of the capacitive RF-DAC simultaneously also acts as its reference as discussed previously in Section 6.1.2. This is not different for the capacitive cancellation RF-DAC. Therefore utmost care has been taken on two supply related topics: First, the concept of the supplies, i.e. the required supply domains, and second, the necessary supply quality, e.g. achieved by voltage regulation.

Intuitively, the capacitive RF-DAC generally has two different supply domains that need to be separated: A digital supply for the DAC's data path

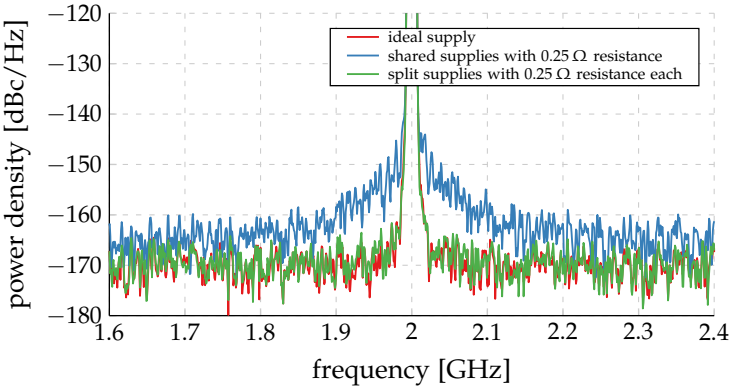


Figure 6.35: Simulated output spectra with shared and split supply connections of the cell array and LO distribution with ideally resistive supplies for a 40 MHz bandwidth signal at $f_{\mathrm{LO}} = 2\,\mathrm{GHz}$.

and decoding. Further, to isolate the sensitive portions of the circuit from the switching ripple and digital currents, an analog supply with good noise performance and negligible disturbances is required. This is especially critical for the capacitor cell array. Further, such supply properties are also needed for the phase noise critical path of the LO distribution internal to the RF-DAC. These critical blocks are already highlighted in the floorplan shown in Figure 6.24.

A simple approach is to have one common analog supply for both the cell array and the LO distribution, as both portions require low noise supplies. This supply domain scenario is sketched in Figure 6.24 with the noise critical blocks highlighted. Unfortunately, this is an unfeasible approach, as the simulation based analyses reveal. Exemplary, the spectra, focused on the noise floor, with an ideal and a resistive shared supply are shown in Figure 6.35.

Essentially, there are two reasons for this behavior: The current drawn by the column LO drivers has a digital-like profile, since there is quite some switching activity on this supply when the individual buffers are activated and disabled. Otherwise the current follows the absolute value of input code, like the cell array, but quantized with the number of columns, i.e. with four bits in this implementation. Contrary, the current drawn by the cell array is quantized with the number of cells, i.e. eight bits. This additional current

quantization noise and the high frequency noise of the switching activity heavily degrade the spectral performance [34].

The other reason is the aggravated modulation of the LO phase through this very supply. The currents from the LO distribution and the cell array both cause a voltage drop via the supply impedance, causing this undesired effect. Essentially it is a nonlinear amplitude to phase conversion, adding to the degradation of spectral performance.

To solve this issue, these two supplies are split and regulated individually. By means of separate supplies for the cell array and the LO distribution, the spectral performance can be restored, as exemplary shown for a single LO frequency and signal in Figure 6.35.

Furthermore, Figure 6.36 shows the smoothed voltages for split and shared supplies. With these plots, the performance degradation is clearly visible, observing the disturbances caused by the quantized current profile of the LO drivers.

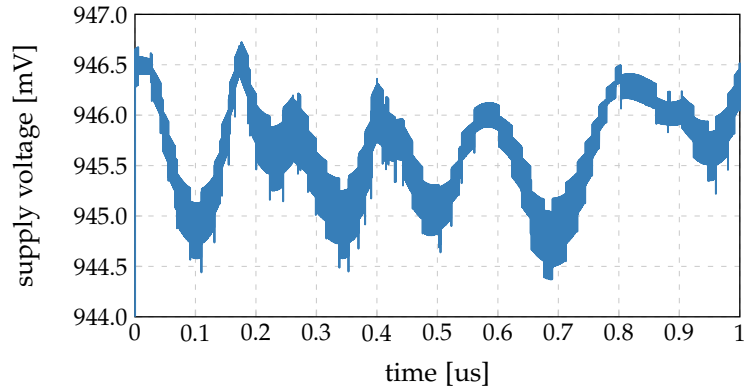
Essentially, three supply domains, with individual requirements on their quality and regulation are needed:

- digital portions of the RF-DAC
- cell array
- LO distribution and drivers

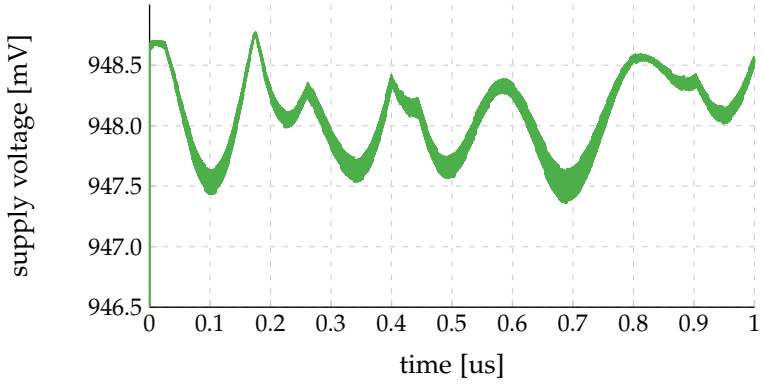
Figure 6.37 shows an updated floorplan of the cancellation RF-DAC reflecting the individual supply domains. In the following section the requirements on these supplies are discussed.

6.3.5 Supply Quality and Regulation

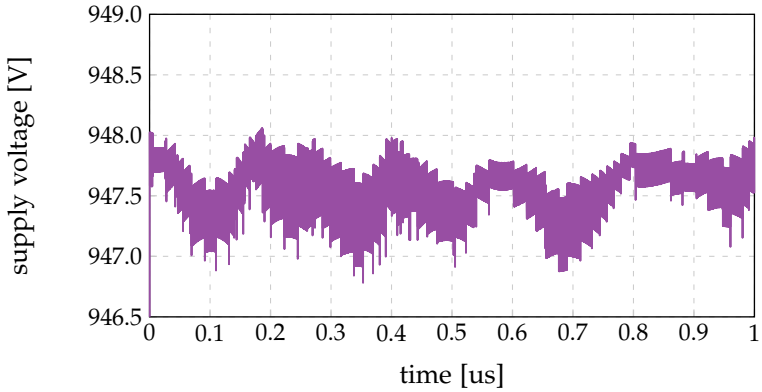
The issue of required supply domains is covered in the previous section. In this section, the requirements on their quality and the respective regulation, are discussed.



(a) Shared supply voltage.



(b) Separate supplies: cell array.



(c) Separate supplies: LO distribution.

Figure 6.36: Smoothed time domain voltages for shared and split supplies.

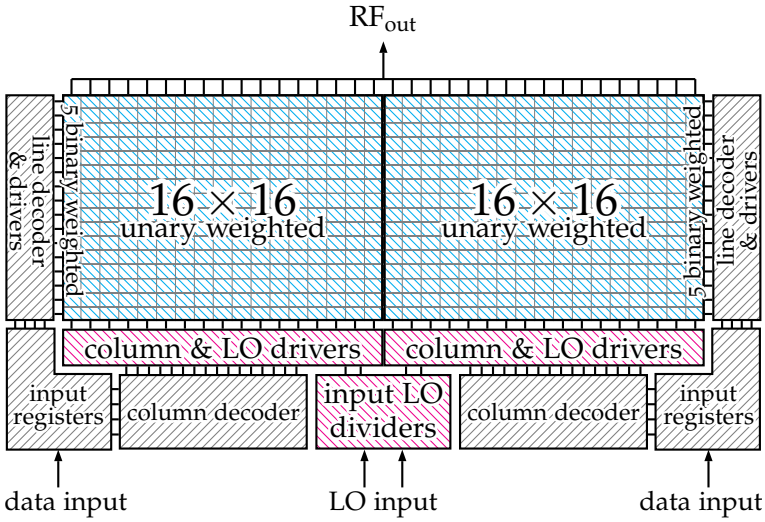


Figure 6.37: Floorplan of the capacitive cancellation RF-DAC highlighting the individual supply domains. Blue: capacitor cell array, red: LO distribution and drivers, and gray: general digital blocks.

6.3.5.1 Digital Supply

The supply of the digital portions is the least sensitive of the RF-DAC's supplies. There is no direct connection to any of the noise critical signals. Essentially, a stable voltage with sufficiently low IR-drop is required, to guarantee error-free operation of all the logic blocks.

On the demonstrator, this supply is directly supplied externally. There is no dedicated supply regulator on the chip, but a substantial amount of decoupling capacitances to stabilize this supply voltage.

6.3.5.2 Cell Array

The cell array has the most sensitive supply in this SIC system. It is connected to the output of the RF-DAC by means of inverters driving the capacitors, essentially acting as switches. In order to understand the requirements on

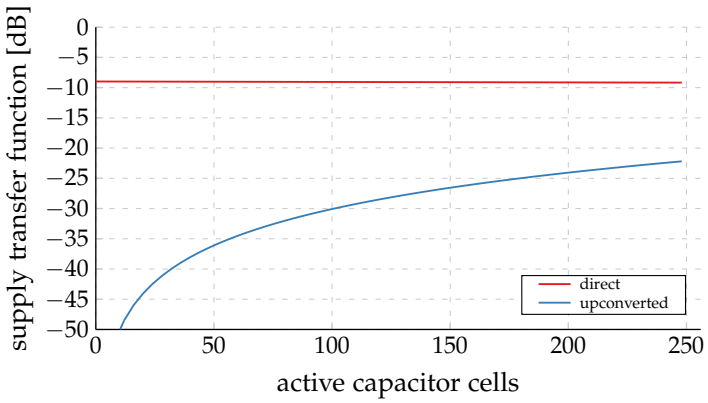


Figure 6.38: Periodic steady state analysis of the supply transfer function to the output signal for the direct and upconverted signal portions at 100 MHz offset.

the needed regulation of this supply, its impact on the output signal needs to be evaluated.

As the RF-DAC acts as an upconverting system, there are two possibilities the supply voltage influences the output signal: First, disturbances present in the frequency span of interest, e.g. in vicinity of the LO frequency, are also visible on the output. Second, the supply voltage is also sampled and upconverted by the RF-DAC operation, where essentially disturbances in the baseband, i.e. around 0 Hz, are translated to the LO frequency [196], [203].

To identify the dominant contribution for the cancellation RF-DAC, periodic steady state analyses are performed. The number of active cells, i.e. the input code of the DAC, is varied in this analysis. Both contributions, the direct feedthrough and the upconverted portion, are depicted in Figure 6.38.

These analyses reveal that the direct feedthrough, neglecting any frequency translation, is the dominant portion of the supply distortion seen at the output. Not only that, there is virtually no dependency on the number of active DAC cells. This is a result of the employed single-ended capacitor cell architecture, where essentially the average capacitance in each LO period connected to either supply rail is independent of the input code.

Contrary, the contribution that is upconverted from the baseband is linearly (in amplitude) dependent on the number of active capacitor cells. When as-

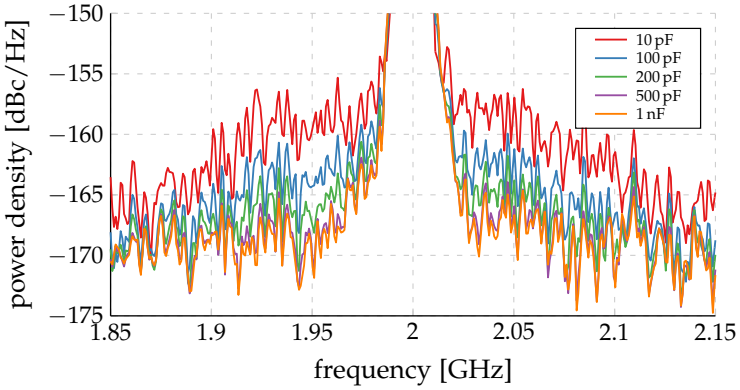


Figure 6.39: Simulated output spectra with an RLC supply network with different values of the decoupling capacitance for a 40 MHz bandwidth signal at $f_{LO} = 2\,GHz$.

suming a PAPR of approximately 6 dB at 3 dB backoff, the contribution by frequency translation is 20 dB or further below direct feedthrough.

Concluding this result, the main supply disturbances degrading the output signal in vicinity to the LO frequency are a result of direct feedthrough. For the targeted operating frequency of $1.4 \sim 2.7\,GHz$, the most viable means for a clean supply voltage is its decoupling capacitance. Proper regulation with active circuitry for the required currents at these frequencies is impractical if not impossible in the given CMOS technology.

With the help of further simulation based analyses, a minimum value for the required decoupling capacitance of the cell array supply is estimated. A portion of this capacitance can be placed directly in the individual capacitor cells, e.g. as MOS-transistor based capacitors. The bigger portion of capacitors needs to be placed outside the capacitor array, spread along its border. Figure 6.39 shows the output spectra for various values of the decoupling capacitance for one example combination of LO frequency and signal bandwidth. Judging by the executed analyses, a minimum decoupling capacitance of 200 pF is required for this cancellation RF-DAC implementation.

Furthermore a readily available low bandwidth and low noise low-dropout regulator (LDO) is used for active supply regulation, i.e. to set the DC value and to provide some supply rejection. It is an already existing design focus-

ing on low power and low noise operation and not further detailed in this work.

6.3.5.3 Local Oscillator Distribution

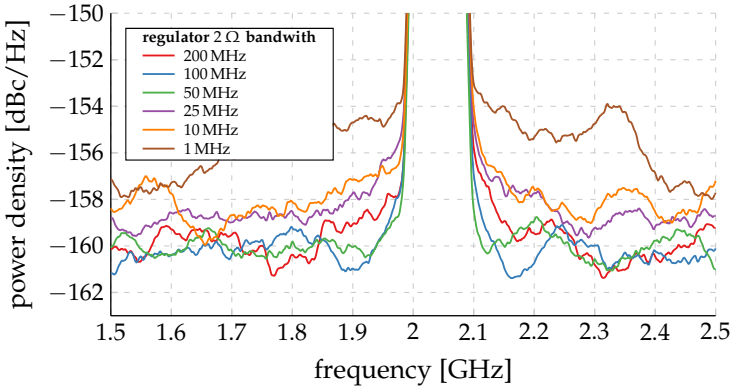
The other analog supply is also critical in terms of noise and disturbances. Any noise on this LO distribution supply will directly convert to phase noise via the LO drivers. Any disturbances, such as undesired or injected tones, will directly convert to spurs on the LO and eventually modulate with the RF-DAC signal and compromise the spectral performance.

Furthermore, sufficient load regulation is essential to mitigate the modulation of the LO phase previously discussed in Section 6.3.4. The dynamic input signal dependent voltage drop across the supply impedance is proportional to the load current, which in turn depends on the number of active LO dividers. Since this number essentially changes with the DAC's input signal, fast dynamics are to be expected regarding this variable load current.

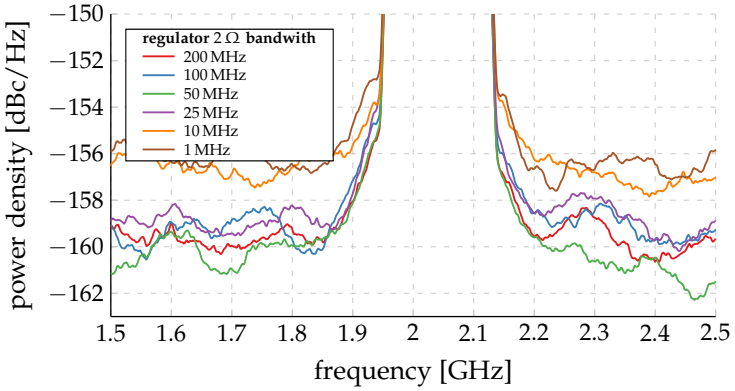
To mitigate this issue, a linear supply regulator covering this signal bandwidth is employed. To evaluate the requirements on the regulator load regulation, simulation based analyses for different RF-DAC signal bandwidths are performed. An idealized LDO model is used with varying regulation bandwidth, although the frequency, where the output impedance exceeds 2 Ω, is observed. Such output impedance curves are shown in Figure 6.40c. Additionally to the single-pole characteristics of the regulator, its output impedance is limited to 5 Ω, accounting for the pass device's drain-to-source impedance. Furthermore, a parallel capacitance is added, acting as the decoupling capacitance.

The regulation bandwidth mostly influences the noise floor of the DAC. Shown in Figure 6.40 are the output spectra for two signal bandwidths, 20 MHz and 100 MHz. For 100 MHz signal bandwidth, the regulator's output impedance must be below 2 Ω up to at least 10 MHz and 25 MHz to not significantly degrade the noise floor for 20 MHz and 100 MHz signal bandwidths respectively.

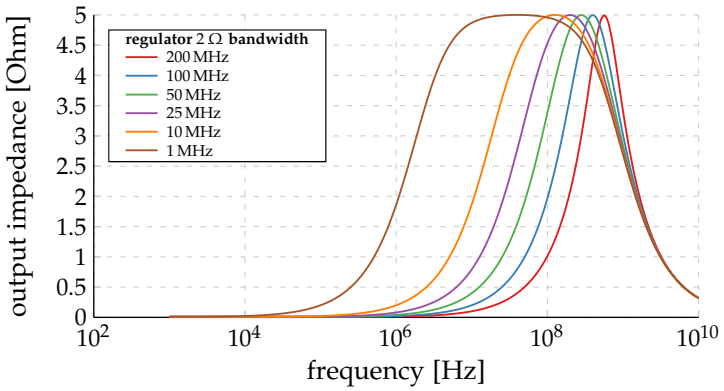
To cover most of the SIC scenarios, also accounting for frequency shifts implying higher effective signal bandwidths, a bandwidth of roughly 100 MHz



(a) Output spectra for 20 MHz signal bandwidth.



(b) Output spectra for 100 MHz signal bandwidth.



(c) Idealized LDO output impedances.

Figure 6.40: Simulated and smoothed output spectra for a 2 GHz LO frequency with an idealized LDO regulator with different regulation bandwidths on the RF-DAC's LO distribution supply.

with an output impedance lower than approximately $2\,\Omega$ is required of this high bandwidth LDO. The design of the employed high bandwidth LDO is detailed in Section 6.4.

6.4 Ultra-High Bandwidth Low-Dropout Regulator

As reasoned in Section 6.3.5.3, a dedicated high bandwidth LDO for the cancellation RF-DAC's LO distribution's supply is required. The goal is to provide superior load regulation, a low output impedance, and ultra high regulation bandwidths.

The specification of the regulator includes:

- Line voltage (power rail): $1.15\,\mathrm{V} \pm 5\,\%$
- Output voltage: $0.95\,\mathrm{V}$
- Minimum load current: $0\,\mathrm{mA}$
- Maximum load current: $15\,\mathrm{mA}$
- Worst case phase margin: $> 45^\circ$ in all specified cases
- Output impedance: $< 0.5\,\Omega$ up to $10\,\mathrm{MHz}$ and $< 2\,\Omega$ up to $100\,\mathrm{MHz}$ for load currents above $5\,\mathrm{mA}$
- External load capacitance: none, no additional external connections
- Internal load capacitance: $\leq 100\,\mathrm{pF}$, lower preferred due to area restrictions

6.4.1 Flipped Voltage Follower

LDOs published in literature with similar performance [204]–[206], especially in terms of regulation bandwidth, rely on the principle structure of the flipped voltage follower (FVF) [207], [208]. The essential FVF-based LDO circuit topology is shown in Figure 6.41.

The LDO structure employs two loops: A slow loop potentially having high gain but small bandwidth that sets the bias potential V_B and therefore also the output voltage V_{out}. The second loop is composed by the pass device M_P and the CG amplifier M_C. This second loop is designed to be a fast loop, with

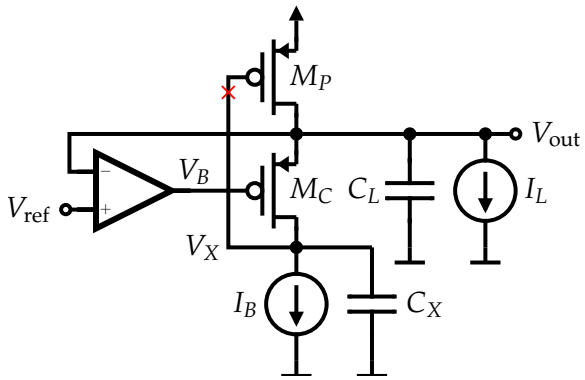


Figure 6.41: Principal FVF-based LDO circuit structure.

lower gain but large bandwidth, providing the desired voltage regulation at high frequencies.

For stability considerations of the regulator it can be assumed that only the fast loop is of interest. If designed correctly, the slow bias loop has no gain at the frequencies of interest and therefore has no influence on the stability of the entire regulator. In the following, only the fast loop is considered in the stability analysis, and the bias potential V_B is considered as constant.

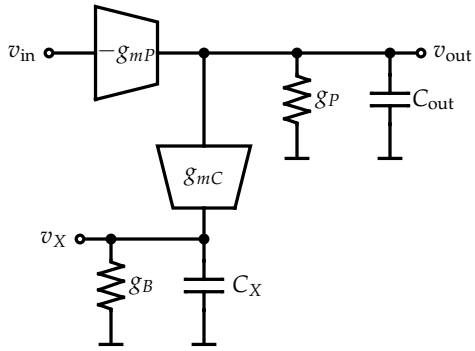
The respective transconductance model is shown in Figure 6.42a and the small signal equivalent circuit model in Figure 6.42b. The capacitor C_X not only accounts for parasitic capacitance at this node, but also includes the gate capacitance of the pass transistor M_P (or the input capacitance of any buffer circuit driving it). The open loop transfer function derived from the equivalent small signal circuit model is

$$\frac{v_X}{v_{\text{in}}} = -A_{\text{DC}} \cdot \frac{1 + \frac{s}{z_1}}{1 + \frac{s}{p_1} + \frac{s^2}{p_2}} \tag{6.8}$$

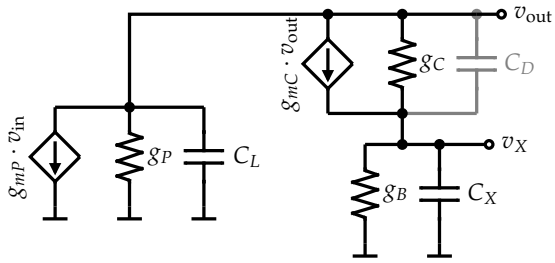
$$A_{\text{DC}} = \frac{g_{mP}g_{mC} + g_{mP}g_C}{g_P g_B + g_{mC}g_B + g_C g_B + g_P g_C}$$

$$z_1 = \frac{g_{mC}g_C}{C_D}$$

$$p_1 = \frac{g_P g_B + g_{mC}g_B + g_C g_B + g_P g_C}{C_L(g_B + g_C) + C_D(g_B + g_P) + C_X(g_P + g_{mC} + g_C)}$$



(a) Transconductance model.



(b) Small signal model.

Figure 6.42: Equivalent linearized circuit models of the FVF circuit shown in Figure 6.41, where the red cross indicates where the loop is broken.

$$p_2 = \frac{g_P g_B + g_{mC} g_B + g_C g_B + g_P g_C}{C_L C_X + C_L C_D + C_X C_D}$$

Similarly, the open loop transfer function derived from the transconductance model is a simplified version as

$$\frac{v_X}{v_{in}} = -\frac{g_{mC} g_{mP}}{g_B g_P + g_B g_{mC}} \cdot \frac{1}{\left(1 + \frac{s}{\frac{g_B}{C_X}}\right)\left(1 + \frac{s}{\frac{g_P + g_{mC}}{C_L}}\right)} \tag{6.9}$$

As seen from the equations, especially from (6.9), the FVF-based LDO regulator is a two pole system. One of the poles is associated with the output node, which usually is the dominant one due to the large load capacitance C_L at the LDO output. The other pole is related to the output of the CG amplifier M_C, which is driving the gate of the pass device M_P. An exemplary bode plot is sketched in Figure 6.43.

Such a two pole system is prone to have stability issues, which is the case for the targeted specification in the given technology. One possibility to move the second pole at v_X to higher frequencies, is to insert a high bandwidth buffer driving the pass device gate, reducing the effective C_X. But also the insertion of a PMOS source follower, dubbed buffered FVF-based LDO in literature, did not achieve the necessary relief to obtain more than 45° of

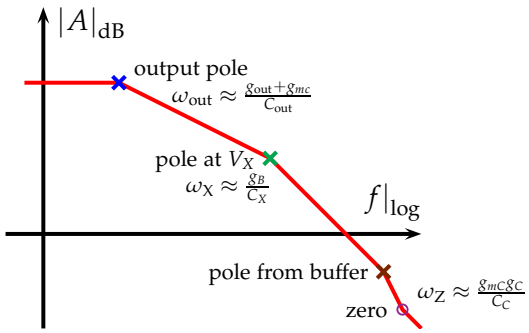


Figure 6.43: Exemplary bode plot of the FVF-based LDO circuit structure.

phase margin with reasonable bias currents. To overcome this shortcoming, a novel frequency compensation scheme for FVF-based high bandwidth LDO regulators is introduced in the next section.

6.4.2 Frequency Compensation Schemes

In order to improve the stability of the buffered FVF-based LDO, a feed-forward path is added, bypassing the output node and the dominant pole associated with it. The application of this frequency compensation principle to buffered FVF-based LDOs is sketched in Figure 6.44 [209]. The feed-forward transconductance g_{mF} obtains the signal at the pass transistor's gate M_P and directly injects a current into node V_X, essentially bypassing the output node V_{out}.

The proposed frequency compensation can be implemented in two variants, depending on how the bias points are maintained. The first approach, shown in Figure 6.45a, capacitively couples the input of the feed-forward transconductance g_{mF} and directly injects into node V_X. Alternatively, the second option is to capacitively couple the output of the feed-forward transconductance g_{mF} and directly connect its input as sketched in Figure 6.45b.

These differences allow for distinct circuit implementation possibilities and slightly different stability behavior. The two approaches are discussed and analyzed in the following sections.

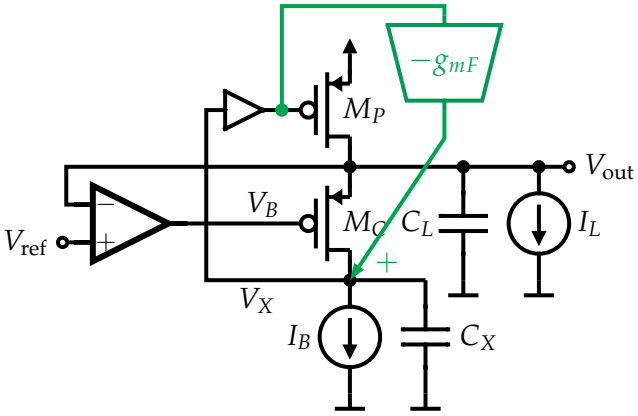
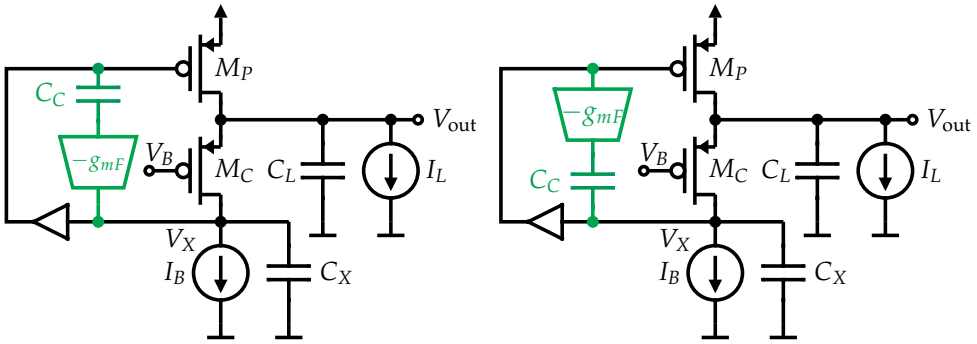


Figure 6.44: Buffered FVF-based LDO circuit structure with the introduced feed-forward transconductance g_{mf} bypassing the output node V_{out}.



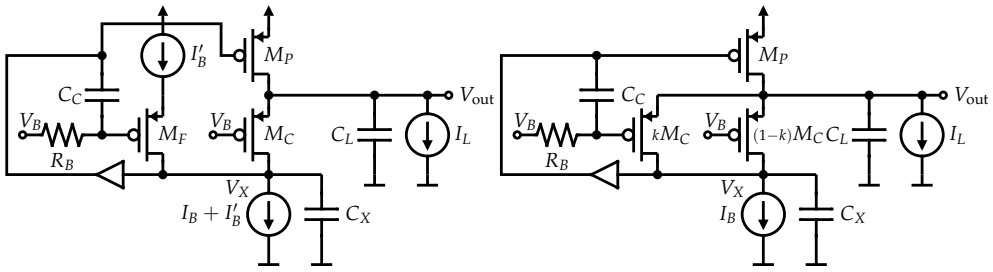
(a) Capacitively coupled input.

(b) Capacitively coupled output.

Figure 6.45: Different implementation possibilities of the proposed frequency compensation scheme depending on how the feed-forward transconductance g_{mf} is coupled.

6.4.2.1 Capacitively Coupled Input

Possible circuit implementations of the compensation approach sketched in Figure 6.45a are shown Figure 6.46. The first approach, shown in Figure 6.46a, introduces a replica transistor M_F of CG amplifier M_C which is directly coupled to node V_X. The bias current needs to be provided by current source I'_B. The gate potential is reused as V_B, set by the low frequency bias loop. The



(a) Dedicated feed-forward transistor M_F. (b) Current reuse architecture.

Figure 6.46: Different transistor level implementations of the proposed frequency compensation scheme having the feed-forward transconductance g_{mF} capacitively coupled at its input.

gate potential is coupled capacitively onto the gate of M_F by means of C_C and the bias resistor R_B, which decouples the gate from the bias voltage V_B.

The second approach, sketched in Figure 6.46b, reuses a portion k (with $0 < k \leq 1$) of the CG amplifier M_C. The portion of M_C that is used in the feed-forward path is similarly biased with R_B and capacitively coupled via C_C to the pass device gate. A distinct advantage of this current reuse implementation is that no additional bias currents needs to be introduced and therefore there is no drawback in power consumption and current efficiency.

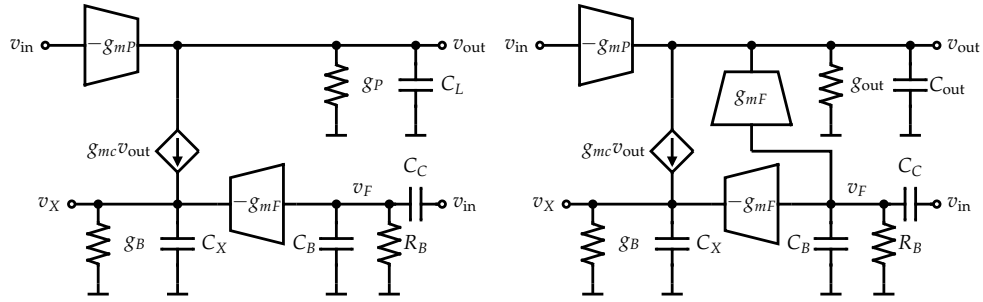
While the two approaches are similar enough, there are slight differences in their frequency behavior. The respective transconductance models are shown in Figure 6.47. Essentially, the difference between the two is the additional g_{mF} in the current reuse implementation.

The resulting open loop transfer characteristics, for the case of the dedicated transistor M_F depicted in Figure 6.47a, are

$$\frac{v_X}{v_{\text{in}}} = -A_{\text{DC}} \cdot \frac{1 + \text{s}\,\zeta_1 + \text{s}^2\,\zeta_2}{\left(1 + \frac{\text{s}}{p_1}\right)\left(1 + \frac{\text{s}}{p_2}\right)\left(1 + \frac{\text{s}}{p_3}\right)} \tag{6.10}$$

$$A_{\text{DC}} = \frac{g_{mP} g_{mC}}{g_B (g_P + g_{mC})}$$

$$\zeta_1 = R_B \left(C_B + C_C + C_C \frac{g_{mF}(g_P + g_{mC})}{g_{mP} g_{mC}} \right)$$



(a) Dedicated feed-forward transistor M_F.

(b) Current reuse architecture.

Figure 6.47: Equivalent linearized transconductance models of the two possibilities of the proposed frequency compensation scheme having the feed-forward transconductance g_{mf} capacitively coupled at its input.

$$\zeta_2 = R_B \frac{g_{mF} C_C C_L}{g_{mP} g_{mC}}$$
$$p_1 = \frac{g_P + g_{mC}}{C_L}$$
$$p_2 = \frac{g_B}{C_X}$$
$$p_3 = \frac{1}{R_B (C_B + C_C)}$$

and similarly, for the current reuse case,

$$\frac{v_X}{v_{in}} = -A_{DC} \cdot \frac{1 + s\,\zeta_1 + s^2\,\zeta_2}{\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right)\left(1 + \frac{s}{p_3}\right)} \tag{6.11}$$
$$A_{DC} = \frac{g_{mP} g_{mC}}{g_B (g_P + g_{mC})}$$
$$\zeta_1 = R_B \left(C_B + C_C + C_C \frac{g_{mF} g_P}{g_{mP} g_{mC}} \right)$$
$$\zeta_2 = R_B \frac{g_{mF} C_C C_L}{g_{mP} g_{mC}}$$
$$p_1 = \frac{g_P + g_{mC}}{C_L}$$

$$p_2 = \frac{g_B}{C_X}$$
$$p_3 = \frac{1}{R_B(C_B + C_C)}$$

Essentially, the difference between the two implementations is within the term ζ_1.

A more detailed transfer function can be derived from the full blown small signal equivalent circuit model. Unfortunately, due to the increased circuit complexity, there is hardly any insight gained from these heavily cluttered expressions. Therefore, they are not repeated herein this analysis.

The effect of the frequency compensation can already be seen by the transconductance models. Compared to the original open loop transfer function, an additional pole $p_3 \approx \frac{1}{R_B(C_B+C_C)}$ is introduced. This pole is associated with node v_F in Figure 6.47, a result of the coupling circuitry for M_F or $k \cdot M_C$ respectively, which does obviously not exist in the original circuit. The frequency location of p_3 is effectively chosen with the value of R_B, assuming that C_B, which incorporates the gate capacitance of M_F and the parasitic capacitance of this node, is determined by other factors, e.g. layout.

Furthermore, and more importantly, two additional zeros are introduced, which can be used to stabilize the circuit. Assuming that the two zeros are sufficiently separated in frequency and that $C_B \ll C_C$, they can be approximated as

$$z_1 \approx \frac{1}{\zeta_1} \tag{6.12}$$
$$= \frac{1}{R_B(C_B + C_C) + R_B C_C \frac{g_{mF}(g_P+g_{mC})}{g_{mP}g_{mC}}}$$
$$z_2 \approx \frac{\zeta_1}{\zeta_2} \tag{6.13}$$
$$= \frac{g_{mP}g_{mC}}{g_{mF}C_L} + \frac{g_P + g_{mC}}{C_L}$$

for the dedicated feed forward transistor M_F. Similarly, for the current reuse approach, this approximation is very similar

$$z_1 \approx \frac{1}{\zeta_1} \tag{6.14}$$

$$\begin{aligned} & = \frac{1}{R_B(C_B + C_C) + R_B C_C \frac{g_{mF} g_P}{g_{mP} g_{mC}}} \\ z_2 \approx & \frac{\zeta_1}{\zeta_2} \\ & = \frac{g_{mP} g_{mC}}{g_{mF} C_L} + \frac{g_P}{C_L} \end{aligned} \tag{6.15}$$

In both cases, z_1 is at lower frequencies compared to p_3 and can be potentially exploited to gain several degrees of phase margin. The second zero z_2 incorporates the output pole frequency p_1 and a term $\frac{g_{mP}}{C_L}$ scaled by the ratio of the feed forward and CG transconductances $\frac{g_{mC}}{g_{mF}}$, which essentially moves this zero's frequency.

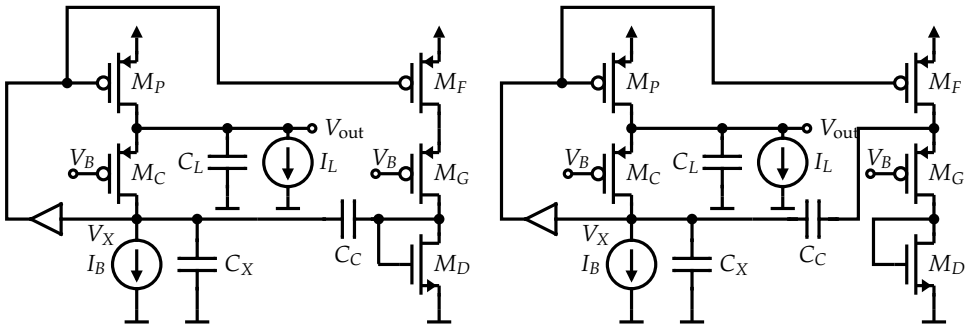
6.4.2.2 Capacitively Coupled Output

Transistor level implementations of the alternative compensation approach, capacitively coupling the feed forward transconductance's output, sketched in Figure 6.45b, are shown Figure 6.48. A replica feed forward transistor M_F, practically consisting of few fingers of the pass device used as a sensing device, is introduced including a replica CG amplifier M_G and a diode connected dummy load M_D.

The two different implementations differ only in the node that is injected into V_X. The current through the replica path is load current dependent in either implementation. The pass transistor gate potential is directly fed to M_F, which also defines the current through this branch.

The simplified transconductance model for the implementation shown in Figure 6.48b is sketched in Figure 6.49. The analysis of the alternative implementation as shown in Figure 6.48a yields a qualitatively identical result and is skipped here.

M_G and M_D can be approximated as $\frac{1}{g_{mG}}$ seen from M_F. The respective open loop transfer function is derived, when incorporating this conductance g_{mG}



(a) Cascoded feed forward signal. (b) Direct feed forward signal.

Figure 6.48: Different transistor level implementations of the proposed frequency compensation scheme having the feed-forward transconductance g_{mf} capacitively coupled at its output.

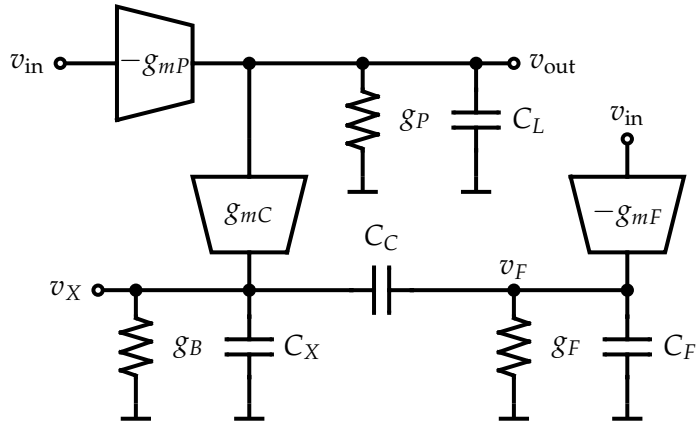


Figure 6.49: Simplified equivalent transconductance model of the proposed frequency compensation scheme capacitively coupling the output of the feed-forward transconductance g_{mF}.

into g_F on node v_F, as

$$\frac{v_X}{v_{in}} = -A_{DC} \cdot \frac{1 + s\,\zeta_1 + s^2\,\zeta_2}{\left(1 + \frac{s}{p_1}\right)(1 + s\,\rho_1 + s^2\,\rho_2)} \tag{6.16}$$

$$
\begin{aligned}
A_{\mathrm{DC}} &= \frac{g_{mP} g_{mC}}{g_B (g_P + g_{mC})} \\
\zeta_1 &= \frac{1}{g_F} \left(C_F + C_C + C_C \frac{g_{mF} (g_P + g_{mC})}{g_{mC} g_{mP}} \right) \\
\zeta_2 &= \frac{g_{mF} C_C C_L}{g_F g_{mC} g_{mP}} \\
p_1 &= \frac{g_P + g_{mC}}{C_L} \\
\rho_1 &= \frac{C_F + C_C}{g_F} + \frac{C_C + C_X}{g_B} \\
\rho_2 &= \frac{C_C C_F + C_C C_X + C_F C_X}{g_B g_F}
\end{aligned}
$$

Similarly to the input coupled feed-forward transconductance, two zeros are generated. They also have very similar frequencies compared to the previously discussed approach. Furthermore, an additional pole is introduced as well, associated with the feed-forward circuitry. The major difference though is the change of the v_X's pole frequency due to the direct connection of the coupling capacitance C_C.

When assuming well separated poles introduced by the polynomial term $1 + s\,\rho_1 + s^2\,\rho_2$, the second pole can be approximated as

$$
p_2 \approx \frac{1}{\rho_1} = \frac{1}{\frac{C_F + C_C}{g_F} + \frac{C_C + C_X}{g_B}} \tag{6.17}
$$

Compared to the original pole at $\frac{g_B}{C_X}$, it moved to lower frequencies. Furthermore, the ratio of $\frac{g_{mF}}{g_{mC}}$, i.e. the ratio of transistor fingers, determines the zero locations similarly to the input coupled version.

6.4.3 Circuit Implementation

Two variants of the previously described voltage regulator have been implemented. The main difference is the value of the on-chip output capacitance. The first design features only a load capacitance of $C_L = 30\,\mathrm{pF}$, which is used for the capacitive cancellation RF-DAC's LO distribution supply in the SIC

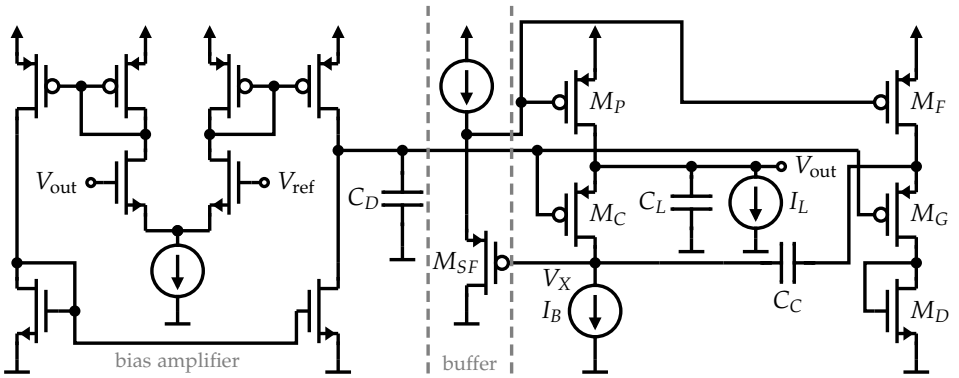


Figure 6.50: Transistor level schematic of the first LDO implementation featuring a load capacitance of only $C_L = 30\,\text{pF}$.

system, due to its area restriction in this part. The second design has a bigger load capacitance, slightly exceeding $C_L = 100\,\text{pF}$, also featuring a more complicated pass gate driving circuit.

Further required blocks, such as a reference voltage generator and a bias current generator, are available and not part of the LDO regulator itself. Therefore they are not further discussed in this work.

6.4.3.1 First Design: $C_L = 30\,\text{pF}$

As already mentioned, the first implementation features a load capacitance of only $C_L = 30\,\text{pF}$ due to area restrictions in the cancellation RF-DAC. The transistor level schematic of the LDO is shown in Figure 6.50. The frequency compensation scheme employed is discussed previously in Section 6.4.2.2, capacitively coupling the feed-forward transconductance's output.

The buffer driving the gate of the pass transistor M_P is implemented as the PMOS source follower M_{SF}. The low frequency amplifier is a plain differential pair with current mirror outputs, setting the bias potential of the CG amplifier. The coupling capacitor is chosen as $C_C = 265\,\text{fF}$.

In nominal conditions, the low frequency amplifier consumes roughly $500\,\mu\text{A}$ of bias current. The CG amplifier is biased at $400\,\mu\text{A}$ and the source follower

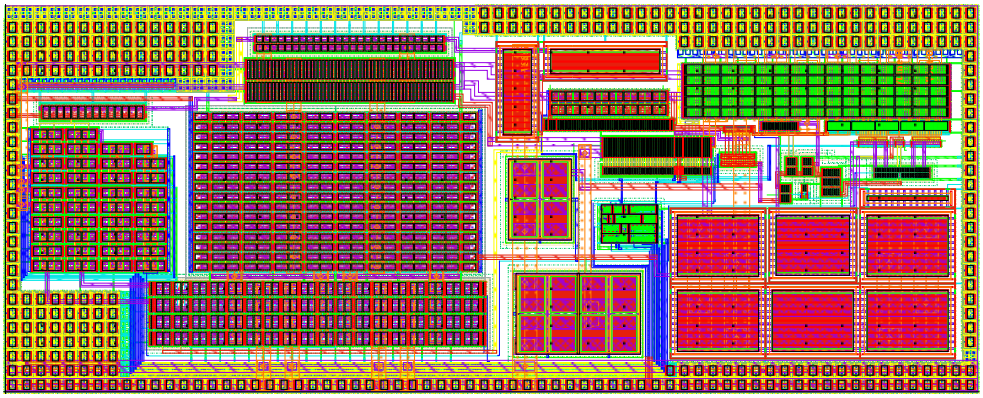


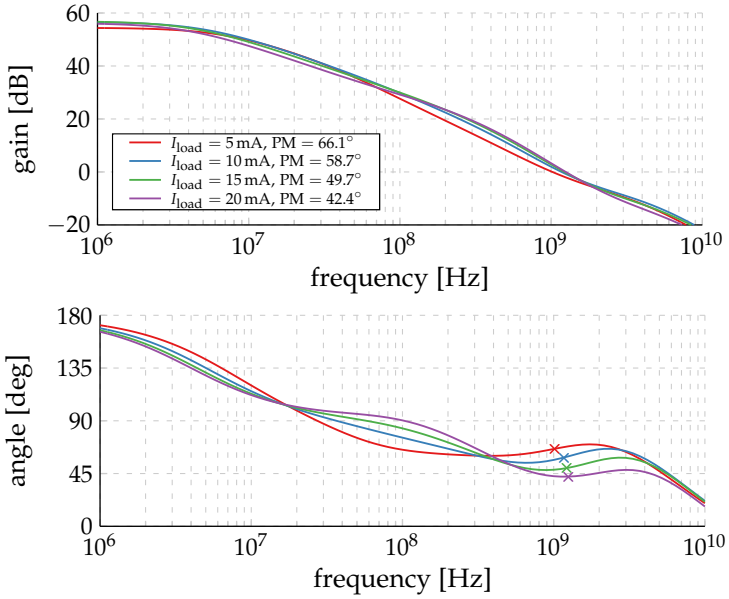
Figure 6.51: Physical drawing of the implemented first LDO variant. The dimensions are approximately $160 \times 63\,\mu m^2$

buffer at 700 µA, in order to shift its pole to sufficiently high frequencies. Finally, the feed forward branch's bias current varies from few microamperes at zero load current up to 125 µA at 15 mA load current.

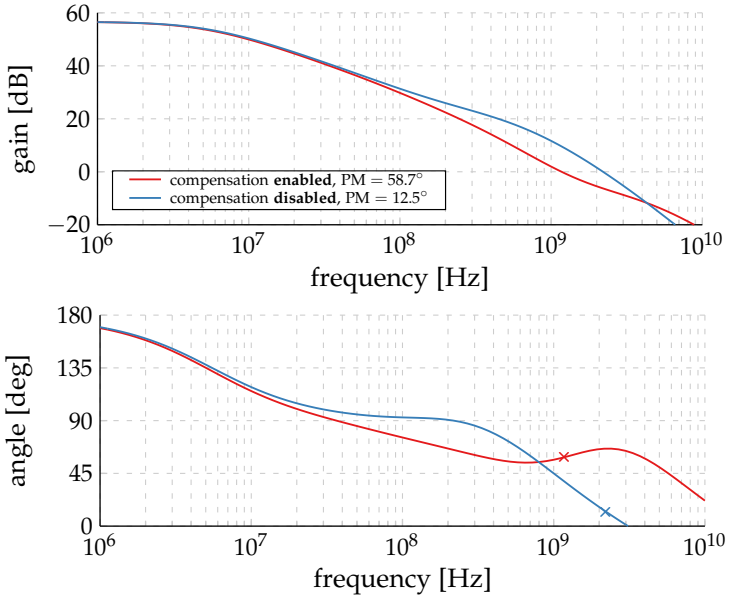
The physical drawing of this LDO variant is shown in Figure 6.51. All values are simulated with the post-layout extracted RC-coupled netlists. The current efficiency at 15 mA load current varies between 88 % and 90 % versus PVT including all internal biasing circuitry. The simulated worst case phase margin is 48° over all conditions with the extracted netlist.

Simulated open loop transfer characteristics are shown in Figure 6.52a. The unity gain frequency is above 1 GHz in all cases. To demonstrate the effect of the proposed frequency compensation, the uncompensated transfer function, when disconnecting the coupling capacitor C_C, is plotted in Figure 6.52b for reference. As clearly visible from the figure, the introduced frequency compensation is necessary and allows for ultra high bandwidth operation.

Similarly, the power supply rejection ratio (PSRR) and output resistance are shown in Figure 6.53 and Figure 6.54 respectively for nominal conditions. The output impedance seen by the RF-DAC is below 2 Ω for frequencies above 100 MHz for load currents bigger than 5 mA as specified. The PSRR is always better than −13 dB for the entire frequency range, thanks to the high regulation bandwidth of the LDO.



(a) Compensation enabled.



(b) Comparison with and without frequency compensation for a load current of 10 mA.

Figure 6.52: Open loop transfer characteristics of the LDO regulator with the proposed frequency compensation for different load currents simulated in nominal conditions.

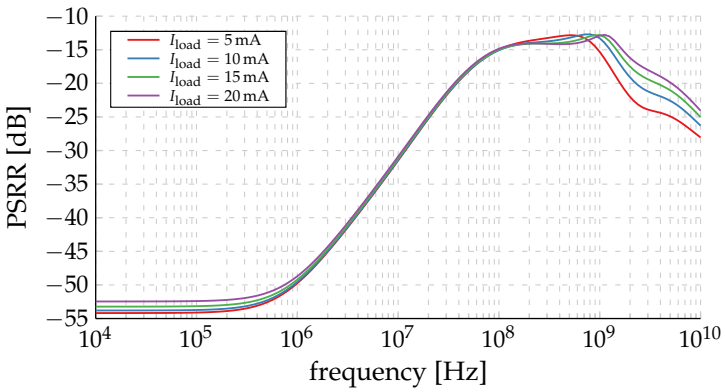


Figure 6.53: Simulated PSRR of the LDO regulator in nominal conditions.

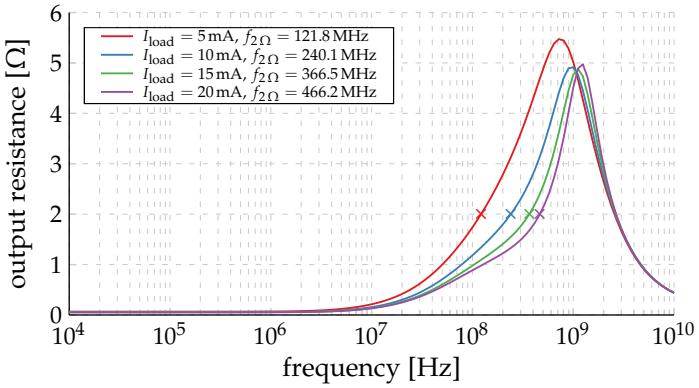


Figure 6.54: Simulated output impedance of the LDO regulator in nominal conditions for various load currents.

6.4.3.2 Second Design: $C_L \geq 100\,pF$

The second LDO variant employs the same frequency compensation mechanism. Contrary to the previous implementation, it features a load capacitance of $C_L = 100\,pF$. Furthermore, the driver for the pass transistor's gate uses a more complicated enhanced super source follower (SSF) structure [210], [211]. The transistor level schematic of this LDO variant is sketched in Figure 6.55.

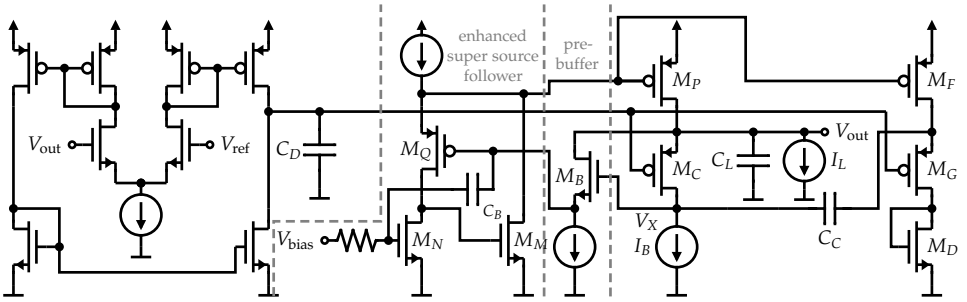


Figure 6.55: Transistor level schematic of the second LDO implementation featuring a load capacitance of $C_L \geq 100\,\text{pF}$.

The essential regulator structure, including the biasing amplifier, is very similar to the previous implementation. The rather simple gate driver, implemented as a PMOS source follower in the first design, is replaced by an enhanced SSF structure: The NMOS source follower M_B acts as a pre-buffer, decoupling node V_X from M_Q's gate. Transistor M_Q acts as a source follower for low frequencies, setting the potential of the pass gate. At higher frequencies, it operates more like a CS amplifier, driving the gate of M_M, which in turn acts as a CS amplifier, driving M_P's gate at high frequencies. To further boost the frequency behavior of the SSF structure, it is enhanced by means of C_B, which capacitively couples to the gate of the current source M_N, further pushing out the pole generated by the buffer.

In this design the coupling capacitance $C_C = 50\,\text{fF}$. The bias current of the CG amplifier M_C is chosen as 150 µA. The pre-buffer is biased at 60 µA while the SSF takes 390 µA, M_Q taking 140 µA and the CG transistor M_M 250 µA. Finally, the current through the feed-forward branch again varies with the load current and ranges from few microamperes and reaches 45 µA at 15 mA.

The physical drawing of this second LDO implementation is shown in Figure 6.56. All simulated values are derived from analyses with the post-layout extracted RC-coupled netlists. The current efficiency at 15 mA load current varies between 92 % and 94 % versus PVT including all internal biasing circuitry. The simulated worst case phase margin is 44°.

Compared to the first implementation, this variant offers a higher current efficiency, i.e. dissipates less power. This comes at the cost of increased output

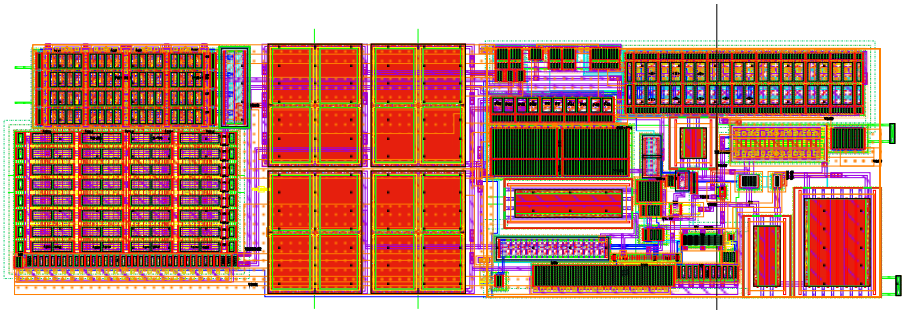


Figure 6.56: Physical drawing of the implemented second LDO variant. The dimensions are approximately $95 \times 28\,\mu m^2$

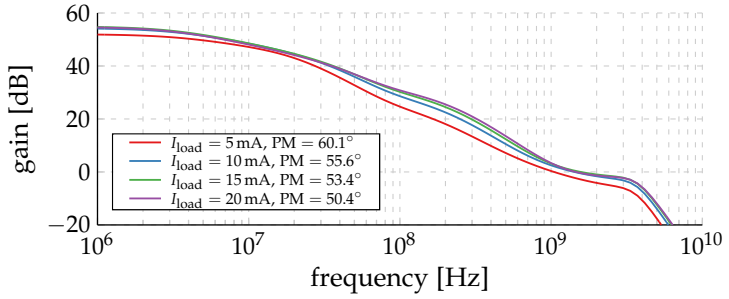
capacitance required. Also the circuit complexity, especially concerning the enhanced SSF, is increased.

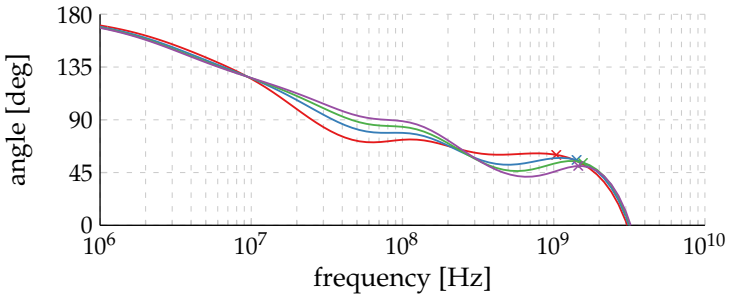
Simulated open loop transfer characteristics for various load currents I_L are shown in Figure 6.57a. Again, the effect of the proposed frequency compensation is demonstrated in Figure 6.57b where it is compared to the open loop characteristics of uncompensated LDO by disconnecting C_C. The unity gain frequency is above 1 GHz in all cases allowing for ultra high regulation bandwidths.

Similarly, the PSRR and output impedance are shown in Figure 6.58 and Figure 6.59 respectively. PSRR is below -15 dB for load currents above 5 mA for all frequencies. The output impedance is below $2\,\Omega$ for frequencies up to 300 MHz in all cases, resulting in greatly improved performance compared to the previous implementation.

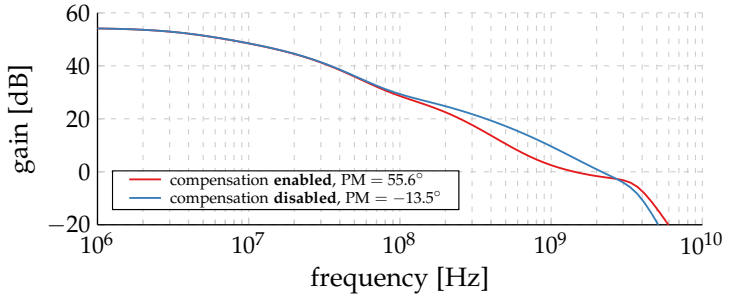
6.4.4 Conclusion

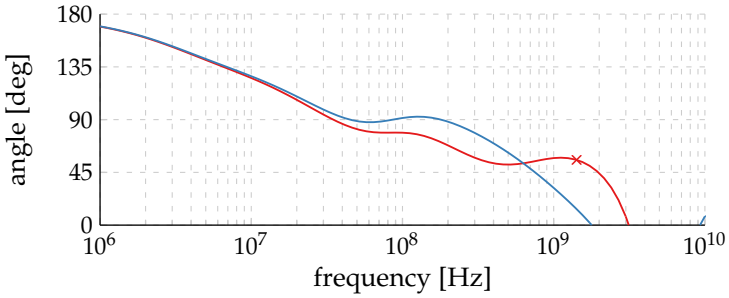
In this section novel frequency compensation schemes for FVF-based LDOs are developed, presented, and analyzed. These approaches enable LDO regulators with ultra-high regulation bandwidths at feasibly low power consumptions. Tailored to the needs of the cancellation RF-DAC, two candidate circuits with regulation bandwidths exceeding 200 MHz are implemented with





(a) Compensation enabled.





(b) Comparison with and without frequency compensation for a load current of 10 mA.

Figure 6.57: Simulated open loop transfer characteristics of the second LDO regulator implementation with the proposed frequency compensation for different load currents in nominal conditions.

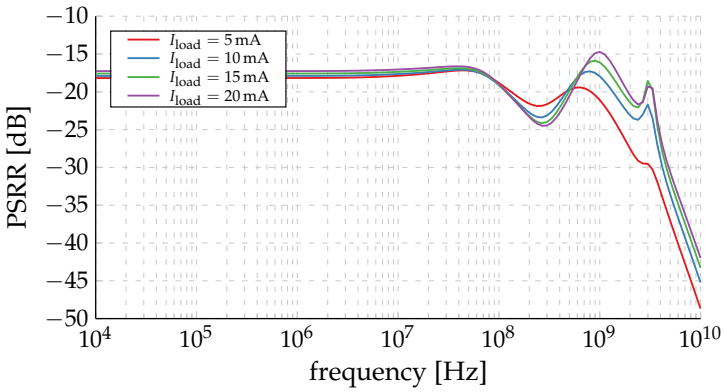


Figure 6.58: Simulated PSRR of the second LDO regulator in nominal conditions.

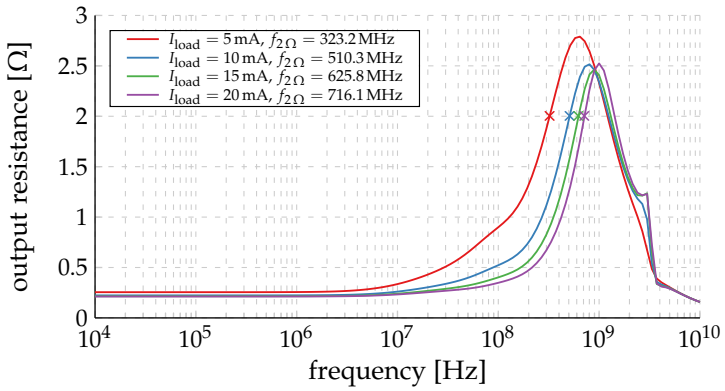


Figure 6.59: Simulated output impedance of the LDO with enhanced SSF in nominal conditions for various load currents.

differing secondary requirements, e.g. size of the output capacitance, power consumption, etc.

A resulting patent application [209] covering the presented novel frequency compensation schemes for the FVF circuit and FVF-based LDOs demonstrates the novelty and extension of the state-of-the-art.

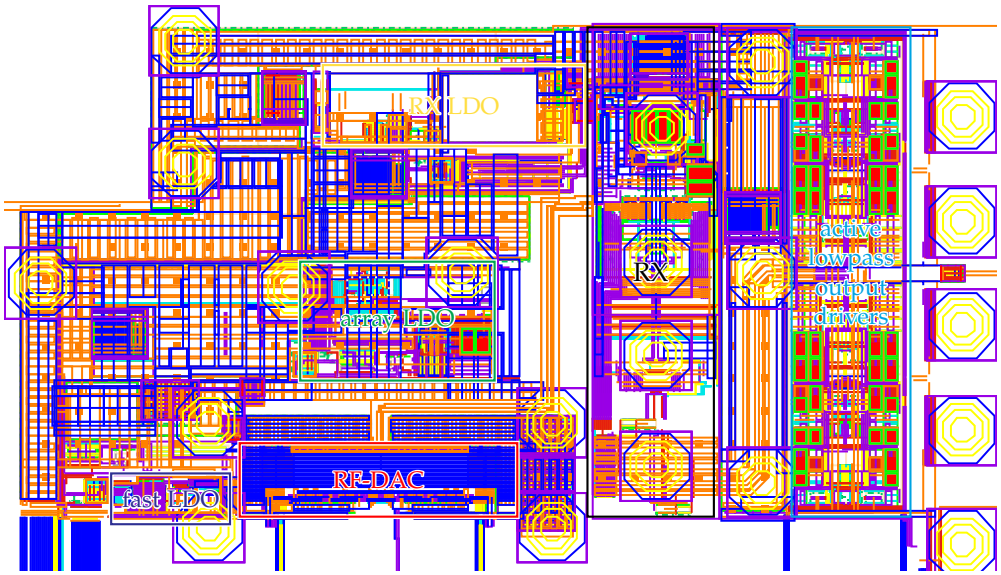


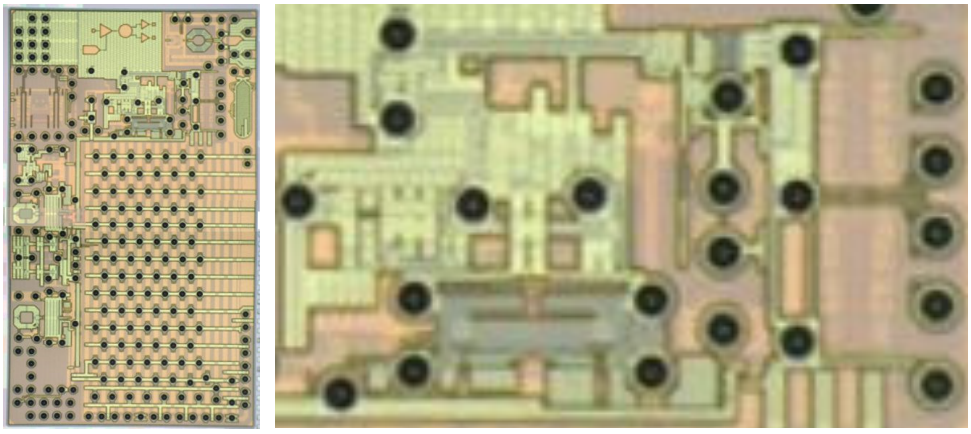
Figure 6.60: Physical drawing of the entire implemented SIC system including the RX and cancellation RF-DAC.

6.5 Cancellation System

The physical drawing of the entire SIC system, including the cancellation RF-DAC, the modified RX, active lowpass filters and output drivers, and all auxiliary circuitry such as LDOs and bias generators, is shown in Figure 6.60. The respective chip micrograph is shown in Figure 6.61.

The TX subsystem, generating the SI, is included on the same chip but not shown in the physical drawing in Figure 6.60. Additionally to the previously discussed supply regulators in Section 6.3.5 and Section 6.4, another readily available LDO for the RX is included, deriving 0.95 V from the 1.15 V input. The active lowpass output drivers are supplied externally with 1 V.

Input matching of the RX to 50 Ω is achieved with an external inductive matching network, as described in Section 6.2.1. Data to the cancellation RF-DAC is fed through a high speed data bus, driven by the preceding sample rate converter and DSP circuitry, as discussed in Section 4.2.



(a) (b)

Figure 6.61: Chip micrograph of the (a) manufactured prototype test chip and (b) zoom of the SIC portion.

6.6 Simulation Results

This section details simulated results of the entire designed SIC system described in Section 6.5, including all necessary blocks in the signal path, as well as auxiliary circuitry such as supply regulators and biasing circuits. For the simulations, RX input signals are applied with an ideal 50 Ω input port to the input matching network, which is external to the chip. An idealized inductive input matching network for the 2 GHz LO middle frequency is added at the RX input.

All digital input data, i.e. the data fed to the cancellation RF-DAC, is precomputed and preconditioned for the simulation setup, and fed directly to the cancellation DAC input, omitting any circuitry of the DSP blocks. Similarly, programming bits and data of the mixed-signal blocks, which would also be set by the digital block on the chip, are set with ideal sources. These simplifications allow for practicable simulation run times with meaningful analog accuracy.

The system is simulated with the Cadence Spectre circuit simulator [212]. Both, post-layout parasitic extracted netlists and schematic versions, are sim-

ulated. If not denoted otherwise, the schematic versions are used due to the heavily increased run times, spanning weeks, when using parasitic extracted netlists, compared to few days with the schematic versions.

6.6.1 Cancellation RF-DAC Performance

As a first step, the performance of the cancellation RF-DAC is simulated. In order to provide proper loading of the DAC's output, also the entire RX is added in the simulation, but no RF input signal is applied. The RX LO frequency is set to be the same as the cancellation RF-DAC's one, to avoid any resampling artifacts, as discussed in Section 4.2.5.

Time domain simulation results and the accompanying spectra of a 99 MHz complex exponential signal at −30 dBFS fed to the cancellation RF-DAC for a 2 GHz LO frequency are shown in Figure 6.62 and Figure 6.63 respectively. IM3 and the I/Q image power are shown in Figure 6.64a for signal frequencies ranging from 1 MHz to 100 MHz.

Similarly spurious-free dynamic range (SFDR) and signal-to-distortion ratio (SDR), excluding any thermal noise, are shown in Figure 6.64b. The SFDR is evaluated for the Nyquist zone of interest around the carrier, e.g. from $\frac{1}{2} \cdot f_{\mathrm{LO}}$ to $\frac{3}{2} \cdot f_{\mathrm{LO}}$.

Linearity of the cancellation RF-DAC in its non-canceling mode, i.e. without a canceled input signal present, is obviously degraded by the RX linearity, e.g. its various intercept points (IPs). Figure 6.65 shows the resulting powers of the fundamental and third harmonic for single tones at 99 MHz at varying power levels applied at the input and via the cancellation RF-DAC.

Clearly visible in the figure is the expected nonlinear behavior, essentially a result of the LNA loading the cancellation RF-DAC's output. While the fundamental's power increases with one dB per dB, the respective power of the third harmonic increases with 3 dB per dB input power. This is true not only for the cancellation DAC, but also for the main input signal, as also plotted in Figure 6.65. Somewhere between −15 dBFS and −10 dBFS (or −32 dBm and −27 dBm when referring to the input) the LNA starts to saturate, clearly indicated by the third harmonics' powers. Of course, when an interfering

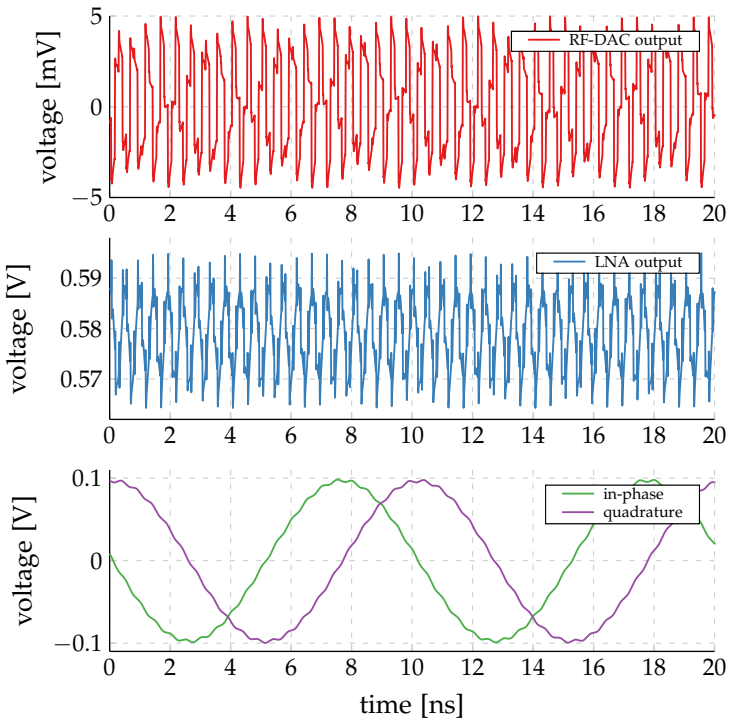


Figure 6.62: Simulated time domain signals when the cancellation RF-DAC is excited with a 99 MHz complex exponential signal at −30 dBFS with 2 GHz LO frequency in nominal conditions excluding thermal noise. Shown are the single-ended cancellation RF-DAC output, the LNA output, and the in-phase and quadrature differential baseband signals.

signal is properly canceled, LNA performance can be restored to linear operation, despite the large signal powers present at the input and cancellation RF-DAC.

In Figure 6.66 the cancellation RF-DAC output for 20 MHz and 100 MHz bandwidths signals at −30 dBFS are shown. The 100 MHz bandwidth signal is additionally shifted by −100 MHz in the frequency domain, effectively creating a 150 MHz bandwidth for the DAC. In fully RC-coupled extracted simulations of the entire SIC block, the error vector magnitudes (EVMs) [213]–[216] are below 0.7 % in all cases up to 100 MHz analyzed signal bandwidths, and frequency shifts ranging from −100 MHz to 0 MHz for LO frequencies

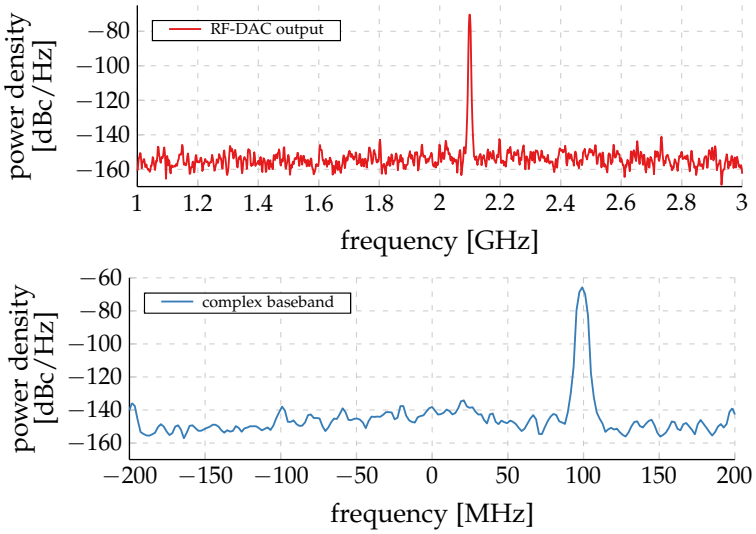


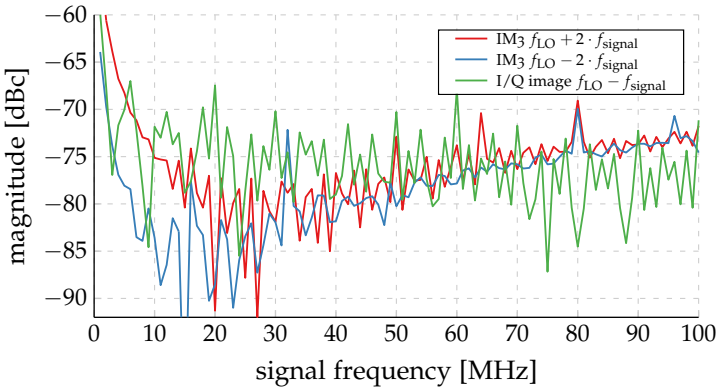
Figure 6.63: Accompanying spectra related to the signals shown in Figure 6.62.

of 1.4 GHz to 2.7 GHz. EVM performance is limited by quantization noise at −30 dBFS signal levels. Similarly, for −30 dBFS, the ACLR [132] values are lower than −45 dB, limited by quantization noise, and for −10 dBFS, the ACLR is better than −61 dBc. These values prove excellent performance of the cancellation RF-DAC.

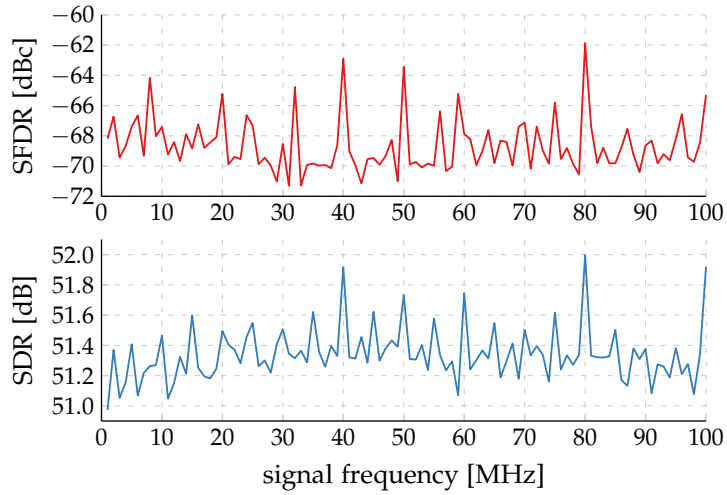
6.6.2 Cancellation of Single Tone Complex Exponentials

For this set of simulations the LO frequencies of the RX and the cancellation RF-DAC are kept equal to avoid any resampling artifacts as discussed in Section 4.2.5. Initially, an LO frequency of $f_{RX} = 2\,GHz$ is chosen to reduce the number of required simulations. An idealized inductive input matching network for this LO frequency is added at the RX input.

As a starting point, single tone complex exponentials are applied as stimuli to the cancellation system. Time-domain simulations with the schematic version of the systems are performed for the typical case without any thermal noise. No adaptive or other algorithms are employed due to the long settling times required, which can be up to several milliseconds. Instead, separate



(a) IM3 and quadrature image.



(b) SFDR and SDR.

Figure 6.64: Simulated cancellation RF-DAC performance parameters for −30 dBFS at 2 GHz LO frequency in nominal conditions excluding thermal noise.

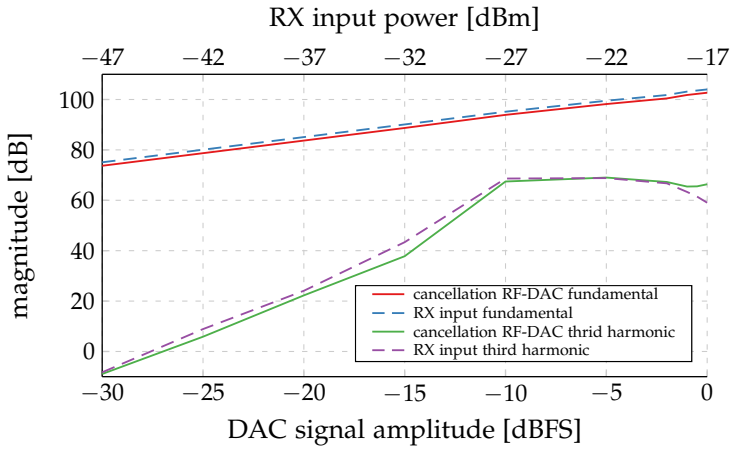


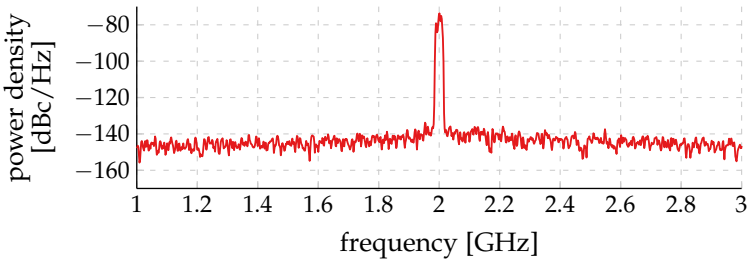
Figure 6.65: Fundamental and third harmonic powers for single tone complex exponential inputs at 99 MHz applied at the RX input and through the cancellation RF-DAC. Arbitrary units on the y-axis.

simulations are run for the main and cancellation signals to analyze the individual transfer characteristics and eventually compute the required signal modifications to achieve cancellation.

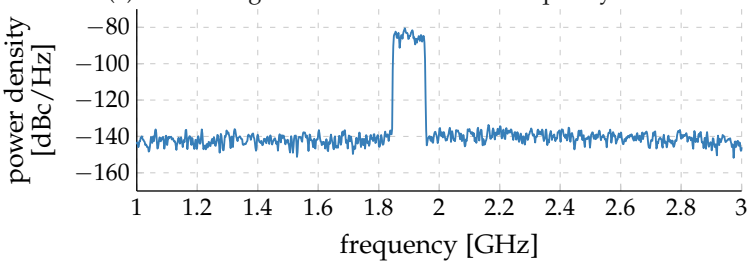
A signal frequency sweep from 1 MHz to 100 MHz is executed, effectively resulting in sinusoidals ranging from 2001 MHz to 2100 MHz with a 2 GHz LO frequency. In the case of using the main RX input, a signal amplitude of 1 mV is used, which translates to an input power of 0.02 µW or −47 dBm at 50 Ω. Similarly, when the cancellation RF-DAC is operated, it's amplitude is set to −30 dBFS. These low signal powers are used in the beginning to ensure sufficiently linear operation. Further on, the signal powers are increased.

The transfer characteristics in amplitude and phase for both main and cancellation inputs are shown in Figure 6.67a for the LNA output, i.e. in the RF domain. Furthermore, in Figure 6.67b the very outputs of the entire RX is shown, i.e. the analog complex baseband output. Exemplary, RF domain and baseband spectra for the 99 MHz signal frequency are shown in Figure 6.68 along with cancellation spectra discussed below.

Figure 6.67a reveals a very flat frequency response at the LNA output for a 100 MHz signal bandwidth, which is well within 1 dB for both the main and

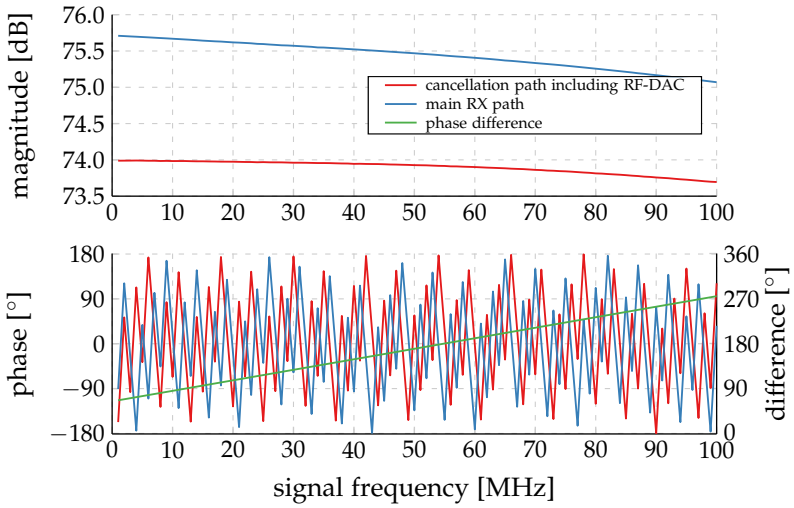


(a) 20 MHz signal bandwidth and no frequency shift.

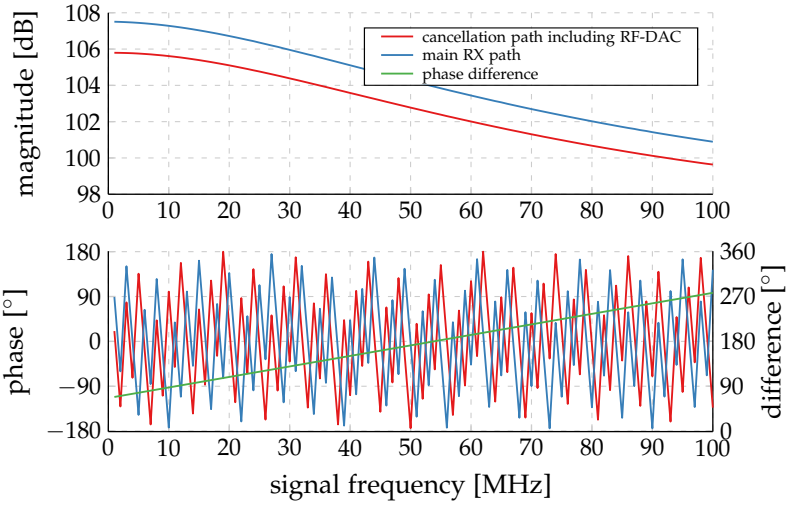


(b) 100 MHz signal bandwidth and −100 MHz frequency shift.

Figure 6.66: Spectra of simulated cancellation RF-DAC multi tone signals with different bandwidths and frequency offsets at −30 dBFS. RC-coupled parasitic extracted netlists are used. The quantization noise floor of $13 + 1$ physical bits is degraded due to the 30 dB of backoff.

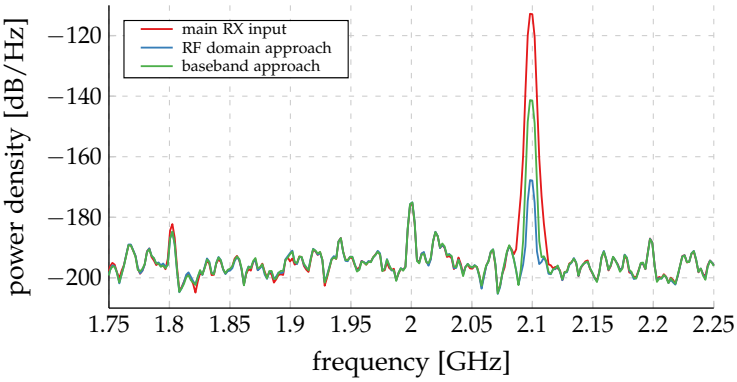


(a) RF domain at $f_{\mathrm{LO}} + f_{\mathrm{signal}}$.

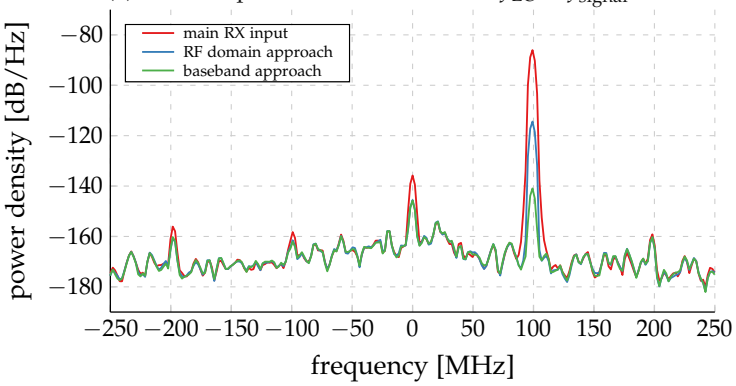


(b) Complex baseband outputs at f_{signal}.

Figure 6.67: Simulated transfer characteristics for the main and cancellation path to the LNA and baseband outputs, when the RX input peak power is −47 dBm and the cancellation RF-DAC is operated at −30 dBFS with LO frequencies of 2 GHz.



(a) LNA output in the RF domain at $f_{\mathrm{LO}} + f_{\mathrm{signal}}$.

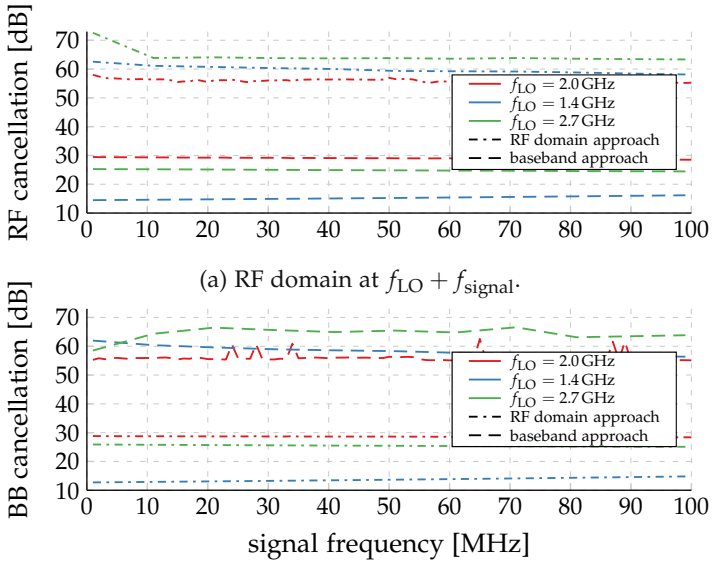


(b) Complex baseband outputs at f_{signal}.

Figure 6.68: Simulated spectra of the LNA and baseband outputs with only an RX input signal and the two cancellation approaches. The LO frequency is 2 GHz and the signal frequency 99 MHz. Arbitrary units on the y-axes.

the cancellation paths. Simulations indicate that the phase shift through the main RX is smaller than through the cancellation RF-DAC. The phase difference is nearly linear, resulting from a frequency independent delay present in the cancellation path. The baseband paths clearly exhibit the low pass characteristics of the output buffer as shown in Figure 6.67b.

In simulations, there are essentially two different possibilities to calculate the proper cancellation signal. First, the output of the LNA in the RF domain can be nullified. Obviously, in implementations this approach is not directly



(a) RF domain at $f_{LO} + f_{signal}$.

(b) Complex baseband outputs at f_{signal}.

Figure 6.69: Simulated cancellation performance at the LNA and baseband outputs, when the RX input peak power is $-47\,dBm$ for different LO frequency for various signal frequencies.

suitable. Though, it is expected that properly designed DSP algorithms can mimic such behavior. Second, the baseband signals are used to obtain the cancellation signal. This method is directly suitable for implementations, since these low frequency signals can be easily digitized and fed to DSP algorithms which in turn generate a cancellation signal. Regardless of the variant of this indirect calculation of the cancellation signal chosen, capable DSP algorithms are required to create suitable input data for the cancellation RF-DAC.

Figure 6.69 shows the cancellation performance for both approaches for varying signal frequency at different LO frequencies. The cancellation signal is the original signal fed to the cancellation RF-DAC weighted with the difference in amplitude and phase of the previously simulated signals. Spectra for the two cases at the LNA and baseband outputs are shown in Figure 6.68.

These simulations reveal a cancellation performance better than 55 dB over the entire signal frequency range up to 100 MHz. This is only true for either one of the two signals, i.e. either in the RF domain or in baseband, depending

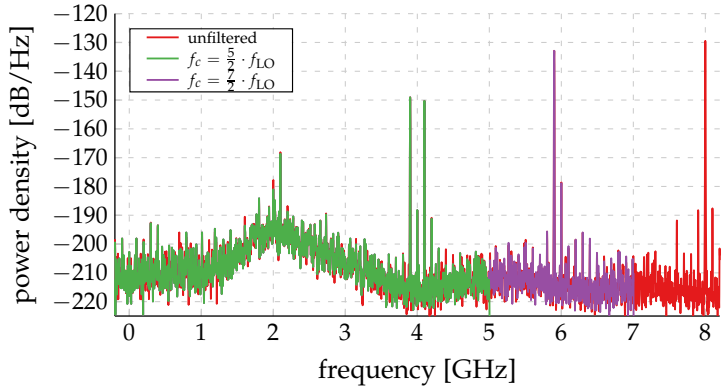
on the chosen approach. Critical to this behavior is the limited cancellation performance in either scenario of the respective other non-optimized signal in the RX, which can drop down to 15 dB. In cases where the SI power degrades the RX performance, especially this behavior of limited RF domain cancellation at the LNA output can pose a limiting factor. Essentially, more complicated DSP algorithms and models may be required to properly model and restore RX performance.

The reason for this counterintuitive behavior is the absence of any filtering at the cancellation RF-DAC output. Due to the sampling operation and the LO harmonics, signal images are present at multiples of the LO frequency. This behavior is shown in the zoomed out version of the RF domain spectrum for a 99 MHz complex exponential shown in Figure 6.70a. It shows the LNA output when the SIC is trying to nullify this output. The most prominent image is located at $3 \cdot f_{\mathrm{LO}} + f_{\mathrm{signal}}$, i.e. at 6.099 GHz in this example.

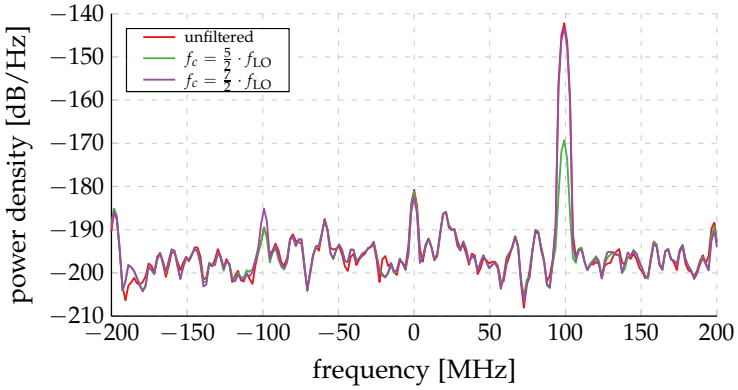
This very image is also responsible for the imperfect cancellation of the baseband outputs when using the RF domain approach. To verify this behavior, the RF domain LNA output signal is artificially lowpass filtered at cutoff frequencies of $\frac{5}{2} \cdot f_{\mathrm{LO}}$ and $\frac{7}{2} \cdot f_{\mathrm{LO}}$. The respective spectra are also shown in Figure 6.70a. The version of the signal filtered with a cutoff frequency of $\frac{7}{2} \cdot f_{\mathrm{LO}}$, includes the prominent signal image at $3 \cdot f_{\mathrm{LO}} + f_{\mathrm{signal}}$.

This image is downconverted to DC, i.e. directly into baseband, by the respective third harmonic of the RX LO. This harmonic shifts a non-negligible signal portion into baseband, as shown in Figure 6.70b, which shows the respective baseband output spectra for the discussed signals. This phenomenon essentially is the reason why perfect cancellation cannot be achieved simultaneously at both LNA and baseband outputs. As is shown later in Section 6.6.4, this behavior is not necessarily a limiting issue.

A power sweep is performed, shown for two signal frequencies of 9 MHz and 99 MHz in Figure 6.71, similar to the one shown in Section 6.6.1 in Figure 6.65. This simulation results show both the signal amplitude and phase shift at the LNA output in the RF domain. Interestingly, for high signal powers, the phase shift towards the output changes by almost 10°, which is an indication of nonlinear operation. Importantly, the phase difference between the main and cancellation paths also change with the signal power. This is a



(a) LNA output in the RF domain.



(b) Complex baseband outputs.

Figure 6.70: Simulated spectra of the LNA and baseband outputs with artificially lowpass filtered versions. The LO frequency is 2 GHz and the signal frequency 99 MHz. Arbitrary units on the y-axes.

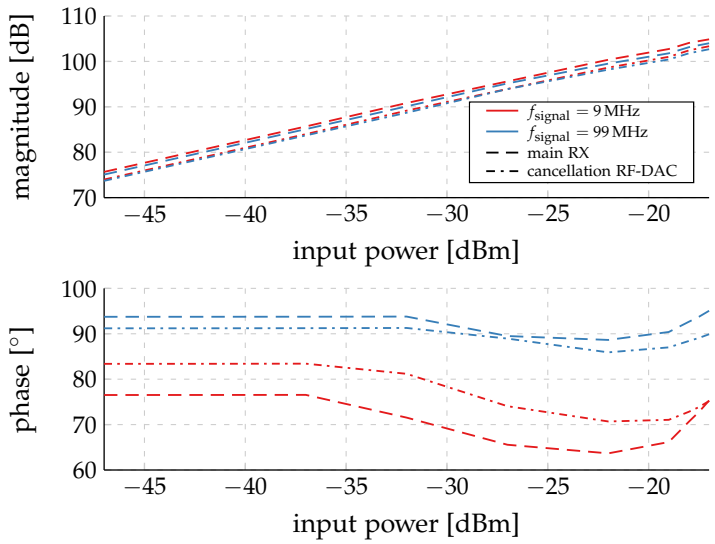
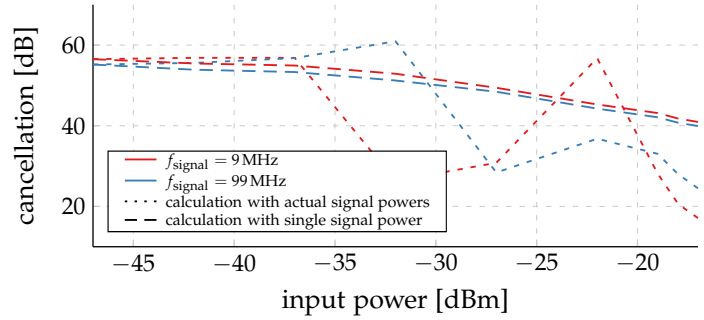


Figure 6.71: Simulated transfer functions at the LNA output for different signal powers. The LO frequency is 2 GHz. Arbitrary units on the magnitude y-axis.

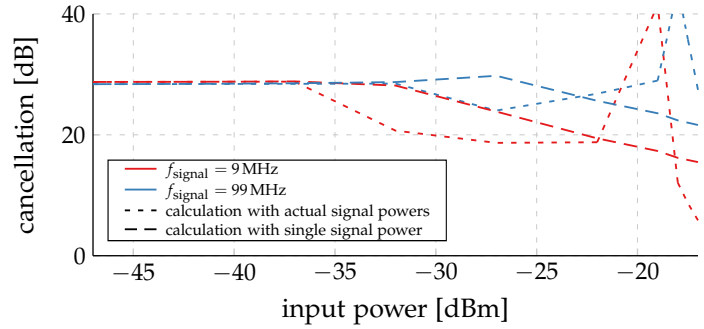
critical for cancellation performance and needs to be considered in DSP when calculating the cancellation signals.

The same power sweep is performed with activated SIC. First, the simulated cancellation performance for the RF domain approach is depicted in Figure 6.72. In addition to calculating the signal weights in the RF domain, two further possibilities are explored: First, in the naive approach, the main and cancellation transfer functions are evaluated at the actual power levels. Thus, the weights are calculated at the actual signal power levels the cancellation is performed at. The second option is calculating the weights once at fixed power levels of e.g. −47 dBm for the RX input port and −30 dBFS at the cancellation RF-DAC and further properly scaling the power of the cancellation signal according to the RX input power.

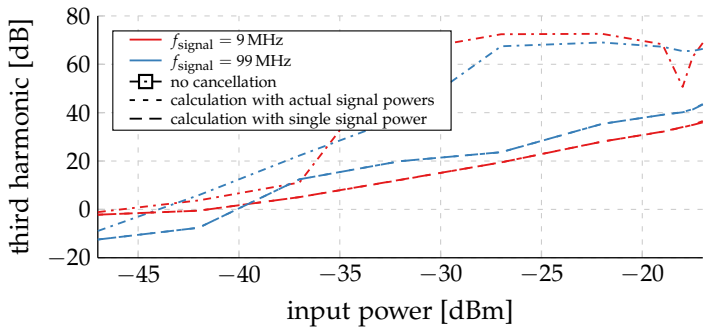
As shown in Figure 6.72, a behavior similar to the previous analyses is observed. The cancellation performance is better by roughly 25 dB at the LNA output rather than in baseband due to the high order signal images as explained above. But more interesting in this power analysis is the behavior of the two additional methods of cancellation signal calculation: The naive ap-



(a) LNA output in the RF domain. Signals evaluated at $f_{LO} + f_{signal}$.



(b) Complex baseband outputs. Signals evaluated at f_{signal}.



(c) Third harmonic powers at the LNA output. Signals evaluated at $f_{LO} \pm 3 \cdot f_{signal}$. Arbitrary units on the y-axis.

Figure 6.72: Simulated LNA and baseband outputs for activated SIC with different input powers. The cancellation signals are calculated with the RF domain approach. The LO frequency is 2 GHz.

proach of calculating the cancellation signals directly at the canceled signal powers results in heavily degraded cancellation performance as the input signal power increases. The reason for this behavior is the nonlinear operation of the RX, which results in an obviously wrong calculation of the cancellation signal. In turn, the second method yields improved cancellation performance which degrades by less than 15 dB as the input signal power increases by more than 30 dB. The simulated cancellation is always above 40 dB in these scenarios, even at input powers exceeding the specified −20 dBm.

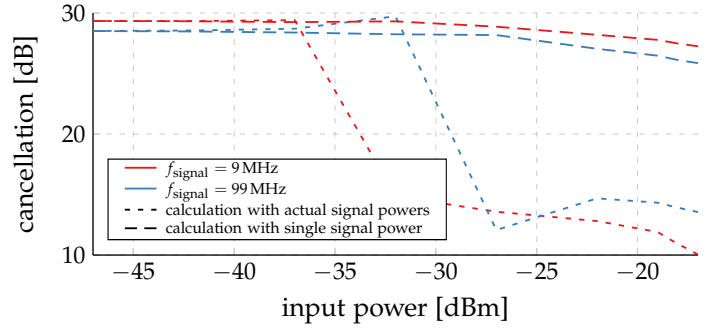
But most importantly, the RX performance can be restored, which is clearly visible in Figure 6.72c: Without any SIC active, around −35 dBm input power, the harmonic power strongly increases, which is a clear indication of RX saturation and nonlinear operation. When the cancellation is active, the power of the third harmonic increases by approximately 3 dB per dB increase of input power, which is an indicator for still operating the RX far away from its IPs.

A very similar behavior is observed in Figure 6.73, where the baseband approach is used to calculate the respective cancellation signals. The cancellation performance degrades by approximately 20 dB for input signals above −20 dBm when using the second approach of calculating the cancellation signals at low signal powers. With the naive method the cancellation drops below 15 dB at input powers exceeding −35 dBm. For these cases obviously the nonlinear operation of the entire RX, including the active lowpass filters, is a limiting factor when no adaptive and iterative algorithms are employed.

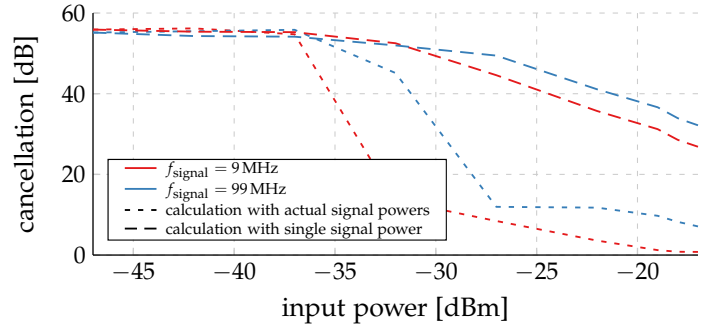
But again, the RX performance can be restored, as seen in Figure 6.73c, where the increase of the third harmonic is reduced to the expected 3 dB per dB characteristic. In any weight calculation case, the RX operation can be improved and linearized with the presented approach.

6.6.3 Cancellation of Multi Tone High Bandwidth Signals

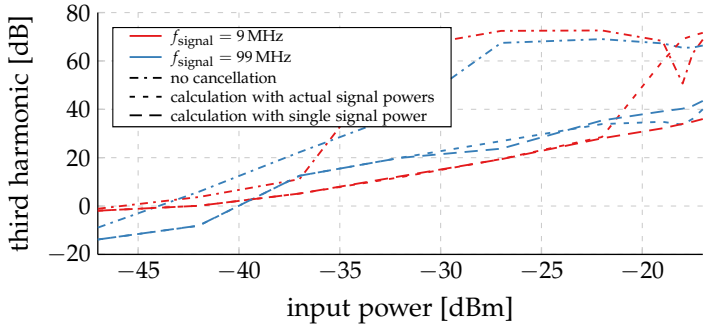
More practical insight into the circuit's feasibility and performance is obtained by evaluating the cancellation of multi tone high bandwidth signals, which are used in real world applications. For these simulations though, an increased tone spacing compared to LTE and 5G-NR [217] of 1 MHz is used



(a) LNA output in the RF domain. Signals evaluated at $f_{\text{LO}} + f_{\text{signal}}$.



(b) Complex baseband outputs. Signals evaluated at f_{signal}.



(c) Third harmonic powers at the LNA output. Signals evaluated at $f_{\text{LO}} \pm 3 \cdot f_{\text{signal}}$. Arbitrary units on the y-axis.

Figure 6.73: Simulated LNA and baseband outputs for activated SIC with different input powers. The cancellation signals are calculated with the baseband approach. The LO frequency is 2 GHz.

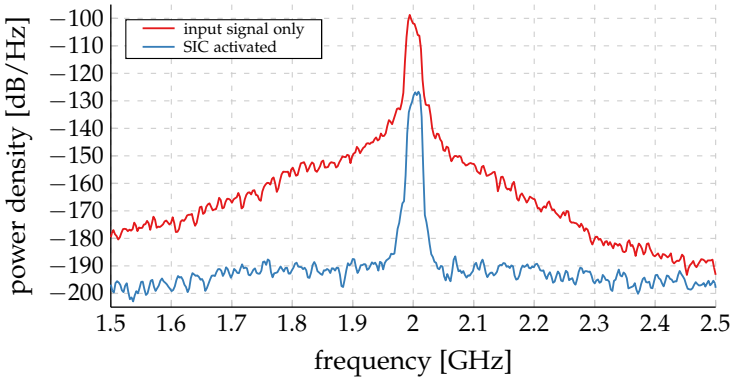
to effectively reduce simulation times while maintaining similar signal properties (e.g. RMS power, PAPR, amplitude distribution, ...).

For the reported results, the cancellation signals are directly calculated similarly to the single tone complex exponentials discussed in the previous section. Essentially, this analysis should show the performance of the analog and RF circuitry, given a proper digital cancellation signal. Furthermore, within simulations, iterative and adaptive approaches are unfeasible due to the long simulation times and high number of iterations required. Thus, improved SIC performance compared to the values reported below are possible for more sophisticated methods of cancellation signal calculation, e.g. by using iterative approaches.

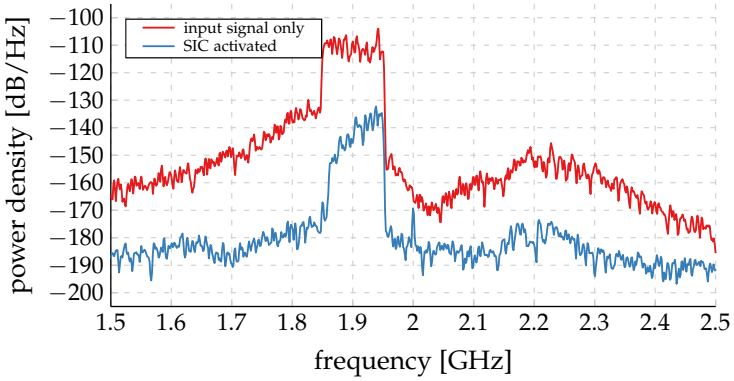
Figure 6.74 shows spectra of 20 MHz and 100 MHz bandwidth signals before and after cancellation for a 2 GHz LO frequency. Cancellations of 30.1 dB and 29.7 dB are achieved, i.e. the overall SI signal power integrated over the signal bandwidth is reduced by the reported cancellations. More importantly, the spectral regrowth at the LNA output is significantly reduced, since the SIC linearizes the RX operation.

Cancellation performances for different LO frequencies, bandwidths, and signal powers are shown in Figure 6.75. Cancellation performances are generally above 25 dB are achieved in all cases at the LNA output, except for the 20 MHz bandwidth case with a 1.4 GHz LO frequency. In this case the performance is limited by the calculation approach of the cancellation signal chosen for these simulations. Iterative methods can also adapt to the nonlinear operation of the LNA in this scenario.

Similar to the single tone case, the cancellation performance, when calculating the cancellation signal with the RF domain approach, is limited by the third harmonic being mixed down into baseband. Still, the LNA is linearized and a cancellation better than 10 dB is achieved. Further SIC can be achieved e.g. by cancellation in the digital domain, since this approach can linearize the RX operation.

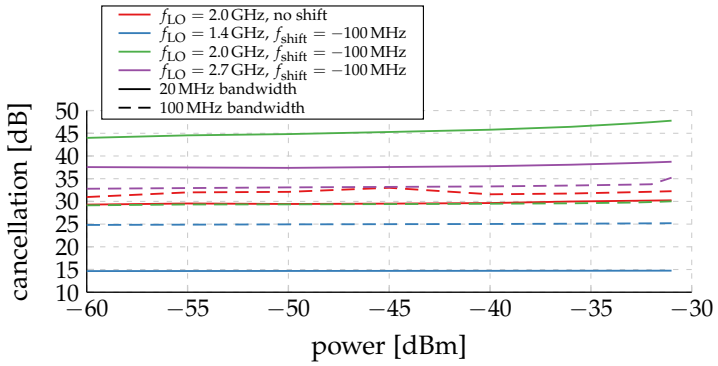


(a) 20 MHz bandwidth signal.

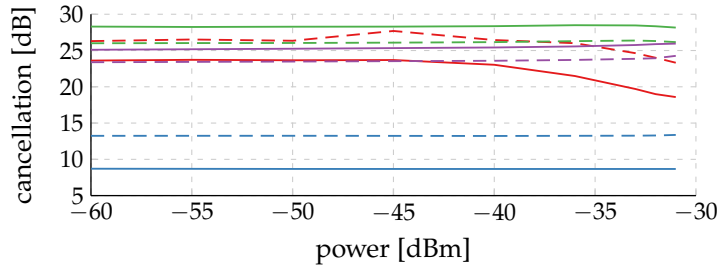


(b) 100 MHz bandwidth signal at −100 MHz offset from the LO.

Figure 6.74: Simulated LNA outputs for different input signals with an RMS power of −33 dBm. The cancellation signals are calculated with the RF domain approach. The LO frequency is 2 GHz.



(a) LNA output in RF domain.



(b) Complex baseband outputs.

Figure 6.75: Simulated cancellation performance for different bandwidths and SI power levels. The cancellation signals are calculated with the RF domain approach.

6.6.4 Restoring Receiver Performance with SIC

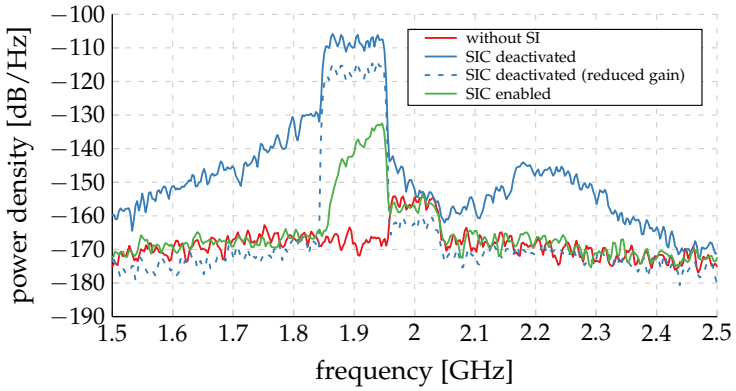
Finally, the feasibility and performance of the designed RF-domain SIC circuit is proven with simulations where both, a desired RX signal and blocking TX-induced SI, are present. For these analyses, only a subset of the possible combinations of frequencies, bandwidths, and signal powers is reported.

Figure 6.76 shows example spectra of the LNA and baseband outputs with and without cancellation activated, including simulated thermal noise. The 100 MHz bandwidth TX signal is centered at 1.9 GHz, the 80 MHz RX signal at 2.0 GHz, resulting in a frequency spacing of only 10 MHz. Without cancellation, the strong TX SI completely drives the LNA into saturation, raising the noise floor and completely masking the desired RX signal.

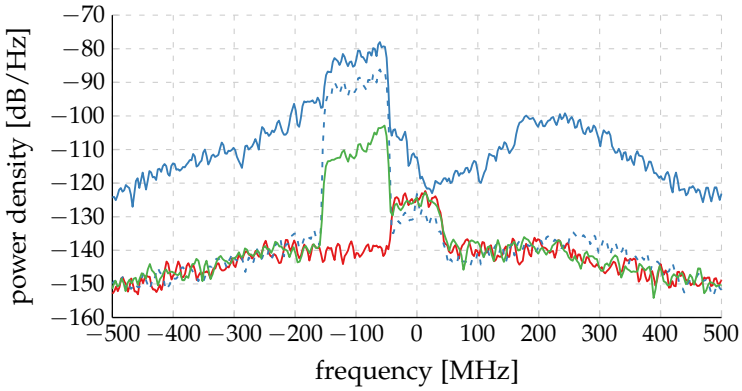
Alternatively to SIC, also the gain of the LNA can be reduced, e.g. by 10 dB as shown in Figure 6.76 with dashed lines. Also in this case, the LNA (output) is not saturated. With this approach, the available SNR of the desired RX signal is obviously reduced. This can be easily observed in Figure 6.76, where thermal noise is included in the analyses and dominates the noise floor, if the RX is not saturated. In this case the thermal noise corrupts the RX signal non-negligibly and limits RX performance. Contrary, when using SIC, the gain of the RX can be increased, further improving its performance.

This behavior can be quantified by e.g. calculating the RX EVM, which directly influences the system's data throughput [213]–[216]. Figure 6.77 and Figure 6.78 show these EVM values, evaluated at the complex BB outputs. Two cases with equal carrier frequencies are shown: a *low* bandwidth case with 20 MHz bandwidths for both the leakage signal at 1.9 GHz and the RX signal centered at the 2 GHz LO, and a *high* bandwidth case, with 100 MHz and 80 MHz bandwidths respectively. All these simulations include thermal noise, greatly prolonging simulation run times. Note that the EVM is directly evaluated from the analog signals without any equalization or other (digital) means of signal enhancement. E.g. the unaccounted low pass characteristics of the active BB low pass filters directly impairs the EVM.

Simulations show, that for low RX powers, the proposed mixed-signal RF domain SIC can improve the analog performance of the RX. This is especially true for low RX signal bandwidths with rather big duplex spacings. For larger



(a) LNA output in the RF domain.



(b) Complex baseband outputs.

Figure 6.76: Simulated LNA and baseband outputs for different scenarios with and without cancellation without thermal noise. The LO frequency is 2 GHz, the 100 MHz TX signal is centered at 1.9 GHz with a −31 dBm RMS leakage power and 7 dB PAPR, while the 80 MHz RX signal is at −85 dBm RMS.

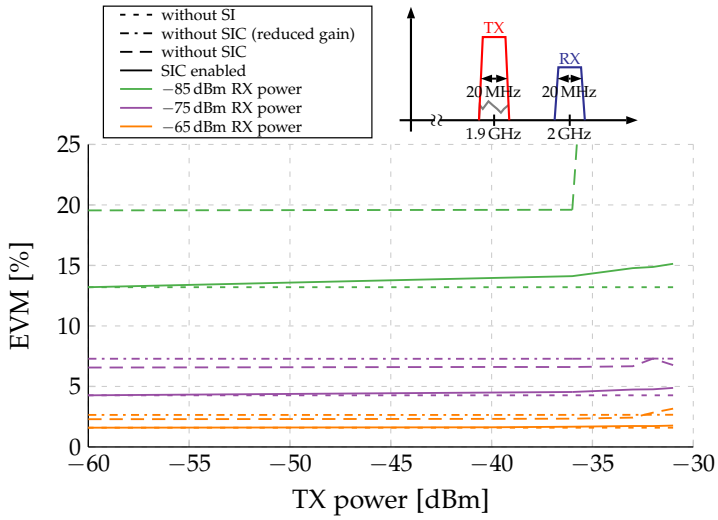


Figure 6.77: Simulated EVM values for various cases with and without SIC, including thermal noise. The LO frequency is 2 GHz, the RX signal has a 20 MHz bandwidth, and the leaked 20 MHz TX signal is centered at 1.9 GHz. The sketched spectrum on top illustrates the scenario.

signal bandwidths, the power per frequency decreases, since the signal power is spread over a wider bandwidth. The thermal noise density of the RX stays constant independent of the signal bandwidth, thus decreasing the SNR.

Furthermore, for low TX-to-RX distances, the EVM is additionally impaired by the residual IMD, i.e. the nonlinear components generated by the RX and nonlinear emissions of the TX close to the carrier, e.g. the adjacent channel region, that fall into the RX band. In these cases, linear SIC is greatly beneficial only for very high leakage levels. With more advanced DSP algorithms covering also these RX and TX nonlinearities, the system performance can be improved. This increase in flexibility is clearly an immense benefit of this mixed-signal SIC approach, while providing cancellation in the RF domain.

Similarly, for low SI powers, the additional power consumption of the SIC system and (slightly) improved signal reception must be traded off. This is especially true for high RX signal strengths, where the signal quality, i.e. the SNR, is inherently better.

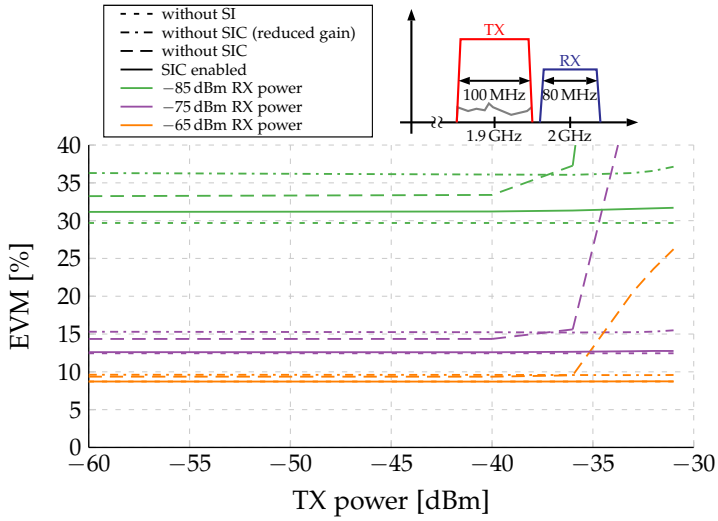


Figure 6.78: Simulated EVM values for various cases with and without SIC, including thermal noise. The LO frequency is 2 GHz, the RX signal has a 80 MHz bandwidth, and the leaked 100 MHz TX signal is centered at 1.9 GHz. The sketched spectrum on top illustrates the scenario.

6.7 Conclusion

The mixed-signal RF domain SIC system, described in Chapter 4 has been implemented in a 28 nm bulk-CMOS technology for operating frequencies ranging from 1.4 GHz to 2.7 GHz. Within this chapter, the circuit design of all key building blocks are discussed:

- augmentation of an analog high performance RX with a cancellation signal injection port,
- the novel single-ended capacitive cancellation RF-DAC architecture, its circuit operation and implementation, and
- a high regulation bandwidth FVF-based LDO regulator with a novel frequency compensation structure for high performance RF-DAC operation.

The entire system discussed in Chapter 4 is revisited on a circuit design level. Implementation details of all required blocks are provided. The feasibility

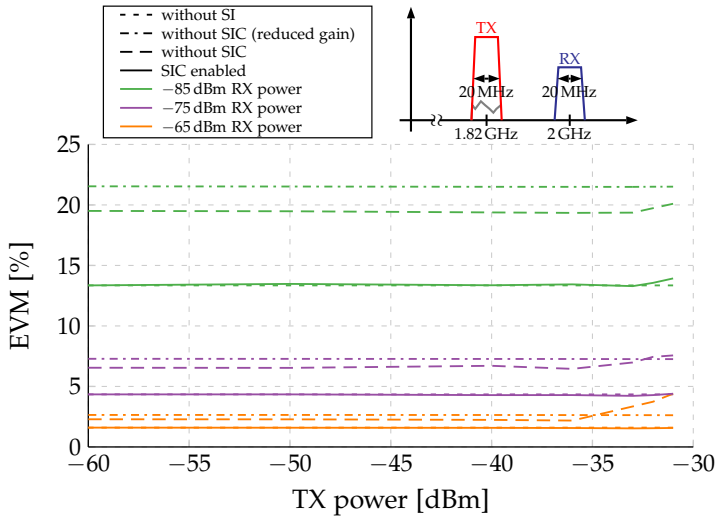


Figure 6.79: Simulated EVM values for various cases with and without SIC, including thermal noise. The LO frequency is 2 GHz, the RX signal has a 20 MHz bandwidth, and the leaked 20 MHz TX signal is centered at 1.82 GHz. The sketched spectrum on top illustrates the scenario.

of the proposed fully integrated approach is demonstrated with extensive simulation based analyses. The designed cancellation RF-DAC exhibits state-of-the-art performance, suitable for its intended SIC application.

The presented results prove the feasibility of the integrated SIC approach. Simulations of the entire designed prototype system demonstrate excellent performance and further emphasize the benefits of the chosen approach:

- fully integrated SIC system without any external component overhead,
- mixed-signal RF-DAC solution, fully benefiting from analog cancellation, whilst keeping all flexibility of digital approaches,
- easily combinable with additional SIC mechanisms, such as fully analog and/or fully digital approaches for further improving cancellation performance, e.g. for in band FD, and
- a low power digital-like circuit implementation suitable for low supply voltages, benefiting from technology scaling, and being portable.

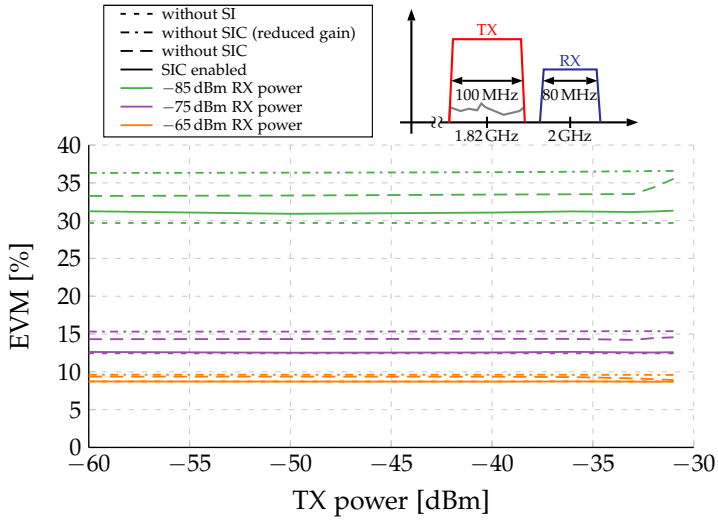


Figure 6.80: Simulated EVM values for various cases with and without SIC, including thermal noise. The LO frequency is 2 GHz, the RX signal has a 80 MHz bandwidth, and the leaked 100 MHz TX signal is centered at 1.82 GHz. The sketched spectrum on top illustrates the scenario.

Throughout the RF-DAC circuit design, a journal paper was published on the subject [9]. A patent application was submitted covering solutions to the discussed sign change issue [192]. Another patent application [209], covering the novel LDO structure, further demonstrates the novelty and the extension to the state-of-the-art.

7 Conclusion and Outlook

Always in motion is the future.

Yoda, from Star Wars

The forecast exponential growth of mobile wireless data traffic essentially drives enhancements of communication technology and standards. A key limiting factor is the limited resource of usable RF spectrum, which is combated by upcoming and currently developed wireless communication standards, such as 5G. A candidate technology in 5G enhancing spectral efficiency and easing spectrum usage is SIC.

In many cases, such as in-band FD and many FDD CA scenarios, the TRX's own TX signal is limiting or blocking reception by degrading RX performance, desensitizing or driving it into nonlinear operation modes. This specific scenario can be combated with SIC, since the TX signal, and its impact on the RX, is principally known to the TRX.

7.1 Mixed-Signal RF Domain Transmitter-Induced Self-Interference Cancellation

In this work, a novel fully integrated mixed-signal RF domain SIC approach has been developed and a demonstrator is implemented. The system is discussed in Chapter 4. This approach includes and combines benefits of alternative SIC approaches, amidst its own:

- cancellation in the RF domain, restoring analog RX performance,
- usage of DSP to generate the cancellation signal digitally, allowing for adaptive and tracking systems and keeping utmost flexibility,

- employing an RF-DAC to directly synthesize the analog cancellation signal in the RF domain, sparing any other analog circuitry, and
- can be easily combined with additional other SIC methods to further improve the system's cancellation performance.

To demonstrate the feasibility of this SIC solution, a fully integrated demonstrator system has been designed and implemented in a 28 nm bulk-CMOS technology. It operates from 1.4 GHz up to 2.7 GHz covering all of the LTE mid and high bands. The designed system consists of two main building blocks: the injection augmented RX, which accepts the cancellation signal, and the cancellation RF-DAC, which translates the digital cancellation signal directly into the RF domain. This work focuses primarily on the circuit design of the aforementioned blocks and necessary auxiliary circuitry. The circuit level design and implementation is detailed in Chapter 6.

A novel single-ended capacitive RF-DAC architecture, avoiding any spacious on-chip inductors, has been introduced in this work. It is a digital-like implementation, perfectly suitable for advanced nanometer CMOS processes. In addition to the converter, an ultra high regulation bandwidth LDO regulator was added to the RF-DAC to ensure high performance operation. The regulator structure features a novel frequency compensation scheme, enabling the required bandwidth and load regulation.

The implemented prototype system features several key advantages, additional to the system level benefits:

- fully integrated SIC system avoiding any external component overhead
- absence of any bulky on-chip inductors, enabling a very compact solution
- low power digital-like implementation suitable for low supply voltages, technology scaling, and portability

The feasibility of the approach is demonstrated by means of the implemented demonstrator system. Excellent performance of the cancellation RF-DAC and the entire SIC enhanced RX system is achieved.

7.2 Quadrature and Multiphase Local Oscillator Generation

In addition to the SIC system and demonstrator, a new quadrature and multiphase LO and/or clock generator architecture has been developed in this work. This circuit allows for local generation of precise LO phases, e.g. quadrature phases, at the same frequency as its input LO. This way, considerable amounts of power spent on LO distribution can be spared, especially on large TRX systems.

Two prototypes have been developed, a differential quadrature and a differential three phase LO generator respectively. The feasibility of the circuit architecture is demonstrated by these LO generator prototype circuits, which exhibit state-of-the-art performance and figures of merit.

The presented circuit architecture features key advantages, such as

- a novel open-loop feed-forward operation with low circuit complexity,
- thus not being vulnerable to stability issues common to feedback systems,
- low device count for low noise operation and low power consumption, and
- enabling digital-like implementations suitable for low supply voltages and nanometer CMOS process technology, with great portability.

7.3 List of Publications

Throughout this dissertation, the conducted research resulted in several publications:

Patent Applications

- **M. Kalcher**, D. Gruber, F. Conzatti, and P. Greco, "Multiphase Signal Generators, Frequency Multipliers, Mixed Signal Circuits, and Methods

for Generating Phase Shifted Signals," PCT Patent Application WO/2018/182585, Oct. 5, 2018
- **M. Kalcher** and D. Gruber, "Concept for a Buffered Flipped Voltage Follower and for a Low Dropout Regulator," German Patent Application 10 2018 129 910.9, Nov. 27, 2018
- D. Ponton, **M. Kalcher**, A. Paussa, E. Thaller, F. Kuttner, and D. Gruber, "Novel Signed-RFDAC Architectures Enabling Wideband and Efficient 5G Transmitters," United States Patent Application 16/364891, Mar. 26, 2019

Peer-Reviewed Journal Papers

- **M. Kalcher**, M. Fulde, and D. Gruber, "Fully-digital transmitter architectures and circuits for the next generation of wireless communications," *e & i Elektrotechnik und Informationstechnik*, vol. 135, no. 1, pp. 89–98, Feb. 1, 2018
- **M. Kalcher**, D. Gruber, and D. Ponton, "1–3 GHz Self-Aligned Open-Loop Local Quadrature Phase Generator with Phase Error Below 0.4," submitted to *Journal of Solid State Circuits*, currently under review

Contributions to Peer-Reviewed Conferences and Workshops

- **M. Kalcher**, D. Gruber, and D. Ponton, "Self-aligned open-loop local quadrature phase generator," in *ESSCIRC Conference 2016: 42nd European Solid-State Circuits Conference*, Sep. 2016, pp. 351–354
- **M. Kalcher** and D. Gruber, "CMOS Open-Loop Local Quadrature Phase Generator for 5G Applications," in *2017 Austrochip Workshop on Microelectronics (Austrochip)*, Oct. 2017, pp. 15–17
- **M. Kalcher** and D. Gruber, "Self-Aligned Open-Loop Multiphase Generator," in *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2019, pp. 1–5
- S. Trampitsch, **M. Kalcher**, D. Gruber, M. Lunglmayr, and M. Huemer, "Modeling Non-Idealities of Capacitive RF-DACs with a Switched State-Space Model," in *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2019, pp. 1–5

- **M. Kalcher**, "Local Oscillators and Quadrature Generation – Phase Noise, Jitter, and Circuits: An Introduction," Jan. 24, 2018

7.4 Outlook

The obvious next step to this work is a full experimental evaluation of the developed prototype. This includes measurements of the performance of the individual circuit blocks, e.g. the RX and the cancellation RF-DAC, and the overall system performance in complete TRX operation. Additionally to evaluating a large set of combinations of carrier frequencies, signal bandwidths, and signal types, the impact of different means of (passive) isolation preceding the RX, e.g. dedicated TX and RX antennas, duplexers, circulators, etc., on SIC and RX performance are to be investigated.

Furthermore, the demonstrator provides a platform to test different DSP algorithms to generate the cancellation signals. The memory based system, detailed in Chapter 4, offers utmost flexibility to evaluate different approaches, e.g. the various options and variants of adaptive algorithms. Apart from performing linear cancellation, also TX-induced nonlinear interfering signal components can be possibly canceled. The developed prototype offers a suitable testbed for investigations towards this direction.

The demonstrator can also be integrated in systems with additional SIC methods, e.g. (external) RF domain and/or fully digital approaches. Such a system is a candidate for enabling in-band FD TRXs. Also for such a scenario, the developed prototype offers vast flexibility suitable for numerous analyses.

Finally, commercial success of SIC technology does not depend on such advances of the state-of-the-art alone. Customer interest and demand of advanced 5G technology, e.g. of cellular operators, must drive development to provide robust solutions that also withstand conditions experienced out in the field that leads to adoption in cutting edge products.

List of Abbreviations

3G third generation.
4G fourth generation.
5G fifth generation.
5G-NR 5G new radio.

AC alternating current.
ACLR adjacent channel leakage ratio.
ADC analog-to-digital converter.

BB baseband.
BER bit error rate.
BPF band pass filter.

CA carrier aggregation.
CAGR compound annual growth rate.
CDMA code division multiple access.
CG common gate.
CMOS complementary metal-oxide-semiconductor.
CS common source.
CW continuous wave.

DAC digital-to-analog converter.
DC direct current.
DFT discrete Fourier transform.
DL downlink.
DNL differential nonlinearity.
DPD digital pre-distortion.
DR dynamic range.
DSP digital signal processing.

EDGE Enhanced Data Rates for GSM Evolution.

ESD electrostatic discharge.
EVDO Evolution-Data Optimized.
EVM error vector magnitude.

FD full duplex.
FDD frequency division duplex.
FIR finite impulse response.
FPGA field-programmable gate array.
FVF flipped voltage follower.
FWA fixed wireless access.

GPRS General Packet Radio Service.
GSM Global System for Mobile Communications.

HSUPA High Speed Uplink Packet Access.

IF intermediate frequency.
IIP3 third order input referred intercept point.
IL insertion loss.
IM2 second-order intermodulation.
IM3 third-order intermodulation.
IMD intermodulation distortion.
IMD2 second-order intermodulation distortion.
INL integral nonlinearity.
IoT internet of things.
IP intercept point.
ISM industrial, scientific, and medical.

LDO low-dropout regulator.
LMS least mean squares.
LNA low-noise amplifier.
LO local oscillator.
LS least squares.
LTE Long-Term Evolution.

MOS metal-oxide-semiconductor.

NF noise figure.
NMOS N-type metal-oxide-semiconductor.

OOB out-of-band.
OSR oversampling ratio.

PA power amplifier.
PAPR peak-to-average power ratio.
PCB printed circuit board.
PMOS P-type metal-oxide-semiconductor.
PPF polyphase filter.
PSRR power supply rejection ratio.
PVT process, supply voltage, and temperature.

QPSK quadrature phase shift keying.

RF radio-frequency.
RF-DAC radio-frequency digital-to-analog converter.
RLS recursive least squares.
RMS root mean square.
RX receiver.

SAW surface acoustic wave.
SCPA switched-capacitor power amplifier.
SDR signal-to-distortion ratio.
SFDR spurious-free dynamic range.
SI self-interference.
SIC self-interference cancellation.
SINR signal-to-interference-and-noise ratio.
SNR signal-to-noise ratio.
SSF super source follower.

TDD time division duplex.
TIA transimpedance amplifier.
TRX transceiver.
TX transmitter.

UL uplink.
UMTS Universal Mobile Telecommunications System.

VGA variable gain amplifier.
VSWR voltage standing wave ratio.

WCDMA wideband code division multiple access.
Wi-Fi Wi-Fi.

ZOH zero-order hold.

Bibliography

[1] "Cisco Visual Networking Index: Forecast and Trends, 2017–2022." [Online]. Available: https://www.cisco.com/c/en/us/solutions/collateral/service-provider/visual-networking-index-vni/white-paper-c11-741490.pdf (cit. on p. 1).

[2] "Ericsson Mobility Report November 2018," 2018, p. 32. [Online]. Available: https://www.ericsson.com/en/mobility-report/reports/november-2018 (visited on 04/23/2019) (cit. on p. 1).

[3] J. M. Voas, "Networks of 'Things' — NIST," NIST, NIST Pubs 800-183, Jul. 28, 2016. [Online]. Available: https://www.nist.gov/publications/networks-things (visited on 01/30/2019) (cit. on p. 1).

[4] G. P. Fettweis, "5G and the future of IoT," in *ESSCIRC Conference 2016: 42nd European Solid-State Circuits Conference*, Sep. 2016, pp. 21–24 (cit. on pp. 1, 7).

[5] Z. Zhang, X. Chai, K. Long, A. V. Vasilakos, and L. Hanzo, "Full duplex techniques for 5G networks: Self-interference cancellation, protocol design, and relay selection," *IEEE Communications Magazine*, vol. 53, no. 5, pp. 128–137, May 2015 (cit. on pp. 1, 13).

[6] S. Hong, J. Brand, J. I. Choi, M. Jain, J. Mehlman, S. Katti, and P. Levis, "Applications of self-interference cancellation in 5G and beyond," *IEEE Communications Magazine*, vol. 52, no. 2, pp. 114–121, Feb. 2014 (cit. on pp. 1, 2, 13, 14).

[7] Y. Kwon, D. K. Park, and H. Rhee, "Spectrum fragmentation: Causes, measures and applications," *Telecommunications Policy*, Optimising Spectrum Use, vol. 41, no. 5, pp. 447–459, Jun. 1, 2017 (cit. on pp. 1, 9).

[8] W. Schacherbauer, T. Ostertag, C. C. W. Ruppel, A. Springer, and R. Weigel, "An Interference Cancellation Technique for the Use in Multiband Software Radio Frontend Design," in *2000 30th European Microwave Conference*, Oct. 2000, pp. 1–4 (cit. on pp. 2, 37, 38, 56).

[9] M. Kalcher, M. Fulde, and D. Gruber, "Fully-digital transmitter architectures and circuits for the next generation of wireless communications," *e & i Elektrotechnik und Informationstechnik*, vol. 135, no. 1, pp. 89–98, Feb. 1, 2018 (cit. on pp. 5, 39, 56, 58, 112–114, 206, 210).

[10] F. Ellinger, "Transceiver Architectures," in *Radio Frequency Integrated Circuits and Technologies*, Springer, Berlin, Heidelberg, 2008, pp. 41–60 (cit. on p. 5).

[11] P. Warder and A. Link, "Golden Age for Filter Design: Innovative and Proven Approaches for Acoustic Filter, Duplexer, and Multiplexer Design," *IEEE Microwave Magazine*, vol. 16, no. 7, pp. 60–72, Aug. 2015 (cit. on p. 5).

[12] A. Nordrum and K. Clark. (Jan. 27, 2017). Everything You Need to Know About 5G (cit. on p. 7).

[13] Z. Ma, Z. Zhang, Z. Ding, P. Fan, and H. Li, "Key techniques for 5G wireless communications: Network architecture, physical layer, and MAC layer perspectives," *Science China Information Sciences*, vol. 58, no. 4, pp. 1–20, Apr. 1, 2015 (cit. on p. 7).

[14] J. Andrews, S. Buzzi, W. Choi, S. Hanly, A. Lozano, A. Soong, and J. Zhang, "What Will 5G Be?" *IEEE Journal on Selected Areas in Communications*, vol. 32, no. 6, pp. 1065–1082, Jun. 2014 (cit. on p. 7).

[15] C.-L. I, M. Uusitalo, and K. Moessner, "The 5G Huddle," *IEEE Vehicular Technology Magazine*, vol. 10, no. 1, pp. 28–31, Mar. 2015 (cit. on p. 7).

[16] Z. Zhang, X. Chai, K. Long, A. Vasilakos, and L. Hanzo, "Full duplex techniques for 5G networks: Self-interference cancellation, protocol design, and relay selection," *IEEE Communications Magazine*, vol. 53, no. 5, pp. 128–137, May 2015 (cit. on p. 7).

[17] J. I. Choi, M. Jain, K. Srinivasan, P. Levis, and S. Katti, "Achieving Single Channel, Full Duplex Wireless Communication," in *Proceedings of the Sixteenth Annual International Conference on Mobile Computing and Networking*, ser. MobiCom '10, New York, NY, USA: ACM, 2010, pp. 1–12 (cit. on pp. 7, 46, 47).

[18] M. Duarte, C. Dick, and A. Sabharwal, "Experiment-Driven Characterization of Full-Duplex Wireless Systems," *IEEE Transactions on Wireless Communications*, vol. 11, no. 12, pp. 4296–4307, Dec. 2012 (cit. on pp. 7, 46, 56).

[19] A. Goldsmith, *Wireless Communications*. Cambridge University Press, Aug. 8, 2005, 676 pp. (cit. on p. 7).

[20] E. Dahlman, S. Parkvall, and J. Skold, *4G: LTE/LTE-Advanced for Mobile Broadband*. Academic Press, Oct. 7, 2013, 537 pp. (cit. on pp. 7–9).

[21] A. Gebhard, R. S. Kanumalli, B. Neurauter, and M. Huemer, "Adaptive self-interference cancelation in LTE-A carrier aggregation FDD direct-conversion transceivers," in *2016 IEEE Sensor Array and Multichannel Signal Processing Workshop (SAM)*, Jul. 2016, pp. 1–5 (cit. on pp. 8, 35).

[22] *LTE; Evolved Universal Terrestrial Radio Access (E-UTRA); User Equipment (UE) radio transmission and reception (3GPP TS 36.101 version 14.5.0 Release 14)*, Nov. 2017 (cit. on pp. 8, 9).

[23] R. S. Kanumalli, T. Buckel, C. Preissl, P. Preyler, A. Gebhard, C. Motz, J. Markovic, D. Hamidovic, E. Hager, H. Pretl, A. Springer, and M. Huemer, "Digitally-intensive transceivers for future mobile communications—emerging trends and challenges," *e & i Elektrotechnik und Informationstechnik*, vol. 135, no. 1, pp. 30–39, Feb. 1, 2018 (cit. on pp. 9, 34, 35).

[24] R. S. Kanumalli, A. Gebhard, A. Elmaghraby, A. Mayer, D. Schwartz, and M. Huemer, "Active Digital Cancellation of Transmitter Induced Modulated Spur Interference in 4G LTE Carrier Aggregation Transceivers," in *2016 IEEE 83rd Vehicular Technology Conference (VTC Spring)*, May 2016, pp. 1–5 (cit. on pp. 9, 10, 35).

[25] G. Yuan, X. Zhang, W. Wang, and Y. Yang, "Carrier aggregation for LTE-advanced mobile communication systems," *IEEE Communications Magazine*, vol. 48, no. 2, pp. 88–93, Feb. 2010 (cit. on p. 9).

[26] M. Iwamura, K. Etemad, M. h Fong, R. Nory, and R. Love, "Carrier aggregation framework in 3GPP LTE-advanced [WiMAX/LTE Update]," *IEEE Communications Magazine*, vol. 48, no. 8, pp. 60–67, Aug. 2010 (cit. on p. 9).

[27] K. I. Pedersen, F. Frederiksen, C. Rosa, H. Nguyen, L. G. U. Garcia, and Y. Wang, "Carrier aggregation for LTE-advanced: Functionality and performance aspects," *IEEE Communications Magazine*, vol. 49, no. 6, pp. 89–95, Jun. 2011 (cit. on p. 9).

[28] C. S. Park, L. Sundström, A. Wallén, and A. Khayrallah, "Carrier aggregation for LTE-advanced: Design challenges of terminals," *IEEE Communications Magazine*, vol. 51, no. 12, pp. 76–84, Dec. 2013 (cit. on p. 10).

[29] A. Elmaghraby, R. S. Kanumalli, W. Schelmbauer, A. Mayer, S. Herzinger, D. Schwartz, M. Huemer, and R. Weigel, "A Mixed-Signal Technique for TX-Induced Modulated Spur Cancellation in LTE-CA Receivers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. PP, no. 99, pp. 1–14, 2018 (cit. on pp. 10, 41).

[30] S. Sadjina, K. Dufrene, R. S. Kanumalli, M. Huemer, and H. Pretl, "A Circuit Technique for Blocker-Induced Modulated Spur Cancellation in 4G LTE Carrier Aggregation Transceivers," in *2017 Austrochip Workshop on Microelectronics (Austrochip)*, Oct. 2017, pp. 23–28 (cit. on pp. 10, 41, 42).

[31] L. Miller, *Carrier Aggregation Fundamentals For Dummies*. 2016. [Online]. Available: `https://www.qorvo.com/design-hub/ebooks/carrier-aggregation-for-dummies` (visited on 03/08/2018) (cit. on p. 12).

[32] M. Z. Waheed, D. Korpi, A. Kiayani, L. Anttila, and M. Valkama, "Digital self-interference cancellation in inter-band carrier aggregation transceivers: Algorithm and digital implementation perspectives," in *2017 IEEE International Workshop on Signal Processing Systems (SiPS)*, Oct. 2017, pp. 1–5 (cit. on pp. 12, 36).

[33] D. Bharadia, E. McMilin, and S. Katti, "Full Duplex Radios," in *Proceedings of the ACM SIGCOMM 2013 Conference on SIGCOMM*, ser. SIGCOMM '13, New York, NY, USA: ACM, 2013, pp. 375–386 (cit. on pp. 13, 14).

[34] M. Fulde, A. Belitzer, Z. Boos, M. Bruennert, J. Fritzin, H. Geltinger, M. Groinig, D. Gruber, S. Gruenberger, T. Hartig, V. Kampus, B. Kapfelsberger, F. Kuttner, S. Leuschner, T. Maletz, A. Menkhoff, J. Moreira, A. Paussa, D. Ponton, H. Pretl, D. Sira, U. Steinacker, and N. Stevanovic, "13.2 A digital multimode polar transmitter supporting 40MHz LTE Carrier Aggregation in 28nm CMOS," in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2017, pp. 218–219 (cit. on pp. 14, 56, 58, 145, 150, 155).

[35] F. Conzatti, L. Dorrer, P. Torta, C. Kropf, D. Patzold, J. S. P. Garcia, V. Rallos, and N. Schembera, "A CT $\Delta\Sigma$ ADC with 9/50 MHz BW achieving 73/71 dB DR designed for robust blocker tolerance in 14 nm FinFET," in *ESSCIRC 2017 - 43rd IEEE European Solid State Circuits Conference*, Sep. 2017, pp. 139–142 (cit. on pp. 14, 56).

[36] G. Chen, Y. Gong, P. Xiao, and J. A. Chambers, "Physical Layer Network Security in the Full-Duplex Relay System," *IEEE Transactions on Information Forensics and Security*, vol. 10, no. 3, pp. 574–583, Mar. 2015 (cit. on p. 15).

[37] S. Beck, S. T. Kim, K. Lim, M. M. Tentzeris, and J. Laskar, "A multiband WCDMA SAW-less receivers with frequency selective feedback loop," in *2011 IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug. 2011, pp. 1–4 (cit. on p. 19).

[38] H. Hedayati, W. F. A. Lau, N. Kim, V. Aparin, and K. Entesari, "A 1.8 dB NF Blocker-Filtering Noise-Canceling Wideband Receiver With Shared TIA in 40 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 5, pp. 1148–1164, May 2015 (cit. on p. 19).

[39] M. N. Hasan, Q. J. Gu, and X. Liu, "Tunable Blocker-Tolerant On-Chip Radio-Frequency Front-End Filter With Dual Adaptive Transmission Zeros for Software-Defined Radio Applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 12, pp. 4419–4433, Dec. 2016 (cit. on p. 19).

[40] M. Mikhemar, H. Darabi, and A. Abidi, "A tunable integrated duplexer with 50 dB isolation in 40 nm CMOS," in *2009 IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, Feb. 2009, 386–387, 387a (cit. on p. 19).

[41] M. Mikhemar, H. Darabi, and A. A. Abidi, "A Multiband RF Antenna Duplexer on CMOS: Design and Performance," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 9, pp. 2067–2077, Sep. 2013 (cit. on p. 19).

[42] S. H. Abdelhalem, P. S. Gudem, and L. E. Larson, "Hybrid transformer-based tunable integrated duplexer with antenna impedance tracking loop," in *Proceedings of the IEEE 2013 Custom Integrated Circuits Conference*, Sep. 2013, pp. 1–4 (cit. on p. 19).

[43] M. Elkholy, M. Mikhemar, H. Darabi, and K. Entesari, "Low-Loss Integrated Passive CMOS Electrical Balance Duplexers With Single-Ended LNA," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 5, pp. 1544–1559, May 2016 (cit. on p. 19).

[44] S. Kannangara and M. Faulkner, "Adaptive duplexer for multiband transreceiver," in *Radio and Wireless Conference, 2003. RAWCON '03. Proceedings*, Aug. 2003, pp. 381–384 (cit. on p. 20).

[45] ——, "Analysis of an Adaptive Wideband Duplexer With Double-Loop Cancellation," *IEEE Transactions on Vehicular Technology*, vol. 56, no. 4, pp. 1971–1982, Jul. 2007 (cit. on p. 20).

[46] T. O'Sullivan, R. A. York, B. Noren, and P. M. Asbeck, "Adaptive duplexer implemented using single-path and multipath feedforward techniques with BST phase shifters," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 1, pp. 106–114, Jan. 2005 (cit. on p. 20).

[47] R. Eslampanah, S. Ahmed, M. Williamson, J.-M. Redouté, and M. Faulkner, "Adaptive Duplexing for Transceivers Supporting Aggregated Transmissions," *IEEE Transactions on Vehicular Technology*, vol. PP, no. 99, pp. 1–1, 2015 (cit. on p. 21).

[48] V. Aparin, G. Ballantyne, C. Persico, and A. Cicalini, "An integrated LMS adaptive filter of TX leakage for CDMA receiver front ends," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 5, pp. 1171–1182, May 2006 (cit. on pp. 21, 22).

[49] H. Kim, S. Woo, S. Jung, and K.-H. Lee, "A CMOS Transmitter Leakage Canceller for WCDMA Applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 9, pp. 3373–3380, Sep. 2013 (cit. on pp. 21–24).

[50] J. Zhou, A. Chakrabarti, P. R. Kinget, and H. Krishnaswamy, "Low-Noise Active Cancellation of Transmitter Leakage and Transmitter Noise in Broadband Wireless Receivers for FDD/Co-Existence," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 12, pp. 3046–3062, Dec. 2014 (cit. on pp. 23, 24, 27, 50).

[51] J. Zhou, P. R. Kinget, and H. Krishnaswamy, "20.6 A blocker-resilient wideband receiver with low-noise active two-point cancellation of $>$ 0 dBm TX leakage and TX noise in RX band for FDD/Co-existence," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014 IEEE International*, Feb. 2014, pp. 352–353 (cit. on pp. 23, 24).

[52] F. Bruccoleri, E. Klumperink, and B. Nauta, "Wide-band CMOS low-noise amplifier exploiting thermal noise canceling," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 2, pp. 275–282, Feb. 2004 (cit. on pp. 23, 24, 50).

[53] S. Blaakmeer, E. Klumperink, D. Leenaerts, and B. Nauta, "Wideband Balun-LNA With Simultaneous Output Balancing, Noise-Canceling and Distortion-Canceling," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 6, pp. 1341–1350, Jun. 2008 (cit. on pp. 23, 24, 50).

[54] J. Li, R. Shu, and Q. J. Gu, "Passive interferometer for wideband and linear transmitter leakage cancellation," in *2015 Asia-Pacific Microwave Conference (APMC)*, vol. 1, Dec. 2015, pp. 1–3 (cit. on pp. 24, 25).

[55] T. Zhang, A. R. Suvarna, V. Bhagavatula, and J. C. Rudell, "An Integrated CMOS Passive Self-Interference Mitigation Technique for FDD Radios," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 5, pp. 1176–1188, May 2015 (cit. on pp. 25, 26).

[56] D. Montanari, G. Castellano, E. Kargaran, G. Pini, S. Tijani, D. D. Caro, A. G. M. Strollo, D. Manstretta, and R. Castello, "An FDD Wireless Diversity Receiver With Transmitter Leakage Cancellation in Transmit and Receive Bands," *IEEE Journal of Solid-State Circuits*, pp. 1–15, 2018 (cit. on pp. 26, 27, 43).

[57] E. Kargaran, S. Tijani, G. Pini, D. Manstretta, and R. Castello, "Low power wideband receiver with RF Self-Interference Cancellation for Full-Duplex and FDD wireless Diversity," in *2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Jun. 2017, pp. 348–351 (cit. on pp. 26, 27).

[58] J. Zhou, T.-H. Chuang, T. Dinc, and H. Krishnaswamy, "Integrated Wideband Self-Interference Cancellation in the RF Domain for FDD and Full-Duplex Wireless," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 12, pp. 3015–3031, Dec. 2015 (cit. on pp. 27, 28).

[59] ——, "19.1 Receiver with $>$ 20 MHz bandwidth self-interference cancellation suitable for FDD, co-existence and full-duplex applications," in *2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, Feb. 2015, pp. 1–3 (cit. on pp. 27, 28).

[60] L. E. Franks and I. W. Sandberg, "An alternative approach to the realization of network transfer functions: The N-path filter," *The Bell System Technical Journal*, vol. 39, no. 5, pp. 1321–1350, Sep. 1960 (cit. on pp. 28, 40, 43, 93).

[61] A. Mirzaei, H. Darabi, A. Yazdi, Z. Zhou, E. Chang, and P. Suri, "A 65 nm CMOS Quad-Band SAW-Less Receiver SoC for GSM/GPRS/EDGE," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 4, pp. 950–964, Apr. 2011 (cit. on pp. 28, 40, 93).

[62] A. Ghaffari, E. A. M. Klumperink, M. C. M. Soer, and B. Nauta, "Tunable High-Q N-Path Band-Pass Filters: Modeling and Verification," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 5, pp. 998–1010, May 2011 (cit. on pp. 28, 40, 43, 93).

[63] S. Tijani and D. Manstretta, "A Low-Power Active Self-Interference Cancellation Technique for SAW-Less FDD and Full-Duplex Receivers," *Journal of Low Power Electronics and Applications*, vol. 7, no. 4, p. 27, Nov. 13, 2017 (cit. on pp. 29, 30).

[64] H. Yüksel, D. Yang, Z. Boynton, C. Lee, T. Tapen, A. Molnar, and A. Apsel, "A Wideband Fully Integrated Software-Defined Transceiver for FDD and TDD Operation," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 5, pp. 1274–1285, May 2017 (cit. on pp. 29–31).

[65] D. Yang, H. Yüksel, C. Newman, C. Lee, Z. Boynton, N. Paya, M. Pedrone, A. Apsel, and A. Molnar, "A fully integrated Software-Defined FDD transceiver tunable from 0.3-to-1.6 GHz," in *2016 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, May 2016, pp. 334–337 (cit. on pp. 29, 30).

[66] S. O. Haykin, *Adaptive Filter Theory*, 5 edition. Upper Saddle River, New Jersey: Pearson, Jun. 2, 2013, 912 pp. (cit. on p. 32).

[67] A. Frotzscher and G. Fettweis, "A Stochastic Gradient LMS Algorithm for Digital Compensation of Tx Leakage in Zero-IF-Receivers," in *IEEE Vehicular Technology Conference, 2008. VTC Spring 2008*, May 2008, pp. 1067–1071 (cit. on p. 33).

[68] A. Frotzscher, *Schätzung und Kompensation des Senderübersprechens in Frequenzduplex-Sendeempfängern*. Jörg Vogt Verlag, 2010, 203 pp. (cit. on p. 33).

[69] M. Kahrizi, J. Komaili, J. Vasa, and D. Agahi, "Adaptive filtering using LMS for digital TX IM2 cancellation in WCDMA receiver," in *2008 IEEE Radio and Wireless Symposium*, Jan. 2008, pp. 519–522 (cit. on p. 33).

[70] C. Lederer and M. Huemer, "LMS based digital cancellation of second-order TX intermodulation products in homodyne receivers," in *2011 IEEE Radio and Wireless Symposium (RWS)*, Jan. 2011, pp. 207–210 (cit. on p. 33).

[71] T. I. Laakso, V. Valimaki, M. Karjalainen, and U. K. Laine, "Splitting the unit delay [FIR/all pass filters design]," *IEEE Signal Processing Magazine*, vol. 13, no. 1, pp. 30–60, Jan. 1996 (cit. on p. 33).

[72] A. Kiayani, L. Anttila, and M. Valkama, "Modeling and dynamic cancellation of TX-RX leakage in FDD transceivers," in *2013 IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug. 2013, pp. 1089–1094 (cit. on p. 33).

[73] V. Volterra, *Theory of Functionals of Integral and Integro-Differential Equations*. Dover Publ., 1959, 316 pp. (cit. on p. 33).

[74] A. Gebhard, C. Motz, R. S. Kanumalli, H. Pretl, and M. Huemer, "Nonlinear least-mean-squares type algorithm for second-order interference cancellation in LTE-A RF transceivers," in *2017 51st Asilomar Conference on Signals, Systems, and Computers*, Oct. 2017, pp. 802–807 (cit. on p. 34).

[75] R. Gerzaguet, L. Ros, F. Belvèze, and J.-M. Brossier, "Performance of a digital transmitter leakage LMS-based cancellation algorithm for multi-standard radio-frequency transceivers," *Digital Signal Processing*, vol. 51, pp. 35–46, Apr. 1, 2016 (cit. on p. 34).

[76] R. Gerzaguet, L. Ros, F. Belveze, and J. M. Brossier, "Joint estimation of complex gain and fractional delay for Tx leakage compensation in FDD transceivers," in *2014 21st IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Dec. 2014, pp. 80–83 (cit. on p. 34).

[77] P. L. Lui, "Passive intermodulation interference in communication systems," *Electronics Communication Engineering Journal*, vol. 2, no. 3, pp. 109–118, Jun. 1990 (cit. on p. 34).

[78] L. Larson, D. Kimball, P. Asbeck, P. Draxler, J. Deng, and M. Li, "Digital predistortion techniques for linearized power amplifiers," in *2006 Asia-Pacific Microwave Conference*, Dec. 2006, pp. 1048–1051 (cit. on p. 34).

[79] P. Desgreys, V. N. Manyam, K. Tchambake, D. K. G. Pham, and C. Jabbour, "Wideband power amplifier predistortion: Trends, challenges and solutions," in *2017 IEEE 12th International Conference on ASIC (ASICON)*, Oct. 2017, pp. 100–103 (cit. on pp. 34, 62).

[80] M. Omer, R. Rimini, P. Heidmann, and J. S. Kenney, "A compensation scheme to allow full duplex operation in the presence of highly nonlinear microwave components for 4G systems," in *2011 IEEE MTT-S International Microwave Symposium*, Jun. 2011, pp. 1–4 (cit. on p. 34).

[81] K. Narendra and P. Gallman, "An iterative method for the identification of nonlinear systems using a Hammerstein model," *IEEE Transactions on Automatic Control*, vol. 11, no. 3, pp. 546–550, Jul. 1966 (cit. on p. 34).

[82] P. Sliwinski, *Nonlinear System Identification by Haar Wavelets*, ser. Lecture Notes in Statistics. Berlin Heidelberg: Springer-Verlag, 2013 (cit. on p. 34).

[83] A. Kiayani, L. Anttila, and M. Valkama, "Digital Suppression of Power Amplifier Spurious Emissions at Receiver Band in FDD Transceivers," *IEEE Signal Processing Letters*, vol. 21, no. 1, pp. 69–73, Jan. 2014 (cit. on p. 35).

[84] M. Omer, R. Rimini, P. Heidmann, and J. S. Kenney, "All digital compensation scheme for spur induced transmit self-jamming in multi-receiver RF frond-ends," in *2012 IEEE/MTT-S International Microwave Symposium Digest*, Jun. 2012, pp. 1–3 (cit. on p. 35).

[85] H. T. Dabag, H. Gheidi, P. Gudem, and P. M. Asbeck, "All-digital cancellation technique to mitigate self-jamming in uplink carrier aggregation in cellular handsets," in *2013 IEEE MTT-S International Microwave Symposium Digest (MTT)*, Jun. 2013, pp. 1–3 (cit. on p. 36).

[86] H. T. Dabag, H. Gheidi, S. Farsi, P. S. Gudem, and P. M. Asbeck, "All-Digital Cancellation Technique to Mitigate Receiver Desensitization in Uplink Carrier Aggregation in Cellular Handsets," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 12, pp. 4754–4765, Dec. 2013 (cit. on p. 36).

[87] H. Gheidi, H. T. Dabag, Y. Liu, P. M. Asbeck, and P. Gudem, "Digital cancellation technique to mitigate receiver desensitization in cellular handsets operating in carrier aggregation mode with multiple uplinks and multiple downlinks," in *2015 IEEE Radio and Wireless Symposium (RWS)*, Jan. 2015, pp. 221–224 (cit. on p. 36).

[88] A. Kiayani, M. Abdelaziz, L. Anttila, V. Lehtinen, and M. Valkama, "Digital Mitigation of Transmitter-Induced Receiver Desensitization in Carrier Aggregation FDD Transceivers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 11, pp. 3608–3623, Nov. 2015 (cit. on p. 36).

[89] C. Yu and A. Zhu, "Modeling and suppression of transmitter leakage in concurrent dual-band transceivers with carrier aggregation," in *2015 IEEE MTT-S International Microwave Symposium*, May 2015, pp. 1–3 (cit. on p. 36).

[90] C. Yu, W. Cao, Y. Guo, and A. Zhu, "Digital Compensation for Transmitter Leakage in Non-Contiguous Carrier Aggregation Applications With FPGA Implementation," *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 12, pp. 4306–4318, Dec. 2015 (cit. on p. 36).

[91] W. Schacherbauer, A. Springer, T. Ostertag, C. C. W. Ruppel, and R. Weigel, "A flexible multiband frontend for software radios using high IF and active interference cancellation," in *2001 IEEE MTT-S International Microwave Sympsoium Digest (Cat. No.01CH37157)*, vol. 2, May 2001, 1085–1088 vol.2 (cit. on pp. 37, 38, 56).

[92] W. Schacherbauer, "Realisierung eines flexiblen Hochfrequenz-Frontends für Multistandard-Mobilfunkanwendungen," Johannes Kepler Universität Linz, Linz, Oct. 2001, 177 pp. (cit. on pp. 37, 38, 56, 63, 64).

[93] A. Kiayani, M. Z. Waheed, L. Anttila, M. Abdelaziz, D. Korpi, V. Syrjälä, M. Kosunen, K. Stadius, J. Ryynänen, and M. Valkama, "Adaptive Nonlinear RF Cancellation for Improved Isolation in Simultaneous Transmit–Receive Systems," *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, no. 5, pp. 2299–2312, May 2018 (cit. on p. 37).

[94] A. Kiayani, L. Anttila, and M. Valkama, "Active RF cancellation of nonlinear TX leakage in FDD transceivers," in *2016 IEEE Global Conference on Signal and Information Processing (GlobalSIP)*, Dec. 2016, pp. 689–693 (cit. on p. 37).

[95] L. Ding, G. T. Zhou, D. R. Morgan, Z. Ma, J. S. Kenney, J. Kim, and C. R. Giardina, "A robust digital baseband predistorter constructed using memory polynomials," *IEEE Transactions on Communications*, vol. 52, no. 1, pp. 159–165, Jan. 2004 (cit. on p. 37).

[96] M. Isaksson, D. Wisell, and D. Ronnow, "A comparative analysis of behavioral models for RF power amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 1, pp. 348–359, Jan. 2006 (cit. on p. 37).

[97] L. Calderin, S. Ramakrishnan, A. Puglielli, E. Alon, B. Nikolić, and A. M. Niknejad, "Analysis and Design of Integrated Active Cancellation Transceiver for Frequency Division Duplex Systems," *IEEE Jour-*

nal of Solid-State Circuits, vol. 52, no. 8, pp. 2038–2054, Aug. 2017 (cit. on pp. 38, 39).

[98] S. Ramakrishnan, L. Calderin, A. Puglielli, E. Alon, A. Niknejad, and B. Nikolić, "A 65nm CMOS transceiver with integrated active cancellation supporting FDD from 1GHz to 1.8GHz at +12.6dBm TX power leakage," in *2016 IEEE Symposium on VLSI Circuits (VLSI-Circuits)*, Jun. 2016, pp. 1–2 (cit. on pp. 38, 39).

[99] S. Ramakrishnan, L. Calderin, A. Niknejad, and B. Nikolić, "An FD/FDD transceiver with RX band thermal, quantization, and phase noise rejection and >64dB TX signal cancellation," in *2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Jun. 2017, pp. 352–355 (cit. on pp. 38, 39).

[100] S.-M. Yoo, J. Walling, E. C. Woo, B. Jann, and D. Allstot, "A Switched-Capacitor RF Power Amplifier," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 12, pp. 2977–2987, Dec. 2011 (cit. on pp. 38, 56, 58, 87, 112, 114, 115, 134).

[101] A. Mirzaei, M. Mikhemar, D. Murphy, and H. Darabi, "A 2 dB NF Receiver With 10 mA Battery Current Suitable for Coexistence Applications," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 4, pp. 972–983, Apr. 2014 (cit. on p. 40).

[102] A. Elmaghraby, *Transmitter Leakage Cancellation in Cellular Handset Receivers*. München: Dr. Hut, Jul. 18, 2016, 140 pp. (cit. on p. 41).

[103] S. Sadjina, K. Dufrêne, R. S. Kanumalli, M. Huemer, and H. Pretl, "Interference mitigation in LTE-CA FDD based on mixed-signal widely linear cancellation," in *2018 22nd International Microwave and Radar Conference (MIKON)*, May 2018, pp. 558–561 (cit. on p. 41).

[104] S. Sadjina, R. S. Kanumalli, A. Gebhard, K. Dufrêne, M. Huemer, and H. Pretl, "A Mixed-Signal Circuit Technique for Cancellation of Interferers Modulated by LO Phase-Noise in 4G/5G CA Transceivers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 11, pp. 3745–3755, Nov. 2018 (cit. on pp. 41, 117).

[105] D. Montanari, D. Manstretta, R. Castello, and G. Castellano, "A 0.7 – 2 GHz auxiliary receiver with enhanced compression for SAW-less FDD," in *ESSCIRC 2017 - 43rd IEEE European Solid State Circuits Conference*, Sep. 2017, pp. 27–30 (cit. on p. 43).

[106] G. R. Kenworthy, "Self-cancelling full-duplex RF communication system," U.S. Patent 5691978A, Nov. 25, 1997 (cit. on p. 45).

[107] S. Chen, M. A. Beach, and J. P. McGeehan, "Division-free duplex for wireless applications," *Electronics Letters*, vol. 34, no. 2, pp. 147–148, Jan. 1998 (cit. on pp. 45, 46).

[108] A. C. V. Gummalla and J. O. Limb, "Receiver architecture for high-speed wireless LAN protocols," in *Gateway to 21st Century Communications Village. VTC 1999-Fall. IEEE VTS 50th Vehicular Technology Conference (Cat. No.99CH36324)*, vol. 2, 1999, 1207–1211 vol.2 (cit. on p. 46).

[109] F. Tobagi and L. Kleinrock, "Packet Switching in Radio Channels: Part II - The Hidden Terminal Problem in Carrier Sense Multiple-Access and the Busy-Tone Solution," *IEEE Transactions on Communications*, vol. 23, no. 12, pp. 1417–1433, Dec. 1975 (cit. on p. 46).

[110] A. C. V. Gummalla and J. O. Limb, "Design of an access mechanism for a high speed distributed wireless LAN," *IEEE Journal on Selected Areas in Communications*, vol. 18, no. 9, pp. 1740–1750, Sep. 2000 (cit. on p. 46).

[111] B. Radunovic, D. Gunawardena, P. Key, A. Proutiere, N. Singh, H. V. Balan, and G. DeJean, "Rethinking Indoor Wireless: Low Power, Low Frequency, Full-duplex," *Microsoft Research*, Jul. 24, 2009. [Online]. Available: `https://www.microsoft.com/en-us/research/publication/rethinking-indoor-wireless-low-power-low-frequency-full-duplex/` (visited on 06/24/2018) (cit. on p. 46).

[112] A. Raghavan, E. Gebara, E. M. Tentzeris, and J. Laskar, "Analysis and design of an interference canceller for collocated radios," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 11, pp. 3498–3508, Nov. 2005 (cit. on p. 46).

[113] M. Jain, J. I. Choi, T. Kim, D. Bharadia, S. Seth, K. Srinivasan, P. Levis, S. Katti, and P. Sinha, "Practical, Real-time, Full Duplex Wireless," in *Proceedings of the 17th Annual International Conference on Mobile Computing and Networking*, ser. MobiCom '11, New York, NY, USA: ACM, 2011, pp. 301–312 (cit. on p. 46).

[114] M. Duarte and A. Sabharwal, "Full-duplex wireless communications using off-the-shelf radios: Feasibility and first results," in *2010 Conference Record of the Forty Fourth Asilomar Conference on Signals, Systems and Computers*, Nov. 2010, pp. 1558–1562 (cit. on pp. 46, 48, 56).

[115] S. S. Hong, J. Mehlman, and S. Katti, "Picasso: Flexible RF and Spectrum Slicing," *SIGCOMM Comput. Commun. Rev.*, vol. 42, no. 4, pp. 37–48, Aug. 2012 (cit. on pp. 47, 48).

[116] S. Hong, J. Mehlman, and S. Katti, "Picasso: Full Duplex Signal Shaping to Exploit Fragmented Spectrum," in *Proceedings of the 10th ACM Workshop on Hot Topics in Networks*, ser. HotNets-X, New York, NY, USA: ACM, 2011, 16:1–16:6 (cit. on p. 47).

[117] Y.-S. Choi and H. Shirani-Mehr, "Simultaneous Transmission and Reception: Algorithm, Design and System Level Performance," *IEEE Transactions on Wireless Communications*, vol. 12, no. 12, pp. 5992–6010, Dec. 2013 (cit. on p. 49).

[118] D. Korpi, Y. S. Choi, T. Huusari, L. Anttila, S. Talwar, and M. Valkama, "Adaptive Nonlinear Digital Self-Interference Cancellation for Mobile Inband Full-Duplex Radio: Algorithms and RF Measurements," in *2015 IEEE Global Communications Conference (GLOBECOM)*, Dec. 2015, pp. 1–7 (cit. on p. 49).

[119] T. Huusari, Y.-S. Choi, P. Liikkanen, D. Korpi, S. Talwar, and M. Valkama, "Wideband Self-Adaptive RF Cancellation Circuit for Full-Duplex Radio: Operating Principle and Measurements," in *Vehicular Technology Conference (VTC Spring), 2015 IEEE 81st*, May 2015, pp. 1–7 (cit. on p. 49).

[120] D. Yang, H. Yüksel, and A. Molnar, "A Wideband Highly Integrated and Widely Tunable Transceiver for In-Band Full-Duplex Communication," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 5, pp. 1189–1202, May 2015 (cit. on p. 50).

[121] D. J. van den Broek, E. A. M. Klumperink, and B. Nauta, "An In-Band Full-Duplex Radio Receiver With a Passive Vector Modulator Downmixer for Self-Interference Cancellation," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 12, pp. 3003–3014, Dec. 2015 (cit. on pp. 51, 52).

[122] M. T. Bohr and I. A. Young, "CMOS Scaling Trends and Beyond," *IEEE Micro*, vol. 37, no. 6, pp. 20–29, Nov. 2017 (cit. on p. 56).

[123] K. Lee, I. Nam, I. Kwon, J. Gil, K. Han, S. Park, and B.-I. Seo, "The impact of semiconductor technology scaling on CMOS RF and digital circuits for wireless application," *IEEE Transactions on Electron Devices*, vol. 52, no. 7, pp. 1415–1422, Jul. 2005 (cit. on p. 56).

[124] C. H. Jan, M. Agostinelli, H. Deshpande, M. A. El-Tanani, W. Hafez, U. Jalan, L. Janbay, M. Kang, H. Lakdawala, J. Lin, Y. L. Lu, S. Mudanai, J. Park, A. Rahman, J. Rizk, W. K. Shin, K. Soumyanath, H. Tashiro, C. Tsai, P. VanDerVoorn, J. Y. Yeh, and P. Bai, "RF CMOS technology scaling in High-k/metal gate era for RF SoC (system-on-chip) applications," in *2010 International Electron Devices Meeting*, Dec. 2010, pp. 27.2.1–27.2.4 (cit. on p. 56).

[125] K. Koli, S. Kallioinen, J. Jussila, P. Sivonen, and A. Parssinen, "A 900-MHz Direct Delta-Sigma Receiver in 65-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 12, pp. 2807–2818, Dec. 2010 (cit. on p. 56).

[126] R. B. Staszewski, "Digitally intensive wireless transceivers," *IEEE Design Test of Computers*, vol. 29, no. 6, pp. 7–18, Dec. 2012 (cit. on p. 56).

[127] S. Balasubramanian, S. Boumaiza, H. Sarbishaei, T. Quach, P. Orlando, J. Volakis, G. Creech, J. Wilson, and W. Khalil, "Ultimate Transmission," *IEEE Microwave Magazine*, vol. 13, no. 1, pp. 64–82, Jan. 2012 (cit. on p. 56).

[128] M. R. Sadeghifar and J. Wikner, "A survey of RF DAC Architectures," in *Proceedings of the Swedish System On Chip Conference, SSOCC 2010*, 2010 (cit. on p. 56).

[129] M. Fulde and F. Kuttner, "Digital Enhanced Transmitter Concepts for Nanometer-CMOS Technologies," *SpringerLink*, pp. 253–267, 2015 (cit. on pp. 56, 113, 135).

[130] A. Passamani, D. Ponton, E. Thaller, G. Knoblinger, A. Neviani, and A. Bevilacqua, "13.9 A 1.1V 28.6dBm fully integrated digital power amplifier for mobile and wireless applications in 28nm CMOS technology with 35% PAE," in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, IEEE, Feb. 2017, pp. 232–233 (cit. on pp. 56, 58).

[131] Intel® XMM™ 7480 Modem for LTE-Advanced Services, [Online]. Available: `https://www.intel.com/content/www/us/en/wireless-products/mobile-communications/xmm-7480-brief.html` (visited on 07/15/2018) (cit. on p. 58).

[132] 3GPP, "Evolved Universal Terrestrial Radio Access (E-UTRA); User Equipment (UE) radio transmission and reception," 3rd Generation Partnership Project (3GPP), Technical Specification (TS) 36.101, Mar. 2017, Version 14.3.0 (cit. on pp. 60, 61, 185).

[133] H. G. Myung, "Introduction to single carrier FDMA," in *2007 15th European Signal Processing Conference*, Sep. 2007, pp. 2144–2148 (cit. on p. 61).

[134] R. Bhat, J. Zhou, and H. Krishnaswamy, "Wideband Mixed-Domain Multi-Tap Finite-Impulse Response Filtering of Out-of-Band Noise Floor in Watt-Class Digital Transmitters," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 12, pp. 3405–3420, Dec. 2017 (cit. on p. 62).

[135] K. D. Chu, M. Katanbaf, C. Su, T. Zhang, and J. C. Rudell, "Integrated CMOS transceivers design towards flexible full duplex (FD) and frequency division duplex (FDD) systems," in *2018 IEEE Custom Integrated Circuits Conference (CICC)*, Apr. 2018, pp. 1–11 (cit. on p. 62).

[136] A. C. M. Austin, O. Afisiadis, and A. Burg, "Digital predistortion of hardware impairments for full-duplex transceivers," in *2017 IEEE Global Conference on Signal and Information Processing (GlobalSIP)*, Nov. 2017, pp. 878–882 (cit. on p. 62).

[137] B. Widrow and I. Kollár, *Quantization Noise: Roundoff Error in Digital Computation, Signal Processing, Control, and Communications*. Cambridge, UK: Cambridge University Press, 2008, 780 pp. (cit. on p. 63).

[138] T. Hentschel and G. Fettweis, "Sample rate conversion for software radio," *IEEE Communications Magazine*, vol. 38, no. 8, pp. 142–150, Aug. 2000 (cit. on p. 66).

[139] F. M. Gardner, "Interpolation in digital modems. I. Fundamentals," *IEEE Transactions on Communications*, vol. 41, no. 3, pp. 501–507, Mar. 1993 (cit. on p. 66).

[140] L. Erup, F. M. Gardner, and R. A. Harris, "Interpolation in digital modems. II. Implementation and performance," *IEEE Transactions on Communications*, vol. 41, no. 6, pp. 998–1008, Jun. 1993 (cit. on p. 66).

[141] T. Georgantas, K. Vavelidis, N. Haralabidis, S. Bouras, I. Vassiliou, C. Kapnistis, Y. Kokolakis, H. Peyravi, G. Theodoratos, K. Vryssas, N. Kanakaris, C. Kokozidis, S. Kavadias, S. Plevridis, P. Mudge, I. Elgorriaga, A. Kyranas, S. Liolis, E. Kytonaki, G. Konstantopoulos, P. Robogiannakis, K. Tsilipanos, M. Margaras, P. Betzios, R. Magoon, N. Bouras, M. Rofougaran, and R. Rofougaran, "9.1 A 13 mm^2 40 nm multiband GSM/EDGE/HSPA+/TDSCDMA/LTE transceiver," in *2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, Feb. 2015, pp. 1–3 (cit. on p. 71).

[142] S. Tadjpour, P. Rossi, L. Romano, R. Chokkalingam, H. Firouzkouhi, F. Shi, M. Leroux, D. Gerna, A. Venca, J. Vasa, B. Ramachandran, B. Brunn, A. Pirola, D. Ottini, A. Milani, E. Sacchi, M. Behera, X. Chen, U. Decanis, M. Tedeschi, S. DalToso, W. Eyssa, C. Cakir, C. Prakash, Y. He, N. Damavandi, R. Srinivasan, D. Shum, X. Fan, C. Yu, E. Pehlivanoglu, H. Zarei, A. Loke, G. Uehara, R. Castello, and Y. Song, "A multi-band Rel9 WCDMA/HSDPA/TDD LTE and FDD LTE transceiver with envelope tracking," in *European Solid State Circuits Conference (ESSCIRC), ESSCIRC 2014 - 40th*, Sep. 2014, pp. 383–386 (cit. on p. 71).

[143] T. Hornak, K. L. Knudsen, A. Z. Grzegorek, K. A. Nishimura, and W. J. McFarland, "An image-rejecting mixer and vector filter with 55-dB image rejection over process, temperature, and transistor mismatch," *IEEE Journal of Solid-State Circuits*, IEEE Journal of Solid-State Circuits, vol. 36, no. 1, pp. 23–33, Jan. 2001 (cit. on pp. 71, 72).

[144] J.-S. Syu, C. Meng, and Y.-C. Yen, "5.7 GHz Gilbert I/Q Downconverter Integrated With a Passive LO Quadrature Generator and an RF Marchand Balun," *IEEE Microwave and Wireless Components Letters*, vol. 18, no. 2, pp. 127–129, Feb. 2008 (cit. on p. 72).

[145] G. Yong and C. Saavedra, "A wideband feedback compensated quadrature generator," in *IEEE Sarnoff Symposium, 2009. SARNOFF '09*, Mar. 2009, pp. 1–4 (cit. on p. 72).

[146] K.-h. Kim, P. W. Coteus, D. Dreps, S. Kim, S. V. Rylov, and D. J. Friedman, "A 2.6 mW 370 MHz-to-2.5 GHz open-loop quadrature clock generator," in *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International*, Feb. 2008, pp. 458–627 (cit. on p. 72).

[147] A. Elshazly, A. Balankutty, Y.-Y. Huang, Y. Kai, and F. O'Mahony, "A 2 GHz-to-7.5 GHz quadrature clock-generator using digital delay locked loops for multi-standard I/Os in 14 nm CMOS," in *2014 Symposium on VLSI Circuits Digest of Technical Papers*, Jun. 2014, pp. 1–2 (cit. on pp. 72, 92).

[148] K. Yousef, H. Jia, A. Allam, A. Anand, R. Pokharel, and T. Kaho, "An eight-phase CMOS injection locked ring oscillator with low phase noise," in *2014 IEEE International Conference on Ultra-WideBand (ICUWB)*, Sep. 2014, pp. 337–340 (cit. on pp. 72, 92).

[149] A. Valero-Lopez, S. T. Moon, and E. Sanchez-Sinencio, "Self-calibrated quadrature generator for WLAN multistandard frequency synthesizer," *IEEE Journal of Solid-State Circuits*, IEEE Journal of Solid-State Circuits, vol. 41, no. 5, pp. 1031–1041, May 2006 (cit. on pp. 72, 92).

[150] K. Bhardwaj, S. Narayan, S. Shumarayev, and T. Lee, "A 3.1 mW phase-tunable quadrature-generation method for CEI 28G short-reach CDR in 28 nm CMOS," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International*, Feb. 2013, pp. 412–413 (cit. on pp. 72, 92).

[151] M. Kalcher, D. Gruber, and D. Ponton, "Self-aligned open-loop local quadrature phase generator," in *ESSCIRC Conference 2016: 42nd European Solid-State Circuits Conference*, Sep. 2016, pp. 351–354 (cit. on pp. 72, 74, 76, 78, 82–84, 86, 87, 91, 109).

[152] M. Kalcher, D. Gruber, and D. Ponton, "1–3 GHz Self-Aligned Open-Loop Local Quadrature Phase Generator with Phase Error Below 0.4," submitted to *Journal of Solid State Circuits*, currently under review (cit. on pp. 72, 74–76, 78–80, 82–91, 109, 210).

[153] M. Kalcher and D. Gruber, "CMOS Open-Loop Local Quadrature Phase Generator for 5G Applications," in *2017 Austrochip Workshop on Microelectronics (Austrochip)*, Oct. 2017, pp. 15–17 (cit. on pp. 72, 84, 109, 210).

[154] M. Kalcher, D. Gruber, F. Conzatti, and P. Greco, "Multiphase Signal Generators, Frequency Multipliers, Mixed Signal Circuits, and Methods for Generating Phase Shifted Signals," PCT Patent Application WO/2018/182585, Oct. 5, 2018 (cit. on pp. 72, 109).

[155] M. Kalcher and D. Gruber, "Self-Aligned Open-Loop Multiphase Generator," in *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2019, pp. 1–5 (cit. on pp. 72, 94, 96–98, 102–105, 107–110, 210).

[156] M. Benyahia, J. B. Moulard, F. Badets, A. Mestassi, T. Finateu, L. Vogt, and F. Boissieres, "A digitally controlled 5 GHz analog phase interpolator with 10 GHz LC PLL," in *International Conference on Design Technology of Integrated Systems in Nanoscale Era, 2007. DTIS*, Sep. 2007, pp. 130–135 (cit. on pp. 73, 84).

[157] S. Kumaki, A. H. Johari, T. Matsubara, I. Hayashi, and H. Ishikuro, "A 0.5 V 6-bit scalable phase interpolator," in *2010 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, Dec. 2010, pp. 1019–1022 (cit. on p. 84).

[158] R. Kreienkamp, U. Langmann, C. Zimmermann, T. Aoyama, and H. Siedhoff, "A 10-gb/s CMOS clock and data recovery circuit with an analog phase interpolator," *IEEE Journal of Solid-State Circuits*, IEEE Journal of Solid-State Circuits, vol. 40, no. 3, pp. 736–743, Mar. 2005 (cit. on p. 84).

[159] T. Sato, K. Okada, and A. Matsuzawa, "A new figure of Merit of LC oscilators considering frequency tuning range," in *2011 IEEE 9th International Conference on ASIC (ASICON)*, Oct. 2011, pp. 586–589 (cit. on p. 93).

[160] Y. Moon, D.-K. Jeong, and G. Ahn, "A 0.6-2.5-GBaud CMOS tracked 3× oversampling transceiver with dead-zone phase detection for robust clock/data recovery," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 12, pp. 1974–1983, Dec. 2001 (cit. on p. 93).

[161] M.-. E. Lee, W. J. Dally, J. W. Poulton, P. Chiang, and S. E. Greenwood, "An 84-mW 4-Gb/s clock and data recovery circuit for serial link applications," in *2001 Symposium on VLSI Circuits. Digest of Technical Papers (IEEE Cat. No.01CH37185)*, Jun. 2001, pp. 149–152 (cit. on p. 93).

[162] W.-H. Chen, G.-K. Dehang, J.-W. Chen, and S.-I. Liu, "A CMOS 400-Mb/s serial link for AS-memory systems using a PWM scheme," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 10, pp. 1498–1505, Oct. 2001 (cit. on p. 93).

[163] D. Birru, "A novel delay-locked loop based CMOS clock multiplier," *IEEE Transactions on Consumer Electronics*, vol. 44, no. 4, pp. 1319–1322, Nov. 1998 (cit. on p. 93).

[164] D. J. Foley and M. P. Flynn, "A 3.3 V, 1.6 GHz, low-jitter, self-correcting DLL based clock synthesizer in 0.5 µm CMOS," in *2000 IEEE International Symposium on Circuits and Systems. Emerging Technologies for the 21st Century. Proceedings (IEEE Cat No.00CH36353)*, vol. 2, May 2000, 249–252 vol.2 (cit. on p. 93).

[165] L. J. Cheng and Q. Y. Lin, "The performances comparison between DLL and PLL based RF CMOS oscillators," in *ASICON 2001. 2001 4th International Conference on ASIC Proceedings (Cat. No.01TH8549)*, Oct. 2001, pp. 827–830 (cit. on p. 93).

[166] O. Casha, I. Grech, F. Badets, D. Morche, and J. Micallef, "Analysis of the Spur Characteristics of Edge-Combining DLL-Based Frequency Multipliers," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 56, no. 2, pp. 132–136, Feb. 2009 (cit. on p. 93).

[167] D. Sager, G. Hinton, M. Upton, T. Chappell, T. D. Fletcher, S. Samaan, and R. Murray, "A 0.18 µm CMOS IA32 microprocessor with a 4 GHz integer execution unit," in *2001 IEEE International Solid-State Circuits Conference. Digest of Technical Papers. ISSCC (Cat. No.01CH37177)*, Feb. 2001, pp. 324–325 (cit. on p. 93).

[168] D. Harris and M. A. Horowitz, "Skew-tolerant domino circuits," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 11, pp. 1702–1711, Nov. 1997 (cit. on p. 93).

[169] J. Black W.C. and D. Hodges, "Time interleaved converter arrays," *IEEE Journal of Solid-State Circuits*, vol. 15, no. 6, pp. 1022–1029, Dec. 1980 (cit. on p. 93).

[170] A. Buchwald, "High-speed time interleaved ADCs," *IEEE Communications Magazine*, vol. 54, no. 4, pp. 71–77, Apr. 2016 (cit. on p. 93).

[171] F. Lin, P. Mak, and R. Martins, "3.9 An RF-to-BB current-reuse wideband receiver with parallel N-path active/passive mixers and a single-MOS pole-zero LPF," in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, Feb. 2014, pp. 74–75 (cit. on p. 93).

[172] A. Molnar and C. Andrews, "Impedance, filtering and noise in n-phase passive CMOS mixers," in *Proceedings of the IEEE 2012 Custom Integrated Circuits Conference*, Sep. 2012, pp. 1–8 (cit. on p. 93).

[173] W. Yuan and J. S. Walling, "A multiphase switched capacitor power amplifier in 130 nm CMOS," in *2016 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, May 2016, pp. 210–213 (cit. on p. 93).

[174] Y. Zhou and J. Yuan, "A 10-bit wide-band CMOS direct digital RF amplitude modulator," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 7, pp. 1182–1188, Jul. 2003 (cit. on p. 112).

[175] P. Eloranta, P. Seppinen, S. Kallioinen, T. Saarela, and A. Parssinen, "A Multimode Transmitter in 0.13 µm CMOS Using Direct-Digital RF Modulator," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 12, pp. 2774–2784, Dec. 2007 (cit. on p. 112).

[176] Z. Boos, A. Menkhoff, F. Kuttner, M. Schimper, J. Moreira, H. Geltinger, T. Gossmann, P. Pfann, A. Belitzer, and T. Bauernfeind, "A fully digital multimode polar transmitter employing 17b RF DAC in 3G mode," in *2011 IEEE International Solid-State Circuits Conference*, IEEE, Feb. 2011, pp. 376–378 (cit. on p. 112).

[177] B.-U. Klepser and F. Kuttner, "Radio Frequency Digital to Analog Converter," U.S. Patent 8854242 (B1), Oct. 7, 2014 (cit. on pp. 112, 114).

[178] J. Bastos, A. M. Marques, M. S. J. Steyaert, and W. Sansen, "A 12-bit intrinsic accuracy high-speed CMOS DAC," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 12, pp. 1959–1969, Dec. 1998 (cit. on p. 113).

[179] A. Van den Bosch, M. A. F. Borremans, M. S. J. Steyaert, and W. Sansen, "A 10-bit 1-GSample/s Nyquist current-steering CMOS D/A converter," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 3, pp. 315–324, Mar. 2001 (cit. on pp. 113, 139).

[180] B. Razavi, "Basic Principles of Digital-to-Analog Conversion," in *Principles of Data Conversion System Design*, Wiley-IEEE Press, 1995, pp. 45–78 (cit. on p. 113).

[181] S. Luschas and H. S. Lee, "Output impedance requirements for DACs," in *Proceedings of the 2003 International Symposium on Circuits and Systems, 2003. ISCAS '03*, vol. 1, IEEE, May 2003, I-861-I-864 vol.1 (cit. on p. 113).

[182] F. Kuttner, "Compensation of nonlinearity of single ended Digital to analog converters," U.S. Patent 7675442 (B2), Mar. 9, 2010 (cit. on p. 113).

[183] S. Zhou and M.-C. Chang, "A CMOS passive mixer with low flicker noise for low-power direct-conversion receiver," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 5, pp. 1084–1093, May 2005 (cit. on p. 118).

[184] H. Khatri, L. Liu, T. Chang, P. S. Gudem, and L. E. Larson, "A SAW-less CDMA receiver front-end with single-ended LNA and single-balanced mixer with 25 % duty-cycle LO in 65 nm CMOS," in *IEEE Radio Frequency Integrated Circuits Symposium, 2009. RFIC 2009*, Jun. 2009, pp. 13–16 (cit. on p. 118).

[185] A. Mirzaei, H. Darabi, J. Leete, and Y. Chang, "Analysis and Optimization of Direct-Conversion Receivers With 25 % Duty-Cycle Current-Driven Passive Mixers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 9, pp. 2353–2366, Sep. 2010 (cit. on p. 118).

[186] P. E. P. Filho, M. Ingels, P. Wambacq, and J. Craninckx, "An Incremental-Charge-Based Digital Transmitter With Built-in Filtering," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 12, pp. 3065–3076, Dec. 2015 (cit. on p. 126).

[187] W. Yuan, V. Aparin, J. Dunworth, L. Seward, and J. S. Walling, "A Quadrature Switched Capacitor Power Amplifier," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 5, pp. 1200–1209, May 2016 (cit. on p. 127).

[188] J. Horn. (May 17, 2000). The Relationship between Harmonic Distortion and Integral Non-Linearity, [Online]. Available: http://www.hit.bme.hu/~papay/edu/DSP/inl.htm (visited on 08/27/2018) (cit. on p. 129).

[189] H. Fraz, N. Bjorsell, J. S. Kenney, and R. Sperlich, "Prediction of Harmonic Distortion in ADCs using dynamic Integral Non-Linearity model," in *2009 IEEE Behavioral Modeling and Simulation Workshop*, Sep. 2009, pp. 102–107 (cit. on p. 129).

[190] J. Duan, L. Jin, and D. Chen, "A new method for estimating spectral performance of ADC from INL," in *2010 IEEE International Test Conference*, Nov. 2010, pp. 1–10 (cit. on p. 129).

[191] ——, "INL based dynamic performance estimation for ADC BIST," in *Proceedings of 2010 IEEE International Symposium on Circuits and Systems*, May 2010, pp. 3028–3031 (cit. on p. 129).

[192] D. Ponton, M. Kalcher, A. Paussa, E. Thaller, F. Kuttner, and D. Gruber, "Novel Signed-RFDAC Architectures Enabling Wideband and Efficient 5G Transmitters," United States Patent Application 16/364891, Mar. 26, 2019 (cit. on pp. 132–134, 206, 210).

[193] A. Passamani, F. Kuttner, and M. Fulde, "Method for operating radio frequency digital to analog conversion circuitry in the event of a first and a subsequent second input sample with different signs and an digital to analog conversion circuitry," U.S. Patent 9647678 (B2), May 9, 2017 (cit. on p. 133).

[194] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE Journal of Solid-State Circuits*, IEEE Journal of Solid-State Circuits, vol. 33, no. 2, pp. 179–194, Feb. 1998 (cit. on p. 136).

[195] R. M. Gray and D. L. Neuhoff, "Quantization," *IEEE Transactions on Information Theory*, vol. 44, no. 6, pp. 2325–2383, Oct. 1998 (cit. on p. 137).

[196] S. Trampitsch and D. Gruber, "Compensation of non-linearity at digital to analog converters," U.S. Patent 9900016 (B1), Feb. 20, 2018 (cit. on pp. 138, 158).

[197] M. Gustavsson, J. J. Wikner, and N. Tan, *CMOS Data Converters for Communications*, ser. The Springer International Series in Engineering and Computer Science. Springer US, 2000 (cit. on p. 139).

[198] M. Fulde, "Switched Capacitor RFDACs For Power Efficient Multi-mode Transmitter," Sep. 30, 2015 (cit. on p. 145).

[199] D. Gruber, "Multi-Mode RFDAC-based TX Systems for Cellular Transceivers in Scaled CMOS Technologies," Oct. 17, 2016 (cit. on p. 145).

[200] D. Ponton and A. Passamani, "Concept of Capacitor Scaling," pat. PCT/US2018/024983 (cit. on p. 148).

[201] X. He and J. van Sinderen, "A Low-Power, Low-EVM, SAW-Less WCDMA Transmitter Using Direct Quadrature Voltage Modulation," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 12, pp. 3448–3458, Dec. 2009 (cit. on p. 148).

[202] C. Andrews and A. C. Molnar, "A Passive Mixer-First Receiver With Digitally Controlled and Widely Tunable RF Interface," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 12, pp. 2696–2708, Dec. 2010 (cit. on p. 148).

[203] S. Trampitsch, D. Gruber, M. Lunglmayr, E. Thaller, and M. Huemer, "Digital compensation of DC-DC converter voltage ripple for Switched-Capacitor Power Amplifiers," in *2016 14th IEEE International New Circuits and Systems Conference (NEWCAS)*, IEEE, Jun. 2016, pp. 1–4 (cit. on p. 158).

[204] P. Hazucha, T. Karnik, B. A. Bloechel, C. Parsons, D. Finan, and S. Borkar, "Area-efficient linear regulator with ultra-fast load regulation," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 4, pp. 933–940, Apr. 2005 (cit. on p. 162).

[205] Y. Lu, Y. Wang, Q. Pan, W. H. Ki, and C. P. Yue, "A Fully-Integrated Low-Dropout Regulator With Full-Spectrum Power Supply Rejection," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 3, pp. 707–716, Mar. 2015 (cit. on p. 162).

[206] Y. Lu, C. Li, Y. Zhu, M. Huang, S. P. U, and R. P. Martins, "A 312 ps response-time LDO with enhanced super source follower in 28 nm CMOS," *Electronics Letters*, vol. 52, no. 16, pp. 1368–1370, 2016 (cit. on p. 162).

[207] R. G. Carvajal, J. Ramirez-Angulo, A. J. Lopez-Martin, A. Torralba, J. A. G. Galan, A. Carlosena, and F. M. Chavero, "The flipped voltage follower: A useful cell for low-voltage low-power circuit design," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, no. 7, pp. 1276–1291, Jul. 2005 (cit. on p. 162).

[208] J. Ramirez-Angulo, M. R. Valero-Bernal, A. Lopez-Martin, R. G. Carvajal, A. Torralba, S. Celma-Pueyo, and N. Medrano-Marqués, "The Flipped Voltage Follower: Theory and Applications," in *Analog/RF and Mixed-Signal Circuit Systematic Design*, M. Fakhfakh, E. Tlelo-Cuautle, and R. Castro-Lopez, Eds., vol. 233, Berlin, Heidelberg: Springer Berlin Heidelberg, 2013, pp. 269–287 (cit. on p. 162).

[209] M. Kalcher and D. Gruber, "Concept for a Buffered Flipped Voltage Follower and for a Low Dropout Regulator," German Patent Application 10 2018 129 910.9, Nov. 27, 2018 (cit. on pp. 165, 180, 206, 210).

[210] P. Wambacq, V. Giannini, K. Scheir, W. V. Thillo, and Y. Rolain, "A fifth-order 880 MHz/1.76 GHz active lowpass filter for 60 GHz communications in 40 nm digital CMOS," in *2010 Proceedings of ESSCIRC*, Sep. 2010, pp. 350–353 (cit. on p. 176).

[211] M. D. Matteis, A. Pezzotta, S. D'Amico, and A. Baschirotto, "A 33 MHz 70 dB-SNR super-source-follower-based low-pass analog filter," in *ESSCIRC 2014 - 40th European Solid State Circuits Conference (ESSCIRC)*, Sep. 2014, pp. 363–366 (cit. on p. 176).

[212] Spectre Circuit Simulator, [Online]. Available: `https://www.cadence.com/content/cadence-www/global/en_US/home/tools/custom-ic-analog-rf-design/circuit-simulation/spectre-circuit-simulator.html` (visited on 10/26/2018) (cit. on p. 182).

[213] R. A. Shafik, M. S. Rahman, A. R. Islam, and N. S. Ashraf, "On the error vector magnitude as a performance metric and comparative analysis," in *2006 International Conference on Emerging Technologies*, Nov. 2006, pp. 27–31 (cit. on pp. 184, 201).

[214] H. Ochiai and H. Imai, "Performance analysis of deliberately clipped OFDM signals," *IEEE Transactions on Communications*, vol. 50, no. 1, pp. 89–101, Jan. 2002 (cit. on pp. 184, 201).

[215] T. Deepa and R. Kumar, "Performance of comparison metrics on M-QAM OFDM systems with high power amplifier," in *2012 World Congress on Information and Communication Technologies*, Oct. 2012, pp. 909–914 (cit. on pp. 184, 201).

[216] M. Iwamoto, S. Matsuoka, H. Iwasaki, and H. Otsuka, "Transmission performance of OFDM with 1024-QAM in the presence of EVM degradation," in *2014 IEEE Asia Pacific Conference on Wireless and Mobile*, Aug. 2014, pp. 12–16 (cit. on pp. 184, 201).

[217] 3GPP, "Evolved Universal Terrestrial Radio Access (E-UTRA); Physical layer procedures," 3rd Generation Partnership Project (3GPP), Technical Specification (TS) 36.213, Mar. 2017, Version 14.2.0 (cit. on p. 196).

[218] M. Kalcher, D. Gruber, and D. Ponton, "Self-aligned open-loop local quadrature phase generator," in *ESSCIRC Conference 2016: 42nd European Solid-State Circuits Conference*, Sep. 2016, pp. 351–354 (cit. on p. 210).

[219] S. Trampitsch, M. Kalcher, D. Gruber, M. Lunglmayr, and M. Huemer, "Modeling Non-Idealities of Capacitive RF-DACs with a Switched State-Space Model," in *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2019, pp. 1–5 (cit. on p. 210).

[220] M. Kalcher, "Local Oscillators and Quadrature Generation – Phase Noise, Jitter, and Circuits: An Introduction," Jan. 24, 2018 (cit. on p. 211).