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X-Ray Radiation Effects on CMOS Integrated Circuits and Radiation Hradening

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"... Getting an education was a bit like a communicable sexual disease. It made you unsuitable for a lot of jobs and then you had the urge to pass it on. ..."

—Terry Pratchett, "Hogfather"

GRAZ UNIVERSITY OF TECHNOLOGY

Abstract

Faculty of Electrical and Information Engineering
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Doctor of Science
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This thesis summarizes my work in the frame of a research project, intending development of radiation hard integrated circuit design guidelines for next generation computed tomography. Under the influence of ionizing radiation integrated circuits degrade their parameters. To ensure reliable operation, the effects of ionizing radiation on electronics must be understood, and mitigation techniques and testing methods developed.

Within this work I investigate effects of X-ray radiation, typically used in computed tomography imaging, on susceptible semiconductor devices: diodes and MOS transistors. For this investigation I have designed two test chips, including standard and custom layout devices and circuit blocks, covering variety of parameters. The studied parameters included in particular different size, doping, layout and gate oxide thickness of different types of MOS transistors as well as area and perimeter of different types of diodes. The effects of X-ray radiation were studied in dependence on these parameters, leading to development of radiation hardening methodology.

One of the important steps in radiation hardened circuit design is circuit simulation. In this thesis my novel model for radiation hardened transistor simulation is presented and evaluated. Also, methodology for circuit radiation effects simulation is presented. This methodology allows not only to anticipate effect radiation will have on the circuit behaviour, but to track origins of radiation effects on the circuit level to the device level.

Although many standard guidelines for radiation effects testing exist, all of them require many engineering decisions for best testing procedure for a particular application. Within this work methodology for radiation effects testing at the circuit development stage is proposed, including electrical characterization and parameters extraction methodology, together with X-ray irradiation procedure. Finally, comparison of test results from different X-ray sources and facilities, according to the proposed results unification methodology, is presented.

Altogether, this work provides comprehensive study on X-ray effects on integrated circuits, methods for their mitigation, and procedures for radiation effects testing in research and development stage.

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With this I apologize to all of those I have failed to mention by name. I could continue this list much longer, but I need to give the reader a chance to actually find out what these years of research, you all have supported me through, were about.

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Abbreviations

BP	**B**onding **P**lan
CMOS	**C**omplementary-**M**etal-**O**xide-**S**emiconductor
CREAM	**C**ircuit **R**adiation **E**ffects **A**nalysis and **M**itigation
CT	**C**omputed **T**omography
DC	**D**irect **C**urrent
DD	**D**isplacement **D**amage
ELT	**E**nclosed **L**ayout **T**ransistor
EMI	**E**lectro-**M**agnetic **I**nterference
ESD	**E**lectro-**S**tatic **D**ischarge
FOXFET	**F**ield **O**xide **F**ield **E**ffect **T**ransistor
IC	**I**ntegrated **C**ircuit
LEO	**L**ower **E**arth **O**rbit
MiAMoRE	**Mi**tigation **A**nalysis and **Mo**delling of **R**adiation **E**ffects
MOSFET or **MOS**	**M**etal **O**xode **S**emiconductor **F**ield **E**ffect **T**ransistor
PCB	**P**rinted **C**ircuit **B**oard
RINCE	**R**adiation **I**nduced **N**arrow **C**hannel **E**ffect
RISCE	**R**adiation **I**nduced **S**hort **C**hannel **E**ffect
SEE	**S**ingle **E**vent **E**ffect
SLM	**S**cribe **L**ine **M**onitor
STI	**S**hallow **T**rench **I**solation
TID	**T**otal **I**onizing **D**ose

Motivation and Scope

"...It is well known that a vital ingredient of success is not knowing that what you're attempting can't be done..."

—Terry Pratchett

Ionizing radiation can be encountered in a vast amount of environments and applications: starting with relatively intuitive ones, like nuclear power plants or outer space, through less obvious and more everyday, like medical imaging, and to least expected, like commercial applications used in our surroundings, with background radiation. Under the influence of ionizing radiation electronic devices and circuits can change their properties and behaviour. This was first reported by Hughes and Giroux in [1], and since then remains a topical issue. These changes in electronic devices and circuits may lead to an operational error or a malfunction of the final application. One of the challenges today is to ensure correct operation of the electronic devices and systems in the environment of ionizing radiation.

1 Basics: Ionizing radiation and its effects on electronic devices

Ionizing radiation is kind of radiation possessing enough energy to ionize material. Fig. 1 illustrates different types of ionizing radiation. Here, simplified classification of radiation is given.

Ionizing radiation can be wave (like X- and gamma-rays) or particle (like alpha, beta or neutron radiation). It can also be directly and indirectly ionizing. The directly ionizing radiation is the charged particle flux radiation, such as high energetic protons and electrons (e.g. alpha and beta radiation). As the charged particle interacts with

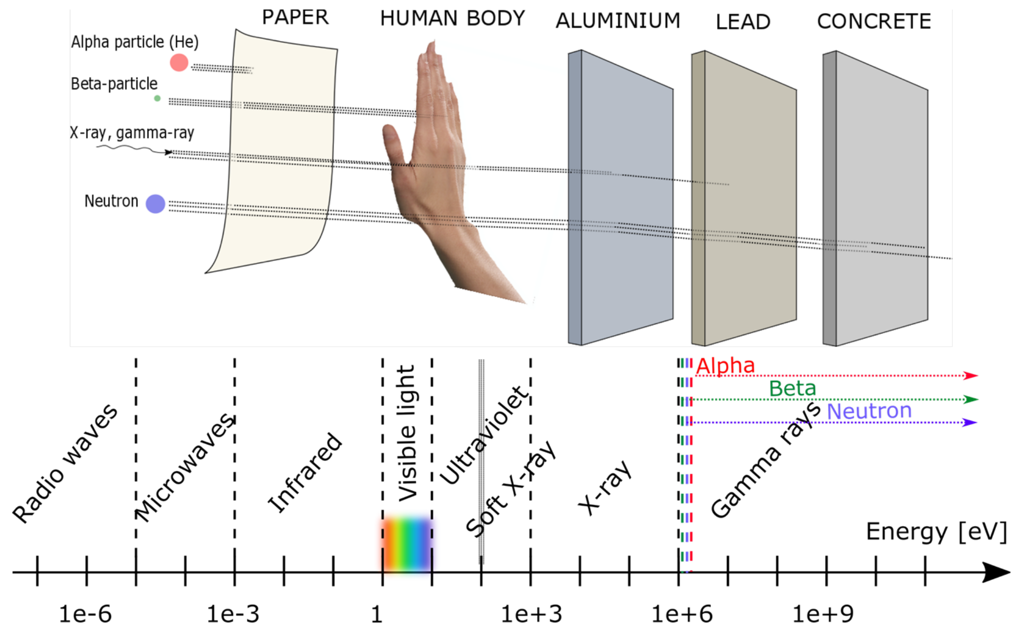


FIGURE 1: Different types of ionizing radiation and their placement within energy spectrum.

matter, its energy together with charge ionizes this matter. The indirectly ionizing radiation is kind of radiation with no charged particles involved (e.g. gamma, X-ray or neutron radiation). In this case radiation influences charged particles in the matter which in turn interact within matter, ionizing it. In case of wave radiation, photons transfer their energy to secondary electrons and they deposit kinetic energy to the matter leading to dose accumulation. Neutrons on the other hand can physically knock out atoms out of their place in the crystal lattice, changing physical properties of material.

Depending on type of radiation and interaction mechanism, different effects can occur in a semiconductor device. Generally, effects of ionizing radiation on semiconductor devices can be sub-divided into two categories: single event effects and cumulative effects [2].

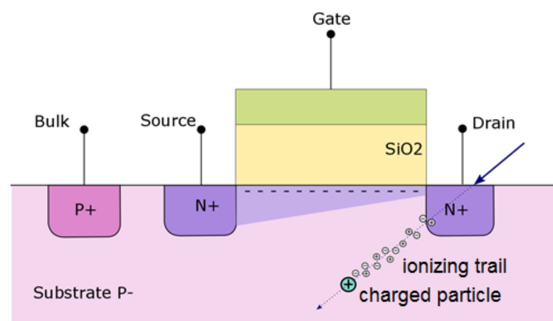


FIGURE 2: Illustration of single energetic charged particle striking an NMOS transistor leading to single event effect (SEE).

Single event effects (SEE), as the name suggests, occur when a single particle strikes the device. They are caused by charged particles, such as protons or heavy ions. When such particle strikes the device, it leaves ionization trail within the semiconductor material. The charge is then collected by the neighbouring nodes, leading to voltage or current spikes in the circuit. SEE is illustrated by Fig. 2. SEE can be destructive (such as latch-up or burn-in), or non-destructive (such as single event bit-flip or single event transient). Type of SEE is often defined by the effect it has on the particular circuit [3], [4].

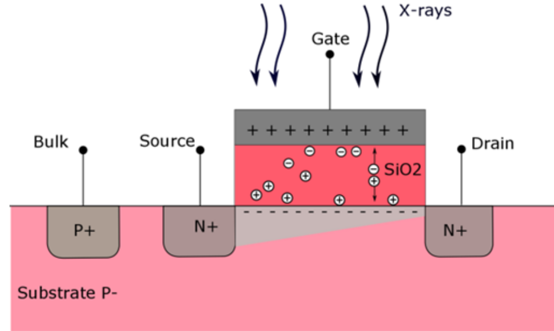


FIGURE 3: Illustration of charge trapping in gate oxide of a Silicon-based NMOS transistor under constant exposure to X-rays, leading to total ionizing dose (TID) effect.

Cumulative effects occur when the semiconductor device is exposed to ionizing radiation over a longer period of time. There are two kinds of cumulative effects: total ionizing dose (TID) effects and total displacement damage (DD).

TID effect takes place in the insulating layers of a semiconductor device or circuit. Under this effect excessive charge is trapped in SiO_2 and on its interface (Fig. 3). This charge creates a parasitic electric field, leading to device parameter shifts [5], [6].

DD in turn is a change in the crystal structure of the semiconductor. It occurs when an energetic particle has enough mass to knock atoms out of their place in crystal lattice, creating a vacancy-interstitial pair (Fig. 4), changing the physical properties of the material [7], [8].

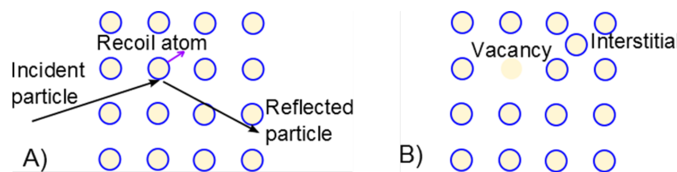


FIGURE 4: Illustration of incident particle hitting crystal lattice of semiconductor material leading to displacement damage (DD).

Table 2 summarizes the effects of ionizing radiation on semiconductor devices and circuits, including origin of the effect, place of its occurrence and the consequences on device and circuit level.

TABLE 2: Effects of ionizing radiation on semiconductor devices - summary.

	SEE	TID	DD
Origin	single energetic charged particle	exposure over time	
		all kinds of radiation	particles with mass
Occurrence	Si	SiO_2	Si
Effect	Ionization trail	Trapped charge	Vacancy-Interstitial
Consequence	latch-up, transient, bit flip...	V_{th} shift, increased leakage current, increased noise...	breakdown voltage change, increased noise, gain decrease...

2 Motivation: New generation of computed tomography

Computed tomography (CT) is one of the key diagnostic tools of the modern medicine [9]. However, this powerful tool is connected with a certain risk for the patient exposed to ionizing radiation. For example, the typical dose equivalent (total dose absorbed by a living tissue) of a chest CT is 7 mSv [10]. This corresponds to 7 years of the annual dose limit of civilian population in European Union [11]. The major objectives of the modern CT developments are patient exposure reduction together with improvement of image quality. This requires high speed high precision read-out electronics. In 2010 ams AG has launched a new revolutionary CT sensor solution developed in close cooperation with Siemens AG, the worldwide market leader for CT-scanners [12]. This sensor integrated circuit (IC) is based on a 3D integration of die stacking technology with photo sensor and read-out circuit connected realizing the shortest interconnects [13]. This new CT solution yielded dramatic improvements in linearity, noise reduction, speed and power consumption. To provide even better image resolution maintaining chip area, single channel read-out circuit acquiring X-ray image must be shrank in size even further.

The new much tighter spacing of photo detector and readout ICs raises new challenges for X-ray radiation hardness of the IC design. The circuits must provide precision measurement and maintain their accuracy over the possibly long lifetime under the

influence of ionizing radiation. That is why a comprehensive study of the effects of X-rays on ICs and their mitigation is needed to facilitate radiation hard IC development for the next generation CT, enabling in the next 5-10 years new solutions with improved medical imaging resolution at lowered x-ray exposure for the patients

3 Scope of the thesis

The focus of this thesis lies on the effects of X-ray radiation on integrated circuits, for two reasons. First of all, this is the kind of radiation relevant for the CT, and next generation CT is the main driver for this work. Additionally, X-ray effects are relevant for other application fields with other types of radiation. The major effect caused by X-rays is TID effect. Study of X-ray effects allows to isolate TID from other effects occurring under other types of radiation. So this study can be also used as a stepping-stone to further radiation hardness investigations involving other effects.

The potential industrial utilization of the scientific findings of my work is one of the major concerns in its implementation, so a commercial Complementary Metal-Oxide Semiconductor (CMOS) IC manufacturing process was chosen. Focusing on economic aspects, a 180 nm CMOS technology with shallow trench insulation (STI) was selected, offering a good trade-off between performance and costs. Fig. 5 illustrates a cross-section of the CMOS process.

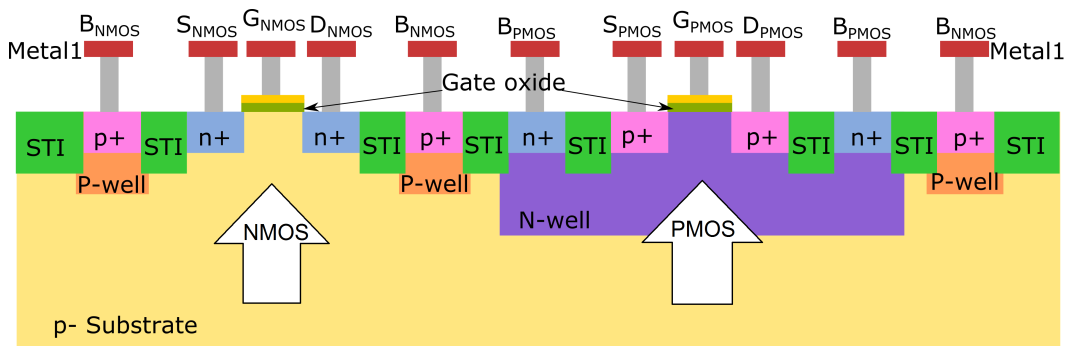


FIGURE 5: Illustration of commercial p-substrate CMOS process. Cross-section of an NMOS and a PMOS transistors.

Within this thesis I address three main subjects: X-ray effects and their mitigation, modelling and testing. In this way I cover major steps in the IC development flow in order to enable industrial radiation aware IC design in the future. The scope of my work is defined as follows:

Vision of this work is to enable next generation CT: with reduced patient dose, improved image quality and increased reliability - better diagnostics for better health.

Mission of this work is to provide scientific and industrial community with comprehensive study on X-ray effects on integrated circuits, methods for their mitigation, and procedures for radiation effects testing in research and development stage.

Subject of this work is X-ray effects on semiconductor devices and circuits in a commercial CMOS process with STI.

Methods used in this work include device and circuit design and layout, modelling, variety of electrical measurements, irradiation tests and analytical device and circuit parameters extraction.

Novelty of this work lies in its generalist approach to a specific topic of X-ray effects on semiconductor devices and circuits. In my work all aspects relevant to IC development for X-ray environment are addressed: from single device effects, through modelling of devices and circuits, and to X-ray effects testing. The main contributions to the state of science and state of the art are:

- Comprehensive study of X-ray effects on integrated devices and circuits, in particular substrate doping and gate extension area influence on TID effects.
- New data on low TID (<25 krad) effects on DC and noise performance of MOS transistors.
- Approach to radiation aware IC design: device choice, dimensioning and layout.
- Novel isosceles trapezoid model for annular gate transistor equivalent aspect ratio estimation.
- Circuit-level radiation effects analysis by means of macro-modelling, applied in circuit simulator.
- Methodology for X-ray effects characterization. The highlights are test structure development and parameter extraction methodology, including novel threshold voltage extraction technique adaptation for gate and STI components separation.
- Methodical approach to X-ray testing beyond standards and X-ray test results unification between different irradiation sources and facilities.

4 Structure of the thesis

This work is sub-divided into three main parts; together with this Motivation and the Conclusions it covers 4 years of intensive scientific work on the X-ray effects on ICs and methodology for radiation hardening, done in the frame of funded Austrian Funding Agency (FFG) project Cotomics (number 5082678). Every chapter is supported by a short introduction highlighting the state of science and a short conclusion summarizing main scientific findings presented within the chapter.

Chapter I deals with effects of X-rays on the integrated devices and approaches to their mitigation on device and circuit level. The main focus lies on integrated diode structures and MOS transistors, as those constitute the majority of devices in an integrated circuit. This chapter is sub-divided into three sections: transient X-ray effects, TID effects, and radiation hardening by design. Here the devices behaviour and parameters before, during and after irradiation is studied and analysed. It is concluded with circuit radiation hardening methodology.

In Chapter II the methodology of radiation hardening implementation is discussed. This chapter deals primarily with modelling, as a key step to reliable circuit design. It is subdivided into two sections: modelling of radiation hardened enclosed layout transistors (ELTs), and modeling of circuit radiation effects.

Chapter III of my thesis summarizes the testing methodology beyond standards necessary to be able to ensure robustness of ICs against X-rays. This chapter consists of two sections: dealing with test structures, their parameters and extraction of these parameters, and X-ray test development and dosimetry.

I finish this thesis with Conclusions and Outlook, highlighting my scientific contribution to the state of the art, and with an outlook on the future scientific opportunities, triggered with my research.

I provide details, vital for reproducibility of my research results in two Appendixes. In Appendix A one can find experimental details on how the results presented in this thesis were obtained, and Appendix B gives an inside on noise measurements.

Chapter I

X-Ray Effects and their Mitigation

"...Learnin' how not to do things is as hard as learning how to do them..."

—Terry Pratchett, "A Hat Full of Sky"

Introduction

X-rays possess enough energy to ionize semiconductor materials, silicon and silicon dioxide in particular. Effects of such ionizing radiation have been studied for the past few decades [14], [15]. Unlike effects of particle and heavy ion radiation, dealing usually with instantaneous single event effects (SEE) [16], [17], in the context of X-ray the focus lies on cumulative effects and TID [2]. Still, there exists an SEE equivalent in this context - X-ray pulse induced transient [18].

The basic mechanism behind TID - the charge trapping - has been topical for few decades [19], [20], [6]. Still, not all phenomena are understood, triggering further research activities [21], [22]. Also the known mitigation techniques have to be adapted to the emerging technologies, as the transistor features scale down [23], [24].

In this chapter I deal with the particularities of the X-ray effects on basic building blocks of an integrated circuit - diodes and transistors. I analyse the basic mechanisms behind the qualitative and quantitative effects and their dependence on the various device parameters. This comprehensive study advances the state of scientific knowledge

about X-ray effects, covering transient effects and TID effects and dependence of the TID effects on device size, doping and layout.

I conclude with a summary on the mitigation techniques and radiation hard by design methodology as a set of design guidelines for analog and mixed signal ICs operating under exposure to X-rays. The innovative design methodology in its simplicity can be easily integrated in the standard industrial design flow, facilitating research and development in the field of radiation hard integrated circuits. Unique in their completeness the design guidelines allow ensuring of radiation hardness with close to no complex mitigation techniques - by simple dimensioning and smart device choice. Only the residual effect has to be mitigated with specific circuit and layout techniques.

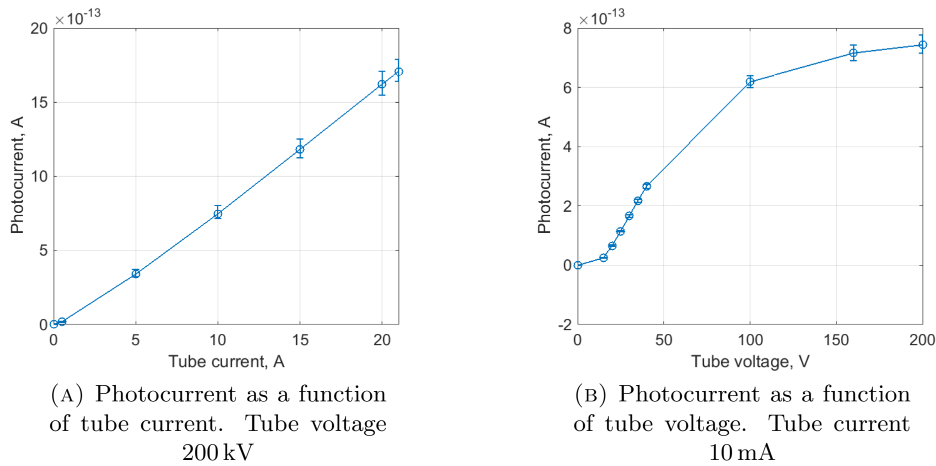
The data presented in this chapter and used for the analysis has been obtained in the experiments described in Appendix A.

1 Transient effects

Traditionally, transient radiation effects on electronics are analysed in context of high dose rate upsets [25]. However even at lower dose rates and moderate ionizing radiation energies transient effects can take place. Under the influence of photons of certain energy semiconductors undergo photoelectric effect [26], [27]. The generation of electron-hole pairs due to the photoelectric effect depends on the intensity of the photon beam and the wavelength (influencing penetration depth). In the case of X-rays, the energy the photon deposited in the silicon can be enough to generate two to fifty thousand electron-hole pairs. This phenomenon is widely used in photon counting detectors, but can lead to undesired noise, current and voltage spikes when an X-ray pulse hits the circuit under operation. Alexander in his work [18] gives a comprehensive overview of the few decades of research in the area of transient radiation effects. The particular interest in this research area lies on transient effects modelling for very high dose rate radiation, whereas only little is reported about medium and low dose rate radiation of moderate energy, like X-rays.

In the frame of my thesis I consider transient effects of X-ray radiation in the context of radiation hard IC design. The current density generated by an X-ray pulse is particularly important in this context. In this section my experimental results on transient effects

on integrated diodes fabricated in a commercial CMOS process with STI are presented. The photocurrent of integrated diodes generated by a 60 keV X-ray source is shown in Fig. I.1 as a function of tube current (A) and of tube voltage (B).



(A) Photocurrent as a function of tube current. Tube voltage 200 kV

(B) Photocurrent as a function of tube voltage. Tube current 10 mA

FIGURE I.1: Average (points), and minimal and maximal (bars) $10\times10\,\mu$m diode photocurrent as a function of X-ray tube current (A) and voltage (B)

The linear dependence observed in the Fig. I.1A corresponds to the intensity linearity of the X-ray source. The non-linear dependence of the photocurrent on the tube voltage as seen in Fig. I.1B illustrates difference in depth of collection region for the different energy of X-rays. A sketch of the energy spectrum of the X-ray source, reflecting the spectral distribution of X-ray intensity in arbitrary units (a.u.), is shown in Fig. I.2. The dominant spike corresponds to K-shell characteristic energy of the X-ray target (in the discussed case Tungsten). It is superimposed on the Bremsstrahlung emitted as the tube is bombarded with a beam of electrons. The intensity of the generated X-rays is defined by tube current and the energy spectrum of the X-rays by the tube voltage.

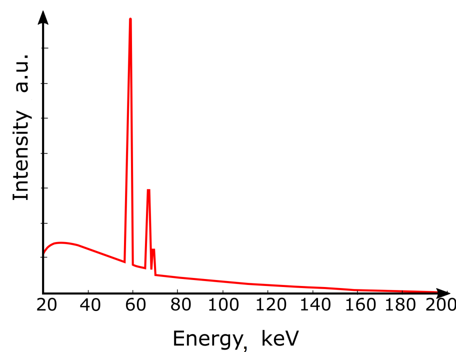


FIGURE I.2: Qualitative sketch of the energy spectrum of Tungsten target X-ray source (Logarithmic Y-scale)

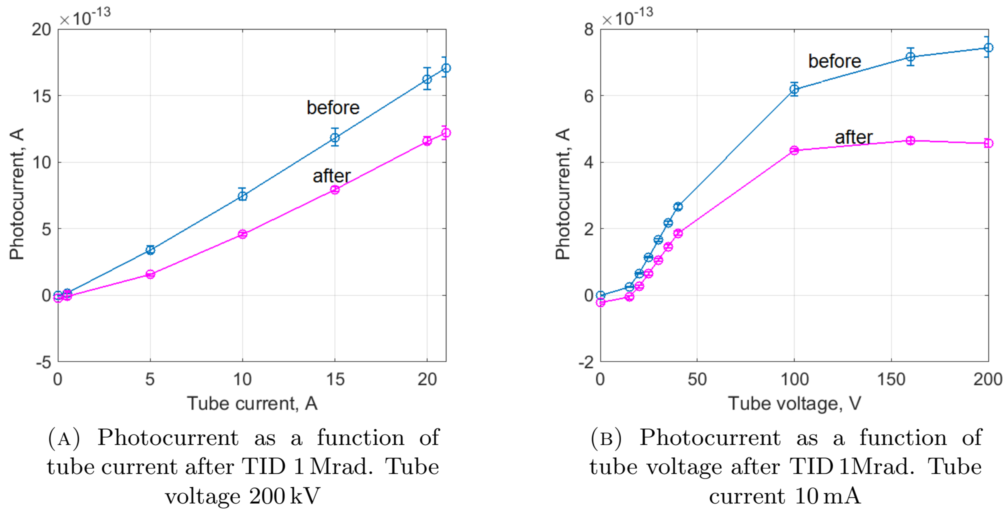
The photocurrent is proportional to the area of the diode, dose rate and thus intensity of the X-ray beam, and depth of the collection region [25]. The non-linearity of the photocurrent dependent on the tube voltage (and thus mean energy of the beam) is related to the different penetration depth and absorption coefficient of different energies of X-ray in silicon. This means on the one hand variation in dose rate and on the other hand variation in charge collection depth. These quantities changing with different speed along the tube voltage lead to a non-linearity in the photocurrent response. In contraty the tube current changes only the intensity and thus the dose rate, leading to linear dependence of the photocurrent on the tube current at constant voltage.

The quantitative behaviour of the photocurrent depends on the afore mentioned factors as well as on the fabrication process of the device. The higher the doping of the silicon in the exposure region, the less effect the produced photocurrent will have. The results shown in Fig. I.1 show general robustness of the analysed devices. The order of magnitude of the photocurrent at maximal tube voltage (Fig. I.1A) varies between 1 and 10 fA/μm^2. Such photocurrent can be considered insignificant for most circuits. The results presented here are obtained from a 180 nm CMOS technology. This allows to assume that with scaling down of the technology nodes incorporating higher doping levels, higher photocurrent values would be required to cause behaviour changes in a circuit. However, capacitances in smaller technology nodes are also getting smaller, thus the photocurrent values have to be carefully taken into account in radiation tolerant design, as will be discussed later in Section 3 of this chapter.

Finally, I report the difference in photocurrent between virgin and pre-irradiated samples. Fig. I.3 illustrates photocurrent of the same $10{\times}10\,\mu$m $N+$ in substrate diode before irradiation and after TID of 1 Mrad. In this figure the induced photocurrent is significantly lower after irradiation. Thus, TID has influence on the charge collection efficiency at given energy or on material absorption properties. This hints on the change DC performance of the diodes. This change is discussed in the next subsection.

2 Total Ionizing Dose Effects

Under continuous exposure to X-rays integrated circuit devices change their electrical parameters. This cumulative phenomenon is called TID Effect. It has been topical for



(A) Photocurrent as a function of tube current after TID 1 Mrad. Tube voltage 200 kV

(B) Photocurrent as a function of tube voltage after TID 1Mrad. Tube current 10 mA

FIGURE I.3: Average (points), and minimal and maximal (bars) 10×10 μm diode photocurrent as a function of X-ray tube current (A) and voltage (B) before irradiation (blue) and after TID of 1 Mrad (magenta).

a few decades now [1], [28]. The basic mechanisms behind TID are electron-hole pair generation, charge trapping and tunnelling [5], [29], [30], [31]. Under the influence of ionizing radiation the photoelectric effect takes place in the semiconductor and insulating layers of ICs, leading to electron-hole pairs generation [27]. In the insulating layers, electrons with higher mobility escape the matter, leaving the less mobile holes trapped inside the silicon dioxide. This trapped charge, and the charge consequently trapped on the interface to silicon, creates a parasitic electric field, effectively changing the electrical parameters of the devices. In this section I focus on two integrated circuit devices - diodes and MOS transistors.

Usually radiation effects on diodes are only scarcely reported in literature and very little fundamental analysis of the effects is presented. So, in [19] the cause of the parameter shift is formulated without additional analytical substantiation. Later works dealing with radiation effects on diodes and refering to [19] consider these devices in context of bandgap voltage references and as a part of bipolar transistors [32], [33], [34], [35], [36]. There are also many works dealing with proton radiation effect on diodes, such as [4] or [37], [36], hinting on similar physical mechanisms of degradation. However, a comprehensive methodical study of TID effects on different types of diodes is, to the best of my knowledge, missing in available literature. Within my thesis I contribute to closing of this gap with a methodical empirical and analytical study of TID effects on different types of diodes.

Nevertheless, the main focus of TID effects research remains with MOS transistors, due to sensitivity of both gate oxide and STI to radiation induced charge trapping [14], [38]. In this thesis the results of my methodical experimental and analytical investigations of these effects on a comprehensive set of custom-designed test devices is presented. The analysis includes dependence of the TID effects on various physical transistor parameters, such as size, doping and layout.

First, I was able to complement investigations of Faccio and his group on radiation effects size dependence [39] to hold for different technologies and substantiate them with extensive amount of measurement data on a big MOSFET size variation set. In particular I detect the limits of the radiation induced narrow channel effect (RINCE) [40], [41] and the radiation induced short channel effect (RISCE) [39] effects in the commercial 180 nm CMOS technology, not reported before. I also extrapolate the obtained results for other technology nodes using similar processing. The extension of the state of the art knowledge with the new comprehensive data set is significant for future circuit developments and allows generalization of design guidelines, as will be discussed in more detail in Section 3.

Further, I provide in depth analysis of radiation effects dependence on doping within one technology. The works of King et al. [23] and Rezzak et al. [42] have pointed out higher radiation tolerance of the technologies with higher doping levels. However, in this context it is difficult to directly compare the devices from different technologies, due to different minimal feature size and other processing steps. Here I present new data on the standard and high doping MOS transistors TID response and substantiate higher radiation tolerance of high doping devices with a multi-physics simulation.

Finally, I complete this section with layout dependent effects. On the one hand I reproduce and extend the data on enclosed layout transistor radiation tolerance against the standard layout, as first proposed by the group of Heijne and Snoyes [43]. On the other hand, I present analysis of the layout dependent TID effects enhancement, caused by gate extension area, as first reported by Liu et al. in [44]. To the best of my knowledge, the study of gate extension area influence on the TID effects in MOS transistor has never been conducted before and thus presents precious addition to the current state of science.

2.1 Diodes

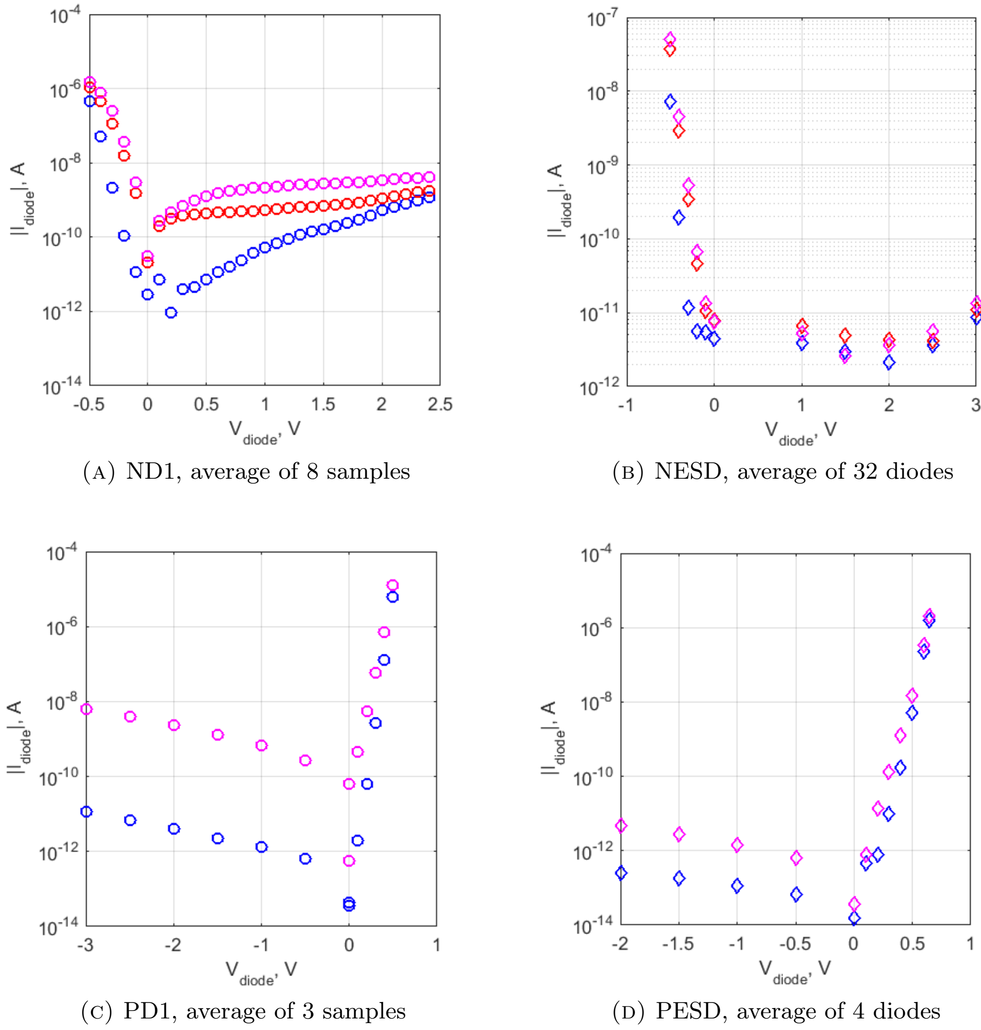
Usually TID effects on diodes are analysed in the context of vertical bipolar transistors as used in bandgap voltage references [32], [35]. There is very little literature giving in-depth analysis of the diode parameter change. Fig. I.4 illustrates this change. Here the I-V characteristics of the diodes measured before and after irradiation is depicted. These results were obtained in the frame of my experiments described in Appendix A. From this I-V characteristics it is clear that ideality factor (the slope of forward bias characteristics), saturation current and reverse bias current change after irradiation. This change is coming from the charge trapping in STI and on its interface. Similar effects have been reported in [19].

In my work I report and analyse parameter change in different types of diodes ($N+$ in Substrate and $P+$ in N-well) of different size (area to perimeter ratio), as summarized in Table I.1. This range of custom-designed test devices allows a solid conclusion on the nature of the effects, proving the hypothesis stated in earlier works [19], [32] that the change in diodes performance is primarily induced by charge trapped on the interface of the STI.

Table I.1: Experimental Structures

Type	Name	Area, μm^2	Perimeter, μm
$N+$ in Substrate	ND1..2	139400	55760
	ND3..4	99000	39600
	ND5	95000	38000
	ND6	62600	25040
	NESD1..4	72	202.9
$P+$ in N-well	PD1	313600	35840
	PD2	443450	50680
	PD3	989800	113120
	PESD1..2	107	302

Tables I.3 and I.2 summarize average parameters shifts before and after 1 Mrad TID of different diodes. In Table I.3 shift of diode ideality factor after 1 Mrad TID is given. In Table I.2 saturation current after irradiation $I_{SAT1Mrad}$ is referred to saturation current before irradiation I_{SAT0}, the same as saturation current densities $J_{SAT1Mrad}$ and J_{SAT0}. Total diode current is defined via its area Ja_{SAT} and sidewall (perimeter) Jp_{SAT} current density components. In the high perimeter small area device main contribution to the



(A) ND1, average of 8 samples

(B) NESD, average of 32 diodes

(C) PD1, average of 3 samples

(D) PESD, average of 4 diodes

FIGURE I.4: Average measured I-V characteristics of the $N+$ in Substrate (a, b) and $P+$ in N-Well (c, d) diode arrays (a, c) and ESD diodes (b, d) before irradiation and after 300 krad (a, b, c, d) and 1 Mrad (a, b) TID

saturation current comes from the sidewall current density Jp_{SAT}. Here higher change in the current can be observed, hinting to the major contribution of the STI interface traps - trapped charge on the interface between STI and Si.

TABLE I.2: Measurement Results: saturation current

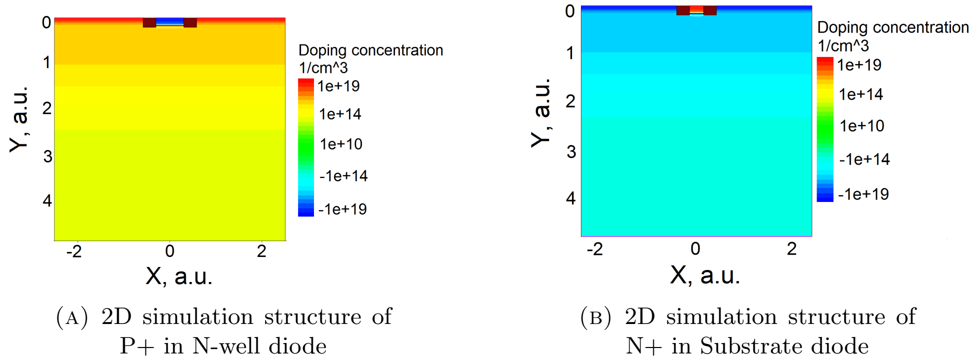
<table>
<tr><th>Diodes</th><th>$\frac{I_{SAT1Mrad}}{I_{SAT0}}$</th><th>Area component $\frac{Ja_{SAT1Mrad}}{Ja_{SAT0}}$</th><th>Side-wall component $\frac{Jp_{SAT1Mrad}}{Jp_{SAT0}}$</th></tr>
<tr><td>ND</td><td>1.8e+3</td><td rowspan="2">1.5e+3</td><td rowspan="2">2e+3</td></tr>
<tr><td>NESD</td><td>2.3e+3</td></tr>
<tr><td>PD</td><td>1.4e+3</td><td rowspan="2">1.25e+3</td><td rowspan="2">4.2e+3</td></tr>
<tr><td>PESD</td><td>3.2e+3</td></tr>
</table>

Table I.3: Measurement results: ideality factor

Diodes	Ideality factor shift $\Delta\eta$
ND	0.535
NESD	0.559
PD	0.532
PESD	0.539

In order to analyse this phenomenon in more detail, I have performed multi-physics simulations in Sentaurus TCAD. For this, a 2-D structure, incorporating substrate, active region and STI, has been drawn, and defects concentration before and after irradiation in the STI oxide and on its interface was defined separately. For the simplicity of the analysis an ideal semiconductor has been assumed before irradiation, without any trapped states. Since radiation induced trapping is highly dependent on the quality of the silicon and the insulating regions and thus on a particular process [45], a qualitative analysis has been performed instead of quantitative, at few arbitrary chosen values of traps concentration.

Fig. I.5 illustrates the simulation structures: $P+$ in N-well (A) and $N+$ in Substrate (B) diodes. The dimensions of the structure has been chosen according to the typical 180 nm CMOS process design rules.

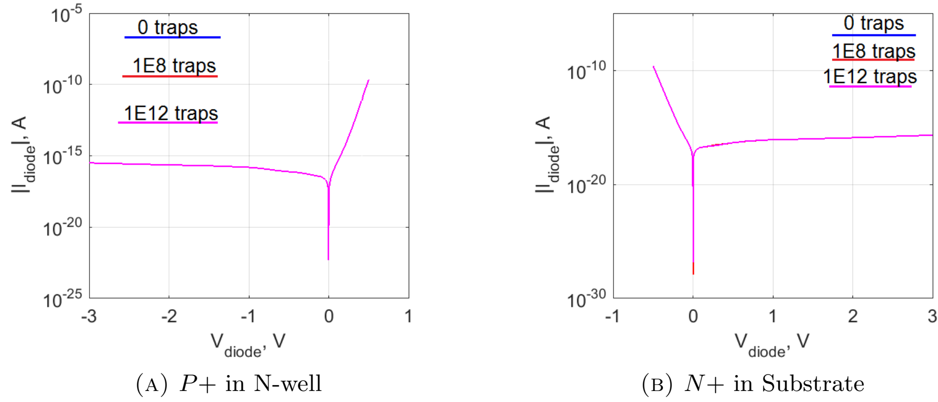


(A) 2D simulation structure of P+ in N-well diode

(B) 2D simulation structure of N+ in Substrate diode

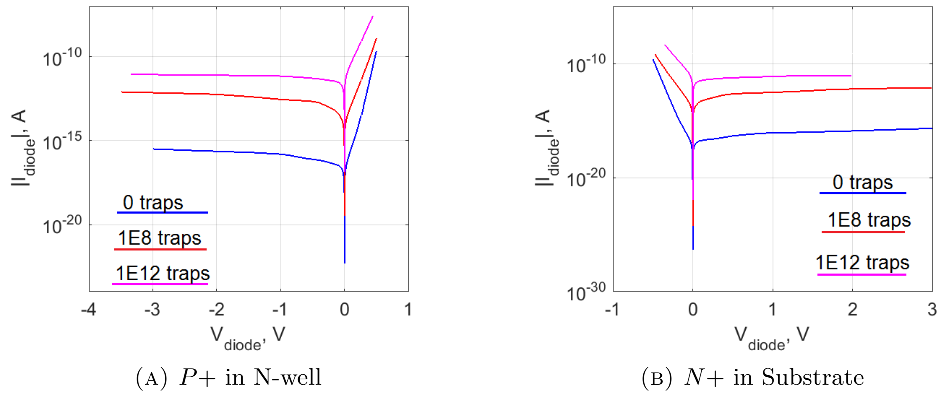
Figure I.5: TCAD Sentaurus 2D simulation structures of P+ in N-well and N+ in Substrate diodes

The results of the simulation are shown in Fig. I.6 and Fig. I.7. Here, IV characteristics extracted from the simulation before and after introduction of traps is shown. As it can be seen from Fig. I.6, chosen oxide traps concentrations have no influence on the diode performance. On the other hand, interface traps lead to similar characteristics shift as has been observed in the experimental results, as it can be seen in Fig. I.7.



(A) $P+$ in N-well (B) $N+$ in Substrate

FIGURE I.6: Simulated diode I-V characteristics before and after introduction of different number of oxide traps



(A) $P+$ in N-well (B) $N+$ in Substrate

FIGURE I.7: Simulated diode I-V characteristics before and after introduction of different number of interface traps

As ideality factor is a particularly interesting diode parameter, I have investigated its dependence on interface traps concentration, shown in Fig. I.8. Here, the ideality factor of an $N+$ in Substrate diode has been extracted for various interface traps concentrations N_{it} at two substrate temperatures: 300 K (blue) and 400 K (red). The general dependence is close to exponential. The irregularity of 300 K curve suggests that a different model is used by the simulator starting from N_{it}=1E8 $\frac{1}{cm^3}$ in the given structure, whereas 400 K simulation is steady within the simulation range. This suggests in future work the models have to be tuned to the particular fabrication process and expected operating temperature to be able to forecast parameter changes due to TID. Still, the obtained simulation results allow to support conclusion on the experimentally observed phenomena.

The main conclusion of the conducted investigations is that STI interface traps are main

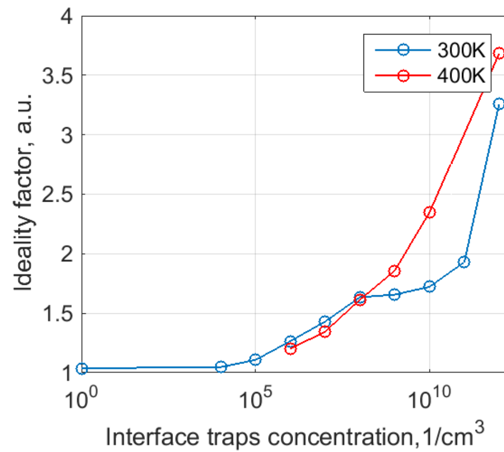


FIGURE I.8: Simulated ideality factor of $N+$ in Substrate diode as a function of interface traps concentration at 300 K (blue) and 400 K (red).

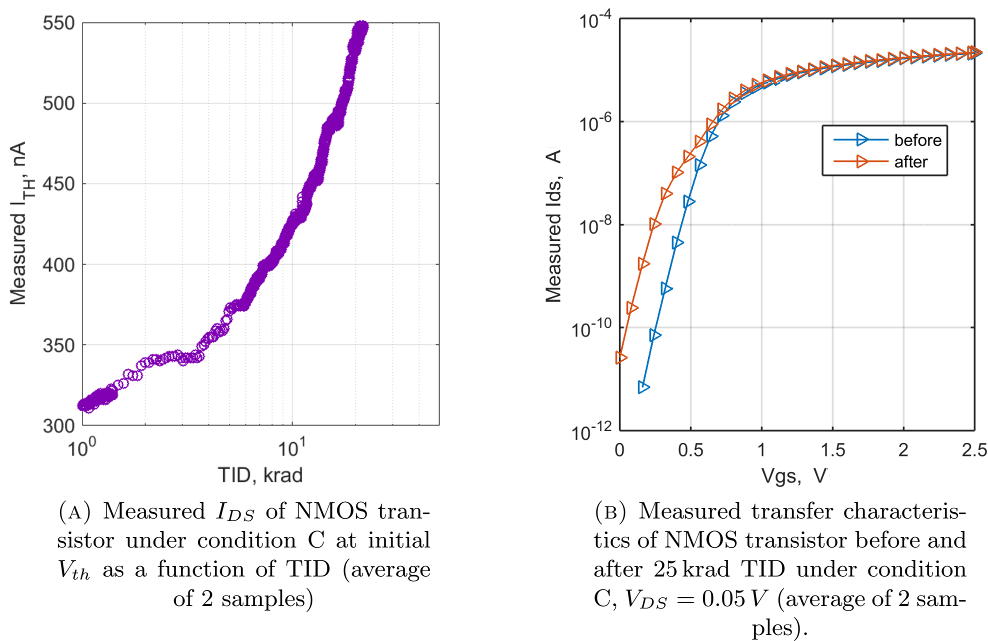
contributors to diode parameters degradation after irradiation, whereas STI oxide traps have only minor influence. One of the possible mitigation techniques would be to use diode of the inner side of the edgeless transistor (discussed later in the chapter), where diode is surrounded by the gate oxide rather than STI.

2.2 MOS Transistors

Within this thesis I have focused on a limited range of MOS transistor parameters, including such DC parameters as threshold voltage, leakage current and transconductance, and flicker ($1/f$ or pink) noise. I have restricted my work to these parameters as they are the most relevant for analog and mixed signal IC design. I present experimental results for different types of transistors: thin (t_{GOX} <4 nm) and medium (t_{GOX} >10 nm) gate oxide NMOS and PMOS. Although it is generally known thin gate oxide devices are more robust to TID effects [6], even in the nanoscale process nodes some circuit blocks still require wider operating ranges and higher voltages, thus it is vital to study such devices. Furthermore, this study, combined with intensive literature research, allows to extrapolate the findings on TID effects to different technology nodes of commercial CMOS processes with STI. Altogether presented study both recreates and substantiates existing statements and hypotheses as well as presents new findings, such as doping dependence within one technology node, gate extension area influence on TID effect, or low dose effects on the noise of transistors.

2.2.1 DC parameters

Fig. I.9A illustrates drain current of a transistor monitored in-situ during irradiation as a function of TID (detailed experiment description can be found in Appendix A). It is a medium oxide NMOS transistor, thus more susceptible to radiation. Here a rapid increase in drain current at a given voltage is observed at TID as low as 10 krad, hinting to threshold voltage shift at this dose. This also correlates with transfer characteristics shift shown in Fig. I.9B.



(A) Measured I_{DS} of NMOS transistor under condition C at initial V_{th} as a function of TID (average of 2 samples)

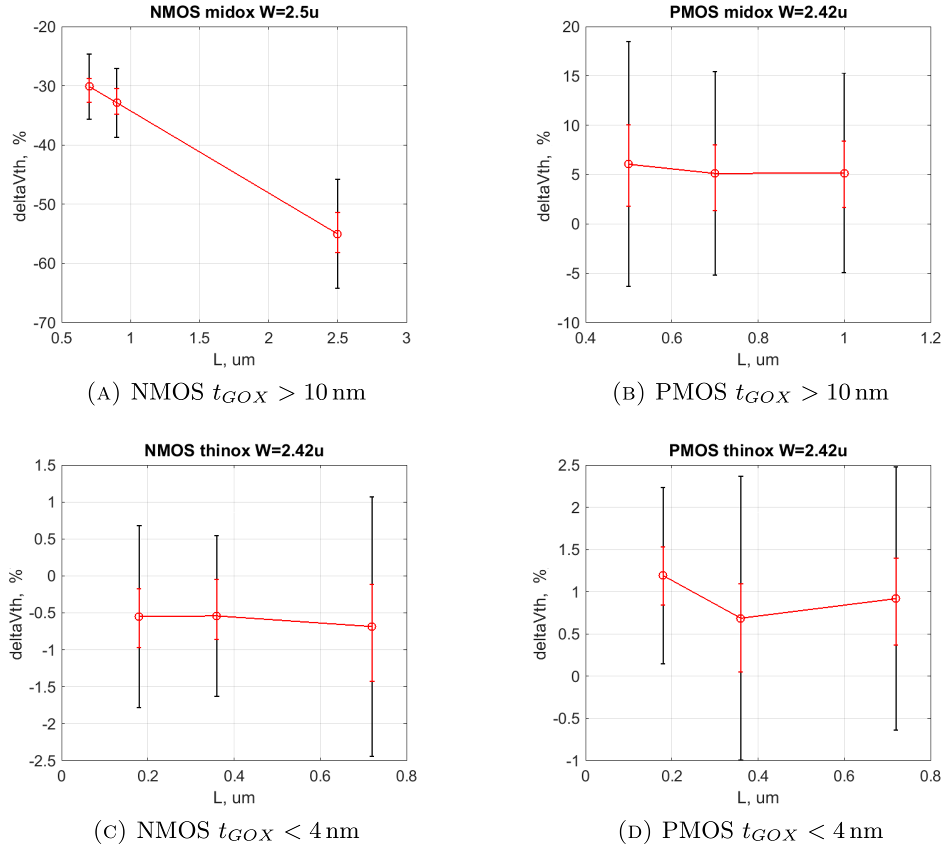
(B) Measured transfer characteristics of NMOS transistor before and after 25 krad TID under condition C, $V_{DS} = 0.05\,V$ (average of 2 samples).

FIGURE I.9: NMOS transistor characteristics change with increasing TID.

Such characteristics shift are analysed further on in this chapter. I have analysed the influence of X-ray radiation on the threshold voltage shift, leakage current and transconductance in dependence on various factors. The actual physical realisation of a transistor has major influence on the quantitative radiation effect [43], [46]. In this subsection I analyse the parameters change as a function of transistor size, doping, and physical layout realisation. This study included different bias conditions, but I report and discuss only the worst case bias [47].

Size Dependence of the radiation effects in MOS transistors has been studied by many groups. In their work [40] Gaillardin et al. first spoke about radiation induced narrow channel effect (RINCE) and later on Faccio and his team [39] have expanded the

concept also to radiation induced short channel effect (RISCE). In my work I extend these studies with new data, showing the boundaries for the minimal radiation effect in a commercial 180 nm CMOS technology [48], as transistor dimensioning is an important step in any circuit design. Together with analysis of the literature I extrapolate my discoveries to a simple guideline for transistor dimensioning for integrated circuits implementation.

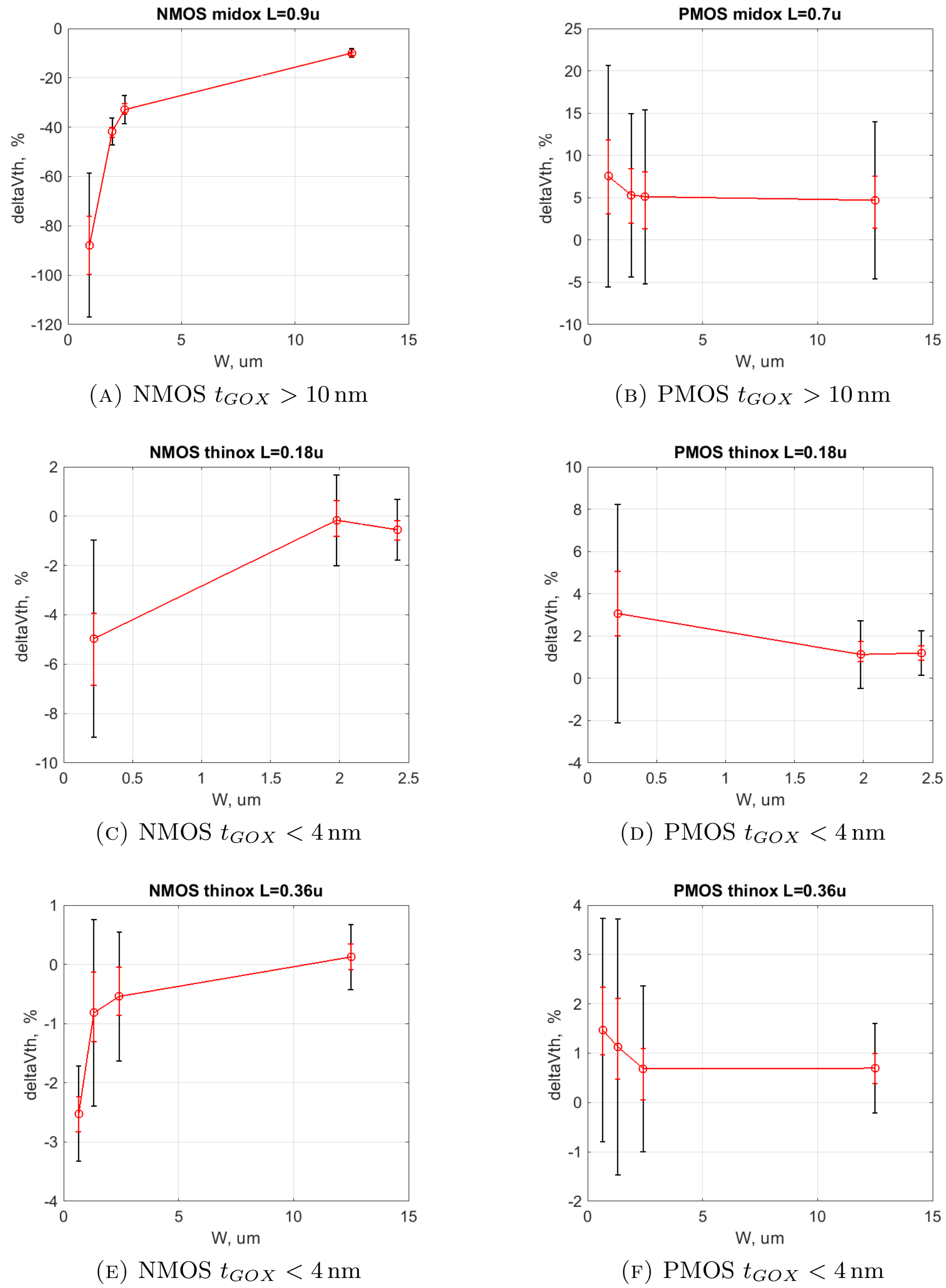


(A) NMOS $t_{GOX} > 10$ nm (B) PMOS $t_{GOX} > 10$ nm

(C) NMOS $t_{GOX} < 4$ nm (D) PMOS $t_{GOX} < 4$ nm

FIGURE I.10: Relative threshold voltage shift ΔV_{th} of the medium oxide (A-B) and thin oxide (C-D) NMOS (A, C) and PMOS (B, D) transistors after TID=300 krad as a function of channel length: average (red line), min-max bar (red bar) and 3σ bar (black bar) data of 20 samples irradiated under worst case condition.

Fig. I.10 illustrates the relative threshold voltage shift ΔV_{th} of the medium oxide (A-B) and thin oxide (C-D) NMOS (A, C) and PMOS (B, D) transistors after TID=300 krad as a function of the channel length. From these plots two conclusions can be made. First, RISCE is easier detectable on thin oxide devices. Second, there is not only the minimal (originating from the actual RINCE effect), but also maximal length limit (originating from other effects), in order to minimize the TID effect. Both these observations have a common physical ground: the channel length is contributing to a layout effect, discussed



(A) NMOS $t_{GOX} > 10\,\text{nm}$ (B) PMOS $t_{GOX} > 10\,\text{nm}$

(C) NMOS $t_{GOX} < 4\,\text{nm}$ (D) PMOS $t_{GOX} < 4\,\text{nm}$

(E) NMOS $t_{GOX} < 4\,\text{nm}$ (F) PMOS $t_{GOX} < 4\,\text{nm}$

FIGURE I.11: Relative threshold voltage shift δV_{th} of the medium oxide (A-B) and thin oxide (C-F) NMOS (A, C, E) and PMOS (B, D, F) transistors after TID=300 krad as a function of channel width: average (red line), min-max bar (red bar) and 3σ bar (black bar) data of 20 samples irradiated under worst case condition.

few paragraphs later - the gate extension area effect. From the given plots, the optimal length of transistor lies near twice minimal length.

Fig I.11 depicts the relative threshold voltage shift ΔV_{th} of the medium oxide (A-B) and thin oxide (C-F) NMOS (A, C, E) and PMOS (B, D, F) transistors after TID=300 krad as a function of the channel width. Here, the wider the channel gets, the less TID effect

can be observed in NMOS transistors. In PMOS transistors the effects tends to saturate around 2 μm. From an extensive study on 65 nm CMOS technology, conducted by Faccio and his group [39] it is known that the limit for RINCE lies somewhere between 1 and 5 μm. It is thus consequent to state the limit lies around 2 μm for the given 180 nm technology. Similarity of my findings to findings on 65 nm process node suggest RINCE to be technology independent for technologies incorporating STI between 180 nm and 65 nm.

Based on these findings, a great deal of radiation hardness of a circuit can be achieved only by careful dimensioning of the transistors in critical nodes. This will be summarized in section 3 of this chapter, together with other radiation hard design guidelines.

Doping Dependence of the TID effects has not been studied into detail so far. In their work King et al. [23] report robustness of the high threshold voltage discrete components fabricated in 14 nm FinFET technology. Here they presume higher body doping leads to the higher charge needed to switch on parasitic edge transistor. However the FinFET technology differs significantly from standard planar CMOS [49]. There have been also reports of doping influence on TID induced parameter shifts in CMOS technologies. So, in their work Rezzak et al. [42] compare two technology nodes - 90 nm and 65 nm. They assume higher radiation hardness of the latter due to higher body doping. In the course of my work I have also observed the same phenomenon - within one technology. Some CMOS technologies offer varieties of devices with the same gate oxide and similar properties, but different threshold voltage levels: low, standard and high. This is usually achieved by the introduction of different doping.

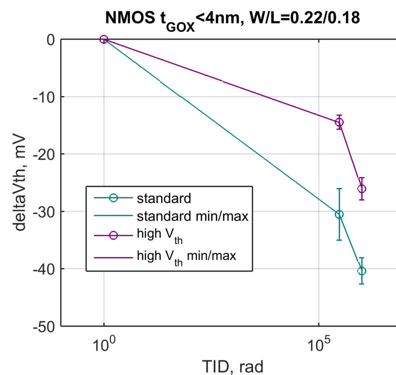
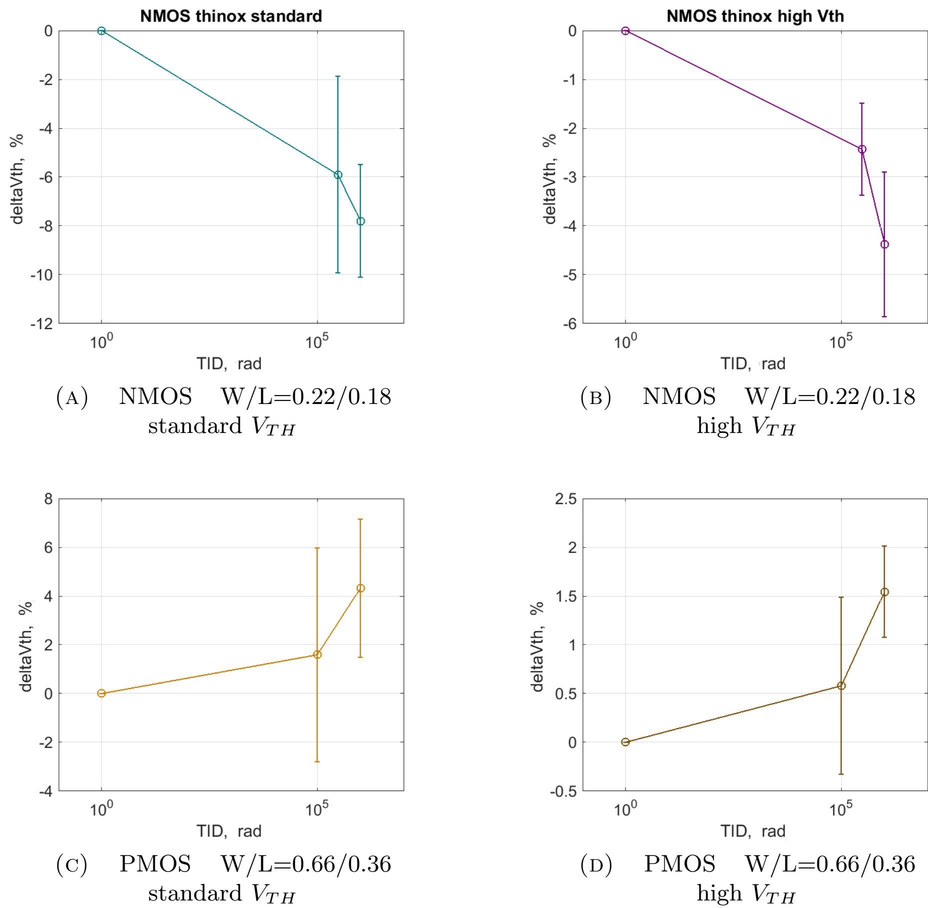


FIGURE I.12: Absolute threshold voltage shift as a function of TID for standard (blue) and high (purple) threshold voltage NMOS transistors



(A) NMOS W/L=0.22/0.18 standard V_{TH}

(B) NMOS W/L=0.22/0.18 high V_{TH}

(C) PMOS W/L=0.66/0.36 standard V_{TH}

(D) PMOS W/L=0.66/0.36 high V_{TH}

FIGURE I.13: Relative threshold voltage shift as a function of TID of NMOS (A, B) and PMOS (C, D) transistors with t_{GOX} <4 nm with standard (A, C) and high (B, D) threshold voltage

Fig I.12 illustrates absolute threshold voltage shifts of NMOS transistors under the worst case bias condition for standard and high threshold voltage devices. Fig. I.13 illustrates relative threshold voltage shift of NMOS and PMOS transistors with standard and high threshold voltage.

To the best of my knowledge, no fundamental analysis of this effect can be found in literature. In order to investigate the basic mechanisms behind this phenomenon I have performed TCAD simulation, comparing same geometrical structures with different doping levels. A 3D NMOS transistor model, as illustrated in Fig. I.14, has been implemented with different body doping concentration. Consequently multi-physics simulation after injection of different number of oxide traps has been performed. From the obtained I-V characteristics threshold voltage and threshold voltage shift have been extracted within Matlab environment with the same method as for the measurement data (see Appendix A). The obtained results are presented in Fig. I.15.

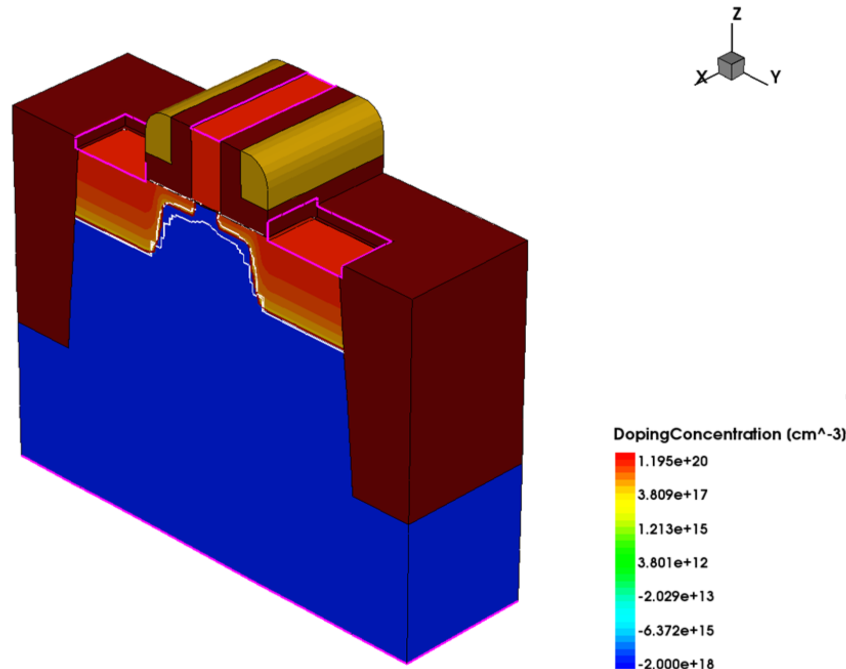


FIGURE I.14: 3D model of an NMOS transistor in TCAD simulation

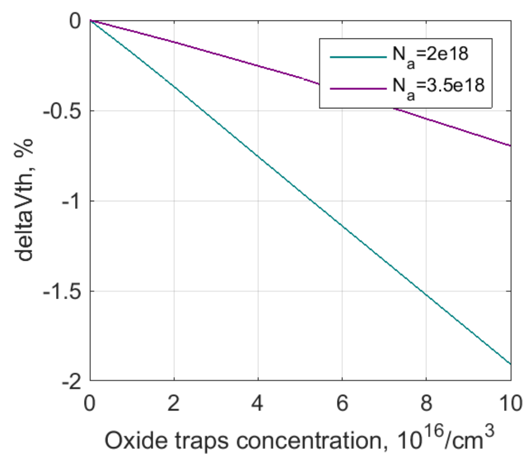


FIGURE I.15: Simulated threshold voltage shift of NMOS transistor with two different levels of body doping concentration as a function of oxide traps concentration

As it can be seen, the threshold voltage shift of the transistor model with higher body doping is lower at the same oxide traps concentration level, than for the lower body doping transistor. This result is quite similar to the behaviour observed empirically with increasing TID. This finding leads to two conclusions from the point of view of radiation hard design. First, smaller technology nodes are advantageous not only because of gate oxide thickness, but also due to their higher doping concentration. Secondly, if within one technology node few options of doping concentration (usually high or low threshold voltage shift options) at the same gate oxide thickness of the device are

available, choosing the higher doping option enables higher TID tolerance.

Layout Dependence of the radiation effects on the MOS transistor is strong. So, there is a special TID effects mitigation technique called enclosed layout transistor (Fig. I.16), improving post-radiation behaviour of the device [43], [46]. But also other parameters of geometrical realization can have impact on the extent of radiation effect. So Liu et al. in their work [44] have first reported apparent dependence of the radiation effects on the extension of the gate above the STI. In the following two sub-paragraphs I report and analyse the aforementioned phenomena in a comprehensive study of layout effects.

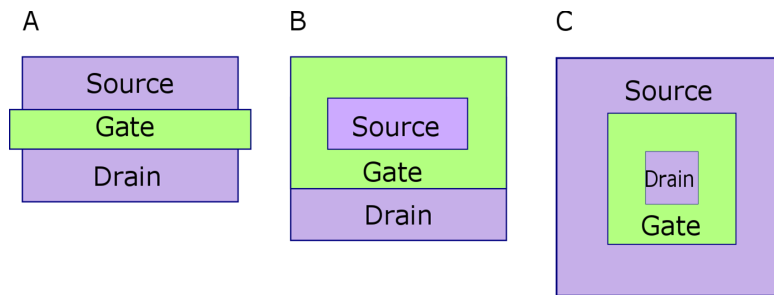
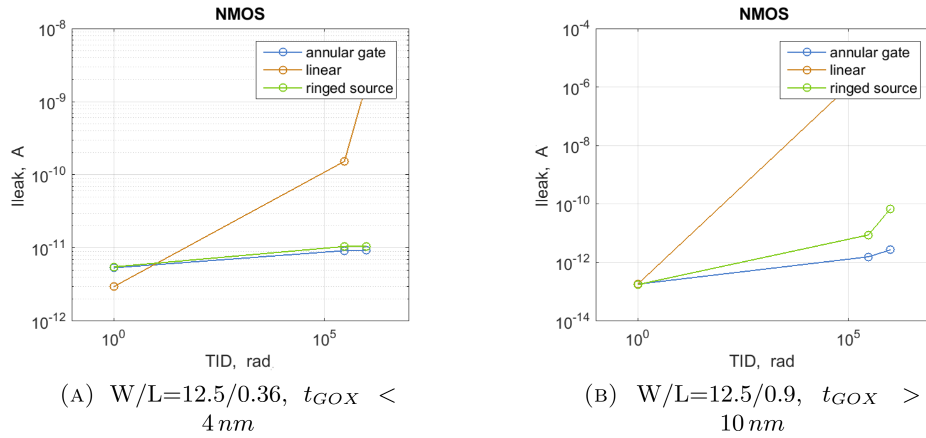


FIGURE I.16: Illustration of standard linear (A) and enclosed layout (B, C) transistors: standard linear layout (A), ringed source layout (B) and annular gate layout (C).

Standard and Enclosed Layouts have been continuously analysed throughout the years [46], [24]. First proposed by team of Heijne and Snoeys [43], nowadays ELT is a well established radiation hardening technique. For the completeness of my study I have implemented and analysed transistors of the same channel dimensions in standard and enclosed layout. The results are consistent with the expectations from the literature study showing significant difference in radiation hardness of these layouts. Fig. I.17 illustrates radiation induced leakage current as a function of TID for NMOS transistors with the same equivalent aspect ratio in standard linear, ringed source [50] and annular gate [46] layouts.

Although ELT has been primarily developed to mitigate TID induced leakage current [46], [50], as it is present in standard layout transistors, it is also effective in partial mitigation of threshold voltage shift - the contribution caused by the STI trapped charge. Fig. I.18 demonstrates the difference in threshold voltage shift of a medium oxide NMOS

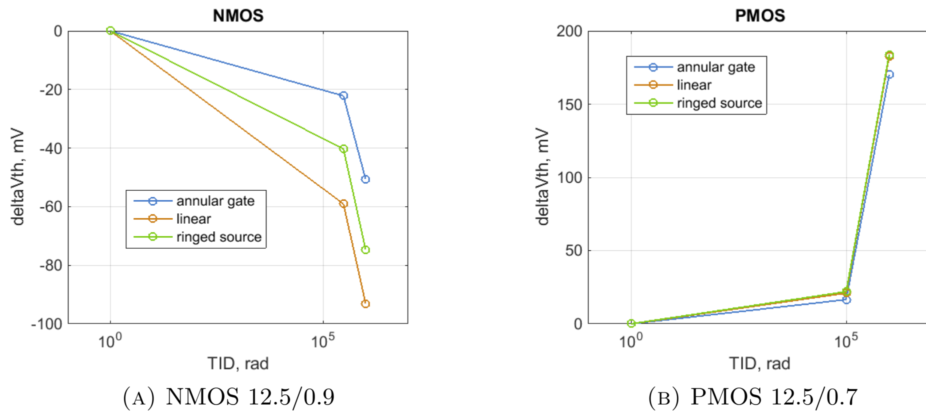


(A) W/L=12.5/0.36, t_{GOX} < 4 *nm*

(B) W/L=12.5/0.9, t_{GOX} > 10 *nm*

FIGURE I.17: Leakage current of thin (A) and medium (B) gate oxide NMOS transistors in standard linear (brown), ringed source (green) and annular gate (blue) layout as a function of TID

and PMOS transistors of different sizes, implemented as ELT and as standard layout transistor.



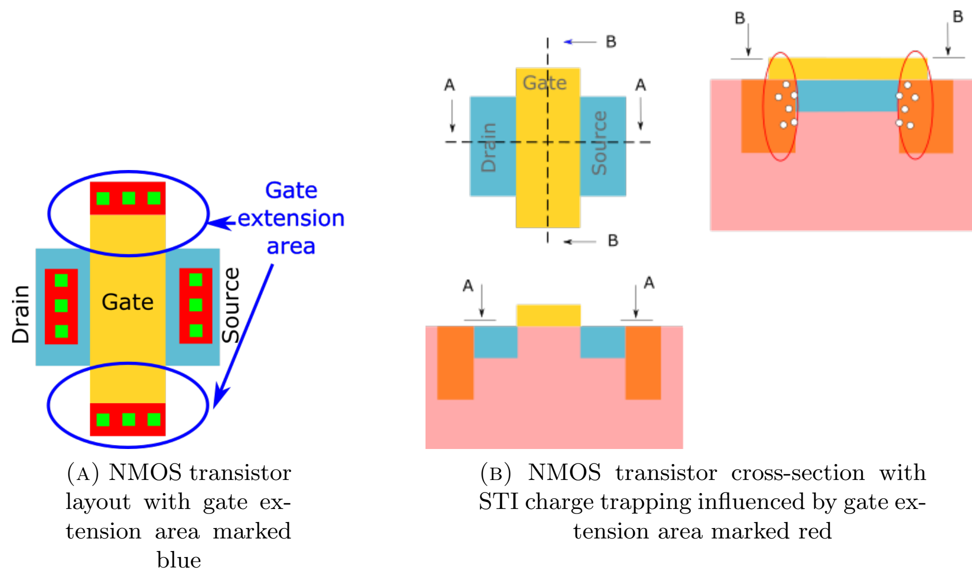
(A) NMOS 12.5/0.9

(B) PMOS 12.5/0.7

FIGURE I.18: Threshold voltage shift of linear layout and ELT NMOS (A) and PMOS (B) transistors with t_{GOX} >10 nm. Average of 8 samples.

Gate Extension Area Dependence is a new analysis not presented yet in literature. In their work Liu et al. [44] analysed possible ways to harden transistors with the influence on the STI charge trapping. In the course of their investigations they have experimentally discovered a major influence of gate extension area on the TID induced leakage current coming from the parasitic structure on the transistor edge. In [44] the researchers compare wide and narrow channel MOS transistors, whereby the narrow channel transistor has smaller gate extension area than the wide transistor. This makes

it difficult to differentiate between the RINCE [40] and the actual effect of the gate extension area. Liu et al. have analysed the phenomenon with a 3D simulation and stated a hypothesis for radiation hardening: to use wide channel transistors with small gate extension area. This study led me to the deeper empirical analysis of the geometrical realization of the transistor on its post-irradiation behaviour, presented in this paragraph. In particular I experimentally prove major influence of the gate extension area on the TID induced DC parameter shift of MOS transistors. The vast variety of transistor aspect ratio I have implemented in my work allows me to separate gate extension ratio effects from RINCE and RISCE effects.



(A) NMOS transistor layout with gate extension area marked blue

(B) NMOS transistor cross-section with STI charge trapping influenced by gate extension area marked red

FIGURE I.19: Illustration of gate extension area and its effect on charge trapping in the underlying STI as layout (A) and as a simplified cross-section of an NMOS transistor in a commercial CMOS process.

First, let me define the gate extension area. Fig. I.19 shows the typical MOS transistor layout and a simplified NMOS transistor cross-section in a commercial CMOS process. In conventional CMOS technologies, a certain extension of the poly-silicon is required for gate contacting. To improve reliability and matching of the devices, it is common to contact the gate on both sides, as shown in Fig. I.19A. This extension influences the charge trapping in the STI underneath similarly to the charge trapping in gate oxide (Fig. I.19B). Thus, in the worst case bias [47] the charge trapping in the STI regions below gate extension area will be enhanced. Thus, the larger the area of the extension, the more STI is influenced by it, the larger should the TID effect be.

The experimental results proving the above stated are presented in Fig. I.20. Here the difference in absolute threshold voltage shifts of thin and medium oxide NMOS transistors irradiated up to 300 krad TID as a function of gate extension area is illustrated. Two important observations are derived from these plots:

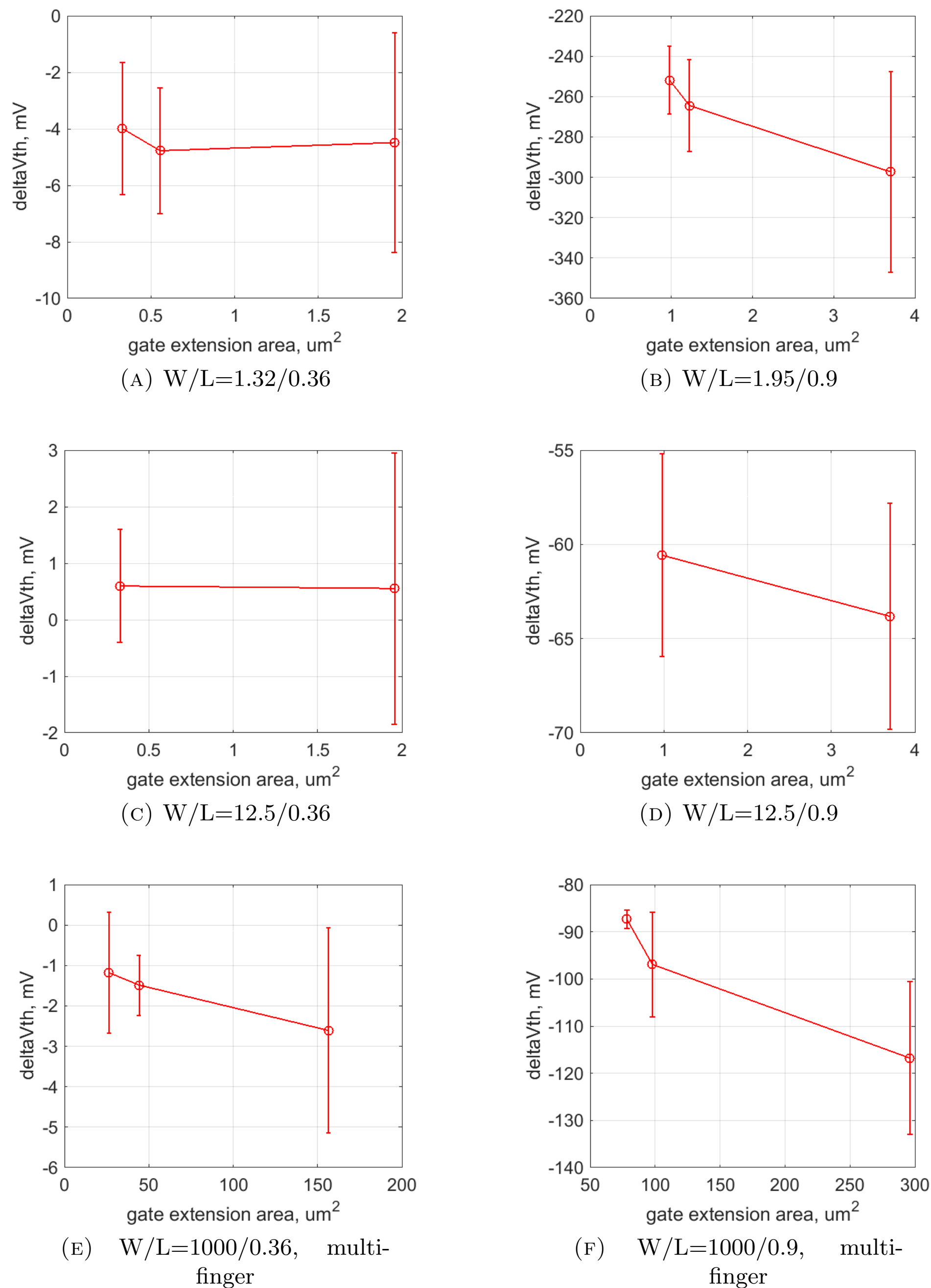


FIGURE I.20: Absolute threshold voltage shift after 300 krad TID of NMOS transistors with t_{GOX} <4 nm (A, C, E) and t_{GOX} >10 nm (B, D, F). Average (lines), and minimal and maximal (bars) of 8 samples.

- the average threshold voltage shift is in most cases higher for the devices with larger gate extension area;
- the variation of the effect between samples is greater for larger gate extension area.

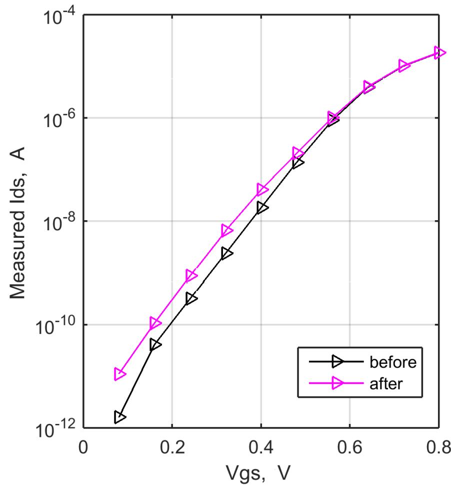
This allows to conclude the larger the gate extension area, the worse the TID effect, both on absolute parameter shift and on matching between samples after irradiation.

2.2.2 Flicker noise

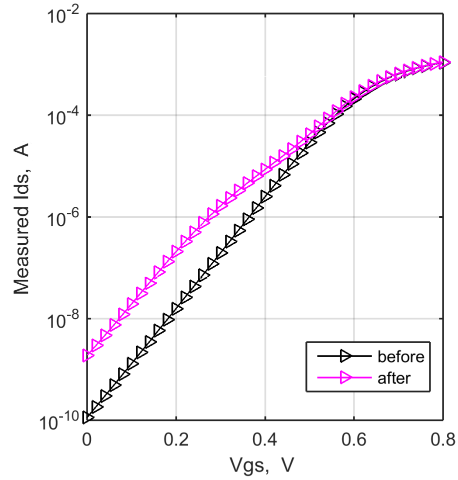
Before the influence of the trapped charge becomes noticeable in DC characteristics, it can be observed in the noise performance of the device [51], [52]. As CMOS technologies below 180 nm, with gate oxide thickness t_{OX} <4 nm, are less susceptible to TID effects, most of the studies focus on doses above 100 krad [21, 22, 52, 53]. However, already at lower doses significant parameter shifts may occur. Here results of my experiments on TID effects on noise performance of MOS transistors for doses below 25 krad are discussed. It is a unique and important contribution to the state of science, as low TID effects are relevant for more applications, for example space missions at Lower Earth Orbit (LEO) with expected TID below 25 krad. Parts of the presented study has been published at RADECS 2018 in Gothenburg [54]. Experimental details on noise measurements can be found in Appendix B.

Fig. I.21 illustrates the transfer characteristics and flicker noise of two medium oxide NMOS transistor with same channel length and different channel width. The change in the threshold voltage and leakage current, as discussed in previous sub-section can be also observed in these plots. The dominant effect is an order of magnitude increase in the leakage current. But for the very wide transistor also threshold voltage shift is more significant. These changes correlate also with the change in noise characteristics, especially for the bigger multi-finger device (Fig. I.21D).

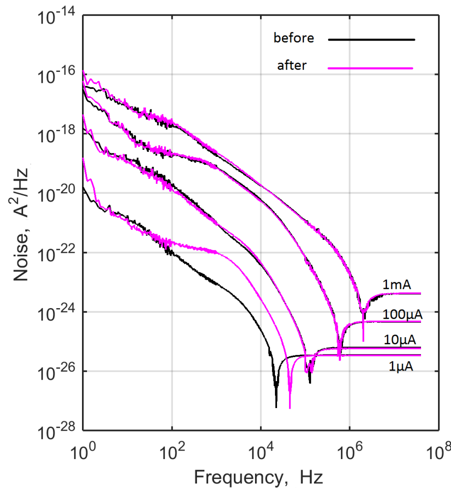
PMOS transistors are considered more robust to TID effects at moderate doses, where no rebound effect is observed and under normal operating conditions, trapping the charge at a much slower rate, compared to NMOS [51], [6]. Also the noise performance of these devices is supreme compared to NMOS equivalents [55]. Fig.I.22 depicts transfer and noise characteristics of the medium oxide PMOS transistors. Here the change after



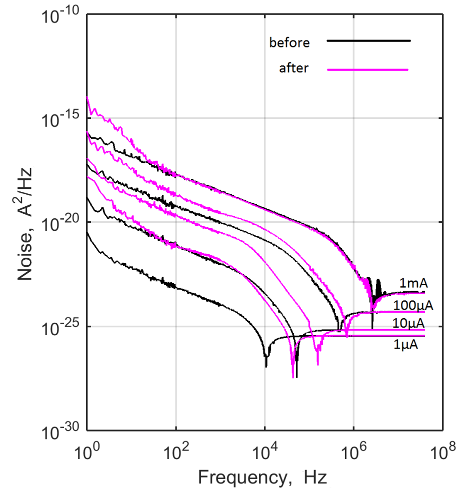
(A) Measured transfer characteristics of NMOS t_{GOX} >10 nm W/L = 12.5/0.9. Average of 4 samples



(B) Measured transfer characteristics of NMOS t_{GOX} >10 nm (W/L = 1000/0.9). Average of 4 samples.



(C) Measured $S_{I_{DS}}$ of NMOS t_{GOX} >10 nm (W/L = 12.5/0.9). Average of 2 samples.

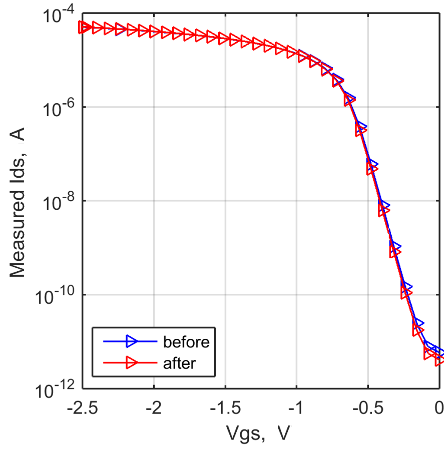


(D) Measured $S_{I_{DS}}$ of NMOS t_{GOX} >10 nm (W/L = 1000/0.9). Average of 2 samples

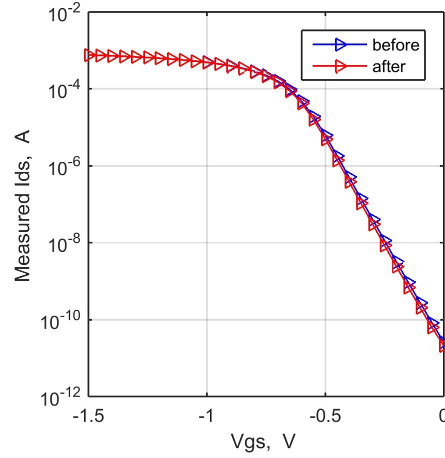
FIGURE I.21: Measured transfer characteristics (A, B) and noise $S_{I_{DS}}$ (C, D) of NMOS t_{GOX} >10 of different size before and after 15 krad TID under the worst case irradiation bias (condition B, average of 2 samples).

15 krad TID is minor both in DC and in noise characteristics. For the bigger multi-finger device, a slight decrease of the 1/f noise can be observed.

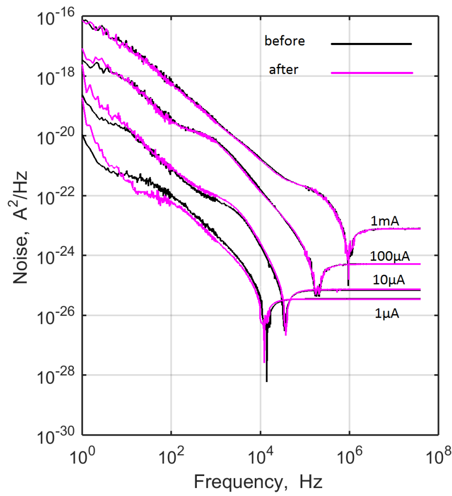
For the thin oxide devices, close to no measurable difference in transfer or noise characteristics could be detected. Fig. I.23 illustrates noise characteristics of thin oxide NMOS and PMOS transistors with W/L=1000/0.36. Deviations of the post-irradiation characteristics from pre-irradiation of the NMOS transistor can both originate from



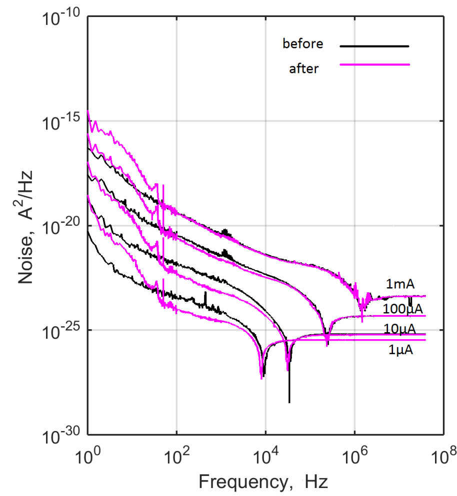
(A) Measured transfer characteristics of PMOS t_{GOX} >10 nm (W/L = 12.5/0.7). Average of 4 samples.



(B) Measured transfer characteristics of PMOS t_{GOX} >10 nm (W/L = 1000/0.7). Average of 4 samples.



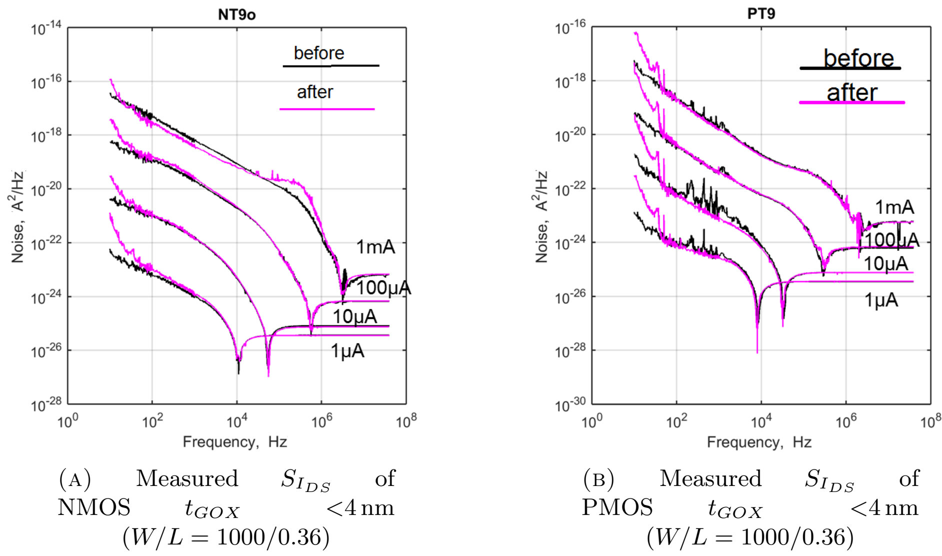
(C) Measured $S_{I_{DS}}$ of PMOS t_{GOX} >10 nm (W/L = 12.5/0.7). Average of 2 samples.



(D) Measured $S_{I_{DS}}$ of PMOS t_{GOX} >10 nm (W/L = 1000/0.7). Average of 2 samples.

FIGURE I.22: Measured transfer characteristics (A, B) and noise $S_{I_{DS}}$ (C, D) of PMOS transistors before and after 15 krad TID.

measurement set-up variations (see Appendix A) and recombination of process induced interface traps, similar to medium oxide PMOS devices. For PMOS, these deviations clearly lie within measurement accuracy. The observed negligible change in the noise characteristics of the thin oxide devices thus once again proves higher robustness of the thin gate oxide transistors to ionizing radiation.



(A) Measured $S_{I_{DS}}$ of NMOS t_{GOX} <4 nm ($W/L = 1000/0.36$)

(B) Measured $S_{I_{DS}}$ of PMOS t_{GOX} <4 nm ($W/L = 1000/0.36$)

FIGURE I.23: Measured noise $S_{I_{DS}}$ of t_{GOX} <4 nm ($W/L = 1000/0.36$) NMOS (A) and PMOS (B) before (black) and after (magenta) 15 krad TID. Average of 2 samples.

Although thin oxide transistors are known to be more robust against TID, thicker oxide devices are still unavoidable in some circuit blocks, e.g. interfacing stages, where high dynamic ranges are desired. An important conclusion for noise sensitive design in this case is that for wide channel devices already at 15 krad TID $1/f$ noise of very wide NMOS devices increases. For example, the $1/f$ noise current in 1000 μm/0.9 μm transistor increases from 10 nA$_{RMS}$ to 30 nA$_{RMS}$ at the bandwidth between 10 Hz and 1 kHz and the DC current I_{DS}=100 μA. The PMOS transistors show slight improvement of the $1/f$ noise in the frequency range between 100 Hz and 1 kHz at 15 krad TID, which is a practical feature, since PMOS transistors already have supreme noise behaviour. These results point out the significance of TID effects on thick gate oxide MOS transistors in state-of-the-art technologies at very low doses, previously not reported.

3 Radiation Hardening by Design

Based on the experimental and simulation results discussed in the section above, radiation hardening by design can be implemented. In my work I present the first comprehensive summary of the radiation aware design techniques, applicable in the standard industrial product development process. The advantage of such summary is that it is directly implementable into a commercial CMOS process circuit development flow. First, because this set of techniques is structured in a similar way as typical process related

design guidelines. Secondly, because it gives a quick and comprehensive overview of design decisions and risks connected to them.

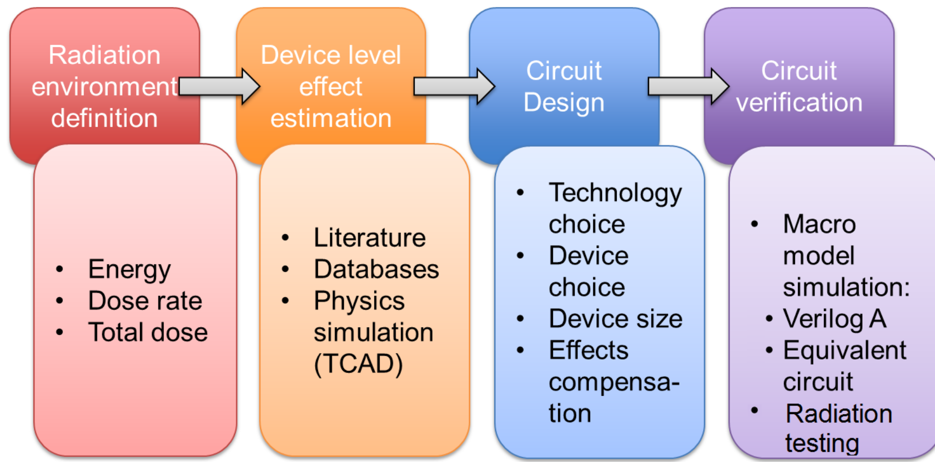


FIGURE I.24: Radiation aware IC development flow.

Radiation aware IC development involves a broad competence and tool portfolio (Fig. I.24). To start with radiation hard design, one has to know the expected operation environment, including type of source, its energy, dose rate and expected total dose. Then the expected effect on the single devices and circuit blocks can be estimated based on the literature studies, taken from databases or with the help of multi-physics simulation tools like Sentaurus TCAD [56]. For example, the comprehensive overview of X-ray effects resulting from my theoretical and empirical investigations, presented earlier in this chapter, can be used for this purpose. With this knowledge, the radiation hardened circuit design can be approached, as covered in this section. Afterwards the circuit can be verified with the help of techniques presented in the next chapters. If the result is satisfactory the development goes to the prototype stage, otherwise some of the steps have to be repeated.

Radiation hardening can be achieved on multiple levels: by technology, device or circuit hardening on layout and topology levels (Fig. I.25). The process can be generally subdevided into three phases: basic level radiation hardening, radiation hardness estimation and residual radiation hardening (Fig. I.26). In this chapter I cover basic level radiation hardening. This involves radiation aware design decisions on device and topology choice. Techniques and methods proposed in this section can help to avoid radiation hardness requirements related design iterations and save thus development and production costs. This way, residual radiation hardening, such as system level hardening by means of shielding or software techniques can be minimized or even avoided. The important link

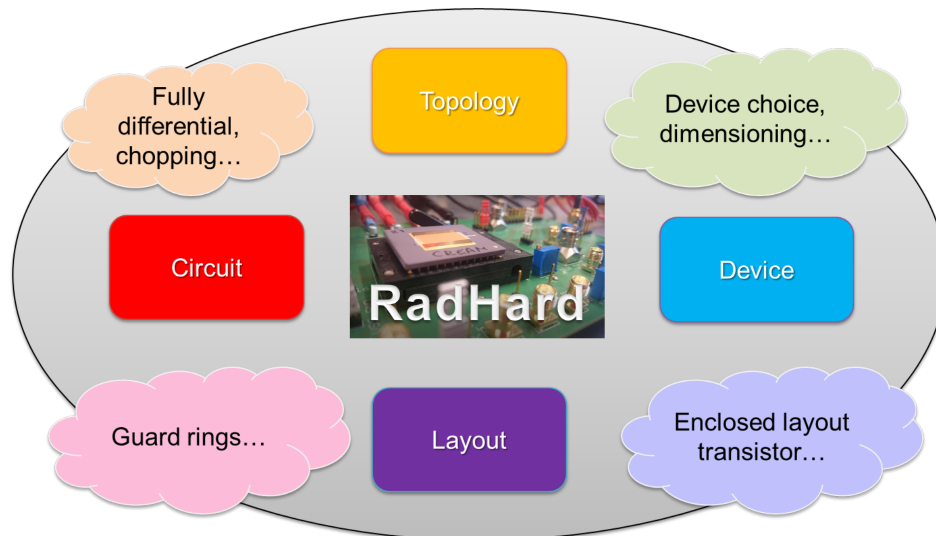


FIGURE I.25: Possible approaches to radiation hardening

between the two radiation hardening phases, the effect propagation analysis and risk management will be covered in the next chapter.

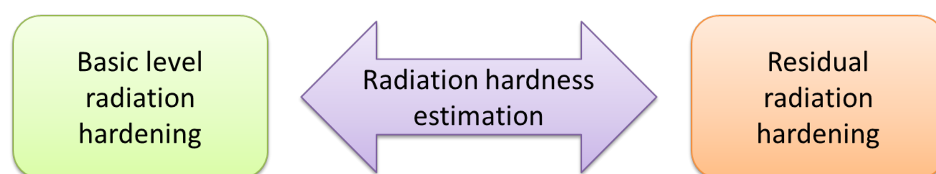


FIGURE I.26: Three phases of radiation hardened design

The general approach to basic level radiation hardening consists of the following steps: technology and process options choice, device choice, device dimensioning and physical realization. The residual effects on circuit level can be then estimated within SPICE simulation (e.g. in Cadence Virtuoso) with the help of the models proposed in Chapter 2 and compensated on topology level. Additionally, radiation effects can be limited by lowering operating voltages of the circuit [47], [48] or by the means of software [57]. These approaches to radiation hardening, however, lie beyond the scope of this thesis. The radiation hardened design flow is visualized in Fig. I.27.

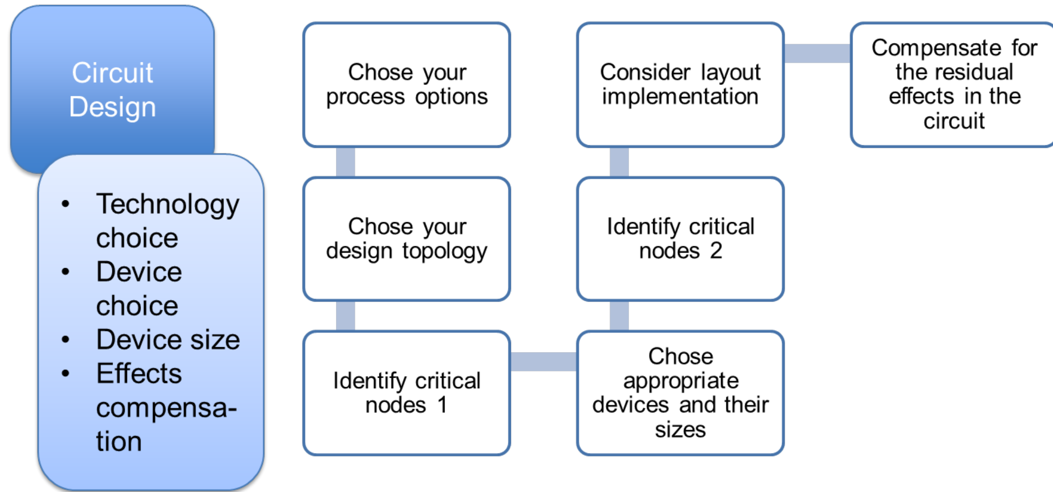


FIGURE I.27: Radiation aware circuit design flow

Technology and process options choice refers to the decision, which technology node is most suitable for the particular application, together with the estimation of its intrinsic radiation hardness, and choice of additional process options, enhancing radiation hardness. In this case, two considerations have to be taken into account: gate oxide thickness and device doping. The thinner the gate oxide, the more robust is the device against TID; and the higher the doping is, the less effect can be expected for the same TID.

Device choice refers to the particular transistor choice within the chosen technology node. Here, same considerations as in technology and process options choice apply, with less flexibility than in the first step. At this point it is also necessary to decide on the type of the device for the particular circuit nodes. As PMOS devices are more robust to TID they should be used in critical circuit nodes. NMOS devices, suffering more from TID effects have to be used with care and the effects have to be taken into account in circuit simulation.

Fig. I.28 visualizes priority of use of devices and options available within a CMOS process from the point of view of their intrinsic radiation hardness. It also points out measures, necessary for radiation hardness assurance in case of a particular transistor implementation. The fields marked green stand for minor TID effects and thus low risk, and red stands for severe TID parameter shifts and high risk. While one can implement devices from the upper part of the table without any additional radiation hardening considerations, the devices from lower part have to be radiation hardened to be able to

Just do nothing

Know your effect

Compensate for the effect

Use only with special mitigation!

Priority of use	Gate oxide thickness	Transistor Type	V_{th} option (doping)
1	<u><4nm</u>	PMOS	High
2			Standard
3			Low
4		NMOS	High
5			Standard
6			Low
7	4nm<tox<10nm	PMOS	High
8			Standard
9			Low
10		NMOS	High
11			Standard
12			Low
13	<u>>10nm</u>	PMOS	High
14			Standard
15			Low
16		NMOS	High
17			Standard
18			Low

FIGURE I.28: Priority of devices and device options use for radiation hard design valid up to 1 Mrad TID

operate after 300 krad TID. The underlined t_{GOX} <4 nm and t_{GOX} >10 nm indicate gate oxide thickness of the devices implemented on the test-chips within my PhD research.

Dimensioning is the next important step in radiation tolerant circuit design. RISCE and RINCE effects should be avoided. This means, a good design practice is to use devices with more than double minimal channel length, and with minimum 2 μm width for the CMOS process nodes between 180 nm and 65 nm. The minimal size devices (W_{min}/L_{min}) must be avoided at all times, as the effect on them is most enhanced. Also the upper limitation for length of the NMOS transistors, originating from the layout related effect of gate extension area, has to be carefully considered in designs, where very long channel transistors are required. The summary of the transistor dimensioning guideline is given in Table I.4.

Physical realization or layout is the final consideration of the basic level radiation hardening. At this point, the gate extension area effect has to be considered. The compromise between conventional reliability, area, circuit performance and radiation

TABLE I.4: MOS transistor dimensioning for radiation hardness

Transistror type	Channel length guideline	Finger width guideline
NMOS	$1.5L_{min} < L < 2.5L_{min}$	$W \geq 2\,\mu$m, the wider the better
PMOS	$L \geq 2L_{min}$	

hardness has to be done here, as minimizing gate extension area might require minimizing number of contacts and eventually asymmetrical realization of the transistor layout. Polysilicon routing, commonly used in digital cells for area optimization reasons should be avoided as well as redundant poly to metal contacts, increasing the polysilicon area. Another consideration during layout realization is implementation of ELTs where necessary. If the design incorporates thicker gate oxide NMOS transistors, it is strongly recommended to realize them as ELTs. Here the choice between ringed source and annular gate transistor can be made. The ringed source allows more flexibility in aspect ratio, but it is less robust than annular gate. Implementation of ELTs requires additional modelling effort to be able to simulate circuits incorporating such devices in a standard commercial design kit. The challenging task of ELT modelling is covered in the next chapter.

Finally, in addition to the single device layout, the **overall circuit** design and layout has to be considered. First of all, the radiation induced inter-device leakage currents (leakage current of the field oxide transistor structures) has to be minimized. This is achievable through the implementation of the guard rings, as a common good design practice recommends. Further, the possible transient currents with current density of few $fA/\mu m^2$ have to be taken into account in the circuit design, as in sensitive circuits and in big structures they might lead to circuit performance degradation.

Fig. I.29 illustrates different realizations of a simple CMOS inverter layout. The area optimized standard layout on Fig. I.29A has few potentially radiation soft spots: polysilicon routing between NMOS and PMOS leading to gate extension area TID enhancement, and linear layout of the NMOS transistor. Fig. I.29B-D demonstrate alternative realizations of the same standard cell. Here the trade-off between radiation hardness and other circuit parameters is highlighted once again, as all these techniques require higher circuit area and eventually lead to increased parasitics.

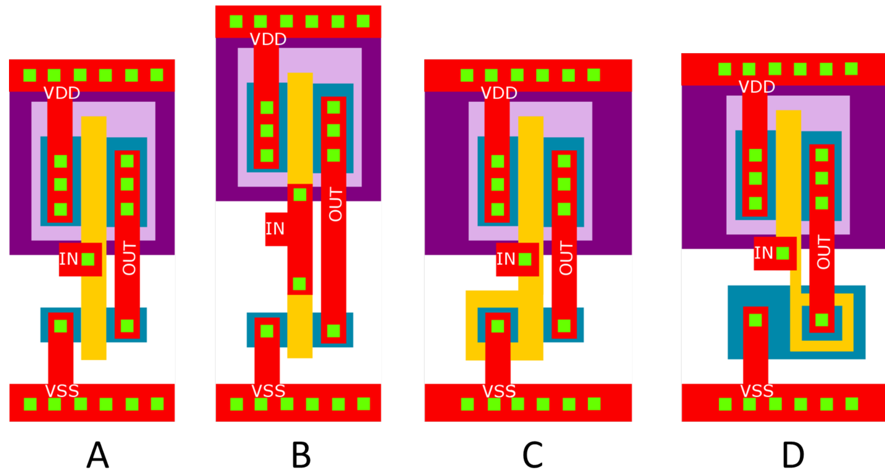


FIGURE I.29: Illustration of CMOS inverter layout: standard (A), with decreased gate extension area (B), with ringed source NMOS (C), and with annular gate NMOS (D)

Conclusion

Under the influence of X-rays integrated circuits change their behaviour and basic properties. In the course of my work I have studied these effects from different perspectives.

First, I have investigated transient effects of medium energy range X-rays on integrated circuits, not reported before. The effect is negligible up to dose rate of 300 rad/s. However, the actual effect on circuit performance has to be evaluated separately depending on the circuit topology and layout.

Secondly, I have presented TID effects on different types of diodes and have proven the major contribution of interface traps to the related parameter changes (ideality factor and saturation current) with a multi-physics simulation in Sentaurus TCAD. To the best of my knowledge such study has not been published before. These results, completed with on-going deep level spectroscopy measurement are currently in publication preparation and will be submitted for Transactions on Nuclear Science in the near future.

Thirdly, I have conducted methodical analysis of TID effects on MOS transistors. I have considered major aspects, enhancing or mitigating the effects. For the first time until now I have reported and analysed doping concentration influence on TID effects in MOS transistors within one technology node. With this study I have proven the hypothesis known from the literature, that the higher the doping is, the more robust the devices are to TID effects: on the one hand, doping influences the charge trapping process on the interface, on the other hand, more charge is required to achieve the same parameters

shift as in lower doping devices. I have also reproduced discoveries on size dependence of TID effects for a 180 nm CMOS technology [48], with a comprehensive set of data. This has allowed me to extrapolate my findings to formulate a general guideline for device dimensioning in order to avoid RINCE and RISCE. The unique empirical study of gate extension area influence on the TID effects supports the rare theoretical studies that can be found in literature. Thanks to the broad spectrum of custom-designed test devices in my experimental studies I was able to isolate gate extension area effect from RINCE and RISCE. This has allowed to derive precious guideline for radiation hardened circuit design. For the completeness of the study the ELTs were included. My experimental results support effectiveness of this mitigation technique not only against radiation induced current, but also for the STI contribution to the threshold voltage shift of medium gate oxide MOS transistors (NMOS and PMOS).

Fourthly, I have conducted a low dose effect study on the noise performance of different types of transistors [54]. The results have shown that medium oxide transistors are susceptible already to doses as low as 15 krad. The noise performance of NMOS transistors with t_{GOX} >10 nm becomes worse with increasing TID. The thin gate oxide devices are not susceptible to such low doses, as was expected.

Finally, from the achieved results I have derived a unique in its completeness and simplicity set of design guidelines. This set of guidelines can be easily incorporated in a standard IC development process in any commercial CMOS process with STI between 180 nm and 65 nm process nodes. Together with the results reported in this chapter, these guidelines can be a powerful radiation hardening tool for analogue designers.

Chapter II

Radiation Hardening Implementation Methodology

"...Always be wary of any helpful item that weighs less than its operating manual..."

—Terry Pratchett, "Jingo"

Introduction

Radiation hardness design guidelines are only one side of the radiation hardness implementation process. Implementation of these guidelines requires deep understanding of causes and consequences, and the trade-offs that have to be met. One of the powerful tools facilitating this decision process is modelling. In the course of my research I have extensively used macro-modelling [58]. In this chapter I deal with two aspects of such modelling.

First, I discuss device modelling. ELT is a reliable technique for TID mitigation. However, implementing such modified transistor into a circuit can cause some difficulties, due to unconventional geometry of the device. So, actual geometrical realization of such device often requires profound knowledge of fabrication process, as some device topologies are not conform with design rules of particular process (e.g. not all processes allow round gates). Also parasitics extraction and device model for circuit simulation present particular challenge. One of the ways to deal with the latter is to find an equivalent linear layout device with corresponding behaviour and use it as a macro-model

for ELT [59]. Here I present a comprehensive study of available ELT models and introduce an improved isosceles trapezoid model for annular gate transistor, as published in [60], [61] and presented at RADECS 2018 in Gothenburg [62].

Second, I describe macro-modelling approach to circuit level radiation effects estimation and analysis. This approach allows fast and simple pass/fail simulation of the circuit and facilitates analysis of the weak circuit nodes. I discuss this methodology on the example of two simple circuit blocks: a simple inverter and a bandgap voltage reference. These examples allow to unfold the capabilities of the simulation technique for circuit design, analysis and optimisation for radiation hardness.

1 Modelling of Enclosed Layout Transistor

As it was mentioned in the previous chapter, there are two basic types of enclosed layout transistor realization - the ringed source and the annular gate. Since these layouts have been introduced, many approaches were proposed for modelling of such device. The common way is to find an equivalent standard layout transistor. The first step here is to find equivalent channel dimensions. Although many different models for equivalent aspect ratio estimation can be found in literature [50], [63], [64], it is not always clear how to apply them to the particular layout realization according to design rules of a given process. In this section I give an overview of existing models and discuss their adaptations for different physical realizations of the layout [61], [60]. I also present my novel isosceles trapezoid model for annular gate aspect ratio estimation, as first reported by our group in [61], [60] and [62].

1.1 Ringed source models

As I have reported in [61] and [60], ringed source layout is not a very popular radiation hardening technique, as such transistors suffer more TID induced parameter shift than annular gate devices. However, the ringed source layout allows more flexibility in aspect ratio and is easier to realize without design and process rules violation. Such transistor also has lower total area consumption in comparison with an annular gate device. Still, taking into account low popularity of ringed source layout, only few models have been developed for equivalent channel dimensions calculation.

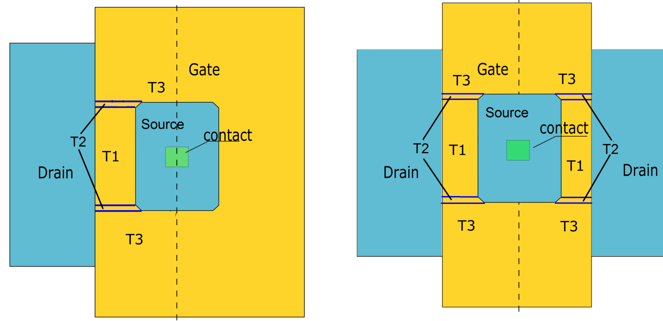


FIGURE II.1: Possible realizations of ringed source layout

Here I discuss two major contributions: by Nowlin et al. [50] and by Ramos-Martos et al. [65], which is an extended version of [50]. Fig. II.1 illustrates two of many possible realizations of the ringed source layout. In order to estimate equivalent aspect ratio according to [50] and [65] such transistor is sub-divided into 5 main regions. The "as drawn" transistor region T1 is the most straightforward to understand, with the constant width and length of the channel across this sub-section. The edge regions with constant width and variable length are marked as T3, and the T2 corner regions are the most challenging with variation of length and width of the channel across them. In the models proposed in [50] and [65] it is assumed that only the part of the gate to the left of the source region middle-line (marked with dashed line) is contributing to effective W/L. This is illustrated by Fig. II.2. The effective total aspect ratio of the ringed source transistor according to [50] can be calculated as follows:

$$\frac{W}{L} = m \cdot (\frac{W}{L})_1 + n \cdot ((\frac{W}{L})_2 + (\frac{W}{L})_3) \tag{II.1}$$

where m is the number of drains, and n is the number of corners per drain; for example in Fig. II.2: $m = 1$ and $n = 2$.

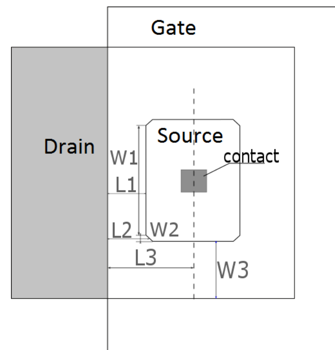


FIGURE II.2: Geometrical model of single drain ringed source transistor.

For this model it can be assumed the corner contributions are overestimated [50]. In order to correct for this overestimation the n coefficient can be used as a fitting parameter.

Additional correction of the model accuracy with empirical coefficients was proposed by Ramos-Martos et al. in [65]. Model for single drain transistor is defined as follows:

$$\frac{W}{L} = (\frac{W}{L})_1 + 2 \cdot ((\frac{W}{L})_2 + \frac{2 \cdot n_c + 3}{4} \cdot (\frac{W}{L})_3) \tag{II.2}$$

where n_c is number of source contact rows.

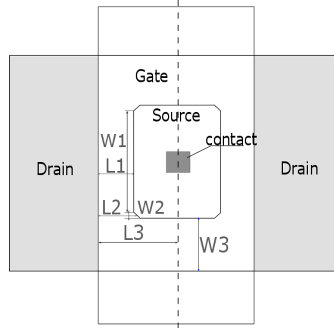


Figure II.3: Geometrical model of double-drain ringed source transistor.

In the case of double-drain transistor, as illustrated in Fig. II.3, equivalent aspect ratio is calculated as follows:

$$\frac{W}{L} = 2 \cdot (\frac{W}{L})_1 + 4 \cdot ((\frac{W}{L})_2 + \frac{n_c + 5}{6} \cdot (\frac{W}{L})_3) \tag{II.3}$$

Such modelling approach allows to vary empirical coefficients to achieve the best fit for the particular design solution. The main drawback is that one has to have extensive experimental data on the devices planned for use in the design in order to determine suitable coefficients, as the presented coefficients are valid for a specific process and realization of the layout.

Still, these models give good first approximation of the equivalent aspect ratio, as can be taken from Table II.1. Here the equivalent aspect ratio of different test structures calculated according to the presented models and extracted from measured transfer characteristics of the devices is summarized. Device names are according to their designation on test chip MiAMoRE (see Appendix A).

TABLE II.1: Equivalent aspect ratio of ringed source transistors

Device name	W/L after [50]	W/L after [65]	W/L extracted from measurements
PTrs1	4.6	4.9	4.3
PTrs3	39.4	42.9	38.6
PM1rs	2.4	2.7	2.9
PM3rs	22.1	26.3	25.7
NTrs1	4.6	4.1	4.5
NTrs2	7.7	8.6	8.2
NTrs3	39.4	42.9	43.5
NMrs1	1.9	2.1	2.3
NMrs2	3.3	4.5	4.1
NMrs3	16.2	19.3	19.9

1.2 Annular gate models

Annular gate layout is a very popular radiation hardening technique to mitigate radiation induced leakage current. It has been first proposed by Snoeys and his team [46], [66] in early 2000s and is widely used ever since. That is why many models of such transistor are available. However, it is not always easy to apply one of such models to a particular transistor realization.

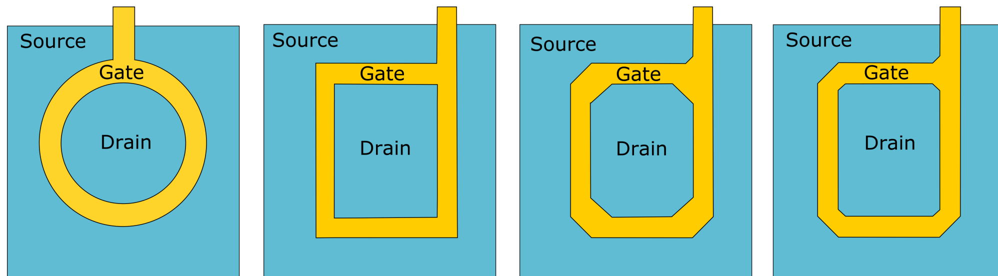


FIGURE II.4: Different realizations of annular gate layout

Fig. II.4 illustrates few out of many different ways to realize annular gate layout. The main difference between the possible realizations lies in the gate geometry. The implementation depends on the fabrication process and connected with it design rules. Also, optimization of area and parasitic capacitance play a great role in final layout configuration choice. In my work I consider four major available models for equivalent aspect ratio estimation of annular gate transistor, together with my novel isosceles trapezoid approximation, as first reported in [61]. I point out the challenges of existing models application and analyse their accuracy. I also propose adaptation of one of the models to a particular layout style, optimized for minimal area. I describe the novel isosceles

trapezoid approximation as geometry independent annular gate model. Finally, I extend the annular gate modelling with additional stress effects, such as STI stress [67].

The three major annular gate transistor models, popular within community, come from groups of Snoeys [66], Giraldo [63] and Xue [64]. The fourth one, popular for its simplicity and geometry independence, is the mid-line approximation. As most commercial fabrication technologies do not allow circular geometries, only square and cut-corner models are discussed. The test structures implemented in my study are cut-corner annular gate transistors, optimized for minimal area, as shown in Fig. II.5.

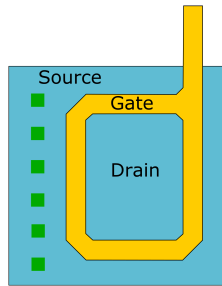
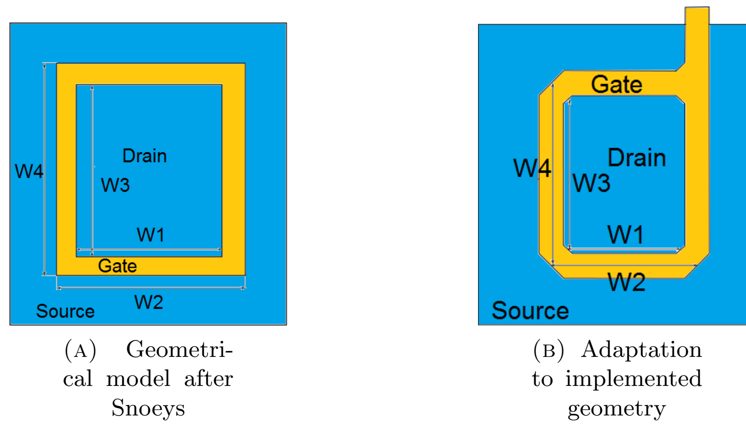


FIGURE II.5: Area optimized annular gate transistor.



(A) Geometrical model after Snoeys

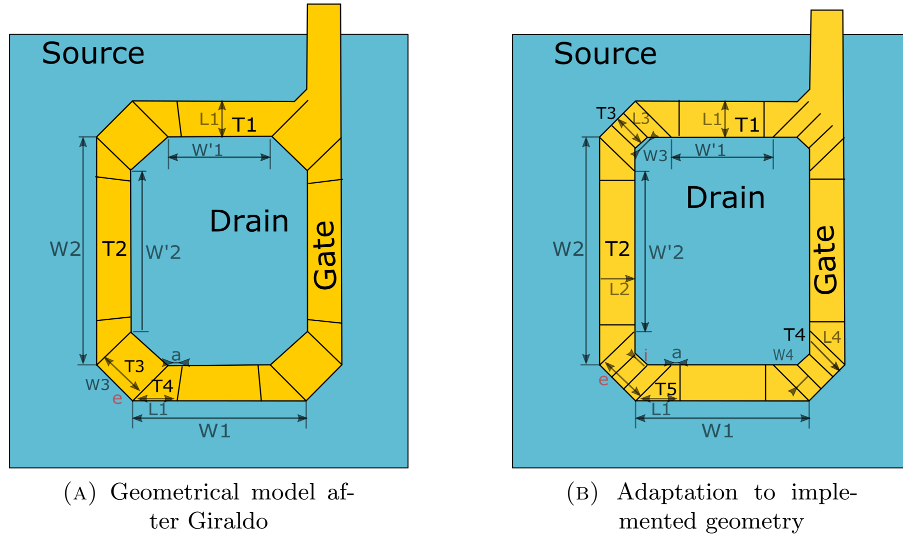
(B) Adaptation to implemented geometry

FIGURE II.6: Geometrical model of annular gate transistor after Snoeys (A) and its adaptation to cut-corner geometry (B).

The first model considered is the one proposed by Snoeys and his group in [66]. Here they present a model for a rectangular annular gate transistor, as shown in Fig. II.6A. The equivalent aspect ratio is calculated as follows:

$$\frac{W}{L} = \frac{4}{ln\frac{W_2}{W_1}} + \frac{4}{ln\frac{W_4}{W_3}} \tag{II.4}$$

Clearly, this model has to be adjusted for application to other layout geometries. Fig. II.6B depicts such adjustment for the cut-corner transistors as implemented in this study.



(A) Geometrical model after Giraldo

(B) Adaptation to implemented geometry

FIGURE II.7: Geometrical model of annular gate transistor after Giraldo (A) and its adaptation to realization with different inner and outer cut-corner dimensions (B).

The second model considered is the one proposed by Giraldo and his group in [63]. Here they propose to sub-divide the annular gate transistor into 3 types of sub-transistors, as depicted in Fig. II.7A, using conformal mapping technique. The equivalent aspect ratio is then defined as:

$$\frac{W}{L} = 4 \cdot 2\left(\frac{a}{ln(\frac{W_1'}{W_1'-2aL})} + \frac{1}{\Delta(a)}\frac{1-a}{-ln(a)} + \frac{1}{2}\frac{e}{L_1\sqrt{2}}\right) \tag{II.5}$$

where $\Delta(a)$ is defined as:

$$\Delta(a) = \frac{1}{2}\sqrt{a^2+2a+5} \tag{II.6}$$

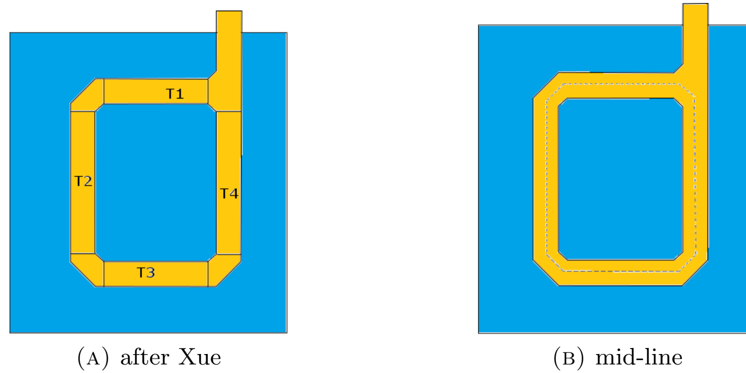
In this model, the length of the inner and outer corner "cuts" is equal (parameter e in Fig. II.7A). In the area optimized layout the inner (parameter i in Fig. II.7B) and outer (parameter e in Fig. II.7B) cuts are not equal, thus the model from [63] has to be adapted. Here I propose an adaptation as illustrated in Fig. II.7B. In this case the annular gate transistor in sub-divided into five different sub-transistors instead of four:

$$\frac{W}{L} = 2 \cdot ((\frac{W}{L})_1 + (\frac{W}{L})_2 + 2 \cdot (\frac{W}{L})_3 + 4 \cdot ((\frac{W}{L})_4 + (\frac{W}{L})_5)) \tag{II.7}$$

A simpler approach has been proposed by Xue et al. in [64], where they suggest to subdivide the annular gate transistor into four linear layout sub-transistors, and to compensate for corners contribution with an empirical coefficient. The geometrical model is illustrated in Fig. II.8A. Equivalent aspect ratio is then calculated as follows:

$$\frac{W}{L} = \sum \frac{W}{L}_i + C_{ab} \tag{II.8}$$

where W_i and L_i are width and legth of the transistor T_i correspondingly, and C_{ab} is the empirical coefficient.



(A) after Xue

(B) mid-line

FIGURE II.8: Geometrical model of annular gate transistor after Xue (A) and the mid-line approximation model (B).

The fourth state-of-the-art model for equivalent aspect ratio calculation is the mid-line approximation. It is illustrated by Fig. II.8B. The dashed line represents the middle of line of the transistor channel. Along this line, average width and average length of the annular gate is taken as equivalent aspect ratio. The great advantage of such method is its independence of the layout realization. However, it is less accurate than other models, optimized for their particular use cases [61].

The accuracy of the presented models is given in Table II.2, where equivalent aspect ratio according to four discussed models together with the aspect ratio extracted from measured transfer characteristics of the annular gate transistors are summarized. Device names are according to their designation on test chip MiAMoRE (see Appendix A). The

estimation error related to the extracted aspect ratio is given in Table II.3. As it can be seen, all models result in differently accurate estimation for different actual transistors.

TABLE II.2: Equivalent aspect ratio of annular gate transistors

Device name	W/L after [66]	W/L after [63]	W/L after [64]	W/L by mid-line	W/L extracted from measurements
PTann3	36.2	36.2	34.5	35.1	31.6
PMann3	22.6	19.3	19.9	18.6	17.2
NTann3	36.2	36.2	34.5	35.1	34.9
NMann3	12.9	15.3	13.1	12.9	13.8

TABLE II.3: Error of equivalent aspect ratio of annular gate transistors related to extracted W/L

Device name	W/L after [66]	W/L after [63]	W/L after [64]	W/L by mid-line
PTann3	14%	14%	9%	11%
PMann3	31%	12%	15%	8%
NTann3	4%	4%	-1%	0.5%
NMann3	-6%	10%	-5%	-6%

In order to combine the advantages of the physical estimation correctness and geometrical independence, I have proposed a novel isosceles trapezoid approximation for equivalent aspect ratio estimation [61], [62]. This method is based on the approach from [63], but uses different transistor subdivision. It is illustrated by Fig. II.9.

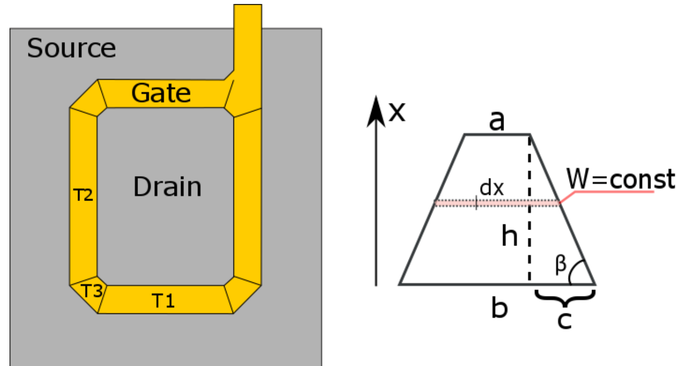


FIGURE II.9: Isosceles trapezoid approximation for equivalent aspect ratio calculation of an annular gate transistor.

In this model, unlike above reported ones, the annular gate transistor is subdivided into isosceles trapezoids. Then, similar to [63], aspect ratio of sub-transistors is derived from the drain-source current I_{DS} definition as follows [62]:

$$I_{DS} = -W \cdot Q_{inv}(x) \cdot v(x) \tag{II.9}$$

where velocity $v(x)$ is defined as:

$$v(x) = \mu_n \frac{dV}{dx} \tag{II.10}$$

with μ_n being electrons mobility; and the charge $Q_{inv}(x)$ equals to:

$$Q_{inv}(x) = -C_{ox}(V_{GS} - V(x) - V_{th}) \tag{II.11}$$

where C_{ox} is oxide capacitance, V_{GS} is gate-source voltage and V_{th} is threshold voltage. Substituting (II.10) and (II.11) into (II.9) we obtain:

$$I_{DS} = W \cdot C_{ox}(V_{GS} - V(x) - V_{th}) \cdot \mu_n \frac{dV}{dx} \tag{II.12}$$

The width W of the transistor is then moved to the left side of (II.12) and integrate it along the x-axes, as indicated in Fig. II.9:

$$\int_0^h I_{DS} \frac{dx}{W} = C_{ox} \cdot \mu_n \int_0^{V_{DS}} (V_{GS} - m \cdot V_{CS} - V_{th}) \; dV_{CS} \tag{II.13}$$

The boundary conditions of the expression are defined as follows:

$$W(x) = b - \frac{2}{\tan \beta} \cdot x \tag{II.14}$$

$$W(0) = b \tag{II.15}$$

$$W(h) = a = b - 2c = b - \frac{2h}{\tan \beta} \tag{II.16}$$

This allows the following description:

$$\int_0^h \frac{dx}{W(x)} = \int_0^h \frac{dx}{b - \frac{2x}{\tan \beta}} \tag{II.17}$$

$$\int_0^h \frac{dx}{W(x)} = -\frac{\tan\beta}{2} \ln(b \cdot \tan\beta - 2x)|_0^h \tag{II.18}$$

$$\int_0^h \frac{dx}{W(x)} = -\frac{\tan\beta}{2} \ln(1 - \frac{2h}{b \cdot \tan\beta}) = \frac{L}{W} \tag{II.19}$$

The total equivalent aspect ratio is then sum of the single sub-transistors equivalent aspect ratios, calculated according to (II.20):

$$\frac{W}{L} = -\frac{2}{\tan\beta \cdot \ln(1 - \frac{2h}{b \cdot \tan\beta})} \tag{II.20}$$

In order to evaluate this new equivalent aspect ratio calculation model, transfer characteristics of annular gate and standard layout transistors designed with the same aspect ratio have been measured and compared [62].

Fig. II.10 illustrates the test structures of this investigation: the area optimized annular gate transistor, and two linear layout transistors of the same dimensions with different diffusion region extension (RX). Different RX of the transistors allow to evaluate the influence of additional stress factors, such as STI stress [67] on the results.

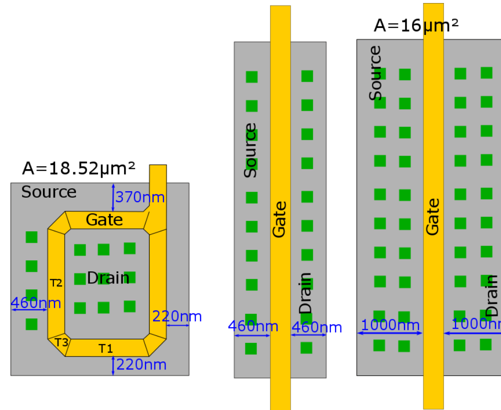


Figure II.10: Implemented test structures

The measured transfer characteristics of the above shown transistors are depicted in Fig. II.11. The difference between these measurement results is significant, although transistors were designed with the same aspect ratio. Such differences are caused by STI stress effect [67]. Fig. II.12 compares measured and simulated transfer characteristics of standard layout transistors with different STI stress levels. Simulation result for

RX=460 nm is much closer to the measurement result of the same transistor, than unstressed simulation to the RX=1000 nm measurement. That is why for accurate comparison of the annular gate transistor and standard layout transistor more precise definition of STI stress than available in the standard vendor's simulation models is necessary.

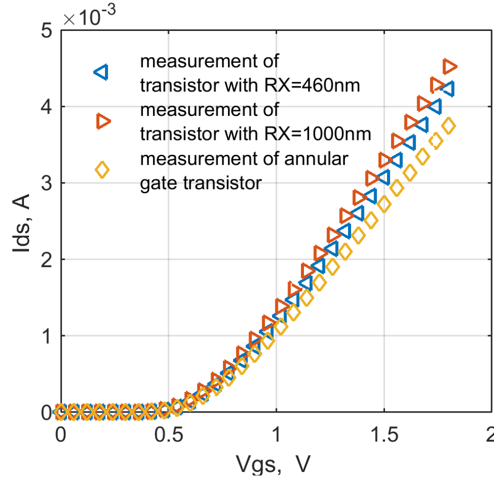


FIGURE II.11: Measured transfer characteristics of the two standard NMOS transistors with different RX and an annular gate transistor at $V_{ds} = 1.8\,V$

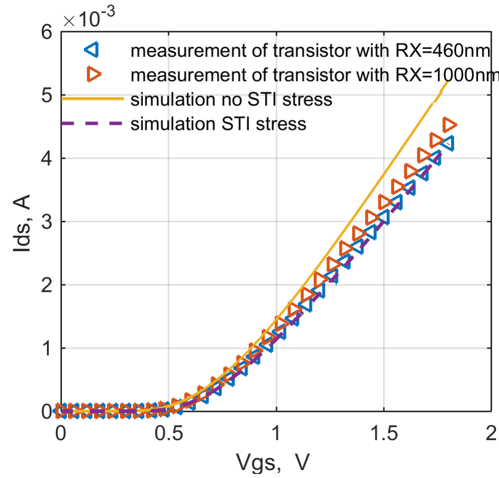
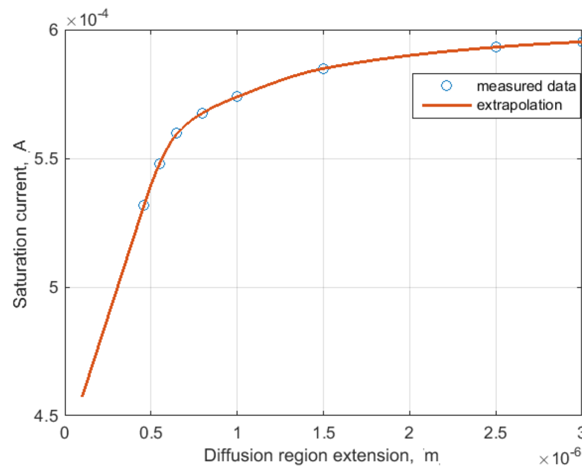


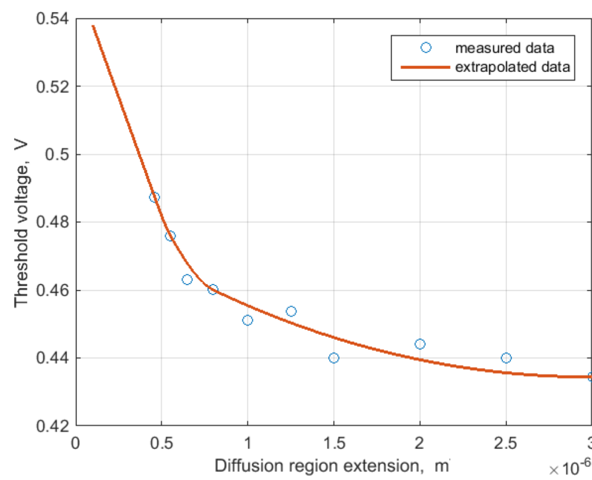
FIGURE II.12: Measured transfer characteristics of the two standard NMOS transistors with different RX and simulation with and without STI stress at $V_{ds} = 1.8\,V$

From Fig. II.10 it can be assumed that the annular gate transistor suffers even higher STI stress than the standard layout one with RX=460 nm. In order to estimate the actual STI stress on the annular gate transistor, extrapolation of the parameters degradation as a function of RX has been performed. The results of this extrapolation are illustrated by Fig. II.13. These results have been consequently incorporated into macro-model simulation, as shown in Fig. II.14. This macro-model consists of sub-transistors with equivalent aspect ratio, calculated according to (II.20). For each sub-transistor,

corresponding level of STI stress in form of threshold voltage shift and saturation current degradation, as obtained from extrapolation, was introduced.



(A) Saturation current



(B) Threshold voltage

FIGURE II.13: Extrapolation of saturation current (A) and threshold voltage V_{th} (B) as a function of diffusion region extension RX

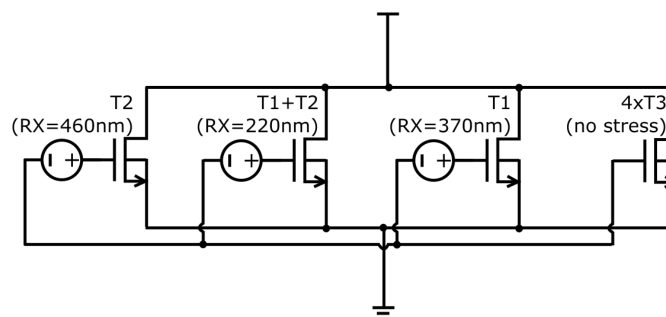


FIGURE II.14: Equivalent sub-circuit simulation model for STI stress simulation in an asymmetrical annular gate transistor

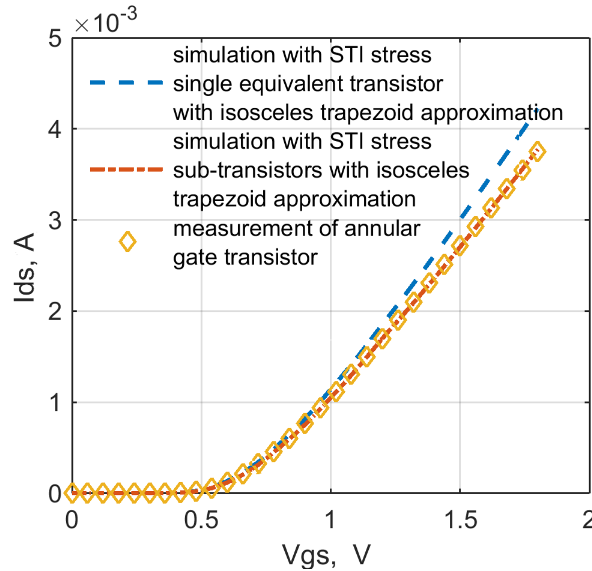


Figure II.15: Measured transfer characteristics of the annular gate transistor and simulation of the single equivalent standard transistor with STI stress and of the sub-circuit model with corresponding STI stress at $V_{ds} = 1.8\,V$

Fig. II.15 shows measured transfer characteristics of annular gate transistor together with two simulation results: for the equivalent standard layout transistor, calculated by isosceles trapezoid model, and for the sub-circuit model, incorporating STI stress at each single sub-transistor calculated by isosceles trapezoid model. Fig. II.16 illustrates the relative error of the equivalent aspect ratio models between the simulated and measured transfer characteristics for isosceles trapezoid model and mid-line approximation. Lower than 3% error can be achieved with isosceles trapezoid model when taking into account STI stress.

This proves the universality of the isosceles trapezoid model from two prospectives: on the one hand, it allows geometrical flexibility sustaining very high accuracy, on the other hand, it allows simple macro-model incorporation of additional stress effects, such as STI stress.

2 Modelling of Circuit Radiation Effects

The concept of macro-modelling is not only applicable to modelling of special layout devices like ELT [59], but also for the integration of radiation effects into circuit simulation [58]. In the frame of my work I apply this concept to analyse effectiveness of the proposed radiation hardness design guidelines on selected circuit blocks. For this I

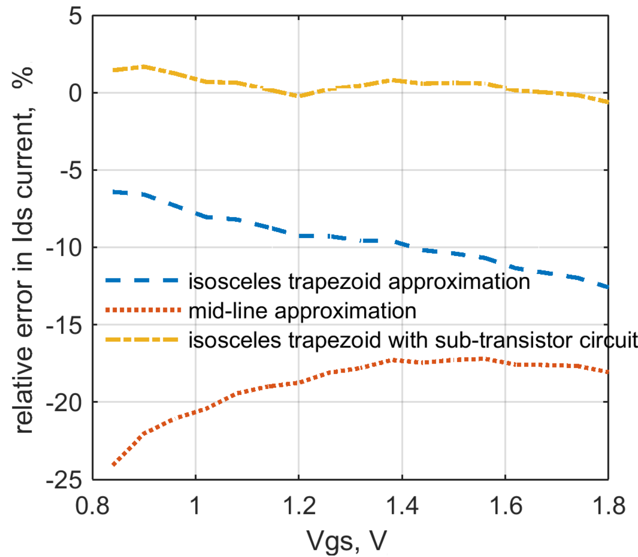


FIGURE II.16: Relative error of approximation models between simulated and measured transfer characteristics

introduce simple macro-model of TID effects on DC characteristics of the single devices, incorporating parameter shifts according to my experimental results and conduct circuit simulations with these models in Cadence environment using Spectre simulation tool.

Within this section I present three case studies on two simple circuit blocks: an inverter and a bandgap voltage reference. These circuit blocks were chosen for this study because they are present in most complex circuit designs. Also, these circuits illustrate well the connection between single device parameters shift and circuit performance change. The most common devices within considered circuit blocks are MOS transistors and diodes.

Fig. II.17 illustrates the used macro-models of NMOS and PMOS transistors. Here, threshold voltage shift is represented by additional DC voltage source at the gate. The radiation induced leakage current is implemented only in NMOS transistor, as increase of PMOS leakage current due to TID is negligible compared to process and temperature related leakage current variation.

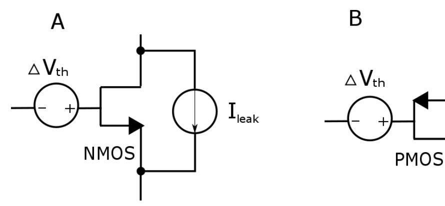


FIGURE II.17: Macro-model of TID induced DC parameter shift of NMOS (A) and PMOS (B) transistors

The behavioural macro-model of a diode is expressed with the diode equation and variable parameters included in it: ideality factor n and saturation current I_s, as in II.21.

$$I_{diode} = I_s \cdot (\exp^{\frac{V_{diode}}{n \cdot V_T}} - 1) \tag{II.21}$$

2.1 Inverter case study

A simple CMOS inverter can be found in most ICs. It is used in digital as well as in analogue circuits and often serves as a test vehicle for process characterisation [68], [69]. That is why I have chosen it for this case study. On the one hand, change in inverter characteristics is easy to follow down to single device characteristics change; on the other hand, it is easy to compare effectiveness of different radiation hardening measures on such simple circuit.

First, the TID effect on a simple inverter, as shown in Fig. II.18 is analysed. Fig. II.19 is an illustration of TID effects on the transfer characteristics of such inverter. This subject has been discussed in detail in my master thesis [70]. Decrease in output voltage at "high" originates from voltage drop across the on-resistance of PMOS transistor with leakage current of the NMOS transistor flowing through it. Threshold shift of the inverter is caused by both leakage current of NMOS and threshold voltage shift of NMOS and PMOS, whereas NMOS threshold voltage shift is dominant at TID below 1 Mrad.

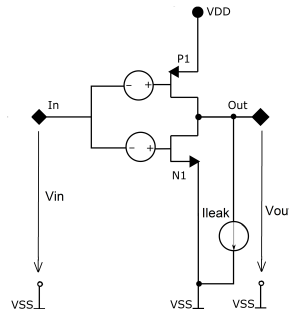


FIGURE II.18: Schematics of inverter macro-model incorporating TID effects.

Within this work I present a case study demonstrating effect of radiation aware transistor dimensioning on TID induced inverter parameters shift. I also compare simulation results with experimental results obtained from MiAMoRE test chip (see Appendix A).

In the simulation my empirical values of single device parameter shifts for 300 krad TID, as reported in Chapter I, are used. These results have been obtained in the course of my

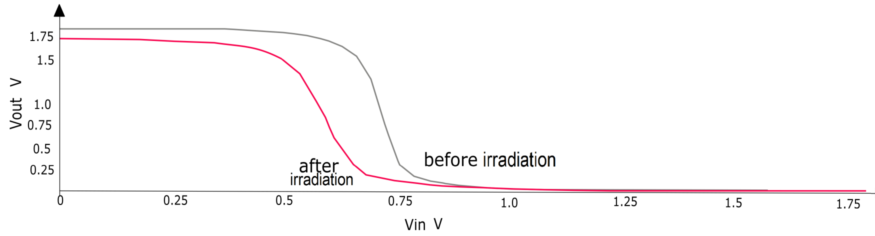


FIGURE II.19: TID effects on inverter transfer characteristics.

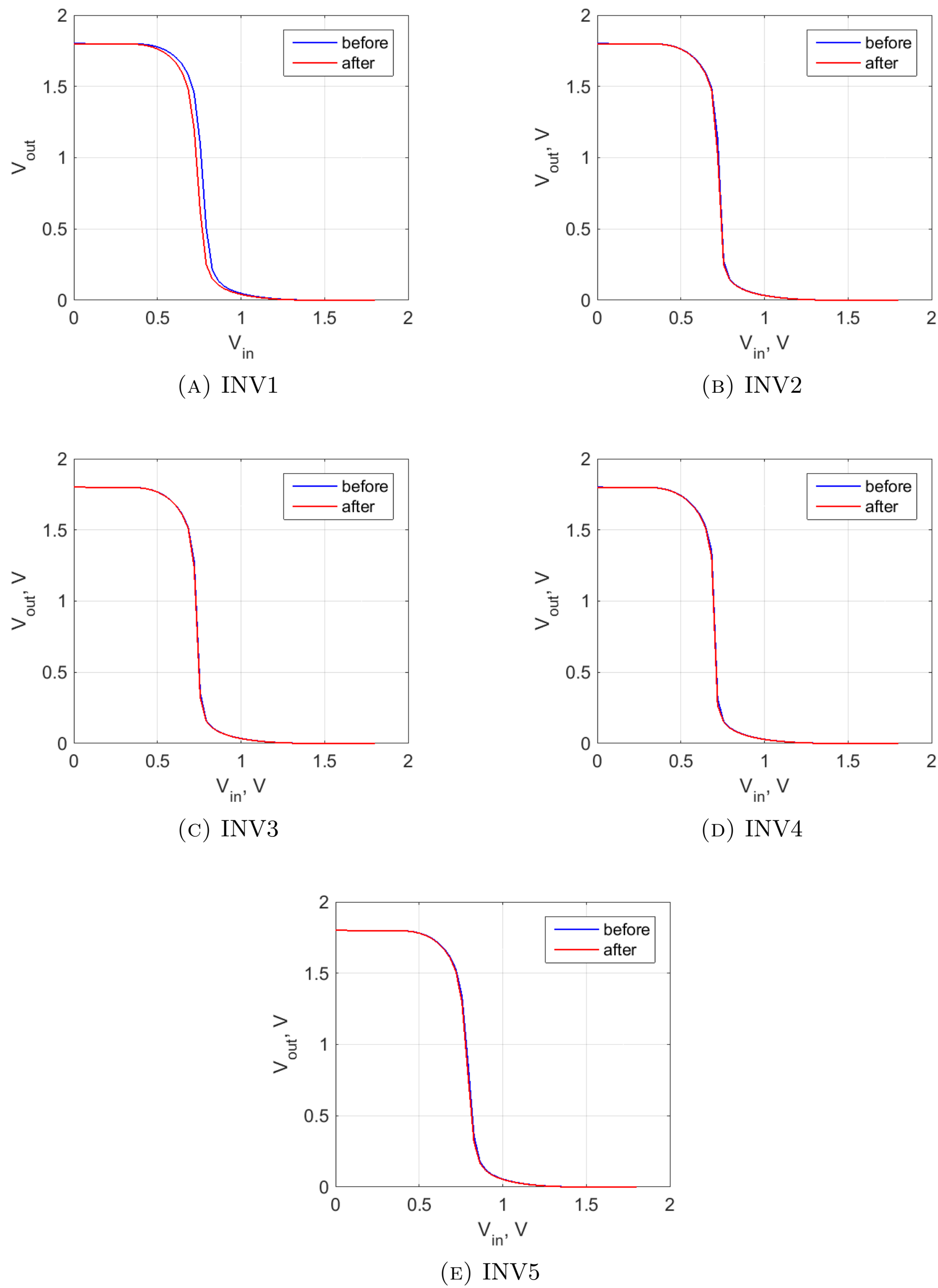
experiments described in Appendix A. The measurement results on a standard inverter implemented on MiAMoRE test chip presented later on have also been obtained from the same experiments (Appendix A).

TABLE II.4: Dimensions of simulated inverters

Inverter name	PMOS		NMOS	
	W, nm	L, nm	W, nm	L, nm
INV1	400	180	350	180
INV2	800	360	700	360
INV3	2400	360	2100	360
INV4	2400	1080	2100	1080
INV5	2400	180	2100	180

Table II.4 summarizes the simulated inverters dimensions. The dimensions were chosen as follows. INV1 corresponds to the minimal standard inverter available in a commercial 180 nm CMOS design kit. Transistors within this inverter suffer the most severe TID effects, enhanced by both RINCE and RISCE. INV2 is scaled by 2 to maintain the same W/L ratio for the single transistors; in this inverter no more RISCE is present, but still some RINCE. INV3 eliminates RINCE effect, maintaining relation between PMOS and NMOS currents, but changing W/L ratio of single transistors. INV4 maintains W/L ratio of the single transistors and eliminates both RINCE and RISCE. INV5 maintains relation between PMOS and NMOS, changing W/L of single transistors; here RINCE is mitigated, but not RISCE. The length of transistors is kept short to maintain the speed of the inverter as much as possible.

Fig. II.20 depicts the simulation results. Here transfer characteristics of the five inverters with different dimensions before and after irradiation are shown. The curve "after" is obtained by incorporating single device parameter shifts into the model depicted in Fig. II.18. From the plots it can be concluded that INV3 (Fig. II.20C) and INV4 (Fig. II.20D) are the most radiation hard, and INV1 (Fig. II.20A) is the least radiation hard.



(A) INV1 (B) INV2

(C) INV3 (D) INV4

(E) INV5

FIGURE II.20: Simulated transfer characteristics of differently dimensioned inverters before and after irradiation according to the model depicted in Fig. II.18

More exact evaluation is possible with the help of the plot in Fig. II.21. Here the difference between the inverters transfer characteristics after 300 krad TID and before irradiation is plotted as a function of the input voltage. The most prominent characteristics shift can be observed in INV1, and the smallest shift is designated to INV3. Looking back at the Table II.4 it can be noticed that this conclusion is in agreement with radiation hard design MOS transistor dimensioning guidelines, presented in Chapter I.

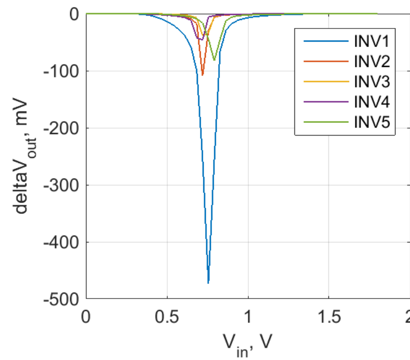
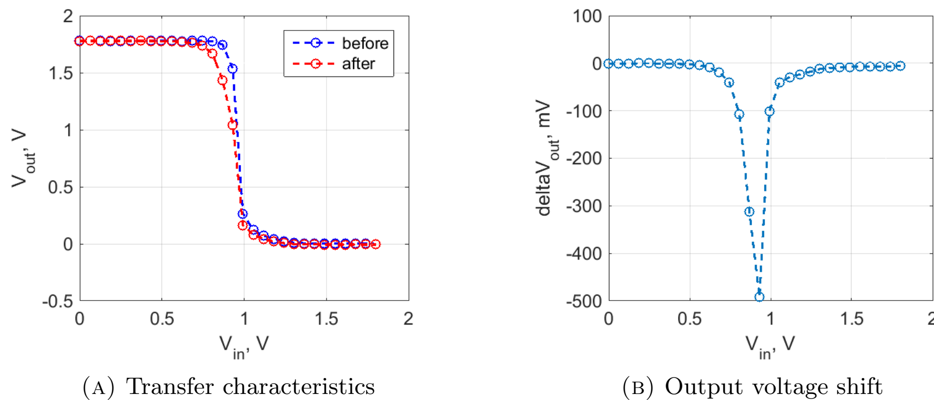


FIGURE II.21: Simulated inverter output voltage shift after irradiation for different dimensions of inverters.



(A) Transfer characteristics (B) Output voltage shift

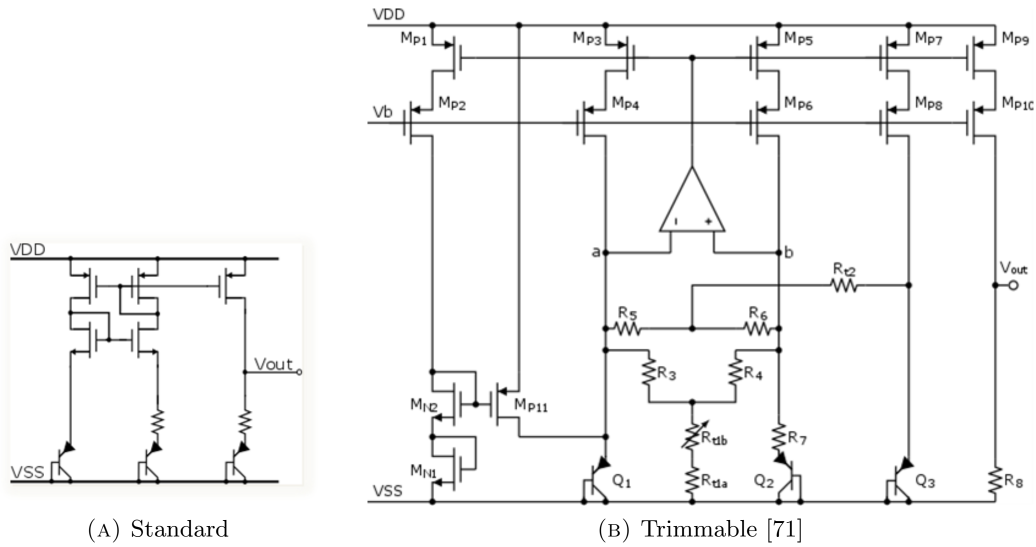
FIGURE II.22: Measured transfer characteristics (A) before and after 300 krad TID and output voltage shift after 300 krad TID of a standard inverter with PMOS W/L=400/180 and NMOS W/L=350/180. Average of 8 samples.

Fig. II.22 depicts the measurement results on a standard inverter with PMOS W/L=400/180 and NMOS W/L=350/180. The transfer characteristics on Fig. II.22A were obtained before and after 300 krad TID, and the output voltage shift shown in Fig. II.22B depicts the difference between these two transfer characteristics. The maximal shift in this case reaches 500 mV, which is very close to the simulated value of 485 mV for the same inverter dimensions.

This allows two conclusions. First, conducted simulations have proven that appropriate transistor dimensioning can indeed achieve high level of radiation hardness. Second, macro-model of single device radiation effects gives excellent qualitative and good quantitative estimation of expected radiation effects on the circuit level.

2.2 Bandgap voltage reference case study

Bandgap voltage reference is required throughout most analogue and mixed-signal circuits, as it provides a temperature stable reference is required by other circuit blocks. Stability of the output voltage of the bandgap reference is thus vital; not only temperature independence, but also TID independence has to be provided. In this study I analyse two different bandgap voltage references, as shown in Fig. II.23: a standard bandgap voltage reference (A), as can be found in the design kit, and a radiation hardened trimmable one (B), designed by Mario Auer [71]. These circuits are analysed from two perspectives. On the one hand, propagation of device level radiation effects to the circuit level is analysed. On the other hand, radiation hardness of the studied designs is investigated.



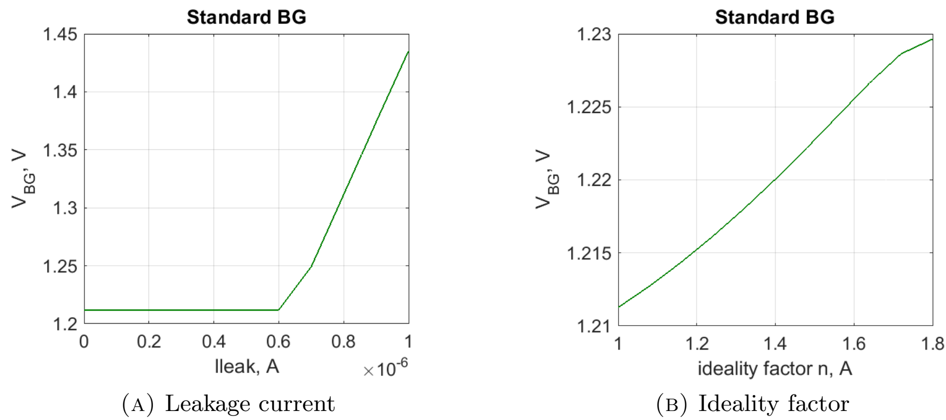
(A) Standard (B) Trimmable [71]

Figure II.23: Simplified schematics of standard (A) and radiation hardened trimmable (B) bandgap voltage references

The most TID susceptible devices in a bandgap reference are the diodes and the NMOS transistors. In the standard bandgap voltage reference long and narrow NMOS transistors are used in the current source circuit block, to avoid channel length modulation and improve matching. As already stated in Chapter 2, such devices suffer enhanced TID effects. In case of radiation hardened trimmable bandgap reference, NMOS TID effects have been mitigated on device and circuit levels [71]. The amount of NMOS transistors was reduced to the necessary minimum, transistors were dimensioned to avoid RINCE and RISCE effects, and ELT NMOS were implemented in critical circuit nodes. Additionally, circuit topology measures have been taken. In addition to programmable

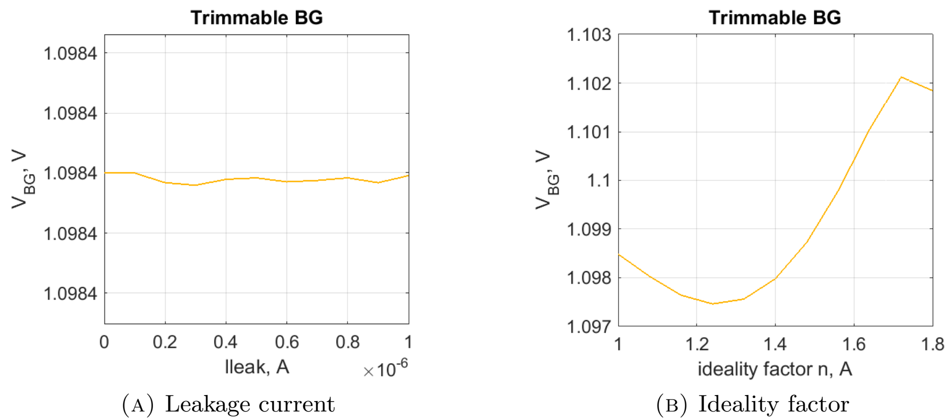
trimming resistors, fixed value resistors were introduced. The fixed resistors allow negative source voltage for NMOS transistors, mitigating TID induced leakage current. Altogether these measures allowed to minimize leakage current and its contribution to circuit degradation. Diodes in both circuits were implemented as a diode connection of standard PNP bipolar junction transistor, thus leaving them susceptible to TID effects.

Simulation of the TID effects on bandgap voltage references was performed within Cadence environment in Spectre simulator. The macro-models used incorporated current source representing leakage current of NMOS transistors, and Verilog A model of diodes with variable ideality factor n. Values of the TID dependent parameters for simulation were varied according to experimental results on device level, as reported in Chapter 2.



(A) Leakage current (B) Ideality factor

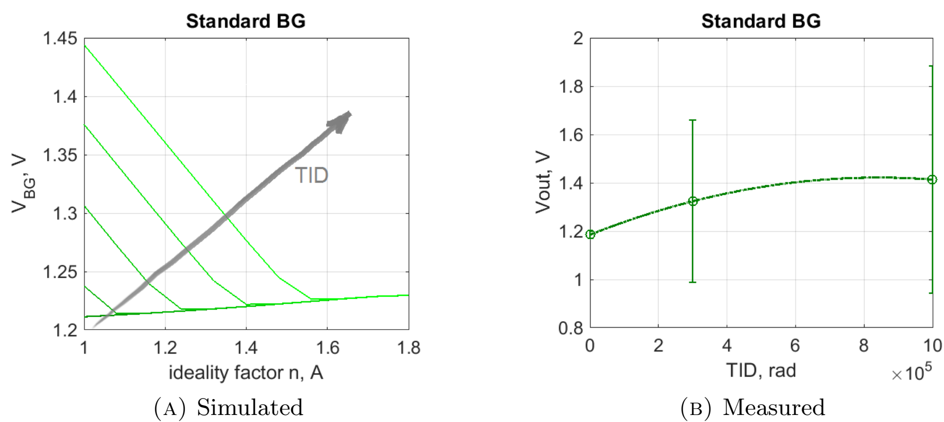
FIGURE II.24: Simulated output voltage of the standard bandgap voltage reference as a function of TID dependent parameter: leakage current of NMOS transistors (A and ideality factor of diodes (B).



(A) Leakage current (B) Ideality factor

FIGURE II.25: Simulated output voltage of the trimmable bandgap voltage reference as a function of TID dependent parameters: leakage current of NMOS transistors (A) and ideality factor of diodes (B).

Fig. II.24 and Fig. II.25 show the results of the simulations with single parameter variation for the two investigated bandgap voltage reference topologies. From Fig. II.24 can be concluded that the leakage current is a major contributor to overall circuit performance. However, TID induced increase of ideality factor causes constant increase of circuit output voltage, whereas leakage current becomes significant only after it reaches a certain value (in this particular case 600 nA). From Fig. II.25 it becomes obvious that leakage current has been mitigated and has negligible influence on the overall circuit performance. In this case TID induced ideality factor increase is the main contributor to the output voltage change.

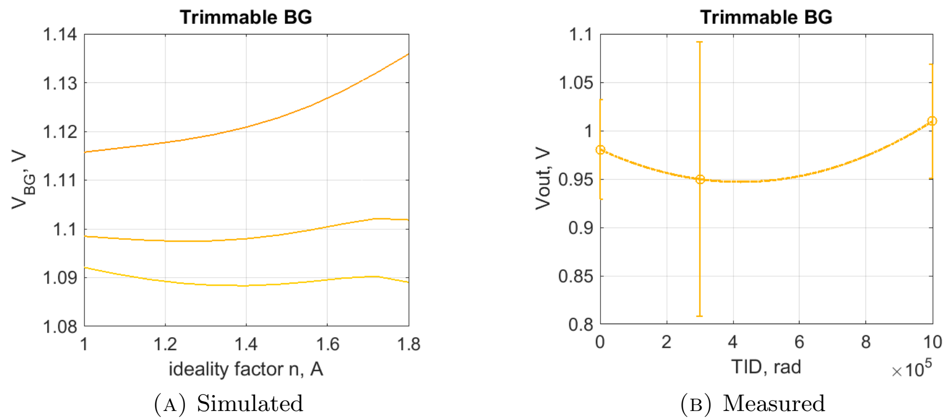


(A) Simulated (B) Measured

Figure II.26: Output voltage of the standard bandgap voltage reference simulated with TID induced ideality factor and leakage current shifts (A) and measured average of 7 samples, with 3σ bars (B).

Fig. II.26 illustrates output voltage of the standard bandgap voltage reference, simulated with both TID dependent parameters variation (A) and measured (B) in the course of experiments described in Appendix A on a custom designed test chip CREAM. The simulation fits qualitatively the measurement results.

Fig. II.27 shows output voltage of the radiation hardened trimmable bandgap voltage reference, simulated (A) with both TID dependent parameters varied at typical, worst speed and worst power process corners, and measured (B) on test chip CREAM (Appendix A). From these plots it can be seen that this design is more sensitive to process parameters variation, and so is the radiation hardness of the design. In this case the ideality factor of the diode is the main contributor to the overall circuit TID performance. TID effect on the ideality factor of the diode strongly depends on the quality of the neighbouring STI. Since SiO_2 of the STI is usually less controlled than the quality of the gate oxide, more variation can be expected in the radiation response of this device,



(A) Simulated (B) Measured

FIGURE II.27: Output voltage of the trimmable bandgap voltage reference simulated with TID induced ideality factor and leakage current shifts at process corners (A) and measured average of 7 samples (B).

leading to less stable overall circuit performance. Still, thanks to mitigation of NMOS leakage current contribution the trimmable bandgap voltage reference is more robust against TID effects than the standard one.

This case study, together with the previous one, shows the simulation methodology allows to evaluate radiation effects on the given circuit for the expected TID levels in the design stage, for both radiation sensitive and radiation hardened circuit designs.

Conclusion

Actual implementation of radiation hardened design brings many challenges with it. First of all, the trade-offs between radiation hardness, circuit area and its performance are necessary. Secondly, radiation hardened devices have to be incorporated into circuit simulation. Finally, circuit radiation hardness has to be anticipated in early design stages.

Macro-modelling is a powerful tool finding implementation throughout the whole radiation aware design process. On the one hand it enables simulation of radiation hardened devices, like ELTs. On the other hand it allows incorporation of TID effects into circuit simulation.

In this chapter I have given a comprehensive overview of the existing ELT equivalent aspect ratio models. For these state-of-the-art models I have developed adaptations for

the particular area optimized layout realization [60], [61]. I have also introduced my novel isosceles trapezoid approximation model, both geometry flexible and physically accurate with precision as good as 3% relative error [61], [62]. The isosceles trapezoid approximation has been proven to be useful where additional stress effects have to be taken into account, such as in case of STI stress effect [62].

The macro-modelling approach to circuit level radiation effects analysis has been applied. In two case-studies I have proven the following: First, radiation hard design guidelines on MOS transistor dimensioning allow to achieve high level of TID tolerance. Second, implementation of macro-models for single device TID effects provides good estimation of circuit level radiation effects. Third, macro-model simulation can be effectively used to deduce major contributors to the circuit level radiation effects.

These findings allow formulation of the unique and simple radiation hard design methodology, easily integrable into standard IC product development process. Without the need for special radiation hardness simulation tools, analog designers can evaluate criticality and radiation hardness of the given circuit on early design stages, thus avoiding timely and costly re-designs. The only requirement is knowledge of expected device level radiation effects. This knowledge can be gained through dedicated experiments, but also from the literature, and with the help of multi-physics simulation tools.

Chapter III

Testing Beyond Standards

"...It is still magic even if you know how it's done..."

—Terry Pratchett, "A Hat Full of Sky"

Introduction

Radiation hardening of integrated circuits involves extensive preparatory work. In order to develop radiation hard design guidelines, extensive testing is needed. Usually, standards prescribe use of "best engineering judgement" [72] for test matrix definition. It is even more so for when it comes to radiation tolerance characterization of a fabrication process or a family of processes to develop design guidelines, instead of a single device. Here, due to variety of testing conditions to consider, no standard procedure can be defined. That is why in my work I address testing beyond standards. In this chapter subjects of device parameters measurement and extraction and of radiation testing are covered, X-ray testing in particular.

In order to extract relevant device parameters, many steps are required. The test structures have to be defined and developed, appropriate set of measurements defined and optimized for time accuracy and simplicity, before the parameters can actually be extracted. In the first section of this chapter I discuss the methods suitable for these tasks to achieve the most useful results for consequent radiation hard design guidelines formulation. Particular focus lies here also on the parameters extraction techniques.

Extraction of the semiconductor device parameters is a heterogeneous field. Different vendors use different techniques to characterize their devices. Threshold voltage alone can be extracted in a number of ways [73], all offering their advantages and having their drawbacks. Extraction of the parameters after irradiation can become even more challenging. Having faced such challenge I propose a methodology for electrical characterization of the integrated devices.

A further aspect of the device characterization is conducting the irradiation tests. Radiation hardness assurance is a standardized process for the space research. There, the test methodology, radiation source, irradiation conditions and dosimetry are well defined [74], [75], [72]. Typically, electronics for high energy physics also follows procedures defined in these standards. MIL-STD-883 Method 1019.4 [74] together with ESCC 22900 [75] define ^{60}Co gamma-ray source for TID tests. ^{60}Co has mean energy of approximately 1 MeV. Advantage of this radiation source is almost constant absorption in silicon across the gamma-ray energy spectrum. However, this absorption is relatively low compared to X-rays, leading to longer test time at the same intensity. X-ray testing offers accelerated dose accumulation. The disadvantage of X-rays is a very non-homogeneous absorption of low and medium energy X-rays along the spectrum, and variable penetration depth of different X-rays. These factors make the dosimetry particularly challenging.

Standard guide ASTM F1892-12 [72] defines sources recommended for use in radiation hardness testing for custom applications. Within this standard guide the use of ^{60}Co, ^{137}Cs and low energy X-ray source (10 keV) is covered. Low energy X-ray testing is explicitly recommended for transistor characterization. Such X-ray testing has been used for pre-compliance and research purposes by many groups [76], [77], [78]. For low energy X-ray testing the L-line radiation of tungsten target X-ray source (W-tube) is used [79], with 11 keV energy peak, resulting in 10 keV mean photon energy. This methodology of testing is regulated by standard guideline ASTM F1467-18 [80]. However, other X-ray sources, such as copper target X-ray tube (Cu-tube), can result in similar spectrum while offering higher dose rate. Also K-line radiation of W-tube can be used for testing, with 67.244 keV energy peak and mean energy of 60 keV, resulting in higher flexibility of dose rate and radiation intensity for transient effects testing. In this case, careful dose administration and accurate dosimetry are of vital importance. The dosimetry challenges often overweight the advantages of flexibility of such test methods, thus leaving them

unregulated by standardization bodies. Still, the flexibility of a full W-tube spectrum and Cu-tube testing is of great value for research purposes. That is why subject of overcoming above named challenges of careful dose administration and dosimetry at non-standard X-ray sources and results alignment between them are addressed later in this chapter.

1 Parameters Measurement and Extraction

First of all, the relevant parameters have to be defined. Their definition depends greatly on the target application and on target radiation environment, and thus the expected effects. For example, in the frame of my work I have focused on threshold voltage and leakage current of MOS transistors, together with flicker noise. These parameters were chosen as major, suffering TID effects in X-ray radiation environment, relevant for post-irradiation IC performance. Of course, other parameters, such as transistor gain, saturation current or sub-threshold slope would have also been relevant. Here, the mentioned above "best engineering judgement" had to be applied to limit number of tested parameters. As one of the practical aspects of my investigations was integrability of the developed methods into a standard industrial development process, they had to be economically reasonable and time efficient.

1.1 Test-structures development

Test structures development is in the first place driven by the set of pre-defined parameters of interest. Test structures have to be developed in such a way, to cover maximal amount of parameter variation with minimal amount of test structures, to be able to conduct all the necessary tests in minimal time. In the afore mentioned example of MOS transistors as test structures important variations include, but are not limited to: channel length, channel width, gate extension area, type of transistor, gate thickness, doping level, layout, etc. Varying these physical parameters with same accuracy would result in few hundreds of devices. Taking into account other parameters that have to be varied in radiation hardness testing (bias, temperature, dose rate...) full test of such device set

would require millions of measurements. Thus a smart approach to test structures development and test minimization is required. In my work test structures development is done in three steps: preliminary tests, and first and second custom-designed test chips.

First, preliminary tests on standard structures, provided by manufacturer (see Appendix A Table A.3) were performed. The procedure for testing of these structures was developed by my colleague Alicja Michalowska-Forsyth. The tests were conducted in collaboration. Consequently I have analysed the results of these tests. Based on these results, I have identified the most important physical parameters and the minimal amount of structures in these variations.

TABLE III.1: Test structures implemented on the first custom-designed test chip with corresponding parameter variations.

<table>
<tr><th>Structure type</th><th>Varied parameters</th></tr>
<tr><td rowspan="7">MOS transistor</td><td>Type</td></tr>
<tr><td>t_{GOX}</td></tr>
<tr><td>Doping</td></tr>
<tr><td>Layout</td></tr>
<tr><td>Size</td></tr>
<tr><td>Gate extension area</td></tr>
<tr><td>Metal shield</td></tr>
<tr><td rowspan="2">Capacitor</td><td>Type</td></tr>
<tr><td>Size</td></tr>
<tr><td rowspan="2">Diode</td><td>Type</td></tr>
<tr><td>Area</td></tr>
<tr><td rowspan="2">Resistor</td><td>Type</td></tr>
<tr><td>Resistance</td></tr>
<tr><td>BJT</td><td>Aspect ratio</td></tr>
<tr><td>Digital blocks</td><td>Topology</td></tr>
</table>

The second step was the development and test of the custom-designed test chip MiAMoRE (Mitigation, Analysis and Modelling of Radiation Effects) incorporating test structures with corresponding parameter variations, described in more detail in Appendix A. The structures on MiAMoRE test chip included mainly single devices, but also few simple digital blocks. The exhaustive list of the test structures is given in Appendix A Table A.1. Table III.1 summarizes types of the test structures and their corresponding parameters variations addressed within my study on the MiAMoRE test chip. Table III.2 illustrates in more detail the parameters variation of MOS transistors implemented on the MiAMoRE test chip. Cells marked in green mean the parameters combination is implemented on the test chip, cells marked in red mean it is not. The grey cells mark overlapping of the same parameters in the matrix and are to be disregarded.

Table III.2: MOS transistor parameters variation matrix

MOS transistor parameters variation matrix		Type		tGOX		Doping		Layout		Size		other	
		NMOS	PMOS	<4nm	>10nm	standard	high	linear	enclosed	varL	varW	gate extension	metal shield
Type	NMOS												
	PMOS												
tGOX	<4nm												
	>10nm												
Doping	standard												
	high												
Layout	linear												
	enclosed												
Size	var L												
	varW												
other	gate extension												
	metal shield												

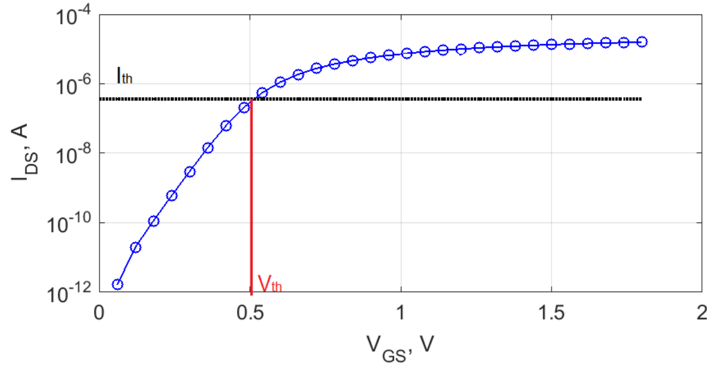
In the third step, more complex structures, incorporating single devices and digital blocks from the second step, were implemented on the second custom-designed test chip CREAM (Circuit Radiation Effects Analysis and Mitigation), along with few simple structures and single devices. In this step the scientific investigation of the propagation of single device radiation effects to the circuit level was in the focus. For this reason, circuits with and without mitigation measures were both incorporated onto the test-chip. In this step fewer unique structures were implemented for advantage of statistical strength of experiments. Here, all structures were placed at least twice on a single chip. This allows to ensure a better reproducibility of the test results and careful monitoring of intra-die and inter-die variation of the effects. The detailed list of the test structures, implemented on the CREAM test chip is given in Appendix A Table A.2.

1.2 Parameters extraction techniques

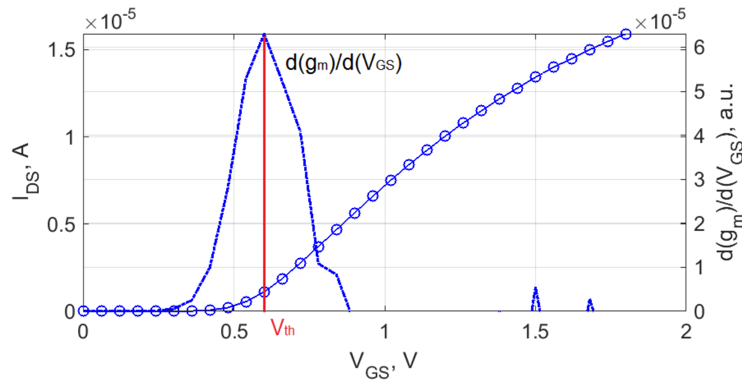
Parameters of the test structures can be extracted in a number of ways. First of all, some of the parameters can be taken from the direct measurement. An example for this could be the direct single point measurement of the leakage current of a MOS transistor. Other parameters have to be extracted from the measured characteristics by different methods. In the frame of my investigations a particular challenge was to extract the threshold voltage of MOS transistors before and after irradiation. That is why I dedicate this sub-section to the threshold voltage extraction methodology. Moreover, considerations involved in the V_{th} extraction hold also for other parameters and other test structures.

The main challenge in pre- and post-irradiation threshold voltage extraction is unification of the extraction methodology for results comparison. Reproducibility of the results is an important requirement in any kind of testing. As different vendors implement different methods to extract threshold voltage, it is sometimes difficult to compare achieved results with process corners and with other works. Thus, a transparent methodology for results unification is needed. This requires two scientific conclusions: which extraction method is most suitable for pre- and post-irradiation parameters extraction and how does it compare with other methods, used by scientific and industry community.

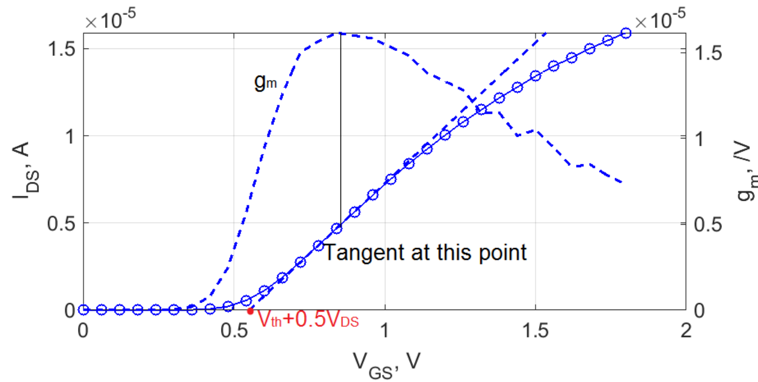
In the course of my research, I have analysed the suitability of the three most popular threshold voltage extraction methods [73] for pre- and post-irradiation parameters extraction. Fig. III.1 illustrates these methods, applied to the measured pre-irradiated transfer characteristics of an NMOS transistor with t_{GOX} <4 nm and W/L=0.22/0.18. The three methods, described in [73], yield different threshold voltage values for the same device. The difference comes from threshold voltage definition. It has been vastly discussed in literature [73] and exceeds the scope of this work. In the radiation hardness assurance process, the absolute value of the parameters is of less concern, than relative parameter shift. Thus reliability of extraction methodology both before and after irradiation has to be provided. In the following paragraphs, the above mentioned methods are applied to measured transfer characteristics of NMOS transistors with different gate oxide thickness before and after irradiation, demonstrating different extent of TID effects. The comparability of the threshold voltage before and after irradiation, allowing parameter shift evaluation, is elaborated in this analysis.



(A) Constant current (possible both in linear and saturation region)



(B) Transconductance derivative (linear region characteristics)

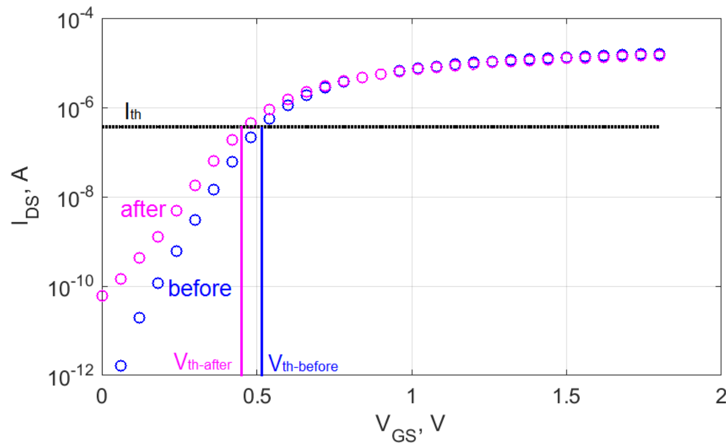


(C) Linear extrapolation (linear region characteristics)

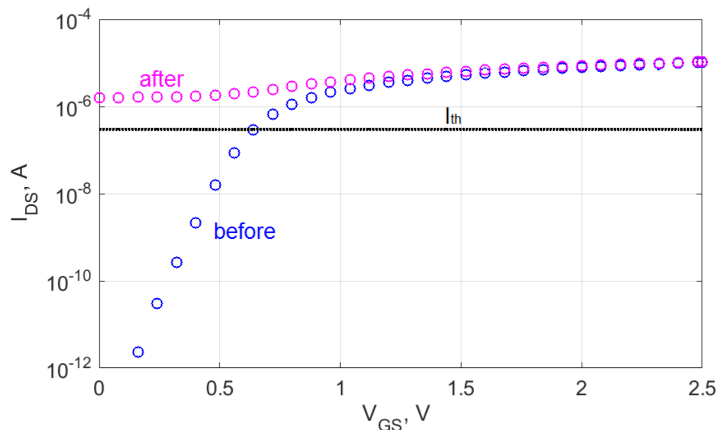
FIGURE III.1: Threshold voltage extraction methods on example of measured NMOS (t_{GOX} <4 nm and W/L=0.22/0.18) transfer characteristics in linear region (V_{DS}=0.05 V) before irradiation.

The constant current method [73] (Fig. III.1-A) is vastly implemented by semiconductor manufacturers for its time efficiency. Here the threshold voltage is defined as the gate-source voltage at a pre-defined threshold drain current, which is measured directly. The major drawback of this method for post-irradiation characterization is

the value of the threshold current. The leakage current of NMOS transistors after irradiation can become few orders of magnitude higher than the pre-defined threshold current, which is illustrated by Fig. III.2. Here, as previously discussed in Chapter I, transistor with thicker gate oxide (Fig. III.2B) suffers more severe characteristics change after irradiation than the transistor with thinner gate oxide (Fig. III.2A). Implementation of the constant current method for threshold voltage extraction becomes thus impossible for the devices with severe leakage current increase. In other words, constant current method is not suited for reliable comparison of device parameters before and after irradiation.



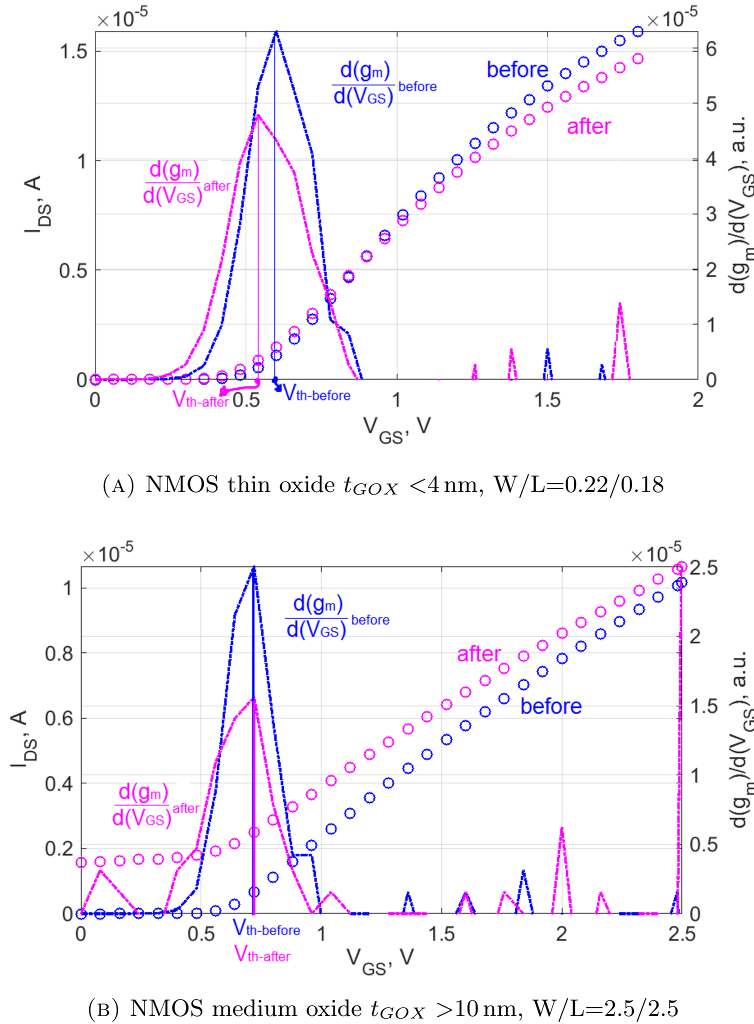
(A) NMOS thin oxide t_{GOX} <4 nm, W/L=0.22/0.18



(B) NMOS medium oxide t_{GOX} >10 nm, W/L=2.5/2.5

FIGURE III.2: Constant current method threshold voltage (V_{th}) extraction from measured transfer characteristics of thin t_{GOX} <4 nm (A) and medium t_{GOX} >10 nm (B) oxide NMOS transistors before (blue) and after (magenta) TID of 1 Mrad V_{DS}=50 mV.

The transconductance derivative method [73] is the second one considered. In this method threshold voltage is defined as gate-source voltage at the maxima of transconductance derivative, as illustrated by Fig. III.1-B. The advantage of this method is its independence of series resistance of the device. However, reliable threshold voltage extraction with this method requires many more measurement points in the transfer characteristics of the investigated transistor. Also reliable extraction after irradiation can become challenging for this reason, as illustrated by Fig. III.3.

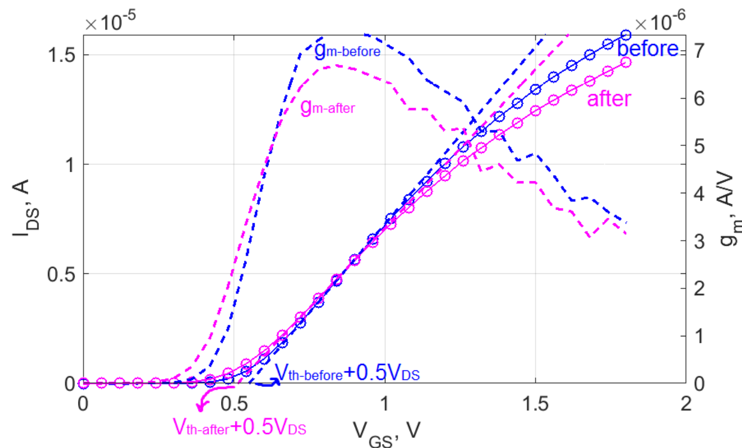


(A) NMOS thin oxide t_{GOX} <4 nm, W/L=0.22/0.18

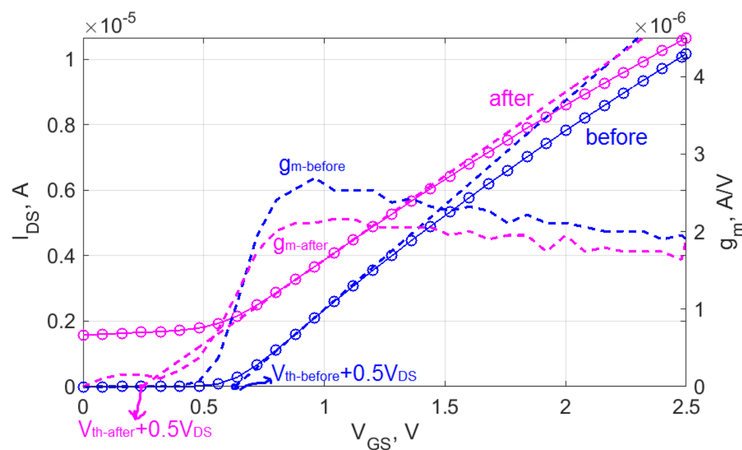
(B) NMOS medium oxide t_{GOX} >10 nm, W/L=2.5/2.5

FIGURE III.3: Transconductance derivative method threshold voltage (V_{th}) extraction from measured transfer characteristics of thin t_{GOX} <4 nm (A) and medium t_{GOX} >10 nm (B) oxide NMOS transistors before (blue) and after (magenta) TID of 1 Mrad V_{DS}=50 mV.

The linear extrapolation method implementation is illustrated by Fig. III.1-C. In this method the threshold voltage is extracted from the transfer characteristics of a MOS transistor in linear region (e.g. at V_{DS}=50 mV). First, the derivative of the transfer characteristics in the linear region is taken. Then a tangent to the transfer characteristics is drawn at the point of maximal g_m. This tangent is extrapolated to cross the x-axes. The crossing of the x-axes of the linear extrapolation of the tangent to the transfer characteristics at the point of maximal g_m results in $V_{th} + \frac{1}{2}V_{DS}$, and allows to extract V_{th}. The main disadvantage of this method is its sensitivity to series resistance. However, if the series resistance is negligible, it provides reliable results [73]. The advantage of this method is its applicability both before and after irradiation, as illustrated by Fig. III.4.



(A) NMOS thin oxide t_{GOX} <4 nm, W/L=0.22/0.18



(B) NMOS medium oxide t_{GOX} >10 nm, W/L=2.5/2.5

FIGURE III.4: Linear extrapolation method threshold voltage (V_{th}) extraction from measured transfer characteristics of thin t_{GOX} <4 nm (A) and medium t_{GOX} >10 nm (B) oxide NMOS transistors before (blue) and after (magenta) TID of 1 Mrad V_{DS}=50 mV.

It is also possible to differentiate between gate trapped charge induced threshold voltage shift and STI trapped charge induced one with this method, with a slight adaptation. In order to do so, one additional step is necessary in the extraction. To define gate trapped charge induced component, $V_{th} + \frac{1}{2}V_{DS}$ is defined as a cross-section of linear extrapolation of the tangent with a new virtual abscissa [48]. This new virtual abscissa is defined by the initial leakage current of the transistor before irradiation, as illustrated by Fig. III.5. Difference between the value extracted by conventional linear extrapolation and by the adjusted one gives STI trapped charge contribution to the threshold voltage shift.

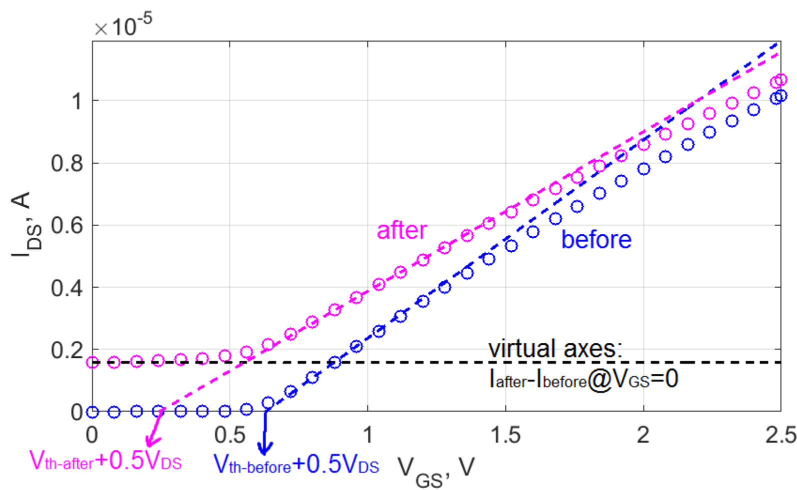


FIGURE III.5: Linear extrapolation method adaptation STI and gate trapped charge induced threshold voltage shift separation. Extracted from measured transfer characteristics of NMOS transistor with t_{GOX} >10 nm and W/L=2.5/2.5 before (blue) and after TID of 1 Mrad (magenta), V_{DS}=50 mV.

Validity of this method is demonstrated by Table III.3. Here absolute threshold voltage shifts in mV after 1 Mrad TID for NMOS transistor with t_{GOX} >10 nm and W/L=12.5/0.9 in standard and annular gate layouts are given. For the standard layout transistor, threshold voltage shift extracted conventionally (ΔV_{th}) and with the help of virtual X-axes ($\Delta V_{th-virtual}$) are given. The latter is very similar to threshold voltage shift of the annular transistor of the same dimension. Taking into account device parameters deviations due to additional stress effects, such as STI stress, the similarity validates usability of the presented method. However, to prove its universality, study of more different size transistors would be needed.

Table III.4 summarizes results of the threshold voltage extraction with different methods for thin and medium oxide NMOS transistors before and after irradiation. It can be

TABLE III.3: Threshold voltage shift of NMOS transistors with t_{GOX} >10 nm and W/L=12.5/0.9 after 1 Mrad TID extracted by means of conventional linear extrapolation ΔV_{th} and with the help of virtual X-axes $\Delta V_{th-virtual}$.

Layout	Standard		Annular gate
ΔV_{th}, mV	ΔV_{th}	$\Delta V_{th-virtual}$	ΔV_{th}
	55	91	57

TABLE III.4: Threshold voltage extraction methods: results comparison

		Constant current	Transconductance derivative	Linear extrapolation
Thin oxide	before	0.48 V	0.48 V	0.52 V
	after	0.42 V	0.42 V	0.48 V
Medium oxide	before	0.64 V	0.56 V	0.60 V
	after	NaN	0.56 V	0.21 V

concluded from these results, that only linear extrapolation can be applied to both transistor types reliably before and after irradiation.

Altogether, the linear extrapolation threshold voltage extraction method in both conventional [73] and adapted [48] forms was proven to be the most reliable and useful out of the considered three for TID characterization of MOS transistors.

1.3 Electrical characterization design

Electrical characterization of the test structures before, during and after irradiation has to be accurate and time efficient. Standard guide ASTM F1892-12 [72] prescribes time between irradiation and test and the time between two irradiation steps to be minimized and recorded. Standard MIL-STD-883 Test Method 1019 [74] allows the time between irradiations to be up to 20% of the incremental irradiation time or 2 hours, whichever is greater. With these restrictions, electrical characterization has to be optimized with regard to time, in addition to the accuracy of the measurement. Moreover, preliminary irradiation experiments reported in [48] show rapid annealing of some structures within the allowed 2 hours time between irradiation steps, setting even stricter requirements for the electrical characterization.

Trade-off between test time, accuracy and complexity is thus the central piece of effective electrical characterization methodology in radiation testing [81]. This trade-off can be achieved on the one hand with the smart design of test structures and optimization of their number, as covered by Subsection 1.1, and on the other hand, by test automation

and measurement plan optimization together with data reduction. In the latter it is important to ensure meaningful data set for post-processing of the results.

Realization of automated measurement brings with it measurement error, as it requires additional hardware and routing. Let us consider an example. Major part of test structures on the first custom designed test chip are MOS transistors. One of the critical parameters for these devices is their leakage current, which is typically very low (<1 nA) before irradiation. To realize automated measurement of over 100 devices, a digitally controlled switch matrix has to be implemented. One of the ways to realize it is by using multiplexers to switch between drains of single devices. But in order to be still able to measure low leakage currents, the multiplexers have to have low leakage too. Very low leakage multiplexers, such as MAX328CPE possess strongly current dependent on-resistance R_{ON}, as illustrated by Fig. III.6. This means at each value of drain current the drain-source voltage seen by the device will deviate from the applied voltage by $R_{ON} \cdot I_{DS}$, as illustrated by output characteristics of a PMOS transistor in Fig. III.7. So, during measurement of transfer characteristics of the transistors, the voltage drop between drain and source will depend on transistor current and applied voltage, changing the R_{ON}, making parameter extraction from this characteristics unreliable, as each point of $I_{DS} = f(V_{GS})$ is taken at different value of V_{DS}.

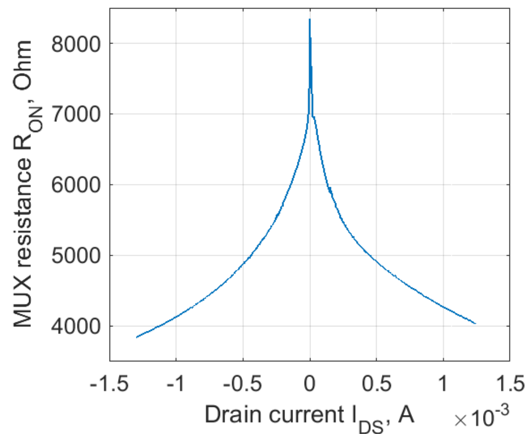


FIGURE III.6: R_{ON} of MAX328CPE multiplexer as a function of drain current.

Also long connection paths with different length for different devices that have to be compared can lead to similar problematic. That is why a compromise between low leakage and low R_{ON} has to be found. For this reason, for MiAMoRE and CREAM tests AD708/709 multiplexers were used, with R_{ON} <10 Ω and typical leakage current

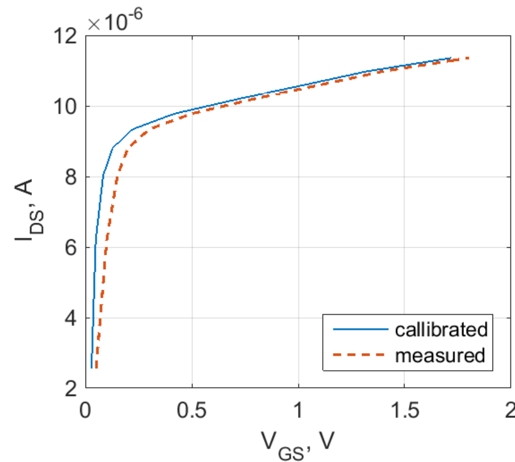


FIGURE III.7: Output characteristics of PMOS transistor with t_{GOX} <4 nm (see Appendix A) measured with MAX328CPE multiplexer (in red) and calibrated with recalculation of V_{DS} value by taking corresponding R_{ON} value.

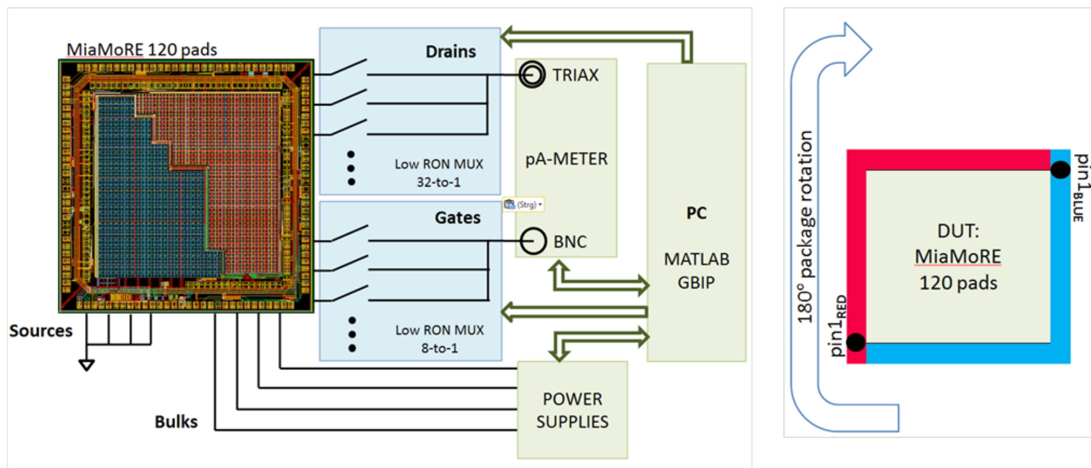
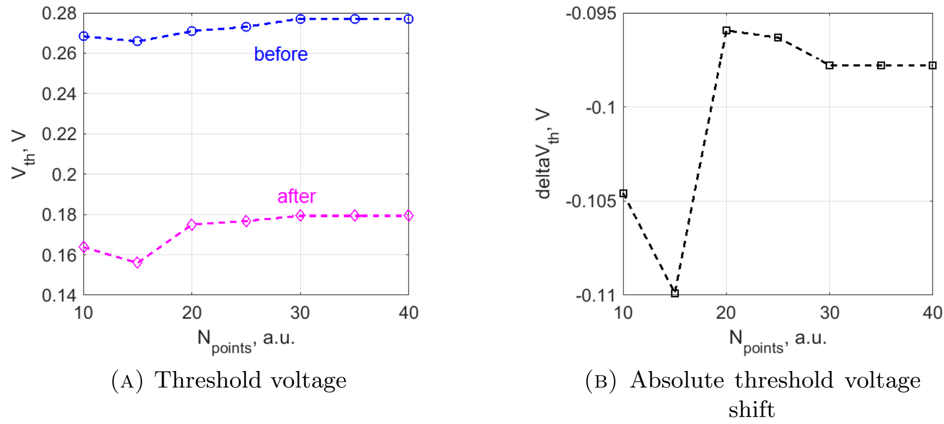


FIGURE III.8: Block diagram of semi-automated electrical characterization system for MiAMoRE test chip (picture credit: Alicja Michalowska-Forsyth).

<1 nA. Also a compromise between hardware complexity and degree of automation is necessary. Out of these considerations I propose implementation of semi-automated measurement system. Although not suitable for large scale industrial testing, it allows accurate and reliable pre-compliance data collection. Fig. III.8 illustrates such semi-automation principle for MiAMoRE test chip [81].

I have designed MiAMoRE test chip with diagonal symmetry in layout. In this case, only half of the chip is tested in one go, and then re-plugging is required. This way number and length of connections and multiplexers is minimized still allowing fast automated measurement. After the first half of the chip is characterized, it has to be turned around by 180°.



(A) Threshold voltage

(B) Absolute threshold voltage shift

FIGURE III.9: Threshold voltage before and after (A) and absolute threshold voltage shift after 1 Mrad TID of NMOS transistor with t_{GOX} <4 nm and W/L=5/5 (see Appendix A), extracted from transfer characteristics with number of measurement points N_{points} by means of linear extrapolation at V_{DS}=50 mV.

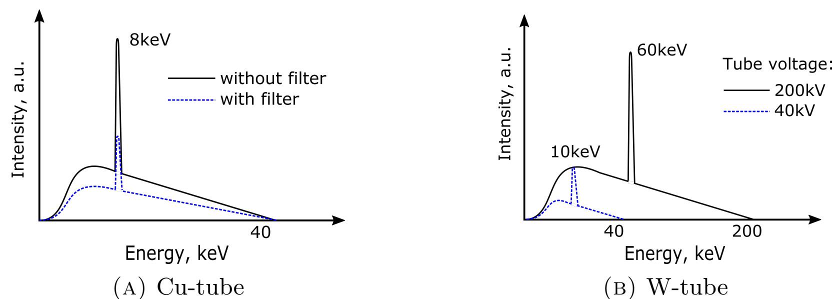
Further important step in electrical characterization optimization is minimization of necessary measurements and number of measurement points. Fig. III.9 shows results of my scientific investigation on this matter. Here, threshold voltage has been extracted by the means of conventional linear extrapolation [73] before and after TID of 1 Mrad. The transfer characteristics of the one transistor with different number of measurement points were used for this extraction. As a result, threshold voltage before and after irradiation as a function of number of measurement points N_{points} (Fig. III.9-A) and absolute threshold voltage shift after 1 Mrad TID (Fig. III.9-B) were obtained. From these plots it can be seen that the minimal number of points necessary for reliable MOS transistor parameters extraction yields to 30.

Altogether, my scientific investigations resulted in the methodical approach to parameters measurement and extraction, presented on example of MiAMoRE test chip characterization. It allowed to reduce test time of a single sample to less than 30 minutes for over 100 test structures. This methodical approach has been consequently applied to CREAM test chip characterization and can be further used for any pre-compliance radiation hardness characterization.

2 X-ray Testing and Dosimetry

Challenges of X-ray testing have been addressed multiple times by various groups. The latest contribution of CERN [79] gives a good overview of the available TID testing methods and facilities. The standard guide ASTM F1892-12 [72] defines ^{60}Co, ^{137}Cs and low energy X-ray source (10 keV) suitable for TID testing. But also other radiation sources, such as pulsed X-ray generators or electron beams are sometimes used for testing [79]. Usage of an X-ray diffractometer is also possible in this context, provided the right energy can be set up, but is not regulated by any standard procedure.

CT scanners and industrial X-ray machines usually incorporate W-tube as radiation source; as irradiation source should best emulate the target radiation environment, X-ray source was the preferred environment for my investigations. The standard procedure of TID testing with X-ray source is defined by ASTM F1467-18 [80]. In this standard guide, use of 10 keV tester in TID effects testing on semiconductor devices is addressed. As discussed in detail in [79], the L-line characteristic radiation of W-tube is typically used in such tests. This is achieved by limiting the X-ray spectrum with tube voltage on the one hand, and filtering low energy components on the other, to make the radiation harder. Alternatively, K-line Cu-tube radiation (approximatelly 8 keV) can be used, offering higher intensity at the same tube voltage. Similar to W-tube, the spectrum can be hardened with filters. Finally, the use of the full W-tube spectrum can be made, using characteristic K-line radiation. In this case low energy components, including L-line radiation, can be filtered out to harden the spectrum. Fig. III.10 illustrates these three discussed spectra.



(A) Cu-tube (B) W-tube

Figure III.10: Scetch of Cu- (A) and W-tube (B) photon energy spectra with different experimental settings (marked in black solid and blue dashed lines)

In the course of my scientific investigations I have performed experiments on both Cu-tube and W-tube making use of all three presented spectra possibilities, at three different irradiation facilities, as described in Appendix A. One challenge using these sources for TID testing lies in accurate dose administration and reliable dosimetry. A further challenge is comparison of the experimental results from different facilities offering different dosimetry tools and methods. The procedure for facility choice, dosimetry for wide-spectrum X-ray testing and methodology of experimental results comparison is discussed further in this section. Parts of this work have been presented in the frame of an invited talk at RADHARD Symposium in Seibersdorf, Austria in 2018 [82].

2.1 Irradiation source and irradiation facility choice

Choice of irradiation facility is dictated by a number of factors. First of all, the irradiation source has to correspond to the expected application environment. This means the energy spectrum, dose rates and TID should be chosen taking into account the expected environmental conditions. Also logistical factors, such as geographical location, time availability and infrastructure play significant role. Possibility to conduct 24/7 experiments may as well influence the decision. And last but not least, the cost efficiency is relevant. Table III.5 summarizes the factors relevant for the facility choice in my investigations, and how the three considered facilities fulfil these factors. The costs are normalized to the lowest given quote.

TABLE III.5: Irradiation facility choice

Facility	I-A	II-B	II-C
Tube target	Cu	W	
Maximal photon energy, keV	40	160	200
Tube voltage, kV	10 to 40	160	15 to 200
Tube current, mA	10 to 40	10	0.05 to 21
24/7 experiment possible	✓	×	✓
Booking prior, weeks	0	6-8	2-4
Location	In-house	180 km	150 km
Costs, a.u.	10 per sample	10 per hour	1 per hour
Dosimetry tools	Timepix [83]	Ionization chamber	
Measured quantity	Intensity	air Kerma	dose to water
Source calibration for TID(Si)	×	✓	×

All three facilities offer better service in one or the other aspect. Facility I-A offers excellent logistics in terms of location and access times. Facility II-B provide outstanding

dosimetry of a certified lab. The X-ray machine at Facility II-C provides the most flexibility in terms of energy range and dose rate. That is why it has been decided to use all three facilities in the course of my investigations.

2.2 Dosimetry

Accurate dose to Si measurement for medium energy range X-rays is not a straight forward task. First of all, X-ray beam generated by an X-ray tube is a heterogeneous mixture of different energies. Along these energies Silicon has different absorption coefficients. Thus, only knowing the exact X-ray spectrum it is possible to accurately define dose to Silicon with standard dosimetry tools, such as ionization chamber [79]. Standard guide ASTM E1894-08 [84] provides guidelines in selecting dosimetry tools for flash X-ray experiments. Such sources, unlike industrial X-ray machines, yield a relatively low TID due to their pulsed character. Thus, dosimetry techniques from this standard can not always be directly implemented for steady state X-ray testing. Also, different irradiation facilities can provide different dosimetry tools and reference values: water or air Kerma, intensity of photon beam of known energy, etc. In TID testing, however, it is important to know dose to Si or SiO_2. Thus, dose unification effort is needed.

Table III.6 summarizes dosimetry tools available at the used facilities and the unification effort connected with these dosimetry methods.

Table III.6: Dosimetry tools and methods

Facility	I-A	II-B	II-C
Instrument	Timepix [83]	Ionization chamber	
Quantity	No. of photons	air Kerma	dose to water
Units	$cnt/mm^2/s$	Gy/h	Gy/min
Unification after [85] with μ_{en}	for single energy (8 keV)	for measured spectrum	for theoretical spectrum

The methodology of dose unification is generally stated in ASTM E666-14 [85]. However, practical implementation of the general methodology reveals additional challenges. So, the standard procedure requires precise knowledge of the X-ray spectrum: not only the inherent, emitted by the source, but also scattered within the experimental set-up. Not every facility disposes of in-situ spectrum measurement. This motivates the need to use theoretical data, introducing additional uncertainties to the dose estimation.

For example, in facility II-C the available dosimetry tool measures dose to water. In this case, dose in Si can be calculated according to [85] using absorption coefficients for the theoretical X-ray spectrum. In the course of my experiments, three X-ray tube settings were used, resulting in different spectra (Fig. III.10-B). In case of the settings yielding the spectrum depicted in black solid line, with 60 keV peak, the calculation for mono-energetic photon beam was chosen. This was possible under the assumption that the mean energy peak is dominating other spectral components. In case of the settings yielding the spectrum depicted in dashed blue line, with 10 keV peak, all low energy spectral components had to be taken into account. Fig. III.11 illustrates water and silicon absorption coefficients [86] for this part of spectrum. As it can be seen, ratio between the coefficients changes rapidly and is non-homogeneous with energy. That is why it was important to consider all spectral components.

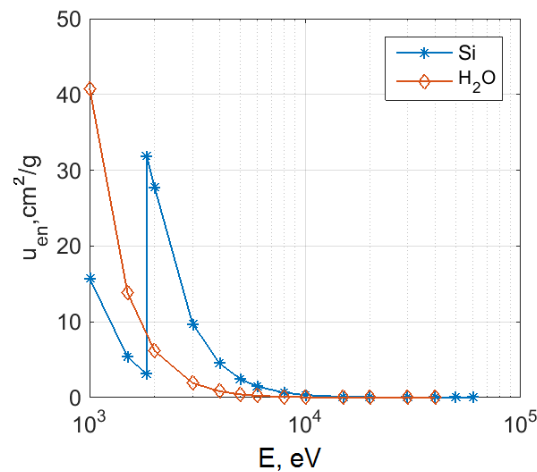


FIGURE III.11: Mass-energy absorption coefficients of silicon and water.

2.3 Irradiation facilities comparison

In order to ensure comparability of the results achieved in the course of my scientific investigations, additional effort in irradiation facilities comparison is required.

First of all, the reference test structures were needed. These test structures were characterized in every irradiation campaign, and TID effects consequently compared. Secondly, dose estimation had to be unified, independent of available dosimetry tools. So, the unification has been done according to ASTM E666 standard [85], as discussed above.

Thirdly, dose rate and TID steps had to be defined in a way that the results can be reproducible.

Table III.7 summarizes irradiation test plan to ensure reliable facility comparison.

TABLE III.7: Irradiation test plan for facilities comparison

Facility	I-A	II-B	II-C	
Test chip	MiAMoRE			CREAM
Dose rate, rad/s	0.01 1 100	1.5	1.5 10 300	300
TID_{MAX}	1 Mrad	25 krad	1 Mrad	1 Mrad
Mean energy, keV	8	60	10 60	60

The proposed methodology involves the following:

The reference test structures are MOS transistors on MiAMoRE test chips. These were irradiated at all facilities under all conditions. The reference facility is facility II-B. As facility II-C is the most flexible in terms of X-ray source settings, the energy spectra and dose rates of other two facilities were reproduced at this one.

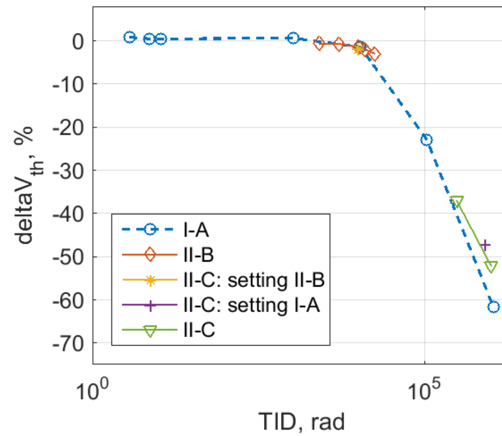


FIGURE III.12: Threshold voltage shift of NMOS transistor within MiAMoRE test chip with t_{GOX} >10 nm and W/L=1.95/0.9 as a function of TID after irradiation at different facilities and X-ray source settings.

Finally, after unification of the total dose according to [85] the threshold voltage shift of the chosen transistors as a function of dose was compared between all three facilities [87]. Fig. III.12 illustrates results of this scientific investigation [82]. As it can be seen, the results yield to good comparability, proving applicability of the proposed methodology.

Conclusion

Many guidelines to TID characterization of semiconductor devices exist. However, characterization of radiation effects is unique for each device and application, the same as radiation environments are. That is why most standards highlight the need of "best engineering judgement" [72] when it comes to trade-offs between accuracy, time, complexity and cost of this process. Often, no standard procedure can be applied for custom test structures and specific application field. That is why testing beyond standards is an important topic for the scientific and engineering community.

In the frame of my scientific investigations I have developed adjustable methodology for TID characterization of custom test structures with X-rays. Within this methodology I address the process of test structures development, analyse suitable parameters extraction techniques and important scientific and engineering considerations for the electrical test development. The subject of non-standardized irradiation tests with low and medium energy X-rays was investigated, together with methodology for unification of experimental results from different irradiation facilities and X-ray sources.

The test structures development has been addressed on the example of my test chip MiAMoRE. In particular, scientific approach to test structures number optimization while maintaining high parametric variability was introduced. Also, methodical three step development of radiation hardness assurance was implemented [81]: from standard test structures provided by vendor, through custom radiation hardened and not radiation hardened test structures on MiAMoRE test chip, to more complex circuit blocks incorporating the structures from the previous two steps.

As the MOS transistor has been one of the most prominent test structures, relevant for my investigations, it was crucial to ensure reliable parameters extraction. Methodical scientific analysis of threshold voltage extraction revealed linear extrapolation to be most suitable for TID effects study. My novel adaptation of this threshold voltage extraction method [48] allows to separate between gate and STI trapped charge contribution to the threshold voltage shift - valuable information for TID effects analysis.

On the subject of electrical characterization design, a methodical approach to test time and accuracy optimization was developed [81]. On the example of MiAMoRE test chip electrical characterization, the most important scientific and engineering considerations

were elaborated. Also, a simple-to-use method for the optimization of the number of necessary measurement points was introduced. These scientific investigations yielded a total test time below 30 minutes for a test chip with over 100 test structures.

Further, considerations for irradiation testing with low and medium energy X-rays were discussed. First of all, factors influencing radiation source and facility choice were elaborated. Then the dosimetry tools and methods were discussed. Scientific approach to dose unification between different sources and dosimetry tools was presented [87]. Finally, a method for reliable results comparison from different irradiation facilities and sources was introduced [82].

Altogether, my scientific investigations resulted in the methodical approach to radiation effects on semiconductor devices and circuits testing using low and medium energy X-rays. This novel methodology, contributing to state of the art testing according to standards, can be integrated into the IC development flow, to create radiation hardened IC products.

Conclusions and Outlook

CT is one of the most powerful diagnostic tools of modern medicine. X-rays used in this medical imaging technique are detected by photo-sensors and read out by ICs. In the new generation of CT hybridization of sensors and readout electronics is expected. In this case the readout ICs will be exposed to X-rays. Under influence of ionizing radiation, such as X-rays, semiconductor devices and circuit change their parameters. In the frame of my PhD thesis I have studied X-ray effects on ICs fabricated in a commercial CMOS process with STI, to enable reliable image readout for new generation CT. In this last chapter I summarize the scientific findings of my investigations, give an outlook of the future possibilities these findings empower, and discuss further related scientific questions that are yet to solve.

Scientific Findings and Contributions

The main scientific findings of my investigations can be subdivided into three groups, similar to this thesis. The first group covers the findings related to X-ray effects on devices and methods of their mitigation. The second group is related to the radiation hardening implementation and modelling in particular. The third group of findings deals with irradiation test methodology and radiation effects characterization. Many of these scientific findings have already been recognized by national and international scientific community in frame of journal publications [2], [61], [71], conference publications [48], [62], [54], workshop posters [60], [87], and invited talks [81], [82]. Further dissemination of yet unpublished findings is planned: one paper for Microelectronics Reliability Journal, another one for Transactions on Nuclear Science and a few conference papers for Radiation Effects on Components and Systems Conference (RADECS 2019).

In the frame of my PhD I have investigated X-ray effects on CMOS ICs with the help of custom-designed test structures within two test chips MiAMoRE and CREAM, fabricated in a commercial 180 nm CMOS technology. This investigation yielded a comprehensive summary of the X-ray effects (transients and TID) depending on a variety of factors. In this thesis transient effects of medium energy X-rays on integrated circuits were scientifically investigated for the first time. My experimental studies have shown it has a negligible effect with transient current density below 10 fA/μm up to dose rate of 300 rad/s. Also, a unique study of TID effects on different types of integrated diodes was conducted. Within this study I have proven the major contribution of STI interface traps to the ideality factor, saturation current and reverse current change after irradiation, by means of measurement and multi-physics simulation. My investigations included also TID effects on MOS transistors, and their dependence on various factors. So, for the first time, I have experimentally and by means of simulation proven substrate doping influence on TID effects in MOS transistors with same gate oxide thickness within same technology node. This finding allows an important conclusion for radiation hardening of ICs - the higher the substrate doping is, the more robust is the device against TID. I have extended discoveries on size dependence of TID effects for a 180 nm CMOS technology [48]. Meticulous literature study, manifold custom-designed test structures and comprehensive set of measurement data from my experiments allowed to consequently formulate a general guideline for device dimensioning to minimize TID effects. Yet another important finding is gate extension area influence on TID effects. The unique empirical study of this effect on a broad spectrum of custom test structures substantiates rare hypothesis from rare theoretical studies that can be found in literature. This finding has also allowed an important conclusion for radiation hardened IC design - the bigger the gate extension area, the worse are TID effects. The last finding regarding X-ray effects concerned low TID effects on flicker noise of the transistors [54]. My experiments have shown that medium oxide transistors are susceptible already to doses as low as 15 krad, whereas thin oxide devices remain unchanged by such low doses. These results are most relevant for low-noise designs where thicker gate oxide transistors are required in I/O stages. The conclusions drawn from these findings could be then summarized in a unique in its simplicity and completeness guideline to radiation aware IC design. The recommendations to device choice, dimensioning and layout can be easily included into standard IC development process in any commercial CMOS process with STI between 180 nm and 65 nm.

The actual implementation of radiation hardening in practice can require tremendous simulation effort. This includes simulation models of radiation hardened devices and parametric functional simulation of circuit radiation effects. Within my PhD research I have adopted the macro-modelling principle for both purposes. I have developed a novel isosceles trapezoid model for equivalent aspect ratio estimation of an annular gate transistor [61], [60]. This model is physically accurate and independent of actual transistor geometry. It also allows incorporation of additional stress effects into device and circuit simulation [62]. Further I have introduced a methodology of macro-modelling implementation for circuit level radiation effects analysis. It not only allows to estimate radiation hardness of the given circuit at early design stage, but also to track which device parameter shifts contribute the most to the overall circuit performance degradation after irradiation.

Finally, I have addressed the subject of X-ray effects characterization. Here my methodology for test structures development to reach sufficient parametric variation with least number of tested devices has been presented [81]. I have also scientifically investigated threshold voltage extraction methods and their suitability for TID characterization of MOS transistors. This investigation has proven linear extrapolation to be the most suited method of threshold voltage extraction. I have also introduced a novel adaptation of this method [48] to separate gate oxide traps contribution to threshold voltage shift from STI traps contribution, proving it with experimental data. I have developed methodology of electrical characterization time optimization, reducing test time to half an hour per sample with over 100 test structures within one packaged chip using a single-channel measurement equipment [81]. Last but not least, I have developed a methodology for X-ray testing, complementing standardized test methods, perfectly suitable for research and development purposes. Within this methodology I proposed a procedure of dose unification between different dosimetry tools [87]. Along with it, a unique procedure for results unification and comparison between different X-ray sources and facilities has been developed, yielding in excellent results comparability [82].

Outlook: industrial implementation and further research

Within my PhD research I have conducted application driven fundamental research. My scientific findings and developments can be directly implemented in standard industrial IC development process, to enable within the next 5-10 years new IC solutions with improved medical imaging resolution at lowered X-ray exposure for the patients.

Although the main focus of this study lies on CT application, its findings can be successfully used in other fields. So, for example, space electronics can be also designed relying on this work. The typical TID requirements for space missions do not exceed 1 Mrad, thus making the presented results comprehensive.

The achieved results can also serve as a stepping-stone to various further research activities. So, the usability of the proposed radiation hardening methodologies for advanced technology nodes below 45 nm (e.g. FinFET) can be investigated. For this purpose, the developed testing methodology can be adopted.

Also, gained knowledge on low dose TID effects and on X-ray induced transients facilitates expansion of the study to SEE. This leads to yet another research question: What happens to the IC under multi-stress conditions. This starts with SEE sensitivity change with increasing TID [88], [89]. But also other environmental influences, like temperature, electromagnetic interference (EMI) or electrostatic discharge (ESD), combined with TID may lead to an unexpected circuit behaviour. This subject has been raised to the attention of scientific community by few groups [90], [91], [92], [93]. Still, a lot of questions remain unanswered, leaving room for further research activities.

Finally, standardization activities on X-ray testing using different X-ray sources can be triggered. Such standardized procedure would enable simple cost and time efficient pre-compliance radiation tests decreasing time to market.

"...Now ... if you trust in yourself ... and believe in your dreams ... and follow your star ... you'll still get beaten by people who spent their time working hard and learning things and weren't so lazy. Goodbye..."

—Terry Pratchett, "The Wee Free Men"

Appendix A

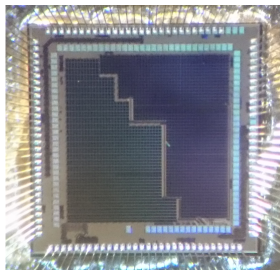
Experimental details

"...I don't think I've drunk enough beer to understand that..."

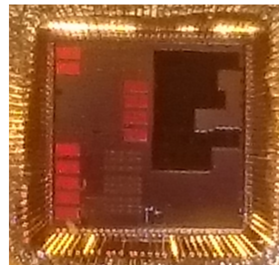
—Terry Pratchett, "The Last Continent"

1 Experimental structures

All the data presented in this thesis has been obtained in a row of experiments on my custom-designed test chips: MiAMoRE (Mitigation, Analysis and Modelling of Radiation Effects) and CREAM (Circuit Radiation Effects Analysis and Mitigation). The test chips have been fabricated in a commercial 180 nm CMOS technology incorporating shallow trench isolation. Photographs of the MiAMoRE and CREAM chips are shown in Fig. A.1. Table A.1 and Table A.2 summarize the different structures that I have implemented on each test chip. Both test chips were designed based on knowledge obtained from initial experiments on scribe line monitor (SLM) devices test chips, provided by foundry, summarized in Table A.3.



(A) MiAMoRE



(B) CREAM

Figure A.1: Photographs of MiAMoRE (A) and CREAM (B) test chips

Table A.1: Test material - MiAMoRE

Structure	Type	Parameters				Comment
MOST		t_{GOX}	V_{th}	W/L	layout	
NT1				0.22/0.18		
NT2				0.66/0.36		
NT3				1.32/0.36		
NT4				1.98/0.18		Size
NT5				2.42/0.18	Standard	
NT6				2.42/0.36		variation
NT7				2.42/0.72		
NT8				12.5/0.36		
NT9			standard	1000/0.36	(multi-finger)	
NT2oc				0.66/0.36	Gate extension	
NT3oc				1.32/0.36	area 0.55 μm	Gate
NT9oc				1000/0.36	(multi-finger)	extension
NT2o				0.66/0.36	Gate	area
NT3o				1.32/0.36	extension	variation
NT8o	NMOS	<4 nm		12.5/0.36	area 1.96 μm	
NT9o				1000/0.36	(multi-finger)	
NTann3				12.5/0.36	Annular gate	
NTrs1				0.66/0.36	Ringed	Enclosed
NTrs2				1.32/0.36	source	layout
NTrs3				12.5/0.36		
NTh1				0.22/0.18		
NTh2				0.66/0.36		
NTh3				1.32/0.36		
NTh4				1.98/0.18		High
NTh5				2.42/0.18	standard	substrate
NTh6			high	2.42/0.36		doping
NTh7				2.42/0.72		
NTh8				12.5/0.36		
NTh9				1000/0.36	(multi-finger)	
PTh1				0.22/0.18		
PTh2				0.66/0.36		High
PTh3			high	1.32/0.36	standard	substrate
PTh4				1.98/0.18		doping
PTh5				2.42/0.18		

Structure	Type	Parameters				Comment
MOST		t_{GOX}	V_{th}	W/L	layout	
PTh6				2.42/0.36		High
PTh7			high	2.42/0.72	standard	substrate
PTh8				12.5/0.36		doping
PTh9				1000/0.36	(multi-finger)	
PT1				0.22/0.18		
PT2				0.66/0.36		
PT3				1.32/0.36		
PT4				1.98/0.18		
PT5		<4 nm		2.42/0.18	standard	Size
PT6				2.42/0.36		variation
PT7				2.42/0.72		
PT8				12.5/0.36		
PT9				1000/0.36	(multi-finger)	
PTann3				12.5/0.36	Annular gate	
PTrs1				0.66/0.36		
PTrs2	PMOS			1.32/0.36		
PTrs3				12.5/0.36	Ringed	Enclosed
PM1rs				0.95/0.7	source	layout
PM2rs				1.95/0.7		
PM3rs				12.5/0.7		
PMann3			standard	12.5/0.7	Annular gate	
PM1				0.55/0.5		
PM2				0.75/0.55		
PM3				0.9/0.7		
PM4				1.9/0.7		
PM5				2.5/0.5	standard	Size
PM6		>10 nm		2.5/0.7		variation
PM7				2.5/1		
PM8				12.5/0.7		
PM9				1000/0.7	(multi-finger)	
NM1				0.5/0.7		
NM2				0.75/0.7		
NM2ms	NMOS			0.75/0.7	standard	(metal shield)
NM3				0.95/0.9		

<table>
<tr><td>Structure</td><td rowspan="2">Type</td><td colspan="4">Parameters</td><td rowspan="2">Comment</td></tr>
<tr><td>MOST</td><td>t_{GOX}</td><td>V_{th}</td><td>W/L</td><td>layout</td></tr>
<tr><td>NM4</td><td rowspan="12">NMOS</td><td rowspan="12">>10 nm</td><td rowspan="12">standard</td><td>1.95/0.9</td><td rowspan="6">standard
(multi-finger)</td><td rowspan="6">Size variation</td></tr>
<tr><td>NM5</td><td>2.5/0.7</td></tr>
<tr><td>NM6</td><td>2.5/0.9</td></tr>
<tr><td>NM7</td><td>2.5/2.5</td></tr>
<tr><td>NM8</td><td>12.5/0.9</td></tr>
<tr><td>NM9</td><td>1000/0.9</td></tr>
<tr><td>NMann1</td><td>5.4/0.9</td><td rowspan="3">Annular gate</td><td rowspan="6">Enclosed layout</td></tr>
<tr><td>NMann2</td><td>8/0.9</td></tr>
<tr><td>NMann3</td><td>12.5/0.9</td></tr>
<tr><td>NMrs1</td><td>0.95/0.9</td><td rowspan="3">Ringed source</td></tr>
<tr><td>NMrs2</td><td>1.95/0.9</td></tr>
<tr><td>NMrs3</td><td>12.5/0.9</td></tr>
<tr><td>Structure</td><td colspan="2" rowspan="2">Type</td><td colspan="4">Parameters</td></tr>
<tr><td>Capacitor</td><td>C_{cap}, pF</td><td>Size</td><td colspan="2">number of sub-cells</td></tr>
<tr><td>MOSC1</td><td colspan="2" rowspan="2">MOS</td><td rowspan="3">30</td><td>10× 10</td><td colspan="2">40</td></tr>
<tr><td>MOSC2</td><td>20× 10</td><td colspan="2">20</td></tr>
<tr><td>MIMC</td><td colspan="2">MIM</td><td>24× 24</td><td colspan="2">1</td></tr>
<tr><td>Structure</td><td colspan="2" rowspan="2">Type</td><td colspan="4">Parameters</td></tr>
<tr><td>Diode</td><td>Area</td><td>Perimeter</td><td colspan="2">number of sub-cells</td></tr>
<tr><td>D1</td><td colspan="2" rowspan="3">Nwell in Sub</td><td rowspan="6">100μm</td><td rowspan="6">40μm</td><td colspan="2"></td></tr>
<tr><td>D2</td><td colspan="2"></td></tr>
<tr><td>D3</td><td colspan="2"></td></tr>
<tr><td>PD1</td><td colspan="2" rowspan="3">P+ in Nwell</td><td colspan="2"></td></tr>
<tr><td>PD2</td><td colspan="2"></td></tr>
<tr><td>PD3</td><td colspan="2"></td></tr>
<tr><td>Structure</td><td colspan="2" rowspan="2">Type</td><td colspan="4">Parameters</td></tr>
<tr><td>FOxFET</td><td colspan="2">metal/no metal</td><td colspan="2">Spacing, μm</td></tr>
<tr><td>STI1</td><td colspan="2" rowspan="6">N+ in Sub</td><td colspan="2" rowspan="3">metal</td><td colspan="2">0.28</td></tr>
<tr><td>STI2</td><td colspan="2">0.5</td></tr>
<tr><td>STI3</td><td colspan="2">1</td></tr>
<tr><td>STI4</td><td colspan="2" rowspan="3">no metal</td><td colspan="2">0.28</td></tr>
<tr><td>STI5</td><td colspan="2">0.5</td></tr>
<tr><td>STI6</td><td colspan="2">1</td></tr>
</table>

Structure		Type	Parameters		
Resistors			Resistance, kΩ	Size	Number
OPRRPRES		High-ohmic	80.4	2/50	2
OPRPPRES		Precision	1.7	2/50	8
Structure		Type	Parameters		
BJT			Size		Number
PNP1		PNP	2/1		20
PNP1			2/2		10
Structure		Type	Comment		
Inverter	INV1	Standard	Minimal size		
	INV2	Inverted source			
Ring oscillator	RO	Standard	With standard inverters		
	RO_RH	Radiation hardened	with inverted source inverters		
Output buffer	OutBuff	Radiation hardened	As in RO, for test		
Frequency divider	FD	Radiation hardened	D Flip-Flop based with output buffer, for test		
Total unique structures			103		
Total structures on chip			140		

Both test chips MiAMoRE and CREAM were realized for ceramic package with 120 pins. Ceramic package, as typically used for engineering samples was chosen in the first place for the possibility to de-lid the sample for irradiation tests. For MiAMoRE test chip two I/O pad rings (for two bonding diagrams) were placed around the chip to enable exhaustive testing of all relevant parameters. The bonding diagrams were planned in a way so that some of the test structures are present on both, as reference devices, and some are unique for the specific bonding diagram (BP1 or BP2). For CREAM test chip with fewer test structures, there have been only one bonding diagram. In total 40 samples of MiAMoRE test chip, 40 samples of CREAM and 5 SLM samples were available. Out of these samples, the most representative were chosen for TID testing.

Within different experiments, described later in this appendix, 39 MiAMoRE chips, 12 CREAM chips and 4 SLM chips have been tested after TID stress. This corresponds to minimal sample size for TID testing defined by [72].

TABLE A.2: Test material - CREAM

Structure	Parameters			
Diode	Type	Segment area	Segment perimeter	number of Segments
ND1 and ND2	N+ in Sub	$100\,\mu m^2$	$40\,\mu m$	1394
ND3 and ND4				990
ND5				950
ND6				626
NESD1...NESD4		$72\,\mu m^2$	$202.9\,\mu m$	1
PESD1..PESD4	P+ in Nwell	$107\,\mu m^2$	$302\,\mu m$	
PNESD1	P+ in Nwell to VDD N+ in Sub to VSS	$107\,\mu m^2$	$302\,\mu m$	
PNESD2				
PNESD3				
PNESD4				
Current mirror	Type	Realization		Number on chip
CMN	NMOS	Simple		2
CMNRH		Radiation hardened		
CMP	PMOS	Simple		
CMPW		Wilson		
Current source	Realization			Number on chip
CS	Simple			2
CSRH	Radiation Hardened			
T-Gate switch	Realization			Number on chip
TG	Simple			2
TGRH	Radiation Hardened			
TGLL	Low leakage			
Bandgap	Type		Realization	
BG	Simple		Standard	
BGRH	Trimmable		Radiation Hardened	
Amplifier	Realization			Number on chip
CSA	Single-ended charge sensitive radiation hardened			7
Buff	Differential radiation hardened, used as a buffer			1
Total unique structures			20	
Total structures on chip			46	

Table A.3: Test material - SLM chips provided by foundry

Chip	Device	Parameters		
	MOS Transistor	Type	t_{GOX}	W/L
SLM chip 1	PFET1	PMOS	<4 nm	0.22/5
	PFET2			0.22/0.18
	PFET3			5/5
	PFET4			5/0.18
	PFETM1		>10 nm	5/0.5
	PFETM2			5/5
	PFETM3			0.5/0.5
	PFETM4			0.5/5
	NFETM1	NMOS		5/5
	NFETM2			5/0.7
	NFETM3			0.5/0.7
	NFETM4			0.5/5
	NFET1		<4 nm	5/0.18
	NFET2			5/5
	NFET3			0.22/5
	NFET4			0.22/0.18
SLM chip 2	Diode	Type	Area, μm^2	Perimeter, μm
	NWA	N-Well in Sub	8500	440
	NWP			17340
	NXP	N+ in Sub	2691	7588
	NXA		2296	192
	PNWA	P+ in N-Well		
	PNWP		2691	7588

2 Electrical characterization

All test structures were electrically characterized before and after irradiation, as well as at selected TID steps. The electrical characterization was semi-automated to optimize both test time and test complexity. The instruments for electrical characterization were controlled with Matlab program from computer via GPIB interface. During a single run, some mechanical changes in the set-up (re-plug of cables or chips) were required. This allowed simpler printed circuit board (PCB) design with less parasitics influencing measurement results.

A principal measurement set-up for DC characterization is depicted in Fig. A.2. The principal components here are the characterization PCB for the particular test chip characterized, power supplies for this PCB and for the chip under characterization, the pA-meter for precise current measurement, and computer with automated measurement

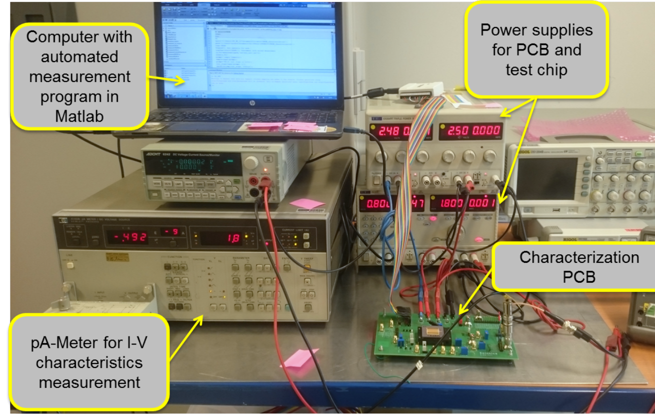
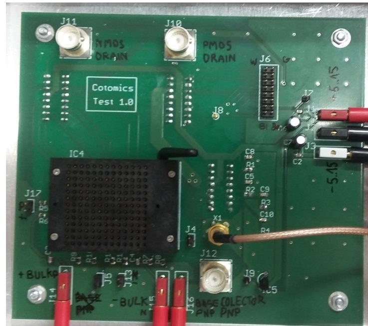


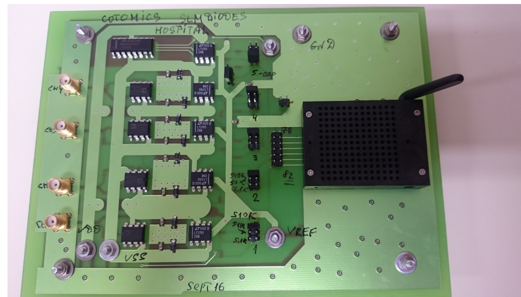
FIGURE A.2: Measurement set-up for electrical characterization of DC parameters

program in Matlab. Depending on structure and chip under test, additional measurement instruments, such as source-meter, oscilloscope or multimeter also seen in the photograph, were included into set-up.

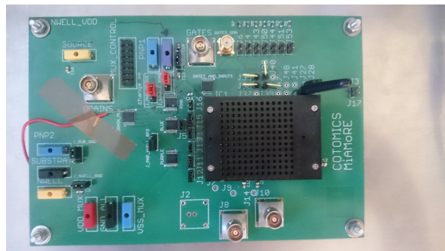
The PCBs for electrical characterization of SLM chip 1, SLM chip 2, MiAMoRE and CREAM are shown in Fig. A.3.



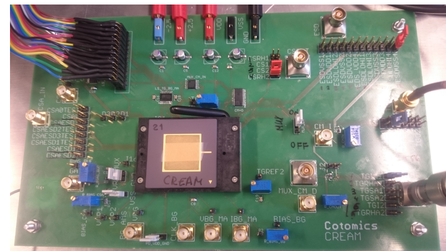
(A) SLM chip 1



(B) SLM chip 2



(C) MiAMoRE



(D) CREAM

FIGURE A.3: PCB for electrical characterization of test chips SLM chip 1(A), SLM chip 2(B), MiAMoRE (C) and CREAM (C).

PCBs for SLM chip 1 and SLM chip 2 have been designed by the project leader Alicja Michalowska-Forsyth. As the results obtained from the initial experiments conducted

on these two PCBs served as a starting point for my investigations, I briefly describe the major considerations within these experiments, and corresponding hardware.

Three major measurements were performed on SLM chip 1: transfer and output characteristics of MOS transistors, and I-V characteristics of bipolar transistors. For the SLM chip 1 characterization PCB, two major factors were taken into account. First, low leakage multiplexers were chosen to ensure accurate leakage current measurements of the MOS transistors. Secondly, test time was kept below 1 hour to ensure measurement pauses between irradiation steps at remote location are according to standard [72].

From the experiments on SLM chip 1 not only the major radiation effects in given technology, but also minor flaws in measurement set-up have been identified. So, the low leakage multiplexers for automated measurement of the transistors have influenced the measurement results with relatively high voltage drop on drain of the MOS transistors during transfer characteristics measurement. Also, irradiation interruptions time of 2 hours has been found to be too long to avoid annealing in the particular experimental set-up. These discoveries have had major influence on future test design for MiAMoRE and CREAM test chips, discussed later on.

SLM chip 2 was used in transient X-ray effects measurements under actual CT in a hospital. This lead to main design requirements to the characterization PCB. First, the periphery electronics had to be spatially separated from the test chip: the measurement circuitry on PCB was located aside from the test chip, and the measurement instruments were situated in the control room behind a lead door. Secondly, few options for current sensing had to be realized to allow few orders of magnitude measurement window, as radiation source was not well defined.

In this experiment we have experienced major electromagnetic compatibility issues, due to spatial separation of measurement equipment from the device under test, as illustrated by Fig. A.4. From the measurements it can be assumed that the noise from the hospital environment is picked up be the long cables acting as antennas, overlapping with actual X-ray transient signal, collected by means of charge sensitive amplifier, realized on board. In order to avoid such problems it has been decided to integrate this experiment on one of the future chips, which has been realized on CREAM test chip with charge sensitive amplifier (CSA).

FIGURE A.4: Illustration of experimental setup and measured signal during the hospital experiment.

PCBs for MiAMoRE and CREAM chips were designed by myself. The results reported and analysed in this work are entirely based on these experiments.

MiAMoRE test chip incorporates over 100 devices (see Table A.1). Thus it has been a great challenge to find an appropriate trade-off between test time, test complexity and test accuracy. First of all to ensure accuracy, different kind of multiplexers, than in SLM tests, was used. The multiplexers with both sufficiently low leakage current and low on-resistance, were chosen. During the design of MiAMoRE its testability had to be ensured. Having 120 pins to be tested the complexity of PCB would have been enormous, and the connections long. This would lead to accuracy decrease. That is why a design decision to make a rotatable chip has been made, as shown in Fig. A.5. This way measurement periphery on PCB had to suffice only for half the pins, requiring however manual 180° rotation of the chip half the way through characterization.

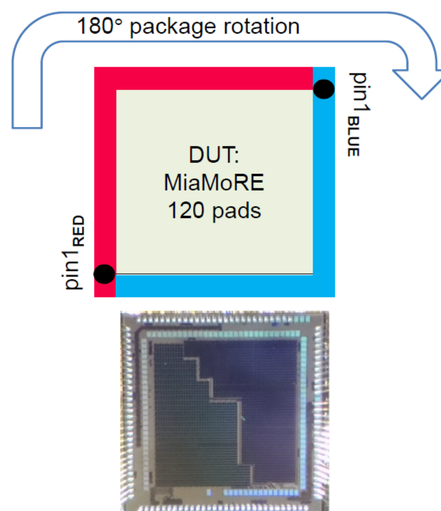


FIGURE A.5: Diagram of MiAMoRE chip rotation for test

As physically re-plugging the chip is a timely procedure, the measurement time had to be additionally reduced. Also, having observed some rapid annealing in experiments on SLM samples, the test time had to be kept even shorter. That is why measurements have been reduced down to transfer characteristics for MOS transistors, and I-V sweeps for other devices. Transfer characteristics of MOS transistors were measured at two values of drain-source voltage in linear and saturation region before and after irradiation. At the chosen TID steps, only linear region transfer characteristics were measured and separate single point leakage current measurement was performed. These measurements suffice to extract relevant DC parameters. Also number of measurement points was carefully optimized down to 30 per device. Altogether this allowed measurement time of 12 minutes per chip side and total time below half an hour. Also flicker noise of chosen devices has been characterized. Noise measurements are described separately in Appendix B.

There are less structures on CREAM test chip, than on MiAMoRE, but these structures are more heterogeneous. This means high variety of measurements to be performed in electrical characterization. Test design was individual for every group of structures. So, some structures could be measured automatically via multiplexers. For some structures, such as ESD protection structures, direct measurement was necessary to ensure accurate leakage current measurement. During CREAM characterization the most time consuming part was thus re-plugging the jumpers and cables for such semi-automated measurements, and performing manual measurements where necessary. To increase usability of the measurement, a Matlab program, combining automatic measurement and instructions for manual measurements was implemented. Total test time was 40 minutes.

All measurements were done at room temperature of 24°C±6°C as defined by standard guide ASTM F1892-12 [72].

3 Irradiation experiments

Within this section I only discuss experiments the results of this work originate from. For SLM chips experiments results see [48]. All relevant experiments were conducted with X-ray sources. There have been three facilities (A, B and C) and two types of X-ray tubes: one with copper target (I) and two with tungsten target (II). All structures have been

remotely electrically characterized before irradiation and after the target TID. Some of the structures have been characterized at intermediate TID steps, few structures were monitored in-source during irradiation. Time between irradiation steps never exceeded 2 hours, as recommended by [72] and [74]. Fig. A.6 illustrates experimental flow. Table A.4 summarizes conducted experiments.

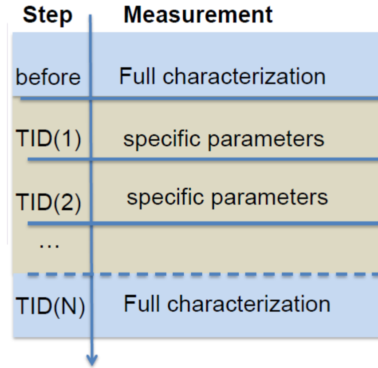


Figure A.6: Principal diagram of irradiation experiments flow.

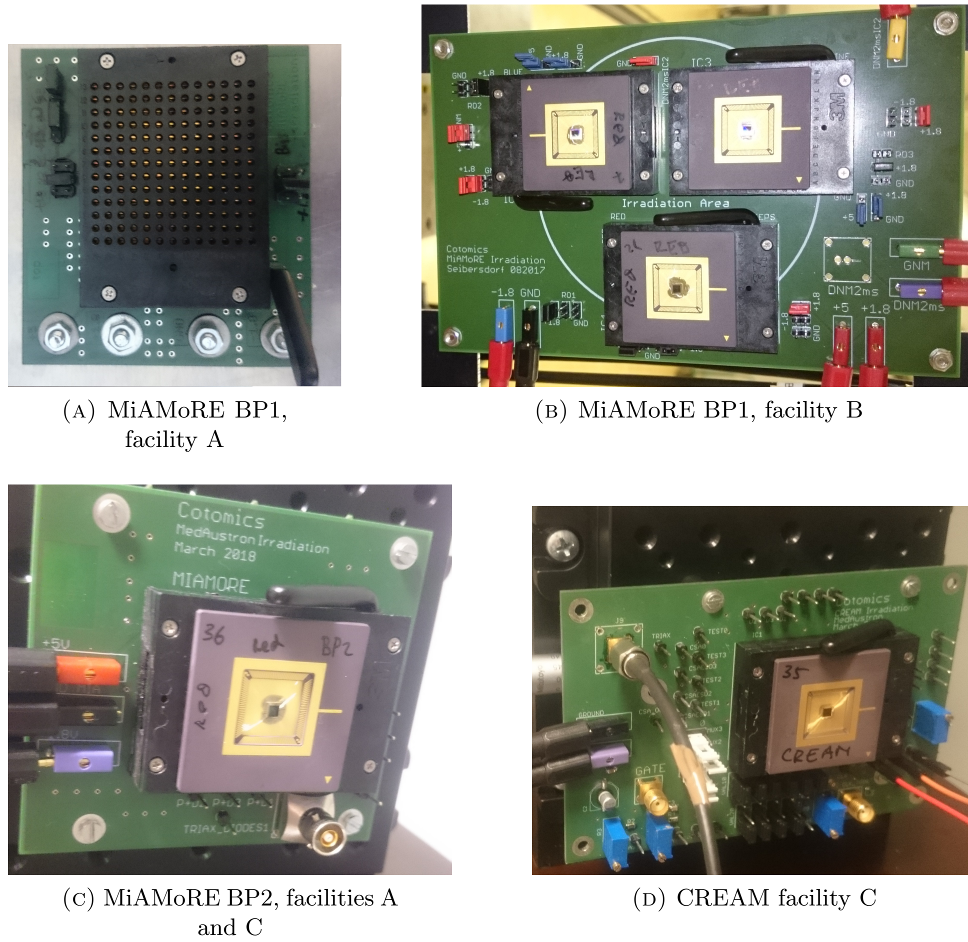
Table A.4: Irradiation experiments

Experiment	Facility	Test chip	Number of		
			samples	unique bias conditions	dose rates
1	I-A	MiAMoRE	6	2	3
2	II-B		8	5	1
3	I-A		14	4	3
4	II-C		5	1	3
		CREAM	12	1	3

In all experiments a separate PCB for electrical bias of the test structures under irradiation was used, in order to avoid radiation effects on measurement periphery. These PCBs are shown in Fig. A.7.

PCB design was dictated by irradiation facility capabilities. So, at irradiation facility B, irradiation of multiple chips at once due to 10 cm diameter of uniform X-ray field was possible, contrary to other facilities offering local irradiation of <1 cm, due to field intensity gradients.

Tables A.5-A.9 summarize bias conditions during irradiation during corresponding experiment and the samples tested at these conditions. Terminals not listed in these tables were either left floating or set to 0 V. Tables A.10-A.14 summarize dose rates during corresponding experiments and lists samples tested at these dose rates.



(A) MiAMoRE BP1, facility A

(B) MiAMoRE BP1, facility B

(C) MiAMoRE BP2, facilities A and C

(D) CREAM facility C

FIGURE A.7: PCBs for electrical bias during irradiation.

TABLE A.5: Bias conditions during Experiment 1 - MiAMoRE test chip

Sample #	9, 10, 12, 13, 14, 15	
Device group	V_{GS}, V	Other terminals
NMOS t_{GOX} <4 nm	+1.8	0
NMOS t_{GOX} >10 nm	+5	0
PMOS	0	
other structures	0	

Table A.6: Bias conditions during Experiment 2 - MiAMoRE test chip

	Sample #	6	16	2	19	7	21	4	22
V_{GS}, V	NMOS t_{GOX} <4 nm	0.6				1.8			
	PMOS	0							
	NMOS t_{GOX} >10 nm	0		0.6		5		0.6	
V_{DS}, V	NM2ms	0		0.05		0		0.05	
	other	0							
V_{STI}, V		-1.8				1.8		-1.8	1.8
V_{cap}, V	MOS capacitor	0							
	MIM capacitor	0				5			
Inverter input		RO_{out}				1.8 V			
Inverter VDD, V		0							
V_{res}, V		0.6				1.8			

Table A.7: Bias conditions during Experiment 3 - MiAMoRE test chip

Bias condition		GREEN	BLUE	ORANGE		PINK						YELLOW			
Bonding plan		BP1						BP2							
Sample #		8	17	3	25	23	24	26	28	30	32	34	29	31	33
V_{GS}, V	NMOS t_{GOX} <4 nm	+1.8	0	+1.8		0.7		1.8				0.7			
	NMOS t_{GOX} >10 nm	0	+5			0.7						+5			
	FOXFET	-1.8		+1.8		0									
V_{DS}, V	NMOS t_{GOX} <4 nm	0				0.7		0				0.7			
	NMOS t_{GOX} >10 nm	0				0.7						0			
	FOXFET	0													
V_{DD}, V	Inverter	+1.8	–			+1.8		–							
INV_{IN}, V		0	–			+1.8		–							

Table A.8: Bias conditions during Experiment 4 - MiAMoRE test chip

Sample #	27, 36, 37, 38, 40	
Device group	V_{GS}, V	Other terminals
NMOS t_{GOX} <4 nm	+1.8	0
NMOS t_{GOX} >10 nm	+5	0

Table A.9: Bias conditions during Experiment 4 - CREAM test chip

Sample #	Structure	Terminal	Bias	
6, 7, 8, 11, 12, 13, 14, 15, 21, 31, 36, 40	CSA	Switch Gate	1.8 V	10 kHz rectangular wave
	BandgapRH	val1	1.8 V	
		val2	0 V	
	T-Gate	Input	1.8	1 kHz rectangular wave
		Enable	0	
11, 12, 13, 14			1.8	

Table A.10: Beam settings and dose rates during Experiment 1 - MiAMoRE test chip

Sample #	9, 10, 12, 13, 14, 15					
Condition	Tube		Energy		Filter	Dose
	voltage	current	maximal	mean		rate
a	40 V	40 mA	40 keV	8 keV	Al 0.2 mm	0.01 rad/s
b					Al 0.1 mm	1 rad/s
c					no	100 rad/s

Table A.11: Beam settings and dose rates during Experiment 2 - MiAMoRE test chip

Sample #	2, 4, 6, 7, 16, 19, 21, 22			
Tube		Energy		Dose
voltage	current	maximal	mean	rate
150 kV	10 mA	150 keV	60 keV	1.5 rad/s

Table A.12: Beam settings and dose rates during Experiment 3 - MiAMoRE test chip

Sample #	3, 8, 17, 23, 24, 25, 26, 28, 29, 30, 31, 32, 33, 34					
Condition	Tube		Energy		Filter	Dose
	voltage	current	maximal	mean		rate
a	40 V	40 mA	40 keV	8 keV	Al 0.2 mm	0.01 rad/s
b					Al 0.1 mm	1 rad/s
c					no	100 rad/s

Table A.13: Beam settings and dose rates during Experiment 4 - MiAMoRE test chip

Samples#	Condition	Tube		Energy		Dose
		voltage	current	maximal	mean	rate
38, 40	α	200 kV	21 mA	200 keV	60 keV	300 rad/s
27	β	150 kV	10 mA	150 keV	60 keV	1.5 rad/s
36, 37	γ	40 kV	14 mA	40 keV	10 keV	10 rad/s

Table A.14: Beam settings and dose rates during Experiment 4 - CREAM test chip

Samples #	6, 7, 8, 11, 12, 13, 14, 15, 21, 31, 36, 40			
Tube		Energy		Dose
voltage	current	maximal	mean	rate
200 kV	21 mA	200 keV	60 keV	300 rad/s

Appendix B

Noise Measurements

"No! Please! I'll tell you whatever you want to know!" the man yelled.

"Really?" said Vimes. "What's the orbital velocity of the moon?"

"What?"

"Oh, you'd like something simpler?"

—Terry Pratchett, Night Watch

Flicker noise ($1/f$) measurements were performed on a noise measurement system as described in [94]. First, DC characteristics of the device under test were measured. From these characteristics appropriate measurement system parameters are calculated and set. Then the noise measurement at pre-defined drain current values is performed.

Noise measurements were performed on 8 samples before irradiation. Additionally, wafer level noise measurements were performed on the same wafer lot prior to irradiation experiments. This was done to make a pre-selection of the most suited samples for irradiation, representing the most average behaviour. The noise measurements after irradiation were then performed on 2 representative samples out of 8 irradiated, due to limited time of access to measurement facilities and to avoid annealing of the radiation effects. Noise measurements after irradiation were conducted within 36 hours after irradiation. Until then, samples were stored in a temperature controlled environment at 0°C, to preserve the effects. In order to avoid condensation silica gel was put into the storage boxes prior to cooling.

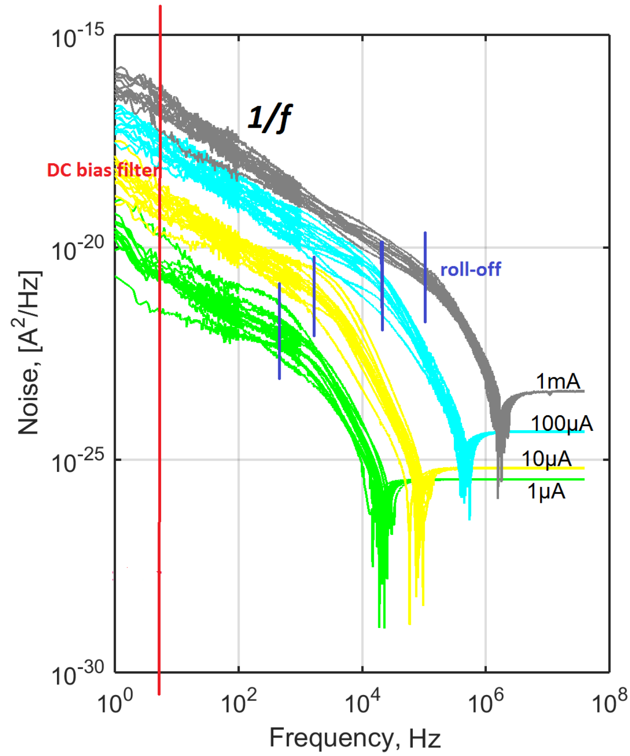


FIGURE B.1: Measured drain current noise density $S_{I_{DS}}$ of NMOS with t_{GOX} >10 nm over 13 dies (not irradiated). Blue markers indicate average roll-off frequency of the measurement system for the particular current setting

Fig. B.1 illustrates the noise spread between different dies for NMOS with t_{GOX} >10 nm and W/L=1000/0.9 at different current levels. The valid $1/f$ data is in the region between red and blue markers. The limiting factor at lower frequencies is the contribution of the DC bias filter with corner frequency around 3 Hz (red marker). The blue marker indicates the roll-off frequency of the measurement system for a particular device and current setting.

All noise measurements were performed in temperature controlled environment at 25°C [72] and the identical hardware set-up was used before and after irradiation to minimize measurement error.

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