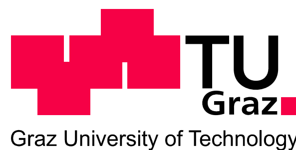
Gerald Rescher, BSc

Electrical characterization of SiC MOSFET interface properties

MASTER THESIS

For obtaining the academic degree
Diplom-Ingenieur

Master Programme of
Technical Physics



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Graz, March 2015

Deutsche Fassung:
Beschluss der Curricula-Kommission für Bachelor-, Master- und Diplomstudien vom 10.11.2008
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Kurzfassung

Silicium war für lange Zeit der Halbleiter der Wahl für Leistungselektronik. Halbleiter mit großer Bandlücke wie Siliciumcarbid (SiC) und Galliumnitrid (GaN) versprechen allerdings eine Steigerung der Performance von zukünftigen Leistungselektronikbauteilen. Sie ermöglichen den Betrieb bei höherer Temperatur, höherer Leistungsdichte, höherer Spannung und höherer Frequenz als Bauteile basierend auf herkömmlicher Siliciumtechnologie. Die Forschung an Halbleitern mit großer Bandlücke läuft bereits seit einigen Jahrzehnten. Kommerziell erhältlich sie allerdings erst seit einigen Jahren. Das liegt vor allem an der noch immer relativ schlechten Zuverlässigkeit im Vergleich zu Bauteilen basierend auf Silicium. Erste kommerzielle Siliciumcarbid Metall Oxid Halbleiter Feldeffekttransistoren (englisch: metal oxide semiconductor field effect transistors (MOSFETs)) sind seit 2011 verfügbar.

Diese Arbeit beschäftigt sich mit der Untersuchung der Grenzflächeneigenschaften von Siliciumcarbid MOSFETs im Hinblick auf ihre Zuverlässigkeit. Die Grenzfläche in SiC-MOSFETs zwischen Siliciumdioxid und Siliciumcarbid ist hauptverantwortlich für die elektrischen Eigenschaften von MOSFETs. Hier auftretende Defekte sind direkt in der Performance des Chips zu sehen. Die Industrie kennt bereits mehrere Möglichkeiten zur Verringerung der Grenzflächendefektdichte während der Produktion. Dieses sogenannte *annealing* (english für Aushärten bzw. Ausglühen) in einer bestimmen Gaskomposition bei hoher Temperatur sorgt zwar für einen starken Rückgang der Defektdichte, allerdings liegt diese immer noch weit über dem Niveau von Siliciumhalbleitern. Eine Optimierung des *Annealing*-Vorgangs ist deshalb von großem Interesse für die Industrie. Die vielversprechensden Ergebnisse bezüglich der Reduktion der Grenzflächendefektdichte zeigt zur Zeit *annealing* unter einer Stickstoffmonoxid (NO) Atmosphäre. Der Einfluss der *Annealing* Zeit und *Anneling* Temperatur auf die Zuverlässigkeit des MOSFETs in Hinblick auf Spannungs-Temperatur Instabilität (english: bias temperature instability

(BTI)) und Betriebswiderstand wurde untersucht und eine starke Abhängigkeit von den *Annealing* Parametern festgestellt.

Die Arbeit wurde in Kooperation mit der KAI - Kompetenzzentrum für Automobil- und Industrieelekronik GmbH und der Infineon Technologies Austria AG realisiert. Die wesentlichen Ergebnisse dieser Arbeit wurden auf der europäischen Konferenz für Siliciumkarbid und verwandte Materialien (European Conference of Silicon Carbide and Related Materials (ECSCRM) 2014) präsentiert.

Abstract

Silicon has long been the semiconductor of choice for power electronics. Wide band gap semiconductor materials like silicon carbide (SiC) and gallium nitride (GaN) promise a better performance in future power devices. They allow an operation at higher temperatures, higher power density, higher voltage and higher frequency than silicon based devices. Research focusing on wide band gap semiconductor materials has been going on for many decades. However, SiC metal oxide semiconductor field effect transistors (MOSFETs) are only since a few years commercially available. First SiC-MOSFETs are available since 2011. This is mainly due to the more severe reliability issues compared to silicon based devices.

This thesis investigates the interface properties of silicon carbide MOSFETs with respect to their reliability properties. The interface between the silicon dioxide and the silicon carbide is mainly responsible for the electrical properties of the device. Defects in this region impact the output characteristics of the devices directly. To reduce the density of interface states the industry uses annealing in certain gas atmospheres. However, the resulting defect density is still much higher than in silicon based devices and strongly dependent on the annealing process used. Therefore, an optimization of the annealing process is of great interest for the industry. At the moment, the highest reduction in defect density is achieved by nitrous oxide (NO) annealing. The impact of the annealing time and annealing temperature on the on-resistance and the reliability after bias temperature instability stress tests was investigated in this thesis and a strong dependence on the annealing parameters was observed.

The thesis resulted from a cooperation with KAI - Kompetenzzentrum Automobil- und Industrieelektronik - GmbH and Infineon Technologies Austria AG. The main results were presented at the European Conference for Silicon Carbide and Related Materials (ECSCRM 2014).

Danksagung

Diese Arbeit wäre ohne die Unterstützung von Freunden, Kollegen und Familie nicht möglich gewesen. Ich bedanke mich hiermit bei all den Leuten, die mich auf diesen Weg begleitet haben.

Angefangen bei meinem Studienkollegen Klaus Lang, der mir immer mit Rat und Tat zur Seite stand. Des Weiteren bedanke ich mich bei meinen Kollegen bei Infineon Technologies Austria. Insbesondere bei Paolo del Croce und dem restlichen Team von ATV BP PD1 bei welchen ich die ersten Einblicke in die Entwicklung von Halbleiterprodukten bekommen habe und Thomas Aichinger für seine Unterstützung während meiner Diplomarbeit.

Ich bedanke mich weiters bei all meinen Kollegen am Kompetenzzentrum für Automobil und Industrieelektronik für ihre Unterstützung während meiner Arbeit. Besonders hervorheben möchte ich hierbei Michael Nelhiebel, dafür diese Chance bekommen zu haben, und Gregor Pobegen der sich immer Zeit für alle meine Anliegen und Fragen nahm.

Ich bedanke mich natürlich auch bei Prof. Peter Hadley für die einwandfreie Betreuung meiner Diplomarbeit.

Besonderer Dank gilt natürlich meinen Eltern, die mich mein ganzes Leben lang auf meinem Weg unterstützt und mir all das erst ermöglicht haben.

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Part I.

FUNDAMENTALS

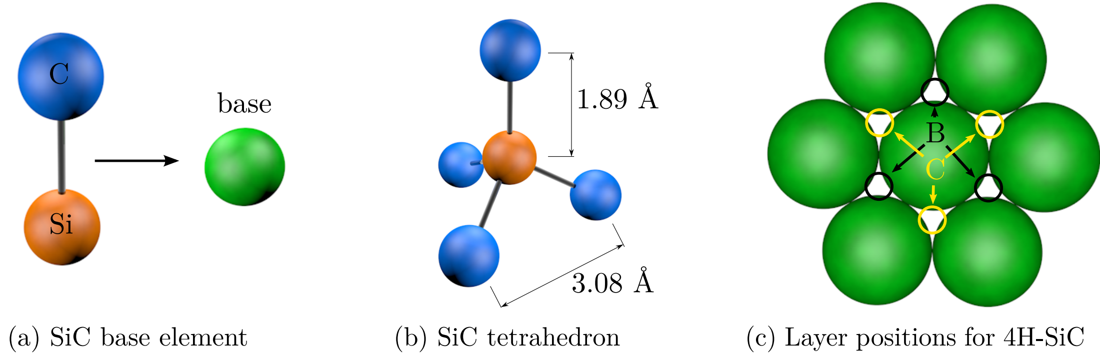
1

Material properties of silicon carbide

1.1. The silicon carbide crystal

The common building block for a silicon carbide (SiC) crystal is the SiC tetrahedron (see Fig. 1.1b) consisting of four carbon atoms bound to one silicon atom (or one carbon atom bound to four silicon atoms). Silicon carbide forms a large amount of different crystal structures called polytypes. So far, more than 250 SiC polytypes have been reported. The basic structural elements is the SiC bilayer composed of one silicon (Si)-plane and the adjacent carbon (C)-plane. A particular polytype can be constructed of a certain stacking sequence of the tetrahedrally bonded SiC bilayers. The next layer can be aligned in two different ways according to Fig. 1.1c. The resulting lattice structure can be cubic, hexagonal or rhombohedral. The labeling of the polytypes consists of the stacking sequence of the bilayers and the lattice structure. Examples for the different structures are 3C-SiC for a 3-layer cubic structure, 2H, 4H- and 6H- SiC for a hexagonal structure and 16R- and 21R-SiC for a rhombohedral structure.

Out of the high amount of all the polytypes, the 4H-SiC is the preferred one for semiconductor devices because of its wide band gap of about 3.26 eV and the relatively high



(a) SiC base element (b) SiC tetrahedron (c) Layer positions for 4H-SiC

Figure 1.1.: (a) Base element of the SiC crystal consisting of one silicon and one carbon atom. For easier understanding of the conventional unit cell (see Fig. 1.2), the basis is shown as a single green or yellow sphere. (b) The SiC tetrahedron and bond lengths. (c) Stacking positions of the layers B and C relatively to layer A. Every circle in (c) marks a point on the conventional unit cell of the 4H-SiC crystal and therefore represents two atoms.

nearly isotropic electron mobility ($\mu_{\max} \approx 950\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$) [1][2][3]. 4H-SiC consists of three layers A, B and C in the stacking order ABCB as shown in figure 1.2. Figure 1.1c shows the position of the layers B and C stacked up with respect to layer A [4].

The Si-C bond length is about 1.89 Å which is less than the bond length of silicon in a silicon crystal (about 2.35 Å) [5] and therefore leading to a much higher physical stability. Some material properties of 4H - silicon carbide are far superior than the silicon ones like the much higher critical field (SiC: $2.2\,\mathrm{MV\,cm^{-1}}$, Si: $0.3\,\mathrm{MV\,cm^{-1}}$) and high thermal conductivity (SiC: $3.7\,\mathrm{W\,cm^{-1}\,K^{-1}}$ vs Si: $1.5\,\mathrm{W\,cm^{-1}\,K^{-1}}$). Also SiC has a much lower intrinsic carrier concentration than silicon and, thus, devices build with this material are less susceptible to difficulties due to high intrinsic carrier concentrations at temperatures beyond 600° [6]. These properties make SiC the preferred material for high power and high temperature semiconductor devices. Table 1.1 shows a comparison between the key constants of 4H-SiC and silicon.

1.2. Electronic properties

The electronic structures of six SiC polymorphs were calculated by Ching et al. [10] using the orthogonalized linear combination of atomic orbitals method (OLCAO). Fig. 1.3 shows the calculated band structures of the six silicon carbide polytypes 3C, 2H, 4H, 6H ,16R and 21R. All calculated polytypes have indirect band gaps. The calculated

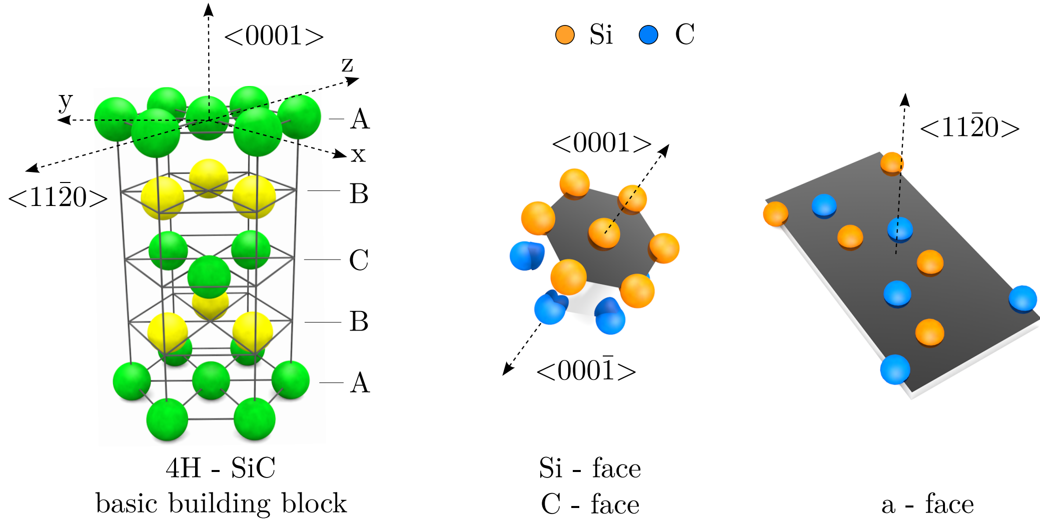


Figure 1.2.: 4H-SiC basic building block and two example faces important for oxide growth. Note that the green and yellow spheres represent a pair of C and Si atoms as shown in Fig. 1.1.

values of the band gaps are listed in Table 1.2. Note that the calculated band gaps are underestimated by about 1 eV due to the calculation method used. However, the relative variations in the size of the gap values between different polytypes are expected to be similar to experimental values.

Calculations done by G.L. Zhao and D. Bagayoko [11] show a better agreement with the experimental data. The 4H-SiC electronic structure and density of states calculated by them are shown in Fig. 1.4. They calculated a indirect 4H-SiC band gap of 3.11 eV,

Table 1.1.: Key constants of 4H-SiC and silicon [7][8][9].

Quantity	**4H-SiC**	**Silicon**
Band gap E_{G} (eV)	3.26	1.12
electron mobility μ_{e} ($\mathrm{cm^2\,V^{-1}\,s^{-1}}$)	1000	1400
$\mu_{\perp}$ / $\mu_{\parallel}$	0.8	1
hole mobility μ_{h} ($\mathrm{cm^2\,V^{-1}\,s^{-1}}$)	115	471
electron effective mass m^* / m_0	0.29-0.42	0.26
critical field ξ_{c} ($\mathrm{MV\,cm^{-1}}$)	2.2	0.3
dielectric constant ε_{s} / ε_0	6.5-6.7	11.7
Young's modulus Y (GPa)	100-750	47
Thermal conductivity θ ($\mathrm{W\,cm^{-1}\,K^{-1}}$)	3.7	1.5
Debye temperature T_{d} (K)	1300	640

Table 1.2.: Bandgap for different SiC polytypes.

Polytype	**calc. E_G (eV) [10]**	**exp. E_G (eV) [12]**
3C	1.602	2.39
2H	2.471	3,33
4H	2.433	3.27
6H	2.202	3.02
15R	2.156	n.a.
21R	2.034	n.a.

which is very close to the experimental value. Also charge-transfer calculations were done by [11] showing that silicon atoms donate about 1.4 electrons/atom that are received per carbon atom. Therefore, the ionic formula of 4H-SiC can be written as $Si^{+1.4}C^{-1.4}$.

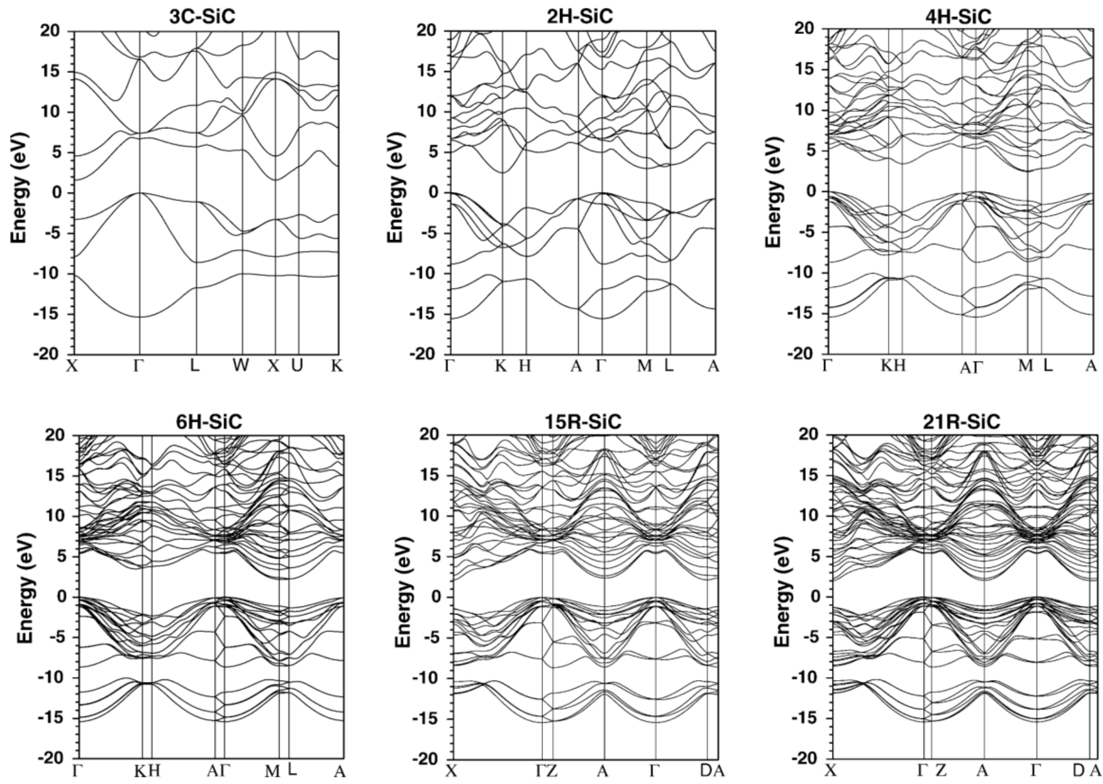
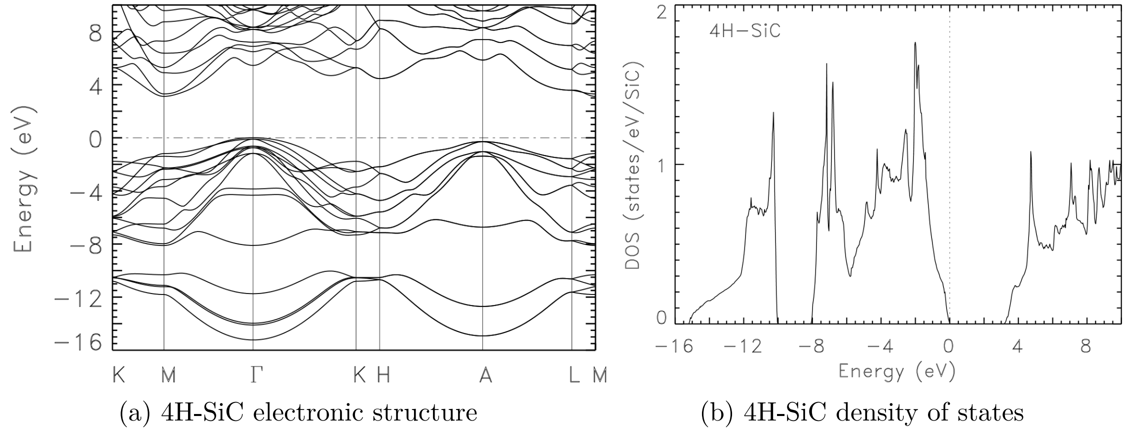


Figure 1.3.: Electronic structure of multiple SiC polytypes [10].



(a) 4H-SiC electronic structure

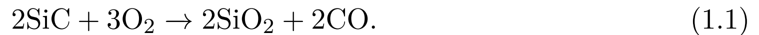
(b) 4H-SiC density of states

Figure 1.4.: 4H-SiC electronic structure and density of states as published in [11].

1.3. Crystal faces and oxidation

The most commonly used faces for 4H-SiC device fabrication are the (0001) Si-face, the $(000\bar{1})$ C-face and the $(11\bar{2}0)$ a-face (see Fig. 1.2). They differ in the density of silicon and carbon atoms. The Si-face has 100 % silicon atoms, the C-face has 100 % carbon atoms and the a-face has 50 % of each. This leads to distinct oxidation rates and interface properties for every crystal face.

A main benefit of SiC is the possibility to grow a thermal oxide. As for silicon, the native oxide of SiC is silicon dioxide (SiO_2). Therefore, the silicon process technology can be straightforwardly transferred to silicon carbide. As in silicon, oxygen inserts in the semiconductor to from SiO_2. In SiC, some of the oxygen is also necessary to remove the carbon by forming carbon monoxide (CO). A net oxidation reaction can be written as



$$2\mathrm{SiC} + 3\mathrm{O}_2 \rightarrow 2\mathrm{SiO}_2 + 2\mathrm{CO}. \qquad (1.1)$$

The oxidation rate in SiC scales with the carbon content of the crystal face. The SiO_2 growth rate on the Si-face is about 10 times slower than on silicon ((001)-face) and about 5 times slower on the C-face [7]. The quality of the SiC-SiO_2 interface is a critical parameter in oxide based devices. However, modern oxide growth and depositing techniques are

still causing a lot of interface defects. The reduction of these defects via post oxidation annealing POA is partially treated in this thesis.

2

Device physics

Silicon carbide technology is suitable to outperform silicon technology in high power devices. The operating voltages of devices are limited by the blocking voltage of the pn-junction and therefore limited by the electrical breakdown field of the material. The breakdown field of silicon carbide ($\xi_c \approx 2.2\,\mathrm{MV\,cm^{-1}}$) is more than 7 times higher than the breakdown field of silicon ($\xi_c \approx 0.3\,\mathrm{MV\,cm^{-1}}$). In the case of a one-sided junction (n doping $\ll$ p doping), the width of the depletion layer is approximately given by

$$x = \sqrt{\frac{2\varepsilon V}{q N_\mathrm{d}}} \tag{2.1}$$

with the density of positively charged donor atoms N_d, the dielectric constant of the semiconductor ε, the elementary charge q and the bias voltage V. The field reaches its maximum at the junction

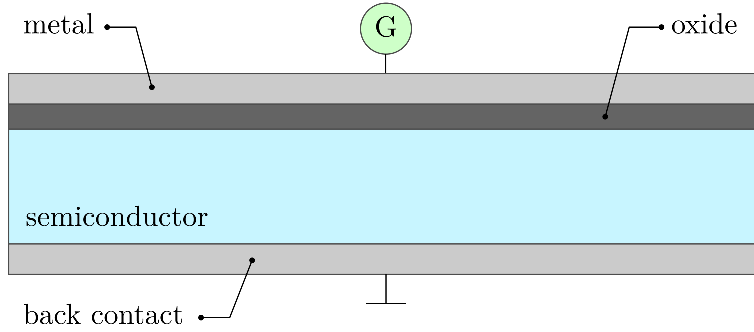


Figure 2.1.: Schematics of a MOS-structure consisting of a semiconductor with an insulating layer and the contact metals on the top (from now on called gate contact) and the bottom.

$$\xi_{\max} = -\frac{2V}{x} = -\sqrt{\frac{2qN_\mathrm{d}V}{\varepsilon}}. \tag{2.2}$$

If the maximum electrical field $\xi_{\max}$ reaches the critical field ξ_c avalanche breakdown occurs. Therefore, the maximum blocking voltage V_c supported by the junction can be described as

$$V_\mathrm{c} = \frac{\varepsilon\xi_\mathrm{c}^2}{2qN_\mathrm{d}}. \tag{2.3}$$

The maximum blocking voltage for a SiC junction is therefore expected to be about 30 times higher than the blocking voltage of a Si junction [7].

Silicon carbide can be straightforwardly processed in a fabrication line originally developed for silicon processing. Today, the development of SiC metal oxide semiconductor field effect transistors (MOSFETs) is of great interest for the industry. Therefore, the next sections give a short review on metal oxide semiconductor (MOS) structures and MOSFETs.

2.1. The MOS structure

The MOS-structure is the fundamental part of a MOSFET (see section 2.2). The basic concept of a MOS structure (or MOS-capacitor) is shown in Fig. 2.1. It consists of a

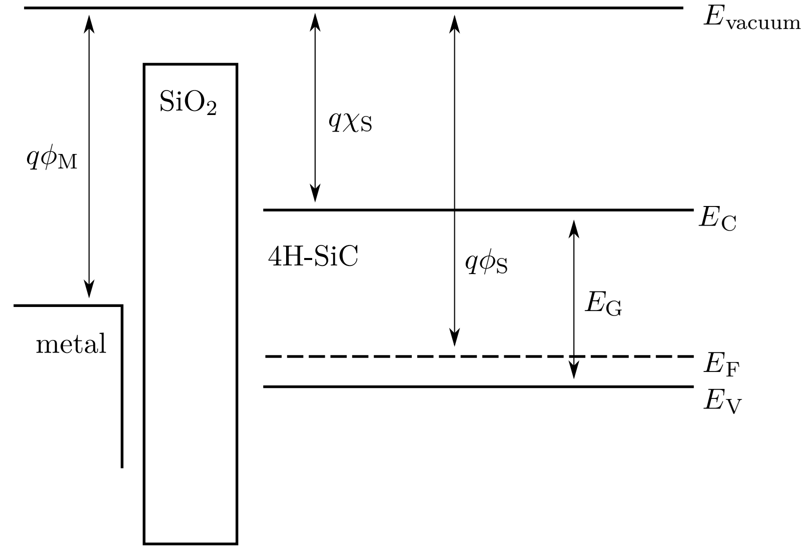


Figure 2.2.: Schematic energy band diagram for a p-doped 4H-SiC MOS structure without contact between the different materials. The picture shows the work function for the semiconductor ϕ_S and the metal ϕ_M, the band gap E_G and the electron affinity χ.

semiconductor with a thin insulating layer on top (oxide). On the insulating layer a metal contact is placed. A second metal layer forms an ohmic contact with the semiconductor at the bottom of the structure (bulk contact).

A schematic energy band diagram for the different layers of a p-doped 4H-SiC MOS structure is shown in Fig. 2.2. As soon as the layers are connected, the balancing of the Fermi level causes a band bending (see Fig. 2.3 (b)). The strength of the bending depends on the difference in the work functions of the metal ϕ_M and the semiconductor ϕ_S.

Depending on the voltage on the top metal (from now on referred to as gate), one can distinguish three different bias regimes: accumulation, depletion and inversion. Fig. 2.3 shows the energy bands as a function of the voltage on the gate V_G for a nMOS capacitor. Starting at no electrical contact (a), the Fermi levels balance after forming a contact causing a band bending (b). By decreasing the gate voltage V_G, the amount of electrons at the SiC/oxide interface decreases. One can also describe this as an increase in hole density at the SiC/oxide interface. The Fermi level E_F comes close to the valence band E_V of the semiconductor. Therefore, the bias condition is called accumulation (c). By increasing the gate voltage, one will reach the flat band voltage V_FB. The flat band

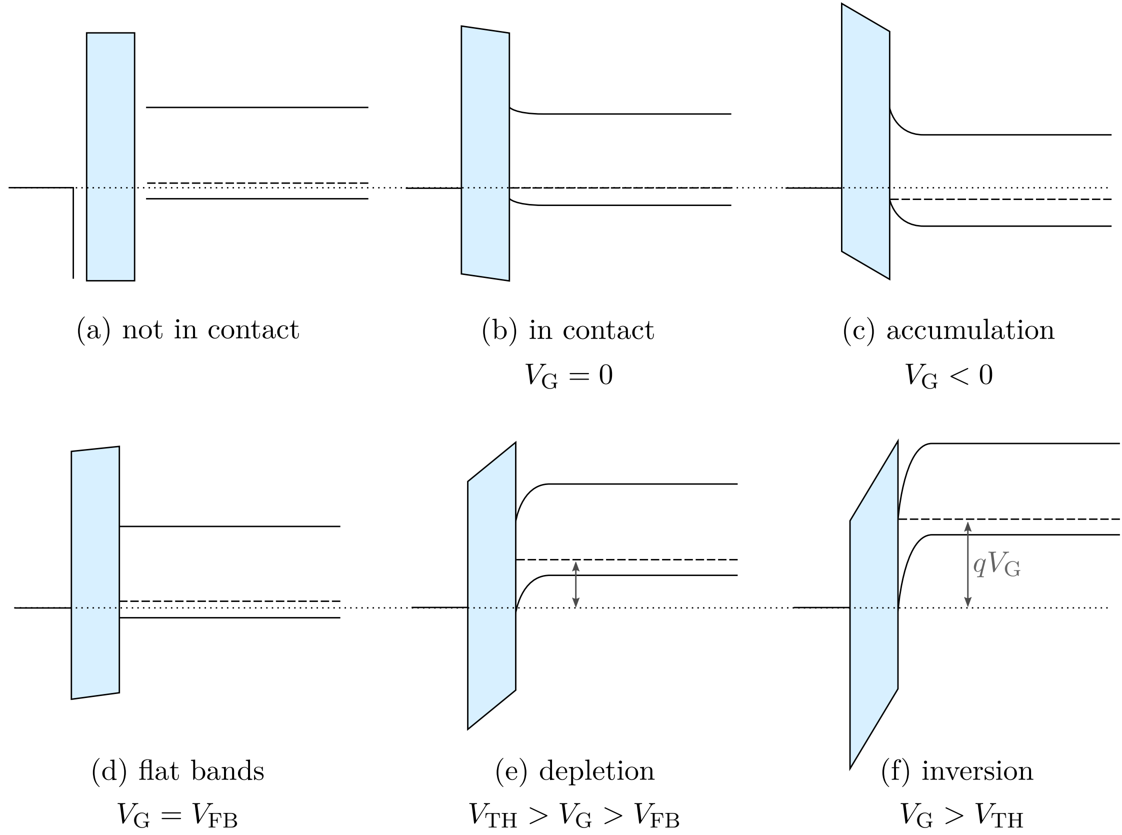


Figure 2.3.: The different bias conditions for a p-SiC MOS structure. (a) Layers not in contact. (b) The Fermi levels balance causing a band bending. (c) Negative bias causes an increase in hole density at the interface (accumulation). (d) By increasing the bias, the band bending disappears (Flat band voltage V_{FB}). (e) Further increasing of the bias leads to depletion of electrons at the interface. (f) If the bias voltage reaches the threshold voltage V_{TH}, a inversion layer forms.

voltage corresponds to the voltage which when applied to the gate electrode yields a flat energy band in the semiconductor (d). Further increase of the gate voltage will cause a further increase of the Fermi level in the semiconductor. As soon as the Fermi level exceeds the intrinsic Fermi level E_{Fi} (the middle of the band gap $E_{\mathrm{Fi}} \approx E_{\mathrm{V}} + E_{\mathrm{G}}/2$) the bias condition is called depletion due to the decrease in hole density at the interface (e). For a even higher gate voltage, the Fermi level of the semiconductor will come close to the the conduction band E_{C} of the semiconductor. If this happens, a conducting channel is formed at the interface. Electrons are accumulated at the interface. The bias condition is called inversion (f).

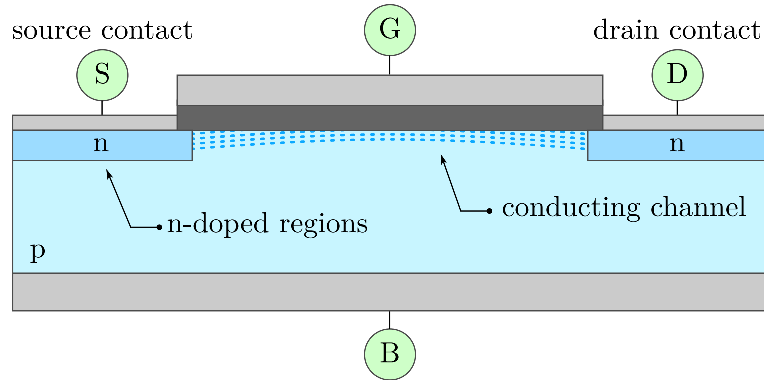


Figure 2.4.: The basic principle of a n-channel MOSFET. The MOS-structure is extended by two further contacts: source (S) and drain (D). Source and drain are connected to a highly n-doped region next to the oxide region. In inversion, a conductive layer forms at the interface (dotted area). This allows current to flow from one contact to another. Usually the bulk contact (B) is externally short circuited with the source contact.

2.2. The metal oxide semiconductor field effect transistor

The MOSFET is by far the most used transistor type in analog and digital circuits. The MOSFET is based on the MOS-structure. The basic idea is to control the magnitude of a electric current by a gate voltage V_{G} and the effect of the formation of a conductive layer. In principle, there are two ways to build a MOSFET depending on the doping of the bulk. A MOSFET with a p-doped bulk is called an nMOSFET or n-channel MOSFET because the conductive channel will be n-type. A MOSFET with a n-doped bulk is called a pMOSFET or p-channel MOSFET because the conductive channel will be p-type.

A sketch of an n-channel MOSFET is shown in Fig. 2.4. A pMOSFET is equivalent except for the opposite doping type, meaning n changes to p and vice versa. The MOS-structure is extended by a source and a drain contact. These two metals form a ohmic contact with the highly doped n-area beneath. The highly doped n area has to extend under the gate area region to ensure a conducting path over the hole gate length in inversion. In inversion, a conduction n-channel forms between the two highly doped n areas. If a voltage V_{DS} is applied between source and drain, a electric current I_{D} flows between drain and source.

The operation of a MOSFET can be separated into three different modes: cutoff, linear region and saturation region. The output characteristics of a MOSFET are shown in Fig.

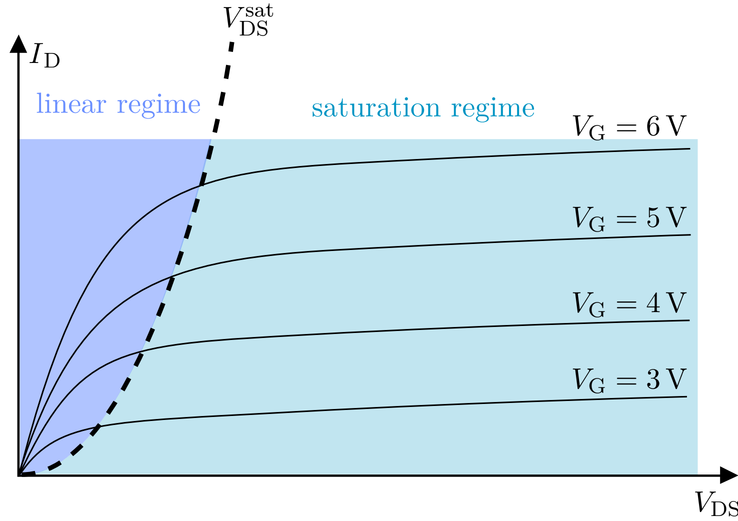


Figure 2.5.: Output characteristics of a MOSFET. If $V_{DS} < V_{DS}^{sat}$ the drain current increases nearly linear with gate voltage. If $V_{DS} \geq V_{DS}^{sat}$ the MOSFET becomes a gate-voltage controlled current source. The Early effect is now the only remaining impact of the source-drain voltage V_{DS} on the output current.

2.5. If the gate voltage V_G is lower than the threshold voltage V_{TH} no inversion layer will form. Therefore, no current can flow between drain and source ($I_D = 0\,A$). This mode is called cutoff, subthreshold or weak-inversion mode. In the linear region ($V_G > V_{TH}$ and $V_{DS} < V_{DS}^{sat}$) the current of the MOSFET is approximately given by

$$I_D = \frac{W}{L} \cdot C_{OX} \cdot \mu \cdot \left((V_G - V_{TH})V_{DS} - \frac{{V_{DS}}^2}{2} \right) \quad (2.4)$$

with the width of the channel W, the length of the channel L, the oxide capacitance C_{OX}, the mobility μ, the gate voltage V_G, the threshold voltage V_{TH} and the drain-source voltage V_{DS}.

If $V_G > V_{TH}$ and $V_{DS} \geq V_{DS}^{sat}$ the inversion layer forms but the channel narrows near the drain due to the high drain voltage V_{DS} (saturation). The drain current I_D in the saturation regime is approximately given by

$$I_{\mathrm{D}} = \frac{W}{L} \cdot C_{\mathrm{OX}} \cdot \mu \cdot \frac{(V_{\mathrm{G}} - V_{\mathrm{TH}})^2}{2}(1 + \lambda(V_{\mathrm{DS}} - V_{\mathrm{DS}}^{\mathrm{sat}})) \tag{2.5}$$

with the channel-length modulation parameter λ. λ models current dependence on drain voltage due to the Early effect which is the linear increase of drain current in saturation regime.

3

Defects

This section is based on the references [7, 13, 14]. Defects are the main reason for the limited electrical properties and the poor reliability of SiC devices. For MOSFETs one has to distinguish three defect areas (see Fig. 3.1): bulk defects, oxide defects and interface defects.

The most important area for the MOSFET is the active interface region where the conducting channel forms. Defects in this region are the main reason for undesirable properties like poor mobility or reliability. Large interfacial defect densities not only degrade the channel mobility by scattering and trapping of carriers. For n-channel devices an electron inversion layer is formed if the gate bias is large enough for the Fermi level to be close to the semiconductor conduction band edge. In this case, trap levels situating within the band gap are filled with electrons reducing the density of free carriers and yielding negatively charged centers. This leads to a reduced carrier lifetime and enhanced Coulomb scattering resulting in a low mobility. The poor quality of the SiC/SiO_2 interface has two origins: the relatively wide band gap and the presence of carbon [7].

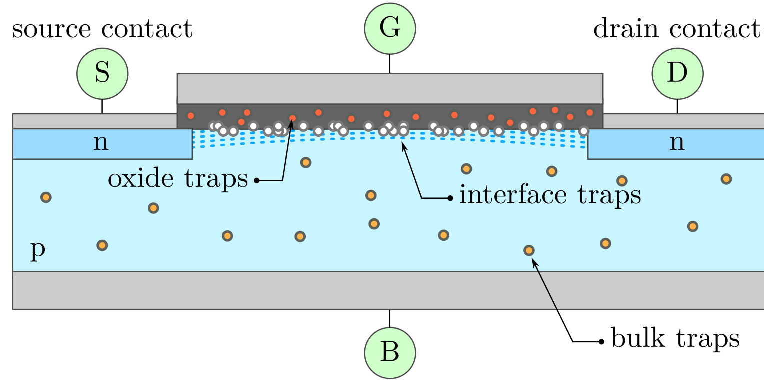


Figure 3.1.: Bulk, oxide and interface traps in a MOSFET.

According to [16], interface traps can be divided into two categories: acceptor-like traps and donor-like traps depending on their energetically position in the band gap. A sketch of these traps is given in Fig. 3.3. Acceptor-like trap states are located in the upper half of the band gap, whereas donor-like traps are located in the lower half of the band gap. Acceptor-like traps can either be neutrally or negatively charged. If the trap is neutral, it can become negatively charged by either electron capture or hole emission. If the acceptor-like trap is negatively charged, it can become neutral charged by either electron emission or hole capture. Donor-like traps can either be neutral or positive charged. If the donor-like trap is neutrally charged, it can become positive by either electron emission or hole capture and vice versa.

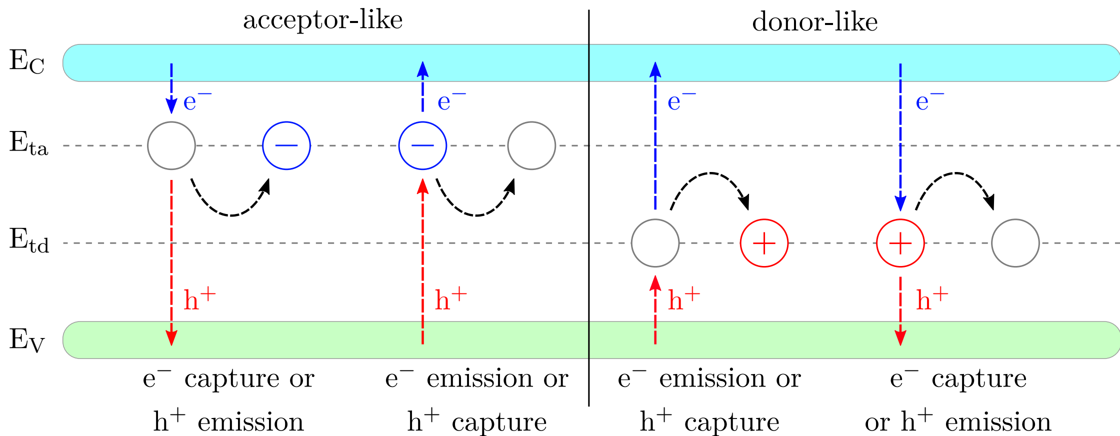


Figure 3.3.: Acceptor-like and donor-like trap states in their charging conditions.

In 4H-SiC-MOSFETs the density of interface states in the upper half of the band gap close to the conduction band edge E_C is most likely the reason for the poor electrical

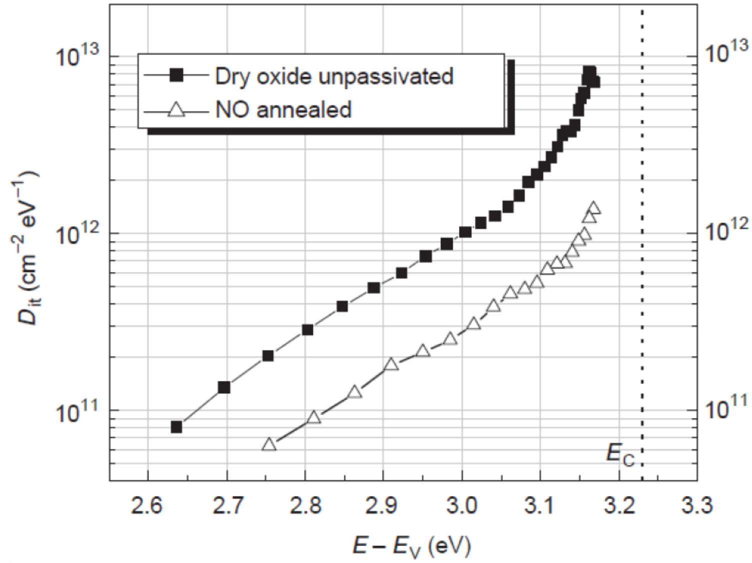


Figure 3.2.: Density of interface states D_{it} in unpassivated 4H-SiC and NO annealed 4H-SiC. The D_{it} increases exponentially near the conduction band edge E_C [15].

properties. Fig. 3.2 shows the density of interface states D_{it} in the upper part of the band gap of 4H-SiC. The D_{it} is exponentially increasing by about 2 orders of magnitude near the conduction band edge E_C. It is not entirely clear whether the interface states are intrinsic to the SiO_2/4H-SiC system or result from a non optimized thermal oxidation processes [17]. SiC polytypes with a narrower band gap like 3C-SiC ($E_G \approx 2.39\,\text{eV}$) or 6H-SiC ($E_G \approx 3.02\,\text{eV}$) show lower D_{it} values most probably because these states lie outside their band gap and are therefore electrically inactive. Consequently, the n-channel MOSFET mobility of unpassivated 6H-SiC devices ($\leq 100\,\text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$) is much higher than the mobility of unpassivated 4H-SiC devices ($\leq 10\,\text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$).

According to [14], the interfacial and near interfacial defects, that could contribute to the density of states within the band gap of 4H-SiC, are shown in Fig. 3.4. The first group of defects can be explained by carbon-clusters [18, 19]. The valence band of small clusters is located in the band gap of 4H-SiC and therefore creates donor-like states. However, the conduction band edge of small clusters lies well beyond the conduction band edge of 4H-SiC, resulting in no trap states near E_C. Large carbon clusters can produce acceptor-like states near E_C but are less likely to form compared to smaller carbon clusters [19]. The second group of defects might originate from inclusions of other polytypes like 3C in the 4H material due to localized polytype conversion during

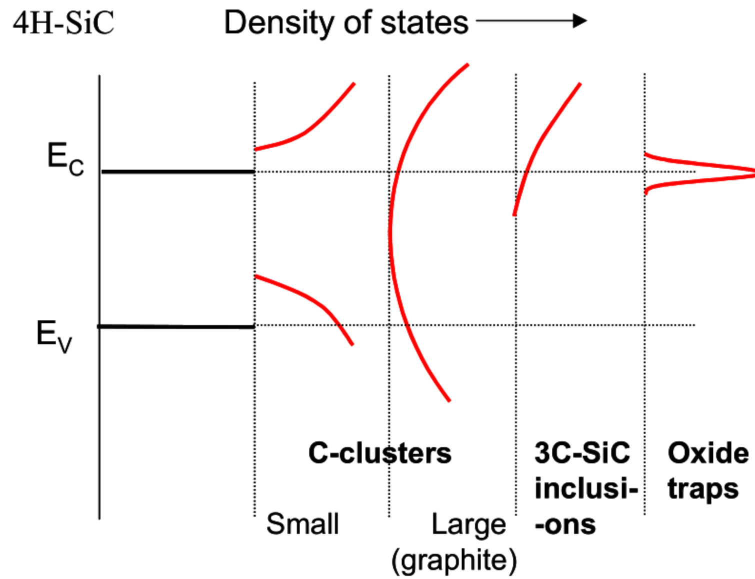


Figure 3.4.: Schematic of interfacial and near interfacial defects that could contribute to the density of states within the band gap of 4H-SiC [14].

oxidation [20]. The third and probably most severe group of defects originates from oxide traps. The high density of states located between the conduction band of 4H-SiC and 6H-SiC correspond to the levels previously observed at Si/SiO_2 interfaces. These states are located at 2.8 eV below the SiO_2 conduction band which is 0.1 eV below the 4H-SiC conduction band edge. They have a slow response time and a wide energy distribution [7] and are usually attributed to oxygen vacancies in the near-interfacial region. The measurements done in this work (see chapter 7) also support oxide traps to be the main reason for reliability issues after positive bias temperature stress (PBTS).

Still, 4H-SiC is the preferred SiC polytype for MOSFETs due to the high theoretical mobility and wide band gap. To reduce the high amount of defects, annealing is an important step in the manufacturing of modern MOSFETs. A review on nitrogen annealing can be found in the next chapter (4).

4

Nitrogen annealing

The following review of nitrogen annealing in silicon carbide is based on the references [2, 21, 22, 23, 24, 25]. The high amount of defects (see Sec. 3) at the SiC/SiO_2 interface and in the near interface oxide results in poor electrical properties. According to [2], MOSFETs fabricated using 4H-SiC exhibit channel mobilities about 100 times lower than the bulk value ($\mu_{max} \approx 950\,cm^2\,V^{-1}$ [3]) and about 10 times lower than other polytypes like 6H-SiC or 16R-SiC. One of the main reasons for this is the high D_{it} near E_C of 4H-SiC (see Sec. 3). It has been established that annealing in NO or N_2O provide significant improvements such as the reduction of interface trap density, increased channel carrier mobility and increased reliability (cf. Fig 4.1).

4.1. Nitridation model

Nitridation is involved in two sets of mechanisms at the SiC/SiO_2 interface: First, the creation of strong Si≡N bonds that passivate interface traps due to dangling and strained bonds. Second, the removal of carbon and complex silicon-oxycarbon (SiO_xC_y) bonds.

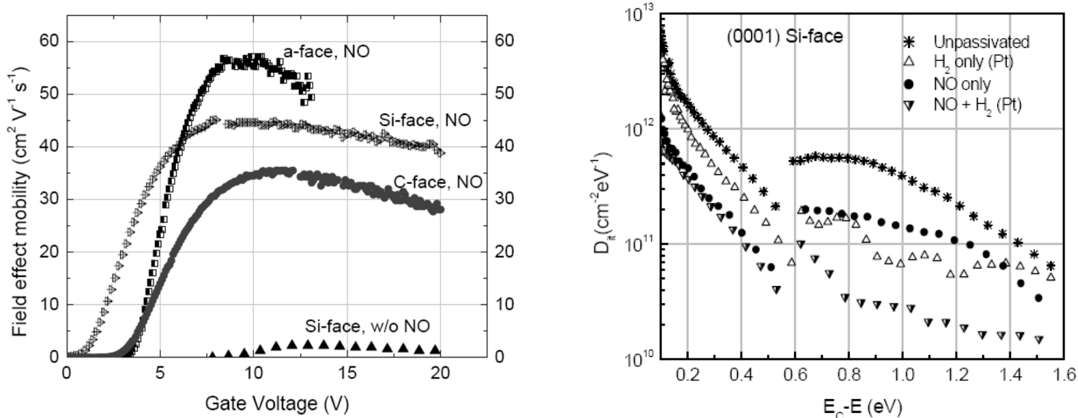


Figure 4.1.: Mobility (left) and density of interface traps (right) with and without NO POA [7].

The mechanisms leading to the formation of Si≡N bonds are already known from the Si/SiO_2 interface [26, 27]. Nitrogen binds to dangling Si bonds and replaces oxygen in strained Si-O bonds and forms strong Si≡N bonds. In SiC the nitridation reduces the initial interface trap density significantly. This does not happen for nitridation in silicon but is analogous to interface trap passivation with hydrogen in silicon. The hydrogen binds to dangling Si bonds and forms Si-H bonds. The hydrogen passivation shifts the trap energy levels to higher energies which lie outside the silicon band gap. This passivation is not effective in silicon carbide because of the much wider band gap. The hydrogen passivated trap energy levels are still located in the SiC band gap. The energy levels of the much stronger Si≡N bonds are outside the energy gap of SiC, meaning that they are electrically passive defects.

The second role of nitridation is the removal and passivation of carbon. Most of the carbon atoms released by oxidation of the SiC substrate react with the existing oxygen and create CO molecules that diffuse out of the oxide:

$$\mathrm{C} + \mathrm{O} \rightarrow \mathrm{CO} \tag{4.1}$$

Some of the carbon remains at or near the interface, either as isolated atoms or in the form of carbon clusters. Nitridation not only passivates the carbon related interface traps by the formation of electrically inactive C-N bonds. More importantly the nitridation

removes interstitial carbon as well as carbon from already formed carbon clusters. As a result, nitrided SiC/SiO_2 interfaces show a reduced number of Si oxycarbon bonds. An example for the impact of NO annealing on the device mobility and the density of interface states is given in figure 4.1.

4.2. Nitrous oxide (N_2O) and nitric oxide (NO) passivation

Annealing is mostly done in NO or N_2O atmospheres. Devices with thermally grown oxides annealed in NO or N_2O usually feature an increased mobility [28, 29, 30] and increased reliability [31, 32]. This is due to the reduction of the interface trap density [33, 14, 34]. The quality of the anneal is highly dependent on the annealing parameters like gas composition, temperature, pressure and time. Devices annealed in NO show better electrical properties than devices annealed in N_2O. However, NO gas is highly toxic which makes high demands on processing and safety. N_2O, in turn, is less harmful and is therefore the preferably used gas. By further optimizing of the POA parameters, the N_2O anneal might lead to equally good electrical properties as the NO anneal as shown by [22].

For NO and N_2O, the nitridation only happens at the SiC/SiO_2 interface. The amount of incorporated nitrogen at the interface is about the same for both annealing techniques. X-ray photoelectron spectroscopy (XPS) analyses done by [21] reveal dramatic differences between argon annealed and nitrided oxides. Existence of suboxides and complex oxide-carbon compounds at the interface of argon (Ar)- annealed oxides is shown. In the case of nitrided oxides the complex suboxides and oxide-carbon bonds are removed. Strong $Si{\equiv}N$ bonds are created and the intensity of C-C bonds is significantly reduced. At least in the XPS spectra, no difference between NO and N_2O is shown (cf. Fig. 4.2). This means that the chemical reactions responsible for the significant improvement of the interface quality achieved by NO annealing also take place during N_2O annealing.

The reason for this is the dissociation of N_2O into N_2, NO and O_2 during postoxidation:

$$4N_2O \rightarrow 2NO + O_2 + 3N_2 \tag{4.2}$$

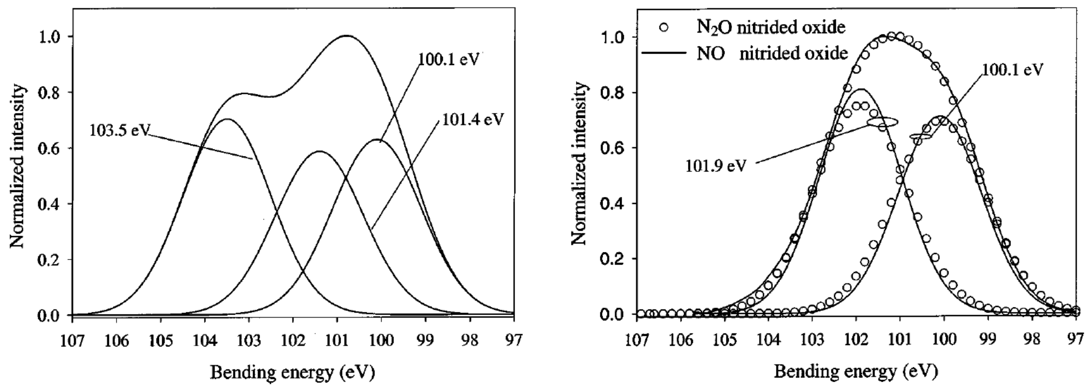


Figure 4.2.: XPS spectra of the interface composition of argon annealed (left) and NO or N_2O annealed oxides (right). The binding energies correspond to Si-C (100.1 eV), Si-O_xC_y (101.4 eV), Si-O_x (103.5 eV) and Si-O_xN_y (101.9 eV). The Si-O_xC_y bonds are completely removed by the nitridation and less harmful Si-O_xN_y bonds are formed [21].

The NO component will cause the same chemical effects that occur in pure NO oxidation, while the O_2 component will cause further oxidation. At high temperatures also NO decomposes in:

$$2NO \rightarrow N_2 + O_2 \tag{4.3}$$

At these temperatures, N_2 is inserted but the O_2 removes the nitrogen and increases the oxide thickness. This removal of nitrogen during NO POA does not happen in the case of Si/SiO_2. In Si/SiO_2 the existence of O_2 also causes different depth profiles of nitrogen at the N_2O and NO nitrided Si/SiO_2 interfaces. Figure 4.3 shows the secondary ion mass spectrometry (SIMS) profile of N_2O and NO annealed samples according to the XPS measurements done by [21]. There is no big difference in the peak position or intensities for the NO and N_2O annealed samples, which is clearly a difference to Si/SiO_2 case. Therefore, the rate of nitridation relative to the rate of oxidation must be much higher in the case of SiC.

The nitrogen peak (cf. Fig 4.3) follows the interface if the oxide grows. The maximum value of incorporated nitrogen saturates at a certain value depending on POA parameters as shown in figure 4.4. In a nutshell, the NO reacts with silicon and carbon at the interface to incorporate nitrogen. O_2 produced by the thermal decomposition of NO

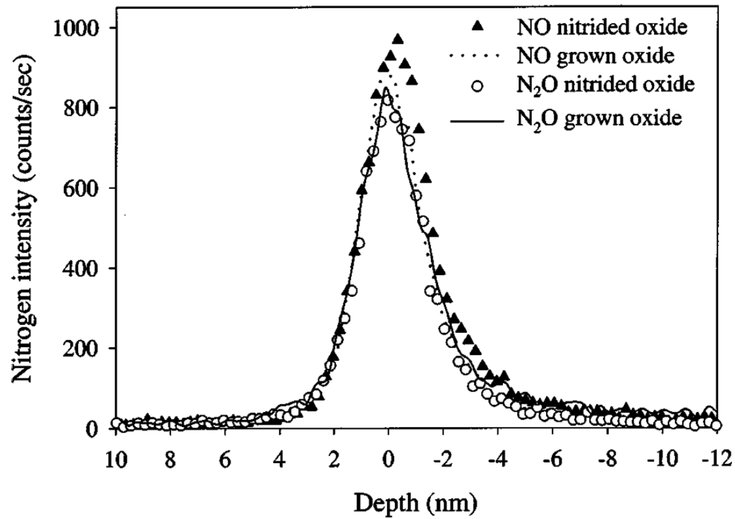


Figure 4.3.: SIMS profiles for NO and N_2O annealed and grown samples. Both techniques show about the same peak. NO POA leads to a slightly higher nitrogen density. Unlike in silicon, the existence of oxygen does not lead to a different depth profile in SiC [21].

oxidizes the substrate and removes nitrogen from the interface. Initially, the nitridation reaction is faster than oxidation and results in an increase in nitrogen content. After a temperature-dependent time, the nitridation and oxidation reactions begin to equalize, and the nitrogen content decreases. When the two reactions reach equilibrium, the nitrogen incorporated by nitridation is balanced by the removed nitrogen [2].

According to [23], NO and N_2O annealing is reducing fast states (π bonded C) and decreasing the D_{it} over the whole energy gap. But only NO is effective in removing slow states (oxide or near- interface states). Annealing in NH_3 might lead to a further reduction of these slow states.

4.3. Ammonia (NH_3) passivation

To eliminate the problem of further oxidation during post oxidation anneal, POA in atmospheres that do not contain oxidizing species are helpful. For this purpose NH_3 POA was used in recent studies [24, 35, 36]. The impact of NH_3 POA on the D_{it} and the mobility is shown in figure 4.5. Like NO POA, also NH_3 reduces the D_{it} and increases the mobility. Figure 4.5 (right) compares a SIMS profile for N_2O and NH_3 annealed

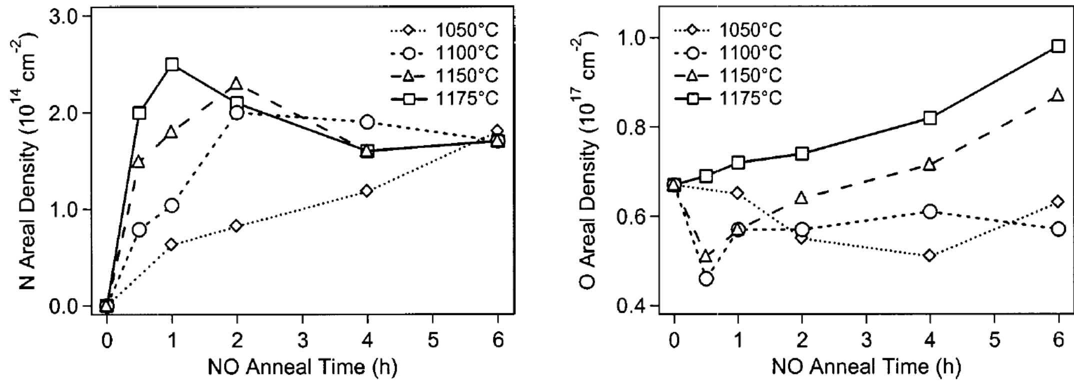


Figure 4.4.: Nitrogen content (left) measured by nuclear reaction analysis (NRA) and oxygen content (right) measured by Rutherford backscattering spectrometry (RBS) at the interface for different NO POA parameters [2].

oxides. The main difference is the nitrogen incorporation in the oxide, which does not happen for NO or N_2O POA.

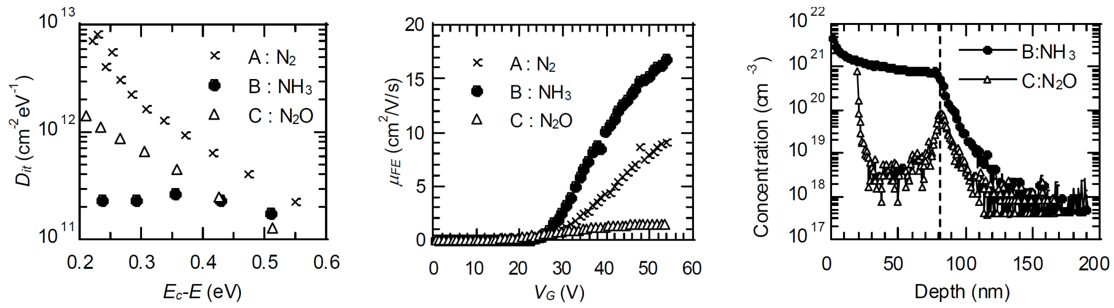


Figure 4.5.: Density of interface states (left) and mobility (middle) for three different POA conditions including NH_3 POA. SIMS profiles for NH_3 and N_2O annealed samples (right). In contrast to N_2O and NO (cf. figure 4.3), the nitrogen incorporation during NH_3 annealing is not limited to the interface and occurs throughout the oxide [24].

Annealing SiO_2 in NH_3 incorporates large amounts of nitrogen. The interfacial nitrogen concentration is about 10 times higher than in NO annealed oxides [24]. Furthermore NH_3 POA removes oxygen, which significantly changes the oxide stoichiometry, increases the dielectric constant and decreases the breakdown field [2].

4.4. Summary

Today annealing with NO or N_2O is an important step to achieve devices with good electrical properties. However, there are still a lot of questions remaining on the exact mechanics of the annealing process. The exact impact of the POA depends on multiple parameters like the POA temperature, POA time, gas composition and of course all additional interface characteristics of the device itself (e.g. oxide grow techniques and crystal faces). Therefore further optimizing of the POA process is one of the most important steps to produce improved devices in the future.

One topic in this thesis is the impact of the NO-POA temperature and NO-POA time on bias temperature instability (BTI) and R_{on}. The results are shown in chapter 7.

Part II.

CHARACTERIZATION AND STRESS TECHNIQUES

5

MOSFET characterization techniques

5.1. Output characteristics

The easiest way to analyze a MOSFET is by having a look at the output characteristics. The drain current I_{D} in the linear regime is approximately given by the equation

$$I_{\mathrm{D}} = \frac{W}{L} \cdot C_{\mathrm{OX}} \cdot \mu \cdot \left((V_{\mathrm{G}} - V_{\mathrm{TH}})V_{\mathrm{DS}} - \frac{{V_{\mathrm{DS}}}^2}{2} \right) \tag{5.1}$$

and in the saturation regime by the equation

$$I_{\mathrm{D}} = \frac{W}{L} \cdot C_{\mathrm{OX}} \cdot \mu \cdot \frac{(V_{\mathrm{G}} - V_{\mathrm{TH}})^2}{2} (1 + \lambda(V_{\mathrm{DS}} - V_{\mathrm{DS}}^{\mathrm{sat}})) \tag{5.2}$$

with the width of the channel W, the length of the channel L, the oxide capacitance C_{OX}, the mobility μ, the gate voltage V_{G}, the threshold voltage V_{TH}, the channel-length modulation parameter λ and the drain-source voltage V_{DS} (see section 2.2). The channel width W and channel length L are known from the MOSFET layout. V_{DS} and V_{G} are given

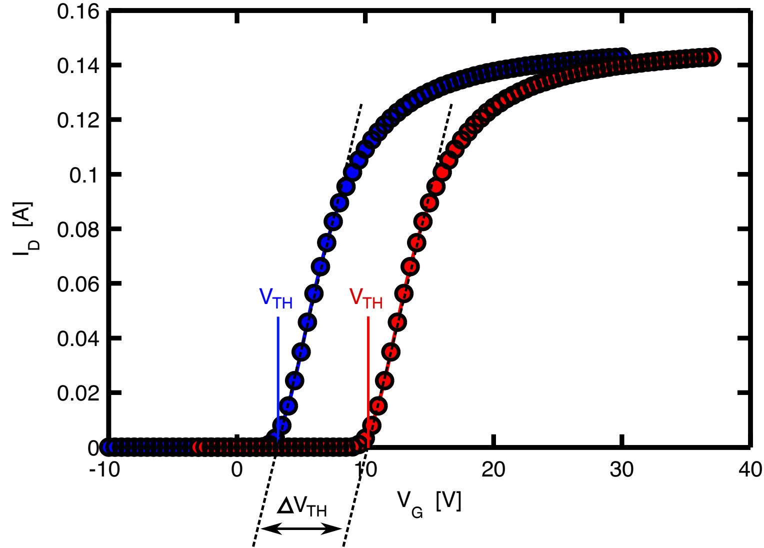


Figure 5.1.: Extraction of the threshold voltage shift via ELR method (see 5.1.1)

by the experiment and the oxide capacitance C_{OX} can be obtained by capacitance-voltage (CV) measurements (see section 5.2).

For the extraction of the important MOSFET parameters, like the threshold voltage V_{TH} or the electron mobility μ, multiple methods have been developed [37]. In the next two sections a short overview is given about how the extraction of the threshold voltage and the mobility is done in this thesis to determine the impact of the nitric oxide post oxidation anneal on the device parameters.

5.1.1. Extraction of the threshold voltage

The threshold voltage value is the most important electrical parameter in modeling MOSFETs. However, there are a lot of different techniques for the extraction of the threshold voltage. A review of eleven different MOSFET threshold voltage extraction methods were done by Ortiz-Conde et al. in 2002 [38]. The extrapolation in the linear regime (ELR) method is perhaps the most popular threshold voltage extraction method. It consists of finding the gate-voltage axis intercept of the linear extrapolation of the I_{D}-V_{G} curve at its maximum first derivative point. The method is sketched in Fig. 5.1 for two different I_{D}-V_{G} curves. The main drawback of this method is that the maximum slope point might be uncertain, because the I_{D}-V_{G} characteristics can deviate from ideal straight line behavior at gate voltages even slightly above the threshold voltage, due

to mobility degradation effects and due to parasitic source and drain series resistances. Therefore, the threshold voltage value extracted using this method, often referred to as the extrapolated V_{TH}, can be strongly influenced by parasitic series resistances and mobility degradation effects [38].

For the work in this thesis, we are mainly interested in the threshold voltage shift ΔV_{th} after a certain stress procedure. An example is given in Fig. 5.1. The blue curve corresponds to the unstressed device while the red curve corresponds to a stressed device. If the slope of the I_{D}-V_{G} curve after the stress do not change (meaning the stress does not change the mobility), the determination of the threshold voltage shift is rather straightforward. This behavior was observed for the BTI stress (see section 6.1). In this case, the curves are shifted in a parallel manner which allows for using a constant current criterion.

5.1.2. Mobility extraction method of Ghibaudo

For the work in this thesis, the method of G. Ghibaudo [39] has been chosen because it allows a simple and independent determination of the threshold voltage V_{TH} and the low field mobility μ_0 in the linear region. It is based on the combined exploitation of the drain current ($I_{\mathrm{D}}/V_{\mathrm{G}}$) and transconductance ($g_m/V_{\mathrm{G}}$) characteristics. Note that the threshold voltage V_{TH} obtained by the method of Ghibaudo is considerably higher than the threshold voltage obtained by other methods [38]. For this reason, the V_{TH} obtained by the method of Ghibaudo is flagged by a superscript G ($V_{\mathrm{TH}}^{\mathrm{G}}$).

The drain current I_{D} of a MOSFET is given by

$$I_{\mathrm{D}} = \frac{W}{L} \cdot C_{\mathrm{OX}} \cdot \frac{\mu_0}{1+\theta(V_{\mathrm{G}} - V_{\mathrm{TH}}^{\mathrm{G}})}(V_{\mathrm{G}} - V_{\mathrm{TH}}^{\mathrm{G}}) \cdot V_{\mathrm{DS}} \tag{5.3}$$

with the channel length L, the channel width W, the gate capacitance C_{OX}, the low field mobility μ_0, the mobility reduction factor θ, the gate voltage V_{G} and the drain-source voltage V_{DS}. The Term

$$\frac{\mu_0}{1+\theta(V_{\mathrm{G}} - V_{\mathrm{TH}}^{\mathrm{G}})} = \mu_{\mathrm{EFF}} \tag{5.4}$$

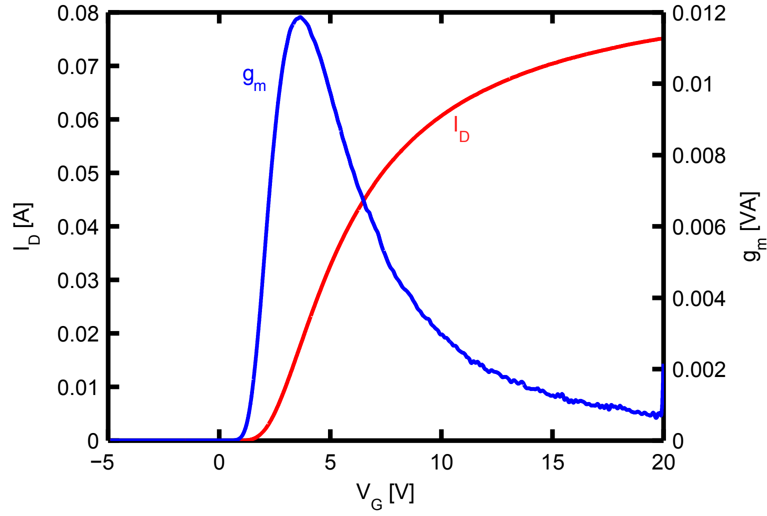


Figure 5.2.: Drain current (red) and transconductance (blue) of an n-channel MOSFET in the linear region ($V_{\mathrm{DS}} \approx 0.1\,\mathrm{V}$).

is called effective mobility μ_{EFF} and describes a mobility reduction with gate voltage V_{G}. Differentiating the drain current with respect to V_{G} (Eq.5.3) yields the transconductance

$$g_m = \frac{W}{L} \cdot C_{\mathrm{OX}} \cdot \frac{\mu_0}{[1+\theta(V_{\mathrm{G}} - V_{\mathrm{TH}}^{\mathrm{G}})]^2} \cdot V_{\mathrm{DS}}. \tag{5.5}$$

A typical plot for drain current and the transconductance is shown in Fig. 5.2.

To get rid of the mobility reduction factor θ we divide the expression for the drain current (Eq. 5.3) by the square root of the transconductance (Eq. 5.5), which yields to

$$\frac{I_{\mathrm{D}}}{\sqrt{g_m}} = \sqrt{\frac{W}{L} C_{\mathrm{OX}} \mu_0 V_{\mathrm{DS}}} \cdot (V_{\mathrm{G}} - V_{\mathrm{TH}}^{\mathrm{G}}). \tag{5.6}$$

One can bring this into the form of a linear equation

$$y = K \cdot x + K \cdot D \tag{5.7}$$

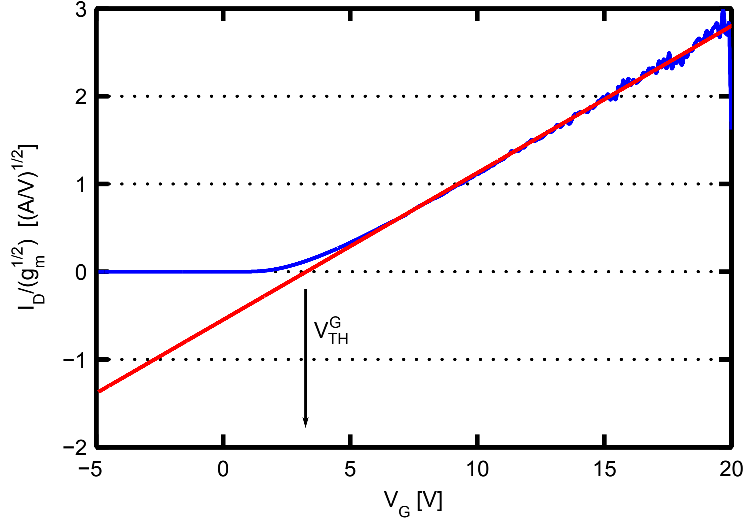


Figure 5.3.: Drain current I_D divided by the square root of the transconductance g_m (blue) and linear fit (red) in strong inversion and linear region to extract the MOSFET parameters.

which leads to

$$\frac{I_\mathrm{D}}{\sqrt{g_m}} = \sqrt{\frac{W}{L} C_\mathrm{OX} \mu_0 V_\mathrm{DS}} \cdot V_\mathrm{G} - \sqrt{\frac{W}{L} C_\mathrm{OX} \mu_0 V_\mathrm{DS}} \cdot V_\mathrm{TH}^\mathrm{G}. \tag{5.8}$$

Thus, it is possible to determine the parameters V_TH^G and μ_0 by fitting the $I_\mathrm{D}/\sqrt{g_m}$ characteristics at high gate voltages (strong inversion) with a first order polynomial (see Fig. 5.3). Hence the value of V_TH^G is not needed a priori to deduce the value of μ_0 or vice versa. Out of the fit parameters K and D (Eq. 5.7) the threshold voltage V_TH^G and the mobility μ_0 is given by

$$V_\mathrm{TH}^\mathrm{G} = -D \tag{5.9}$$

$$\mu_0 = \frac{K^2 L}{W C_\mathrm{OX} V_\mathrm{DS}}. \tag{5.10}$$

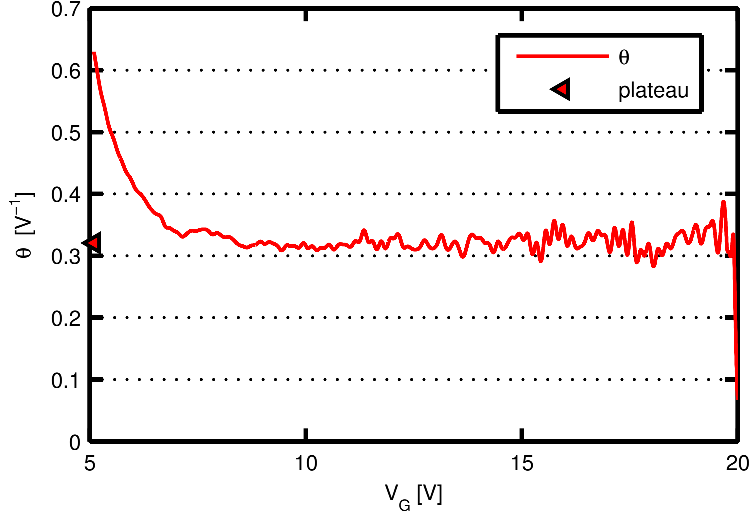


Figure 5.4.: Mobility reduction factor θ as a function of gate voltage V_{G}. In strong inversion, a plateau occurs for the mobility reduction factor θ. This plateau value is used for the calculation of the effective mobility μ_{EFF}.

Knowing the threshold voltage $V_{\mathrm{TH}}^{\mathrm{G}}$ it is now possible to determine the mobility reduction factor

$$\theta = \left(\frac{I_{\mathrm{D}}}{g_m (V_{\mathrm{G}} - V_{\mathrm{TH}}^{\mathrm{G}})} - 1 \right) \frac{1}{V_{\mathrm{G}} - V_{\mathrm{TH}}^{\mathrm{G}}}. \tag{5.11}$$

The mobility reduction factor includes the effects of the source-drain series resistances R_{SD} and is given by

$$\theta = \theta_0 + R_{SD} C_{\mathrm{OX}} \mu_0 \frac{W}{L} \tag{5.12}$$

with the intrinsic mobility reduction factor θ_0. Knowing θ further leads to the effective mobility μ_{EFF} (see Fig. 5.5)

$$\mu_{\mathrm{EFF}} = \frac{\mu_0}{1 + \theta (V_{\mathrm{G}} - V_{\mathrm{TH}}^{\mathrm{G}})}. \tag{5.13}$$

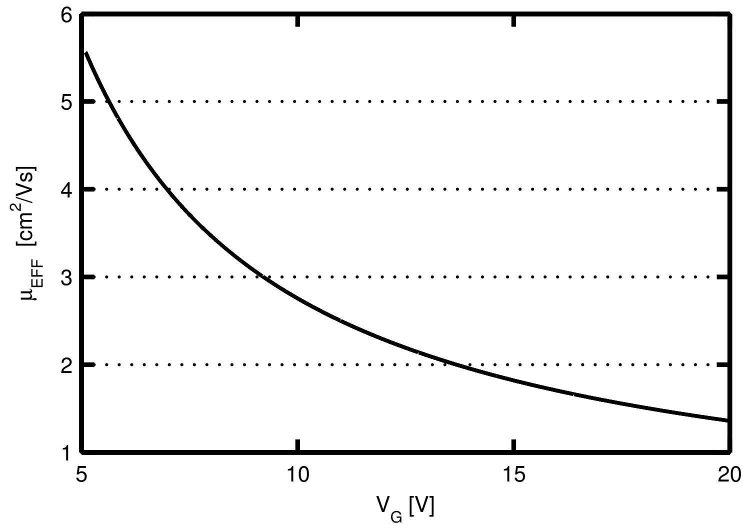


Figure 5.5.: Effective mobility μ_{EFF} as a function of gate voltage V_{G} in strong inversion and linear region.

With the effective mobility μ_{EFF} and the threshold voltage $V_{\mathrm{TH}}^{\mathrm{G}}$ one now has a good model for the drain current as a function of the the gate voltage in strong inversion with the formula

$$I_{\mathrm{D}} = \frac{W}{L} \cdot C_{\mathrm{OX}} \cdot \mu_{\mathrm{EFF}} \cdot (V_{\mathrm{G}} - V_{\mathrm{TH}}^{\mathrm{G}}) \cdot V_{\mathrm{DS}}. \tag{5.14}$$

Fig. 5.6 shows the result of the calculation for the drain current as a function of gate voltage in strong inversion and low drain voltage (linear region).

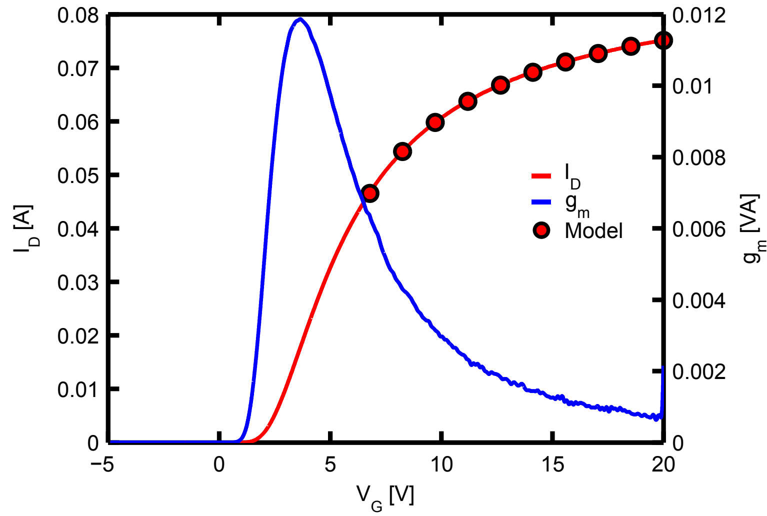


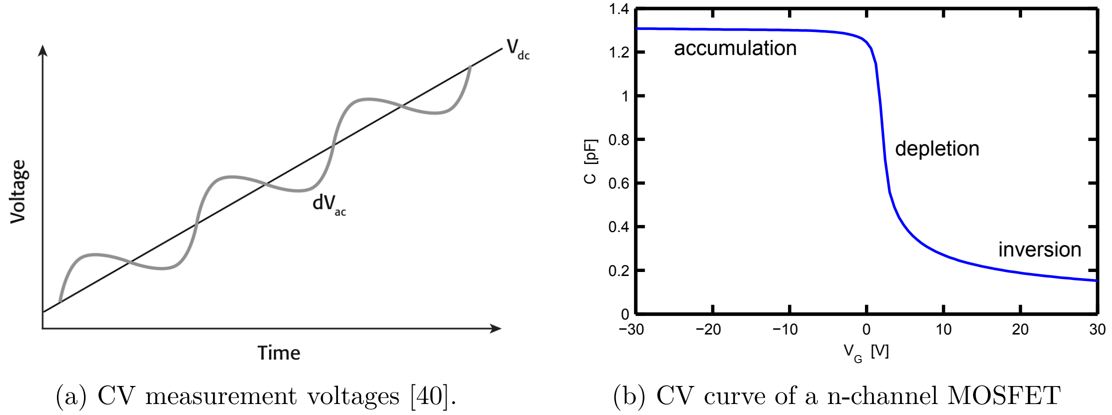
Figure 5.6.: Calculated drain current (red circles) as a function of gate voltage in strong inversion and linear regime ($V_{\mathrm{DS}} \approx 0.1\,\mathrm{V}$).

5.2. Capacitance-voltage profiling

Capacitance-voltage (CV) testing is widely used to determine semiconductor parameters in MOSCAP and MOSFET structures like the oxide capacitance, the oxide thickness, flatband capacitance, flatband voltage, threshold voltage, metal-semiconductor work function difference, effective and total bulk oxide charge and doping concentrations. However, in this thesis CV measurements where mainly used to determine the oxide capacitance C_{OX}. Capacitance is the change in charge q per change in voltage V

$$C = \frac{\Delta q}{\Delta V}. \tag{5.15}$$

CV measurements in a semiconductor a made using two voltage sources shown in Fig. 5.7a. An AC voltage with fixed frequency and amplitude and a DC voltage with swept in time amplitude. The magnitude and frequency of the AC voltage are fixed. The magnitude of the DC voltage is swept in time. The purpose of the DC voltage bias is to allow sampling of the material at different depths in the device. The AC voltage bias provides the small signal bias so the capacitance measurement can be performed at a given depth in the device [40]. A typical high-frequency CV curve of a n-channel



(a) CV measurement voltages [40].

(b) CV curve of a n-channel MOSFET

Figure 5.7.: AC and DC voltage of a CV measurement [40] (a) and typical CV curve of a n-channel MOSFET (b).

MOSFET is shown in Fig. 5.7b. The three modes of operation, accumulation, depletion and inversion, are well defined in the curve.

For a n-channel MOSFET, the oxide capacitance C_{OX} is obtained in the strong accumulation region. This is where the voltage is negative enough that the capacitance is essentially constant and the CV curve is almost flat. The oxide thickness can also be extracted from the oxide capacitance. Note that for very thin oxides the slope of the CV curve does not flatten and the measured oxide capacitance differs from the actual oxide capacitance. However this is not the case for the power MOSFETs measured in this thesis due to their very thick oxide ($d_{\mathrm{OX}} \approx 70\,\mathrm{nm}$). In strong accumulation, the MOSFET gate capacitance acts like a parallel plate capacitor. The oxide thickness is then given by the simple equation

$$d_{\mathrm{OX}} = \frac{A_{\mathrm{G}}}{C_{\mathrm{OX}}} \varepsilon_{\mathrm{SiO_2}} \tag{5.16}$$

with the gate area A_{G} and the permittivity of the oxide $\varepsilon_{\mathrm{SiO_2}}$.

5.3. Charge pumping

The following review on charge pumping is a based on the references [13, 41, 42].

5.3.1. Motivation

Charge pumping (CP) is a important and reliable technique for the characterization of interface traps in MOSFETs. The technique was first described by Brugler and Jespers in 1969 [43]. Interface traps are of high interest because they are located in the region where the channel of the MOSFET forms. Charged traps act as scattering centers and reduce the mobility. Therefore, interface traps affect the electrical properties of the devices. Nowadays, CP is used in semiconductor industry as standard characterization tool for monitoring process stability and device reliability.

5.3.2. Fundamentals

The method is based on the interaction between free carriers of the semiconductor valence and conduction bands with trap states at the semiconductor-dielectric interface. The main idea is the detection of interface traps due to their capability to keep carriers for a certain amount of time. The following discharge of the trap leads to a detectable current. The measurement itself is done by high frequency pulsing the gate between accumulation and inversion while source and drain is grounded. Figure 5.8 shows the basic principle of CP for an n-channel MOSFET. A high gate voltage leads to inversion causing a negative charging of traps by electrons. Afterwards the gate bias is switched back to accumulation. Non-captured channel electrons flow back to drain/source. Accumulated holes recombine with the trapped electrons causing an detectable charge pumping current I_{CP} at the bulk.

The resulting substrate current is proportional to the number of trapping centers at the semiconductor-dielectric interface. The maximum charge pumping current $I_{\mathrm{CP}}^{\mathrm{max}}$ can be calculated as

$$I_{\mathrm{CP}}^{\mathrm{max}} = A_{\mathrm{G}} f q N_{\mathrm{CP}} \tag{5.17}$$

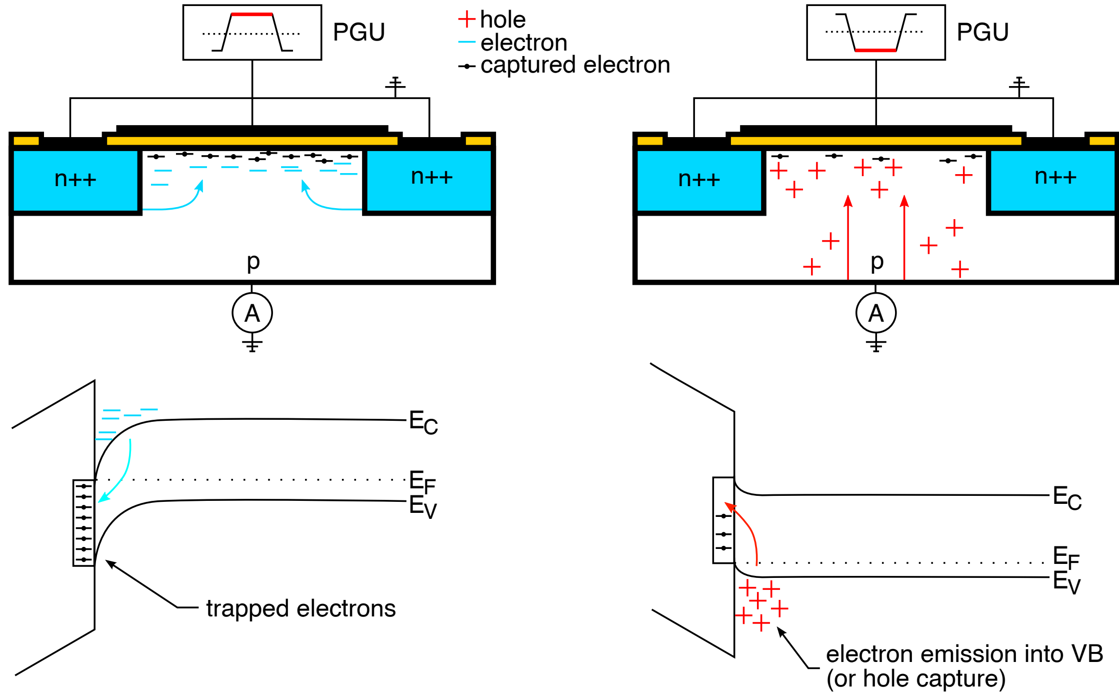


Figure 5.8.: Basic principle of charge pumping for a n-channel MOSFET. During the high level of the gate pulse, inversion leads to a trapping of carriers at the interface (left). During the low level of the pulse the trapped (stored in interface states) carriers become re-emitted causing a detectable charge pumping current at the bulk. [41]

where A_{G} is the effective gate area, f the frequency of the gate pulse, q the electronic charge and N_{CP} the number of pumped charges per unit area.

The average density of interface states D_{it} is given by

$$\overline{D_{\mathrm{it}}} = \frac{N_{\mathrm{CP}}}{\Delta E_{\mathrm{CP}}} \tag{5.18}$$

for a certain active charge pumping window ΔE_{CP}. The value of ΔE_{CP} depends on several parameters like the rise/fall time of the gate pulse, the temperature and of course the material parameters. The exact value of ΔE_{CP} can be deduced from Shockley-Read-Hall (SRH) theory from capture and emission time constants [44]. Using equation 5.17 and equation 5.18 one can write the average D_{it} as a function of ΔE_{CP} as

$$\overline{D_{\mathrm{it}}} = \frac{I_{\mathrm{CP}}^{\max}}{A_{\mathrm{G}} f \Delta E_{\mathrm{CP}}}. \tag{5.19}$$

If the slope of the gate pulse is too steep or the channel of the devices is too long, a geometric charge pumping current $I_{\mathrm{CP}}^{\mathrm{geo}}$ may superimpose the real I_{CP}. The $I_{\mathrm{CP}}^{\mathrm{geo}}$ is due to carriers which do not leave the channel area fast enough during the transition of the gate pulse. One can effectively avoid this effect by using devices with short channels, less steep gate pulses or applying a slight reverse bias to the source-drain pn-junction to evacuate the channel more efficiently and simultaneously decrease the channel width by increasing the space-charge-regions of the junction. G. Van den Bosch [45] published a simple method to determine the presence of any geometric component. For short channel devices and less steep gate pulses, the $I_{\mathrm{CP}}^{\mathrm{geo}}$ is negligible in most cases.

Trap emission and trap capture

CP relies on the finite emission and capture time of carriers into traps. In SRH theory, the transition probability between a trap and the semiconductor valence and conduction bands is described by means of the transition time constants τ. Meaning a transition occurs with a probability of $(1 - 1/e) \approx 63\%$ until the time τ. In general, one has to distinguish between electron and hole capture or emission. In SRH theory the time constant for electron capture τ_{cn} is approximately given as

$$\tau_{\mathrm{cn}} = \frac{1}{\nu_{\mathrm{thn}} \sigma_{\mathrm{n}} n_{\mathrm{s}}} \approx \frac{1}{\nu_{\mathrm{thn}} \sigma_{\mathrm{n}} N_{\mathrm{C}}} \cdot \exp\left(\frac{E_{\mathrm{C}} - E_{\mathrm{Fn}}}{k_{\mathrm{B}} T}\right) \tag{5.20}$$

and for hole capture as

$$\tau_{\mathrm{cp}} = \frac{1}{\nu_{\mathrm{thp}} \sigma_{\mathrm{p}} p_{\mathrm{s}}} \approx \frac{1}{\nu_{\mathrm{thp}} \sigma_{\mathrm{p}} N_{\mathrm{V}}} \cdot \exp\left(\frac{E_{\mathrm{Fp}} - E_{\mathrm{V}}}{k_{\mathrm{B}} T}\right) \tag{5.21}$$

with the concentration of free holes p_{s} and electrons n_{s}, the effective density of states in the conduction N_{C} and valence band N_{V}, the quasi Fermi levels for electrons E_{Fn} and holes E_{Fp} at the interface, the capture cross section for electrons σ_{n} and holes σ_{p} and the thermal velocity of electrons ν_{thn} and holes ν_{thp}.

The counterpart to the capture process is the emission process. It is understood as a transition from a lower to a higher energy state. If an electron is emitted from a defect state into the conduction band it is called electron emission. If a hole is emitted from a defect state into the valence band, it is called hole emission. The emission time constants for holes τ_{ep} and electrons τ_{en} can be approximated as

$$\tau_{\mathrm{en}} = \frac{1}{\nu_{\mathrm{thn}}\sigma_{\mathrm{n}}n} \approx \frac{1}{\nu_{\mathrm{thn}}\sigma_{\mathrm{n}}N_{\mathrm{C}}} \cdot \exp\left(\frac{E_{\mathrm{C}} - E_{\mathrm{t}}}{k_{\mathrm{B}}T}\right) \tag{5.22}$$

and

$$\tau_{\mathrm{ep}} = \frac{1}{\nu_{\mathrm{thp}}\sigma_{\mathrm{p}}p} \approx \frac{1}{\nu_{\mathrm{thp}}\sigma_{\mathrm{p}}N_{\mathrm{V}}} \cdot \exp\left(\frac{E_{\mathrm{t}} - E_{\mathrm{V}}}{k_{\mathrm{B}}T}\right) \tag{5.23}$$

with the free electron density in the conduction band n and the free hole density in the valence band p when the energy of the Fermi-level is equal to the energy of the trap ($E_{\mathrm{F}} = E_{\mathrm{t}}$).

CP threshold and flat band voltage

Figure 5.9 shows the typical pulse setup for a CP measurement. According to equations 5.20 and 5.21, the capture time constants are exponentially dependent on the energy difference between the band edges and the Fermi level. Therefore, the capture and emission time depend strongly on the pulse low V_{GL} and high levels V_{GH}. The minimum time required to fill all trap levels below E_{Fn} during the high level duration of the gate pulse t_{H} is approximately τ_{cn}. The minimum time required to empty all trap levels above E_{Fp} during the low level duration of the gate pulse t_{L} is approximately τ_{cp}. This means there is a critical upper Fermi level position $E_{\mathrm{Fn}}^{\mathrm{crit}}$ defined by V_{GH} and a critical lower Fermi level position $E_{\mathrm{Fp}}^{\mathrm{crit}}$ defined by V_{GL} which must be exceeded to ensure complete filling or emptying. This critical levels can be calculated using equations 5.20 and 5.21 by setting $\tau_{\mathrm{cp}} \approx t_{\mathrm{L}}$ and $\tau_{\mathrm{cn}} \approx t_{\mathrm{H}}$:

$$E_{\mathrm{Fn}}^{\mathrm{crit}} \approx E_{\mathrm{C}} - k_{\mathrm{B}}T \cdot \ln\left(\nu_{\mathrm{thn}}\sigma_{\mathrm{n}}N_{\mathrm{C}}t_{\mathrm{H}}\right) \tag{5.24}$$

$$E_{\mathrm{Fp}}^{\mathrm{crit}} \approx E_{\mathrm{V}} - k_{\mathrm{B}}T \cdot \ln\left(\nu_{\mathrm{thp}}\sigma_{\mathrm{p}}N_{\mathrm{V}}t_{\mathrm{L}}\right) \tag{5.25}$$

The voltages corresponding to E_{Fn} and E_{Fp} are called CP threshold voltage $V_{\mathrm{TH}}^{\mathrm{CP}}$ and CP flatband voltage $V_{\mathrm{FB}}^{\mathrm{CP}}$, respectively. The maximum charge pumping current $I_{\mathrm{CP}}^{\mathrm{max}}$ is only achieved if the gate pulse exceeds both $V_{\mathrm{TH}}^{\mathrm{CP}}$ and $V_{\mathrm{FB}}^{\mathrm{CP}}$.

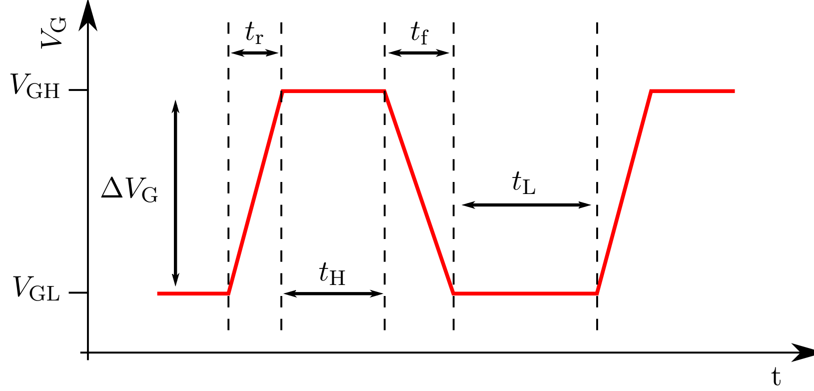


Figure 5.9.: Typical pulse geometry for a CP measurement. The I_{CP} depends on the total amplitude ΔV_{G}, the duration of the high t_{H} and low t_{L} level, the rise t_{r} and fall t_{f} time and the frequency f of the gate pulse.

CP active energy window

As mentioned before, the energy window of every CP measurement does not cover the entire band gap. In principle, the active energy window could cover the entire band gap if the rise t_{r} and fall time t_{f} of the gate pulse would be infinitely fast. However, in experiment one cannot switch arbitrarily fast. The obvious reason is the limited speed of the measurement equipment making a zero-time switch impossible from the hardware point of view. Furthermore, one has to slow down the switching speed to allow non-captured carriers to leave the channel area. Therefore, the active energy window in a CP measurement is always smaller than the entire band gap because some of the trapped carriers are re-emitted during the transition of the gate pulse. The time spans where carriers can get lost are termed emission times and are given by the relevant fractions of the rising and falling pulse slopes:

$$t_{\mathrm{en}} = \frac{V_{\mathrm{TH}}^{\mathrm{CP}} - V_{\mathrm{FB}}^{\mathrm{CP}}}{\Delta V_{\mathrm{G}}} t_{\mathrm{f}} \tag{5.26}$$

$$t_{\mathrm{ep}} = \frac{V_{\mathrm{TH}}^{\mathrm{CP}} - V_{\mathrm{FB}}^{\mathrm{CP}}}{\Delta V_{\mathrm{G}}} t_{\mathrm{r}} \tag{5.27}$$

The upper boundary of the active energy window ΔE_{CP} is now given by the trap state E_{t} which has an electron emission time constant τ_{en} equal to t_{en}. The lower boundary of ΔE_{CP} is equal to the trap state E_{t} which has an hole emission time constant τ_{ep} equal to t_{ep}. Using the equations 5.26 and 5.27 and setting them equal to 5.22 and 5.23 one can calculate the active energy window:

$$\Delta E_{\mathrm{CP}} = E_{\mathrm{G}} - 2k_{\mathrm{B}}T \cdot \log\left(\sqrt{\nu_{\mathrm{thn}}\nu_{\mathrm{thp}}}\sqrt{\sigma_{\mathrm{n}}\sigma_{\mathrm{p}}}\sqrt{N_{\mathrm{C}}N_{\mathrm{V}}}\sqrt{t_{\mathrm{f}}t_{\mathrm{r}}} \cdot \frac{V_{\mathrm{TH}}^{\mathrm{CP}} - V_{\mathrm{FB}}^{\mathrm{CP}}}{\Delta V_{\mathrm{G}}}\right) \tag{5.28}$$

By using the intrinsic carrier density n_{i}:

$$n_{\mathrm{i}} = \sqrt{N_{\mathrm{C}}N_{\mathrm{V}}} \exp\left(-\frac{E_{\mathrm{G}}}{2k_{\mathrm{B}}T}\right) \tag{5.29}$$

one can reformulate this to:

$$\Delta E_{\mathrm{CP}} = 2k_{\mathrm{B}}T \cdot \log\left(\frac{\Delta V_{\mathrm{G}}}{n_{\mathrm{i}}\sqrt{\nu_{\mathrm{thn}}\nu_{\mathrm{thp}}}\sqrt{\sigma_{\mathrm{n}}\sigma_{\mathrm{p}}}\sqrt{t_{\mathrm{f}}t_{\mathrm{r}}}(V_{\mathrm{TH}}^{\mathrm{CP}} - V_{\mathrm{FB}}^{\mathrm{CP}})}\right) \tag{5.30}$$

An experimental way to determine $V_{\mathrm{FB}}^{\mathrm{CP}}$ and $V_{\mathrm{TH}}^{\mathrm{CP}}$ is shown in the next section (see figure 5.13).

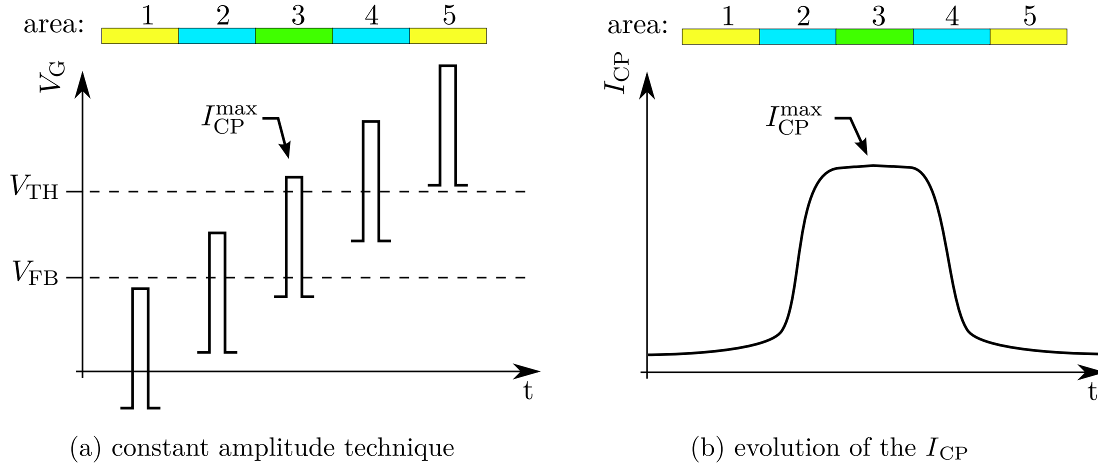
Two-level CP measurement techniques

Most common techniques for CP measurements are the so-called two-level techniques. The I_{CP} is controlled by the two levels of the gate pulse. The high level V_{GH} and the low level V_{GL}.

The most frequently used CP technique in literature is the constant amplitude technique. The levels V_{GL} and V_{GH} are changed simultaneously while the amplitude of the gate pulse is kept constant. Figure 5.10 shows the response of the I_{CP} on the gate pulse.

The measurement usually starts in accumulation. As soon as the high level of the gate pulse comes close to the charge pumping threshold voltage $V_{\mathrm{TH}}^{\mathrm{CP}}$ the I_{CP} increases significantly and saturates when $V_{\mathrm{GL}} < V_{\mathrm{FB}}^{\mathrm{CP}}$ and $V_{\mathrm{GH}} > V_{\mathrm{TH}}^{\mathrm{CP}}$. For constant amplitude CP measurements, $V_{\mathrm{FB}}^{\mathrm{CP}}$ and $V_{\mathrm{TH}}^{\mathrm{CP}}$ are probed at the same time. If the doping changes along the channel also $V_{\mathrm{FB}}^{\mathrm{CP}}$ and $V_{\mathrm{TH}}^{\mathrm{CP}}$ changes as a function of the position. This makes it hard to interpret the I_{CP} curves because there might be a unknown decrease in the I_{CP} due to a simultaneously rising low level of the pulse above $V_{\mathrm{FB}}^{\mathrm{CP}}$ like shown in figure 5.12.

To avoid this problem, one can use the fixed base level or fixed high level CP technique shown in figure 5.11. By doing so, the I_{CP} is only dependent on the high or low pulse level and not on both. For a constant base the measurement starts with a low ΔV_{G} at a very low V_{GL}. ΔV_{G} is increased stepwise until a saturation of I_{CP} occurs. Figure 5.13 shows the outcome of a constant base and constant high level CP measurement. The values of $V_{\mathrm{GL}} < V_{\mathrm{FB}}^{\mathrm{CP}}$ and $V_{\mathrm{GH}} > V_{\mathrm{TH}}^{\mathrm{CP}}$ can be determined by the derivation of the I_{CP} allowing a further tuning of V_{GL} and V_{GH} and therefore decreasing measurement time. Note that the maintenance of ΔE_{CP} is very important for a constant base/high measurement. Therefore one has to keep the slope of the gate pulse ($\Delta V_{\mathrm{G}}/\Delta t$) constant.



(a) constant amplitude technique

(b) evolution of the I_{CP}

Figure 5.10.: Schematic impact of the gate pulse level (a) on the charge pumping current I_{CP} (b). In deep accumulation with V_{GL} and V_{GH} below $V_{\mathrm{FB}}^{\mathrm{CP}}$, no I_{CP} is detected (area 1). As soon as V_{GH} comes close to $V_{\mathrm{TH}}^{\mathrm{CP}}$, the I_{CP} starts to increase and stays at maximum as long as $V_{\mathrm{GL}} < V_{\mathrm{FB}}^{\mathrm{CP}}$ and $V_{\mathrm{GH}} > V_{\mathrm{TH}}^{\mathrm{CP}}$ holds.

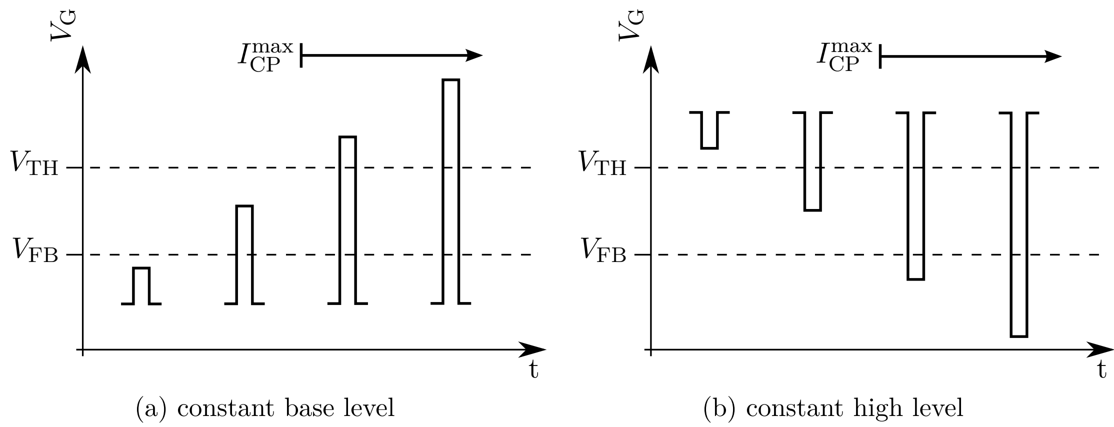


Figure 5.11.: Pulse level evolution for constant base level (a) and constant high level (b) CP techniques. The maximum I_{CP} is achieved as soon as the gate pulse encompasses $V_{\text{FB}}^{\text{CP}}$ and $V_{\text{TH}}^{\text{CP}}$.

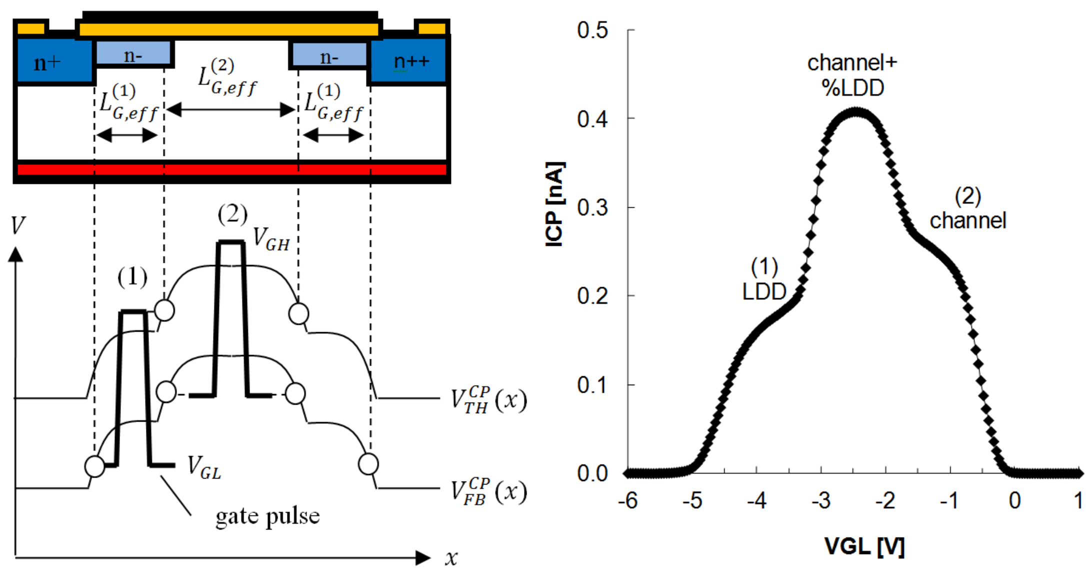


Figure 5.12.: Constant amplitude CP for a lightly doped drain (LDD) MOSFET. The I_{CP} mixes up for the channel and the LDD area like shown on the right. Therefore it is harder to distinguish the right values for V_{GL} and V_{GH} to cover the I_{CP} of the whole area. [41]

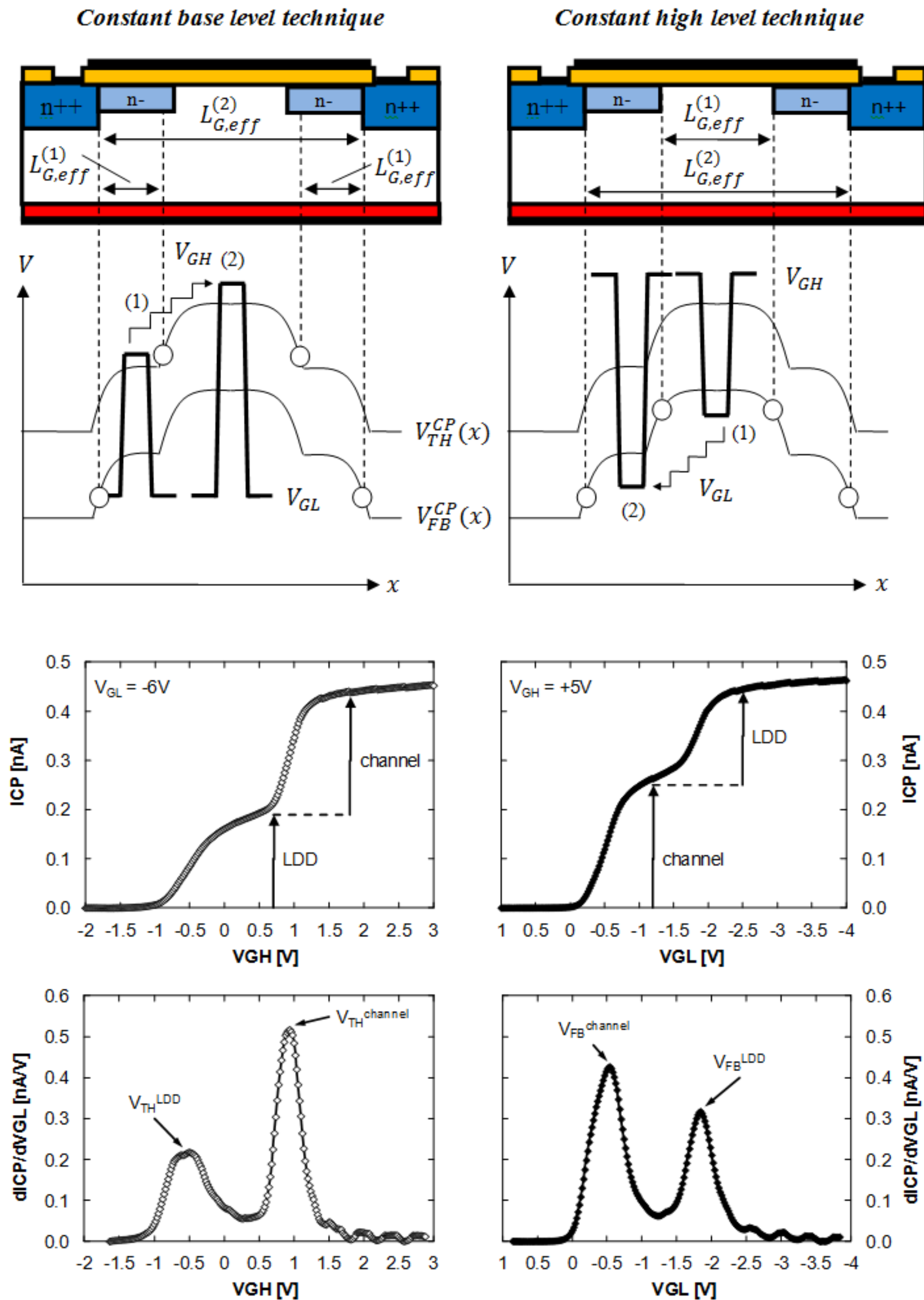


Figure 5.13.: Constant base level (left column) and constant high level (right column) CP for a LDD MOSFET. The I_{CP} response is shown in row 2. In contrast to constant amplitude CP, it is easy to distinguish the I_{CP} for each area. The determination of $V_{\mathrm{FB}}^{\mathrm{CP}}$ and $V_{\mathrm{TH}}^{\mathrm{CP}}$ can be done by the derivation of the I_{CP} curve like it is shown in the third row. [41]

6
MOSFET stress techniques

6.1. Bias temperature instability

6.1.1. Motivation

Bias temperature instability (BTI) is a key reliability issue in modern MOSFETs. BTI is the instability of important MOSFET parameters like the threshold voltage shift ΔV_{th} due to a gate bias. BTI causes a change in the output characteristics (I_{D}-V_{G}-curve) of the device. The change in the drain current I_{D} is a damage of the MOSFET and might lead to malfunction also in other parts of the circuit. Therefore it is of great interest to minimize the threshold voltage shift caused by bias temperature instability to maximize the device reliability.

6.1.2. Stress mechanics

One distinguishes between negative bias temperature instability (NBTI) and positive bias temperature instability (PBTI) according to a positive or negative stress bias on the

gate electrode with respect to all other contacts of the device. The stress itself is called positive bias temperature stress (PBTS) or negative bias temperature stress (NBTS) (see figure 6.1).

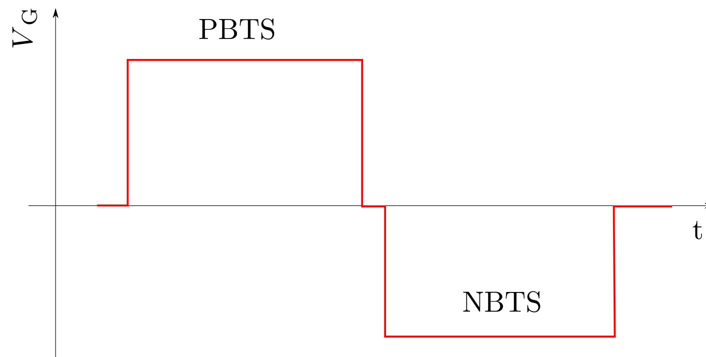


Figure 6.1.: Schematic drawing of PBTS and NBTS.

The trapping mechanisms of BTI are similar to the trapping mechanisms in charge pumping CP (see section 5.3). During the high/low level of the gate pulse, carriers are trapped at or near the SiC-SiO_2 interface region (see figure 6.2). In charge pumping most of the carriers trapped have a short capture time constant (τ_{cn} for electrons or τ_{cp} for holes as mentioned in 5.3) because the high level of the gate pulse is only maintained for a short period of time (typically some ms). For BTI the gate is biased for a much longer time. Therefore, more and more carriers can occupy traps.

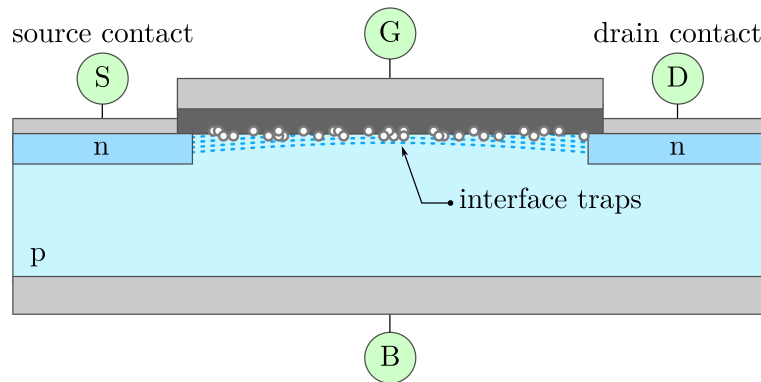


Figure 6.2.: Schematic drawing of BTI-caused carrier trapping in MOSFETs interface or near interface traps indicated as white circles.

The impact of the BTI on the transfer characteristic of an n-channel MOSFET is shown in Fig. 6.3. If the gate is stressed with a positive bias, electrons are captured (or holes emitted) near the interface causing a threshold voltage shift ΔV_{th} to a higher voltage (red arrow). A negative bias causes electron emission (or hole trapping). In this case the threshold voltage is shifted to lower voltages (blue arrow). The degradation caused by BTI exhibits logarithmic dependence on time (see Fig. 6.4).

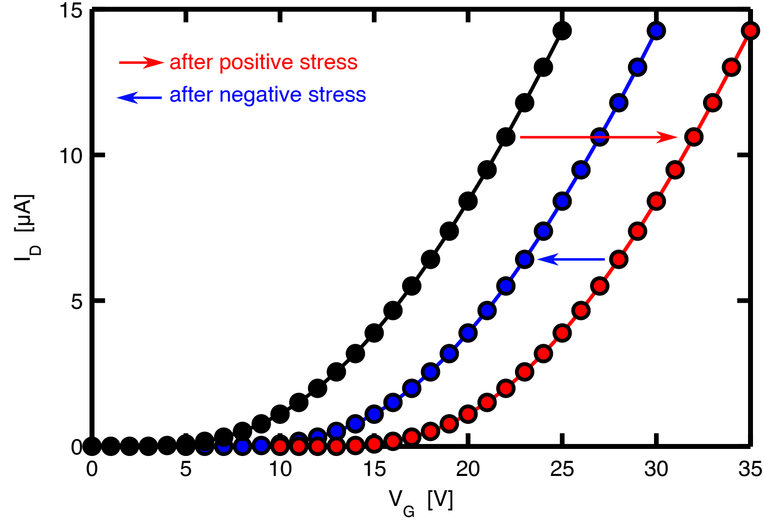


Figure 6.3.: Impact of bias temperature stress on the I_{D}-V_{G} characteristics of an n-channel MOSFET. The positive stress causes electron trapping near the interface which results in a threshold voltage shift to the right. Negative bias stress empties the traps causing a threshold voltage shift to the left. For a p-channel MOSFET the threshold voltage shifts the other way around.

The density of charges at the interface n can be extracted from the equation for the capacitance

$$C_{\mathrm{OX}} = \frac{Q}{V} = \frac{nq}{V} \tag{6.1}$$

which leads to

$$n = \frac{C_{\mathrm{OX}}}{q} V. \tag{6.2}$$

The change in the number of charges at the interface (trapped charges) Δn after positive or negative bias stress can therefore be calculated from the threshold voltage shift ΔV_{th}

by the formula

$$\Delta n = \frac{C_{\mathrm{OX}}}{q} \Delta V_{\mathrm{th}}. \tag{6.3}$$

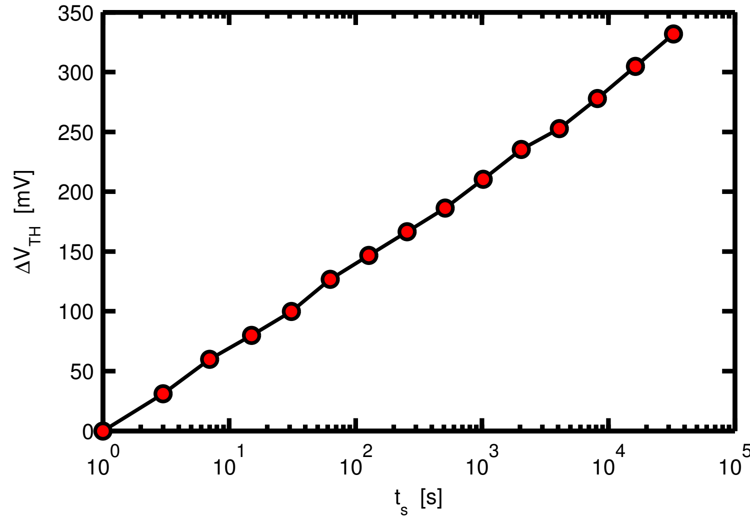


Figure 6.4.: Impact of positive bias stress of 30 V on a n-channel SiC-MOSFET at 150 °C. The threshold voltage shift exhibits a logarithmic dependence on the stress time.

6.2. Hot carrier degradation

In this thesis, no hot carrier degradation (HCD) stress was done. However, for completeness this section gives a short overview on HCD because it is one of the most important stress techniques for high-power devices.

Carriers in a the channel of a MOSFET are accelerated by the lateral electric field caused by the voltage between source and drain V_{DS}. By increasing V_{DS}, carriers might be able to reach very high kinetic energies (*hot* electrons). The carrier energy is lost in two different ways. First, the carriers may cause impact ionization close to the drain region. If the impact ionization creates an electron-hole pair within the space charge region, the electron-hole pair is separated by the electric field of the space charge region. This is the reason why a substrate current can be observed during HCD stress. Second, the carriers might overcome a potential barrier for the activation of point defects close to the

semiconductor-insulator interface. These defects act as charges causing poor electrical behavior of the device. Similar to BTI, HCD causes a threshold voltage shift ΔV_{th} and furthermore a strong decrease in the mobility μ. The degradation caused by HCD is located near the drain side of the device. The reason for this is the larger kinetic energy of the carriers in this region.

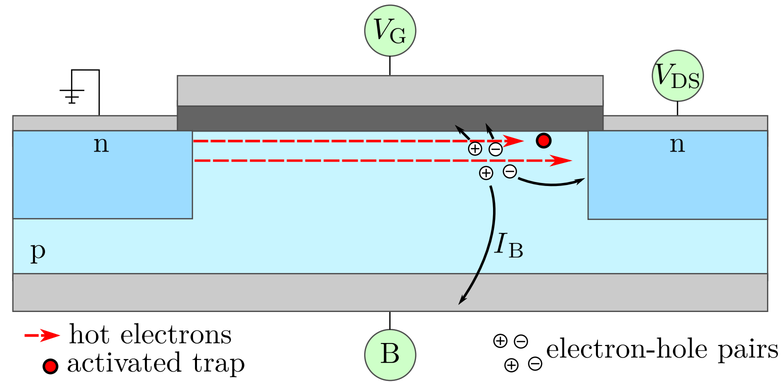


Figure 6.5.: Schematic drawing of a HCD stress. Hot carriers (red arrows) are causing impact ionization and creation of electron-hole pairs and the activation of interface/near interface defects (red circle).

Part III.

RESULTS

7

Impact of nitric oxide post oxidation anneal on the bias temperature instability and the on-resistance

The content of this chapter has been published in the proceedings of the European Conference of Silicon Carbide and Related Materials 2014 (ECSCRM)

7.1. Motivation

High temperature annealing in an nitric oxide (NO) or nitrous oxide (N_2O) containing atmosphere is an important process to enhance the electrical properties of SiC devices. However, there are still a lot open questions concerning the microscopic mechanisms of the annealing process. The impact of the post oxidation anneal (POA) depends on multiple parameters like the POA temperature T_{POA}, POA time t_{POA}, gas composition and of course all additional interface characteristics of the device itself (e.g. oxide growth

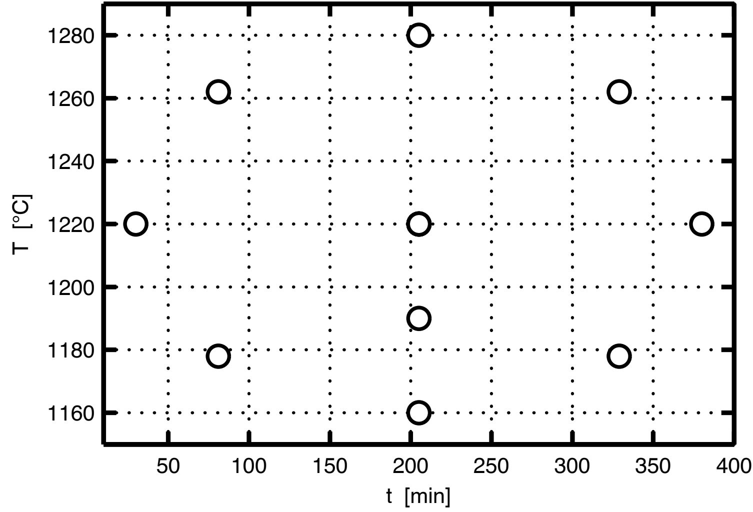


Figure 7.1.: Available NO-POA time and temperature combinations.

techniques and crystal faces). Therefore, further optimizing the POA process is one of the important steps to produce improved devices in the future.

This chapter describes the impact of the NO-POA time t_{POA} and NO-POA temperature T_{POA} on the on-resistance R_{on} and on the device reliability (threshold voltage shift ΔV_{th}) during positive bias temperature stress (PBTS).

7.2. Experimental setup

The MOSFETs were fabricated on 4H-SiC substrates. The devices have a 70 nm thick SiO_2 oxide deposited via chemical vapor deposition (CVD). The oxide thicknesses were verified via CV measurements using an Agilent 4294A impedance analyzer. All samples were annealed in an NO containing atmosphere at various temperatures and times. The available combinations are shown in Fig. 7.1.

At least four devices of each NO-POA process variant were subjected to PBTS at 150 °C according to the test procedure outlined in figure 7.2. The PBTS duration was increased by a factor of ten from one stress run to the next. A positive stress voltage of 30 V was chosen which corresponds to an electric field of about 4.3 MV cm^{-1}. As indicated in Fig. 7.2, the characterization also contains a low non-destructive negative bias phase of −10 V (−1.4 MV cm^{-1}) for 1 second to accumulate holes at the SiC-SiO_2 interface. This bias phase removes a large fraction of the threshold voltage drift. The measurements were

performed using an Agilent B1500A parameter analyzer. The overall PBTS time for all samples was 1111 seconds (4 cycles). The on-resistances of the unstressed devices were measured on roughly 80 virgin samples of each NO-POA split group. The complete measurement setup is sketched in Fig. 7.3.

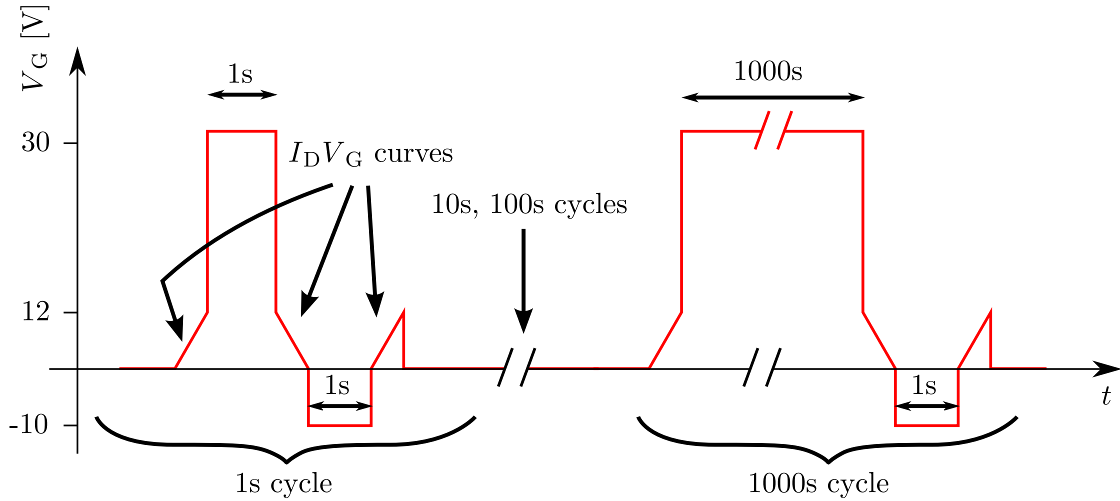


Figure 7.2.: Test procedure for PBTS measurements. The PBTS duration was increased by a factor of ten from one cycle to the next. A positive stress voltage of 30 V was chosen which corresponds to an electric field of about $4.3\,\mathrm{MV\,cm^{-1}}$. Before and after the stress, an I_D-V_G curve was measured to analyze the shift caused by the stress. A low non-destructive negative bias phase of -10 V resulting in an electric field of $-1.4\,\mathrm{MV\,cm^{-1}}$ was used to analyze the recovery behaviour of the ΔV_{th}.

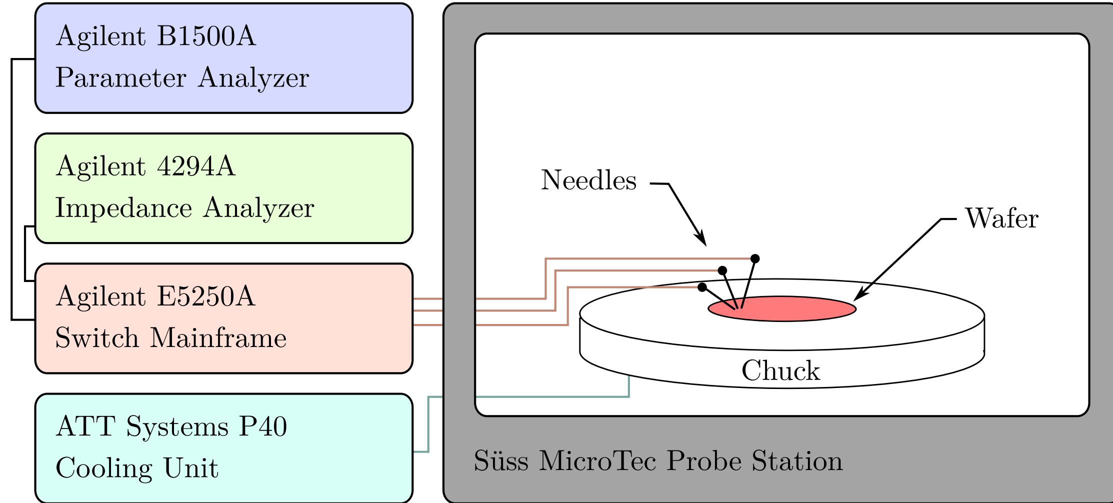


Figure 7.3.: Schematic experimental setup. The Agilent B1500 parameter analyzer was used as current or voltage source. Capacitance-voltage measurements were done with the Agilent 4294A impedance analyzer. The chuck temperature was controlled by the ATT Systems P40 cooling unit. An Agilent E5150A switching matrix was used to connect multiple needles to one device.

7.3. The impact of the annealing temperature

The change in threshold voltage shift ΔV_{th} and on-resistance R_{on} for a constant POA time of 205 minutes and various POA temperatures T_{POA} is shown in Fig. 7.4. A significant trend is observed for both threshold voltage shift and on-resistance. For ΔV_{th}, the measurement shows a decrease with higher POA temperature T_{POA} (see Fig. 7.4a) which can be described by a linear model

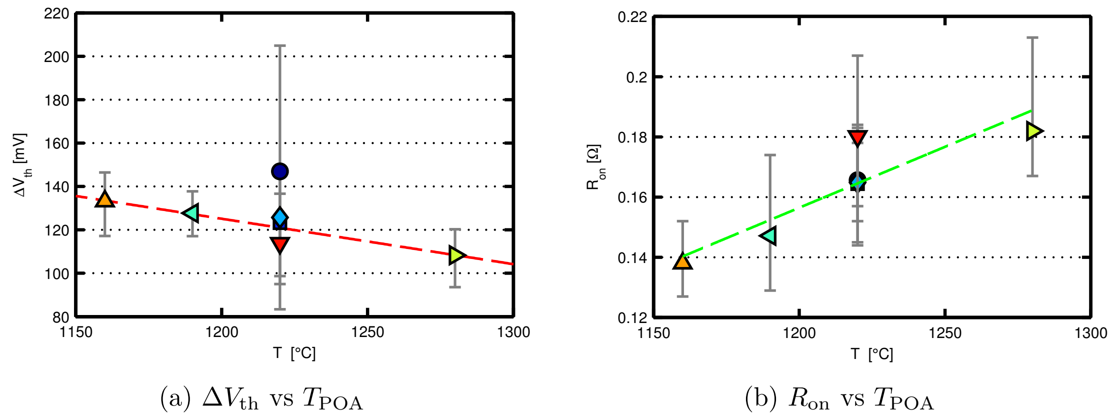
$$\Delta V_{\mathrm{th}} = 0.433\,\mathrm{V} - 2.09 \times 10^{-4}\,\mathrm{V\,K^{-1}} \cdot T_{\mathrm{POA}}. \tag{7.1}$$

In contrast to the ΔV_{th}, the R_{on} is increasing with T_{POA} (see Fig. 7.4b). The impact of the POA temperature on the R_{on} can be described as

$$R_{\mathrm{on}} = -0.419\,\Omega + 3.91 \times 10^{-4}\,\Omega\,\mathrm{K^{-1}} \cdot T_{\mathrm{POA}}. \tag{7.2}$$

The opposite impact of the POA temperature at constant POA time on the threshold voltage shift and the on-resistance leads to the ΔV_{th}-R_{on} correlation shown in Fig. 7.7.

This means optimizing the NO-POA temperature for low on-resistance has negative effects on the threshold voltage shift and vice versa.



(a) ΔV_{th} vs T_{POA} (b) R_{on} vs T_{POA}

Figure 7.4.: Impact of T_{POA} on the threshold voltage shift (a) and the on-resistance (b).

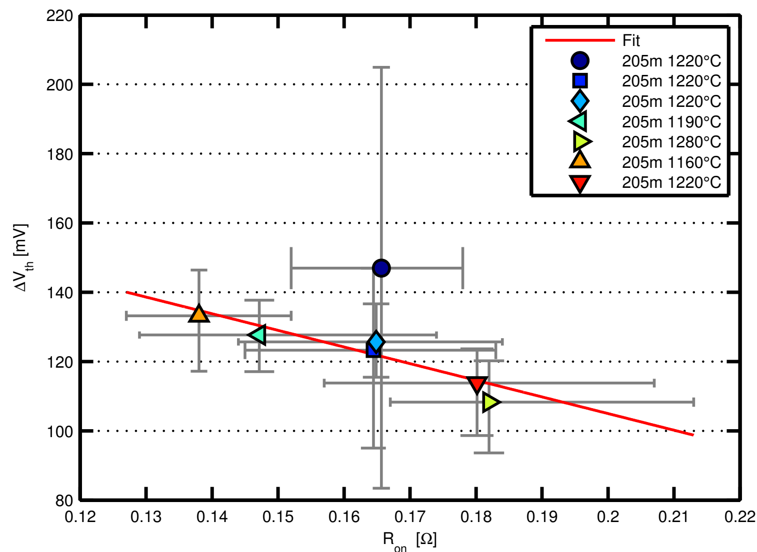


Figure 7.5.: ΔV_{th} vs R_{on} for various POA temperatures and constant POA time of 205 min.

7.4. The impact of the annealing time

The change in threshold voltage shift and on-resistance for a constant T_{POA} of 1220 °C and various POA times is shown in Fig. 7.6. Like the post oxidation anneal (POA)

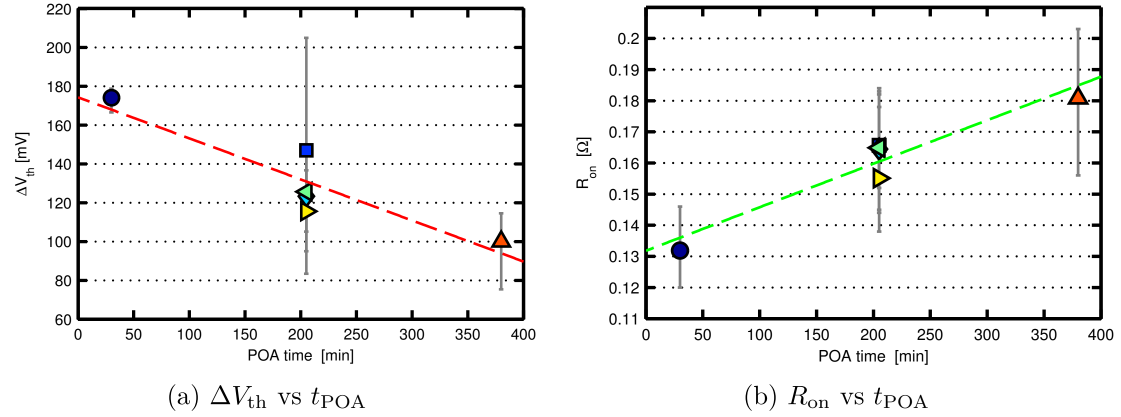
temperature (section 7.3), also the POA time t_{POA} shows a different impact on ΔV_{th} and R_{on}. For ΔV_{th}, the measurement shows a decrease with longer POA time (see Fig. 7.6a) which can be described by

$$\Delta V_{\mathrm{th}} = 0.174\,\mathrm{V} - 3.52 \times 10^{-6}\,\mathrm{V\,s^{-1}} \cdot t_{\mathrm{POA}}. \tag{7.3}$$

The R_{on} is increasing with t_{POA} (see Fig. 7.6b) and can be described as

$$R_{\mathrm{on}} = 0.132\,\Omega + 2.33 \times 10^{-6}\,\Omega\,\mathrm{s^{-1}} \cdot t_{\mathrm{POA}}. \tag{7.4}$$

The contrary impact of the POA time at constant POA temperature on the threshold voltage shift and the on-resistance leads to the ΔV_{th}-R_{on} correlation shown in figure 7.7. Therefore, also for a NO-POA at constant temperature one has to optimize the t_{POA} for both R_{on} and ΔV_{th} depending on the design target.



(a) ΔV_{th} vs t_{POA}

(b) R_{on} vs t_{POA}

Figure 7.6.: Impact of t_{POA} on the threshold voltage shift (a) and the on-resistance (b).

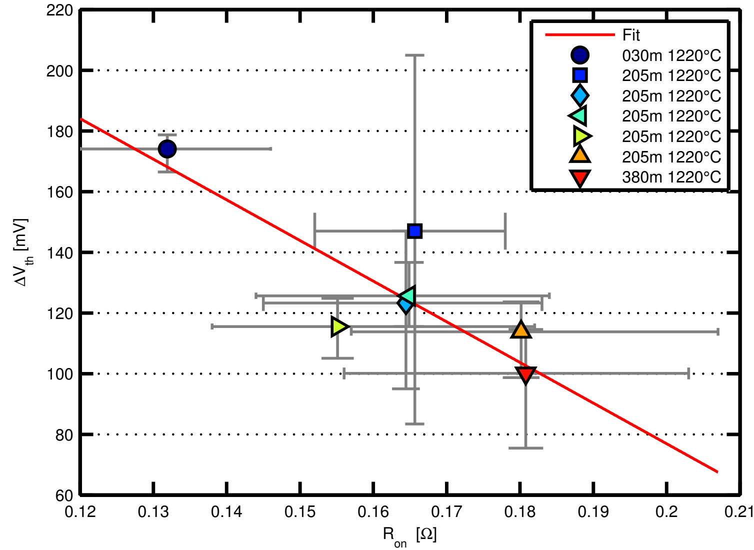


Figure 7.7.: ΔV_{th} vs R_{on} for various POA times and a constant POA temperature of 1220 °C.

7.5. Combined impact of POA temperature and POA time

The impact of the POA time and POA temperature is shown in Fig. 7.8 for the threshold voltage shift and in Fig. 7.9 for the on-resistance. The same trend as before is observed. As shown in Fig. 7.8, the NO-POA causes a increase in threshold voltage shift for shorter NO-POA times and lower NO-POA temperatures. The total increase in threshold voltage shift is about 90% within the measured nitric oxide (NO)-POA range. As opposed to the change in ΔV_{th}, the on-resistance of the devices increases with NO-POA temperature and time as shown in Fig. 7.9. The overall increase in R_{on} is about 60%. This means that a NO-POA process optimized for low R_{on} tends to show an increased threshold voltage shift (see section 7.6). Note that the observed change in R_{on} cannot be explained by a change in oxide capacitance C_{OX} because R_{on} is inversely proportional to C_{OX} in standard transistor models and the maximum change in C_{OX} during the NO-POA is only about 15%.

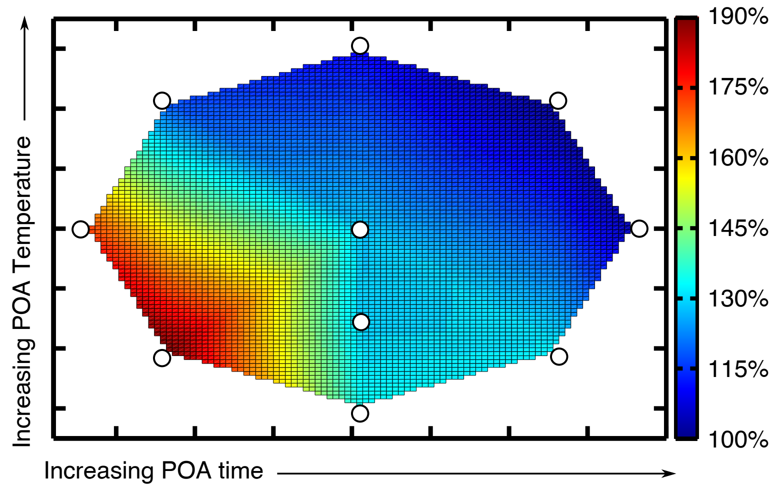


Figure 7.8.: Threshold voltage shift ΔV_{th} as a function of POA time and POA temperature.

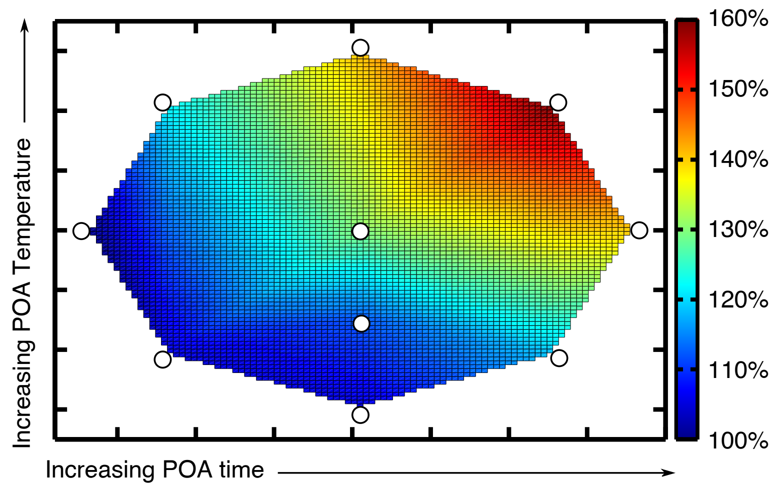
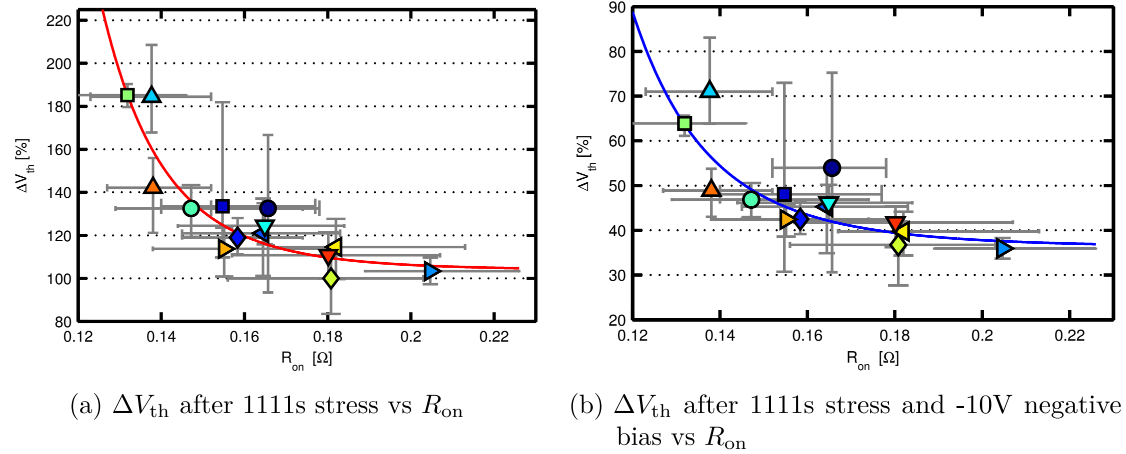


Figure 7.9.: On-resistance R_{on} as a function of POA time and POA temperature.

7.6. Threshold voltage shift as a function of on-resistance and the impact of the negative bias

A NO-POA process optimized for low R_{on} tends to show an increased threshold voltage shift and vice versa as shown in Fig. 7.10. A large fraction of the ΔV_{th} can be straightforwardly recovered by applying a negative bias of $-10\,\mathrm{V}$ to the gate. A negative pulse of one second results in the recovery of roughly 65 % of the ΔV_{th} (see Fig. 7.11).

This indicates that some defects which trap electrons during PBTS can be efficiently discharged by applying a negative bias to the gate. Similar observations on Si-MOSFETs were attributed to charging and discharging of near-interface oxide traps [46].



(a) ΔV_{th} after 1111s stress vs R_{on}

(b) ΔV_{th} after 1111s stress and -10V negative bias vs R_{on}

Figure 7.10.: The contrary impact of the NO-POA temperature and time on the threshold voltage shift and the on-resistance leads to the ΔV_{th}-R_{on} characteristics shown in (a). The impact of the $-10\,\mathrm{V}$ negative bias is shown in (b). The values are normalized to the wafer with the smallest threshold voltage shift after 1111s stress (◊).

The fraction of recoverable shift ($\approx 65\,\%$) is independent of the NO-POA time and temperature (see Fig. 7.11). This indicates the defect types annealed by every NO-POA process variant are the same. Only the amount of annealed defects changes for every NO-POA split.

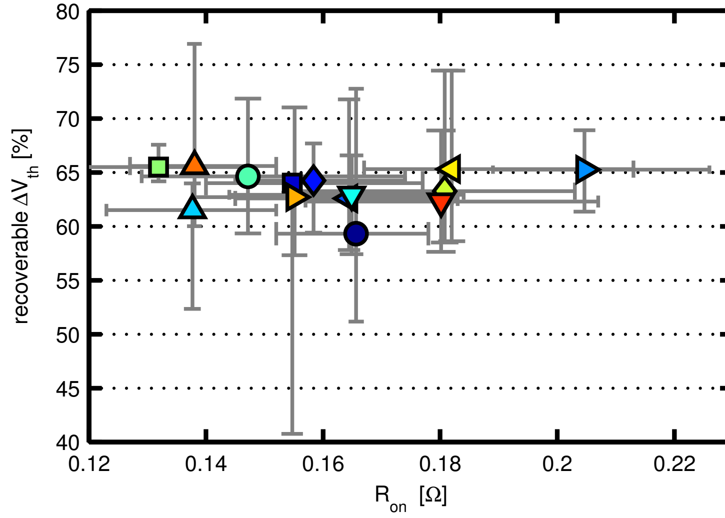


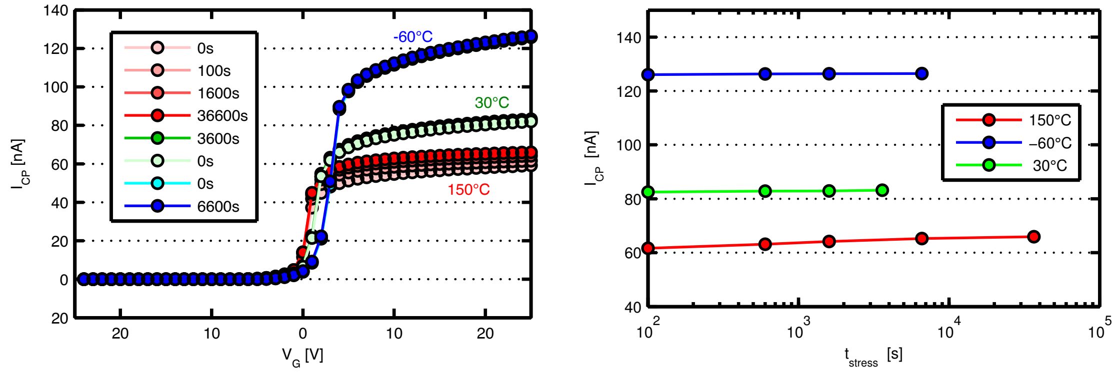
Figure 7.11.: Recoverable part of the threshold voltage shift for a negative bias of −10 V for one second. The amount of shift recovered does not depend on the NO-POA time or temperature.

7.7. Defect analysis

Despite a large ΔV_{th} ($\approx 600\,\text{mV}$), only a negligibly small decrease in the low field mobility ($< 4\,\%$) could be detected after 1111 seconds PBTS. Interface defects act as scattering centers and degrade the mobility. This supports the idea that most of the degradation during PBTS happens within the oxide or near the SiO_2/SiC interface.

According to section 5.3, charge pumping (CP) is a sensitive tool to measure the density of interface traps. Therefore CP measurements were done to estimate the number of interface traps caused by PBTS. Due to a non changing mobility after PBTS, also the I_{CP} should stay the same if the traps are not located at the interface. Figure 7.12 shows the I_{CP} for different PBTS stress times and temperatures. The devices were stressed and measured at −60 °C, 30 °C and 150 °C. At −60 °C and 30 °C the I_{CP} does not change with PBTS time, although the 6600 s positive bias stress at −60 °C results in about 550 mV effective ΔV_{th}. Even at 150 °C only a small increase in the $I_{\text{CP}}^{\text{max}}$ of about 8 % is observed after a 36 600 s positive bias stress.

Therefore also the CP measurements suggest traps in the near interface or the oxide are responsible for the threshold voltage shift caused by PBTS.



(a) I_{CP} for different PBTS stress temperatures and times

(b) Maximum I_{CP} for different PBTS times and temperatures

Figure 7.12.: Charge pumping current I_{CP} for different PBTS stress times and temperatures. As shown in (b), PBTS does not have a large impact on the maximum charge pumping current although the stress duration was very long leading to a large threshold voltage shift of several hundred mV. The decrease in I_{CP} for higher temperatures is due to a narrower CP energy window ΔE_{CP} (see section 5.3).

7.8. Summary

The NO-POA time t_{POA} and NO-POA temperature T_{POA} have a contrary impact on the on-resistance R_{on} and on the threshold voltage shift ΔV_{th} during positive bias temperature stress (PBTS). The NO-POA causes a decrease in overall threshold voltage shift for longer NO-POA times and higher NO-POA temperatures. Considerable agreement exists [25, 47, 35] that the NO-POA leads to nitrogen incorporation at the SiC/SiO_2 interface and extends a few nanometers into the oxide. It is speculated that nitrogen passivates defects at or near the SiC/SiO_2 interface thereby reducing the number of electron traps and increasing the density of hole traps in the oxide. This would explain a lower threshold voltage shift for enhanced NO-POA time and temperature. In contrast, the R_{on} increases with t_{POA} and T_{POA}. The reason for this is not clear at the moment. A possibility is an increase in interface roughness due to nitrogen incorporation similar to what was reported for N_2O anneals [24] or the formation of a SiO_xN_y interface layer with different electrical properties [25]. The Si-vacancy is most probably not responsible for the decrease in mobility for increased POA parameters due to a decrease of this defect during nitridation [48]. According to Lelis et al. [49], the main near-interface defect is likely some variation of the E'-type oxide defect, which is associated with an oxygen vacancy. This is the only

type of oxide defect reported in SiC-MOSFETs using the electrically detected magnetic resonance (EDMR) technique [50]. The E'-type defect might be responsible for a part of the threshold voltage shift during positive bias temperature stress by catching a second electron at elevated temperatures and become net negatively charged [51].

To conclude, optimizing the NO-POA for low R_{on} can have negative effects on the threshold voltage stability of the device. To get a reliable SiC MOSFET with excellent performance, one has to optimize the NO-POA for both BTI and R_{on}.

8 Conclusion and Outlook

The wide band gap semiconductor material silicon carbide (SiC) promise a better performance for future power devices. SiC allows an operation at higher temperature, higher power density, higher voltage and higher frequency than silicon based devices.

The interface between the silicon dioxide and the silicon carbide is mainly responsible for the electrical properties of the device. Defects in this region impact the output characteristics of the devices directly. To reduce the density of interface states the industry uses annealing in certain gas atmospheres. High temperature annealing in nitric oxide (NO) containing atmosphere is an important process to enhance the electrical properties of the devices. This thesis investigates the impact of the NO post oxidation anneal (POA) on the reliability of SiC power MOSFETs. The quality of the POA depends strongly on the POA temperature and the POA time. Therefore, an optimization of the annealing process is of great interest for the industry.

The impact of the annealing time and annealing temperature on the on-resistance and the reliability after bias temperature instability stress tests was investigated in this thesis and a strong dependence on the annealing parameters was observed. The NO-POA time and NO-POA temperature show a contrary impact on the on-resistance R_{on} and on

the threshold voltage shift ΔV_{th} during positive bias temperature stress (PBTS). The NO-POA causes a decrease in threshold voltage shift for longer NO-POA times and higher NO-POA temperatures. In contrast, the on-resistance increases with POA time and POA temperature. The best device performance is observed for POA temperatures below 1180 °C and POA times of at least 200 minutes. Both, on-resistance and threshold voltage shift show the best results within the design of experiment.

The main mechanisms and/or defects responsible for bias temperature instability and mobility limiting factors in 4H-SiC devices are still unknown. A possible explanation is an increase in interface roughness due to nitrogen incorporation and further oxidation during (high-temperature) POA or the formation of a SiO_xN_y interface layer with different electrical properties. Further investigations on interface roughness and composition are possible by electron energy loss spectroscopy (EELS) or X-ray reflectometry (XRR) and might lead to a better understanding of the modifications at the interface caused by the post oxidation anneal. The silicon vacancy causes an decrease of mobility and is significantly reduced by nitridation [48]. Thus, the Si-vacancy is most probably not responsible for the decrease in mobility for increased POA parameters. According to Lelis et al. [49], the main near-interface defect is likely some variation of the E'-type oxide defect, which is associated with an oxygen vacancy. This is the only type of oxide defect reported in SiC-MOSFETs using the electrically detected magnetic resonance (EDMR) technique [50]. The E'-type defect might be responsible for a part of the threshold voltage shift during positive bias temperature stress by catching a second electron at elevated temperatures and become net negatively charged [51].

Although significant improvements on the device reliability and characteristics were achieved in the last years, further investigations on the defects are necessary for further device improvements. The most promising techniques for the defect identification are the time dependent defect spectroscopy (TDDS) and electrically detected magnetic resonance (EDMR) measurements combined with theoretical density functional theory (DFT) simulations.

Symbols

Symbol	Description	Unit
A_{G}	gate area of a MOSFET	cm^2
C_{OX}	Oxide capacitance of the MOSFET	F
D_{it}	density of interface traps	$\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$
E_{C}	Energy at the bottom of the conduction band	eV
E_{Fi}	intrinsic Fermi energy	eV
E_{Fn}	quasi Fermi level for electrons	eV
E_{Fp}	quasi Fermi level for holes	eV
E_{F}	Fermi energy	eV
E_{G}	band gap energy	eV
E_{V}	Energy at the top of the valence band	eV
E_{t}	trap energy	eV
I_{CP}	charge pumping current	A
I_{D}	drain current	A
$I_{\mathrm{CP}}^{\mathrm{geo}}$	geometric charge pumping current	A
$I_{\mathrm{CP}}^{\mathrm{max}}$	maximum charge pumping current	A
N_{CP}	number of pumped charges per unit area	cm^{-2}
N_{C}	effective density of states in the conduction band	cm^{-3}
N_{V}	effective density of states in the valence band	cm^{-3}
R_{on}	on resistance of a MOSFET	Ω
T_{POA}	post oxidation annealing temperature	K
T_{d}	Debye temperature	K
T	temperature	K
V_{DS}	drain-source voltage	V
$V_{\mathrm{TH}}^{\mathrm{G}}$	threshold voltage extracted by the method of Ghibaudo	V
V_{TH}	threshold voltage	V
$V_{\mathrm{FB}}^{\mathrm{CP}}$	charge pumping flat band voltage	V

Symbol	**Description**	**Unit**
V_{FB}	flat band voltage	V
V_{GH}	high level of the gate pulse	V
V_{GL}	low level of the gate pulse	V
V_{G}	gate voltage	V
$V_{\mathrm{TH}}^{\mathrm{CP}}$	charge pumping threshold voltage	V
V	voltage	V
Y	Young's modulus	Pa
ΔE_{CP}	active charge pumping energy window	eV
ΔV_{G}	total amplitude of the gate pulse	V
ΔV_{th}	threshold voltage shift	V
μ_0	low field mobility	$\mathrm{cm^2\,V^{-1}\,s^{-1}}$
μ_{EFF}	effective mobility	$\mathrm{cm^2\,V^{-1}\,s^{-1}}$
μ_{e}	electron mobility mobility	$\mathrm{cm^2\,V^{-1}\,s^{-1}}$
μ_{h}	hole mobility	$\mathrm{cm^2\,V^{-1}\,s^{-1}}$
μ_{max}	maximal bulk mobility	$\mathrm{cm^2\,V^{-1}\,s^{-1}}$
μ	mobility	$\mathrm{cm^2\,V^{-1}\,s^{-1}}$
ν_{thn}	thermal drift velocity of electrons	$\mathrm{cm\,s^{-1}}$
ν_{thp}	thermal drift velocity of holes	$\mathrm{cm\,s^{-1}}$
ϕ_{M}	work function of the metal	V
ϕ_{S}	work function of the semiconductor	V
σ_{n}	capture cross section of electrons	$\mathrm{cm^{-2}}$
σ_{p}	capture cross section of holes	$\mathrm{cm^{-2}}$
τ_{cn}	time constant for electron capture in SRH theory	s
τ_{cp}	time constant for hole capture in SRH theory	s
τ_{en}	time constant for electron emission in SRH theory	s
τ_{ep}	time constant for hole emission in SRH theory	s
τ	transition time constant	s
θ	thermal conductivity	$\mathrm{W\,cm^{-1}\,K^{-1}}$
ξ_{c}	critical field	$\mathrm{MV\,cm^{-1}}$
d_{OX}	Oxide thickness	cm
f	frequency	Hz
k_{B}	Bolzmann constant $k_{\mathrm{B}} = 8.617\,332\,478 \times 10^{-5}\,\mathrm{eV\,K^{-1}}$	$\mathrm{eV\,K^{-1}}$
n_{i}	intrinsic carrier density	$\mathrm{cm^{-3}}$
n_{s}	concentration of free electrons	$\mathrm{cm^{-3}}$
n	free electron density in the conduction band	$\mathrm{cm^{-3}}$

Symbol	Description	Unit
p_{s}	concentration of free holes	cm^{-3}
p	free hole density in the valence band	cm^{-3}
q	the elementary charge $1.602\,176\,565\,35 \times 10^{-19}\,\mathrm{C}$	C
t_{H}	high level duration of the gate pulse	s
t_{L}	low level duration of the gate pulse	s
t_{POA}	post oxidation annealing time	s
t_{f}	fall time of the gate pulse	s
t_{r}	rise time of the gate pulse	s

Acronyms

I_D-V_G	drain current vs gate voltage characteristics of a MOSFET.
4H-SiC	specific polytype of the silicon carbide crystal.
Ar	argon.
BTI	bias temperature instability.
C	carbon.
CO	carbon monoxide.
CP	charge pumping.
CV	capacitance-voltage.
CVD	chemical vapor deposition.
ELR	extrapolation in the linear regime.
H	hydrogen.
HCD	hot carrier degradation.
LDD	lightly doped drain.
MOS	metal oxide semiconductor.
MOSCAP	metal oxide semiconductor capacitor.
MOSFET	metal oxide semiconductor field effect transistor.
N	nitrogen.
N_2	dinitrogen.
N_2O	nitrous oxide.

NBTI	negative bias temperature instability.
NBTS	negative bias temperature stress.
NH_3	ammonia.
NO	nitric oxide.
NRA	nuclear reaction analysis.
O	oxygen.
O_2	dioxygen.
OLCAO	orthogonalized linear combination of atomic orbitals method.
PBTI	positive bias temperature instability.
PBTS	positive bias temperature stress.
POA	post oxidation anneal.
RBS	Rutherford backscattering spectrometry.
Si	silicon.
SiC	silicon carbide.
SIMS	secondary ion mass spectrometry.
SiO_2	silicon dioxide.
SRH	Shockley-Read-Hall.
XPS	X-ray photoelectron spectroscopy.

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