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Leakage Current Measurement in a Scribe Line Module

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Kurzfassung

Niedrige Leistungsaufnahme und längere Zeiten zwischen den Wiederaufladungen der Batterien sind ein wichtiges Merkmal von modernen Elektronikgeräten. Des Weiteren erlauben niedrige Leckströme und Stand-By Ströme fortschrittlichere Anwendungen wie Energy Harvesting in rauen Umgebungen oder in Smart Sensors.
Die Überwachung kleiner Ströme und deren statistische Analyse gestalten sich schwieriger, je kleiner die Messwerte werden. Process Control Monitoring (PCM) Teststrukturen werden in der Scribe Line jedes Produktwafers platziert. Diese Strukturen werden als Scribe-Line-Monitors (SLMs) bezeichnet.
Die Breite der Scribe Line schränkt die Größe der Bauteile und somit die zu messenden Stromstärken ein. Zusätzlich finden PCM Messungen auf einer nominellen Temperatur statt.
Diese Arbeit beschreibt die Entwicklung und Messung einer integrierten SLM-Teststruktur zur Messung kleiner Ströme bei Raumtemperatur bis in den fA-Bereich. Der Fokus liegt hierbei besonders auf der Messung von Dioden-Leckströmen. Bei der Entwicklung wurde auf Bauteile zurückgegriffen, die in allen Prozessoptionen zur Verfügung stehen. Dies gewährleistet eine breite Einsatzfähigkeit der Schaltung in der Fertigung.
Die entwickelte SLM-Teststruktur wird künftig auf Produktionswafern integriert und bietet die Möglichkeit kleine Ströme zu überwachen. Bei Aufnahme vieler Messdaten für ein Bauteil kann dessen Strom statistisch bewertet werden. Dies stellt ausschlaggebende Informationen über den Prozess im Generellen bereit und ist besonders wichtig für eine statistische und Worst Case Modellierung in SPICE.

Abstract

Low power consumption and long run-time between battery recharging are key features for modern consumer electronics. Furthermore, low leakage and stand-by currents enable advanced applications e.g. for energy harvesting in harsh environments or for smart sensors.

Leakage current monitoring and statistical analysis becomes more challenging the smaller the current is. Process control monitoring (PCM) test structures are placed in the scribe line on each product wafer, the structures are referred to as scribe-line monitors (SLMs). The scribe line width limits the devices size and hence the value of the current. Furthermore PCM measurements run at nominal temperature $T_{nom} = 27^o$ C only in order to enable high wafer throughput.

This thesis covers the design and measurement of an integrated SLM test structure for measuring small currents down to the fA-range at room temperature. Diode leakage current is of special interest. The circuit can be implemented in any module of the base process because a commonly available device set was used.

The SLM test structure will be integrated on product wafers and offers the opportunity to monitor small currents. A statistical data analysis can be performed after recording for particular devices multiple times. The outcomes provide crucial information about the process in general and are specifically important for statistical and worst case SPICE modeling.

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List of Symbols

Symbol	Unit	Description
A	m^2	Area
B	Hz	Bandwidth
c_A	$\mathrm{F/m}^2$	Specific area capacitance
c_P	F/m	Specific perimeter capacitance
C	F	Capacitance
D	m^2/s	Diffusion constant
$\mathbf{E}$	V/m	Electric field
ϵ	F/m	Permittivity, dielectric constant
ϵ_0	F/m	Permittivity of free space, dielectric constant of free space
ϵ_r	1	Relative permittivity, relative dielectric constant
f	Hz	Frequency
g_m	$1/\Omega$	Transconductance
G	1	Gain
$\mathbf{H}$	A/m	Magnetic field
H	1	Transfer function, frequency response
i	A	Time-dependent electric current
I	A	Constant electric current
j	1	Imaginary unit
$\mathbf{J}$	$\mathrm{A/m}^2$	Current density
J_A	$\mathrm{A/m}^2$	Specific area current
J_P	A/m	Specific perimeter current
k_B	J/K	Boltzmann constant
L	m	Device length
μ	$\mathrm{m}^2/(\mathrm{V}\cdot\mathrm{s})$	Mobility
μ_m	H/m	Permeability
μ_0	H/m	Permeability of free space
μ_r	1	Relative permeability
n	$1/\mathrm{m}^3$	Electron density
N	$1/\mathrm{m}^3$	Doping concentration
ω	1/s	Angular frequency
p	$1/\mathrm{m}^3$	Hole density
P	m	Perimeter
q	C	Elementary charge

Symbol	Unit	Description
Q	C	Electric charge
r_o	Ω	Output resistance
R	Ω	Electric resistance
s	1/s	Complex frequency
t	s	Time
T	K	Temperature
τ	s	Life time
v	V	Time-dependent voltage
V	V	Constant voltage
W	m	Device width

Chapter 1

Introduction

Motivation

Device and process characterization is an essential task for a semiconductor chip manufacturer. Circuit simulator models and costumers require information on process and device behavior and their statistical distribution. Process and device parameters are measured on special test structures on wafers. After wafer production these structures are probed by the tester and the readings are stored. Additionally a particular quantity can be investigated and wafers that meet the specification are selected for further processing, e.g wafer sort testing, packaging, etc. In general early identification and removal of wafers or chips which do not fulfill the specification prevents costs. The obtained process and device parameters are used to improve circuit simulator and device models. One such quantity of interest is the leakage current of p-n-junctions. It is a crucial quantity for chip power consumption and a key performance parameter for certain devices like photodiodes.

Problem

Test structures on a typical product wafer are placed in the scribe which is the silicon area in-between the individual chips. This area is lost when the chips are cut from the wafer at the end of chip fabrication. The pad pattern and dimension of the available area is referred to as the scribe-line-monitor (SLM). Hence leakage currents of p-n-junctions are difficult to measure on typical product wafers as the device dimensions are limited. Furthermore the temperature is fixed to nominal temperature during wafer test measurements. Thus the traditional approach of measuring the leakage current at high temperatures is not applicable.

A circuit for leakage current measurement suitable for wafer test measurement is the goal of this thesis. The circuit has to be designed to be implemented in any module of the base process. This limits the available devices to a commonly available set. In order to keep the application as general as possible, the circuit is specified to measure different kinds of devices under test (DUTs), like diodes and transistors.

Literature offers numerous sources for the measurement of small currents on a wafer [1, 2, 3, 4, 5, 6]. Each serves a special purpose like the investigation of stress induced leakage current [4, 5] and the device under test (DUT) of these papers is well defined. The test structures discussed in literature are not constrained by the available area. However, principle design ideas are used from these sources.

A discussion of the fundamentals is given at the beginning of the thesis to understand the following design concept. The design of the individual components of the circuit are outlined followed by the presentation of this particular implementation. Next the components are separately simulated prior to the whole test structure. Simulation results are used to estimate the measurement accuracy of the design. The actual measurements performed to evaluate the circuit are given next. A summery, a concluding discussion and proposed future works finalize the thesis.

Chapter 2

Fundamentals

Prior to the discussion of the test structure principle knowledge on parasitic current sources in an integrated circuit (IC), current measurement and properties of selected integrated devices are presented. In this progress terms used throughout this thesis are outlined.
The origin and impact of leakage currents is presented first. This covers a brief discussion on carrier movement and device physics. This is followed by an outline on the importance of leakage current for ICs.
Current measurement methods and their limitations are highlighted next. Basic relations between current and voltage for different electronic devices are presented and their applicability investigated.
The wafer test environment and its measurement capabilities are presented. They define the requirements for the design such as the allowed output quantities and minimal drivable current.
A literature research on published test structures is given. This includes the utilized measurement methods and the encountered problems for these test structures. The basic conditions for these circuits are discussed as they have a high impact on the design concept.
A review on integrated devices and the fabrication process concludes this chapter.

2.1 Leakage Current

Each non-ideal current flowing into a terminal of a device can be regarded as a leakage current. Integrated semiconductor devices, e.g. diode, resistors, field-effect transistors (FETs), bipolar junction transistors placed in silicon are fabricated on the same substrate. This is contrary to discrete electronics where each device is packaged separately. The junctions between the substrate and any other regions are reverse biased for proper operation. The reverse bias causes a reverse current called leakage current. The most prominent of this currents is the p-n-junction leakage current. The Shockley equation 2.1 gives the current I flowing through a diode [7].

$$I = J_s \cdot A \cdot \left(e^{\frac{q \cdot V}{m \cdot k_B \cdot T}} - 1 \right) \tag{2.1}$$

where A is the junction area, V the applied forward bias voltage, m the ideality factor or quality factor, q the elementary charge, k_B the Boltzmann constant, T the absolute temperature and J_s the saturation current density. The latter is determined by [7]

$$J_s = q \cdot \frac{D_p}{L_p} \cdot p_{n0} + q \cdot \frac{D_n}{L_n} \cdot n_{p0}$$
$$J_s = q \cdot n_i^2 \cdot \left(\frac{D_p}{L_p \cdot N_D} + \frac{D_n}{L_n \cdot N_A} \right)$$

where n and p are the carrier concentrations of electrons and holes. The index letter gives the region where the quantity is used, e.g. p_n is the minority hole density in the n region. The index 0 means the quantity at equilibrium. D is the diffusion constant and L the diffusion length. Both are indexed accordingly for electrons and holes. N_A and N_D are the doping concentrations for acceptors and donors. The intrinsic charge carrier density n_i is related to the hole and electron density at equilibrium, p_0 and n_0 by

$$n_i^2 = p_0 \cdot n_0$$

where $p_0 = N_A$ in the p-type and $n_0 = N_D$ in the n-type semiconductor.
The saturation current is determined by the doping concentrations and the minority charge carrier concentrations. A low leakage current device is heavily doped. Furthermore the saturation current is temperature dependent due to its relation to the minority charge carrier concentrations, the intrinsic charge carrier concentration n_i, and the diffusion constant as a function of temperature $D = f(T)$. This effect is usually more pronounced than the temperature dependency given in equation 2.1. The diode reverse current increases in an exponential manner with higher temperatures.
This exponential temperature dependency is utilized for devices with a small leakage current at room temperature. The temperature is increased and the current rises to a measurable value.
p-n-junction leakage current is not limited to diodes. It is encountered in various devices

utilizing reverse biased p-n-junctions, like transistors, well resistors and capacitors.
Besides p-n-junctions there are numerous other sources for leakage current. One worth mentioning is the gate leakage current of MOS transistors. Due to impurities in the oxide current can flow from the gate electrode to the drain, source and body terminals. An additional issue is encountered for very thin gate oxide used in modern process technologies. Charge carriers can tunnel through the barrier separating the gate from the substrate. Gate leakage current is especially interesting for storage cells. A higher gate leakage current means that cells have to be refreshed more often. Thus a transistor used in a storage cell is intended to have a low gate leakage current.

2.2 Current Measurement

Traditional measurement techniques convert the current into a voltage. Hence the discussion on current measurement focuses on current-voltage relations of different electric devices. More exotic current relations e.g. the one to the magnetic field strength **H**, etc. are omitted. These relations are not suitable for wafer test as they are either too time consuming, the necessary measurement equipment is not available or too expensive.
The three primitive electric components resistance R, capacitance C and inductance L are discussed. The current-voltage relations of each of them are investigated next.

2.2.1 Resistive Current Measurement

The commonly applied method for current measurement utilizes a resistor. Ohm's law gives the current-voltage relation of a resistor with resistance R as per equation 2.2.

$$v = R \cdot i \tag{2.2}$$

The resistance simply scales the current of interest i and converts it to a voltage v. This voltage is measured and the current calculated using the known resistance.
The lower bound of the current measurement range is therefore determined by the reverse function of equation 2.2.

$$I_{min} = \frac{V_{min}}{R_{max}} \tag{2.3}$$

The resistive measurement of a low current requires either a sensitive voltage measurement or a high resistance. These quantities are usually limited by some means. Voltage can be measured down to the μV-range under wafer test conditions with satisfying accuracy. A leakage current of several fA would therefore require a resistance in the MΩ-range. This resistor would take up too much area for an SLM test structure. Besides is the absolute value of integrated resistors inaccurate and noise of high resistance is an additional issue.

2.2.2 Inductive Current Measurement

The next device to be investigated is the inductor. They typically require a large area and their inductance L is difficult to reproduce with small deviations. Hence an inductor is not appropriate for current measurement in ICs. Furthermore their ideal current-voltage relation as presented in equation 2.4 is not suitable for stationary DC current measurement as no voltage drop is caused.

$$v = L \cdot \frac{di}{dt} \tag{2.4}$$

2.2.3 Capacitive Current Measurement

A capacitor is the most promising device for measuring low currents. It requires little area compared to the aforementioned resistor and inductor while being able to measure the current. The current-voltage relation of a capacitance C is derived next. The detailed discussion outlines the impact of several quantities on the measurement accuracy.
The terminal current of a capacitance is the change of stored charge Q over time t.

$$i = \frac{dQ}{dt} \tag{2.5}$$

The capacitance C relates the stored charge Q and the voltage v between the terminals of the capacitor.

$$Q = C \cdot v \tag{2.6}$$

Substituting the above relation in equation 2.5 gives

$$i = C \cdot \frac{\partial v}{\partial t} + v \cdot \frac{\partial C}{\partial t} \tag{2.7}$$

The capacitive current is not determined by the static absolute values of voltage and capacitance. It depends on the change of both quantities over time. While in most applications the change of capacitance with time can be neglected it is retained for further analysis in this thesis. It will become important when voltage-dependent capacitance is considered.
Before this delicate matter the basic properties of the simplified relation are discussed. Assuming a constant capacitance reduces equation 2.7 to

$$i = C \cdot \frac{dv}{dt} \tag{2.8}$$

The advantage of current measurement using a capacitor is determined by the above relation. Even a very low current flowing through an arbitrary large capacitance causes a

change in voltage over time. A given detectable difference in voltage Δv determines the required charging time Δt. Measurement accuracy of this method depends on accuracies of determining Δv, Δt and on the voltage dependence of the capacitor. In the ideal case of $C = const.$ the capacitance does not depend on the terminal voltages.
The impact of a capacitance change over time was outlined previously. Generally capacitances of integrated devices are voltage dependent. Examples are MOS-capacitors, polysilicon capacitors (PIP-capacitors), etc. As the voltage changes due to the charging of the capacitor also the capacitance varies over time. This causes a more complicated current-voltage relation. Substituting a voltage-dependent capacitance $C(v)$ in equation 2.6 and further on in 2.5 yields

$$i_C = \frac{C(v) \cdot v}{dt}$$

Solving the derivative results in

$$i_C = C(v) \cdot \frac{dv}{dt} + v \cdot \frac{dC(v)}{dt}$$

Applying the chain rule to the last derivative yields

$$i_C = C(v) \cdot \frac{dv}{dt} + v \cdot \frac{dC(v)}{dv} \cdot \frac{dv}{dt}$$

$$i_C = \left(C(v) + v \cdot \frac{dC(v)}{dv} \right) \cdot \frac{dv}{dt} \tag{2.9}$$

The current now also depends on the absolute voltage. Its influence is scaled by the change of capacitance with voltage.
Besides the capacitor used to convert the current into a voltage there are usually additional parasitic capacitances involved. They react in exactly the same way as the integrating capacitor does. This will be highlighted more detailed when discussing the available devices in section 2.5.

2.3 Measurement Environment

The circuit is designed to be probed by production test equipment. Thus there are certain constrains compared to laboratory equipment typically used for device characterization and circuit evaluation. The available equipment and the resulting constrains will be discussed in this section. These constrains have a major impact on the design process, as they define e.g. the minimal drivable current.
During wafer test measurements the wafer is at a constant temperature of $T_{Nom} = 27\,^{o}\mathrm{C}$. Thus the usual approach of heating the wafer and measure the increased leakage current

is not feasible.
The wafer is contacted using a probe card. This is basically a printed circuit board (PCB) with needles soldered onto it. Some probe cards come with additional components such as amplifiers or specialized measurement circuits. State of the art is using triax-cable and -wiring to the soldering joint. The guard shield prevents leakage currents. In this case the setup is limited by the switching matrix. It causes leakage currents and limits the current to values greater than 100 pA.
Measurement time is intended to be short. Although this is not a hard constrain for the design the measurement time has to be minimized.

2.4 Test structures

Literature offers multiple circuit designs for the measurement of low currents [1, 2, 3, 4, 5, 6]. Some aim to avoid a certain piece of measurement equipment [2, 3] or investigate other processes related to small currents [6]. However, most of them are designed to investigate a certain property of either a particular device or the current itself. This is a major difference to the goal of this thesis, where the DUT may be replaced by another kind of device.
This section briefly discusses the test structures presented in literature. Finding an approach for the circuit design is the target of this literature research. Therefore the given circuits are investigated for their usability in the upcoming test structure.

Girard *et al.* [2, 3] reported on a circuit capable of measuring low current and capacitance. The proposed circuit is printed in figure 2.1 and will be discussed further on.

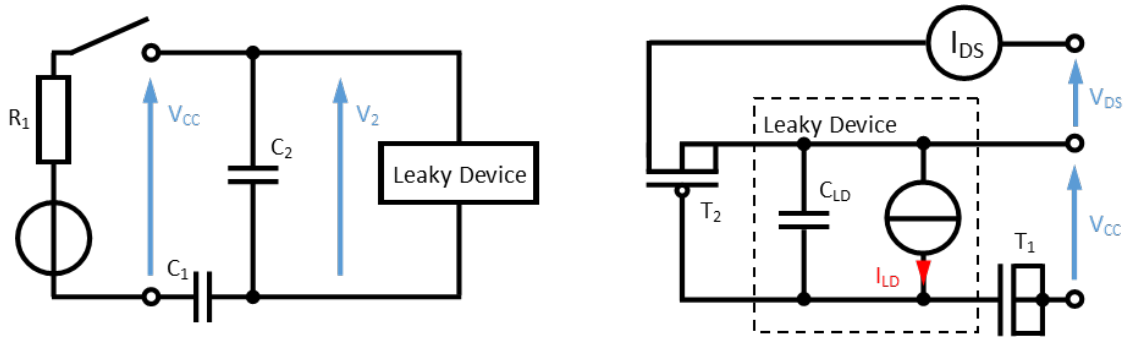

Figure 2.1: Left: Functional diagram of the circuit by Girard *et al.*. According to [2], page 93.
Right: Implementation of Girard *et al.* using MOS transistors. According to [2], page 94.

The leaky device on the left hand side of figure 2.1 is assumed to be a voltage-dependent capacitance $C_{LD}(V)$ and a current source I_L in parallel. Before the measurement all capacitors are discharged. At $t = 0s$ the supply voltage V_{CC} is applied by closing the switch. The voltage $V_2(t = 0s)$ is determined by

$$V_2(t = 0s) = V_{CC} \cdot \frac{C_1}{C_1 + C_2 + C_{LD}(V_2)}$$

The leakage current source I_L causes a decrease of voltage V_2. The initial slope of the voltage $dV_2/dt|_{t=0s}$ is recorded and used to calculate the current.

$$I_L(t) = \left[C_1 + C_2 + C_{LD}(V_2(t)) + V_2(t) \cdot \frac{dC_{LD}}{dV_2}\right] \cdot \frac{dV_2}{dt} \tag{2.10}$$

This formula is similar to equation 2.9 presented in the discussion on capacitive current measurement.
On the right hand side of figure 2.1 a suggested implementation by Girard *et al.* is printed. The capacitors are formed by the gate capacitance of MOS transistors. Besides transistor T2 is used to sense the slope of V_2. Similar structures for the high impedance detection of the voltage change are utilized in other papers [6, 4] as will be presented later.
The voltage dependency of C_{LD} is neglected and the modulation of the drain-source current I_{DS} by V_2 is determined by the linear regime of transistor T2 [2].

$$I_L(t) = (C_1 + C_2 + C_{LD}) \cdot \frac{dV_2(t)}{dI_{DS}(t)} \cdot \frac{dI_{DS}(t)}{dt}$$
$$\frac{dV_2(t)}{dI_{DS}(t)} = \frac{L}{\mu \cdot C_{ox} \cdot W \cdot V_{DS}}$$

The last equation can be obtained by the drain source current equation for the linear regime [2, 7].
In their latter work Girard *et al.* obtained the capacitance variation versus bias by applying different supply voltages V_{CC} [3].

$$C_{ld(atV_2=V_{2i})} = C_1 \cdot \left[\frac{V_{CC}}{V_{2i}} - \left(1 + \frac{C_2}{C_1}\right)\right] \tag{2.11}$$

where V_{2i} is the initial ($t = 0s$) value of V_2. Hence the approximation of a constant capacitance C_{LD} is no longer required and equation 2.10 can be used.
The circuit of Girard *et al.* seems promising for an implementation in an SLM. Two transistors are sufficient to measure the leakage current. The layout can be altered to be applied to high-side and low-side DUTs. Unfortunately the recorded voltage slope dV_2/dt also changes the voltage at the DUT. The resulting change in current has to be negligible. This limits the method to high impedance DUTs. For low impedance DUTs a different structure for the voltage slope generation has to be used. However, the detection of the voltage slope by a high impedance amplifier is a powerful solution.
In their latter work Girard *et al.* implemented a simultaneous measurement of the capacitance [3]. The idea of measuring the current and capacitance at the same time is retained and used for the test structure to come. This offers the possibility to replace existing test structures for capacitance measurement.

A similar test structure was used by Matsuda to investigate the relation between capacitor shape and its leakage current and capacitance [6]. The operating mode of the sensing transistor T2 has been altered. While Girard *et al.* used the linear regime Matsuda utilized the sub-threshold region and the exponential relation of the weak inversion drain-source current to the gate voltage. Thus a smaller change in voltage is needed and the requirement for a high impedance DUT is eased.

Inatsuka *et al.* developed another test structure, which employs a common gate circuit to block the DUT from the voltage swing at the capacitor [4]. The circuit schematic is shown in figure 2.2.

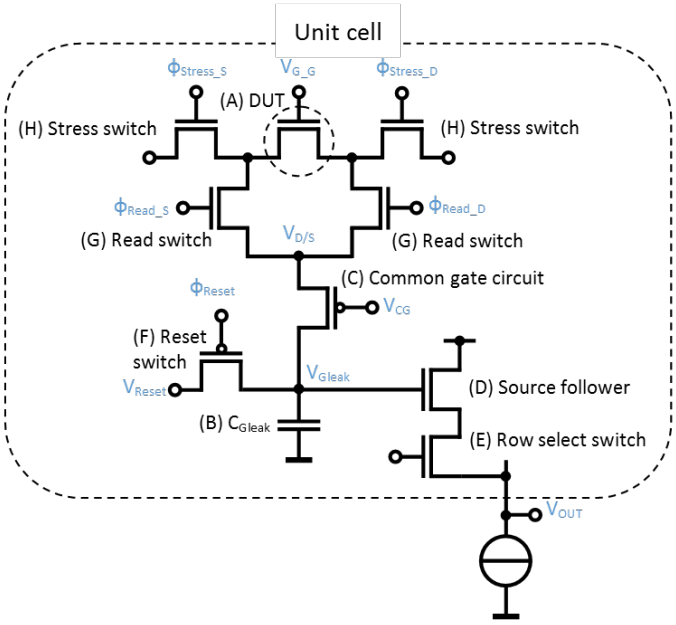

Figure 2.2: Test structure by Inatsuka *et al.*. According to [4], page 3.

The transistor marked with (C) is the common gate device. It stabilizes the potential at the DUT (A) while the voltage V_{Gleak} at the capacitor (B) is changing. The transistors (G) are the read switches. They are used to connect the DUT to the measurement circuit. The stress switches marked with (H) are used to apply a high voltage to the gate oxide of the DUT. The voltage across the capacitor (B) is sensed by a source follower (D) similar to [2]. After a measurement cycle the voltage is reset by the transistor (F). The row select switch (E) is used to address the circuit in an array of identical unit cells.
The measurement is done in two stages. First the background current I_{BG} composed of the leakage currents of the devices in the circuit is recorded. The DUT is unbiased by applying 0 V to the gate contact V_{G_G} in this process. The second part is the measurement of I_{Total} while the DUT is biased. This current comprises the leakage current of the DUT and the parasitic ones from all other devices. Finally the current of interest is calculated by the difference $I_{Gleak} = I_{Total} - I_{BG}$.

Each of the aforementioned designs assume a highly precise and well known capacitance. This devices usually suffer from strong variations on a typical production wafer. Mismatch

between two capacitors and deviation from the nominal value are as large as 20 %. A measurement method has to be found, where either the current is independent of the capacitance or can be eliminated in the equation. Another solution is the determination of the capacitance prior or simultaneous with the leakage current measurement.

2.5 Process Technology

The test structure is fabricated in a 0.35 μm CMOS process. This process is used for p-type doped substrates. An additional constraint is the re-usability of the test structure design in different processes modules. Therefore devices available in most process families are used and the number of metal layers is reduced to a maximum of three.
First the influence of device geometry on properties of integrated components is presented. This is followed by a review of selected integrated devices.

2.5.1 Device Geometry

Integrated devices are despite their 2D-appearance in CAD programs three-dimensional. The layout of an integrated device is printed in figure 2.3 to clarify the dimension notation.

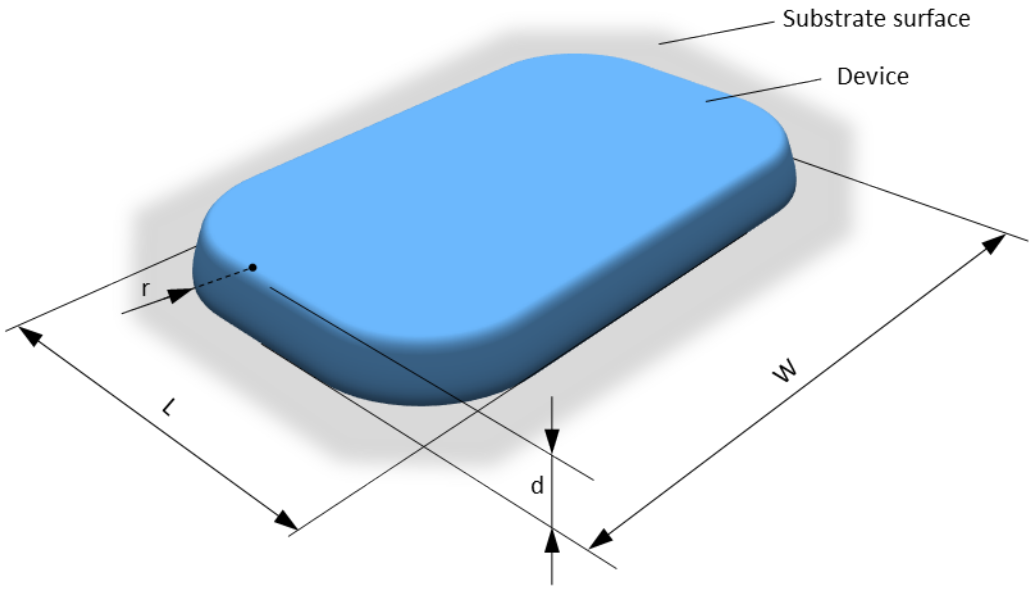

Figure 2.3: Geometry of an integrated device on top of the substrate surface. The same dimensions are used for devices integrated inside the silicon.

Designers are able to set the top surface size via the width W and length L only. The thickness d and corner radius r are determined by the process and the device. Hence the device properties are usually reduced to an area and a perimeter component. A generic property P of a device is the sum of its area P_A and perimeter component P_P.

$$P = P_A + P_P \tag{2.12}$$

The area and perimeter property can be represented by the device dimension W and L and the specific value p. For a rectangular device the area and perimeter components can be written as

$$P_A = W \cdot L \cdot p_A$$
$$P_P = 2 \cdot (W + L) \cdot p_P$$

Two devices with equal area do not have the same properties in general. The perimeter component has to be accounted for.
For a full characterization at least two devices with different dimensions are required. Commonly one has a high aspect radio W/L to raise the perimeter component P_P over the area component P_A.
More advanced models consider the impact of corners and the overall device shape. A more detailed discussion is omitted, as it is beyond the scope of this thesis.

2.5.2 Capacitor

Capacitors are crucial components and can be integrated in various ways. Each type has its own benefits and drawbacks. This review focuses on the integration capacitance used for the current-voltage conversion. Hence properties such as voltage dependency of the capacitance are primarily highlighted. The most prominent kinds of capacitors used in ICs are discussed in the sections to come.

Junction Capacitor

The junction capacitor is the junction capacitance of an ion implanted or diffused tub (well). A exemplary cross-section is given in figure 2.4.

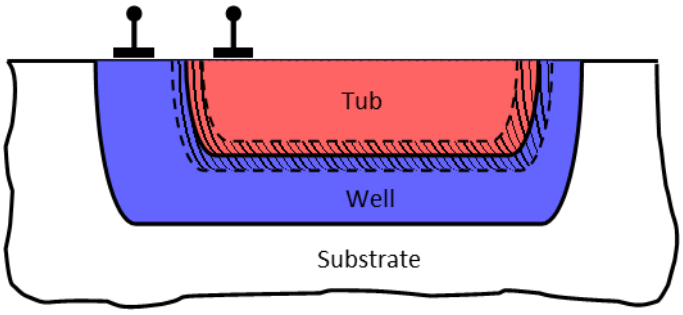

Figure 2.4: Cross-section of a junction capacitor (shaded area) in a well.

The capacitance is determined by the width of the depletion layer thickness and therefore changes with the applied voltage. According to Sze the capacitance for a one-sided abrupt junction equals [7]

$$C = \frac{dQ_c}{dV} = \sqrt{\frac{q \cdot \epsilon \cdot N_B}{2 \cdot (V_{bi} + V_r - 2 \cdot k_B \cdot T/q)}} \tag{2.13}$$

where V_{bi} is the build-in voltage, V_r the reverse bias voltage and N_B the lower doping concentration given as

$$N_B = \frac{N_A \cdot N_D}{N_A + N_D} \approx \begin{cases} N_D & \text{if } N_A >> N_D \\ N_A & \text{if } N_D >> N_A \end{cases}$$

The discussion on voltage-dependent capacitance was given in section 2.2.3. The change of capacitance over voltage dC/dv is usually unknown because of arbitrary doping profiles and has to be measured for device characterization and modeling.

MOS Capacitor

This capacitor is formed by the gate to silicon capacitance as pictured in figure 2.5. The gate as used in a MOSFET forms the top plate of the capacitor. The underlying silicon is heavily doped and acts as the bottom plate. The heavy doping enhances conductivity and reduces the parasitic resistor.

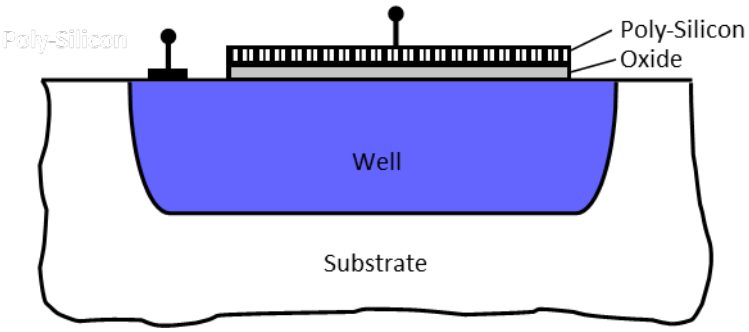

Figure 2.5: Cross-section of a MOS capacitor.

The connection of this kind of capacitor is crucial. The bottom plate has to be connected to a stable potential. Otherwise the depletion width to the substrate changes and hence the parasitic capacitance. Besides the voltage swing at the bottom plate is limited. Its potential must not forward bias the junction to the substrate.
The voltage across the capacitance is also limited. A high voltage damages the oxide and alters the properties of the capacitor such as capacitance and leakage current.

Poly-Insulator-Poly Capacitor

The poly-insulator-poly (PIP) capacitor is an extension of the MOS capacitor. Above the first poly-silicon plate a second one is deposited. Thus a triple layer structure is obtained as given in figure 2.6.

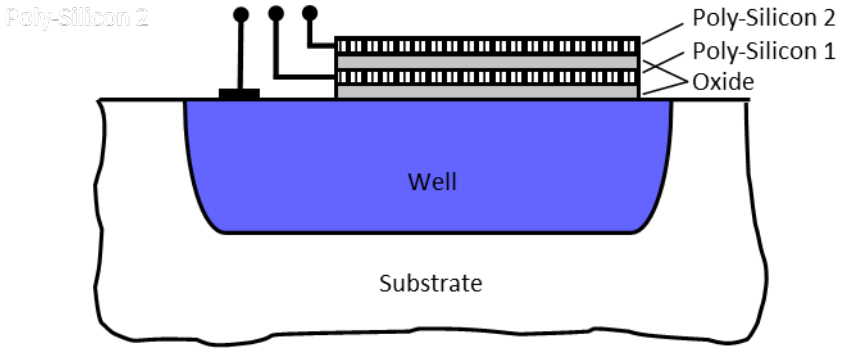

Figure 2.6: Cross-section of a poly-insulator-poly capacitor.

The two poly-silicon plates are used as the capacitor. Besides there is a parasitic capacitor between the bottom plate and the underlying well. This is basically the same structure as the MOS capacitor although the thicker field oxide is used. The impact of this parasitic capacitor can be eliminated if the potential between the bottom plate and the well is constant.

Metal-Insulator-Metal Capacitor

The metal-insulator-metal (MIM) capacitor is built up by two metal layers. The parasitic capacitance to the silicon is lowered compared to the PIP capacitor. Different realizations of MIM capacitors are available. An exemplary structure with the MIM capacitor placed in the inter-layer dielectrics (ILD) is presented in figure 2.7.

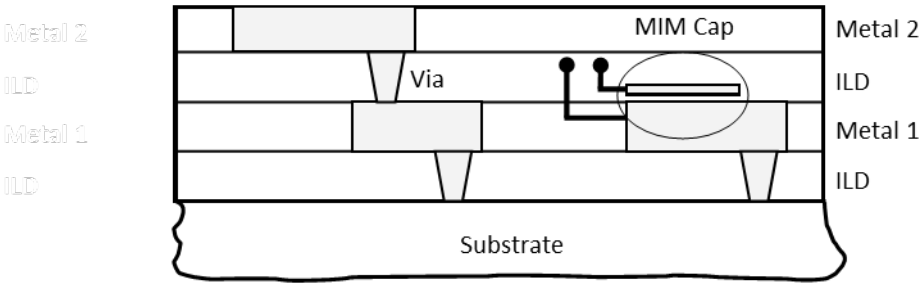

Figure 2.7: Cross-section of a metal-insulator-metal capacitor. The metal plates forming the capacitor are placed in the ILD for this example.

2.5.3 Transistors

The most essential device used in ICs is the Metal-Oxide-Semiconductor (MOS) transistor. Further on transistor refers to a MOS transistor, despite there are numerous variants available. A cross-section along its length is shown in figure 2.8.

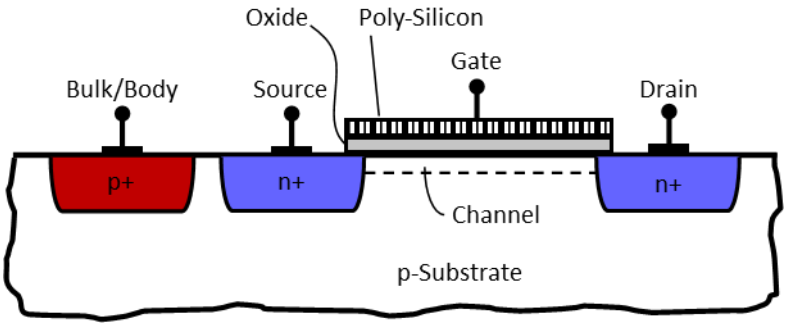

Figure 2.8: Cross-section of an n-type metal-oxide-semiconductor (MOS) transistor. A thin insulating oxide separates the poly-silicon gate from the channel inside the semiconducting p-doped substrate. The potential at the gate enables the control on the channels conductivity. The source and drain diffusion are visible on the left and right hand side of the channel. The substrate is connected by the bulk or body contact.

A transistor can be operated in different regimes depending on the gate-source voltage V_{GS}, the drain-source voltage V_{DS} and the threshold voltage V_{th}. The drain current I_D is given according to the Shichman-Hodges model to study the operation modes [8]. Besides is the body effect omitted for the illustration of the transistor operation and its basic current-voltage relations.
The transistor is turned off or in sub-threshold operation for a gate-source voltage V_{GS} smaller than the threshold voltage V_{th}. The drain current I_D exhibits an exponential behavior with gate-source voltage V_{GS}.

$$I_{D,sub-th} \approx \frac{W}{L} \cdot I_{D0} \cdot e^{\frac{q \cdot (V_{GS} - V_{th})}{n \cdot k_B \cdot T}} \tag{2.14}$$

where W is the gate width and L the gate length. I_{D0} is the drain current at $V_{GS} = V_{th}$ normalized by W/L and n is the slope factor. The latter is related to the gate oxide capacitance per unit area C_{ox} and the capacitance of the depletion layer C_D by

$$n = 1 + \frac{C_D}{C_{ox}}$$

The transistor operates in the linear mode if the gate-source voltage V_{GS} exceeds the threshold voltage V_{th} while the drain-source voltage V_{DS} is smaller than $V_{GS} - V_{th}$. The drain current I_D is given by

$$I_{D,lin} = \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot \left(\left(V_{GS} - V_{th}\right) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right) \tag{2.15}$$

where μ is the charge carrier mobility. For small drain-source voltages the last term can be neglected.

$$I_{D,lin} = \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot \left(V_{GS} - V_{th}\right) \cdot V_{DS} \tag{2.16}$$

The drain current shows a resistive dependency over the drain-source voltage. The resistance can be controlled by the gate-source voltage.
The saturation regime is reached by increasing the drain-source voltage V_{DS} from the linear regime until it exceeds $V_{GS} - V_{th}$. The channel is pinched-off at the drain. This changes the current relation to

$$I_{D,sat} = \frac{\mu \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot \left(V_{GS} - V_{th}\right)^2 \cdot \left[1 + \lambda \cdot \left(V_{DS} - V_{DSsat}\right)\right] \tag{2.17}$$

where λ is the channel-length modulation factor. It determines how the effective channel length is affected by the drain voltage. It is usually approximated to be inversely proportional to the gate length L.

$$\lambda \approx \frac{1}{L} \tag{2.18}$$

The operation modes, the voltage relations and the drain current I_D according to a simple model are collected in table 2.1.

Table 2.1: Transistor operation modes and current relations as a function of terminal voltages.

Turned off (Sub-threshold)	Linear	Saturation
$V_{GS} < V_{th}$	$V_{GS} > V_{th}$ $V_{DS} < V_{GS} - V_{th}$	$V_{GS} > V_{th}$ $V_{DS} > V_{GS} - V_{th}$
$I_{D,sub-th} \sim e^{\frac{q \cdot (V_{GS} - V_{th})}{n \cdot k_B \cdot T}}$	$I_{D,lin} \sim \frac{W}{L} \cdot \left(V_{GS} - V_{th}\right) \cdot V_{DS}$	$I_{D,sat} \sim \frac{W}{L} \cdot \left(V_{GS} - V_{th}\right)^2$

An important quantity for a transistor is its transconductance g_m. The higher the transconductance the more sensitive is the drain current to a change in gate-source voltage. It is defined as the derivative of drain current I_D over gate-source voltage V_{GS}. Thus the transconductance of a transistor operated in saturation mode equals

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{2 \cdot I_D}{V_{GS} - V_{th}} \sim \frac{W}{L} \tag{2.19}$$

According to equation 2.19 the transconductance can be increased by forcing more current through the transistor or increase the gate-source voltage, respectively. Note that the drain current is proportional to the square of the difference between gate-source and threshold voltage. Furthermore is drain current proportional to the device dimension ratio W/L as per equation 2.17. Thus the transconductance is also proportional to the gate width W and inversely proportional to the gate length L.
The output conductance g_{ds} give the change of drain current I_D on a variation in drain-source voltage V_{DS}. For a transistor in saturation mode it is calculated by

$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}} = \lambda \cdot I_D \tag{2.20}$$

Substituting equation 2.18 into 2.20 yields

$$g_{ds} = \frac{1}{r_o} \approx \frac{I_D}{L} \tag{2.21}$$

where r_o is the output resistance. The output conductance g_{ds} of a transistor in saturation mode can be increased by either increasing the drain current I_D or decreasing the gate length L.

The transistors available in the process option are of major impact on the design. Insulated transistors allow operation of FETs beyond V_{SS} because transistor bodies are insulated to substrate. High-voltage devices are needed for designs utilizing higher supply voltages. The process chosen for the design of the test structure offers no special type of MOS transistors. Therefore the standard transistor supply voltage limit is $V_{DD} = 3.3\,\mathrm{V}$.
The drain/source to substrate junction leakage current of the transistor is proportional to its width W as the junction area increases. Besides this leakage current there is also a capacitive component to the current. The depletion layer forms a capacitor as mentioned in section 2.5.2 which has to be charged on change in voltage. These capacitive components are especially important for a transistor along the DUTs leakage current path.

Chapter 3

Circuit Design

Previously the fundamentals for this thesis were discussed, including sources of leakage current and measurement principles. Published test structures for measurement of small currents were presented as well as the process used to fabricate the SLM test structure.
This chapter covers the design process of the circuit for the SLM test structure. The concept orientates on test structures from literature. The concept is outlined in a top-down manner. First a presentation of the whole circuit concept is given. The individual circuit components are discussed separately afterward. This chapter presents the design in a general manner. The actual implementation is given in the next chapter.
Connection and communication of the test structure with the external measurement environment is discussed as a conclusion for this chapter.

3.1 Circuit Concept

The measurement method of choice is recording the voltage slope on a capacitor caused by the leakage current of interest. The voltage slope itself can be determined in two ways. Either one measures a fixed amount of time and evaluates the change in voltage, or records the time the voltage takes to reach a certain potential. In both cases the differential dv/dt is approximated by the relation of voltage change Δv to the difference in time Δt.

$$\frac{dv}{dt} \approx \frac{\Delta v}{\Delta t} \tag{3.1}$$

This is viable if the voltage slope is constant, i.e. the curvature or second derivative with respect to time $d^2v/dt^2 \cong 0\,\mathrm{V/s^2}$. This is not true in general. An example was already encountered in section 2.2.3. Solving equation 2.9 for the voltage slope gives

$$\frac{dv}{dt} = \left(C(v) + v \cdot \frac{dC(v)}{dv} \right)^{-1} \cdot i_C$$

Deriving this equation on more time does not yield a curvature of $0\,\mathrm{V/s^2}$. In order to reduce the error caused by the approximation the change of capacitance with voltage has to be negligible. Thus the bracket in the above equation reduces to C and the curvature is determined by the change in leakage current di_C/dt only. For a non-zero curvature of voltage the accuracy can be improved by minimizing the difference in voltage Δv and time Δt. Hence the measurement must be as short as possible. But as the approximations error decreases the uncertainty in voltage measurement increases due to the smaller change in voltage. Thus there is a trade-off in the measurement time.
As mentioned previously the voltage slope can be determined by either measuring a fixed interval of time or wait until the voltage reaches a certain potential.
The fixed time method measures the voltage change after a predefined period. A decrease in current also means a reduced voltage difference. When this difference becomes too small the measurement time must be adapted. In order to change the measurement time at least some information on the leakage current is required.
The fixed voltage method on the other hand simply alters its measurement time on a change in current inherently.
For the test structure the latter is chosen, because the DUT has to be interchangeable. Thus even for a change in current over decades the measurement settings can be retained. However, the measurement will take very long for small leakage currents.
Hence the quantity measured is the integration time Δt. This is the time it takes to (dis)charge the capacitance and for the voltage to pass a certain potential interval.
The difference in voltage can be easily determined by two comparators. Both compare the voltage on the integration capacitor with a constant pass voltage. One has a higher pass voltage V_{Ph}, the other a lower one V_{Pl}. The difference between the pass voltages equals Δv.

$$\Delta v = V_{Ph} - V_{Pl} \tag{3.2}$$

Once the voltage on the integration capacitor reaches the pass voltage the comparator output changes. The voltage changes further until it passes the second pass voltage. A simple logic circuit suffices to detect and process the two comparator signals.

Girard *et al.* used their circuit to simultaneously measure the current and capacitance [2, 3]. This idea is reused for the SLM test structure. Contrary to Girard *et al.* not the capacitance of the leaking devices is measured but the one of the integration capacitor. Although two different devices are measured at the same time, the leaking device is further on referenced as DUT.
At first the combination of two different DUTs (D_1 and D_2) and capacitors (C_1 and C_2) is examined. Thus four different combinations are viable. The leakage currents I_{D1} and I_{D2} for each of the combinations are determined by

$$
\begin{aligned}
I_{D1} &= C_1 \cdot \frac{\Delta v}{\Delta t_1} \\
I_{D1} &= C_2 \cdot \frac{\Delta v}{\Delta t_2} \\
I_{D2} &= C_1 \cdot \frac{\Delta v}{\Delta t_3} \\
I_{D2} &= C_2 \cdot \frac{\Delta v}{\Delta t_4}
\end{aligned}
$$

In order to reduce the time one measurement takes the voltage slope $\Delta v/\Delta t$ has to be increased. This is achieved by an amplifier with gain G. The four equations above combined with the gain can be written in a matrix notation

$$
\underbrace{\begin{bmatrix}
1 & 0 & -G \cdot \frac{\Delta u}{\Delta t_1} & 0 \\
1 & 0 & 0 & -G \cdot \frac{\Delta u}{\Delta t_2} \\
0 & 1 & -G \cdot \frac{\Delta u}{\Delta t_3} & 0 \\
0 & 1 & 0 & -G \cdot \frac{\Delta u}{\Delta t_4}
\end{bmatrix}}_{\mathbf{A}} \cdot \underbrace{\begin{pmatrix} I_{D1} \\ I_{D2} \\ C_1 \\ C_2 \end{pmatrix}}_{\mathbf{x}} = \underbrace{\begin{pmatrix} 0 \\ 0 \\ 0 \\ 0 \end{pmatrix}}_{\mathbf{b}} \tag{3.3}
$$

This is a homogeneous system of equations, since the constant vector $\mathbf{b}$ is the null vector. The trivial solution is both currents and capacitance to be 0 or $\mathbf{x} = 0$. The existence of further solutions is determined by the matrix $\mathbf{A}$. A system with a non-singular matrix, i.e. the matrix has a non-zero determinant, has the null solution only. A singular matrix leads to an infinite number of solutions.
The determinant of the matrix $\mathbf{A}$ equals

$$
|\mathbf{A}| = \begin{vmatrix}
1 & 0 & -G \cdot \frac{\Delta u}{\Delta t_1} & 0 \\
1 & 0 & 0 & -G \cdot \frac{\Delta u}{\Delta t_2} \\
0 & 1 & -G \cdot \frac{\Delta u}{\Delta t_3} & 0 \\
0 & 1 & 0 & -G \cdot \frac{\Delta u}{\Delta t_4}
\end{vmatrix} = \frac{\Delta u}{\Delta t_1} \cdot \frac{\Delta u}{\Delta t_4} - \frac{\Delta u}{\Delta t_2} \cdot \frac{\Delta u}{\Delta t_3}
$$

The ratio between two integration times is determined by the ratio between the leakage currents or capacitance. Two leakage currents with $I_2 = c \cdot I_{D1}$ leads to $\Delta t_3 = \Delta t_1/c$ and $\Delta t_4 = \Delta t_2/c$, where c is an arbitrary positive non-zero constant. The determinant becomes

$$|\mathbf{A}| = \frac{\Delta u}{\Delta t_1} \cdot \frac{c \cdot \Delta u}{\Delta t_2} - \frac{\Delta u}{\Delta t_2} \cdot \frac{c \cdot \Delta u}{\Delta t_1} = 0$$

Thus the matrix is singular and there are an infinite number of solutions.
In order to obtain a unique solution for the leakage current and capacitance a non-zero constant vector $\mathbf{b}$ has to be created. This requires a known quantity to be introduced into the system. One of the lines in the above system is replaced with an external defined equation. Using a constant external current to charge one of the capacitors gives for the fourth equation

$$I_e = C_2 \cdot G \cdot \frac{\Delta v}{\Delta t_e}$$

The capacitor C_2 is chosen arbitrarily and the index e stands for external.
By replacing the fourth line the modified system of equations becomes

$$\begin{bmatrix} 1 & 0 & -G \cdot \frac{\Delta u}{\Delta t_1} & 0 \\ 1 & 0 & 0 & -G \cdot \frac{\Delta u}{\Delta t_2} \\ 0 & 1 & -G \cdot \frac{\Delta u}{\Delta t_3} & 0 \\ 0 & 0 & 0 & +G \cdot \frac{\Delta u}{\Delta t_e} \end{bmatrix} \cdot \begin{pmatrix} I_{D1} \\ I_{D2} \\ C_1 \\ C_2 \end{pmatrix} = \begin{pmatrix} 0 \\ 0 \\ 0 \\ I_e \end{pmatrix} \tag{3.4}$$

The basic concept is set with the system of equations 3.4. The integration times Δt are measured and the system of equations is solved for leakage currents and capacitances. These components which were mentioned during the development of this concept will now be briefly summarized.
The conversion from a current to a voltage slope is performed by the front stage. An amplifier reduces the time one measurement takes. A pair of comparators detects when the voltage on the integration capacitor passes two defined potentials. The output signals of the comparators are processed by a simple logic circuit. Additionally it resets the capacitor voltages and sets the switches to connect a certain diode and capacitor. A functional diagram is pictured in figure 3.1.

3.2 Front Stage

The design of the front stage orientates on the circuit proposed by Inatsuka *et al.* [4]. Their circuit is shown in figure 2.2 and implements a number of devices which can be omitted for the SLM test structure. The SLM of this thesis is not used for stress investigations. Besides the DUTs are not structured in an array as the area of an SLM is limited. Thus the row select switch (E), read switches (G) and stress switches (H) can be removed. This

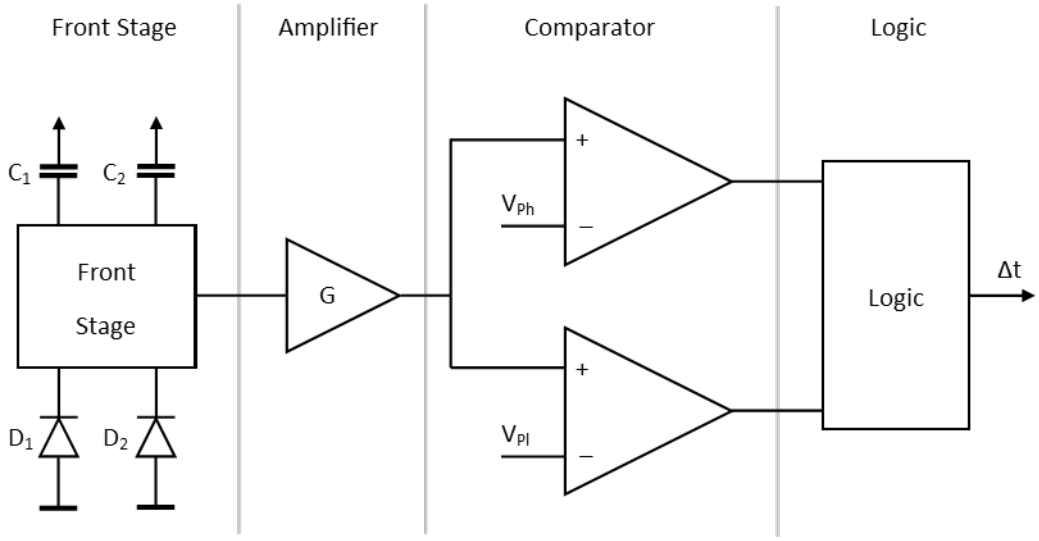

Figure 3.1: Functional diagram of the concept with the individual circuit components.

leaves a reduced circuit to start from.
The DUT in figure 2.2 is connected to the positive supply. Some DUTs feature terminals which are hard-wired to the substrate. The substrate is p-doped for the processes discussed in this thesis. In order to measure such DUTs with one contact fixed to the p-substrate the circuit of Inatsuka *et al.* has to be mirrored. Figure 3.2 illustrates the principle front stage circuit for the SLM test structure. Each DUT is built into a separate front stage. The logical signals **reset**, **swC1** and **swC2** are detailed in section 3.5.

The front stage converts the DUT leakage current into a negative voltage slope. An exemplary front stage output voltage V_{FS} is printed in figure 3.3.

The integration capacitor must not exhibit a change in capacitance versus voltage, i.e. $C(v) = const.$ The integration time is proportional to the integration capacitance as given by the system of equations 3.4. In order to minimize the time the measurement takes a small capacitance is preferred. But the amplifiers bandwidth determines the lower bound for the capacitance. A small capacitance results in a steep slope which must be amplified with the very same gain G as a more gentle slope.
The most critical equation of the system 3.4 is usually the reference current I_e in the fourth line. The capacitor charged by the reference current must be sufficiently large for the voltage slope to match the amplifiers bandwidth. The second capacitor can be smaller. The larger capacitance must be set in conjunction with the amplifiers gain and bandwidth. The discussion on the gain-bandwidth-product (GBP) is given in the amplifier section 3.3.

The common gate transistor N_1 inhibits a voltage change on the DUT during measurement. This is especially important for a DUT with a low differential output resistor. Otherwise any change in bias voltage alters the leakage current.
A high transconductance g_m is required to efficiently control the bias of the DUT. According to equation 2.19 the ratio W/L has to be high as well. A small gate length L on the other hand increases the output conductance g_{ds} of the common gate transistor as given

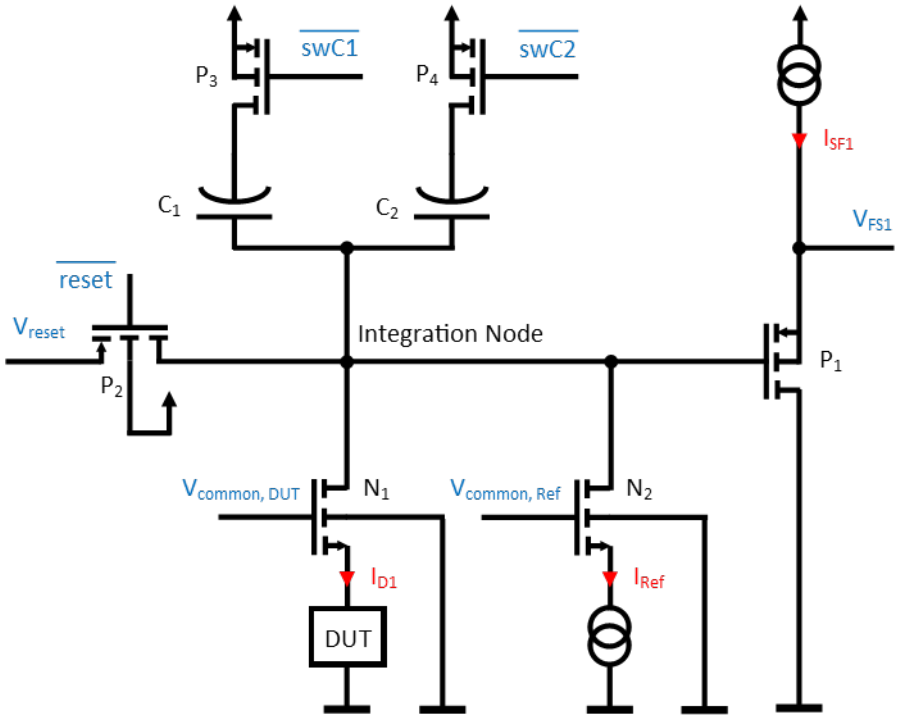

Figure 3.2: Design of the front stage adapted from Inatsuka *et al.* [4].

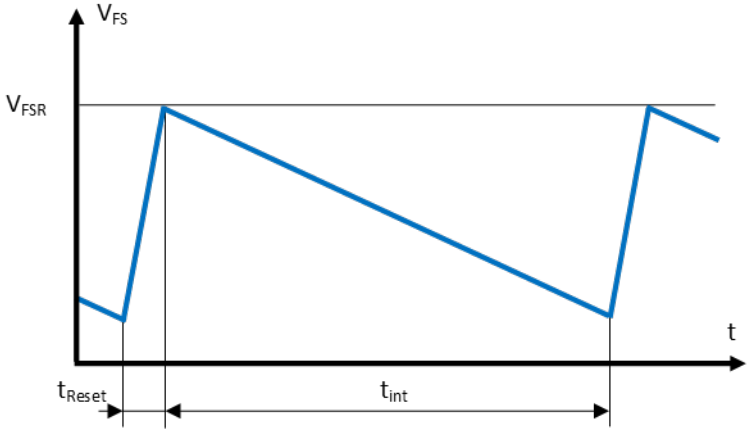

Figure 3.3: Schematic conversion from a current to a voltage slope in the front stage. During a measurement the voltage drops as the capacitance is discharged. The integration time Δt is a part of the shown time t_{int}. On a reset the capacitor is recharged and the voltage reaches its reset level V_{FSR}.

by equation 2.21. But a high output resistance is required to suppress the effect of the voltage change at the integration node on the DUT bias.
The current flowing into a transistor is larger for a wide device. The diffusions of source and drain feature a depletion layer capacitance. This capacitance has to be charged along

with the integration capacitor as they are connected in parallel. Hence the depletion capacitance has to be minimized. This can be done by decreasing the gate width W, which scales the whole device width.
Thus the transistors dimensions have to be set to achieve maximal control on the bias voltage of the DUT at minimum current leaking into the transistor. The common gate transistor can be omitted for high impedance DUTs and this parasitic current is eliminated.

The reset transistor recharges the integration capacitor and establishes the reset potential V_{FSR} at the integration node. The load on this transistor is minimal as it has to charge a high-impedance node. The critical quantity is its parasitic current drained from the integration node. Therefore the gate width W of the reset transistor has to be minimized. The length L can be increased to reduce sub-threshold current.

The transistors used to toggle the capacitor connected to the integration node are designed similar to the reset transistor. The main problem is their parasitic current. Thus their dimensions are minimized.

The source follower senses the voltage at the integration node. Its output voltage V_{FS} is basically the voltage at the integration node plus the gate-source voltage V_{GS}. Its gate capacitance is connected to the integration capacitor in parallel and must therefore be small. This requires a minimum for the gate width W and length L. This on the other hand decreases the transconductance g_m and control on the output voltage. Depending on the process the impact of the additional capacitance is negligible compared to the effect of poor output control. Thus the use of a slightly larger transistor for the source follower is justified.

3.3 Amplifier

The signal generated by the front stage is amplified to reduce the measurement time. This increases measurement throughput and improves the accuracy of the approximation for the voltage slope in equation 3.1. Before the amplifier design is presented its requirements have to be defined.
The input impedance must be high. Otherwise the load on the front stage source follower is too much and it will not work properly.
Usually one wants to have an amplifier with a high gain which is beneficial for accuracy and measurement time as mentioned before. But according to the gain-bandwidth-product (GBP) the bandwidth B decreases with increasing gain G. Therefore the gain is limited by the bandwidth B, which in turn is determined by the shortest measurement time and the highest measurable current, respectively. This is especially important for the reference current, which is usually high compared to the DUT current.
There are no special requirements for the amplifiers output. It is loaded with the input capacitance of the comparators and the feedback-loop. Both can easily be driven by the amplifier.

The type of amplifier (i.e. single- or differential-input) used is also determined by the front

stage. The output potential of the front stage during reset V_{FSR} changes due to process variations. It does not change over time, but from test structure to test structure. The amplifier must be able to handle this not well defined potential. The output potential of the front stage V_{FS} can be written as the sum of the ideal potential $V_{FS,i}$ plus its deviation ΔV_{FS}. Applying the gain the output voltage of the amplifier V_A is given by

$$V_A = G \cdot V_{FS} = G \cdot V_{FS,i} + G \cdot \Delta V_{FS}$$

The second addend of the above equation means the comparators shifts the starting point of the voltage slope. The comparator lower pass voltage has to be higher than this potential for each test structure. This results in comparator pass voltages close to the positive supply voltage. Depending on the input stage this may influence their sensitivity.
The impact of the process variation can be eliminated by using a differential-input amplifier as pictured in figure 3.4.

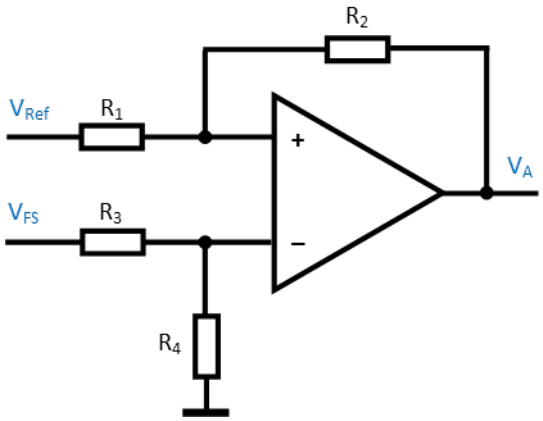

Figure 3.4: First circuit for the amplifier.

The output voltage of the amplifier is given by

$$V_A = G \cdot (V_{Ref} - V_{FS})$$

The reference input voltage V_{Ref} is set slightly lower than the minimal front stage output potential $V_{FS,i} - \Delta V_{FS}$. Hence the amplifiers output voltage is $\approx 0\,\mathrm{V}$ at the beginning of the measurement. If the reference input voltage is chosen properly this is true even for the worst case process variation.
But for the required high input impedance of the amplifier the resistors are very large and not suitable for an SLM. An instrumentation amplifier is also not viable. Its two extra operational amplifiers (OPAMPs) require too much area.
The amplifier used for the test structure comes from Tietze and Schenk [9] and is printed in figure 3.5. Its inputs are directly connected to the gate contacts of two MOS transistors ensuring a high input impedance.

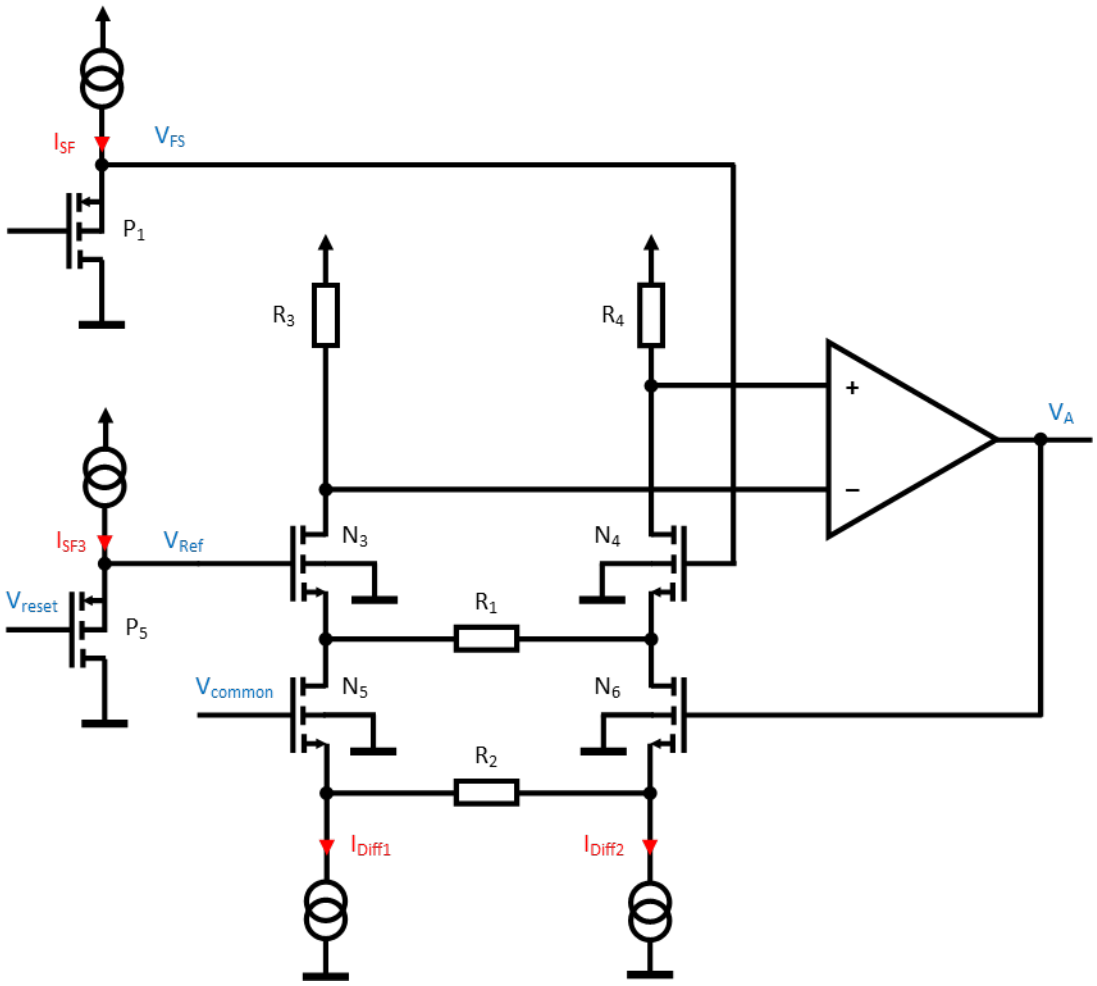

Figure 3.5: Design of the amplifier adapted from Tietze & Schenk [9]. The source follower of the front stage and the reference voltage are visible on the left hand side.

A difference in the input voltages causes a current flow through the resistor R_1. The current mirror on the low side of the input stage ensures the same current in both branches. Thus the current has to flow through resistor R_2 to obtain equality in current flow. As R_2 is greater than R_1 the caused voltage drop is larger as well. The feedback loop sets the output voltage in a way to redirect the current through resistor R_2.
The output voltage is determined by

$$V_A = \frac{R_2}{R_1} \cdot (V_{Ref} - V_{FS}) + V_{Common}$$

The ratio between the two resistors equals the gain.

$$G = \frac{R_2}{R_1} \tag{3.5}$$

The resistors R_1 and R_2 determine the gain as given by equation 3.5. But there are some constrains for the resistance. They are given by the GBP as mentioned at the beginning of this section. The highest current (usually the reference current) forced into the integration capacitance results in the shortest measurement time. Hence there is a minimum bandwidth while the GBP is determined by the OPAMP. This results in a maximum gain of

$$G_{max} = \frac{GBP}{B}$$

Besides the bandwidth can not be fully exploited. The measurement result is directly related to the gain, which is decreased by a factor of $1/\sqrt{2}$ at the corner frequency. Thus the bandwidth of the amplifier has to be higher than required by the reference current source.

3.4 Comparator

The comparator tells the logic when the amplifier output voltage V_A is in between the lower V_{Pl} and higher pass voltage V_{Ph}. The difference between higher and lower pass voltages gives Δv per equation 3.2. Thus for a short measurement time this difference has to be as small as possible. However the comparators do not perfectly change their output when the input voltage reaches the pass voltage. Instead they toggle their output signals in an interval around the ideal switching point. This introduces an error in Δv and consequently in the measurement result. The error introduced by the comparators is constant. Its significance can be reduced by the increasing the difference Δv. Denoting Δv by the sum of its ideal value Δv_i and the error δv gives

$$\Delta v = \Delta v_i + \delta v$$

For large Δv_i this can be approximated by $\Delta v \approx \Delta v_i$. This leads to a lower bound for the higher pass voltage V_{Ph}.

The comparator output signals **loComp** and **hiComp** for a typical amplifier output voltage over time are printed in figure 3.6 along with other signals of the logic. When the test structure is reset the amplifier output voltage drops with a limited slope. This will become important for the consecutive logic circuit.

3.5 Logic

Before discussing the design of the logic circuit a few terms are clarified. A signal is denoted in bold letters, e.g. **signal**. The inverted signal has a bar on top, e.g. $\overline{\textbf{signal}}$. The two possible states of a signal *low* and *high* are written italic. The logical And is denoted by a dot '.' and the logical Or by a plus '+'.

The output signals **hiComp** and **loComp** of the comparators are processed by the logic. In addition there are three signals coming from the external measurement equipment. The select signals **S0** and **S1** which determine the line of equation 3.4 to be recorded and an external reset signal **Reset**.
The logic has to generate the output signal and several control signals like the internal reset and switching signals. The required signals are

- **output**
- Internal **reset**
- Current source control signals **swD1**, **swD2** and **swRef**
- Capacitance control signals **swC1** and **swC2**

The control signals **swD1**, **swD2** and **swRef** determine which current source is used. **swD1** means DUT1 is active. Analog for **swD2** with DUT2 and **swRef** with the external reference current source.
In a similar fashion is the active capacitor selected by the capacitance control signals.

Figure 3.6 is a graphical representation of the signals **output** and **reset**. It is used to present the design process of the logic.

The internal **reset** is discussed first as it is reused for the other signals. **reset** must be set every time **hiComp** is *high* and hold its state until **loComp** returns to *low*. An RS-flip-flop is used to generate the **reset**. Its set signal $\mathbf{S_r}$ and reset signal $\mathbf{R_r}$ are

$$\mathbf{S_r} = \mathbf{hiComp}$$
$$\mathbf{R_r} = \overline{\mathbf{loComp}}$$

The external **Reset** offers the possibility to manually reset the test structure. This is done by combining the output signal of the RS-flip-flop $\mathbf{Q_r}$ with the incoming **Reset** by a logical Or operation.

$$\mathbf{reset} = \mathbf{Q_r} + \mathbf{Reset}$$

The **output** signal as presented in the concept section 3.1 is *high* while the amplifier output voltage is between the two pass voltages V_{Pl} and V_{Ph}. As mentioned in the previous section 3.4 the amplifier output voltage drops with a limited slope. Thus for a short time **hiComp** becomes *low* while **loComp** is still *high*. This would tell the logic that the structure is still integrating the DUT current. In fact the reset is applied to the test structure. This results in faulty behavior. A simple combination of **loComp** and **hiComp** would result in a glitch in **output** (dotted line in figure 3.6). In said time the **reset** is triggered. It is used to avoid the glitch.
An RS-flip-flop is used to obtain the **output** signal. Its set signal $\mathbf{S_o}$ is basically the **loComp**, which can be blocked if either the **hiComp** or **reset** are *high*. The reset signal $\mathbf{R_o}$ of the flip-flop is an OR-combination of **hiComp** and **reset**.

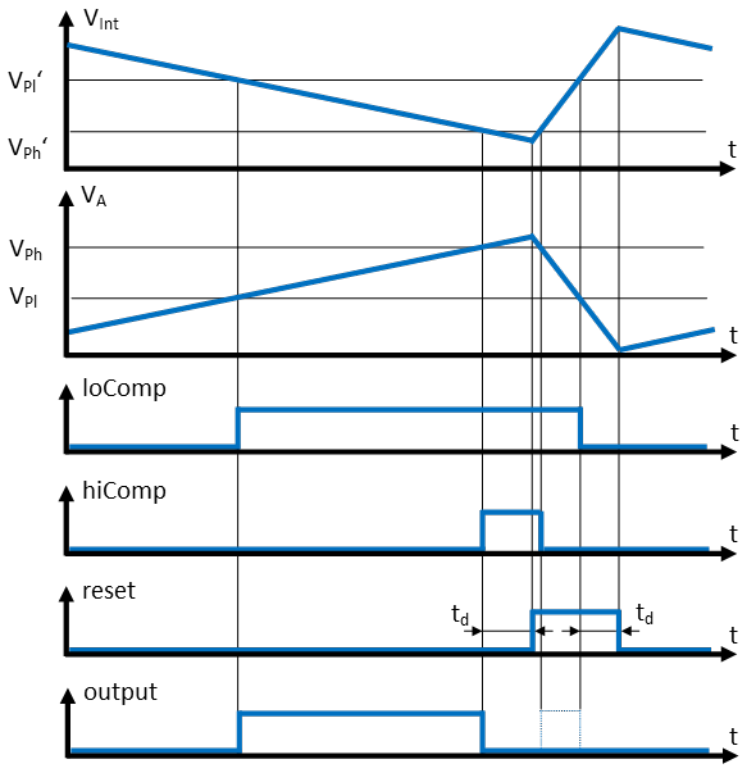

Figure 3.6: The logic signals **reset** and **output** are a combination of the comparator outputs. These are determined by the amplifier output. However, to emphasize the reset process the amplifier output is mapped to the voltage at the integration node. Hence V_{Pl} and V_{Ph} and their equivalents V'_{Pl} and V'_{Ph} are printed. The delay of logic gates t_d is considered for the fast reset process. A glitch in the **output** signal occurs if the comparator outputs are used exclusively. The glitch is presented by the doted line.

$$\mathbf{S_o} = \mathbf{loComp}.\overline{(\mathbf{hiComp} + \mathbf{reset})}$$
$$\mathbf{R_o} = \mathbf{hiComp} + \mathbf{reset}$$

The control signals **swD1**, **swD2**, **swRef**, **swC1** and **swC2** are determined by basic Boolean algebra. Figure 3.7 is used to obtain the equations.

The current source control signals are determined by figure 3.7 as

$$\mathbf{swD1} = \overline{\mathbf{S0}}.\overline{\mathbf{S1}}$$
$$\mathbf{swD2} = \mathbf{S0}.\overline{\mathbf{S1}} + \overline{\mathbf{S0}}.\mathbf{S1}$$
$$\mathbf{swRef} = \mathbf{S0}.\mathbf{S1}$$

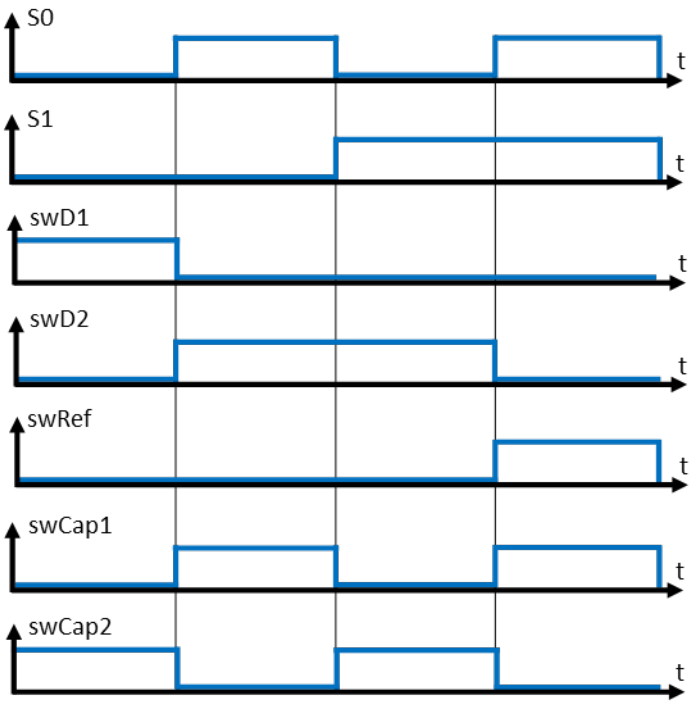

Figure 3.7: The logic signals controlling the switches in the test structure are primarily determined by the select signals **S0** and **S1**.

The capacitor control signals are additionally manipulated by the **reset**. On a reset all capacitors have to be connected to the integration node in order to get a well defined state. Thus the equations for **swC1** and **swC2** include the **reset** signal.

$$\mathbf{swC1} = \mathbf{S0} + \mathbf{reset}$$
$$\mathbf{swC2} = \overline{\mathbf{S0}} + \mathbf{reset}$$

3.6 External Connection and Application

This section concludes the design chapter and presents how the test structure is connected to external measurement equipment.
There are eight pins for each test structure:

- VDD: Positive supply voltage.
- VSS: Ground potential (0 V).
- Reset: External reset of the test structure.
- Ibias: Bias current to operate the source follower, amplifier and comparator.

- Iref: Reference current used to obtain a unique solution for the system of equations 3.4.
- S0 and S1: Pins for the select signals to choose a line in the system of equations 3.4 to be recorded.
- Output: The duration of the output signal's *high*-sequence is the integration time Δt used in the system of equations 3.4. Depending on the applied select signals **S0** and **S1** this time is either Δt_1, Δt_2, Δt_3 or Δt_e.

The measurement itself is done by applying the select signals and record the duration of the output signal's *high*-sequence. This equals the integration time Δt used to calculate the results. Once the integration time is recorded the measurement equipment changes the select signals and repeats the recording of the duration of the *high*-sequence. A reset must be performed each time the select signals are changed to ensure proper operation. After all four integration times Δt are recorded the system of equations 3.4 is solved by the measurement equipment or a computer.

Chapter 4

Implementation for Scribe Line Module

The previous chapter outlined the design of the test structure in a general manner. The measurement method and components of the test structure were presented. This includes the requirements each of the components must meet.
This chapter shows the actual implementation in account for the fabrication process, its available devices and limitations. The properties of the individual devices, e.g. the transistor dimensions W and L, were optimized by simulation. The discussion and presentation of these simulations would inappropriately increase the length of this thesis. Instead the requirements for a certain device and possible trade-offs are outlined. This chapter acts as a guideline for designing the test structure without detailing each individual device parameter available to the designer.
However, some of the device parameters are important and are discussed in the later chapters. Therefore after the trade-offs were presented the essential device parameters and circuit component properties for this particular implementation are listed.
The presentation of the test structure components is done in a similar fashion as in the previous design chapter. First the front stage will be discussed, followed by the amplifier, comparator and logic. In addition there is a section listing the different reference voltages and bias currents at the end of the chapter. These values are used in the subsequent chapter detailing the simulation of the test structure.

4.1 Front Stage

The front stage converts the leakage current of the DUT into a voltage slope by charging a capacitor. This voltage slope is then buffered by a source follower. Next the requirements for the individual devices of the front stage are discussed.

The integration capacitor can be integrated using various device types as detailed in section 2.5.2. The process option determines which are available. The capacitors on hand in the chosen process are the junction capacitor, the MOS capacitor and the PIP capacitor. The MIM capacitor is not available in each process and can therefore not be utilized. The choice for the capacitor has a major impact on the overall test structure performance.
One of the most important properties concerning the needs for the current measurement is the voltage dependence of the capacitance $C(v)$. Its impact was detailed in section 2.2.3 and has to be negligible. The PIP type offers the lowest voltage dependence of the capacitors on hand.
The general concept presented in section 3.1 requires to toggle the capacitors C_1 and C_2. The connection of the three contacts (top plate, bottom plate and well) is crucial. The integration capacitance $C_{1,2}$ is formed by the top and bottom plate. The parasitic capacitor C_{para} created by the presence of the well has to be eliminated by some means. The configuration in figure 4.1 is assumed as a start.

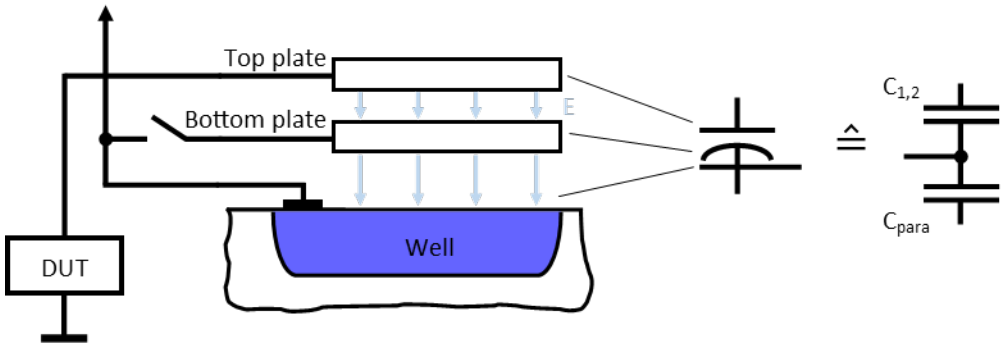

Figure 4.1: The connection of the integration PIP capacitor is critical. The impact of the parasitic capacitor has to be eliminated by circuit design. The symbol in the center is used further on for a PIP capacitance. The equivalent circuit for the capacitor is printed on the outermost right hand side.

The top plate is connected to the DUT and the well to the supply voltage. During measurement the switch is closed and the bottom plate wired to the supply voltage. Therefore the voltage between bottom plate and well is constant. This forces the current exclusively into the integration capacitance. When the capacitor is disconnected by opening the switch the bottom plate is floating. The two capacitors $C_{1,2}$ and C_{para} are therefore connected in series. This decreases the effect but does not fully eliminate the parasitic capacitance. A different circuit has to be used.
The problem arises from the non-constant voltage between the top plate and well. Generally, the voltage between them does not have to be 0 V. The derivative with respect to time in equation 2.8 of a constant voltage is 0 V/s and therefore inhibits current flow. The

principle circuit is pictured on the left hand side of figure 4.2.

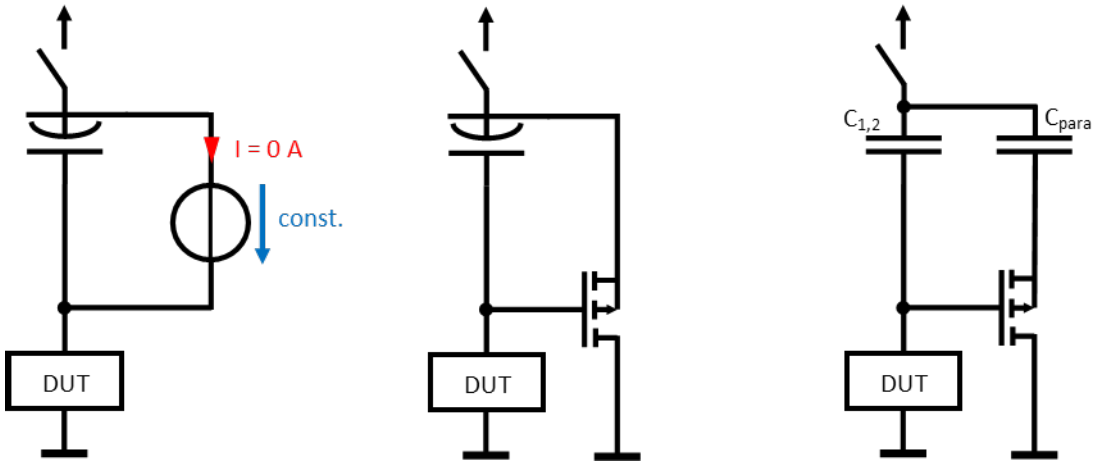

Figure 4.2: Schematic circuit used to toggle the integration PIP capacitor.
Left: Principle circuit. A constant voltage between top plate and well inhibits current flow.
Center: Implementation utilizing the output voltage of the front stage. The transistor shown is the source follower.
Right: Equivalent circuit for the capacitor to clarify the wiring.

The DC voltage source is already realized by the source follower. The well has to be wired to the output of the front stage. Thus the capacitor can effectively be removed by disconnecting the bottom plate from the supply voltage.
During a measurement cycle the bottom plate is connected to the supply voltage and separates the integration capacitor from its parasitic counterpart. Both capacitors are charged independently.
Note: In a simulation environment one has to be aware of the circuit pictured on the right hand side of figure 4.2. In order to obtain the right current in a simulation the corresponding contact has to be selected. Selecting the bottom plate contact yields the sum of currents into the integration capacitor and into the parasitic capacitor. In order to obtain the current into the integration cap the top plate contact has to be selected.
One capacitance is determined by the reference current. This capacitor must be large enough to cause a sufficiently slow voltage slope $\Delta v/\Delta t$ that can pass the amplifier. Thus the capacitor charged by the reference current source is determined in conjunction with the minimum bandwidth of the amplifier. The trade-off between gain and bandwidth is detailed in section 4.2. A large capacitance relaxes the gain-bandwidth trade-off for the amplifier. But a large capacitance results in long integration times and in turn negatively affects the voltage slope approximation 3.1.
The second capacitor can be smaller. But both are connected to the integration node. Thus even with the wiring detailed above to efficiently disconnect one of the capacitors there is still some parasitic impact left. The source follower is unable to perfectly reproduce the integration voltage change at its output. Therefore the disconnected capacitor still contributes to the total capacitance at the integration node. This is a problem when the

difference between the capacitances is large. Hence the capacitance must be in the same order of magnitude.
The implemented capacitance values of C_1 and C_2 are given in the summary at the end of this section.

The common gate transistor N_1 stabilizes the voltage on the DUT. Otherwise the bias condition and thus the current changes. The common gate transistor can also be interpreted as a cascode for the DUT. But the common gate transistor itself also features currents flowing into its drain and source diffusion. Hence there is a trade-off for the common gate transistor. One has to decide between additional current drained by the common gate transistor and the change of DUT current over voltage.
The common gate transistor can be removed for a DUT with high differential impedance, as the current will not change significantly on a change in voltage. A low differential impedance DUT requires the use of a common gate transistor.
The parasitic current into the common gate transistors S/D diffusions can be reduced by decreasing the transistor width W.
The device length L influences the output impedance of the common gate transistor. A higher output resistance blocks the voltage swing on the integration capacitor more efficiently. Thus the transistor length L is usually bigger than the width W. The implemented common gate transistors dimensions are $W = 0.4, \mu$m and $L = 2\,\mu$m.
The common gate transistor is also used to switch between the two current sources, the DUT and the external reference current source, respectively. A second transistor N_2 identical to the common gate transistor N_1 is introduced and connected to the integration node. The switch is operated by the gate voltage as usually by either applying a common gate voltage V_{Common} or 0 V.

The reset transistor P_2 shown in figure 3.2 charges the integration node in the front stage to a defined potential V_{reset}. The output voltage becomes V_{FSR}. This voltage is pictured as the starting voltage of the integration capacitor in figure 3.3. The transistor must not add a significant capacitance to the integration node. Therefore it is set to minimum width $W = 0.4\,\mu$m. The sub-threshold leakage current has to be reduced as well. The body contact is wired to the supply voltage V_{DD} in order to reduce the depletion layer capacitance at the diffusion. The device length is increased accordingly until the sub-threshold leakage current becomes negligible. This results in a gate length of $L = 2\,\mu$m.

The transistors P_3 and P_4 toggle the integration capacitors C1 and C2. There is no special requirement for these. Thus they are set to a minimum size of $W = 0.4\,\mu$m and $L = 0.35\,\mu$m.

The source follower transistor P_1 amplifies the signal at the integration node for further processing. It offers a high input impedance while being able to drive a certain amount of current at its output. The major problem of this device is the trade-off between its input capacitance and output current. The design of the source follower a slightly larger device is suggested. Its dimensions are set to $W = 1.5\,\mu$m and $L = 1\,\mu$m.

The DUTs for this particular test structure are n-well/p-substrate diodes. According to the model files the specific area current is $J_A = 2.8\,\mu A/m^2$ and the specific perimeter current is $J_P = 7.59\,pA/m$.

There are different methods to integrate the DUT into the front stage. Either all DUTs are connected into a single front stage or each has its own front stage.
The implementation of multiple front stages reduces the number of devices connected to the integration node and therefore parasitic current to a minimum. A major drawback is mismatch between the distinct front stages.
The opposite is true for the single front stage implementation. The matching is improved while the parasitic current becomes larger.
The additional parasitic current is considered to be the more serious problem. Thus two front stages (one for each DUT) are used in a test structure. The reference current source is connected to the front stage with the higher DUT current. The additional device needed to switch the current source has less impact due to the higher DUT current.

The reference current is determined by the external measurement equipment. The probe card and wiring limits the lower bound. A stable and accurate current can be provided by the available measurement equipment when the absolute value of the reference current is greater than 100 pA.

The nominal currents at $T = 25\,^{\circ}\mathrm{C}$ are $I_{D1} = 6.33\,\mathrm{fA}$ and $I_2 = 3.73\,\mathrm{fA}$. The capacitances are $C_1 = 1.5\,\mathrm{pF}$ and $C_2 = 0.5\,\mathrm{pF}$. The reference current is $I_e = -200\,\mathrm{pA}$.

4.2 Amplifier

For the operational amplifier a pre-designed type from the library is used. The measurements are expected to take a long time compared to the bandwidth of the amplifier. Hence the corner frequency is of little interest. But noise is important as it causes jitter in the integration time. Thus a low-noise amplifier with p-type input transistors is chosen.
The OPAMP offers power-down switches, which were removed in order to save area.

The transistors N_3 and N_4 shown in figure 3.5 form the differential input pair and have a high transconductance g_m. Thus their W/L-ratio is high as well as the current flowing through them which is determined by the current source.

The transistors N_5 and N_6 form the differential pair for the feedback loop. These two also have a high W/L-ratio as they set the control of the OPAMP on the input circuit.
The gate voltage of N_5 sets the output voltage at 0 V input voltage difference. The output voltage starts to increase from this voltage towards the pass voltages of the comparator. Therefore it has to be below the lower pass voltage. The gap between has to be as small as possible to reduce measurement time. On the other hand the gap must be large enough to counter mismatch. A detailed presentation is given in section 4.5.
The resistors on the high side are passed by the current flowing through the current mirrors. The voltage drop determines the input potentials for the OPAMP. As the OPAMP has a p-type input the potential has to be a certain amount below the supply voltage. However, this leaves less voltage for the transistors in the external differential input stage. This limits the lower bound of the voltage. The resistance has to be chosen accordingly.
The gain is set to $G = 50$.

4.3 Comparator

There are no special requirements for the comparators themselves. Hence they are taken from the library. The power-down switches and any non-essential components are removed to save area. The output driver transistors can also be shrunk as the comparators are loaded with logic gates only.

The lower pass voltage V_{Pl} is set a certain amount higher than the amplifier output voltage during reset V_{Common}. The difference is chosen in accordance with the worst case amplifier output voltage.
The higher pass voltage V_{Ph} determines the end of the measurement cycle. Once the amplifier output voltage reaches the higher pass voltage V_{Ph} the circuit can be reset. The upper bound of the higher pass voltage V_{Ph} is determined by the p-type input of the comparators. A large higher pass voltage causes worse behavior of the comparator.
The pass voltages are provided by the voltage divider discussed in section 4.5.

4.4 Logic

The signals presented in the design section 3.5 tell if a certain component is active. Depending on the actual switch to connect the device it can be necessary to logically invert the signal. Most of the switches are realized as T-gates and require inverted and non-inverted signals anyway.
For the realization of the logic circuit NOR, NAND and NOT gates were available only. Therefore the aforementioned equations have to be reformulated to obtain suitable expressions. A detailed presentation of the reformulation is omitted.
The **reset** signal is generated by a NOR flip-flop. Its set and reset input equations are listed here to obtain a collection of all logic signals.

$$\mathbf{S_r} = \mathbf{hiComp}$$
$$\mathbf{R_r} = \overline{\mathbf{loComp}}$$

A NAND flip-flop is used for the **output** signal, i.e. its inputs are **low**-active. Thus the input equations become

$$\overline{\mathbf{S_o}} = \overline{\mathbf{loComp}.\left(\overline{\mathbf{hiComp} + \mathbf{reset}}\right)}$$
$$\overline{\mathbf{R_o}} = \overline{\mathbf{hiComp} + \mathbf{reset}}$$

The current source and capacitance control signals for NOR and NAND gates are

$$\mathbf{swD1} = \overline{\mathbf{S0} + \mathbf{S1}}$$
$$\mathbf{swD2} = \overline{\mathbf{S0}.\overline{\mathbf{S1}}}.\overline{\overline{\mathbf{S0}}.\mathbf{S1}}$$
$$\mathbf{swRef} = \overline{\overline{\mathbf{S0}} + \overline{\mathbf{S1}}}$$
$$\mathbf{swC1} = \overline{\overline{\mathbf{S0}}.\overline{\mathbf{reset}}}$$
$$\mathbf{swC2} = \overline{\mathbf{S0}.\overline{\mathbf{reset}}}$$

4.5 Reference Voltages and Bias Currents

The reference voltages mentioned in the previous sections are generated by a voltage divider. It offers good accuracy and control of the reference voltages but must not be loaded. However, the reference voltages are used to bias the gates of MOS transistors. Their load on the voltage divider is negligible.
The reset voltage V_{reset} is generated by a separate voltage divider as it is loaded during reset. This load would cause a change in the other voltages if only one voltage divider is implemented.
An external current source provides the bias current for the test structure. Current mirrors are used to generate the bias currents for the individual components.
The voltage divider and current mirrors are printed in figure 4.3, their device parameters are listed in table 4.1.

The properties of the voltage divider and current sources are listed in table 4.2.

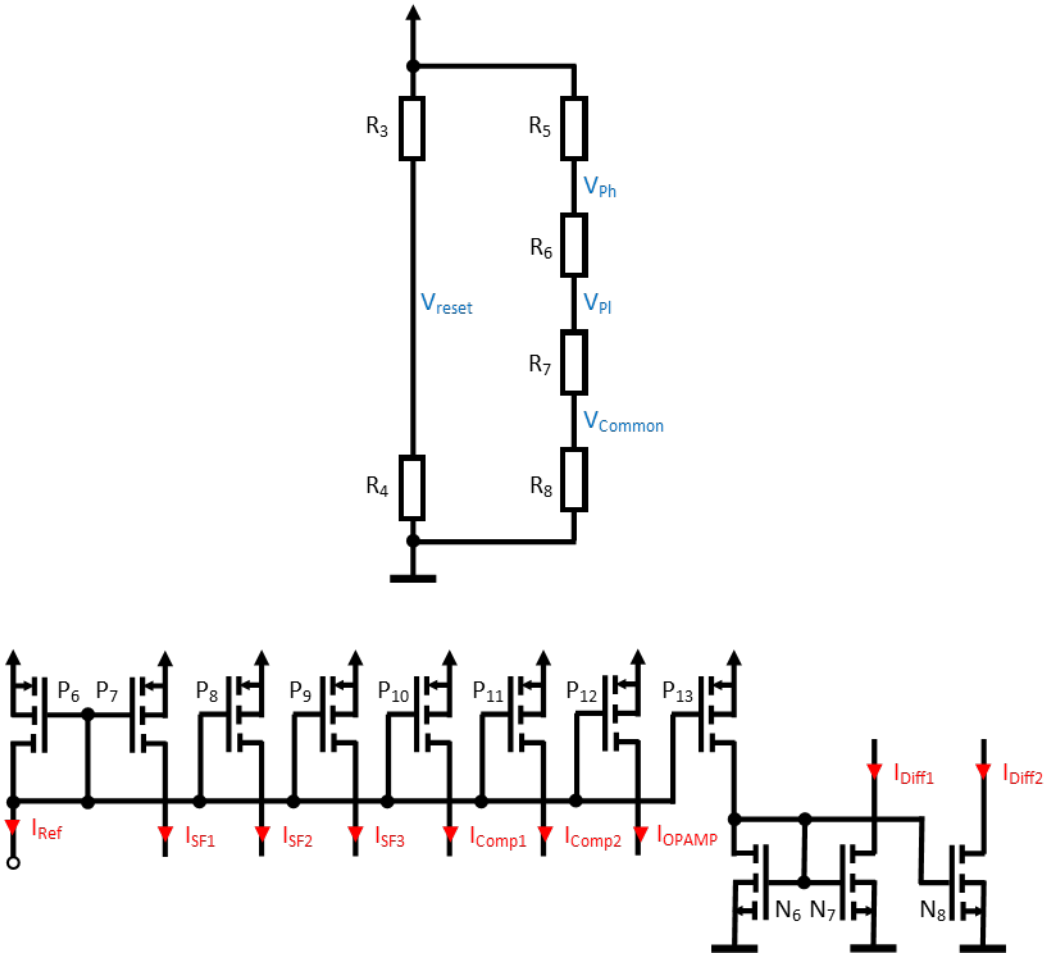

Figure 4.3: The reference voltages are set by a voltage divider. The bias current for the individual circuit components is generated by current mirrors and an external current source.

Table 4.1: Device parameters for voltage divider and current mirrors.

Device	Width	Length
R_3	2 μm	35 μm
R_4	2 μm	43.4 μm
R_5	2 μm	45.5 μm
R_6	2 μm	14 μm
R_7	80 μm	7 μm
R_8	80 μm	49 μm
P_6	8 μm	2 μm
P_7	2 μm	2 μm
P_8	2 μm	2 μm
P_9	2 μm	2 μm
P_{10}	80 μm	2 μm
P_{11}	80 μm	2 μm
P_{12}	80 μm	2 μm
P_{13}	80 μm	2 μm
N_6	3 μm	2 μm
N_7	60 μm	2 μm
N_8	60 μm	2 μm

Table 4.2: Essential properties of the voltage divider and current mirrors.

Property	Value
V_{DD}	3.3 V
V_{Reset}	1.83 V
V_{Ph}	2 V
V_{Pl}	1.6 V
Δv	0.4 V
V_{Common}	1.4 V
I_{bias}	-1 μA
I_{SF1-3}	-250 nA
$I_{Comp1,2}$	-10 μA
I_{OPAMP}	-10 μA
$I_{Diff1,2}$	200 μA

Chapter 5

Circuit Simulation

In the previous chapters the test structure was first designed in a general manner and later on implemented for the particular fabrication process. The individual components and their requirements were outlined. The test structure converts the small DUT leakage current into a rectangular voltage pulse with corresponding width.
This chapter focuses on SPICE simulation results for verification and validation of the design deduced previously.
It consists of three parts:
First the nominal simulation of the circuit itself using a Spectre simulator. This is done in order to verify the design. Internal signals like the leakage current are investigated. In a similar manner as in chapter 3 the circuit components are individually discussed. After the individual components the entire test structure as a whole is simulated. The output signal is recorded and the corresponding leakage current is calculated. The result is compared to the value obtained by simulation and device specification.
A Monte-Carlo simulation and processing of the results using Matlab is the second part. Thus the variation of the measurement due to device mismatch is investigated. The test structure must exhibit less variation than the DUTs.
The third part is a post-layout simulation. It is performed in order to understand the impact of parasitic effects on the test structure. This focuses on the capacitance caused by the wiring and parasitic components.

5.1 Verification

The simulation with nominal values for the parameters is used to verify the design. First the front stage is investigated. This especially includes the current to voltage slope conversion. Thereafter the test structure components amplifier, comparator and logic are separately discussed. The **output** signal is recorded for all four measurement modes to conclude the verification. The current and capacitance are obtained by solving the system of equations 3.4. The results are compared to the values from the front stage simulation. It is important to alter the simulator settings. Due to the small leakage currents the parameter 'gmin' has to be changed. 'gmin' sets the minimum conductance between each node. This conductance has to be significantly smaller than the conductance of the DUT. Otherwise the 'gmin'-current introduced by the simulator exceeds the DUT leakage current and inhibits the investigation.

5.1.1 Front Stage Simulation

The most crucial signals regarding measurement accuracy are the voltages at the source follower output, the DUT and the integration node as well as the DUT leakage current. The signals were investigated for all four current-capacitance combinations. The first set (I_{D1} and C_1; **S0** = *low*, **S1** = *low*) is used to present the front stage simulation.
The front stage is simulated while separated from the rest of the test structure in a special test bench. It provides the necessary voltages, currents and signals to operate the front stage.
The signals are chosen in such a way that the simulation is similar to the operation in the actual test structure. Thus the values listed in table 4.2 are used for the reset voltage V_{reset}, the common gate voltage V_{Common} and the source follower current I_{SF1-3}.
The initial conditions for the front stage are equal to the reset state. This is done by performing a DC simulation prior to the transient simulation. The **reset** is set *high* during the DC simulation and the operating points are saved. They are then loaded in the transient simulation by selecting the corresponding check box in the transient simulation options. Thus the transient phenomenon is avoided and simulation time reduced.
The change of the integration voltage in the test bench must cover the voltage swing in the whole design. The design is reset by the logic when the signal **hiComp** is set *high*. This happens when the amplifier output voltage reaches the higher pass voltage V_{Ph}. The voltage has to be mapped to the integration node voltage in order to determine the minimum time between two resets.
The amplifier output voltage changes from V_{Common} to V_{Ph} in one measurement cycle. The change in integration node voltage is obtained by taking the gain G into account. The minimum time between two resets is therefore determined by

$$T_{reset,min} = \frac{C_1}{I_{D1}} \cdot \frac{V_{Ph} - V_{Common}}{G} = \frac{1.5\,\mathrm{pF}}{6.33\,\mathrm{fA}} \cdot \frac{2\,\mathrm{V} - 1.4\,\mathrm{V}}{50} = 2.84\,\mathrm{s} \tag{5.1}$$

The simulation time is set to cover three individual measurement cycles. Thus a change in the operating point can be detected.

The simulated DUT current, DUT bias voltage, integration node voltage and source follower output voltage are printed in figure 5.1. The change in voltage is obtained by a delta-marker, which gives the difference between the two individual markers. A trace marker is used for the current. Ideal values are further on referenced by the index i.

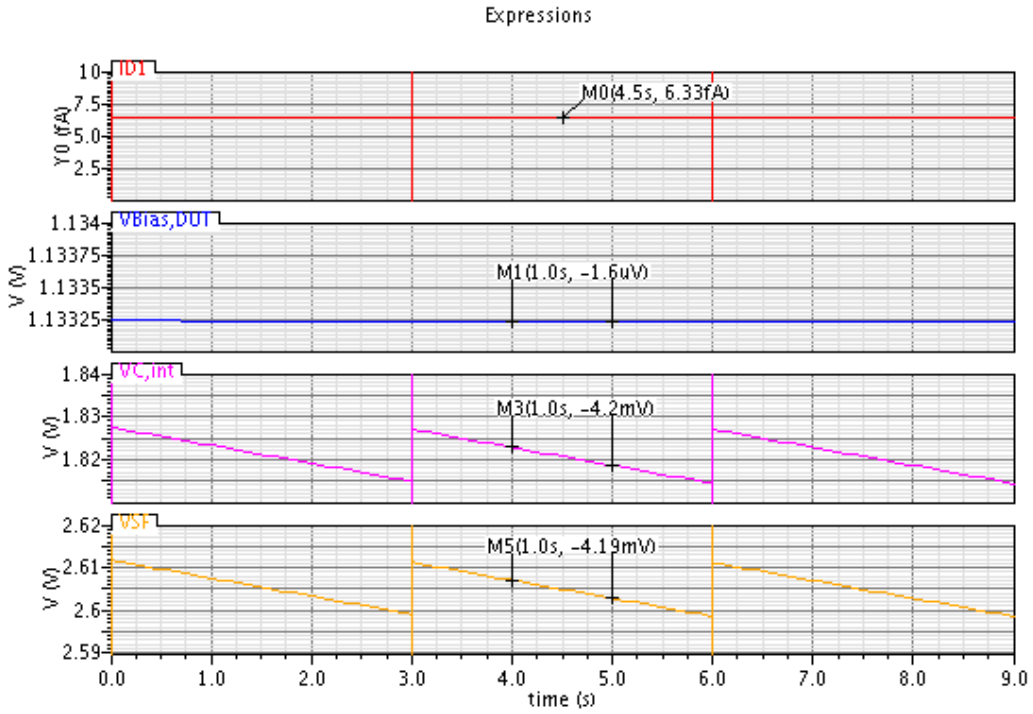

Figure 5.1: Simulation of the front stage measuring the DUT current I_{D1}. Top: Ideal DUT leakage current $I_{1,i}$. Above center: DUT bias voltage v_{Bias}. Below center: Integration node potential v_{int}. Bottom: Source follower output voltage v_{SF}.

The ideal DUT current is obtained by the red line (top) in figure 5.1 and equals $I_{1,i} = 6.33\,\mathrm{fA}$. The ideal change in voltage at the integration node $\Delta v_{int,i}/\Delta t$ is calculated by

$$\frac{\Delta v_{int,i}}{\Delta t} = -\frac{I_{1,i}}{C_1} = -4.22\,\mathrm{mV/s}$$

This value is close to the simulated one of $\Delta v_{int}/\Delta t = -4.2\,\mathrm{mV/s}$ as shown by the magenta line (below center) in figure 5.1. The leakage current into the other devices can therefore be considered negligible. The DUT current flows into the integration capacitance only.
The DUT bias voltage change is $\Delta v_{Bias}/\Delta t = -1.6\,\mu\mathrm{V/s}$ according to the blue line (above center) in figure 5.1. It is sufficiently small, proving the common gate transistor to work properly.
The front stage output voltage generated by the source follower output voltage is presented as the orange line (bottom) in figure 5.1. The source follower changes the voltage slope from $\Delta v_{int}/\Delta t = -4.2\,\mathrm{mV/s}$ to $\Delta v_{SF}/\Delta t = -4.19\,\mathrm{mV/s}$. In section 3.2 the trade-off for the source follower transistor is outlined. In order to improve the voltage transfer

the transistor size has to be increased. This on the other hand causes additional current flowing into its gate and limits accuracy. The difference in the voltage slope is therefore considered viable.
The simulation results can be used to calculate the relative error for nominal values. The source follower output voltage slope is used to calculate the DUT current I_{D1}.

$$I_{D1} = -C_1 \cdot \frac{\Delta v_{SF}}{\Delta t} = -1.5\,\mathrm{pF} \cdot (-4.19\,\mathrm{mV/s}) = 6.29\,\mathrm{fA}$$

The relative error $\Delta_r x$ is determined by

$$\Delta_r x = \frac{x - x_i}{x_i} \cdot 100\,\% \tag{5.2}$$

where x is the measured or calculated value and x_i is the ideal value. Thus the relative error $\Delta_r I_{D1}$ for the DUT current I_{D1} equals

$$\Delta_r I_{D1} = \frac{I_{D1} - I_{1i}}{I_{1i}} \cdot 100\,\% = \frac{6.29\,\mathrm{fA} - 6.33\,\mathrm{fA}}{6.33\,\mathrm{fA}} \cdot 100\,\% = -0.6\,\%$$

The relative error is sufficiently small for application in device characterization.

The reference current is investigated in the same manner. It is especially critical due to the short time it takes to charge the integration node. The simulation results are printed in figure 5.2.

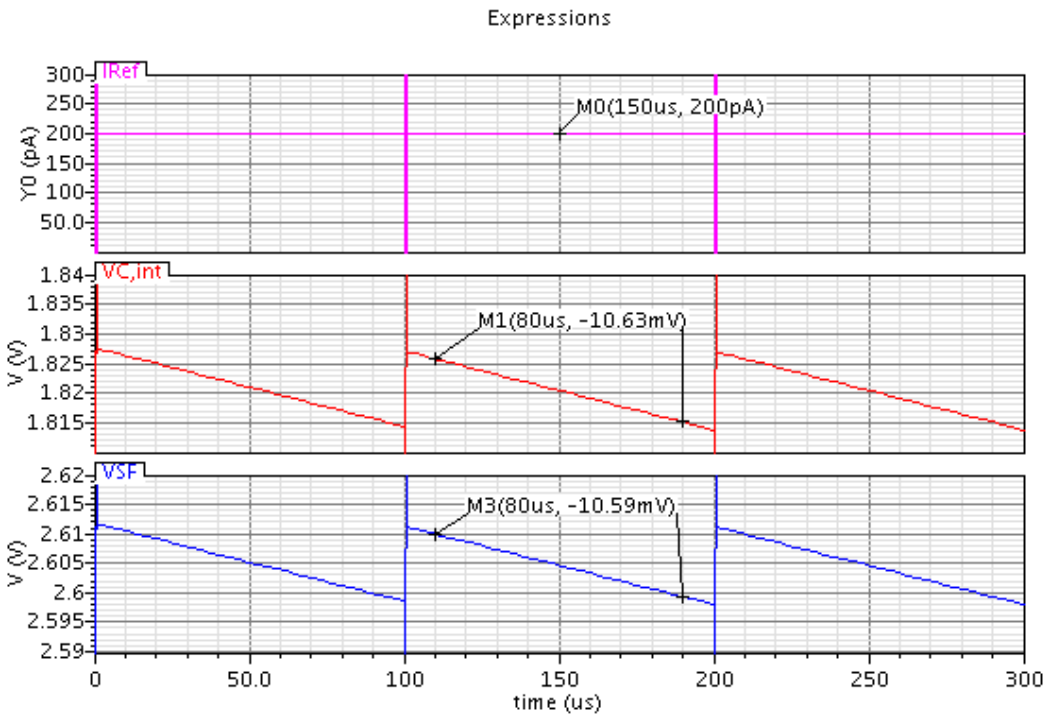

Figure 5.2: Simulation of the front stage measuring the reference current I_e. Top: Ideal reference current $I_{e,i}$. Center: Integration node potential v_{int}. Bottom: Source follower output voltage v_{SF}.

The current calculated by the voltage slope equals

$$I_e = -C_1 \cdot \frac{\Delta v_{SF}}{\Delta t} = -1.5\,\mathrm{pF} \cdot \frac{-10.59\,\mathrm{mV}}{80\,\mu\mathrm{s}} = 198.6\,\mathrm{pA}$$

The relative error is obtained by equation 5.2.

$$\Delta_r I_e = \frac{I_e - I_{ei}}{I_{ei}} \cdot 100\,\% = \frac{198.6\,\mathrm{fA} - 200\,\mathrm{pA}}{200\,\mathrm{pA}} \cdot 100\,\% = -0.7\,\%$$

The DUT and reference current are properly detected by the front stage. The relative error in current to voltage slope conversion is below 1 % for both.

5.1.2 Amplifier

The amplifier was separated from the test structure and embedded into a special test bench. This gives better control of the input voltages. These are set according to the

front stage output voltage V_{FS} and the reference voltage V_{Ref}. The amplifier output load is a 100 pF capacitor to account for the comparator input. The test bench is printed in figure 5.3.

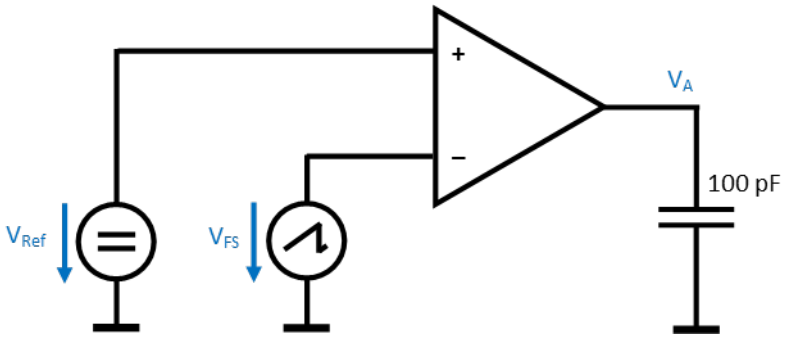

Figure 5.3: Test bench used to simulate the amplifier.

The principle function and linearity of the amplifier is verified by a DC sweep of the input voltage V_{FS} while observing the output voltage V_A. The output voltage range has to cover the region between the two pass voltages of the comparator. Between them the gain has to be constant for proper operation. The input voltage must therefore reach a value of

$$V_{FS,min} = V_{Ref} - \frac{V_{Ph} - V_{Common}}{G} \tag{5.3}$$

during the sweep. The starting value of the input voltage is set above the reference voltage V_{Ref}. Thus input voltage difference is negative at the beginning of the sweep. Negative input voltage difference is investigated to prevent malfunction at the beginning of the integration process in the front stage. The simulation results are shown in figure 5.4.

The output voltage is lower than V_{Common} for $V_{FS} \geq V_{Ref}$ as expected. For positive input voltage difference the output voltage increases linearly. The gain is calculated by

$$G = \frac{V_A - V_{Common}}{V_{Ref} - V_{FS}} \tag{5.4}$$

and shown in figure 5.4. The gain G matches the design value of 50 as given in section 3.3. The deviations in gain of 0.3 and -0.05 at the lower and higher pass voltage are negligible. An AC simulation is performed to obtain the bandwidth B of the amplifier. The DC output voltage is set in the middle of the two pass voltages V_{Pl} and V_{Ph} by applying a corresponding DC input voltage. Thus the amplifier is in a defined operating point. The simulation results are printed as a Bode plot in figure 5.5.

The bandwidth equals 483 kHz. This is related to a sinusoidal signal with a period of $T = 2.07\,\mu$s. This is well below the reference current measurement time, which can be approximated by

$$\Delta t_e = \frac{\Delta v \cdot C_1}{G \cdot I_e} = \frac{0.4\,\text{V} \cdot 1.5\,\text{pF}}{50 \cdot 200\,\text{pA}} = 60\,\mu\text{s} \tag{5.5}$$

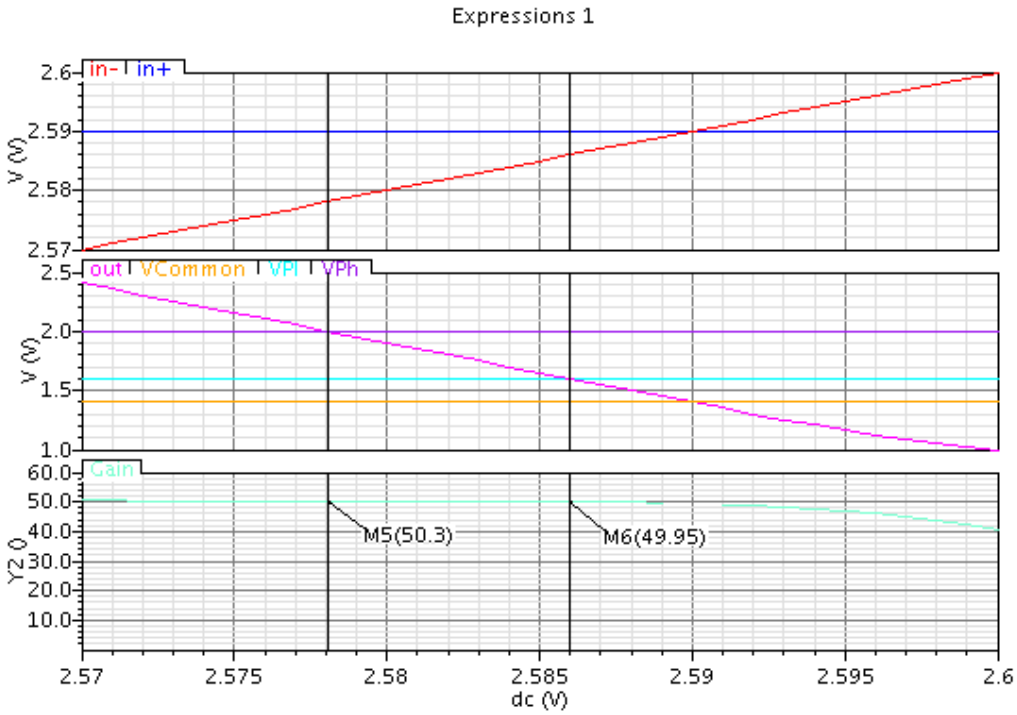

Figure 5.4: DC sweep of the input voltage to verify the amplifier. Top: The increasing input voltage and constant reference voltage. Center: Output voltage. Bottom: Gain.

But the amplified signal is not sinusoidal. A transient simulation is performed to prove a constant gain for the reference current measurement. Therefore a voltage slope steeper than the one of the reference current measurement is applied to the amplifier. The voltage slope caused by the reference current can be obtained by the values used in equation 5.5. The resulting output voltage slope equals $\Delta v/\Delta t_e = 6.6\,\mathrm{V/ms}$. This result is divided by the Gain G to obtain the input voltage slope of $-0.13\,\mathrm{V/ms}$. The input voltage slope for the transient simulation is set to $-0.2\,\mathrm{V/ms}$. The input voltage V_{FS} starts above the reference voltage V_{Ref} and ends at $V_{FS,min}$ given by equation 5.3, similar to the DC simulation. The gain is calculated by equation 5.4. The resulting graph is printed in figure 5.6.

The transient simulation gives a gain varying between 49 and 49.97 for the voltage range between V_{Pl} and V_{Ph}. This is considered sufficiently close to the designed value of 50. The non-constant gain outside this range is of no importance as it is not used in the system of equations 3.4. The negative peak in the gain at $50\,\mu\mathrm{s}$ is caused by the division by zero as the input voltages difference becomes zero.

5.1.3 Comparator

The critical quantity for the comparator is its sensitivity rather than switching speed. An ideal comparator switches its output when both inputs are at the same potential.

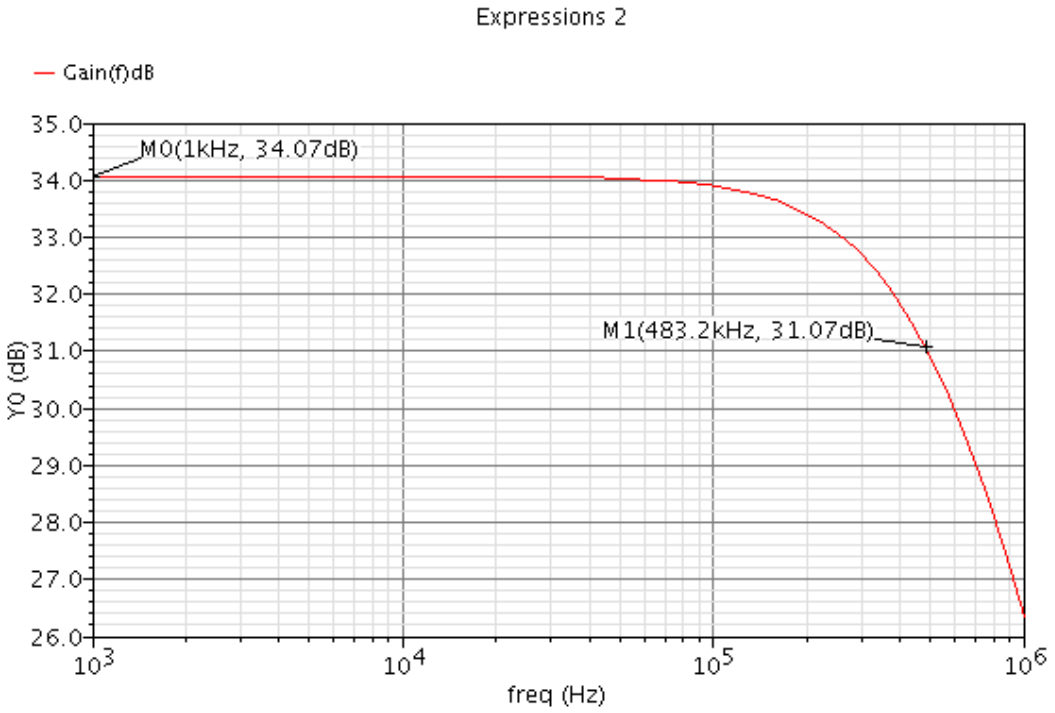

Figure 5.5: Bode plot of the amplifier obtained by an AC simulation.

A real comparator switches in an interval ΔV_c around this ideal point. This interval effectively changes the pass voltages V_{Pl} and V_{Ph}. The integration interval Δv as given by equation 3.2 becomes

$$\Delta v = (V_{Ph} + \Delta V_{c,h}) - (V_{Pl} + \Delta V_{c,l})$$

The impact of the interval ΔV_c can therefore be neglected if it is the same for both comparators. But since the comparators have different pass voltages the interval is supposed to be unequal and object of investigation. This is done by a DC sweep analysis similar to the one performed for the amplifier in the previous section 5.1.2. The input voltage is varied from a value below the lower pass voltage V_{Pl} to one greater than the higher pass voltage V_{Ph}. In order to detect the interval ΔV_c the voltage step has to be sufficiently small. The voltage step is set to $10\,\mu V$. The simulation results are shown in figure 5.7.

The interval Δv_i is obtained by the difference between the actual input voltage at a switching event $V_{in,h/l\Uparrow}$ and the corresponding pass voltage. Trace markers are used to obtain the values as shown in figure 5.7.

$$\Delta V_{c,h} = V_{in,h\Uparrow} - V_{Ph} = 2.00085\,V - 2\,V = 850\,\mu V$$
$$\Delta V_{c,l} = V_{in,l\Uparrow} - V_{Pl} = 1.60087\,V - 1.6\,V = 870\,\mu V$$

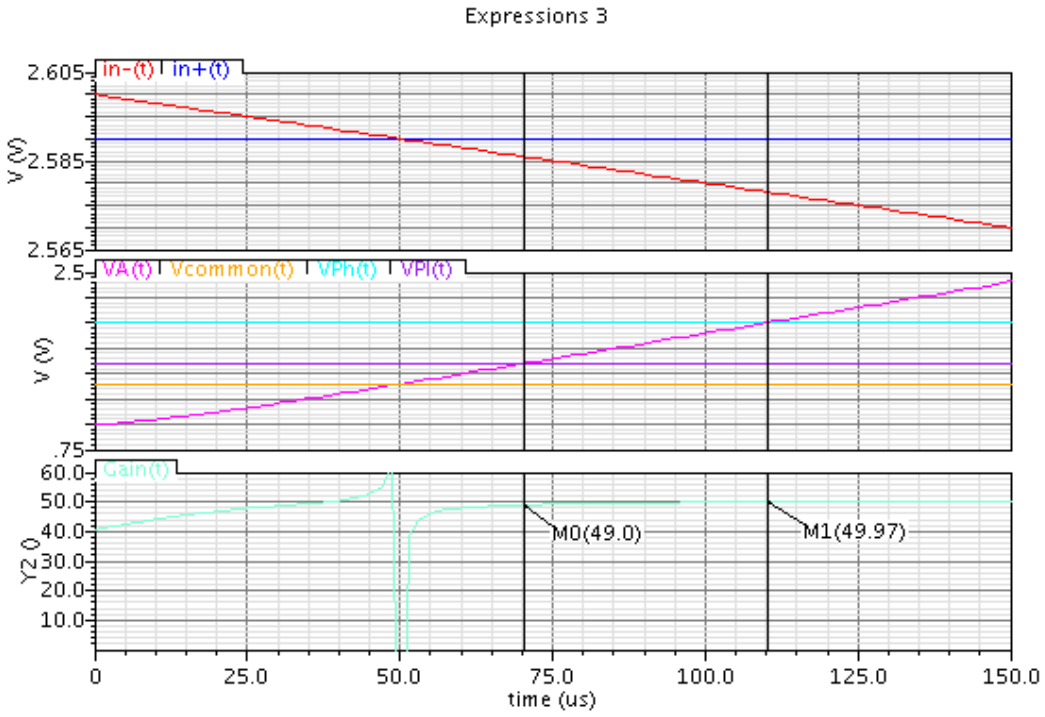

Figure 5.6: Transient simulation of the amplifier to prove constant gain during reference current measurement.

The difference between the two intervals is used to calculate the relative error in the integration interval Δv by equation 5.2.

$$\Delta_r v = \frac{\Delta v - \Delta v_i}{\Delta v_i} \cdot 100\,\% = \frac{\Delta V_{c,h} - \Delta V_{c,l}}{\Delta v_i} \cdot 100\,\% = \frac{850\,\mu V - 870\,\mu V}{0.4\,V} = -0.005\,\%$$

The relative error is negligible small and the comparator works properly.

5.1.4 Logic

The logic is investigated by a transient simulation. A DC simulation is unable to reveal problems with timing and oscillations. The signals are generated by voltage sources with rectangular output signals. The outputs of the logic are loaded with 100 pF. The general approach of observing the logic's output signals **swD1**, **swD2**, **swRef**, **swC1**, **swC2** and **reset** for every combination of input signals **S0**, **S1**, **Reset**, **loComp** and **hiComp** is exaggerated. Most of the combinations are not used by the test structure. A reduced set of test vectors is applied to verify the logic.

Similar to the logic's design in section 3.5 the signals are investigated separately. First the internal **reset** and the **output** are observed as a function of **loComp**, **hiComp** and

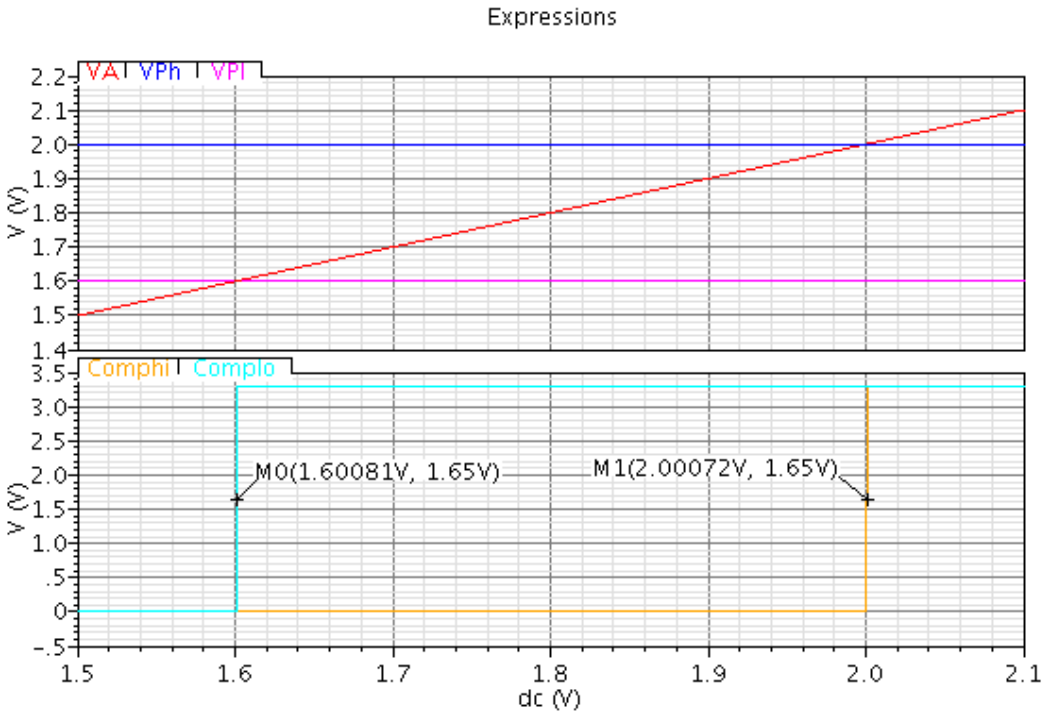

Figure 5.7: DC sweep of the input voltage to verify the comparator. Top: The increasing input voltage and pass voltages V_{Pl} and V_{Ph}. Bottom: Comparator output signals **hiComp** and **loComp**.

Reset. In order to represent actual operation of the test structure the signal **hiComp** is set *high* only when **loComp** is *high* as printed in figure 3.6.
The simulation results are printed in figure 5.8.

The internal **reset** is set *high* once **hiComp** is *high* and holds until **loComp** becomes *low*. The external **Reset** is also working as designed.
The **output** is *high* as long as **loComp** is *high* while **hiComp** is *low* (i.e. the test structure integrates the DUT leakage current). The glitch discussed in section 3.5 and shown in figure 3.6 is avoided by the design. The **output** is processed as intended.

The control signals **swD1**, **swD2**, **swRef**, **swC1** and **swC2** are examined next. The input signals for this test are **S0**, **S1** and **reset**. The latter is controlled by **Reset** while **loComp** and **hiComp** are *low*. This allows for the direct control of the internal **reset**, which is actually used to process the control signals.
Figure 5.9 shows the transient simulation results for the control signals.

The current source control signals **swD1**, **swD2** and **swRef** work well. The capacitance control signals **swC1** and **swC2** are set by the select signals **S0** and **S1** as intended. The external **Reset** and therefore the internal **reset** causes both **swC1** and **swC2** to be set *high*. This allows for appropriately recharge the capacitance at the integration node on a reset.

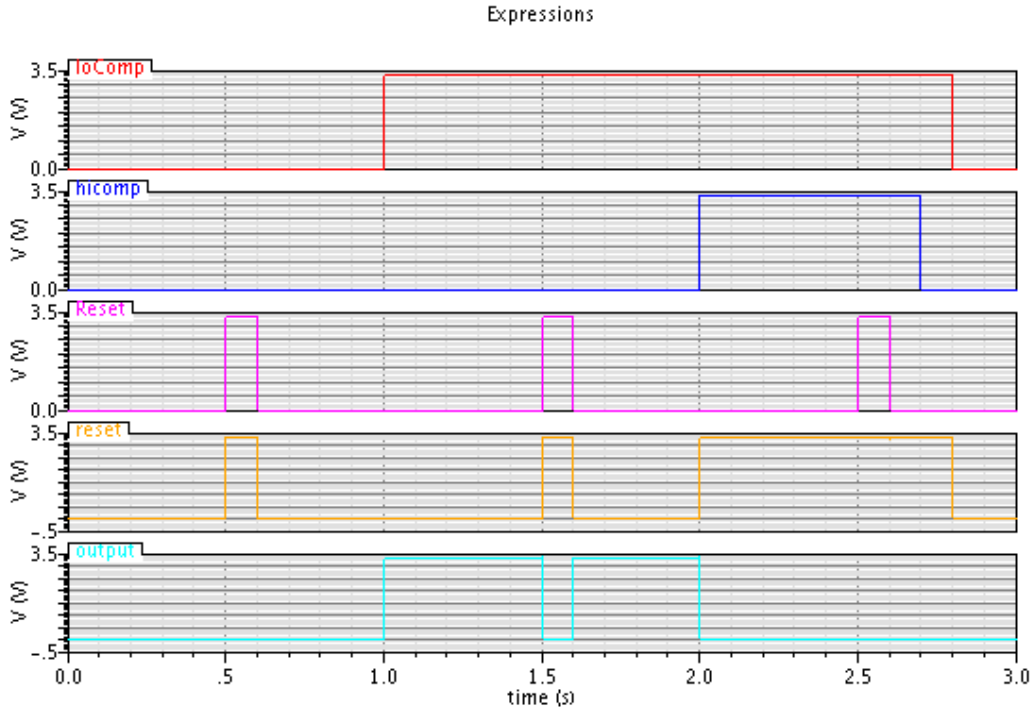

Figure 5.8: Transient simulation of the logic's **reset** and **output** signal controlled by the comparator outputs **loComp**, **hiComp** and external **Reset**.

5.1.5 Test Structure

The individual components have proven to be fully functional in the previous sections. The consecutive processing of the voltage slope by the front stage, the amplifier, the comparator and the logic has to be investigated. Therefore the output signal is observed and the associated currents and capacitances are calculated by solving the system of equations 3.4. The obtained values are compared to the simulated ones.
The test structure is connected to a test bench, which represents the external measurement equipment. The voltages and currents for the pins of the test structure are detailed in section 3.6. Their values are given in section 4.1 and 4.5. The test bench with the inlaying test structure is printed in figure 5.10.

Before the operation of the test structure is investigated a couple of DC parameters are obtained. They are later on used to verify the test structure measurement readings. The DC parameters includes the consumed current I_DD, the voltage V_{Bias} at the bias current pin and the voltage V_{Ref} at the reference current pin.
In order to keep the current consumption and voltages constant a permanent external **Reset** is applied to the test structure. The DC simulation results are listed in table 5.1.

A transient simulation is used to obtain the **output** signal. During simulation the select signals **S0** and **S1** are operated to cover each combination. Hence each of the four lines in the system of equations 3.4 is simulated. The **Reset** is triggered on each change of the

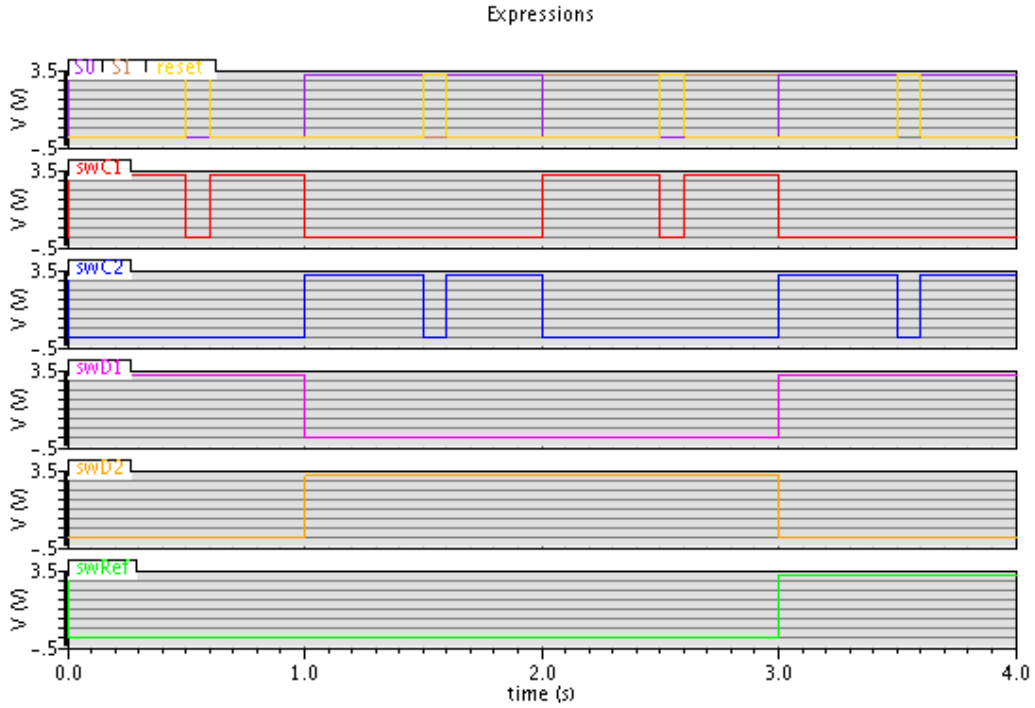

Figure 5.9: Transient simulation of the logic's control signals **swD1**, **swD2**, **swRef**, **swC1** and **swC2** as a function of **Reset** and select signals **S0** and **S1**.

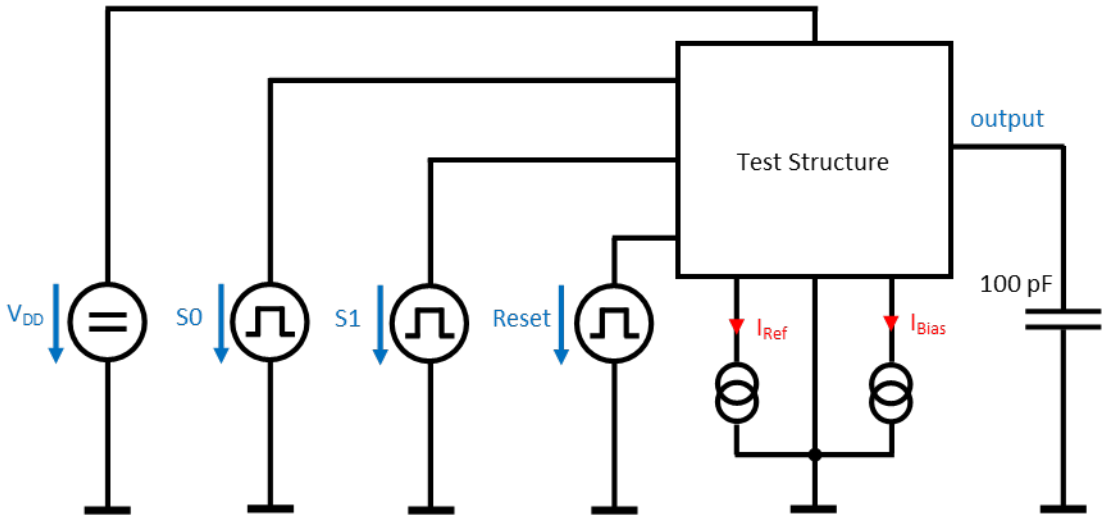

Figure 5.10: Test bench provides the test structure with supply voltage, bias and reference current in the simulation. It defines the select signals and reset. The output is loaded with a 100 pF capacitor.

select signals. Since the voltage slopes are different for each current-capacitor-combination the integration times differ as well. The first equation is simulated for 20 s. The second

Table 5.1: Simulated DC parameters of the test structure. The consumed supply current I_{DD}, the voltage V_{Bias} at the bias current pin and the voltage V_{Ref} at the reference current pin are used to verify measurement readings later on.

I_{DD}	V_{Bias}	V_{Ref}
3.64 mA	2.51 V	0.87 V

one for 15 s. The third for 25 s. The last equation with the reference current source takes 100 μs. The simulation results for the four different equations are printed in figure 5.11.

The integration times Δt are obtained by delta markers as shown in figure 5.11. The system of equations 3.4 is solved by Matlab. The calculated results along with their nominal values and relative errors are listed in table 5.2.

Table 5.2: Calculated results, nominal values and relative errors for the ideal test structure at T = 25 ^{o}C.

Quantity	Calculated	Nominal	Relative Error
I_{D1}	6.32 fA	6.33 fA	-0.16 %
I_{D2}	3.72 fA	3.73 fA	-0.27 %
C_1	1.502 pF	1.5 pF	0.13 %
C_2	0.509 pF	0.5 pF	1.8 %

The relative errors for the resulting quantities are small and suffice for the use of device characterization.

5.2 Monte-Carlo Simulation

After the verification of the test structure it has to be validated. The test structure is used for device characterization and as such its variation must be significantly smaller than the variation of the DUTs. This is investigated by two Monte-Carlo simulations. The first time with the actual device model, the second time with an ideal non-varying counterpart. The distribution of the results for the ideal model has to be narrower than the device model. The results of the individual simulations are calculated and compared to the ideal current.
However there is no ideal diode with the same characteristics available. But the actual diode model does not feature any Monte-Carlo parameters except for its size fluctuations. The capacitors are replaced with ideal devices. Unlike the test structure simulation in section 5.1.5 each line of the system of equations 3.4 is simulated separately. The simulation is started and the **output** signal read back by Matlab. The program then starts the simulation of the next line. Matlab extracts the pulse width for each line and solves the system of equations 3.4. This is repeated until the user-defined limit for the number of Monte-Carlo runs is reached.

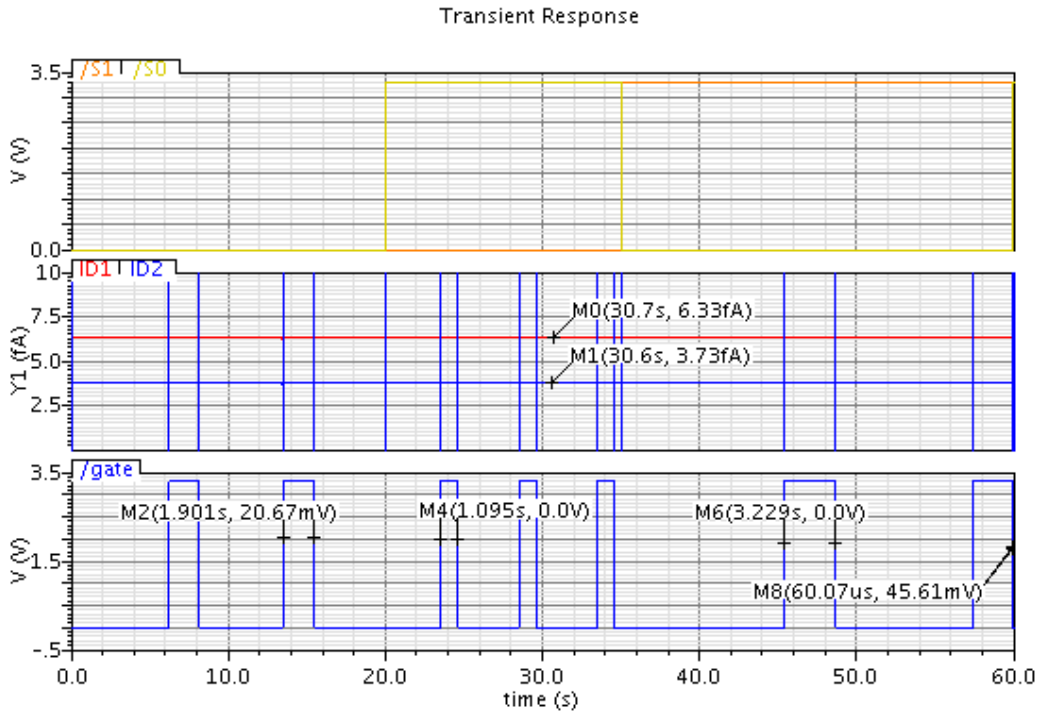

Figure 5.11: Simulation of the ideal test structure for each of the four lines in the system of equations. From 0 s to 20 s first line, 20 s to 35 s second line, 35 s to 60 s third line, from 60 s to 60 s + 100 μs fourth line. Top: Select signals **S0** (yellow) and **S1** (orange). Center: DUT leakage currents I_{D1} (red) and I_{D2} (blue). Bottom: **output** signal.

The individual results are then further processed. They are collected in a user-defined number of bins. The interval between the minimum and maximum time detected is evenly divided by the number of bins.
A normal distribution for the occupation of this bins is assumed and fitted to the obtained results. The mean μ and the standard deviation σ are calculated. The number of simulation results in a certain bin is printed as a bar along with the normal distribution, its mean μ and 3σ confidence interval.

The obtained plot for the D_1 leakage current I_{D1} is shown in figure 5.12.

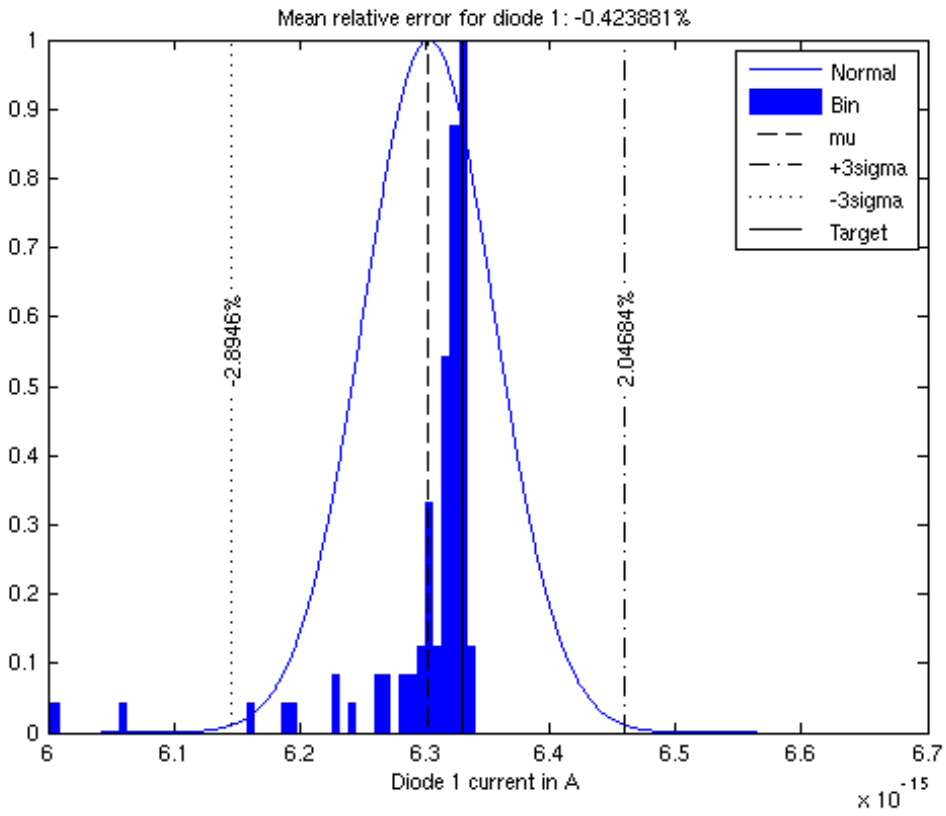

Figure 5.12: Monte-Carlo simulation result for D_1 leakage current I_{D1} with 100 runs. The individual simulation results are collected in bins. The number of results in one bin are presented as a bar. A normal distribution (blue line) is fitted to the results. Its mean μ and $3\,\sigma$ confidence interval are presented by vertical lines.

The obtained plot for the D_2 leakage current I_{D2} is shown in figure 5.13.

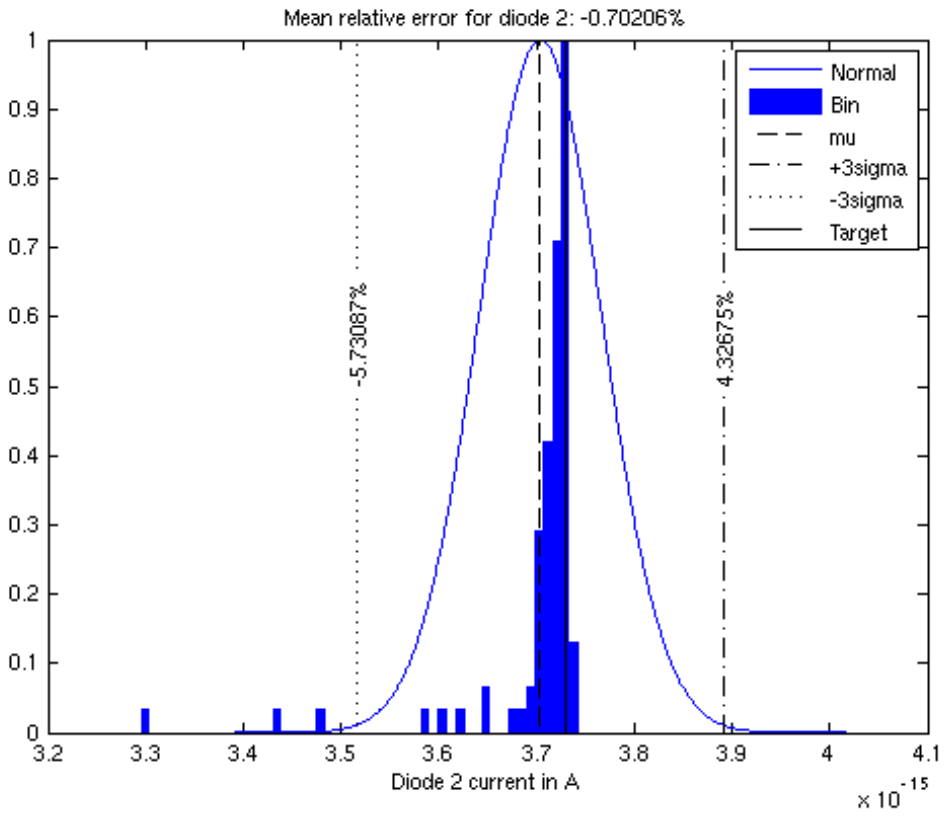

Figure 5.13: Monte-Carlo simulation result for D_2 leakage current I_{D2} with 100 runs. The individual simulation results are collected in bins. The number of results in one bin are presented as a bar. A normal distribution (blue line) is fitted to the results. Its mean μ and $3\,\sigma$ confidence interval are presented by vertical lines.

The Monte-Carlo simulation indicates a normal distribution of the leakage currents in the range of several percent. However the leakage currents do not follow a normal distribution. Instead they are distributed in an inverse log-normal manner. The majority of the simulation results are close to the nominal value.

The capacitors are simulated twice. The first time with the actual device model installed. The second time the capacitor is replaced by its ideal counterpart. A difference in variance indicates that the distribution is mainly determined by the capacitors.
The obtained plot for capacitor C_1 is shown in figure 5.14.

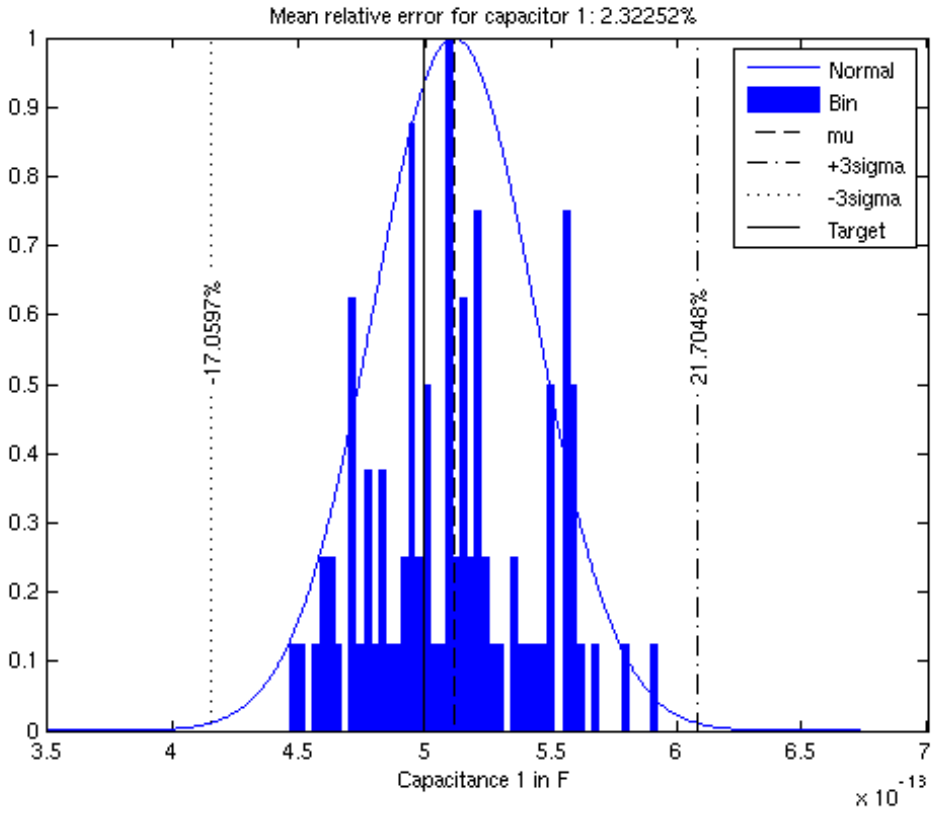

Figure 5.14: Monte-Carlo simulation result for capacitor C_1 with 100 runs. The individual simulation results are collected in bins. The number of results in one bin are presented as a bar. A normal distribution (blue line) is fitted to the results. Its mean μ and $3\,\sigma$ confidence interval are presented by vertical lines.

The obtained plot for capacitor C_2 is shown in figure 5.15.

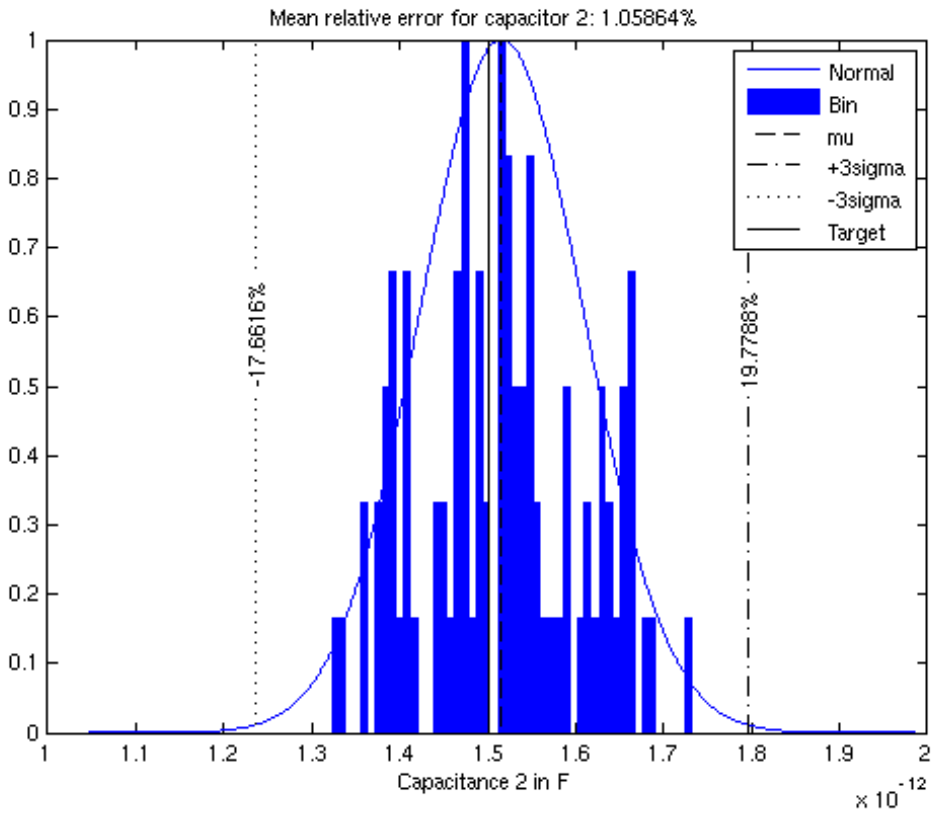

Figure 5.15: Monte-Carlo simulation result for capacitor C_2 with 100 runs. The individual simulation results are collected in bins. The number of results in one bin are presented as a bar. A normal distribution (blue line) is fitted to the results. Its mean μ and $3\,\sigma$ confidence interval are presented by vertical lines.

The obtained plot for the ideal capacitor model C_1 is shown in figure 5.16.

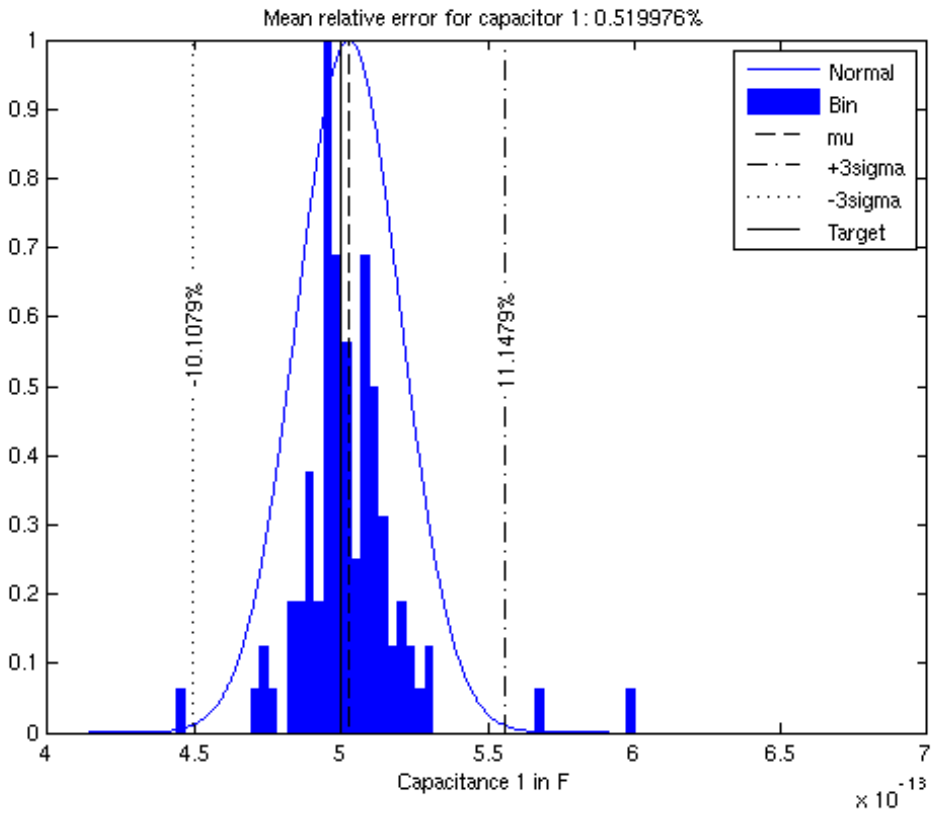

Figure 5.16: Monte-Carlo simulation result for ideal capacitor C_1 with 100 runs. The individual simulation results are collected in bins. The number of results in one bin are presented as a bar. A normal distribution (blue line) is fitted to the results. Its mean μ and $3\,\sigma$ confidence interval are presented by vertical lines.

The obtained plot for the ideal capacitor model C_2 is shown in figure 5.17.

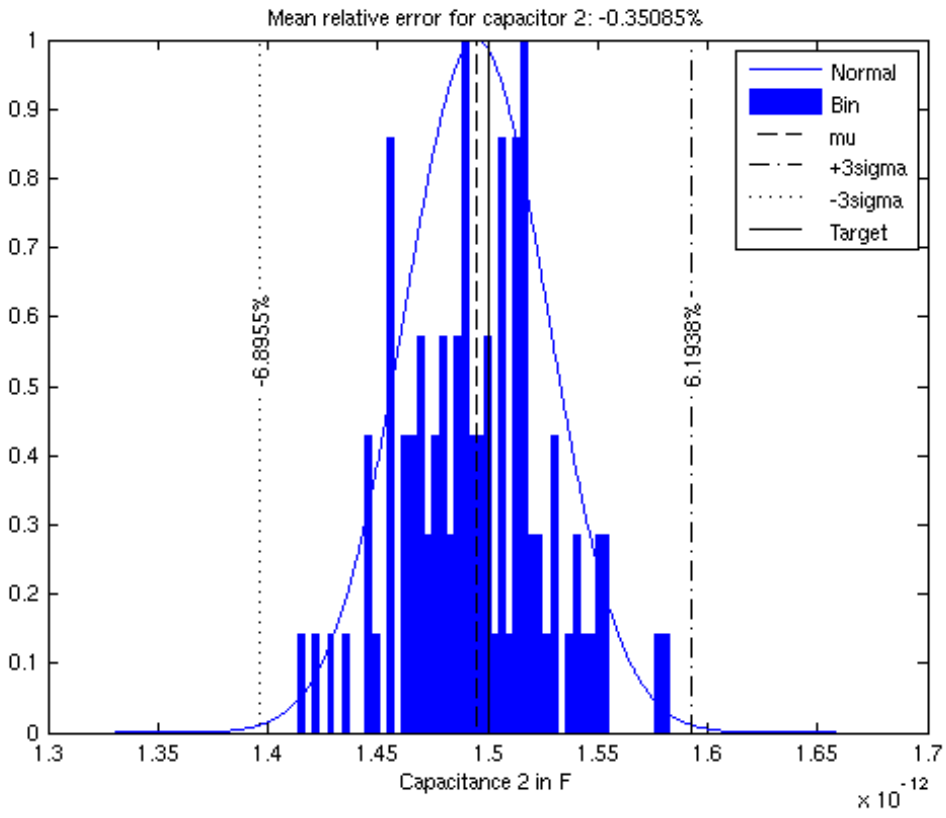

Figure 5.17: Monte-Carlo simulation result for ideal capacitor C_2 with 100 runs. The individual simulation results are collected in bins. The number of results in one bin are presented as a bar. A normal distribution (blue line) is fitted to the results. Its mean μ and $3\,\sigma$ confidence interval are presented by vertical lines.

A comparison of the results shown in figure 5.14 and 5.16 yields that capacitor C_1 varies more than the test structure readings with the ideal device in place. The same is true for the second capacitor C_2. The variance shown in figure 5.15 exceeds the one printed in figure 5.17.

5.3 Parasitic Extraction and Simulation

The test structure's performance may be influenced by its layout, especially the parasitic capacitance between its wiring. Therefore after the layout is finished a parasitic capacitance extraction is performed. The parasitic extraction adds the capacitance formed for example by the metal lines to the original circuit. The resulting netlist is simulated in the same way as the nominal circuit previously discussed in section 5.1.5. The test bench is retained while replacing the nominal test structure with its extracted analog. Depending on the actual capacitance at the integration node it may be necessary to adept the simulation time. The simulation result after the parasitic extraction is printed in figure 5.18.

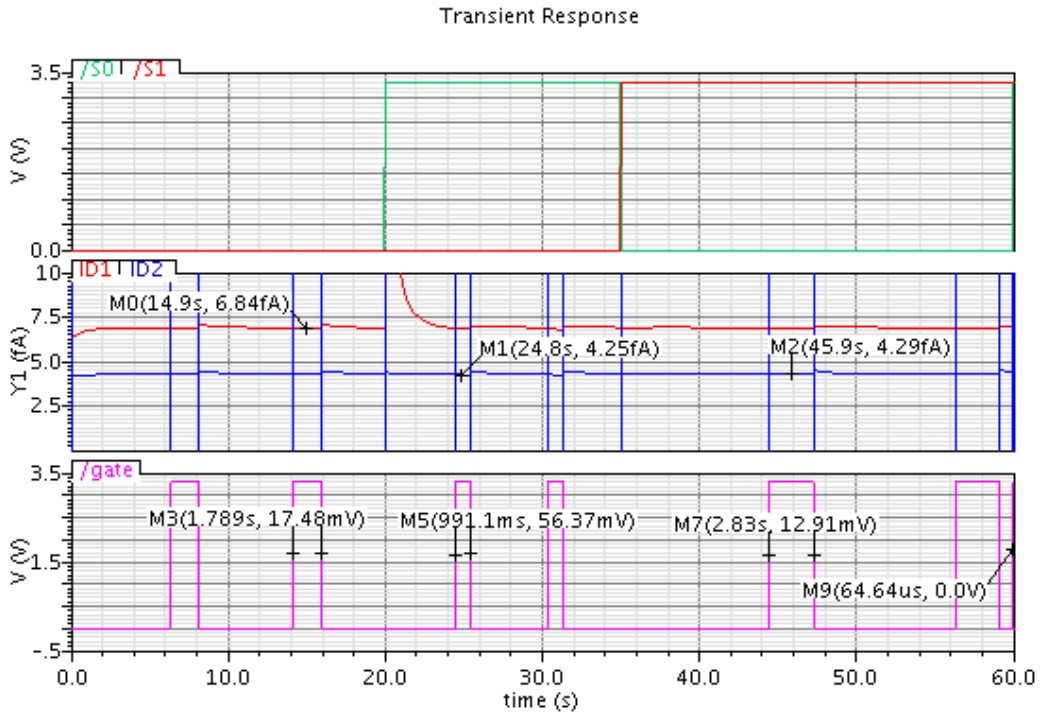

Figure 5.18: Simulation of the test structure after parasitic extraction for each of the four lines in the system of equations. From 0 s to 20 s first line, 20 s to 35 s second line, 35 s to 60 s third line, from 60 s to 60 s + 100 μs fourth line. Top: Select signals **S0** (green) and **S1** (red). Center: DUT leakage currents I_{D1} (red) and I_{D2} (blue). Bottom: **output** signal.

The DUT currents show stronger variations over time compared to the prior nominal simulation. These variations come from switching the current sources and capacitors. However the current settles to a stable value after a short time. The nominal DUT currents I_{D1} and I_{D2} are sensed during the *high*-sequence of the **output** signal as shown in figure 5.18. The DUT current I_{D2} is the mean value of the markers M1 and M2. The calculated results along with their nominal values and relative errors are listed in table 5.3.

The obtained results are compared to those of the nominal circuit simulation detailed in

Table 5.3: Calculated results, nominal values and relative errors for the test structure after parasitic extraction. T = 25 ^{o}C.

Quantity	Calculated	Nominal	Relative Error
I_{D1}	7.23 fA	6.84 fA	5.7 %
I_{D2}	4.57 fA	4.27 fA	7 %
C_1	1.62 pF	1.5 pF	8 %
C_2	0.57 pF	0.5 pF	14 %

section 5.1.5. The extracted simulation predicts less accurate results than the nominal circuit. The reference current (**S0** and **S1** are *high*) gives a longer integration time (64.64 μs) while all other integration time become shorter.

Chapter 6

Measurement of SLM

The simulations in chapter 5 verified and validated the design and implementation of the test structure. Its performance is ultimately determined by measurement. The test structure is fabricated in a 0.35 μm CMOS process.
The opportunity to connect internal signals to spare pads for testing was missed. Thus the test structure has to be investigated by the output signal, the supply current and the voltage on the bias pads. Structure internal signals are not accessible. Therefore an occasional failure of the test structure can hardly be analyzed.
Two different test structures are used. The first has its DUTs covered with metal to block impinging light. The metal cover on the second SLM is removed and its DUTs are open-topped. The DUTs can be regarded as photodiodes. Thus the impact of stray light can be investigated by comparing the result of both SLMs. Besides the test structure may be used for low intensity light detection.
The measurement results have to be verified. Therefore a predefined SLM3 already used in wafer test which features the DUTs is placed next to the previous SLM1 and SLM2. The leakage current of SLM3 is measured at elevated temperatures. The readings are extrapolated to room temperature and compared to the results obtained by the test structure SLM1.
Wafer orientation, relative coordinates of the dies and alignment of the SLMs are illustrated by figure 6.1.

This chapter details the measurement setup and the used equipment for investigating the test structure. First the consumed current I_{DD} at the positive supply pad and the voltages on the bias V_{Bias} and reference V_{Ref} pads are measured. The values are compared to simulation results. The reset mechanism is verified next. Then the **output** signal is then recorded for a single line of the system of equations 3.4. The integration time Δt is compared to its simulated counterpart. Subsequently all four lines in the system of equations 3.4 are investigated.
This procedure is done for ten test structures in total. These are selected from different locations at the wafer in order to evaluate the stray of the obtained results. All of the selected SLMs have their DUTs covered with metal, i.e. the SLM on the right hand side of each group of SLMs is used. Table 6.1 lists the relative positions of the test structure to the reference die 1. The reference die is located in the middle of the wafer.

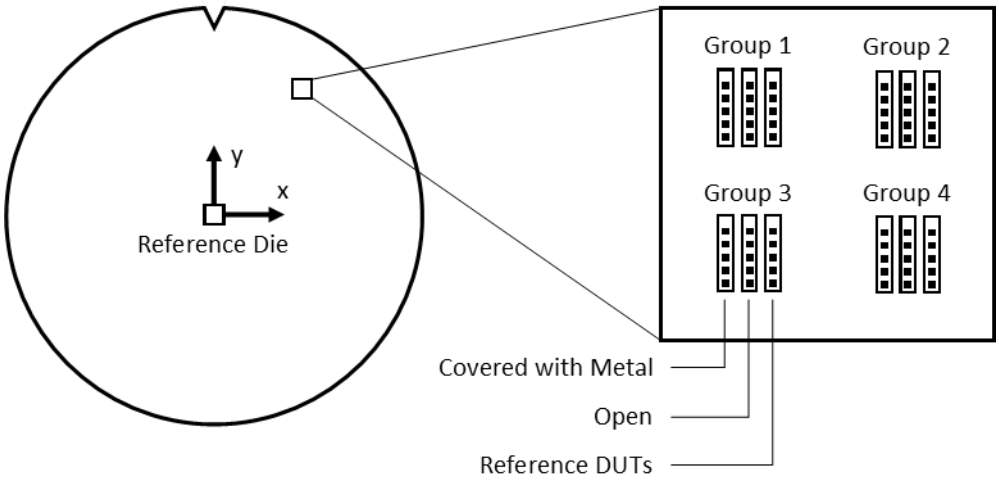

Figure 6.1: Illustration of wafer orientation and coordinates x and y originating from the reference die. The notch is in the north. The position and numeration of the four groups of SLMs on a single die is shown on the right hand side. Each group consists of three SLMs. The DUTs on the SLM1 on the left hand side are covered with metal to block impinging light. The SLM2 in the center does not have this metal cover and its DUTs are considered open. The SLM3 on the right hand side is predefined and already used in wafer test. It comes with the same junctions used as DUTs in the test structure and serves as an on-wafer reference.

Table 6.1: Test site positions on the wafer. Test site 1 serves as the reference location in the middle of the wafer. The distance is given in number of dies along the corresponding direction. The group used on a die is indicated in the appropriate column.

Test site	x in dies	y in dies	Group
1	0	0	1
2	-4	4	1
3	-4	4	4
4	2	2	1
5	2	2	4
6	-2	2	1
7	2	-2	1
8	-4	-4	1
9	4	-4	1
10	5	1	1

6.1 Measurement Setup

The measurement equipment consists of a parameter tester, a switching matrix and an oscilloscope. The source-measurement-units (SMUs) of the parameter tester supplies the test structure and provides the bias I_{Bias} and reference current I_{Ref}. This additionally enables simultaneous measurement of the consumed current I_{DD} and voltages on the bias V_{Bias} and reference V_{Ref} pad. The **output** signal is recorded by the oscilloscope. The wafer is connected by a probe card, which is designed for the SLM contact pad pattern. The SMUs for the reference and the bias current as well as the oscilloscope are directly connected to the probe card's terminals. Especially the reference current is very sensitive and the connected wire must be as short as possible. The remaining pads are controlled by the switching matrix. Thus the logic signals **S0** and **S1** can conveniently be changed and the external **Reset** can be triggered by the switching matrix. The measurement setup is shown in figure 6.2.

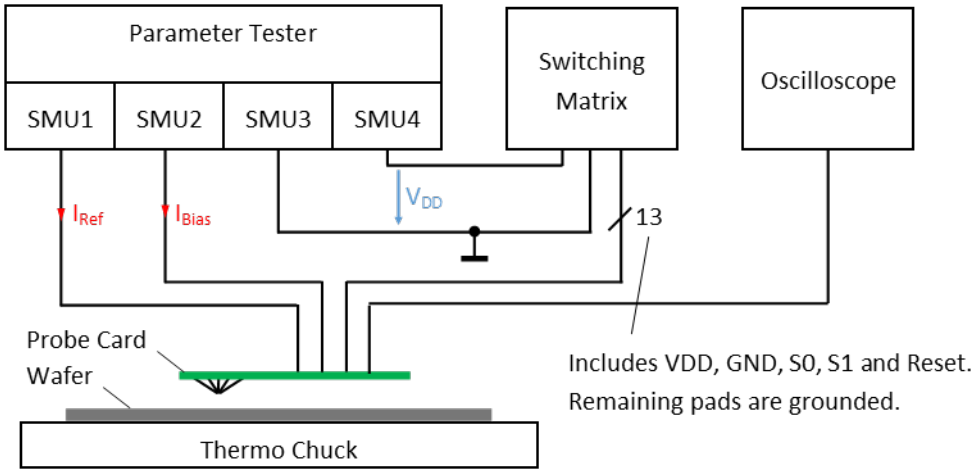

Figure 6.2: Measurement setup for the test structure.

The measurement equipment used is given in table 6.2.

Table 6.2: List of measurement equipment.

Type	Manufacturer	Model
Parameter Analyzer	Agilent	4155B
Oscilloscope	Tektronix	DPO2024
Switching Matrix	Keithley	707A

The test structure is supplied with $V_{DD} = 3.3\,\mathrm{V}$, with a bias current $I_{Bias} = -1\,\mu\mathrm{A}$ and with a reference current $I_{Ref} = -200\,\mathrm{pA}$, where the parameter analyzer has to sink the currents. This is in accordance with the values implemented in section 4.1 and 4.5.

6.2 IDDQ

Before dynamic measurements are performed the consumed current is compared to simulation results. In addition the voltages V_{Bias} and V_{Ref} at the bias current pad and the reference current pad are recorded. The test structure's current consumption may change during the integration of the leakage current. Hence the external **Reset** is *high* during this test. This inhibits any switching and change of internal voltages. The correct operation of the reset is tested in the next section 6.3.
The simulation and measurement are performed with **S0** and **S1** being *low*. The consumed current and both voltages are recorded by the parameter analyzers SMUs. Simulation and measurement results are given in table 6.3.

Table 6.3: Measured DC parameters of ten test structures. The consumed supply current I_{DD}, the voltage V_{Bias} at the bias current pin and the voltage V_{Ref} at the reference current pin are verified by the simulation results.

Test site	I_{DD}	V_{Bias}	V_{Ref}
1	3.6 mA	2.50 V	1.05 V
2	3.6 mA	2.49 V	1.04 V
3	3.5 mA	2.49 V	1.03 V
4	3.6 mA	2.49 V	1.03 V
5	3.6 mA	2.49 V	1.05 V
6	3.5 mA	2.46 V	1.04 V
7	3.5 mA	2.43 V	1.05 V
8	3.6 mA	2.48 V	1.07 V
9	3.5 mA	2.44 V	1.07 V
10	3.6 mA	2.47 V	1.07 V
Measurement Mean	3.6 mA	2.47 V	1.05 V
Simulation	3.64 mA	2.51 V	0.87 V

The test structures current consumption I_{DD} and bias voltage V_{Bias} are close to the simulation results considering the measurement uncertainties. The voltage V_{Ref} on the reference pad is approximately 200 mV higher than its simulated counterpart as given in table 5.1. But it is not limited by its compliance value of 3.3 V and the parameter analyzer shows -200 pA on its port.

6.3 Reset Test

The test structure is reset by the internal **reset** signal and the external **Reset**. The serviceability of both signals has to be investigated using the **output** signal only.
During a *high*-sequence of the **output** signal the external **Reset** is triggered. The **output** has to become **low** immediately and must not change as long as the **Reset** is triggered. A test sequence is printed in figure 6.3.

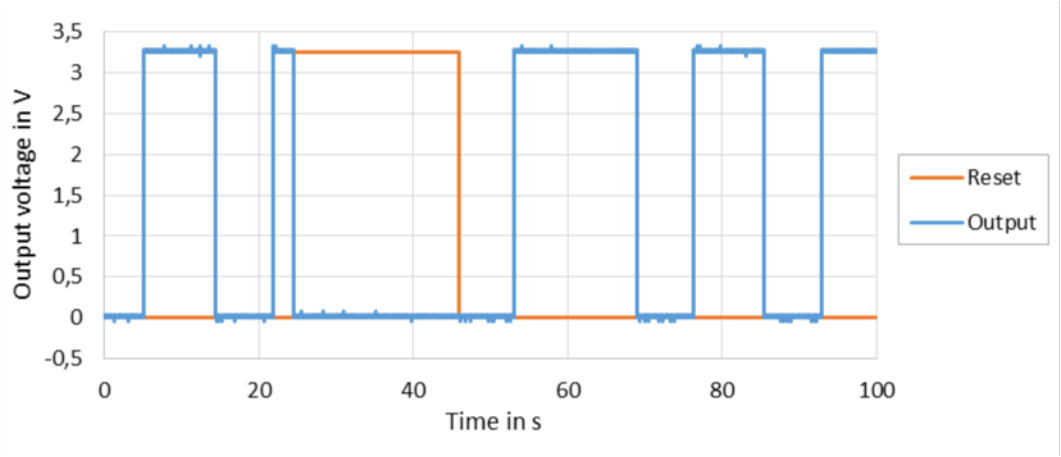

Figure 6.3: Test of the reset. On a reset the **output** has to be *low*, i.e. the output voltage has to be 0 V. The external **Reset** is given by the orange line. The delay between **Reset** switching to 0 V and the output voltage becoming 3.3 V is the time the integration capacitor takes to be charged, i.e. the amplifier output voltage V_A reached the lower pass voltage V_{Pl}. The test structure resets itself once V_A reaches the higher pass voltage V_{Ph}.

The external **Reset** forces the **output** to *low* as demanded.
Figure 6.3 also shows two output *high*-sequences after the **Reset**. This indicates, that the internal **reset** is triggered once the amplifier output voltage V_A reaches the higher pass voltage V_{Ph}. Therefore the whole reset mechanism is operational.

6.4 Evaluation of Measurement Readings

The basic functionality of the test structure has been investigated by IDDQ and reset test. The **output** signal is recorded for each test site listed in table 6.1 and each **S0**-**S1**-combination. Therefore the external **Reset** is triggered every time the select signals **S0** and **S1** are changed.
The simulation results printed in figure 5.11 suggest a constant integration time Δt. This is not true for the measurement record. The measured integration time is strongly varying. The oscilloscope's reading for test site 1 and for both select signals **S0** and **S1** being *low* is shown in figure 6.4 as an example.

Furthermore this is also the case when using the reference current source, i.e. **S0** and **S1** are *high*. Thus there is no definite confirmation for the reference current to be conducted to the integration capacitor.
Noise from the amplifier or the voltage divider providing the pass voltages may potentially cause the variation in integration time. The mean integration time $\overline{\Delta t}$ for each record is computed using a Matlab routine. The calculated mean integration times along with the leakage currents and capacitances obtained by solving the system of equations 3.4 are listed in table 6.4.

The results exhibit a strong deviation and are far from the nominal values given in chap-

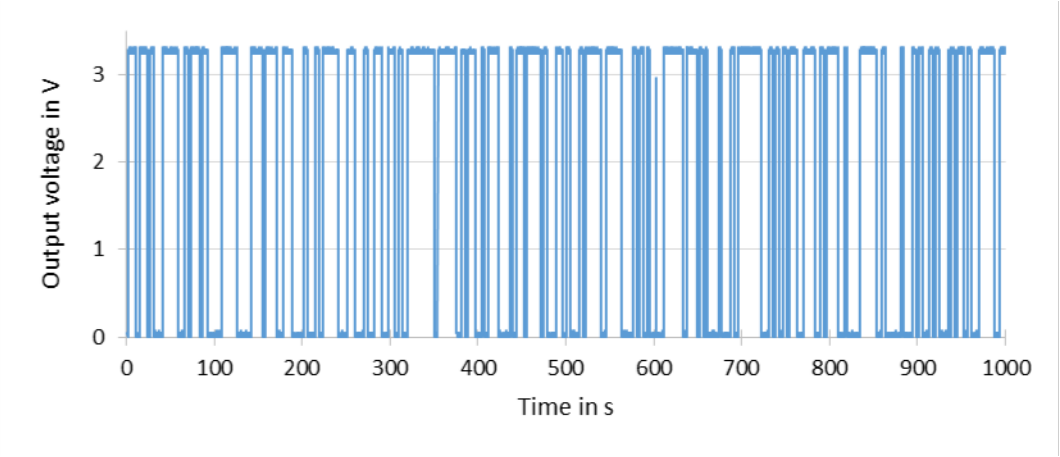

Figure 6.4: Output voltage of test site 1 recorded for the first line of the system of equations 3.4, i.e. **S0** and **S1** are *low*. The integration time shows strong variation.

Table 6.4: Mean integration times $\overline{\Delta t}$ for the ten test structures. The mean integration time is obtained by Matlab. The DUT leakage current and the integration capacitance are determined by solving the system of equation 3.4 for these integration times.

Test site	$\overline{\Delta t_1}$	$\overline{\Delta t_2}$	$\overline{\Delta t_3}$	$\overline{\Delta t_e}$	I_{D1}	I_{D2}	C_1	C_2
1	1.80 s	0.46 ms	0.92 s	2.47 ms	274 fA	537 fA	61.8 pF	30.9 fF
2	2.53 s	0.41 ms	5.11 s	2.53 ms	200 fA	99 fA	63.3 pF	5.1 fF
3	2.46 s	3.04 ms	1.79 s	2.38 ms	193 fA	266 fA	59.5 pF	101.1 fF
4	8.91 s	0.57 s	2.84 s	3.14 ms	71 fA	221 fA	78.5 pF	15.8 pF
5	1.75 s	0.97 s	2.40 s	2.53 ms	289 fA	211 fA	63.3 pF	25.6 pF
6	9.06 s	1.56 s	5.33 s	3.57 ms	79 fA	134 fA	89.3 pF	26.1 pF
7	5.46 s	1.64 s	4.52 s	3.26 ms	119 fA	144 fA	81.5 pF	29.6 pF
8	5.22 s	1.74 s	6.11 s	2.99 ms	115 fA	98 fA	74.8 pF	21.3 pF
9	1.50 s	1.48 s	4.02 s	2.29 ms	305 fA	114 fA	57.3 pF	21.1 pF
10	3.13 s	2.74 s	3.52 s	3.61 ms	231 fA	205 fA	90.3 pF	70.3 pF

ter 4. Another attempt is to plot the distribution of the integration times and use the most common one $\widetilde{\Delta t}$. The distribution of the integration time for test site 1 and both select signals **S0** and **S1** being *low* is printed in figure 6.5.

This plot is evaluated for each test site and select signal combination. The most common integration times $\widetilde{\Delta t}$ and the leakage currents and capacitance resulting from the system of equations 3.4 are listed in table 6.5.

The leakage currents and capacitance show strong variation and deviate from the nominal values given in chapter 4. Therefore this first realization of the test structure has to be reported inoperative for the time being. Further investigations require a rework of the test structure layout featuring pads connected to internal signals. Thus the front stage output voltage V_{FS}, the amplifier output voltage V_A and the comparator signals **loComp** and

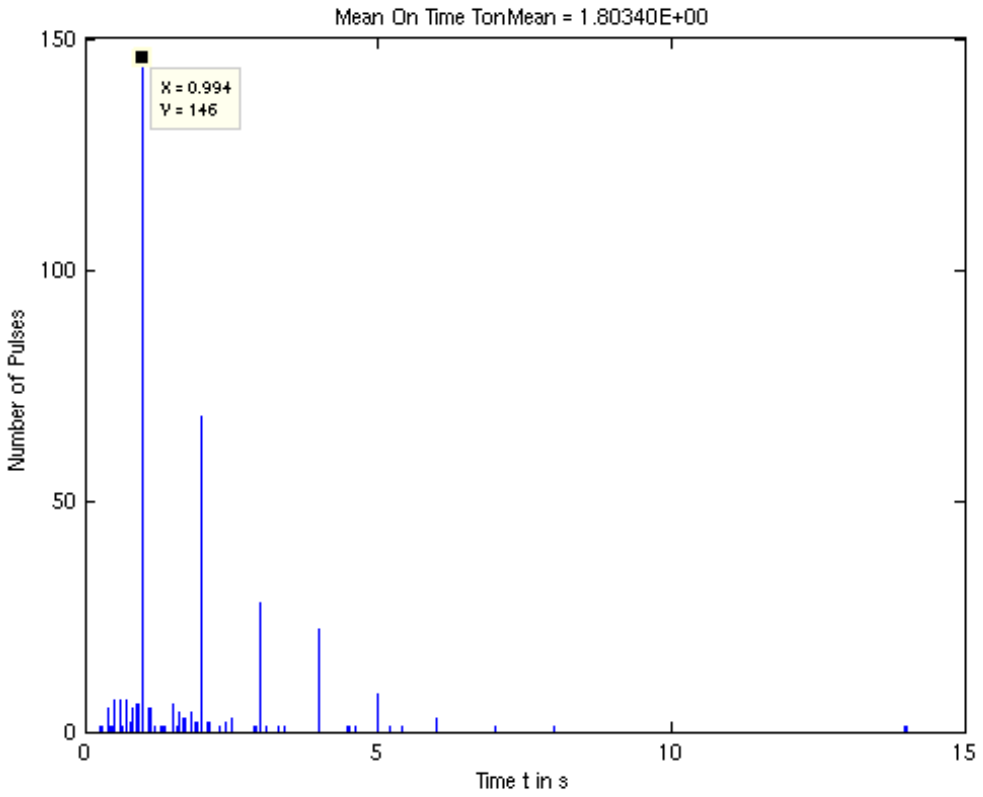

Figure 6.5: Distribution of the integration time for test site 1 and the first line of the system of equations 3.4, i.e. **S0** and **S1** are *low*. The integration time occuring the most is used for further analysis.

hiComp are accessible. This would allow for detection of the malfunctioning component.

Table 6.5: Most common integration times $\widetilde{\Delta t}$ for the ten test structures. The integration times are assigned to bins and plotted by Matlab. The most common ones are listed here. The DUT leakage current and the integration capacitance are determined by solving the system of equation 3.4 for these integration times.

Test site	$\widetilde{\Delta t_1}$	$\widetilde{\Delta t_2}$	$\widetilde{\Delta t_3}$	$\widetilde{\Delta t_e}$	I_{D1}	I_{D2}	C_1	C_2
1	0.99 s	0.1 ms	1.00 s	0.99 ms	200 fA	198 fA	24.75 pF	2.48 fF
2	2.00 s	0.1 ms	1.00 ms	1.00 ms	100 fA	200 pA	25.00 pF	2.50 pF
3	2.00 s	0.1 s	1.00 s	0.99 ms	99 fA	198 fA	24.75 pF	2.48 pF
4	2.99 s	1.0 s	1.00 s	1.01 ms	68 fA	202 fA	25.25 pF	25.25 pF
5	1.00 s	1.0 s	2.00 s	1.00 ms	200 fA	100 fA	25.00 pF	12.50 pF
6	5.00 s	1.0 s	1.99 s	1.00 ms	40 fA	101 fA	25.00 pF	12.60 pF
7	2.00 s	1.0 s	1.00 s	1.00 ms	100 fA	200 fA	25.00 pF	25.00 pF
8	2.00 s	1.0 s	4.00 s	1.00 ms	100 fA	50 fA	25.00 pF	6.25 pF
9	2.00 s	1.0 s	2.00 s	1.00 ms	100 fA	100 fA	25.00 pF	12.50 pF
10	2.00 s	1.0 s	1.01 s	1.00 ms	100 fA	198 fA	25.00 pF	24.75 pF

6.5 Reference Devices

A predefined SLM is fabricated next to the test structures. This SLM3 features the same devices used as leakage current DUT in the actual test structures. There are two devices available to extract the area I_A and perimeter I_P component of the leakage current. The individual currents are referred to as I_{ARD} for the area and I_{PRD} for the perimeter reference device.
The reference SLM is measured at elevated temperatures. Thus the leakage current increases in an exponential manner as discussed in section 2.1. A parameter analyzer usually suffices for the measurement.
The reference devices are measured at five different temperatures ranging from 50 °C to 150 °C. Care must be taken to disconnect the probes after each measurement as the needles extend during the heating process. The perimeter reference devices all over the wafer are found to be short-circuited. Thus no precise information on the area and perimeter component can be obtained. But the remaining area device is used to estimate the area current component I_A. The reverse current I_{ARD} of the area reference device recorded over the reverse bias voltage V_{Rev} at different temperatures is shown in figure 6.6.

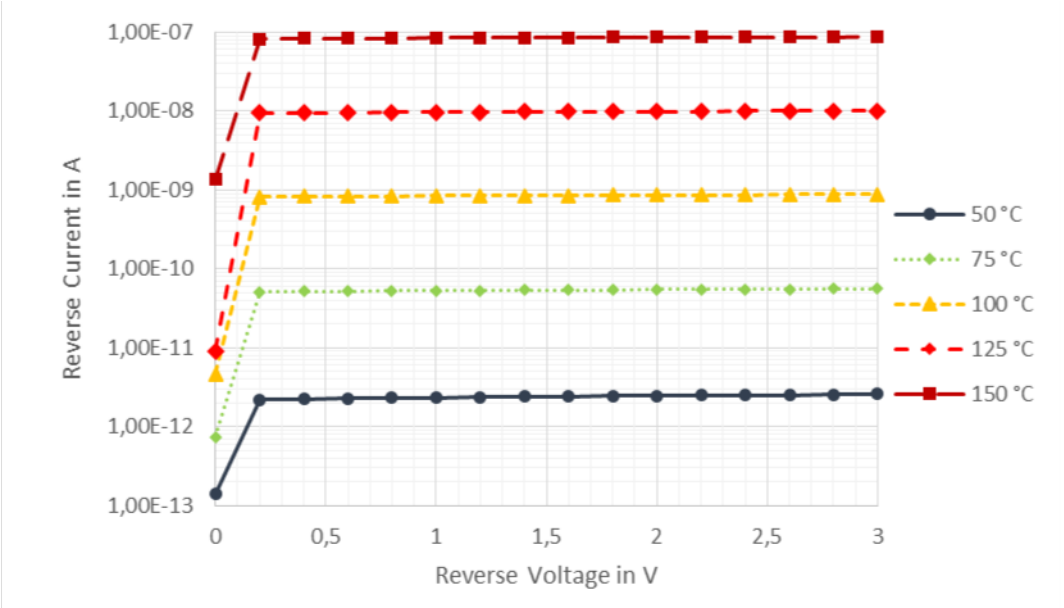

Figure 6.6: Leakage current I_{ARD} of the area reference device over reverse bias voltage V_{Rev}. Semi-logarithmic scale. Temperatures ranging from 50 °C to 150 °C.

The reverse current increases in a exponential manner as suggested in section 2.1. For $T = 50\,°C$ the current I_{ARD} of approximately 3 pA is considered too small to be measured accurately. It is therefore excluded from further discussions.
The reverse current at a reverse bias voltage of $V_{Rev} = 3\,V$ is extrapolated to $T = 25\,°C$ using a simple exponential fit, as printed in figure 6.7.

According to the extrapolated fit the area reference device current at $T = 25\,°C$ is approximately $I_{ARD} = 400\,fA$.

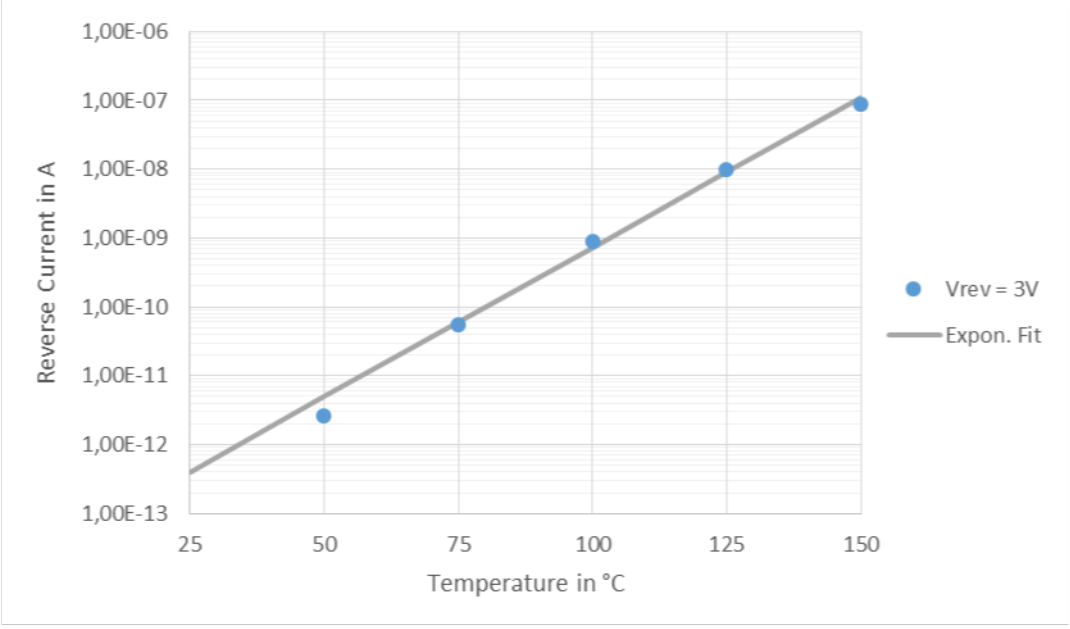

Figure 6.7: Leakage current I_{ARD} of the area reference device over temperature. Semi-logarithmic scale. $V_{Rev} = 3\,\mathrm{V}$. The data at $T = 50\,^{\circ}\mathrm{C}$ is omitted for the simple exponential fit.

The specific area and perimeter current, $J_A = 2.8\,\mu\mathrm{A/m^2}$ and $J_P = 7.59 \cdot 10^{-12}\,\mathrm{A/m}$ are given by the process parameter document. With diode dimensions of $A = 70 \times 250\,\mu\mathrm{m}^2$ the ideal area reference device current according to equation 2.12 becomes

$$
\begin{aligned}
I_{ARD,i} &= A \cdot J_A + P \cdot J_P \\
I_{ARD,i} &= 17.5 \cdot 10^{-9}\,\mathrm{m^2} \cdot 2.8\,\mu\mathrm{A/m^2} + 640\,\mu\mathrm{m} \cdot 7.59 \cdot 10^{-12}\,\mathrm{A/m} \\
I_{ARD,i} &= 53.9\,\mathrm{fA}
\end{aligned}
$$

Thus the extrapolated value is approximately one order of magnitude bigger than the ideal reference value $I_{ARD,i}$. This is potentially due to the missing perimeter component from the second device.
The reason for the short-circuited perimeter device was not identified by the time this thesis was concluded.

Chapter 7

Conclusion

A test structure capable of measuring low current, e.g. leakage currents at room temperatures is designed. The test structure requires little area and is therefore suitable for fabrication in a scribe line module. This furthermore allows for recording a large number of devices and deduce statistical quantities for device characterization.
In addition to the low currents the design measures the capacitance used to convert the current into a voltage slope. This slope is detected by defining two potentials and measuring the time it takes the capacitor voltage to pass the interval between them. The external measurement equipment records this integration time and solves a linear system of equations to calculate the current and capacitance.
Simulations indicate a nominal deviation between the calculated and simulated leakage current in the low percentage range. The variation due to device mismatch must be lower then variations of the current itself. Monte-Carlo simulations are used to prove this matter. They suggest a small variation of the results.
The test structure is manufactured in a 0.35 um CMOS process technology. Measurement data of ten test sites are in good agreement with simulation for terminal voltages and currents. The digital control for DUT selection and the reset mechanism are found to be functional.
Measured integration time data show strong fluctuations and two statistical attempts for extracting leakage current and capacitance values are introduced and discussed.
Parameters are determined for ten test sites and a reference diode where reasonable differences are found between each structure.
As there are no pads available for sensing internal circuit nodes viable measurements and investigations are presented.

7.1 Future Works and proposed Improvements

For further investigation the test structure has to be fabricated with additional pads connected to internal signals. Thus the reason for the fluctuations can be localized and the corresponding component redesigned.

In addition some proposed improvements have been deduced while the test structure was fabricated. This improvements focus on the front stage.
Simulations show that only a small portion of the leakage current is lost due to devices connected to the integration node. Thus both DUTs and the external reference current source are placed into a single front stage. This reduces the error caused by capacitance mismatch and requires less area.
Furthermore the measurement time is reduced by charging both capacitors with the reference current instead of only one.
A fifth equation is added to the system. By applying a well defined voltage slope du_e/dt at the integration node the voltage interval Δv and the gain G can be obtained.
Alongside the previous improvements an adjustment is put into effect. The system of equations 3.4 is reformulated to result in the area and perimeter specific currents and capacitance, i.e. J_A, J_P, c_A and c_P. It therefore takes the DUT area A_D, the DUT perimeter P_D, the capacitor area A_C and the capacitor perimeter P_C into account. The improved system of equation becomes

$$\begin{bmatrix} A_{D1} & P_{D1} & -\frac{A_{C1}}{\Delta t_1} & -\frac{P_{C1}}{\Delta t_1} & 0 \\ A_{D2} & P_{D2} & -\frac{A_{C1}}{\Delta t_2} & -\frac{P_{C1}}{\Delta t_2} & 0 \\ 0 & 0 & \frac{A_{C1}}{\Delta t_3} & \frac{P_{C1}}{\Delta t_3} & 0 \\ 0 & 0 & \frac{A_{C2}}{\Delta t_4} & \frac{P_{C2}}{\Delta t_4} & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{\Delta t_5} \end{bmatrix} \cdot \begin{pmatrix} J_A \\ J_P \\ \frac{\Delta v}{G} \cdot c_A \\ \frac{\Delta v}{G} \cdot c_P \\ \frac{\Delta v}{G} \end{pmatrix} = \begin{pmatrix} 0 \\ 0 \\ I_e \\ I_e \\ \frac{du_e}{dt} \end{pmatrix}$$

The test structure can be reduced when the simultaneous measurement of the capacitance is not required. The simplified system of equations allows for the calculation of the currents only.

$$\begin{bmatrix} A_{D1} & P_{D1} & -\frac{1}{\Delta t_1} \\ A_{D2} & P_{D2} & -\frac{1}{\Delta t_2} \\ 0 & 0 & \frac{1}{\Delta t_3} \end{bmatrix} \cdot \begin{pmatrix} J_A \\ J_P \\ \frac{\Delta v}{G} \cdot C \end{pmatrix} = \begin{pmatrix} 0 \\ 0 \\ I_e \end{pmatrix}$$

The capacitance switching can be improved as well. There is still a small amount of current flowing into a disconnected PIP capacitor. This is due to the depletion layer capacitance of the transistor used to disconnect the bottom plate. In lieu of disconnecting the bottom plate of the capacitors they can be connected to the front stage output. Thus the parasitic capacitance of the transistor is charged by the source follower instead of the leakage current.

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