Ing. Philipp Schneider, BSc

Modelling and simulation of noise sources and propagation paths in 65 nm CMOS microcontrollers

MASTER'S THESIS

to achieve the university degree of

Master of Science

Master's degree programme: Electrical Engineering

submitted to

Graz University of Technology

Supervisor

Ass.Prof. Dipl.-Ing. Dr.techn. Gunter Winkler
Univ.-Prof. Dipl.-Ing. Dr.techn. Bernd Deutschmann

Institute of Electronics

Dipl.-Ing. Thomas Steinecke
Principal EMC Design Microcontrollers of Infineon Technologies AG

Graz, June 2015

AFFIDAVIT

I declare that I have authored this thesis independently, that I have not used other than the declared sources/resources, and that I have explicitly indicated all material which has been quoted either literally or by content from the sources used. The text document uploaded to TUGRAZonline is identical to the present master‘s thesis dissertation.

Date

Signature

Confidentiality clause

This master thesis contains confidential data of Infineon Technologies AG.

This work may only be made available to the first and second reviewers and authorized members of the board of examiners. Any publication and duplication of this master thesis - even in part - is prohibited.

An inspection of this work by third parties requires the expressed permission of the author and Infineon Technologies AG.

Sperrvermerk

Das vorliegende Dokument enthält vertrauliche Daten der Firma Infineon Technologies AG.

Veröffentlichungen oder Vervielfältigungen des vorliegen Dokuments, auch nur auszugsweise, sind ohne ausdrückliche Genehmigung der Firma Infineon Technologies AG nicht gestattet.

Das Dokument ist lediglich den betreuenden Professoren zugänglich zu machen.

Ohne schriftliche Genehmigung der Firma darf dieses Dokument nicht in der Bibliothek der Universität ausgelegt werden.

Danksagung

Diese Diplomarbeit wurde am Institut für Elektronik an der Technischen Universität Graz und in der Abteilung IFAG ATV MC D AS EMC an der Firma Infineon Technologies AG durchgeführt.

Ein herzliches Dankeschön geht an alle, die mich bei der Erstellung meiner Diplomarbeit unterstützt haben. Ein besonderer Dank geht an das EMV-Team für Mikrokontroller, im speziellen Jack Kruppa von Infineon Technologies AG, an Ralf Buender von ANSYS, und an die Professoren Gunter Winkler und Bernd Deutschmann für die sehr gute Unterstützung.

Besonders möchte ich mich bei meiner Freundin Kristina Maierhofer bedanken, denn ohne ihre moralische Unterstützung und hilfreichen Anregungen wäre ich niemals fertig geworden.

Philipp Schneider
Graz, Österreich, Mai 2015

Abstract

This thesis deals with the modeling and simulation of a 65 nm Complementary metal-oxide-semiconductor (CMOS) microcontroller in the field of Electromagnetic compatibility (EMC).
Since, the EMC requirements of the automotive industry become more and more stringent, the responsibility is shifted more and more to the integrated circuit (IC) manufacturers in order to observe the specified limits. The automotive industry requests an EMC simulation model for the elimination of sources of interference in the course of the development process already. In this way, the principal of "first time right" is followed. An EMC simulation model for an integrated custom block (chip macro model (CMM)) is a power integrity network model, which describes the switching of the transistors along supply network by a noise generator. Within the scope of this thesis, a dynamic voltage drop power-ground noise model on-chip is developed. In particular, CMM of a phase locked loop (PLL) on a microcontroller chip is created.
The results of the CMM show a quantitative agreement of the harmonic frequencies with the measurement results.

Kurzfassung

Die vorliegende Arbeit beschäftigt sich mit der Modellierung und Simulation eines 65 nm CMOS-Mikrocontrollers im Bereich Elektromagnetische Verträglichkeit (EMV).
Da die EMV-Anforderungen seitens der Automobilbranche immer strenger werden, wird der IC Hersteller immer mehr in die Pflicht genommen um diese Anforderungen einzuhalten zu können. Der Automobilsektor erwartet sich ein EMV-Simulationsmodell, um bereits im Entwicklungsprozess Störquellen erkennen und beseitigen zu können. Ein EMV-Simulationsmodel für einen kundenspezifischen Funktionsblock (CMM) ist ein power integrity-Model, dass die schaltenden Transistoren über die Versorgungsleitungen als Rauschgenerator darstellt.
In dieser Arbeit wurde ein "Dynamic Voltage Drop power-ground noise"-Models einer phase locked loop auf einem Mikrocontroller erstellt. Die Modellierung und Simulation wurde mit dem Layout-basiertem Tool *Totem* von der Firma *ANSYS* durchgeführt.
Die Ergebnisse der Simulation des CMM zeigen eine quantitative Übereinstimmung der harmonischen Frequenzen mit den Messergebnissen.

Contents

List of Abbreviations

BGA	ball grid array. 58
CGU	clock generation unit. 33
CMM	chip macro model. 9, 11, 24, 36, 37, 50, 53, 59, 62
CMOS	Complementary metal-oxide-semiconductor. 9, 11
CPM	chip power model. 60, 62
dB	decibel. 56
DC	direct current. 20, 40, 54, 55
DCO	Digitally Controlled Oscillator. 46
DCRO	Digitally Controlled Ring Oscillator. 45, 46
DSM	Delta Sigma Modulator. 45, 46
DVD	Dynamic Voltage Drop. 11, 25, 36, 38, 51
ECU	electronic control unit. 28
EM	electro migration. 35
EMC	Electromagnetic compatibility. 9, 21, 23, 24, 26, 28, 32
EMI	Electromagnetic Interference. 20, 32, 58, 60–62
EMV	Elektromagnetische Verträglichkeit. 11
FFT	Fast Fourier Transformation. 52
FM	frequency modulation. 20, 33, 54–57, 59
GDS	Graphic Database System. 35
GND	ground. 25

IC	integrated circuit. 9, 11, 21, 23, 24, 26, 28, 29, 35, 49, 59
IP	intellectual property. 35
IVR	internal voltage regulator. 45, 46
MUX	Multiplexer. 45
PCB	printed circuit board. 35, 42, 49, 58, 60, 62
PDN	Power Distribution Network. 23, 25, 40, 41, 59, 60
PI	power integrity. 9, 11, 23, 24, 36, 38
PLL	phase locked loop. 9, 11, 20, 24, 33, 36, 38, 45–47, 53–57, 59, 60
PQ	Phase Quantizer. 45, 46
PSD	Power Spectral Density. 20, 54, 55
RAM	random-access memory. 30
RC	resistor capacitor. 38, 41
RF	radio frequency. 28
RLC	resistor-inductor-capacitor. 38, 41, 49
RTL	Register Transfer Language. 35
SoC	System on Chip. 24, 35, 58
SPICE	Simulation Program with Integrated Circuit Emphasis. 35, 47, 60
SSCG	Spread Spectrum Clock Generator. 33, 55, 60
SysclkPLL	System Clock Phase Locked Loop. 19, 45
uC	microcontroller. 19, 24, 27, 30, 31, 33
UIF	Universal Interference Model. 32
VCO	voltage controlled oscillator. 20, 33, 46, 54–57
VDD	power supply voltage. 25, 41
VSSA	Voltage Source Source Analog. 53

List of Figures

List of Tables

CHAPTER 1

Problem statement, research objectives and outline

1.1 Introduction

Microelectronics have become integral parts of this world. Especially in auto-mobility, there are a variety of complex IC with different tasks. These ICs are distributed throughout an automobile on various control devices. The core part of each controller is its microcontroller in which the most important operations are performed.
The performance of a microcontroller is dependent on the number of its transistors. For this reason, smaller technology nodes need to be developed, in order to be able to increase the number of transistors on the same size of chip area. At the same time, the supply voltage is reduced and decreases the power consumption needed. However, this technology trend is effecting the Power Distribution Network (PDN) on-chip inducing larger dynamic voltage fluctuations due to dynamic voltage drop, $L \cdot \frac{\mathrm{d}i}{\mathrm{d}t}$ noise or LC resonance [10]. These three effects have a significant negativ impact on the EMC performance of an IC.

The quality analysis of the PDN of an IC is the so-called power integrity (PI). And verifies the supply voltage fluctuating in a defined voltage (e.g. $\pm$ 10%) range.

1.2 Problem Statement and Motivation

Since, the EMC requirements of the automotive industry become more and more stringent, the responsibility is shifted more and more to the IC manufacturers in order to observe the specified limits. The automotive industry requests an EMC simulation model for the elimination of sources of interference in the course of the development process already. In this way, the principal of "first time right" is followed. An EMC simulation model is a PI network model, which describes the switching of the transistors along supply network by a noise generator.
Within the scope of this thesis, a dynamic voltage drop power-ground noise model on-chip is developed. In particula, chip macro model (CMM) of a PLL on a 65 nm micro-controller chip is created. A PLL is a control system synchronising an oscillator or a precise clock source with an input signal [11]. A layout based modelling and circuit simulation is generated by use of the software Totem/RedHawk by ANSYS, formerly known Apache.

The objectives of this masters thesis is the development of a PLL model and its correlation with measurements results.

1.3 Outline: The roadmap through this thesis

First, the literature on test specifications of conducted emissions measurements are reviewed. Next, the largest sources of interference of the uC used in this study are discussed. Thereafter, the state of the art EMC technology for System on Chip (SoC) PI verification is described in detail. Finally, the study results are presented and the conclusion and future prospects conclude this thesis.

CHAPTER 2

Theoretical Background

2.1 Indroduction

The transistors connected to a power supply voltage (VDD) or ground (GND) cause current peaks at the PDN when switched. This process is called a Dynamic Voltage Drop (DVD). A PDN, considered as short transmission line, consists of a resistance load per unit length R', an inductance per unit length L', an admittance per unit length, and a capacity per unit length according to the transmission line theory [12, pp. 1192-1203].

$$\frac{\mathrm{d}U}{\mathrm{d}z} = -\left(R' + jwL'\right) I \tag{2.1}$$

$$\frac{\mathrm{d}I}{\mathrm{d}z} = -\left(G' + jwC'\right) U \tag{2.2}$$

Considering only the time change of the voltage reduces to the following equations [13, pp. 38-42]:

$$u(t) = i(t)R + L * \frac{\mathrm{d}i(t)}{\mathrm{d}t} \tag{2.3}$$

$$i(t) = C * \frac{\mathrm{d}u(t)}{\mathrm{d}t} \tag{2.4}$$

The equation 2.3 shows that all parasitic components are used. The smaller the change in current, the smaller the change in voltage becomes when neglecting the resistance. As already mentioned in chapter 1.1, the power supply is restricted may to vary only within a predefined voltage range.

2.2 Test Specification

2.2.1 Indroduction

In the generic IC EMC Test Specification of ZVEI (German Electrical and Electronic Manufacturers e. V.) all standards and directives are summarized.

2.2.2 Bandwidth of Digital Waveforms

The clock of digital circuits can be represented piecewise-linear as shown in figure 2.1. In addition, a rise time τ_r and fall time τ_f is defined. Generaly, the rise and fall times are predetermined at 10% and 90% of the level A respectively, see figure 2.1 where τ_r is the rise time and τ_f is the fall time.
The emission limits 2.2.3 in the regular frequency range are therefore strongly dependent on the rise time and fall time. The duration of the pulse τ is defined at $\frac{A}{2}$ [1].

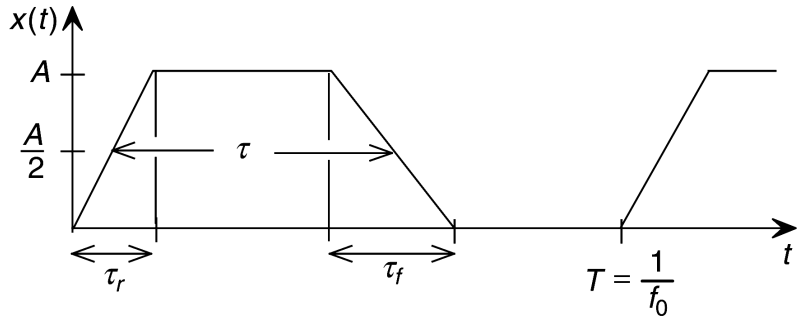

Figure 2.1.: Periodic trapezoidal pulse train [1]

The calculation of the Fourier coefficients gives the following result:

$$c_n = 2A\frac{\tau}{T}\left|\frac{sin(\pi\, f\, \tau)}{\pi\, f\, \tau}\right|\left|\frac{sin(\pi\, f\, \tau_r)}{\pi\, f\, \tau_r}\right| \qquad \tau_r = \tau_f \tag{2.5}$$

The equations 2.6 and 2.7 shows the effect of Rise/Fall-time on Spectral Content:

$$\Theta_n = 2A\frac{\tau}{T}\left|\frac{sin(\frac{n\pi\tau}{T})}{\frac{n\pi\tau}{T}}\right|\left|\frac{sin(\frac{n\pi\tau_r}{T})}{\frac{n\pi\tau_r}{T}}\right| \qquad \tau_r = \tau_f \tag{2.6}$$

$$20\,log_{10}(\Theta_n) = 20\,log_{10}(2A\frac{\tau}{T}) + 20\,log_{10}\left|\frac{sin(\frac{n\pi\tau}{T})}{\frac{n\pi\tau}{T}}\right| + 20\,log_{10}\left|\frac{sin(\frac{n\pi\tau_r}{T})}{\frac{n\pi\tau_r}{T}}\right| \tag{2.7}$$

The spectrum of the periodic trapezoidal pulse signal looks like 2.2, and illustrates that the first bend is located at $\frac{1}{\pi\tau} = \frac{f_0}{\pi D}$ and the second bend at $\frac{1}{\pi\tau_r}$.

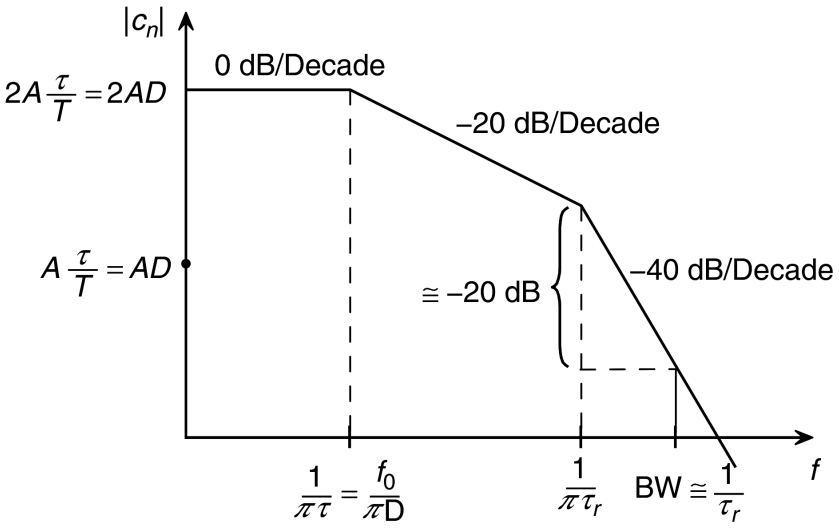

Figure 2.2.: Spectral bounds of a periodic trapezoidal pulse train [1]

With respect to this definitions, the test specifications of the emission limits for uCs can be derived.

2.2.3 Generic IC EMC Test Specification

In this document the technical basis for the definition and characterization of the EMC behavior of an IC in terms of radio frequency (RF) emission and immunity in the frequency range from $150\,kHz$ to $1\,GHz$ is defined. [2]

EMC limits for automotive ICs

All pins used for EMC in an automotive IC have to be defined according to the limits given in the following chapters.
The limit classes are according to the requirements given by the application. The EMC requirements are defined by the application itself, electronic control unit (ECU) housing, number of power grounds, etc.

Table 2.1.: EMC limits for automotive ICs [2, pp. 50]

limit class	description
I	low EMC requirement
II	medium EMC requirement
III	high EMC requirement
C	customer specific
C-BS	customer specific: external bus systems

Emission level scheme

The level scheme shown in figure 2.3 describes the emission levels of ICs in a easy way.

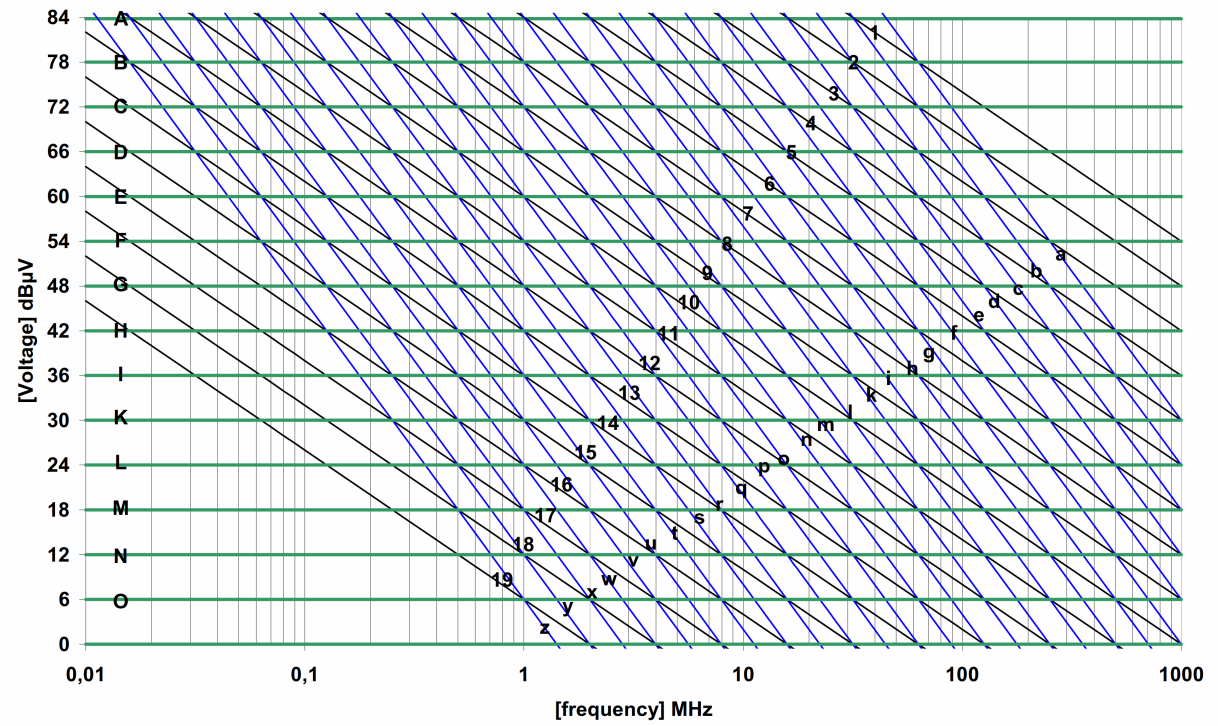

Figure 2.3.: Emission level scheme according IEC61967-2 and IEC61967-4 [2, pp. 50]

First, the correct emission level and the class limit for the pin used with the correct functionality and operating modes are selected by means of 2.4. Switching digital data pins, analogue power outputs and many other disturbance sources produce switching harmonics. The spectrum is calculated by Fourier transformation of the signal waveform as described in 2.2.2.

Limit class	150 Ω method		1 Ω method		TEM cell method
	global	*local*	*global*	*local*	
I	8-H	6-F	10-K	8-H	I
II	10-K	8-H	12-M	10-K	L
III	12-M	10-K	14-O	12-M	N
C	*customer specific*				

Figure 2.4.: General emission limit classes [2, pp. 51]

Emission limits for uCs with external digital bus systems

Adapted limits customer specific for external bus systems of uCs with RAM or flash in a 'Worst case' setting configuration and software loop with random-access memory (RAM) copy.
The following limits were used in this thesis as a reference, because the measurements were performed with the 150 Ω conducted emission method.

Conducted emission 150 Ω limit port pins:

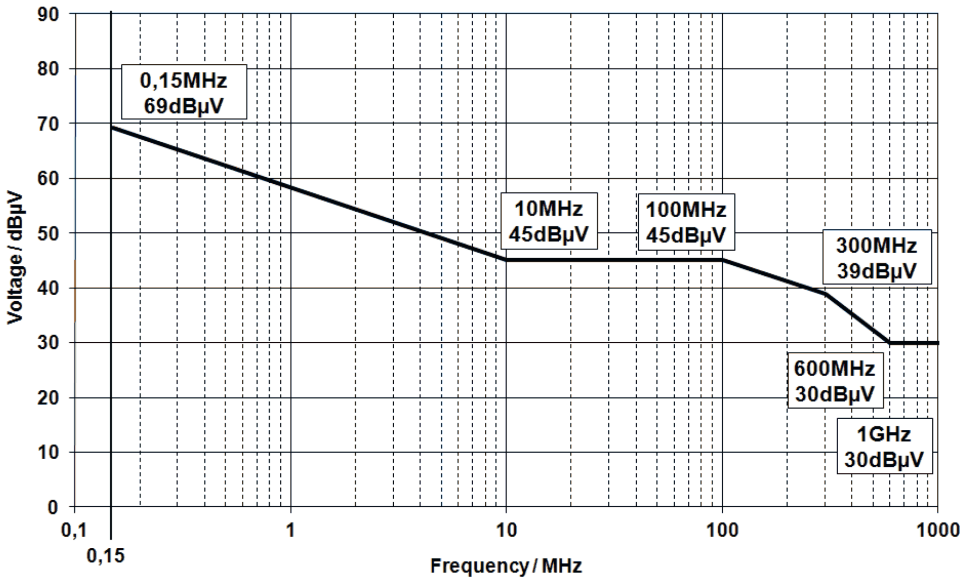

Figure 2.5.: Limit line conducted emission 150Ω for port pins of uCs with external digital bus systems [2, pp. 53]

Conducted emission 150Ω limit supply pins:

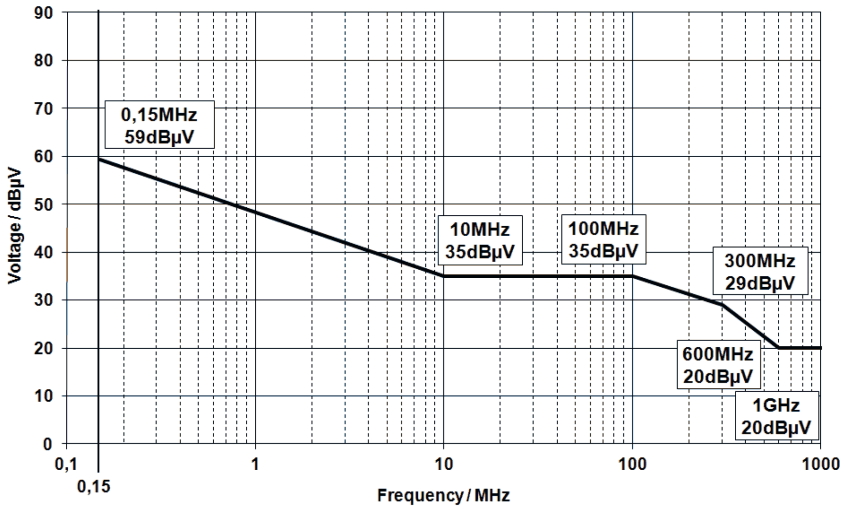

Figure 2.6.: Limit line conducted emission 150Ω for supply pins of uCs with external digital bus systems [2, pp. 53]

2.3 Largest sources of interference of a microcontroller

2.3.1 Introduction to EMC

The figure 2.7 gives an overview of the EMC Universal Interference Model (UIF). This coupling between the source and receptor occurs inside of an equipment or outside of an equipment. [3]

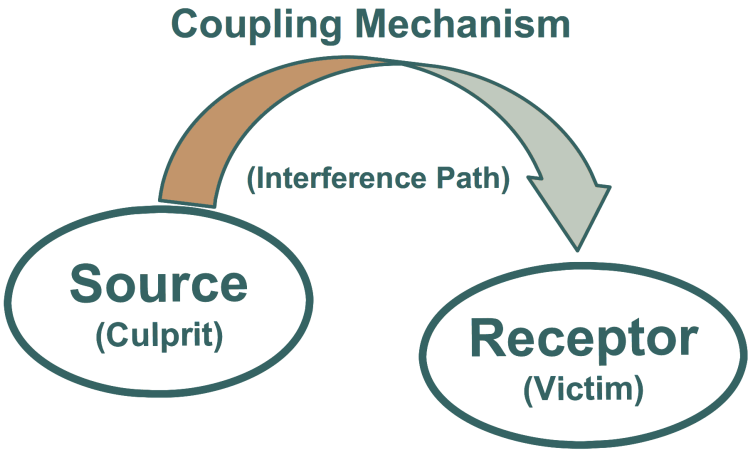

Figure 2.7.: Universal Interference Model [3, pp. 1]

1. Electromagnetic Interference (EMI)
   The UIF model perceives that all EMI conditions given depend on three components:
   - The interference can be created in the source or culprit itself.
   - The coupling mechanism or interference path consists of two main mechanisms: Conduction and Radiation.
   - At the receptor or victim, the interference influences the functionality. Victims are therefore susceptible circuits.
2. Electromagnetic Compatibility (EMC)
   EMC is achieved by changing one or a combination of the three blocks of the UIF. It is carried out by:
   - Reducing the quantity of noise at the culprit.
   - Preventing coupling between source and receptor.
   - Protecting or robustness the victim

2.3.2 Sources of electromagnetic interference

The largest sources of interference of a uC for higher frequencies is the clock generation unit (CGU). This unit is produces a very accurate clock frequency from a PLL. In the PLL is a VCO, which produces an output frequency of $400\,MHz$. The second harmonic of $400\,MHz$ is $2 \cdot 400\,MHz = 800\,MHz$ and lies precisely in the lowest emission limit boundaries, see figures 2.5 for port pins or 2.6 for supply pins.
A suppression of these frequencies by a Spread Spectrum Clock Generator (SSCG) is reached by [4]. Hereby, the narrow-band signal is modulated to the maximum level by a FM in order to control and reduce the emission level and jitter (figure 2.8), so that a trade off between maximum level and cycle to cycle jitter is achieved [14, pp. 6].

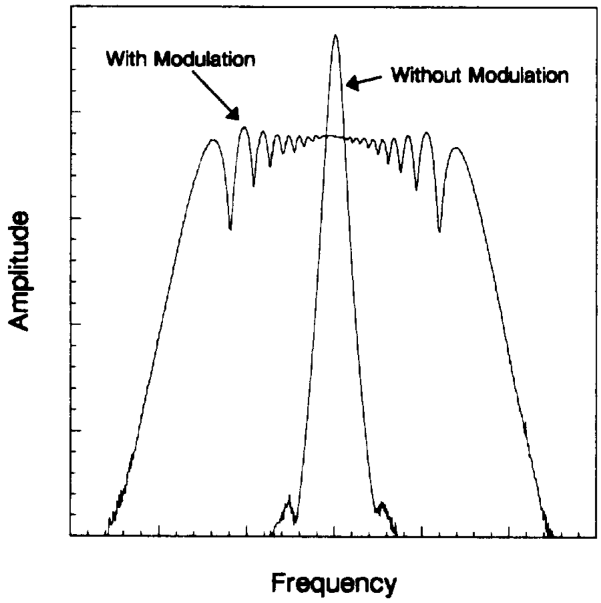

Figure 2.8.: Frequency domain representation at a harmonic of a trapezoidal clock signal with and without SSCG [4]

2.3.3 Interference coupling paths

Essential prerequisite for the technical and economic control of electromagnetic compatibility is the detailed knowledge of the possible parasitic coupling mechanisms between interference sources and receptors 2.7. Furthermore, the influences on the coupling mechanisms and related basic rules need to be known in order to avoid couplings in the system design. [5, pp. 41-58]

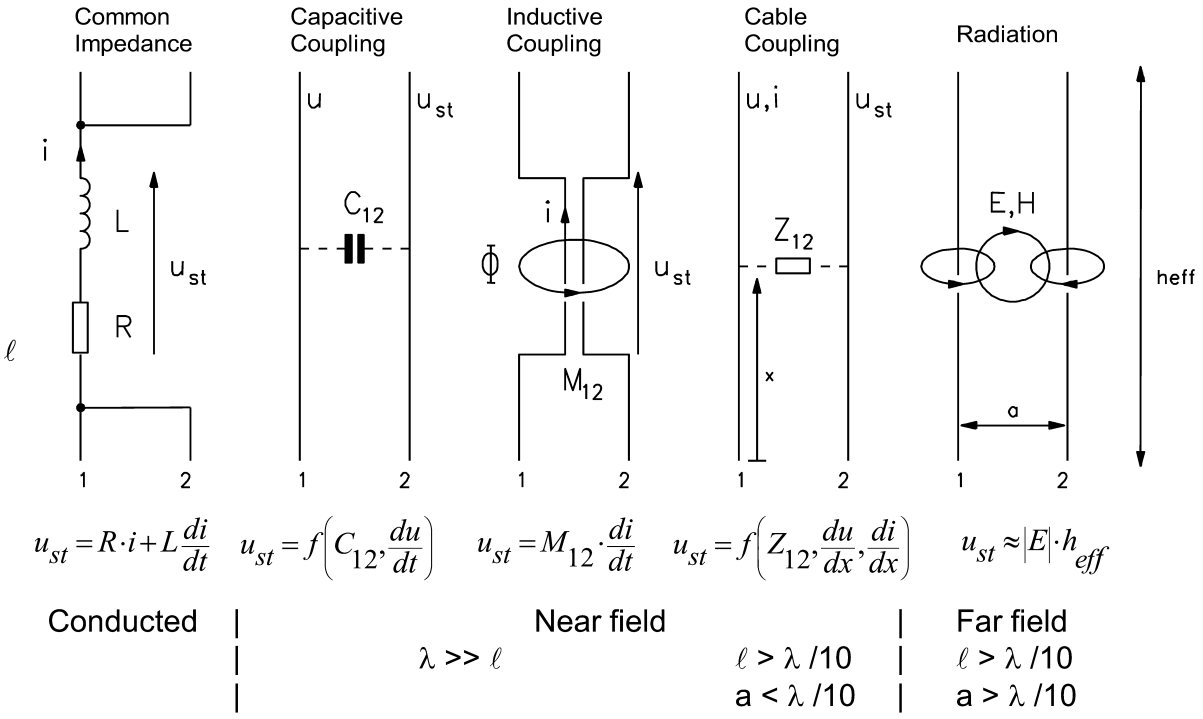

Figure 2.9.: Interference coupling paths [5]

2.4 State of the Art - EMC Tools for SoC Power Integrity Verification

2.4.1 Indroduction

In the field of layout-based power/noise integrity analysis at the on-chip level, there is currently only one useful tool from the company ANYSYS/Apache available. Other companies, e.g. Cadence and Synopsis, set there research focus to chip design and logic-timing verification. The engineering simulation software developer ANSYS has acquired the company Apache in 2011. Thus, ANSYS can provide a complete analyzing tool from the IC to the final products in the near future. [6]

2.4.2 Overview of the noise platform

The noise platform consists of four tools:

- PowerArtist - Register Transfer Language (RTL) Design

  ANSYS PowerArtist allows RTL to Graphic Database System (GDS) design for an early power RTL estimation and analysis for low power consumption. GDS is a database file format for layout data of ICs.

- Totem - Analog intellectual property (IP)

  ANSYS Totem is a transistor-level power-ground noise and an electro migration (EM)-analysis Simulation Program with Integrated Circuit Emphasis (SPICE) level accuracy simulation platform for analog, mixed-signal and custom digital designs.

- Redhawk - SoC Digital

  ANSYS RedHawk is a full-chip cell-based power-ground design and verification platform with a SPICE engine.

- Sentinel-SSO - Package and System

  ANSYS Sentinel-SSO is a power noise and timing analysis tool for printed circuit boards (PCBs).

2.4.3 Totem

The model of the PLL is a PI model for DVD (see 2.4.4). The tool TOTEM can design a model on transistor-level and create a CMM for RedHawk.
One of the fundamental technologies is Totem's Vectorless Dynamic statistical analysis engine (see 2.4.4), which calculates realistic worst-case switching scenarios without requiring functional vectors [6, 7].

TOTEM's features

- Connectivity Analysis
- Static Voltage Drop (IR) Analysis
- Dynamic Voltage Drop (DVD)
- Substrate Noise Coupling
- Reliability Analysis, e.g. EM or ESD

Totem Flow for Chip Macro Model (CMM)

The figure 2.10 shows the basic workflow of the generation of a CMM. In detail, these blocks are explained in chapter 3.

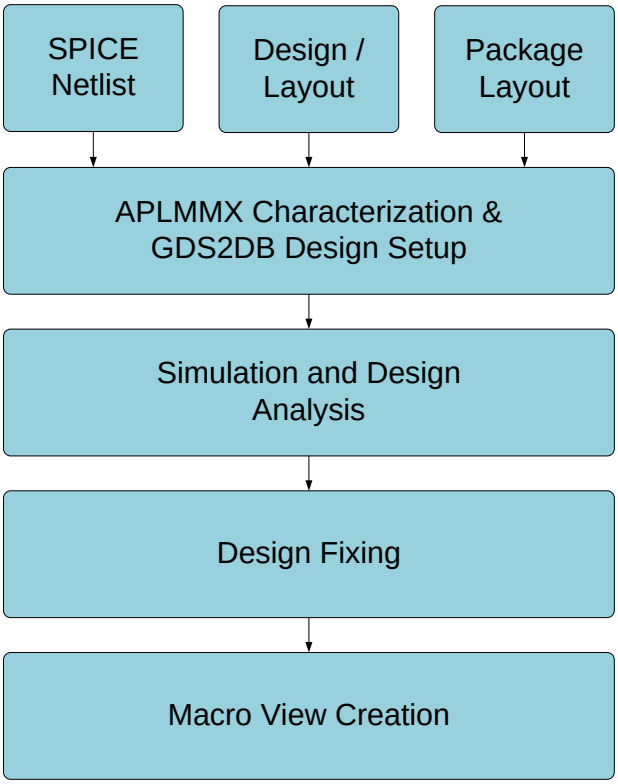

Figure 2.10.: Totem work flow - Chip Macro Model (CMM) [6]

2.4.4 Dynamic Voltage Drop (DVD)

The main purpose of this study is the development of a DVD power-ground noise model of a digital PLL.
In the past, Dynamic Voltage Drop was customary neglected. The Designers assumed that the DVD is avoided by the existing decoupling capacitors, and that the cycle time is long enough to charge the decoupling capacitors. However, if the clock frequency increases, the clock time is not sufficient long to charge the decoupling capacitors. To verify the PI for DVD, all decoupling capacitors need to be extracted and the inputs are determined with increased power consumption, including the register states to subsequently perform a transient simulation on the resulting resistor capacitor (RC) network. [10]

Statistical Vector Less Dynamic Power Supply Analysis

To achieve transistor-level accuracy, the vector less dynamic analysis, which flow is shown in figure 2.11, is composed of three processes: 1. switching scenario creation, 2. resistor-inductor-capacitor (RLC) parasitic extraction, and 3. current-profile characterization and transient simulation. [7]

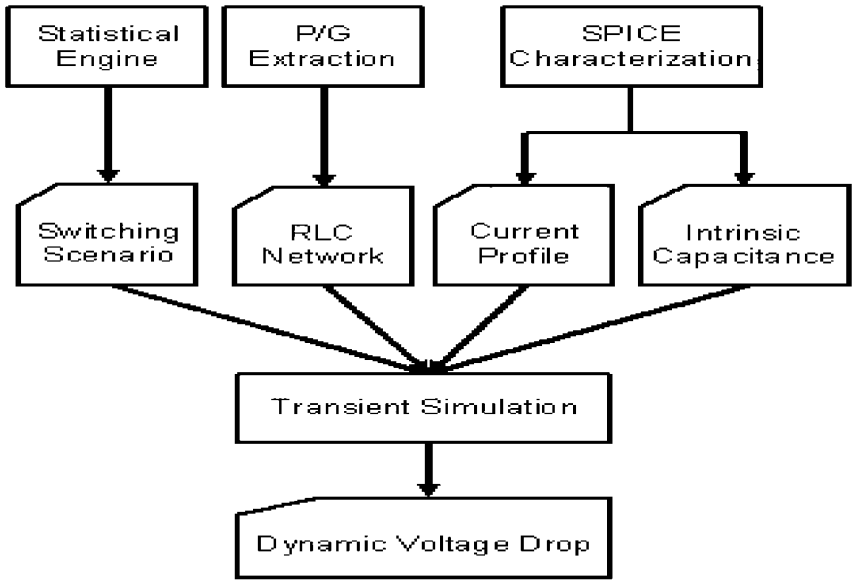

Figure 2.11.: Vectorless Dynamic P/G noise analysis flow [7, pp. 510]

Input Data Preparation for Static Voltage Drop

A DC voltage source modelling the power supply is connected to a chip model. Transistors are modelled as DC average current sources and the PDN is modelled solely by its resistive properties. [6]

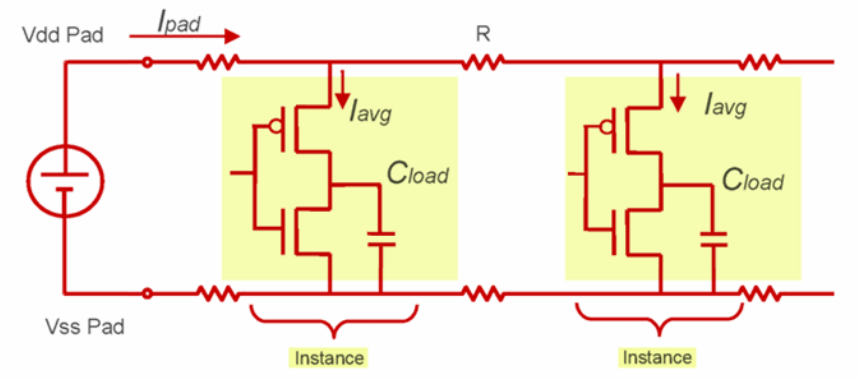

Figure 2.12.: Static IR drop analysis modeling [6]

The modelling of the layout data requires the technology data, the current probes, and the voltage sources.

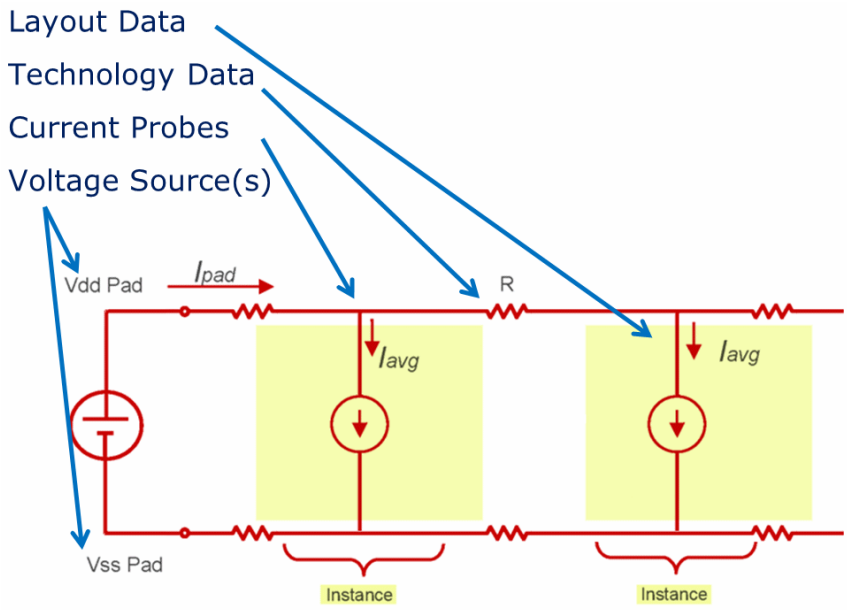

Figure 2.13.: Static IR drop analysis modeling with average current sources [6]

Input Data Preparation for Dynamic Voltage Drop

In the dynamic case, the PDN is modelled with the RLC-network. The current ($i_c(V,t)$) induced by the transistors when switched is dependent on time and voltage concerning dynamic conditions. For the non-switching instance, a RC-network is used for modelling. All capacitive coupling components are included.
The chip model where the transistors are modelled is linked to the power supply. The transistor is modelled as a time-domain current profile which is a function of load, VDD level and input slew. By the R, L and C components the PDN is modelled for dynamic simulation. [6]

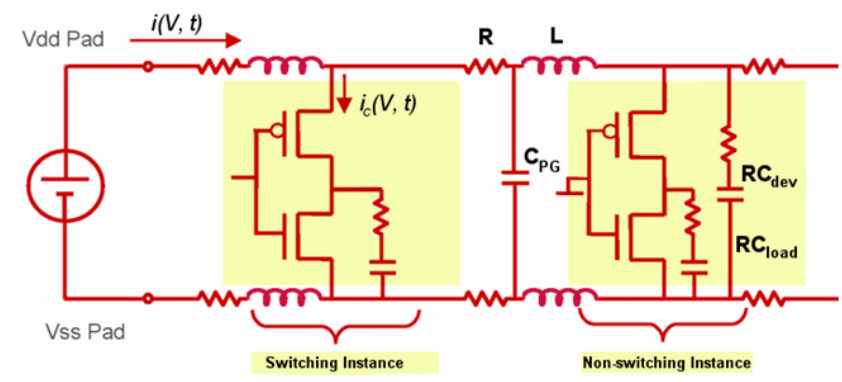

Figure 2.14.: Dynamic voltage drop analysis modelling [6]

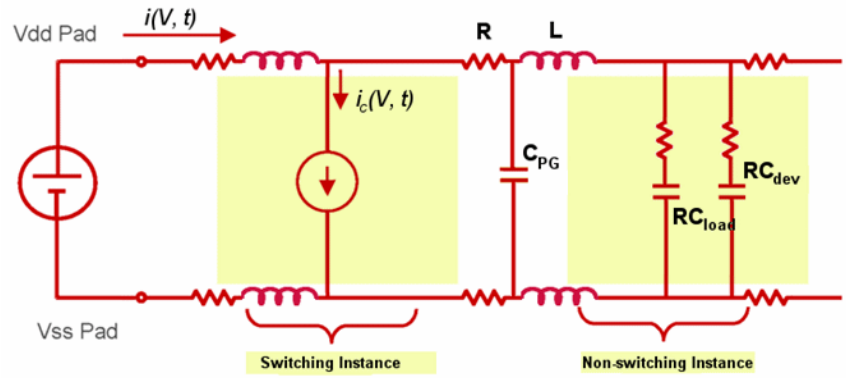

Figure 2.15.: Dynamic voltage drop analysis modelling as time-domain profile [6]

In the complete model, the internal and external voltage sources, the PCB, Package, layout extraction, the technology data, and the flows are represented by the transistors. The active devices are the drains for all currents.

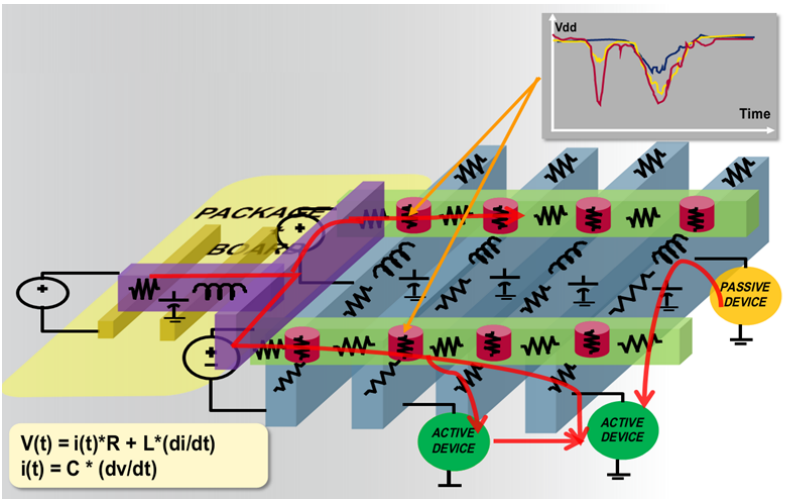

Figure 2.16.: Totem methodology for dynamic voltage drop analysis [6]

A simple calculation can be performed by equations 2.3 and 2.4.

CHAPTER 3

Modelling and Simulation

3.1 Indroduction

The generation of a power-ground noise model of a analog, mixed-signal block is split into two paths: the electric path and the physical path, which are shown in figure 3.1 [6]

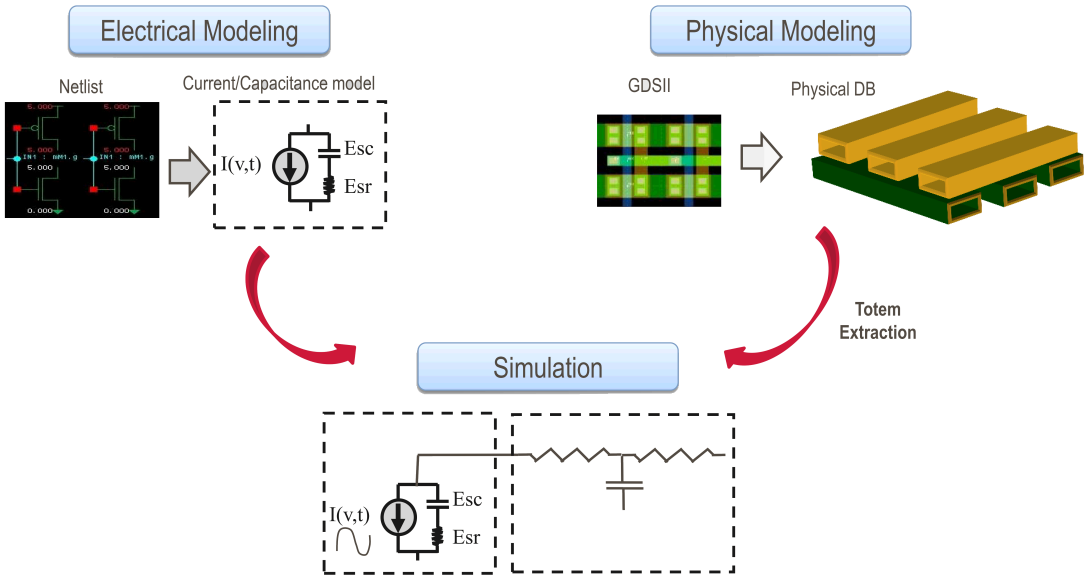

Figure 3.1.: Custom Circuit Modeling in Totem [6]

3.2 Electrical path modelling

The figure 3.2 shows the electrical path flow with all the required input data for the dynamic analysis.

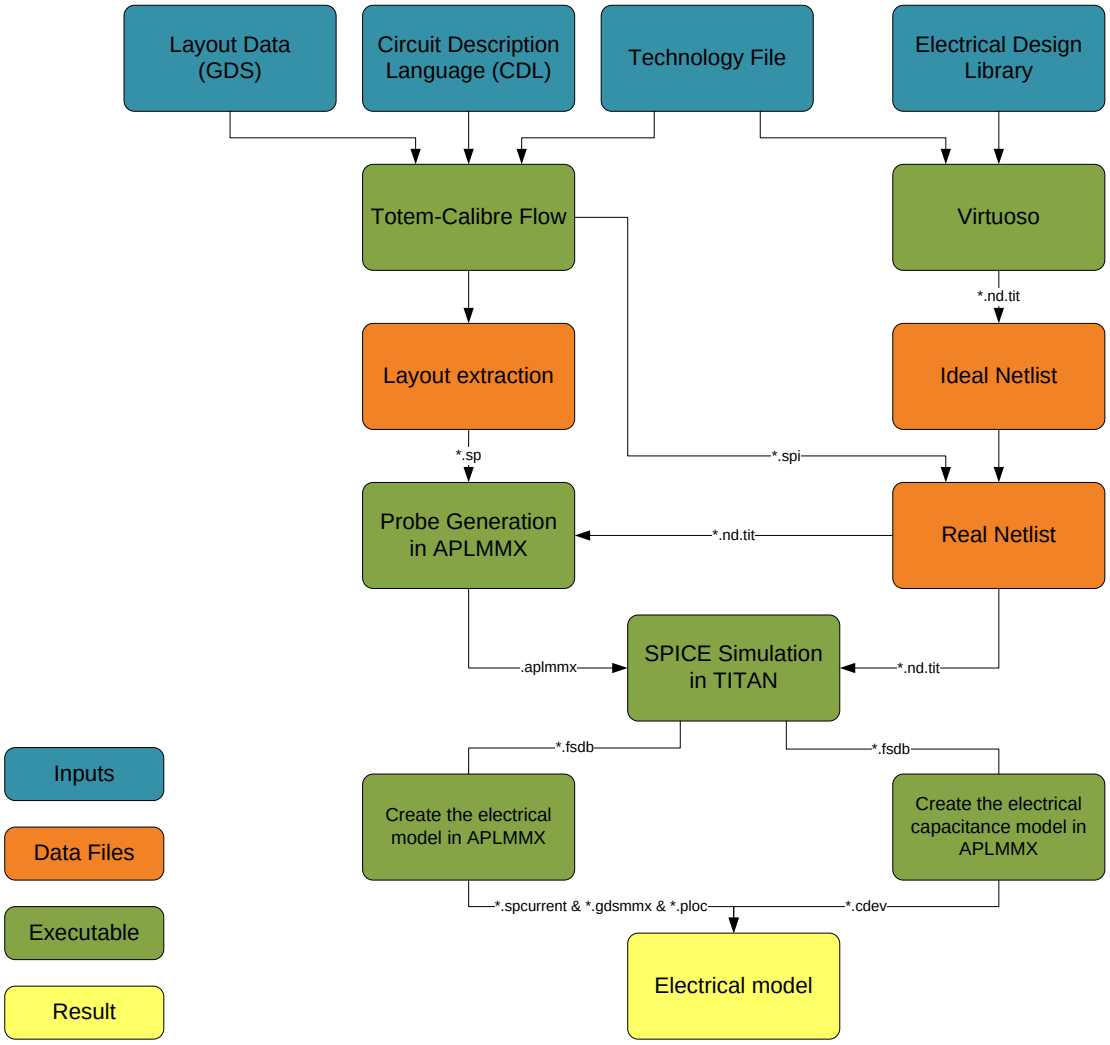

Figure 3.2.: Electrical Modelling Flow

3.2.1 Block diagram of the Phase Locked Loop (PLL)

The PLL exists of four blocks: the digital PLL core, the analog test Multiplexer (MUX), the Digitally Controlled Ring Oscillator (DCRO), the Phase Quantizer (PQ), the Delta Sigma Modulator (DSM), and the internal voltage regulator (IVR).

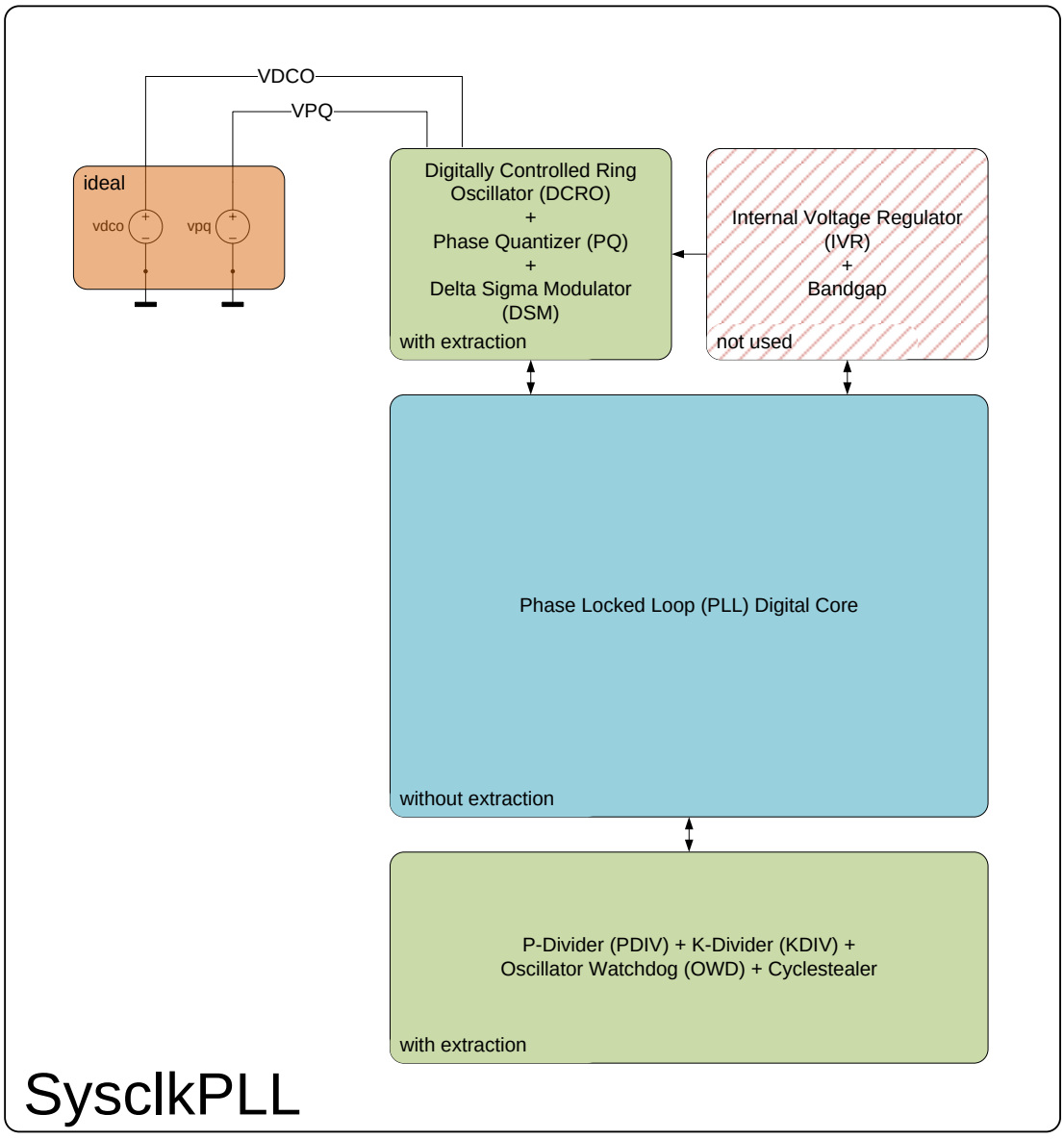

Figure 3.3.: Block diagram of the SysclkPLL

Phase Locked Loop (PLL) Digital Core

For the digital PLL core, the extracted spice netlist is not used, due to the huge amount of transistors in this block which would enormously increase the simulation time needed.

PDIV, KDIV, OWD and Cyclestealer

The blocks PDIV, KDIV, OWD and Cyclestealer are modelled with the extracted netlist.

Digitally Controlled Ring Oscillator (DCRO), Phase Quantizer (PQ) and Delta Sigma Modulator (DSM)

This block is the most important of all, and is modelled with the extracted netlist.
The VCO integrated in the DCRO generates the highest interferences.

Internal voltage regulator (IVRint) for the PLL core

For better power supply rejection, the analog parts of the PLL core (Digitally Controlled Oscillator (DCO) and PQ) are supplied by an IVRint which is internally subdivided into to independent blocks for DCRO, PQ and DSM. The IVRint is supplied by the internal voltage supply of $1.8\,V$ and provides a precision voltage supply of $1.3\,V$. The IVRint can be set in power down mode. When releasing the power down mode, the IVRint takes maximum $50\,\mu s$ unitl IVRint reached its final voltage level. For this reason, the block IVRint is used. Instead of the IVRint, ideal voltage sources are used.

3.2.2 Netlist Generation with VIRTUOSO and Totem-Calibre Flow

The ideal netlist and the extraction netlist are created using the tools Virtuoso and Totem-Calibre Flow.

3.2.3 Probe Generation in APLMMX

This step generates the necessary inputs for the Totem flow, which involves identification of the transistors that are connected to the power and ground network, and the creation of a set of probes for these transistors, as shown in figure 3.2.

3.2.4 SPICE Simulation in Titan

TITAN is a general purpose network analysis program for nonlinear electrical circuits and is similar to SPICE.

The work flow of modelling and simulation for a PLL in TITAN is:

1. Normal run -> Pnom, VDD $= 1.3\,V$, T $= 27\,C$, XTAL $= 20\,MHz$
2. Run with extraction and identifying which extraction is necessary -> real netlist
3. Run with real netlist and iProbes (*.aplmmx)

3.2.5 Electrical Model in APLMMX

The electrical model is created using the APLMMX tool of Totem. Thereby, the generated simulation outputs from Titan are converted for the device currents. The outputs of the APLMMX are the current file (<cell>.spcurrent), the transistor model mapping file (<cell>.gdsmmx), and the capacitance model (<cell>.cdev).

3.3 Physical path modelling

The figure 3.4 shows the physical path flow with all the required input data for the dynamic analysis.

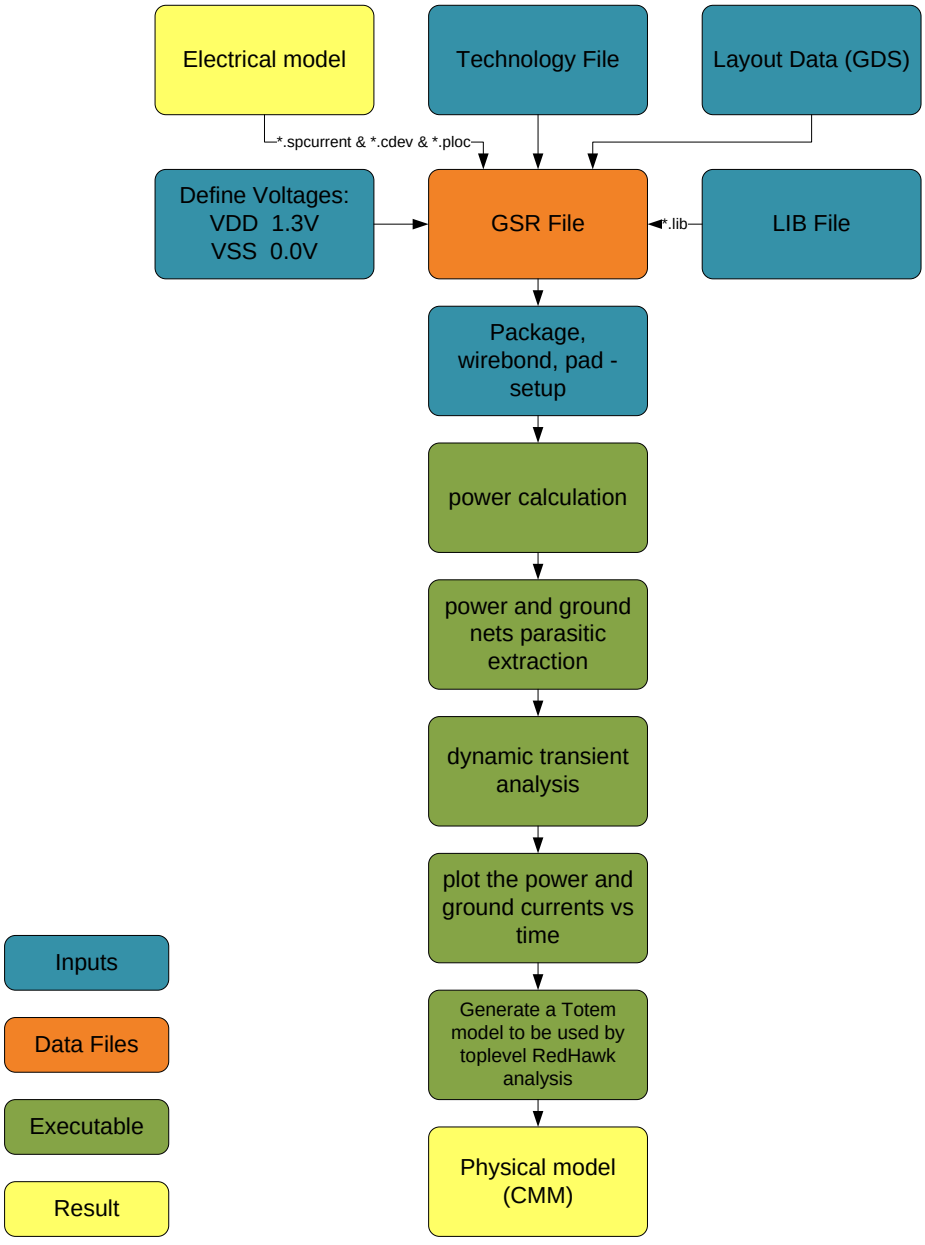

Figure 3.4.: Physical Modelling Flow

3.3.1 Setting Up and Running Totem Dynamic Analysis

The GSR File for Totem dynamic voltage drop analysis requires the following inputs.

- Electrical model with the APL Files (*.spcurrent, *.cdev and *.ploc)
- The technology file provides technology information about the process and specifies parameters for each metal layer and type of via. A separate technology file is needed for each IC process.
- Layout Data in GDSII format is coming from the layout extraction.
- Define Voltages for VSS nets and VDD nets.
- LIB File is required to specify one custom lib file to be used in the design.
- Simulation parameters: Frequency, DYNAMIC_SIMULATION_TIME and DYNAMIC_TIME_

3.3.2 Pad, Wirebond and Package Parameters

High quality models of off-chip RLC circuit elements such as the package and PCB are required in order to achieve an accurate simulation of circuit power.

The following resistance values are adopted so that a visible change can be seen.

```
setup package -power -r 5
setup package -ground -r 5
setup wirebond -power -r 100
setup wirebond -ground -r 100
setup pad -power -r 0
setup pad -ground -r 0
```

where
-power -ground : selects which P/G net to define
-r <R_Ohms> : specifies equivalent resistance value in Ohms
-c <C_pF> : specifies equivalent capacitance value in picoFarads
-l <L_pH> : specifies equivalent inductance value in picoHenrys

3.3.3 Power calculation

The power is calculated using the *perform pwrcalc* command.
Some of the information that can be checked in the power summary report is:

- Does the total power consumption make sense?
- Are clock network and the clock power values reasonable?
- Is the power reported by clock frequency as be expected?

3.3.4 Power and grounds nets parasitic extraction

After the power calculation, the network extraction is performed using *perform extraction -power -ground -l -c* commands. The perform extraction command builds connectivity and performs extraction for the selected elements of the selected power/ground nets.

3.3.5 Dynamic transient analysis

When all standard design steps are completed, the following dynamic analysis commands re used to perform vectorless analysis:

perform analysis -vectorless

3.3.6 Plot and generate a Totem model

Perform *plot current* command to make sure that appropriate current is assigned.
The *export model -mmx -dir <name> command* Totem Model (CMM) is generated for RedHawk.

3.3.7 TCL Command File for Dynamic Analysis

A sample TCL command file for DVD analysis is shown following:

```
##### import global system requirements and set up the tool
setup design dynamic.gsr

##### pad, wirebond and package parameters
setup package -power -r 5
setup package -ground -r 5
setup wirebond -power -r 100
setup wirebond -ground -r 100
setup pad -power -r 0
setup pad -ground -r 0

##### power calculation
perform pwrcalc

##### power and ground nets parasitic extraction
perform extraction -power -ground

##### dynamic transient analysis
perform analysis -vectorless

##### plot the power and ground currents vs time
plot current -pad -o <file-name>

##### save the database (reopen with  import db)
export db SYSCLKPLL_1_40_2_200MHz_dynamic.db

# Generate a Totem model to be used by toplevel RedHawk analysis
export model -mmx -dir cmm_1_40_2_200MHz_20_periods
```

3.4 Simulation results

3.4.1 Indroduction

The transient simulation results were created and saved with the *plot current -pad -o <filename>* command. This noise signal has an offset and is limited in time. By subtracting the DC value, a typical noise signal is generated.
With a Fast Fourier Transformation (FFT) , a time signal is transformed to a spectrum in frequency domain are described in Appendix A.1.

3.4.2 Ground noise currents of the PLL with VCO = 400 MHz in time-domain

The time-limited current flow in the CMM on the ground path (Voltage Source Source Analog (VSSA)) is shown in figure 3.5. By finite simulation of $1\,\mu s$, only frequencies above $2\,MHz$ are considered according to Shannon [15]. The simulation contains all extractions and all current probes from the PLL on the ground supply VSSA.

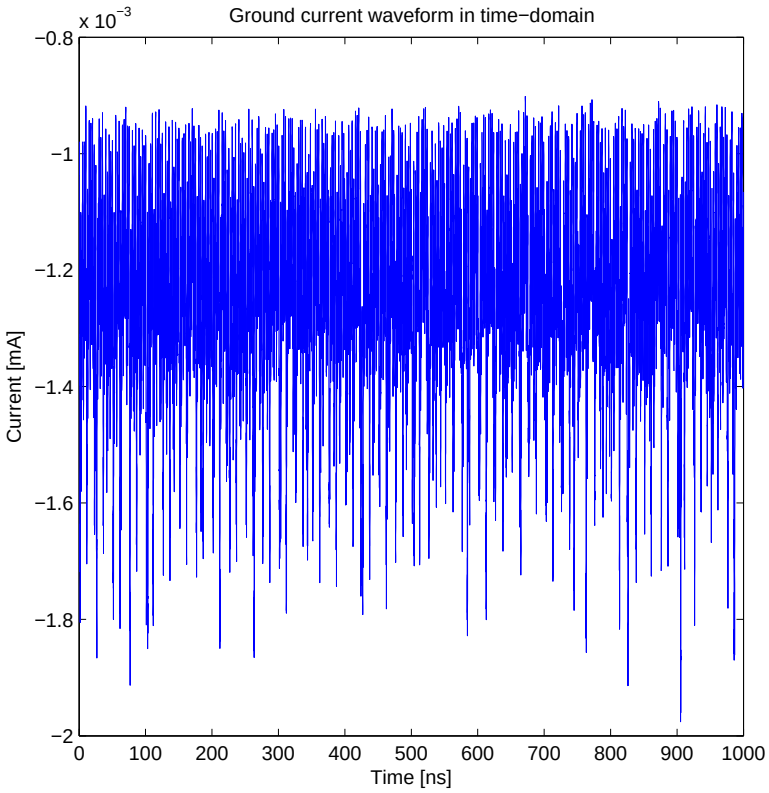

Figure 3.5.: Ground current waveform of the PLL on the Pin VSSA in time-domain

3.4.3 Ground noise currents of the PLL with VCO = 400 MHz in frequency domain

In the figure 3.6, the harmonic frequencies from $400\,MHz$ to $2.4\,GHz$ are illustrated as a PSD.
The peak values with and without FM are compared in the table 3.2.

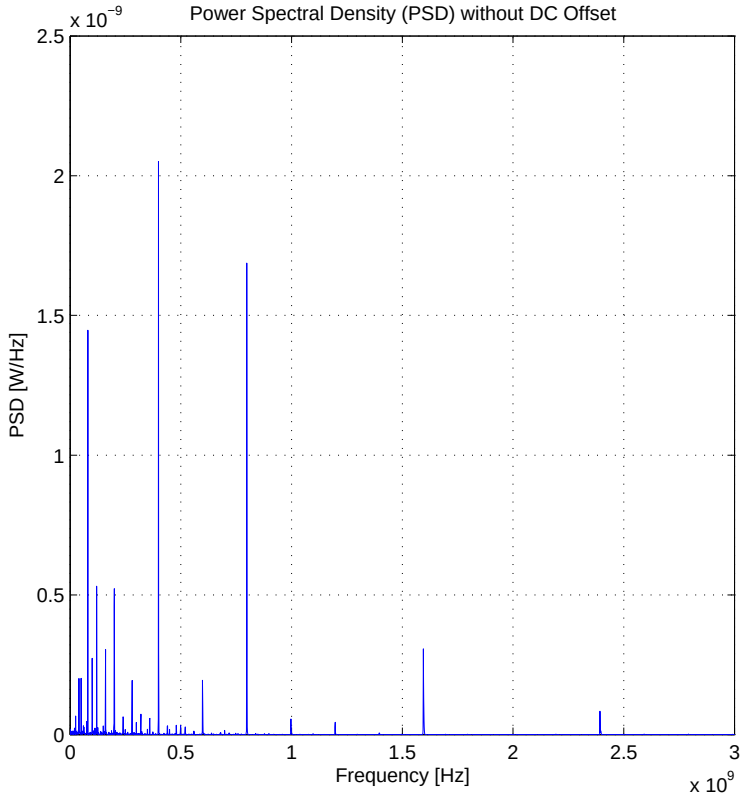

Figure 3.6.: PSD without DC Offset of a PLL Ground (VCO = 400 MHz)

In order to reduce the harmonic level, the SSCG was used as can be clearly seen in the figure 3.7 recognizable.

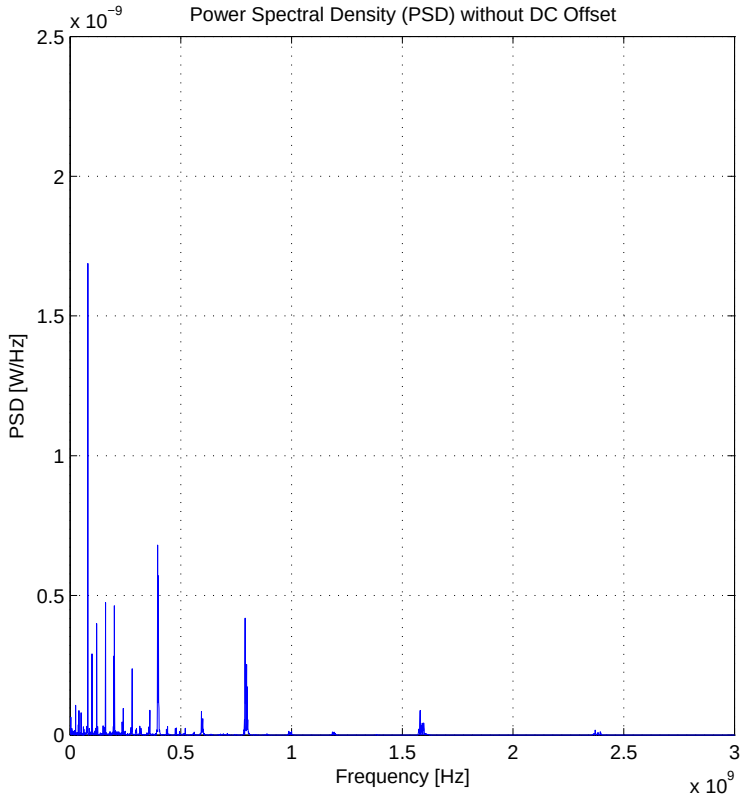

Figure 3.7.: PSD without DC Offset of a PLL Ground with FM (VCO = 400 MHz)

Table 3.1.: Comparison of the PSD peak values from figures 3.6 and 3.7

PSD of a PLL		**PSD of a PLL with FM**	
Frequency [MHz]	**PSD [nW/Hz]**	**Frequency [MHz]**	**PSD [nW/Hz]**
81	1.447	81	1.688
201	0.522	201	0.463
400	2.051	396	0.680
799	1.687	791	0.419
1596	0.307	1582	0.088

3.4.4 Ground noise currents of the PLL with VCO = 400 MHz in frequency domain in dBμV

The next two figures 3.8 and 3.9 show the ground noise spectrum with the decibel (dB) on the reference level of $1\,\mu V$ on the ordinate. Comparing the results (Table 3.2) without FM (Fig. 3.8) and with FM (Fig. 3.9) at the 1st harmonic ($400\,MHz$) shows an improvment of approximately $4\,dB$ when considering FM.

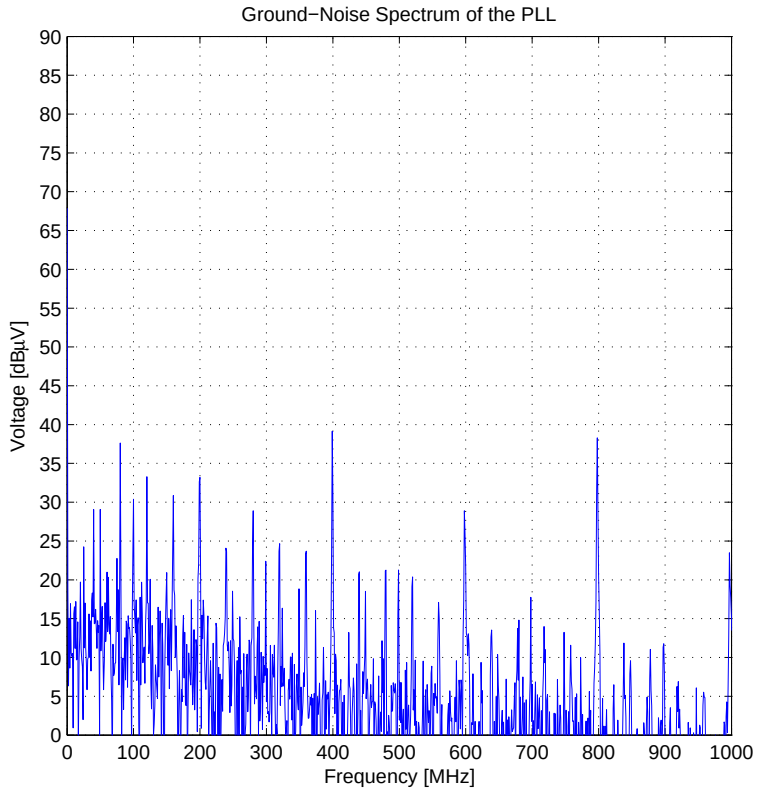

Figure 3.8.: Ground-Noise Spectrum of a PLL Ground (VCO = 400MHz)

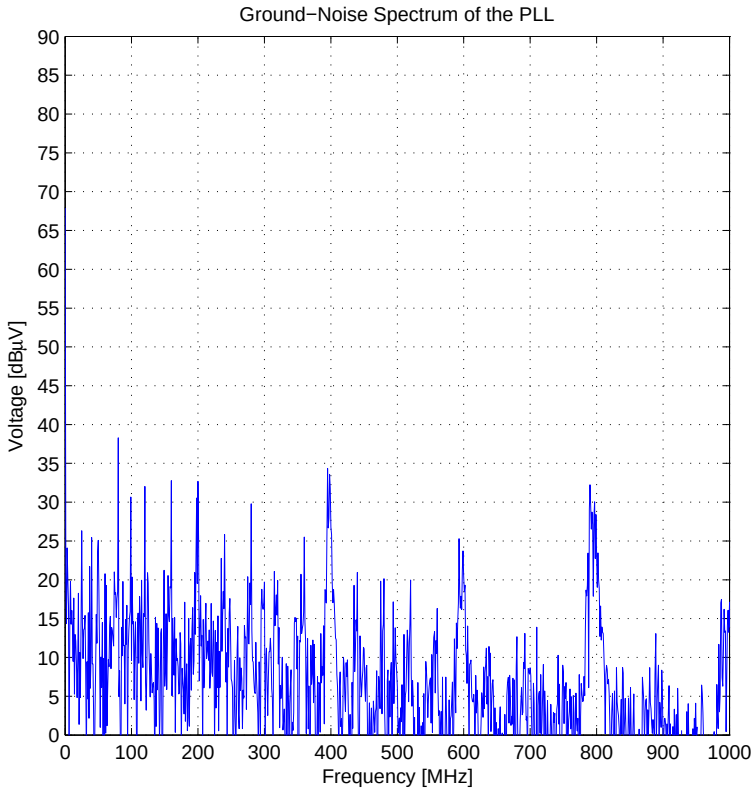

Figure 3.9.: Ground-Noise Spectrum of a PLL Ground with FM (VCO = 400MHz)

Table 3.2.: Compare the highest voltage peaks in the figures 3.8 and 3.9

Ground-Noise Spectrum of the PLL		**Ground-Noise Spectrum of the PLL with FM**	
Frequency [MHz]	**Voltage [dBµV]**	**Frequency [MHz]**	**Voltage [dBµV]**
81	38	81	38
201	33	201	33
400	39	399	34
799	38	791	32
1596	31	1582	25

3.4.5 Measurement results

The measurement is an emission peak investigation of oscillator, SysPLL, ErayPLL. The device TC277C-PD with a ball grid array (BGA) package was used.

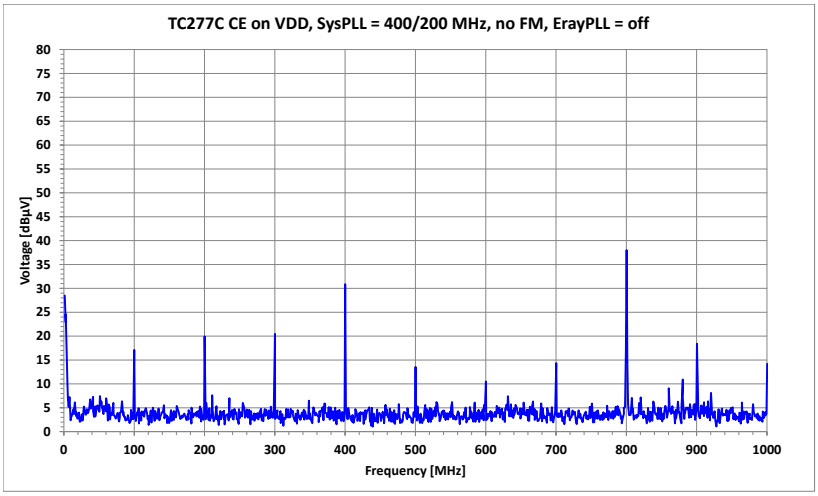

Figure 3.10.: Measurement TC277C CE on VDD, SysPLL = 400/200 MHz, no FM, ErayPLL = off [8]

3.4.6 Correlation of simulation and measurement

A correlation of the simulation results with the measurement results can only be carried out quantitatively. This means that only the frequency position of the interference signal can be evaluated. Since the models of the SoC, package (bonding and leadframe), PCB and the EMI receivers are not yet available, a qualitative evaluation can not be provided. However, the highest frequencies of 400 MHz and 800 MHz can be detected. With a design optimization lowering the level, an improvement at the system level can be achieved.

CHAPTER 4

Summary and future work

4.1 Summary and conclusion

In this thesis, a dynamic voltage drop power-ground noise model on IC -level was created of a PLL.
The creation of the chip macro model (CMM) was generated by an electrical flow and a physical flow. By means of the electrical flow, the current file (<cell>.spcurrent), the transistor model mapping file (<cell>.gdsmmx), and the capacitance models (<cell>.cdev) were produced.
The output from the physical flow was the generated model which will be used RedHawk. In addition, a plot of ground current waveform in time-domain from the PLL is shown in figure 3.4.2.
This model includes all the extractions of PDN and for all the current probes of the transistors.
A plot (see 3.8) from the ground currents signal versus time-domain is transformed with a matlab code A.1 to the frequency domain (spectrum). Comparing the results (Table 3.2) without FM (Fig. 3.8) and with FM (Fig. 3.9) at the 1st harmonic ($400\,MHz$) shows an improvment of approximately $4\,dB$ when considering FM.
The correlation between the spectrum (see 3.8) and the measurement results (see 3.10) shows clearly the harmonic frequencies $400\,MHz$, $800\,MHz$, $1200\,MHz$ and $1600\,MHz$.

4.2 Future work

4.2.1 Long time Simulation with FM

In order to obtain a very good correlation between simulation and measurement results, the simulation time for the SSCG must be significantly increased.
With a simulation time of $25\,\mu s$, the frequencies $80\,kHz$ to $2\,MHz$ would be recorded.

4.2.2 Chip power model (CPM), Package and printed circuit board (PCB)

The next task is the generation of the chip power model (CPM) with the RedHawk tool. A CPM is a compact and accurate SPICE model of the full-chip PDN. To complete the CPM further blocks for clock generation need to be modelled:

- pierce oscillator
- PLLs
- fast switching I/O pads driving high loads

After warts, the package, PCB, and the EMI receiver can be added to the model. The modelling package and PCB are created using the tools Speed2000 and Power-SI [16].

4.2.3 EMI receiver model

The model of the EMI receiver is a major part of the system simulation.
In Figure 4.1 the principle of the EMI receiver is shown. The implementation of this EMI receiver model is composed of two parts: the transient simulation model and the digital post processing part. [9]

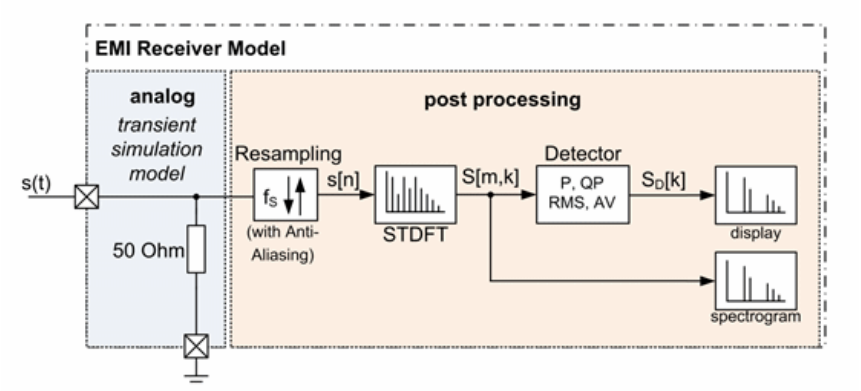

Figure 4.1.: Principle of an emission simulation with an analogue circuit simulated in Spice and a post processing with the EMI receiver [9]

4.2.4 System simulations

The complete model with CMM, CPM, package/bonding model, PCB model, 150 Ω/1 Ω network model and EMI receiver model is shown in figure 4.2.

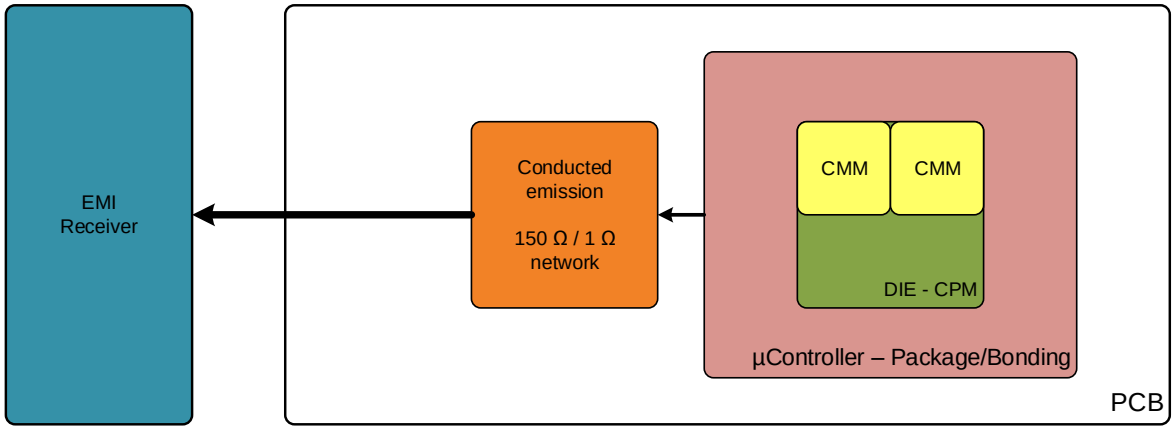

Figure 4.2.: System Simulation Overview

Finally, the system simulation is performed using the complete model, and the compliance to the measurement results can be analysed.

Bibliography

[1] Clayton R. Paul. Practical papers, articles and application notes bandwidth of digital waveforms. IEEE-EMCS Newsletter, pages 58–65, 2009. 223.

[2] Joester Michael, Dr. Frank Klotz, Dr. Wolfgang Pfaff, and Thomas Steinecke. Generic ic emc test specification. ZVEI, 2010.

[3] A.S. de Beer. Structure for the introduction of emc design. IEEE, pages 1–5, 2008. ISBN: 978-1-4244-1699-8.

[4] Hardin K.B., Fessler J.T., and Bush D.R. Spread spectrum clock generation for the reduction of radiated emissions. IEEE, pages 227–231, 1994. ISBN: 0-7803-1398-4.

[5] Ernst Habiger. Elektromagnetische Verträglichkeit, volume 2. VEB Verlag Technik Berlin, 1988. ISBN 3-341-00620-6. Störbeeinflussungen in Automatisierungsgeräten und -anlagen.

[6] ANSYS. Products. Website, 2015. https://www.apache-da.com/products".

[7] Shen Lin, Makoto Nagata, Kenji Shimazaki, Kazuhiro Satoh, Masaya Sumita, Hiroyuki Tsujikawa, and Andrew T. Yang. Full-chip vectorless dynamic power integrity analysis and verification against 100uv/100ps-resolution measurement. IEEE, pages 509–512, 2004. ISBN: 0-7803-8495-4.

[8] T. Steinecke, G. Fries, and C. Colditz. Aurix microcontrollers: Emission contribution of oscillator and system & eray plls. Emission peak investigation of oscillator, SysPLL, ErayPLL.

[9] Klaus Hörmaier. Excessive electromagnetic interferences as fault - methodology for automotive electromagnetic compatibility with respect to functional safety. Document submitted at TU Graz 2015.

[10] Shen Lin and Chang N. Challenges in power-ground integrity. IEEE, pages 651–654, 2001. ISBN: 0-7803-7247-6.

[11] Roland Best. Theorie und Anwendungen des Phase-locked Loops, volume 4. AT Verlag Aarau, 1987.

[12] Ulrich Tietze, Christoph Schenk, and Eberhard Gamm. Halbleiter-Schaltungstechnik. Springer Verlag, 2002.

[13] Karl Küpfmüller, Wolfgang Mathis, and Albrecht Reibiger. Theoretische Elektrotechnik Eine Einführung, volume 19. Springer Vieweg, 2013.

[14] FUITSU. Spread spectrum clock generator (sscg) user guide. Website, 20009. http://www.edn.com/Pdf/ViewPdf?contentItemId=4137607".

[15] C.E. Shannon. Communication in the presence of noise. Proceedings of the IRE, pages 10–21, 1949. ISBN: 978-1-4244-1699-8.

[16] Vanthana Dhanaraj. Construction of a full-blown 32-bit microcontroller soc conducted electromagnetic emission model and correlation of simulation and measurement results. in progress.

APPENDIX A

Time-domain to frequency-domain

A.1 FFT conversion with MATLAB

```
clear
cla                    % Clear current axes
close all

%%% Import data files:

file_name = ['current_pad_400_20ps_1000ns_vssa_extra0'];
%file_name = ['current_pad_400_20ps_1000ns_FM_vssa_extra0'];

file_name_xls = strcat(file_name,'.xls')

y = xlsread(file_name_xls);
%A4 = xlsread('current_pad_600_20ps_1000ns_FM_vssa_extra0.xls');

L=length(y)
x = 1:1:length(y);

figure % opens new figure window for time-domain

plot(x/50,y);
title('Ground current waveform in time-domain');
xlim([0. 1000]);
%ylim([0. 2.5e-9]);
xlabel('Time [ns]');
ylabel('Current [mA]');
```

```
%%% Save plot in PDF-format
set(gcf, 'PaperPosition', [0 0 6 6]); % Position the plot further to
    the left and down. Extend the plot to fill entire paper.
set(gcf, 'PaperSize', [6 6]); % Keep the same paper size
saveas(gcf,strcat(file_name,'_time_domain') , 'pdf')

figure % opens new figure window for PSD

% analysis resolution from totem tool
DYNAMIC_TIME_STEP = 20e-12;  % Definition in the Totem tool

fs = 1/DYNAMIC_TIME_STEP;  % Sample frequency
NFFT=L;
y_wo_mean = detrend(y,'constant'); % Signal without DC offset

X=fft(y_wo_mean,NFFT); % FFT transformation
Px=X.*conj(X)/(NFFT*L); % Power of each frequency components
fVals=fs*(0:NFFT/2-1)/NFFT;  % x-axis in Hz and one side spectrum

% Find the maximum paeks in the plot
[pks_1,locs_1] = findpeaks(Px(1:NFFT/2),'MinPeakHeight',5e-11);
%plot(fVals,Px(1:NFFT/2),fVals(locs_1),pks_1,'or');
plot(fVals,Px(1:NFFT/2));
grid on
title('Power Spectral Density (PSD) without DC Offset');
xlim([0. 3.0e9]);
ylim([0. 2.5e-9]);
xlabel('Frequency [Hz]');
ylabel('PSD [W/Hz]');

%%% Save the PSD plot in a PDF-format
set(gcf, 'PaperPosition', [0 0 6 6]); % Position the plot further to
    the left and down. Extend the plot to fill entire paper.
set(gcf, 'PaperSize', [6 6]); % Keep the same paper size
saveas(gcf,strcat(file_name,'_fft') , 'pdf')

%%% Save the maximum PSD peaks in a excel file
C1 = num2cell([locs_1,round(pks_1/(1e-12))]);
T1 = cell2table(C1,'VariableNames',{'Frequency_in_MHz' '
    PSD_in_pW_pro_Hz'});
delete(strcat(file_name,'_fft.csv'));
```

```
writetable(T1,strcat(file_name,'_fft.csv'),'Delimiter',';')


Y = fft(y,NFFT)/length(y);
f = fs/2*linspace(0,1,NFFT/2+1)/1e6;

figure % opens new figure window for FFT

% Find the maximum peaks in the plot
[pks_2,locs_2] = findpeaks(20*log10((2*abs(Y(1:NFFT/2+1)))/(1e-6)),'
    MinPeakHeight',20);
%semilogx(f,20*log10((2*abs(Y(1:NFFT/2+1)))/(1e-6)));  % log plot of
    the x-axis
plot(f,20*log10((2*abs(Y(1:NFFT/2+1)))/(1e-6))); % linear plot of the
     x-axis
grid on
xlim([0. 1000]);
ylim([0. 90]);
title('Ground-Noise Spectrum of the PLL');
xlabel('Frequency [MHz]');
ylabel('Voltage [dB\muV]');
set(gca,'YTick',[0:5:90])

%%% Save the ground-noise spectrum plot in a PDF-format
set(gcf, 'PaperPosition', [0 0 6 6]); % Position the plot further to
    the left and down. Extend the plot to fill entire paper.
set(gcf, 'PaperSize', [6 6]); % Keep the same paper size
saveas(gcf,strcat(file_name,'_fft_dB'), 'pdf')

%%% Save the maximum ground-noise spectrum peaks in a excel file
C2 = num2cell([locs_2,round(pks_2)]);
T2 = cell2table(C2,'VariableNames',{'Frequency_in_MHz' '
    Voltage_in_dBuV'});
delete(strcat(file_name,'_fft_dB.csv'));
writetable(T2,strcat(file_name,'_fft_dB.csv'),'Delimiter',';')
```