Miniaturized RFID Tags Exploring Passive Boosting Technologies

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Abstract

The geometrical dimensions of high frequency (HF) radio frequency identification (RFID) transponders are in the centimeter range. For example, the size of an RFID credit card is defined in the ISO/IEC 7810 [52]. Beside standard ID1 dimensions, ID/2 and further smaller geometries are defined and will be defined in future. This is also true for ultra-high frequency (UHF) frequency band RFID tags. Which of these antenna dimensions or frequency bands is finally chosen depends on the application.

This thesis deals with the smallest possible RFID tag dimensions – for instance, the chip-scaled RFID tag. The main aim of the first part of this work was to examine the feasibility of such tag types. Therefore, the focus was to develop overall miniaturized RFID systems in the HF as well as UHF frequency band. Moreover, combined solutions, so-called comprehensive tags, were investigated. Not only inductive coupled systems but also capacitive coupled tags were investigated. As a result, more than one hundred different tags were developed and manufactured with a wide spectrum of packaging and complementary metal-oxide-semiconductor (CMOS) technologies. Out of this bundle, this document presents four novel highly miniaturized RFID systems in detail:

- A small, HF based, embedded ball grid array (eWLB) system in package (SiP) that can be used as a miniaturized biomedical diagnostic device.
- The world's smallest wafer level packaging (WLP) based HF security micro-controller
- A monolithic, silicon based dual band (HF and UHF) RFID tag with a on chip antenna
- A novel one square millimeter capacitive coupled RFID tag

Due to the high degree of miniaturization, these RFID systems are limited in terms of performance and reading distance. To overcome these limitations, the second part of this thesis deals with passive boosting technology. The aim was to analyze and to develop booster antenna structures that improve the RFID tag performance. Again, inductive coupled booster antennas as well as capacitive coupled systems were investigated. Furthermore, near- and far-field booster antennas were developed. For the very first time, the booster antenna technology was discussed in detail and categorized into four classes. In addition, passive boosting material was researched. In particular, it was shown that antennas printed onto ferrite as substrate can be used to improve the performance of HF tags in a metallic environment.

Beside the research of this novel and unprecedented work, novel applications and new possibilities were highlighted.

Acknowledgments

This work has been carried out at the Institute of Microwave and Photonic Engineering at the Graz University of Technology in cooperation with the Contactless and RF-Exploration (CRE) Department at Infineon Technologies Austria AG.

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Chapter 1

Introduction

We live in the age of technology and information. Nowadays everybody is able to communicate with each other all over the world. The Internet provides unlimited information and provides us with gateways to an endless virtual environment. More and more electronic devices are equipped with computers to access to this world. In order to fuse the world to a whole, Kevin Ashton proposed a new term [48] 1999 that should announce a new age in information technology - The Internet of Things (IoT). This concept describes an overall interconnection of literally everything. By ”tagging” things, equipping objects with identifiers, everything could be registered and managed in the virtual world of the Internet. This could be realized with barcodes or Quick Response (QR) codes for example. Due to additional functionalities, radio-frequency identification (RFID) technology seems to be the perfect interface to accomplish the concept of the IoT.

Besides tagging objects, steady, on-going development in the field of RFID technology is creating more and more capabilities and varieties of new applications. One of the main goals in developing RFID improvements is to reduce the size of the overall RFID system. The RFID transponder geometry in particular is becoming more and more miniaturized. Such millimeter sized, fully integrated, monolithic RFID transponders can be used to tag even the smallest objects, such as jewelry, medical pills or even insects for example. But there are far more opportunities than just tagging items! Equipped with secure elements, miniaturized RFID transponders could be used for branding objects. Then - embedded into paper for example - valuable documents or money would be unforgeable. Recently, more and more RFID tags provided with sensors have been presented. Temperature-, impedance- or any other physical parameter can be measured by RFID sensor nodes [55] [97]. Medical usage, such as implanted diagnostic devices [82], is just one more example of further future RFID applications. Doubtless the potential of miniaturized RFID sensor-nodes connected to the Internet is unimaginable high.

However, small RFID systems lead to a number of limitations in energy transfer and communication distance. To overcome these problems research has to be done in the field of miniaturized antennas, front-end designs, packaging concepts and boosting technologies. This work focuses on these topics and constitutes a basis for further miniaturization.

1.1 Scope of Work

This thesis examines small form factor RFID systems, i.e., reduced size RFID systems with in particular minaturized RFID tags. Therefore, this thesis pushes the high frequency (HF) as well as ultra high frequency (UHF) RFID technology to its geometric limits. Particular attention is paid to small antenna design and different coupling mechanism. Thus not just the tags it self is investigated. Capacitive as well as inductive coupling behavior of the overall RFID systems are analyzed. To provide a wide spectrum of RFID tag miniaturization, several technologies are used and investigated.

Furthermore this work examines the use of passive booster technology, that improves the communication performance of small RFID devices. For the very first time different types of booster antennas are developed and categorized into antenna classes. Again, a vary of technologies are applied to develop and to produce the particular booster structure.

In addition this thesis examines materials that improve the overall RFID communication performance.

At each point, novel wireless applications are identified and illustrated.

1.2 Outline and Related Work

The main contributions of this thesis contained in Chapter 2, Chapter 3 and Chapter 4 are briefly summarized in this section.

1.2.1 Small Form Factor RFID Systems

Chapter 2 deals with the basic theory of miniaturized RFID tag antennas at 13.56 MHz and 868 MHz. It is shown that small radiating elements with decreasing antenna volume become more and more inefficient. Doubtless the highest possible level of miniaturization is to produce a monolithic RFID chip with an on-chip antenna. Therefore, this section provides detailed research on the literature about state of the art silicon based chip antennas. It is shown that silicon is not well suited as antenna substrate. Thus small radiating elements, based on silicon, become inefficient and inapplicable. However, this does not apply to near-field antennas that are used in proximity coupled RFID systems. Coils and loop antennas which are inductively coupled via the magnetic field are able to establish an RFID communication. Therefore, small coupled coils are discussed. Furthermore a brief overview of important near-field parameters is given.

1.2.2 Small RFID Tags

Chapter 3 shows millimeter scaled RFID transponder developments. It comprises four, fully operational RFID tag types which are produced in different packaging technologies. Each tag is designed to operate in designated application scenarios. Thus, each tag has its advantages and drawbacks. The development portfolio of this chapter comprises:

- A three-dimensional (3D) packaging concept that combines the RFID technology with a novel medical bio-chip. This multi-chip RFID tag development allows complex blood diagnosis, such as diagnosing sepsis. Due to the novel embedded wafer-level ball grid array (eWLB) technology used, the presented RFID system in package (SIP) can be produced very small (5.6 mm x 3.6 mm) and efficient. This development enables new capabilities and will lead to affordable diagnostic systems in the field of complex medical applications.
- A secure element transponder that is equipped with an RFID antenna directly on the top of the chip. This $20 - 30\,\mu$m thick copper antenna is fabricated with two stacked redistribution layers. Therefore a wafer-level packaging (WLP) technology is used. The presented 2.2 mm x 2.2 mm small RFID secure element transponder makes it possible to brand small valuable items, such as jewelery.
- A silicon based dual band RFID transponder (tag) that is suited with an on-chip antenna. As the name - dual band - suggests, the presented transponder is able to operate at 13.56 MHz and 868 MHz. This type of RFID tag represents a monolithic device that comprises the tag as well as the tag-antenna within a standard complementary metal-oxide-semiconductor CMOS technology. Doubtless this represents the highest possible level of RFID tag miniaturization.
- A novel capacitively coupled RFID tag that is produced in a low cost 130 nm CMOS process. In contrast to the already described tag types this transponder uses the electric field as a communication channel. Similar to the dual band RFID tag, this transponder is able to operate at 13.56 MHz and 868 MHz. Due to the non-resonant capacitive coupling mechanism, the tag can be applied in novel applications. For example, it can be used to tag small metal objects.

Note that each RFID tag type development is novel. Chapter 3 highlights the benefits of these highly miniaturized RFID tags. Furthermore, system parameters such as the reading distance are investigated. In addition, several application scenarios are introduced. The author hopes the presented work will lead to even more novel applications and enable new capabilities.

Related Work

The first part, 3.1 of the presented work in Chapter 3 was developed within the European EU FP7 project "Best-reliable ambient intelligent nano sensor systems" (e-Brains)(Project-no FP7-ICT-257488) [104]. The main aim of the project was to create a new generation of sensors which are realized with the help of heterogeneous technologies. These technologies

should increase the feasibility of high-performance sensor devices equipped with smart wireless communication and optimized in terms of size. As shown in Section 3.1, the development of a smart bio-sensor grain was successful. Furthermore, it should be mentioned that the development of the used eWLB technology was also financially supported by the ENIAC Joint Undertaking and the "Bundesministerium für Bildung und Forschung (BMBF)" in the project Efficient Silicon Multi-Chip System-in-Package Integration (ESiP).

The monolithic silicon-based RFID chips (3.2, 3.3 and 3.4) that are presented in Chapter 3 are based on work which was done in the area of the so-called Comprehensive Transponder System (CTS) project that was funded by the Austrian research funding agency FFG with the program FIT-IT [27] and Infineon Technologies Austria AG in 2006. The goal of the CTS project was to combine several Industrial, Scientific and Medical (ISM) frequency bands (LF,HF and UHF) that are defined for RFID applications into one single RFID chip. Note that this work relates to many different publications, e.g. [22–24, 35–40, 56, 70, 95]. The first prototype of the chip was already presented by [71] in 2008. In 2011, the first fully operating and improved comprehensive chip was published by [94]. The chip was able to operate with standard RFID antennas at the particular frequency band. To present the dual band capability of the chip and its outstanding performance, [67] developed a novel dual band tag antenna. Since then, many improvements have been and continue to be made by the Contactless and Radio Frequency Exploration (CRE) Department of Infineon Technologies Austria AG. In this thesis the latest version of the digital core and modified analog front ends of this outstanding work and project are reused.

1.2.3 Passive Boosting Technologies

Chapter 4 deals with the possibility to boost the performance of highly miniaturized RFID transponders with passive boosting structures. Therefore, this chapter is closely related to the results of Chapter 3. The performance and reading distance of highly miniaturized RFID transponder are limited. Moreover, a small RFID tag is forced to operate with the appropriate reader and its small coupling antenna. To overcome this limitations in some application scenarios, different materials, such as ferrite, can be applied. As it is shown in Chapter 4, the communication channel benefits from the presented boosting material.

The main focus of Chapter 4 lies in the passive booster antenna technology. This technology allows a parameter transformation of small antennas to larger areas. In other words, small transponders are coupled (non-galvanic) to larger antennas. Note, that no active or amplifying components are used. It is shown, that in combination with booster antennas, small transponders can be compared with conventional sized RFID tags. Due to the fact, that the presented booster technology is new, an novel antenna categorization is presented. Therefore, four different types are developed and introduced. Furthermore all advantages and drawbacks of the particular technology are discussed. Additionally

Chapter 4 shows that each booster antenna type enables new application scenarios and possibilities.

Related Work

The passive booster antenna technology provides several advantages, such as improving the overall robustness the RFID communication link. Therefore, state of the art smart cards are more and more equipped with inductively coupled booster antennas. [46] presents one of the first available smart cards presented by Infineon, that uses the inductively coupled booster antenna technology. However, the size of the coupling structure as well as the coil module is large. In contrast to this approach, Chapter 4 shows a feasibility study to combine chip scaled RFID tags with specially designed booster antennas. Due to this research, additional boosting technologies have been developed. For example, this thesis reports for the first time booster antennas that bases on a capacitive coupling concept.

Chapter 2

Small Form Factor RFID Systems

In the following sections the physics and theory of miniaturized RFID antennas operating at HF (13.56 MHz) and UHF (868 MHz) are discussed. In particular it will be shown that miniaturized (millimeter-sized) radiating RFID antennas become inefficient, especially on silicon as a substrate. However, the possibility of designing near-field loop antennas still remains. Field simulations and calculations present the outstanding capabilities of the magnetic and electric coupling in the near-field region. Note that additional booster antenna constructions presented in Chapter 4 are able to transform these near-field capabilities into radiating electromagnetic antennas that are able to operate in the far-field. 1

2.1 Radiating Electrically Small Tag Antennas

Nowadays antenna applications have a limited amount of available space and volume. Mobile phones, for instance, operate at 900 MHz/ 1800 MHz/ 1900 MHz GSM(2G) or 1955 MHz/ 2155 MHz UMTS(3G) frequency bands. The wavelength λ/ of these frequencies lies between $14 - 33$ cm. Due to the size limitation of mobile phones and other portable devices, small antennas, such as $\lambda/5$ and $\lambda/10$ antennas, are applied. This work focuses on highly miniaturized RFID transponders with HF (13.56 MHz) and UHF (868 MHz) operation frequencies. In the following the millimeter-scaled HF and UHF antennas are investigated.

Antenna miniaturization and electromagnetic wave propagation has been a research topic for decades. In 1947 Wheeler [109] addressed the first fundamental limit of a so-called "electrically small antenna" (ESA). He described the theoretical limits of bandwidth and radiation efficiency of antennas with very small dimensions. Based on Wheeler's work [109], an electrically small antenna is defined with dimensions d related to the equation 2.1.1.

$$d < \frac{\lambda}{2 \cdot \pi} \tag{2.1.1}$$

This relation is also often expressed by

$$k \cdot a < 0.5 \tag{2.1.2}$$

One year later, in 1948, Chu [16] described a boundary and sphere that encloses the ESA with $k \cdot a < 0.5$, while $k = 2\pi/\lambda$ (free space wavenumber) and a is the radius of the sphere in meter. This area is called the "Chu sphere". If this product is less than 0.5 the radiating element can be called ESA. Figure 2.1 illustrates the Wheeler product at the used frequencies 13.56 MHz and 868 MHz. As shown, an electrically small radiating 868 MHz antenna requires a sphere radius of 27.5 mm. As it can be seen, conventional 13.56 MHz RFID systems do not use radiating far-field antennas, since the ESA would already require a large sphere radius of 1.76 m.

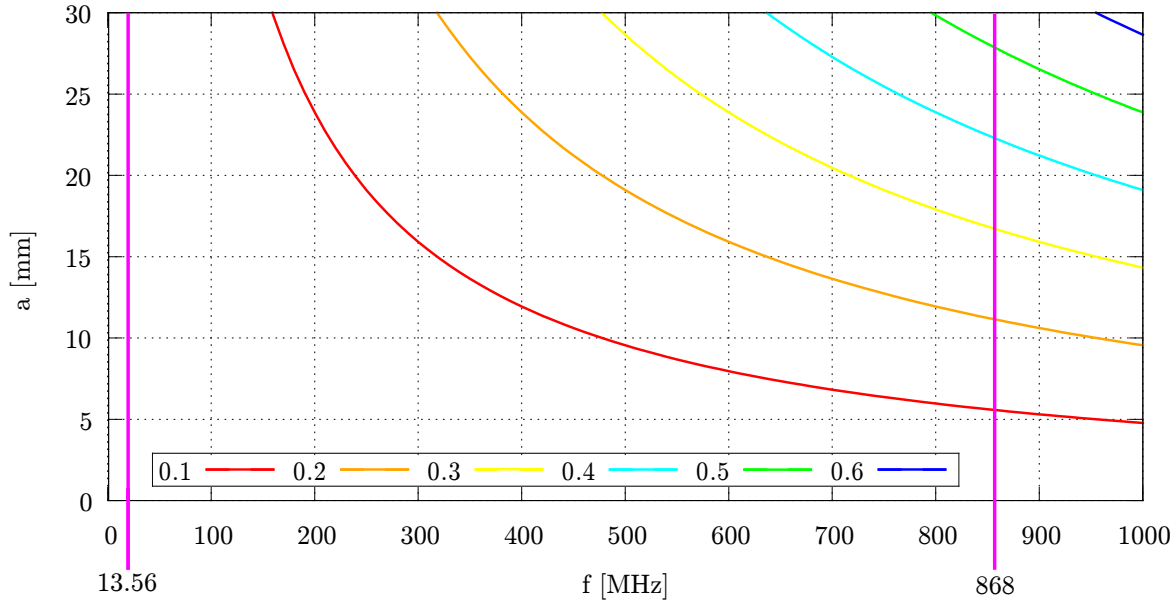


Figure 2.1: Wheelers product $k \cdot a$. The RFID operating frequencies at 13.56 MHz and 868 MHz are highlighted. If the product is < 0.5 the radiating element can be called an electric small antenna.

2.1.1 Radiation Efficiency

The antenna radiation efficiency is described by the factor η and can be calculated with the ratio of radiated power P_{rad} and delivered power to an antenna P_{in}. This factor can be also calculated by the resistive losses [115]:

$$\eta = \frac{P_{rad}}{P_{in}} = \frac{R_{rad}}{R_{rad} + R_{loss}} \tag{2.1.3}$$

While R_{rad} (Ω) describes the radiation resistance, R_{loss} (Ω) represents the overall material losses in dielectrics and the resistance of the conductor itself. The more the dimensions

of an antenna decrease, therefore reducing the product $k \cdot a$, the more R_{loss} dominates. As a result the efficiency also decreases.

2.1.2 Bandwidth Issues

It is well known that the bandwidth of an antenna is related to its geometrical dimensions [6]. Indeed, conventional RFID applications are using a very narrow frequency band. Therefore small antennas are feasible in some applications. Nevertheless the impedance of the particular RFID transponder and thus the frequency band can be shifted easily by tagging different objects. Diverse materials in the RFID transponder environment interact with the antenna structure. In any case, the design of an RFID transponder has to consider the environment. Unfortunately, it is one of the fundamental antenna rules that antennas with more volume have more bandwidth. Thus enlarging the antenna surfaces and dimensions, so that it is realized with bow-tie antenna configurations [92], the bandwidth is increased. A bow-tie antenna can be seen as many parallel dipoles with different lengths. Thus, many resonance frequencies and a broad bandwidth can be generated. [15] illustrates the relation between antenna dimensions and bandwidth for a presented electrical small antenna (0.24λ x 0.05λ).

2.1.3 Tag Impedance-Matching and Size-Reduction Techniques

In order to transfer the maximum power to the antenna, impedance matching is required [91]. Electrically small antennas can be matched at any operation frequency, using a matching network with reactive components. In general RFID antenna layouts are designed to embed this matching network. By avoiding lumped components, the RFID transponder can be obtained as a low-cost device. Unfortunately the additional network increases the overall loss resistance R_{loss} (see Formula 2.1.3). Especially electrical small antennas R_{loss} often exceeds the radiation resistance R_{rad}, which causes an additional reduction of the efficiency and performance.

In contrast to conventional antennas, the RFID transponder design does not need the 50Ω boundary anymore. Here the antenna designer has to consider the impedance of the transponder itself and all packaging effects. Typically the chip behaves capacitively, due to the integrated energy-storage. In order to achieve the conjugate complex match, the impedance of the antenna and its embedded matching network has to be inductive. This can be achieved easily by adding a shortened circuit which acts inductive. Then this configuration is connected to the radiating element (e.g a dipole) via galvanic or inductive coupling. Figure 2.2 illustrates common matching methods, such as the T-match, inductive coupled match or matching via nested slot antennas. A detailed description of this methods is presented by Marrocco [76]. [76] also describes and summarizes common size-reduction techniques, such as meandering and inverted-F configurations. A highly miniaturized meandered UHF RFID antenna can be found in [69] (1.7 cm x 1.4 cm) and

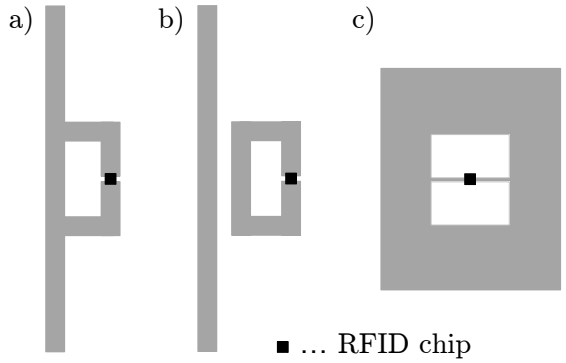


Figure 2.2: Common matching methods for UHF RFID antennas. Each antenna layout embeds a matching network to ensure a conjugate complex match to the capacitive impedance of the UHF RFID transponder: a) T-match method b) Inductive coupling match c) Matching via nested slot [76]

[15] (8.3 cm x 1.7 cm). However, both publications underline that the input resistance and antenna efficiency is distinct decreased. Furthermore, as already described, the bandwidth decreases with smaller antenna dimensions.

2.2 Silicon (Based) RFID Chip

Previous discussions have shown that the decreasing volume ($k \cdot a < 0.5$) of radiating far-field antennas leads to inefficiency. In order to increase the miniaturization level and to achieve the goal of on-chip antennas, higher frequencies have to be used. As [90] shows, a 1.5 mm x 3 mm scaled 5.8 GHz RFID transponder with on-chip antenna is feasible (meandered dipole). However, [90] as well as several other publications face the same problem: The standard semiconductor processes are not able to support the realization of efficient monolithic integrated radiating antennas. This is caused by two simple facts:

- Due to the substrate conductivity of $10 - 60\,\mathrm{S/m}$ (depending on the technology) [44], the material loss R_{loss} increases significantly. Therefore the efficiency will decrease as shown in formula 2.1.3.
- Due to the high dielectric constant of $\varepsilon \approx 11 - 12$ (depending on the technology), only a small amount of the power will be radiated into the air ($\varepsilon = 1$).

[5] illustrates the antenna design on silicon as substrate by giving an example with a dipole on silicon. Due to the difference of $\varepsilon = 1$ air and $\varepsilon = 11.7$ silicon, just 3% of the power will be radiated. 97% of the feed power will be confined into the substrate. Moreover, due to the substrate conductivity, surface waves cause additional losses. Nevertheless, [5] gives examples to counteract and to reroute the power, such as using metal shields

and reflectors at the top or bottom side of the silicon. Furthermore, a silicon lens is presented (see [5]). However these techniques are expensive post-processing steps and not suitable for each frequency band. Conventional CMOS process chip metals are arranged very close to each other. By using the first and the last metal, distances of $\approx 15\mu m$ can be achieved. Therefore metal shields can not be applied at a large distance from the antennas. Coupling between shield and antenna at frequency bands at $< 100GHz$ is unpreventable. Again, these antenna structures suffer from the standard semiconductor technology and provide less efficiency.

State of the art on-chip antennas are using high-resistivity substrates and operate at $6 - 90$ GHz frequency bands. A list of recent reported on-chip antennas can be found in table 2.1.

Reference/Developer	f $[GHz]$	Antenna type	Chip dimensions
Radiom[90]	5.8	Dipole	1.5 mm x 3 mm
Mustafa[75]	18	Dipole	3 mm x 0.21 mm
Dagan[18]	24	Dipole	3.6 mm x 1.6 mm
Chiou[14]	35 and 94	Dipole	1 mm x 2.9 mm
Kuo[57]	60	Yagi Uda	1.5 mm x 2 mm
Pan[85]	94	Dogbone array	2.2 mm x 1.6 mm
Sarkas[98]	120	Slot antenna	2.2 mm x 2.6 mm
Abbasi[1]	220	Slot antenna	2.75 mm x 1.75 mm

Table 2.1: State of the art monolithic integrated radiating antennas. The antennas are produced on high-resistive substrate in order to increase the antenna efficiency. The operation frequency of millimeter-scaled on-chip antennas is in the upper GHz range

2.3 Magnetically Coupled Near Field Tag Antennas

As discussed, the laws of nature do not allow the design of an effective, radiating, millimeter scaled antenna that operates at 13.56 MHz or 868 MHz. However, this does not apply to near-field antennas that are used in proximity coupled RFID systems. In this case, the reading distance between RFID interrogator and transponder is many times smaller than the wavelength of the magnetic field used. Due to the different effects and behaviors, it is very important to distinguish between near-field and far-field. If the distance between the interrogator and transponder is small, the electromagnetic wave propagation can be neglected [25]. Thus, only the magnetic field and its parameters have to be investigated. Equations 2.3.1 and 2.3.2 show the wavelength of HF and UHF.

$$\lambda_{HF} = \frac{c}{f} = \frac{3 \cdot 10^8\,\mathrm{m/s}}{13.56 \cdot 10^6\,\mathrm{Hz}} \approx 22.1\,\mathrm{m} \tag{2.3.1}$$

$$\lambda_{UHF} = \frac{c}{f} = \frac{3 \cdot 10^8\,\mathrm{m/s}}{868 \cdot 10^6\,\mathrm{Hz}} \approx 34.6\,\mathrm{cm} \tag{2.3.2}$$

The near-field of the particular frequency band ends with an distance of [25]:

$$r_{NF_{HF}} = \frac{\lambda_{HF}}{2 \cdot \pi} \approx 3.5\,\mathrm{m} \tag{2.3.3}$$

$$r_{NF_{UHF}} = \frac{\lambda_{UHF}}{2 \cdot \pi} \approx 5.5\,\mathrm{cm} \tag{2.3.4}$$

A detailed discussion of the near and far field, especially of the UHF RFID system, can be found in [76].

In this thesis the miniaturized antennas presented are millimeter scaled. To establish communication, small custom-built interrogator antennas are used. The reading distances of the tags are several millimeters. Thus the HF as well as UHF RFID systems operate in the near-field region. With the exception of the capacitive coupled RFID system, presented in section 3.4, all systems use the magnetic field as a communication channel.

2.3.1 Magnetic Field Strength

An electric current that flows in a wire causes a magnetic field. Figure 2.3 illustrates a small ($diameter = 10\,\mathrm{cm}$) coil that is connected to a current source. The wire thickness is 5 mm. As illustrated, the magnetic field is a vector field around the wire. The field direction can be determined with the "right hand rule" [25].

The magnetic field strength is directly proportional to the current I in the wire and decreases by distance r. Thus, for long and straight wires, the field strength can be calculated with equation 2.3.5 [25].

$$H = \frac{I}{2 \cdot \pi \cdot r} \tag{2.3.5}$$

This relation is also illustrated within the magnetic field simulation (performed with CST microwave [105]) in figure 2.4 at distances $> 2.5\,\mathrm{mm}$. In addition, the field strength is measured from the center of the wire, shown in figure 2.3, along the z+ axis. As can be seen, there is no field available in the center of the wire. The simulation uses a 5 mm thick copper wire and a 13.56 MHz signal. Thus the field strength increases rapidly underneath the wire surface ($\approx 20\,\mu\mathrm{m}$). This is related to the well known skin effect, which is caused by opposing eddy currents induced by the alternating magnetic field.

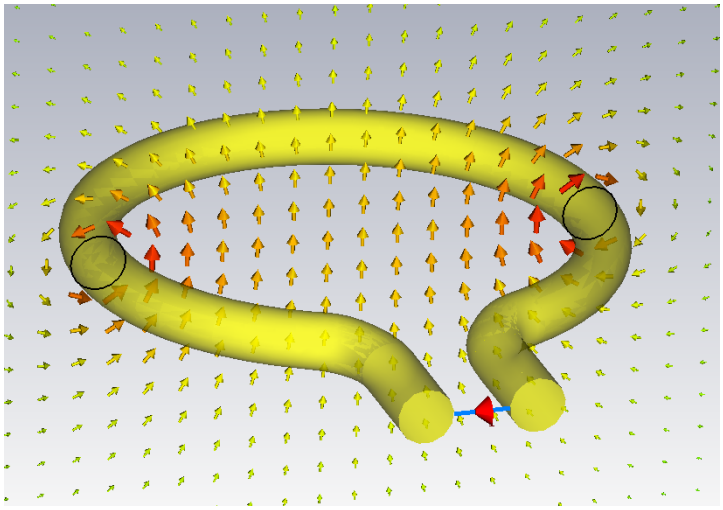


Figure 2.3: Magnetic field propagation in a small ($d = 10\,\text{cm}$) coil. The wire thickness is 5 mm.

The skin effect describes the AC distribution inside the conductor and is related to the material and frequency used. As the current density J is largest near the surface of the conductor, the field strength is at its maximum [25].

2.3.2 Skin Depth

As already mentioned, the largest current density is near the surface of the conductor. Then it decreases exponentially towards the center of the wire. The skin depth is defined as a value where J is reduced to 1/e [54]. Thus it can be said that 63% of the alternating current flows between the surface of the wire and the skin depth δ. In the simulation, shown in figure 2.4, a copper wire and a frequency of 13.56 MHz is used. Therefore the skin depth δ is very small $\approx 20\mu m$. It can be calculated with the approximation [54]:

$$\delta = \sqrt{\frac{2 \cdot \rho}{\omega \cdot \mu_r \cdot \mu_0}} \tag{2.3.6}$$

Where ρ represents the resistivity of the conductor, ω is the angular frequency, μ_r the relative permeability of the conductor and μ_0 the free space permeability ($\mu_0 = 4 \cdot \pi \cdot 10^{-7}\,\text{N/A}^2$). In the case of non-metallic conductors, such as silicon, δ can be calculated more precisely with [54]:

$$\delta = \frac{1}{\omega} \cdot \{(\frac{\mu \cdot \varepsilon}{2})[(1 + (\frac{1}{\rho \cdot \omega \cdot \varepsilon})^2)^{1/2} - 1]\}^{-1/2} \tag{2.3.7}$$

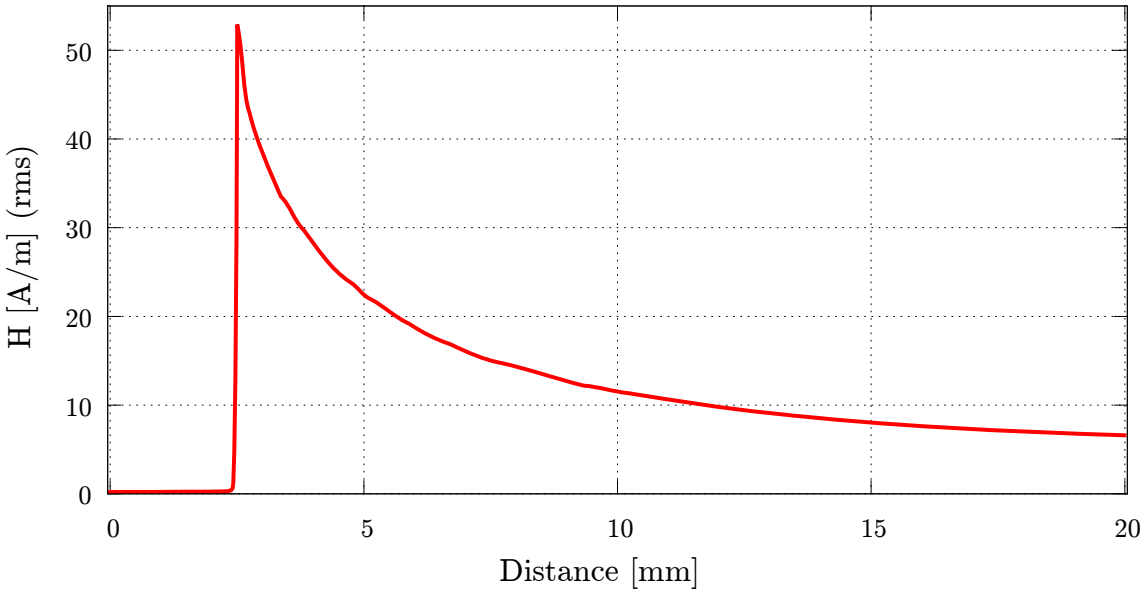


Figure 2.4: Field strength H from the loop center, shown in figure 2.3, in z+ direction.

This expression makes it possible to consider the permittivity ε of the material ($\varepsilon = \varepsilon_r \varepsilon_0$).

This thesis presents multiple near field RFID antennas that are arranged very close to metallic and other disturbing materials, for example antennas that are arranged on the top of a silicon based chip. The antenna generates a magnetic field that can be easily damped and shielded by particular materials, such as chip metals. Again this effect is related to the skin depth. In other words, the relationship of disturbing material parameters and the operation frequency used describes how much magnetic field is able to penetrate. Figure 2.5 shows the skin depth versus the operation frequency of some investigated metals. The frequencies 13.56 MHz and 868 MHz are highlighted. Chip metals typically consist of copper or aluminium. As can be seen, the skin depth for copper is $\approx 20\mu m$ at 13.56 MHz and $\approx 2.5\mu m$ at 868 MHz. In general, the thickness of chip metals in a state of the art CMOS process is smaller than one μm. Moreover, the chip metals are very fragmented and not solid metal surface structures. This consideration already hints that chip scaled RFID coil antennas are feasible.

2.3.3 Magnetic Flux Density

The magnetic flux density (B) is related to the field and the permeability (μ) of the medium where the field is measured. Therefore the flux density is defined by [25]:

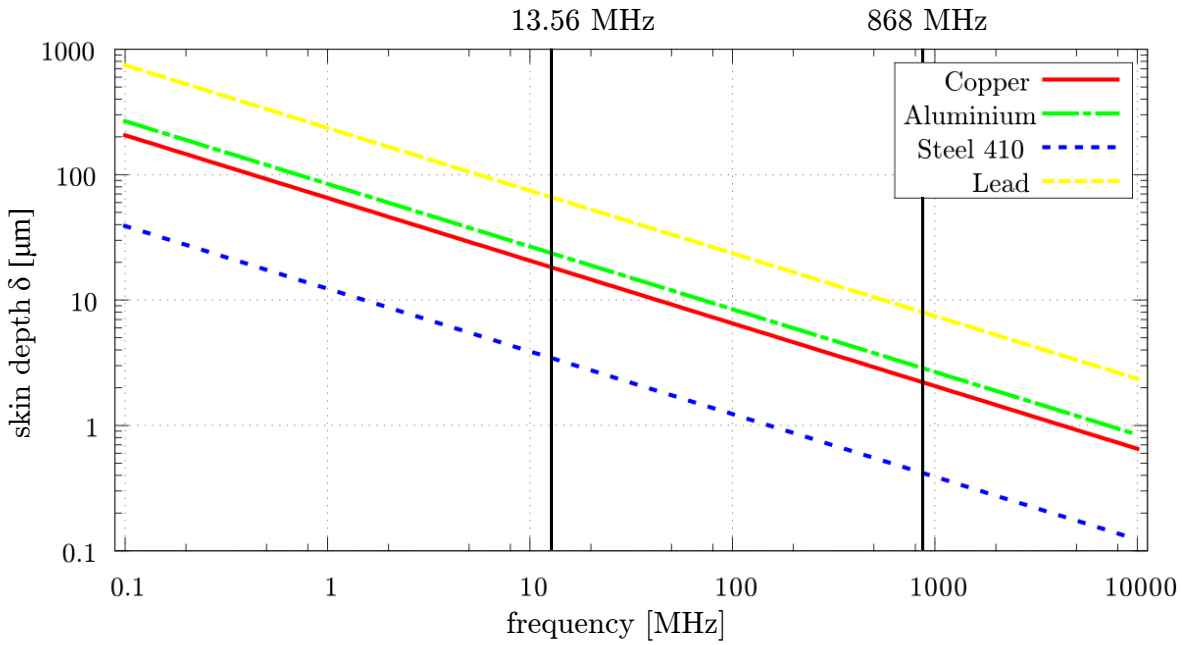


Figure 2.5: Skin depth of different materials at HF and UHF

$$B = \mu_0 \cdot \mu_r \cdot H = \mu \cdot H \tag{2.3.8}$$

2.3.4 Optimum Near Field Antenna Size

In inductive coupled near field RFID systems, the antennas used are typically designed as coils with one or more windings. Certainly the magnetic field strength is often measured in the middle of the antenna. Again the field strength is directly proportional to the current that flows in the coil and decreases by distance. The field strength of an simple loop antenna (or coil), such as that shown in Figure 2.3, can be approximated with formula 2.3.9 [25].

$$H = \frac{I \cdot N \cdot R^2}{2 \cdot \sqrt{(R^2 + z^2)^3}} \tag{2.3.9}$$

Where N represents the number of windings, R is the radius of the loop antenna and z the distance to the center of the coil in z-direction. Note that this expression is only valid for very short distances and planar coils: $length \ll R$. In addition it is only valid in the near field region: $z < \lambda/2\pi$.

Figure 2.6 shows calculations of three different very small antenna geometries. The graphs represent the field strength values along the z axis H(z). As can be seen, the

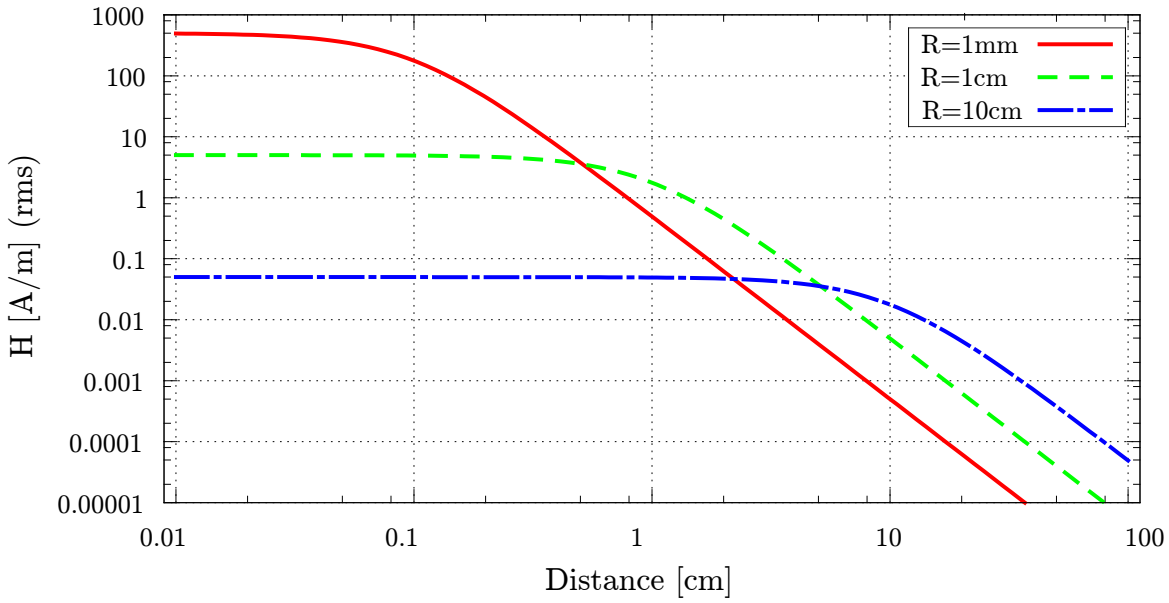


Figure 2.6: Magnetic field strength in the middle of small loop antennas. In contrast to a large loop antenna, a small coil provides a strong field strength. Nevertheless H decreases rapidly at a distance of $\approx \sqrt{2}$ and larger antennas perform better.

smallest antenna ($R = 1\,\text{mm}$) generates the highest available field strength in the center of the antenna. Nevertheless, a bigger antenna provides a higher field strength at larger distances to the antenna. In contrast, the smaller antenna already loses a lot of field strength with increased distance. Thus it can be said that, depending on the application (= desired reading distance), the antenna geometries can be optimized. With regard to [25], the optimum size of the antenna can be calculated with:

$$R = z \cdot \sqrt{2} \tag{2.3.10}$$

With this observation, reading distance limitations of small RFID transponders can be ascertained. Due to the decreasing field strength, millimeter scaled RFID near field antennas are not able to propagate a strong magnetic field over larger distances (e.g. cm).

Chapter 3

Small RFID Tags

The miniaturization of RFID transponders is one of the most challenging objectives. Due to the steady decreasing transistor scaling, the number of transistors on silicon is increasing exponential [72]. Therefore the required area of silicon decreases too. Regarding [29], 9 nm transistors can be seen as a physical scale limitation. Note that this dissertation uses 130 nm and 65 nm Complementary metal-oxide-semiconductor (CMOS) processes. As it is discussed, the integrated circuit (IC) development is pushing the miniaturization of RFID silicon chips to its limits. Although the size of analog parts cannot be decreased arbitrarily. The dimensions of inductors, capacitors as well as the transistor dimension in the analog front-end and voltage regulation depends to the required parameters of the particular component. Nowadays the size of a conventional HF and UHF RFID chip is small as a grain. In contrast to the size of the silicon chip the RFID antenna represents the largest component of the tag. In general the size of the antenna is related to the read range, since small RFID antennas cannot reflect a strong signal or in other words, have less influence to the field of a reader device. Nevertheless as this work shows, highly miniaturized antennas are feasible although the read range is limited. Figure 3.1 describes the presented miniaturization levels of RFID tags. The illustrated pyramid is separated into the following classes:

Conventional RFID transponder ($> 2cm^2$)
Starting from the bottom of the pyramid, the size of the transponder decreases with the particular technology to the top. The size of conventional HF as well as UHF RFID transponders is large - several cm^2. In this category near-field HF and UHF loop antennas, as well as the electromagnetic dipole and its derivate are deployed.

While the HF frequency band and loop antennas typically dominate the near-field RFID applications, UHF RFID systems are used in the far-field region. Nevertheless, UHF loop antennas can be also found in some near-field application scenarios. An overview of conventional UHF near-field antennas can be found in [76]. The size of these standard near-field RFID tags is related to the reading distance. Thus, standard near-field tags are several cm^2 large.

A small UHF far-field antenna becomes less and less applicable. This is simply related to the limited space to realize a λ/x ($x = anyfactor$) antenna, such as a dipole. Certainly there are many UHF antenna-size reduction techniques, such as meandering a dipole or

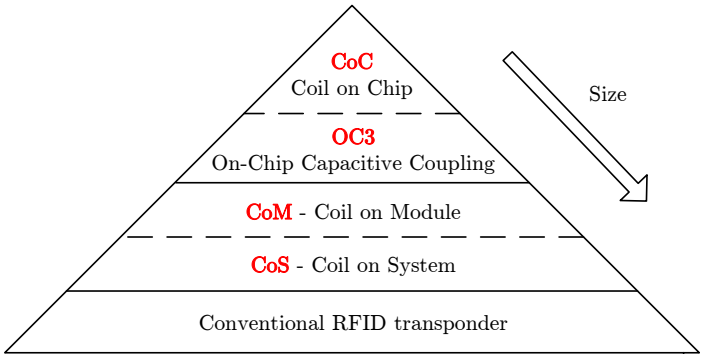


Figure 3.1: Size comparison of different RFID transponder miniaturization methods: The operation frequency of the presented transponders is $\leq$ 868 MHz. All types of miniaturized RFID tags are developed within this work and presented in this chapter. Each category has its advantages and drawbacks, as it is shown in the particular section.

inverted-F antenna (IFA) configurations [65]. However, a degradation of the radiation efficiency is unavoidable. One of the smallest UHF RFID antennas, presented in [65], has a size of 0.05 λ x 0.04 λ. Smaller than 2 cm^2 sized 868 MHz far-field antennas become more and more inefficient. Smaller radiating antenna geometries can be achieved with microwave RFID technology (2.4 GHz and 5.8 GHz).

Coil on Module (CoM) & Coil on System (CoS) ($2cm^2 > CoM \,\&\, CoS > 2mm^2$)
This class of miniaturization still describes two separate components. The RFID antenna, realized on a module, and the RFID silicon chip. At this level of miniaturization, the word antenna can be replaced by the word coil (CoM/CoS). Thus, just near-field loop antennas - coils - for HF as well as for UHF are feasible. These HF or UHF coils are produced separately and connected to the RFID chip in very small packages. Several packaging technologies lead to different miniaturization levels. This category includes coil-carrier devices connected to the RFID chip, for example a little FR4 board. In November 2012 Murata released one of the "first mass-produced 3.2 mm x 3.2 mm x 0.7 mm HF CoM RFID memory-tag" [103]. In this case a Low Temperature Cofired Ceramics (LTCC) packaging technology was used. A multi layer HF RFID antenna is arranged in several ceramic layers, assembled and connected to an HF RFID tag. The Coil on System (CoS) technology is similar to the CoM concept. The major difference lies in additional components, such as sensors which are connected to the RFID chip.

Coil on Chip (CoC) ($\sim 1mm^2$)
Doubtless the highest possible level of miniaturization is to produce a monolithic RFID chip suited with a chip scaled coil. To realize the coil, CMOS process metals or redistribution layers are used. As it is shown in the next sections, this technology allows to develop RFID transponders with a size less than $1mm^2$. This concepts is representing the top of the pyramid, shown in figure 3.1.

On-Chip Capacitive Coupling (OC3) ($\sim 1mm^2$)
The on-chip capacitive coupling represents a novel couple mechanism for RFID systems that was developed within this PHd work. Instead of inductively coupled coils, the capacitive coupling of metal surfaces is utilized. This allows a further miniaturization of the RFID transponder. This work presents a $1.2mm^2$ sized capacitive coupled RFID tag. However, in contrast to inductive coupling the capacitive coupling mechanism causes a further limitation regarding the reading distance.

3.1 System in Package Tags

This section presents a novel three-dimensional (3D) embedded wafer-level ball grid array (eWLB) system in package (SiP) solution for biochips and micro labs. This miniaturized 3D SiP includes three major components, a complementary metal oxide semiconductor (CMOS)-tunnel magneto resistance (TMR) sensor biochip for magnetic bead-sensing stacked on a radio frequency identification microchip and a 13.56 MHz coil antenna for wireless energy and data transfer. The power supply and the serial peripheral interface (SPI) chip interconnections between the CMOS-TMR sensor biochip (slave) and the RFID microchip (master) are implemented with a novel embedded Z-line (EZL) vertical contact technology through the mold compound. The 13.56 MHz antenna is embedded into the fan-out area of the bottom redistribution layer of the eWLB. With this setup it is possible to maximize the RFID reading distance and to ensure a displacement to the TMR sensor surface. An overall volume of the 3D SiP of only 5.6 mm x 3.6 mm x 0.7 mm could be achieved, applying the eWLB technology. Due to the RFID technology the developed 3D SiP does not need any external contacts and cabling. Therefore it can be encapsulated into harsh environments. In addition the top fan-out surface of the eWLB can be used for adhesive bonding to higher level analyzing setups. The results demonstrate that innovative SiP technology using the eWLB technology combined with chip and antenna design allow to realize modern subsystems e.g. for medical applications.

Original Publications Related to this Section

W. Pachler, K. Pressel, J. Grosinger, G. Beer, W. Bösch, G. Holweg, C. Zilch, and M. Meindl, „A Novel 3D Packaging Concept for RF Powered Sensor Grains" In: Electronic Components & Technology Conference (ECTC), 2014 IEEE International Conference on. May 2014

3.1.1 Packaging concepts for medical applications

The point-of-care (POC) technology for health care already makes inroads into our life [7]. Various simple biological rapid tests are available on the market, such as blood glucose testing, pregnancy testing, and hemoglobin diagnostics. These tests are fast, low-cost, effective and simple. However the diagnostic of life-threatening infections and complex illnesses such as sepsis and cancer is still done by laboratories. If there is a serious illness suspicion, specialists need to analyze blood or tissue samples with time-consuming and expensive procedures.

Recently, the number of reported highly miniaturized sensor grains or micro labs has increased significantly. Amperometric measurements with biochips [61], impedance

spectroscopy [64], or even deoxyribonucleic acid (DNA) detection using complementary metal oxide semiconductor (CMOS) sensor arrays [74] [100] were published in the last years. Indeed these prototypes promise affordable POC diagnostics for complex diseases. Nevertheless the custom made analyzing hardware and data interfaces are far away from commercial viability. In particular the biochip packages are connected with bond wires [61, 64, 74, 100]. The bond wires and the non-active/sensing chip surface are encapsulated with silicone or epoxy. The mechanical robustness and commercial viability of this approach are debatable. Furthermore the analyzing hardware is often realized with external microcontroller- or field-programmable gate array (FPGA)-boards. The dimensions of such assemblies lead to various drawbacks for POC diagnostic systems.

To introduce the POC technology into the consumer market, the work presented here, demonstrates a novel approach for the design of heterogeneous three-dimensional (3D) biochip packaging. All biochip components are assembled within a minimum volume utilizing the embedded wafer-level ball grid array (eWLB) technology. The presented system in package (SiP) includes a CMOS-tunnel magneto resistance (TMR) sensor biochip for magnetic bead-sensing, which is stacked on a radio frequency identification (RFID) microchip, and a 13.56 MHz coil antenna for wireless energy and data transfer. The RFID chip enables the SiP to work autonomously. Other benefits of the presented SiP are that it can easily be attached to higher level systems and that it assures an unprecedented prototype in the field of biochip and in general fluidic micro labs due to planar surfaces simplifying sealing. This application demonstrates that the eWLB technology has outstanding capabilities to design innovative SiP solutions.

The section is organized as follows. First a brief description of the CMOS-TMR biochip and its application is provided. Then the design of the eWLB 3D SiP is presented. This section focuses on all the SiP components and the benefits achieved by applying the eWLB packaging technology using for the first time the vertical contact embedded Z-line (EZL) technology. Next, the results on the contactless RFID communication interface of the presented eWLB SiP and the 13.56 MHz antenna is shown. A electromagnetic field simulations of the antenna in the package and verify them by measurements is discussed. Finally, conclusions is drawn that point out the unique concept which enables new capabilities and leads to affordable POC diagnostic systems in the field of complex medical applications.

3.1.2 TMR Biochip Application

The presented CMOS-TMR biochip was developed within the EU-funded project “eBrains” [104]. The main aim of the biochip is to detect magnetically marked bio-molecules from test substances, such as a blood sample. After a preparation procedure and the immobilization of these DNA molecules (see Figure 3.2), magnetic beads are hybridized on to the sensor array of the biochip. Special bound magnetic beads can be detected by the use of the TMR biochip surface. TMR cells change the resistance with the magnetic field

[8]. Therefore the biochip also comprises analog-to-digital converter (ADC) and memory banks to detect and save the change of these resistances. Different pathogens, which are detected, can lead to a complex diagnosis, such as to diagnose sepsis.

The chip features 8 x 16 sensor spots with 32 x 32 TMR cells each. In contrast to recently reported biochips, we packaged the TMR biochip with a novel eWLB technology concept. The eWLB 3D SiP, which is the main focus of the paper, can be easily attached to a micro-fluidic card as shown in Figure 3.2. Furthermore the SiP could also be applied to realize intelligent measurement tapes.

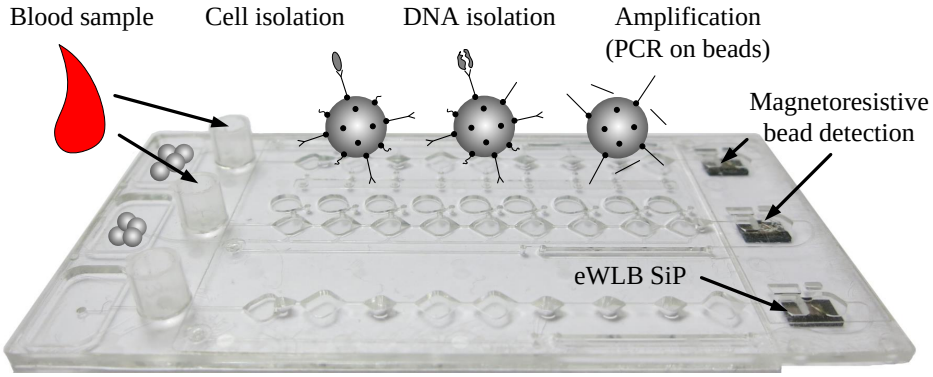


Figure 3.2: POC micro-fluidic card: A blood sample is inserted to a micro-fluidic cartridge and binds to paramagnetic beads. Three steps are fulfilled until the presented eWLB 3D SiP detects the magnetic beads: cell isolation, DNA isolation, and amplification. Circle: one of the three eWLB SiPs.

3.1.3 3D eWLB Biochip Packaging Concept

The main focus of the presented SiP is the innovative eWLB packaging concept. The eWLB technology is an innovative packaging technology developed during recent years [68]. The technology was developed to cross the interconnect gap, to achieve further miniaturization, and to reduce parasitic effects. The package has excellent capabilities for high frequency applications and allows outstanding capabilities to design innovative SiP solutions. During recent years Infineon developed a magnitude of toolbox elements for this technology [86]. Within this work novel and unrepresented toolbox elements were developed and applied to the example of the presented novel medical application. Figure 3.3 shows the example of a basic eWLB package [111]. The cross section shows a silicon chip that is connected via a redistribution layer to solder balls. These balls than can be connected to other components such as a FR4 board. The fan-out area provide additional space for the redistribution layer routing to further balls. As it is presented this fan-out area can be also used for novel radio frequency capabilities.

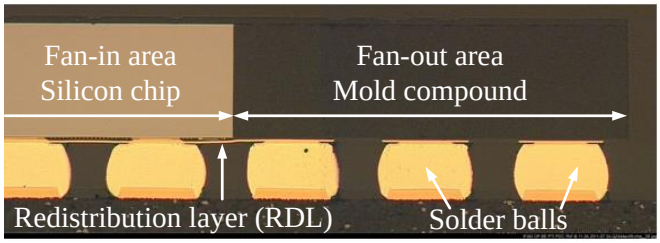


Figure 3.3: Basic eWLB package: The fan-out area can for example be used for the design of inductors, antennas, or vertical contacts [10].

Figure 3.4 shows a schematic of the eWLB process flow. This is provided here to demonstrate the packaging of the medical SiP demonstrator setup. Regarding [9] the process flow can be divided into three main parts:

- **Reconstitution:** Regarding to the used packaging concept, the chips are arranged onto a metal carrier. A sticky tape fixes the chip position. Then, the mold-process creates a new wafer filled with a molding substance. After this process the metal carrier and the sticky tape can be removed.
- **Redistribution:** As the name of this part of the eWLB process flow suggests, a redistribution layer is added onto the top of the generated mold-wafer. Therefore a two dielectric layers are used to embed the redistribution layer. One dielectric layer separates the RDL from the chip and the second dielectric Layer is used for encapsulation.
- **Ball apply with singulation:** The last eWLB process flow step adds connections to the redistribution layer. Therefore large solder balls are used. After this step the package is ready for laser marking and the eWLB wafer can be diced into pieces.

In case of wireless energy/data transfer the ball apply for external connections is simple skipped. The eWLB assembly technology offers outstanding capability for 3D system integration. On the one hand chips can be advantageously placed side by side. On the other hand the chips can be stacked in the package and additional passive components can be integrated. The fan-out area provides more space for additional solder balls and routing. Furthermore it can be used to add passive components to the package, as reported in [110]. Due to the material characteristics of the mold compound (e.g. dielectric constant $\varepsilon_r = 4.1$) [110], the fan-out area can also be used for antennas. The reported eWLB packages are typically mounted to higher level carrier boards connected via solder balls. Figure 3.5 shows various toolbox elements to generate SiP devices. The cross-section on the left shows two dies stacked and a redistribution layer (RDL) on top and bottom of the eWLB. In addition passive components were soldered on top of the package. Furthermore a through encapsulated via (TEV) vertical contact was designed. Two choices were investigated in the past: (i) via bars that are based on printed

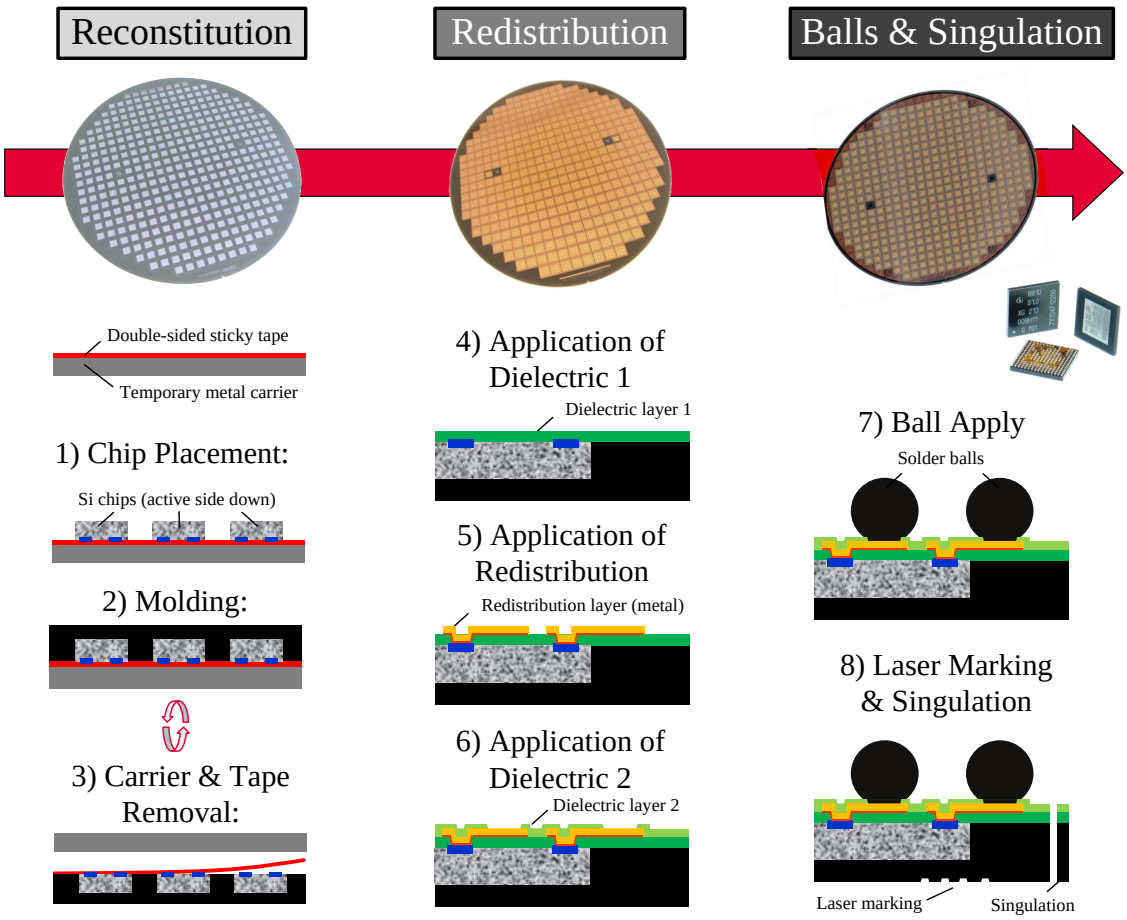


Figure 3.4: The three main parts of the eWLB process flow: reconstitution, redistribution, and balling and singulation. In the case of wireless energy/data transfer of the presented eWLB packaging concept, the ball apply for external connections is simple skipped.

circuit board (PCB) technology (shown in the middle); (ii) TEV filled with copper by electroplating (applied in the left SiP).

For this work two chips, the power management RFID chip, and the TMR biochip with an array of 8 x 16 independent sensor cells are required to be integrated. This work disclaims the use of any external contact. An RFID microcontroller chip provides the data and energy interface between the biochip and a reader device. In order to miniaturize the size of the biochip package, the chips were stacked above each other. The area of the overall package was designed to meet 5.6 mm x 3.6 mm. Due to the smaller size of the TMR biochip (4.3 mm x 2 mm), 43% of the resulting top surface was fabricated as fan-out mold compound. While the top fan-out surface is used for adhesive bonding and fluidic sealing to the already described micro-fluidic plastic card, the bottom

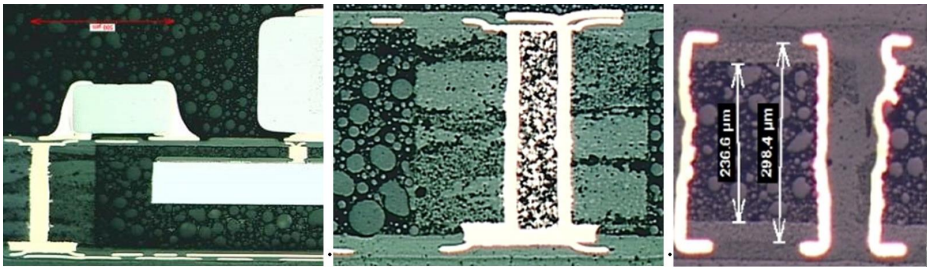


Figure 3.5: Various toolbox elements to build SiP devices: The figure shows a 3D-SiP with two dice stacked and passives on top (picture on the left), a TEV made of via bars (picture in the middle), and a TEV made with laser drilling and filled with copper by electroplating (picture on the right).

fan-out area provides enough area to embed the high frequency (HF) RFID antenna. The RFID antenna itself, as well as the routing is realized with two RDLs. Each coil antenna with more than one winding needs an underpass. To realize this underpass and to interconnect the bottom RDL with the top RDL through the mold compound, a novel vertical contact, the so-called EZL technology is used. The produced eWLB wafer as well as the reconstitution step and arrangement of each component (RFID chip, TMR biochip and EZL) is illustrated in Figure 3.6.

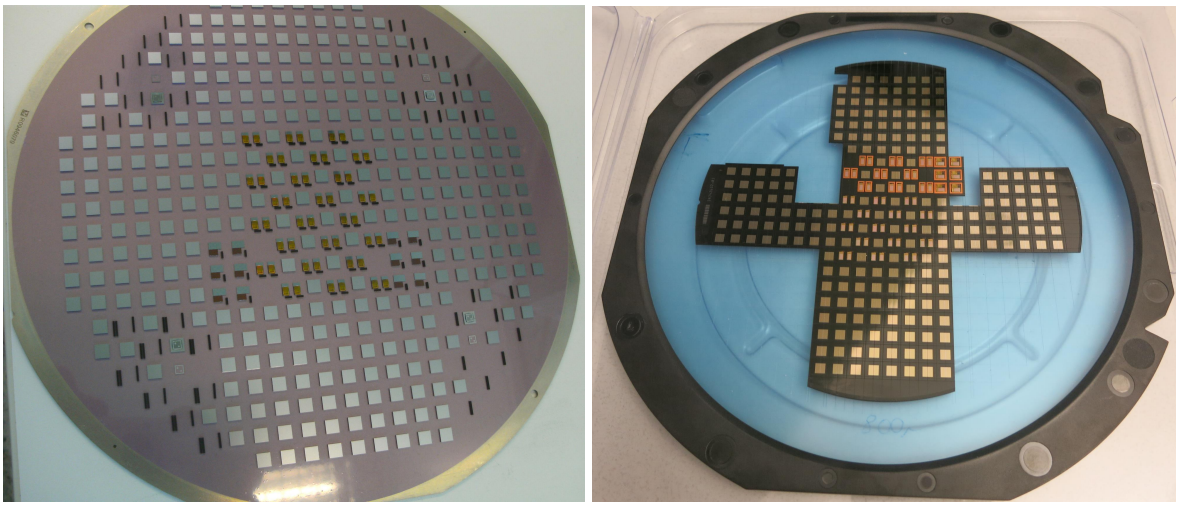


Figure 3.6: (left) reconstitution step: the chips and the EZL is arranged in the proper position onto temporary metal carrier with a double-sided sticky tape (see Fig. 3.4); (right) final produced eWLB wafer. After the molding process the carrier is removed, dielectrics and RDLs are created. Finally the singulation process cuts the wafer into autonomous pieces.

The EZLs are prepared components based on the eWLB RDL technology. Contact lines are generated by the eWLB thin film technique just on mold compound. This mold

compound is then cut into pieces. The components are then turned by 90° and placed as independent components on the artificial wafer (see Figure 3.4: eWLB redistribution). The EZL has the advantage that much finer structures can be generated than for via bars and laser drilled TEVs.

Figure 3.7 shows a top view of the EZL component (black) together with the power management chip, which is stacked onto the TMR sensor chip before molding (compare Figure 3.4 left). Figure 3.7 shows the two semiconductor chips stacked on each other together with the EZL component, which includes the vertical contacts, next to them. Only a limited number of the two active devices were available due to early silicon on shared reticle. Thus, a few quadratic silicon dummy chips to compensate voids had to be used. Identical silicon content is needed during molding to achieve homogeneous moldflow. Additionally a small number (12 samples per eWLB wafer) of the side by side packaging concept is realized as a backup solution. As the name side by side suggests, both chips are arranged next to each other. However, this chip arrangement requires a larger SiP space. Nevertheless this concept was added for comparison reasons. Both concepts and layouts are illustrated in Figure 3.8. Again for visualization the reconstitution step is highlighted. The size of the side by side concept is increased to 6.9 mm x 6.9 mm.

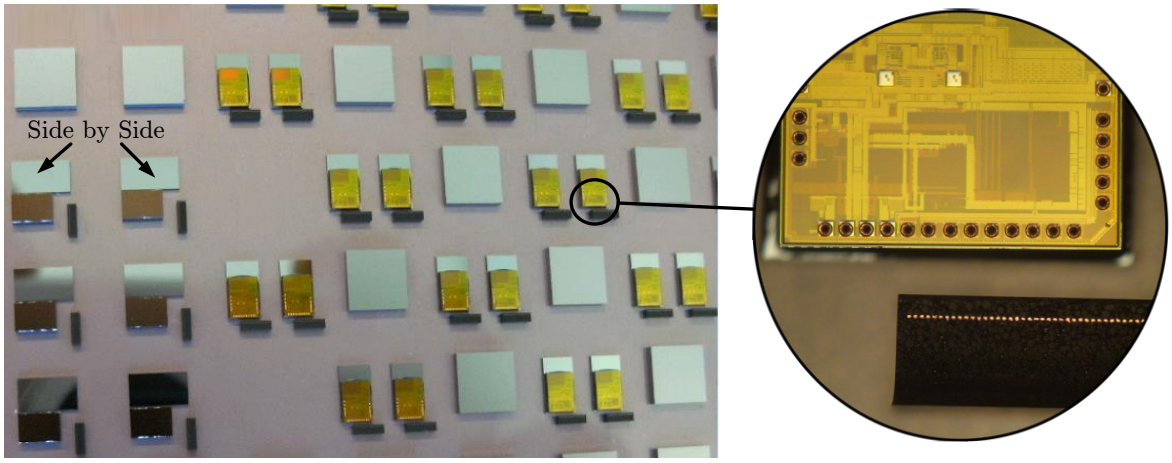


Figure 3.7: (left) The two stacked semiconductor chips next to the black EZL device with a quadratic dummy silicon chip before molding; (right) the top view of an EZL device (black) with the power management chip (yellow) is highlighted. Additionally a large side by side design/concept was added to the process flow for comparison reasons (marked left).

Fig 3.9 shows a computer tomographic picture of the produced SiP. The chips and all metallic materials are illustrated. The size of the bottom chip (blue) is 3000 μm x 2100 μm. It is directly connected to the HF coil antenna. As it can be seen the coil antenna, realized on the bottom RDL, surrounds the chip at its fan-out area. Due to the fact, that no chip metal coats the antenna, the parasitic capacitance of the

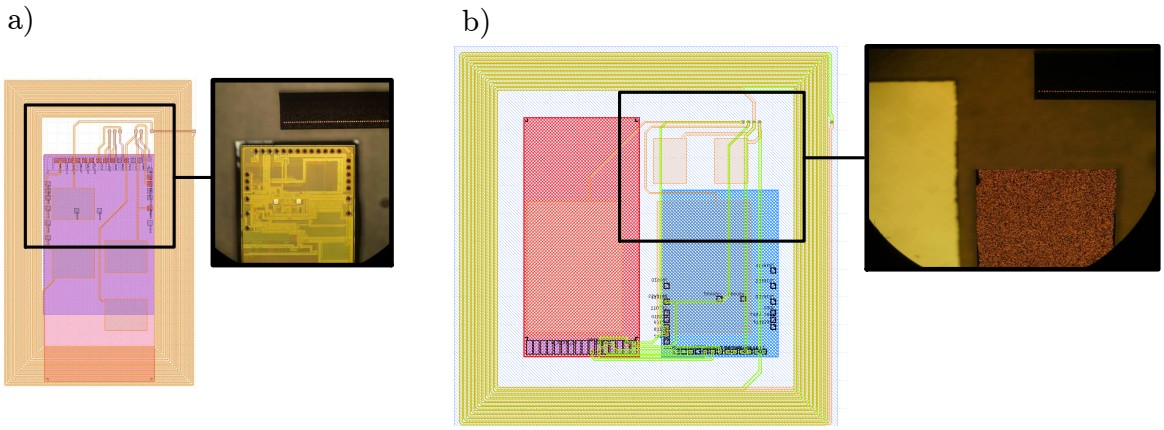


Figure 3.8: a) presented miniaturized face to face (stacked) eWLB concept. The chip arrangement at the reconstitution step is highlighted. The overall size of the package is 5.6 mm x 3.6 mm b) side by side backup packaging concept. By arranging the chips next to each other, the required eWLB SiP space increases to 6.9 mm x 6.9 mm

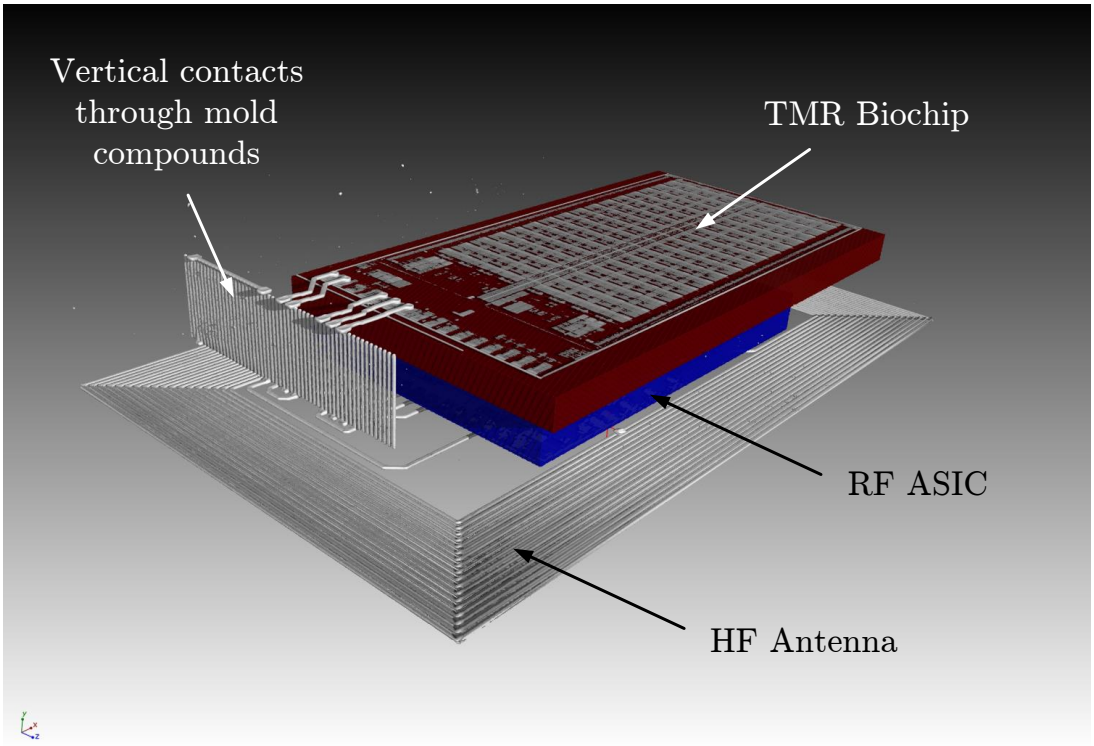


Figure 3.9: Computer tomography of the produced eWLB package. The biochip and the radio frequency communication chip are arranged above each other. The interconnection is realized with vertical contacts through the mold compounds.

antenna could be minimized. The size of the top chip (red) is 2075 μm x 4300 μm. The computer tomography image shows the chip metals and the TMR sensor array. The TMR biochip is connected with the top RDL. There are five interconnections. While the first two connections (left) provide the power supply (VDD and GND), the other connections realize the data interface to the RF chip. The data interface is designed as serial peripheral interface (SPI). Therefore there are three more connections: MISO (master in slave out), MOSI (master out slave in), and CLK (clock). Fig 3.10 illustrates the produced novel eWLB package with chip stacking and through mold compounds. The overall size of this eWLB packaging concept is 5.6 mm x 3.2 mm. Furthermore Fig 3.10 illustrates the produced backup concept. In contrast to the stacked version the size of the side by side concept is increased significantly to 6.9 mm x 6.9 mm. In order to enable the liquid to touch the TMR biochip sensor surface, all dielectric layers are opened at this certain area. This functional area can be also seen in Fig 3.10 (shiny TMR surface).

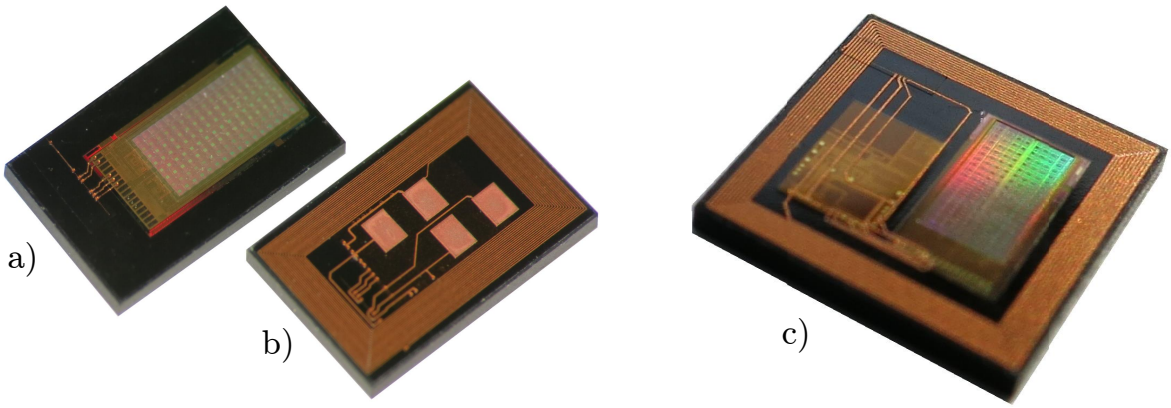


Figure 3.10: a) top side and b)bottom side of the produced novel SiP eWLB package with stacked chip arrangement. The overall size of the eWLB SiP package is 5.6 mm x 3.2 mm. c) Produced side by side eWLB package. Within this concept the chips are arranged next to each other. Therefore the overall size is increased to 6.9 mm x 6.9 mm. The dielectric layers on the top side are opened at the sensor area.

3.1.4 Contactless Communication Interface

As already mentioned in chapter 2, near field RFID transponder (tag) antennas that operate in the HF band at 13.56 MHz are resonant loop antennas. The geometrical dimensions and the antenna environment determine the electrical parameters of the antenna, i.e. the value of the inductance, resistance, and parasitic capacitance. Due to the magnetic coupling between two loop antennas of the RFID reader and the tag, the RFID reader is able to transfer energy and data by modulating the magnetic field. In this presented application a high-end Infineon micro-controller with an RFID interface

is used. This controller supports the 13.56 MHz ISO 14443 A/B ?? and ISO 18092 ?? (NFC) standard.

Loop antenna design

In order to design a small resonant loop antenna for the tag, the input impedance of the tag microchip has to be considered. A simplified equivalent circuit of the presented SiP HF RFID tag is illustrated in Figure 3.11. It is important to note that this equivalent circuit is only precisely correct at the designed operating frequency of 13.56 MHz. Moreover this equivalent circuit can only used due to the outstanding capabilities of the eWLB molding substance and the RF-supporting fan-out area. The losses in the mold compound are negligible. Nevertheless it has influence to the parasitic capacitance.

The analog frontend of conventional HF RFID chips is usually equipped with an additional parallel on-chip capacitor. Typically the capacitor values are in the range of several picofarad (pF). With a good resonant antenna design no additional passive tuning elements are needed. Due to the fact that the size of the presented SiP and therefore the size of the loop antenna (smaller value of inductance) are miniaturized to single digits of millimeters, this additional chip capacitance is increased to 56 pF.

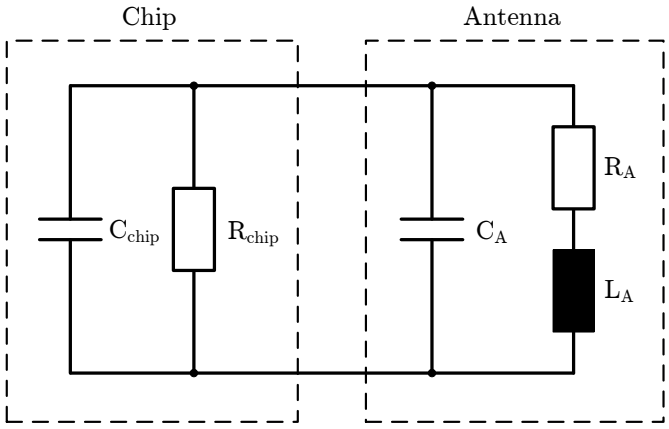


Figure 3.11: Equivalent circuit of the tag: The voltage dependent elements, the capacitance C_{chip} and the resistance R_{chip}, represent the tag chip. The connected HF antenna is characterized by the frequency dependent capacitance C_A, resistance R_A, and inductance L_A circuit.

The values of C_{Chip} and R_{Chip} are voltage dependent as already mentioned and illustrated in Figure 3.11. Due to the well-defined application of the presented eWLB SiP application a chip capacitance of $C_{Chip} = 56\,\text{pF}$ is chosen. The HF antenna is characterized by the frequency dependent capacitance C_A, resistance R_A, and inductance L_A circuit. The coil inductance L_A depends on the size of the antenna, especially on the length of the

wire-track and the number of windings (due to mutual coupling from one winding to each other). The resistance R_A describes the losses in the antenna. The resistance includes not only the frequency independent material specific resistive losses of the coil metal; it also describes frequency dependent losses due to eddy currents and the skin effect. The proximity effects of metallic environments influence the antenna [88]. Due to the small eWLB 3D SiP, the metals of the two chips, the EZL and the RDL routing influence the electrical parameters of the small antenna. These effects have to be considered in the antenna design. As already mention before, the capacitance C_A describes the parasitic capacitance of the antenna. As it can be seen in Figure 3.10, the coil antenna is embedded in the fan-out area of the eWLB package and surrounds the RFID chip. As a result, no chip metal is in close vicinity of the antenna and the electric coupling. Thus, the parasitic capacitance is minimized. The remaining capacitance C_A is due to the electric coupling between the coil windings. This coupling is affected by the dielectric constant of the mold compound ($\varepsilon_r = 4.1$). Figure 3.12 shows the bottom side of the package and the RDL of the eWLB SiP. The fabricated bottom RDL can also be seen in Figure 3.10b. This RDL is used to realize the coil antenna and to connect to the RFID chip. Measurement pads and connections for possible additional passive capacitors were added to the design (Figure 3.12). The overall size of the coil spans to 3570 μm x 5775 μm. The track width and the gap width between the coil windings is 20 μm. In order to design a resonant loop antenna, the electric parameters of the coil have to fulfill Equation 3.1.1:

$$f_\mathrm{r} = \frac{1}{2 \cdot \pi} \cdot \sqrt{\frac{1}{L_\mathrm{A} \cdot (C_\mathrm{Chip} + C_\mathrm{A})} - \frac{{R_\mathrm{A}}^2}{{L_\mathrm{A}}^2}} \tag{3.1.1}$$

Antenna simulation and measurements

The electromagnetic simulation of the antenna is done with the 3D electromagnetic field simulator CST Microwave Studio [105]. The simulation shows that 19 coil windings generate the required inductance of L_A. The unknown parasitic capacitance C_A and the resistance R_A of the 13.56 MHz antenna are also determined by simulation. The inductance and the parasitic capacitance of the simulated 19 turn loop antenna is $L_A = 2.33\,\mu$H and $C_A = 2.45$ pF. The magnetic field and thus the loop antenna is slightly influenced by the eWLB packaged CMOS chips as shown in Figure 3.13. We observe that the magnetic field is damped to the top side. At the bottom side the magnetic field is able to propagate unhindered.

Figure 3.14 shows the simulated and measured reflection coefficient S11 at the antenna input. The measurement was done with a vector network analyzer. The illustrated Smith Chart is normalized to 50 Ω. Figure 3.14 also considers the the parallel capacitor C_{Chip} of the chip at the simulation and measurement ports. The material resistance of the RDL coil is displayed at the direct current (DC) or low frequencies (e.g. 500 kHz). The simulation

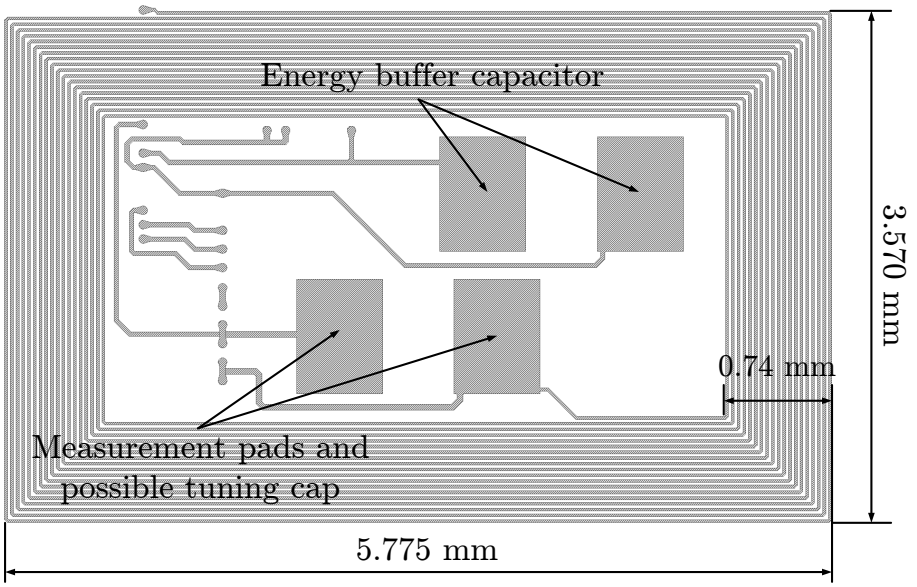


Figure 3.12: Geometric dimensions of the coil antenna (bottom side of eWLB package - redistribution layer): The HF RFID coil antenna consist of 19 windings with track and gap widths of 20 um.

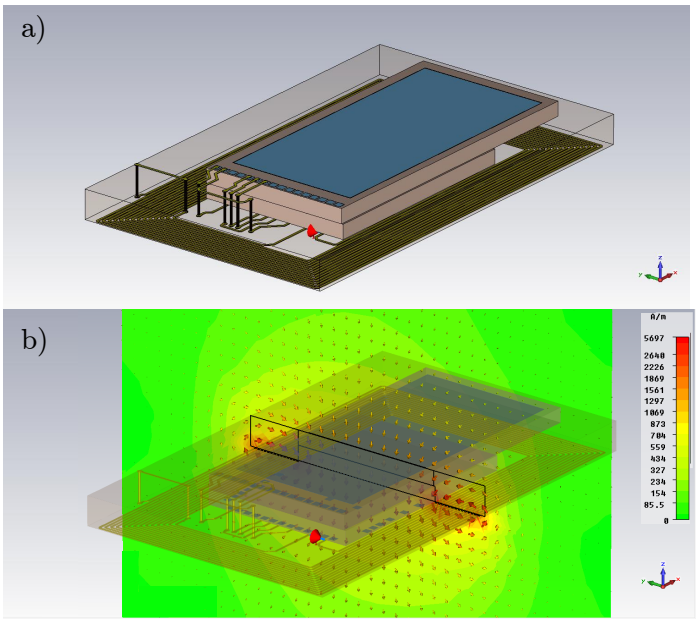


Figure 3.13: a) 3D image of the eWLB SiP b) Electromagnetic simulation with the finite element simulator CST [16]: The magnetic vector field is displayed. We observe that the magnetic field is slightly damped to the top side. At the bottom side the magnetic field is able to propagate unhindered.

fits to the measured $R_A = 34\,\Omega$ @500 kHz. As already mentioned this part of R_A describes the real part losses due to the coil metal. The inductance and the parasitic capacitance of the simulated 19 turn loop antenna is $L_A = 2.33\,\mu$H and $C_A = 2.45\,$pF. These values were verified by measurements, using an appropriate measurement bridge configuration. As it is illustrated in the Smith Chart (see Figure 3.14) the imaginary parts of the simulated coil is zero at the resonance frequency (markers 1, 2 = 13.56 MHz), meaning the antenna design is well matched to the RFID chip capacitance. The measured operation frequency (marker 2) is slightly shifted to the capacitive area due to measurement tolerances. Thus the measured resonance frequency of the produced SiP is 13.43 MHz.

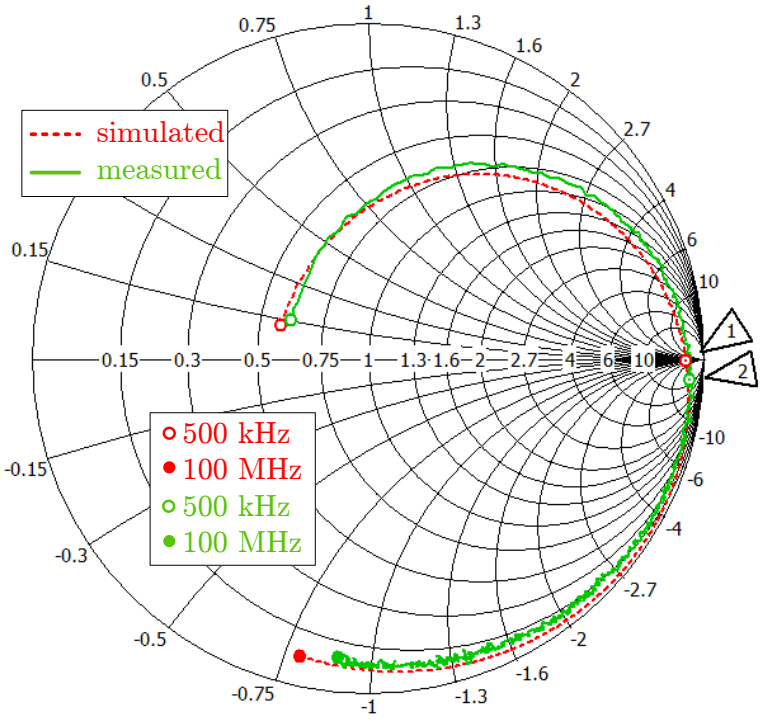


Figure 3.14: Simulated and measured reflection coefficient S11. We observe that the imaginary part of the presented SiP coil antenna is precisely matched to 13.56 MHz (marker 1,2). Note that the Smith chart is normalized to 50 Ω.

Contactless communication measurement

Additionally a contactless measurement setup verified the communication between the SiP tag and the reader. At the reader side a two winding 6 mm x 6 mm coil antenna was connected to the vector network analyzer. This reader antenna has a self-resonance frequency far beyond 13.56 MHz. In order to analyze the influence of the already described

microfluidic card to the SiP antenna, the overall system with this card was tested (see Figure 3.2). Therefore the SiP eWLB was attached to the microfluidic card and moved towards the 6 mm x 6 mm couple antenna. Figure 3.15 shows the measured real part of the reader coil antenna. The maximum of the real part shows the SiP tag resonance frequency that is $f_r = 13.43\,\text{MHz}$. This result shows that the card does not influence the eWLB SiP and the value of the resonance frequency verifies the contact based measurement results of Figure 3.14.

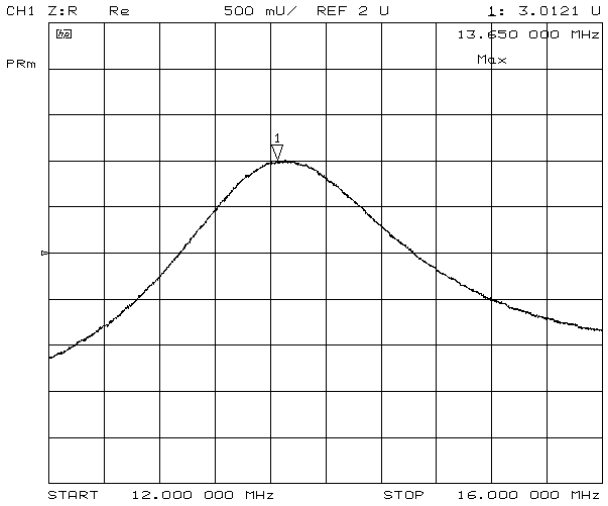


Figure 3.15: Real part of a coupling coil: The resonance frequency of the SiP coil-antenna is $f_r = 13.43\,\text{MHz}$.

Additionally the read range was measured by the use of a similar sized reader antenna (see Figure 3.16). This antenna form is applied three times in the DNA analyze tool that read out and analyzes the micro-fluid card data. The antenna dimension is 7 mm x 5.5 mm. It consist of four windings with a track width of $100\mu m$ and a $100\mu m$ gap between the tracks. A matching network is used to match the impedance to the input-impedance ($\sim 40\Omega$) of the used duali reader device [19]. This 13.56 MHz reader is USB powered. The internal chip driver supports a maximum current of 150 mA @ USB voltage (5 V). As it is common in reader design two drivers are connected but phase-displaced by 90 degrees. With losses in the driver, filters, miss match and material an output power of 1 W can be estimated.

Topology and structure measurement

Indeed the computer tomography, shown in figure 3.9, provides already a lot of information about the structure and the overall topology of the presented SiP. Nevertheless, to analyze the SiP structure even more precisely, a cross section measurement was performed. Therefore the SiP is cut, polished and analyzed with a microscope. Figure 3.17 shows a closer look of the antenna and the environment around the EZL. Both silicon chips are

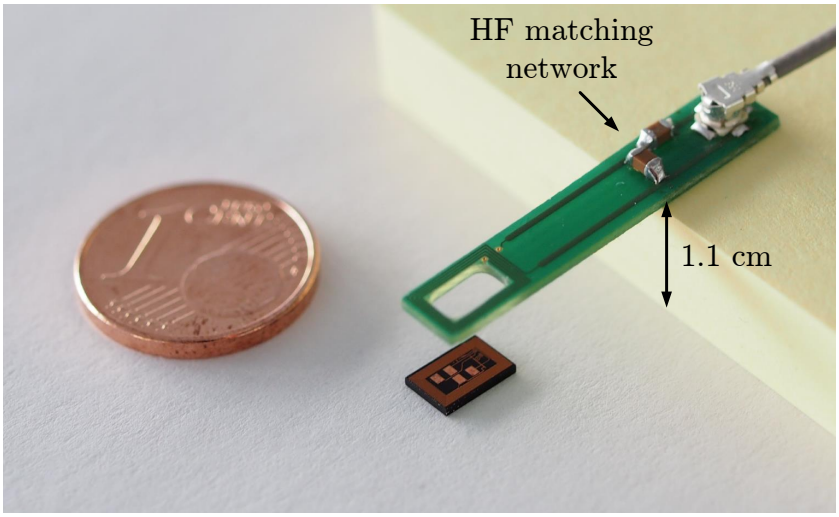


Figure 3.16: Read range measurement setup: A 7 mm x 5.5 mm four winding reader antenna is used to read out the eWLB SiP data. By the use of the duali reader device [19] a maximum read range of 1.1 cm could be achieved.

illustrated. It can be seen that the RDL tracks of the coil are displaced more than one μm from the silicon chips.

3.1.5 Next Generation of Point-Of-Care Applications

Figure 3.18 illustrates a future point-of-care (POC) application. A test substance is analyzed by the eWLB packaged micro lab. The eWLB SiP itself is mounted onto a conventional measurement tape. In contrast to Figure 3.2 this test setup presents an example to use a eWLB 3D SiP autonomously.

Summary and Outlook

The presented 3D SiP based on the eWLB technology provides a model for next generation biochip and micro lab packaging. It is shown that the fan-out area of the eWLB can be perfectly used to attach the sensitive biochip sensor-surface to higher level analytic hardware, such as microfluidic cartridges. Furthermore it is shown that the fan-out area allows outstanding capabilities to realize antennas. A 13.56 MHz coil antenna and an RFID power management chip, enables the presented SiP to work autonomously through the contactless communication interface. Energy as well as data is transferred due to the RFID technology. Due to chip-stacking in the eWLB package, the 3D SiP could be minimized to a volume of only 5.6 mm x 3.6 mm x 0.7 mm. This work demonstrates that the eWLB technology has outstanding capabilities to build complex and innovative

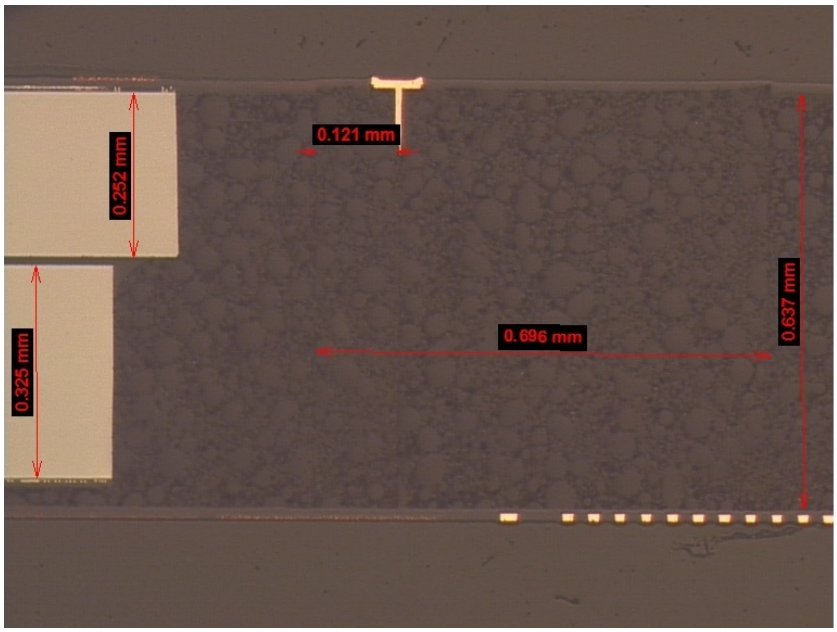


Figure 3.17: Cross section of the presented SiP: Both chips, the EZL and the RDL antenna arranged in the fan-out are illustrated.

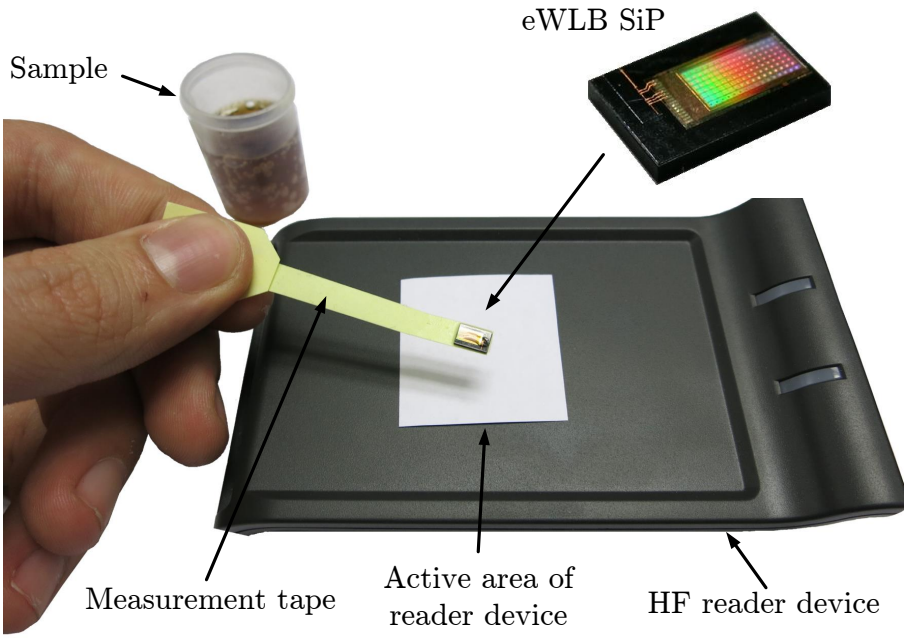


Figure 3.18: Measurement tape and modified reader device. Due to the contactless interface the presented SiP is able to work autonomously.

packaging solutions. To the authors vision the presented biochip 3D SiP packaging concept accelerates the progress in complex POC developments.

3.2 Coil on Chip Tags

This section deals with an innovative coil on chip integration for the Infineon ISO/IEC14443 [50] SLE78-family security micro controller that enables new capabilities and novel applications.

The list of state of the art applications and usages of the Infineon security controller used is long [47]. Typically this type of chip is connected to a large antenna with geometries similar to the specified dimensions of the ISO/IEC 7810 (ID-1, ID-2, ID-3 and ID-000)standard [52]. Within this standard, the geometries and physical characteristics of identification cards are defined. Therefore, one of the core usages of these Infineon security controller lies in government identification, such as ePassport and electronic ID card applications. With regard to [47], target applications lie also in:

- Government Identification
  - ePassports / National eID cards
  - eDriver licenses
  - Social and health care cards
- Authentication and Brand Protection
  - Printer cartridges
  - Mobile phones
  - Music players / Game stations
  - Monitor devices
  - Mobile control units
- Object Identification
- NFC
  - Mobile payment
  - Transport and eTicketing
  - Access control
  - NFC-enabled mobile ID
  - Loyalty programs
  - Device pairing
  - Smart poster reading
  - Peer to Peer information exchange

Indeed, a HF RFID tag miniaturization has become state of the art in many other applications. Products like [66, 73, 108] represent highly integrated RFID solutions with innovative packaging concepts. Often based on the ISO/IEC15693 vicinity standard [51], these transponder solutions seem to be the best way to miniaturize 13.56 MHz RFID tags. However, these state of the art miniaturized 13.56 MHz RFID transponders are equipped with small sized, low power consumption memory RFID tags. Moreover, the packaging concepts used, such as low temperature co-fired ceramic (LTCC) technology, lead to a high manufacture effort (used in [73]). Indeed this technology is well suited for applications such as object identification. Nevertheless, the opportunities for memory transponders and low power state machines are very limited.

Conventional ISO/IEC15693 vicinity RFID tags operate with a magnetic field strength between 5 A/m(rms) and 150 mA/m(rms) [51]. The reading distance used is not specified in the ISO/IEC15693 standard. It mainly depends on the reader structure, the transponder and the geometrical dimensions. Typically the ISO/IEC15693 transponders operate at distances < 150 cm. In contrast to ISO/IEC15693 (vicinity), ISO/IEC14443 [50] proximity RFID systems operate at distances < 10 cm. Within this standard, the power consumption of the RFID transponders is significantly higher than ISO/IEC15693 tags. Thus energy-hungry high-end micro-controller and security elements can be deployed. Furthermore, the ISO/IEC14443 standard operates with higher magnetic field strengths in order to provide the required power transfer. With regard to the standard, the magnetic field strength lies between 1.5 A/m(rms) and 7.5 A/m(rms) [50].

Secure authentication, brand protection applications and many others, do need powerful and high-performance secure elements and micro-controller features. Doubtless geometrical dimensions of such high performance transponders will play a decisive role in future applications.

Due to these facts, this section presents a combination of an Infineon SLE78-family high-end micro-controller and a high Q, double layer, chip scaled antenna using the wafer-level ball grid array (WLB) technology. During the course of this research 33 different antenna designs were developed and fabricated. This large variety makes it possible to take into account future die sizes for secure micro-controllers. Additionally, different antenna forms and geometries are studied and compared in performance and robustness. The chip metals as well as the overall chip structure (silicon and different doped semiconductor layers) are considered in the particular antenna design. Furthermore, as is presented in this section, the WLB technology is pushed to its limits. At the very limits of the RDL electroplating process, a minimum spacing between antenna tracks could be achieved. Thus, coils with a high quality factor and high inductance value could be realized on the small available chip area.

By the use of a fully integrated chip-scaled transponder with the presented coil on chip technology, the list of applications can be extended. Moreover, with regard to the geometrical aspects, the presented high end secure micro-controller with on chip antenna enables new capabilities and novel applications. To the author's knowledge, this

section presents the smallest fully integrated high end secure element transponder in the world.

3.2.1 WLP Packaging Technology

Nowadays, the RDL technology represents an integral part of packaging technologies. Already used within the eWLB packing method, as seen Section 3.1, the RDL is deployed in many other advanced packaging concepts, such as TSV applications, silicon interposers, 3D integration, chip stacking concepts and many more. Originally the RDL was used to connect silicon dies to a printed circuit board or higher level packaging concepts [107]. This concept is called wafer-level packaging (WLP). As the name wafer-level packaging suggests, the redistribution and interconnections are limited to wafer level and therefore to the fan-in area of one chip. Nowadays WLP is widely spread in common chip packaging manufactures, inexpensive and well proven.

As already briefly described in Section 3.1, the redistribution process is an adjustable technology which enables the possibility of antenna design. In contrast to the eWLB process, used in Section 3.1, the antenna design within the WLP concept is limited to the fan-in area of the chip. Therefore chip materials, such as the chip metals, deteriorate the performance of magnetic antennas.

However, as shown in this section, the WLP technology makes chip-scaled transponder solutions possible. Besides fully integrated antennas, this packaging concept leads to the highest possible transponder miniaturization.

In order to achieve a high inductance of the coil antenna, two stacked redistribution layers are used. Figure 3.19 shows the stacked layers and the applied WLP process. It is separated into five manufacturing steps:

- **Application of Dielectric 1:** This dielectric layer is used as a brace layer for the antenna. It has a thickness of $\sim 7\mu m$ and consists of low temperature curing (LTC) imide [107]. Therefore a displacement to the chip can be granted. Holes are designated to realize vias. In contrast to "normal" imide which cures at temperatures around 380°C a LTC imide cures at 240°C. Thus a LTC imide is applicable for temperature sensitive microchips.
- **Application of Redistribution 1:** The first RDL is arranged on the top of the first dielectric layer. Within this layer the first part of the coil antenna is realized. The RDL consists of a copper layer with a thickness of $\sim 3 - 10\mu m$. The RDL thickness is related to the particular antenna design. At this process step the mechanical stress of the wafer is usually low and the surfaces are very planar.
- **Application of Dielectric 2:** The typical WLP technology ends with the second dielectric layer. It covers the redistribution process and protects the RDL, against corrosion for example. For the presented coil on chip development, a second RDL is used. Therefore a second dielectric LTC imide, with a thickness of $\sim 7\mu m$, is

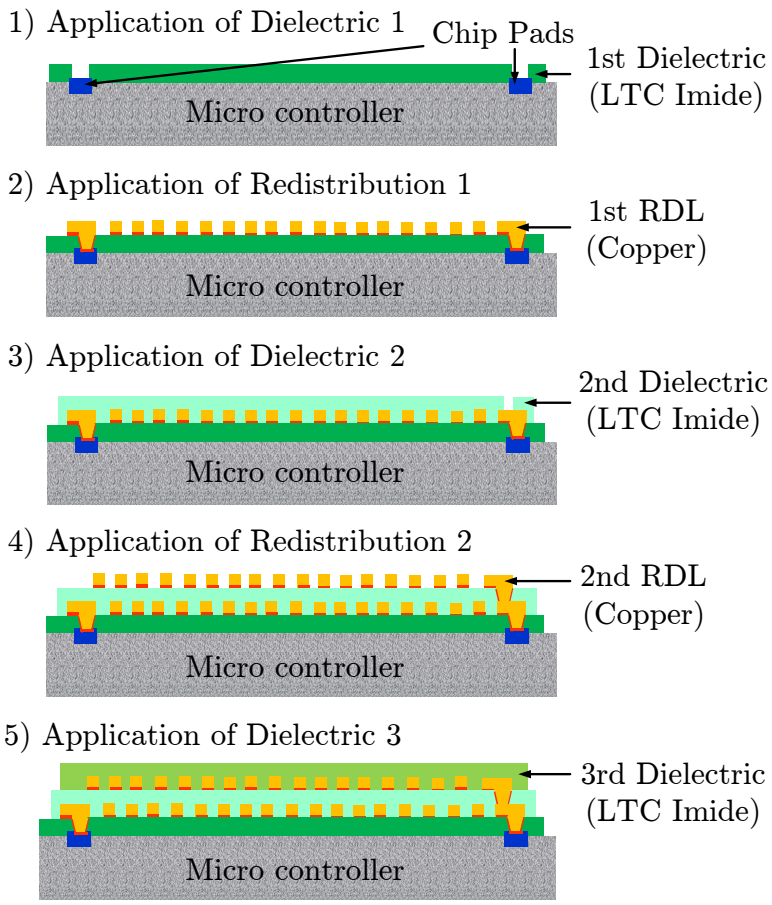


Figure 3.19: Five manufacture steps of the presented double layer coil on chip technology: Three dielectric and two redistribution layers are used to produce a high inductance coil on the top of the Infineon security micro controller. After the illustrated process and dicing the produced RFID transponder is ready to use.

deployed as carrier and spacer for an additional RDL. Due to the first RDL, the surface is not planar anymore. Thus the mechanical stress is increased.

- **Application of Redistribution 2:** Each coil needs a underpass. In Section 3.1 the underpass was realized with a second RDL on the opposite side of the structure. Thus only one redistribution layer on each side is needed. With a second, stacked RDL the underpass can be realized within the coil on chip development. Moreover the inductance of the coil can be increased significantly using the second RDL as an additional part of the coil. Due to the non-planar surface of the second dielectric layer, the second RDL process characteristics and geometrical dimensions, e.g. the gap between coil tracks, are very limited. Again the thickness of the RDL copper layer lies between ~ 3 and $10\mu m$.

- **Application of Dielectric 3:** The last dielectric layer (LTC Imide $\sim 7\mu m$) is used for encapsulating the overall miniaturized transponder. It protects the antenna against mechanical forces and prevents corrosion of the top copper RDL.
- **Additional packaging steps:** Similar to the eWLB process, used in Section 3.1, the ball grid applied for external connections is simply skipped. Therefore the WLP process used ends with the last dielectric layer.

3.2.2 Design and Simulations

Due to the WLP technology, the size of the antenna is limited to the fan-in area of the security micro-controller. Although the chip is produced in a 90 nm technology, the size of the chip is 2.1 mm x 2.1 mm. The reason for such large chip dimensions are the high end features of the used controller. Large memory banks, secure elements and the controller logic require large digital parts and therefore a large chip area. Furthermore, the analog part supports different communication interfaces. A contact based ISO 7816 [53] interface as well as the contactless interface ISO 14443 [50] is provided by the used SLE78-family micro-controller chip. These interfaces, interconnection pads, band gaps, different power supply regulators and many more analog parts require additional chip area. However, as is shown in this section, the performance of an autonomous RFID transponder equipped with the presented coil on chip technology benefits from larger chip dimensions.

Within the coil on chip design, the antenna is arranged at the fan-in area of the security micro-controller. Therefore the chip itself has a significant influence on the antenna design. The controller as well as the chip structure have to be analyzed in order to locate disturbing chip metals and conductive material. After analyzing and collecting all required material constants the RFID antenna design is realized by means of the electromagnetic field simulator FEM in Advanced Design System [2].

Chip Structure Influence

As a first step, the chip structure and chip metals have to be analyzed to provide material constants for further simulations. Figure 3.20 illustrates the chip layout of a typical ISO 14443 [50] capable Infineon RFID test chip. Note that, due to disclosure policies, the security related chip layout of the Infineon micro-controller used cannot be provided at this point. As can be seen in Figure 3.20, the layout consists of several metal layers that are interconnected tightly. Furthermore, the metallic wires and interconnections are arranged very close to each other. Nevertheless, there are no large solid metal surfaces that cover the complete layout. Thus, the design of a coil on chip RFID tag is feasible. The layout and its chip metals can be seen as a fragmented metallic sheet that still causes eddy currents. Especially at higher frequencies $>$ 13.56 MHz, this

fragmented sheet must not be neglected. Certainly it has to be considered in the antenna design.

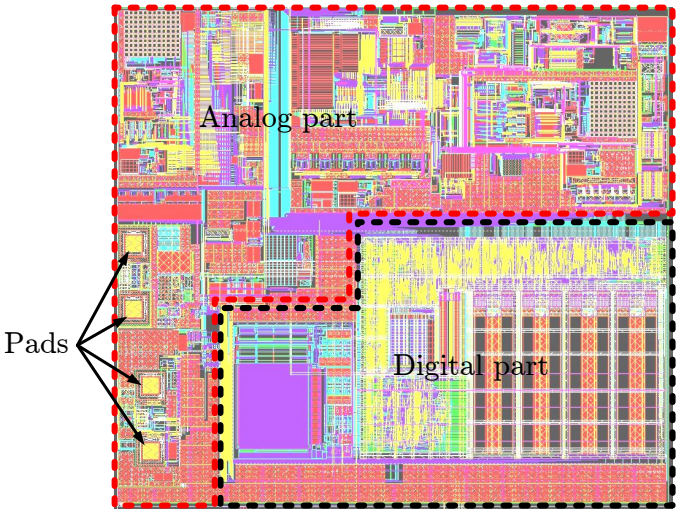


Figure 3.20: A typical RFID chip layout: The layout mainly consists of a digital part, an analog part and connection pads. An RFID antenna on the top of such chips is influenced by the layout. Chip metals, conductive layers as well as the substrate deteriorate the antenna performance. Therefore the layout has to be considered within the RFID tag design.

Nowadays it is not possible to simulate a coil on chip antenna in combination with such a complex chip layout. The number of necessary mesh cells would exceed the conventional computing power. In the following a method is introduced which makes it possible to estimate an equivalent solid metal plate. Then this plate can be used to replace the particular chip layout during the coil on chip simulation.

The plate can be seen as a good conductive resistor that is inductively coupled to a particular coil that is arranged close to the plate. To measure this resistance value, two sensing coils are fabricated. Figure 3.21 illustrates the layout of these coils. The diameter of the two and three winding coils is smaller than the chip size. Thus, if the chip is arranged on the top of one coil, it is able to cover all coil tracks. The track as well as the gap between the tracks, is 0.1 mm. Both coils are produced on FR4 with a thickness of 0.3 mm.

The measurement setup is illustrated in Figure 3.22. A Network Analyzer (ZVL from Rohde&Schwarz) [87] is connected to one sensing coil. As can be seen, a parallel capacitor is connected on the backside of the coil. Due to the capacitor, a parallel resonating circuit is realized. With this setup two measurements were performed: a) A real part measurement with the chip on the top of the sensing coil. b) A real part measurement without the chip. The chip is arranged upside down, thus the chip metals cover all coil

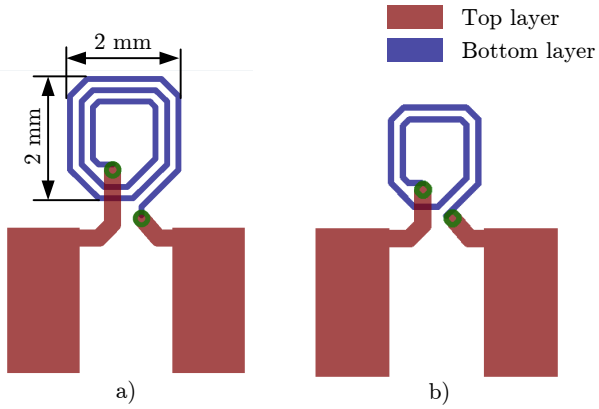


Figure 3.21: Layout of two sensing coils to measure the equivalent sheet resistance of a chip. The size of the coils (2 mm x 2 mm) is smaller than the chip dimensions (2.1 mm x 2.1 mm) in order to measure the chip influence.

tracks. Only the green lacquer ($\sim 10\,\mu$m) of the FR4 board separates the coil from the chip metals. An equivalent circuit of both measurements is illustrated in Figure 3.23. The figure is separated into two columns. In the first row the measurement setup is illustrated schematically. The second row represents the corresponding equivalent circuit. As can be seen, the chip is represented by a resistor R_{Plate} that is inductively coupled to the sensing coil $L_{Senscoil}$. The resistive losses of the sensing coil are given by $R_{Senscoil}$. As already mentioned, the capacitor C_{Res} generates a resonating circuit. The third row of Figure 3.23 shows the parallel equivalent circuit of the measurement setup. In case of resonance, the equivalent capacitor C_P and inductor L_P cancel each other. Thus, just the resistance R_P remains. This equivalent circuit is also true in case of the inductively coupled chip structure. In case of resonance the parallel equivalent capacitor C_{P2} and inductor L_{P2}, which include all inductive and capacitive parts of the inductive coupled equivalent circuit above, cancel each other. In this case the remaining resistor can be seen as a parallel circuit of R_P and R'_{Plate}. By measuring the value of R_P as well as the value of $R_P||R'_{Plate}$, the resistor R'_{Plate} can be calculated by:

$$R'_{\mathrm{Plate}} = \frac{R_{\mathrm{P}} \cdot R_{\mathrm{R_P||R'_{Plate}}}}{R_{\mathrm{P}} - R_{\mathrm{R_P||R'_{Plate}}}} \tag{3.2.1}$$

In the presented chip structure influence measuring method, the chip and its metals are seen as a perfect, inductively coupled, one winding inductor with an resistance of R_{Plate}. Thus eddy currents and resistive losses can be estimated. R_{Plate} can be calculated by using the well known transformer formula:

$$\frac{Z_1}{Z_2} \approx \frac{U_1}{U_2} \cdot \frac{I_1}{I_2} \tag{3.2.2}$$

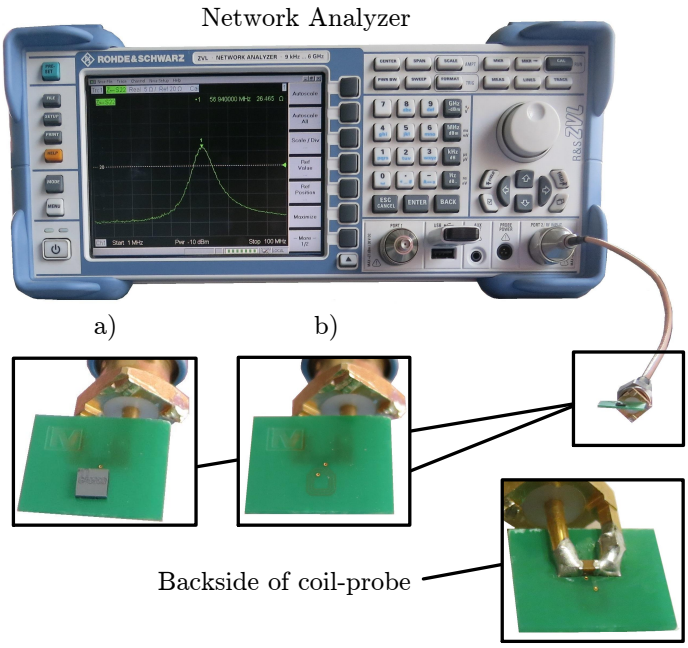


Figure 3.22: Measurement setup to measure the influence of the chip structure used. The real part of a 2 mm x 2 mm three winding coil is measured in two steps: a) in combination with the chip; b) without the chip. The three winding coil is equipped with an additional parallel capacitor (backside of the FR4). At the resonating frequency the real part peak value is measured.

$$\frac{N_1}{N_2} \approx \sqrt{\frac{Z_1}{Z_2}} \tag{3.2.3}$$

By using the three winding sensing coil ($Senscoilwindings = 3$), R_{Plate} can be calculated with following formula :

$$R_{\mathrm{Plate}} \approx \frac{R'_{\mathrm{Plate}}}{Senscoilwindings^2} \tag{3.2.4}$$

To verify the presented measurement method, two different sensing coil types (shown in Figure 3.21) and three different resonating circuits were used. The values of each component can be found in table 3.1. As is illustrated in Figure 3.22, both measurements were performed with each sensing coil setup. Figure 3.24 shows the first real part measurement. As can be seen, the peak value of the real part at the resonating frequency of 25.1 MHz is 15 Ω. When the chip is arranged on the top of the coil (see Figure 3.22), the resonating circuit is damped to 13.1 Ω. Within this measurement an equivalent inductively coupled resistor $R'_{Plate} = 105\,\Omega$ can be calculated by the use of formula 3.2.1. This resistor represents the resistance of a fictive inductively coupled mirrored coil (three windings) in the disturbing chip structure. To calculate the equivalent resistance value of

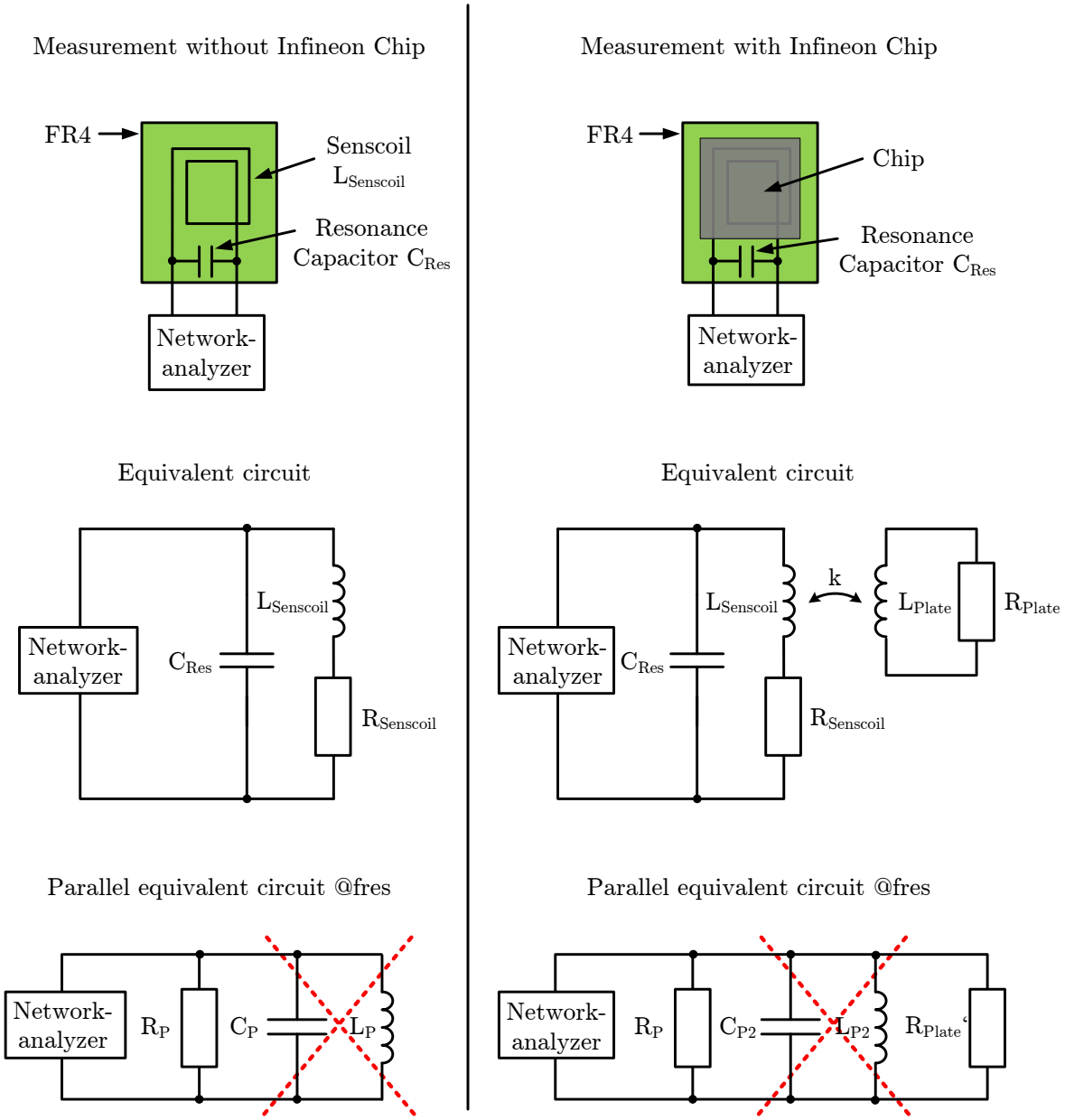


Figure 3.23: Influence measurements: When the chip is arranged on the top of the sensing coil, the real part of the overall circuit is measured. At the resonating frequency the capacitor C_P and inductor L_P cancel each other. Therefore the values of the resistor R_P as well as $R_P||R'_{plate}$ remains. Due to this real part measurement of these resistors, the metal resistance R_{Plate} can be calculated.

a fictive one winding coil, formula 3.2.4 is used. Therefore a resistor $R_{Plate} \approx 12\,\Omega$ can be determined. To verify the result, the measurements were repeated with the second and third sensing coil setup. Figure 3.25 and Figure 3.26 shows the real part measurements of the particular setup. Again the values of $R_{\mathrm{P}} = 36.5\,\Omega$ and $R_{\mathrm{R_P}||\mathrm{R'_{Plate}}} = 27.4\,\Omega$ lead to the equivalent chip structure resistance of $R_{Plate} \approx 12\,\Omega$ (Figure 3.25). This result is also verified by using the two winding sensing coil setup (Figure 3.26): The values $R_{\mathrm{P}} = 4.28\,\Omega$ and $R_{\mathrm{R_P}||\mathrm{R'_{Plate}}} = 3.95\,\Omega$ lead to $R_{Plate} \approx 12\,\Omega$. Within this measurement process all component values for the equivalent circuits, shown in Figure 3.23, were determined.

	$L_{Senscoil}$	$R_{Senscoil}$	C_{Res}
1st sensing coil setup: Three winding coil	20 nH	0.55 Ω	2200 pF
2nd sensing coil setup: Three winding coil	20 nH	0.55 Ω	390 pF
3rd sensing coil setup: Two winding coil	11.6 nH	0.34 Ω	8200 pF

Table 3.1: Three resonating sensing coil setups

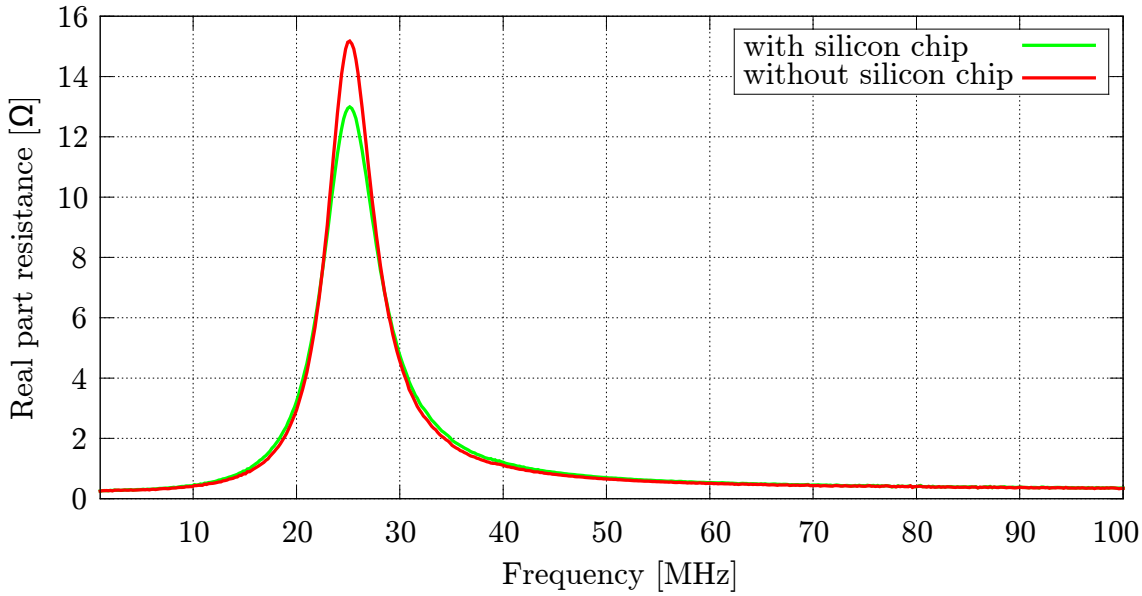


Figure 3.24: Real part measurement of the chip influence: The real part peak value is 15 Ω without the chip. When the chip is mounted on the top of the first sensing coil setup, the resonating circuit is damped to 13.1 Ω peak value.

Within the presented method the sheet resistance ($\Omega/square$) of an equivalent fragmented metal plate, generated by the chip structure/layout, can be determined. Therefore the previous measurement results and equivalent circuits are used in FEM-simulations. Figure 3.27 illustrates the 3D view of the simulated measurement setup. As can be seen, an equivalent metal sheet with a thickness of one μm is used to represent the chip structure

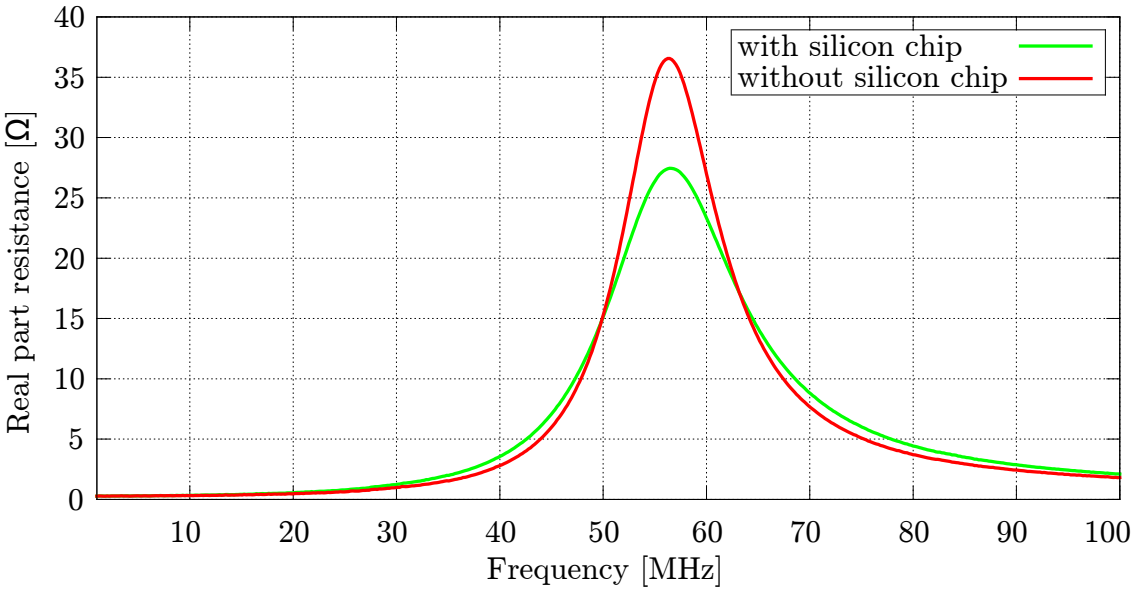


Figure 3.25: Real part measurement of the chip influence: The real part peak value is 36.5 Ω without the chip. When the chip is mounted on the top of the second sensing coil setup, the resonating circuit is damped to 27.4 Ω peak value.

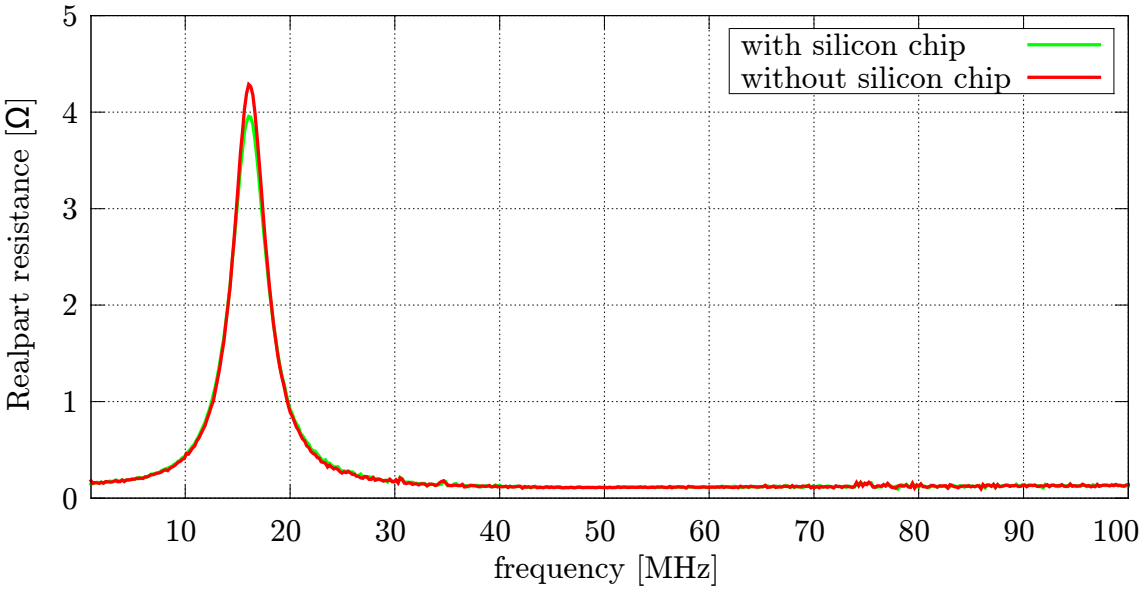


Figure 3.26: Real part measurement of the chip influence: The real part peak value is 4.28 Ω without the chip. When the chip is mounted on to the top of the third sensing coil setup, the resonating circuit is damped to 3.95 Ω peak value.

influence. The left picture of Figure 3.27 shows the magnetic field inside this plate, while the right picture illustrates the magnetic field profile of the overall system. 170k mesh cells (see Figure 3.28) are used for the presented simulations. In order to match the measured Z-parameter, the conductivity of the one μm metal plate was varied. This parametric sweep made it possible to determine a conductivity of 0.1 MS/m. Thus a sheet resistance of 10 Ω/square can be calculated. Figure 3.29 shows this fitted Z-parameter of simulation and measurement results. As already described, the measured Z-parameters of the coil are damped by the metal chip structure. This effect can be also realized with an equivalent metal plate with a sheet resistance of 10 Ω/square. Figure 3.30 visualizes the damping effects of a one μm pure copper plate. As can be seen, this good conductivity of 47 MS/m leads to a significant damping. In this case, the copper sheet resistance can be calculated to 0.02 Ω/square.

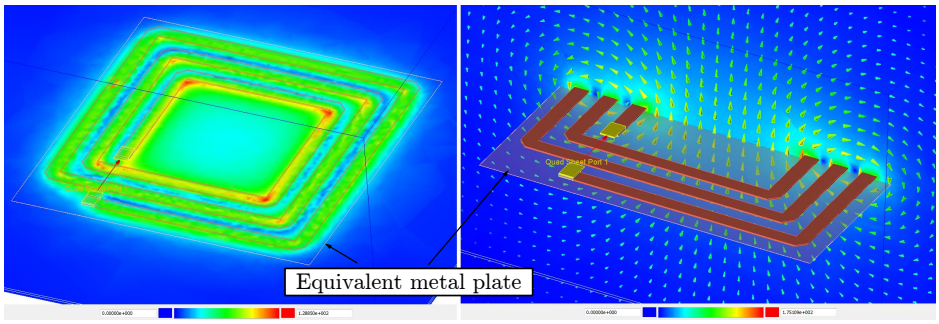


Figure 3.27: FEM simulation to determine the sheet resistance ($\Omega/square$) of an equivalent fragmented metal plate. Left picture: the magnetic field inside the equivalent metal plate (causing eddy currents). Right: overall magnetic field profile of the measurement coil in and the determined equivalent metal plate.

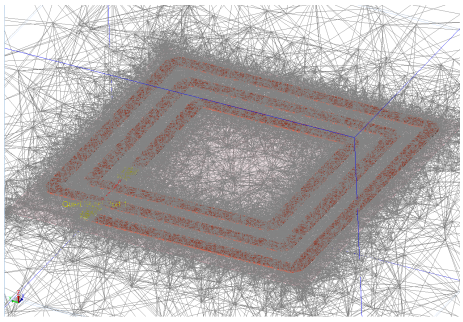


Figure 3.28: Mesh cells of simulated measurement setup. In order to provide precise simulations and to mesh the one μm equivalent metal plate, the meshing is defined to 170k cells.

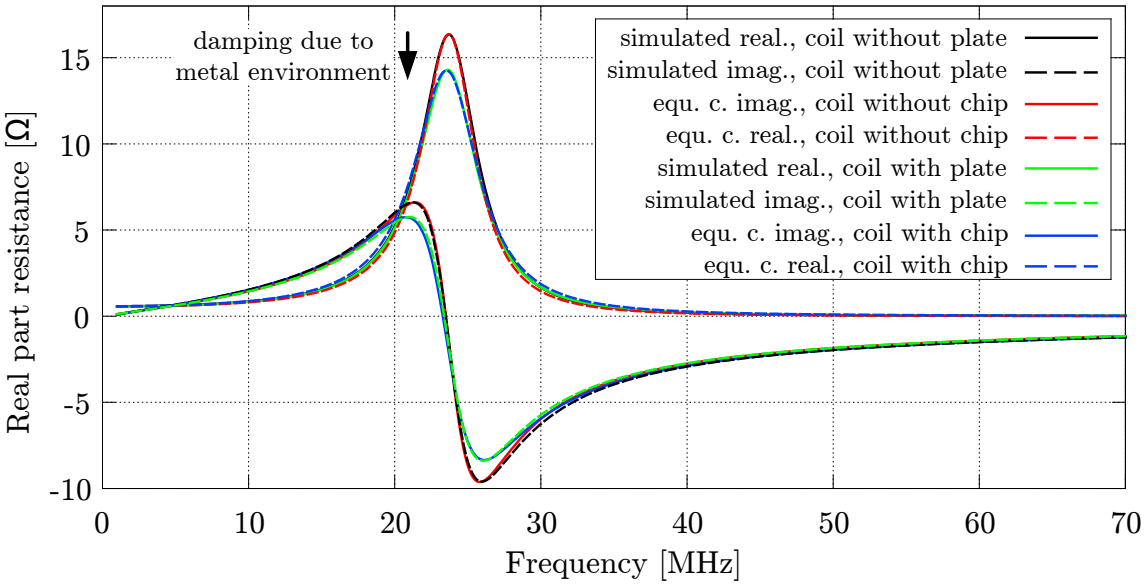


Figure 3.29: Simulation of the equivalent metal plate conductivity. The metal conductivity value sweep allows a fitting of the simulated Z-parameters to the measured values. Therefore a sheet resistance of 10 Ω/square was determined.

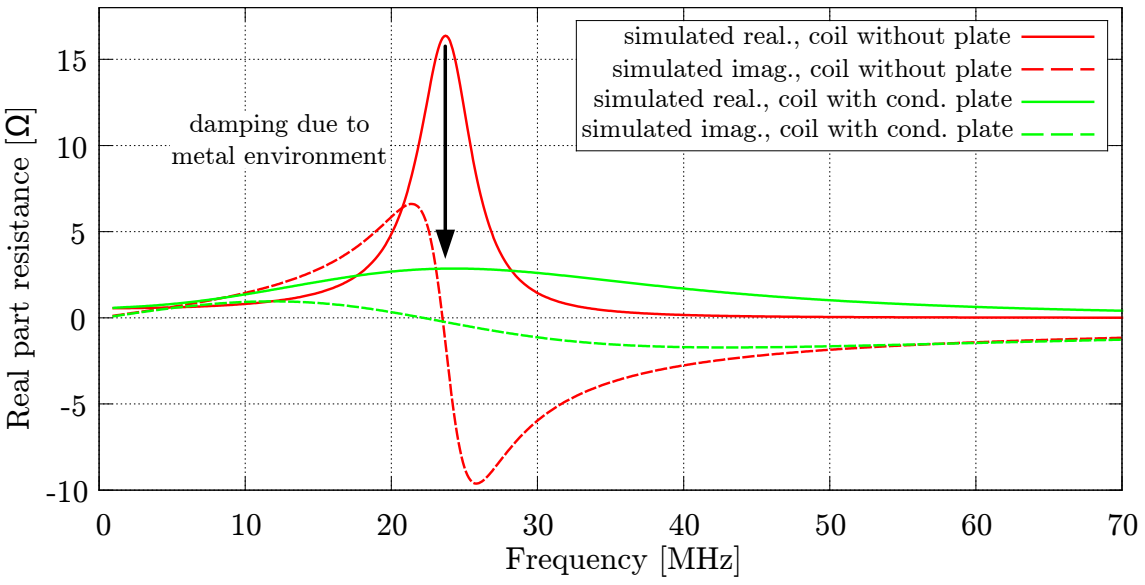


Figure 3.30: Simulation with decreased sheet resistance. In case of a plate conductivity similar to copper (47 MS/m) the Z-parameters are damped significantly.

Coil on Chip design

During this research, 33 antenna designs were developed and fabricated. This large variety makes it possible to take into account future die sizes and novel antenna geometries. Tables 3.2 and 3.3 list all simulated and fabricated antenna designs. As is illustrated, the antennas are categorized into the classes: "20u20u flute", "Pads for capacitor", "Broad lines", "ISO pads reachable", "Small spacing" and "With hole".

20u20u flute	Pads for capacitor	Broad lines	ISO pads reachable
20u20u15W	Kap20u20u0402	30u20u16W	Pf20u20u17W
20u20u16W	Kap20u20u2L	30u20u18W	Pf20u20u19W
20u20u17W	Kap20u20uV2	40u20u16W	Pf20u20u22W
20u20u18W	Kap40u20u0402	Kap40u20u1L	Kl20201000u
20u20u20W	Kap40u20uV3	Kap40u20u2L	Kl20201500u
20u20u24W	myDmove20u20u	Kap50u20u2L	Kl2020MyNFC

Table 3.2: Coil on Chip Variants

Small spacing	With hole
20u10u1L	Loch20u20u
20u08u1L	Loch40u20u
20u15u1L	Loch50u20u
20u15u1LV2	
20u20u1L	
20u20u1LV2	

Table 3.3: Coil on Chip Variants

- **20u20u flute:** "20u20u" stands for 20 μm track with and 20 μm gap between the tracks of the RFID antenna/coil. This category is designed to avoid process deviations and design errors. Therefore the number of windings are varied around the golden design, namely "20u20u17W". The particular numbers "15W", "16W", "17W" etc. represent the number of the windings used at one layer. Excluding the category "Small spacing", each antenna is designed with the already described double layer RDL technology. Thus the antenna design "20u20u17W" consists of 34 windings.
- **Pads for capacitor:** This antenna type provides pads to connect an additional parallel capacitor. By reducing the number of windings, the coil inductance decreases significantly. As a matter of fact, the resonating frequency of the transponder

system increases. In order to operate at 13.56 MHz an additional parallel capacitor is needed.

- **Broad lines:** As the name "broad lines" suggests, the track with of the particular coil design is varied. Again, the caption "30u20u" or "40u20u" describes track with and spacing. Due to the decreased resistance of the coil, this category is able to achieve high quality factors.
- **ISO pads reachable** Beside the contactless interface ISO 14443 [50] the Infineon SLE78-family micro-controller used supports the contact-based ISO 7816 [53] interface. This category makes it possible to take into account a dual interface communication. Therefore the coil on chip is designed to provide space for ISO 7816 interconnections.
- **Small spacing** The "Small spacing" category pushes the WLP technology to its limits. This coil consists of 20 μm track with and less than 10 μm spacing. Therefore captions such as "20u10u" are used. Note that the sign "08" represents a further decreased spacing (8 μm).
- **With hole** Within this category the dielectric layers of the WLP technology used are omitted in the middle of the antenna design. The resulting hole makes it possible to arrange ferrite material in the middle of the coil. Due to this method, the inductance can be increased.

In the following the simulation and design process of the antenna "20u20u17W" is presented. This type is part of the 20u20u flute category. The layouts of all six variants of this category are illustrated in Table 3.2.2. As already described, the name "20u20u" stands for 20 μm track width and 20 μm spacing. The size of all 20u20u designs is 2.1 mm x 2.1 mm. The particular layout and design, of all other antennas and categories can be found in the appendix A.1.

20u20u17W Coil on Chip simulation

The antenna design was done by means of the electromagnetic field simulator ADS (Advanced Design System [2]). Therefore the already described RDL technology was used to generate an ADS substrate stack. This stack is illustrated in figure 3.31. As can be seen, no reference ground plane or covers are used. The stack consists of the silicon chip (500 μm silicon) plus *one* μm equivalent metal plate, namely "Mplate". On the top of the metal plate the described RDL technology is applied: Two redistribution layers which are separated by the WLP dielectric substrate. Finally, a WLP dielectric substrate encapsulates the overall RDL antenna. For simulation, one RDL via is used to connect both redistribution layers. Indeed another two RDL vias are needed to connect the RDL antenna to the chip metals (Mplate). Nevertheless these vias can be neglected in the presented simulation layout.

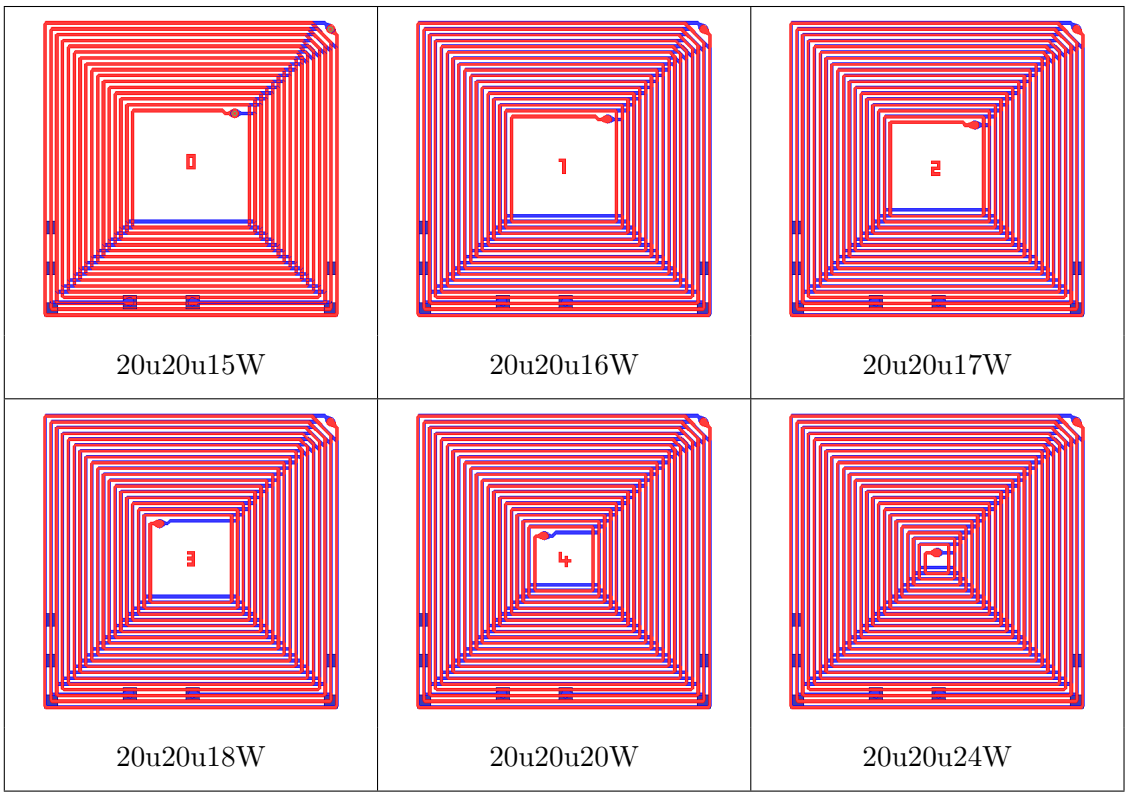


Table 3.4: 20u20u Flute category: The number of windings are varied around the golden design, namely "20u20u17W", to avoid process deviations and design errors. All variants are simulated, produced, measured and analyzed.

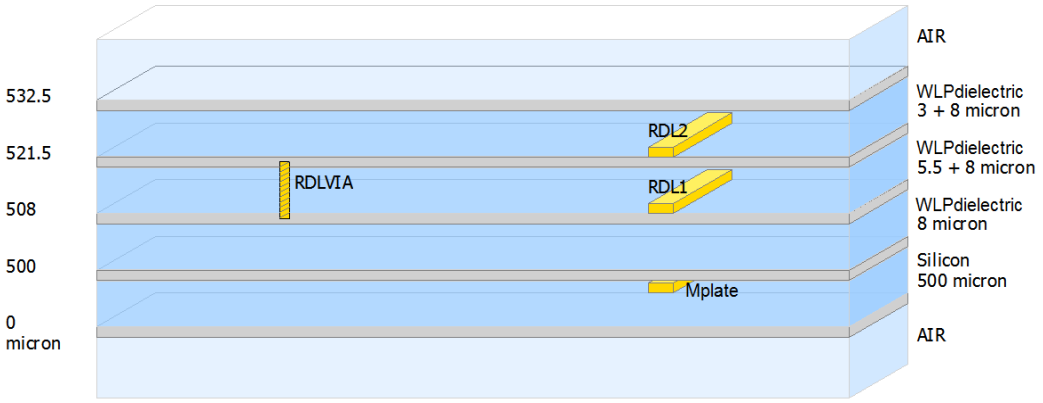


Figure 3.31: ADS substrate stack used: A 500 μm thick silicon substrate and the already described *one* μm equivalent metal plate with a conductivity of 0.1 MS/m represent the silicon chip used. Three WLP dielectrics and two redistribution layers, RDL1 and RDL2, represent the WLP technology used. RDL1 as well as RDL2 are used to design the coil on chip structure.

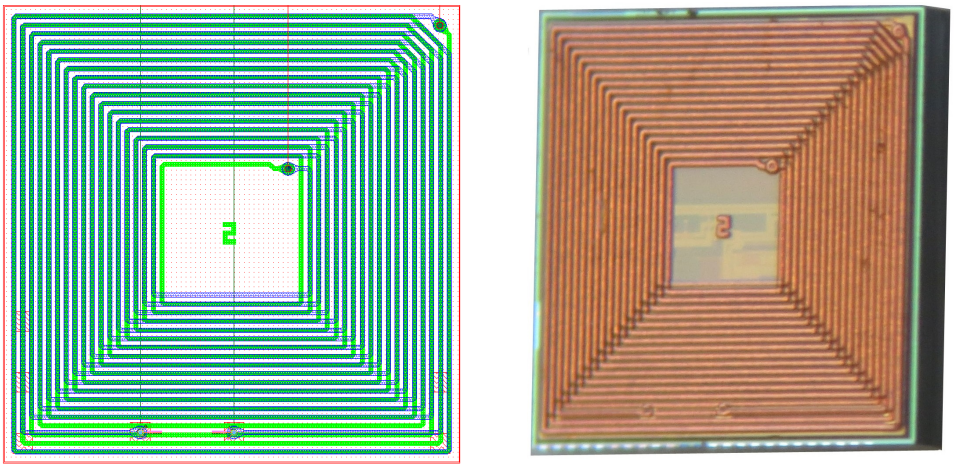


Figure 3.32: Left picture: Layout of the "20u20u17W" design in ADS. The redistribution layer RDL1 (blue) and RDL2 (green) is used to design the 34 winding coil. Two vias (black) are needed to connect both redistribution layers. The equivalent metal plate (red) is arranged below the coil, as it is shown in 3.31. Right picture: produced RFID transponder.

A detailed layout as well as the produced 20u20u17W transponder is illustrated in figure 3.32. As can be seen, both redistribution layers (green and blue) are arranged above the red equivalent metal plate. As already described, this 2.1 mm x 2.1 mm large metal plate represents all chip metals. For simulation, a 50 Ω differential port is connected to the lower (blue) redistribution layer.

The magnetic field simulation, shown in figure 3.33, illustrates the propagated H-field. Within this simulation it can be seen that the H-field is slightly damped by the equivalent metal plate. Nevertheless a propagation and thus an RFID communication is still feasible. The field strength is concentrated in the middle of the structure. This kind of simulation already gives a short overview about the limited read range of the presented CoC transponder system. As is described in [25], the magnetic field strength decreases by distance. For such rectangular loop antennas the magnetic field strength can be also calculated with:

$$H = \frac{N \cdot I \cdot a \cdot b}{4\pi \cdot \sqrt{(\frac{a}{2})^2 + (\frac{b}{2})^2 + x^2}} \cdot \left(\frac{1}{(\frac{a}{2})^2 + x^2} + \frac{1}{(\frac{b}{2})^2 + x^2}\right) \tag{3.2.5}$$

The magnetic field caused in the center of the antenna is directly proportional to the current I and the number of windings N. The parameter x represents the distance to the antenna in vertical z-direction. By increasing the distance, the field strength is reduced. The geometrical values of the antenna are given by the parameters coil length a and the coil with b. Note that this formula is only valid for distances (x) smaller than $\lambda/2\pi$.

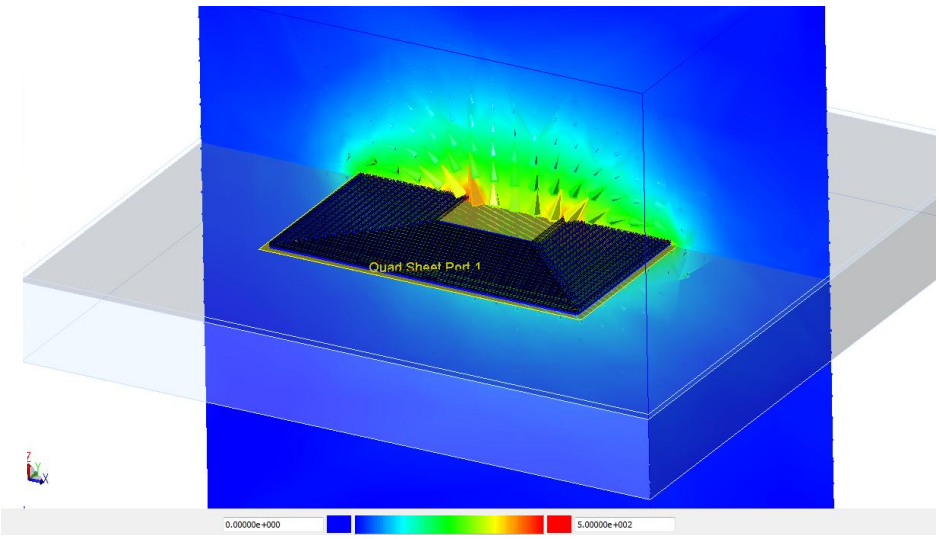


Figure 3.33: Magnetic field simulation of the presented coil on chip design. Due to the equivalent metal plate (yellow) the field is slightly damped to the bottom. Nevertheless a propagation is possible. The field simulation already gives a short overview of the limited read range of such miniaturized 2.1 mm x 2.1 mm coils.

With distances larger than $\lambda/2\pi$ there is the continuous transition from the near field into the electromagnetic wave propagating far field.

As expected, the simulation of the 20u20u17W antenna shows damped inductor behavior. The real part as well as the imaginary part of the stacked coil antenna are illustrated in figure 3.34 and 3.35. It can be seen that the resonating frequency of the 20u20u17W coil on chip antenna is 58 MHz. At the resonating frequency the imaginary part is zero while the real part has a maximum. The result of 58 MHz signifies a relatively large parasitic capacitance of the stand alone antenna. To extract standard RLC values an equivalent circuit is fitted to the simulation results. Due to the disturbing metal environment a standard coil equivalent circuit cannot be used anymore. Therefore an ADS optimization tool was used to fit the proposed equivalent circuit shown in figure 3.36. As is illustrated in 3.42 and 3.35, the proposed equivalent circuit fits well and provides the RLC values. It can be seen that the parasitic capacitance has a relatively large value of 4.1 pF. This is mainly caused by the stacked layout of the coil antenna. Moreover, the capacitance is given by the equivalent metal plate that is arranged below the antenna.

There are three types of the high security SLE78xx RFID chipcard controller used available. Each type has a different input capacitance: 27 pF, 56 pF and 78 pF. In order to resonate at the operating frequency of 13.56 MHz an adequate antenna design is necessary. The larger the antenna inductance, the smaller the chip capacitance and vice versa. Usually, ID1 cards with class 1 antennas [52] are used to operate with the type one (27 pF) chip card controller. In order to operate with very small and low inductive

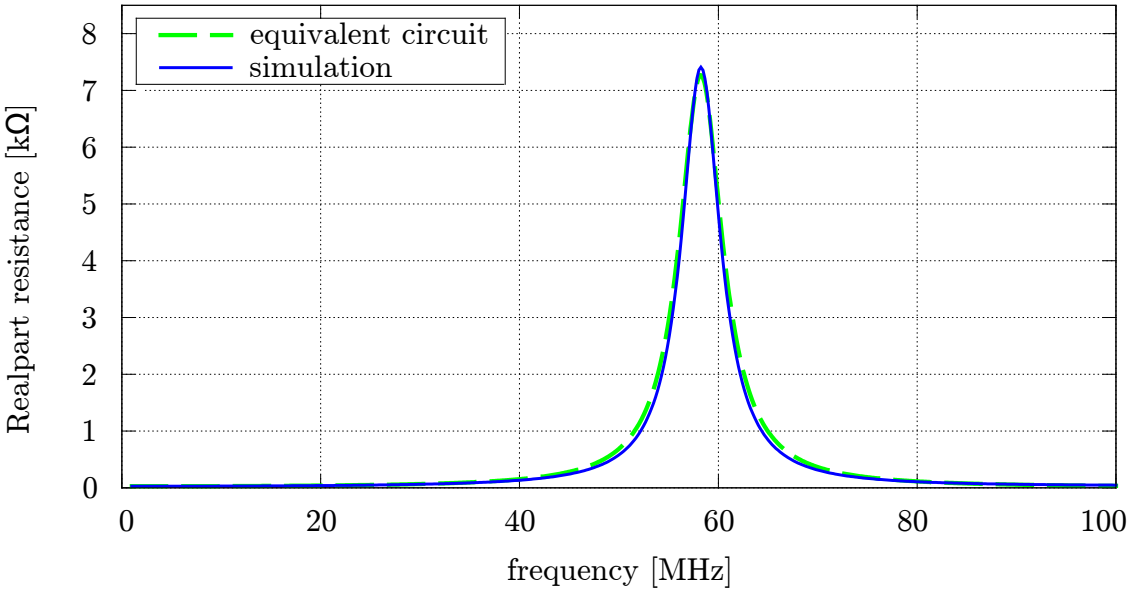


Figure 3.34: Real part simulation of the 20u20u17W coil on chip design. An equivalent circuit, shown in 3.36, is used to fit the simulation results.

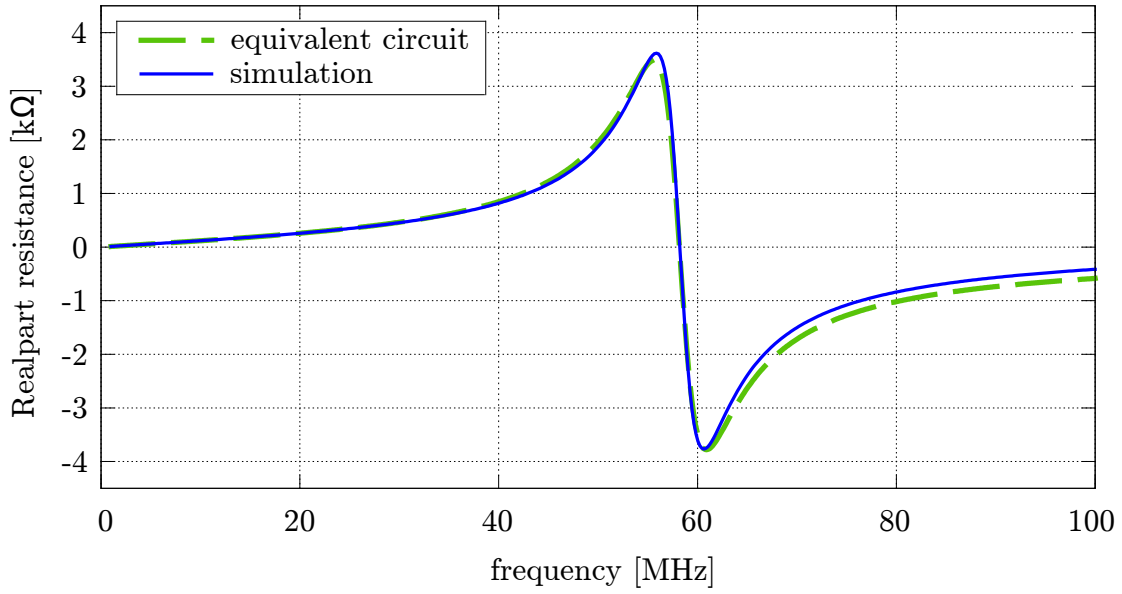


Figure 3.35: Imaginary part simulation of the 20u20u17W coil on chip design. An equivalent circuit, shown in 3.36, is used to fit the simulation results.

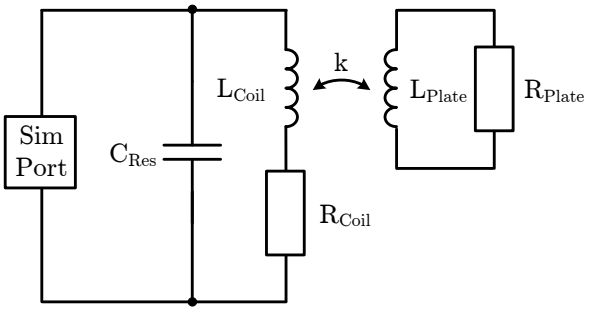


Figure 3.36: Equivalent circuit of the presented 20u20u17W coil on chip design. The coil, realized with two redistribution layers, consists of an inductor $L_{Coil} = 1.8\,\mu$H and the resistor $R_{Coil} = 27.5\,\Omega$. A parallel parasitic capacitor is represented by $C_{Coil} = 4.1\,$pF. The circuit is damped by the metallic structures of the chip. Similar to the first measurement setup shown in figure 3.23 an equivalent metal plate is represented by $L_{Plate} = 20\,$nH and $R_{Plate} = 15\,\Omega$. The coupling coefficient k is estimated to 0.95.

coils, such as such as Class 4, 5 or 6 antennas [52], type 3 is used. A co-simulation in ADS, using the presented 20u20u17W coil on chip antenna model in combination with a parallel capacitor of 78 pF, shows that the presented antenna design is well suited to operate in combination with the type three SLE78xx high security chip card controller.

3.2.3 Realization

As already described, 33 different antenna designs were developed. This large variety makes it possible to take into account future die sizes and novel antenna geometries. Furthermore, each antenna type consists of two different layouts. One design is directly connected to the chipcard controller with two RDL vias. In addition, this design is totally encapsulated with WLP dielectric. The second design represents the particular measurement structure. In contrast to the full functional coil on chip design the measurement structure is not connected to the chip. Moreover, it provides small pads to measure the particular coil impedance with an wafer prober. Therefore one WLP-reticle was realized with 66 different antenna layouts (33 different antenna designs plus 33 measurement structures). An eight inch mono-reticle chip card controller wafer was used for the WLP process. A picture of the wafer after the WLP process is illustrated in figure 3.37. The wafer consists of more than 5000 high security controller chips. It provides space for 73 full WLP-reticles. As already mentioned, each WLP reticle consists of 66 different antenna designs. Therefore one wafer provides at least 73 chips from one design. A closer look to the 66 different designs of one WLP-reticle is given by figure 3.38. As can be seen, the wafer is diced and ready to use. In the middle of the reticle the 20u20u17W chip is highlighted.

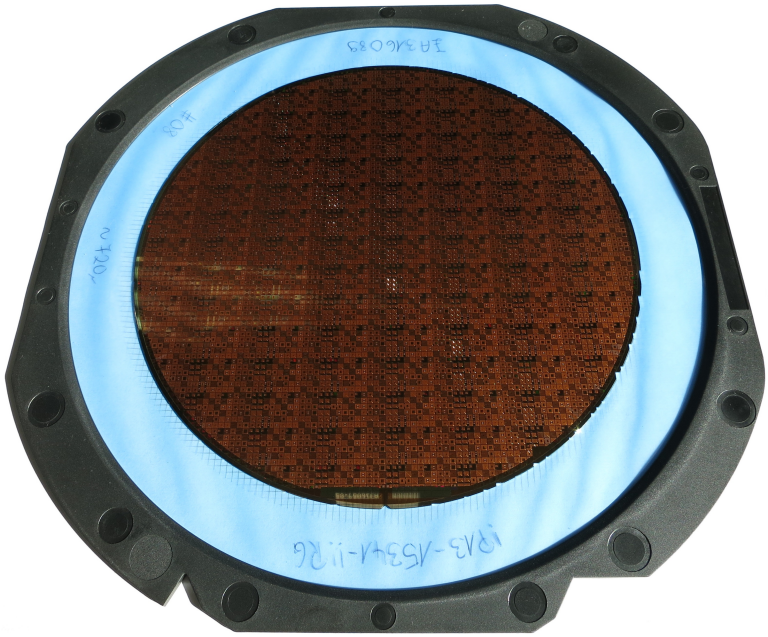


Figure 3.37: Mono reticle wafer after WLP process. The so called "eight inch" wafer (diameter = 200 mm) comprises 73 full reticles. Nevertheless, some chips in reticles near the boarder can also be used. All in all, one wafer contains more than 5000 high security controllers equipped with the presented coil on chip technology.

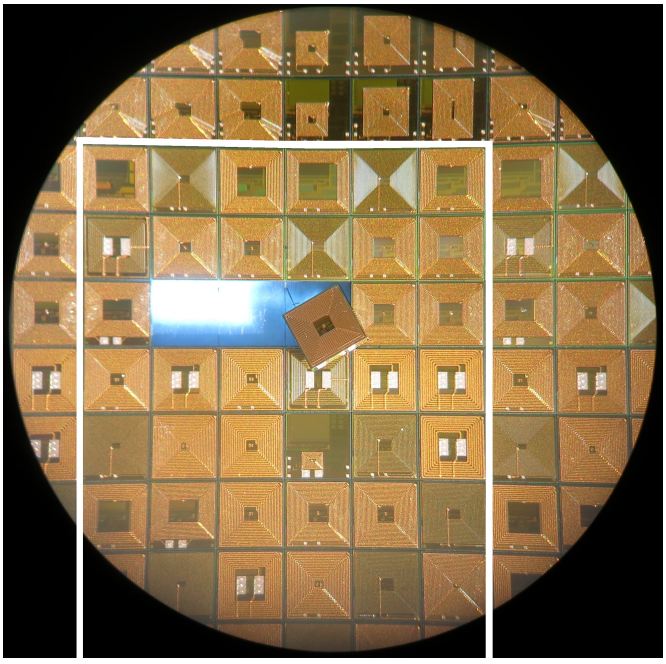


Figure 3.38: Microscope view of the produced WLP wafer: One reticle with all 33 different antenna designs is highlighted and marked with white lines. The presented 20u20u17W design is picked out and highlighted in the middle of the reticle.

3.2.4 Measurements

In the following, different measurement methods are introduced to verify the simulation results and to analyze the overall WLP structure. Starting with standard contact based impedance measurements with a vector network analyzer, this section also describes an automatic contactless measurement process. This process can be further used as functionality test, antenna measurement and firmware writing in mass productions. Additionally, the topography and the physical structure of the presented coil on chip transponder is analyzed with cross section and light detection and ranging (LIDAR) measurements.

Contact based measurement

To verify all simulation results, each coil on chip design was measured with a vector network analyzer. Therefore all 33 measurement structures are arranged onto a plastic carrier. Due to the metallic environment of the wafer prober this plastic spacer is needed. As can be seen in figure 3.39 the arrangement of each measurement chip is similar to the specific positions in the WLP-reticle. The 33 functional chips that are connected to the antennas with RDL vias are not mounted onto the measurement matrix.

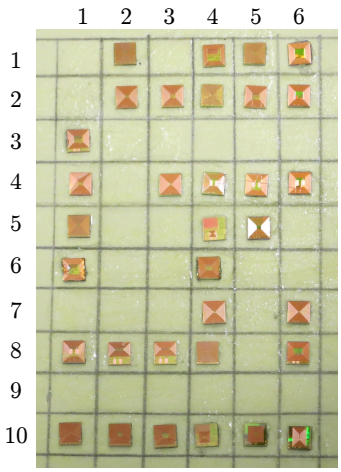


Figure 3.39: Measurement matrix of all 33 different antenna designs. Each design is realized as a measurement structure and as a fully functional, chip connected transponder. The measurement matrix uses the same chip arrangement as the WLP-reticle and comprises all measurement structures.

Figure 3.40 illustrates the measurement setup used. It consists of a wafer prober and a vector network analyzer. A needle card, equipped with two needles, was used to connect the coil on chip measurement samples to the vector network analyzer. A needle

touchdown of the presented 20u20u17W design can be seen in figure 3.41. Certainly the analyzer was calibrated on the end of the two needles. Therefore a custom build calibration kit (open, short, load) was used. As already described, the measurement samples are not connected to the chip pads. Thus the impedance of the designed two layer coil that is arranged on the top of the chip can be measured without any chip circuit influences.

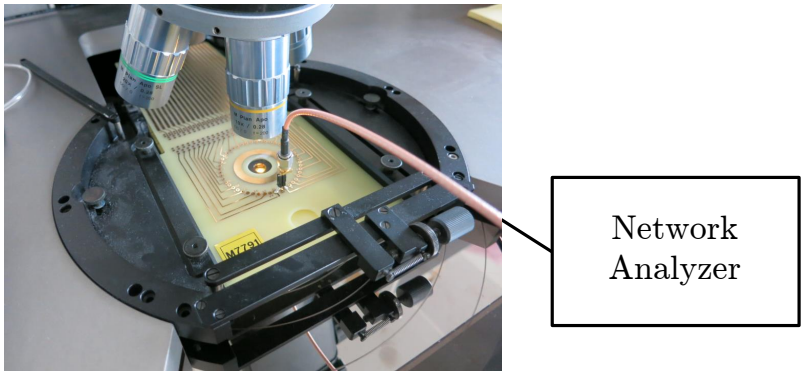


Figure 3.40: Measurement setup: A wafer prober was used to connect the measurement structures to the vector network analyzer. A two-needle card connects the particular antenna design. The calibration on the end of the needles is realized with a custom build calibration kit.

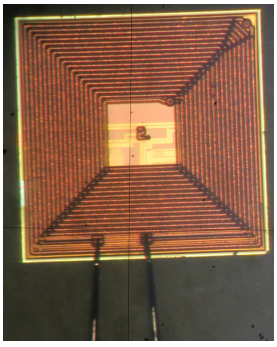


Figure 3.41: Needle touch down at the presented 20u20u17W antenna design: As can be seen, the measurement structure consists of the same layout as the specific chip connected 20u20u17W design. The measurement structures are not connected to the chip and equipped with additional measurement pads.

The measurement results of the 20u20u17W design are illustrated in figures 3.42 and 3.43. It can be seen that the imaginary part as well as the real part of the coil impedance fits well with the simulation results already discussed. Thus a connected 78 pF type three SLRE78xx chip card controller will work properly and operate at 13.56 MHz.

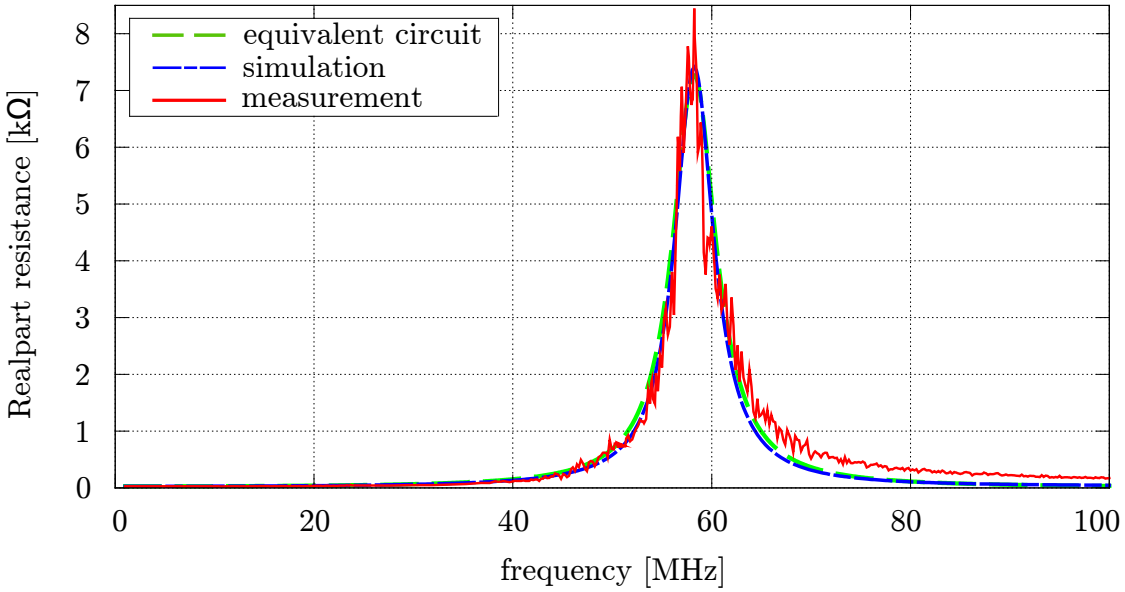


Figure 3.42: Real part measurement of the 20u20u17W coil on chip design.

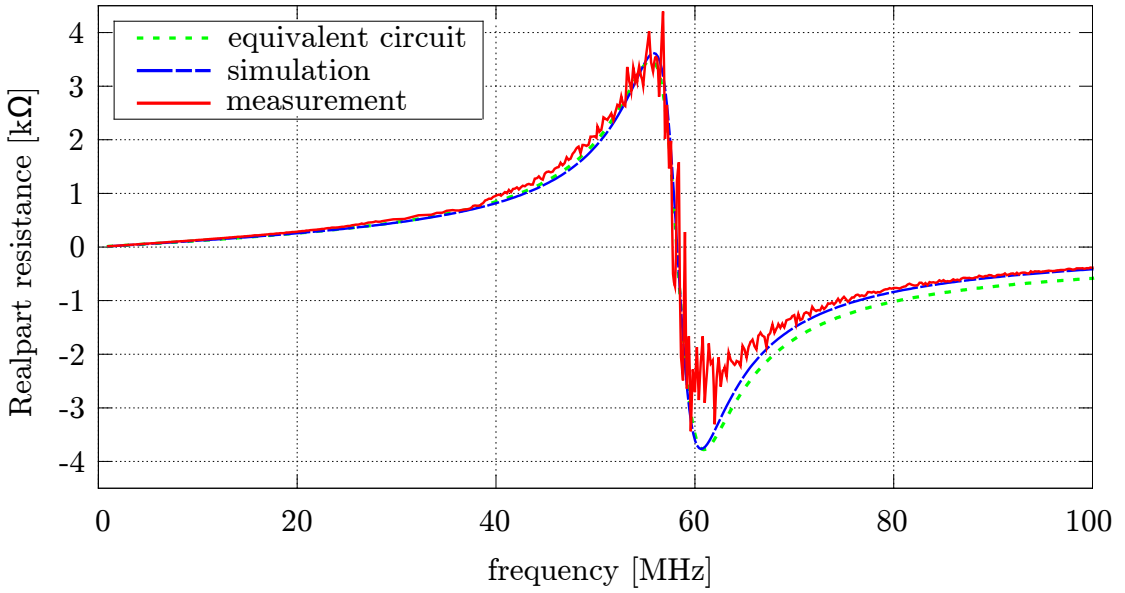


Figure 3.43: Imaginary part measurement of the 20u20u17W coil on chip design.

Contactless measurement

To verify the overall transponder design (antenna + connected chip), a contactless measurement was performed. As a first step this measurement was realized similarly to the method already described in 3.1.4. Therefore a six winding 3 mm x 3 mm coil antenna, shown in figure 3.44, was connected to the vector network analyzer. This antenna has a self-resonance frequency far beyond 13.56 MHz. If this sensing antenna is arranged very close to a coil on chip sample, the coupled resonating circuit can be measured. The measurement result of the 20u20u17W design is illustrated in figure 3.45. Due to the sensing antenna (L_{sens} = 78 nH), the overall real part increases to a self resonating peak far beyond 13.56 MHz. Nevertheless the real part peak of the coupled 20u20u17W transponder can be measured. As can be seen the resonating frequency of the 20u20u17W antenna design and the connected type three 78 pF chip card controller is 13.545 MHz. This result verifies the overall transponder design.

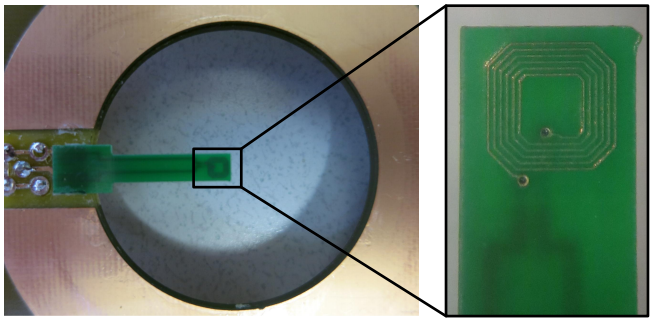


Figure 3.44: Resonance frequency measurement setup: A 3 mm x 3 mm sensing coil is arranged in the middle of a needle-less needle card. If a coil on chip sample is arranged very close to the antenna, the particular resonating frequency can be measured.

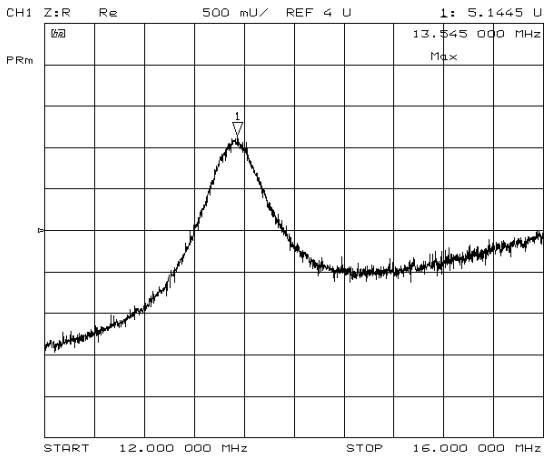


Figure 3.45: Real part of a sensing coil: The resonance frequency of the coupled coil on chip security controller, namely "20u20u17W", is f_r = 13.5 MHz.

Due to the large number of samples per wafer (see figure 3.37) this measurement process is improved and automated in a second step. Therefore the six winding sensing coil is mounted directly on to the wafer prober. With this setup, shown in figure 3.46, the measurement process already described is performed directly at the WLP wafer. A computer program developed for this purpose enables a fully automated measurement process. Therefore the prober is used to step from one chip to another, while performing a resonance frequency measurement. Indeed this fully automated system can be used as a test method in mass production. Besides the antenna performance measurements, this system could be also used to communicate with the specific transponder. Thus functionality tests and software writing (e.g. firmware) to the transponder memory are feasible.

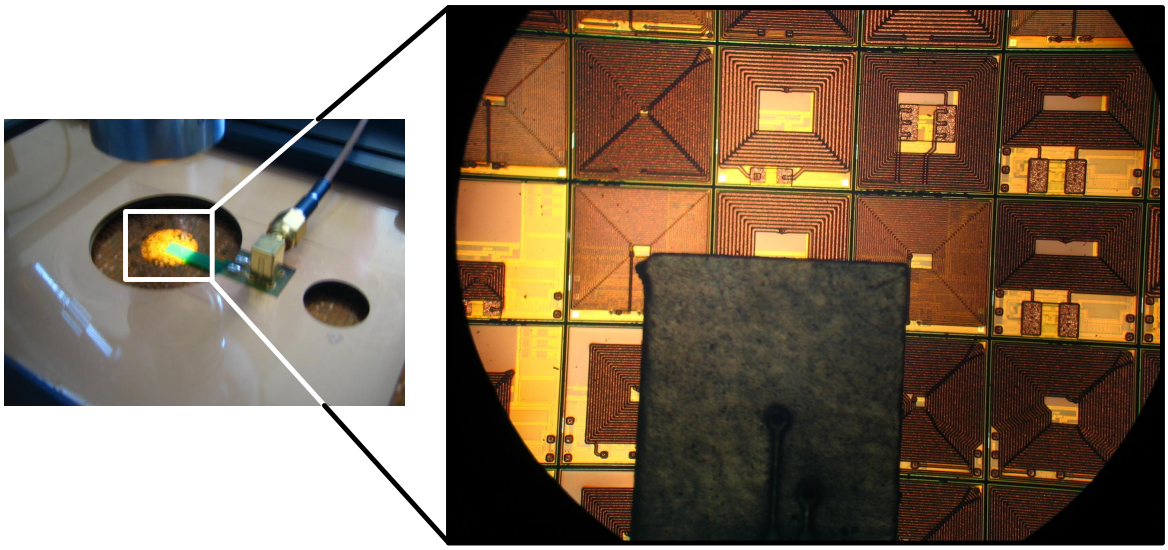


Figure 3.46: Automated measurement system: The 3 mm x 3 mm sensing coil is arranged very closely to the WLP wafer ($\sim 300\,\mu$m). By stepping from one sample to the other, the specific transponder design can be checked and measured.

Topography and physical structure measurements

In the following, the physical structure of the presented coil on chip design is analyzed. Moreover, a further coil on chip design is introduced - the "20u08u1L" (see table 3.3). This transponder design displays the outstanding WLP capabilities. In contrast to the 20u20u17W design, this variant comprises a coil with 20 μm track width and 8 μm track spacing. The extension "1L" points out that the design uses just one layer. Due to the extremely small track spacing, a stacked second layer is not feasible anymore. Although the number of windings per layer could be increased to 31, the available inductance is not high enough. Therefore the 78 pF chip card controller used is not able to operate at

13.56 MHz. Simulation as well as measurements show that the 20u08u1L transponder resonating frequency is 18.48 MHz. In any case, this design identifies the limits of the RDL miniaturization used and demonstrates the maximum available inductance at one layer ($L_{20u08u1L} = 961\,\text{nH}$). Indeed, in order to operate at 13.56 MHz the chip capacitance has to be increased to at least 140 pF. Figure 3.47 illustrates a unusable 20u08u1L design after the first RDL process step. As it is highlighted, a small coil defect is caused by resist adhesion. It can be seen that three coil windings are shortened by remaining copper material. Thus the 20u08u1L design experiment points out the limitations of the RDL process used. Around 10% of all produced 20u08u1L structures are affected.

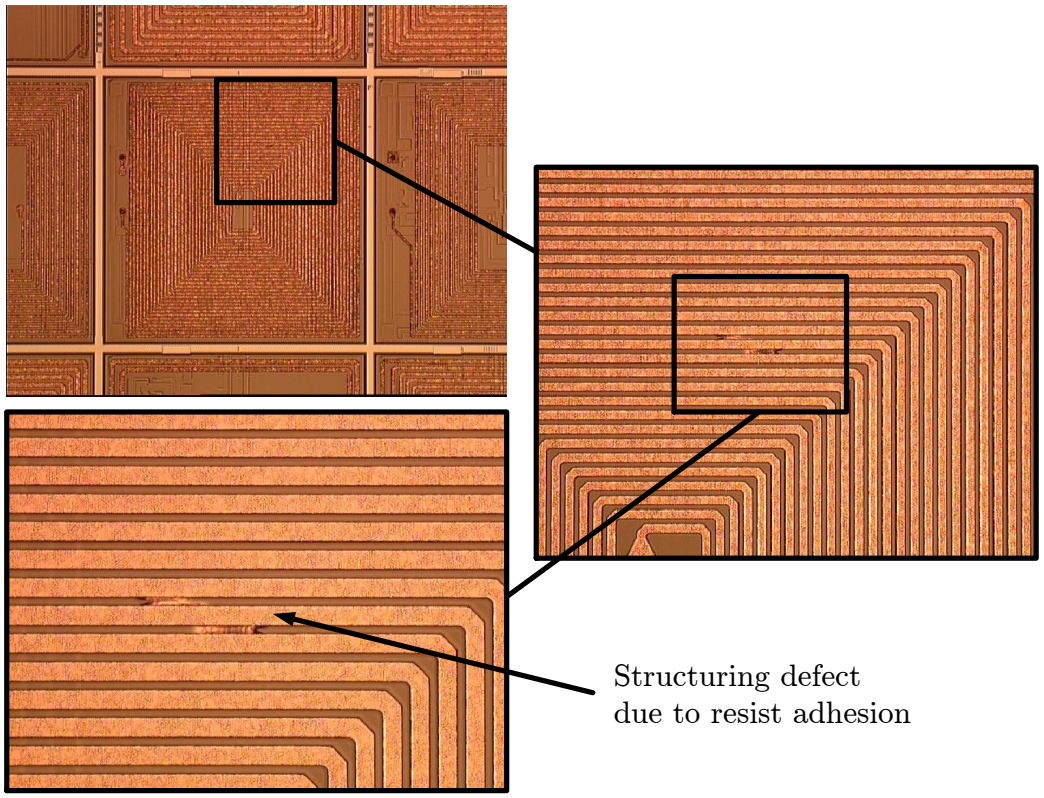


Figure 3.47: Structure defect at one of the 20u08u1L designs: Due to the small track spacing of the coil the electroplating process is pushed to its limits

To analyze the topography of both coil designs a light detection and ranging (LIDAR) measurement was performed. These measurement results are shown in figure 3.48 and figure 3.49. As can be seen in figure 3.49, a gap of 8 μm is truly challenging. It can not be guaranteed that there is no copper between the coil tracks at the bottom anymore. Nevertheless, the presented topography is still feasible and allows further WLP miniaturization. A 3D scan of the specific design is shown in figure 3.50 and 3.51.

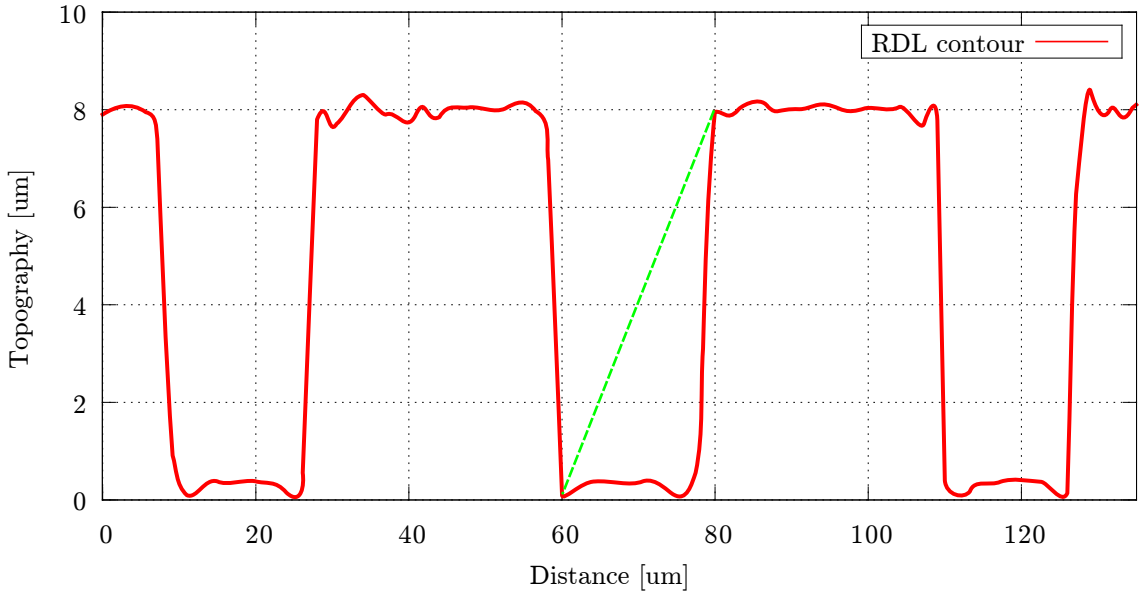


Figure 3.48: 20u20u17W design: 2D surface scan of RDL with 20μm track width and gap between coil tracks

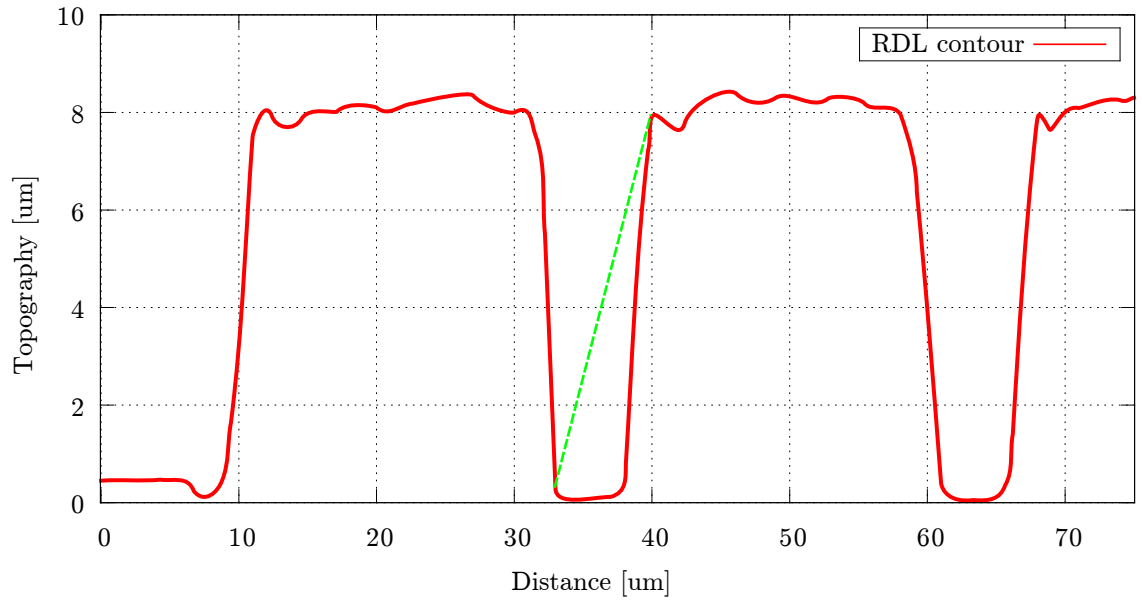


Figure 3.49: 20u08u1L design: 2D surface scan of RDL with 8μm gap between coil tracks. The track width of the coil is 20μm

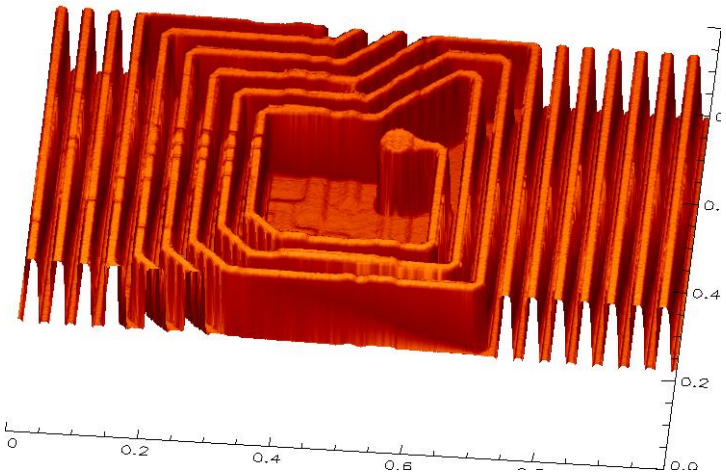


Figure 3.50: 3D surface scan of RDL with $20\mu m$ coil track space.

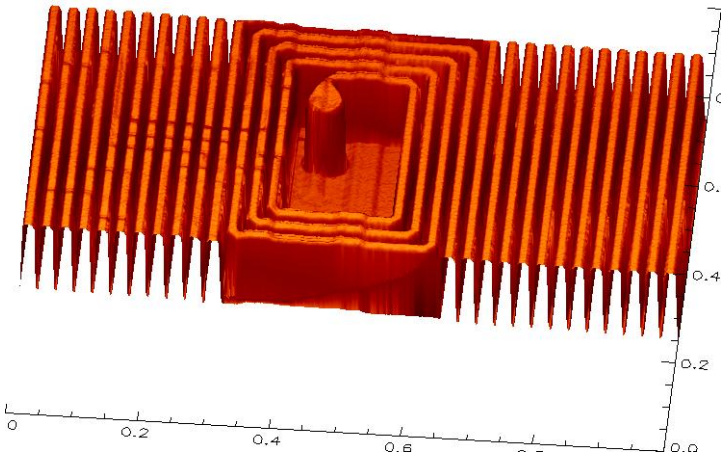


Figure 3.51: 3D surface scan of RDL with $8\mu m$ coil track space.

The cross section measurement allows an even more precise structure analysis. Moreover, process deviations can be observed. These cross section analyses are illustrated in figures 3.52 and 3.53 (for the 20u20u17W design) as well as in figure 3.54 and 3.55 (for the 20u08W1L design). As can be seen, both chips are cut along the dashed lines. After the cutting process, four points (a,b,c and d) are chosen for further investigation. A closer look at the points of interest (see figures 3.53 and 3.55) shows the increasingly rough surface caused by stacking the RDL layers. Therefore each coil track is stacked directly and parallel onto each other. A displaced coil track adjustment would decrease the surface quality and therefore the robustness of the overall structure. All highlighted views include dimensions measurements. It can be seen that the particular coil on chip design and WLP process was executed very precisely. The process deviation is smaller than one μm. Due to the bumpy surface of the second dielectric shown in figure 3.55, it is obvious that a second RDL layer with smaller track spaces ($< 8\mu m$) is not feasible.

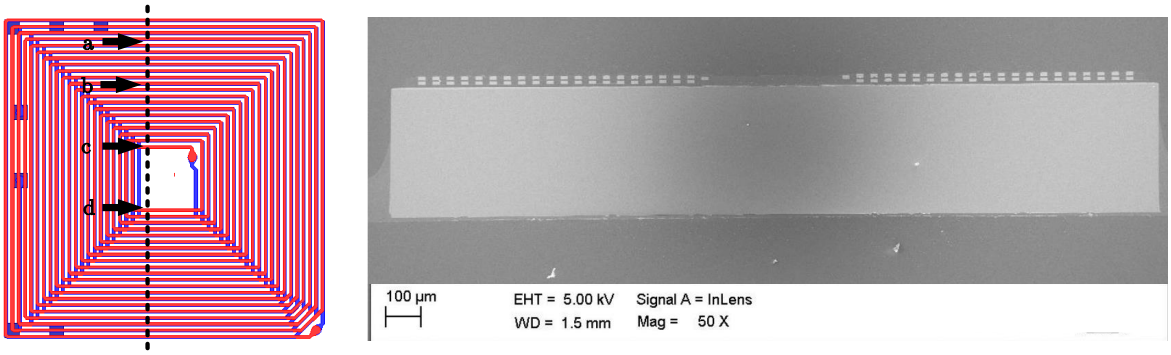


Figure 3.52: Left picture: 20u20u17W design layout. The dashed line marks the applied cross section. Positions a,b,c and d are used for further investigation. Right picture: Cross section of the presented 20u20u17W design. The stacked double layer coil on the top of the silicon chip is visible.

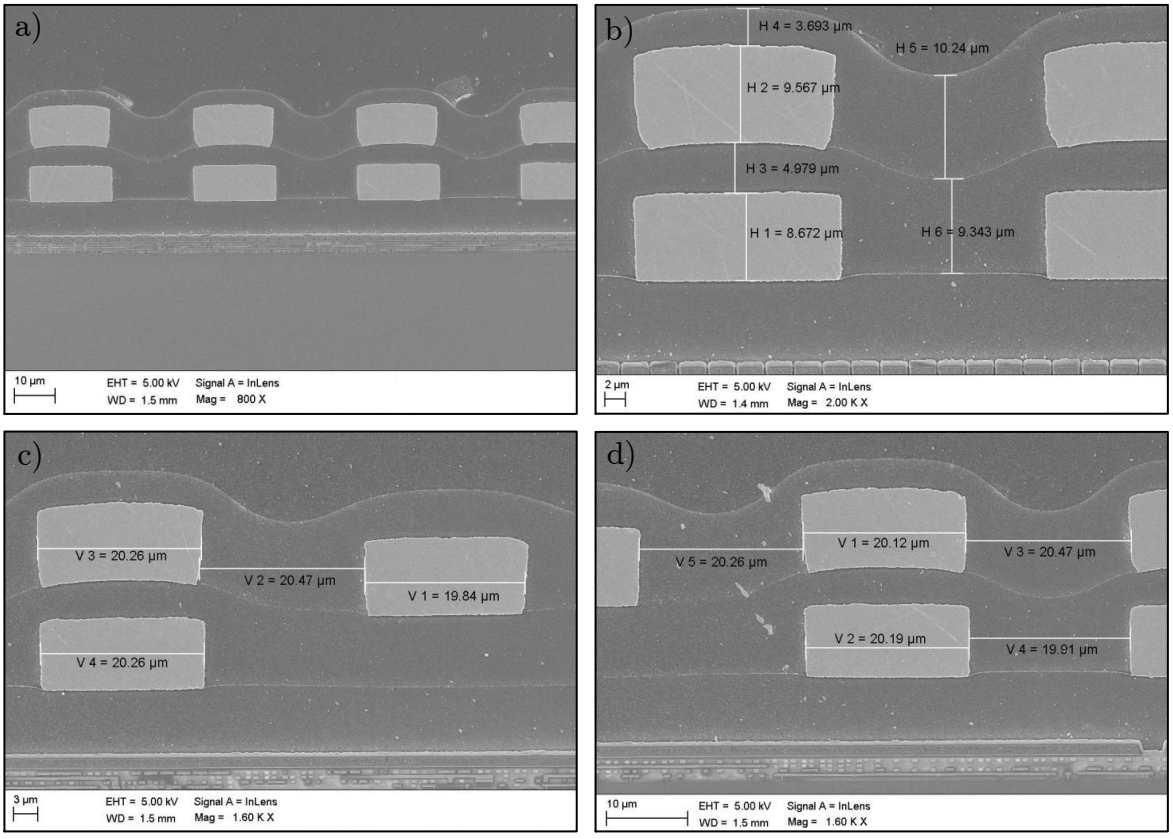


Figure 3.53: Points of interest that are illustrated in figure 3.52. Positions a,b,c and d are analyzed.

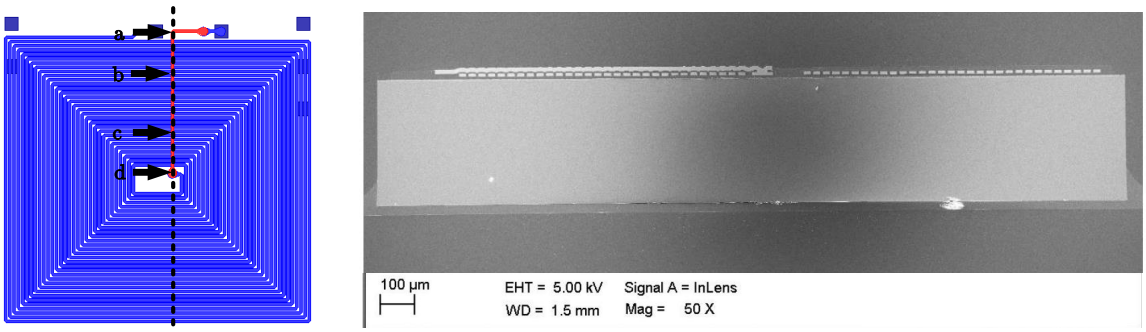


Figure 3.54: Left picture: 20u08u1L design layout. The dashed line marks the applied cross section. Position a,b,c and d are used for further investigation. Right picture: Cross section of the presented 20u08u1L design. Just one layer is used to realize the coil. A second layer realizes the necessary coil underpass.

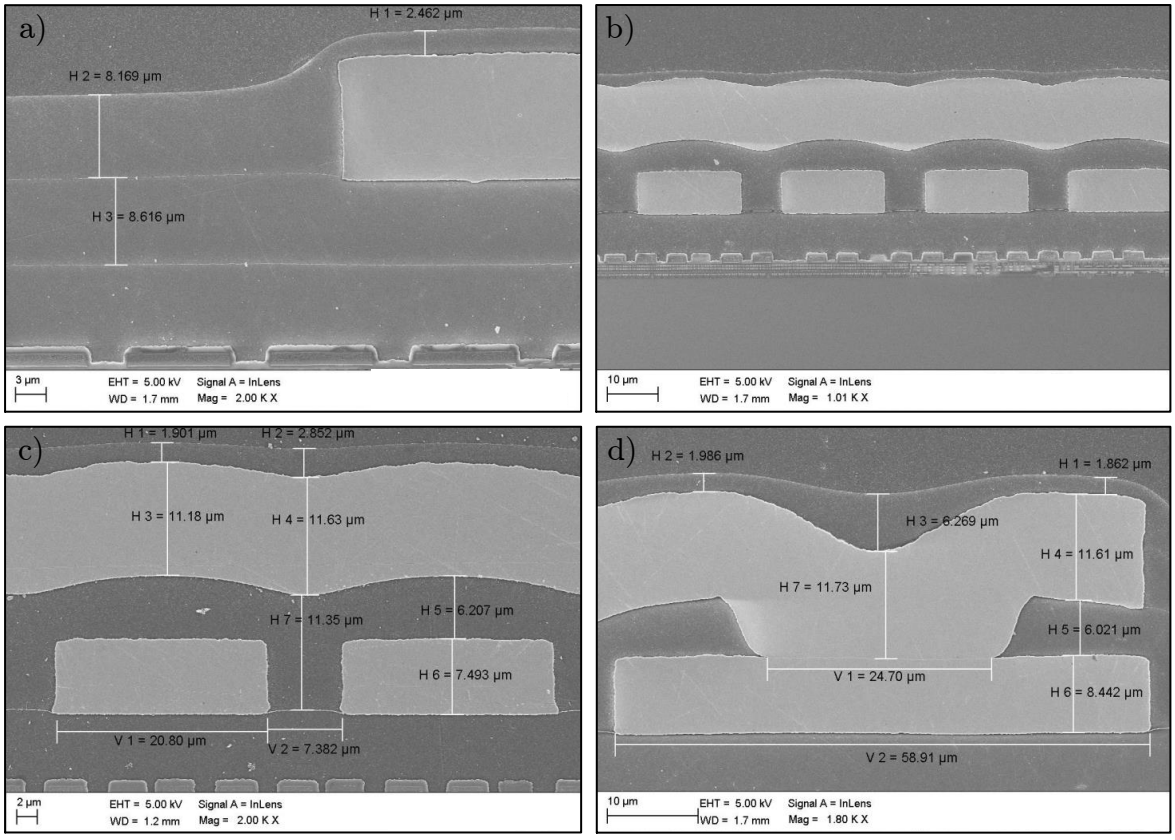


Figure 3.55: Points of interest that are illustrated in figure 3.54. Position a,b,c and d are analyzed.

3.3 Minatiurized Dual Band Tags

This section presents a novel highly miniaturized dual band RFID transponder with an on-chip antenna. The tag has a size of 1.32 mm^2 and was fabricated in a low cost 130 nm complementary metal-oxide-semiconductor process. The dual band RFID tag supports the electronic product code (EPC) generation (gen) 2 high frequency (HF) standard at 13.56 MHz and the EPC gen2 ultra high frequency (UHF) standard at 868 MHz. The custom built on-chip antenna comprises two connected resonanting coils. The antenna enables inductive coupling to an RFID reader in the HF and UHF bands. The maximum tag read range is 2.5 mm at 13.56 MHz and 4.4 mm at 868 MHz. This limited read range can be further increased by different types of booster antennas that will be presented in chapter 4. A typically application scenario of dual band RFID tags is illustrated in figure 3.56.

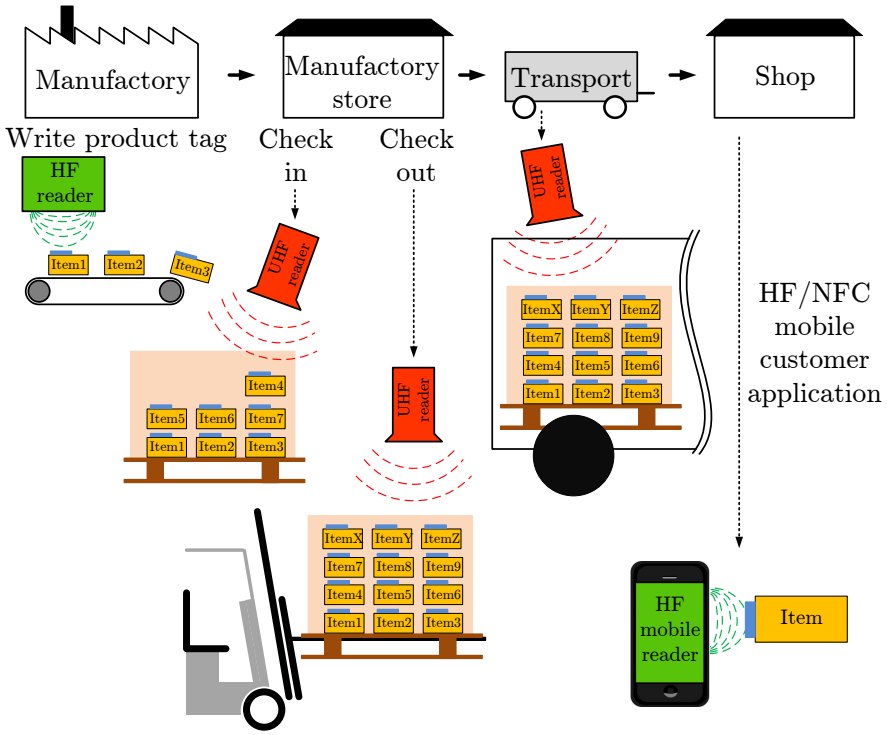


Figure 3.56: Dual band RFID tag application scenario: While the logistic is managed with the state of the art UHF technology, the near field applications such as writing and reading the tag is realized with the HF technology

Original Publications Related to this Section

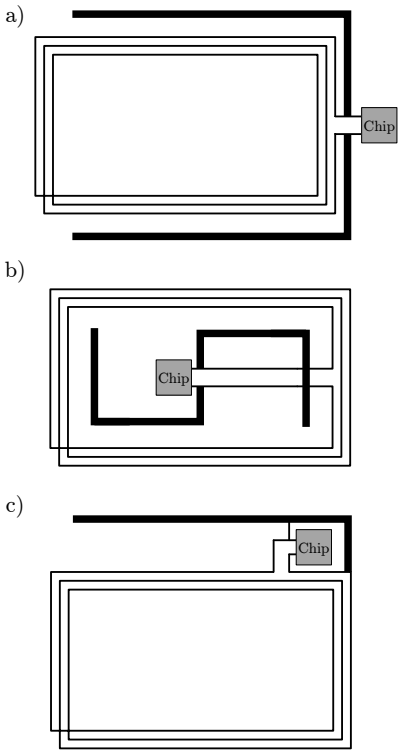
W. Pachler, J. Grosinger, W. Bösch, G. Holweg, and C. Steffan, „A Miniaturized Dual Band RFID Tag" In: RFID-Technologies and Applications (RFID-TA) September 2014, 2014 IEEE International Conference

Dual band radio frequency identification (RFID) transponders (tags) typically operate in the high frequency (HF) range at 13.56 MHz and in the ultra high frequency (UHF) range at $860 - 960$ MHz. Such tags take advantage of both HF and UHF RFID systems. The HF part of the dual band tags is able to provide a near field communication link (e.g., for tag configuration), while the UHF part of the tags provides a long range communication link (e.g., for tag readout).

Previous research on dual band RFID tags has focused on the tag chip design [71, 94] and on the tag antenna design [20, 21, 45, 60, 63, 67]. Typical realizations of dual band antenna designs consist of large HF coil antennas and UHF dipole antennas. The coil has been typically arranged around the dipole [45, 60, 63]. A significant size reduction has been realized by a combination of a shorted loop slot UHF antenna and an HF coil [67]. The main drawback of this implementation is the impairment of the UHF antenna performance due to the HF coil [63]. Thus, dual band antennas have been proposed with the UHF dipoles arranged outside the HF coils [20, 21]. However, this implementation lead to a further increase in size. A other implementation of dual band antennas combines a coil and an inverted-F antenna [77]. The relatively large coil acts as the groundplane of the IFA that is arranged on one side of the rectangular coil. A schematic overview of these researches is shown in figure 3.57.

The size of RFID tags plays an important role in many applications. Thus, miniaturized tags with on-chip antennas have been developed [66, 73, 108]. Mainly the tags operate at a single frequency and are miniaturized to a size of a few square millimeter [66]. Similar to miniaturized HF RFID tags [66, 73], miniaturized UHF RFID tags have been equipped with small coils and communicate with an RFID reader by means of inductive coupling [108]. These UHF RFID tags provide a limited read range in the range of a few millimeter.

So far, no research has been done on miniaturized dual band RFID tags with on-chip antennas. This paper presents a miniaturized RFID tag with a size of $1.32\,\mathrm{mm}^2$ that is equipped with a dual band on-chip antenna. To the authors knowledge this is the first time such a tag is presented. The on-chip antenna is realized by two connected resonating coils operating in the HF and UHF frequency bands. The read range of this tag is limited, but is thus further enhanced by custom-built HF, UHF booster antennas [81, 83].



T. Deleruyelle, P. Pannier, M. Egels, and E. Bergeret, "Dual Band Mono-Chip HF-UHF Tag Antenna," in Antennas and Propagation Society International Symposium (APSURSI), 2010 IEEE, 2010.

K. S. Leong, M. L. Ng, and P. Cole, "Miniaturization of Dual Frequency RFID Antenna with High Frequency Ratio," in Antennas and Propagation Society International Symposium, 2007 IEEE, June 2007.
P. Iliev, P. Le Thuc, C. Luxey, and R. Staraj, "Dual-Band HF-UHF RFID Tag Antenna," Electronics Letters, April 2009.
T. Deleruyelle, P. Pannier, J. Alarcon, M. Egels, and E. Bergeret, "MultiStandard Mono-Chip HF-UHF RFID Tag Antenna," in Microwave Conference (EuMC), 2010 European, 2010.
Z. L. Ma, L. J. Jiang, J. Xi, and T. Ye, "A Single-Layer Compact HF-UHF Dual-Band RFID Tag Antenna," Antennas and Wireless Propagation Letters, IEEE, 2012

Y. Nishioka, K. Hitomi, H. Okegawa, T. Mizuno, T. Fukasawa, H. Miyashita, Y. Konishi, "Novel antenna configuration for HF- and UHF-band hybrid card-type RFID tags," *Antennas and Propagation (EuCAP), 2010 Proceedings of the Fourth European Conference on* , vol., no., pp.1,5, 12-16 April 2010

Figure 3.57: Schematic overview of the previous research. Indeed a few dual band antenna concepts are already developed. Nevertheless, to the authors knowledge, for the first time a miniaturized dual band RFID antenna is reported. Due to the dual band capability, the presented tag can be applied to any kind of inductive coupled booster antenna (see section 4).

3.3.1 Tag Chip

The custom-built dual-band tag chip supports two different RFID standards, the electronic product code (EPC) generation (gen) 2 HF standard operating at 13.56 MHz and the EPC gen2 UHF standard operating at 868 MHz [94]. The analog frontend of the chip is shown in Figure 3.58. T1 is a very large device with a big parasitic capacitance. The large transistor is necessary to convert excessive chip input energy into thermal energy [94]. In particular, such a conversion is necessary in the HF operating mode due to the high amount of energy in the near field communication link. The generated heat mainly spreads through the chip metals. In general, connected metal structure (e.g bondwires) are responsible for a good heat dissipation [12]. Here, the on-chip antenna acts like an additional heat sink. The UHF rectifier is capacitively coupled to the HF rectifier. A built-in voltage multiplication in the UHF part leads to a tag sensitivity of $-11.4\,\mathrm{dBm}$ [94].

An important parameter for the tag antenna design is the input impedance of the chip in absorbing mode [33]. This impedance is mainly governed by the shunt transistor T1 and the HF/UHF rectifier in the chip frontend. The chip impedance Z_{Chip} varies with frequency f and can be computed by means of an equivalent parallel circuit. The circuit consists of a frontend resistance $R_{\text{FE}} = 1100\,\Omega$ and a frontend capacitance $C_{\text{FE}} = 390\,\text{fF}$. The chip impedance can be then calculated by

$$Z_{\text{Chip}} = R_{\text{Chip}} + \jmath X_{\text{Chip}} = \frac{1}{1/R_{\text{FE}} + \jmath\omega C_{\text{FE}}} \tag{3.3.1}$$

R denotes the real part of the chip impedance, while X denotes the imaginary part. $\omega = 2\pi f$ is the angular frequency. The chip impedance is $Z_{\text{Chip,HF}} = (1099 - \jmath 40)\Omega$ at $f = 13.56\,\text{MHz}$ and $Z_{\text{Chip,UHF}} = (170 - \jmath 398)\Omega$ at $f = 868\,\text{MHz}$.

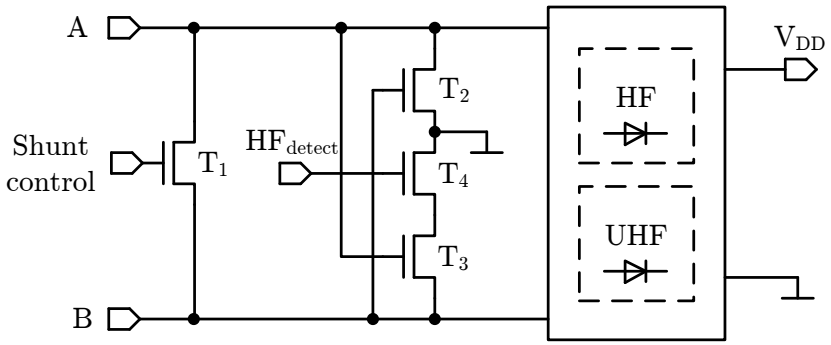


Figure 3.58: Tag chip frontend: The dual-band tag chip supports the EPC gen2 HF and UHF standard. A and B denote the chip input signals. The input impedance of the chip is $Z_{\text{Chip,HF}} = (1099 - \jmath 40)\Omega$ at 13.56 MHz and $Z_{\text{Chip,UHF}} = (170 - \jmath 398)\Omega$ at 868 MHz.

3.3.2 On-Chip Tag Antenna

The dual band on-chip tag antenna must fit perfectly to the chip size that is 1.1 mm × 1.2 mm. Due to this size constraint, the HF and UHF parts of the antenna are realized by two small coils that communicate with an HF reader and a UHF reader via inductive coupling. The HF and UHF coils operate together with the chip as two independent resonant circuits as shown in Figure 3.59. The figure shows a simplified equivalent circuit of the dual band tag. The equivalent circuit consists of the chip with its input signals A and B, an inductance due to the HF coil L_{HF}, a capacitance C_{HF} that tunes the HF coil resonance to 13.56 MHz and an inductance due to the UHF coil L_{UHF}. In HF mode, the small inductance L_{UHF} acts as a short wire that connects the HF parallel resonant circuit — L_{HF} and C_{HF} — to the tag chip. In UHF mode, the capacitance C_{HF} works as a short circuit. Thus, the equivalent circuit of the UHF mode is determined solely by the inductance L_{UHF}. L_{UHF} is matched to the complex conjugate chip impedance $Z^*_{\text{Chip,UHF}}$

Table 3.5: Parameter values of the extended equivalent circuit

Parameter	L_{UHF}	R_{UHF}	L_{HF}	R_{HF}	C_{HF}
Values	31 nH	19 Ω	940 nH	204 Ω	11 pF
Parameter	C_{COIL}	C_{PARA}	R_{PARA}	R_{CON}	
Values	8.8 pF	700 fF	11 Ω	35 Ω	

to assure a high tag power transmission coefficient, i.e., a maximum power transfer from the tag antenna to the chip [33].

The design of the HF coil and the UHF coil was done by means of the 2.5 D electromagnetic field simulator Momentum in Advanced Design System [2]. The on-chip antenna substrate is silicon that has a high permittivity of about $\epsilon_{\mathrm{r}} = 11.7$ [11]. The silicon substrate has a height of 300 μm. The main part of the on-chip antenna is realized with the top metal layer of the complementary metal-oxide-semiconductor (CMOS) process, which has a thickness of 1.2 μm.

The electromagnetic field simulator allows to assess parasitic effects that influence the antenna design. These parasitic effects are modeled by an extended equivalent circuit (see Fig. 3.60). The circuit includes parasitic components due to conductive losses of the HF coil R_{HF} and the UHF coil R_{UHF}. These conductive losses are mainly due to the small thickness of the on-chip antenna metal. Also, the HF coil is formed by two layers, i.e., an additional capacitance C_{COIL} is considered in the HF parallel resonant circuit to model this parasitic effect. Additional parasitic components in the extended equivalent circuit are C_{PARA} and R_{PARA} that are caused by the whole metal stack. R_{CON} models conductive losses in the small connectors of the antenna to the chip. All parameters of the extended equivalent circuit are listed in Tab. 3.5.

The antenna design can be seen in Fig. 3.61. The figure shows that the HF coil is surrounded by the UHF coil.

The two-layer HF coil consists of 28 windings with a width of 10 μm and a spacing between the windings of 1 μm. The coil covers an area of 0.9 mm × 0.9 mm. The inductance of the HF coil is $L_{\mathrm{HF}} = 940\,\mathrm{nH}$. The HF parallel resonant circuit — L_{HF}, C_{HF}, and C_{COIL} — is designed for a resonance frequency of $f_{\mathrm{Res}} = 13.56\,\mathrm{MHz}$ with

$$f_{\mathrm{Res}} = \frac{1}{2 \cdot \pi} \cdot \sqrt{\frac{1}{L_{\mathrm{HF}} \cdot (C_{\mathrm{HF}} + C_{\mathrm{COIL}})} - \frac{{R_{\mathrm{HF}}}^2}{{L_{\mathrm{HF}}}^2}} \tag{3.3.2}$$

leading to the tuning capacitance value of $C_{\mathrm{HF}} = 11\,\mathrm{pF}$. The symmetric UHF coil consists of four windings with a width of 15 μm and a spacing of 2 μm. The UHF coil covers the complete chip size of 1.1 mm × 1.2 mm. The inductance of the coil is $L_{\mathrm{UHF}} = 31\,\mathrm{nH}$.

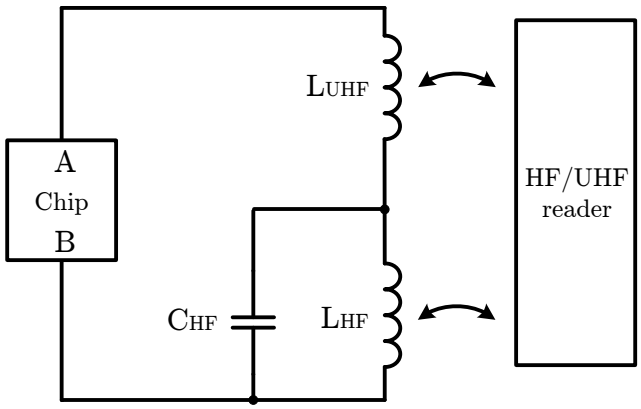


Figure 3.59: Simplified equivalent circuit of the dual band tag: The equivalent circuit consists of the chip, an inductance due to the HF coil L_{HF}, and a capacitance C_{HF} that tunes the HF coil resonance to 13.56 MHz and an inductance due to the UHF coil L_{UHF}. The tag communicates with the HF/UHF reader via inductive coupling.

3.3.3 Realization

Fig. 3.61 shows a photograph of the realized dual band RFID tag with its on-chip antenna consisting of the HF and UHF coils. The tag was fabricated in a low-cost 130 nm CMOS process.

To verify the antenna design, the antenna input impedance $Z_{\mathrm{Ant}} = R_{\mathrm{Ant}} + \jmath X_{\mathrm{Ant}}$ was measured with a wafer prober. The connections of the tag antenna to the chip were cut off to ensure an impedance measurement of the antenna without an influence of the RFID chip. The measurement result is plotted in Fig 3.62. The figure plots the power transmission coefficient of the tag. The power transmission coefficient is calculated according to [33]

$$\tau = \frac{4R_{\mathrm{Chip}}R_{\mathrm{Ant}}}{|Z_{\mathrm{Chip}} + Z_{\mathrm{Ant}}|^2}. \tag{3.3.3}$$

As designed, the transmission coefficient reaches its maxima at the tag operating frequencies at 13.56 MHz and 868 MHz. The measurement agrees with the simulation and with the calculations according to the extended equivalent circuit. Nevertheless, it can be seen that there are main discrepancies in τ at 868 MHz. This is caused by the lossy waver prober environment which was not considered in simulation and calculation.

3.3.4 Tag Read Range

Fig. 3.63a) illustrates the measurement setup related to the read ranges in HF and UHF mode. For this measurements two reader coils with similar geometries are used. The

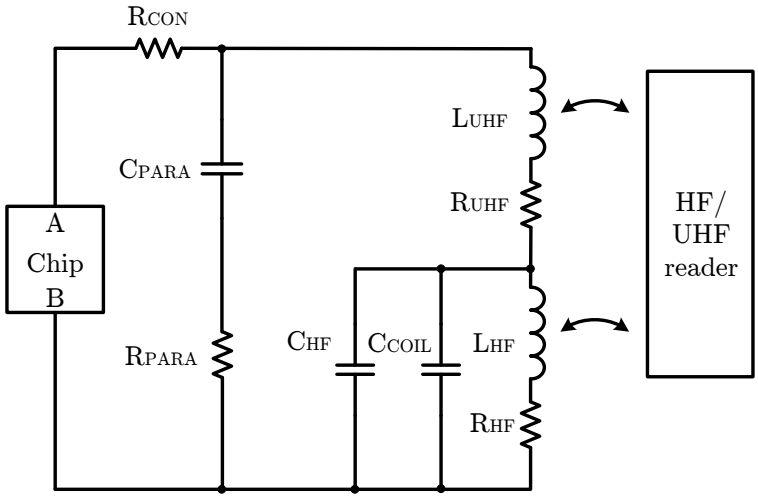


Figure 3.60: Extended equivalent circuit of the dual band tag: The circuit includes additional components due to parasitic effects (R_{UHF}, R_{HF}, C_{COIL}, C_{PARA}, R_{PARA}, and R_{CON}) in comparison to the simplified equivalent circuits shown in Fig. 3.59. The values of the circuit parameters are listed in Tab. 3.5.

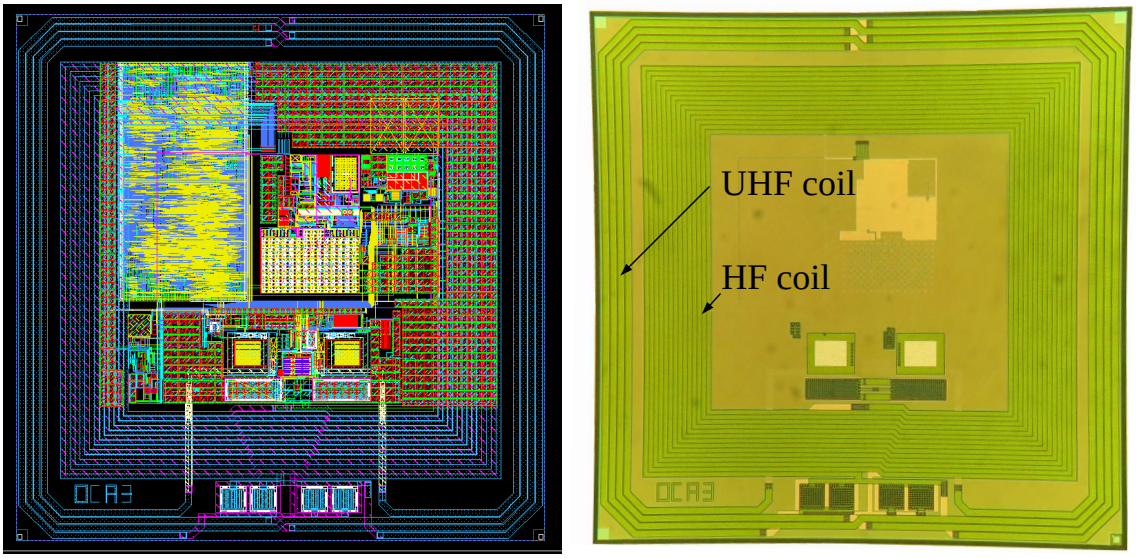


Figure 3.61: (left) layout (right) Photograph of the produced dual band RFID tag and its on-chip antenna: The tag is designed and fabricated in a low-cost 130 nm CMOS process. The two-layer HF coil with 28 windings is arranged in the center of the UHF coil that consists of four windings.

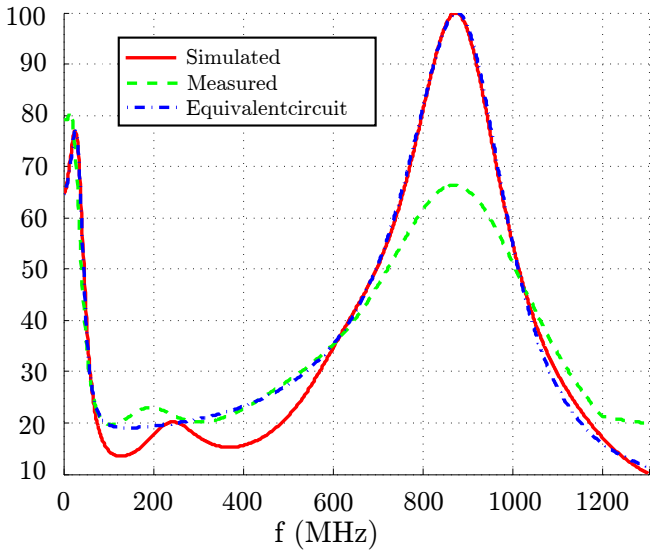


Figure 3.62: Power transmission coefficient of the dual band tag: The coefficient reaches its maxima at the tag operating frequencies at 13.56 MHz and 868 MHz. The measurement agrees with the simulation and with the calculations according to the extended equivalent circuit. The measurement and simulation curves show a small ripple at around 200 MHz that cannot be seen in the equivalent circuit curve. The ripple is caused by a parasitic component that is not included in the equivalent circuit.

HF coil consists of 13 windings. The track and gap width of the coil is 100 μm. The size of the coil is 7 mm x 7 mm. 7 windings are arranged on the top side of the 0.4 mm thick FR4 (Fig. 3.63b) and 6 windings are arranged at the bottom side (not visible). The impedance of this small 13.56 MHz reader coil is $Z_{\mathrm{HF,readercoil}} = (5.1 + \jmath 114)\Omega$. As it is illustrated this impedance is power matched to approximately 50 Ω with two capacitors: a parallel capacitor with 68 pF and a serial capacitor with 33 pF.

The geometry of the UHF coil, illustrated in Fig. 3.63a) and c), is similar. The size of the UHF coil is 7 mm x 7 mm with a 4 mm x 4 mm free area in the middle of the coil. In contrast to the HF coil, the UHF antenna comprises just one thick winding on the top side of the FR4. The impedance of the one winding UHF coil ($Z_{\mathrm{UHF,readercoil}} = (1 + \jmath 56)\Omega$) is power matched to 50 Ω with a tuner. As it can be seen from Fig. 3.63b) and Fig. 3.63c), both antennas are arranged on the top of a yellow paper sheet stack. Both power-matched antennas are connected to the HF/UHF Feig Obit^{TM} RFID readers [78].

Fig. 3.63b) show the measured reading distances of the described measurement setup. With an output power of 0.3 W of both Feig ObitTM RFID reader devices, the maximum reading distance of the dual band tag is 2.5 mm in HF mode and 4.4 mm in UHF mode. The decreased performance in HF mode is mainly caused by the on-chip antenna design.

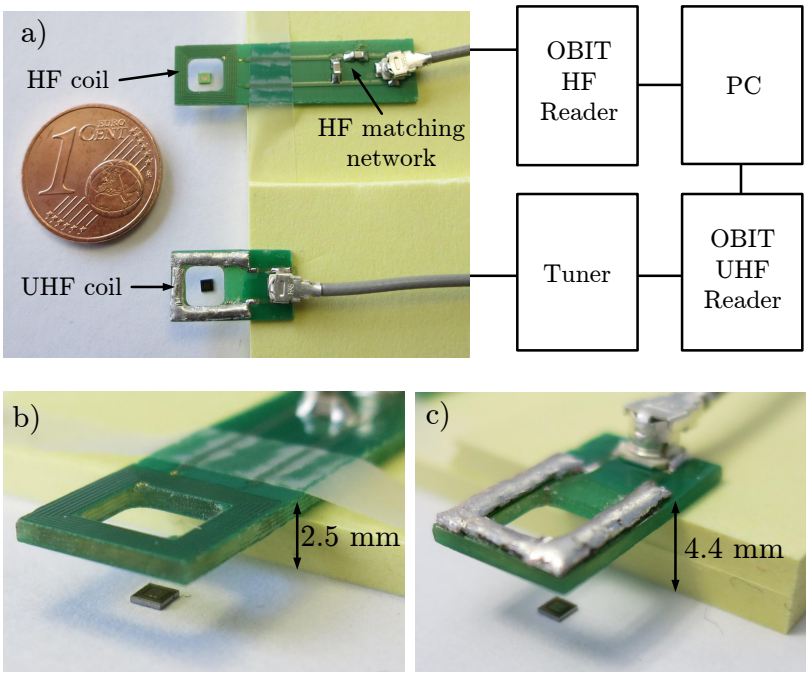


Figure 3.63: Reading distance measurement setup: Part a) of the figure shows a custom-build HF and UHF coils with an inner metal-free area of 4 mm x 4 mm is used to measure the maximum reading distance of the dual band RFID tag. Both reader antennas are matched to 50 Ω and connected to a HF and UHF RFID reader devices that are controlled by a personal computer (PC). Part b) and c) highlight the reading distance measurement of the setup illustrated in a). The antennas are arranged on the top of a paper sheet stack. A maximum reading distance of 2.5 mm in HF mode and 4.4 mm in UHF mode is measured.

As already described, the size of the on-chip HF coil is 25 % smaller than the UHF on-chip coil. Furthermore the UHF on-chip coil surrounds the HF on-chip coil which causes additional losses.

Summarizing, this work presents a novel highly miniaturized dual band RFID tag with an on-chip antenna. The tag size is 1.32 mm. The tag is realized in a low cost 130 nm CMOS process. The dual band tag supports the EPC gen2 HF and UHF standard operating at 13.56 MHz and 868 MHz. The tag provides a stand alone read range of 2.5 mm at 13.56 MHz and 4.4 mm at 868 MHz. This small read range can be extended by the use of booster antennas. This paper uses already reported types of booster antennas to present the all-purpose capability of the dual band RFID tag. A HF booster antenna [81] is able to extend the read range to 40 cm. An UHF booster antenna [83] extend the read range to 2 m. The presented miniaturized dual band RFID tag enables new capabilities: Booster antennas can be easily realized on a flexible substrate and can be attached to the skin of a person like a plaster. The booster antenna then extends the read range of

the dual band tag that is fitted to operate in the body. This extension enables an HF communication of the tag with a handheld or mobile device to configure the implanted tag and enables a UHF communication with an on-body reader of a wireless body area network [34].

3.4 On-chip Capacitive Coupled Tag

As already discussed, highly miniaturized radio frequency identification (RFID) transponders (tags) have been brought to the market. These tags are typically equipped with small on-chip coils and communicate with the RFID reader by inductive coupling at 13.56 MHz. In contrast, this section presents a one square millimeter RFID tag that communicates with the reader by non-resonant capacitive coupling at 13.56 MHz and 868 MHz. This on-chip capacitive coupled (OC3) tag is designed and fabricated in a low cost 130 nm CMOS process. The OC3 tag enables a contactless communication with the RFID reader in metal environments, while tags based on inductive coupling are easily impaired in their operation. Experiments show that the presented OC3 RFID tag is able to communicate with an electronic product code compliant reader in the high frequency and ultra high frequency ranges.

Original Publications Related to this Section

W. Pachler, J. Grosinger, W. Bösch, P. Greiner, G. Hofer, and G. Holweg, „An On-Chip Capacitive Coupled RFID Tag" In: European Conference on Antennas and Propagation, April 2014.

3.4.1 Capacitive coupling mechanism

State-of-the-art miniaturized RFID tags have a few square millimeters of size and typically operate in the high frequency (HF) range at 13.56 MHz [66, 73]. A few other tag solutions operate in the ultra high frequency (UHF) range at 868 MHz [108] and at 2.4 GHz [13].

As already presented, small RFID tags are typically equipped with on-chip antennas realized as highly miniaturized coils that communicate with an RFID reader based on inductive coupling. The on-chip coils are designed to operate at a specific frequency and are typically realized with a number of windings to achieve the desired reading distance of the passive systems. However, multiple on-chip windings lead to high manufacturing costs because of required additional metal layers and vias.

The inductive coupling scheme of the tags is based on magnetic fields [26] and establishes an adequate well contactless communication to the RFID reader in near field applications. However, this communication can be impaired in the presence of metals. The magnetic field can easily be shielded by the metal environment. In addition, eddy currents induced in the metal generate losses and thus reduce the reading distance of the near field communication system.

This section presents a small RFID tag that communicates with the reader by means of a non-resonant capacitive coupling mechanism. So far, this mechanism has been used in the field of non-galvanic chip to chip interconnections [4, 17, 99]. In the following, the presented on-chip capacitive coupled (OC3) tag is denoted as OC3 tag. The OC3 tag uses an additional metal layer on the tag chip surface to communicate with the reader based on capacitive coupling.

The coupling mechanism is non-resonant and thus allows to operate the chip at multiple frequencies, i.e., in the case of a dual-band HF/UHF RFID chip at HF and UHF frequencies. The OC3 RFID tag is not forced to operate at one certain frequency in comparison to on-chip coils. Because OC3 tags need only one additional metal layer on the chip, the manufacturing costs are reduced in comparison to inductively coupled tags.

Additionally, OC3 tags are able to transmit signals through metal barriers [62, 112] and provide an anti-interference feature against magnetic fields [17].

3.4.2 OC3 Implementation

The OC3 RFID tag bases upon a ultra low power multi-frequency passive RFID tag chip that supports the electronic product code (EPC) Generation 2 HF and UHF RFID standards [94]. It has a sensitivity of $-11.4\,\mathrm{dBm}$. The core of the RFID tag (analog and digital part) is equivalent to the RFID tag that was used in section 3.3. Nevertheless, to enable the capacitive coupling mechanism, the analog frontend was modified. Figure 3.64 shows the revised concept of the analog frontend. The analog frontend of the OC3 tag consists of a large metal surface on the top of the chip that acts as one capacitor electrode to communicate with the reader (see Sec.4.3.4). The second electrode of the OC3 tag is realized by the silicon substrate that is connected to the chip ground. This concept differs from state of the art capacitive coupling due to the substrate electrode. Reported capacitive coupled chip to chip interconnections, such as [4, 17, 99], use several capacitive coupled surfaces on the top of the chip. Typically these metal surfaces are arranged next to each other. Due to the minimum chip to chip communication distance(μm), this concept is applicable. Nevertheless, in case of RFID tags and larger read ranges, these coupling surfaces has to be as large as possible. Therefore, as it is shown in Figure 3.64, both (bottom and top) sides of the silicon are used for the presented novel coupling mechanism.

As illustrated in Fig. 3.64, the input of the analog frontend is connected to the top metal surface. The analog frontend is designed similar to a Delon circuit [114], i.e., the OC3 frontend works like a rectifier and a voltage doubler. Transistor T1 represents the positive part of the rectifier and works as a diode-connected transistor with threshold voltage cancelation to generate a high output voltage. Therefore, a bias voltage V_{B} is generated by a current I_{B} and transistor T2. The negative part of the rectifier is realized by transistor T3. Transistor T4 is needed for the clear defined start-up sequence of the

tag and operates in subthreshold. For better understanding, this concept is simplified in Fig. 3.65. The Delon circuit is charging a capacitor that is powering the chip with VDD.

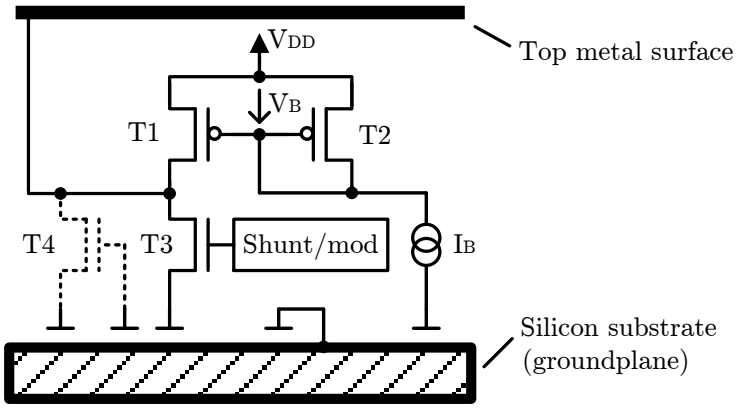


Figure 3.64: Analog CMOS frontend concept of the OC3 RFID tag: The tag bases upon a dual-band HF and UHF RFID tag with a minimum supply voltage of 2.8 V [94]. The frontend is designed similar to a Delon circuit.

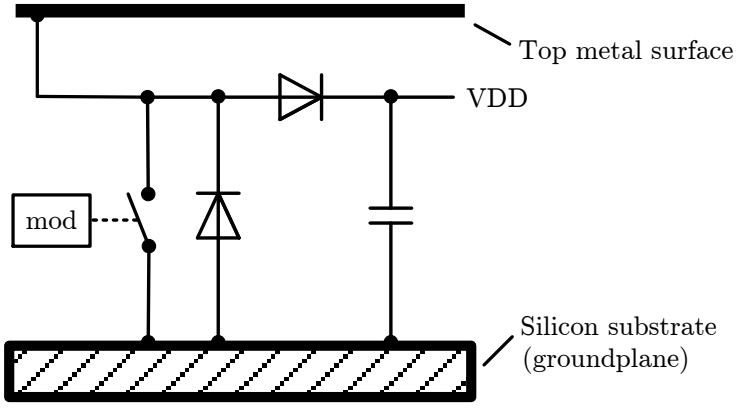


Figure 3.65: Simplified concept of the analog frontend. VDD is generated by a rectifier and stored in a capacitor.

T3 additionally is responsible for the data modulation and the shunt regulation [94]. Thus, the impedance of the chip rectifier is modulated by T3 and varies with the tag EPC. This variation in impedance causes a load modulation [26] and thus allows the communication with the reader. The chip impedance is mainly characterized by the chip rectifier impedance and can be modeled by a parallel circuit of a chip capacitance $C_{\text{chip}} = 810\,\text{fF}$ and a chip resistance R_{chip} that varies with modulation between approximately $40\,\Omega$ and $8\,\text{k}\Omega$. V_{DD} is the supply voltage of the chip. The minimum supply voltage of 2.8 V guarantees a proper shunt regulation and data modulation of the tag.

Figure 3.66 shows the layout of the realized silicon chip and the manufactured prototype. The tag is designed and fabricated in a low-cost 130 nm complementary metal-oxide-semiconductor (CMOS) process. The size of the OC3 tag is one square millimeter. Its thickness is 300 μm that is mainly determined by the thickness of the silicon substrate. Certainly, the thickness can be reduced to e.g 50 μm by polishing the silicon substrate. Note that such very thin capacitive coupled RFID tags - OC3 - enables new capabilities, such as embedding the OC3 into paper. The picture in Fig. 3.66 shows the top metal layer of the chip that is covered with a protective imide layer. The thickness is of the dielectric imide layer is $\sim$ 3 μm and prevent the galvanic contact to the OC3. The dimensions of the OC3, 1 mm x 1 mm x 300 μm, compared to a one euro cent coin, can be seen in Figure 3.67

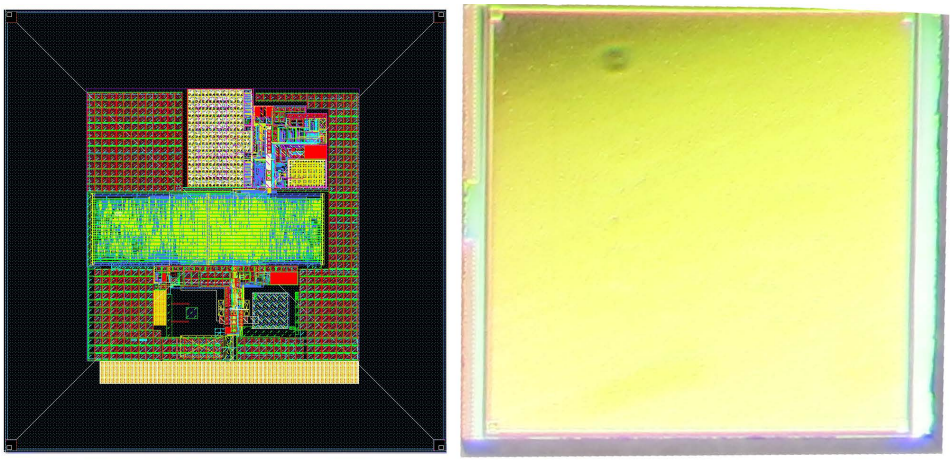


Figure 3.66: Layout (left side) and picture (right side) of the realized OC3 RFID tag: The size of the tag is one square millimeter. The picture on the right shows the top metal layer of the tag. This layer is covered with a protective imide layer with a thickness of 3 μm. The top metal layer and the silicon substrate of the tag act as electrodes to communicate with the RFID reader by means of capacitive coupling.

3.4.3 Experimental Validation

The OC3 tag communicates with the reader by means of a non-resonant capacitive coupling mechanism. The top metal layer and the silicon substrate of the tag act as capacitor electrodes that couple to the corresponding reader electrodes. The entire communication system including the OC3 tag and the reader acts as a simple capacitive voltage divider. A wireless communication with the reader is established as long as the capacitive voltage divider guarantees a voltage supply of 2.8 V to the OC3 tag at the operation frequency. Voltages greater than 2.8 V will be regulated by the shunt-resistor, shown in Figure 3.64.

Figure 3.68 shows the equivalent circuit of the system. The parallel circuit of C_{chip} and

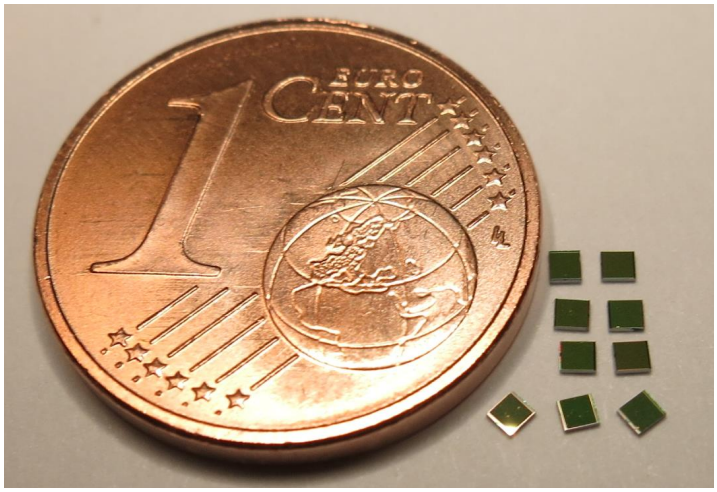


Figure 3.67: OC3 dimensions (1 mm x 1 mm x 0.3 mm) compared to a one euro cent coin.

R_{chip} models the chip that carries the tag EPC. C_{para} represents the parasitic capacitive coupling between the top metal layer and the silicon substrate. C_{para} has a value of about 5 pF and plays a decisive role due to reading performance. The two capacitors C_1 and C_2 model the capacitive coupling between the OC3 tag and the reader. Their values can be determined by

$$C_{\text{i}} = \varepsilon_0 \varepsilon_{\text{r,i}} \frac{A}{d_{\text{i}}}, \tag{3.4.1}$$

where i = (1, 2), $A = 1\,\text{mm}^2$ is the area size of the OC3 tag, d_{i} is the distance between the chip and reader electrodes or rather the reading distance, $\varepsilon_{\text{r,i}}$ is the relative permittivity of electrode environment, and $\varepsilon_0 = 8.854\,\text{pF/m}$ is the vacuum permittivity. Equation 3.4.1 shows that C_{i} decreases significantly by increasing the reading distance.

Figure 4.38 shows the measurement setup to experimentally validate the realized OC3 RFID tag. The tag is placed between two reader electrodes. These electrodes can be implemented by any metal object. In the measurement setup shown in Fig. 4.38, the bottom reader electrode is realized by a 5 cent euro coin, while the top reader electrode is realized by a small metal plate. Thus, the OC3 RFID tag is well suited to tag metal objects (e.g., coins, metallic coffee capsules, or jewelry). The reader electrodes are connected via tuners to an OBID Feig UHF and HF reader [78]. The tuners are used for power matching and voltage magnification between the 50 Ω reader input impedance and the OC3 tag and reader electrode setup. Figure 3.69 shows a picture of the measurement setup.

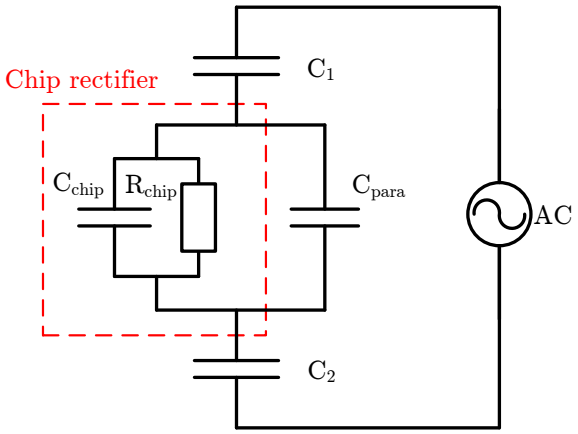


Figure 3.68: Equivalent circuit of the communication system: The combination of the OC3 tag with the reader acts as a capacitive voltage divider consisting of the two capacitances C_1 and C_2 that model the capacitive coupling between the tag and the reader, C_{chip} and R_{chip} characterize the chip, and C_{para} models parasitic capacitive coupling effects. C_{chip} and R_{chip} are predominantly characterized by the chip rectifier.

First test: One coupling surface

In a first test, the maximum reading distance of the OC3 tag was measured by varying the distance d_1 of C_1 (see Eqn. 3.4.1). The electrode environment of C_1 is air with an $\varepsilon_{\text{r},1} = 1$. For the test, the OC3 tag was mounted directly onto the 5 cent euro coin leading to $C_2 \to \infty$, i.e., there is no voltage drop across capacitor C_2. For each distance the impedance transformation, realized by the tuner, was adjusted. Indeed the coupling mechanism is non-resonant. Nevertheless the impedance transformation by the tuner as well as serial resonating circuits performed by booster antennas (OC3 booster antennas: presented in chapter 4.2), allow high voltages at the electrodes. This voltage magnification effects enable the power supply of the chip rectifier (see Figure 3.68)

The EPC of the OC3 tag was detected for a maximum reading distance of $d_1 = 200\,\mu\text{m}$ at 13.56 MHz and 400 μm at 868 MHz. The measurement results show that the energy transfer to the OC3 tag is more efficient in the UHF band. The reason for this is the high reactance of the capacitors at HF in comparison to UHF: The impedance of the OC3 is voltage dependent. The shunt-resistor terminates the signal to 2.8 V. As already described, this is realized by a large transistor (see Figure 3.64) varying between 40 Ω and 8 kΩ. If the OC3 is seen as ideal varying ohmic device without parasitic capacitors, just the impedance of the coupled electrodes is frequency dependent (see Figure 3.68 C1 & C2). Calculation 3.4.2 shows that the impedance/reactance of the generated capacitor is 64 times higher at HF than in UHF. Thus, the energy transfer to the OC3 is more efficient in the UHF band. Therefore the reading distance at UHF could be 64 times higher than in HF. However, the parasitic components C_{chip} and C_{para} decreases the

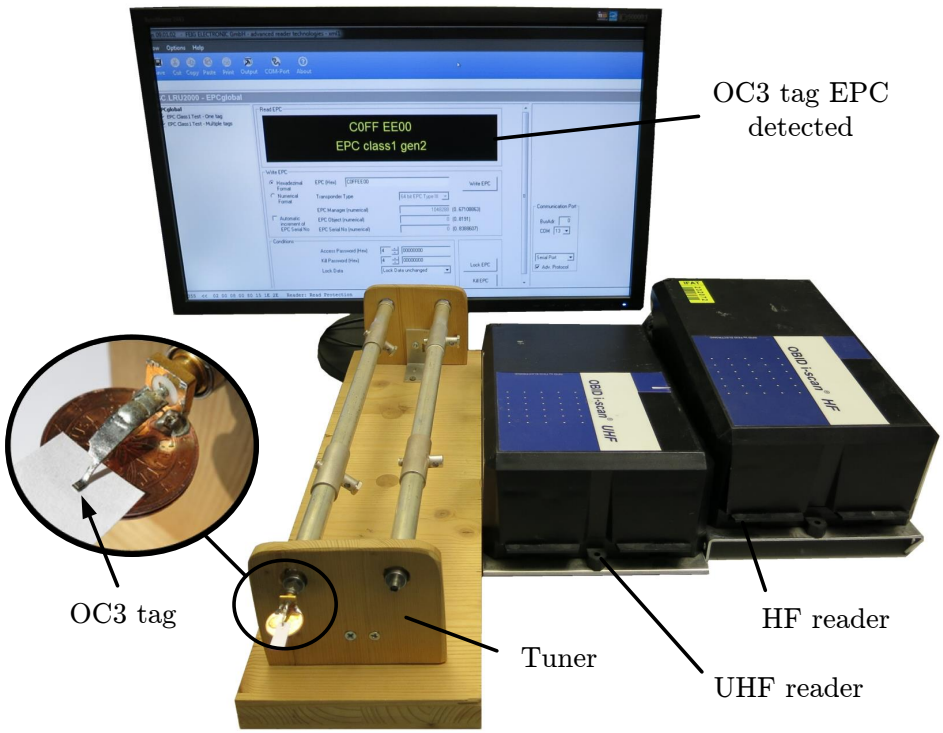


Figure 3.69: Picture of the measurement setup: The screen in the back shows that the OC3 tag EPC (C0FFEE00) is correctly received by the reader. The measurement setup includes the OC3 tag, the tuner, the HF reader, and the UHF reader. The arrangement of the OC3 tag and the reader electrodes is detailed in Fig. 4.38.

theoretical reading distance significantly, as it can be seen in the measurements. The more the reading distance gain increase by frequency, the more it suffers from parasitic capacitors that shorten the rectifier. The parallel capacitor is generated by the stacked metal arrangement of the OC3. As it is illustrated in Figure 3.70, C_{para} is increased by additional chip metals. The used CMOS process uses seven chip metals that are separated by oxide layers with a permittivity of $\varepsilon_{\text{oxide}} = 4.1$. Thus the parallel parasitic capacitor can be calculated to 4.9 pF, by sum all parasitic elements. In general the parasitic elements should be minimized. Although it is not possible to reduce the value of the parasitic capacitor significantly due to the stacked arrangement of the coupling mechanism.

$$\frac{Z_{UHF}}{Z_{HF}} = \frac{-j \cdot \frac{d}{2 \cdot \pi \cdot 868MHz \cdot A \cdot \varepsilon_0 \varepsilon_{\text{r,i}}}}{-j \cdot \frac{d}{2 \cdot \pi \cdot 13.56MHz \cdot A \cdot \varepsilon_0 \varepsilon_{\text{r,i}}}} \approx \frac{1}{64} \tag{3.4.2}$$

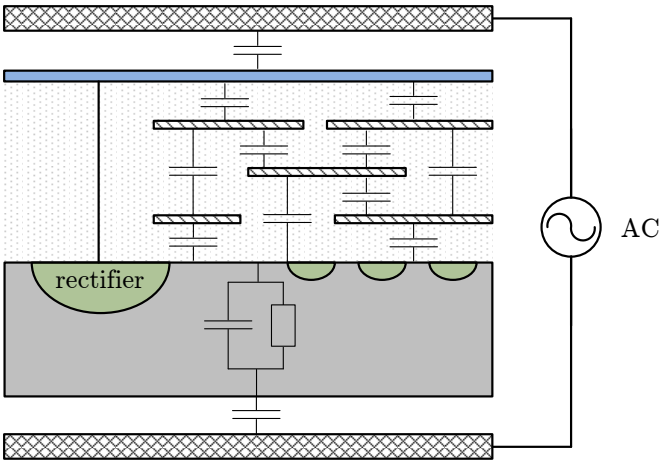


Figure 3.70: Overall OC3 RFID system. The top metal (blue) is connected directly with vias to the rectifier. Due to the stacked arrangement of the top metal surface and the well conductive substrate a parasitic capacitor C_{para} is generated (see Figure 3.68). Additionally this capacitor is increased by other chip metals that shorten the gap between top metal and substrate. The oxide (layer between chip metals) of the used CMOS process has a permittivity of $\varepsilon_{\text{oxide}} = 4.1$. Thus the parallel parasitic capacitor can be calculated to 4.98 pF

Second test: Two coupling surfaces

A second test demonstrates the whole capacitive coupling mechanism of the setup. This test is realized by adding a sheet of paper between the coin and the OC3 tag. This setup leads to $C_2 = 170\,\text{fF}$ (see Eqn. 3.4.1 with $d_2 = 100\,\mu\text{m}$ and $\varepsilon_{\text{r},2} = 2$). A successful HF and UHF communication was established for reduced maximum reading distances of $d_1 = 100\,\mu\text{m}$ at 13.56 MHz and $300\,\mu\text{m}$ at 868 MHz. The reason for the reduction in reading distance in comparison to the first test is the additional voltage drop across C_2.

Summarizing, this section presents a highly miniaturized RFID tag that communicates with the reader by means of a non-resonant capacitive coupling mechanism. So far, small RFID tags are typically equipped with on-chip antennas implemented as highly miniaturized coils that communicate with the RFID reader based on inductive coupling [66, 73, 108]. In contrast to these tags, the coupling mechanism of the presented OC3 tag is non-resonant and thus allows multiple operating frequencies, e.g., at 13.56 MHz and 868 MHz. Additionally, the manufacturing costs of an OC3 tag are reduced in comparison to tags with on-chip coils. A futher benefit of the OC3 tag is the suitability to tag metal objects such as coins, metallic coffee capsules, or jewelry.

A summary of improvements and capabilities of the presented novel chip coupling

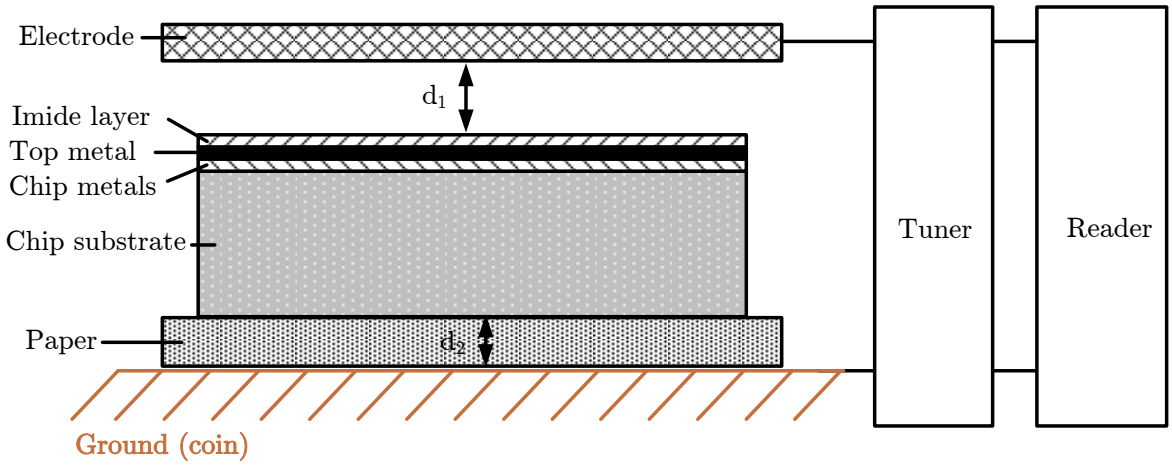


Figure 3.71: Measurement setup for the experimental validation of the OC3 tag: The OC3 tag is tested with an RFID reader at HF and UHF frequencies. The top reader electrode is realized by a small metal plate, while the bottom reader electrode is realized by a 5 cent euro coin. The coupling distance d_1 is defined by a sheet of paper with a thickness of about 100 μm. The matching between the 50 Ω reader input impedance and the setup of the OC3 tag and reader electrodes is realized by a tuner.

mechanism is given by following list:

+ **Reduced area/costs:** Inductive coupled coil antennas consist of a number of windings. These windings are often stacked with several chip metals. Moreover metal layers have to be merged with long vias, to reduce the resistance and to achieve the specified coil quality factor. The presented capacitive coupling mechanism does not need more than one metal layer. The last chip metal is used as capacitive coupling surface. This method allows a independent chip design without any limitations.

+ **Frequency independent:** The capacitive coupling mechanism allows a non-resonant communication. In case of capacitive coupled multi-band RFID transponders, the particular reader setup allows a communication with different frequency bands.

+ **Robustness:** In contrast to resonant coils, the capacitive coupled solid metal surface allows a high level of robustness. While scratches or any other damage to the coil and its coil-tracks will break down the RFID tag functionality the capacitive coupling performance will not be influenced significantly.

+ **Shielding:** The solid metal surface on the top of the RFID chip provide additional protection and shielding. Due to the metal surface, logic arrays as well as analog

parts are less influenced by the chip environment.

+ **Applicable in metal environment:** In contrast to a inductive coupled system that becomes inefficient in applications with metal environment, the metal benefits the capacitive coupling mechanism. Moreover as it is shown, metal objects can be used as reader electrodes.

– **Reading distance:** The reading distance as well as the wireless power transfer suffers from the capacitive coupling mechanism. As it is shown the performance is related to the operation frequency and geometrical dimensions of the RFID tag.

A main drawback of the OC3 tag is its limited reading distance in comparison to small RFID tags based on inductive coupling. The experimental validation of the OC3 tag shows that its maximum reading distance is limited to 200 μm at 13.56 MHz and 400 μm at 868 MHz. However, this drawback can be eliminated by the use of booster antennas, that are presented in chapter 4.2.

3.4.4 Applications

The OC3 enables new capabilities. As presented, small metal objects can be tagged due to the novel and innovative coupling mechanism. Indeed the stacked arrangement of the coupling surfaces reduce the possible reading distance as it is described and illustrated in Section 3.4.3. Nevertheless there are novel application possible that take advantage of this concept. One example is given by Figure 3.64. A coffee capsule is usually made of aluminum. As it is illustrated, the coffee machine capsule fixture can be used as two separate electrodes. Then, this system can be used to read out the OC3 tagged coffee capsule information. This information could comprise date of sale, flavor and origin. Furthermore branding is possible. Additionally the information could be used by the machine for adequate coffee preparation (e.g. brew temperature).

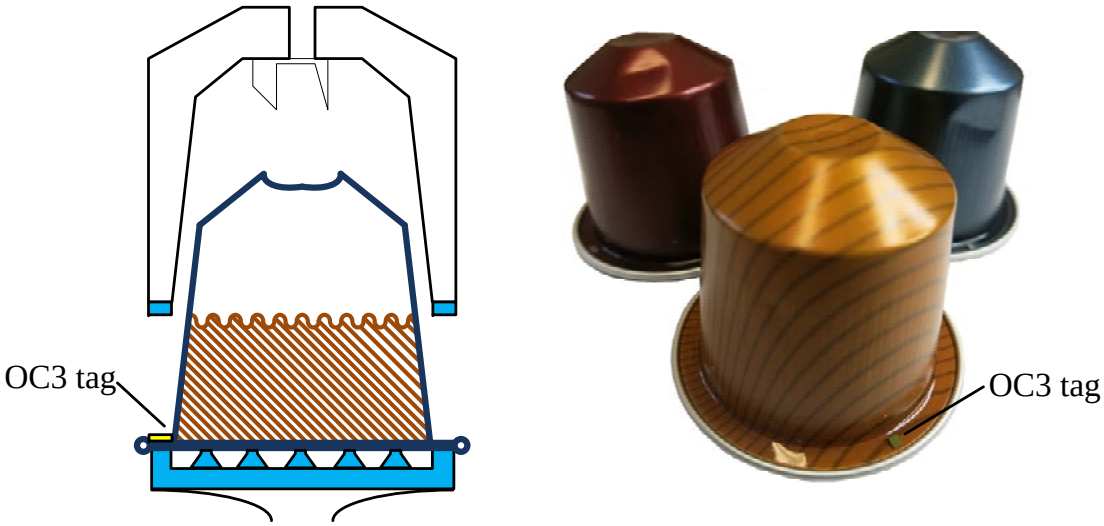


Figure 3.72: Exemplary application sczenario: OC3 RFID tags enables the possibility to tag and identify small metal objects, e.g., coffee capsules or jewelry

Chapter 4

Passive Boosting Technologies

This section deals about antenna boosting technologies. Due to the small structures of the presented RFID transponders (see section 3), the performance and reading distance of the tags are limited. Moreover the particular miniaturized RFID tag is forced to operate in combination with the special designed reader equipment, e.g. small reader antennas or electrodes. As it is shown in section 3, the communication channel of these tags is either the magnetic field or the electric field. Due to the fundamental limits and boundaries of small antennas (see Wheeler [109]) the presented transponders are suited with non-radiating antennas. In other words, wave propagation is not feasible.

Nevertheless this section presents novel antenna add-ons, so called booster antennas to get rid of these limitations. This technology enables a parameter transformation by increasing the effective area of a small antenna to a larger area. Thus, performance and reading distance can be increased significantly. Different types of booster antennas enable the possibility of electromagnetic wave propagation, beam forming, increased coupling coefficient, antenna parameter conversation, and many more. A simplification of the booster antenna concept is illustrated in figure 4.1. As it is shown a booster antenna can be seen as a funnel. Seen from the perspective of the miniaturized RFID tag up to large reader systems it can be said, that a booster antenna extends the effective area of a small antenna to a larger area. Seen from the geometrically larger side down to the small RFID tag, it can be also said, that the booster structure concentrates the available field energy to a single small hot spot. As the name passive boosting technologies suggests no active or amplifying components are used.

Similar to the funnel, shown in figure 4.1, a booster antenna consist of two main, geometrically different parts. A large pickup antenna, that is used to collect an amount of field energy and a very small coupling structure, that is used to focus the collected energy to a small hot spot. In general the coupling structure is realized as a counterpart of the particular miniaturized transponder system. Thus an efficient power transfer can be provided. For example, if the small tag is suited with an inductive coupled coil, the coupling structure of the booster antenna is also designed as a coil. The larger part of the booster antenna, the so called pickup antenna, can be realized as any known antenna type. Thus, booster antennas can be categorized into two main classes: Inductively and capacitively coupled booster antennas. The first classification, shown in figure 4.2, is done

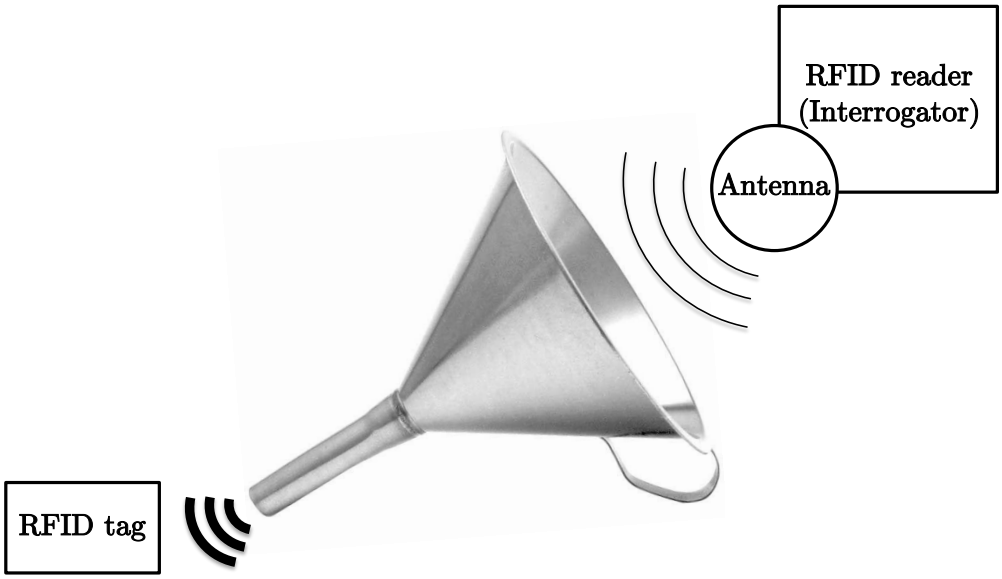


Figure 4.1: A booster antenna acts like a funnel: It extends the effective area of a small antenna to a larger area. In other words: A booster antenna concentrates the field energy to a single small hot spot

by the different smaller part of the booster antenna; the two types of coupling structures. If the coupling structure is realized as a coil, it uses the magnetic field and inductive coupling to communicate with the miniaturized RFID tag. If it is realized similar as a capacitor, with two electrodes, it uses the electric field and capacitive coupling as a communication channel. Due to the large pickup antenna of the booster structure, this two categories can be further split. While the dipole represents an wave propagating electromagnetic antenna, the large coil describes a near field inductive coupled booster system. Both antenna types can be realized in combination with inductive and capacitive coupled RFID tags. Therefore all in all four booster antenna categories can be defined (see figure 4.2). Note that these categories are frequency independent. Theoretically, each antenna type can be realized at the particular frequency band.

Compared to standard RFID transponders, booster antennas provide more advantages than just increasing the reading distance. In following all additional benefits are listened:

+ **Increased reading distance:** As it is shown in examples, booster antennas are able to increase the reading distance from *µmeter* to *meter*.

+ **No galvanic contacts:** In contrast to conventional RFID transponder there is no need for bonding, soldering or any flip chip technology. The chips are connected by a non-galvanic coupling mechanism.

+ **Increased robustness:** Bonding wires and any other galvanic contact to the RFID chip are very susceptible. Depending to the application, bending stretching etc. can easily destroy the RFID transponder. In contrast, a non-galvanic coupling mechanism is indestructible.

+ **Easy assembly process:** The step to connect the RFID chip to the particular antenna can be skipped. To produce a booster antenna system in combination with a miniaturized RFID transponder, the RFID chip is simply mounted onto the designated coupling structure.

+ **Reduced fabrication costs:** Due to the simplification of the assembly process, the costs to produce a booster antenna systems are reduced.

+ **Less electrostatic discharge protection:** The non-galvanic coupling structure has filter capabilities. Thus the chance of electrostatic discharges to the sensible RFID chip is reduced significantly.

+ **Individual antennas for one (chip-)product:** While the chip manufacturer provides the miniaturized RFID tag, the customer is able to design his own booster antenna. Depending to the application, a individual booster antenna can designed.

− **Decreasing performance :** Unfortunately the non-galvanic coupling mechanism provides an additional communication path and therefore losses. Compared to directly connected RFID transponders, the performance of the booster antenna system is slightly decreased.

Beside different types of passive booster antenna structures this section also describes the possibilities of boosting material, such as ferrite, to modify and manipulate antenna parameters. The performance of some RFID transponders can be easily deteriorated by any metal environment. Ferrite is able to shield these negative effects at certain frequencies. Therefore ferrite can be also seen as a passive boosting material.

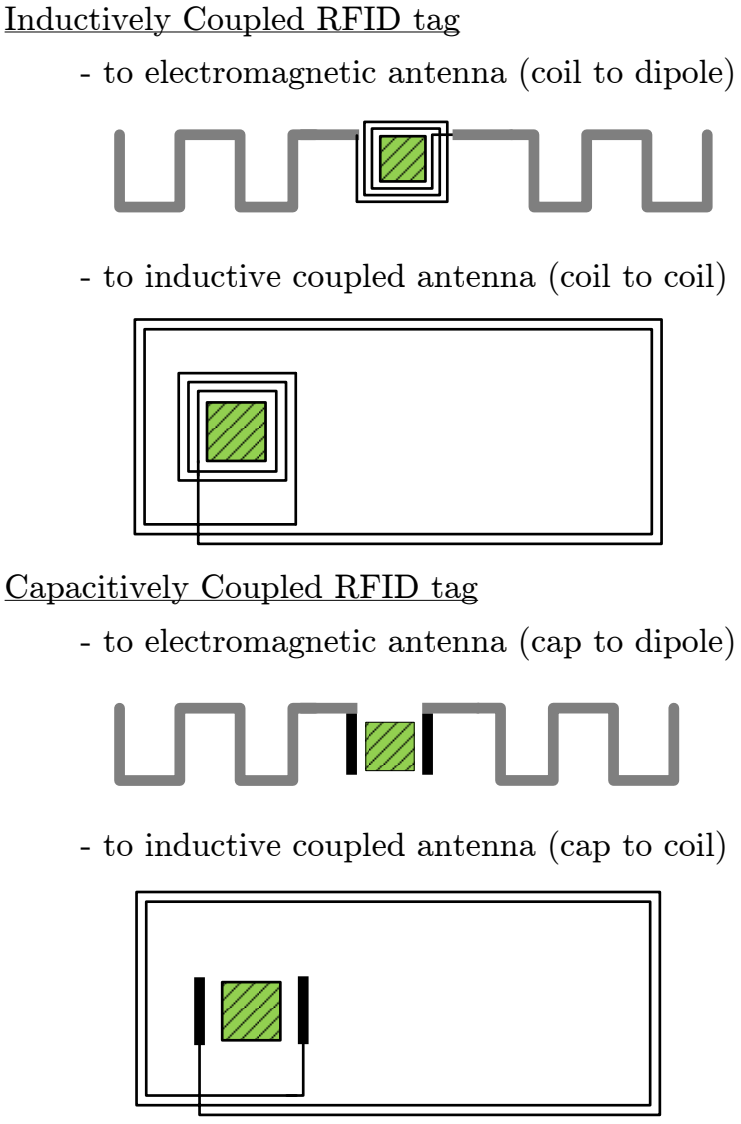


Figure 4.2: Four booster antenna categories: The main categorization is done by the two different coupling structures: inductive (with a coil) and capacitive (with electrodes) coupling to a small RFID tag. The larger part of the booster antenna can be any known antenna structure. Nevertheless it can be divided into two parts: The near field coupled coil antenna and the wave propagating dipole antenna.

4.1 Inductively Coupled Booster antennas

This section presents the booster antenna technology in combination with inductively coupled RFID tags. To illustrate the outstanding inductive coupled booster capabilities, two additional types of highly miniaturized RFID tags are introduced. A one square millimeter HF- (see figure 4.3) and UHF (see figure 4.4) RFID Tag. The centerpiece and core of these tags is already presented in section 3.3. Similar to 3.3, both types are suited with an on-chip-coil and fabricated in a low cost 130 nm CMOS process. To illustrate the high level of miniaturization the chips are compared to the size of a bee (see figure 4.5). Due to the inductive near field coupling mechanism the reading distances of both types are limited (millimeter range). However, the presented booster antennas are able to increase the reading distance significantly (meter). Moreover, as it will be shown in this section, the inductive coupled booster technology enables novel capabilities. While HF booster antennas can be used to power implanted sensors, the UHF technology enables the possibility to produce robust and ultra low cost UHF RFID tags.

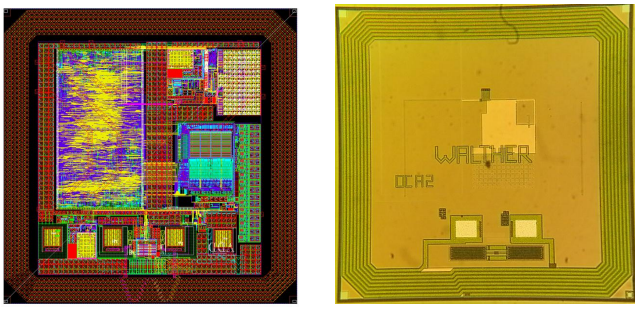


Figure 4.3: HF version of the RFID tag presented in section 3.3: In order to obtain a high inductance, eight on-chip-coil windings are arranged upon each other over five different chip metal layers. Thus the RFID tag is able to operate at the resonating frequency of 13.56 MHz.

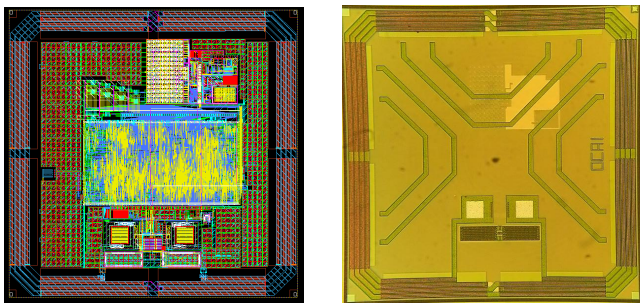


Figure 4.4: UHF version of the RFID tag presented in section 3.3: The UHF RFID tag is suited with a four winding coil, that is complex conjugate matched to the input impedance of the chip.

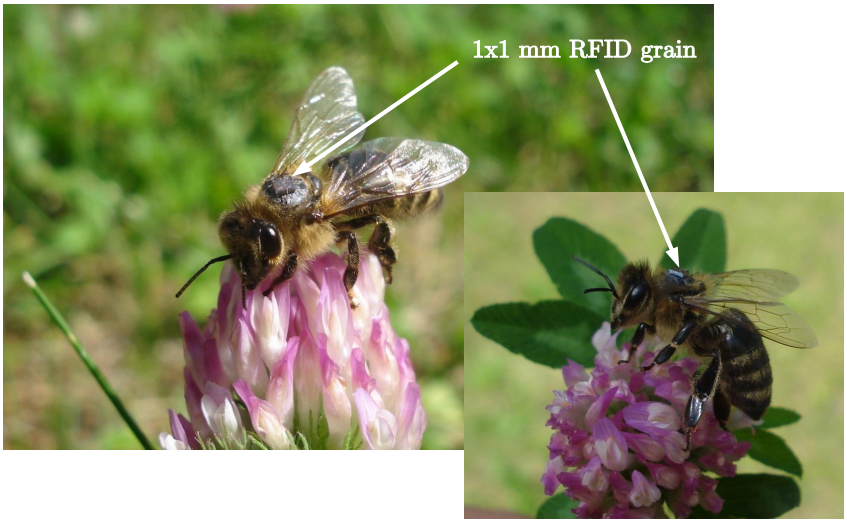


Figure 4.5: The size of the presented one square millimeter RFID grains compared to a bee. The UHF version was used to detect the bee in front of the beehive. (see [80]

4.1.1 Coil to Coil

This work presents a novel passive RFID booster technology to significantly increase the reading distance of small HF RFID Tags. Therefore, a one square millimeter RFID Tag with an on-chip-coil is designed and fabricated in a low cost 130 nm CMOS process (see figure 4.3). In order to obtain a high inductance, the on-chip-coil windings are arranged upon each other over five different chip metal layers. Depending on the environment, the proposed booster antenna is able to increase the reading distance of this small RFID tag from two millimeter up to more than one meter. This technology offers new possibilities in the field of human health monitoring. While the small RFID tag can be used as implanted sensor node, the presented booster antenna is realized in the form of a plaster to increase the reading distance of the in-vivo device. Reading out a blood sugar value with an NFC (Near Field Communication) mobile phone is just one of many future applications.

Considering the inventions and developments in the field of small biomedical sensors, such as measuring the blood pressure, heart beat, continuous glucose monitoring [42], or a simple temperature measurement, it is obvious that these technologies will be transferred to the human body in future in order to facilitate our life. Having a look at the current market situation, it is also evident that such in-vivo diagnostic devices already inroads into our life. The wireless communication and power transfer to such implanted devices is well researched [28] and quite similar to the well-known RFID technology. Typically the implanted device is equipped with a receiver coil. This coil is magnetically coupled to the reader device which is outside of the body. Due to the misalignment and different sizes of these two separated coils the coupling coefficient can be very small. The reader coil has to be attached very precisely and close to the body to increase the coupling coefficient. Nevertheless enough energy can be transferred, for low power applications, e.g. temperature measurements.

In following, this work simulates such applications with an additional improvement: The coil-to-coil booster antenna. The presented system uses the 13.56 MHz frequency band in order to provide a sufficient power transfer. To illustrate a very small implanted sensor node, a one square millimeter RFID transponder (see figure 4.3) is deployed.

Original Publication Related to this Section

Pachler, W., W. Bosch, G. Holweg, and G. Hofer., "A novel booster antenna design coupled to a one square millimeter coil-on-chip RFID tag enabling new medical applications." In: Microwave Conference (EuMC), 2013 European. Oct. 2013, pp. 1003–1006.

Miniaturized HF sensor tag

The centerpiece of the proposed RFID tag is already presented in section 3.3. According to [94] its sensitivity is below −11.4 dBm. The size of this fully EPC (Electronic Product Code) Gen2 [102] compatible passive RFID transponder is less than one square millimeter. Thus the on-chip-coil is designed very small to illustrate a possible implanted diagnostic device. Additionally, the tag is equipped with a temperature and shunt-value sensor. The design of a very small coil-on-chip antenna at a resonating frequency of 13.56 MHz is challenging. High values for inductance and capacitance are needed. To maximize the inductance per area, the coil windings are arranged upon each other. To achieve this requirement, five different metal layers with eight windings each are used. Similar to the coil-on-chip design example, shown in section 3.3, the resistance of the different chip metals is rather high. Nevertheless there is the possibility to combine chip metals with special long vias to get a better conductivity. Due to the small size of the on-chip-coil, the reading distance of the RF tag is only around two millimeter.

Novel coil-to-coil booster antenna concept

State of the art HF booster antennas use the already described geometrical booster effect to increase the reading distance to small devices. Such HF booster antennas transform the antenna of small sized devices, e.g. a coil on chip, to a bigger structure in order to increase the coupling coefficient to the reader. One state of the art HF booster antenna application is deployed in common credit cards. This patented concept (see [32]) increases the reading distance of the credit card module. Thus, the card performance is almost the same as it is with standard "connected" RFID capable ID-1 cards.

The patented antenna (see [32]) is built as a simple serial resonance circuit, resonating at the operating frequency. As shown in figure 4.6a, the inductance of this circuit is divided into two parts. The antenna "aims" to boost the magnetical field collected by the bigger part of the inductance L_{S1} to the small one L_{S2}. Because of the little distance between the smaller part of the inductance and the small HF tag, the coupling coefficient is very high.

In this work, a novel HF booster antenna is presented. Beside the mentioned geometrically booster effect this booster antenna uses an additional electrical effect, to boost the magnetic field and to perform a impedance transformation.

As it can be seen in 4.6b, the design of the antenna includes a serial and a parallel resonant circuit. In contrast to the state of the art booster antenna (see 4.6a), the coupling structure as well as the pickup coil can be seen as independent resonating circuits. Both of them are tuned to the operation frequency of 13.56 MHz. The presented novel design provides several advantages:

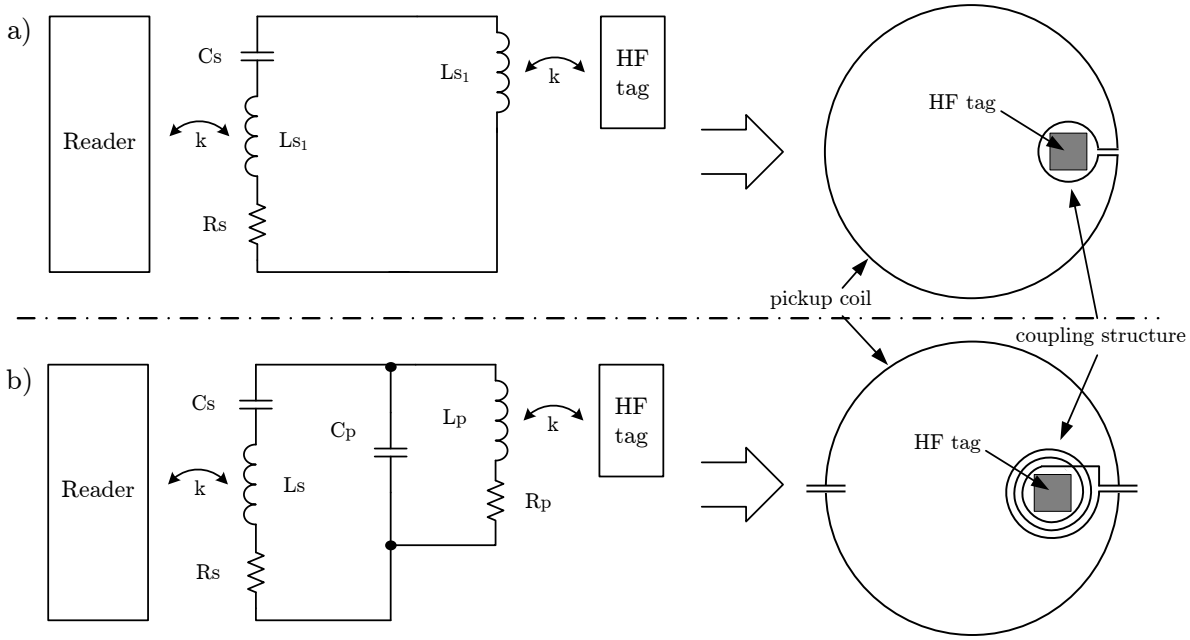


Figure 4.6: a) Conventional HF booster antenna for small HF devices b) novel HF booster antenna.

+ **Current magnification:** In contrast to the serial resonating circuit, the additional parallel resonating circuit causes a current magnification. Therefore the strength of the induced magnetic field in the area of the coupling structure can be increased.

+ **No limitation to the inductance value:** Due to the state of the art serial resonating booster antenna, there is just one resonating inductance value available, namely L_S. It is divided into L_{S1} and L_{S2}. As it can be seen the values are limited. In case of two separated resonating circuits (novel concept), the design and inductance of the coupling structure as well as for the pick up coil can be individual. Thus it can be easily adjusted to the particular application.

+ **No additional resistance to decrease the loading effect** In general, state of the art booster antennas decrease the unwanted loading effect to the reader, by increasing the booster antenna resistance R_S. Thus the quality factor of the serial booster antenna is reduced. Usually this is realized by meandering the wire or changing the used material into a more resistive material. Certainly, a higher real part resistor causes additional losses. However, a parallel resonating circuit has a maximum real part resistance at the operation frequency. Therefore there is no need to increase the resistance in the pickup coil anymore.

+ **No Load modulation amplitude transformation:** The state of the art serial resonating booster antenna transforms high impedances into low values and vice versa. Indeed, the reader structure does not care about the direction of impedance

changes - the signals will be detected anyway. However, by the use of two resonating circuits of the presented novel solution, the transformation is done twice. Thus the tag acts similar as a directly connected tag.

As in the first example, a current is induced in the bigger structure of the antenna -the serial resonance circuit. This current drives the smaller coupling structure -the parallel circuit, which creates a compact magnetic field. Due to the effect that a parallel resonant circuit provides current magnification, the strength of the magnetic field in the area of the coupling structure can be increased. In the first design step, the coupled circuits can be neglected, since the influence of the bad coupled circuits (miniaturized RFID tag and reader) is weak anyway. The phase resonant frequency of the two separate circuits and thus the values of each electrical part can be calculated.

Design example

The size of the presented booster antenna is 80 mm x 50 mm representing the size of a standard ID-card. Two external capacitors are added, to complete the respective resonant circuits which are already described. An alternative solution requires no external components. A capacitance can also be realized with a proper layout. Figure 4.7 shows the layout of the proposed booster antenna.

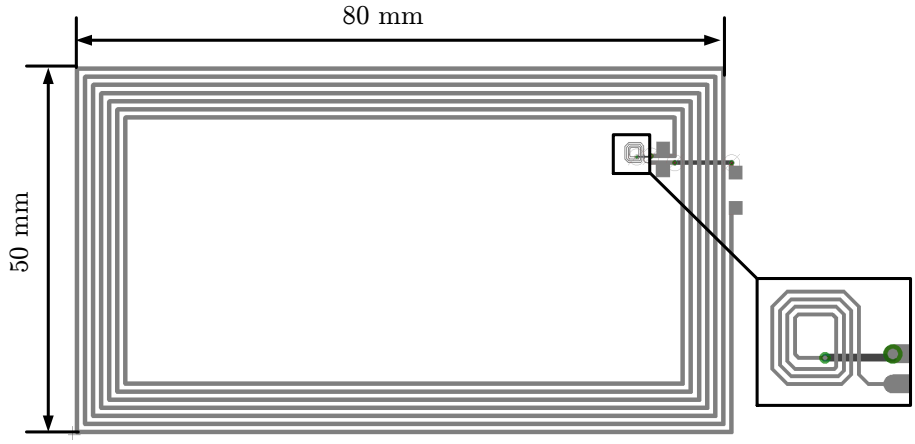


Figure 4.7: Layout of the purposed booster antenna: The seven winding coil has a track width and track space of 5 mm. The track with and space of the four winding coupling structure (highlighted) is 100 μm

The values of the proposed booster antenna, which is shown in 4.6b, are $Rp = 0.9\,\Omega$, $Lp = 35.08\,\mu$H, $Cp = 3.6E$ nF, $Rs = 4.9\,\Omega$, $Ls = 4.2E\,\mu$H and $Cs = 32.79E$ pF. The following observation just describes the booster antenna itself and no coupled circuits. Considering the issue that the energy is coupled into the big coil of the booster antenna,

a voltage source can be placed after L_S. Thus the impedance $\underline{Z}$ of the booster antenna can be calculated with 4.1.1.

$$\underline{Z} = R_S + \jmath\omega L_S - \frac{\jmath}{\omega C_S} + \frac{1}{\frac{1}{\jmath\omega L_P + R_P} + \jmath\omega C_P} \tag{4.1.1}$$

The numeric calculation of the phase resonant frequencies and additionally the locus curve show that three resonance frequencies are possible. Equation 4.1.1 shows that the imaginary part of the antenna's impedance has three solutions for ω (cubic function). If the quality factor of the parallel circuit (equation 4.1.3) is much smaller than the serial circuit (equation 4.1.2), only one solution exists.

$$Q_s = \frac{|X_{L_S}|}{R_S} = \frac{|X_{C_S}|}{R_S} = \frac{1}{R_S} \cdot \sqrt{\frac{L_S}{C_S}} \tag{4.1.2}$$

$$Q_p = \frac{R_P}{|X_{L_P}|} = \frac{R_P}{|X_{C_P}|} = R_P \cdot \sqrt{\frac{C_P}{L_P}} \tag{4.1.3}$$

A closer look to the locus curve

Figure 4.8 shows the well-known impedance curves of the parallel resonating circuit, the serial resonant circuit and the combination of both which is realized by the HF booster antenna. At high frequencies the serial resonant circuit is dominant ($\omega = \infty$). Here, the impedance simply consists of the resistor $R_S = 4.9\,\Omega$, since the capacitor of the parallel circuit acts as a short circuit. The parallel resonate circuit gains influence with decreasing frequency. At the special resonant frequency where the inductance and capacitance cancel each other the imaginary part of the resonating system is zero $Z = R_S + R'_P$. R'_P is the equivalent parallel resistance and is defined in the next section. If the frequency further decreases, the real part of the parallel resonant circuits becomes smaller, and the resistances of the two coils dominate. Whether the quality factor of the parallel resonant circuit increases (for example $R_S = 0.1\,\Omega$), the parallel resonant circuit gets more influence to the system and the three mentioned solutions for the phase resonance appear. Anyway, there is just one solution interesting: $f_r = 13.56\,\text{MHz}$.

Current magnification in the coupling structure

In following a simplification is used to present the magnification feature: If the quality factor of the parallel circuit is high, the circuit can be easily replaced by an equivalent parallel circuit. This is illustrated in figure 4.9. The new values for R'_P and L'_P can be calculated as shown in 4.1.4. L'_P is calculated with the inverse of the susceptance (see equation 4.1.6); R'_P is calculated with the inverse of the conductance in equation 4.1.4 (see equation 4.1.5).

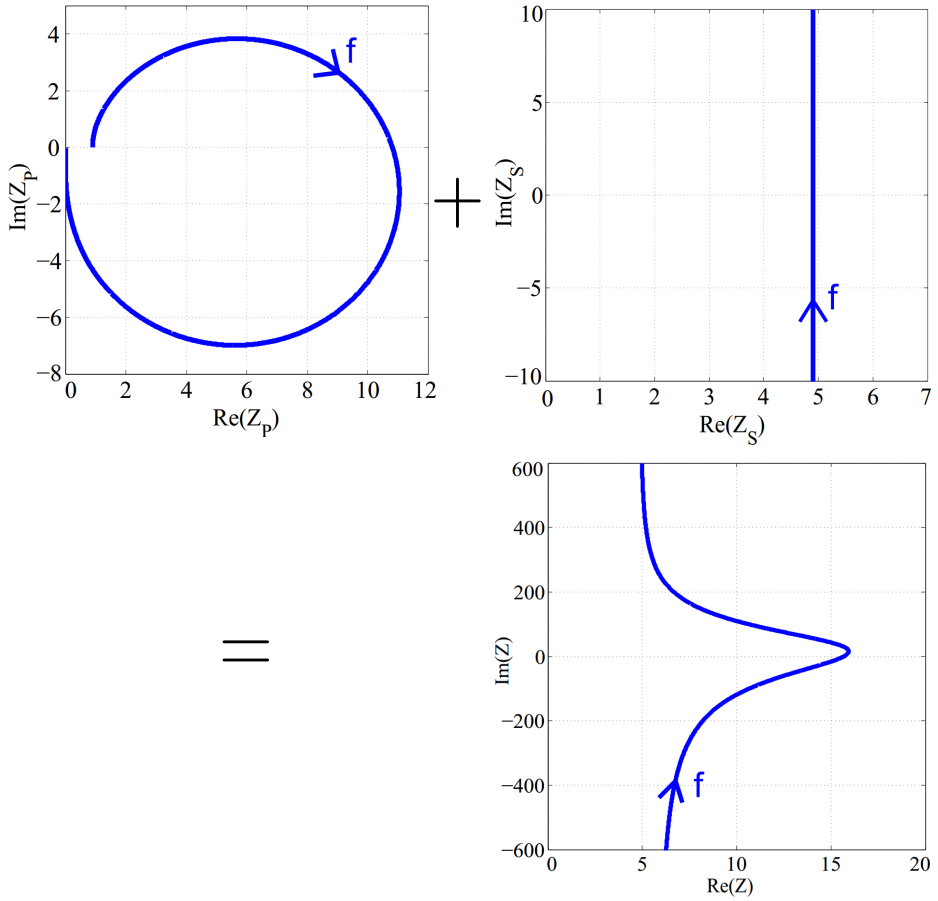


Figure 4.8: Impedance locus of the presented RF booster antenna. It consists of a combination of a standard parallel and serial resonating circuit lotus curve.

$$\underline{Y} = \frac{R_P}{R_P^2 + (\omega L_P)^2} - \frac{\jmath \omega L_P}{R_P^2 + (\omega L_P)^2} = G + \jmath B \tag{4.1.4}$$

$$R_P^{'} = \frac{1}{G} = \frac{R_P^2 + R_P^2 \cdot (\frac{\jmath \omega L_P}{R_P})^2}{R_P} = R_P \cdot (1 + Q_P^2) \tag{4.1.5}$$

$$L_P^{'} = \frac{1}{B} = \frac{\frac{R_P^2}{\omega L_P} + \omega L_P}{\omega} \tag{4.1.6}$$

The current magnification in a parallel resonant circuit depends on the quality factor. A higher quality factor causes a higher current between inductance and capacitor. Additionally, the maximum currents are shifted by frequency. The resulting frequencies can be calculated with equation 4.1.7.

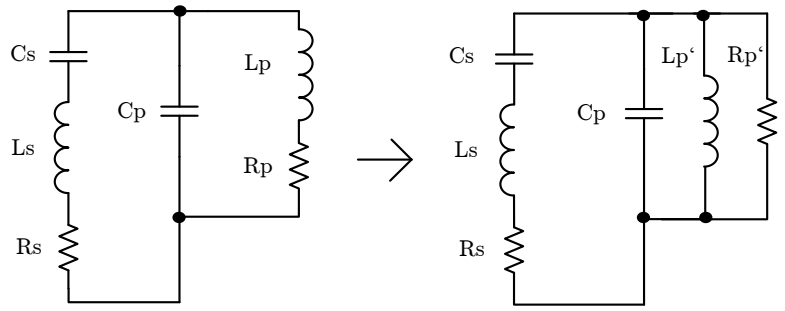


Figure 4.9: Due to the high quality factor of the parallel circuit, the circuit can be easily replaced by an equivalent parallel circuit.

$$\omega_{Imax} = \frac{1}{\sqrt{L'_P \cdot C_P}} \cdot \sqrt{1 - \frac{L'_P}{2 \cdot C_P \cdot R_P^2}} \tag{4.1.7}$$

If the quality factor is high enough the shifting effect decreases and is negligible. The value of these maximums is approximately equivalent to the multiplication of the current flowing into the parallel resonant circuit and the quality factor. It can be calculated with 4.1.3. The quality factor of the parallel resonating circuit in the presented system is 3.32. The equivalent parallel resistor Rp' is 10.8 Ω.

Figure 4.10 shows the calculated current magnification versus frequency. The current in the parallel resonant circuit is 3.32 times bigger than the current that is induced by the serial resonance circuit. This current causes a magnetic field at the small area of the coupling structure and the small HF RFID tag. This effect also can be seen in simulations illustrated in figure 4.11. The position of the small RFID tag is 2 mm above the booster antenna. Here the coupling factor is still sufficient, because of the similar size of the two coils. Furthermore, as it can be seen in the simulation, the magnetic field strength at this area is concentrated to more than 80 A/m.

Quality factor of the presented booster antenna

The quality factor describes the efficiency of a resonant system. The higher the value of Q, the less energy is wasted due to losses. Therefore, Q is very important and has to be determined for the presented system. Due to the simple single serial resonating circuit, the quality factor of the state of the art booster antenna can be easily calculated with equation 4.1.2. In contrast, the presented novel solution consists of two circuits. Both circuits has to be considered as one system. Q describes the relationship between the energy stored in a system to the loss of energy during one period of oscillation. Thus Q can be calculated with equation 4.1.8.

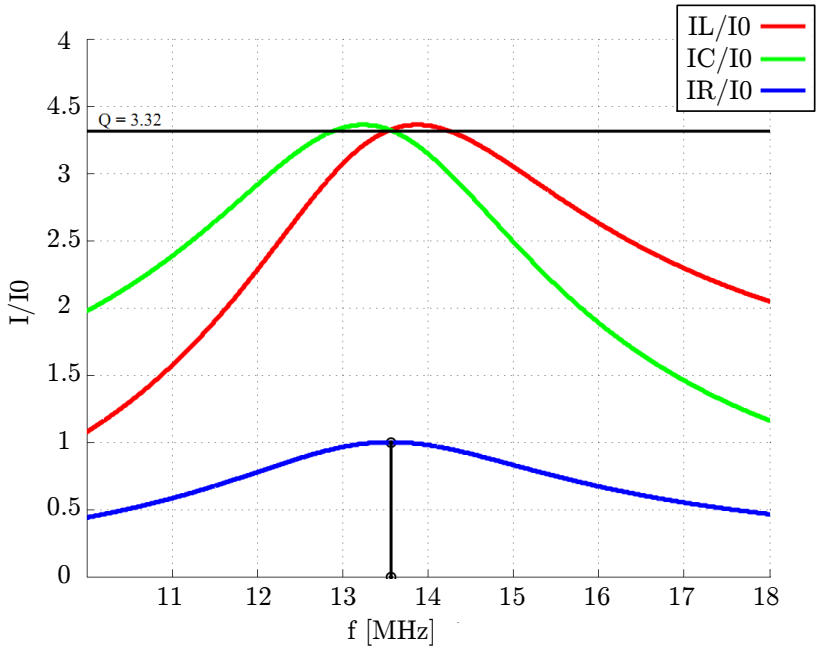


Figure 4.10: Current magnification of the small coupling structure. The current which flows through the small coil is 3.32 times (quality factor) higher than the input current at 13.56 MHz

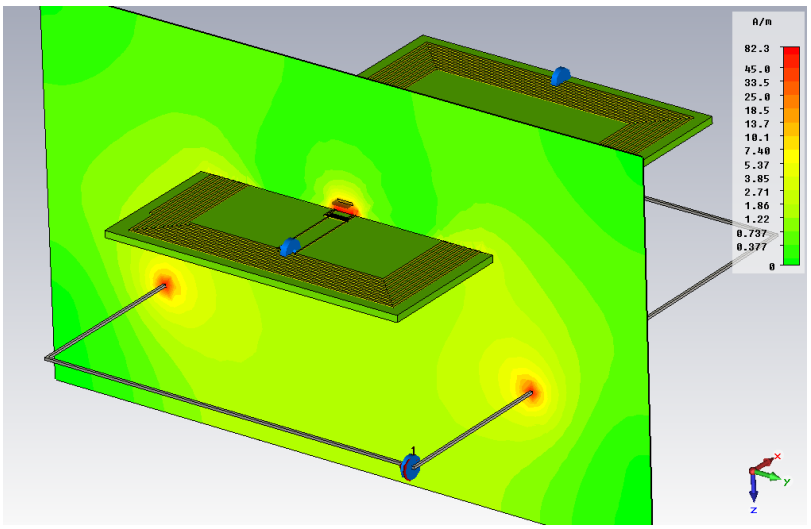


Figure 4.11: H-field simulation in CST-Microwave studio^{TM} [105]. A one loop reader antenna, displaced by 50mm, is powering the proposed booster antenna. It can be seen that the magnetic field is concentrated inside the coupling structure of the booster antenna. Here the one square millimeter on-chip-antenna is placed.

$$Q = \omega \cdot \frac{E}{P} = 2 \cdot \pi \cdot \frac{energy\ stored\ in\ the\ system}{energy\ loss\ per\ period} \tag{4.1.8}$$

To calculate the quality factor the values for energy and the power loss of the systems are needed. As in all resonator circuits, the energy is stored alternately in the inductors and capacitors. In following calculation a point in time is defined where the whole energy is stored in the inductors. Certainly this calculation is also true, if capacitors are taken into account. To calculate and to achieve the maximum available energy, the maximum current has to flow through the inductor. Thus the available energy stored in the system can be calculated with:

$$E_{system} = \frac{1}{2} L_S \hat{i}_0^2 + \frac{1}{2} L_P \hat{i}_P^2 \tag{4.1.9}$$

The losses are determined by all resistors in the system. Therefore the power loss can be calculated with:

$$P_R = \frac{1}{2} \hat{i}_P^2 R_P + \frac{1}{2} \hat{i}_0^2 R_S \tag{4.1.10}$$

The energy is related to power per frequency. Thus the energy loss can be calculated with:

$$E_R = \frac{P_R}{f} = \frac{\pi}{\omega} (\hat{i}_P^2 R_P + \hat{i}_0^2 R_S) \tag{4.1.11}$$

Finally the quality factor of the presented booster antenna concept can be determined with formula 4.1.12. The presented design example has a quality factor of $Q = 23.3$. This result can be also calculated by using the capacitor values in equation 4.1.9.

$$Q = 2\pi \frac{E_{system}}{E_R} = 2\pi \frac{\frac{1}{2} L_S \hat{i}_0^2 + \frac{1}{2} L_P \hat{i}_P^2}{\frac{\pi}{\omega} (\hat{i}_P^2 R_P + \hat{i}_0^2 R_S)} \tag{4.1.12}$$

Device under test

The good performance of the booster antenna is demonstrated by measurements. The measurement setup is shown in figure 4.12. A Feig OBID^{TM} RF Reader [78] is used to read the tag. Its ISO 10373 [49] conform PCD antenna coil is displaced 30 cm below the booster antenna. The small RFID tag is put inside a vessel full of water to emulate human tissue. Due to the one mm vertical space between miniaturized RFID tag and the little coupling structure of the booster antenna, the total reading distance of the overall system decreases. By putting the one square millimeter tag directly onto the

coupling structure, the coupling coefficient reaches an optimum. With this arrangement the reading distance reaches a maximum of one meter with one Watt reader output power.

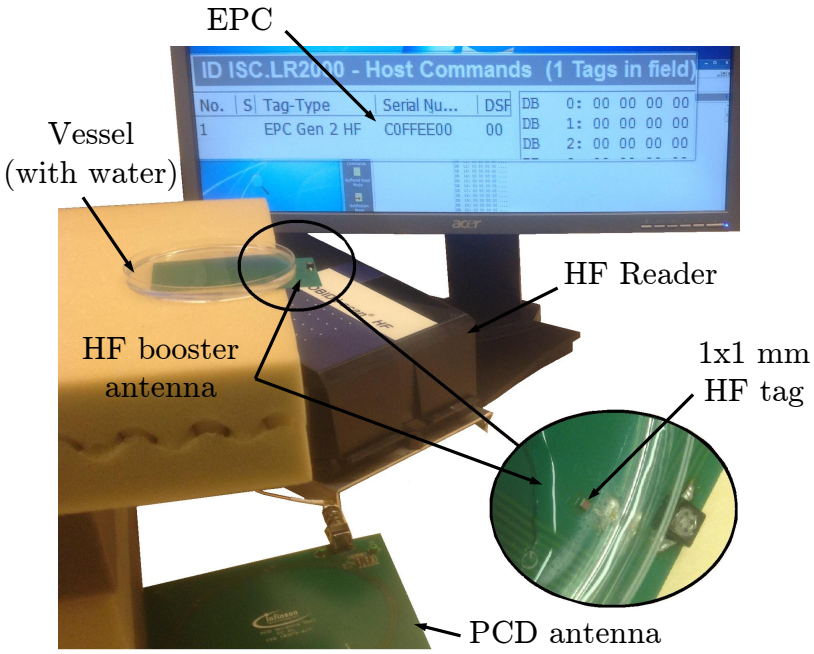


Figure 4.12: Device under test: The booster antenna is powering the one square millimeter RFID tag, which is identified by a reader. The PCD antenna is displaced 30 cm below the booster antenna.

Novel applications

The presented booster antenna can be used as novel, complete passive structure to increase and improve the communication range for small implanted diagnostic devices. As shown in figure 4.13, the booster antenna can be designed as plaster. This plaster can be stuck onto a humans skin, in order to get a sufficient coupling to the implanted diagnostic device. Contrary as in [41], the reader device and its antenna do not have to be placed exactly on a suited position. Furthermore, the reader and its antenna do not have to be close to the body. In this novel application the generated magnetic field is collected by the booster antenna which enables the communication with the implanted device.

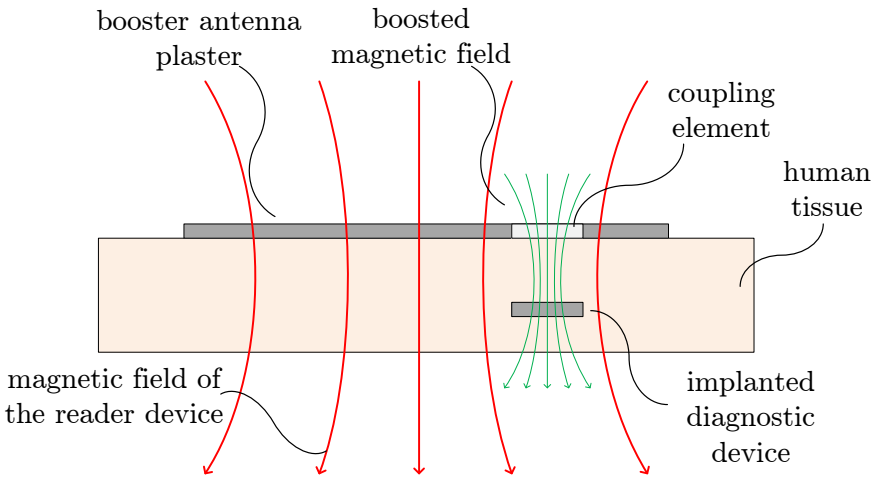


Figure 4.13: Booster antenna designed as plaster. A novel application to transfer data and energy to an implanted diagnostic device

Discussion

This work presents a novel RF booster antenna which is coupled to an RFID tag with an on-chip-antenna. This RFID tag is simulated and fabricated with a 130 mm low cost CMOS process. The size of the RF tag is miniaturized to one square millimeter suitable for implants in medical diagnostic. The reading distance of this tag is two mm. With the use of the presented booster antenna, the distance can be increased to one meter. An additional boosting effect and thus the combination of serial and parallel resonating circuits are envisaged. A measurement setup demonstrates the performance of the booster antenna. Furthermore a novel application for implanted devices is presented.

4.1.2 Coil to Dipole

In the trade and transport service, the UHF RFID technology has been well established. Due to the market demand there is a considerable interest in minimizing the costs of such RFID tags. The cost of these tags comprises three different production processes. Namely the manufacturing costs of the antenna, the RFID die and the assembly process to connect and to join these two parts together.

This section presents an ultra low cost 868 MHz booster antenna, fabricated in an inkjet printing process on cheap flexible polyethylene terephthalate substratum. It increases the operational distance of the already presented highly miniaturized sensor UHF RFID grain (see figure 4.4) (mm to m). The booster antenna is designed to avoid any second layer or underpass. Therefore, and due to the simplification of the assembly works, the overall UHF tag allows much reduced fabrication costs and can be produced at a cost of a single digit cent range.

Original Publications Related to this Section

Pachler, W., I. Russo, W. Bosch, G. Hofer, G. Holweg, and M. Mischitz, „A silver inkjet printed UHF booster antenna on flexible substratum with magnetically coupled RFID die on-chip antenna" In: Antennas and Propagation (EuCAP), 2013 7th European Conference on. Apr. 2013, pp. 1730–1733

Coil to Dipole booster antenna concept

As already described the booster antenna is made up of two components: a conventional antenna (e.g. a dipole) and a coupling structure to provide magnetic coupling with the target device. The equivalent circuit of the presented coil to dipole concept is illustrated in figure 4.14. The coupling structure in combination with the coil-on-chip antenna can be seen as a air-coupled transformer. To provide ideal power transfer to the RFID chip, the dipole has to be complex conjugate matched to the coupling structure and the tag.

To validate this novel concept and to prove the feasibility in a first step, a laboratory experiment, shown in figure 4.15, was performed. Therefore the UHF RFID tag was mounted directly onto a one winding coupling structure. After that, an UHF impedance tuner was used to match the coupled RFID tag to a conventional dipole. As it is illustrated, a reading distance of 1.4 m could be achieved. Note that the UHF reader was adjusted to operate at the minimum output power of 0.1 W. Due to the successful feasibility study the concept could be further improved. Therefore, in a next step, a silver inkjet printed dipole was designed that matches the impedance of the coupling structure and the tag. Thus no additional matching network is needed.

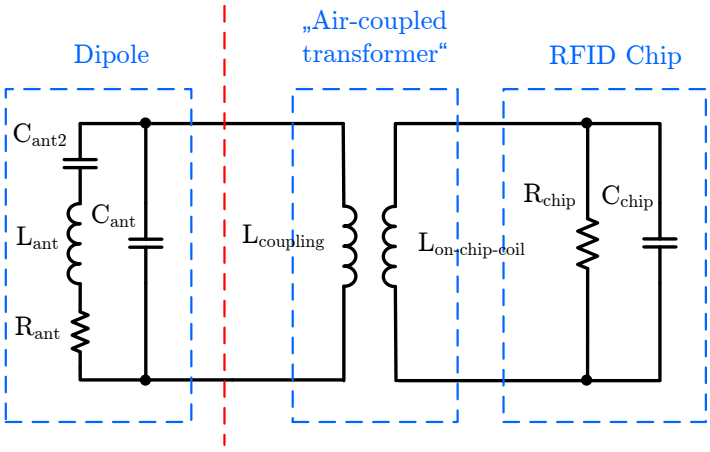


Figure 4.14: Equivalent circuit of the inductive coupled booster antenna concept. The dashed red line indicates that the dipole has to be conjugate matched to the rest of the structure: the air-coupled transformer and the RFID chip.

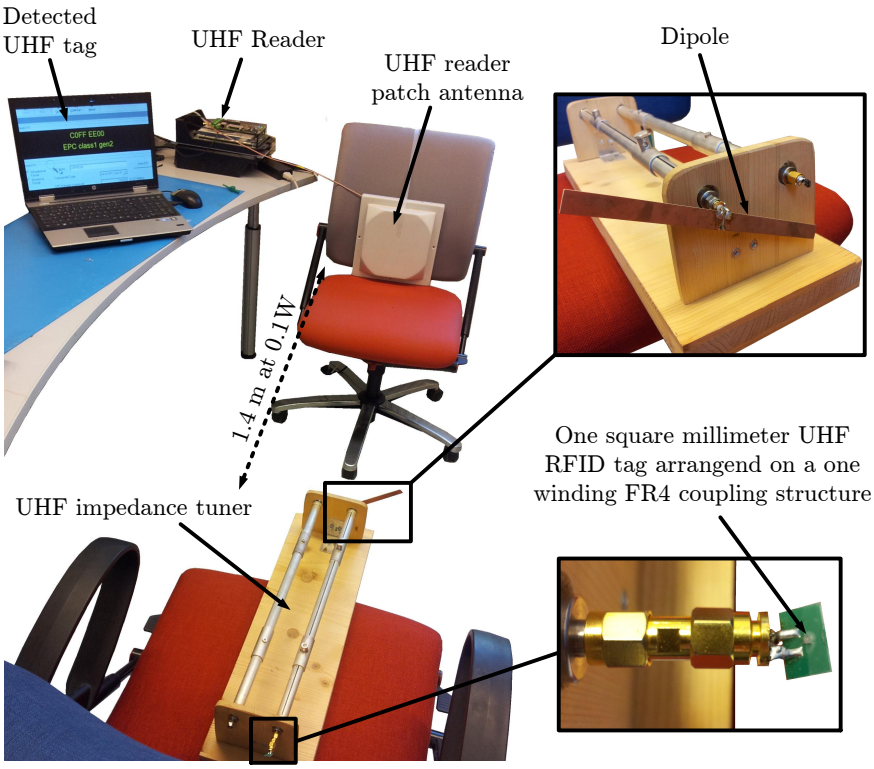


Figure 4.15: Feasible experiment of the coil to dipole booster antenna concept: The one square millimeter UHF RFID tag is arranged directly on to a one winding FR4 coupling structure. This structure is conjugate matched to a conventional dipole by the use of a tuner. With a minimum output power of 0.1 W, a reading distance of 1.4 m could be achieved.

Figure 4.16 shows the impedance measurements of the presented coil to dipole booster prototype. The smith charts are normalized to 50 Ω. As it can be seen (markers at 868 MHz) the coupled RFID tag is well matched to the dipole. $Z_{\text{coupledUHFtag}} \approx Z^*_{\text{matcheddipole}}$.

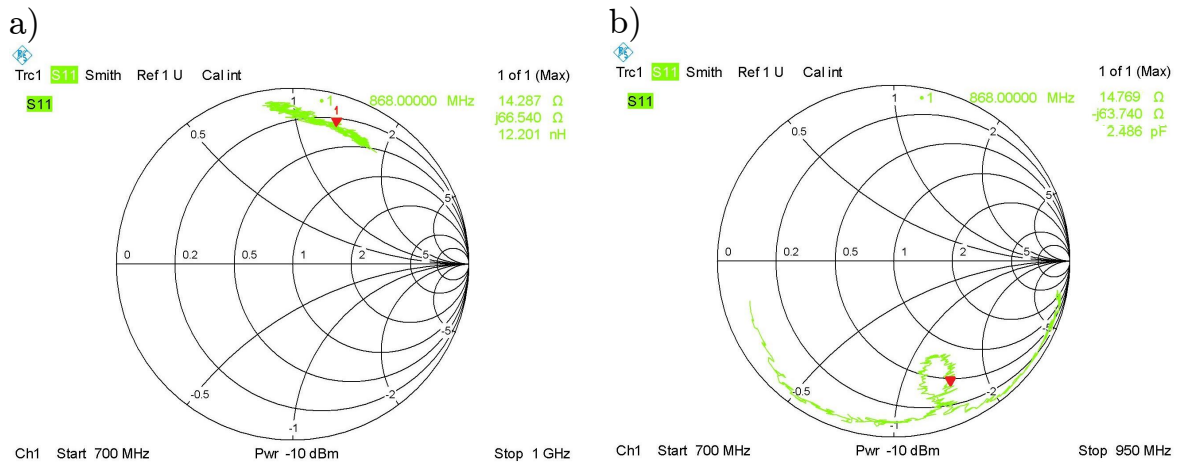


Figure 4.16: Measurements of the presented coil to dipole prototype: a) Impedance of the inductively coupled RFID tag and coupling structure $Z_{\text{coupledUHFtag}} = (14.2 + \jmath 66.5)\Omega$ b) Impedance of the matched dipole and tuner. $Z_{\text{matcheddipole}} = (14.7 - \jmath 63.7)\Omega$. The coupled RFID tag is well matched to the dipole. $Z_{\text{coupledUHFtag}} \approx Z^*_{\text{matcheddipole}}$

Concept of the low cost UHF RFID tag - Inkjet Printing

There is a large number of different conductive silver inks available on the market. As shown in [93], the main challenge in printing high quality conductors is to reduce the sheet resistance. In particular, the temperature used in the curing process plays a decisive role in decreasing the resistance. To keep cost of the produced RFID tag as low as possible, a conventional PET film is used. The melting temperature of PET is approximately 260° C, which allows only low-print processing temperatures. The used Inktec TEC-IJ-010 silver ink should be able to achieve a conductivity of $2.38E7\,\text{S/m}$. Its melting temperature is between $100 - 150°$ C, which allows the usage of the PET substrate. Nevertheless, it was found that there was an interaction between the substrate and the silver ink, which is not negligible. Figure 4.17 illustrates the printed coupling structure. Especially the boarder of the tracks show the interaction between substrate and silver. This effect occurs if the conductor becomes very thin and small. Therefore the conductivity decreases in a non-linear way. A measured conductivity for a 75 μm thick conductor is $0.56E7\,\text{S/m}$, for instance. The result is considered in the design process of the booster antenna.

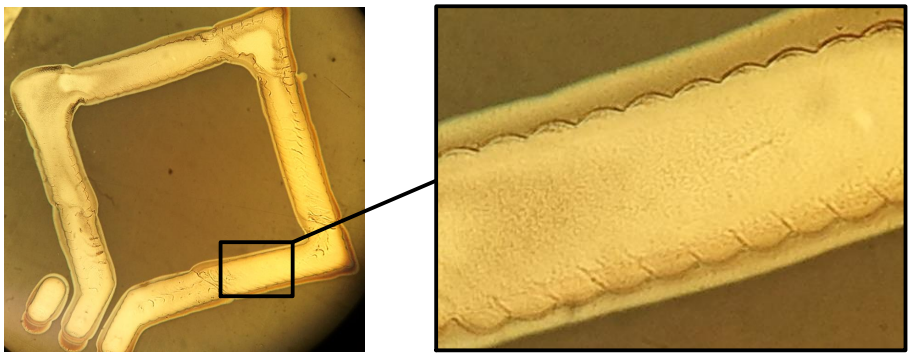


Figure 4.17: Coupling structure manufactured with a silver ink-jet printing process. For measurements GSG-pads are realized.

Design and fabrication of an ultra low cost UHF RFID tag

As already discussed, the coupling structure consists of the primary coil of the air-coupled transformer. The cost-efficient inkjet printing process does not allow any vias or underpasses. Therefore, as it is shown in figure 4.17, a one-turn primary winding is manufactured. The width of this silver track is 75 μm and the height 0.6 nm approximately. Due to the reasons already explained, the conductivity of this small silver track is reduced to $0.56E7\,\mathrm{S/m}$. The inner diameter of this structure is one mm to ensure enough space for a one square millimeter-RFID die. The secondary winding of the air coupled transformer is represented by four windings which are arranged on the RFID chip that is shown in figure 4.4. It is well known that the coupling coefficient depends on the geometrical difference and alignment between these two windings. Better coupling results can be achieved if the primary winding would be similar to the on-chip coil and placed very close to it. A good analysis of such transformers can also be found in [3]. [3] also shows that an offset error of 150 μm reduces the magnitude of power transfer to $-0.5\,\mathrm{dB}$. Thus the presented booster antenna is quite tolerant regarding a misalignment between primary and secondary winding of the air coupled transformer. Anyway, the two coils are located very close to each other to achieve sufficient coupling. The behavior of the transformer as well as the design of the half-wave dipole can be easily evaluated by utilizing CST-Microwave studio TM [105]. The simulation layout, as well as the dipole dimensions can be found in figure 4.18.

The simulated impedance of the one-turn winding and the chip shown in figure 4.19, is $Z_{\mathrm{coupledUHFtag}} = 19.5 + j16.5\Omega$. This impedance has to be conjugate complex matched to the impedance of the half-wave dipole. To avoid a matching network between dipole and coupling structure, the dipole is designed to meet the simulated impedance by controlling the geometrical parameters. Primarily, the resistance of the dipole is controlled by changing the width of the tracks and the reactance by changing the length. Due to the inductive behavior of the coupled RFID tag, the dipole impedance has to be capacitive,

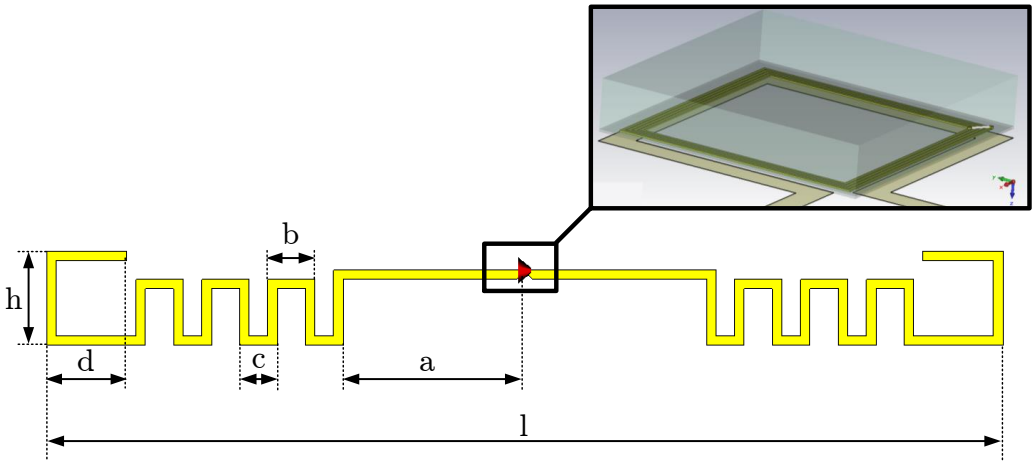


Figure 4.18: Designed dipole antenna to match the purposed air coupling structure. $a = 19\,\text{mm}$, $b = 5\,\text{mm}$, $c = 4\,\text{mm}$, $d = 8.5\,\text{mm}$, $h = 10\,\text{mm}$, $l = 100\,\text{mm}$, the width of the silvertracks is 1 mm, the thickness of the PET is 200 μm with an permittivity of 2.25.

in other words the dipole impedance should be dominated by a negative reactant value. This is valid for dipole antennas which are smaller than $\lambda/2$. If the size of the dipole increases, the input resistance as well as the input reactance increases too. The dipole is resonant slightly below $\lambda/2$. At this point the reactance is zero. In the simulation, a measured silver conductivity of $2E7\,\text{S/m}$, as already described, has to be considered. Figure 4.18 shows the layout of the simulated dipole. The height of the one-layer silver tracks is 0.6 nm. The simulation results of the input impedance in the frequency range between 400 MHz and 1200 MHz are shown in figure 4.19. In addition, the simulated coupling structure with the same frequency range is illustrated. It can be seen that there is a good match between the dipole and the coupling structure at the design frequency of 868 MHz. The simulated radiation pattern of the presented ultra low cost coil-to-dipole UHF booster antenna is shown in figure 4.20. As expected, it is similar to the radiation pattern of a standard half-wave dipole. The simulation shows a maximum gain of 2.11 dBi (decibels over isotropic).

Measurements and Results

In following, measurements have been performed in order to validate the simulated values. The silver-printed coupling structure, shown in figure 4.17, has been measured with a GSG probe, displayed in figure 4.21-b. The impedance of the dipole is measured simple with a network analyzer. As already mentioned, these two impedances are matching each other.

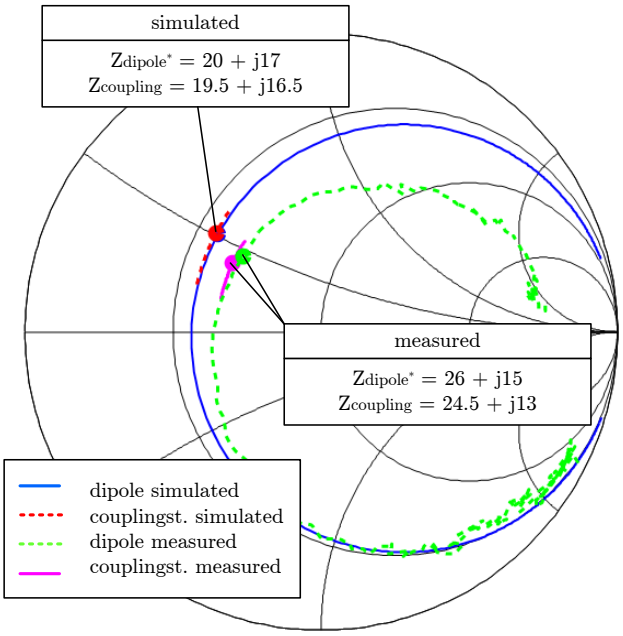


Figure 4.19: Input impedance simulation and measurement results of the presented ultra low cost coil-to-dipole UHF booster antenna. The simulations and measurements show, that the dipole impedance is well matched to the purposed air-coupled transformer and miniaturized UHF tag.

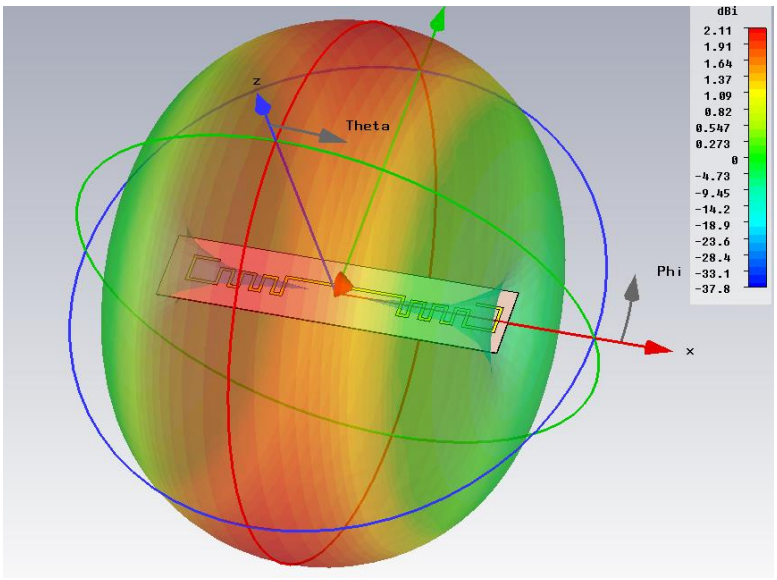


Figure 4.20: Radiation pattern of the presented UHF transponder system. Due to the fact, that the presented coil-to-dipole booster antenna is designed as a half-wave dipole, the radiation pattern is similar. The donut-shaped pattern has a maximum gain of 2.11 dBi.

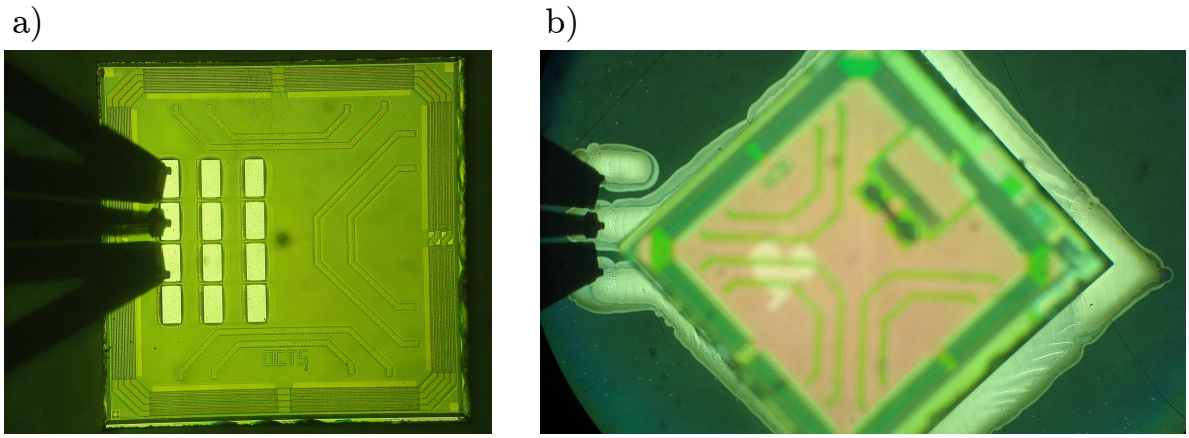


Figure 4.21: GSG probe measurements. left (a): impedance measurement of the coil on chip antenna. right (b): impedance measurement of the coupling structure and the coupled RFID tag, shown in figure 4.4.

Figure 4.19 shows the measured and simulated reflection coefficient (S11) of the coupling structure and the dipole for the frequency range between 400 MHz and 1200 MHz. Comparing simulation and measurement, it becomes clear that the sheet resistance of the silver print is slightly worse than expected. The measured normalized impedance of the coupling structure at 868 MHz is $Z_{\text{coupling}} = (24.9 + \jmath 13)\Omega$, which leads from a simulated resistance of $19.5E7\,\Omega$ to a measured value of $24.5E7\,\Omega$. Nevertheless the measurement shows that the two parts of the booster antenna are still well matched ($Zdipole^* \approx Zcoupling$).

As already mentioned, no additional assembly process is required to produce the overall booster system. To complete the device as an RFID tag, for instance, the RFID die just has to be attached to the designated area around the coupling structure. This process is illustrated in figure 4.22. All tests are done with a conventional UHF gen2 RFID reader [78]. The maximum system range is about 2.1 m @1 W. When increasing the gap between the RFID die and the booster antenna (causing a poor coupling coefficient), the system range decreases proportionally. A maximum displacement of 2 mm was tested.

Discussion

To the author's knowledge, this work presents the first manufactured silver ink-jet printed 868 MHz booster antenna for magnetic coupling to an RFID die. Therefore, a one square millimeter RFID die with an on-chip coil is manufactured in a low-cost 130 nm-CMOS process. Attaching this RFID chip to the presented booster antenna, the reading range is extended up to 2.1 m with one watt reader output power. The booster antenna is divided in two parts: the antenna itself and its coupling structure for magnetic coupling to the die.

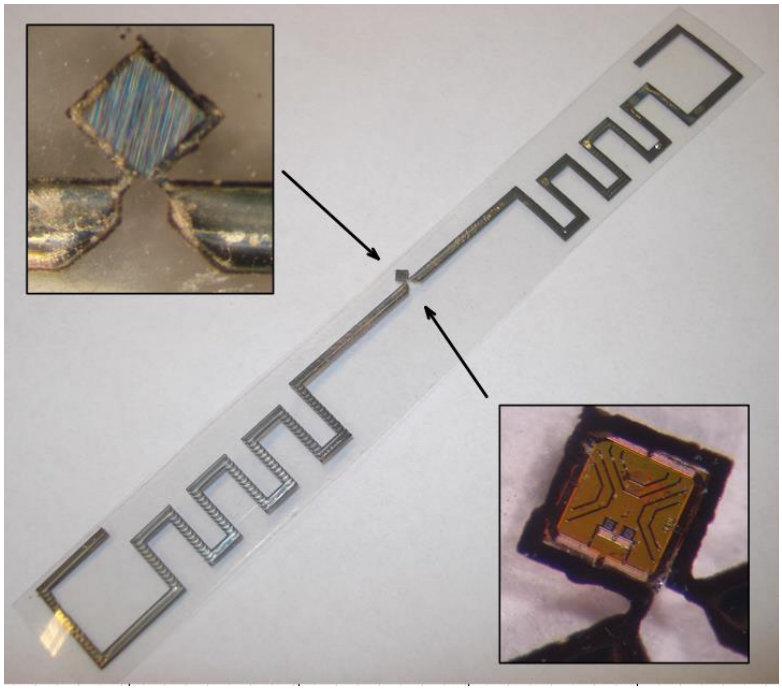


Figure 4.22: Silver printed booster antenna magnetically coupled to the RFID die. The bottom and top view of the coupling structure is highlighted.

Both components are simulated and measured separately. To produce the overall booster antenna system no additional assembly process is required. Thus the manufacturing costs are reduced. Furthermore, due to the low-cost ink-jet and CMOS process the presented device can be produced at a cost of a single digit cent range.

4.2 Capacitively Coupled Booster antennas

This section presents the booster antenna technology in combination with capacitively coupled RFID tags. Therefore the already presented on-chip capacitive coupled (OC3) tag is used (see section 3.4). As already described, this one square millimeter RFID tag communicates with the reader by non-resonant capacitive coupling at 13.56 MHz and 868 MHz. Figure 4.23 shows the already presented OC3. Unfortunately, as it is shown in section 3.4, the reading distance is limited to 200 μm at 13.56 MHz and 400 μm at 868 MHz (@1 Watt reader output power). However, this drawback can be eliminated by the use of capacitive coupled booster antennas. In the following, two custom-built booster antennas are presented that considerably enhance the OC3 RFID tag reading distance at HF and UHF.

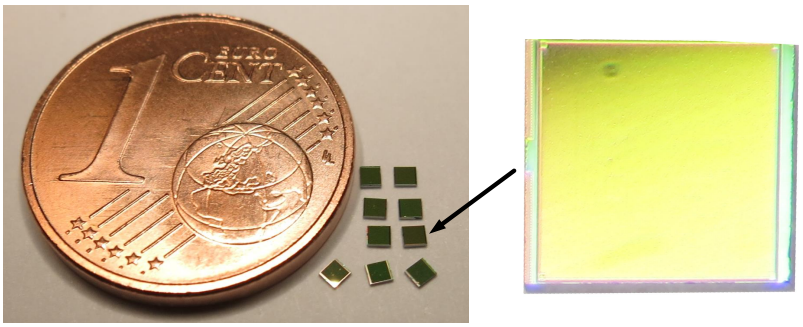


Figure 4.23: The on-chip Capacitive Coupled RFID tag from section 3.4: Dimensions (1 mm x 1 mm x 0.3 mm) compared to a one euro cent coin.

Note that the presented capacitive coupled booster antenna types are designed without any via or underpass. The antennas are realized with two separated conductive layers which are stacked above each other. This enables novel capabilities. For example, as it is shown in figure 4.24, the OC3 transponder can be easily embed into dielectric substrate, such as paper. To improve the performance of the tag, booster structures can be print onto the top and bottom side of the substrate. Note that for this concept, as well as the presented capacitive booster antennas there are patents pending.

Original Publications Related to this Section

W. Pachler, J. Grosinger, W. Bösch, P. Greiner, G. Hofer, and G. Holweg, „An On-Chip Capacitive Coupled RFID Tag" In: European Conference on Antennas and Propagation, April 2014.

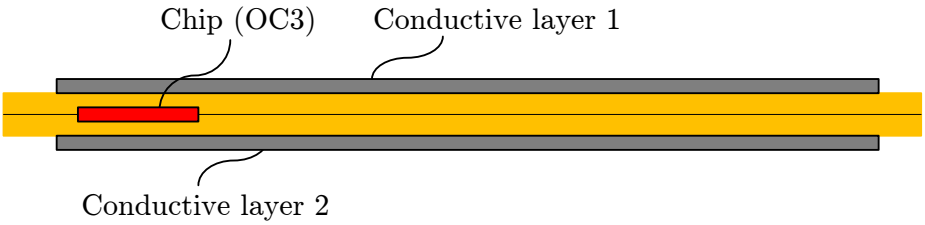


Figure 4.24: Embedded OC3: Due to the capacitive coupling, the OC3 can be embed into dielectric substrate, such as paper. The tag performance can be further increased by adding the presented capacitive boosting concepts onto the top and bottom of the dielectric substrate.

4.2.1 Cap to Coil

The presented cap to coil booster antenna is designed to operate at 13.56 MHz. Therefore, similar to conventional HF RFID tags, the largest part of the booster antenna is represented by an HF coil. Instead of connecting the coil directly to the RFID chip, it is connected to two electrodes - the capacitively coupling structure. Thus this type of booster antenna transforms the communication channel from the magnetic field into the electric field and vice versa.

The presented HF booster antenna consists of two electrically isolated coil antenna layers and two metallic coupling areas to establish capacitive coupling to the OC3 tag. A layout of the two coils can be seen in figure 4.25. The size of the booster antenna is 80 mm × 40 mm similar to standard proximity identification (ID-1) cards [52]. The coupling area to the OC3 tag has a size of 1.1 mm × 1.1 mm. The width as well as the spacing of the nine coil windings is 0.5 mm. The large metal surfaces in the middle of the coils provide a good capacitive coupling between the two coil antenna layers. Thus, there is no need to realizes a galvanic contact between the antenna layers.

The antenna design was done by means of the electromagnetic field simulator ADS (Advanced Design System [2]). One key to obtain a sufficient power supply to the low power OC3 rectifier is to maximize the voltage at the capacitive coupling structure. In the presented design example this is done with a resonating circuit which causes, depending to the quality factor, a high voltage magnification at the resonating frequency of 13.56 MHz. A simplified equivalent circuit of the setup — HF booster antenna and OC3 tag — is shown in Fig. 4.26. The parameters values of the circuit are listed in Tab. 3.5. In contrast to conventional proximity integrated circuit card (PICC) [50] antennas, L_{PICC} is respectively large (9.6 μH) in order to gain a higher voltage and to resonate with small capacitor values. Due to the large number of windings ($N = 9$) and stacking of the two coils a large parallel parasitic capacitor C_{PICC} occurs.

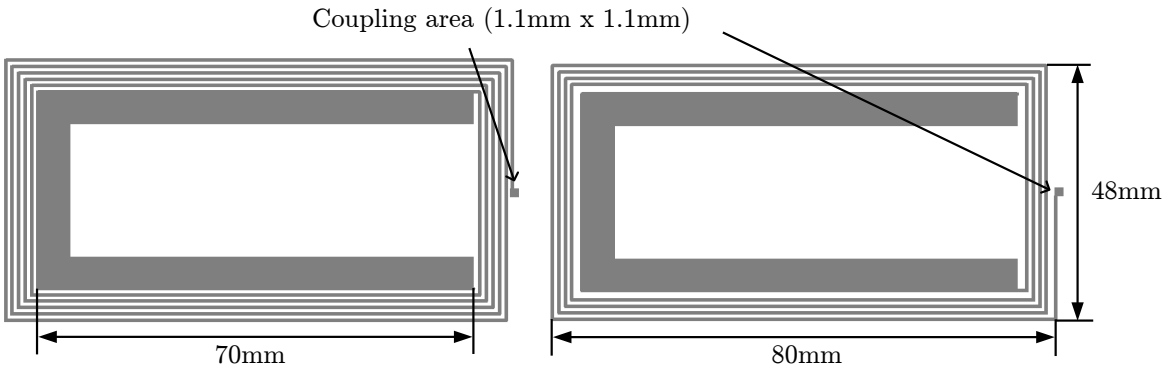


Figure 4.25: HF booster antenna dimensions: The coupling area is designed to provide capacitive coupling to the OC3 tag and is incorporated in the coil structure.

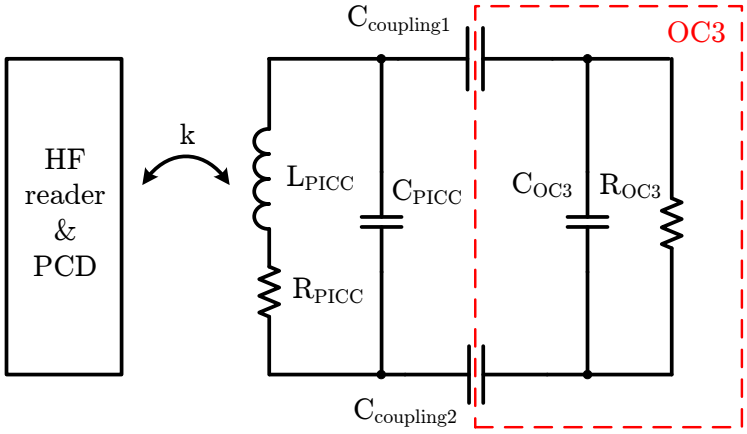


Figure 4.26: Equivalent circuit of the HF booster antenna: The respectively large coil L_{PICC} and its parasitic capacitance C_{PICC} is resonant in combination with the capacitive coupled OC3 tag. The capacitive coupling to the OC3 tag is represented by $C_{\mathrm{coupling1}}$ and $C_{\mathrm{coupling2}}$.

Table 4.1: Parameter values of the HF booster antenna equivalent circuit

Parameter	L_{PICC}	R_{PICC}	C_{PICC}	C_{coupling}
Values	9.6 μH	25 Ω	14 pF	1 pF
Parameter	C_{OC3}	R_{OC3}	k	
Values	810 fF	40 – 8000 Ω	0-1	

The coils are printed on a polyethylene terephthalate (PET) substrate that has a thickness of 100 μm. The thickness of the conductive silver layer is 8 μm. The electrical isolation of the coils is realized by one layer of PET substrate (see Fig. 4.27).

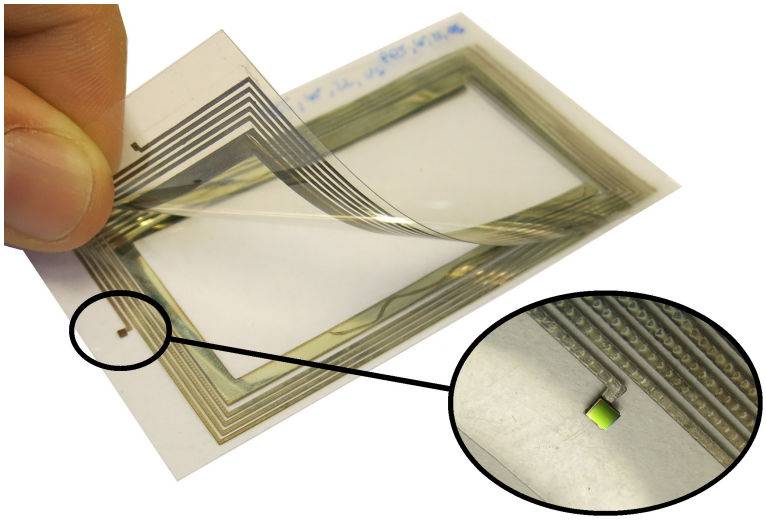


Figure 4.27: Picture of the HF booster antenna and the OC3 tag: The HF booster antenna is based on two planar coil antennas with several windings without a galvanic contact. The serial resonance of the booster antenna and the OC3 tag leads to a voltage magnification at 13.56 MHz and thus enhances the reading distance of the tag.

The functionality of the HF booster antenna was tested with a standard ISO 14443 proximity coupling device (PCD) antenna [50]. A maximum reading distance of 30 cm was achieved with an HF reader output power of 1 W.

4.2.2 Cap to Dipole

The custom-built UHF booster antenna consists of two identical — but mirrored — planar T-matched dipoles. The coupling area is incorporated in the antenna design. The antenna was designed by means of ADS. Figure 4.29 shows the dimensions of one of the T-matched dipoles.

The simulation of the UHF booster antenna shows a good capacitive coupling between the two T-matched dipoles that is guaranteed by large metal surfaces (10 mm × 175 mm) and by its small distance of 100 μm. Therefore, there is no need for a galvanic contact between the two antenna layers. The input impedance of the UHF booster antenna Z_{ant} is power matched to the impedance of the coupling structure and the OC3 tag at 868 MHz, i.e., $Z_{\text{ant}} = (120 + \jmath 175)\Omega$. As it can be seen in figure 4.28, the parallel dipoles are very well matched to the input impedance (marker m1 and m2 = 868 MHz). Nevertheless there is a slight influence due to the capacitive coupling of both dipoles.

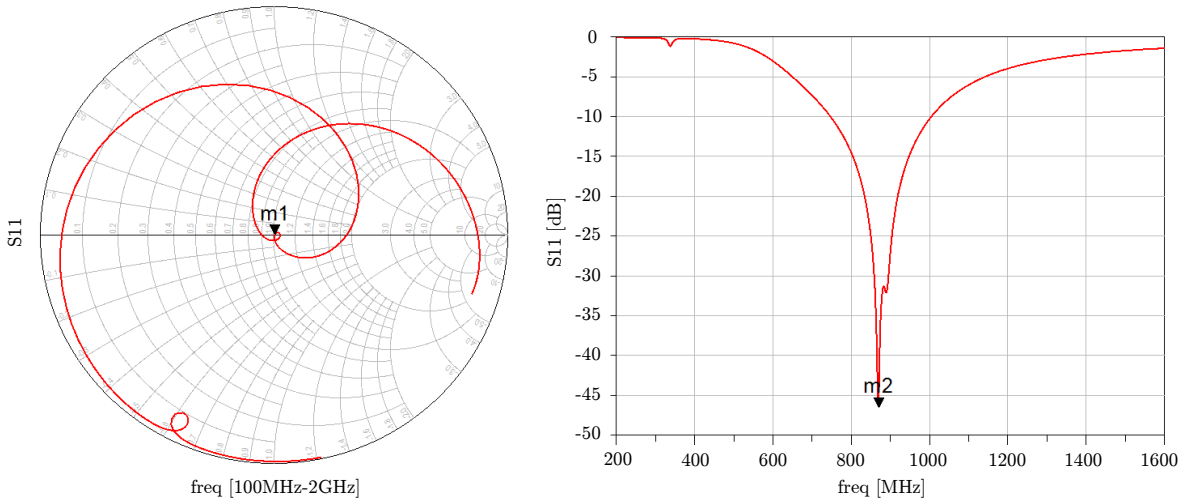


Figure 4.28: Reflection coefficient S11: The smith chart is normalized to the simulation port impedance $Z_{\text{coupling}} = (120 - \jmath 175)\Omega$. As it can be seen the dipole is designed and simulated to operate at 868 MHz (marker m1 and m2)

The antenna layers are printed on an FR4 substrate with a thickness of 1 mm. The conductive copper layer has a thickness of 35 μm and is covered with a 50 μm PET film to assure an electrical isolation between the two antenna layers (see Fig. 4.30).

As shown in Fig. 4.30, the OC3 tag is directly placed at the coupling areas of the UHF booster antenna. With this, the reading distance of the OC3 tag is considerably increased up to 1 m at 1 Watt reader output power.

The presented booster antenna designs consist of two electrically isolated antenna layers and metallic coupling areas to establish capacitive coupling to the OC3 tag. This

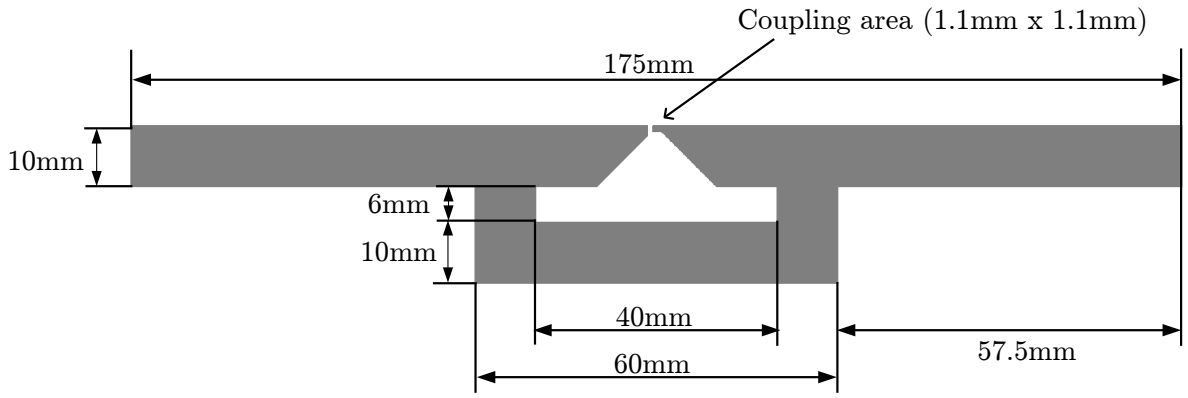


Figure 4.29: Dimensions of the planar T-matched dipole: The coupling area of 1.1 mm × 1.1 mm is designed to provide capacitive coupling to the OC3 tag.

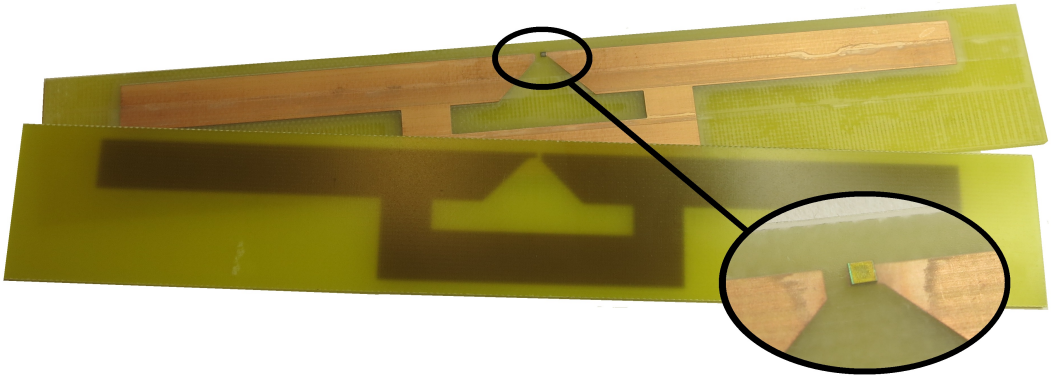


Figure 4.30: Picture of the UHF booster antenna and the OC3 tag: The OC3 tag is directly placed at the coupling areas of the UHF booster antenna. The UHF booster antenna is based on two T-matched dipole antennas without a galvanic contact. The input impedance of the UHF booster antenna is power matched to the impedance of the coupling structure and the OC3 tag at 868 MHz.

implementation has a big advantage in comparison to already presented booster antennas [46]. While the OC3 tag is encapsulated in money, credit cards, or any other dielectric materials, the booster antenna is simply printed onto the top and bottom side of the material. There is no need to use small fragile coupling structures, vias, or underpasses.

4.3 Ferrite Booster Antenna

This section presents a near field communication (NFC) antenna that is printed directly on a ferrite substrate using a silver inkjet printing process. Such a silver inkjet printed ferrite NFC antenna provides a minimum substrate thickness, a good operation on metal objects, and a small assembly effort. The NFC antenna performance is analysed by measurements based on the ISO/IEC standard 10373-6 for proximity identification cards test methods. For this, the antenna is connected to an NFC microchip. Measurements in a non-metal environment show that the ferrite antenna performs equally good a custom-built NFC antenna printed on photo paper substrate, despite additional losses in the ferrite substrate. In a metal environment the ferrite antenna clearly outperforms the photo paper antenna.

Original Publications Related to this Section

W. Pachler, J. Grosinger, W. Bösch, G. Holweg, K. Popovic, A. Bluemel and J.W. List-Kratochvil „A Silver Inkjet Printed Ferrite NFC Antenna" In: Loughborough Antennas & Propagation Conference (LAPC), International Conference on. November 2014

4.3.1 Magnetic Antennas in Metal Environment

In the last decades, more and more mobile devices (smartphones, tablets, or laptops) have been equipped with the near field communication (NFC) technology. The NFC technology is used in short range applications such as ticketing, payment, and peering of two devices. In NFC, a reader device communicates with a transponder (tag) device by inductive coupling. Two coils, one of the reader device and one of the tag, are inductively coupled via a magnetic field. Metal objects in the close vicinity of the devices deteriorate the performance of this coupling mechanism. Eddy currents are induced in the metal environment and generate an opposite oriented magnetic field that weakens the field of the reader device [89]. To mitigate this effect, NFC antennas have been equipped with ferrite sheets that shield the antenna from the disturbing metal [31, 58]. As a result, the battery back of a smart phone for example has less influence on the NFC system.

This work presents an NFC antenna that is directly printed on a ferrite substrate using a silver inkjet printing process. By printing directly on a ferrite substrate, a minimum thickness for NFC antennas can be achieved. Furthermore, the ferrite substrate provides ideal characteristics for the inkjet printing technology. In particular, the ferrite offers a beneficial surface energy and allows high temperatures for the sintering process. Also,

the ferrite substrate offers a good non-galvanic contact from one printed coil winding to the other by providing a high real value of permeability.

Similar to NFC this concept is also used in Wireless Power Transfer (WPT) applications, such as wireless charging. As [43] shows, recent developments in the field of wireless charging provide future application potentials. Moreover a combination of the NFC and wireless charging is imaginable [101]. Indeed NFC differs with a higher operation frequency and lower RF power levels. Anyway [101] describes a concept of NFC-enabled wireless charging.

4.3.2 Design

The layout of the silver inkjet printed antenna can be found in Fig. 4.31. The size of the four winding coil is 45 mm x 75 mm. The antenna pads are used to connect the antenna to radio frequency (RF) devices. The antenna design is based on a simplified equivalent circuit of the antenna. The antenna equivalent circuit can be seen on the right side of Fig. 4.32. The circuit consists of a coil resistance R_A and an inductance L_A. A parallel-connected parasitic capacitance C_A models the capacitive coupling between the single coil windings.

4.3.3 Realization

The antenna layout was printed with a silver inkjet printing process on a flexible ferrite substrate and - for comparison reasons - on a photo paper substrate. The silver ink CCI-300 from Cabot Corporation [10] was used for printing onto the substrates. According to the datasheet, the ink consists of $19 - 21\,\%$ solid silver nanoparticles. The ink viscosity is $11 - 15\,\mathrm{Pa \cdot s}$ at $22°$ C. Fig. 4.34 illustrates the PixDro LP50 inkjet printer [96]. The printer allows a printing accuracy of $5\,\mu$m. The antenna structure is printed with an 800 dpi resolution.

The flexible ferrite sheet FLX-950X from Toda Kogyo Corp. [106] has a size of 135 mm x 135 mm with a thickness of $100\,\mu$m. According to the datasheet, the real part permeability of the ferrite is 150 at 13.56 MHz, while the imaginary part that leads to losses is 3 at 13.56 MHz. The photo paper substrate is specially designed for inkjet printing.

One of the key features of a good metal inkjet printing process lies in the substrate surface energy. The surface energy describes how the silver ink (liquid) is spread over the substrate surface. Besides the drop surface tension (silver ink) and liquid adhesions, this factor leads to a limitation of resolution and accuracy. An overview about the effects of common used substrates, such as glass, hydrophobic paper, FR-4 and, polyimide can be found in [113]. Certainly, this factor can be improved by additional surface treatments, such as plasma, corona or chemical treatments. As [59] shows, this treatments can lead

to better printing results. Anyway, additional surface treatments lead to a higher effort. As it is shown in the presented results, the surface energy of these pure ferrite sheets fits well for the silver printing processes.

In order to increase the conductivity of the coils, several printing runs were realized before the sintering process to increase the thickness of the silver tracks. The number of possible passes mainly depends on surface energy, drop surface tension and liquid adhesions. In this work, two silver ink layers (printing processes) were used in combination with ferrite and four layers with photo paper. The thickness of the sintered silver tracks can be estimated to be 1.8 μm on the ferrite substrate and 3.6 μm on to the photo paper substrate (one silver layer has a hight of about 0.9 μm).

After printing the structures are thermally cured at temperatures well obove 150° C. As the ink contains both solvents and additives, the high temperature causes the vaporization of these elements and the silver nano particles start to sinter. This sintering process leads to a solid silver pattern. According to the datasheet, the CCI-300 silver ink needs a temperature of $100 - 350°$ C for approximately 30 minutes. The higher the temperature and heating time, the higher is the conductivity of the silver particles. However, the photo paper substrate suffers under high temperatures. This effect limits the temperature to 150° C (one hour sintering time). Moreover substrates like PET interact with the silver ink under high temperatures, leading to high resistances [84]. In contrast to photo paper, the ferrite substrate does not suffer from high temperatures and allows a sintering temperature of 250° C (one hour sintering time was used). Beside the used silver nanoparticles [10], other functional materials would be also suitable for the ink jet printing process[30]. Figure 4.35 shows the realized antennas.

Figure 4.37 shows four silver tracks of the presented printed NFC coil. As well as in Fig. 4.36, Fig. 4.37 shows both sides of the ferrite sheets. It can be seen that the bottom surface of the sheet is slit slightly into squares for precise breaking the ferrite sheet into separate pieces. Originally the manufacture uses the small ferrite squares in combination with PET laminates to create flexible ferrite sheets. Just the top side of the ferrite is suitable for silver ink printing. Although the very small gap (μm) between the ferrite squares is no barrier for the conductivity of the 0.5 mm silver track. Unfortunately the capillary action during the sintering process is high and all silver tracks are shortened at every gap. However, the top ferrite surface fits perfectly for inkjet printing.

4.3.4 Measurements

After realization, the antenna parameters are characterized by measurements. The parameters L_A and R_A of the antenna equivalent circuit are measured with an impedance analyzer at low frequencies (i.e., at about 500 kHz). At low frequencies, the capacitive part of the antenna (C_A) is negligible. This allows to measure L_A and R_A of both antenna prototypes (see Tab. 4.2). The self-resonant frequency f_s of the antennas is found at the

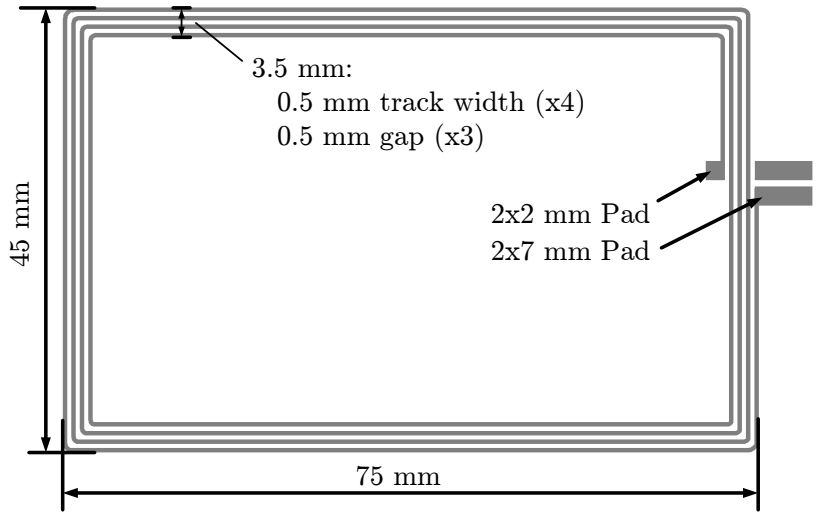


Figure 4.31: Layout of the designed coil antenna: The size is 45 mm x 75 mm with a track width and gap width of 0.5 mm.

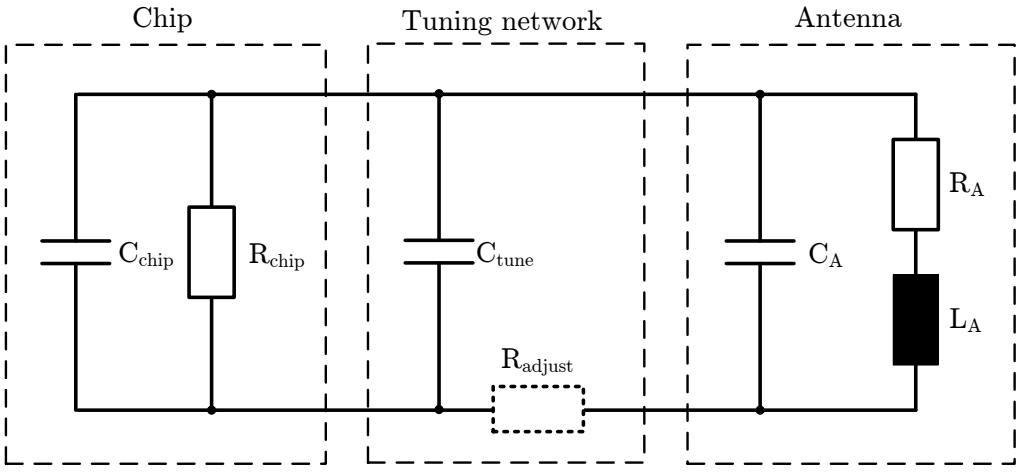


Figure 4.32: Equivalent circuit of the NFC tag: C_{chip} and R_{chip} are representing the NFC chip. R_{A}, L_{A} and C_{A} characterize the antenna. The antenna is connected to the chip with a tuning network. C_{tune} is used to shift the operation frequency to 13.56 MHz. R_{adjust} is used to compensate the resistance difference of the ferrite and photo paper antenna prototypes.

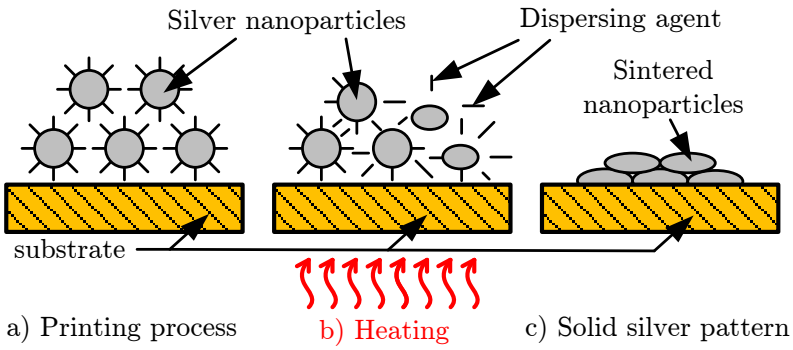


Figure 4.33: Silver inkjet process: First, the silver ink is printed onto the substrate. A dispersing agent is used as a vehicle to carry the silver nanoparticles. After printing, the structure is heated up and the dispersing agent is vaporized. The sintering procedure leads to a solid silver pattern.

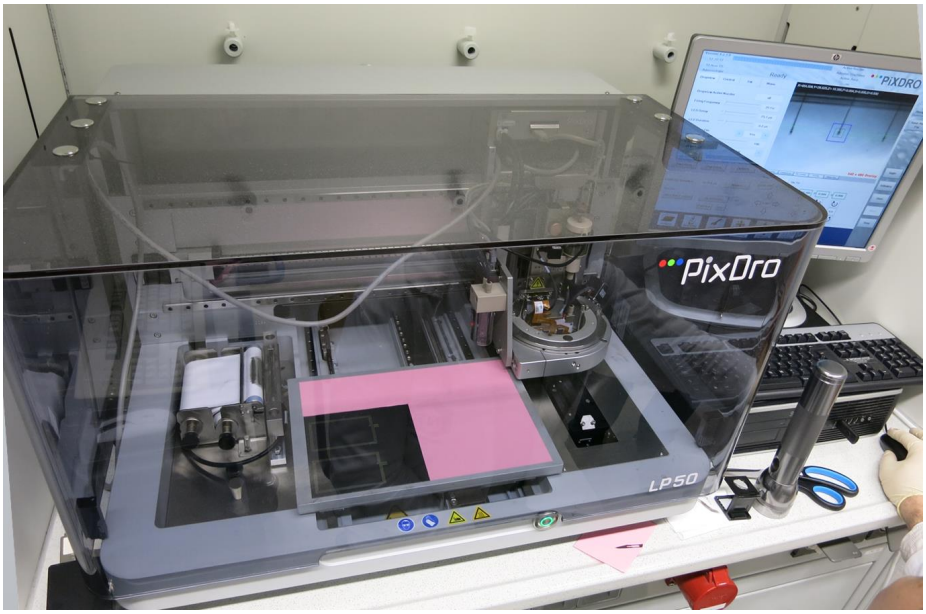


Figure 4.34: PixDro LP50 silver inkjet printer [96]: Two NFC coils are printed onto a ferrite sheet (black). The pink A4 paper sheet shows the possible printing area. 30 nozzles of the cartridge were deployed. A drop analysis and calibration procedure of the nozzles can be seen (three drops, dropping from the cartridge are displayed on the PC screen). One printed silver layer has a height of $\approx 0.9\,\mu$m.

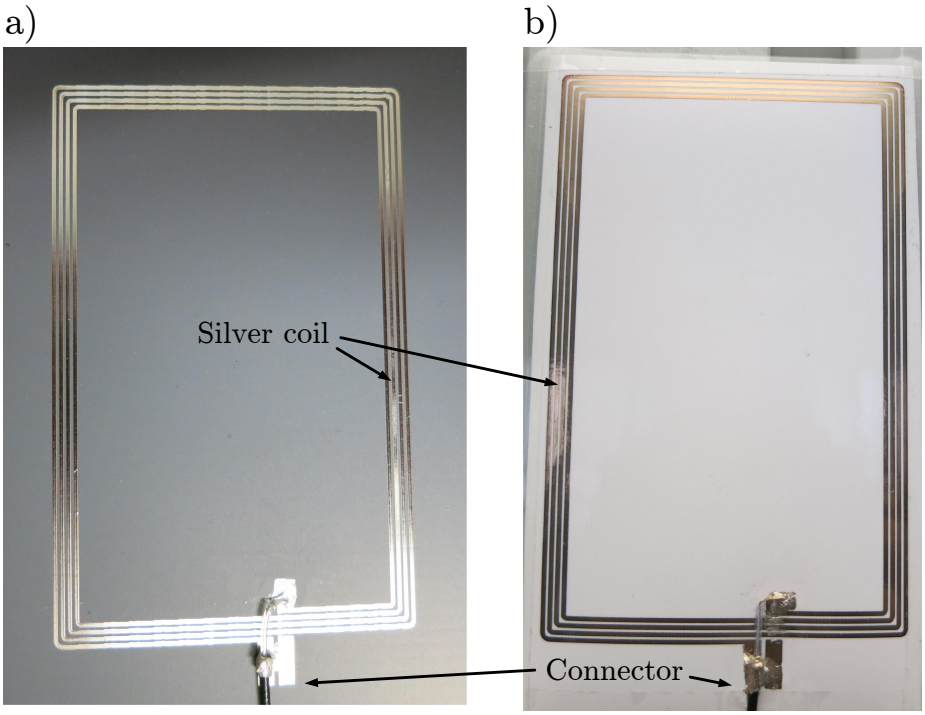


Figure 4.35: Silver inkjet printed NFC antenna prototypes: a) ferrite antenna and b) photo paper antenna. A cable is attached to the connector tab with conductive silver. The cable leads to the NFC tag chip.

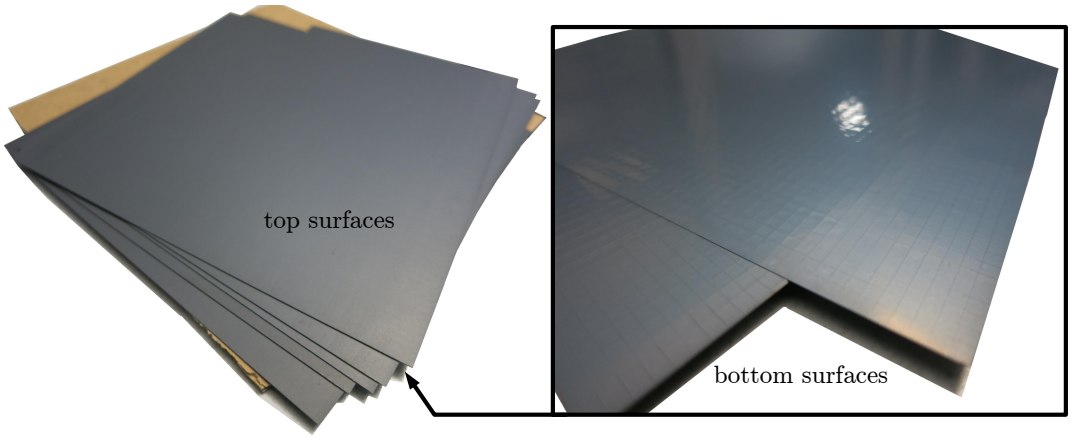


Figure 4.36: Toda Kogyo corp [106] custom made ferrite sheets. The size of the pure ferrite sheets is 135 mm x 135 mm with a thickness of 100 μm. While the top surface is flat, the bottom side is slit slightly into squares, for precise separating.

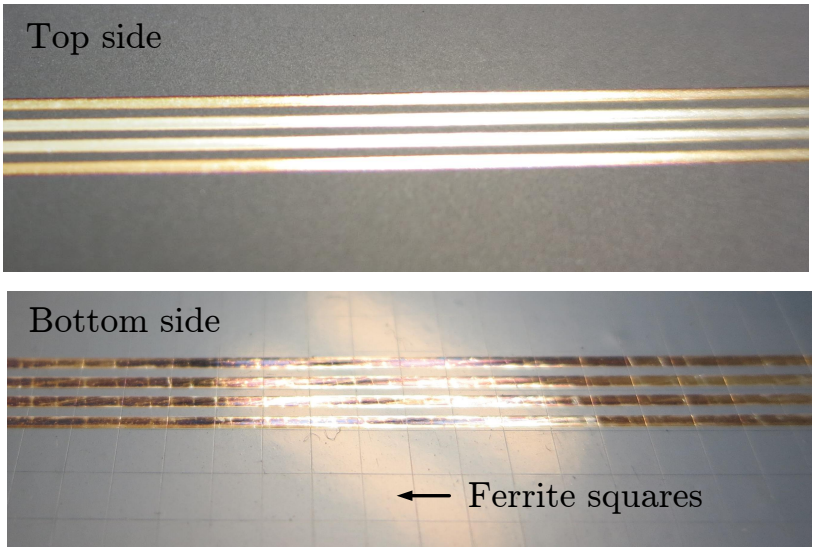


Figure 4.37: Printed NFC coil on the top and bottom side of the ferrite sheet. It is shown that the top surface is well suitable for the silver ink jet printing process. The bottom side is separated into ferrite squares. Due to the capillary action the silver tracks are shortened at the bottom side at each gap.

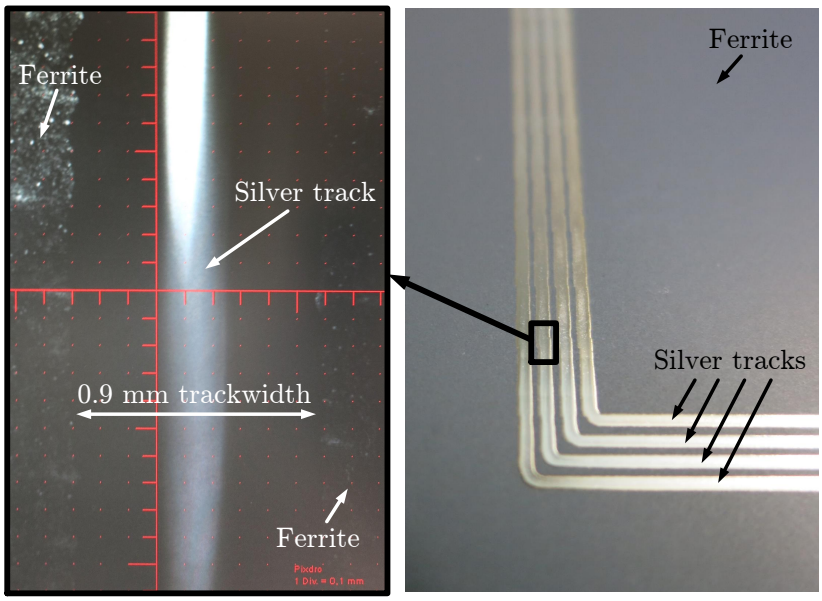


Figure 4.38: Printed NFC coil on the top and bottom side of the ferrite sheet. It is shown that the top surface is well suitable for the silver ink jet printing process. The bottom side is separated into ferrite squares. Due to the capillary action the silver tracks are shortened at the bottom side at each gap.

zero reactance point. With the resonant frequency, the capacitance C_A of the antennas can be calculated by

$$C_\mathrm{A} = \frac{L_\mathrm{A}}{R_\mathrm{A}^2 + (2\pi f_\mathrm{s} L_\mathrm{A})^2} \tag{4.3.1}$$

The measured and calculated parameters are listed in Tab. 4.2.

NFC Tag Performance

Also, the NFC antenna performance is analysed according to the ISO/IEC standard test measurements for proximity identification cards [49]. Therefore, the antennas are connected to NFC microchips. The tag chip is an NFC capable test chip from Infineon. The chip bases on the ISO14443 [50] standard. As illustrated in Fig. 4.32, the chip is characterized by a parallel circuit of a resistance R_chip and a capacitance C_chip. An additional parallel capacitor C_tune is used to tune the tag circuit to the operation frequency of 13.56 MHz. This adjustment of the resonance frequency f_s bases on the following equation:

$$f_\mathrm{s} = \frac{1}{2\pi}\sqrt{\frac{1}{L_\mathrm{A}(C_\mathrm{chip} + C_\mathrm{tune} + C_\mathrm{A})} - \left(\frac{R_\mathrm{A}}{L_\mathrm{A}}\right)^2}. \tag{4.3.2}$$

The resistances R_A of the antenna prototypes are not equal (see Tab. 4.2). In order to compare the performance and the characteristics of the printed antennas an additional resistance $R_\mathrm{adjust} = 19\,\Omega$ is added to the photo paper antenna (see Fig. 4.32). This adjustment leads to a small measurement error because of the two different equivalent circuits. However, the adjustment allows to compare both antennas due to almost equal resistances.

With the ISO10373-6 tag test setup [49], the required minimum magnetic field strength H_min for operation is measured for both NFC tags. A deviation of the resonance frequency of the tag from 13.56 MHz operation frequency of the reader increases the required minimum field strength. This behavior is reflected in the measurement results (see Fig. 4.39). During the measurement, the total parallel capacitance $C_\mathrm{P} = C_\mathrm{chip} + C_\mathrm{tune} + C_\mathrm{A}$ was varied by changing the value of C_tune in 2 pF steps. The ferrite antenna tag requires a minimum field strength of $H_\mathrm{min} = 0.33\,\mathrm{A/m}$, while the photo paper antenna tag requires a minimum field strength of 0.26 A/m. A slightly increased value for the required H_min can be observed at the ferrite antenna due to additional losses in the ferrite substrate. Also, the measurement curves show that the ferrite antenna operates at 13.56 MHz at a lower capacitance in comparison to the photo paper antenna prototype. This is a result of the higher inductance of the printed ferrite antenna (see Tab. 4.2). Furthermore, the measurement curves indicate that both antennas provide low quality factors [25]. A variation of several one digit pF, i.e., a deviation in the resonance frequency, does not deteriorate the performance of the presented NFC tags. Therefore, the NFC tag is suitable to operate in harsh antenna environments.

The ISO10373-6 tag test setup presented in this section was performed in a non-metallic test environment. The measurements in the non-metal environment show that the ferrite antenna performs equally good in comparison to the photo paper antenna, despite additional losses in the ferrite substrate.

Table 4.2: Antenna parameter values of equivalent circuit: The parameters are measured with an impedance analyzer.

Substrate	L_A	R_A	C_A
Paper	2.44 μH	58.2 Ω	2.48 pF
Ferrite	3.31 μH	77.4 Ω	7.81 pF

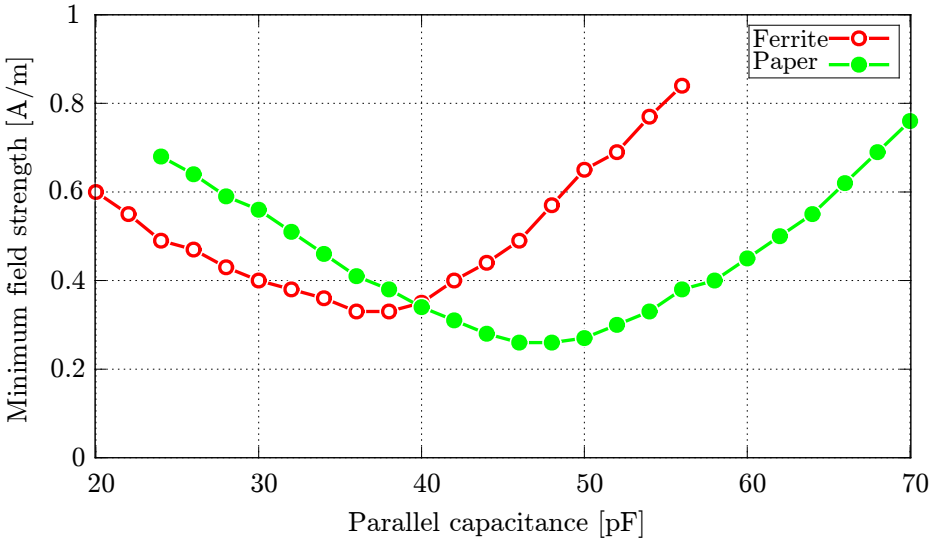


Figure 4.39: Minimum field strength measurement at 13.56 MHz with the ISO10373-6 test setup: The total parallel capacitance is varied by C_{tune} in 2 pF steps. The ferrite antenna prototype exhibits its minimum field strength at a parallel capacitance of 38 pF, the photo paper antenna prototype at 48 pF. The minimum field strength increases by varying the parallel capacitance, i.e., by varying the antenna resonance.

Metal Environment

In the case of a metal environment, the ferrite antenna clearly outperforms the photo paper NFC antenna. This performance enhancement can be seen in simulations as well as in measurements.

The simulations are performed with CST Microwave Studio [105]. The simulation setup is shown in Fig. 4.40. A 100 μm thick copper sheet is arranged below the printed ferrite

antenna. The distance between the cooper sheet and the ferrite antenna is varied between 0 and 5 mm. Fig. 4.40 also shows the magnetic field lines created by the loop antenna. The simulation shows that the magnetic field of the ferrite antenna is not significantly deteriorated by the cooper plate. In contrast, the magnetic field of the photo paper NFC antenna is deteriorated by the metal environment. These different behaviours can be compared in Fig. 4.41 and Fig. 4.42. The figures show the amplitude of the magnetic field versus the distance from the center of the antennas in z-direction for different distances of the metal sheet and the antenna. The metal distance ranges from 0.1mm to 5.1mm. Fig. 4.41 shows that the magnetic field of the ferrite antenna is slightly influenced by the cooper plate, while Fig. 4.42 shows a huge decrease of the magnetic field of the photo paper antenna with a decreasing metal distance. Also, the photo paper antenna creates a weaker magnetic field in the presence of the cooper sheet in comparison to the ferrite antenna (compare Fig. 4.41 and Fig. 4.42 for a metal distance of 5.1mm). Additionally, Fig. 4.41 and Fig. 4.42 illustrate that the optimal field strength is around 10 mm distance as predicted by theory for such an antenna geometry [25].

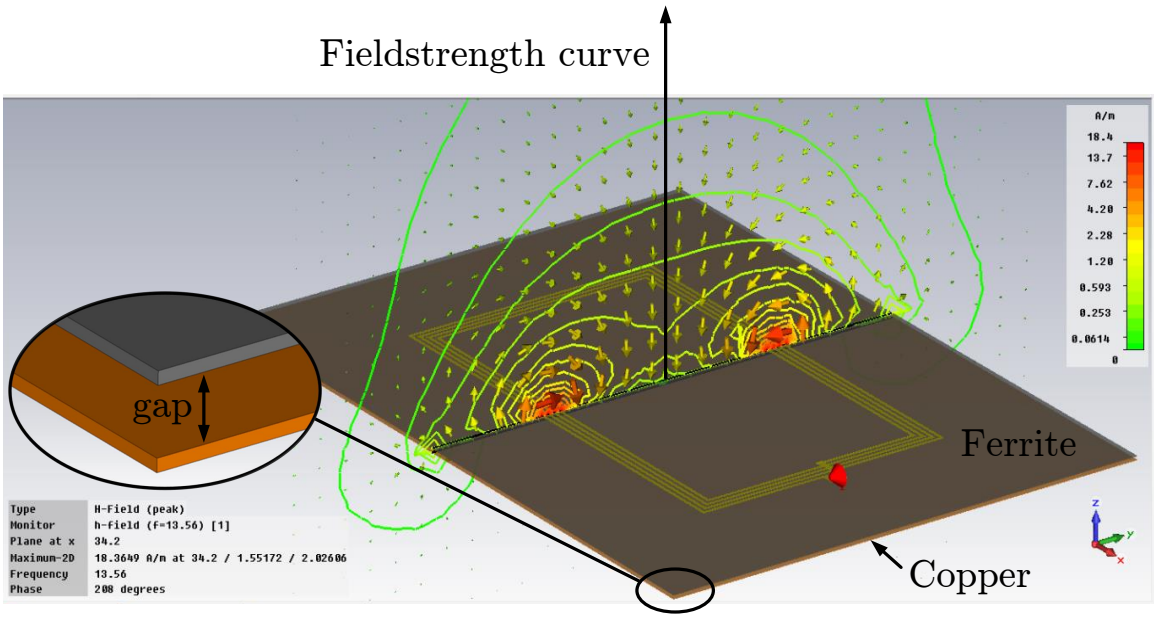


Figure 4.40: Metal environment simulation setup: A 100 μm thick copper sheet is arranged below the printed ferrite antenna. The distance between the cooper sheet and the ferrite antenna is varied between 0 and 5 mm. The magnetic field of the ferrite antenna is not significantly deteriorated by the metal environment. A small deterioration can be seen at the edges of the ferrite substrate.

Also, measurements of the two NFC tag prototypes clearly show that the ferrite antenna outperforms the photo paper antenna in a metal environment. For these measurements, the NFC chips of both tags are additionally equipped with temperature sensors. A mobile phone is used as the NFC reader that is able to read out the temperature values

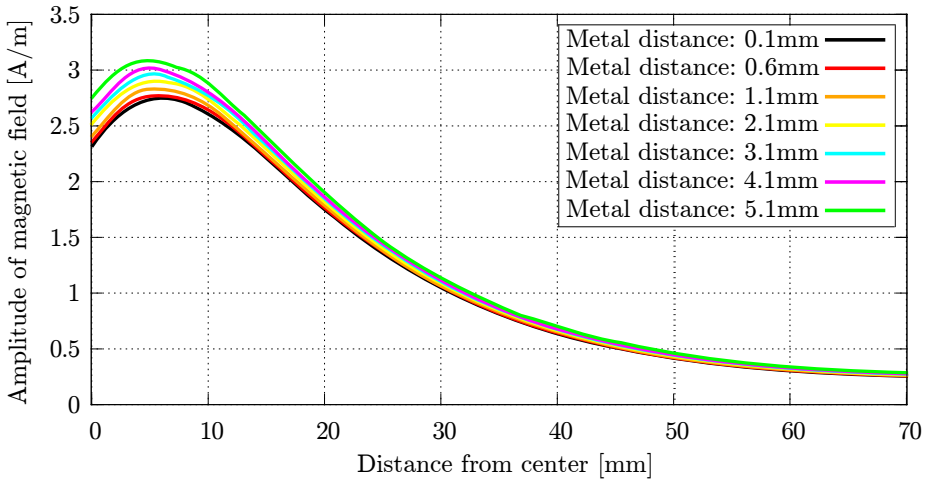


Figure 4.41: Magnetic field of the ferrite antenna for a changing metal environment: The figure shows the amplitude of the magnetic field versus the distance from the center of the antennas in z-direction for different distances $(0.1 - 5.1\text{mm})$ of the cooper sheet and the antenna. The curves shows that the magnetic field of the ferrite antenna is not significantly deteriorated by the cooper sheet.

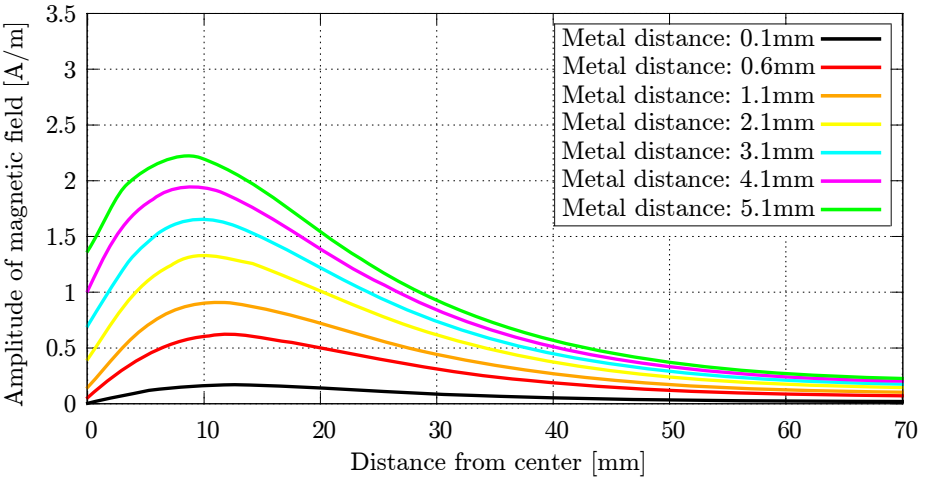


Figure 4.42: Magnetic field of the photo paper antenna for a changing metal environment: The figure shows the amplitude of the magnetic field versus the distance from the center of the antennas in z-direction for different distances $(0.1 - 5.1\text{mm})$ of the copper sheet and the antenna. The magnetic field of the paper NFC antenna is deteriorated by the cooper in the near field of the coil antenna.

of the chip. As in the simulations, a 100 μm thick copper sheet is arranged below the tag antennas. The two different measurement setups are shown in Fig. 4.43. The figure shows the temperature read out with both NFC tags. The NFC tag with the ferrite antenna can be read out while the copper sheet is directly attached to the back of the antenna, while the NFC tag with the photo paper antenna can be only read out for a spacing of 1.4 cm of the antenna and the cooper sheet. The figure also shows that the reading distance of the ferrite antenna in a metal environment is larger than the reading distance of the photo paper antenna.

Summarizing, this section presents an NFC antenna that is directly printed on a ferrite substrate using a silver inkjet printing process. Such an antenna has many advantages in terms of mechanical, economical, and electrical requirements. By printing directly on a ferrite substrate, the realization of NFC antennas with minimum thickness (of about $\approx 100\,\mu$m) is possible. A thin NFC antenna is beneficial in terms of mechanical requirements when integrating the antenna in a mobile phone. In terms of economical aspects, the silver inkjet printing process is cheaper in comparison to other fabrication processes, as e.g., an etching process [79]. The ferrite antenna meets the electrical requirements of an NFC tag or reader antenna. Simulations and measurements in a non-metal environment show that the ferrite antenna performs equally good as a custom-built NFC antenna printed on photo paper substrate. In a metal environment, the ferrite antenna clearly outperforms the photo paper antenna. Figure 4.44 underlines this fact. As can be seen the field strength is reduced significantly with an decreasing gap between paper and metal.

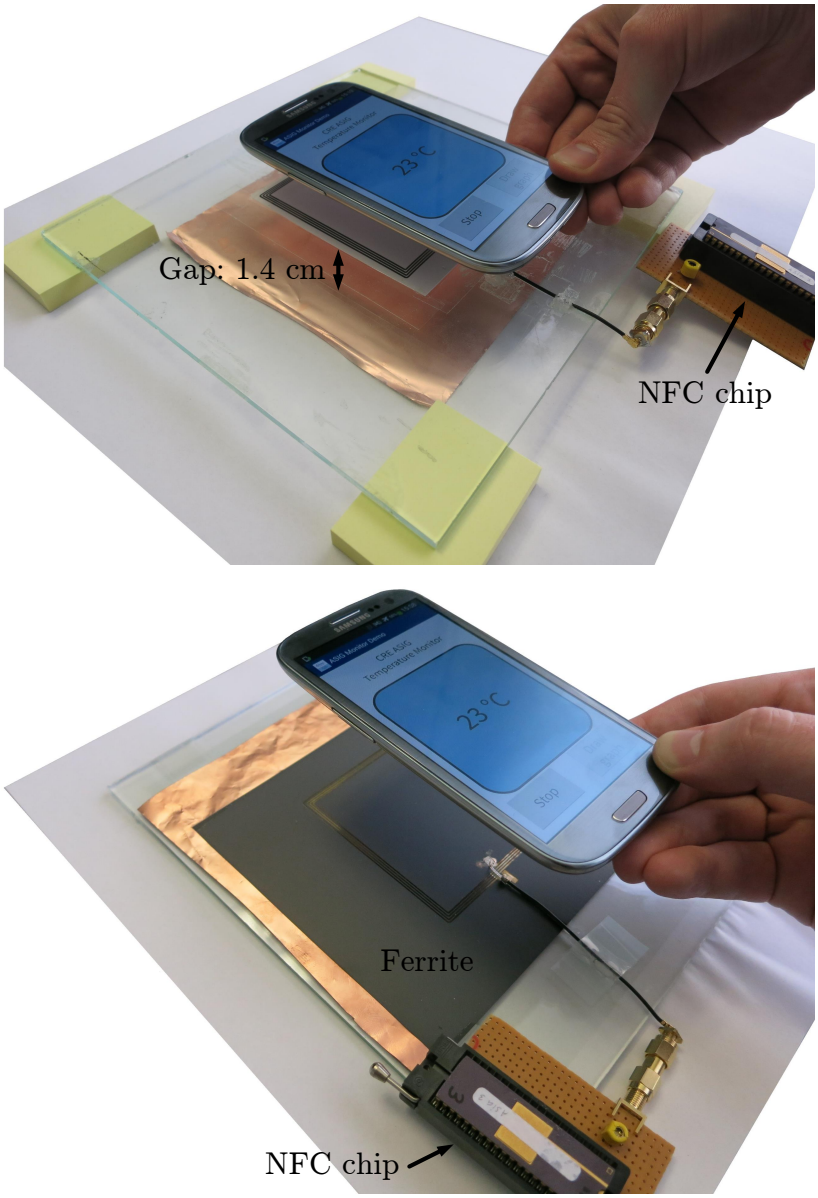


Figure 4.43: Metal environment measurement setups (upper picture: photo paper antenna NFC tag, bottom picture: ferrite antennan NFC tag: The NFC chips of both tags are equipped with temperature sensors. A mobile phone is used as the NFC reader that is able to read out the temperature values of both tags. Due to the shielding effect, the copper sheet can be directly attached to the backside of the ferrite antenna without any performance loss. In contrast, the photo paper NFC antenna has to be displaced more than 1.4 cm to achieve a similar coupling performance. The copper sheet at the back of the photo paper tag antenna clearly deteriorates the photo paper tag performance.

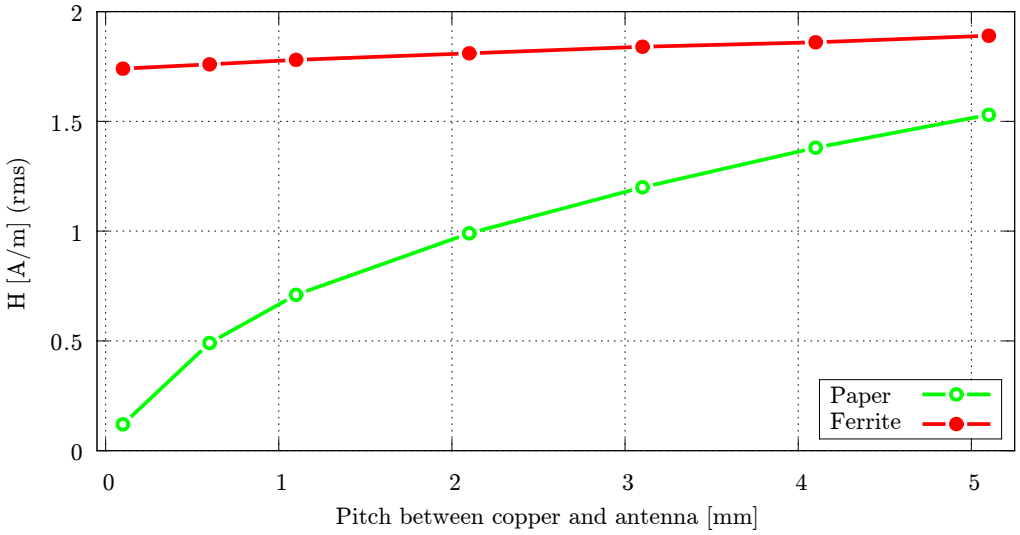


Figure 4.44: Performance comparison between paper and ferrite

Chapter 5

Conclusion

At the time of writing, RFID technology seemed to be limited to standard, galvanically connected antennas. Moreover, only a few miniaturized RFID transponders were available, and if so, typically just as a research result. Due to well-established inductive coupling technology, these types of RFID tags are equipped with coil antennas. Alternative methods, such as capacitive coupling, have been seen as inefficient. In addition, only extremely energy-efficient memory tags were deployed (e.g.[73]). There was undoubtedly a lack of miniaturization research. Moreover, the field of passive boosting technology was not sufficiently explored.

This work examines the art of miniaturized RFID tag design. As a result it uses well-established inductive coupling technology to design highly miniaturized RFID systems. Beside simulation and measurement techniques, this work introduces novel design methods, for instance to determine the equivalent sheet resistances of silicon based microchips. On-chip antennas as well as miniaturized system in packages are investigated within several hardware technologies. Thus, novel and unprecedented millimeter-scaled RFID tags are realized. The operation frequencies of the presented devices are 13.56 MHz and 868 MHz. In addition, this work examines the possibility of capacitively coupled RFID tags. Indeed, the reading distance of this coupling mechanism and overall performance is limited. However, boosting technology can be deployed to get rid of these limitations.

Until now, the field of boosting technologies was largely unexplored. Although booster antennas are applied in state of the art RFID smart cards [46], the technology was not fully matured. This work shows that there are many different booster antenna concepts in existence. Therefore four antenna classes are defined to categorize the particular booster technology. Within this work each concept was developed, investigated and proven with a demonstrator. To the author's knowledge, several concepts, such as the capacitive coupled booster antennas, are novel and presented for the very first time. To round off the topic, boosting materials are investigated. It is shown that ferrite improves the overall RFID system performance. Moreover it can be used as a substrate for silver ink-jet processes.

The author's hope is that, this work will lead to a fundamental basis for future miniaturized RFID tag developments, as well as for the up-coming booster technology.

Appendix A

Appendix

A.1 Coil on Chip Tags

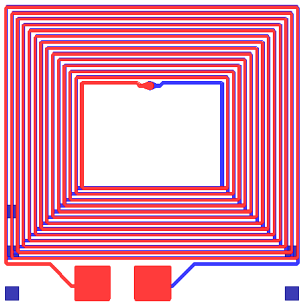
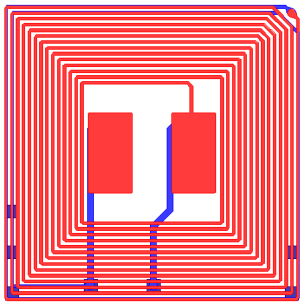
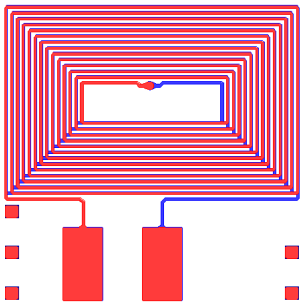
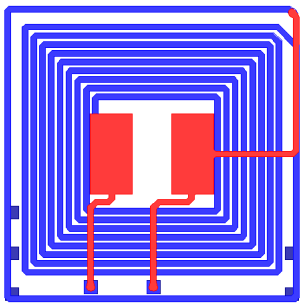
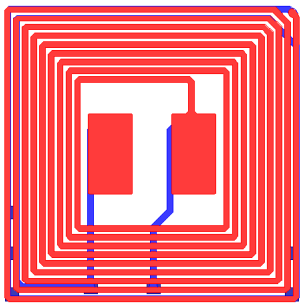
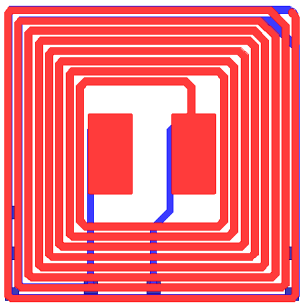
 Kap_20u20u0402	 Kap_20u20u2L	 Kap_20u20uV2
 Kap40u20u0402	 Kap40u20uV3	 myDmove20u20u

Table A.1: CoCs with Additional Pads for Capacitors

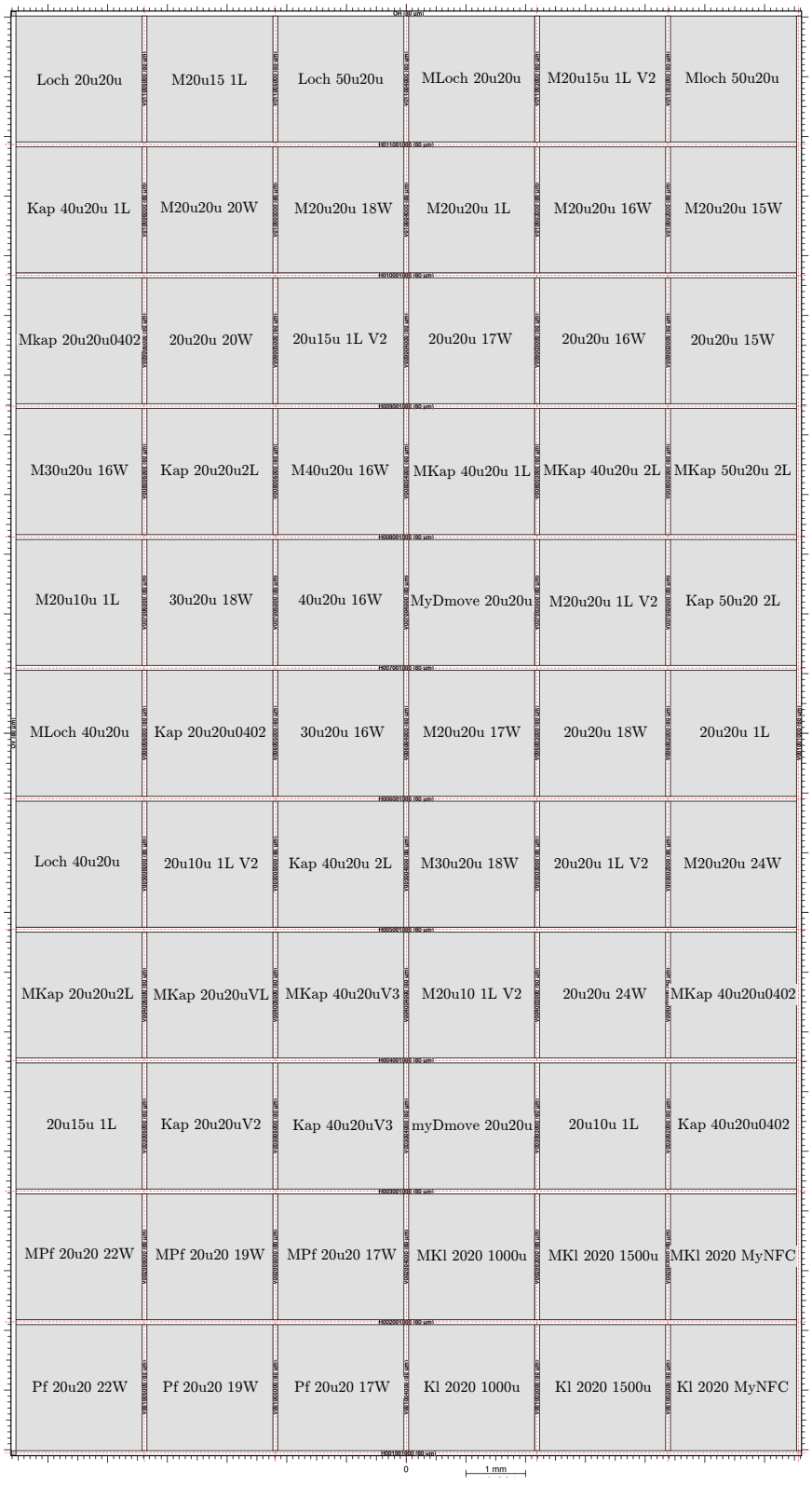


Figure A.1: produced CoC Reticle: The gap between is 80um

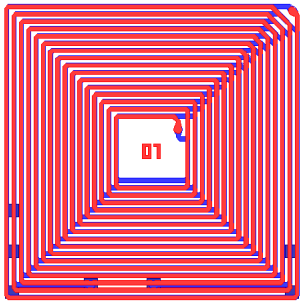
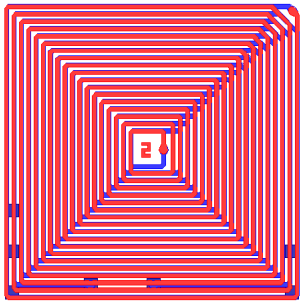
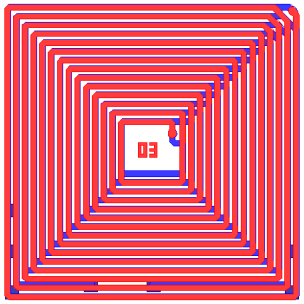
		
30u20u16W	30u20u18W	40u20u16W

Table A.2: CoCs with Increased Quality Factor due to broad lines

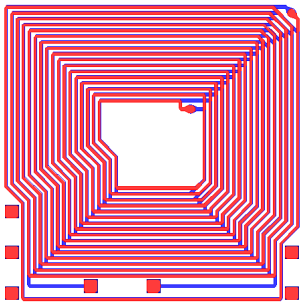
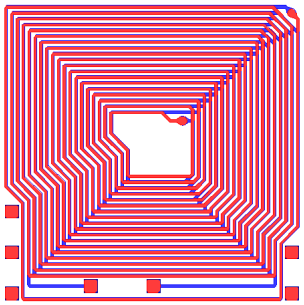
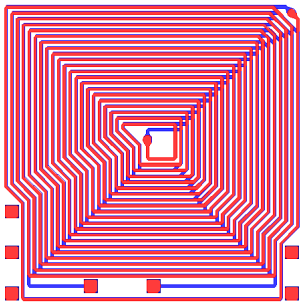
		
Pf20u20u17W	Pf20u20u19W	Pf20u20u22W

Table A.3: CoCs with reachable ISO Pads

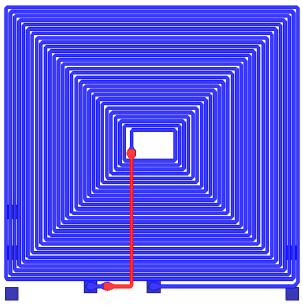
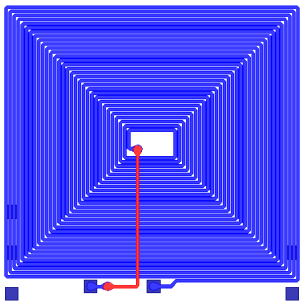
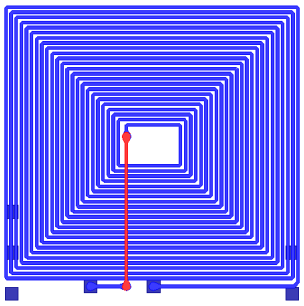
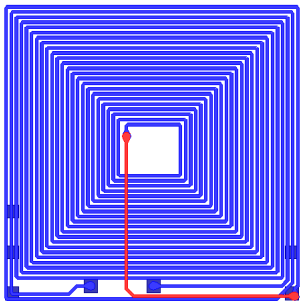
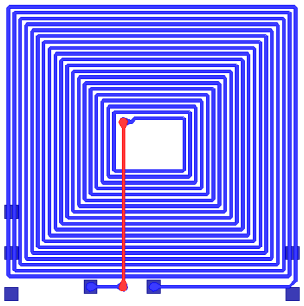
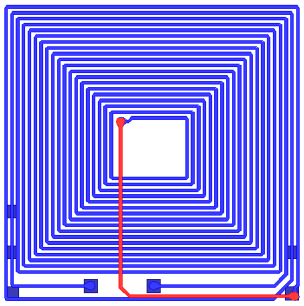
		
20u10u1L	20u10u1LV2	20u20u17W
		
20u15u1L	20u15u1LV2	20u20u1L

Table A.4: CoC with Minimum Spacing with RDL

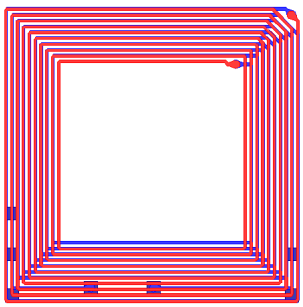
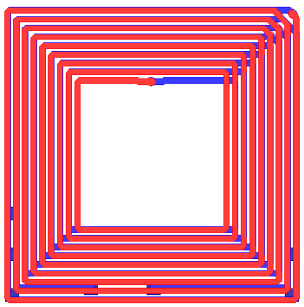
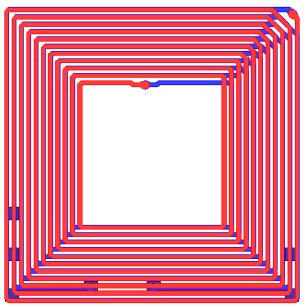
		
Loch20u20u	Loch40u20u	Loch50u20u

Table A.5: CoC with Hole to add Ferrite

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Own Publications

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Honors and Recognitions

First price in the non-student paper competition at the Loughborough Antennas and Propagation Conference with the contribution "A Silver Inkjet Printed Ferrite NFC Antenna," November 2014

Second place in the sudent contest at the IEEE RFID Technology and Applications with the contribution "A Minaturized Dual Band RFID Tag," September 2014