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Ultra-Low-Power Built-In Current Sensor for Peak Detection

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Abstract

Fully integrated systems are becoming increasingly important in modern electronic devices. For relevant quantities, the integration of components usually leads to a reduction of costs, and it can improve the performance of the circuit as well. Also, new market segments or applications might be possible with these additional opportunities.

Besides commonly used devices like different types of transistors, capacitors or resistors, new technologies furthermore allow the integration of special structures such as photo diodes, sensors, antennas or micro-electro-mechanical elements. These new possibilities are driving, among others, today's developments in the area of battery integration as well as entire on-chip energy harvesting circuits, which are using different physical principles to generate the required energy directly on the semiconductor. Wireless sensor nodes are a typical field of application, where the integration of the sensor, power supply as well as interfaces is intended. Due to the limited amount of energy, which can be currently generated and stored, this inevitably leads to the requirement of ultra-low power circuits.

The goal of this thesis was to develop an ultra-low power current sensor which is able to detect small variations of the output current delivered from a charge pump inside an energy harvesting circuit. After a short introduction about current sensor technologies and low power considerations for a typical metal oxide semiconductor (MOS) transistor, two commonly used built-in current sensor architectures will be introduced. Based on one of these topologies, the proposed current sensor was designed and will be explained in detail. The current sensor was manufactured in a 130 nm technology.

Contents

List of Tables

List of Figures

List of Abbreviations

AC	Alternating Current
BDCM	Bulk Driven Current Mirror
BJT	Bipolar Junction Transistor
CDIP	Ceramic Dual In-Line Package
CG	Common Gate
CMOS	Complementary Metal Oxide Semiconductor
CP	Charge Pump
CS	Common Source
DC	Direct Current
DP	Dominant Pole
DUT	Device Under Test
FF	Flip-Flop
GDCM	Gate Driven Current Mirror
MCU	Micro Controller Unit
MOS	Metal Oxide Semiconductor
MPW	Multi Project Waver
NDP	Non-Dominant Pole
PCB	Printed Circuit Board
PTAT	Proportional To Absolute Temperature
RF	Radio Frequency
TC	Test Chip
VCVS	Voltage Controlled Voltage Source
WSN	Wireless Sensor Node

1 Introduction

Current sensors are used in a wide range of applications in modern electronic circuits and devices. They are available as discrete components for printed circuit boards (PCBs) as well as fully integrated circuits for on-chip current measurements or circuit regulation. In general, applications for these sensor devices are battery management, current and voltage regulators, DC-DC converters, automotive power electronics or quiescent current measurements [1]. Most of these implementations require a high accuracy of the used sensor.

Different considerations need to be made for applications in the field of energy harvesting, wireless sensor nodes (WSNs) or a combination of both. A typical implementation of such a WSN based on a PCB reference design [2] is shown in Figure 1.1. The WSN contains a solar cell, a battery charger system as well as a thin film battery for the internal power supply. Moreover an ultra-low power micro controller unit (MCU) and a printed antenna are used for communications.

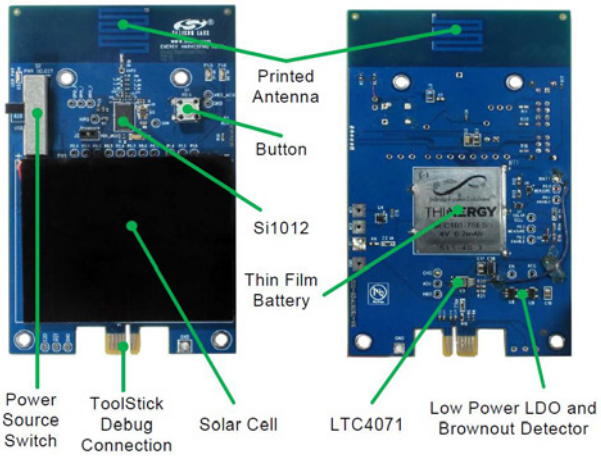


FIGURE 1.1: PCB reference design for a complete wireless sensor node including solar cell, antenna, battery charger system (LTC4071), thin film battery and ultra-low power micro controller unit with integrated transceiver (Si1012) [2].

To enable full integration, the power consumption of the individual components needs to be reduced due to the limited amount of available energy from the built-in source [3]. This is particularly important for the energy harvesting circuit itself which cannot be disabled during operation. Additional circuitry like transceivers could be activated during the communication phase only and then be disabled to reduce the power consumption of the overall circuit [4]. The reduction of the power consumption might lead to a decrease of accuracy. Therefore, new circuit concepts are required to combine reasonable accuracy with an ultra-low power consumption.

Figure 1.2 shows three main components of a typical energy harvesting system with the additional current sensor. The first element is the energy source, which can be based on light, thermal effects, vibrations or radio frequency (RF) [3], [5]. The available voltages at the output of these sensors are usually very small, therefore requiring a charge pump (CP) to generate higher voltage levels. The last building block is the storage element, which is typically a capacitor or battery. Additional circuitry (like sensors, micro controllers or transceivers), which require a higher power consumption during a short time, can be supplied using the storage element.

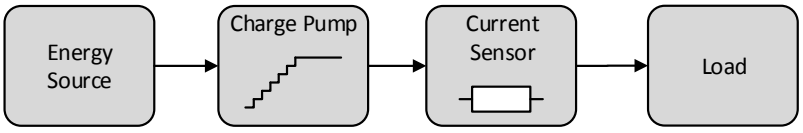


FIGURE 1.2: Block diagram for a typical harvesting system. The basic elements of such an application are an energy source, a charge pump and a storage element.

The target of this thesis was to develop a current sensor which can be used inside an energy harvesting application to monitor the output current of the charge pump. The absolute accuracy of the sensor is not a major design criterion. Nevertheless, small current changes have to be detected. The range of the input DC current can vary from 100 nA to 1 mA, which requires a high dynamic range. The current peaks which need to be detected, have an amplitude of 10 % from the DC input signal. For an input current of 100 nA, this would mean that a variation of 10 nA should be detected. A detailed specification of the peaks can be found in Table 1.1.

Parameter	Value
Input Specification	
Amplitude	min. 10 % of the DC input current
Rise/Fall Time	max. 500 µs
Frequency	typ. 500 Hz
Duty Cycle	typ. 50 %
Output Specification	
Output Voltage Change	min. 50 mV

TABLE 1.1: Specification of a typical input current peak, which should be detected. This specification results from the given application, where the current sensor will be used.

The presented specifications were done in a way so that the sensor can capture a low and a high current value during each occurrence of a peak. Inside the given application for the current sensor, it could be assumed that the detectable peaks have the same phase as the main system clock.

The designed circuit should be fabricated inside a standard 130 nm process without any additional components or technology options (except special digital cells which will be explained in section 5.4.5).

2 Fundamentals

Nowadays, many different current sensor types and architectures can be found on the market. Finding the right architecture for a given application is one of the most important steps during the design phase of a current sensor. Table 2.1 shows the most commonly used architectures, their possibilities for integration inside a semiconductor circuit as well as their robustness in case of extreme operation conditions during a fault scenario [6], [7].

Measurement Method	Accuracy	Isolation	Robustness	Integration
Resistive (Direct)				
Sense Resistor	High	No	High	High
Inductor DC Resistance	Low	No	High	Moderate
Transistor (Direct)				
RDSon	Low	No	Moderate	High
Current Mirror	Moderate	No	Moderate	High
Magnetic (Indirect)				
Current Transformer	High	Yes	High	Moderate
Rogowski Coil	High	Yes	High	Moderate
Hall Effect	High	Yes	Moderate	Moderate

TABLE 2.1: Comparison of different current sensor architectures based on their key parameters and their capabilities for integration [6], [7]. The sensors were separated into direct (resistive and transistor based) and indirect sensor types.

More information about the classification of current sensors and on their measurement methods can be found in section 2.1. The integration of a measurement method depends on the complexity of the used technology, the possible implementation as well as the required area.

2.1 Fundamentals of Current Sensing Circuits

Due to the wide range of current sensor applications and the fact that there are several different types of sensors available, it may become important to specify certain categories, which help to identify the best sensor architecture for a given application. All available sensors can be classified as shown in Figure 2.1.

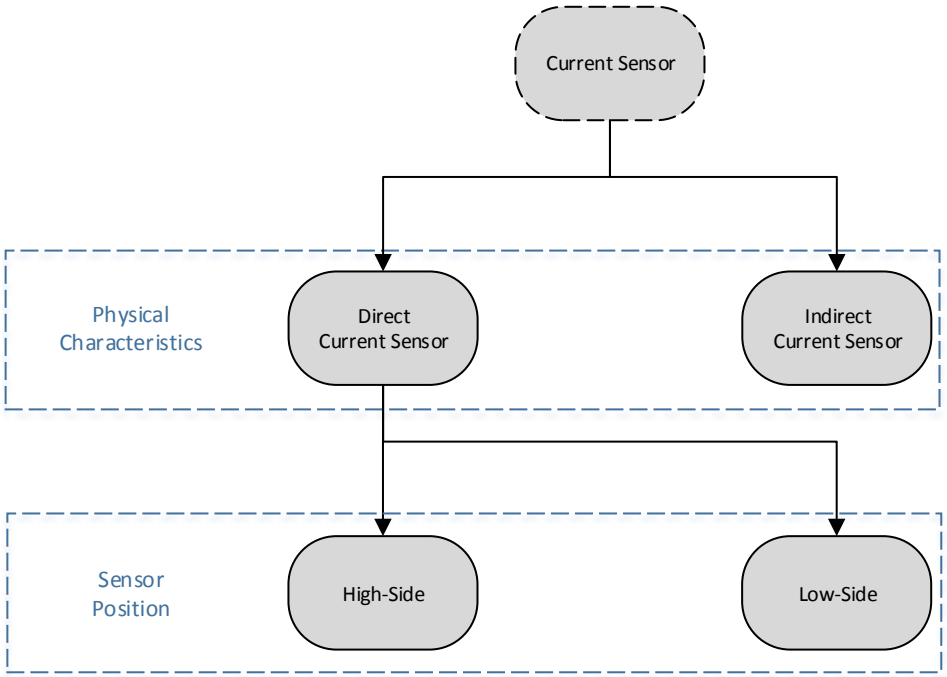
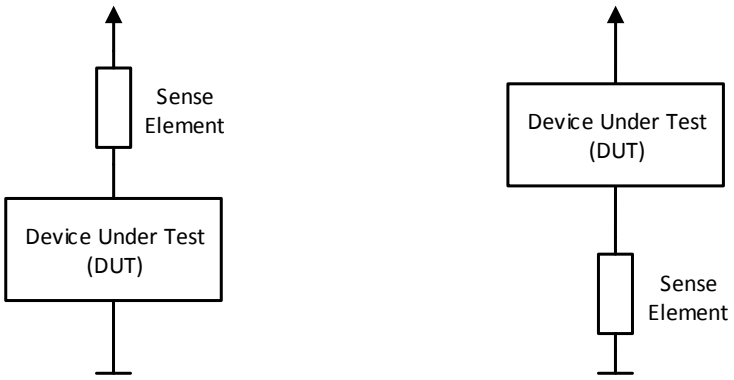


FIGURE 2.1: Overview of current sensor classifications based on their physical measurement principle as well as their actual position inside the system [8].

One major parameter is the physical measurement concept on which the sensor is based [8]. The first approach is to measure the current by generating a copy of the signal to be measured or, respectively, a proportional voltage. This topology is called direct current sensor. On the other hand, the current could also be measured based on the resulting magnetic field. This is called indirect current sensor.

One advantage of the indirect current sensor is the fact that it is isolated from the measurement path which is not possible in case of a direct sensor. The main disadvantage here is the need of a coil or any other magnetic sense element that can be fabricated [7], but it requires more complex technologies or implementations. Furthermore, indirect current sensors can measure only AC currents (except hall sensors), whereas direct types can measure AC as well as DC currents [6]. The interface with the magnetic sense element might be more complex as well, which would require additional circuitry.



(a) High-side sense element. (b) Low-side sense element.

FIGURE 2.2: Basic concept of a high-side and a low-side current measurement. Schematic diagram for the position of the sense element related to the device under test for a high-side (2.2(a)) as well as low-side (2.2(b)) configuration.

The second classification can be done depending on the position of the sense element inside the system [9]. Figure 2.2 shows two positions of the sense element related to the device under test (DUT). For a high-side current sensor, the sense element will be connected directly at the high supply voltage and the DUT to ground (or the low supply voltage). For a low-side current measurement, the arrangement needs to be swapped. As the magnetic field generally does not depend on the position of the sense coil or element, this applies only to indirect current sensors.

Using these classifications, the analyzed current sensor used inside this thesis can be defined as an indirect high-side current sensor. The most popular circuit implementations for such a sensor will be discussed within the next chapters.

2.1.1 Shunt Resistor

The first concept is based on the conversion of the input current to a proportional voltage as explained in section 2.1. Figure 2.3 shows one of the most popular sensor architectures [1], [10] based on a sense resistor. The current to be measured causes a voltage drop at the sense resistor R_{Sense}, which then can be used for further analysis. The output voltage can be calculated as

$$V_{Out} = A\, R_{Sense}\, I_{Sense} \tag{2.1}$$

where A is the gain of the amplifier, V_{Out} the output voltage R_{Sense} the sense resistor and I_{Sense} the current to be measured.

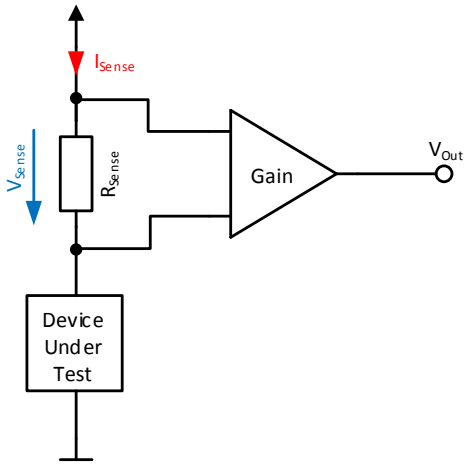


FIGURE 2.3: Architecture of a resistor-based high-side current sensing circuit including amplifier for signal conditioning and/or magnification.

Resistor-based current sensors are used very often, in particular because of their simple architecture, high accuracy and low cost characteristics [1]. For higher input current ranges, the resistor limits the operating range due to the increasing sense voltage. Additional resistor stages could be implemented to reduce this influence.

A very similar approach has already been used for a long time where the resistor is replaced by a diode-connected bipolar junction transistor (BJT) [11]. The collector current of a bipolar transistor can be calculated as [12]

$$I_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right)\left(1 + \frac{V_{CE}}{V_A}\right) \tag{2.2}$$

where I_C is the collector current, I_S the saturation current, V_{BE} the base emitter voltage, V_T the thermal voltage, V_{CE} the collector emitter voltage and V_A the early voltage. The base emitter voltage can be rewritten, under the assumption that $V_{CE} \ll V_A$, as

$$V_{BE} = \ln\left(\frac{I_C}{I_S}\right) V_T \tag{2.3}$$

This logarithmic relation between the base emitter voltage and the current allows a bigger input range for the sensor with the disadvantage of a non-linear output signal.

2.1.2 Current Mirror

The second measurement architecture is based on generating a copy of the current as explained in section 2.1. These types are typically based on current mirrors or similar architectures. They can be found quite often inside complementary metal oxide semiconductor (CMOS) driver circuits and also quiescent current measurements. Although the basic idea is similar in both application scenarios, the architectures have one major difference, which will be explained later in this chapter.

The drain current for a metal oxide semiconductor (MOS) transistor can be represented in a very general form as a function of the gate source voltage [13].

$$I_D = f(V_{GS}) \tag{2.4}$$

where I_D is the drain current and V_{GS} the gate source voltage. On the other hand, if the transistor is driven by a given drain current, this leads to a gate source voltage which is a function of the drain current [13].

$$V_{GS} = f^{-1}(I_D) \tag{2.5}$$

This relationship can be used for the circuit in Figure 2.4 under the assumption that the drain and source voltages of both transistors are equal. This leads to

$$I_{\text{sense}} = f f^{-1}(I_{\text{drive}}) \tag{2.6}$$

where I_{sense} is the sense current and I_{drive} the driving current for the load.

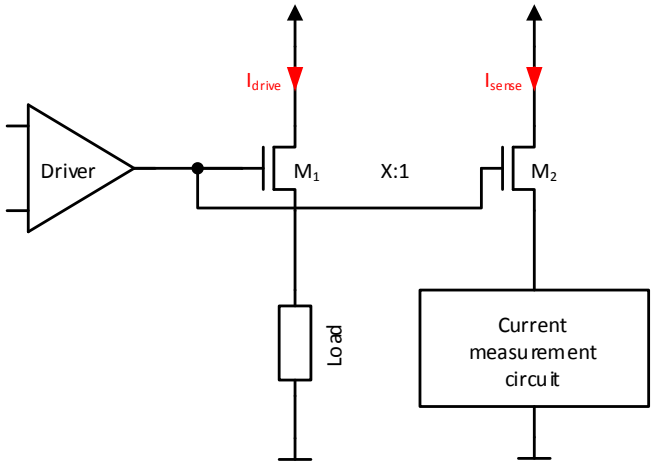


FIGURE 2.4: Current sensor example for high-side driver including drive (M_1) and measurement (M_2) transistor with an aspect ratio X:1.

As shown in Figure 2.4, the current measurement path is separated from the main driving path which remains unchanged. Nevertheless, typical applications still have a dependency of the driving path mainly due to regulation of the drain/source potentials of the transistors, which can be seen in Figure 3.2. This is a basic example for a current measurement circuit inside a high-side driver [14]. Also, bigger current ranges can be detected using different aspect ratios for the drive and sense transistors. Typically, such a measurement approach is preferred due to the fact that no modifications are required on the main current path.

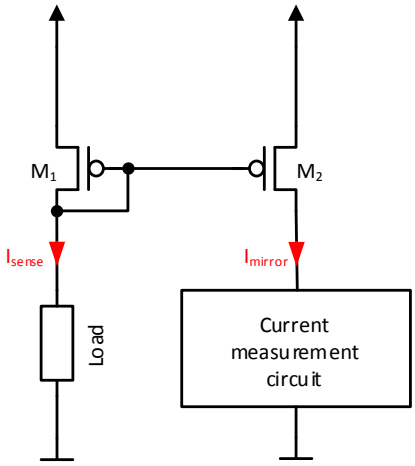


FIGURE 2.5: High-side current sensor using M_1 and M_2 as basic current mirror.

In other cases, like quiescent current measurements, using an already existing transistor might not be feasible. This leads to a typical current mirror inside the measurement path as shown in Figure 2.5. The disadvantage of this topology is the fact that this adds an additional voltage drop of $V_{TH} + V_{DS,sat}$ (without additional circuits to reduce this voltage drop and under the assumption that M_1 operates in saturation) to the measurement path. Here V_{TH} is the threshold voltage of M_1 and $V_{DS,sat}$ is the drain source saturation voltage of M_1.

2.1.3 Gate Back Circuit

The gate back circuit [14], [15] is a small modification of the resistor-based current sensor, which was introduced in section 2.1.1. Figure 2.6 shows the basic concept including the sense transistor M_{Sense} and the driver for the gate voltage. Compared to the resistor-based architecture, the sense element was replaced by a transistor working inside the linear region.

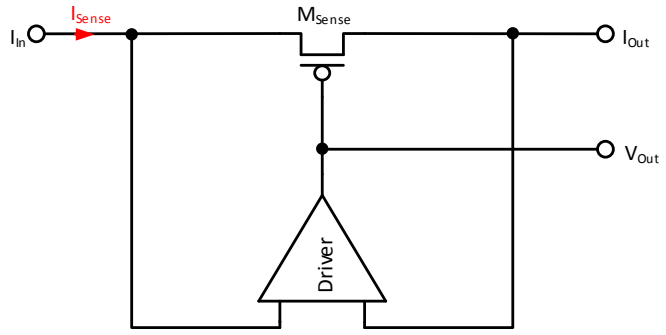


FIGURE 2.6: Gate back current sensor including driver and sense transistor. M_{sense} is controlled by the driver to work inside the linear region.

The drain current for the sense transistor can be calculated using [13]

$$I_D = K' \frac{W}{L} \left[(V_{GS} - V_{TH})\, V_{DS} - \frac{V_{DS}^2}{2} \right] \tag{2.7}$$

where K' is the transconductance parameter (based on the mobility of the charge carriers and the gate oxide capacitance), W and L are the dimensions of the transistor, and V_{DS} is the drain source voltage. Assuming that the driver keeps the drain source voltage at a constant level (which needs to be $\neq 0$), the resulting gate voltage can be calculated as

$$V_{GS} = I_D \frac{L}{K' W\, V_{DS}} + \frac{V_{DS}}{2} + V_{TH} \tag{2.8}$$

which can be simplified, under the assumption that $V_{DS} << V_{TH}$, to

$$V_{GS} = I_D \frac{L}{K' W\, V_{DS}} + V_{TH} \tag{2.9}$$

Equation 2.9 shows that the gate source voltage can be taken as measurement signal that is proportional to the drain current.

2.2 CMOS Transistor in Weak Inversion

For a basic understanding of a CMOS transistor, the device is typically considered to be either turned on ($V_{GS} \geq V_{TH}$) or off ($V_{GS} < V_{TH}$). Unfortunately, the transition between both states is not ideal because of remaining charges inside the channel. Also, it is not possible to fully turn off the device, which would mean that no more current is flowing. Figure 2.7 shows the drain current depending on the gate source voltage [16]. Below a certain gate voltage, the drain current starts to decrease logarithmically by approximately one decade of I_D per 80 mV drop of the gate source voltage [13].

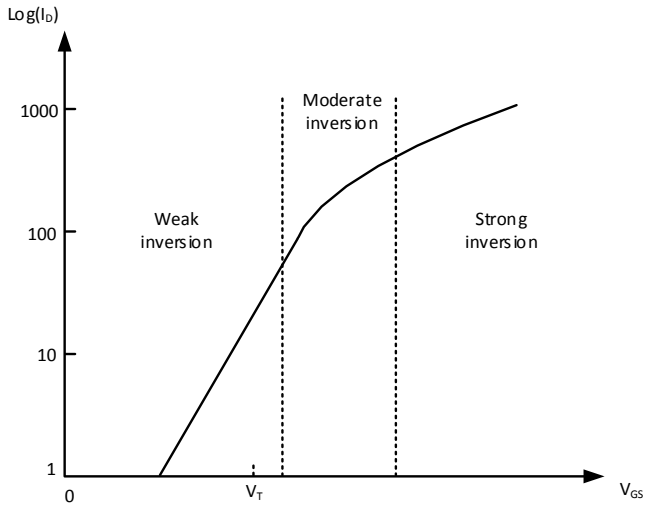


FIGURE 2.7: Inversion regions for a MOS transistor including strong, moderate and weak inversion. The drain current dependency on the gate source voltage is shown with a logarithmic y-axis.

The drain current for a transistor inside weak inversion is given by [12]

$$I_D = \frac{W}{L} I_{D0} \exp\left(\frac{V_{GS} - V_{TH}}{n\,V_T}\right)\left[1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right] \tag{2.10}$$

where n is the the subthreshold slope factor which is typically between one and three [16], and I_{D0} is a process dependent drain saturation current. Here, it is assumed that $V_{DS} > V_T$ which leads to a simplified equation for the drain current which is given by [12]

$$I_D = \frac{W}{L} I_{D0} \exp\left(\frac{V_{GS} - V_{TH}}{n\,V_T}\right) \tag{2.11}$$

Depending on the definition of I_{D0}, different forms for 2.11 can be found in the literature. A second commonly used version of the equation can be found by including the threshold voltage inside the process parameter I'_{D0}, which leads to [17]:

$$I_D = \frac{W}{L} I'_{D0} \exp\left(\frac{V_{GS}}{n\,V_T}\right) \tag{2.12}$$

Equation 2.12 might be preferred in case the parameter I'_{D0} is determined by a simulation or measurement. In this case, the gate source voltage could be connected to ground and the resulting drain current can be used to evaluate I'_{D0}. Nevertheless, compared to 2.11, the effects of the threshold voltage can not be seen easily anymore in 2.12. Based on 2.12 it seams that the drain current is independent of the threshold voltage which is not true due to the fact that the influence is included in a different drain saturation current I'_{D0}.

The weak inversion region starts approximately at [16]

$$V_{GS} < V_{TH} + n\,V_T \tag{2.13}$$

This point may vary as well depending on the chosen literature. Nevertheless it is always in the range of the threshold voltage. Besides other differences between the strong and weak inversion region, there is another very important difference for the transconductance. The transconductance g_m can be calculated based on equation 2.10, which leads to [12]

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{I_D}{n\,V_T} \tag{2.14}$$

Compared to the transconductance inside the strong inversion region [12]

$$g_m = \frac{2}{V_{GS} - V_{TH}} = \frac{2}{V_{OV}} \tag{2.15}$$

there is only a dependency on the slope factor and the thermal voltage but not on the overdrive voltage V_{OV}. Also, the slope of 80 mV gate source voltage per decade of drain current is a very important characteristic for a transistor inside the weak inversion region.

3 State-of-the-Art Solutions

For the following chapter, two frequently used current sensors were analyzed. Their basic functions will be explained, as well as their major advantages and disadvantages. The gate back circuit will be discussed and analyzed in the next chapter since this approach will be used for the proposed solution and therefore analyzed afterwards.

3.1 Bulk-Driven Current Mirror

As already mentioned in section 2.1.2, a basic current mirror, often also called gate-driven current mirror (GDCM), would introduce an additional voltage drop inside the measurement path. To keep this influence, and the consequential losses, as small as possible, additional circuits or different current mirror topologies need to be used. One very common architecture, especially within the area of quiescent current measurements or ultra-low power applications, is therefore the bulk-driven current mirror (BDCM).

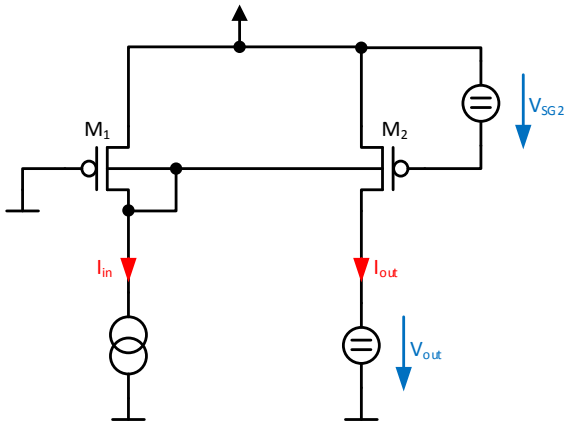


FIGURE 3.1: PMOS bulk-driven current mirror with M_1 inside the linear region and M_2 inside saturation.

Figure 3.1 shows the basic circuit for a PMOS bulk-driven current mirror [18]. The gate of M_1 is connected to ground to keep the transistor inside the linear region to reach a small drain source voltage for M_1. On the other hand, the gate of M_2 is connected to a certain bias voltage to keep the transistor within saturation. This keeps the current more stable related to voltage variations at the output. Nevertheless, the gate of M_2 could be connected to ground as well, to improve the mirror ratio with the disadvantage of a bigger dependency on the output voltage. Besides the shown circuit, different architectures can be found in the literature [18], [19] which are working on the same principle. Conventional circuit concepts like cascodes are also possible for a BDCM [20]–[22].

To derive the transfer function of the BDCM shown in Figure 3.1, the relation between the drain current and the bulk source voltage needs to be derived for both transistors. The drain current for a transistor operating inside the linear region can be written as [23]

$$I_D = K' \frac{W}{L} \left((V_{SG} - V_{TH})\, V_{SD} - \frac{n\, {V_{SD}}^2}{2} \right) \tag{3.1}$$

where the subthreshold slope factor n can be written as [23]

$$n = 1 + \frac{\gamma}{2\sqrt{2\Phi_F - V_{SB}}} \tag{3.2}$$

where γ is the channel length modulation, Φ_F the flat band potential, V_{SB} the source bulk voltage, V_{SG} the source gate voltage and V_{SD} the source drain voltage. The dependency of the drain current on the bulk source voltage can be seen by looking at the threshold voltage, which can be written as [24]

$$V_{TH} = V_{TH0} \pm \gamma \left(\sqrt{2|\Phi_F| - V_{SB}} - \sqrt{2|\Phi_F|} \right) \tag{3.3}$$

where V_{TH0} is the threshold voltage at zero V_{SB}. Using 3.1, 3.2 and 3.3 the bulk source voltage for M_1 can be written as [23]

$$V_{SB,1} \approx \frac{I_{\text{in}}}{K'_1 \frac{W_1}{L_1} (V_{SG,1} - V_{TH0,1})} \tag{3.4}$$

Using 3.1 and 3.3 for the output transistor with the generated bulk source voltage from 3.4, the relation between the input and output current can be calculated. This leads to

$$I_{\text{out}} \approx K' \frac{W_2}{L_2} \frac{1}{2\, n} \left(V_{SG,2} - V_{TH0} + \frac{\gamma}{2\sqrt{2\Phi_F}} \frac{I_{\text{in}}}{K' \frac{W_1}{L_1} (V_{SG,1} - V_{TH0})} \right)^2 \tag{3.5}$$

assuming identical process parameters for both transistors. The bias voltage $V_{SG,2}$ of the output transistor M_2 could be decided to be in the range of V_{TH0} which might minimize the additional offset ($V_{SG,2} - V_{TH0}$) with the disadvantage of more complex biasing.

Using this type of architecture, the voltage drop can be reduced below 50 mV, depending on the aspect ratio [19]. Also, the fast detection time (for example inside quiescence measurements [23]) is a big advantage of this concept. A major disadvantage of the architecture shown in Figure 3.1 is the high non-linearity of the circuit [23].

3.2 Gate Back Circuit

Figure 3.2 shows a typical application for the gate back circuit [15] inside a high-side PMOS driver. To measure the current through M_1, a part of this current (X:1) can be mirrored into a separate branch by M_2. At low currents, the drain source voltage drops below a certain level which can be in the range of the offset voltage of the operational amplifier OP_2 (which regulates together with M_3 the drain voltage of M_2).

To avoid this, the drain source voltage can be kept above the offset voltage (inside the shown example above 40 mV which includes already a certain headroom) by using an additional operational amplifier OP_1.

If the drain source voltage of M_1 drops below the reference level, OP_1 regulates the driver so that the gate voltage for M_2 and M_1 will be increased. This leads to a higher resistance and therefore to an increase in the drain source voltage.

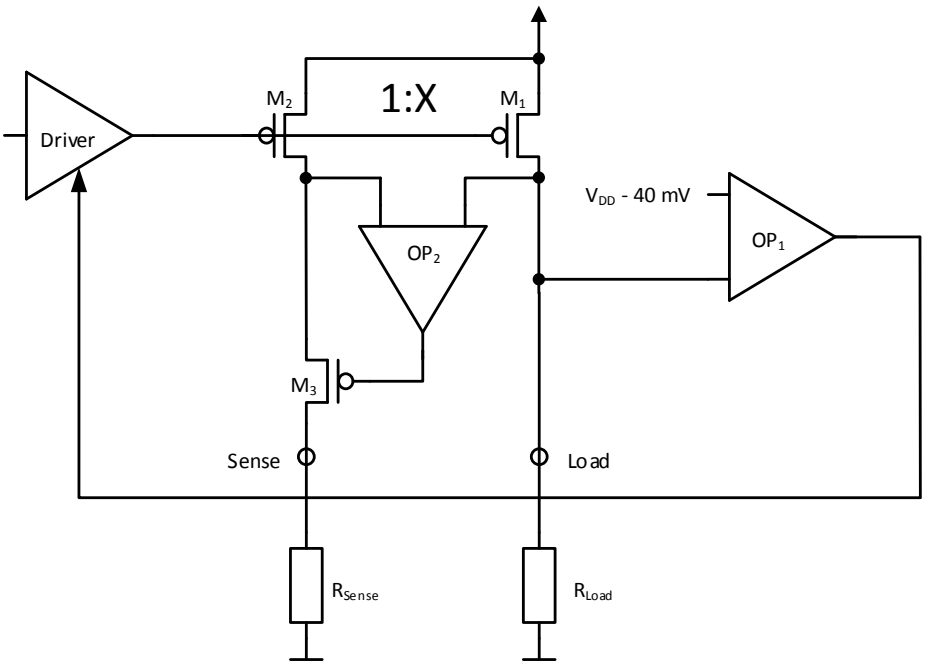


FIGURE 3.2: Typical application for a gate back circuit using a regulated gate driver for drain source voltage regulation. The load transistor M_1 and the sense transistor M_2 are driven by OP_1 in a gate-back configuration.

The ability of a higher linearity (which can be seen in 2.9) compared to the bulk-driven current mirror as well as the possibility of also reaching small values for the drain source voltage are the main reasons for choosing a gate back architecture for the proposed current sensor.

4 Proposed Solution

Within the next section, the proposed circuit will be introduced and the detailed function explained. The concept will be separated into two major parts; the current measurement circuit and the control signal generation. The main requirements on these blocks will be analyzed, as well as the power supply concept and the clocking scheme.

4.1 Concept

The chosen topology is based on the gate-back architecture as explained in section 3.2. Figure 4.1 shows the complete circuit block diagram including bias current generation.

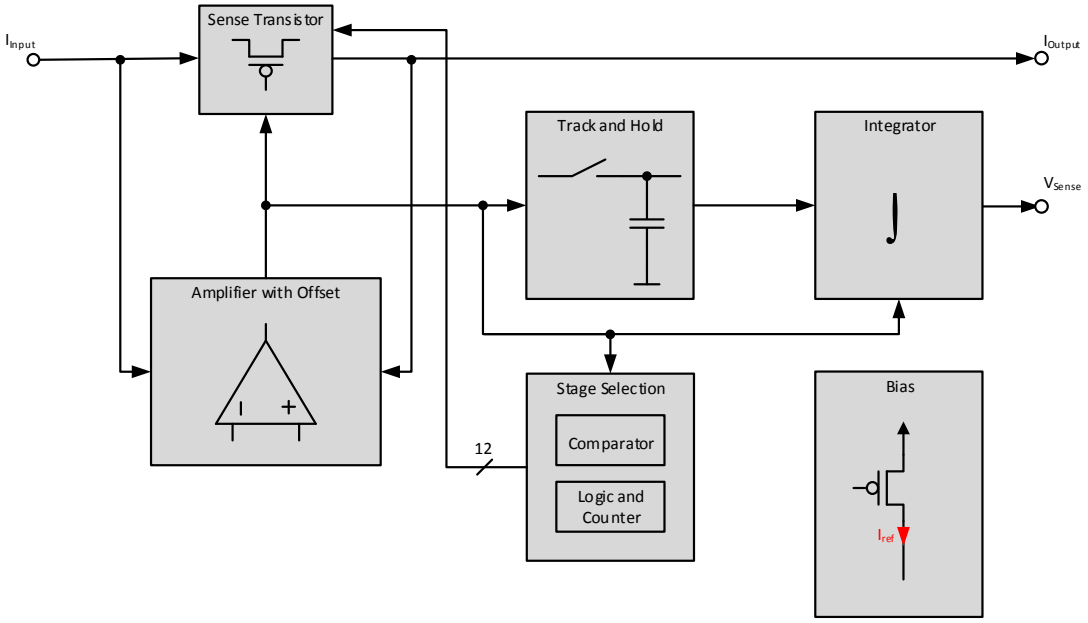


FIGURE 4.1: Block diagram of the complete current sensor based on the gate back architecture with additional control signal generation and bias circuitry. Orange marked blocks are related to the current sensor itself whereas blue marked blocks are related to the control signal generation.

The complete current sensor can be separated into two different circuit blocks. The main sensor (marked orange) translates the input current into a proportional voltage and keeps the voltage drop across the sense element at a constant level. The control signal generation circuit (marked blue) converts the information from the current sensor to a specific output voltage signal depending on the given specification.

4.2 Power Supply Concept

The energy harvesting circuit includes two separate charge pumps. The first one contains a small number of stages and generates the supply for all digital blocks, which is in the range of 600 mV to 800 mV. This voltage is independent from the load conditions of the harvesting circuit and therefore more stable than the high supply voltage. The second charge pump generates the output voltage for the battery which can vary, depending on the current value of the battery, and can reach a maximum of 4 V. Table 4.1 shows the worst-case supply voltage levels for the digital as well as the analog domains.

Specification	Vdd_{Dig}	Vdd_{Ana}
Minimum	600 mV	2 V
Maximum	800 mV	4 V

Table 4.1: Worst-case specifications for the analog and digital supply domains.

Level shifters will be used for the signals that are required within both supply domains. Except digital cells, most of the transistors are designed to work under higher voltage condition. Therefore, no special symbols will be used for these types of transistors in the circuit explanations during this thesis. In case both types of transistors were used within a circuit, the devices for the high supply (analog transistors) will be marked with a thicker gate or mentioned explicitly.

One additional major difference between the two supply voltage domains is the available maximum current which can be delivered from the CP. Compared to the analog supply, the digital domain cannot drive high currents. During normal operation, this has no influence on the circuit, since only leakage current will be required, which is typically in the range of less than 10 nA. However this effect needs to be taken into account especially during start-up, where the digital supply voltage can also be in the range of less than 600 mV which could lead to unstable operating points and therefore higher leakage currents. This means that high current peaks (dynamic losses) need to be avoided.

4.3 Building Blocks

The overall system can be separated into two functional blocks. The first section is the current sensor itself, which regulates the sense transistor and generates a certain gate voltage. The second block converts this gate voltage into a control signal required for the charge pump. Within the two following sections, the main requirements for these functional blocks will be discussed.

4.3.1 Current Sensor

The current sensor consists of a sense transistor, an amplifier and a stage selection. The sense transistor and the amplifier are working inside a gate-back configuration, which keeps the drain source voltage of the sense transistor at a certain level. In addition to the main measurement function, the PMOS transistor should withstand different input and output voltage scenarios as well. Depending on the current value of the battery and the output voltage from the charge pump, either the input or the output voltage of the sensor can have a higher potential. This requires additional circuitry to drive the bulk of the PMOS which should be always on the highest potential.

The stage selection controls the number of sense elements to keep the voltage drop at the defined value at all times. This was done using two comparators for the high and low switching level and a bidirectional counter.

4.3.2 Control Signal Generation

The control signal generation detects a current peak and generates the required voltage at the output of the circuit. The used concept is based on the given requirements related to the peaks occurring, but could be modified to fulfill different control signal demands. For the currently used concept, the gate voltage is compared with a sampled gate voltage, which was taken during the previous half clock period. The difference will be used to charge or discharge a load capacitor. The gate voltage and the sampled value will be interchanged at the input of an amplifier which reduces the effect resulting from errors especially at the track and hold circuit (like charge injection or offsets of the buffer amplifiers).

Although a simple comparator could be used to digitally evaluate the gate voltage and detect a current peak, the specifications and the implementation of the sensor inside the energy harvesting circuit requires an analog concept to generate the output signal of the sensor.

5 Circuit Implementation

In the next section, each block will be analyzed in detail. The main focus will be on the current measurement part of the sensor, however, the control signal generation circuits will be explained as well. All transistors, excepting those in digital standard cells or if mentioned otherwise, are analog transistors which are able to work under the high supply domain conditions.

5.1 Bias

Bias circuits are among of the most essential building blocks inside modern CMOS circuits. One common architecture is the constant-gm bias circuit [13], which was used inside the proposed current sensor as well.

Due to the ultra-low power requirements, a resistor was used instead of a topology without a resistor [25] which would require additional circuitry. Also, concerning area considerations, the resistor is much smaller compared to the remaining energy harvesting circuit, which makes it possible to also use resistors with bigger values.

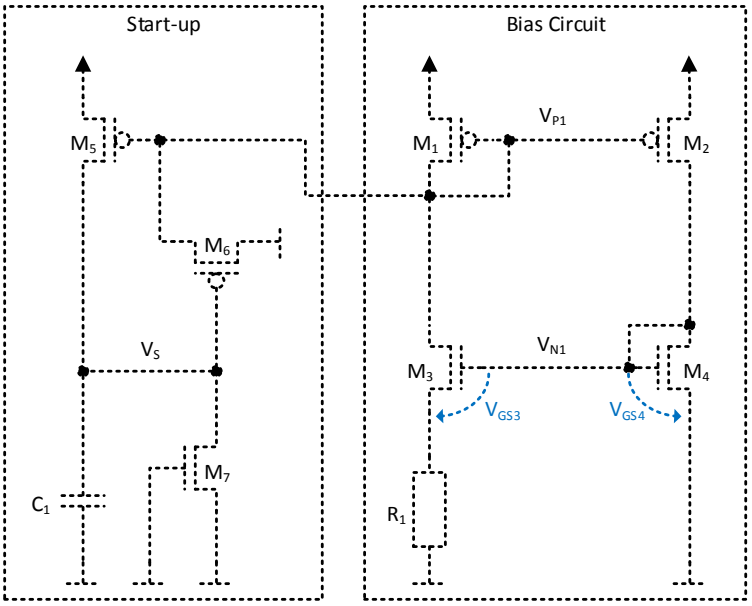


FIGURE 5.1: Basic architecture of the reference current generation including start-up circuit [26].

The currents inside the bias circuit will be calculated for a better understanding. The drain current for an MOS transistor inside the subthreshold region can be expressed as shown in 2.10.

Unfortunately, this equation will not be accurate in case of a constant-gm biasing as shown in Figure 5.1 due to the fact that the source and bulk of M_3 are not connected. Including this effect, the drain current can be calculated as [27]

$$I_{DS} = \frac{W}{L} I_{D0} \exp\left(\frac{V_G}{n V_T}\right) \left[\exp\left(-\frac{V_S}{V_T}\right) - \exp\left(-\frac{V_D}{V_T}\right)\right] \tag{5.1}$$

where V_G is the gate potential, V_S the source potential and V_D the drain potential of the transistor.

Assuming that $V_D > V_T$, the drain current can be expressed as

$$I_{DS} = \frac{W}{L} I_{D0} \exp\left(\frac{1}{V_T}\left(\kappa V_G - V_S\right)\right) \tag{5.2}$$

where κ is the back-gate coefficient, which can be written as $1/n$. Assuming that the currents in both branches are equal, this leads to

$$\frac{W_3}{L_3} I_{D03} \exp\left(\frac{1}{V_T}\left(\kappa_3 V_{N1} - I_{R1} R_1\right)\right) = \frac{W_4}{L_4} I_{D04} \exp\left(\frac{1}{V_T}\left(\kappa_4 V_{N1}\right)\right) \tag{5.3}$$

where I_{R1} is the current through the resistor R_1. Assuming that the technology dependent parameters κ are equal for both transistors and $W_3/L_3 = M\, W_4/L_4$, the drain current for one transistor (which will then be used as bias current) can be written as

$$I_{D,M3} = I_B = \ln(M) \frac{V_T}{R_1} \tag{5.4}$$

where $I_{D,M3}$ is the drain current of the transistor M_3, and I_B the resulting bias current from the circuit. The bias circuit inside this design was dimensioned to 1 nA, which requires a resistor of approximately 30 MΩ.

The temperature dependency of the output current is also a very important characteristic. Taking 5.4 and considering explicitly the temperature coefficients, this would lead to

$$I_B = \ln(M) \frac{k\,T}{q} \frac{1}{R_0\left(1 + \alpha\left(T + T_0\right)\right)} \tag{5.5}$$

where k is the Boltzmann constant, T the temperature, q the elementary charge, α the linear temperature coefficient of the resistor (neglecting higher order temperature coefficients), R_0 the given resistor value at a reference temperature and T_0 the corresponding reference temperature. Based on this equation, the dependency can now be calculated using:

$$\frac{d\,I_B}{d\,T} = -\ln(M) \frac{k}{q} \frac{\left(T_0\,\alpha - 1\right)}{R\left(1 - T_0\,\alpha + T\,\alpha\right)^2} \tag{5.6}$$

It can be seen that the dependency is also related to the current value of the absolute temperature. Nevertheless this influence is rather small and can be neglected for a first approximation. In this case, the temperature variation is only dependent on the part of the thermal voltage (which is the dominant part) and the temperature coefficient of the resistor.

Another important point (especially for bias circuits) is the start-up behavior. Considerations are required in case that there are two possible stable operating points for a circuit. Typically, these are the intended point of operation and another one, where the internal nodes are either at the supply voltage or ground. The used start-up circuit was based on the architecture presented in [26].

Looking only at M_1 - M_4 and R_1, the circuit might have a stable point which would prevent the bias circuit from starting. An initial condition is assumed, where the gates of M_1 and M_2 are at the supply voltage level and the gates of M_3 and M_4 are at ground potential. In this case, no current would flow inside both branches, which would be a stable point as well. To overcome this situation, the start-up circuit consisting of M_5 - M_7 and C_1 needs to be added, considering the previously mentioned initial condition as well as the gate of M_7 at the supply voltage level. In this situation, M_5 would cause no current from the mirror M_1 and M_2, and the capacitor C_1 would be discharged over the leakage current source M_7. Once the voltage on the capacitor reaches approximately one threshold below the supply level, M_6 starts to conduct and pulls the gate voltage of the current mirror M_1 and M_2 towards ground, which forces the bias circuit to start. Additionally, this also causes a current through M_5 which then charges the capacitor C_1 again until it is fully charged. In this state, only the leakage current of M_7 will flow through M_5. It is important to keep the leakage current of M_7 always below the desired bias current value. If this is not the case, the higher leakage current can lead to an increased bias current. This is particularly important for high temperatures.

5.2 Sense Transistor

One main element for a current sensor is the sense element. A PMOS type of transistors is used inside the proposed high-side current sensor. The basic circuit including the bulk regulation is shown in Figure 5.2.

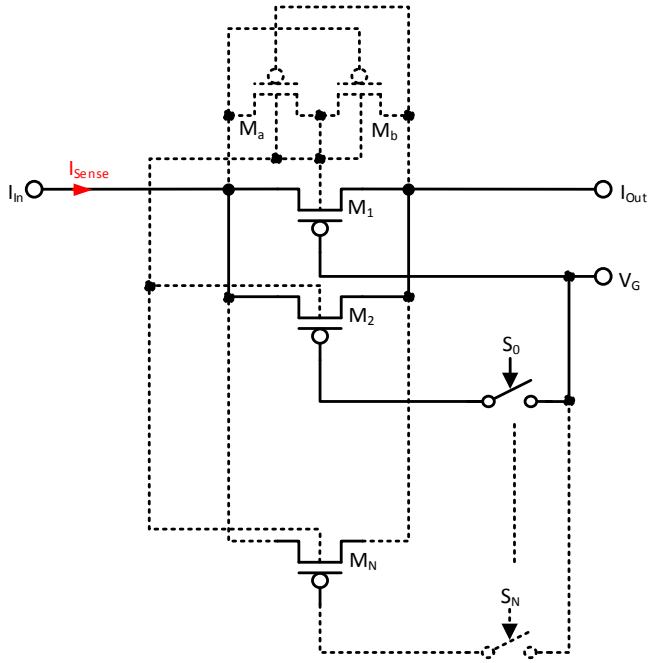


FIGURE 5.2: PMOS sense transistors including bulk regulation and switches for stage selection. In case a certain switch is open, the corresponding gate is connected to the positive supply voltage.

Especially for high-side drivers, NMOS transistors will be used for a long time due to their higher mobility [14], which would result in a lower on resistance [28]. Unfortunately, NMOS high-side transistors would require a gate voltage higher than the input, which would lead to additional circuitry like bootstrap circuits [28] or a charge pump. To overcome this drawback, PMOS transistors were used as high-side sense element. In any case, the advantage of such an ultra-low resistance is not required inside the application.

The PMOS itself is separated into several elements (M_1 to M_N) where N is the number of used stages. The gate voltage of a transistor inside the linear region can be expressed by

$$V_{GS} = \frac{I_D}{K' M V_{DS}} + \frac{V_{DS}}{2} + V_{TH} \tag{5.7}$$

where M is the width-to-length ratio of the transistor. To calculate the required maximum ratio for the specified current range and the number of stages, 5.7 needs to be rewritten, which results in

$$M = \frac{2 I_D}{K V_{DS} (2 V_{GS} - V_{DS} - 2 V_{TH})} \tag{5.8}$$

Taking 5.8, the maximum width-to-length ratio M can be calculated for the current of 1 mA, which results in a ratio of approximately 1000. Switching from one stage to the next, the ratio M changes to a new value. These factor between two following dimension ratios need to be calculated.

Thus a factor c was introduced which was defined as

$$M_{n+1} = c\, M_n \tag{5.9}$$

where M_n is the aspect ratio for the transistor with smaller width, M_{n+1} for the next stage with the larger width and c the factor between both ratios. This leads directly at the switching point to (using 5.7)

$$V_{GS,n} - V_{GS,n+1} = \Delta V_{GS} = \frac{I_{D,n}}{K'\, M_n\, V_{DS}} - \frac{I_{D,n+1}}{K'\, c\, M_n\, V_{DS}} \tag{5.10}$$

Assuming that the drain current stays constant during the switching of the stage and equal V_{DS}, V_{TH} and K' for both stages, this can be simplified and the factor c expressed by

$$c = -\frac{I_D}{\Delta V_{GS}\, K'\, M_n\, V_{DS} - I_D} \tag{5.11}$$

Assuming ΔV_{GS} to be 0.6 V, this results in a factor c of approximately 2. Based on this factor, the number of stages can be calculated:

$$N = \mathrm{ld}\left(\frac{I_{D,max}}{I_{D,min}}\right) = \mathrm{ld}(10000) \approx 13 \tag{5.12}$$

The main limitation of ΔV_{GS} is the minimum possible supply value, especially at low temperatures. Increasing ΔV_{GS} would decrease the number of stages, but also the margin between the comparator reference values and the supply rails (positive rail and ground). The margin to the positive supply rail is more important due to the fact that the sense PMOS transistor should be kept inside the linear region. Considering a different factor than two, the total number of stages could be calculated using [29]

$$\log_b(r) = \frac{\log_a(r)}{\log_a(b)} \tag{5.13}$$

where $\log_a$ is the logarithm with base a. This would result in approximately 8 stages for a factor of three. Nevertheless, to be able to reach supply voltage levels down to 2 V, the factor of two was chosen.

Depending on the current flowing through the measurement path, the transistors M_2 to M_N will be turned on or off. Within the regulated state (where the drain source voltage reaches the desired value), the input voltage will be always higher than the output voltage (by the defined offset of the operational amplifier). Nevertheless, the output voltage might at some point be higher than the input voltage. This can be the case if, for example, a fully loaded battery is attached to the circuit and the charge pump is switched on. In this case, the bulk voltage of the PMOS transistor needs to be regulated in order to avoid forward biased parasitic diodes. This can be done by using the transistors M_a and M_b [30], [31]. Figure 5.3 shows the cross section of these two transistors.

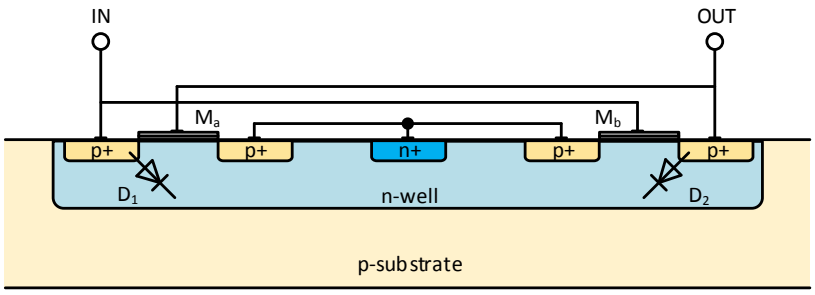


FIGURE 5.3: Cross section of the PMOS sense transistor including parasitic diodes at the input and output of the sense element.

Assuming a higher voltage (of at least on threshold voltage) at the input compared to the output, the gate source voltage of M_a will switch the transistor on and connect the input to the n-well of the transistors. In case the output voltage increases at least one threshold above the input voltage, M_a will be switched off and M_b will conduct, connecting the n-well potential to the output. Assuming a difference voltage smaller than V_{TH} between the input and the output, both transistors are working as a voltage divider with a resistance in the GΩ range, connecting the n-well between the input and output voltage. This could result in a small positive voltage on D_1 or D_2, but this voltage is below the forward voltage of the diodes, which keeps the leakage current small.

5.3 Input Amplifier

Figure 5.4 shows the basic architecture of the input amplifier. It is a two stage amplifier with a common gate (CG) input stage (M_1 and M_2) followed by a common source (CS) stage (M_5) and an active current mirror (M_3 and M_4) as load for the CG structure. The required offset for the amplifier is defined by the aspect ratios for M_1 and M_2.

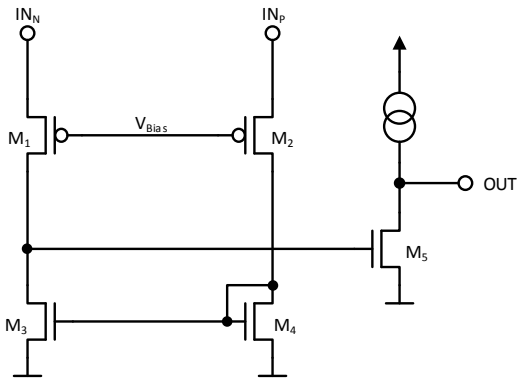


FIGURE 5.4: Input amplifier for the sense element. Basic architecture consists of an input common gate stage with current mirror load followed by a common source stage.

To get the required offset for the operational amplifier, the width and length ratio of the input pair needs to be calculated.

Based on 2.11 we can write the drain currents for both branches and set them equal (due to the current mirror load), which results in:

$$\frac{W_1}{L_1} \exp\left(\frac{V_{GS1} - V_{TH1}}{n\,V_T}\right) = \frac{W_2}{L_2} \exp\left(\frac{V_{GS1} - V_{TH2} - V_{\text{offset}}}{n\,V_T}\right) \tag{5.14}$$

assuming that both threshold voltages are the same and that

$$\frac{W_2}{L_2} = m\,\frac{W_1}{L_1} \tag{5.15}$$

This leads to

$$m = \exp\left(\frac{V_{\text{offset}}}{n\,V_T}\right) \tag{5.16}$$

where m is the required ratio between M_1 and M_2. For a first calculation, n can be considered to be one which would result for a required offset of 20 mV in a ratio of $m \approx 2$.

Now assuming a constant ratio, the equation can be rewritten to

$$V_{\text{offset}} = \ln(m)\; n\,V_T \tag{5.17}$$

which shows the linear dependency of the offset voltage related to the thermal voltage. At the worst-case temperature of −40 °C this would result in an offset voltage of 13.9 mV.

5.3.1 Open Loop Gain

The small signal gain for the CG can be written as [32]

$$a_v = \left(\frac{g_{m1} + g_{m2}}{2}\right)(r_{ds3} || r_{ds1}) \tag{5.18}$$

and for the CS as [32]

$$a_v = g_{m5}\,R_{\text{out}} \tag{5.19}$$

where R_{out} is the output resistance of the CS. Under the assumption that the output resistance of the current source is much higher than r_{ds5}, this equation can be simplified to

$$a_v = g_{m5}\,r_{ds5} \tag{5.20}$$

The transfer function of the sense transistor can be written as

$$\frac{V_{DS}}{V_{GS}} = g_m\,r_{ds} \tag{5.21}$$

where g_m and r_{ds} are the transconductance and the drain source resistance of the sense transistor. This results in an overall gain of

$$a_v = \frac{(g_{m1} + g_{m2})}{2}\,\frac{1}{g_{ds3} + g_{ds1}}\,g_{m5}\,r_{ds5}\,g_m\,r_{ds} \tag{5.22}$$

5.3.2 Poles and Zeros

Finding the position of poles and zeros inside a circuit becomes more difficult with increasing complexity. Nevertheless, it is helpful to know at least the most important poles and zeros of the system and where they are located inside the circuit. For the proposed amplifier, only the dominant pole (DP) and the none dominant pole (NDP) will be discussed. Further information on other poles can be found in the literature (for example [13]).

The input amplifier contains two poles where the DP can be found at the output of the CS stage and the NDP at the output of the CG stage. Looking at the common source stage, the frequency for the dominant pole can be found at [13]

$$f_{pd} = \frac{1}{2\,\pi\,R_{\text{out}}\,C_L} \tag{5.23}$$

where R_{out} is the output resistance of the CS stage and C_L the load capacitance at the output. Using a load capacitance of 3 pF and the assumption that $r_{ds,5} \ll r_{\text{source}}$, this leads to a DP at a frequency of approximately 2.6 Hz.

For the NDP, the calculation can be done similarly using 5.23 where R_{out} is now the output resistance of the CG stage and C_L the capacitance at the output node of the CG stage (input of the CS stage). Again assuming that $r_{ds,1} \ll r_{ds,3}$ and that the load capacitance is mainly defined by the gate capacitance of M_5, this leads to a frequency for the NDP of approximately 9 kHz.

It can be seen that the poles are placed at very low frequencies (especially the dominant pole) which is due to the ultra-low power considerations of the circuit.

Based on the calculations of the open loop gain and the position of the DP and NDP, the Bode diagram of the circuit can be plotted, as it is shown in Figure 5.5.

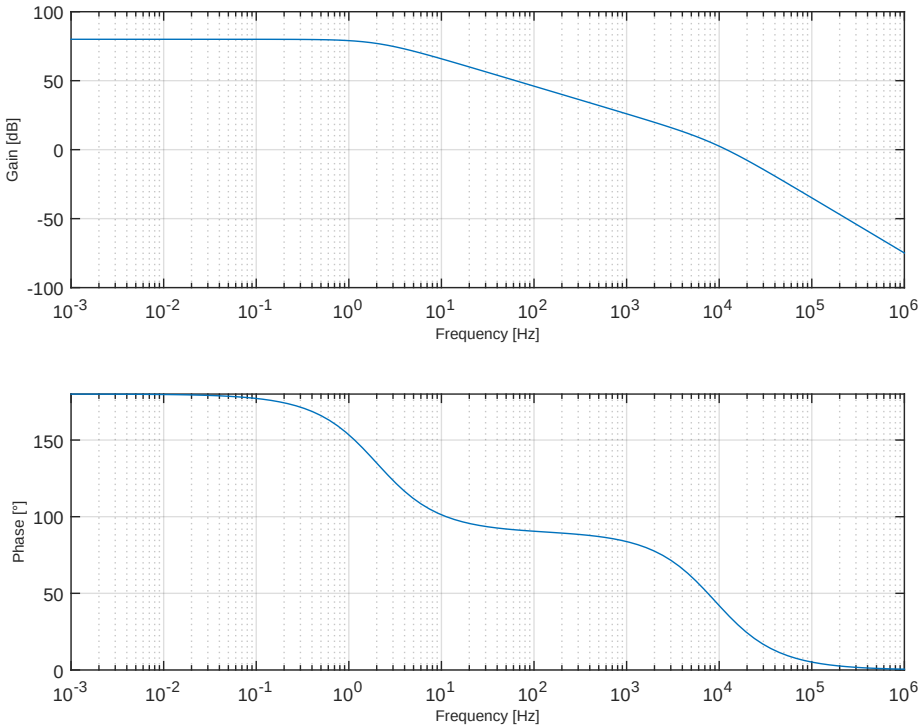


FIGURE 5.5: Calculated Bode diagram for the amplifier including sense transistor. The Bode diagram was based only on the dominant and non-dominant pole.

5.4 Stage Selection

Depending on the input current, different sense transistor dimensions are required to keep the drain source voltage at a constant level. The stage selection circuit compares the current gate voltage of the sense transistor with two reference voltages and drives the required elements accordingly. In case the gate increases above a certain level, a counter will be reduced by one bit, and the biggest sense transistor will be switched off. In case the gate voltage decreases below a reference level, the counter will be increased by one bit, and the next stage of the sense transistor will be added. Two clocked comparators were used for the comparison and one synchronous bidirectional counter for the stage selection. Instead of one rail-to-rail comparator (for example [33]), two single comparators with PMOS and NMOS input pairs were used. The benefit of a rail-to-rail solution is basically the reduction of a second latch with the cost of additional and more complex logic and circuitry.

Inside the current design, a four-bit counter was implemented which generates a 12-bit thermometer code (see chapter 5.4.5). Compared to the calculation, 12 stages instead of 13 will be used. To reduce the number of stages compared to the calculated value, ΔV_{GS} was slightly increased to reduce the number of stages. Figure 5.6 shows the block diagram of the stage selection circuit including comparators and the control logic.

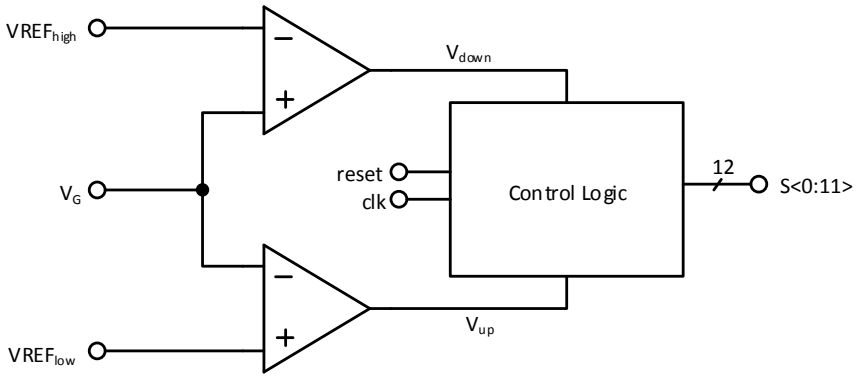


FIGURE 5.6: Overview of the stage selection including comparators and control logic for the generation of the thermometer code based on a 4-bit counter.

5.4.1 Clocking Scheme

The clocked comparators are directly connected to the gate of the sense transistor. The ultra-low power requirements result in a poor slew rate of the amplifier. Therefore, the gate requires a certain amount of time to reach the desired voltage level. This is particularly important after a current peak occurs at the input of the sensor. To avoid comparator decisions during the rising or falling edge of the gate voltage, the clocks for these blocks are shifted by 90 degrees compared to the main system clock. Inside the used application for the current sensor it can be assumed that the peaks have the same phase as the main system clock. Figure 5.7 shows the four main clock signals used inside the system.

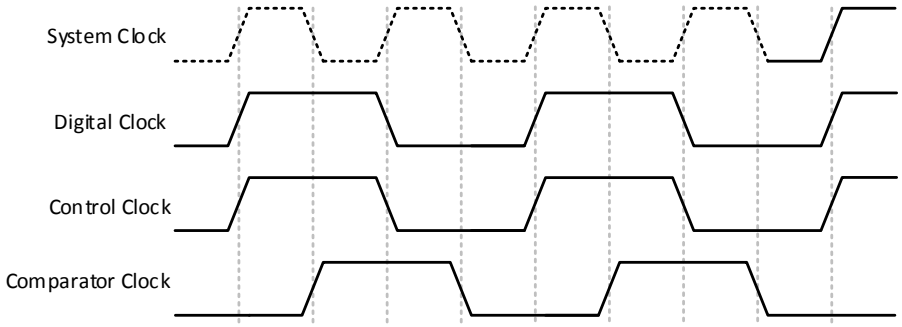


FIGURE 5.7: Timing diagram of the available clock signals including system, digital, control and comparator clock.

The three required clock signals for the current sensor are based on the system clock, which is generated by the CP. The frequency of this clock depends on the CP and was defined as 1 kHz. Based on this signal, the digital clock and the control clock were generated with a frequency of 500 Hz. Furthermore a 90 degree shifted clock was generated for the comparators. Additionally to the frequency and phase of these clocks, they are also inside different power supply domains.

Table 5.1 gives an overview about the used clock signals.

Clock Purpose	Name	Frequency [Hz]	Phase Shift [°]	Supply Domain
System Clock	clk_in	1000	0	digital
Digital Clock	clk_dig	500	0	digital
Control Clock	ctrl	500	0	analog
Comparator Clock	comp	500	90	analog

TABLE 5.1: Overview about the used clock signals, their frequencies and phase shifts compared to the input clock and supply domain.

Figure 5.8 shows the basic circuit of the clock signal generation. It is based on two data flip-flops (FF) to generate the required signals. The output inverter for the ctrl_n signal must be an analog inverter to be able to operate at the higher supply voltage. The input and the digital clock are at the digital supply domain, whereas the remaining control and comparator clocks are at the analog supply domain, which requires additional level shifters.

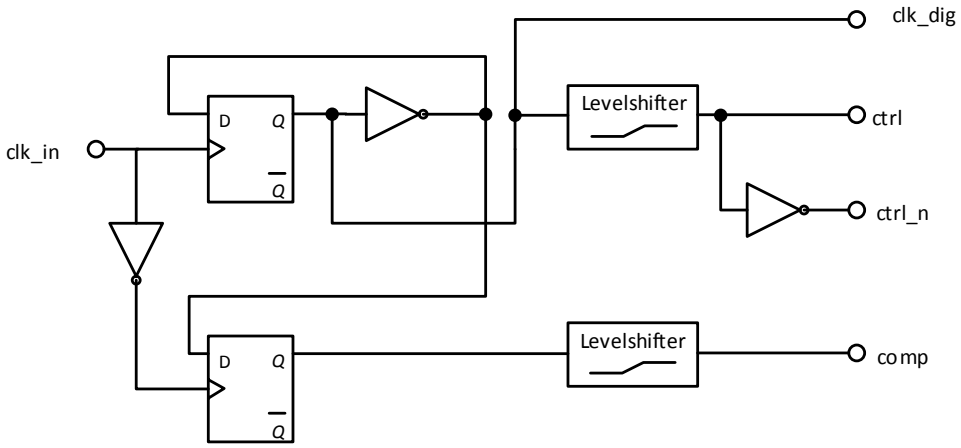


FIGURE 5.8: Clock generation circuit based on the given system clock. The output inverter for the ctrl_n signal must be an analog inverter due to the higher supply voltage after the level shifter.

5.4.2 Reference Voltage

The reference voltage for the comparators defines the switching points for the sense transistor. This does not require a high accuracy, it is, however, important to keep the additional supply current that is required by the reference circuit as small as possible. Improvements on the accuracy of the reference voltage are only necessary in case a smaller minimum supply is to be achieved.

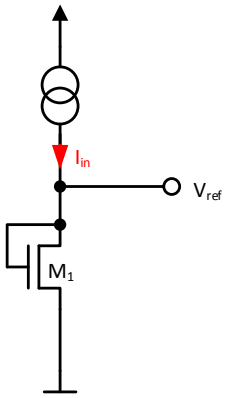


FIGURE 5.9: Reference voltage generation using a current source with a diode-connected transistor as load.

Figure 5.9 shows the basic concept for the reference voltage generation. It is one of the most simple solutions to provide a reference voltage based on a bias current. M_1 is working as a diode-connected transistor, where the gate source voltage will be the resulting reference, which can be calculated, based on 2.12, as

$$V_{\text{ref}} = \ln\left(\frac{I_{\text{in}}}{I_{D0}}\frac{L}{W}\right) V_T \tag{5.24}$$

One major limitation of the reference voltage is its temperature dependency. Looking at 5.24, two temperature dependent parameters can be found: The threshold voltage has a negative dependency which is in the small mV range (typically 2 mV) [32], whereas the dependency of the thermal voltage can be calculated using k/q, which is in the range of $86.2\,\mu\text{V}\,\text{K}^{-1}$. This results in an overall negative temperature dependency of the reference voltage. Detailed analysis as well as a voltage reference with improved temperature stability can be found in [34].

5.4.3 Comparator

Two different comparators were used for the higher and lower reference value. In the following chapter, the circuit will be explained based on a comparator with PMOS input pair. It is based on the proposed design presented in [33]. Figure 5.10 shows the comparator circuit.

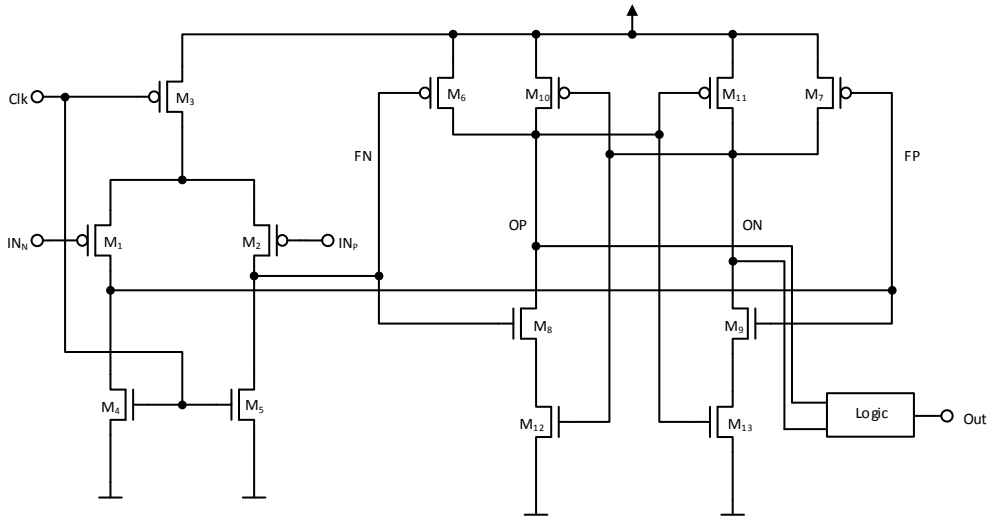


FIGURE 5.10: Comparator with a PMOS input preamplifier stage followed by a latch. The logic for the output signal generation is based on a RS-Flip-Flop.

The basic architecture is a two-stage design with a one gain stage (M_1 to M_5) and a latch (M_6 to M_{13}) as second stage. For a detailed analysis of the block, Figure 5.11 can be used, which shows the behavior of the important nodes during the time when the decision is done. The output logic circuit is based on a RS flip-flop (RS-FF).

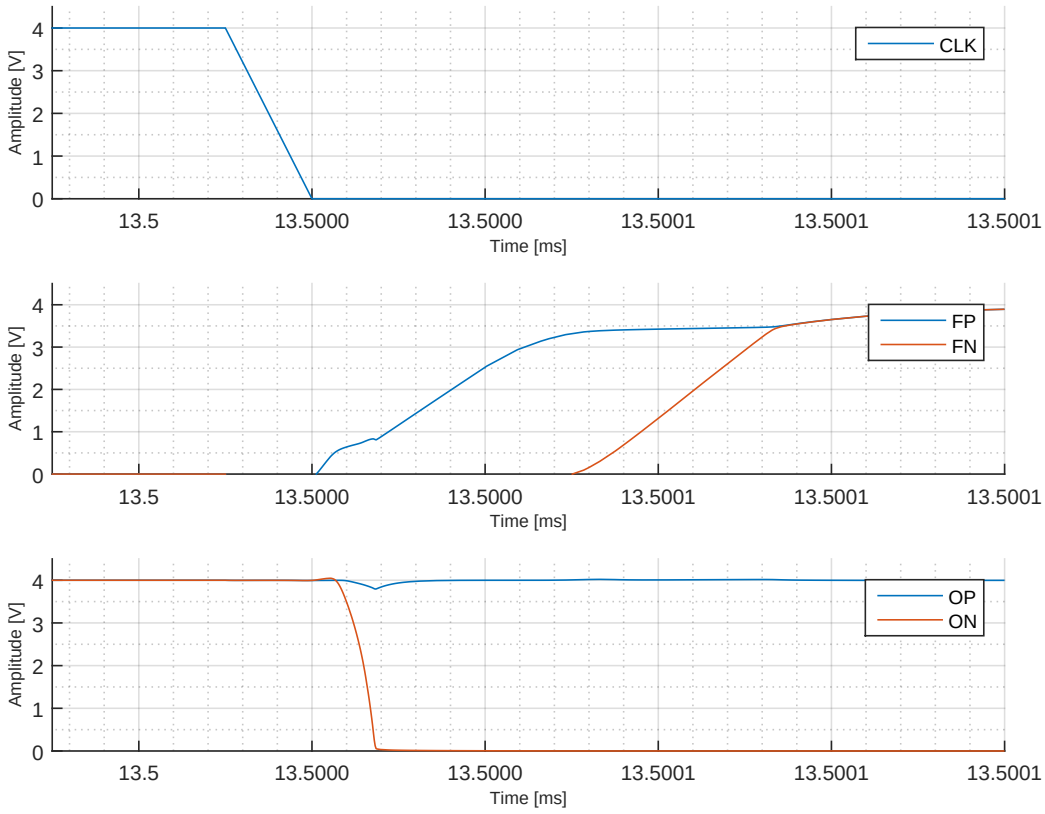


FIGURE 5.11: Internal comparator signals during one comparison phase at the falling clock edge. Internal nodes FN, FP at the output of the preamplifier as well as OP and ON at the output of the comparator are shown.

During the high state of the clock signal, the nodes FN and FP were connected via transistor M_4 and M_5 to ground. M_3 is switched off to avoid leakage currents inside the amplifier branch. Once the clock switches from high to low state, the transistors M_4 and M_5 will be switched off and transistor M_3 will be switched on, providing a bias current for the input pair. The nodes FN and FP will be pulled to the supply level, where their rise time is depending on the input voltage. In our example, FP will be pulled to the supply level first, due to the higher gate source voltage of M_1. Because of the faster ramp of FP, the node ON at the output of the latch will be pulled to ground first. The small logic block then converts these signals to the resulting output signal.

5.4.4 Control Logic

The basic block diagram of the control logic is shown in Figure 5.12. A four bit synchronous bidirectional counter generates the input signal for a combinational logic, which then converts the four-bits to a 12-bit thermometer code. To reduce the losses due to leakage, the circuit is connected to the digital supply. Additionally, standard cells were used with improved leakage characteristics. To be able to drive the stages of the sense transistor, the control signal needs to be shifted up to the higher voltage level. Therefore, each bit requires one additional level shifter.

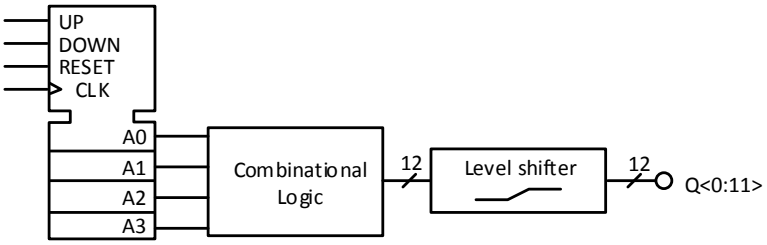


FIGURE 5.12: Block diagram for the control logic. Based on a four-bit counter, the required 12 control bits were generated by a combinational logic and then shifted to the higher supply domain.

The counter itself is based on JK flip-flops as shown in Figure 5.13 [35]. One single stage of the counter has been highlighted with a red dashed rectangle. The number of bits for the counter can be increased by adding the required number of stages. For clarity of the counter and combinational logic, the following circuits will be explained based on a three-bit counter and seven-bit thermometer code.

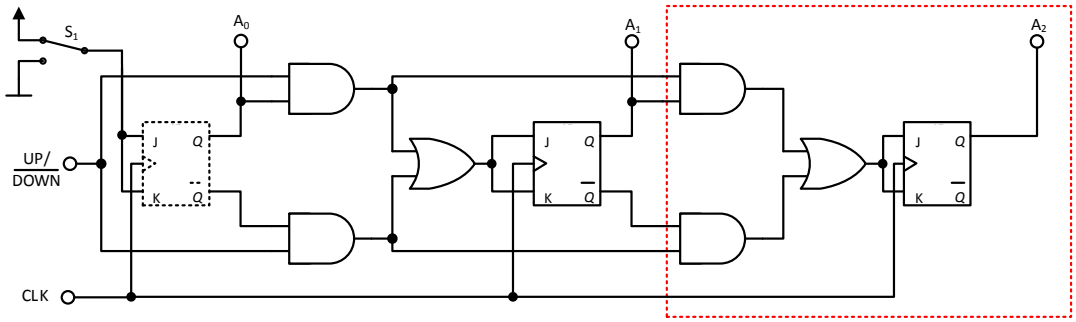


FIGURE 5.13: Block diagram for the bidirectional counter where only three bits are shown for simplicity. The required stage for one bit is marked red. This stage needs to be copied for each additional bit.

Except for the first stage, each stage consists of a JK-FF with three additional logic gates for the counting direction. Since two separate comparators are used for the control of the counting direction, no additional circuitry was implemented to protect the counter from the unwanted state that up and down are both at logic high. In case separate signals for up and down will be used and a scenario exists where both of them could be high, additional circuitry will be required.

Additionally the first FF is driven by a circuitry which connects either ground or the positive supply to the inputs of the FF. This is shown in Figure 5.13 using the switch S_1. If the FF is connected to the positive supply, the counter works in the normal operation mode. In case the FF is connected to ground, the counter can be stopped which is required in case of no valid up/down signal or if the counter reaches the minimum respectively maximum allowed value.

5.4.5 Combinational Logic

To be able to switch the sense transistors accordingly, the output signals from the counter have to be converted to a thermometer code. Table 5.2 shows the logic truth table for a three-bit counter.

A_1	A_1	A_0	S_0	S_1	S_2	S_3	S_4	S_5	S_6
0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0
0	1	0	1	1	0	0	0	0	0
0	1	1	1	1	1	0	0	0	0
1	0	0	1	1	1	1	0	0	0
1	0	1	1	1	1	1	1	0	0
1	1	0	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1

TABLE 5.2: Truth table for the thermometer code with the related control signal S_0 to S_6 for the sense transistor.

Figure 5.14 shows a section of the corresponding circuit for the combinational logic. One single stage, which can be copied and connected accordingly to the input signals for additional stages, was marked with a red dashed rectangle. The level shifters at the output of the circuit, which were required at each output of the combinational logic, are not mentioned.

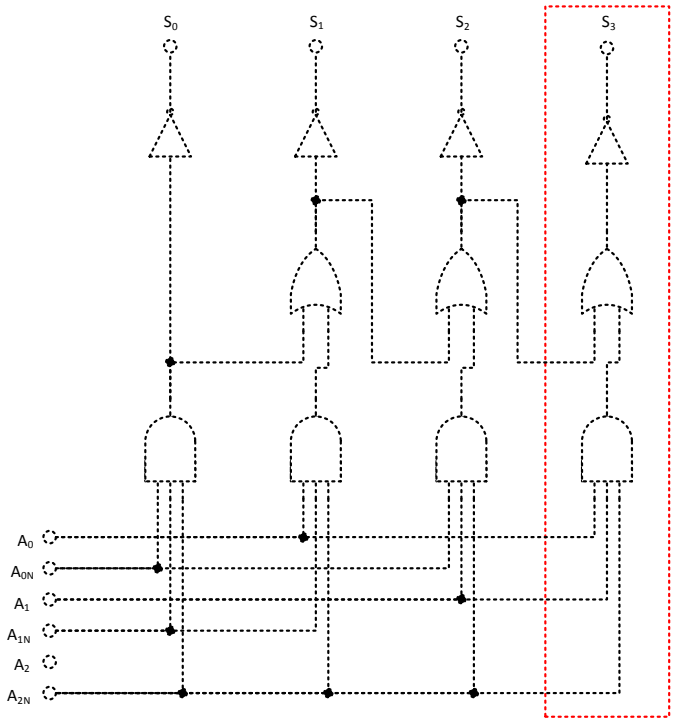


FIGURE 5.14: Section of the combinational logic for the first 4 bits of the thermometer code. The required cells for one additional bit are marked red.

Although the full combinational logic including counter consists of less than 40 logic gates, the leakage current of the logic block becomes important regarding the power consumption, especially for high temperatures. To reduce the leakage current, special logic cells with a very high threshold voltage were used. As explained in section 2.2, each 80 mV of gate source voltage reduction would result in a decreasing drain current by one decade. In case the gate source voltage cannot be changed, the same effect can be achieved by increasing the threshold voltage. In addition to the high threshold voltage, the length of the transistors inside the standard cells was optimized as well.

The supply currents (due to leakage) inside the digital cells are not only important regarding the overall losses of the circuit. Also, the digital CP is not able to drive very high currents. In case the leakage increases above a certain level, it could happen that the CP is not able to deliver this leakage current anymore and the voltage drops even below the specified 600 mV. This can happen due to a high static as well as dynamic supply current.

5.4.6 Level Shifter

The level shifter between the low and high supply is shown in Figure 5.15. Analog transistors for the high supply voltage are marked with a thicker gate inside the schematic. All remaining transistors are regular devices.

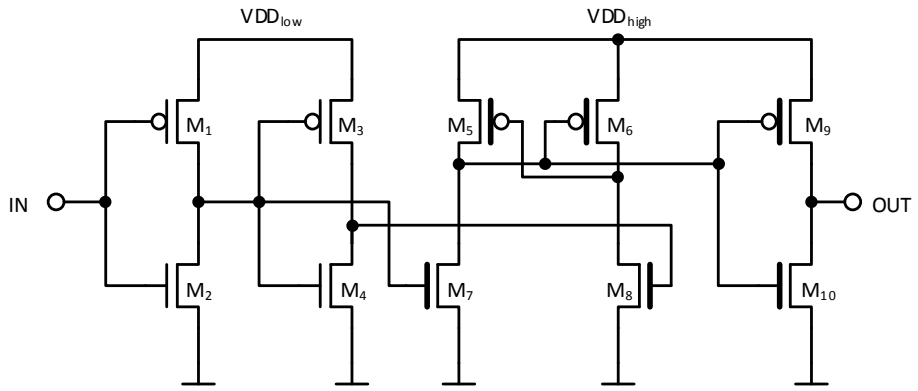


FIGURE 5.15: Level shifter for the interface between the low and the high supply voltage domain. Transistors marked with a thicker gate are analog devices for the high supply domain.

M_1 - M_4 are input inverters to buffer the input signal and generate the control signal for the level shifting core circuit M_5 - M_8. A third inverter at the output buffers the signal again. Assuming a logic high at the input would result in a logic high at the gate of M_8 and a logic low at the gate of M_7, which were driving the half latch M_5 and M_6. M_8 turns on pulling the gate of M_5 to ground and the drain to the high supply rail, which results in a logic low at the output of the level shifter.

5.5 Track and Hold

Figure 5.16 shows the basic circuit for the track and hold stage. It consists of two separate track and hold blocks for each half of the clock cycle. C_1 with S_1 is the first stage and C_2 with S_2 the second one. Additional OP_1 is used as input, and OP_2 as output buffer.

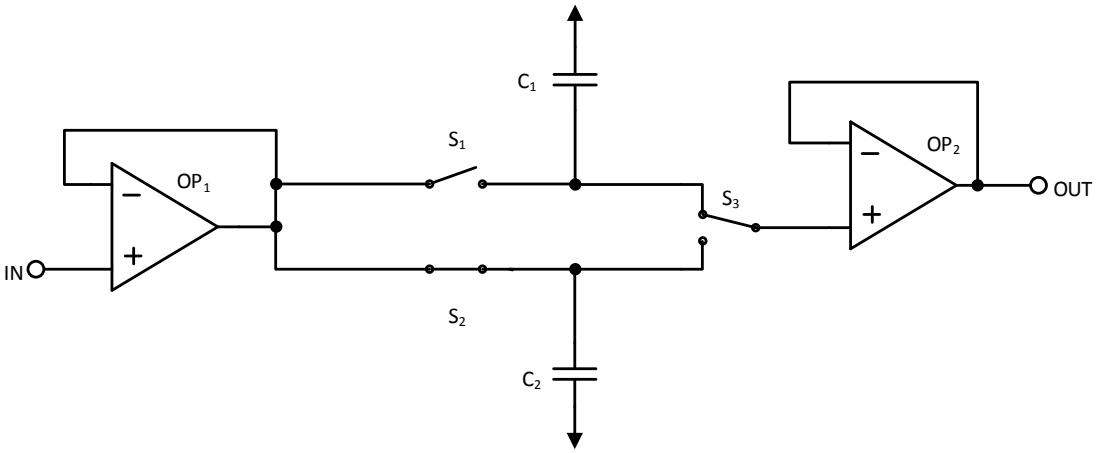


FIGURE 5.16: Track and hold circuit including input and output buffers. The capacitors C_1 and C_2 are each for one half of the system clock period. S_3 switches between the currently held signal.

During the first half clock cycle, S_1 will be closed and S_2 opened. S_3 connects C_2 to the input of the amplifier. During this phase, the value at C_2 will be used on the output, whereas C_1 will be used to store the current input voltage level. During the second clock phase (switch positions which are shown in Figure 5.16), all switches change their positions. The value of C_1 will then be used at the output and C_2 used to store the current input value.

Considering the size of the capacitors, the leakage current is one of the most important parameters due to the small frequency and therefore high period time. The charge on a capacitor can be calculated using

$$Q = C\,V \tag{5.25}$$

where Q is the charge on the capacitor, C the value of the capacitance and V the voltage at the capacitor. Looking at the change of the charge assuming a constant current, this would lead to

$$I\,\Delta T = C\,\Delta V \tag{5.26}$$

As an example, using a frequency of 1 kHz, a leakage current of 40 pA and a maximum allowed voltage drift of 2 mV, would lead to

$$C = \frac{I\,\Delta T}{\Delta V} = \frac{40\,\mathrm{pA}\,500\,\mu\mathrm{s}}{2\,\mathrm{mV}} = 10\,\mathrm{pF} \tag{5.27}$$

The root cause of the high leakage current are the transmission gates in the track and hold circuit. This unwanted leakage current results from the high junction voltages between the substrate/n-well and the source/drain of the switching transistors.

5.6 Control Signal Generation

Based on the gate voltage of the sense transistor and the track and hold circuit, the output signal of the sensor needs to be generated. Figure 5.17 shows the basic architecture of the circuit.

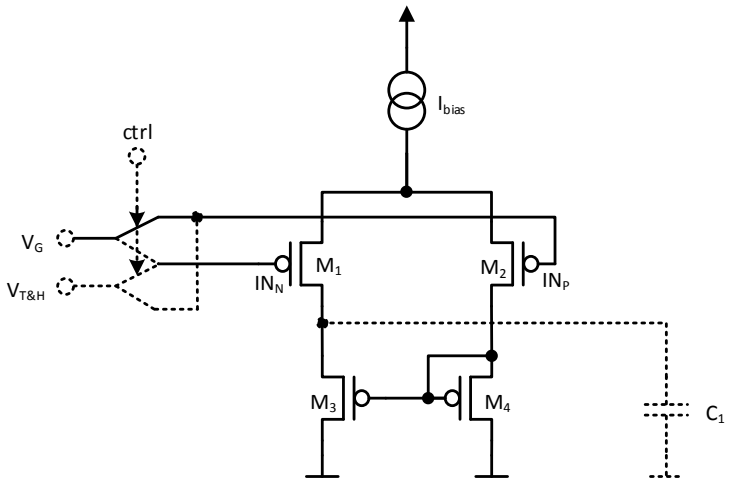


FIGURE 5.17: Output amplifier with load capacitor for integration. The input switches are changing the input signal after each half period of the system clock period.

During the logic high phase of the ctrl signal, the gate voltage will be connected to the positive input of the amplifier and the track and hold signal to the negative input. During the low phase of the ctrl signal, the inputs of the amplifier will be swapped.

Looking at the clock phase where the gate voltage will be connected to the positive input of the amplifier and considering a higher gate voltage compared to the track and hold signal, M_1 will drive a higher current than M_2 and charges the output capacitor C_1. Looking at a lower gate voltage, M_2 will drive a bigger current, which will be mirrored using M_3 and M_4 and discharging the capacitor. In an ideal case, the charging and discharging current would be equal. Nevertheless, due to mismatch of the input pairs and current mirror, this is not actually the case inside the real circuit.

6 Simulation Results

The following chapter contains the simulation results of all important circuit blocks as well as top level simulations. Due to the different supply domains and variations, the wide current range as well as their different combinations, the simulations within the following chapter are going to show only a part of the required simulations that would be needed to fully characterize the circuit. Nevertheless, for important circuit blocks or key parameters, corner or Monte Carlo simulations were performed.

All simulations, unless otherwise noted, are performed at room temperature (27 °C), nominal corner, 600 mV digital supply and 2 V analog supply.

6.1 Bias Circuit

The bias circuit was designed for a typical bias current of 1 nA. Figure 6.1 shows the distribution of the bias current at 4 V power supply and 27 °C. The mean value is close to the

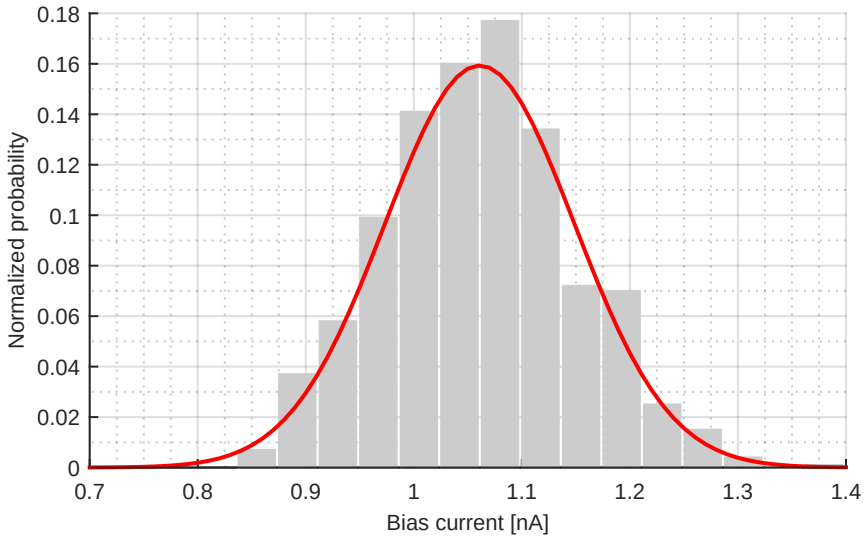


FIGURE 6.1: Distribution of the bias current at 4 V supply voltage, σ =87.945 pA, μ= 1.052 nA and N = 1000.

Additionally to the process parameters, the supply voltage and the temperature may vary as well. A sweep at the worst process corners (slow and fast) and the temperature values of 27 °C, −40 °C and 100 °C is shown in Figure 6.2.

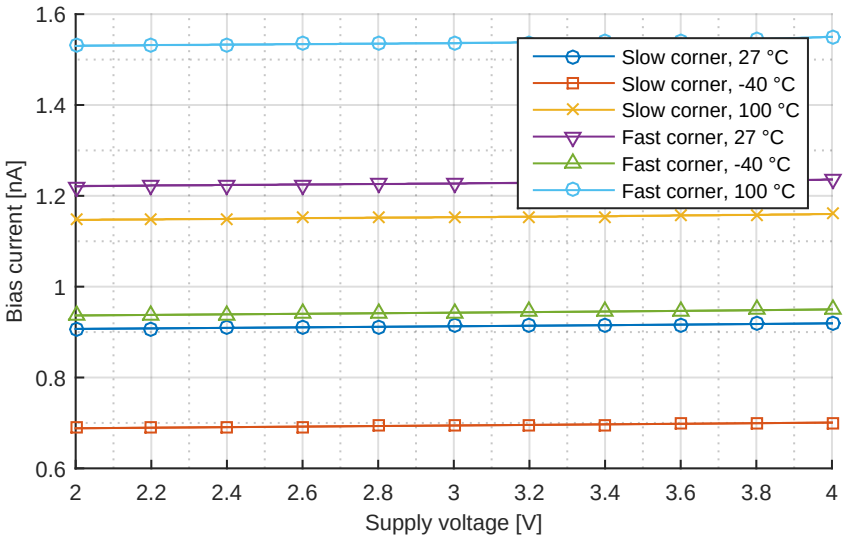


FIGURE 6.2: Temperature and supply voltage dependency of the bias current over process corners. It can be seen that the supply voltage variation can be neglected compared to the process corner and temperature variations.

There are two main effects which cause the shown behavior. The differences between the corners are mainly due to the process variations of the used resistor. On the other hand, the temperature variations were caused by the general behavior of the constant-gm bias circuit which was shown under section 5.1, also called PTAT (Proportional To Absolute Temperature) bias current. In 5.4 it can be observed that the temperature variations are caused by the thermal voltage V_T and the temperature dependency of the resistor. Since the dependency of the resistor is much smaller than the variation of V_T, the resulting dependency is primarily related to the thermal voltage. For a rough estimation, the effect of the resistor can be neglected, which would result in temperature dependency for the bias current of $3.98\,\mathrm{pA\,K^{-1}}$.

To make sure that the start-up of the circuit will work under all conditions, the worst-case scenario for start-up needs to be found and simulated during a transient simulation. Looking at the circuit shown in Figure 5.1, the worst case can be found by forcing V_{N1} to ground and V_{P1} and V_S to the supply. This scenario ensures that no current will flow inside the bias circuit and that M_6 will be switched off. Figure 6.3 shows the start-up scenario inside the process, temperature and supply voltage corners.

It can be seen that the circuit is going to start under all conditions in approximately 20 ms.

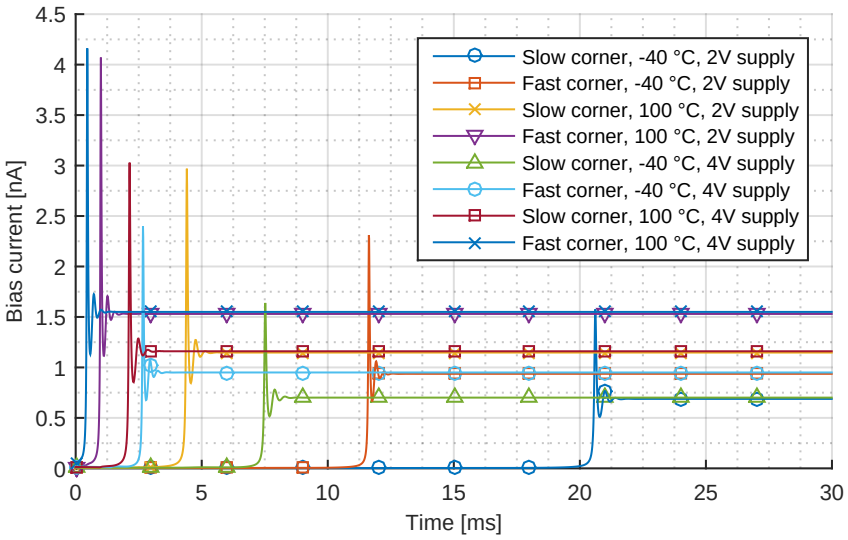


FIGURE 6.3: Start-up behavior of the bias circuit depending on the process corner, supply voltage and temperature. The system start-up time is, under worst condition (slow corner and lowest temperature which results in the smallest leakage current), approximately below 20 ms.

As explained in section 5.1, the leakage current of the start-up transistor has a high temperature dependency. Figure 6.4 shows the basic dependency of an NMOS transistor with L=2 µm and W=600 nm. It can be seen that the leakage current decreases at low temperatures which slows down the start-up. Also, it raises exponentially for high temperatures. Keeping in mind that this current always has to be lower than the bias current, this results in a very small leakage current during start-up. Thus, the start-up of the circuit is slowed down, but it is ensured that the additional devices will have no influe

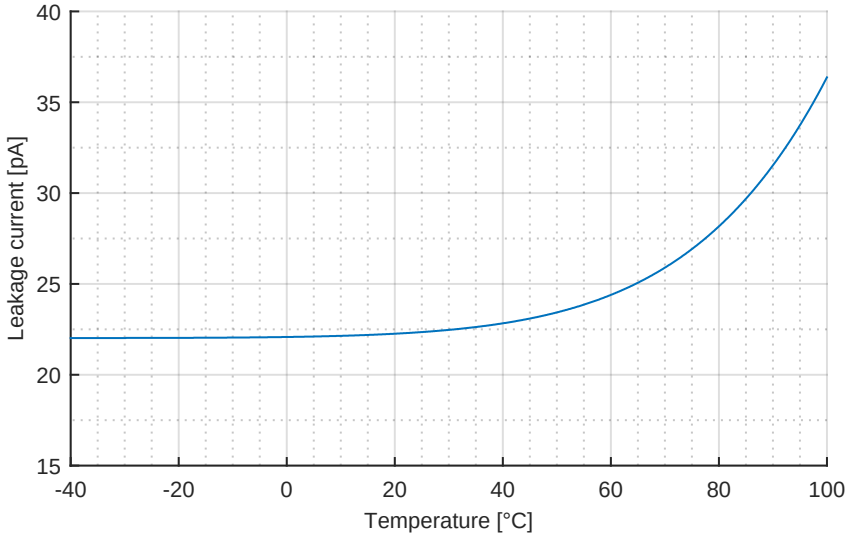


FIGURE 6.4: Leakage current of an NMOS transistor with L=2 µm and W=600 nm depending on the temperature.

6.2 Sense Element and Input Amplifier

Due to the fact that the input amplifier's supply voltage is connected to the battery, which is also the positive input of the amplifier, a view modifications on the simulation circuit are required.

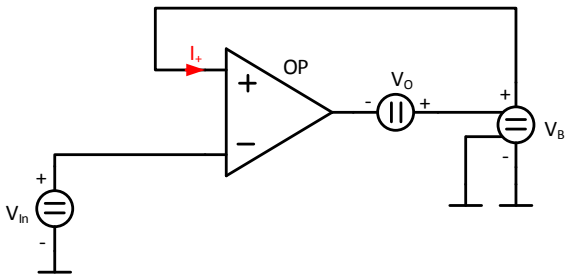


FIGURE 6.5: Basic simulation circuit for the input amplifier without sense element. Additional voltage source V_O and voltage-controlled voltage source V_B required for operation.

Figure 6.5 shows the basic DC simulation circuit for the offset simulation. Due to the architecture of the operational amplifier, the output is not able to drive the input directly, which requires a bias current that is higher than the bias current of the output stage. To overcome this issue, a Voltage Controlled Voltage Source (VCVS) V_B with a voltage magnification of one, was added. This VCVS provides the input current of the amplifier without any influence on the DC node voltages.

Additionally, the voltage source V_O is required. The input of the amplifier will be connected to the positive supply voltage inside the application. In a buffer configuration, this also requires the output of the amplifier to be able to work up to the supply voltage level. Due to the fact that the architecture cannot drive the output up to the positive supply rail, an additional offset was added using the voltage source V_O. Nevertheless, this situation is no real operation scenario and will be used only for offset simulations of the amplifier.

Figure 6.6 shows the spread of the offset voltage at 2 V supply. It is important to keep the desired additional offset voltage above the amount due to mismatch of the amplifier. Because of to the fact that no additional actions were taken to improve the amplifiers mismatch, the built-in offset was designed to be in the range of 15 mV to 20 mV. Additional reduction of the offset generated by mismatch would result in a smaller loss on the sense transistor, but might require additional circuitry for the amplifier.

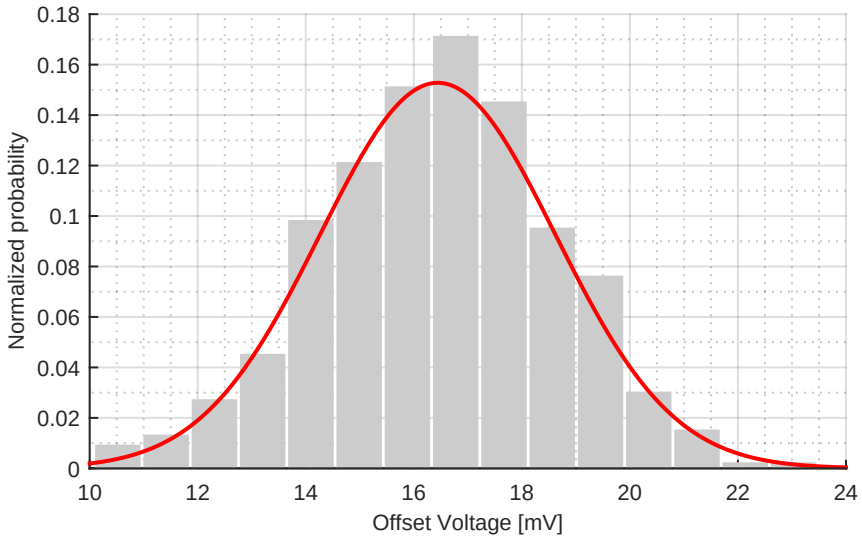


FIGURE 6.6: Distribution of the offset voltage at 2 V supply voltage, $\sigma = 2.177\,\text{mV}$, $\mu = 16.4433\,\text{mV}$ and $N = 1000$.

All remaining simulations were done using the loop including amplifier and sense transistor. Figure 6.7 shows the Bode diagram for the single stages of the amplifier including the sense transistor as well as the total open loop gain and phase. It can be seen that the dominant pole is at approximately 2 Hz coming from the common source stage and the non-dominant pole, at approximately 8 kHz, is coming from the common gate stage. This corresponds to the calculations done within section 5.3.2. Additionally it can be seen that the sense transistor causes an attenuation of approximately −29 dB, which improves the stability of the circuit and helps to avoid a typical Miller capacitor for compensation. The phase margin of the circuit is typically in the range of 30 degrees.

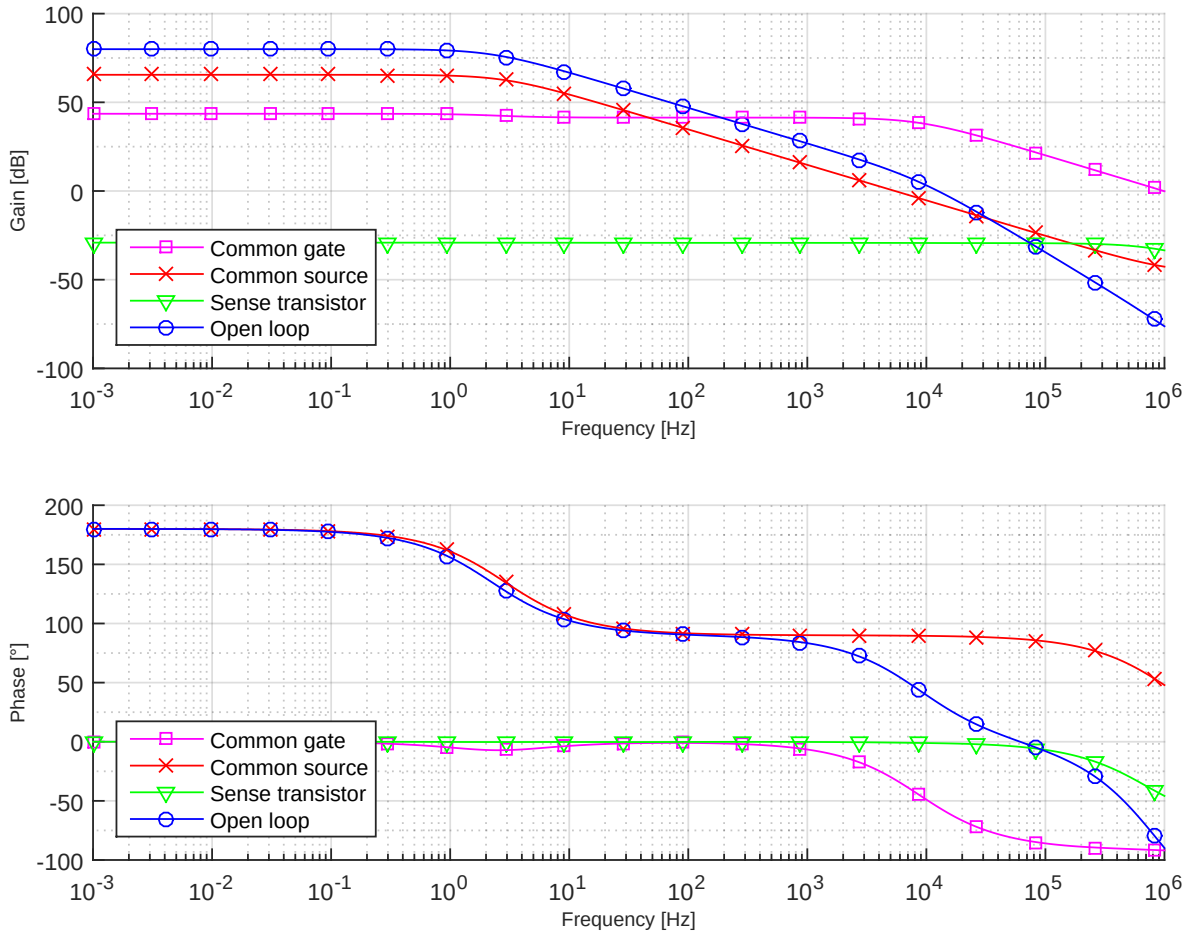


FIGURE 6.7: Bode diagram of the separate amplifier stages. Common gate, common source, sense transistor as well as open loop are shown separately.

One major parameter is the impact of the bias current on the circuit. Therefore, three separate simulations were conducted and compared with a simulation for 1 nA bias current. The first simulation was done using a bias current of 1 nA which was then mirrored into the CG and CS amplifier (with the corresponding mirror ratio). This simulation was used as reference for comparison with the remaining three results. After this, the bias current was doubled which results in a 2 nA bias for both amplifier stages. For the last two simulations, the bias currents of the single stages were doubled separately. This was done using ideal current sources to keep the mirror transistors at the same dimensions. Figure 6.8 shows the simulation results. For reasons of clarity, the starting point of the frequency axis was moved compared to Figure 6.7.

The bias current mentioned above was mirrored with a factor greater than one into the CG or CS stage. Therefore, the current inside the stage itself will be bigger depending on the chosen mirror ratio.

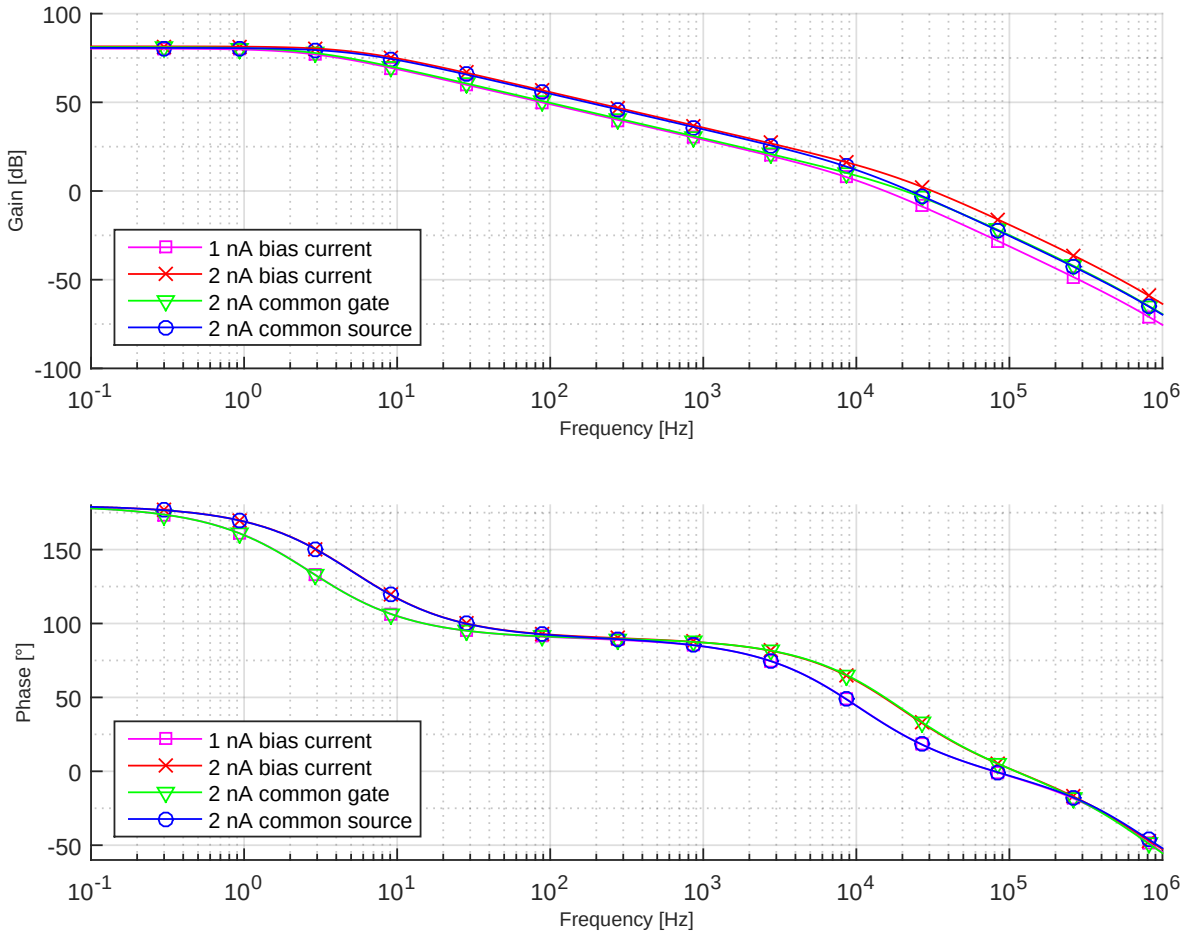


FIGURE 6.8: Bode diagram for the open loop circuit under different bias current scenarios. In case it is not explicitly mentioned, all stages are bias with 1 nA. The effect of the different bias currents can be mainly seen in a shift of the pole, whereas the open loop gain is in a first order independent from the bias current.

Figure 6.8 shows that the bias current only has an impact on the position of the poles, not on the DC gain. A higher current inside the related gain stage will move the pole to higher frequencies due to the reduction of the output resistance. Unfortunately, this behavior makes it difficult to increase the gain (not the transconductance g_m) of the CG or CS stage.

6.3 Reference Voltage

The reference voltages for the comparators can be seen in Figure 6.9 for the lower, and 6.10 for the higher reference voltage.

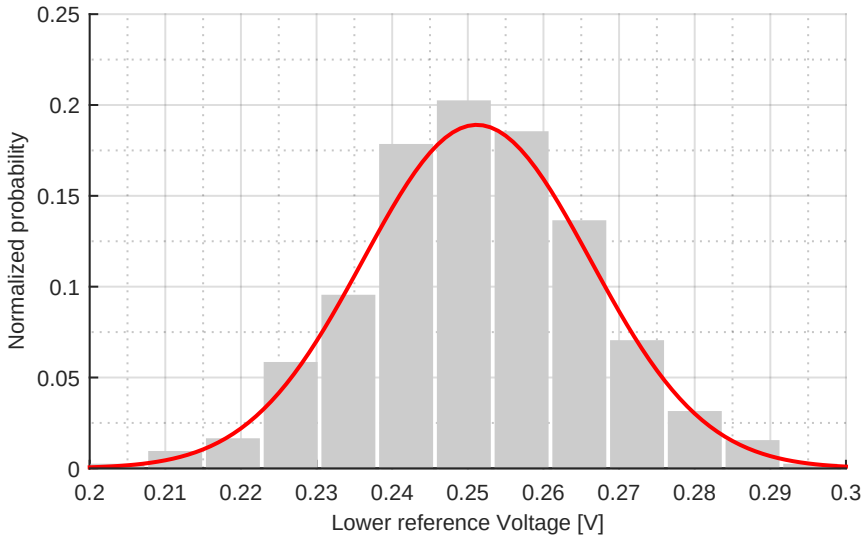


FIGURE 6.9: Distribution of the low reference voltage at 2 V supply, $\sigma = 15.03\,\text{mV}$, $\mu = 251.2\,\text{mV}$ and $N = 1000$.

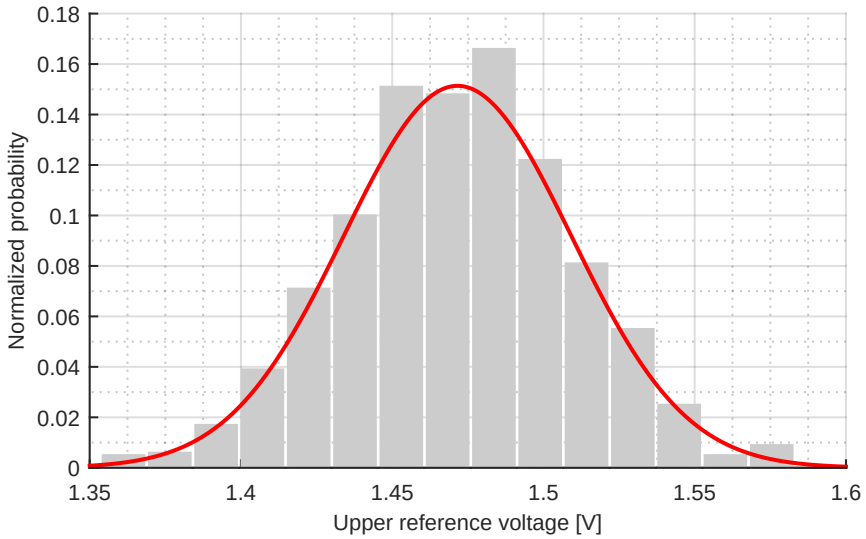


FIGURE 6.10: Distribution of high reference voltage at 2 V supply, $\sigma = 37.65\,\text{mV}$, $\mu = 1.4716\,\text{V}$ and $N = 1000$.

Additional to the process, the temperature variations of the reference voltage need to be considered as well. Figure 6.11 shows these dependencies for the high and low comparator reference voltage. It can be seen that the limiting region for the sense transistors aspect ratio factor will be at the lower possible temperature. Therefore, the current sense element was designed with a ΔV_{GS} in the range of only 800 mV. The availability of a more accurate reference voltage for the comparators would make it possible to increase the aspect ratio factor of the sense transistors to three (compared to two inside the current version) or reducing the minimum supply voltage.

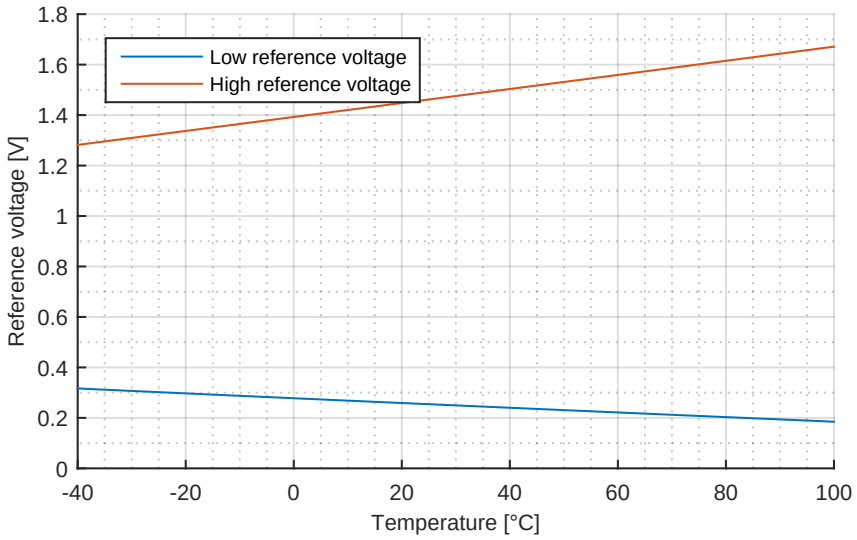


FIGURE 6.11: Temperature dependency of the high and low reference voltages.

6.4 Comparator

The comparator was simulated using two ideal reference voltages: V_{ref} of 1.4 V for the comparator with the NMOS input pair and 400 mV for the PMOS type. For the gate voltage, a ramp was used starting at $V_{ref} - 50\,mV$ and ending at $V_{ref} + 50\,mV$ within 100 ms. Figure 6.12 shows the histogram for the NMOS comparator and Figure 6.13 for the PMOS comparator.

Especially in Figure 6.13 it can be seen that certain bins have a very small probability. This is not caused by the circuit itself, but it rather results from the simulation setup and the fact that the comparators are using a clocked architecture. During the 100 ms ramp, the comparator can make 100 decisions assuming a system clock of 1 kHz. For this reason not all possible input voltage can be covered, which can lead to bins with a very small probability. This effect can be seen even better, if the number of Monte Carlo runs and bins is increased.

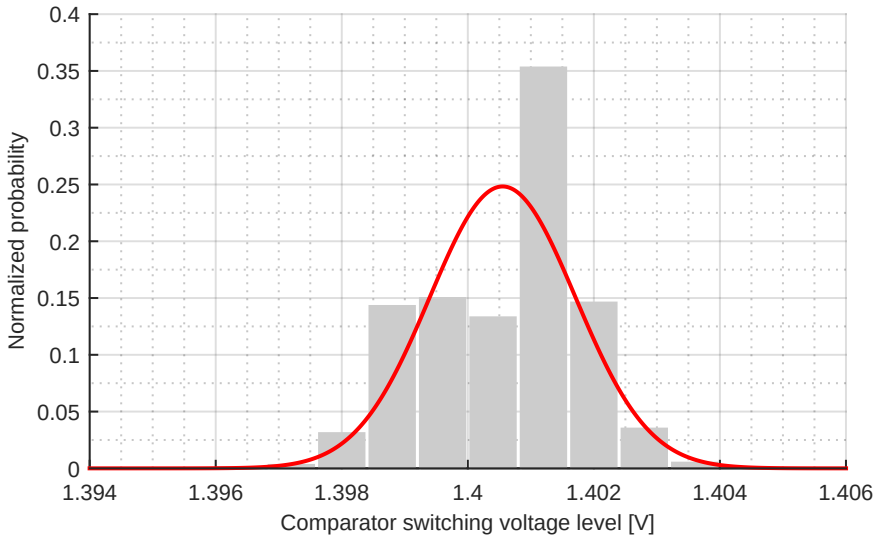


FIGURE 6.12: Distribution of the comparator switching level for the high reference voltage defined at 1.4 V, $\sigma = 1.2\,\text{mV}$, $\mu = 1.4006\,\text{V}$ and $N = 1000$.

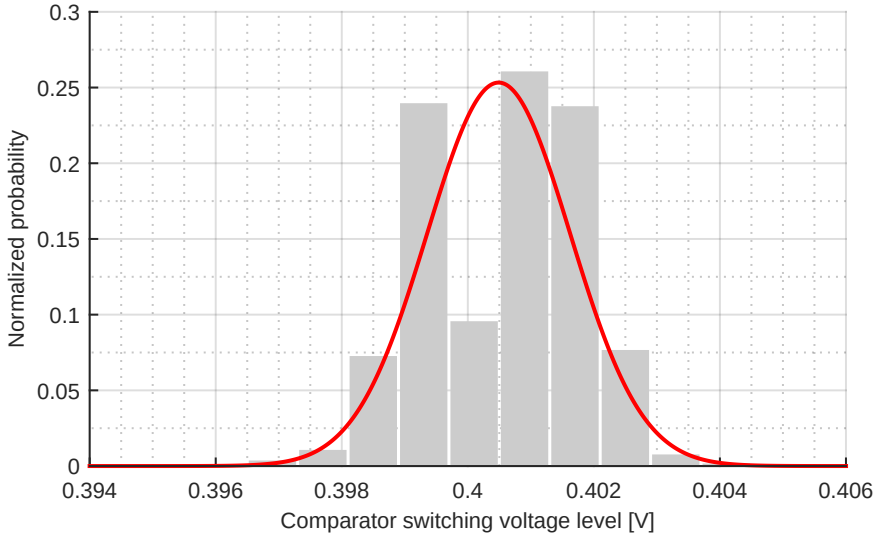


FIGURE 6.13: Distribution of the comparator switching level for the low reference Voltage defined at 400 mV, $\sigma = 1.1\,\text{mV}$, $\mu = 400.5\,\text{mV}$ and $N = 1000$.

6.5 Counter

Figure 6.14 shows the basic timing diagram for the counter. The related voltage levels are normalized to logic true (1) or false (0). This is why information about the voltage domain of the signal cannot be seen in Figure 6.14.

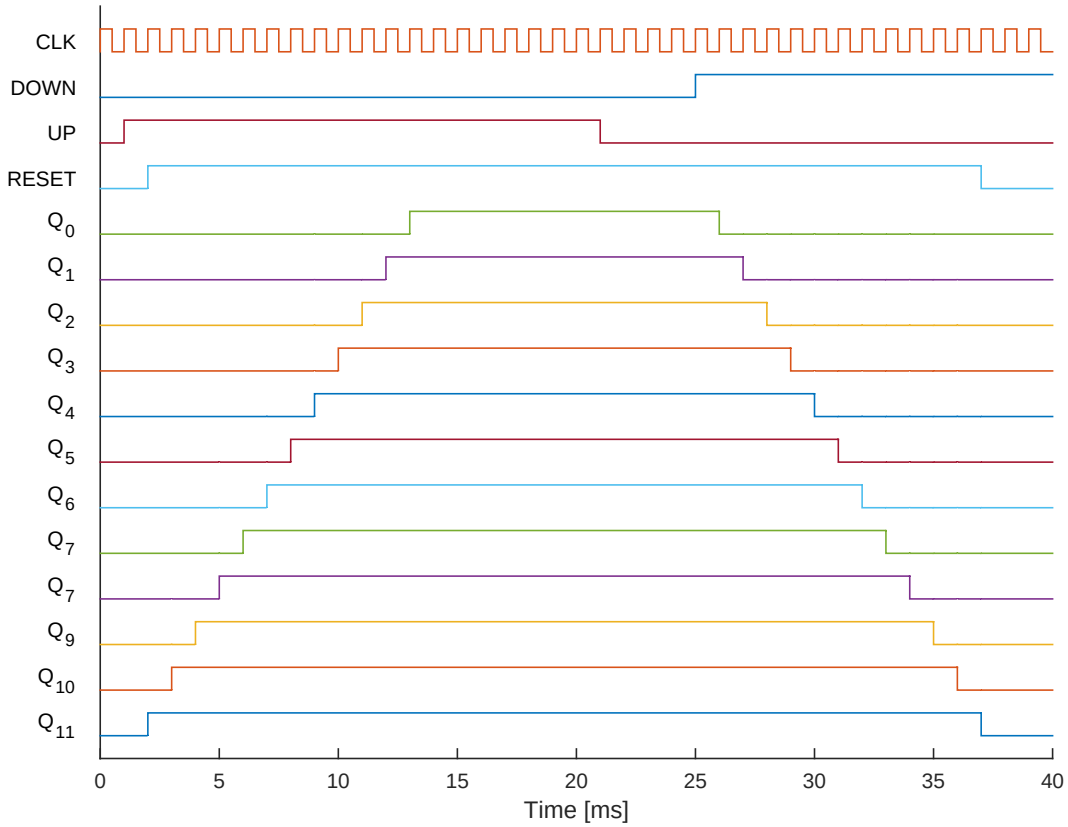


FIGURE 6.14: Timing diagram for the bidirectional counter during the up and down phase. Signals are normalized to logic true and false values.

Additional simulations like reset during the counting were performed but not mentioned explicitly within this thesis. Nevertheless, for a full qualification of the counter, these simulations were required as well.

6.6 Stage Selection

Figure 6.15 shows the gate voltage dependent from an input current ramp over the full range from 100 nA to 1 mA. The margin between the maximum gate voltage (approximately 1 V) to the upper comparator level might be very large which has two reasons. As it can be seen in Figure 6.11, the two comparator levels will come closer with decreasing temperatures. The second important fact is that the gate voltage has a limited slew rate. After each stage change, the gate voltage needs to rise to its higher level. This rise of the gate voltage would result in a decrease of the sense voltage due to the track and hold circuit. Depending on the top level integration of the current sensor, this decrease of sense voltage could lead to an additional increase of the gate voltage directly after the change of the stage. This might again lead to the situation where the gate voltage reaches the higher reference level and changes back to the previous stage, which would result in an unstable behavior. To overcome this issue, the margin from the gate voltage to the high comparator level as well as the capacitor for the integrator at the output were increased.

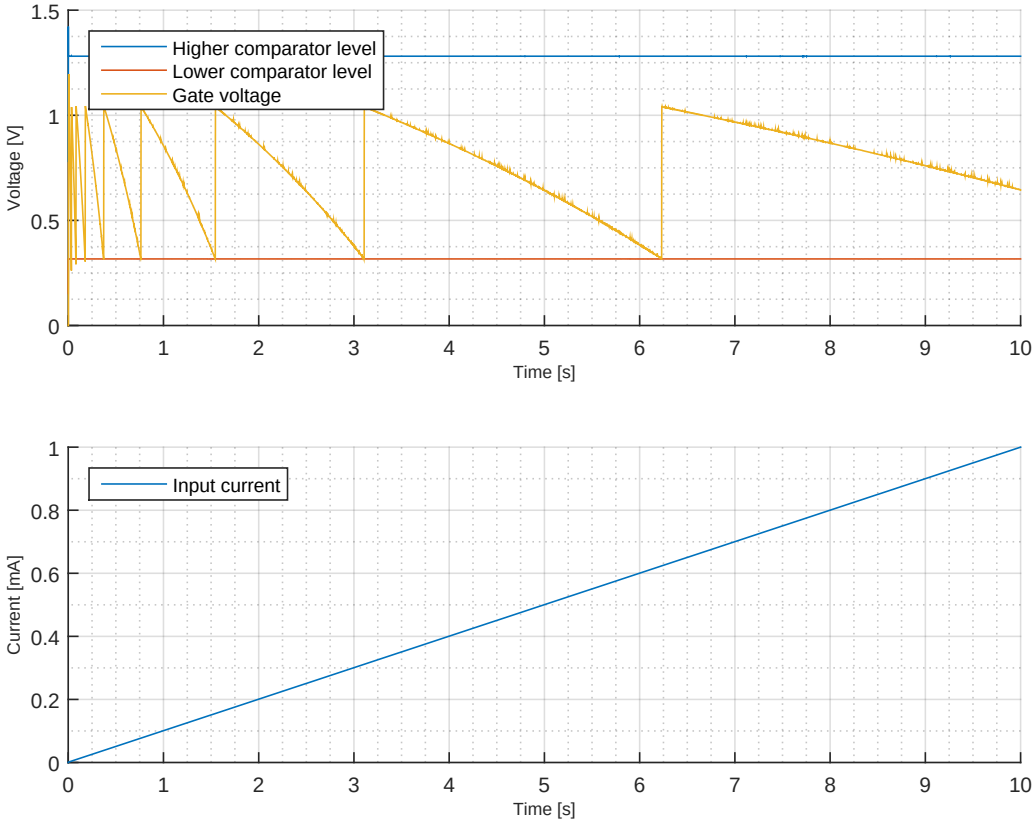


FIGURE 6.15: Gate and comparator reference voltages for an input current range from 100 nA to 1 mA.

Figure 6.16 shows the same simulation as in Figure 6.15 with the only difference of the input source being a logarithmic current source. The characteristic of the source can be written as:

$$I_{\text{Source}} = 100\,\text{nA}\,10^{0.4\,\text{s}^{-1}\,\text{time}} \tag{6.1}$$

where I_{Source} is the output current of the source and "time" the corresponding time.

The maximum gate voltage, which appears after a change of the stage, seems to be slightly higher, especially for a small input current. This can be observed at the gate voltage in Figure 6.16. This is due to the fact that the current changes also while the gate voltage rises from the lower comparator level to the high level after the stage switching.

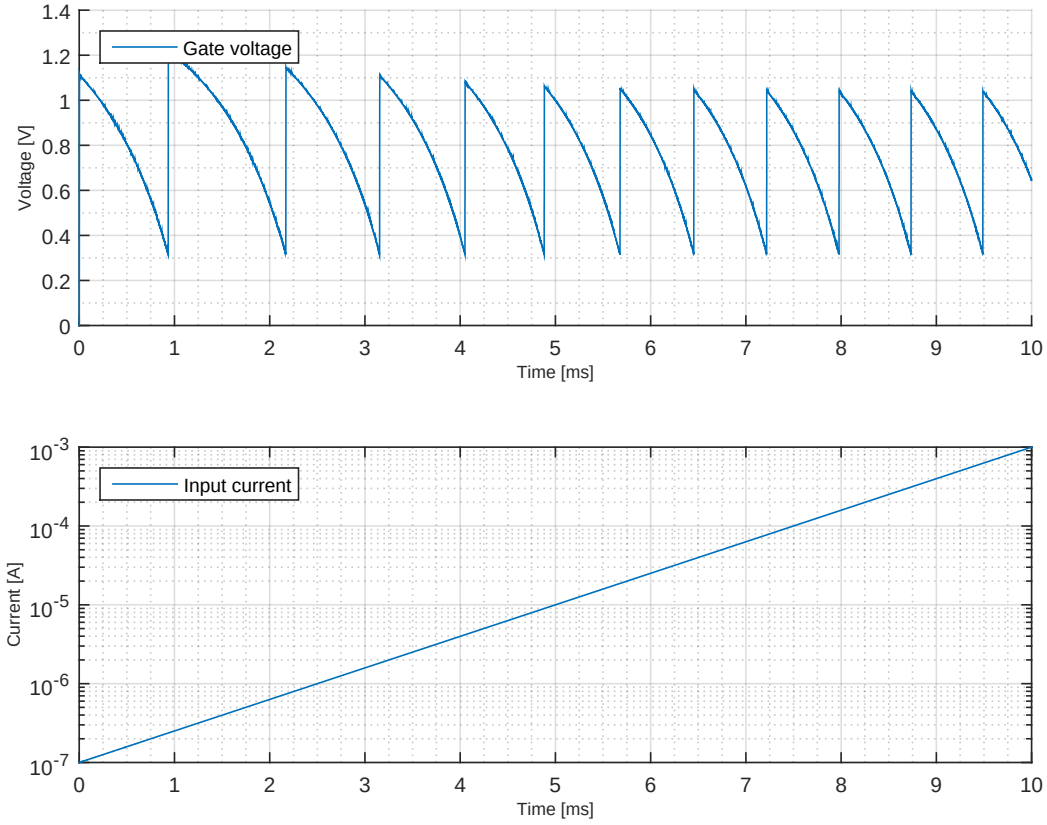


FIGURE 6.16: Gate and comparator reference voltages for an input current range from 100 nA to 1 mA with a logarithmic source.

6.7 Track and Hold

Figure 6.17 shows the basic function of the track and hold circuit with special attention towards the start-up and the possible occurring input voltage range (using a 2 V supply). It can be seen that the track and hold circuit requires a certain start-up time until the capacitors are fully loaded. This time depends on the initial voltage inside the capacitors as well as the current gate voltage level. The output signal might vary during this start-up phase, which, however, has no effect on later measurements.

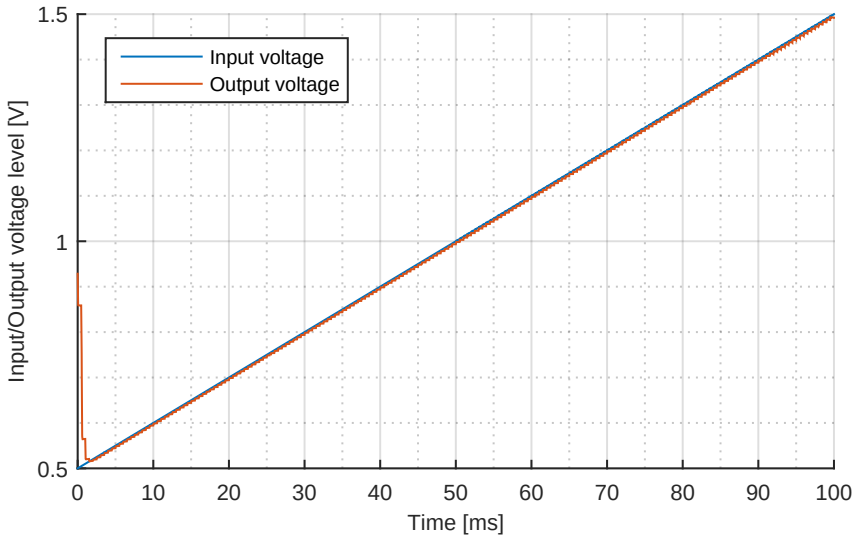


FIGURE 6.17: Input and output voltage of the track and hold stage including start-up behavior as well as the possibly occurring input voltage range.

Figure 6.18 shows a detailed view of the input and output signal, where the proper function of the track and hold circuit can be seen. Also the offset between the input and the output value can be observed which is caused by amplifier mismatches and charge injection of the sample and hold circuit. Due to the architecture of the system, this leads to no additional error and can therefore be accepted. Adding circuitry to reduce, for example, the charge injection, would also increase the leakage current inside the switches, which is unintended as we

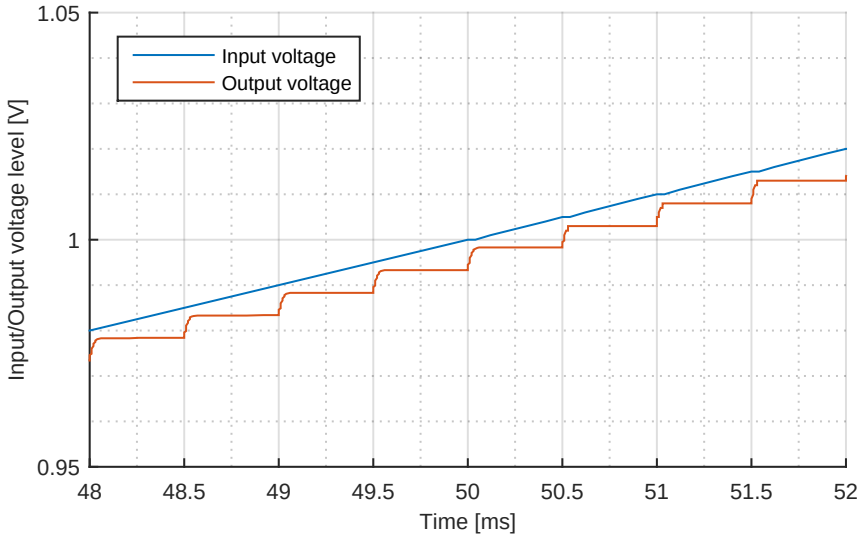


FIGURE 6.18: Detailed view on the input and output signal of the track and hold stage.

6.8 Control Signal

Figure 6.19 shows the basic function of the output stage for an input voltage ramp. Although this is no typical case of operation, it shows one characteristic of the output circuit that needs to be considered. The gate voltage was reduced from 1.5 V to 0.5 V within 100 ms. Additionally, the sense voltage was defined to be at 0.5 V as initial condition.

It can be seen that the output voltage may drift in a random direction (depending on the mismatch inside the output operational amplifier). This effect must be considered either inside the sensor itself or on the next level where the current sensor will be integrated. Within the application where the circuit from this thesis will be implemented, this effect will be considered on top level.

Also, the impact of the start-up behavior from the track and hold circuit can be seen in Figure 6.19. The sense voltage might vary during start-up which changes the absolute value of the voltage, but the circuit should still evaluate only relative changes. Therefore, the absolute value of the output voltage is not important for the measurement itself.

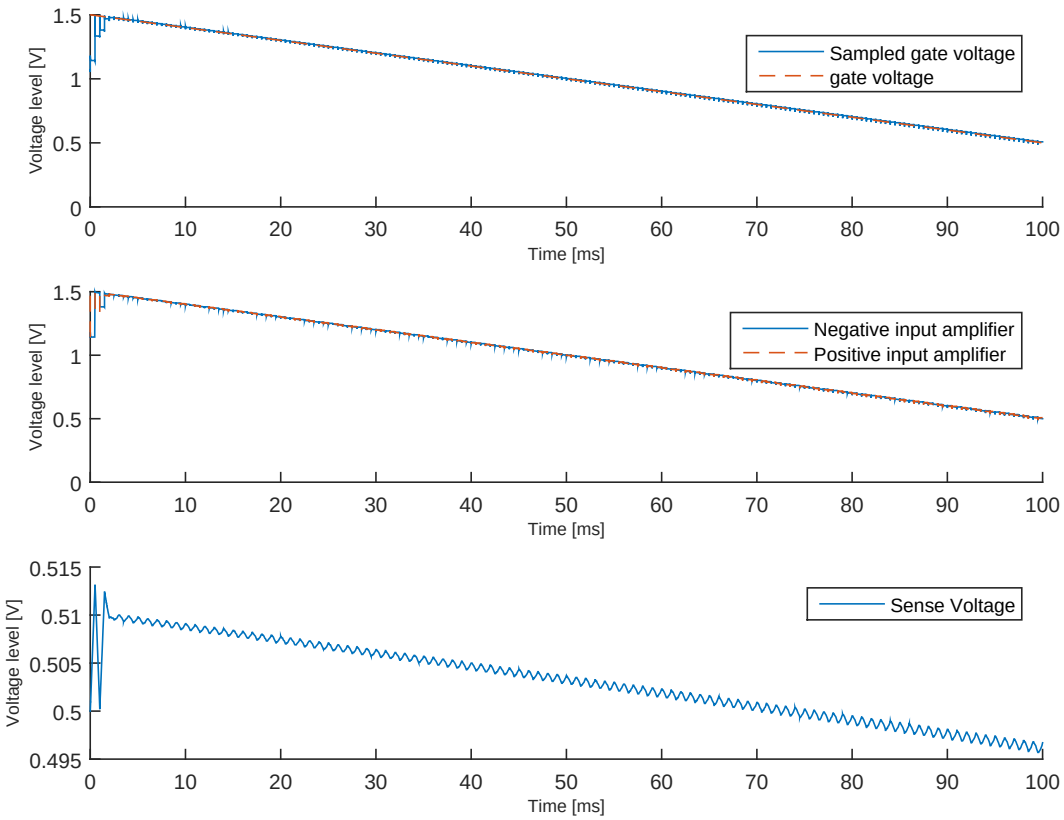


FIGURE 6.19: Output voltage of the control signal generation including the gate and sampled voltage, negative and positive amplifier input as well as output signal. The drift of the sense voltage due to mismatches inside the integrator can be seen.

6.20 shows a detailed view of the charging phases. The available gate and sampled voltage will always be changed after a half clock period. Inside the first half clock phase (starting at 48 ms), the gate voltage will be connected to the positive input of the amplifier and the sampled value at the negative input. This causes a current at the output of the amplifier, which discharges the load capacitance. During the next half clock phase, the input signals are swapped, causing the load capacitor to be charged. Ideally, the sense voltage should be at the same level after the two phases. Due to a difference inside the charging and discharging current, caused by the current mirror, this is not valid inside the real circuit, which leads to the previously mentioned drift. As long as the drift is in the range of less than 1 mV during one measurement cycle (1 ms), this effect can be neglected.

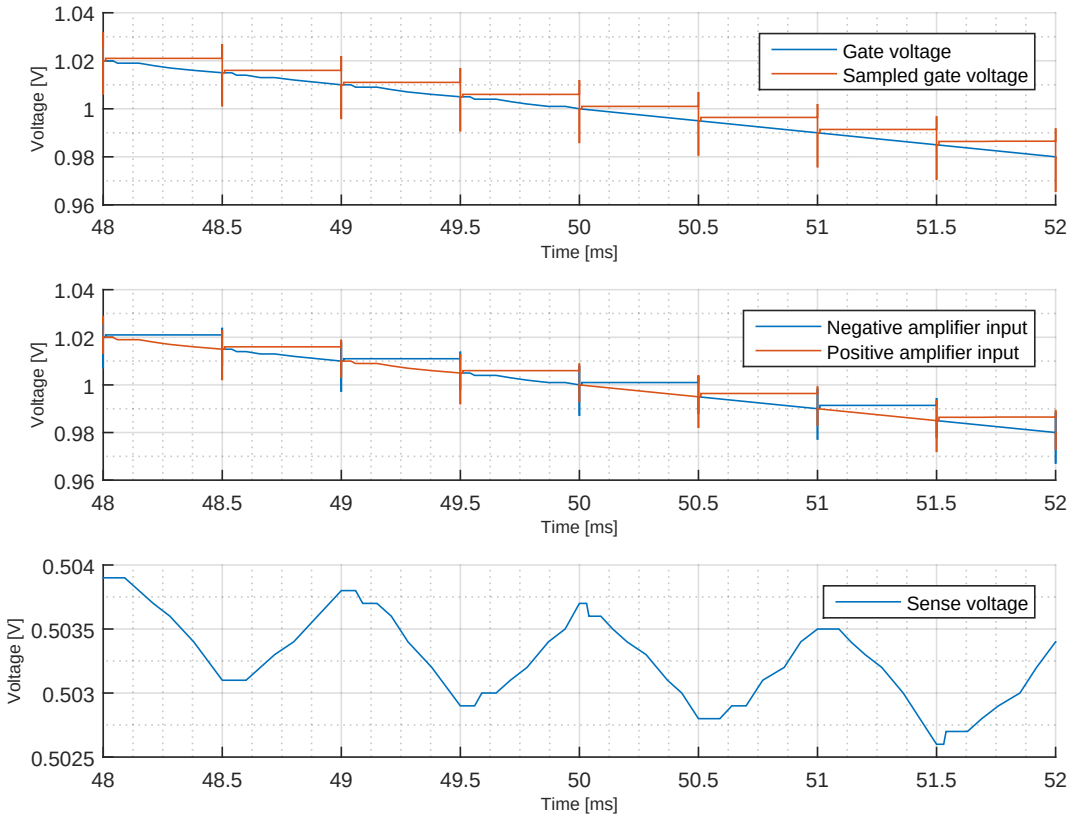


FIGURE 6.20: Output voltage of the control signal generation.

6.9 Top Level

The main measurement signal based on the input current is the gate voltage of the sense element. Figure 6.21 shows the voltage for a 4 V supply and Figure 6.22 for a 2 V supply. It can be seen that the gate voltage is subjected to a wide variation, which would result in a poor absolute accuracy. Nevertheless, the concept of the circuit for the detection of the current peaks does not require high absolute accuracy. Therefore, the variations of the gate voltage can be accepted as well.

Furthermore, an approximation for the input current can be given in any case, which might be enough for certain applications like quiescent current measurement or short circui

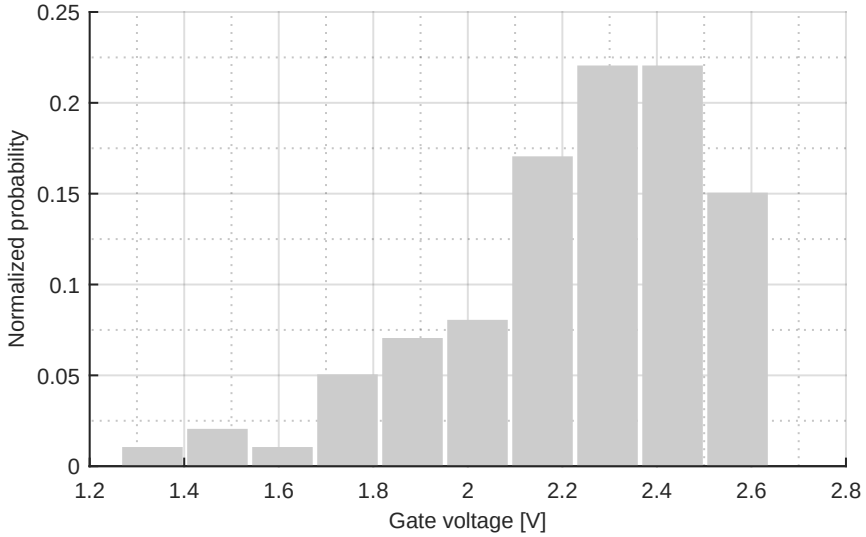


FIGURE 6.21: Gate voltage distribution for a supply level of 4 V with $\sigma = 0.2738\,\mathrm{V}$, $\mu = 2.2392\,\mathrm{V}$ and $N = 100$.

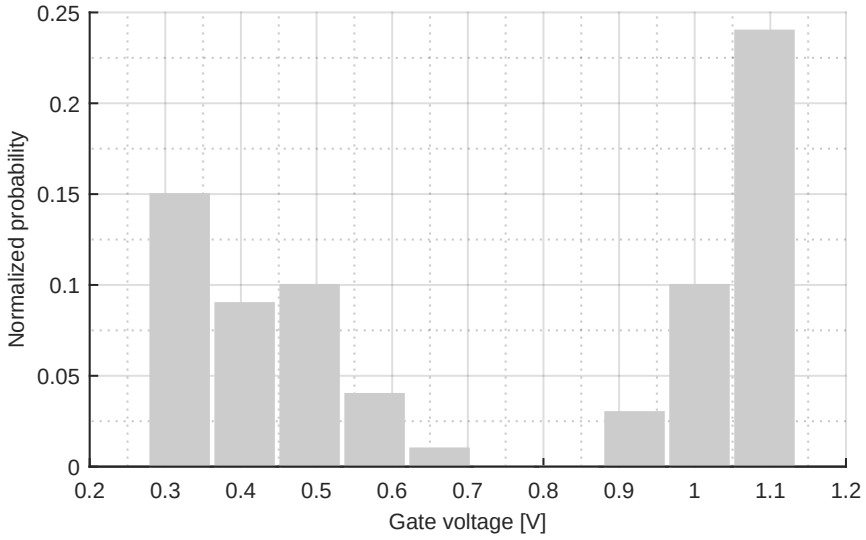


FIGURE 6.22: Gate voltage distribution for a supply level of 2 V with $\sigma = 0.3342\,\mathrm{V}$, $\mu = 0.7304\,\mathrm{V}$ and $N = 100$.

For the simulation of a current peak detection (Figure 6.23 and Figure 6.24), a DC current of 1 µA was used with a 10 % peak. The measured signal was the sense voltage change during the peak, which needs to be above 50 mV.

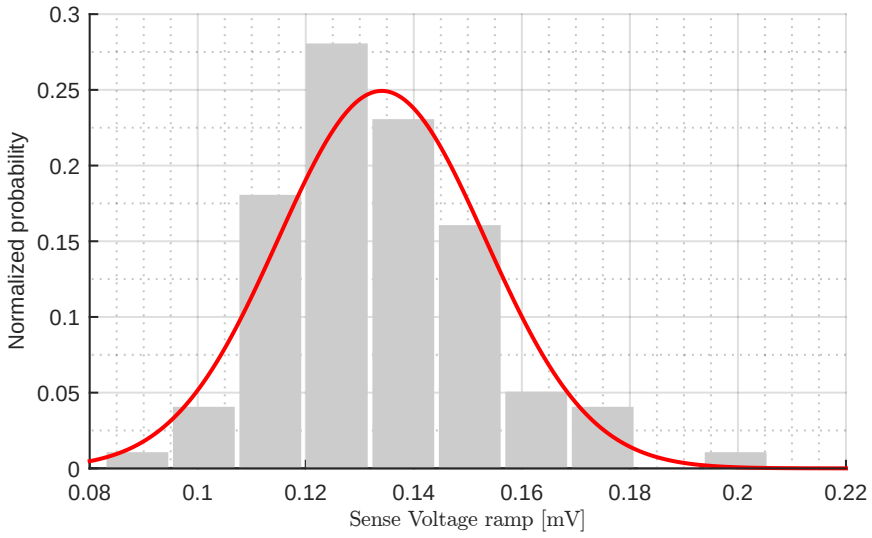


FIGURE 6.23: Sense voltage step during a peak detection for a supply level of 4 V with $\sigma = 19.2\,\text{mV}$, $\mu = 134.1\,\text{mV}$ and $N = 100$.

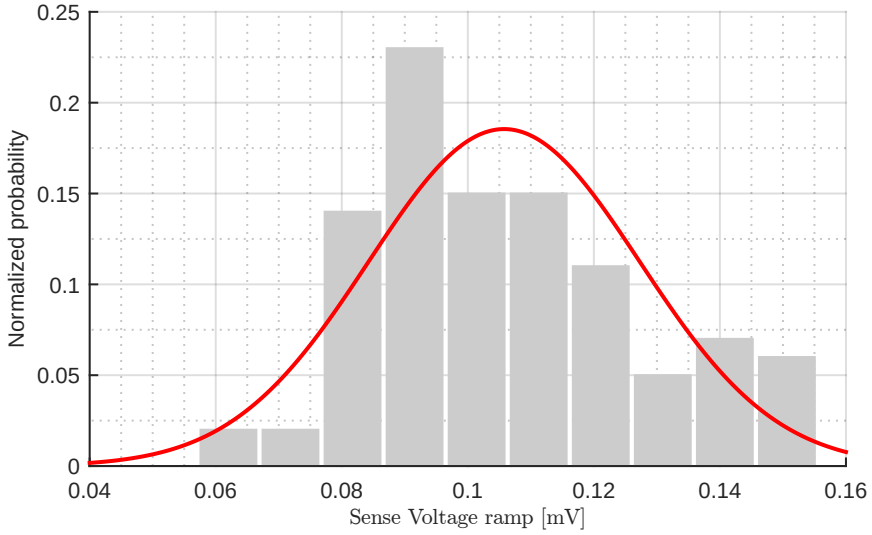


FIGURE 6.24: Sense voltage step during a peak detection for a supply level of 2 V with $\sigma = 21.5\,\text{mV}$, $\mu = 105.8\,\text{mV}$ and $N = 100$.

It can be seen that also the sense voltage is subject to a wide variation, which, as long as the specifications are fulfilled, is no major issue in case of a pure peak detection. Also inside the used energy harvesting circuit, this was accepted due to additional top level circuits which were not influenced by this variation. Therefore, saving power was preferred to an additional accuracy improvement.

6.10 Current Consumption

The current consumptions shown in figure 6.25 and 6.26 were measured under the defined supply voltage condition as mean value during the time from 100 ms to 150 ms. The curre

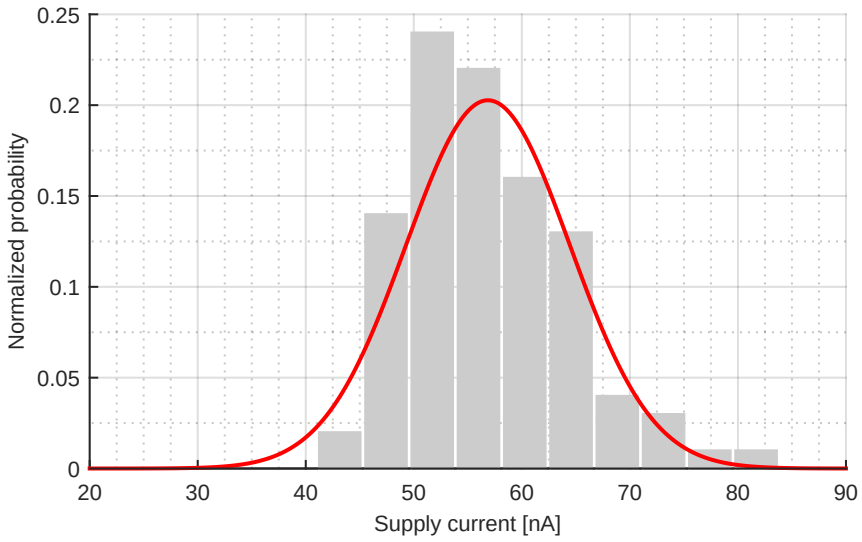


FIGURE 6.25: Current consumption at 4 V analog supply with $\sigma = 7.585\,\text{nA}$, $\mu = 56.86\,\text{nA}$ and $N = 100$.

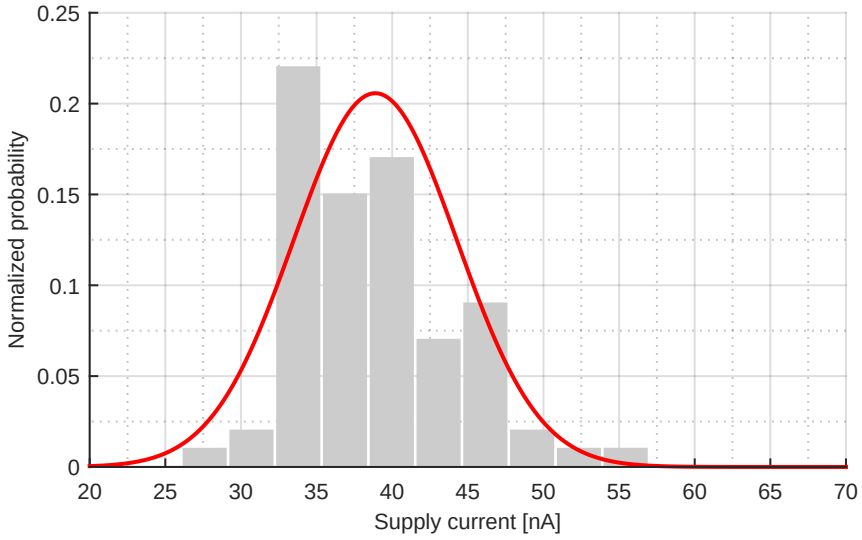


FIGURE 6.26: Current consumption at 2 V analog supply with $\sigma = 5.398\,\text{nA}$, $\mu = 38.9\,\text{nA}$ and $N = 100$.

To see the temperature effect on the current consumption of the circuit, two additional simulations were conducted for the worst-case temperature. Table 6.1 shows the current consumption at 27 °C and Table 6.2 at 100 °C.

	Supply Currents [nA]						
Supply [V]	Sense	Ampl. Out	Bias	Clock Gen.	Ampl. In	T&H	Stage Logic
2	0.138	0.757	2.09	0.093	20.3	10.5	2.76
4	0.668	1.1	2.15	0.530	27.2	10.8	6.15

TABLE 6.1: Supply current for separate blocks and under different supply voltage conditions at 27 °C. The circuit was separated into the sense element, input and output amplifiers, bias circuit, clock generation, track and hold stage and the stage logic.

	Supply Currents [nA]						
Supply [V]	Sense	Ampl. Out	Bias	Clock Gen.	Ampl. In	T&H	Stage Logic
2	2.07	1.11	2.64	1.88	27.8	13.4	14.6
4	4.78	1.31	2.71	2.91	35	14	18.4

TABLE 6.2: Supply current for separate blocks and under different supply voltage conditions at 10 °C. The circuit was separated into the sense element, input and output amplifiers, bias circuit, clock generation, track and hold stage and the stage logic.

Two main effects of the current consumption depending on the temperature can be seen. The analog circuits like sense transistors or amplifiers are increasing due to an increase of the PTAT current. This effect is small compared to the increase of the leakage current, which can be seen inside the logic cells. Looking at the current consumption of the stage logic (which mainly contains logic standard cells), the increase is happening by a factor of approximately three to five. Keeping in mind that already optimized cells were used, this effect is a major cause of a high current consumption under high temperature conditions. In terms of the overall power consumption and compared to the analog supply voltage of up to 4 V, this effect becomes less critical due to the small digital supply voltage (in the range of 600 mV). In this case, the effect might become only important again in case the temperature would be increased up to 140 °C because of the exponential increase of the leakage current.

Considering only the basic peak detection function of the circuit (without the requirement of an accurate analog output signal), the current consumption can be reduced to 15 nA to 20 nA for 2 V supply and 27 °C.

7 Layout Implementation and Test Chip

Together with the full energy harvesting circuit, the proposed current sensor from this thesis was placed on a multi project wafer (MPW). This includes photo diodes, charge pump and the current sensor itself. Due to the early point in time of the MPW, the used current sensor was a preliminary version. Therefore, only the most important blocks will be considered in the following layout chapter. For all improved circuit blocks, the impact on the layout will be mentioned as well.

7.1 Floorplan

Figure 7.1 shows the top level layout for the full test chip. Oscillators and control circuits were required for both the analog as well as the digital charge pump. These blocks are highlighted separately. The photo diodes as well as the analog charge pump are placed at the top of the test chip. Current sensor, digital charge pump and additional circuitry for the analog charge pump are placed at the bottom. For debugging purposes, all main functional blocks (photo diodes, charge pump and current sensor) may be isolated and tested individually. This was achieved by adding additional bond pads as well as metal fuses on the highest metal layer.

The bond pads can be used to analyze and/or control the most important internal signals as well as the supply domains, whereas the fuses can be used to fully isolate functional blocks from each other. Additionally, all photo diodes were connected to ground (using fuses) during the manufacturing process to avoid any unwanted influence of the diodes on the remaining circuits. These fuses need to be cut after manufacturing.

The area of the full test chip (including charge pump and photo diodes) was $0.98\,\mathrm{mm}^2$. All remaining empty spaces were filled with decoupling capacitors for the charge pump.

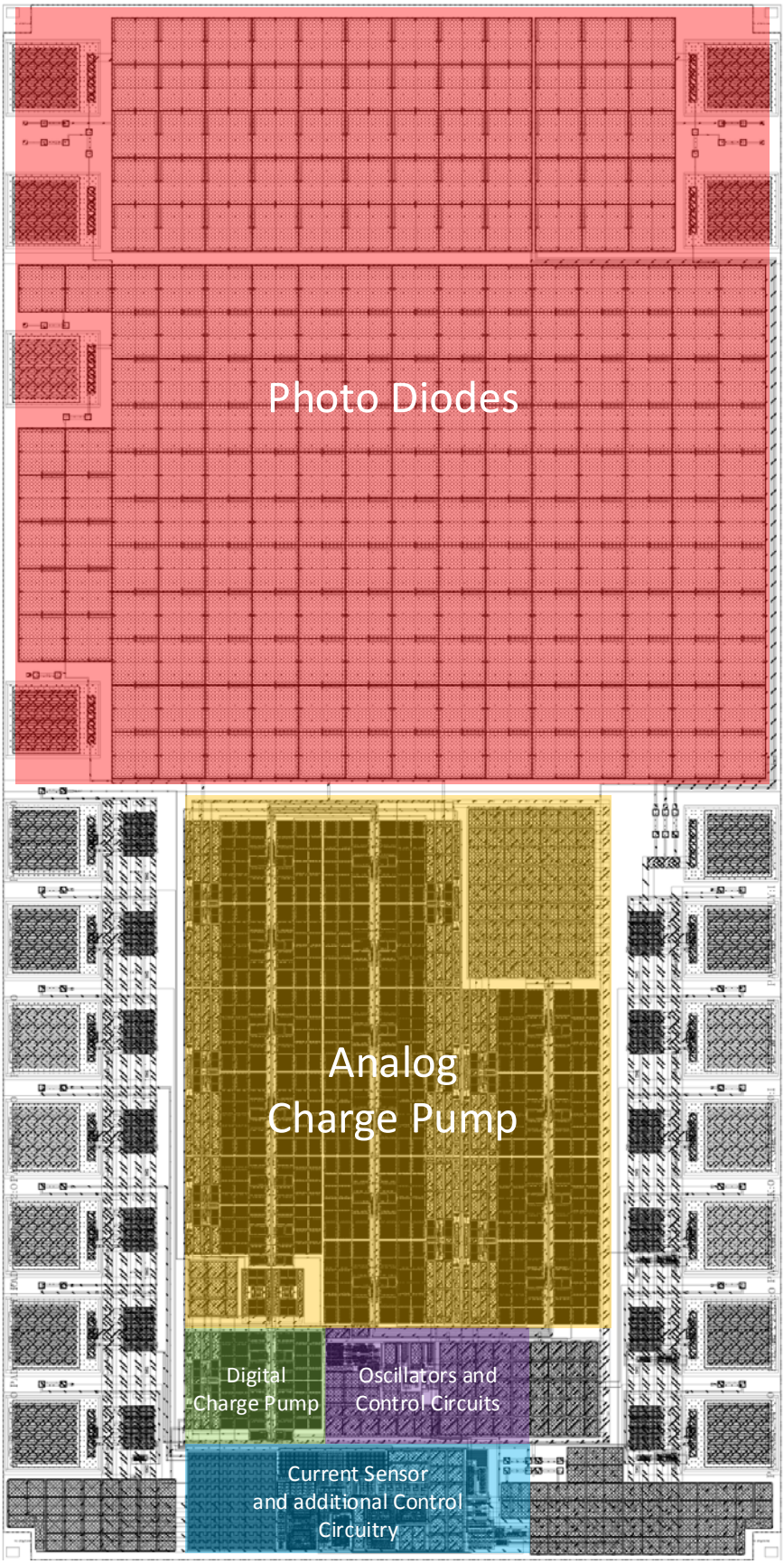


FIGURE 7.1: Top level layout of the test chip including photo diodes, charge pump as well as the proposed current sensor.

7.2 Current Sensor, Top Level

Figure 7.2 shows the floorplan of the current sensor. Approximately 50 % of the area is related to the bias resistor, the sense transistor and the capacitors from the output stage.

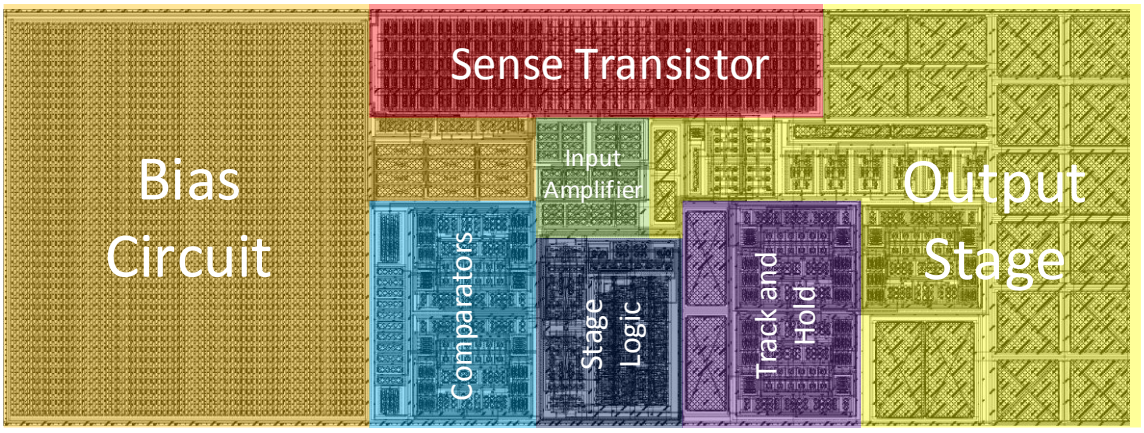


FIGURE 7.2: Layout for the current sensor including all major circuit blocks. The resulting area is mainly caused by the bias circuit resistor, sense transistor as well as output stage capacitors.

Due to the reduced input current range of the sensor, the sense transistors might be smaller compared to the expected final transistor sizes. The size of the current sensor for the MPW was approximately 250 µm x 93 µm, which results in a total area of 23 250 µm^2. The area of the final current sensor will increase roughly a factor of two. The main reasons for this are the higher input current range (which requires bigger sense transistors as well as more level shifters inside the stage logic circuit), the higher output capacitor as well as an increase inside the bias circuit resistor due to reliability reasons.

7.3 Sense Transistor

Figure 7.3 shows a detailed view of the sense transistors including input amplifier, control switches and the output mirror transistors of the bias block. Due to the architecture of the input amplifier, the two input transistors (marked with M_1 and M_2) are not to be placed inside the same n-well. It should be considered that this might add an additional offset to the input amplifier.

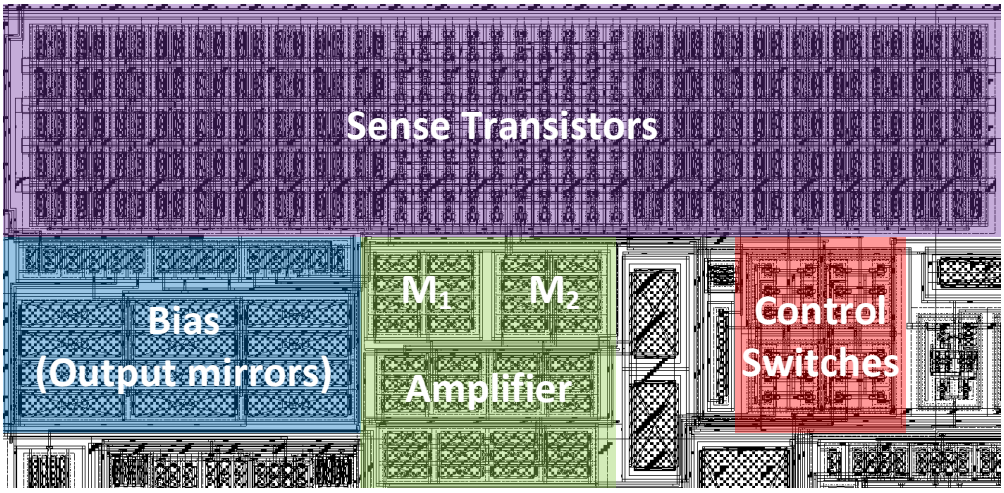


FIGURE 7.3: Layout for the sense transistor including control switches as well as the input amplifier and the output mirror transistors from the bias circuit.

7.4 Control Logic

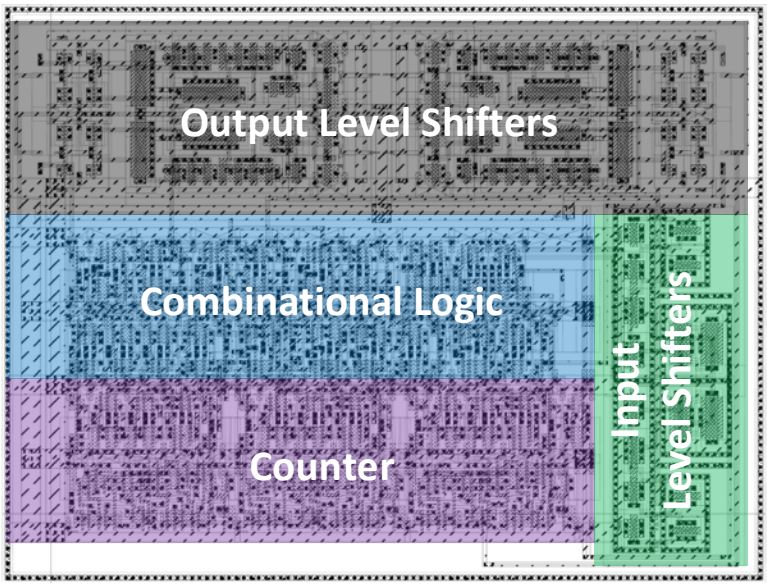


FIGURE 7.4: Layout of the control logic including counter, combinational logic and level shifters.

Figure 7.4 shows the layout for the control logic using a 3-bit counter and 4 output bits for controlling the sense transistor. Looking at the area of the single blocks, it can be seen that the level shifters require a lot of unused space. This is due to design rule related spacing between the different supply domains. Also, additional layers are required for the devices at the high supply level which requires a higher spacing to the devices inside the low supply level as well. The input level shifters do not require such wide spacing as they can be realized using only devices which can be used at the higher voltage. With an increasing number of stages, the area will get bigger as well; mainly due to additional level shifters.

7.5 Test Chip

A test chip of the energy harvesting circuit including the proposed current sensor was fabricated on an MPW. The bonding plan for the package is shown in Figure 7.5. A 24 pin ceramic dual in-line (CDIP) was used for this version of the test chip.

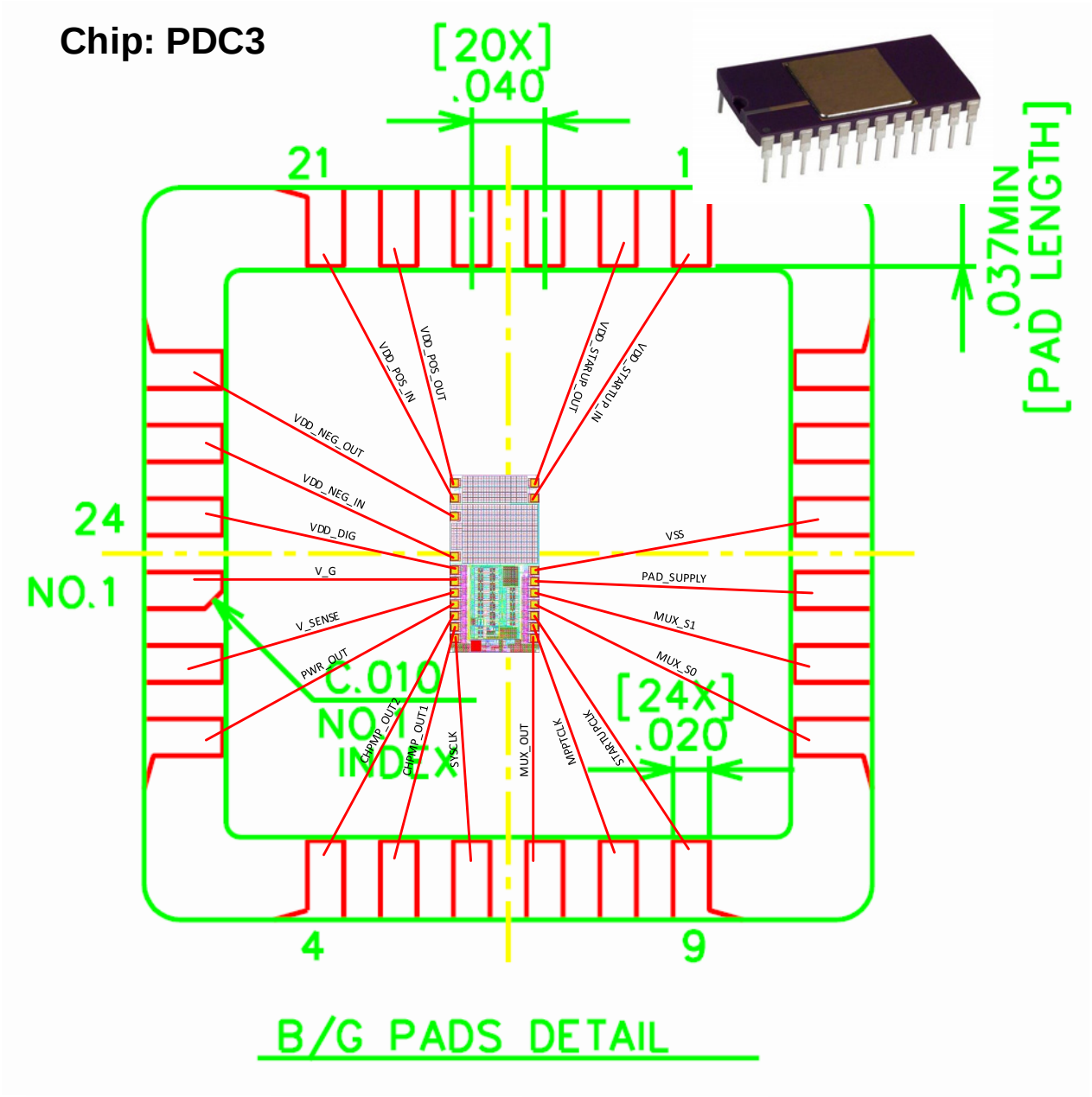


FIGURE 7.5: Bonding plan of the fabricated chip including the signal names for clarity.

Figure 7.6 shows an image of the fabricated test chip inside the final package. The die itself, the bonding wires as well, as the difference between the photo diodes and the remaining circuitry can be seen.

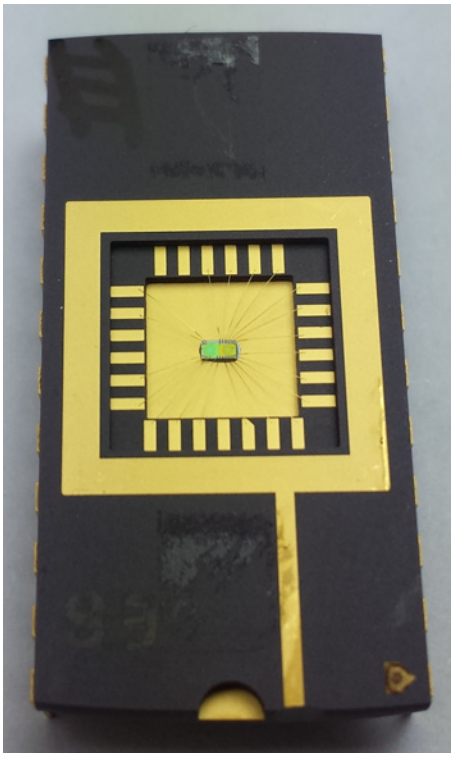


FIGURE 7.6: Image of the packaged test chip, where the die itself, the bonding wires as well as the photo diodes can be seen.

Figure 7.7 shows an image of the fabricated chip on the wafer. Due to the metal filling, only a few important devices and areas can be seen on the image. On the top side of the image, the photo diode arrays are visible, which had to be blocked for the metal filling and other remaining layers which are fabricated. Compared to the photo diodes, the remaining area was, also on the topmost metal, filled with metal filling patterns. Since no physical structures (except bond pads and fuses) were placed on the highest metal and excluded from additional layers, nothing can be seen on the image of the chip anymore.

Figure 7.8 shows a more detailed overview of the available pads as well as their basic functions. Figure 7.9 shows the position and function of the fabricated fuses. These are simple metal bridges on the highest metal level which can be destroyed by a laser. In general, there are two kinds of fuses. The red marked fuses must be destroyed after fabrication, otherwise the function of the circuit is not given anymore. The remaining fuses can be used to disconnect certain supply voltages or circuit blocks for debugging purposes. Additionally, all pads can be removed using the available fuses.

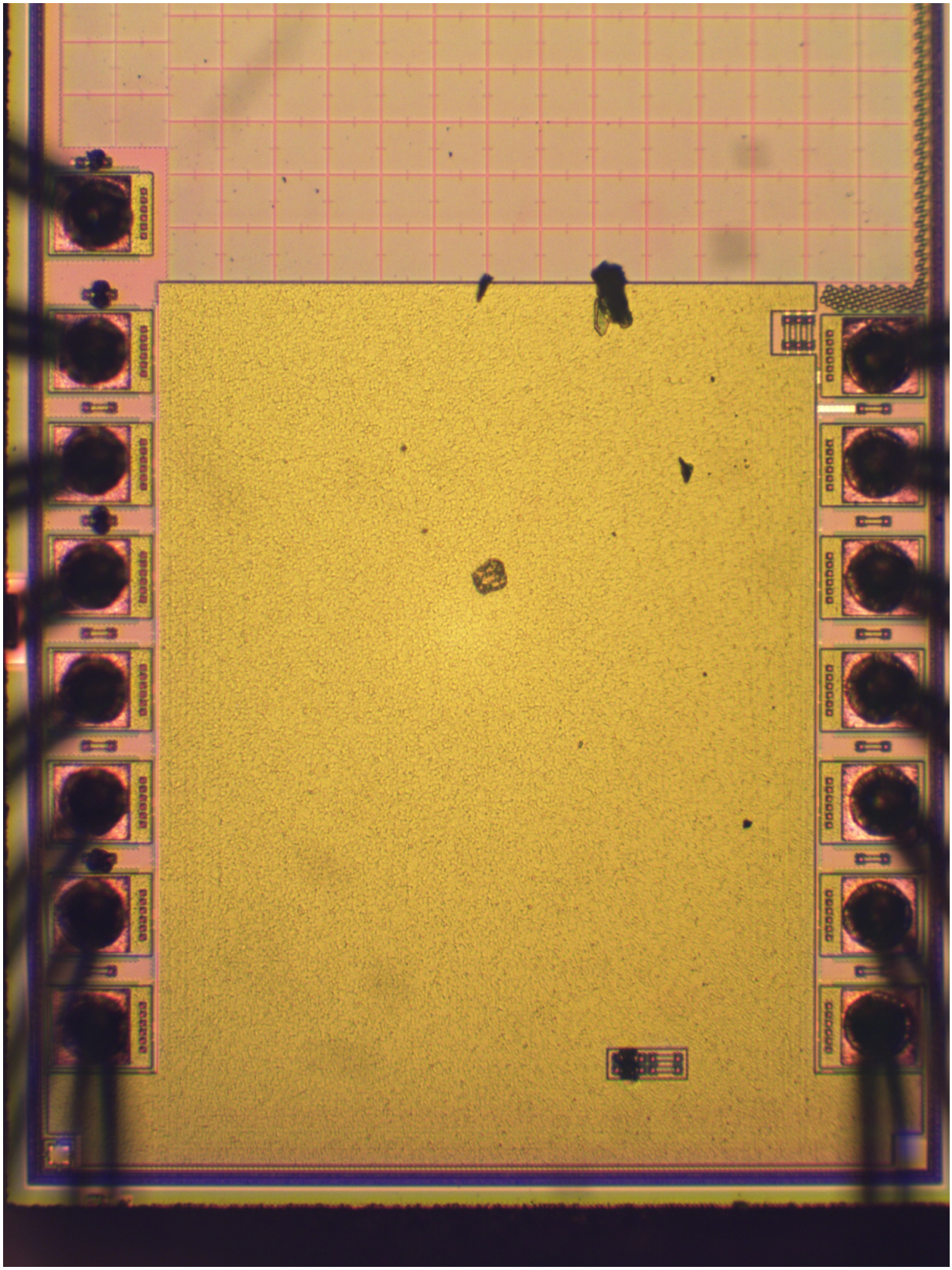


FIGURE 7.7: Image of the chip after fabrication. A part of the photo diode arrays, bonding pads as well as the fuses are visible. In the lower right corner, two fuses can be seen after cutting. The remaining circuits are not visible due to additional layers on top of the metal stack.

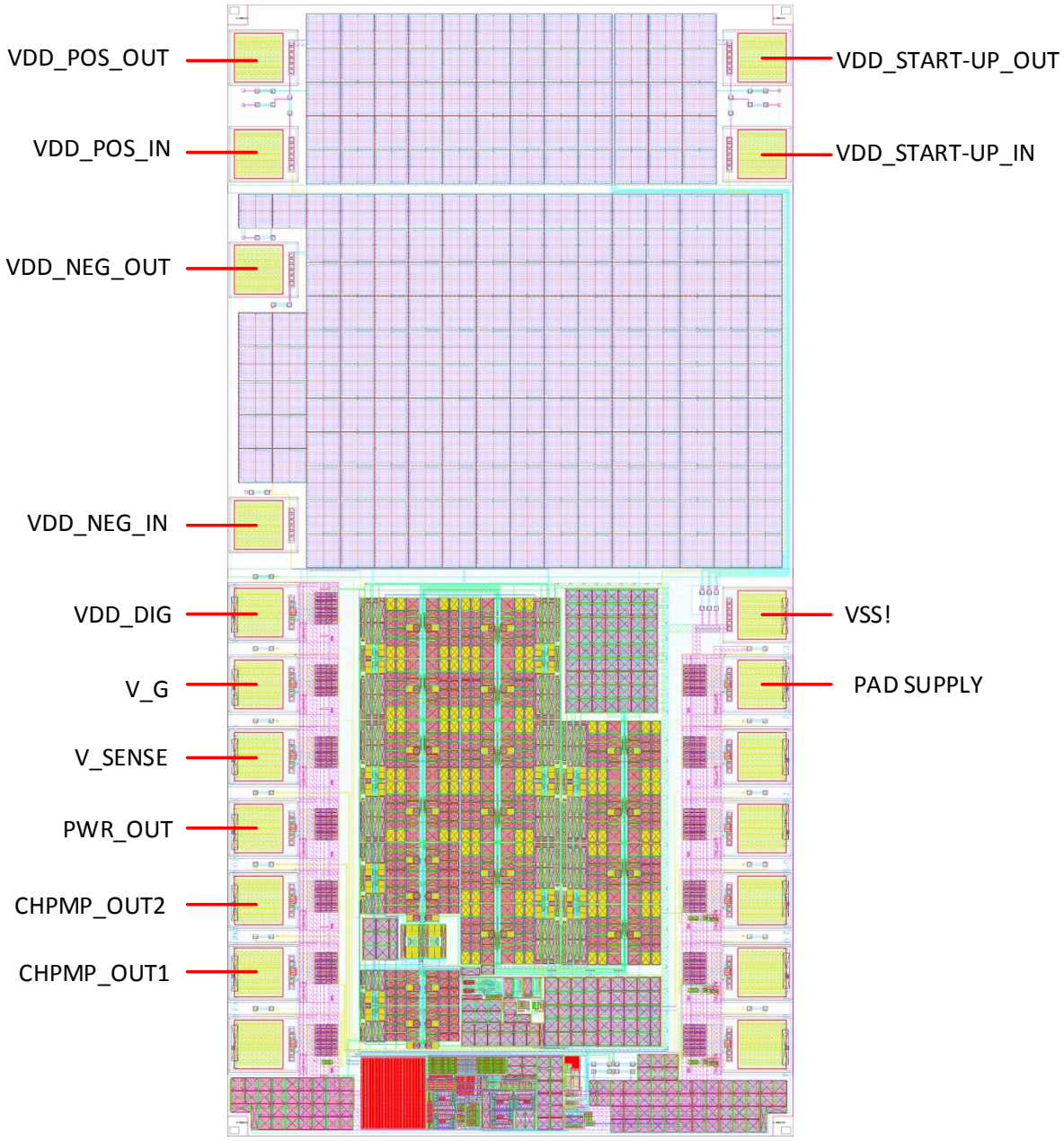


FIGURE 7.8: Position and signal name for the most important bonding pads. V_G is the gate voltage of the sense transistor and V_SENSE the output voltage of the control signal generation. VDD_DIG and PWR_OUT are the digital and analog supply voltages.

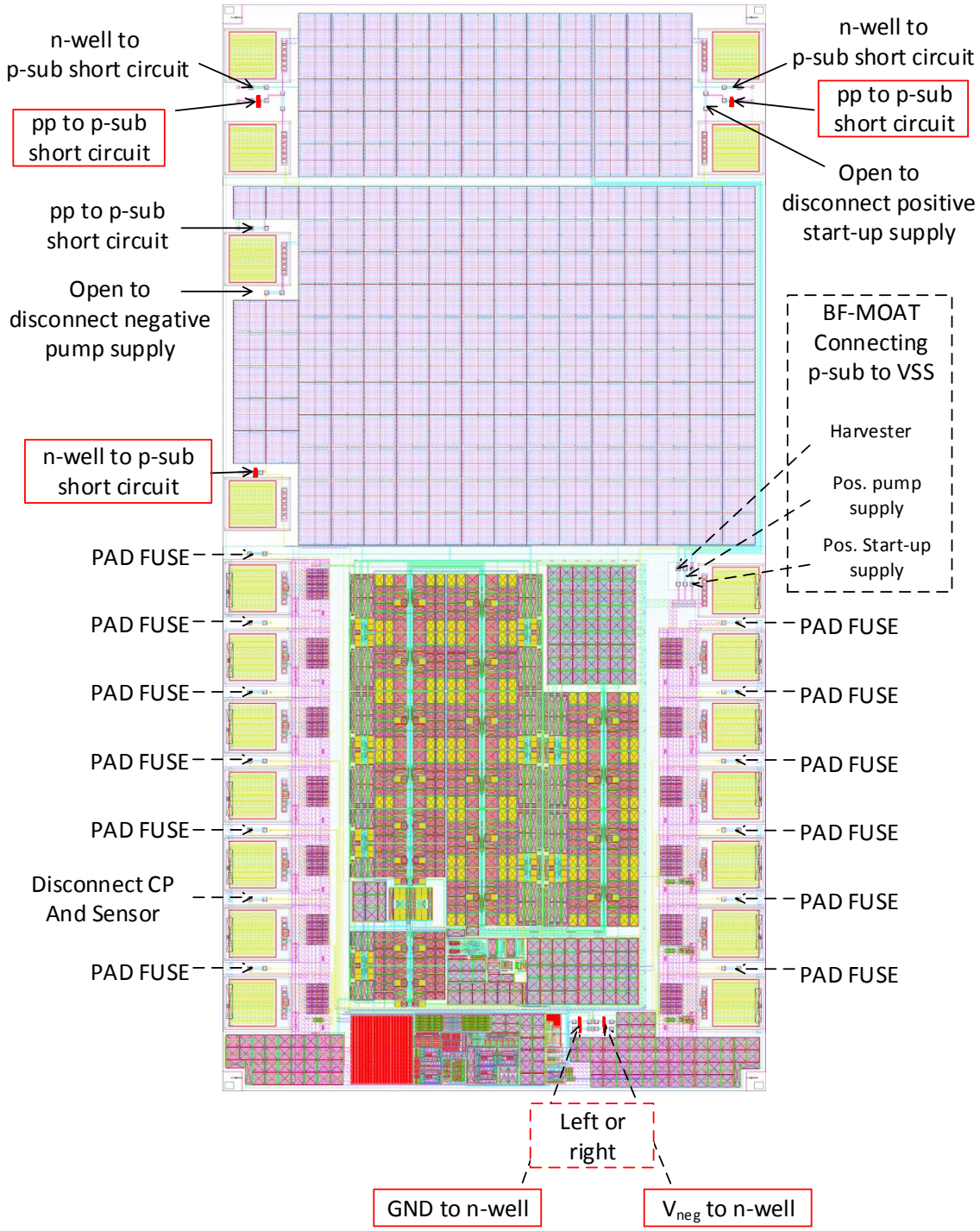


FIGURE 7.9: Detailed position and short explanation of the fuses including the fuse to disconnect the charge pump from the current sensor. Red marked fuses must be destroyed after fabrication to guarantee circuit functionality. PAD FUSES are fuses to disconnect the bonding pads from the circuitry.

8 Conclusion

The goal of this thesis was to develop a sensor for current peak detection with the main focus on ultra-low power consumption. In addition to the peak detection, other variations of the input current can be detected depending on their specifications. Therefore, the proposed sensor can easily be modified in order to be used in other architectures and also with different output signals. This allows also the usage inside regulation loops due to the analog output signal. Using this functionality, high accuracies can be achieved depending on the respective application.

The main focus during the thesis was on the generation of an analog output signal depending on the input current peaks or variations. In the case that the sensor will be used solely for peak detection without the requirement of an analog output signal, the circuit can be adapted easily, moreover leading to a reduced current consumption down to 15 nA for a supply voltage of 2 V.

The circuit was characterized during the test chip phase based on the schematic as well as the layout-extracted data. Besides extensive simulations on the current sensor itself, further possible implementations of the circuit were simulated and analyzed. For the modified circuit after the test chip phase, only schematic simulations were conducted.

The main focus during this thesis was on the power consumption of the circuit. Although the supply voltage of the digital cells was very small compared to the analog circuit blocks, the current consumption was a major problem especially at higher temperatures. Using special digital cells as well as reducing the number of used cells led to a significant reduction of the power consumption. The main analog power consumption was required for the input amplifier as well as for sample and hold buffers. These supply currents could be drastically reduced in case the sensor would be used only for peak detection measurements. This led to the previously mentioned 15 nA current consumption.

Due to the flexibility of the circuit related to input as well as output signals, the architecture may be used in different applications with only a minor amount of modifications. Especially the wider range of supply voltage levels as well as the high input current range required a lot of additional circuitry. In case of an application with limited supply variations and input current ranges, the power consumption of the circuit could again be decreased by reducing the number of stages. In the current version, the sensor includes only the basic measurement function and control signal generation. Controlling of the circuit like reset, clock generation as well as counter measures against the drift of the output voltage were done at a higher level inside the target application.

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