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Development of an Analog Capacitive Based Approximation Sensor

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Abstract

Non-mechanical switches, such as capacitive or resistive sensors that detect user defined input, are becoming more and more important in a variety of fields of application. They are used in mobile phones, domestic appliances, contactless and contact switches and for example, in switches in highly explosive environments with electric fields, where sparks should be avoided at all time.

The advantage of capacitive sensors over mechanical switches is that they can be built into a device and therefore do not have direct contact to environmental factors such as dust, humidity or temperature. Furthermore, there is almost no deterioration, as is the case with mechanical devices, and thus longer lifetime can be achieved.

This thesis illustrates the entire design process of the analog front-end of a capacitive proximity sensor for the automotive business. Firstly, system simulations with ideal components, specifications for each subblock and the technology that has been used are discussed. Secondly, the transistor level circuit design, simulations and the physical design of all components, such as comparators, charge pump, logic circuit and IO ring configuration, are examined. Thirdly, PCB design and sensor plate design are evaluated and the measurement setup is explained.

In the final part of the thesis measurement results are shown and then compared to simulation results. Moreover, findings are presented and difficulties that were encountered during the development process, as well as possible improvements of the system, are addressed.

Kurzfassung

Nichtmechanische Schalter, wie zum Beispiel kapazitive Sensoren oder Widerstandssensoren welche man für Touchscreens verwendet, werden heutzutage immer wichtiger in verschiedensten Anwendungsgebieten. Sie kommen unter anderem in Mobiltelefonen und Haushaltsgeräten als kontaklose Schalter zur Anwendung. Der Vorteil von kapazitiven Sensoren gegenüber mechanischen Schaltern ist, dass sie direkt in ein System eingebaut werden können und daher keinen direkten Kontakt zu Umwelteinflüssen, wie Staub oder Luftfeuchtigkeit, haben. Außerdem gibt es bei diesen Sensoren auch keine Abnutzungserscheinungen, wodurch eine längere Lebensdauer erreicht werden kann.

In dieser Diplomarbeit wird die gesamte Entwicklung des Analogteils eines kapazitiven Annäherungssensors beschrieben: Systemsimulationen mit idealen Bauelementen, Spezifikationen für jede Unterzelle, Auswahl der Technologie, Design auf Transistorebene, Simulationen und Layout aller benötigten Unterzellen (wie zum Beispiel Komparatoren, Ladungspumpe, Logikschaltung) und IO-Konfiguration des Chips. Außerdem wird der Messaufbau, das Design des Evaluierungsboards und das Evaluierungskonzept sowie die verwendeten Sensorplatten erklärt. Danach werden noch die Messergebnisse präsentiert und mit den Simulationsergebnissen verglichen. Zum Schluss wird auf die Schwierigkeiten, die während der Entwicklung aufgetreten sind, eingegangen und besprochen, welche Verbesserungen und Weiterentwicklungen des Systems noch gemacht werden könnten.

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1 Introduction

1.1 Project Description

The aim of this thesis is to develop an analog interface of a capacitive proximity sensor for the automotive market to be used in combination with a passive key less entry (PKE) system. An example of a PKE system can be seen in figure 1.1. The capacitive proximity sensor is placed in a car door handle and should be able to detect an approaching hand. At the moment of detection the communication between the car body unit and the car key starts and thus the car will be unlocked. This is possible due to the setup of a secure communication channel between the car and the key. There is an encrypted communication protocol in place that can lock or unlock the door and also immobilize the engine.

Figure 1.1: Passive keyless entry[23]

By detecting a hand, which is approaching the door handle rather than touching it, the communication, which will only take several milliseconds, can already start. This will result in an unlocked door at the moment somebody opens it, provided that the person has the right car key. The client should not notice anything of this process. Another benefit of using a proximity sensor is that the whole communication process will have lower power consumption, since the communication only starts when the user is very close to the door handle, the rest of the time it is in polling mode. In this mode the chip wakes up every 10 ms to 100 ms, depending on the application, to check if there is an event. The interaction between the user that is in possession of the key and the car is shown in figure 1.2.

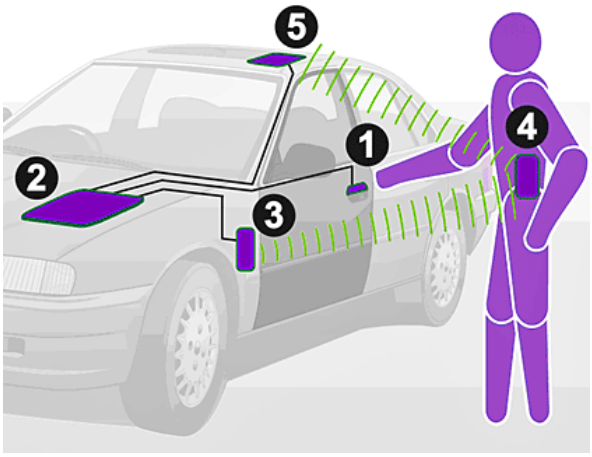

Figure 1.2: Interaction between car key and car [25]

The project was started to investigate the design of a possible new product for NXP Semiconductors. The goal was to develop a prototype of a capacitive approximation sensor targeting the automotive market and to furthermore verify if a product designed by that principle will satisfy customer needs. The product is meant to be built into a car door handle to unlock the door before the customer touches the door handle and thus notices no delay when opening the door. Releasing this chip on the market would benefit NXPs revenue, since three to five sensors would be needed per car. Another benefit of this system is the reduced power consumption compared to a standard PKE system. The polling scheme scheme that normally is employed is very power hungry. With the proximity sensor we target an extremely low power polling scheme of below 50 μA for a very short time. The developed system, which allows detecting a capacitive change on a sensing plate, is based on the patented EDISEN principle (EP 0 723 339 B1).

A current non-automotive NXP implementation of the EDISEN principle makes use of external capacitors. The objective of this thesis was to design the system in a way that the huge external capacitors, in a range between hundred nanofarad and a few microfarad, can be replaced by smaller ones, which can be integrated into the chip. Thus, a higher level of integration will be achieved and the material costs can be reduced.

The system described in this thesis uses a feedback loop to easily overcome slow changes in the environment of the sensor plate such as humidity, temperature and dust. These physical effects should not influence the functionality of the system and should not lead to a false detection of an approaching hand.

The project was divided into the following three segments, each of them being a separate diploma thesis:

1. System modeling with WREAL [10]
2. Analog front-end design and physical implementation
3. Digital processing of front-end output (up/down pulses) [11]

The first diploma thesis illustrates the development of a system model, which helps to investigate the feasibility of a design on a higher level because it allows the simulation of the whole analog and digital circuitry together in reasonable time. With behavioral models the simulation of the described system takes minutes to hours whereas a transistor level simulation would take a few days. By creating this model before the actual design, more detailed specifications can be derived from its simulation results. The development of the behavior models was started at the same time as the analog design, thus not all findings from the system model could be taken into account in the design from the beginning.

The second topic was the analog front-end design, implementation and validation, which is discussed in the following chapters of this thesis.

The third part was the digital post-processing of the output signals of the analog front-end, which is described in a separate diploma thesis. Through digital post-processing via a pulse counter and various filters, the actual detection of an approximation can be evaluated. By using different threshold values and filter types, the system is attractive for a wide range of applications.
The digital post-processing can be done in various different ways:

- Design of a dedicated digital circuit
- Digital implementation on an FPGA (Field Programmable Gate Array)
- Post-processing via LabVIEW (Laboratory Virtual Instrumentation Engineering Workbench)

1.2 Capacitive Sensors and Systems

1.2.1 Capacitive Sensors

Over the last 60 years since capacitive sensing is available, it has always become more common and easier to use. Recent technologies are more advanced and allow better control of the system, also due to the usage of micro controllers. With them, capacitive sensing, post-processing and other system relevant features are possible. Capacitive proximity sensors are becoming more and more popular since a lot of user interfaces are nowadays designed as touch panels, replacing mechanical buttons. The advantage compared to mechanical switches is that there are no moving parts and the whole sensor is not directly exposed to the environment, thus wear, cleaning or accidental spillage is not a problem. [12, 13, 14]

Different methods for capacitive sensing are currently used, for example some techniques use the measurement of the signal's rise and fall time. Also very common is the measurement of a change in frequency or duty cycle. Another possibility is the use of charge balancing via a charge pump, which is also used in this thesis. All the mentioned factors can be changed by the approximation of a finger, which leads to a change in capacitance and thus it can be detected. [1]

Capacitive sensors are used in a wide range of applications such as switches for various fields, for example light dimming or automatic limit switches. They are also used for pressure, spacing or thickness measurement as well as liquid level detectors or ice detectors for air plane wings. [1]

Compared to inductive proximity sensors, which can only be influenced by electrical conductors and the sensitivity can only be adapted by different metal types, capacitive proximity sensors react on any conductive material or material with a different dielectric constant. [12]

1.2.2 Description of a Capacitive System

By applying an electrical charge to two conductive objects, which are placed with a space between them, capacitance is generated.

$$C = \frac{\epsilon_0 \cdot \epsilon_r \cdot A}{d} \tag{1.1}$$

According to the formula above, the capacitance is proportional to the overlapping area of two plates, the permittivity of vacuum, the dielectric constant of the material between the plates and indirectly proportional to the distance between the plates. ϵ_0 being a constant, leads to three possibilities of how a capacitance change can be achieved. A sensing via the change of the dielectric coefficient is, for example, used in capacitive relative humidity sensors where the coefficient and thus the capacitance is changed due to the water that is absorbed by the dielectric material. [15]

In our case the capacitance will be influenced by the distance of the hand or finger to the sensor plate as well as the overlap of the hand or finger and the sensor area. A change of the overlapping area leads to a linear change of capacitance, whereas a change of distance results in a nonlinear change. That means that the change is bigger the closer the hand is to the sensor plate. This makes it difficult to achieve a large detection distance, since the capacitance change is very small if the approaching object is further away. [3]

To measure the capacitance change, different methods can be used. One possibility, for example, would be using an RC oscillator. In this case the oscillator frequency is determined by the sensor capacitance and thus a capacitance change results in a frequency change. The change of frequency or period can then be measured by a micro-controller. This method would require a very complex calibration circuit, since the oscillator frequency is dependent on the supply voltage as well as the ambient temperature. [8, 2, 15]

Another method, which is very accurate but also needs a very complex circuit, is measuring the AC impedance of a capacitor. With this method, the capacitor is sourced by a sine wave and the voltage and current across the capacitor are measured via a four-wire ratio-metric connection, followed by a synchronous demodulator which ensures very accurate results. [8, 2, 15]

A more common method uses a charge amplifier that transforms the sensor capacitor to reference capacitor ratio into a voltage. [8, 2, 15]

For this thesis the following method has been used: a reference capacitor as well as a sensor capacitor are charged to the same voltage and then discharged via a defined current sink. The discharge curves are then compared to reference voltages and thus the capacitance difference is detected.

The advantages of a capacitive proximity approach are that different materials (metal, nonmetal, solids and liquids) can be detected even through other materials like packages or coating. This is the case when the target has a higher ϵ_r than the material in between. Because of this fact, the sensor and chip can be completely protected and thus a long lifetime can be achieved. [19, 20]

Disadvantages of the capacitive proximity approach include the short range and sensitivity to environmental factors, for example to high humidity. A capacitive proximity sensor can also not differentiate between any approaching targets and thus an additional identification mechanism may be needed. [19, 20]

2 Analog System Description

2.1 EDISEN Patent

The concept on which this thesis is based on was developed and patented by a company named EDISEN (**E**rich **Di**ckfeld **Sen**sors). A block diagram of this principle is shown in figure 2.1

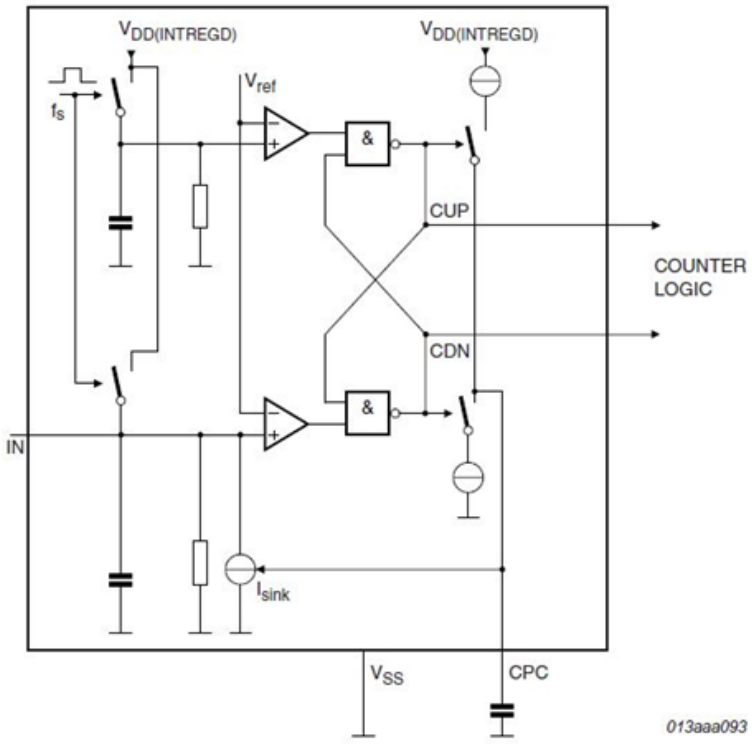

Figure 2.1: EDISEN principle [17]

The discharge time of the capacitance at the sensor input (IN) is compared to the discharge time of an internal capacitor. Pin IN is connected to a sensing plate. Both of these capacitors are periodically charged to the supply voltage via synchronized identical switches at a frequency f_s. During the time the switches are open, the capacitors are discharged via resistors to ground.
If the discharge curve of one of the capacitors falls below the internal reference voltage V_{ref}, the output of the corresponding comparator switches to logic high. The logic circuit that

follows the comparators determines which comparator switched first and gives either a pulse on CUP (charge up pulse → if the reference comparator switches first) or on CDN (charge down pulse → if the input comparator switches first).
The pulses vary the charge on the external capacitor CPC (charge pump capacitor). Whenever a pulse occurs on CUP, the CPC is connected to V_{DD} for a fixed time whereby a voltage rise on CPC is caused. On the other hand, when a pulse occurs on CDN, the external capacitor is connected to ground via a current sink for a fixed time, which causes a decrease of the voltage on CPC. If both capacitors discharge in approximately the same time, the system is in equilibrium, that means that pulses occur alternating, on CUP and CDN. [17]

If the capacitance on the input pin increases, for example due to a hand approaching the sensor plate, the discharge time of the input capacitor increases too. Thus it takes longer for the corresponding voltage to drop below V_{ref}. In this case the discharge voltage on the reference capacitor will reach the reference voltage faster and this leads to a sequence of consecutive pulses on CUP and therefore also the charge of CPC increases. [17]

An integrated calibration mechanism in the form of a voltage controlled current sink tries to equalize the discharge time of the input capacitor with that of the reference capacitor. The current sink is connected to the input pin and is controlled by the voltage on the external capacitor. The rising voltage on CPC leads to a faster discharging of the capacitance on the input. This happens until the discharge voltage on the input capacitor reaches the reference voltage faster and a pulse on CDN leads again to a small discharge of CPC.
A counter logic behind the input circuit will detect an approach if a specified number of consecutive pulses occur on CUP. If the capacitance change on the input is very slow, for example due to dust build-up on the door handle, the system will compensate this change before the sufficient amount of up pulses is reached. Fast changes in capacity, due to an approaching object, are not compensated. [17]

2.2 Architectural Overview

In figure 2.2 a simplified drawing of the newly proposed analog front-end implementation is shown. The detection of a change in capacitance is based on the comparison between the discharge time of the sensor capacitor (C_S) and the discharge time of an internal reference capacitor (C_{ref}). The value of C_{ref} is adjustable in a range between 4 pF and 60 pF to allow usage of the system with a broad range of different sensor plates.

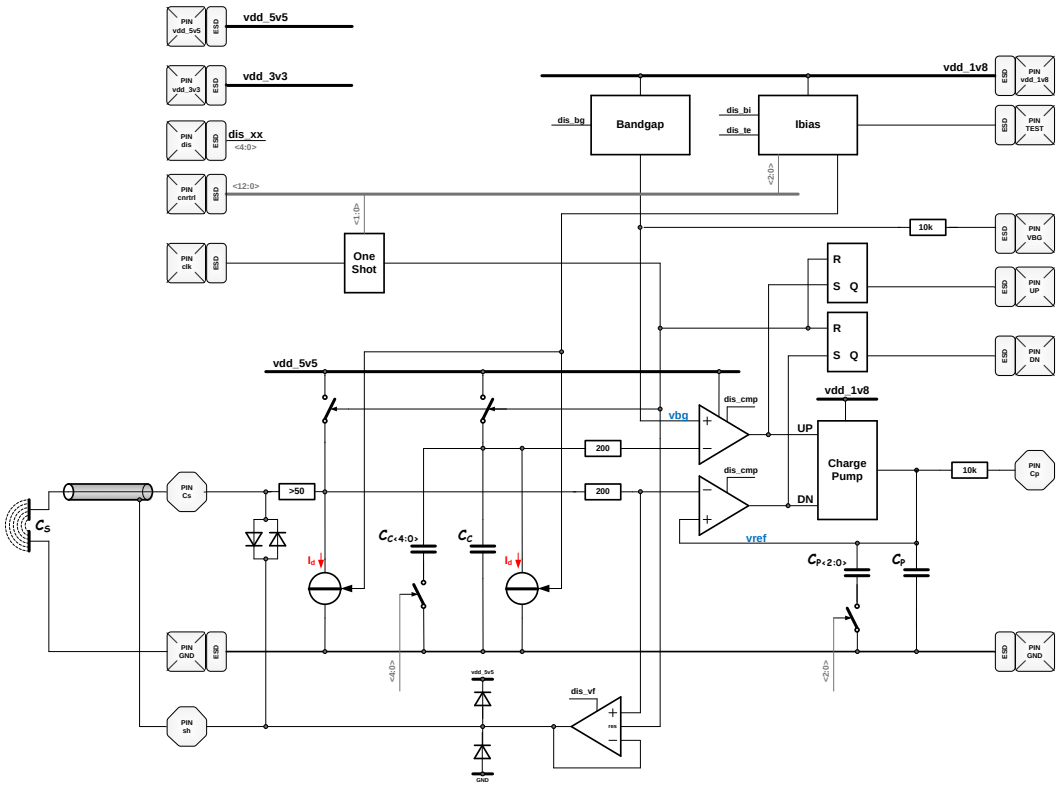

Figure 2.2: Analog front-end block diagram

The sensor C_S is connected to the input via a shielded cable. The input signal is fed back to the shield via a voltage follower to guarantee that the signal and the shield are on the same potential. Because of that, the parasitic capacitance between the signal and the shield does not influence the system and ensures the possibility to place the sensor plate further away from the body module without affecting the functionality. This means that the chip does not have to be built into the door handle, which makes assembly in the car easier.

In the beginning of every clock cycle, when the clock signal is high, C_{ref} and C_S are charged to 5 V simultaneously. When the clock signal is low, both capacitors are discharged via current sources (I_d) of the same size. The discharge curve of C_{ref} is compared with a bandgap reference voltage (vbg), whereas the discharge curve of the sensor capacitor (C_S) is compared with the feedback voltage of a charge pump ($vref$). Depending on the level of the reference voltages, one comparator switches faster than the other. A logic block generates an up or down pulse from the comparators accordingly. An up pulse leads to the charging of a small capacitor ($\approx$ 50 fF), a down pulse leads to a discharging of the same capacitor. In case of an up pulse, this charge is added to the charge pump capacitor (C_{CP}) and causes a rise of $vref$. This voltage is fed back as the reference voltage for the sensor comparator. Through a down pulse, the charge of C_{CP} will be lowered. In the start up phase only up pulses will occur until vref has reached a certain level. From this moment onwards the system will be in equilibrium, which means that alternating up and down pulses will occur.

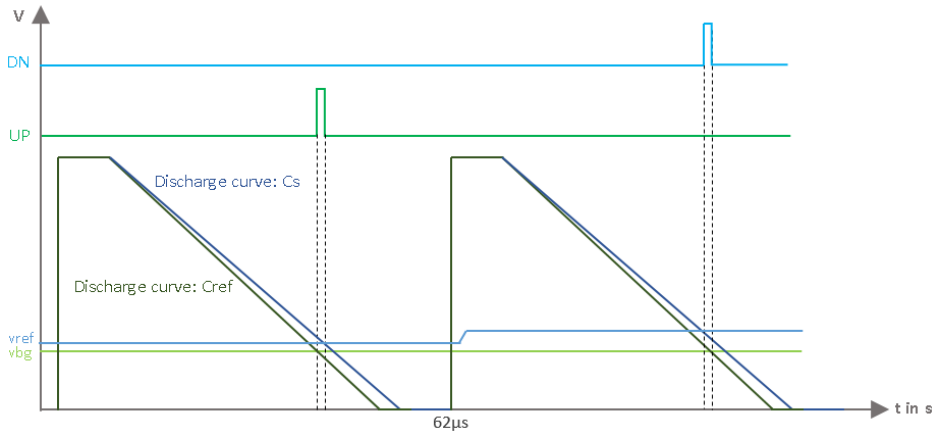

Figure 2.3: Example of one up - down cycle

A hand approaching the sensor plate acts as a parallel capacitor and thereby increases the sensor capacitance. Therefore, the discharging of the sensor capacitor will take longer and the sensor comparator will switch its state later than the reference comparator. The system always tries to reach the equilibrium state due to the voltage feedback. Hence, a sequence of consecutive up pulses will be generated to compensate for the additional capacitance. The reference comparator will switch earlier until the reference voltage is sufficiently increased to reach the equilibrium state again. If the hand is removed from the sensor area, the same applies to consecutive down pulses. The generated up and down pulses are the output of the analog part of the system. The processing of the resulting pulses is done by a digital signal processing unit, which is described in an other thesis. In this thesis the focus lies exclusively on the analog front-end of the system.

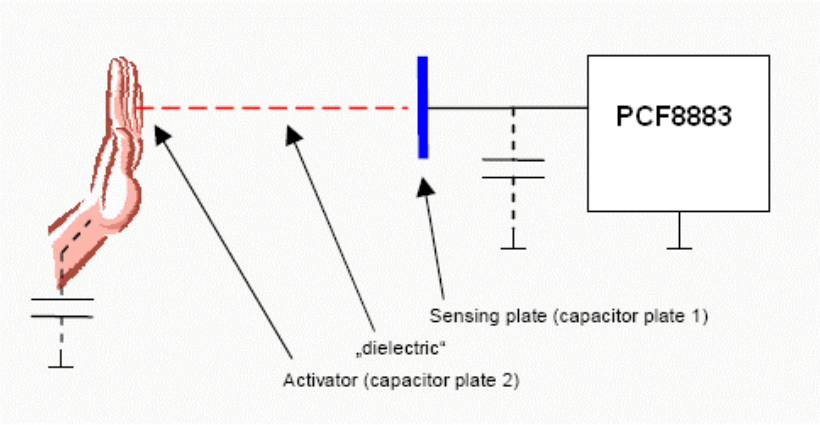

Figure 2.4: Capacitance - approaching hand to sensor plate [26]

A typical timing scheme of an approaching hand is shown in figure 2.5. In section number one of the figure it can be seen that a very fast increase and decrease in capacitance, most likely not being an approaching hand, leads to one or only a few consecutive up pulses and

thus this event is rightly not detected. Section number two shows the change in capacitance leading to a series of consecutive up pulses, which would be detected as an approaching hand. In section number three it can be seen that after a series of up pulses, the system has compensated the additional capacitance at the input and reached an equilibrium state. The last section of the graphic depicts the removal of the capacitance that was added before, leading to a sequence of down pulses and to the detection of the retraction of a hand. The picture also shows the digital post-processing in simplified terms, which could be a counter that counts the up and down pulses and resets at an opposite pulse.

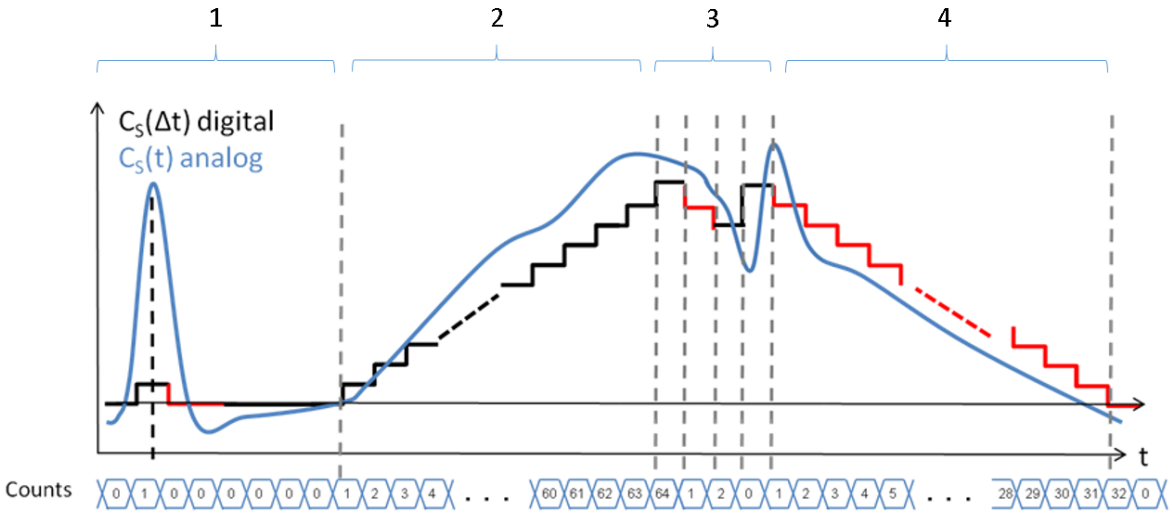

Figure 2.5: Hand approaching signature

The system is designed for operating with a clock frequency of 16 kHz. This frequency was chosen due to customer requirements to detect an approaching hand within 4 ms. An approach is represented by 64 consecutive up pulses, which is an arbitrarily chosen number sufficiently large enough to overcome false detections.
The sensitivity of the system can mainly be adjusted by variation of the trimmable charge pump capacitor. Additional factors and settings that influence the sensitivity will be outlined later in this thesis.

2.3 Requirements and Specification

There already exists a capacitive proximity switch from NXP that operates according to the EDISEN principle, the *PCA*8886 [17]. This chip was designed for the consumer market and hence it is not automotive qualified. Also, the detection distance of the *PCA*8886 is smaller than the new specifications given by the customer. Furthermore, the design data of this chip is not available within NXP. It was therefore decided to start the design from scratch to meet heightened customer requirements.

The high level specifications for the system, which are shown in table 2.1, were defined by collected customer requirements. The practical information regarding feasibility was missing, since this is the first test chip in this field of application. In order to get more detailed specifications, especially for the subblocks, a schematic of the complete system with ideal components was set up and simulated. The information about the needed blocks to fully integrate this system was derived from these simulations as well.

Standby (average) current	$< 50\,\mu$A
Supply voltage IC	3 V to 5 V
Operating temperature	-40 *to* 85 °C
Input capacitance range	5 pF to 60 pF
Range of detectable change of capacitance	20 fF to 300 fF
Resolution	1 fF to 2 fF
Package	small, cheap, standard
Dielectric constant of integration materials (door handle housing, pottering material, etc.)	3 *to* 4
Number of Channels	1 *to* 4
Locking Feature	Touch
Detection range: Finger-2-door handle	5 mm
Detection range: Finger-2-sensing plate)	10 mm
Detection time	16 ms
Number of samples(typical/minimum)	3/1
Unlocking Feature	Proximity + touch
Detection range: Finger-2-door handle	20 mm
Detection range: Finger-2-sensing plate)	25 mm to 27 mm
Detection time	4 ms
Number of samples(typycal/minimum)	2/1

Table 2.1: Customer requirements

2.4 Process Node Description

The process used for the implementation is a CMOS (complementary metal-oxide semiconductor) 0.14 μm process for non-volatile memory applications. The CMOS14 process was chosen because it is possible to integrate the capacitors described in the requirements within a reasonable area. Another reason was that also the digital circuit would function while at the same time maintaining the low current consumption requirements. Implementing this application in very small technology nodes would not be feasible, since the leakage current

increases with shrinking devices. The option AMS NV (analog mixed signal, non-volatile) was chosen, to be able to reuse some already proven circuitry of other projects running on this process type.

It is a six metal process that supports, among others, the following features [18]:

- High-resistive substrate
- Multiple wells:
  - Logic nwell (NWELL), logic pwell (PWELL)
  - Deep nwell (DNWELL)
- Multiple gate oxides:
  - GO1: optical thickness 2.9 nm; nominal operating voltage: 1.8 V
  - GO2: optical thickness 7.2 nm; nominal operating voltage: 3.3 V
  - High Voltage: optical thickness 25 nm; nominal operating voltage: 10 V
- Low-k dielectric for METAL1, 2, 3, 4 ($\epsilon_r = 3.6$)
- Minimum gate length and polysilicon interconnect width: 0.16 μm
- Minimum metal width/space
  - METAL1, 2, 3, 4: 0.256 μm
  - METAL5: 0.512 μm
  - METAL6U: 3 μm

The physical dimensions of the used process are illustrated in figure 2.6. The height of the metal, poly and oxide layers as well as the dielectric constant and thickness of the isolation layer in between is shown.

To be able to supply the chip directly with available voltages (higher than 5 V) in the car, the SOI (silicon on insulator) option could be chosen for a future product integration without having a significant performance loss.

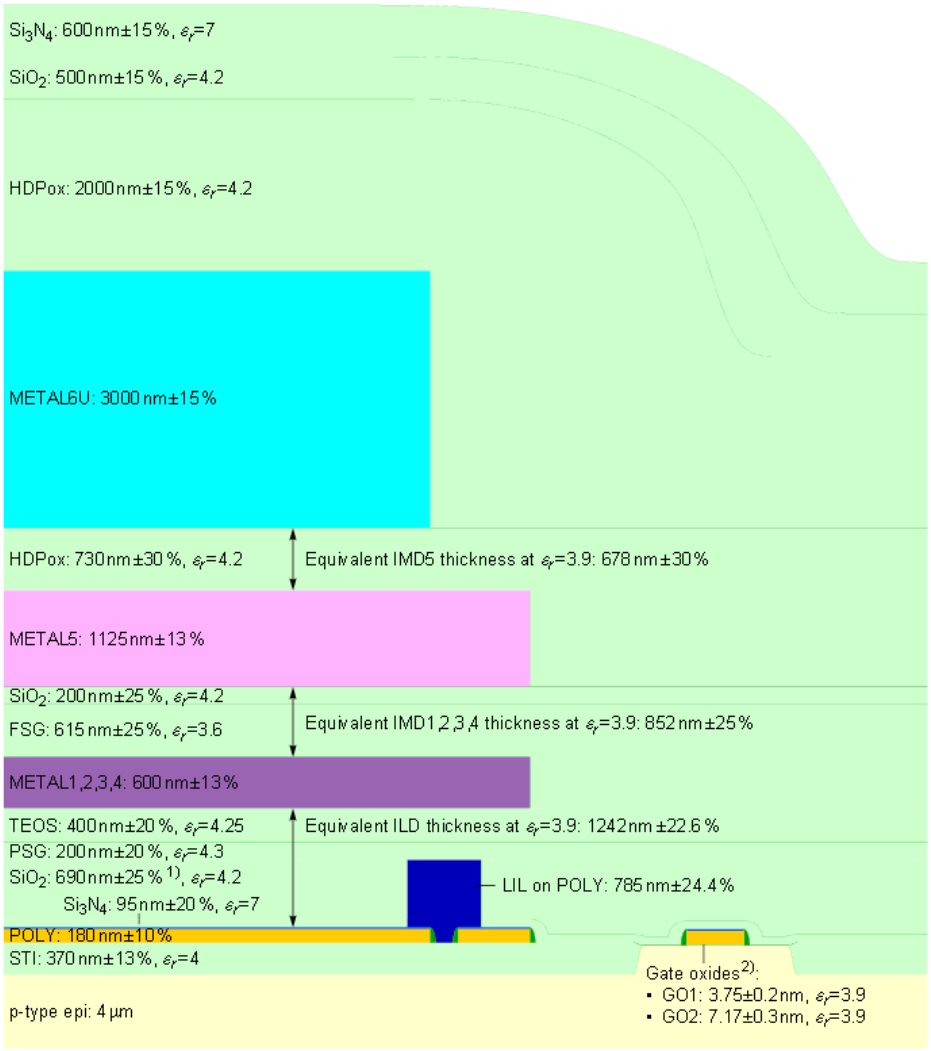

Figure 2.6: Vertical dimensions of CMOS14AMS-RF process [18]

2.5 Transistor Model Used for Simulation

For schematic simulations the NXP/Philips internal model MOS Model 11 (MM11) is used. The parameters that are used in this model are determined from I-V and C-V measurements. It is a symmetrical model, which means that the drain and source have the same behavior. The older MM9 or BSIM4 models, by contrast, have no symmetrical behavior. It is a physics based model that gives an accurate transition description for weak to strong inversion. The MM11 includes DC (direct current)-, AC (alternating current)- and noise modeling. Because of its accurate description of all important physical effects, it is suitable for digital, analog and RF Design for modern and future CMOS technologies. [16]

Among others, the following physical effects are taken into account in the MM11 [16]:

- Mobility reduction
- Bias-dependent series resistance
- Velocity saturation
- Gate-induced drain leakage
- Gate depletion
- Bias-dependent overlap capacitance

In figure 2.7 the basic structure of the MOS Model 11 is shown.

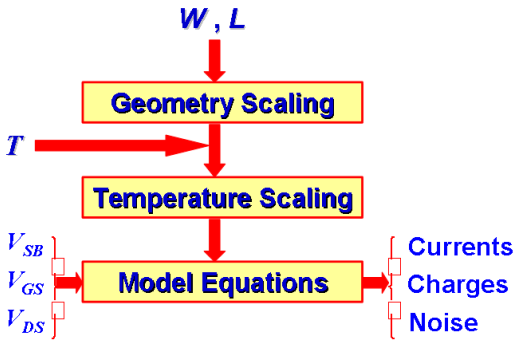

Figure 2.7: Structure of MOS Model 11 [16]

Figures 2.8 and 2.9 show ProMOST simulations of a standard GO1 NMOS and PMOS transistor used in this technology. Both transistors have a width of 10 μm and a length of 2 μm. The figures show the I_{ds} over V_{ds} curves over temperature ($-40\,^{\circ}$C, $25\,^{\circ}$C and $125\,^{\circ}$C) and fast and slow corners. The DC operating points at room temperature are shown as well.

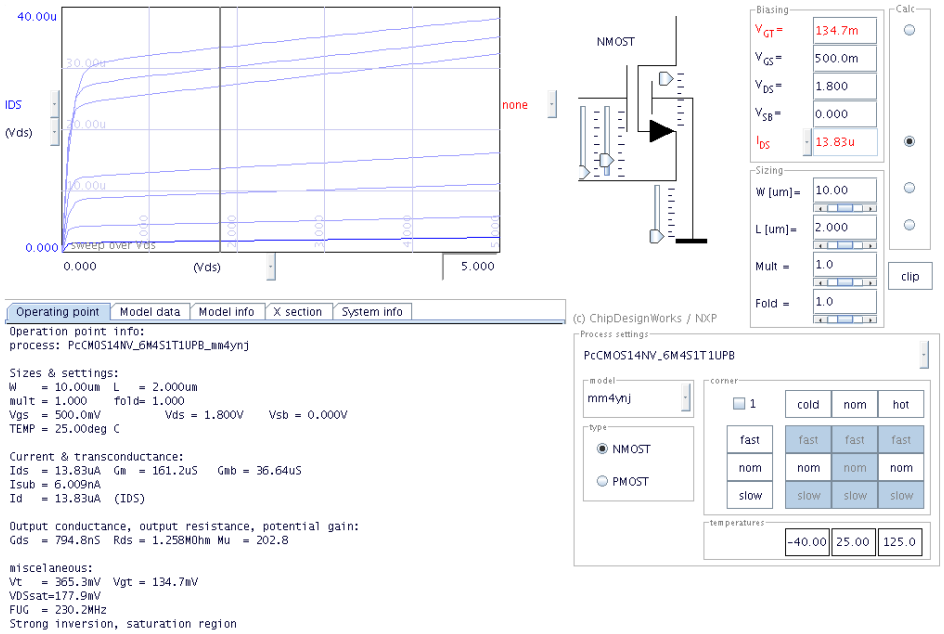

Figure 2.8: NMOS MM4YNJ DC parameters

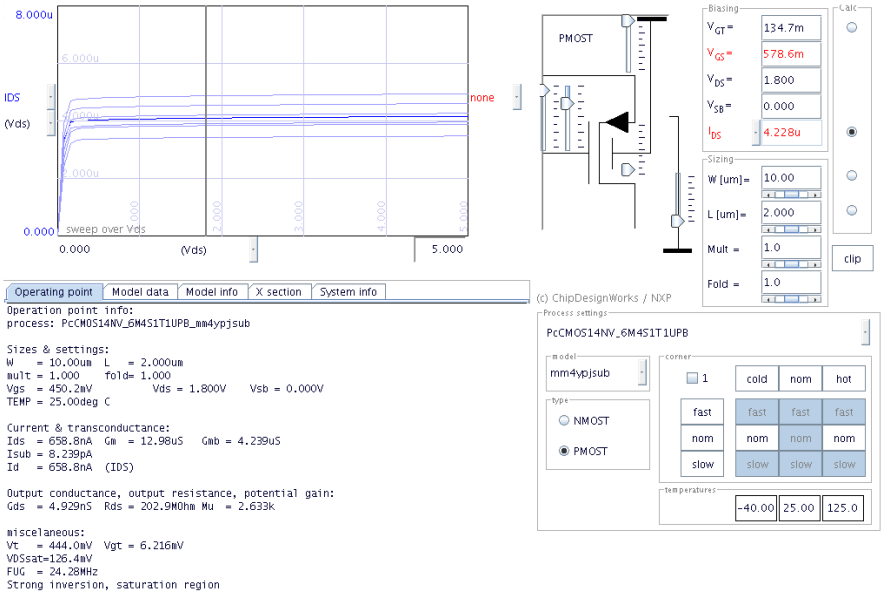

Figure 2.9: PMOS MM4YPJSUB DC parameters

In the following chapters the development of the analog front-end will be discussed. Firstly, it will be shown how a schematic with ideal components is created and simulated and how these ideal components are replaced by transistor level blocks until the whole system is built. Secondly, transistor level simulations and the physical design will be shown and it will be illustrated how a pad-ring is created to be able to access the chip's inputs and outputs from the outside world. Thirdly, the reader will see how all blocks, including the pad-ring, are combined, how a complete chip is built and taped out and how sensor plates and an evaluation PCB are developed to be able to measure the chip in the lab. Finally, measurement results, problems that have occurred during the process, findings and possible improvements for the future will be discussed.

3 System Equations and Simulations

3.1 System Simulations with Ideal Components

The first step of the development was to simulate the system, which is based on the EDISEN principle described in chapter 2.1, with ideal components in *Cadence®Virtuoso®*. This software is used to draw, optimize, simulate and verify analog designs. It is also used to create the physical design as well as all necessary steps to generate a mask set for chip production. The first objective was to build the system with ideal sources, comparators and logic gates for a clock frequency of 16 kHz and 5 V power supply. The reason for choosing this frequency is that customer demands require the chip to detect an approximation (64 consecutive pulses) within 4 ms. The schematic of the system with ideal elements is shown in figure 3.1.

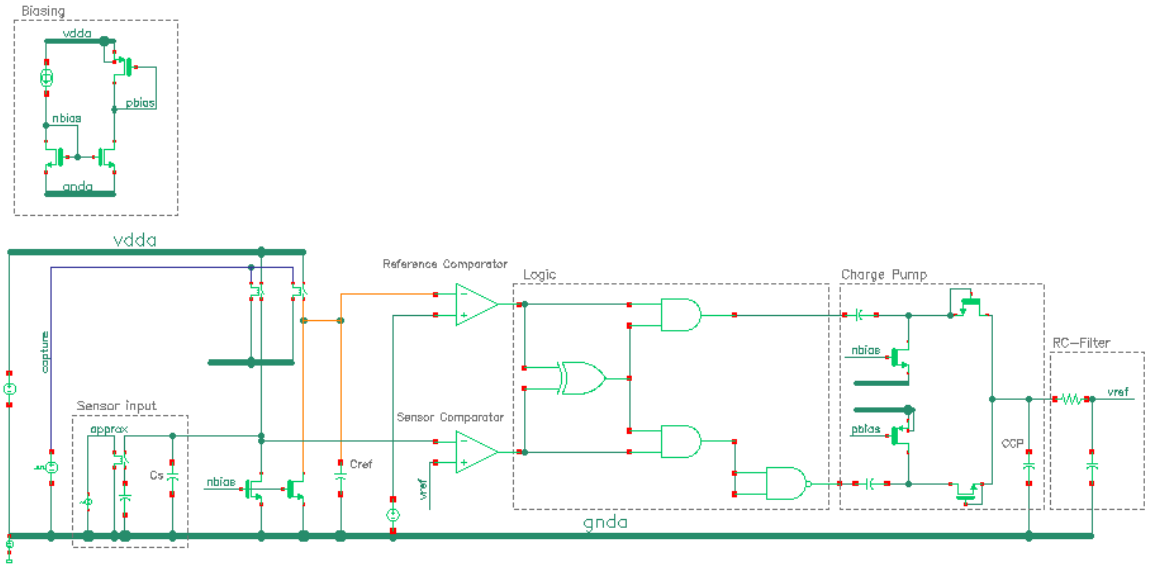

Figure 3.1: First concept with ideal components

The initial approach to accomplish a functioning system was to use a slower clock with a period time of 4 ms and a pulse width of 100 μs. A current of 100 nA was used to discharge the reference capacitor and the external capacitor within one clock period. The voltage on the reference capacitor was compared with a fixed voltage of $\frac{V_{supply}}{2} = 2.5\,\text{V}$, whereas the

sensor capacitor was compared with a variable voltage from the charge pump output.
The logic gates at the comparator outputs detect which of the two comparators' input voltages drops first below the reference voltage, and produce a pulse on either the reference or the sensor side. Due to this pulse, a small capacitor is charged or discharged. This causes the voltage on the charge pump capacitor, which is the reference voltage for the sensor capacitor, to rise or fall. Figure 3.2 shows a schematic of the first charge pump concept.

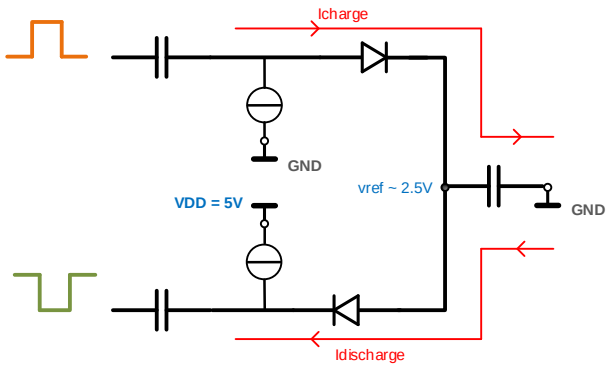

Figure 3.2: Block diagram of the first charge pump concept

Because the input capacitors are of equal size, an equilibrium will be reached as soon as the charge pump voltage is at the same level as the reference voltage and pulses will occur alternately on each side.
If the sensor input capacitor increases, its discharging voltage will reach the charge pump voltage later than the reference capacitor reaches the reference voltage. In this state the reference capacitor will always switch first and therefore pulses will only occur on the upper side. The charge pump voltage will increase until it is high enough that the sensor comparator switches before the reference one. In figure 3.3 a transient simulation result of the circuit described above is shown. The simulation results show the behavior of the chip when switching it on as well as a typical hand approach and removal.
In the start up phase only up pulses occur until the reference voltage ($vref$) reaches a voltage level of about 2.5 V. It can be seen that from this moment on up and down pulses alternate and the system is in equilibrium. At 7.5 s in the simulation the switch at the sensor input was closed and and opened again at 8.5 s. Thus, an extra capacitance was added and removed again after 1 s. The transient results show that when adding the capacitance, only up pulses occur until the system compensates for that change. The system reaches the equilibrium state again in the period of time before the capacitance is removed. Since in this case the capacitance of the sensor input is higher than the reference capacitance, the reference voltage also needs to be higher. When removing the capacitance, a series of down pulses can be seen and after that the system is again in equilibrium. The amount of up and down pulses is not the same, because after the series of up pulses the reference voltage is not at the middle point anymore, leading to an unsymmetrical charge pump behavior. In chapter 4.4 this is described in more detail.

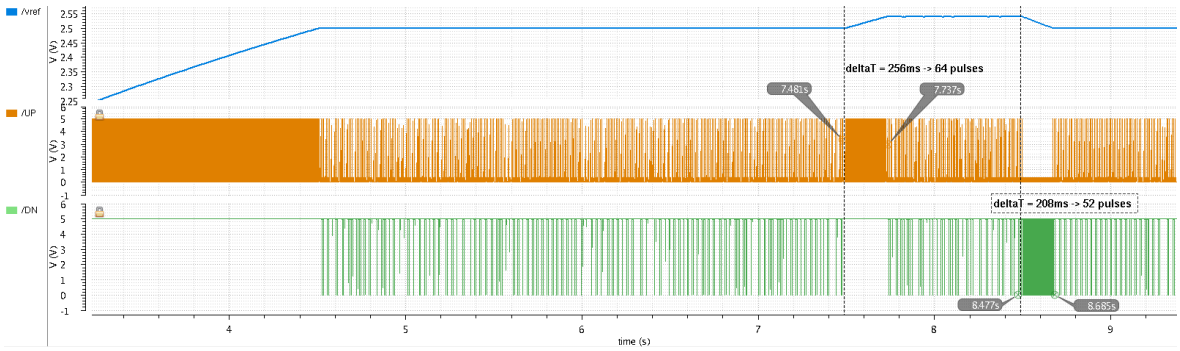

Figure 3.3: Simulation with ideal components

As a next step the system was adapted to the required clock frequency. A clock with a time period of 62 μs and a pulse width of 2 μs was used. Furthermore, the charge pump was adapted to avoid mismatch problems. This was done in such a way that only one capacitor, for adding/reducing charge to/from the charge pump capacitor, is used for both reference and sensor side. Another measure to reduce the power consumption was to shift the comparator output stage and all following blocks to a lower supply voltage. These blocks will be supplied by 1.8 V, which also causes the middle point of the reference voltage to decrease to $\frac{V_{supply}}{2} = 0.9\,\text{V}$.

Another requirement was to drive a long cable going from the body control unit towards the door handle where the sensor plate will be placed. The model of a coaxial cable (shown in figure 3.4) was introduced to simulate the influences of the cable connection on the system.

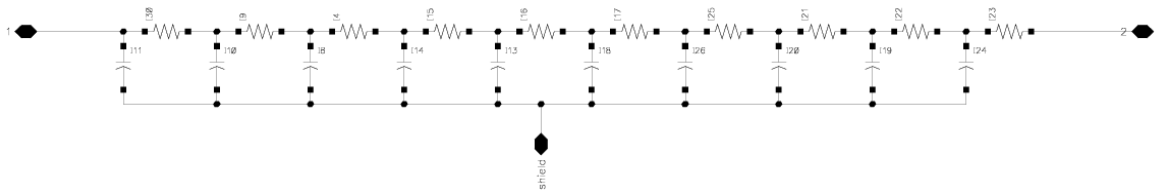

Figure 3.4: Schematic of coaxial cable with parasitic components

The following equations show the calculation of the capacitors and resistors of the cable model under the assumption that a coaxial cable has a capacitance of 100 pF and a resistance of $\frac{1}{42}\,\Omega$ per meter length, assuming a cable with a inner conductor made of copper ($\rho_{cu} = 0.0178\,\frac{\Omega mm^2}{m}$) with a cross sectional area of $0.75\,mm^2$, is used.

$$C = \frac{length\,[m]}{10} \cdot 100\,pF \tag{3.1}$$

$$R = \frac{length\,[m]}{42\,\frac{m}{\Omega} \cdot 10} \tag{3.2}$$

If the shield of the coaxial cable is connected to ground, an additional capacitance will be added to the sensor input. The longer the cable the more capacitance will be added. Since the system application requires the possibility to place the chip at a different position as the sensor plate in the car, the cable influence should be as small as possible. To overcome the influence of a cable capacitance, the sensor input signal is also applied to the cable shield via a voltage follower. Figure 3.5 shows the configuration of the interface between the chip input and a touch sensor as well as the interaction with the human body.

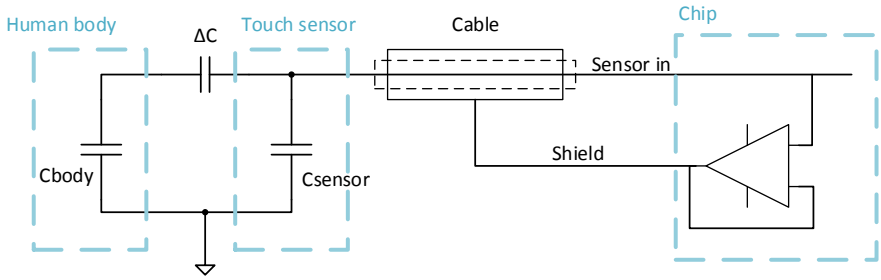

Figure 3.5: Voltage follower configuration

In figure 3.6 the discharge behavior of both the sensor capacitor and the reference capacitor is shown. The reference capacitor was set to 40 pF in this simulation. At approximately 30 μs simulation time, the discharge voltage crosses the bandgap voltage and thus causes the reference comparator to switch. The discharge curve of the sensor capacitor is slightly steeper than the other one because the sensor capacitor was set to a lower value in this simulation. This configuration causes the reference voltage to settle around 784 mV in the equilibrium state.

In this configuration the sensor comparator will also switch at about 30 μs. If the reference capacitor switches first, an up pulse that leads to an increase of the reference voltage is generated. Because of the higher reference voltage, the sensor comparator will switch first in the next clock cycle and a down pulse will be generated.

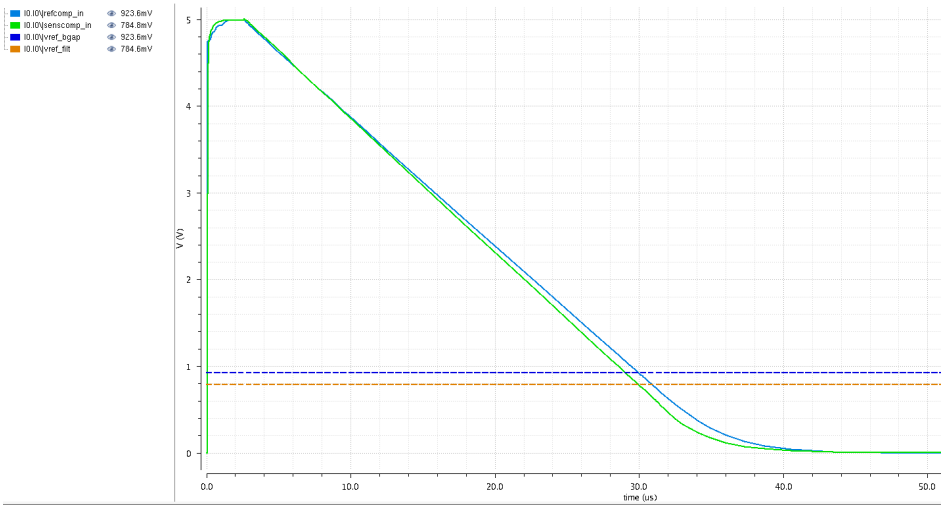

Figure 3.6: Discharge behavior of sensor capacitor and reference capacitor

From these first simulations with ideal components more detailed circuit specifications could be derived, which are necessary for the transistor level design of the sub-blocks. These blocks will step by step replace the ideal components until the whole system is completed at transistor level. In chapter 4 the design of all required blocks will be described in detail.

3.2 System Equations

The following calculations show the expected amount of up pulses, the reference voltage change per femtofarad change as well as the reference voltage change per up or down pulse, for specific system configurations. The result is dependent on several different settings.

$$I = C \cdot \frac{dV}{dt} \tag{3.3}$$

$$dt_{ref} = C_{ref} \cdot \frac{Vdd\_5v5 - vbg}{I_{discharge}} \tag{3.4}$$

The necessary increase of vref after an increase of C_{sensor} by $C_{approach}$ can be calculated the following way:

$$vref_{approach} = Vdd\_5v5 - \frac{I_{discharge} \cdot dt}{C_{sensor} + C_{approach}} \tag{3.5}$$

$$\Delta vref_{total} = vref_{initial} - vref_{approach} \tag{3.6}$$

The amount of voltage increase per clock cycle is dependent on the charge pump capacitor (C_{cp}) and the actual level of the reference voltage. The higher the reference voltage the smaller the voltage increase per clock cycle.

$$Q_{C0} = C_0 \cdot Vdd\_1v8 \tag{3.7}$$

$$vref_1 = \frac{(Q_{C_{CP}} + Q_{C0})}{(C_{CP} + C_0)} \tag{3.8}$$

$$\Delta vref_{step} = vref_1 - vref_0 \tag{3.9}$$

In figure 3.7 the slope change of the discharge curve of the sensor capacitor, at a capacitance increase, is shown. It can be seen that for an increase of capacitance by 100 fF, the reference voltage has to be increased by 14.1 mV to reach an equilibrium state again.

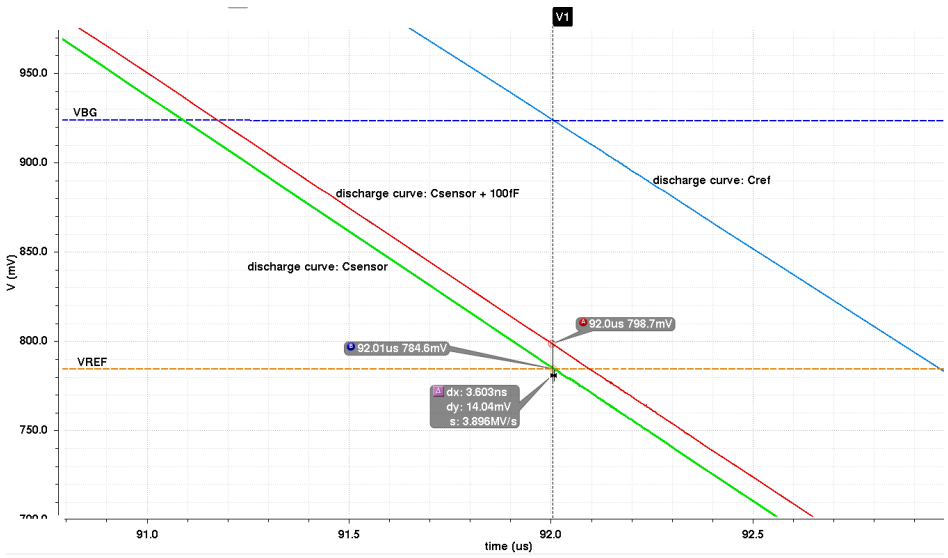

Figure 3.7: Discharge curves and reference voltages

$$Number\ of\ steps = \frac{\Delta vref_{total}}{\Delta vref_{step}} = \frac{14.1\ mV}{145.14\ \mu V} = 74\ pulses \tag{3.10}$$

This means that an increase of C_{sensor} by 100 fF leads to a continuous sequence of more than 74 up pulses.

Charge per up/down pulse	45 fC
vref change per up/down pulse	13 μV to 120 μV
vref change per capacitance change	$\frac{500\,\mu V}{fF}$
Min. theoretical detectable capacitance change	1 fF

Table 3.1: Calculated system sensitivity parameters

The maximum sensitivity can be reached with the smallest reference capacitor setting and the highest charge pump capacitor setting. The high charge pump capacitance setting leads to the biggest ratio between C_0 and C_{CP}, whereby more charge exchange steps are necessary to increase the reference voltage. By setting the reference capacitance to the lowest value, the relative change of the capacitance is higher compared to as it would be at a higher reference capacitance. This means that an added capacitance to a 4 pF sensor capacitor leads to a more significant change of its discharge curve, than it would by adding it to a sensor capacitance of 64 pF. In figure 3.8 this is shown graphically. For illustrative purposes a capacitance change of 1 pF, added to a 2 pF capacitor, is compared to the same change added to a 64 pF capacitor. It can be seen that due to the flatter slope of the curve, the capacitance change applied to the bigger capacitor leads to a required reference voltage change of about 59 mV. Whereas with the smaller capacitor a change of 627 mV is needed and thus a higher sensitivity is achieved.

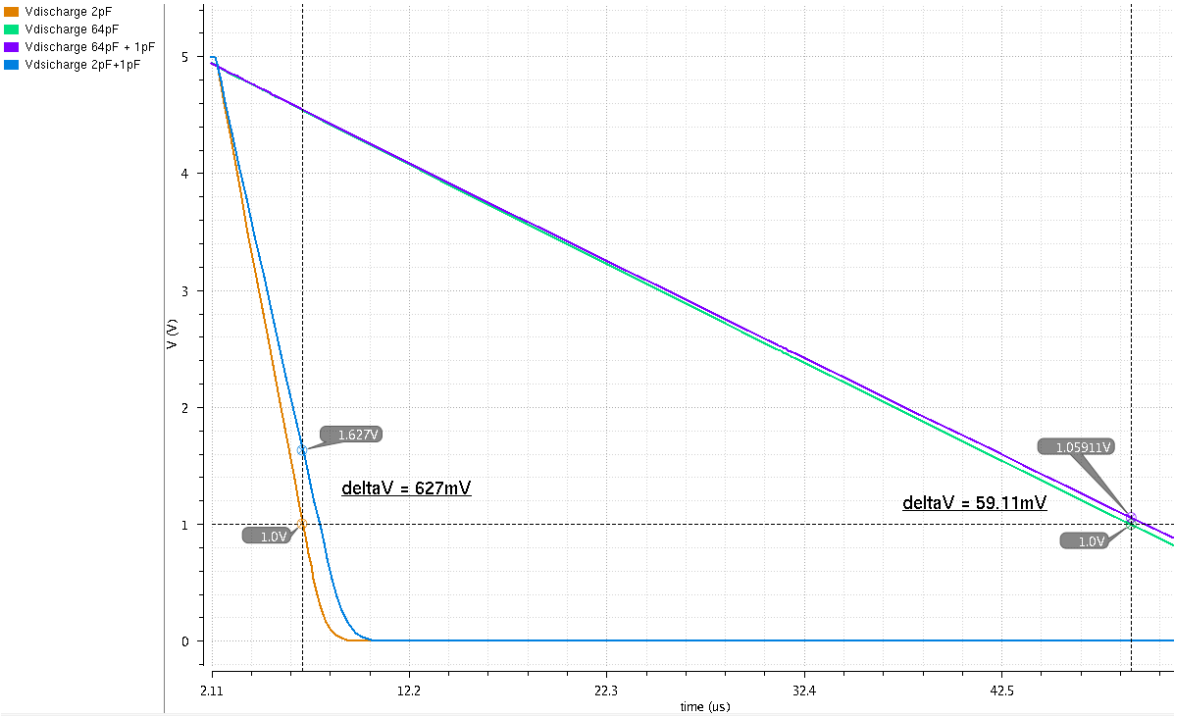

Figure 3.8: Sensitivity depending on reference capacitance

In table 3.9 the calculated number of achieved up pulses, depending on the settings of the

reference, sensor and charge pump capacitor, is shown. With the settings marked in red, the required 64 consecutive up pulses have not been achieved. With the yellow marked settings, 40 to 63 up pulses have been reached, while with the settings marked in green, all the necessary requirements have been met. It can be seen that with the smallest reference capacitance and the largest charge pump capacitance a change of 1 fF can theoretically be detected. In this table the approaching speed, and thus the fact whether or not the system will compensate for the change too fast, was not taken into account.

Ccp [pF]	Csens [pF]	Cref [pF]	Cappr [fF]	dt @dV(5V - vbg)	vref inital	vref approach [V]	delta vref [mV]	stepsize [uV]	approx. # steps
350	4,5	4	1	3,28	1,36	1,36	0,81	63,49	12
350	31	30	1	24,6	1,03	1,03	0,13	109,68	1
350	61	60	1	49,2	0,97	0,97	0,07	118,97	0
1400	3,5	4	1	3,28	0,31	0,32	1,34	53,06	25
1400	29	30	1	24,6	0,76	0,76	0,15	37,19	3
1400	59	60	1	49,2	0,83	0,83	0,07	34,62	2
2800	3,5	4	1	3,28	0,31	0,32	1,34	26,53	50
2800	4,1	4	1	3,28	1,000	1,001	0,975	14,286	68
2800	31	30	1	24,6	1,03	1,03	0,13	13,71	9
2800	61	60	1	49,2	0,97	0,97	0,07	14,87	4
350	3,5	4	20	3,28	0,31	0,34	26,62	212,24	125
350	31	30	20	24,6	1,03	1,03	2,56	109,68	23
350	61	60	20	49,2	0,97	0,97	1,32	118,97	11
1400	3,5	4	20	3,28	0,31	0,34	26,62	53,06	501
1400	31	30	20	24,6	1,03	1,03	2,56	27,42	93
1400	61	60	20	49,2	0,97	0,97	1,32	29,74	44
2800	3,5	4	20	3,28	0,31	0,34	26,62	26,53	1003
2800	29	30	20	24,6	0,76	0,76	2,92	18,60	157
2800	59	60	20	49,2	0,83	0,83	1,41	17,31	81

Figure 3.9: Sensitivity depending on capacitance settings

3.3 Behavioral Modeling

Analog transistor level simulations of large circuits or complete systems take a long time. Therefore, it is not possible to simulate each circuit detail from a systems perspective. A solution for getting a more robust design without sacrificing the time to market is to create behavioral models of the circuit blocks. Behavior models of transistor level circuits offer the possibility to check if circuit level specifications comply with system level specifications. With these models the behavior of the circuit can be simulated in a much shorter time while accuracy is reduced only non-significantly. To model analog behavior, a description language that is able to describe time-continuous analog signals is needed. For this purpose Verilog-AMS (analog mixed signal) is used. It combines the hardware description language Verilog-HDL for describing digital functionality and signals, and Verilog-A, which is used for analog behavior description. Analog voltages or currents are modeled with real valued variables, which are stored as double precision floating point numbers (64-bit sized). [4]

As mentioned earlier, this process was described in a separate thesis about system modeling with WREAL [10]. Some observations from these simulations were used to improve the

analog design. Since the modeling was partly done at the same time as the analog design, not all findings could be taken into account.

In figure 3.10 an example of an analog behavioral modeling simulation can be seen.

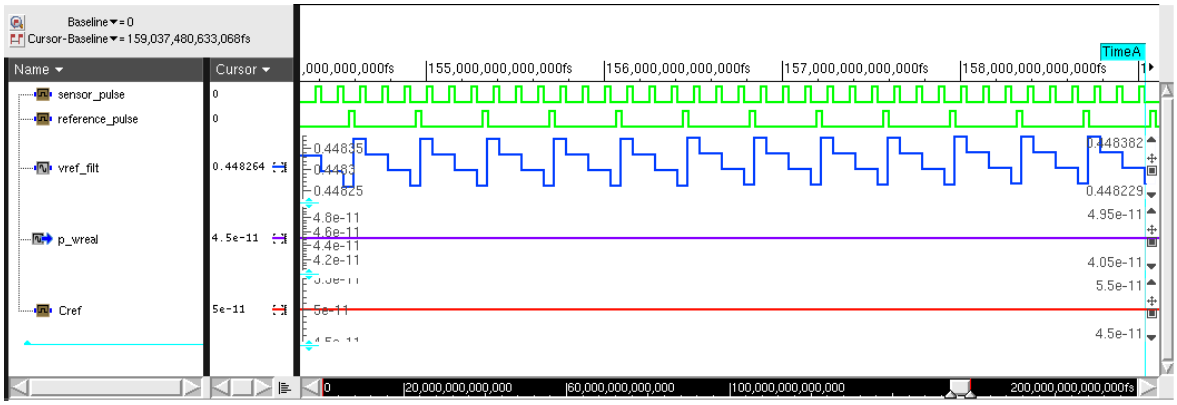

Figure 3.10: Behavioral modeling simulation: up and down pulses + reference voltage in equilibrium state ($C_{ref} = 50\,\text{pF}$, $C_{sens} = 45\,\text{pF}$) [10]

4 Analog Circuit Design and Verification

In this chapter the analog and physical design of all subblocks is described in more detail. Moreover, test bench setup and simulation results on the transistor level as well as on the extracted level are shown.

4.1 Sensor Interface

4.1.1 Description and Specification

Supply voltage	5 V
Input capacitance range	4 pF to 60 pF
Clock period	62 μs
Current consumption	<<

Table 4.1: Design specifications for the sensor interface

The internal reference capacitor was designed, according to specifications of the customer, to be adjustable in a range from 4 pF to 60 pF. In this way it is possible to connect an external sensor plate in the same capacitance range to the chip input. A step size of 2 pF was chosen because WREAL simulations [10] have shown it to be an optimal tradeoff between having as little control signals as possible on the one hand, and having an acceptable small difference (maximum difference of 1 pF) between C_S and C_{ref} on the other hand. The discharge current was derived from an existing bias block, which has already been used in other NXP products and is therefore tested. The requirement for the discharge current was that it is able to discharge 60 pF within 60 μs. This only has to be achieved with the highest trimming setting, to keep the current consumption as low as possible.

$$I = C \cdot \frac{dV}{dt} = 60pF \cdot \frac{5V}{60us} = 5\mu A \tag{4.1}$$

To generate the required current of 5 μA, the 1 μA output from the bias block was multiplied by five via a current mirror for both the reference and sensor capacitor. The biasing will be described in chapter 4.6 in more detail.

4.1.2 Circuit Design

The sensor interface consists of two switches, which are controlled by the clock signal and are closed approximately the first 2 μs of every clock cycle. In this period of time the sensor and the reference capacitor, which is controlled by 5 bits to switch it within the above mentioned range, are charged. C_{sensor} is the input pin with which the sensor plate will be connected. ESD (electrostatic discharge) resistors are placed at the sensor input to protect it from damage. A 200 Ω resistor is also placed between the reference switch and the $refcomp\_in$ pin, which will be connected to the reference comparator, although it is not an input which is bonded. This is done to have the same resistance between the switch and the comparator on both branches and thus avoid incorrect behavior due to mismatch.

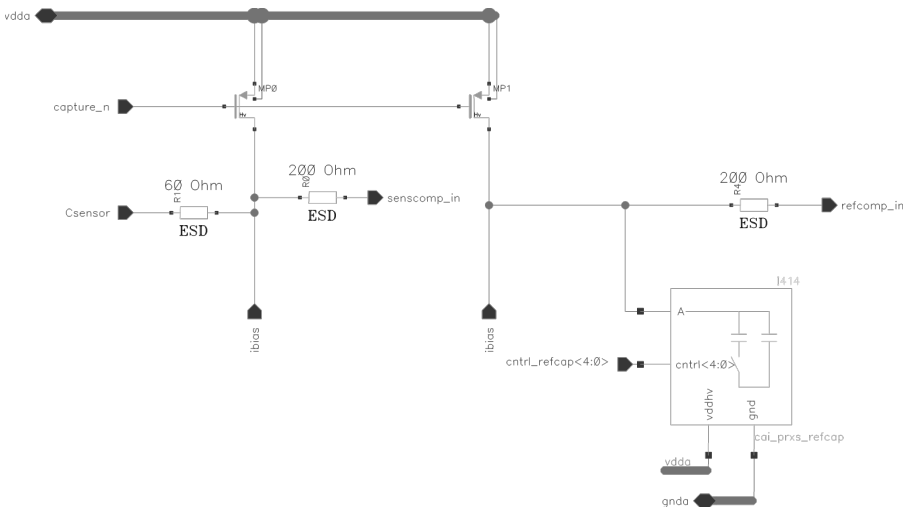

Figure 4.1: Schematic of the sensor interface

4.1.3 Test Bench and Simulation Results

For this part only a very simple test bench was built and is thus not shown here. To run the simulations on the sensor interface, the circuit was supplied by 5 V and a clock signal with a period time of 62 μs, while a pulse width of 2 μs was applied to the switches.

Figure 4.2 shows the transient simulation results of one clock cycle for the lowest (0) and the highest (7) possible trim setting. The blue, orange and green curves represent the charging and discharging of a 64 pF, a 32 pF and a 2 pF capacitor respectively.

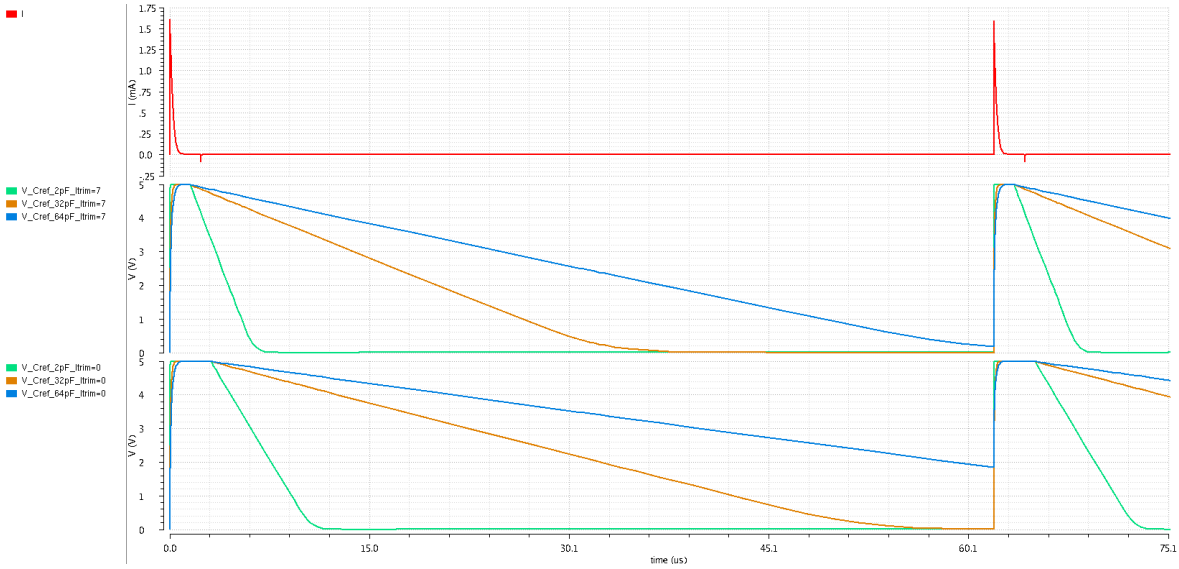

Figure 4.2: Charge and discharge curves of different reference capacitors with highest and lowest trim setting

In figure 4.3 a zoom into the first 2 μs of a clock cycle, where the switches are open, is shown. The charging voltages and currents of the same three reference capacitors as in figure 4.2 can be seen here.

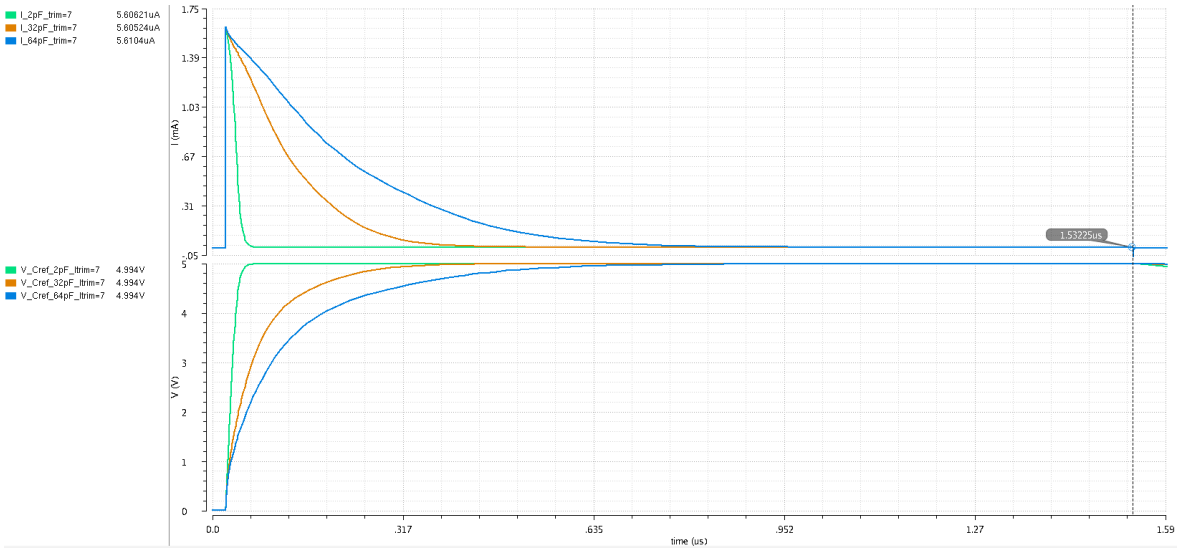

Figure 4.3: Charging voltages and currents of different reference capacitors with trim setting 7

Since there were no special requirements for the layout of the sensor interface, it is not shown here separately. It can be seen in figure 5.10 in chapter 5.4 as part of the analog front-end layout.

4.2 Comparator

4.2.1 Description and Specification

Supply voltage	5 V / 1.8 V
Phase Margin	$> 60\,^{\circ}$
Bandwidth	> 400 kHz
Idc_Vdd_5	$< 2.5\,\mu$A
Idc_Vdd_5 at power down	< 1 nA
Idc_Vdd_1v8	$< 2\ uA$
Idc_Vdd_1v8 at power down	< 1 nA
Offset voltage	-2 mV to 2 mV
Slew rate	$> 900\,\text{V}/\mu\text{s}$

Table 4.2: Design specifications for the comparator

The comparator is supplied by two different voltages, the input stage is supplied with 5 V and the output stage is supplied with 1.8 V. This was done to shift the voltage level from the required 5 V input to a lower voltage in an early phase of the circuit. Consequently, the low power digital logic and the charge pump can also run on 1.8 V to lower the overall current consumption.

The input voltage of 5 V was chosen because on the one hand it was a requirement, since 5 V are always present in a car system, on the other hand it is needed to achieve the required sensitivity. The change of the slope of the capacitor discharge curve, caused by a small capacitance change, is very slight, a sufficiently large change in the slope occurs only at a higher voltage. In figure 4.4 a comparison of the change of the discharge slope of two capacitors is shown. It can be seen that the voltage difference after discharging from 5 V to 3 V is only 216 mV, whereas it is 445 mV when discharging from 5 V to 900 mV ($\approx$ vref). A relatively big capacitance change of 5 pF, as it was chosen here for illustrative purposes, could also be detected with a supply voltage of 2 V. However, it is clearly visible that a detection of the required small capacitance change in the range of several femtofarad would hardly be possible with a smaller supply voltage. With an even higher input voltage the sensitivity could be increased further, but only at the cost of power consumption.

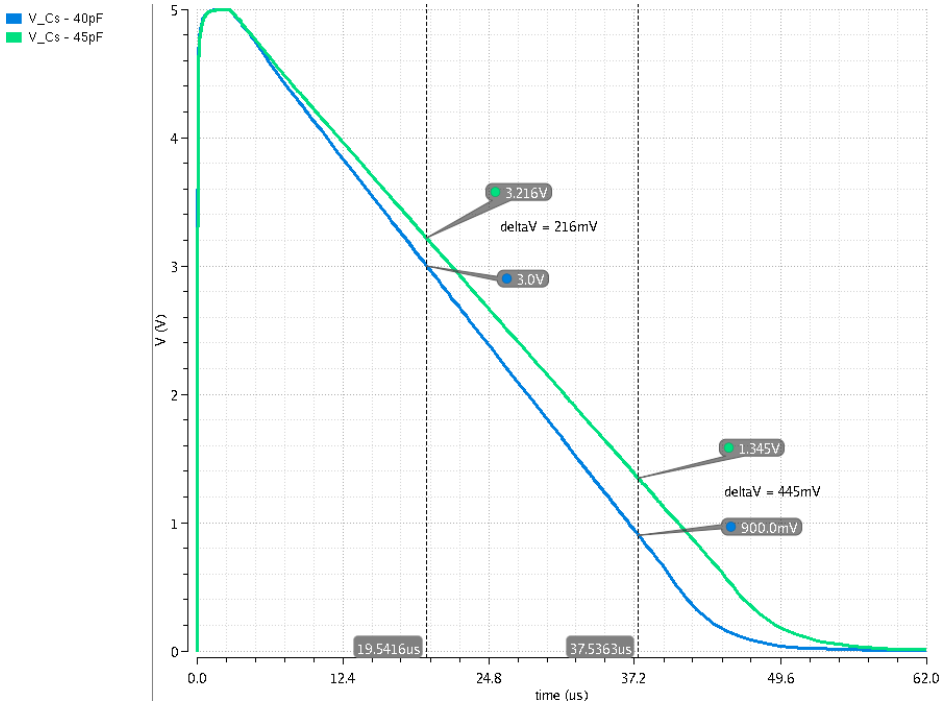

Figure 4.4: Discharge slope difference between two capacitors (40 pF, 45 pF) at 3 V and 900 mV

4.2.2 Circuit Design

In the system level simulations it could be seen that if the system is in equilibrium, the sensor comparator and the reference comparator switch their output at almost the same time. This means that the difference between both signals is so small that it is not possible to create an up or down pulse via the logic gates. Consequently, there would be no pulses at the output if the equilibrium state is reached. Therefore, an adjustable delay was built into the comparators. The signal to enable and disable the delay was derived from the clock input signal and divided by two via a D-FF (D-Flip-Flop). The configuration of the D-FF and the output signals can be seen in figure 4.5. The signal derived from the clock was applied to the reference comparator and the inverted signal was applied to the sensor capacitor. This measure ensures that in each clock cycle only one of the comparators is delayed and hence guarantees that there is always an up or down pulse at the output.

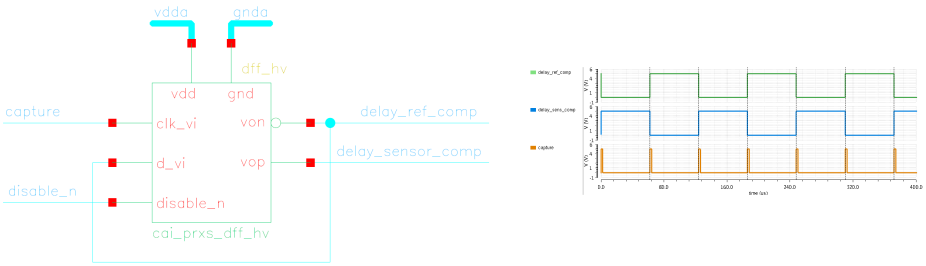

Figure 4.5: D-FlipFlop configuration to divide clock period time by two + transient simulation results

To ensure the stability of the comparator design the phase margin has to be observed. The following equation shows the calculation of the phase margin. A general graphical explanation of the phase and gain margin is shown in figure 4.6.

The PM is determined at the point of unity gain. The phase at this point has to be above $-180\,^\circ$ to ensure a stable, non oscillating system. The difference between $-180\,^\circ$ and the phase at the unity gain point is called phase margin. The value of the PM determines the stability and the speed of the system. A higher phase margin results in a more stable, but slower time response. At a phase margin of $60\,^\circ$ the step response shows very little ringing but still is reasonably fast. Higher values lead to better stability but slower response, thus, a phase margin of $60\,^\circ$ is considered the best trade off between these two requirements. [6, 5, 7]

Phase Margin [6]:

$$\Phi_M = 180 - tangent^{-1}(A\beta) \tag{4.2}$$

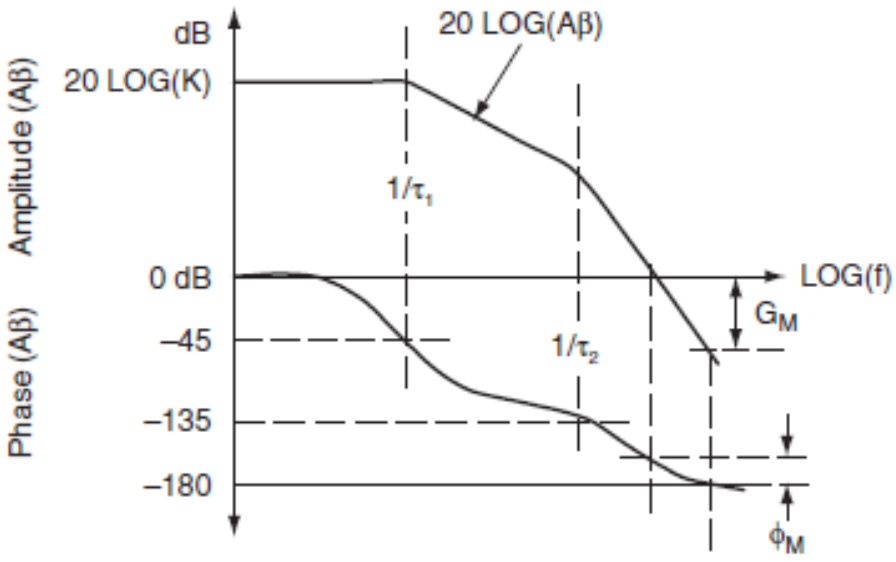

Figure 4.6: Amplitude and phase plot to determine phase and gain margin [6]

How the amplitude and the phase are calculated is described in the following equations:

Transfer function:

$$\underline{H}(j\omega) = \frac{|A_0|}{1 + \frac{j\cdot\omega}{\omega_0}} \tag{4.3}$$

Amplitude:

$$|\underline{H}(j\omega)| = \frac{|A_0|}{\sqrt{1 + (\frac{\omega}{\omega_0})^2}} \tag{4.4}$$

Phase:

$$\Phi(\omega) = -\tan^{-1}\frac{\omega}{\omega_0} \tag{4.5}$$

The schematic of the comparator, including the delay circuit, is shown in figure 4.7.

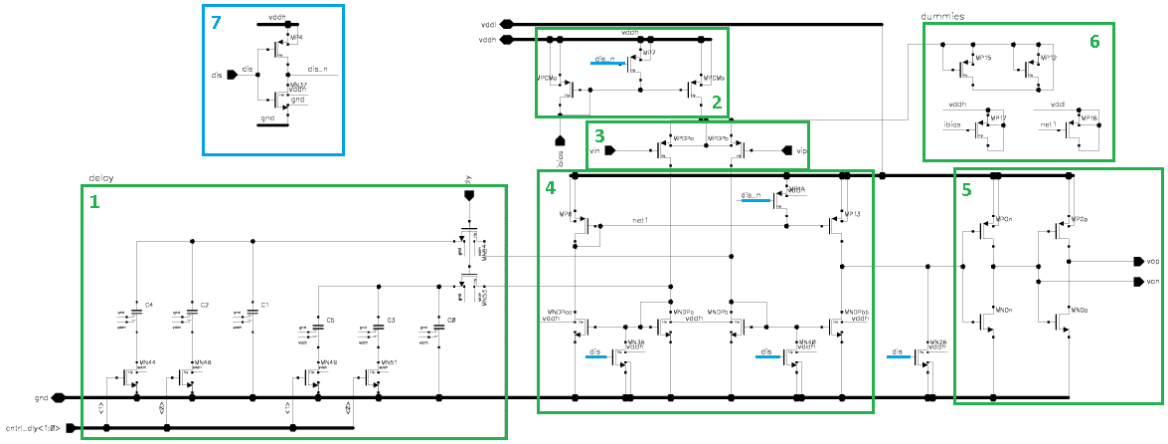

Figure 4.7: Comparator schematic:
1 Delay circuit
2 Bias part
3 Input differential pair
4 Active part
5 Output inverters
6 Dummy transistors
7 Disable signal and pull down/up transistors

4.2.3 Test Bench and Simulation Results

The test bench, which was used for the verification of the comparator, can be seen in figure 4.8. The bias block (see section 4.6), which will be used in the system, is integrated in the test bench, taking the real biasing conditions into account.

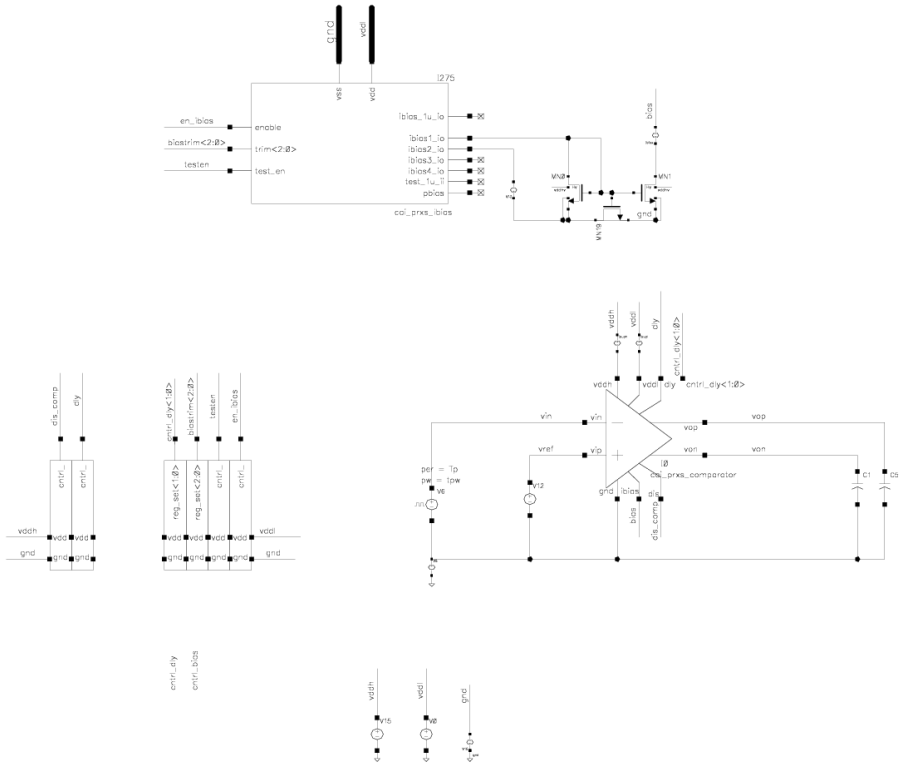

Figure 4.8: Comparator test bench

Figure 4.9 shows how the values for the phase margin (PM) and the bandwidth (BW) are determined in the simulations.

The BW is the frequency at which the gain is 3 dB lower than the original gain. At a higher frequency the gain decreases, which would cause signal distortions when the circuit is operated in this region. [6, 5, 7]

It is very important to simulate the phase margin at all process corners and for the complete required temperature range to ensure that the circuit is stable under all conditions.

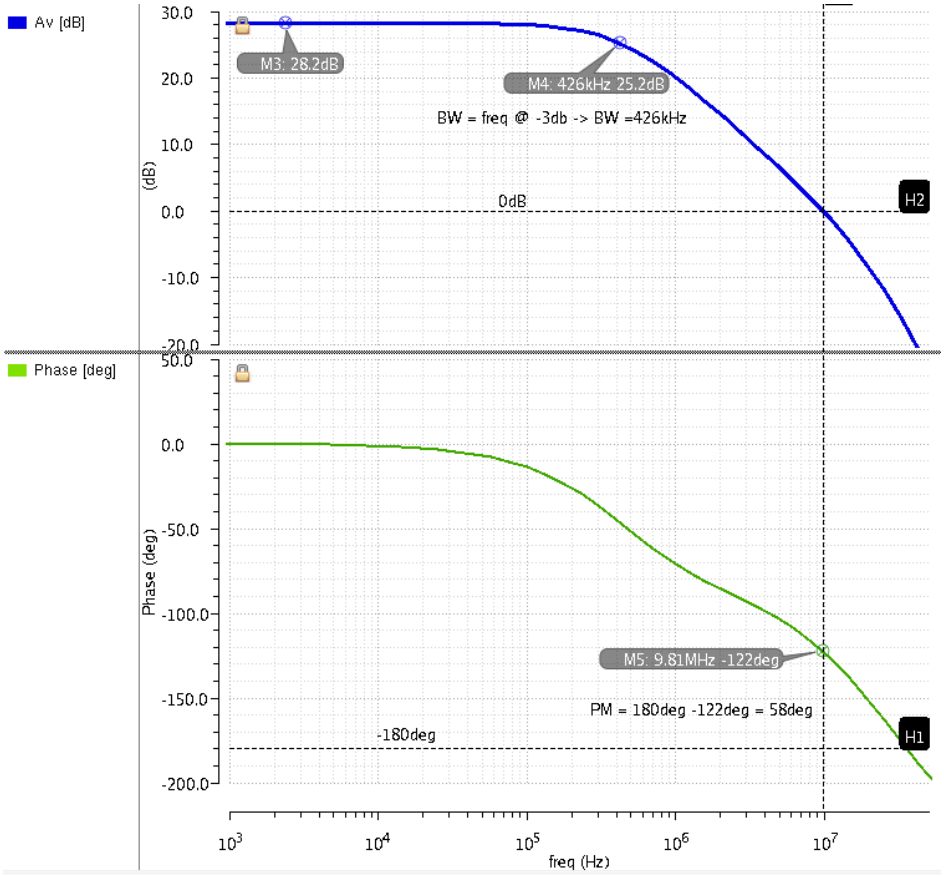

Figure 4.9: Amplitude and phase characteristic of the comparator

In figure 4.10 it is shown how the comparator delay and the rise time are determined in the simulation. The delay time is the period of time from when the comparator input crosses the reference voltage to when the output switches (the output signal reaches half the supply voltage).
The rise time is the time frame that the output signal needs to reach 90% of its end value, starting from 10%.

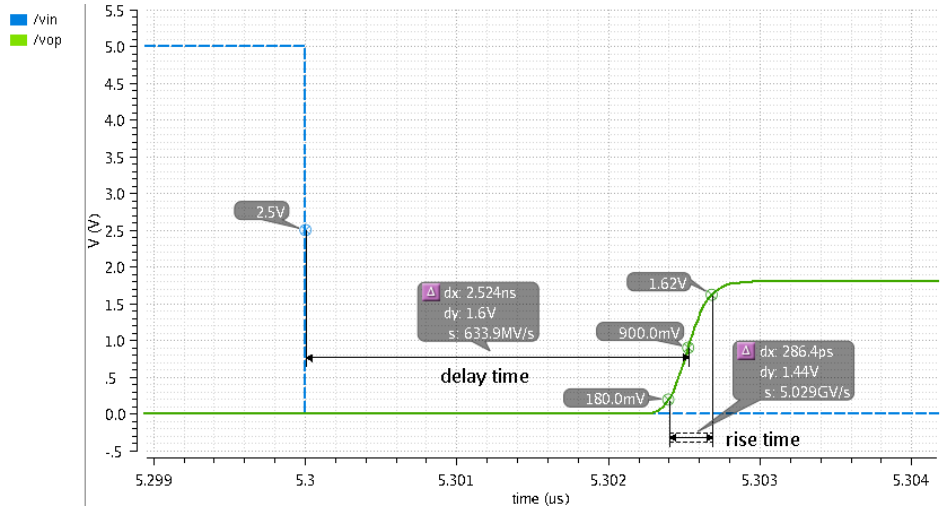

Figure 4.10: Rise time and delay time of comparator

In figure 4.11 the schematic simulation results over process and temperature corners are shown.
Values marked in green are the ones that have met specifications, values marked in yellow have come close to the defined requirements, whereas the values marked in red are outside the specified range. The fact that the bandwidth was lower than targeted in the slow corner was considered still acceptable for the proper functioning of the system.

Corner	temperature	topinclude.scs	Pass/Fail	PM	bw	voff	I_Vdd5v5	I_Vdd1v8	I_Vdd5v5_pd	I_Vdd1v8_pd	slewRate	riseTime	fallTime	tdel
nom	27	nominal	pass	75.54 deg	424.7 kHz	1.5 mV	2.053 uA	1.577 uA	294.9 pA	46.71 pA	5.093 GV/s	282.7 ps	754.2 ps	4.765 ns
PVT_1_0	-40	fast	near	74.15 deg	569.6 kHz	509.3 uV	2.693 uA	2.053 uA	288.2 pA	17.88 pA	6.587 GV/s	218.6 ps	589.8 ps	4.027 ns
PVT_1_1	27	fast	near	74.12 deg	604.3 kHz	1.5 mV	2.72 uA	2.079 uA	299.2 pA	175.6 pA	5.756 GV/s	250.2 ps	677.3 ps	4.72 ns
PVT_1_2	85	fast	near	75.79 deg	612.9 kHz	1.5 mV	2.542 uA	1.966 uA	527.8 pA	3.069 nA	5.007 GV/s	287.6 ps	817.6 ps	5.489 ns
PVT_1_3	-40	fnfp	pass	79.17 deg	454.6 kHz	559.9 uV	2.05 uA	1.615 uA	288.2 pA	17.88 pA	6.566 GV/s	219.3 ps	711 ps	4.106 ns
PVT_1_4	27	fnfp	pass	79.53 deg	481.9 kHz	1.5 mV	2.071 uA	1.637 uA	299.2 pA	175.6 pA	5.718 GV/s	251.8 ps	814.9 ps	4.821 ns
PVT_1_5	85	fnfp	near	81.66 deg	490.6 kHz	1.5 mV	1.937 uA	1.558 uA	527.7 pA	3.069 nA	4.988 GV/s	288.7 ps	985.7 ps	5.617 ns
PVT_1_6	-40	fnsp	near	76.52 deg	397 kHz	500 uV	2.033 uA	1.544 uA	288.2 pA	17.64 pA	5.503 GV/s	261.7 ps	685.1 ps	3.886 ns
PVT_1_7	27	fnsp	pass	75.88 deg	409.1 kHz	1.5 mV	2.055 uA	1.571 uA	297 pA	125.8 pA	4.916 GV/s	292.9 ps	801.9 ps	4.534 ns
PVT_1_8	85	fnsp	pass	77.24 deg	402.2 kHz	1.5 mV	1.922 uA	1.489 uA	432.4 pA	2.079 nA	4.443 GV/s	324.1 ps	977.6 ps	5.192 ns
PVT_1_9	-40	nominal	pass	76.01 deg	407.9 kHz	500 uV	2.032 uA	1.551 uA	286.2 pA	17.1 pA	5.732 GV/s	251.2 ps	650 ps	4.063 ns
PVT_1_10	27	nominal	pass	75.54 deg	424.7 kHz	1.5 mV	2.053 uA	1.577 uA	294.9 pA	46.71 pA	5.093 GV/s	282.7 ps	754.2 ps	4.765 ns
PVT_1_11	85	nominal	pass	77.12 deg	422.4 kHz	1.5 mV	1.918 uA	1.493 uA	354.1 pA	791.8 pA	4.513 GV/s	319.1 ps	914.9 ps	5.514 ns
PVT_1_12	-40	slow	fail	75.63 deg	310 kHz	500 uV	1.627 uA	1.23 uA	284.3 pA	17.01 pA	4.882 GV/s	295 ps	715.8 ps	4.175 ns
PVT_1_13	27	slow	fail	74.98 deg	317 kHz	500 uV	1.645 uA	1.254 uA	292.5 pA	23.43 pA	4.379 GV/s	328.9 ps	834.3 ps	4.897 ns
PVT_1_14	85	slow	fail	76.49 deg	309.7 kHz	1.5 mV	1.537 uA	1.187 uA	314.7 pA	235.5 pA	3.938 GV/s	365.7 ps	1.004 ns	5.651 ns
PVT_1_15	-40	snfp	pass	75.68 deg	423.3 kHz	500 uV	2.031 uA	1.542 uA	284.4 pA	17.15 pA	5.941 GV/s	242.4 ps	631.2 ps	4.329 ns
PVT_1_16	27	snfp	pass	75.42 deg	446.1 kHz	1.5 mV	2.052 uA	1.566 uA	293.9 pA	56.85 pA	5.144 GV/s	279.9 ps	720 ps	5.151 ns
PVT_1_17	85	snfp	pass	77.2 deg	449.9 kHz	1.5 mV	1.916 uA	1.48 uA	375.3 pA	963.8 pA	4.414 GV/s	326.2 ps	866.8 ps	6.105 ns
PVT_1_18	-40	snsp	near	71.18 deg	370.5 kHz	500 uV	2.014 uA	1.505 uA	284.3 pA	17.01 pA	4.905 GV/s	293.6 ps	631.8 ps	4.136 ns
PVT_1_19	27	snsp	near	69.97 deg	378.5 kHz	500 uV	2.037 uA	1.531 uA	292.5 pA	23.43 pA	4.396 GV/s	327.6 ps	738.1 ps	4.85 ns
PVT_1_20	85	snsp	near	71.35 deg	370.2 kHz	1.5 mV	1.902 uA	1.444 uA	314.7 pA	235.5 pA	3.946 GV/s	364.9 ps	886.2 ps	5.594 ns

Figure 4.11: Comparator simulation results

Due to variations in the manufacturing process, transistors do not always behave as expected in nominal simulation. To cover all possible speed differences and thus ensure proper functionality, a simulation over all process corners (fast NMOS/fast PMOS, fast NMOS/slow PMOS, slow NMOS/slow PMOS, slow NMOS/fast PMOS) has to be performed. Figure 4.12 shows the variation of the transistor threshold voltage in the aforementioned process corners.

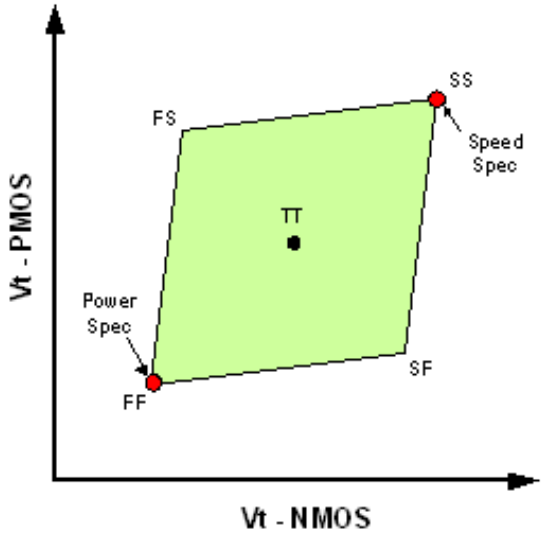

Figure 4.12: V_t variation of PMOS and NMOS over process corners [21]

Figure 4.13 shows the Monte Carlo simulation results of the comparator offset voltage.

Test	Name	Yield	Min	Target	Max	Mean	Sigma
Yield Estimate: 100 %(100 passed/100 pts)		Confidence Level: <not set>		Error Filter: <not set>			
DC_voff							
	voff(summary)	100	-17.5m		20.5m	1.791m	8.183m
	voff	100	-16.43m	info	19.5m	1.618m	7.63m
	voff_PVT_1_0	100	-15.5m	info	18.5m	1.461m	7.387m
	voff_PVT_1_1	100	-15.5m	info	19.5m	1.859m	7.498m
	voff_PVT_1_10	100	-16.5m	info	19.5m	1.95m	7.818m
	voff_PVT_1_11	100	-16.5m	info	20.5m	2.189m	7.906m
	voff_PVT_1_12	100	-15.5m	info	18.5m	1.29m	7.52m
	voff_PVT_1_13	100	-16.43m	info	19.5m	1.618m	7.63m
	voff_PVT_1_14	100	-16.5m	info	19.52m	1.969m	7.856m
	voff_PVT_1_15	100	-16.5m	info	20.5m	2.253m	8.038m
	voff_PVT_1_16	100	-16.5m	info	18.5m	1.16m	7.609m
	voff_PVT_1_17	100	-16.5m	info	19.5m	1.449m	7.734m
	voff_PVT_1_18	100	-16.5m	info	19.5m	1.801m	7.938m
	voff_PVT_1_19	100	-17.5m	info	20.5m	2.019m	8.183m
	voff_PVT_1_2	100	-15.5m	info	19.51m	2.21m	7.659m
	voff_PVT_1_20	100	-16.5m	info	19.5m	1.27m	7.63m
	voff_PVT_1_21	100	-16.5m	info	19.5m	1.626m	7.683m
	voff_PVT_1_22	100	-16.5m	info	20.5m	1.99m	7.91m
	voff_PVT_1_23	100	-16.5m	info	20.5m	2.319m	8.104m
	voff_PVT_1_24	100	-16.5m	info	18.5m	1.15m	7.555m
	voff_PVT_1_25	100	-16.5m	info	18.5m	1.351m	7.592m
	voff_PVT_1_26	100	-16.5m	info	19.5m	1.721m	7.747m
	voff_PVT_1_27	100	-16.5m	info	19.5m	1.97m	7.891m
	voff_PVT_1_3	100	-15.5m	info	20.5m	2.442m	7.726m
	voff_PVT_1_4	100	-15.5m	info	19.5m	1.473m	7.547m
	voff_PVT_1_5	100	-15.5m	info	19.5m	1.9m	7.662m
	voff_PVT_1_6	100	-16.5m	info	20.5m	2.251m	7.94m
	voff_PVT_1_7	100	-16.5m	info	20.5m	2.615m	8.061m
	voff_PVT_1_8	100	-15.5m	info	18.5m	1.347m	7.486m
	voff_PVT_1_9	100	-15.5m	info	19.5m	1.667m	7.53m

Figure 4.13: Monte Carlo simulation results of offset voltage simulation

4.2.4 Physical Design

The physical design of the comparator is shown in figure 4.14. The different stages of the comparator are marked in the picture. It is approximately 67 μm $\times$ 31 μm large.

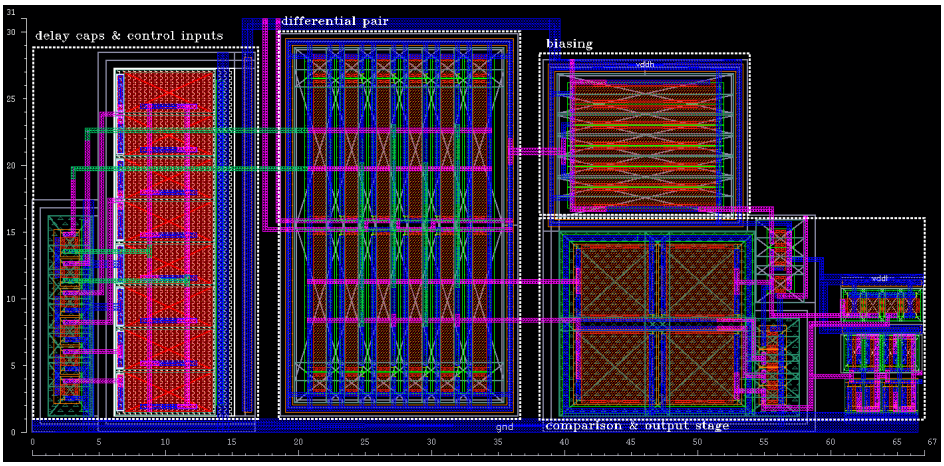

Figure 4.14: Comparator layout

To prevent over- and under-etching effects, temperature or process gradients from influencing the functionality of the circuits, certain rules have to be applied during the physical design process. Devices that should behave in the same exact way have to be matched. That means they have to be placed close to each other, be aligned in the same direction and they have to have the same surrounding elements. If two devices, for example in a differential pair, have to be matched, special placement techniques such as common-centroid or cross-quad should be used to reduce the process influences as much as possible. To avoid over- and under-etching effects on devices that are placed on an edge of a block, so-called dummy devices are inserted to make sure that the active devices all see the same structures around them. [9] Figure 4.15 shows some examples for common matching practices.

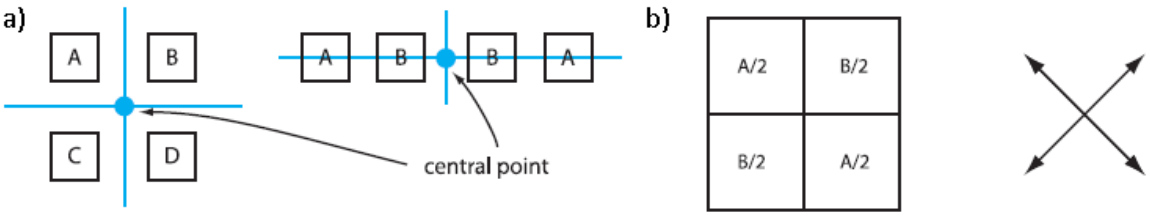

Figure 4.15: Examples of common centroid (a) and cross-quading (b) techniques [9]

After the physical design is completed, it has to be verified if the block is still working according to the specifications. To accomplish this task, a parasitic extraction of the layout is done by generating a new netlist that includes the original devices and on top of that the parasitic resistances of the connection lines as well as the parasitic capacitances, which occur

due to coupling between devices and wire connections. With this newly created netlist, the same simulations can be re-run to compare the results with the ones from the schematic simulation. If necessary, improvements can be made in the physical design to achieve the required results. Figure 4.16 shows a part of the schematic netlist of the comparator. In figure 4.17 parts of the extracted netlist, including the parasitic devices mentioned above, are shown.
o

```
// Library name: cai_prxs_ana_fe_lib
// Cell name: cai_prxs_comparator
// View name: schematic
// Inherited view list: physConfig schematic symbol
MN26 (gnd vddh net0130 dis gnd) nmosHV
MNDPbb (gnd vddh net0130 net088 gnd) nmosHV
MN40 (gnd vddh net088 dis gnd) nmosHV
MN48 (gnd vddh net090 cntrl_dly\<0\> gnd) nmosHV
MNDPb (gnd vddh net088 net088 gnd) nmosHV
MNDPa (gnd vddh net037 net037 gnd) nmosHV
MN38 (gnd vddh net037 dis gnd) nmosHV
MNDPaa (gnd vddh net1 net037 gnd) nmosHV
MN37 (gnd vddh dis_n dis gnd) nmosHV
MN44 (gnd vddh net70 cntrl_dly\<1\> gnd) nmosHV
MN49 (gnd vddh net101 cntrl_dly\<1\> gnd) nmosHV
MN53 (gnd vddh net037 dly net038) nmosHV
MN54 (gnd vddh net088 dly net070) nmosHV
MN51 (gnd vddh net089 cntrl_dly\<0\> gnd) nmosHV
C5 (vddh net038 gnd net101) capPsfCg
C4 (vddh net070 gnd net70) capPsfCg
C2 (vddh net070 gnd net090) capPsfCg
C0 (vddh net038 gnd gnd) capPsfCg
C1 (vddh net070 gnd gnd) capPsfCg
C3 (vddh net038 gnd net089) capPsfCg
```

Figure 4.16: Part of the comparator schematic netlist

```
// Library name: cai_prxs_ana_fe_lib
// Cell name: cai_prxs_comparator
// View name: RCext
MN0n (\27\:von \93\:net0130 \1094\:gnd \1083\:gnd) nm4yn wnom=1.5 lnom=0.2 \
        sa=0.42 sb=0.42 sca=0.699189 scb=2.79709e-06 scc=7.05674e-11
MN0n_1__rcx (\50\:von \129\:net0130 \1107\:gnd \1083\:gnd) nm4yn wnom=1.5 \
        lnom=0.2 sa=0.42 sb=0.42 sca=0.666431 scb=2.79709e-06 \
        scc=7.05674e-11
MN0p (\27\:vop \109\:von \1132\:gnd \1083\:gnd) nm4yn wnom=1.5 lnom=0.2 \
        sa=0.42 sb=0.42 sca=0.747019 scb=2.79715e-06 scc=7.05674e-11
MN0p_1__rcx (\50\:vop \133\:von \1165\:gnd \1083\:gnd) nm4yn wnom=1.5 \
        lnom=0.2 sa=0.42 sb=0.42 sca=1.41205 scb=2.73171e-05 \
        scc=5.91395e-10
MP16 (\51\:vddl \104\:net1 \49\:vddl \16\:vddl) nm4yp wnom=1 lnom=1 \
        sa=0.42 sb=0.42 sca=1.65554 scb=0.000404251 scc=1.2485e-06
MP0n_1__rcx (\22\:von \91\:net0130 \32\:vddl \18\:vddl) nm4yp wnom=2 \
        lnom=0.2 sa=0.42 sb=0.42 sca=1.84151 scb=0.000217193 \
        scc=6.11134e-07
 ...
Cpara13 (\28\:dly \1446\:gnd) capacitor c=1.27624e-17
Cpara14 (\4\:dly \1446\:gnd) capacitor c=1.0774e-17
Cpara15 (\3\:dly \1446\:gnd) capacitor c=5.47423e-18
Cpara16 (\20\:dly \1455\:gnd) capacitor c=3.12071e-18
Cpara17 (dly \1455\:gnd) capacitor c=1.91936e-17
Cpara18 (\2\:dly \1455\:gnd) capacitor c=1.34815e-17
 ...
RRpoly205 (\18\:ibias \246\:ibias) resistor r=4.5947 c=0
RRpoly203 (\267\:ibias \270\:ibias) resistor r=0.3352 c=0
RRpoly201 (\215\:ibias \214\:ibias) resistor r=0.3564 c=0
RRpoly199 (\292\:ibias \294\:ibias) resistor r=19.6 c=0
RRpoly197 (\239\:ibias \229\:ibias) resistor r=5.4 c=0
RRpoly194 (\252\:ibias \43\:ibias) resistor r=29.1283 c=0
 ...
```

Figure 4.17: Parts of the extracted netlist of the comparator

Figure 4.18 shows the simulation results of the extracted netlist. As can be seen in the picture, the results in some corners are slightly inferior to those of the schematic simulation. However, after a thorough review it was decided that the results are satisfactory for the application.

Corner	temperature	topinclude.scs	Pass/Fail	PM	bw	voff	I_Vdd5v5	I_Vdd1v8	I_Vdd5v5_pd	I_Vdd1v8_pd	slewRate	riseTime	fallTime	tdel
nom	27	nominal	near	68.53 deg	388 kHz	1.5 mV	2.053 uA	1.606 uA	234.5 pA	46.87 pA	4.098 GV/s	351.4 ps	945.2 ps	7.285 ns
PVT_1_0	-40	fast	near	67.82 deg	520.4 kHz	531.6 uV	2.693 uA	2.067 uA	227.2 pA	17.85 pA	5.387 GV/s	267.3 ps	759.2 ps	5.873 ns
PVT_1_1	27	fast	near	67.08 deg	551.1 kHz	1.5 mV	2.72 uA	2.1 uA	238.6 pA	177.6 pA	4.446 GV/s	323.9 ps	863.3 ps	7.265 ns
PVT_1_2	85	fast	fail	68.29 deg	555.2 kHz	1.5 mV	2.542 uA	1.993 uA	469.5 pA	3.095 nA	3.728 GV/s	386.3 ps	1.034 ns	8.723 ns
PVT_1_3	-40	fnfp	pass	73.07 deg	415.7 kHz	1.455 mV	2.05 uA	1.635 uA	227.2 pA	17.85 pA	5.31 GV/s	271.2 ps	910.9 ps	6.052 ns
PVT_1_4	27	fnfp	near	73.09 deg	439.7 kHz	1.5 mV	2.071 uA	1.665 uA	238.6 pA	177.6 pA	4.367 GV/s	329.8 ps	1.037 ns	7.506 ns
PVT_1_5	85	fnfp	fail	74.73 deg	444.2 kHz	1.5 mV	1.937 uA	1.595 uA	469.4 pA	3.095 nA	3.636 GV/s	396.1 ps	1.249 ns	9.014 ns
PVT_1_6	-40	fnsp	near	70.32 deg	364.8 kHz	500.1 uV	2.033 uA	1.592 uA	227 pA	17.63 pA	4.861 GV/s	296.2 ps	853.9 ps	5.697 ns
PVT_1_7	27	fnsp	near	69.3 deg	373.9 kHz	1.5 mV	2.055 uA	1.624 uA	236 pA	128.9 pA	4.14 GV/s	347.9 ps	989.6 ps	6.916 ns
PVT_1_8	85	fnsp	fail	70.11 deg	366.3 kHz	1.5 mV	1.922 uA	1.549 uA	336.8 pA	2.127 nA	3.574 GV/s	403 ps	1.188 ns	8.205 ns
PVT_1_9	-40	nominal	near	69.66 deg	375.2 kHz	500.1 uV	2.032 uA	1.579 uA	225.1 pA	17.06 pA	4.907 GV/s	293.4 ps	824.5 ps	5.886 ns
PVT_1_10	27	nominal	near	68.53 deg	388 kHz	1.5 mV	2.053 uA	1.606 uA	234.3 pA	46.87 pA	4.098 GV/s	351.4 ps	945.2 ps	7.285 ns
PVT_1_11	85	nominal	fail	69.65 deg	383.9 kHz	1.5 mV	1.918 uA	1.527 uA	294.4 pA	795.3 pA	3.511 GV/s	410.2 ps	1.13 ns	8.739 ns
PVT_1_12	-40	slow	fail	68.96 deg	286.1 kHz	500 uV	1.626 uA	1.257 uA	223.1 pA	16.98 pA	4.344 GV/s	331.5 ps	887.3 ps	5.956 ns
PVT_1_13	27	slow	fail	67.74 deg	291.3 kHz	500.1 uV	1.645 uA	1.285 uA	231.9 pA	23.4 pA	3.707 GV/s	388.4 ps	1.019 ns	7.327 ns
PVT_1_14	85	slow	fail	69.09 deg	284 kHz	1.5 mV	1.537 uA	1.223 uA	254.5 pA	235.8 pA	3.209 GV/s	448.7 ps	1.218 ns	8.774 ns
PVT_1_15	-40	snfp	near	69.2 deg	389.4 kHz	500 uV	2.031 uA	1.553 uA	223 pA	17.09 pA	4.859 GV/s	296.4 ps	804.4 ps	6.157 ns
PVT_1_16	27	snfp	fail	68.04 deg	408.5 kHz	1.5 mV	2.052 uA	1.581 uA	233.2 pA	56.21 pA	4 GV/s	360 ps	924.4 ps	7.754 ns
PVT_1_17	85	snfp	fail	69.56 deg	409.2 kHz	1.5 mV	1.916 uA	1.499 uA	306.5 pA	948.6 pA	3.376 GV/s	426.6 ps	1.097 ns	9.406 ns
PVT_1_18	-40	snsp	fail	63.69 deg	342 kHz	500 uV	2.014 uA	1.527 uA	223 pA	16.97 pA	4.359 GV/s	330.4 ps	785.9 ps	5.874 ns
PVT_1_19	27	snsp	fail	62.25 deg	349 kHz	500 uV	2.037 uA	1.554 uA	231.9 pA	23.4 pA	3.739 GV/s	385.1 ps	901.6 ps	7.202 ns
PVT_1_20	85	snsp	fail	63.37 deg	339.7 kHz	1.5 mV	1.902 uA	1.471 uA	254.4 pA	235.8 pA	3.237 GV/s	444.9 ps	1.064 ns	8.62 ns

Figure 4.18: Comparator extracted simulation results

4.3 Voltage Follower

4.3.1 Description and Specification

Supply voltage	5 V
Phase Margin	$> 45\,^{\circ}$
Bandwidth	$> 400\,\mathrm{kHz}$
DC current consumption	$< 10\,\mu\mathrm{A}$
Idc power down	$< 10\,\mathrm{nA}$
Offset voltage	$< 3\,\mathrm{mV}$
Slew rate	$< -0.2\,\frac{V}{\mu s}$
Rise time	$< 700\,\mathrm{ns}$
Fall time	$< 20\,\mu\mathrm{s}$

Table 4.3: Design specifications for voltage follower block

An operational amplifier, configured as a voltage follower, was designed to connect the sensor input also to the cable shield, creating a so-called driven shield. It should be able to drive a long cable, as discussed in chapter 3. In the system application the sensor plate will be connected via a coaxial cable to the chip input. If the cable shield would be connected to ground, the capacitance of the sensor input would depend on the cable length. A long cable would also lead to a sensitivity degradation because the higher capacitance causes the system to become less sensitive to capacitance changes. Therefore, the sensor input signal is connected to the cable shield via the voltage follower. In the proposed configuration there is almost no capacitance between the sensor input and the cable shield. Consequently, the influence of the cable length is canceled out up to the length that the follower is able to drive.

The voltage follower configuration is equally important to ensure a proper ESD protection of the input pins. The input pins can not be protected by a standard ESD protection circuit because this would have a high influence on the sensitivity and input behavior. This concept is therefore necessary to be able to protect the input with anti-parallel diodes between the sensor input (Cs) and shield (Sh) pin.

4.3.2 Circuit Design

The requirement of the voltage follower is to follow the sensor input signal, which has a steep rising edge and a flatter falling edge (discharge curve of the sensor capacitor). The supply voltage was set to 5 V, the input signal range is 0 V to 5 V. To follow the steep rising edge of the sensor input signal when the switch is closed and the capacitor is charged, a ”negative” reset is build in. The reset signal, which is the clock signal with the short pulse

width, sets the follower output to 5 V when the clock is high. The strict requirements for low power consumption make it difficult to achieve a short rise time and a very high slew rate without the reset signal respectively. The steepness of the slope of the output signal is limited by the slew rate ($SR = \frac{\Delta V_{OUT}}{\Delta t}$) [7]. To determine the required slew rate, the time span which is needed to discharge the sensor capacitor from 5 V to 0 V has to be calculated. From this value the minimum required slew rate is determined.

$$dt = C \cdot \frac{\Delta V}{I} = 20\,pF \cdot \frac{5\,V}{4\,\mu A} = 25\mu s \tag{4.6}$$

$$SR = \frac{5\,V}{5\,\mu s} = 0.2V/\mu s \tag{4.7}$$

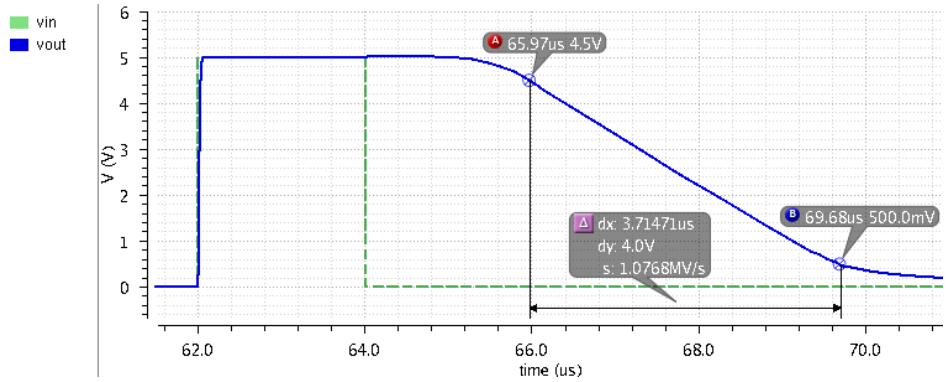

Figure 4.19: Maximum slew rate of voltage follower

The schematic of the voltage follower is shown in figure 4.20.

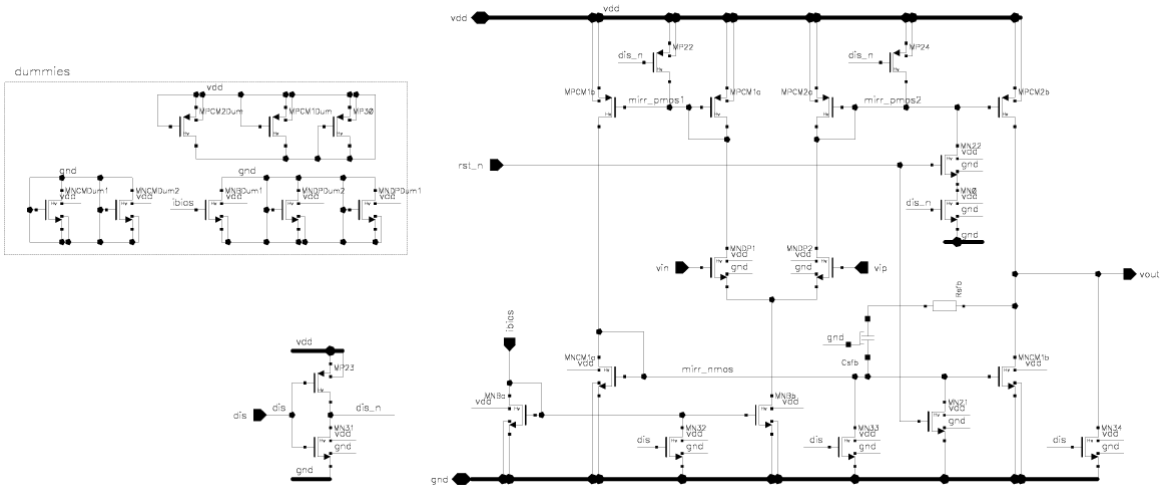

Figure 4.20: Voltage follower schematic

4.3.3 Test Bench and Simulation Results

The test bench, which was used for the verification of the voltage follower, can be seen in figure 4.21. The bias block (see section 4.6), which will be used in the system, is integrated in the test bench and takes the real biasing conditions into account.

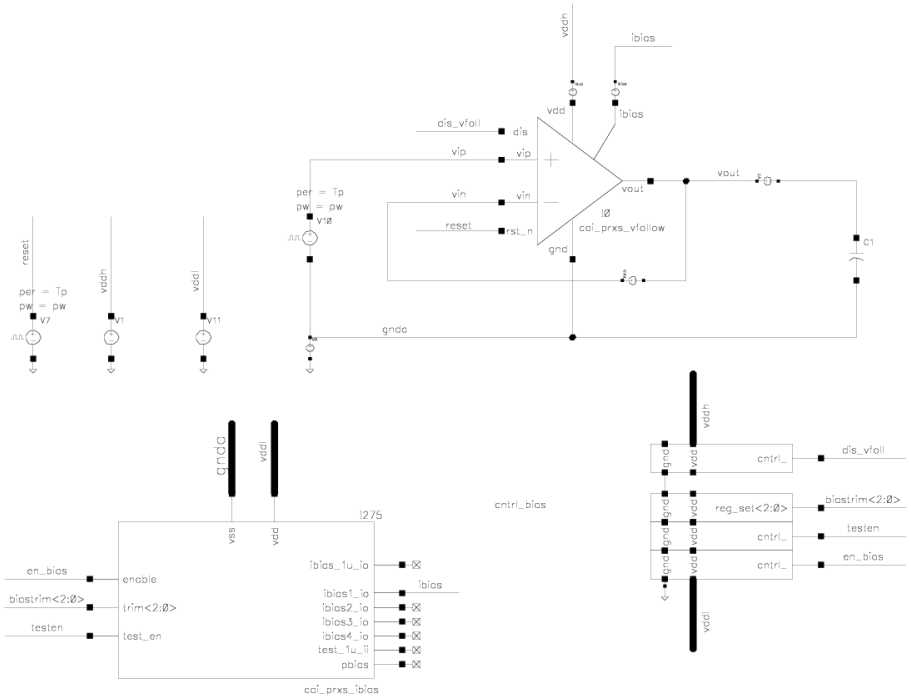

Figure 4.21: Voltage follower test bench

In figure 4.22 the schematic simulation results over process and temperature corners are shown.

Corner	temperature	topinclude.scs	Pass/Fail	bandwith	voff	Phase Margin	Isup	Ibias	Isup_pd	Ibias_pd	riseTime	fallTime	slewRate	tdel
nom	27	nominal	pass	711.9k	2.695 mV	40.03 deg	8.724 uA	53.14 nA	347.8 pA	3.153 pA	427.4 ns	13.1 us	-305.3 kV/s	191.9 ns
PVT_1_9	-40	nominal	pass	779.9k	2.28 mV	48.12 deg	9.013 uA	52.07 nA	334 pA	3.15 pA	315.2 ns	14.73 us	-271.6 kV/s	132.6 ns
PVT_1_8	85	fnsp	near	515.2k	3.078 mV	50.39 deg	8.65 uA	49.94 nA	1.442 nA	3.193 pA	535.7 ns	13.66 us	-292.8 kV/s	241.5 ns
PVT_1_7	27	fnsp	pass	630.3k	2.771 mV	49.24 deg	8.771 uA	53.22 nA	362.6 pA	3.151 pA	431.2 ns	12.9 us	-310.2 kV/s	195.9 ns
PVT_1_6	-40	fnsp	pass	780.6k	2.347 mV	48.21 deg	9.053 uA	52.14 nA	327.7 pA	3.15 pA	318.9 ns	13.62 us	-293.7 kV/s	137.9 ns
PVT_1_5	85	fnfp	near	520.2k	3.099 mV	49.95 deg	8.79 uA	50.08 nA	1.646 nA	4.031 pA	495.6 ns	13.57 us	-294.7 kV/s	220.6 ns
PVT_1_4	27	fnfp	pass	638.2k	2.798 mV	48.8 deg	8.94 uA	53.35 nA	364.5 pA	3.167 pA	399.3 ns	12.8 us	-312.4 kV/s	178.7 ns
PVT_1_3	-40	fnfp	pass	786.8k	2.373 mV	47.8 deg	9.274 uA	52.28 nA	328.3 pA	3.151 pA	295.2 ns	13.52 us	-295.8 kV/s	126 ns
PVT_1_20	85	snsp	pass	508.9k	2.96 mV	50.66 deg	8.444 uA	49.61 nA	454.4 pA	3.167 pA	564.2 ns	14 us	-285.7 kV/s	256 ns
PVT_1_2	85	fast	near	712k	3.039 mV	39.51 deg	8.826 uA	66.29 nA	1.645 nA	4.031 pA	494.8 ns	10 us	-399.9 kV/s	220.3 ns
PVT_1_19	27	snsp	pass	620.1k	2.595 mV	49.51 deg	8.521 uA	52.94 nA	347.4 pA	3.151 pA	455.1 ns	13.48 us	-296.8 kV/s	205 ns
PVT_1_18	-40	snsp	pass	772.4k	2.192 mV	48.49 deg	8.766 uA	51.87 nA	339.2 pA	3.15 pA	337.5 ns	18.27 us	-219 kV/s	139.3 ns
PVT_1_17	85	snfp	pass	514.4k	2.984 mV	50.18 deg	8.57 uA	49.72 nA	665.4 pA	4.012 pA	521.8 ns	13.93 us	-287.1 kV/s	234.1 ns
PVT_1_16	27	snfp	pass	629k	2.617 mV	49.04 deg	8.674 uA	53.07 nA	350.8 pA	3.166 pA	421.7 ns	13.39 us	-298.7 kV/s	187.1 ns
PVT_1_15	-40	snfp	near	856.7k	2.213 mV	39.01 deg	8.974 uA	52 nA	339.9 pA	3.151 pA	311.6 ns	17.87 us	-223.9 kV/s	127.4 ns
PVT_1_14	85	slow	near	417.4k	3.034 mV	52.97 deg	8.4 uA	39.63 nA	454.5 pA	3.187 pA	564.8 ns	17.9 us	-223.4 kV/s	256.3 ns
PVT_1_13	27	slow	pass	525.5k	2.653 mV	51.76 deg	8.485 uA	42.49 nA	347.4 pA	3.151 pA	455.4 ns	17.23 us	-232.1 kV/s	205.2 ns
PVT_1_12	-40	slow	fail	653.3k	2.241 mV	50.75 deg	8.739 uA	41.6 nA	339.2 pA	3.15 pA	337.7 ns	24.93 us	-160.5 kV/s	139.5 ns
PVT_1_11	85	nominal	near	514.7k	3.049 mV	50.29 deg	8.621 uA	49.61 nA	598.9 pA	3.284 pA	529.1 ns	13.78 us	-290.2 kV/s	237.8 ns
PVT_1_10	27	nominal	pass	711.9k	2.695 mV	40.03 deg	8.724 uA	53.14 nA	347.8 pA	3.153 pA	427.4 ns	13.1 us	-305.3 kV/s	191.9 ns
PVT_1_1	27	fast	pass	785.7k	2.733 mV	46.35 deg	9.004 uA	70.71 nA	364.5 pA	3.167 pA	398.7 ns	9.426 us	-424.4 kV/s	178.5 ns
PVT_1_0	-40	fast	pass	991.2k	2.315 mV	45.32 deg	9.322 uA	69.32 nA	328.3 pA	3.151 pA	294.8 ns	9.937 us	-402.5 kV/s	125.9 ns

Figure 4.22: Voltage follower simulation results

4.3.4 Physical Design

The physical design of the voltage follower is shown in figure 4.23. The different stages of the voltage follower are marked in the picture. It is approximately 133 μm $\times$ 72 μm large. The layout techniques described in section 4.2 have also been applied here.

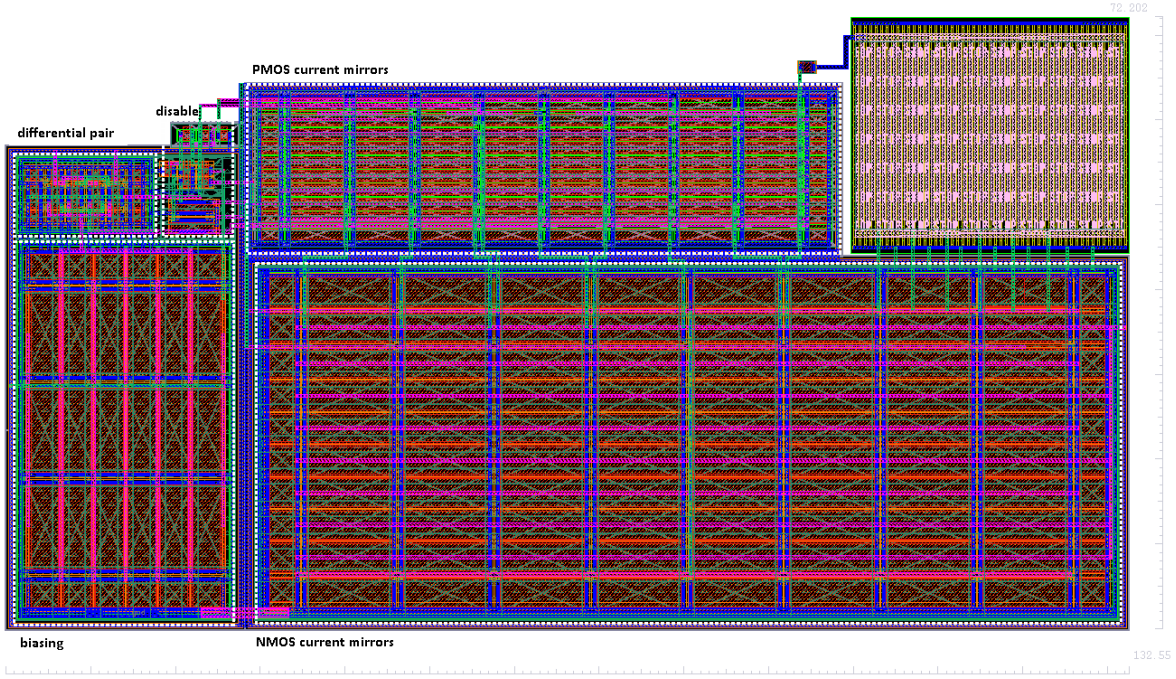

Figure 4.23: Layout of voltage follower

Figure 4.18 shows the simulation results from the RC-extracted layout. The values of the three corners in which the requirements were not met, were considered acceptable.

Corner	temperature	topinclude.scs	Pass/Fail	bandwith	voff	Phase Margin	Isup	Ibias	Isup_pd	Ibias_pd	riseTime	fallTime	slewRate	tdel
nom	27	nominal	pass	592.5k	2.691 mV	45.02 deg	8.868 uA	53.14 nA	1.655 nA	3.15 pA	428.5 ns	14.06 us	-284.5 kV/s	192 ns
PVT_1_0	-40	fast	pass	941.1k	2.311 mV	41.37 deg	9.476 uA	69.32 nA	1.634 nA	3.149 pA	296.7 ns	10.68 us	-374.6 kV/s	125.4 ns
PVT_1_1	27	fast	pass	756.1k	2.729 mV	42.38 deg	9.18 uA	70.71 nA	1.664 nA	3.164 pA	401.1 ns	10.2 us	-392.3 kV/s	179.6 ns
PVT_1_2	85	fast	fail	599.4k	3.032 mV	43.46 deg	9.018 uA	66.29 nA	2.42 nA	4.029 pA	497 ns	10.79 us	-370.6 kV/s	222.7 ns
PVT_1_3	-40	fnfp	pass	757.9k	2.369 mV	43.84 deg	9.413 uA	52.28 nA	1.633 nA	3.149 pA	297.4 ns	14.51 us	-275.7 kV/s	125.6 ns
PVT_1_4	27	fnfp	pass	598.1k	2.795 mV	44.81 deg	9.107 uA	53.35 nA	1.663 nA	3.164 pA	402.3 ns	13.82 us	-289.3 kV/s	179.8 ns
PVT_1_5	85	fnfp	fail	499.4k	3.092 mV	45.98 deg	8.974 uA	50.08 nA	2.417 nA	4.029 pA	496.7 ns	14.64 us	-273.2 kV/s	222.9 ns
PVT_1_6	-40	fnsp	pass	751.5k	2.343 mV	44.09 deg	9.195 uA	52.14 nA	1.631 nA	3.147 pA	321.3 ns	14.71 us	-271.9 kV/s	137.2 ns
PVT_1_7	27	fnsp	pass	593k	2.767 mV	45.1 deg	8.938 uA	53.22 nA	1.656 nA	3.148 pA	434.4 ns	13.88 us	-288.1 kV/s	197 ns
PVT_1_8	85	fnsp	near	493.8k	3.072 mV	46.25 deg	8.833 uA	49.94 nA	1.971 nA	3.191 pA	538.8 ns	14.71 us	-271.9 kV/s	243.9 ns
PVT_1_9	-40	nominal	pass	750.8k	2.276 mV	44.02 deg	9.149 uA	52.07 nA	1.64 nA	3.148 pA	317.8 ns	15.76 us	-253.5 kV/s	132.1 ns
PVT_1_10	27	nominal	pass	592.6k	2.691 mV	45.01 deg	8.868 uA	53.14 nA	1.655 nA	3.15 pA	428.5 ns	14.06 us	-284.5 kV/s	192 ns
PVT_1_11	85	nominal	near	493k	3.045 mV	46.16 deg	8.799 uA	49.81 nA	1.856 nA	3.281 pA	531.4 ns	14.83 us	-269.7 kV/s	240.3 ns
PVT_1_12	-40	slow	fail	613.6k	2.238 mV	46.49 deg	8.868 uA	41.6 nA	1.645 nA	3.148 pA	340.2 ns	26.09 us	-153.3 kV/s	139 ns
PVT_1_13	27	slow	pass	506k	2.65 mV	47.5 deg	8.626 uA	42.49 nA	1.656 nA	3.148 pA	459.6 ns	18.51 us	-216.1 kV/s	203.6 ns
PVT_1_14	85	slow	near	403.2k	3.03 mV	48.72 deg	8.572 uA	39.83 nA	1.756 nA	3.184 pA	569.9 ns	19.2 us	-208.3 kV/s	258.5 ns
PVT_1_15	-40	snfp	pass	750k	2.21 mV	43.94 deg	9.11 uA	52 nA	1.648 nA	3.149 pA	313.8 ns	18.6 us	-215 kV/s	127.2 ns
PVT_1_16	27	snfp	pass	592k	2.614 mV	44.93 deg	8.838 uA	53.07 nA	1.662 nA	3.164 pA	423.5 ns	14.47 us	-276.5 kV/s	186.1 ns
PVT_1_17	85	snfp	pass	492.5k	2.98 mV	46.07 deg	8.753 uA	49.72 nA	1.879 nA	4.01 pA	525.2 ns	14.98 us	-267.1 kV/s	236.4 ns
PVT_1_18	-40	snsp	pass	742.9k	2.188 mV	44.23 deg	8.905 uA	51.87 nA	1.646 nA	3.148 pA	339.1 ns	19.46 us	-205.6 kV/s	138.9 ns
PVT_1_19	27	snsp	pass	586.7k	2.591 mV	45.24 deg	8.68 uA	52.94 nA	1.657 nA	3.148 pA	459.2 ns	14.55 us	-275 kV/s	203.4 ns
PVT_1_20	85	snsp	pass	486.5k	2.956 mV	46.39 deg	8.625 uA	49.61 nA	1.758 nA	3.184 pA	566.8 ns	15.07 us	-265.4 kV/s	258.4 ns

Figure 4.24: Extracted simulation results of voltage follower

4.4 Charge Pump

4.4.1 Description and Specification

Supply voltage	1.8 V
Minimum detected capacitance	20 fF

Table 4.4: Design specifications for the charge pump

The specifications for the charge pump were derived from the system equations (see chapter 3). To achieve the required sensitivity for the system (a capacitance change of 20 fF should be detected), the ratio between C_0 and C_{cp} (C_1, C_5, C_6 and C_7 in figure 4.25) has to be very high. In order to be able to integrate these capacitances on a chip, C_0 has to be very small but still big enough that the parasitic effects do not influence the functionality of the circuit. For C_0 a capacitance value of 50 fF was chosen. Based upon this value, C_{CP} was calculated to obtain the required sensitivity. For reasons of flexibility the charge pump capacitance was made trimmable so that the customer has the possibility to change the sensitivity.

4.4.2 Circuit Design

In figure 4.25 the schematic of the charge pump is shown. The charge pump capacitor is trimmable with a three-bit-signal in 350 pF steps, which leads to eight different possible settings in the range of 350 pF to 2.8 nF. These trimming bits are bonded and thus can be changed from the outside according to the desired sensitivity.

Ideally, the reference voltage is settled in the middle of the supply voltage range, around 900 mV. The value of $vref$ is determined by the different switching times of the reference and sensor capacitor. Since the integrated capacitors are not the same as the sensor plate capacitor, it is not possible to have exactly the same two capacitors. Therefore, the reference voltage will be a bit higher or lower than half of the supply voltage, which leads to an unsymmetrical behavior. This means that if the reference voltage is above 900 mV, a down pulse leads to a bigger charge reduction of C_{CP}, than an up pulse increases the charge, and vice versa for a reference voltage lower than $\frac{V_{Supply}}{2}$. Thus, the number of up pulses differs from the number of down pulses for an addition and removal of the same capacitance. Due to this behavior also the number of achieved up pulses and thus the sensitivity differs, depending on the reference voltage level.

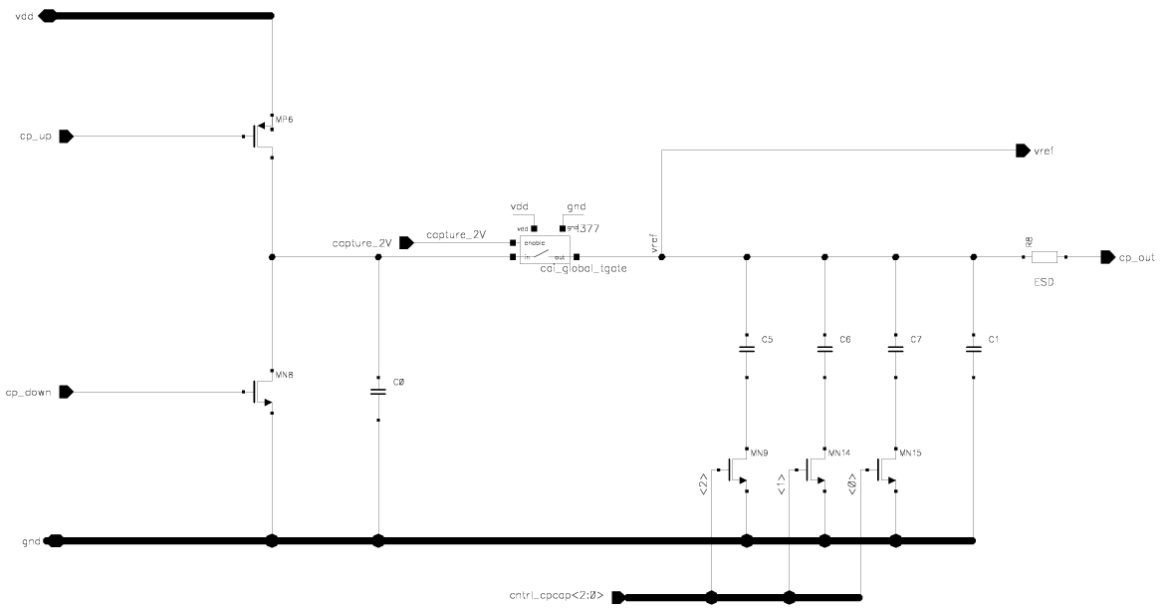

Figure 4.25: Charge pump schematic

At an up pulse, the capacitor C_0 is charged to 1.8 V, which leads to a charge of 90 fC. At the beginning of the following clock cycle, the switch (T-gate) that is controlled by the clock signal is closed and the charge is distributed between C_0 and the charge pump capacitor C_{CP}. This leads to an increase of the charge in the charge pump capacitor and thus to an increased reference voltage. At a down pulse, C_0 is discharged and at the next clock cycle, when the switch is opened, charge from C_{CP} will flow to C_0 and in this way decrease the reference voltage. The calculations that show the amount of voltage change and charge exchange per up/down pulse can be seen in chapter 3. Depending on the actual voltage level of the reference voltage, either the up-steps or the down-steps are bigger.

4.4.3 Test Bench and Simulation Results

For the charge pump circuit, only a simple test bench was created to see the transient behavior when a sequence of alternating up and down pulses is applied to it. The proper behavior within the system was tested in top level simulations.

Figure 4.26 shows the transient simulation results. The change of the reference voltage caused by the up and down pulses is shown at the middle point of the supply voltage. It can be seen that one pulse leads to a change of approximately 107 μV when C_{CP} is set to the smallest possible value (350 pF), whereas for the highest C_{CP} setting (2.8 nF) a vref-change of only 19 μV can be observed. These values match the values calculated in chapter 3 quite well.

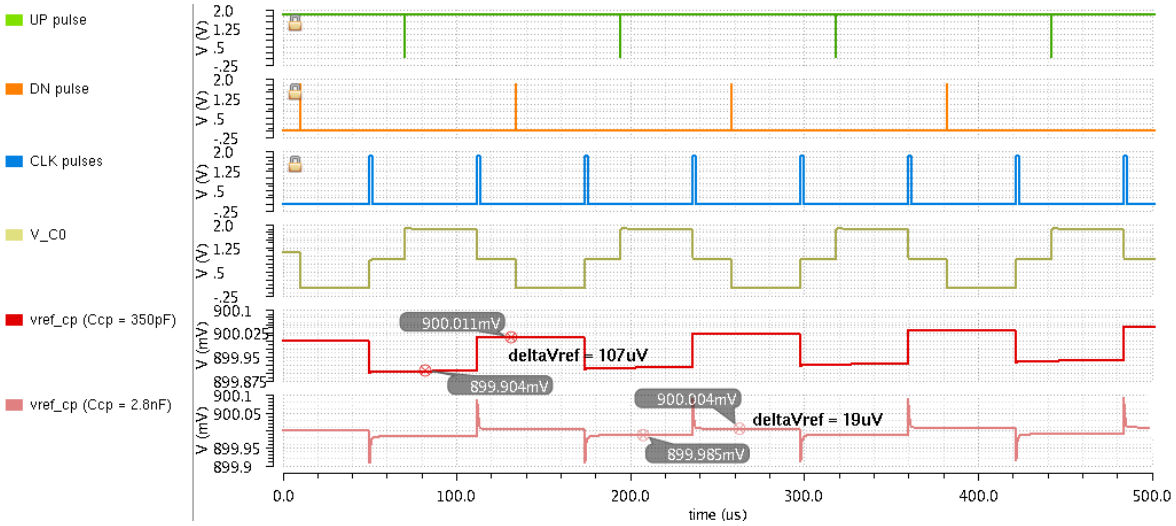

Figure 4.26: Transient simulation of charge pump

Most of the electronic systems require biasing by means of current sources for proper functionality. In order to ensure a working system consisting of the described blocks some additional circuits such as a biasing block, a bandgap reference, level shifters and a pulse generator are needed. These blocks are taken from other NXP projects where the blocks are proven to function correctly because they have already been taped out and measured. These blocks are described in the following sections.

4.5 One-shot

4.5.1 Description and Specification

The one-shot block is needed to generate a short pulse with an adjustable pulse width of about 2 μs from the externally applied clock signal. This clock signal has a duty cycle of 50%, which is not useful in the integrated system. It would lead to a higher current consumption because the sensor and the reference capacitor would have to be discharged in a shorter time frame. Additionally, the switches for charging the input capacitors as well as the ones at the charge pump would be open for a longer time. However, choosing a slower clock frequency leads to an increase of detection time. Therefore, a controllable capacitance that can be adapted within a certain range is used to determine the pulse width.

The circuit specifications are shown in table 4.5.

Supply voltage	$5V$
Current consumption	$< 300nA$
Rise time/fall time	$< 1ns$
Pulse width	$1.5us$ to $5us$

Table 4.5: Design specifications for the one-shot block

4.5.2 Schematic

A simplified schematic of the one-shot block is shown in figure 4.27.

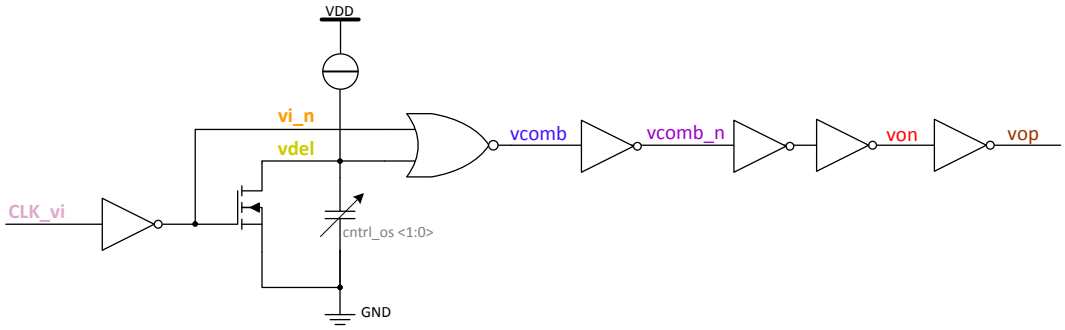

Figure 4.27: Simplified schematic of one-shot block

The signal *vdel* is derived from the inverted clock signal (*vi_n*). Vdel is logic 0 as long as vi_n is logic 1. As soon as *vi_n* turns low, it rises to high with a delay. The delay time can be changed by a 2-bit control signal that switches additional capacitors on or off. These

two signals are combined with a NOR gate (*vcomb*), which is only logic high when both input signals are 0. This is only the case for a short period of time at the beginning of a clock cycle, when *vdel* has not yet reached the threshold voltage of the transistor. Hence a small trimmable pulse in the range of 1.5 μs to 5 μs is generated. By means of some inverters behind the NOR gate, an extra signal conditioning is applied to make sure that the signal edges at the output are sharp and sufficiently steep. The signal behavior is shown in the transient simulation results in figure 4.29.

4.5.3 Test Bench and Simulation Results

The test bench, which was used for the verification of the one-shot block, can be seen in figure 4.28.

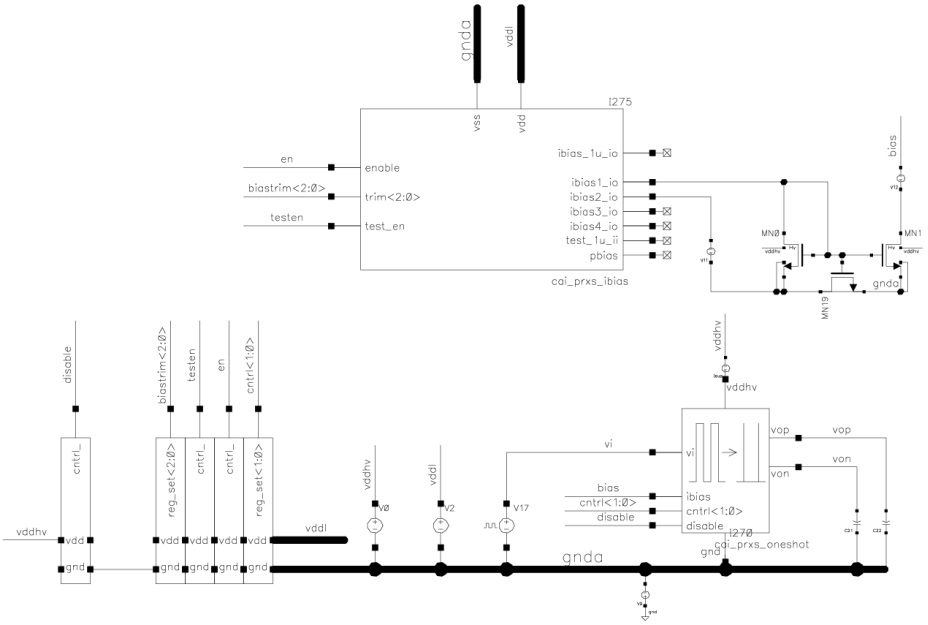

Figure 4.28: One-shot test bench

For this circuit a transient simulation was set up to determine rise and fall time, current consumption, pulse width and delay time. The rise and fall time was calculated as the time the signal needs to reach 90% of its end value, starting from 10%, as already graphically explained in figure 4.10. The current consumption was determined by integration of the transient current and calculation of the slope of this integral. The bias block (see section 4.6), which will be used in the system, is integrated in the test bench, already taking real biasing conditions into account. The highlighted signals in the schematic in figure 4.27 are shown in the transient simulation results in figure 4.29.

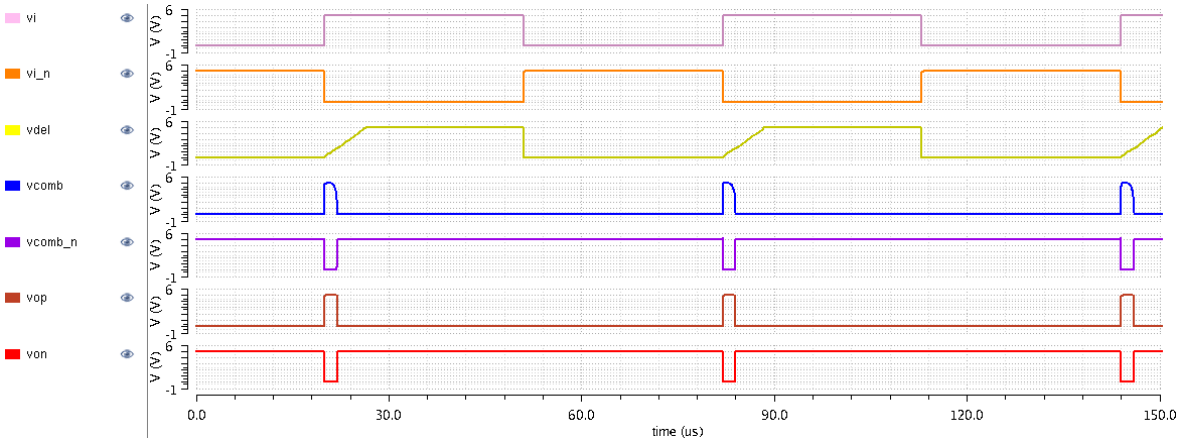

Figure 4.29: Transient simulation results of one-shot block schematic

The summary of the PVT simulations of the important circuit parameters is shown in figure 4.30. The simulations were run on all process corners (fast, fnfp, fnsp, nominal, slow, snfp, snsp) and three different temperatures (−40 °C, 27 °C and 125 °C).

Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max
TRAN	riseTime	736.9 ps	< 1n		pass	619.2 ps	913 ps
TRAN	fallTime	694.4 ps	< 1n		pass	594.7 ps	830.2 ps
TRAN	Isup	180.6 ns	< 300n		pass	150.3 ns	293.8 ns
TRAN	tpw	2.278 us	range 1.5u 5u		pass	1.614 us	4.595 us
TRAN	tdel	22.98n				20.59n	25.71n

Figure 4.30: PVT simulation results of one-shot block schematic

4.5.4 Physical Design

The physical design of the one-shot block is shown in figure 4.31.

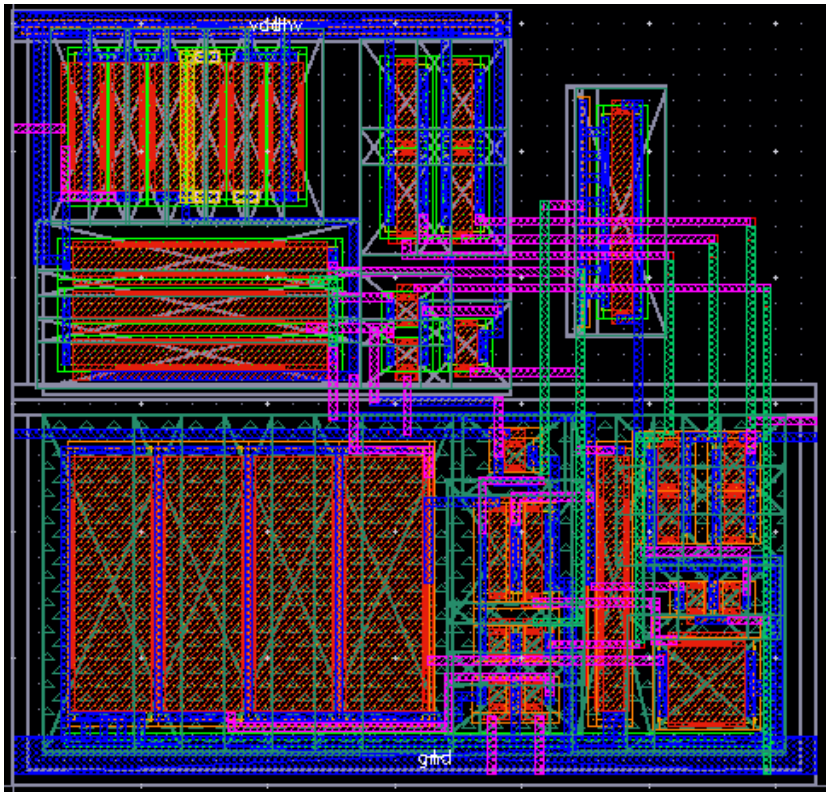

Figure 4.31: One-shot layout

The summary of the PVT simulation results of the extracted layout is shown in figure 4.32. It can be seen that some corners are slightly outside the required boundaries. Since the protrusion is very small and the affected corners are only corners at high temperature (125 °C), it was considered acceptable because the overall specification was only set up to 85 °C.

Test	Output	Nominal	Spec	Pass/Fail	Min	Max
TRAN	riseTime	823.8 ps	< 1n	near	698.9 ps	1.009 ns
TRAN	fallTime	774.2 ps	< 1n	pass	657.9 ps	932.3 ps
TRAN	Isup	205 ns	< 300n	near	171.5 ns	327.6 ns
TRAN	tpw	2.732 us	range 1.5u 5u	near	1.937 us	5.352 us
TRAN	tdel	33.6n			30.01n	37.81n

Figure 4.32: PVT simulation results of RC-extracted one-shot block

4.6 Bias Block

4.6.1 Description

The main part of the bias block was taken from another project. It consists of a PMOS-mirror that provides a current output of 1 μA, four branches that provide a current of 50 nA and a test output with also 1 μA, which has been bonded for functional tests in the lab. A version of the 1 μA, which was multiplied by five, was used for discharging the reference and sensor capacitor. The other currents were needed for the bandgap reference, the voltage follower, the comparators and the one-shot block. The core bias block consists also of a seven-step resistor ladder for trimming. With this, variations that can occur due to production inaccuracies can be compensated.

4.6.2 Schematic

The schematic of the currents derived from the bias block is shown in figure 4.33.

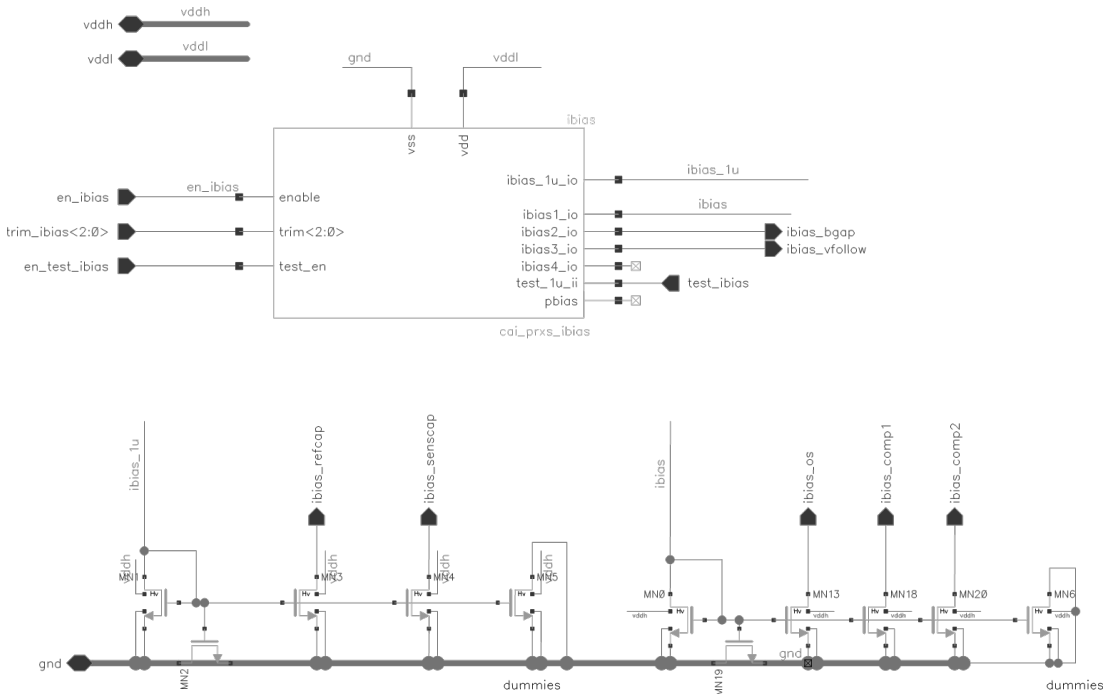

Figure 4.33: Schematic of bias block

4.6.3 Simulation Results

A simulation over process corners and temperature was done to check which values for bias currents and current consumption of the block could be expected. The results can be seen in

figure 4.34.

Corner	temperature	topinclude.scs	Ibias_comparator	Ibias_os	Ibias_caps	Ibias_bgap	Ibias_vfollow	I_vddl	I_vddh
PVT_1_0	-40	fast	517.1n	51.93n	4.693u	45.39n	45.33n	1.19u	90p
PVT_1_1	27	fast	520.5n	52.34n	4.73u	46.34n	46.28n	1.203u	92.71p
PVT_1_2	85	fast	485.2n	48.82n	4.405u	43.53n	43.49n	1.125u	327p
PVT_1_3	-40	fnfp	392.4n	39.38n	3.564u	34.25n	34.21n	913.7n	90p
PVT_1_4	27	fnfp	395n	39.68n	3.6u	35n	34.96n	923.7n	92.71p
PVT_1_5	85	fnfp	368.5n	37.03n	3.362u	32.92n	32.89n	866.1n	327p
PVT_1_6	-40	fnsp	390.8n	39.23n	3.552u	34.17n	34.12n	898.8n	90p
PVT_1_7	27	fnsp	393.6n	39.54n	3.588u	34.92n	34.88n	910.3n	92.71p
PVT_1_8	85	fnsp	366.8n	36.87n	3.346u	32.81n	32.78n	852.6n	327p
PVT_1_9	-40	nominal	390.1n	39.15n	3.544u	34.12n	34.08n	898.7n	90p
PVT_1_10	27	nominal	392.8n	39.46n	3.579u	34.87n	34.83n	909.7n	90.27p
PVT_1_11	85	nominal	365.6n	36.75n	3.332u	32.71n	32.68n	850.6n	113.7p
PVT_1_12	-40	slow	312.5n	31.35n	2.842u	27.28n	27.24n	719.3n	90p
PVT_1_13	27	slow	314.8n	31.61n	2.873u	27.89n	27.86n	728.8n	90.03p
PVT_1_14	85	slow	292.9n	29.42n	2.676u	26.17n	26.15n	681.7n	92.37p
PVT_1_15	-40	snfp	389.4n	39.08n	3.537u	34.08n	34.04n	898.7n	90p
PVT_1_16	27	snfp	392.2n	39.39n	3.57u	34.82n	34.78n	909.2n	90.03p
PVT_1_17	85	snfp	364.8n	36.66n	3.321u	32.65n	32.62n	849.6n	92.37p
PVT_1_18	-40	snsp	387.9n	38.94n	3.525u	34n	33.96n	885.6n	90p
PVT_1_19	27	snsp	390.8n	39.27n	3.557u	34.74n	34.71n	897.2n	90.03p
PVT_1_20	85	snsp	363.6n	36.55n	3.308u	32.58n	32.55n	838.3n	92.37p

Figure 4.34: Simulation of bias block

4.7 Bandgap Reference

4.7.1 Description and Specification

The bandgap block that was used to generate the reference voltage is also used in other products of NXP and its function is ensured by validated silicon. A bandgap circuit, which provides a reference voltage of about half the supply voltage and has as low current consumption, is required.

Supply voltage	1.8 V
Reference voltage	$\approx$ 900 mV
Current consumption	<<

Table 4.6: Specifications for the bandgap reference

4.7.2 Schematic

Figure 4.35 shows a simplified schematic of the used bandgap reference block.

Bipolar transistors connected in a diode configuration are used to create a bandgap reference voltage. Such a diode has a large temperature dependence of about $-2\,\mathrm{mV}/^{\circ}\mathrm{C}$. Since the voltage across the diode-connected transistor decreases linearly with temperature, another voltage, which is proportional to absolute temperature (PTAT), has to be added to it to create a temperature-independent reference voltage. This PTAT voltage is Δvbe on the resistor (R_{PTAT}), as following equations show. Here I_S is the saturation current of the bipolar transistors. [7]:

$$I_C = I_S \exp\left(\frac{V_{BE}}{\frac{kT}{q}}\right) \tag{4.8}$$

$$V_{BE} = \frac{kT}{q} \ln \frac{I_C}{I_S} \tag{4.9}$$

$$\Delta V_{BE} = V_{BE1} - V_{BE1} \tag{4.10}$$

$$\Delta V_{BE} = \frac{kT}{q} \ln \frac{I_{S2}}{I_{S1}} \tag{4.11}$$

A bandgap based on two current mirrors, such as the one that is used here, has two different operating points, where both the currents in the two branches are equal. One where the currents are zero, which has to be avoided, and one where they are bigger than zero, which

is the desired operating point. To assure that the bandgap is operating correctly, a start-up circuit is required. [7]

To force the circuit in the correct operating point, a bias current is used here. Hence the desired reference voltage occurs on the output, which then switches off the start-up circuit and the bandgap reference remains at the right operating point.

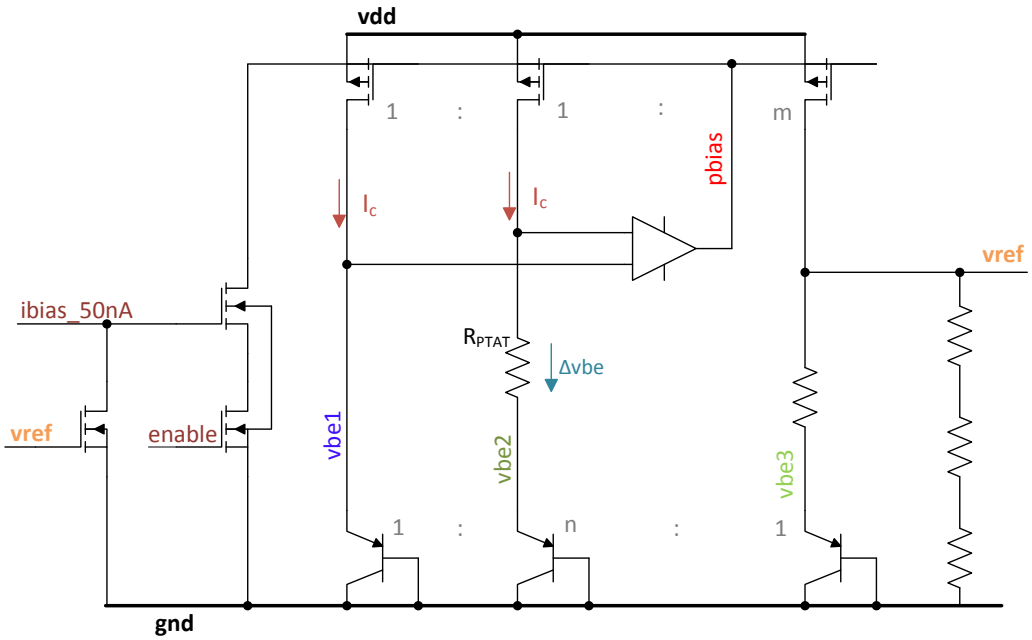

Figure 4.35: Simplified schematic of bandgap reference

4.7.3 Test Bench and Simulation Results

A simulation over process corners and temperature was carried out to check which values for the reference voltage and current consumption can be expected. The results can be seen in figure 4.36.

Corner	temperature	topinclude.scs	Pass/Fail	Isup	vref at 800u
nom	27	nominal			
PVT_1_0	-40	fast	pass	1.088 uA	923.5 mV
PVT_1_1	27	fast	pass	1.232 uA	907 mV
PVT_1_2	85	fast	pass	1.438 uA	906.7 mV
PVT_1_3	125	fast	pass	1.58 uA	901.1 mV
PVT_1_4	-40	fnfp	near	1.652 uA	889.1 mV
PVT_1_5	27	fnfp	pass	942.7 nA	903.7 mV
PVT_1_6	85	fnfp	pass	1.099 uA	902.2 mV
PVT_1_7	125	fnfp	pass	1.206 uA	895.5 mV
PVT_1_8	-40	fnsp	near	1.26 uA	881 mV
PVT_1_9	27	fnsp	pass	936.4 nA	920.4 mV
PVT_1_10	85	fnsp	pass	1.089 uA	923.5 mV
PVT_1_11	125	fnsp	pass	1.197 uA	921.5 mV
PVT_1_12	-40	nominal	pass	1.259 uA	917.7 mV
PVT_1_13	27	nominal	pass	935.7 nA	920.4 mV
PVT_1_14	85	nominal	pass	1.088 uA	923.5 mV
PVT_1_15	125	nominal	pass	1.195 uA	921.5 mV
PVT_1_16	-40	slow	pass	1.253 uA	917.6 mV
PVT_1_17	27	slow	near	755.4 nA	933.8 mV
PVT_1_18	85	slow	near	875.3 nA	940.5 mV
PVT_1_19	125	slow	near	957.8 nA	941.7 mV
PVT_1_20	-40	snfp	near	1.003 uA	941 mV
PVT_1_21	27	snfp	pass	935 nA	920.4 mV
PVT_1_22	85	snfp	pass	1.087 uA	923.6 mV
PVT_1_23	125	snfp	pass	1.188 uA	921.5 mV
PVT_1_24	-40	snsp	pass	1.243 uA	917.5 mV
PVT_1_25	27	snsp	near	930.6 nA	936.1 mV
PVT_1_26	85	snsp	near	1.08 uA	943.7 mV
PVT_1_27	125	snsp	near	1.182 uA	945.7 mV
			near	1.238 uA	945.5 mV

Figure 4.36: Simulation results of the bandgap reference circuit

4.7.4 Physical Design

The physical design of the complete bandgap circuit is shown in figure 5.10 in chapter 5.4 as part of the analog front-end.

Figure 4.37 shows the layout implementation of a bipolar PNP transistor in a CMOS process. The bipolar transistor is built by the parasitic transistor between the PPLUS and NPLUS region.

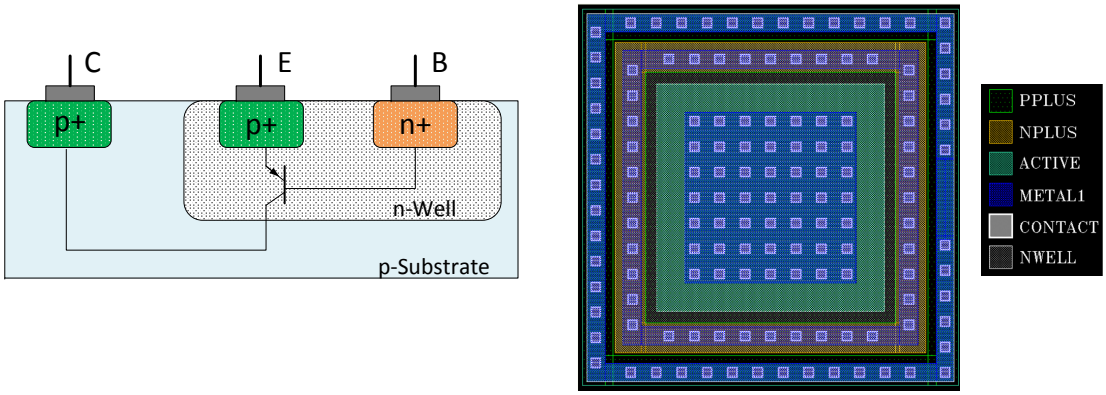

Figure 4.37: Layout of bipolar transistor in CMOS process

4.8 Analog Front-End

4.8.1 Schematic

The whole analog front-end was built with the blocks described in the previous sections. Additionally, some level shifters were needed to shift the disable signal for the D-FF to the higher voltage and to shift the clock signal to the lower voltage, for the logic block and the charge pump. The D-FF is needed to generate the signals that control the comparator delay. The logic block derives the up and down pulses from the comparator outputs. The logic block consists of AND- and XOR-gates as well as some RS-latches and is responsible for creating a pulse on either the upper or lower branch, depending on the comparator outputs. To protect the chip from being damaged by electrostatic discharge, ESD protection diodes and resistors were added to the sensor input. This will be described in more detail later in this thesis. Figure 4.38 shows the schematic of all the blocks that have been used, connected together.

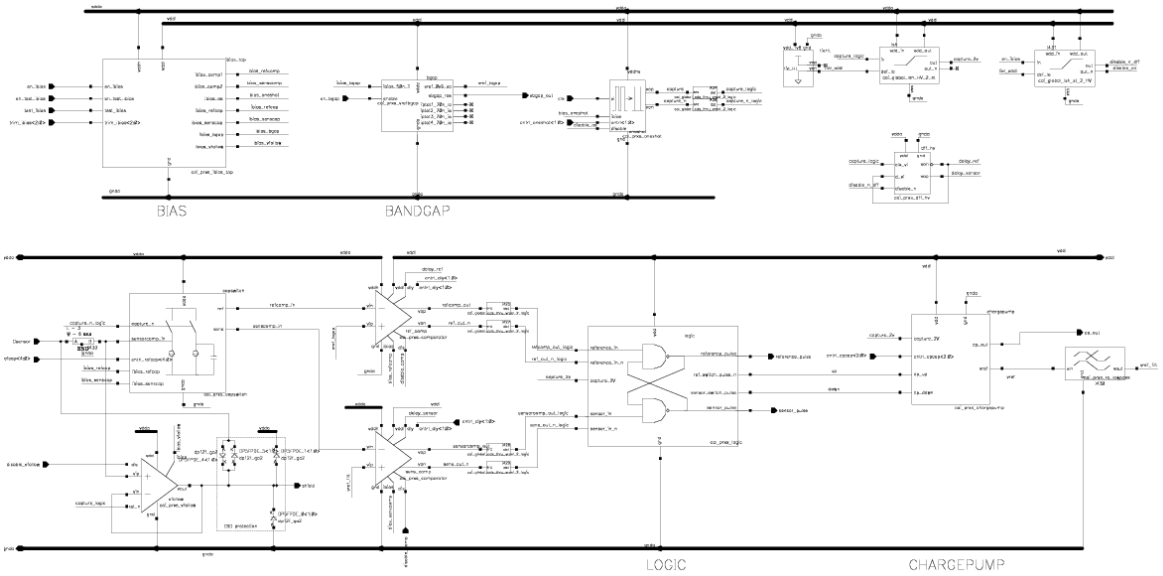

Figure 4.38: Analog front-end schematic

4.8.2 Test Bench and Simulation Results

The test bench which was used to verify the analog front-end is shown in figure 4.39. The system is built to be highly flexible, therefore, a lot of control signals are needed. To be able to set the signals in a convenient way, have a neatly arranged test bench and state setup, a Verilog-A module was used. By doing so, the control values for a bus can be set via a decimal value, and the module calculates for every bit if it has to be set to high or low. The desired voltage level just needs to be connected to the module input. A capacitor, pre-charged to about the level of the bandgap reference voltage, was connected to the charge

pump output to reduce the start up time and hence the simulation time. A fixed capacitance, representing the one of the sensor plate, was connected via the model of the coaxial cable to the sensor input. An additional capacitance, representing the human body ($C_{body} = 100\,\text{pF}$) and the approaching hand (deltaCs), can be added to the sensor capacitance via a switch.

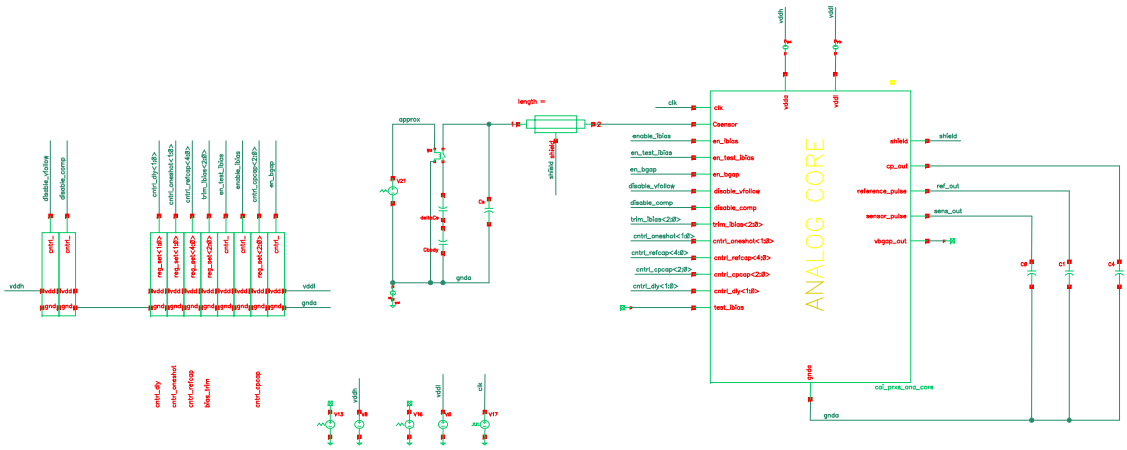

Figure 4.39: Analog front-end test bench

In figure 4.40 the system behavior in one clock cycle is shown. One can see that the discharge curve of the reference comparator crosses the bandgap reference voltage before the discharge curve of the sensor capacitor crosses the charge pump reference voltage. Thus, the reference capacitor switches first. Both comparator outputs are connected to an XOR-gate whose output is the *xor_out* signal. This signal is combined with both comparator outputs via two AND-gates and in this way an up pulse is generated at the output of the logic block. This leads to an increase of the charge pump reference voltage, which will cause the sensor comparator to switch first in the next clock cycle. The up pulse is inverted (active low) because it has to switch a PMOS transistor.

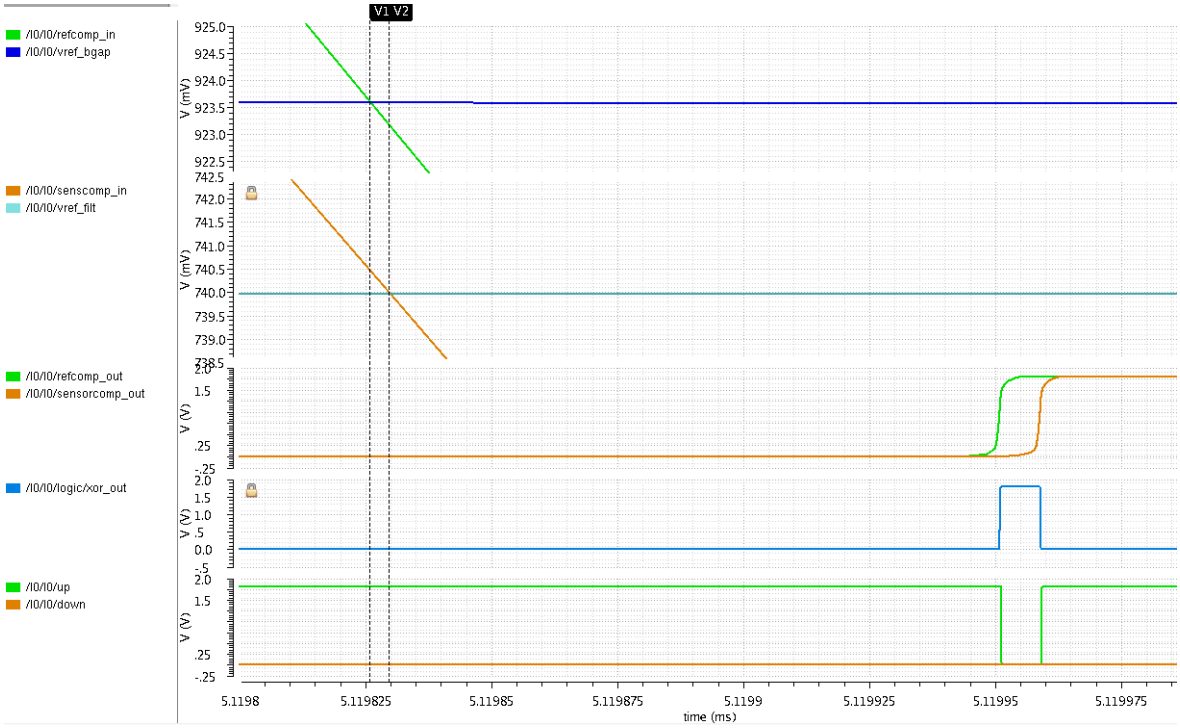

Figure 4.40: Transient simulation output of analog front-end to illustrate one clock cycle

More simulation results are shown in chapter 5.3 and chapter 7.

5 Top Level Verification and System Integration

5.1 IO Circuitry

IO pads are used as interface from the chip to the outside world. Via the IOs the chip can be powered, controlled and measured. Often, special circuitry is implemented in the pads, which protects the chip from damage due to electrostatic discharge (ESD).

In the pad ring of this chip five different types of IOs are used:

- MFIO pad - Multi function IO
- APIO pad - Analog purpose IO
- VDDE pad
- GND pad
- RF pad

The MFIO pads are used for all the control signals and the clock signal. The APIO pads are used for the bias test signal ($test\_ibias$), the bandgap voltage and the Vdd_1v8 supply voltage. For the Vdd_IO and Vdd_5v5 supply, VDDE pads are used. The RF pads, which are simple metal structures, are designed for minimal capacitance. These pads, without integrated ESD protection, are used for the shield input (Sh), the charge pump reference voltage ($vref\_cp$) and the sensor input (Cs). To protect the shield and the sensor input from electrostatic discharge, antiparallel diodes were placed. For the reference voltage, only a serial resistor was utilized because the output was used for test purposes and it was not planned to bond it in a possible product version.

The pads are designed by an NXP in-house team. The block diagram of an MFIO pad is shown in figure 5.1.

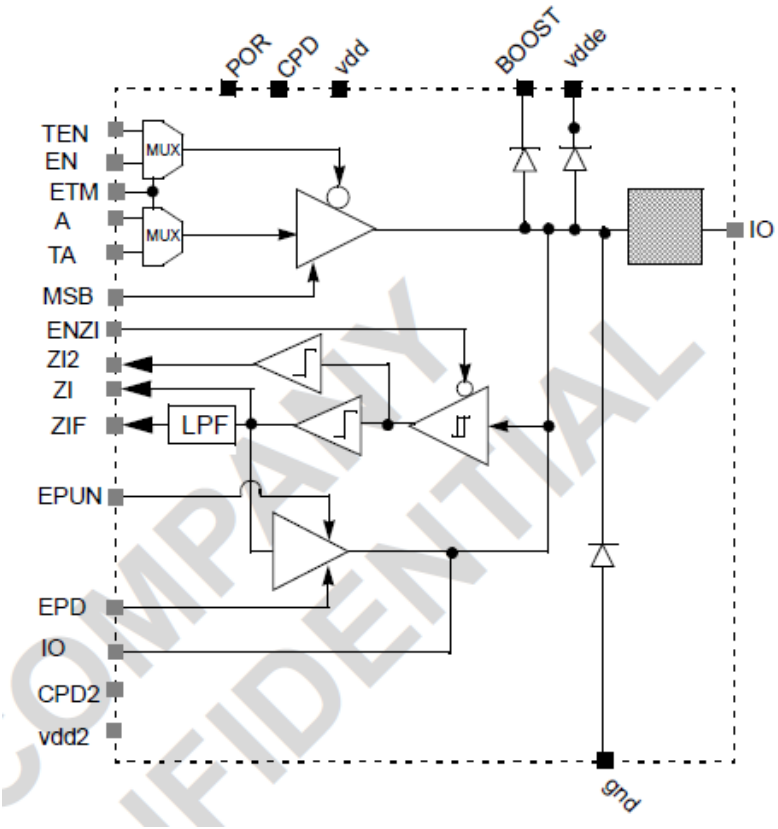

Figure 5.1: MFIO pad [22]

Since the MFIO pad can be used as input or output with different modes, it has to be configured according to one's needs. If a chip has an integrated microcontroller, this configuration is flexible and can be changed during the operation. In this case the chip merely consists of the analog front-end. Therefore, the configuration of the MFIO pads has to be implemented hard-wired and thus determined beforehand.

Figure 5.2 and figure 5.3 show the possible modes in which the pad can be put in and the required settings for that.

Input					Output	Mode
ETM	EN	TEN	A	TA	IO	
L	L	—	L	—	L	Output mode
			H	—	H	
L	H	—	—	—	Z	Input mode [1]
H	—	L	—	L	L	Test mode
				H	H	
H	—	H	—	—	Z	Test input mode [1]

Figure 5.2: Configuration possibilities of MFIO pad part 1 [22]

Input				Output		Mode
IO[1]	ENZI[2]	EPUN[3]	EPD[3]	IO	ZI/ZIF/ZI2	
—	H	—	—	—	L	Receiver disabled
Programmable input options						
Receiver enabled						
Z	L	L	L	h	H	Pull-up
Z	L	L	H	io	IO	Repeater
Z	L	H	L	Z [1]	IO	High impedance
Z	L	H	H	I	L	Pull-down
Receiver disabled						
Z	H	L	L	h	L	Pull-up
Z	H	L	H	Z	L	High impedance
Z	H	H	L	Z	L	High impedance
Z	H	H	H	I	L	Pull-down

Figure 5.3: Configuration possibilities of MFIO pad part 2 [22]

The MFIO pads for the *Proxysense* chip were configured in repeater mode so that the output stays in its state (high or low) even when the input signal is not present anymore.

In figure 5.4 the schematic of an APIO pad is shown.

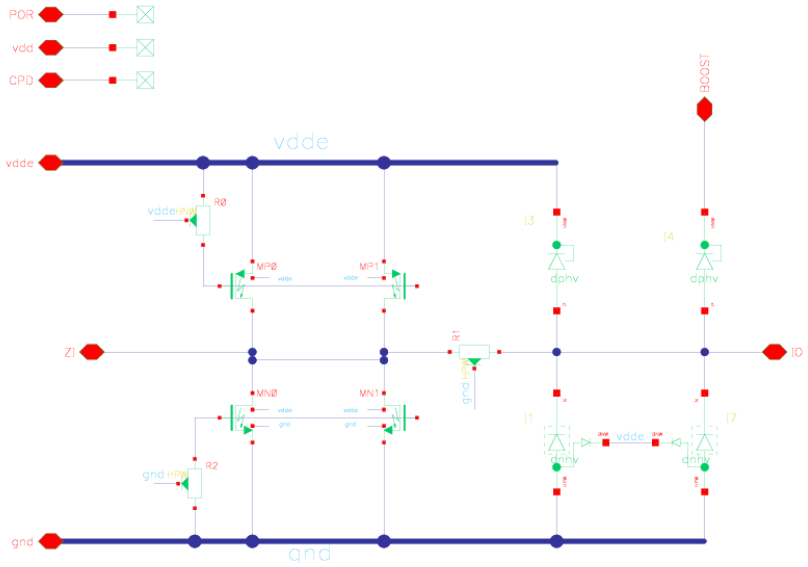

Figure 5.4: Schematic of APIO pad

In figure 5.5 the top view and the 3D view of the used RF pads are shown. It is an octagonal shaped metal6 (top metal layer) pad with stacked metal1 to metal5 structures underneath. Using this structure ensures very low capacity on the one hand, and a good stability, which is needed for connecting the bond wire, on the other hand.

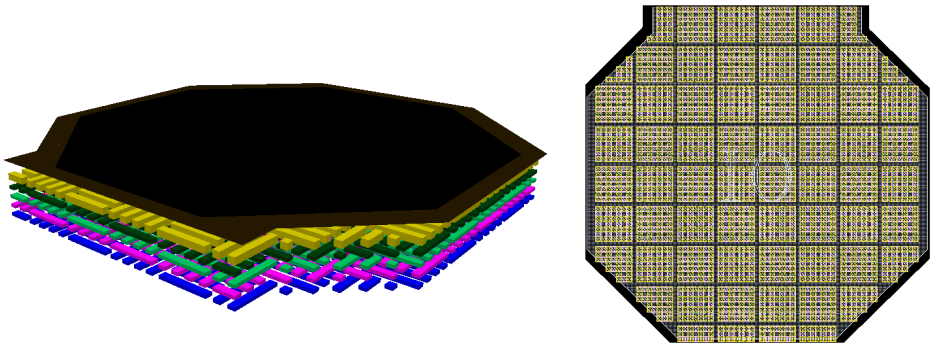

Figure 5.5: RF pad in 3D and top view

As mentioned previously, the system is a stand-alone analog system with no microcontroller on board. Therefore, every control signal needs to be connected to a separate pad separate pad so that the settings can be changed from outside. To fulfill the requirements and have high flexibility, 20 different control signals are used. They are needed for the reference and charge pump capacitors, the bias currents, to control the clock pulse width and to disable single blocks. Together with the pads for the supply and reference voltages, the pads for the clock signal and for the sensor input/output signals, a total of 33 pads have been designed in. In figure 5.6 the schematic and layout of the complete pad ring are shown. The chip is pad limited, which means that the pad size rather than the circuit area determines the chip area, and it has a total area of 2410 μm $\times$ 2370 μm. The layout of the analog front-end covers only less than half of this area, which is pointed out in chapter 4.8. In a possible product version also digital circuitry with a microcontroller would be integrated and thus much less control signals would have to be bonded. Thus, a product chip would not need an area this large.

Since two VDDE pads, which are connected to the supply rails of the complete pad ring, have been used, the ring has been split into two different supply domains. One for Vdd_5v5, which only contains the pad and two big FETs, and the other one for Vdd_IO, which connects all other pads. The RF-pads are located on the left edge above the 5.5 V-domain, while the control signal pads are placed on the upper, lower and right edge of the ring.

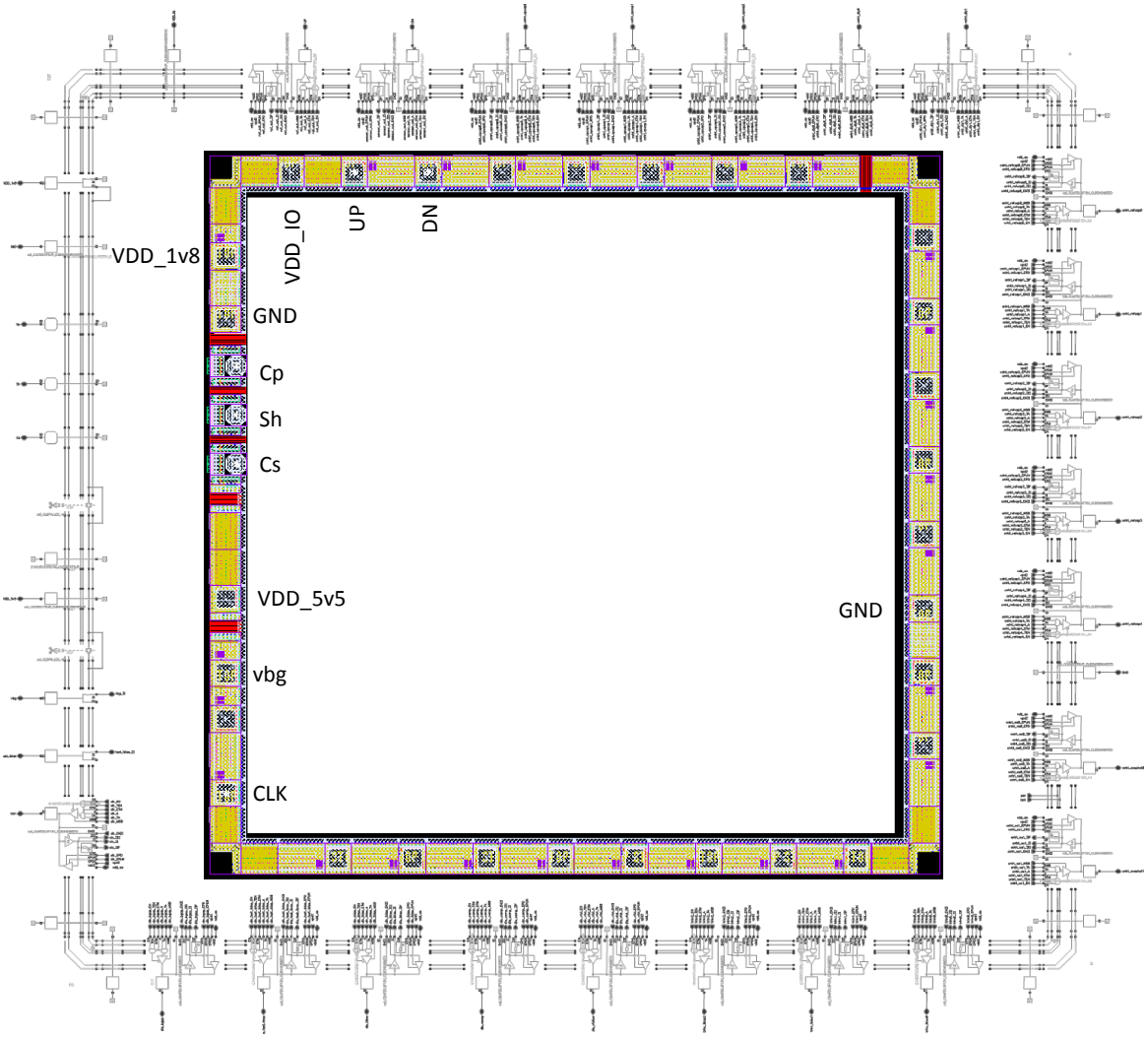

Figure 5.6: Pad ring schematic and layout

5.2 ESD Protection Measures

The supply and ground pads (VDDE pad, GND pad) have big FETs included for ESD protection. To ensure that there is a minimum path length between any IO and a big FET, additional big FETs where added at all four corners of the pad ring. The big FETs are the bright yellow parts in the layout in figure 5.6.

The paths in the pad ring are routed in the top metal layer and in metal stacks, respectively, to make them as low ohmic as possible in order to avoid large voltage peaks in case of an ESD event.

For the bandgap and the charge pump voltage output, only a serial resistor was added and no other ESD measures were taken because it was not planned to bond these signals for a

possible product version of the chip.

The sensor and the shield input are protected by antiparallel diodes.

Figure 5.7 shows the two different supply domains and the ESD protection concept as described above.

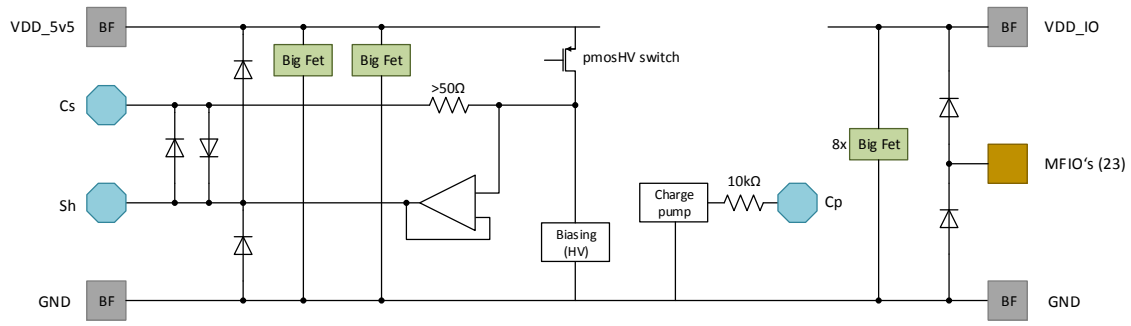

Figure 5.7: ESD protection concept

5.3 Top Level Test Bench and Simulation Results

The test bench for the simulations of the complete *Proxysense* chip is shown in figure 5.8. In this test bench a model of the sensor was added. With this model it is possible to set the sensor area, the ambient temperature, the detection distance and so on. It also has a test input with which capacitance can be added at different times and thus every arbitrary approximation curve can be used as input. This sensor model was developed as part of the aforementioned thesis about modeling [10], in which it was used for system simulations. However, in this thesis the test input was mainly used to mimic a realistic approaching behavior, which is further described in chapter 6 and chapter 7.

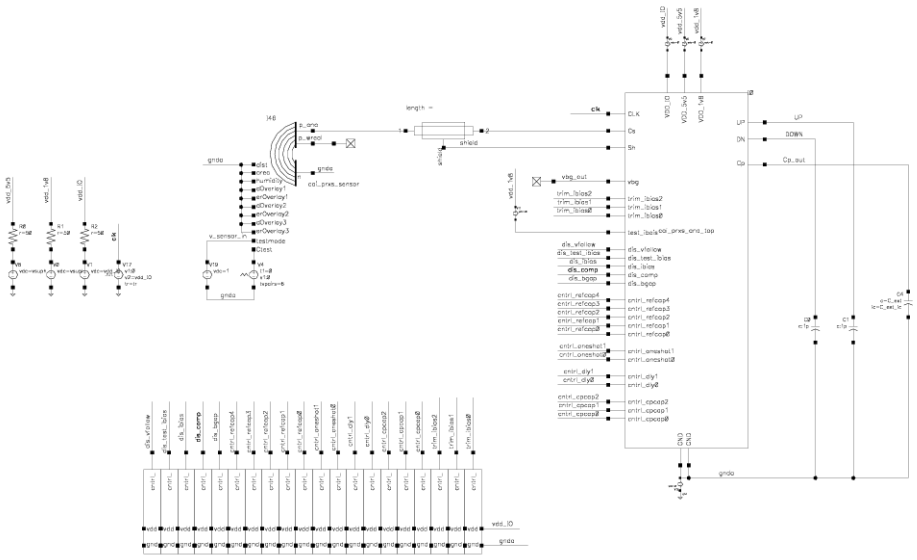

Figure 5.8: Top level test bench for slow approach

In figure 5.9 the transient top level simulation results can be seen. The up and down pulses as well as the behavior of the reference voltage of the charge pump at the start-up of the system and at a mimicked hand approach and removal are shown. For this simulation a fast approach/removal was used, this means that the capacitance was added at once and not gradually. More simulation results with different approach curves are shown in chapter 7.

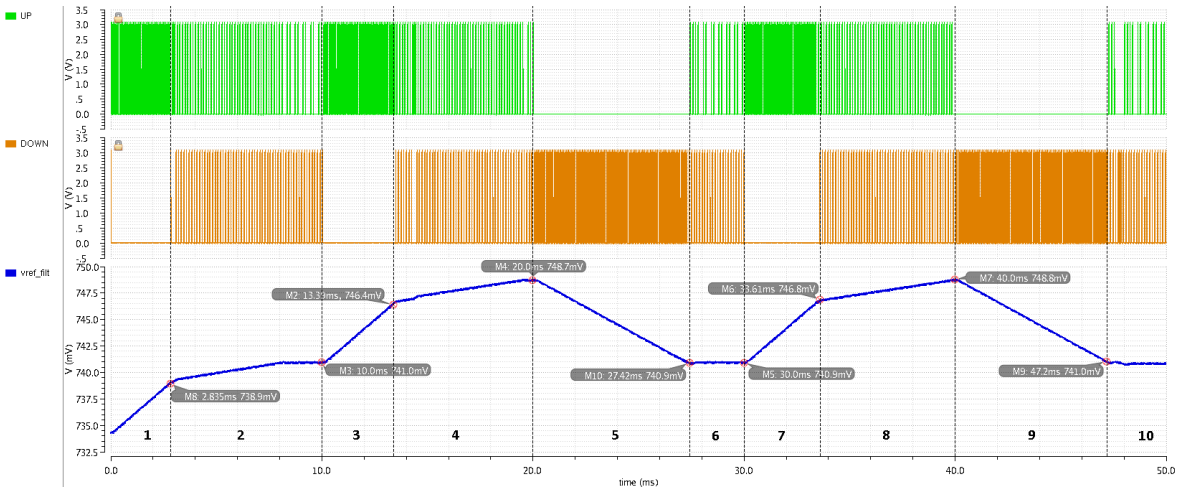

Figure 5.9: Top level simulation: fast approach, $\Delta_C = 70\,\text{fF}$

1. Start-up phase: To speed up the simulation, the charge pump capacitance is initially charged to around 735 mV to be close to the equilibrium point. In this phase only up pulses are present until the equilibrium point is reached. The equilibrium point is reached at about 739 mV, which means that the sensor capacitor is smaller than the reference capacitor in this simulation.

2. Equilibrium phase: Up and down pulses occur alternately. The reference voltage is below 0.9 V, which leads to unequal charge pump behavior. The up-steps are bigger than the down-steps which is why the reference voltage still rises slightly in this phase.
3. Approach phase: At 10 ms a 70 fF capacitance is added to the sensor input, which leads to a longer discharge time of the sensor capacitor and thus the reference voltage has to rise to reach the equilibrium point again. This leads to approximately 54 consecutive up pulses in the simulation.
4. Equilibrium phase: The system has compensated for the additional 70 fF and is in an equilibrium state again.
5. Removal phase: At 20 ms the additional capacitance is removed again, which leads to a series of down pulses to compensate the change. A series of approximately 118 down pulses in a row are necessary to reach the equilibrium point. As mentioned in point 2., the voltage step size of a down pulse is smaller than that of an up pulse and thus more pulses are needed to compensate for the same capacitance change. For a C_{ref} smaller than C_{sensor} it would be the other way round.
6. to 10. show a second approach - removal cycle with the same capacitance to verify if the behavior is always the same.

5.4 Physical Design

The physical design of the complete analog front-end, combining all blocks, is shown in figure 5.10. It covers an area of about 645 μm $\times$ 900 μm and only a small part of the area inside the pad ring.

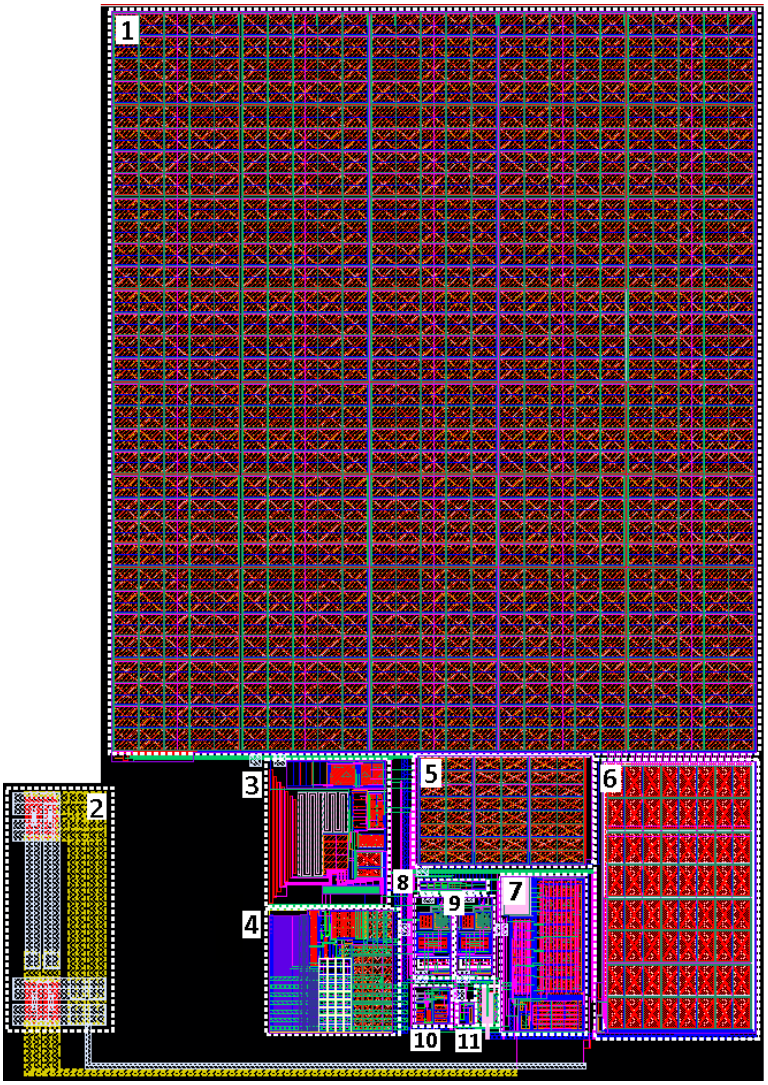

Figure 5.10: 1 Charge pump capacitance Cp (350 pF to 2.8 nF)
2 Connection to Sh and Cs pin with antiparallel ESD diodes
3 Bias block
4 Bandgap reference
5 RC filter
6 Reference capacitance (4 pF to 64 pF)
7 Voltage follower
8 Logic block
9 Reference and sensor comparator
10 One-shot block
11 Level shifter

To complete the entire chip, the analog core layout has to be placed inside the pad ring and connected with it. Before the masks can be sent to production, some special measures have to be taken. The empty areas of the chip are filled with floating metal stripes of all layers as well as with ACTIVE and diffusion layer pieces. This is done to achieve a better mechanical stability of the silicon die and to have a planar surface of the chip, thus guaranteeing that

the height of the layers, which are distributed everywhere around the chip, is the same all-around. Furthermore, a so-called seal ring is placed around the pad ring to prevent moisture from entering the silicon during the sawing of the chip. Finally, it has to be checked if the distance and area rules for mask set production are fulfilled and if all the blocks are connected properly according to the schematics. This is validated with a DRC (design rule check) and an LVS (layout versus schematic) check. In figure 5.11 the layout of the complete *Proxysense* chip is shown.

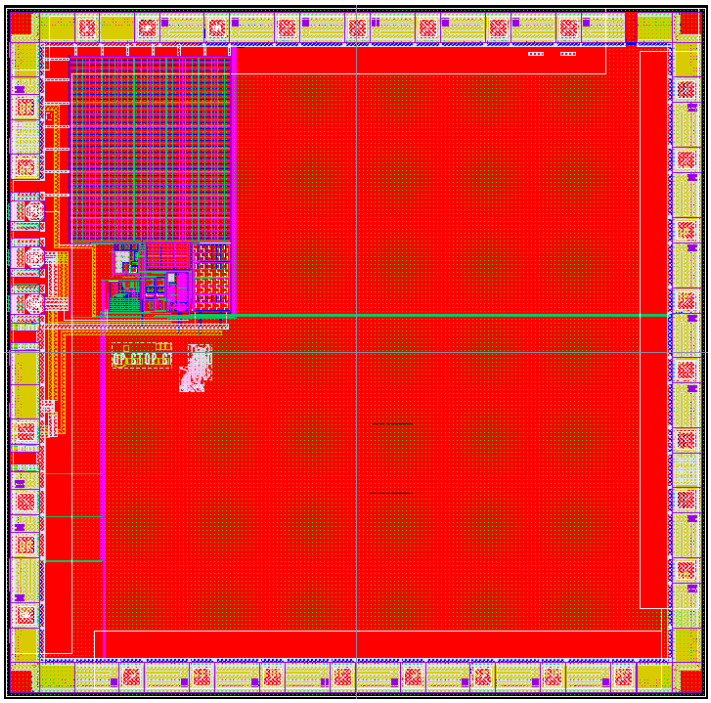

Figure 5.11: Physical design of *Proxysense* chip

5.5 Packaging

The silicon needs to be protected from environmental influences like moisture, mechanical vibrations, etc., to prevent damage or behavioral changes. Therefore, the die is encapsulated in a package with interfaces that are accessible from outside. The chip was sealed into two different packages to have more flexibility during evaluation; a 40-pin Ceramic Dual In-Line package ($CDIL40$) as well as a 32-pin Heat-sink Very-thin Quad Flat-pack No-leads ($HVQFN32$) package. The $CDIL40$ package was chosen, to have the possibility to open it for probing on silicon. In case of chip malfunction it could be necessary to access some internal signals to find the cause for a possible wrong behavior. With this package it is also possible to bond all available pins, including the charge pump reference voltage. The $HVQFN32$ package is much smaller than the other one, therefore, it was chosen for customer demonstration PCBs. Since this package has one pin less than the chip has pads, the $vref\_cp$

pin was not bonded. With these two different setups it could also be verified if bond wire and package pin have an influence on the charge pump behavior.

Figure 5.12 shows the bonding diagram and the pin positions of the *HVQFN*32 package.

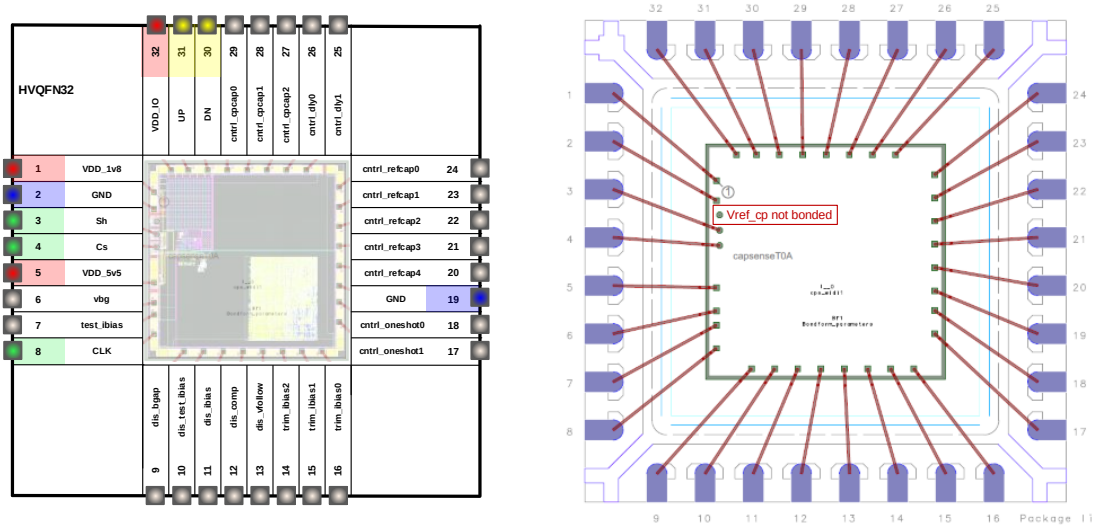

Figure 5.12: Pin positions and **wi**ring **di**agram (WIDI) for *HVQFN*32 package

In figure 5.13 the wiring diagram and the pin positions of the *CDIL*40 package are shown.

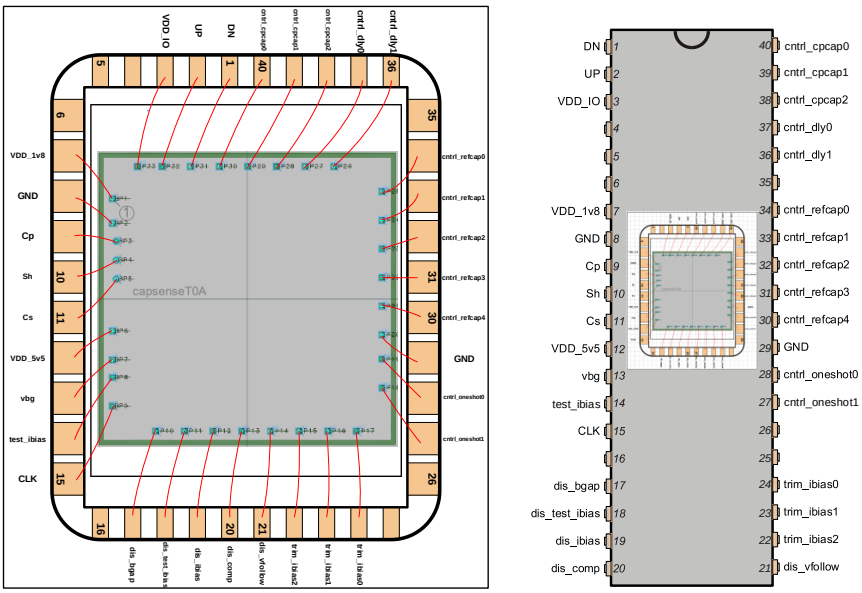

Figure 5.13: Pin positions and wiring diagram (WIDI) for *CDIL*40 package

6 Validation

6.1 PCB Design

6.1.1 Evaluation Board

To test, configure and record the output signals of the manufactured chip, a dedicated evaluation PCB (printed circuit board) was devised. The PCB was designed in such a way that it is possible to to control and monitor the input and output signals of the chip via a PXI (PCI eXtensions for Instrumentation) system. PXI is a PC-based platform from National Instruments for testing, measuring and controlling signals. Requirements for the PCB include the possibility to control the chip via an NXP internal evaluation system called Test Station and via an Altera FPGA (Field Programmable Gate Array). Secondly, it should be possible to test the chip without a digital circuit and to set all control signals via jumpers. Thirdly, every voltage domain should be supplied separately to be able to measure the current consumption per domain. Moreover, it should be possible to apply the clock signal to the chip via a function generator. Lastly, outputs should be provided for the up and down pulses so that they can be observed by means of an oscilloscope.

In figure 6.1 the schematic of the evaluation board is shown and in figure 6.2 the finished board can be seen.

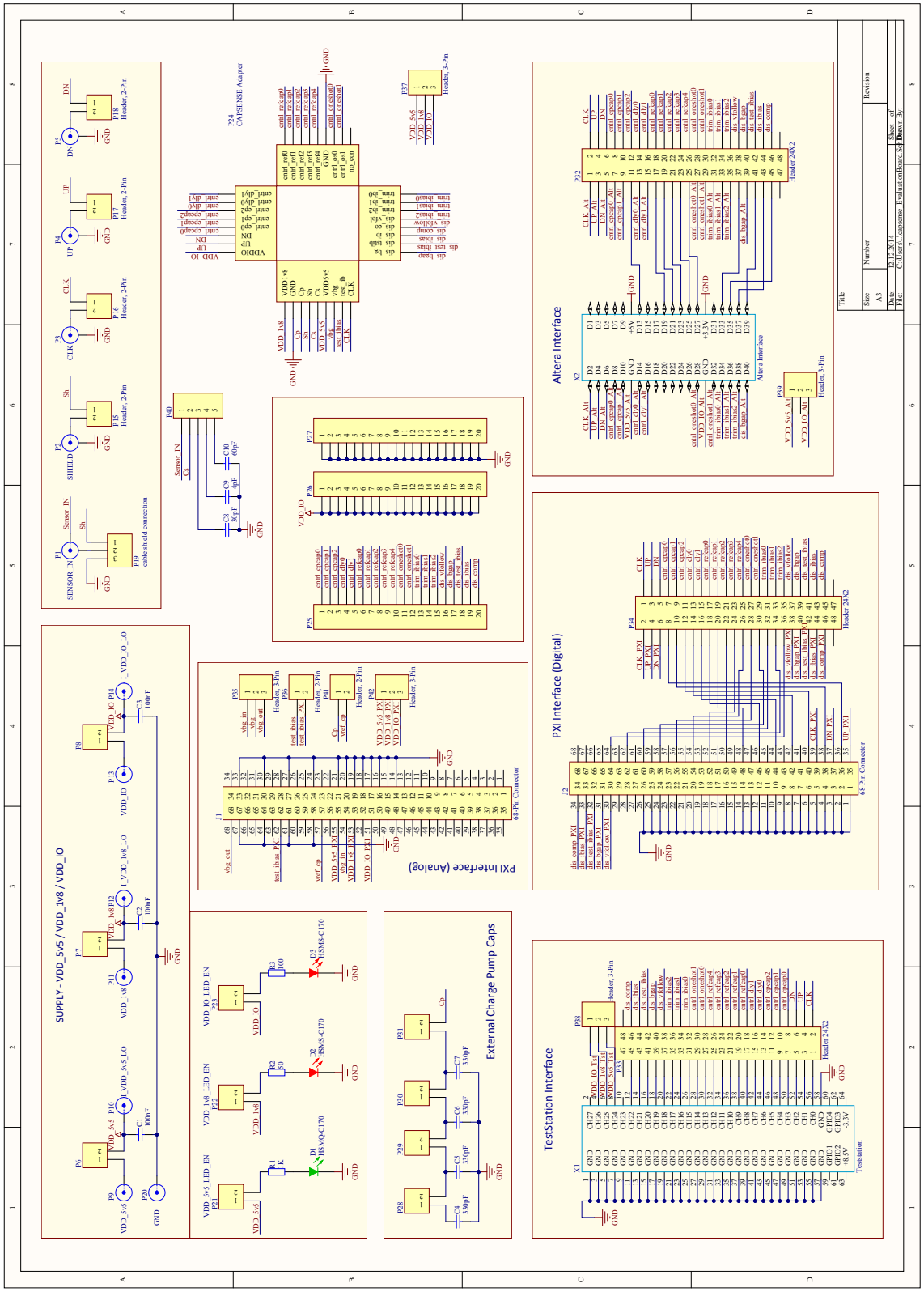

Figure 6.1: Evaluation board schematic

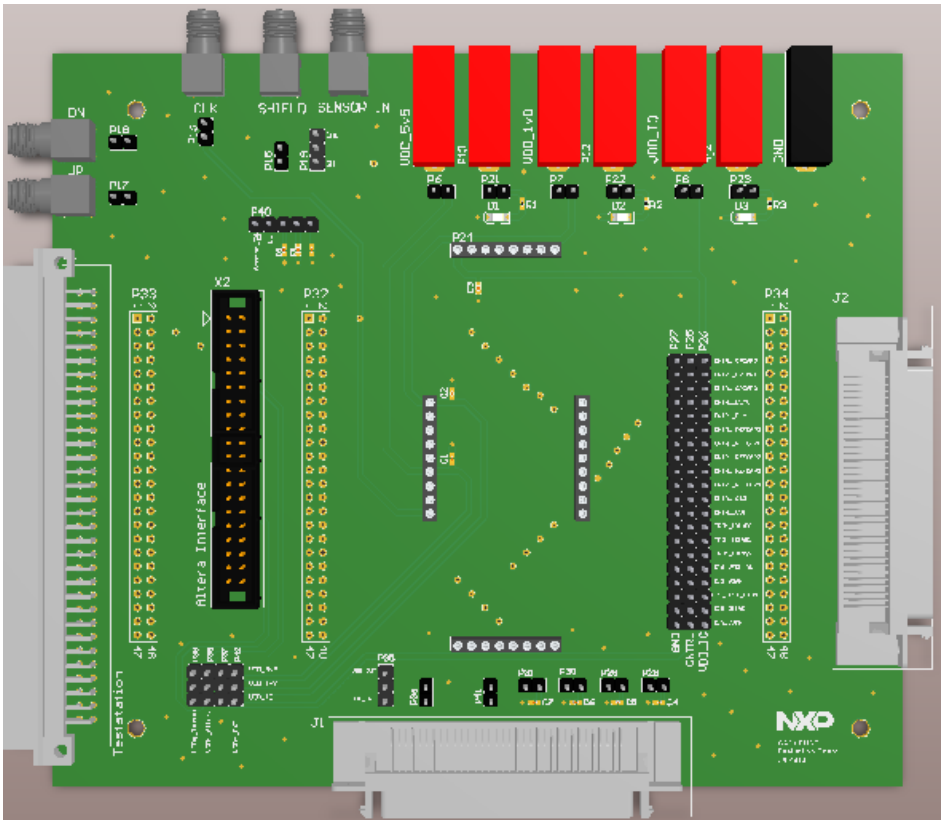

Figure 6.2: Evaluation board

Another requirement was to design the board in such a way that it can be easily used for both the $CDIL40$ package as well as the $HVQFN32$ package without having to resolder, thus eliminating the possibility of destroying or damaging the board.

6.1.2 Sensor Plates

Sensor plates are needed as an interface between the chip and an approaching hand, in order for the chip to be able to detect the hand. A sensor plate has a certain capacitance to ground. A hand that approaches the sensor area causes a capacitance change, which should be detected by the chip. In figure 2.4 in chapter 2 this principle of the hand - sensor interaction is shown.

When first measuring if the chip is working properly, it is important to find out the correct adjustments for the control settings in order to see the expected output signal. At first, sensor plates with different shapes were used where the exact capacitance was not known. The approximate capacitance, which was between 2 pF and 10 pF, was calculated by hand on the basis of the area of the sensor plates and the estimated ϵ_R from the manufacturer. The sensor plate layout is shown in figure 6.3

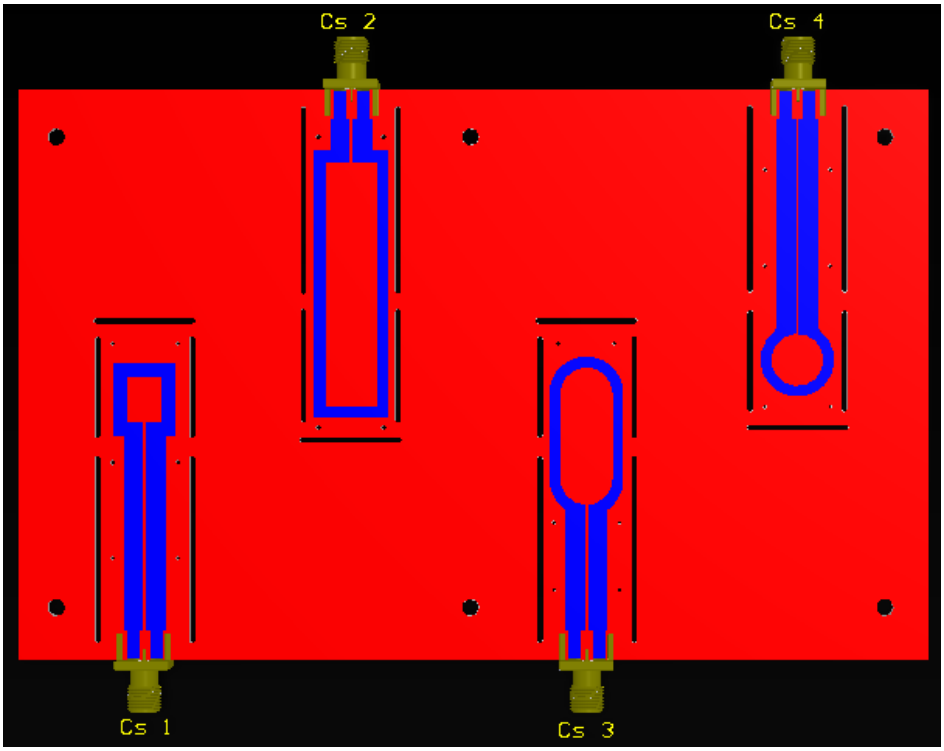

Figure 6.3: Layout of sensor plates

In table 6.1 the capacitance of the sensors in figure 6.3 are shown. The calculated values correspond to the addition of 1.32 pF, which is the capacitance of an SMA (SubMiniature version A) connector, to the simulated values. It can be seen that after adding the offset, the simulations and measurements match very well.

	Simulated	Calculated	Measured
Cs1	4.001 pF	5.321 pF	
Cs2	13.79 pF	15.11 pF	
Cs3	8.354 pF	9.674 pF	9.66 pF
Cs4	4.448 pF	5.768 pF	5.74 pF

Table 6.1: Sensor plate capacitance

The sensor plate, which is shown in figure 6.4, was made for the chip measurements. The area in the center is the sensor area, the regions on the left and right are connected to GND. Two versions of this sensor plate were made, one with an additional GND-area on the bottom side (Cs_5) of the plate and one without the GND-plane on the bottom (Cs_6).

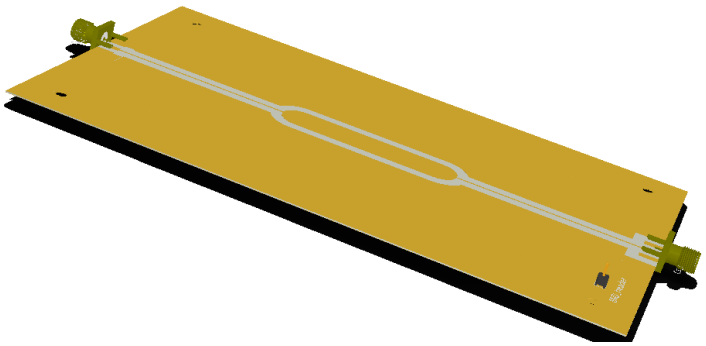

Figure 6.4: Sensor plate

As a first indication for the setting of the reference capacitance, the capacitance of the sensor area towards the GND-plane on the bottom was calculated. The ground areas on the left and right were not considered in this rough estimation.

$$C = \frac{\epsilon_0 \cdot \epsilon_r \cdot A}{d} = \frac{8.8542 \cdot 10^{-12} \frac{As}{Vm} \cdot 4.4 \cdot 478.5\, mm^2}{1.5\, mm} = 12.4\, pF \tag{6.1}$$

- C . . . Capacitance
- ϵ_0 ... vacuum permittivity $8.8542 \cdot 10^{-12} \frac{As}{Vm}$
- ϵ_R ... relative permittivity
- A ... sensor area
- d ... distance between sensor plate and GND

The sensor plate was connected to the sensor input and the internal reference capacitance was set approximately to the value calculated above. However, up and down pulses at the output did not occur as expected. If the reference and sensor capacitance are set to the same value, the system should be in equilibrium. This means that the up and down pulses should occur alternatingly. To reach this state, the reference capacitor had to be set to 40 pF, a value which is about 30 pF higher than that of the calculated sensor capacitance. It was therefore assumed that the sensor plate had a different value than calculated and/or the connection between the sensor input and the chip input on the PCB had an unexpectedly high capacitance. To find out the reason for this difference, the exact value of the sensor plate was determined and the PCB was further investigated.

To determine the capacitance of the sensor input line, measurements with an LCR meter were made. Furthermore, this part of the PCB was extracted and simulated with Momentum to confirm the measurement results. Momentum is a 3D planar electromagnetic simulator integrated into Agilent Advanced Design System (ADS) software. The setup, which was used for the Momentum simulations, is shown in figure 6.5 and figure 6.6.

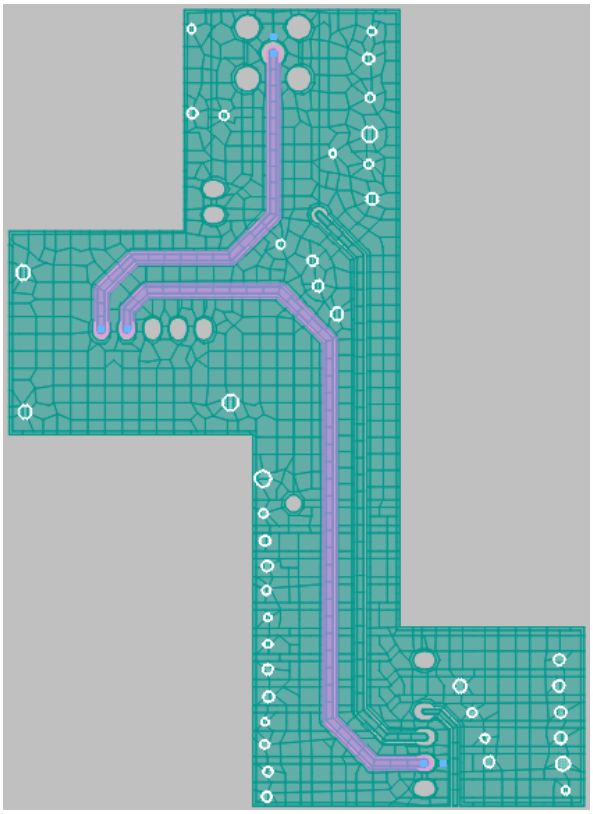

Figure 6.5: Extracted sensor input line on the evaluation board used for Momentum simulations

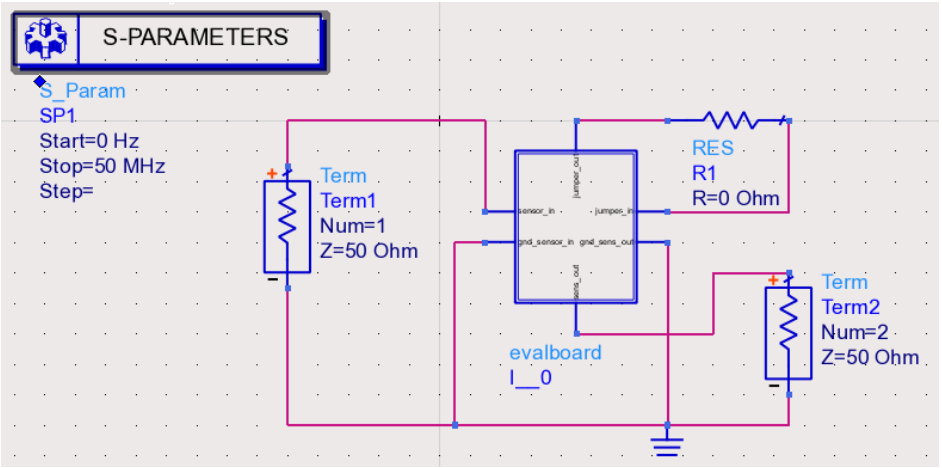

Figure 6.6: Schematic for the Momentum simulation of the sensor input line

The results show that the capacitance between the sensor input line and ground is 30 pF, and the capacitance between the sensor input and the shield line is 14 pF. The latter does not influence the system because both the sensor input and the shield line are connected to the same signal. In table 6.2 the LCR measurement results are shown. The result of the Momentum simulation is shown in figure 6.7. The frequency dependence of the capacitance

value stems from the fact that the impedance (Z-matrix) is calculated as a function of the frequency from the S-parameters, but only in the DC limit, the Z12 (imaginary part) corresponds to the capacitance of the line. For higher frequencies, the Z12 will get an inductance (mutual) component, and it cannot be considered anymore as a single capacitance value.

	no Jumper	P40 on Sensor_*in* P19 on Sh	P19 on GND	P40 open P19 on Sh	P19 on GND
kein Adapter	4.647 pF	13.494 pF	30.337 pF	7.293 pF	12.019 pF
CDIL40	4.634 pF	15.388 pF	33.34 pF	7.53 pF	12.017 pF
HVQFN32		14.717 pF	32.54 pF		

Table 6.2: Capacitance of the sensor input line on the evaluation board

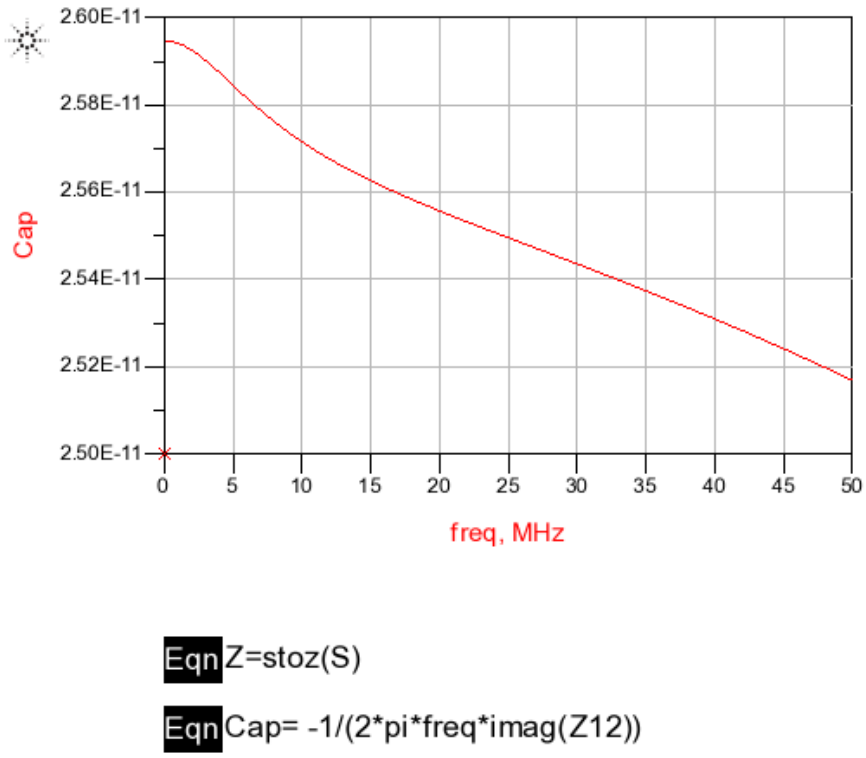

Figure 6.7: Result of the Momentum simulation of the sensor input line

To compare the results of the sensitivity measurement of the *Proxysense* chip with the schematic simulation results, the capacitance change at an approximation was also measured with an LCR meter. Furthermore, Momentum simulations were done to confirm that the simulation results are correct and to ensure for the future development of sensor plates that Momentum simulation is reliable.

The results of the approach measurements were used to figure out the capacitance change

per distance. These findings were used as input for the schematic simulations. Thus, the measurement results could be compared with the simulation results under the same conditions. In figure 6.8 the Momentum simulation configuration of the sensor plate and the approaching plate, representing an approaching hand, are shown. Figure 6.9 shows the corresponding layer stack.

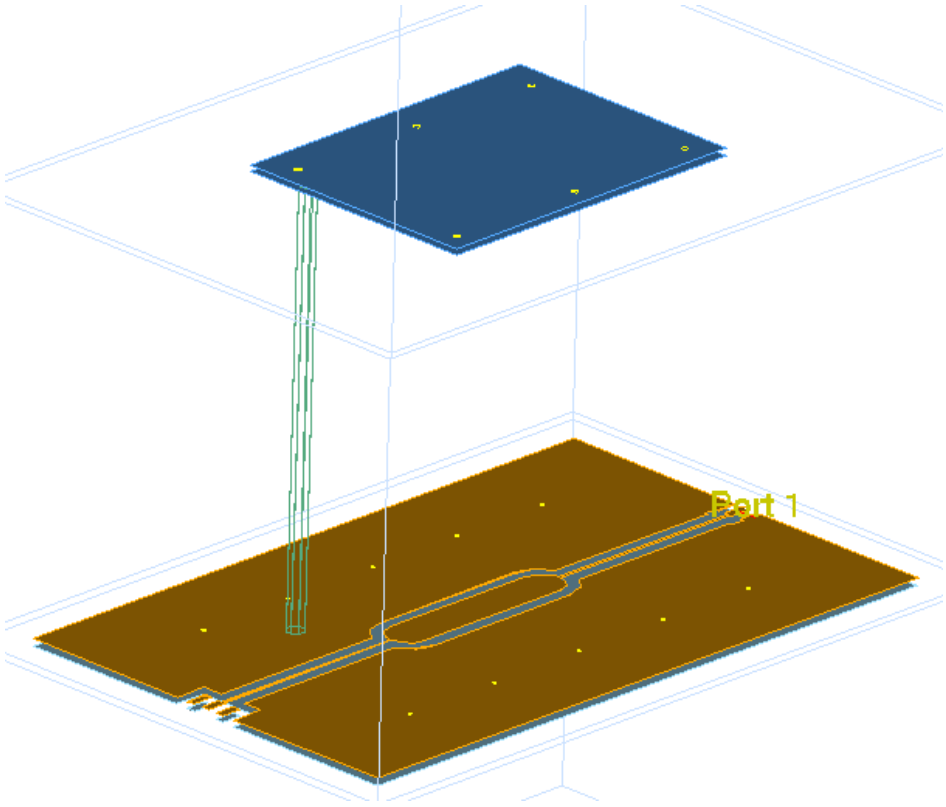

Figure 6.8: Momentum simulation configuration of the sensor plate and the approaching plate

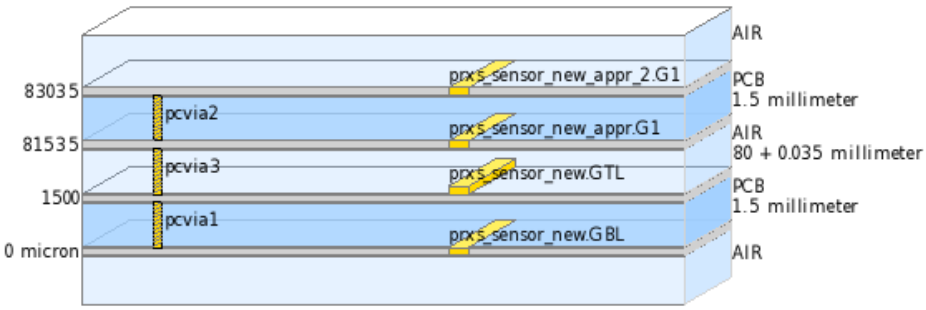

Figure 6.9: Layer stack for approach simulations with Momentum

Figure 6.10 shows a comparison of the Momentum simulation results and measurements with the LCR meter, which were conducted on sensor plate *Cs_5*.

Although the curve shape is the same, there is a small difference between Momentum

simulation results and measurements with the LCR meter. This difference can be caused by the permittivity of the sensor plate that was used in the simulation, whose real value does not correspond exactly to manufacturer claims. On top of that, in the simulation the SMA connector on the sensor plate board, which has a capacitance of 1.32 pF according to measurements, was not considered.

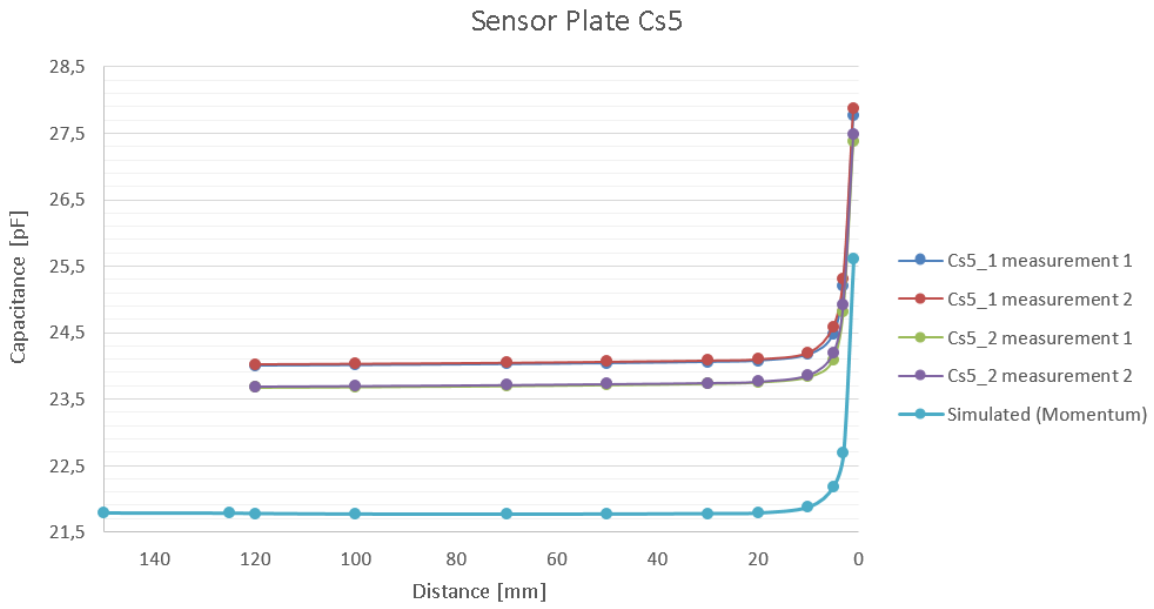

Figure 6.10: Comparison between capacitance measurements and Momentum simulation results of the sensor plate Cs_5

Because of this strong correlation, Momentum simulations can be used for the future development of new sensor structures to determine the expected capacitance value and the capacitance change at an approach. Thus, costs for building prototypes can be reduced.

Because the sensor input line of the evaluation board already has a rather high capacitance on its own, the sensor plate *Cs_6* (8.3 pF) was used for further measurements. With this plate and the sensor input line, the midpoint of the input capacitance range (4 pF to 60 pF) was reached. The measurement results are described in section 6.3.

To be able to do measurements with a lower sensor capacitance, the evaluation board was redesigned. In the new design the connection from the sensor input connector to the chip input is much shorter and is shielded coaxially. Due to this measure a capacitance of 10 pF, which is two-thirds smaller than before, was achieved. The measurement results showed, as expected, that a higher sensitivity could be achieved. To reduce the supply voltage noise,

voltage regulators were added for all three voltage domains. In figure 6.11 the redesigned evaluation board is shown.

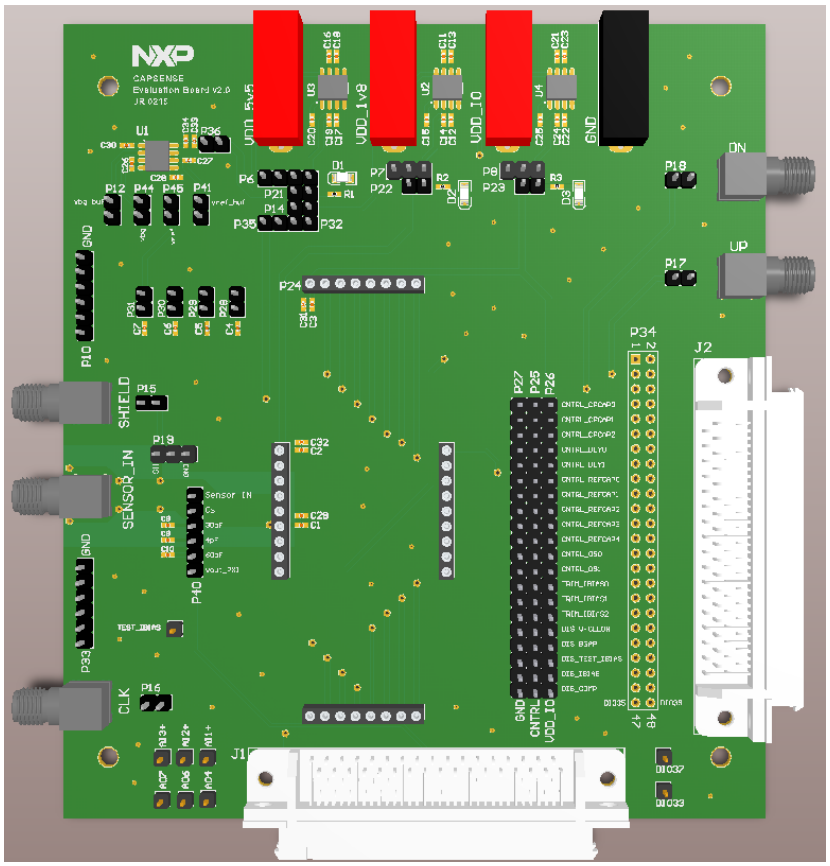

Figure 6.11: Evaluation board version 2

6.1.3 Demonstration Board

In order to show the functionality of the chip to potential customers, a demonstration board was developed. The board was designed with an area of 100 mm × 15.5 mm to be able to fit into a car door handle. To control the *Proxysense*, the micro controller of another chip from NXP Semiconductors (*NCF*2971) was used. The board is supplied with 5 V, and two LDOs are used to get the voltage levels for the other power domains (3 V and 1.8 V). In figure 6.12 the schematic of the demonstration board is shown.

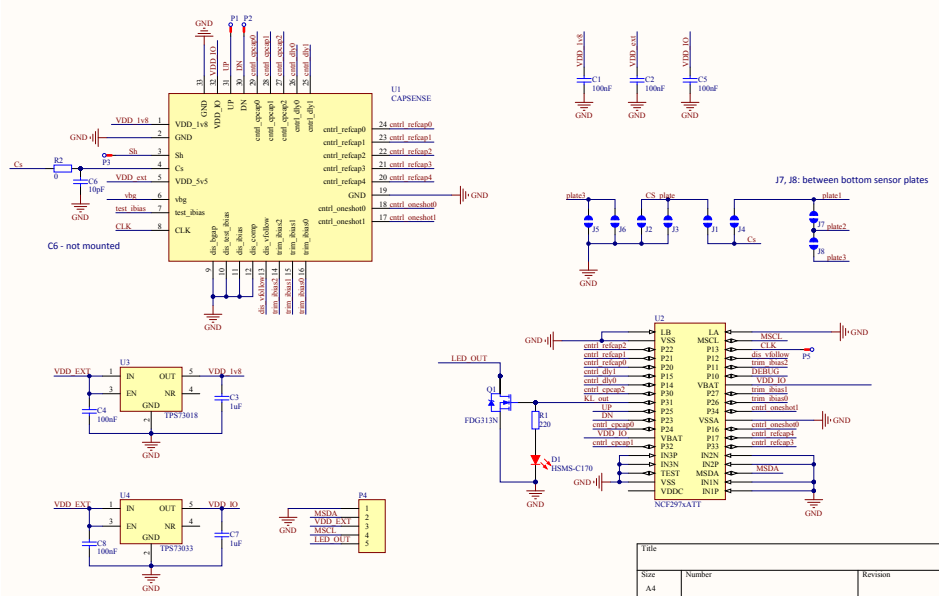

Figure 6.12: Schematic of demonstration board

As shown in figure 6.13 the sensor plate was directly integrated on the board. Thus a smaller sensor capacitance than with the evaluation board could be achieved and the connection between the chip input pin and the sensor plate has no influence on the capacitance.

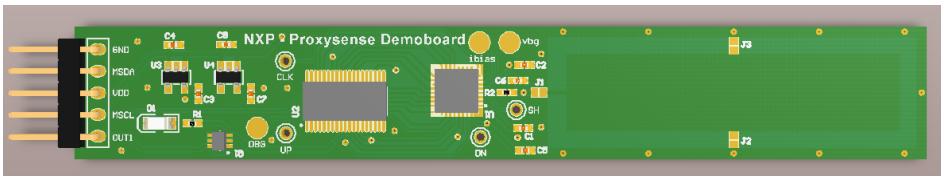

Figure 6.13: Top side of demonstration board with a sensor area of 39 mm × 9 mm (≈ 8.8 pF)

To still have some flexibility with the sensor input capacitance, three smaller sensor areas have been drawn on the bottom side of the demonstration board. These areas can be connected or disconnected via solder jumpers to allow for a change of the sensor area.

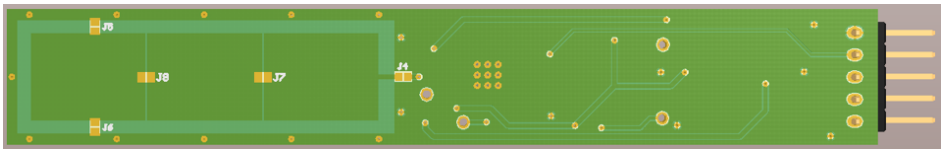

Figure 6.14: Bottom side of demonstration board;
Possibility to adapt sensor area in three steps (3.2 pF, 6.4 pF, 9.6 pF)

This demonstration board was also used to make a rough comparison between the already existing NXP solution (*PCA8886*) and the *Proxysense* chip, which has been developed in

the course of this thesis. The demonstration board *OM*11052 [24], which has approximately the same sensor area, was used to measure the *PCA*8886.

Figure 6.15 shows the results of the sensitivity measurement on both boards with different approaching speeds and distances to the sensor. Cells marked in green show that the approaching object, in this case a simple metal plate, was detected. Cells marked in yellow show the settings that only led to an infrequent detection, and those marked in red show that the object was not detected. This detection matrix clearly shows that the *Proxysense* achieves better results than the *PCA*8886, despite the fact that the lowest sensitivity settings were used due to the leakage in the charge pump capacitors.

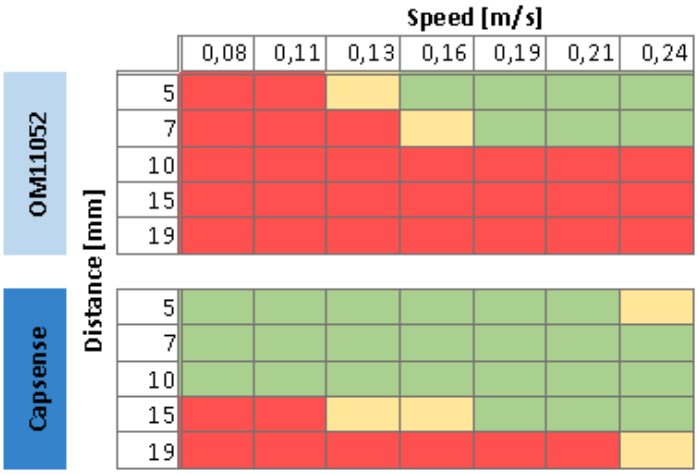

Figure 6.15: Detection matrix comparison between *Proxysense* and *PCA*8886

6.2 Measurement Setup

Figure 6.16 shows a block diagram of the measurement setup.

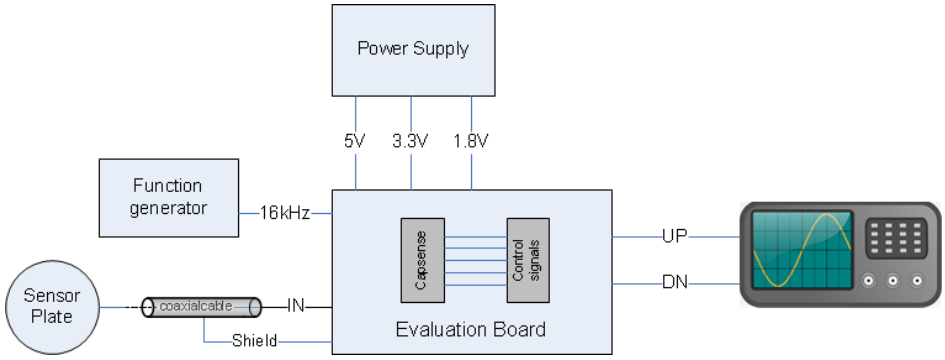

Figure 6.16: Block diagram of measurement setup

After the first measurements it was seen that the measurement results were not completely repeatable. Therefore, a setup configuration was chosen where all parts (PCB, robot arm with approaching plate, ...) were mounted on a wooden plate in order to have the exact same configuration and exactly the same approaching distance. Figure 6.17 shows a picture of the measurement setup in the lab. To mimic an approximation, a small double sided FR4 PCB board (80 mm $\times$ 60 mm) with a copper coating on both sides was mounted on a robot arm. The robot arm was driven by a DC motor. The approximation speed was controlled by supplying the motor with different voltages between 3 V and 15 V. Thus, approaching speeds between 23 $\frac{mm}{s}$ and 405 $\frac{mm}{s}$ were achieved.

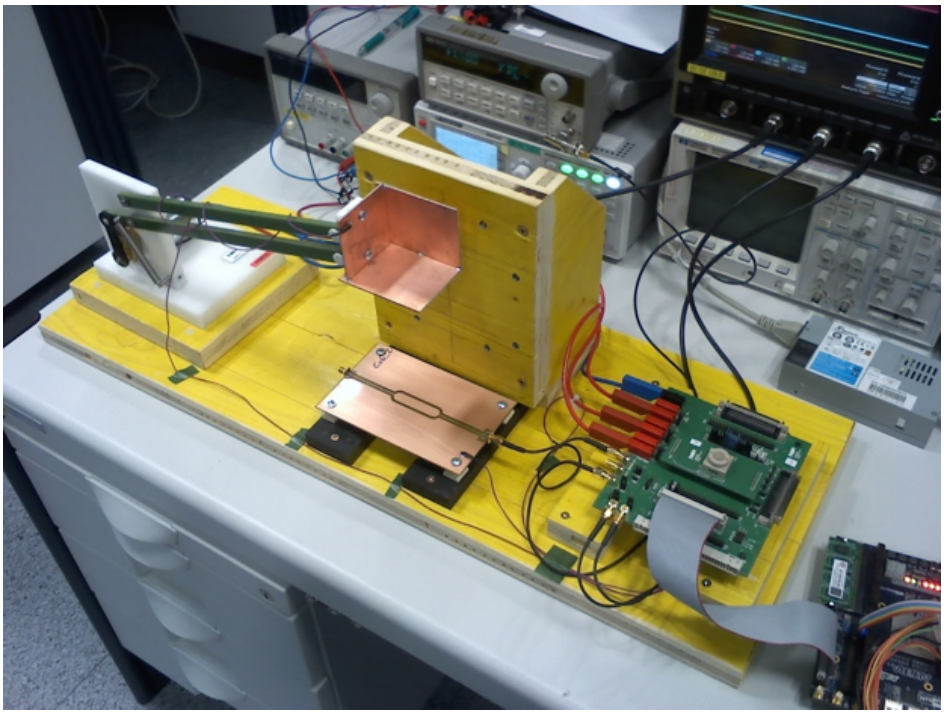

Figure 6.17: Photo of measurement setup

At the first functional test, the goal was to find proper control settings to see the expected output signals. This was not an easy task in the beginning, since the sensor plate capacitance values were not known and some of the control signals also influence other parameters.

After the first measurements with manually set control bits to prove the functionality of the chip, a dedicated LabVIEW VI (virtual instrument) was created (see figure 6.18). In this way it was possible to conduct automated measurement, record up and down pulses and monitor the current consumption of the system.

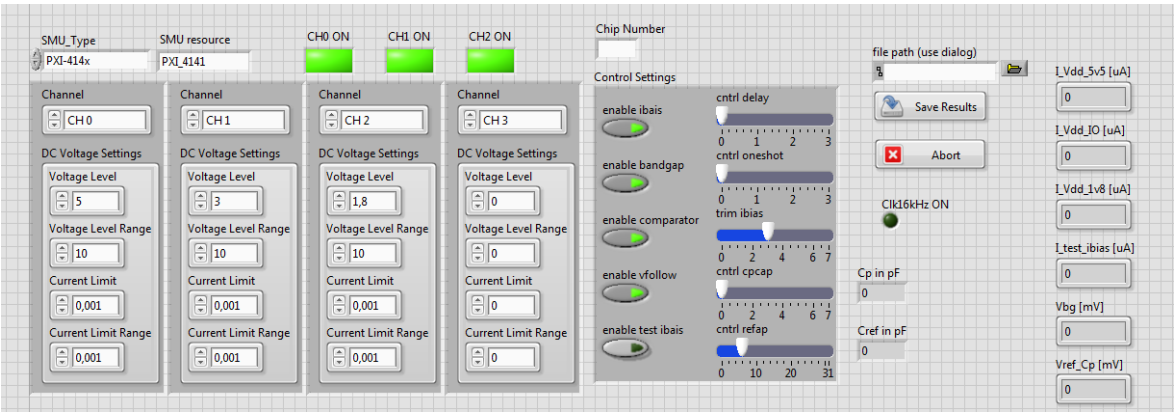

Figure 6.18: LabVIEW control VI

6.3 Measurement Results

6.3.1 DC Measurements

The DC measurement results compared to the simulated values are shown in table 6.3.

Sample	*bias trim*	I_Vdd5v5	I_VddIO (3 V)	I_VddIO (3.3 V)	I_Vdd1v8	*vbg*
13	0	20.26 µA	140.5 nA	1.94 µA	3.11 µA	896.62 mV
14	0	21.15 µA	43.6 nA	1.83 µA	3.07 µA	901.52 mV
15	0	19.87 µA	144.4 nA	1.92 µA	3.07 µA	902.74 mV
13	3	20.46 µA	142.4 nA	1.94 µA	3.99 µA	896.94 mV
14	3	21.17 µA	31.7 nA	1.83 µA	3.93 µA	901.52 mV
15	3	20.08 µA	144.4 nA	1.92 µA	3.93 µA	902.74 mV
13	7	23.83 µA	100.9 nA	1.89 µA	5.40 µA	896.63 mV
14	7	24.26 µA	31.7 nA	1.79 µA	5.34 µA	901.52 mV
15	7	23.15 µA	102.9 nA	1.89 µA	5.35 µA	902.74 mV
sim.	3	17.94 µA	149.9 nA	2.12 µA	4.42 µA	923.5 mV
sim.	7	21.7 µA	173.9 nA	2.14 µA	5.85 µA	923.5 mV

Table 6.3: DC measurement results:
test_ibias disabled, $cntrl\_cpcap = 0$, $cntrl\_dly = 0$, $cntrl\_refcap = 17$, $cntrl\_os = 1$, $Cs = 30$ pF, board 2, $Vdd\_5v5 = 5$ V, $Vdd\_1v8 = 1.8$ V

The results of the first measurement of current consumption and bandgap reference voltage as well as for the basic system behavior was for most parameters as expected after simulations.

The current consumption of the separate blocks was estimated via delta measurements.

comp.	*vfollow*	*bgap*	*bias block*	*test_ibias*	*I_Vdd5v5*	*I_VddIO*	*I_Vdd1v8*
en	*en*	*en*	*en*	*en*	20.075 µA	1.922 µA	4.828 µA
en	*en*	*en*	*en*	*dis*	20.076 µA	1.938 µA	3.925 µA
dis	*en*	*en*	*en*	*dis*	17.401 µA	282.51 nA	2.148 µA
dis	*dis*	*en*	*en*	*dis*	64.355 µA	290.412 nA	2.150 µA
dis	*dis*	*dis*	*en*	*dis*	64.312 µA	282.506 nA	1.202 µA
dis	*dis*	*dis*	*dis*	*dis*	−37.264 nA	290.412 nA	66.92 nA
dis	*en*	*dis*	*en*	*dis*	17.399 µA	292.388 nA	1.196 µA

Table 6.4: DC measurement results:
trim_ibias = 3, *cntrl_cpcap* = 0, *cntrl_refcap* = 17, *cntrl_dly* = 0, *cntrl_os*=1,
Cs = 30 pF, *Vdd_5v5* = 5 V, *Vdd_IO* = 3.3 V, *Vdd_1v8* = 1.8 V, *sample* = 15

Figure 6.19 shows the current measured on the *test_ibias* pin. The current was recorded at a voltage between 0 V and 1.8 V, for all trim settings. This current is copied from the bias block to the test output via a current mirror. By multiplying this current by five, one gets the current for discharging the sensor and the reference capacitors.

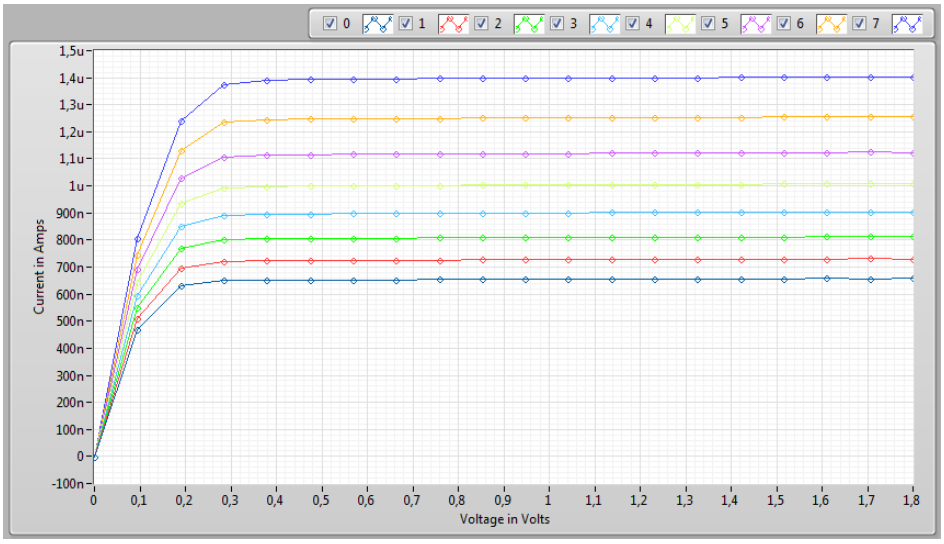

Figure 6.19: Current measured on *test_ibias* pin with all trim settings

In figure 6.20 the discharge curve of the sensor capacitor is shown. The green curve is recorded on the sensor input pin (Cs) and the yellow curve on the shield pin (Sh). Cs is connected to Sh via the voltage follower. It can be seen that the voltage follower works as expected.

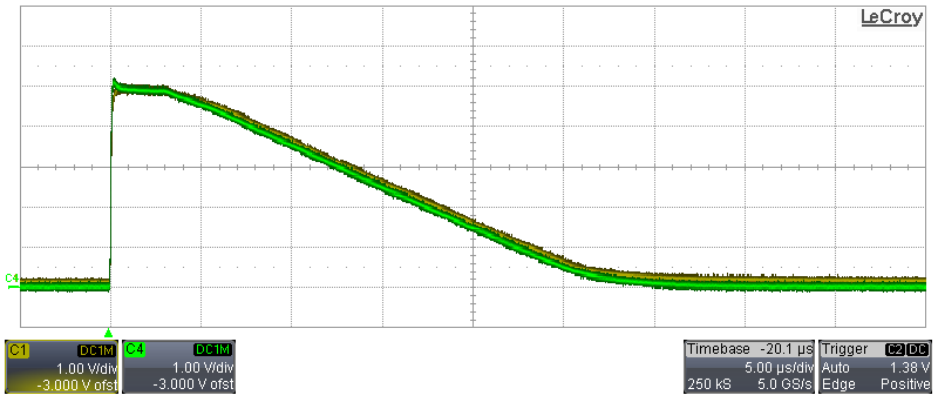

Figure 6.20: Sensor input and shield voltage, Channel 1: Sh, Channel 4: Cs

Figure 6.21 shows the discharge curve of the sensor capacitor with sensor plate *Cs_6* connected to the input. Assuming that the discharge current is 5 μA, the sensor capacitance, including the connection line and the connector, can be determined via the slope of the curve:

$$Cs = I \cdot \frac{dt}{dV} = 5\,\mu A \cdot \frac{11.95\,\mu s}{3.86\,V} = 15.5\,pF \tag{6.2}$$

This value correlates quite well with the measured value on the senor plate (8.2 pF) and the connection line on the PCB (9.2 pF). The difference can result from various factors. On the one hand, the delta measurement via the oscilloscope is not very accurate, on the other hand, the LCR meter measurement setup was not stable, hence not exactly the same for different measurements. This measurement was performed to have an indicative value for the setting of the internal reference capacitor.

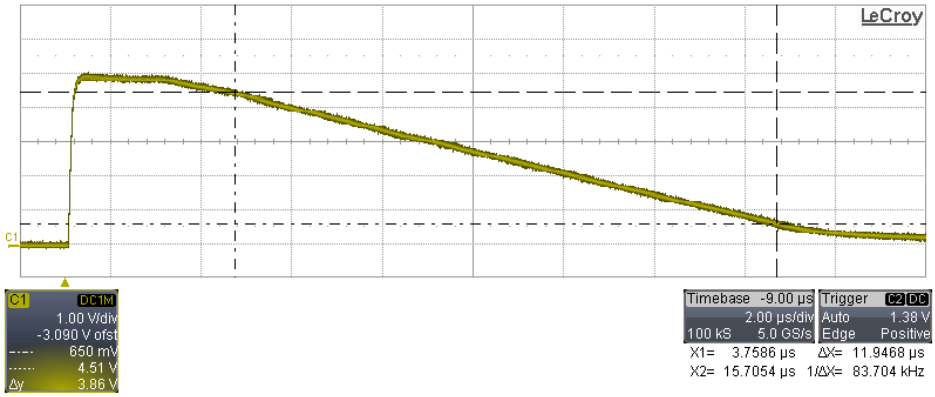

Figure 6.21: Discharge curve of sensor capacitor: Cs connected to sensor plate Cs_6

For the measurements described in the next section, the sensor plate *Cs_6* and the improved version of the evaluation board were used.

6.3.2 Pulse Measurements

With the LabVIEW VI up and down pulses were recorded in form of zeros and ones, since it is difficult to graphically compare an amount of data that is this large. The data did not show a long sequence (64 consecutive pulses); possible reasons for this are described in chapter 7. Therefore, a MATLAB® script was written, which calculates the behavior of the charge pump reference voltage ($vref\_cp$) from the recorded data. The same equations as in chapter 3 were used for that. With these calculations it could be made visible that a capacitance change occured. Also with a filter, for example a moving average filter, a detection can be extracted from the data, but it was not possible to detect an approaching object within 4 ms as required.

Figures 6.22 and 6.23 show the equilibrium state, once using a fixed sensor capacitance of 30 pF on the input and once connecting the sensor plate Cs_6. Here, the signal on channel 2 is the clock signal, the up and down pulses are recorded on channels three and four. It can be seen that by connecting a sensor plate, the system is more sensitive towards environmental influences. Thus, the up and down pulses do not always alternate exactly.

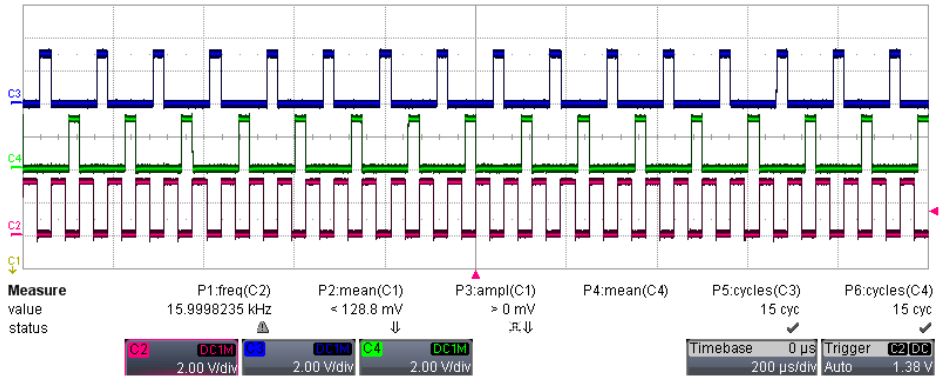

Figure 6.22: Equilibrium when fixed external Capacitor (Cs = 30 pF) is connected

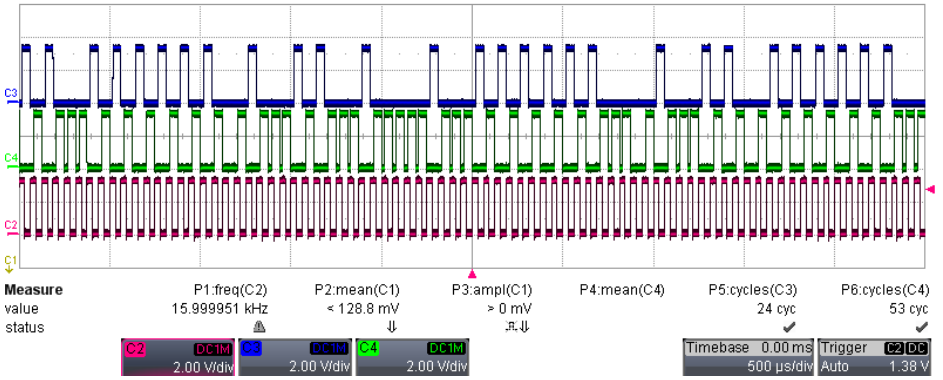

Figure 6.23: Equilibrium when sensor Plate Cs_6 is connected

The following figures show the calculated vref_cp shape of robot arm or hand approaches

while different settings were used.

Figure 6.24 shows a comparison of approaches with the robot arm while using different voltage levels for the motor that operates the robot arm. Here, a higher voltage means also a higher approaching speed. A voltage of 7 V corresponds to a speed of 0.18 $\frac{m}{s}$, whereas a voltage of 3 V leads to a speed of 0.08 $\frac{m}{s}$. It can be seen that the sensitivity increases with a higher speed because the capacitance changes in a shorter time. At a slower change of the sensor capacitance, the system already compensates for it and therefore the change of the reference capacitance is smaller. Thus, very slow changes, for example from dust or changes in the ambient temperature, are compensated for and not falsely detected as a hand approach.

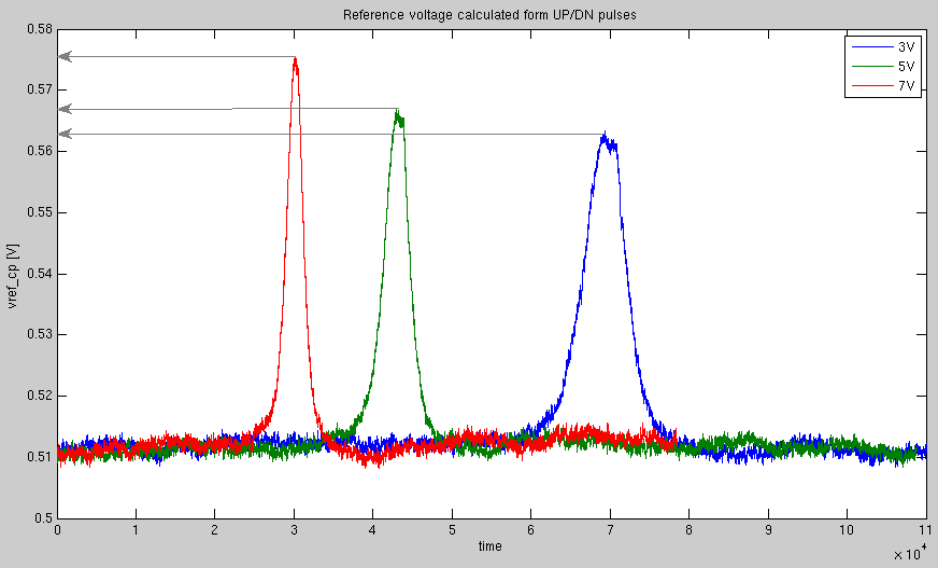

Figure 6.24: Comparison of the charge pump reference voltage between approaches with different robot arm speeds

Figure 6.25 shows a comparison of approaches with the robot arm using different clock frequencies. It can be seen that the clock frequency does not have an impact on the sensitivity.

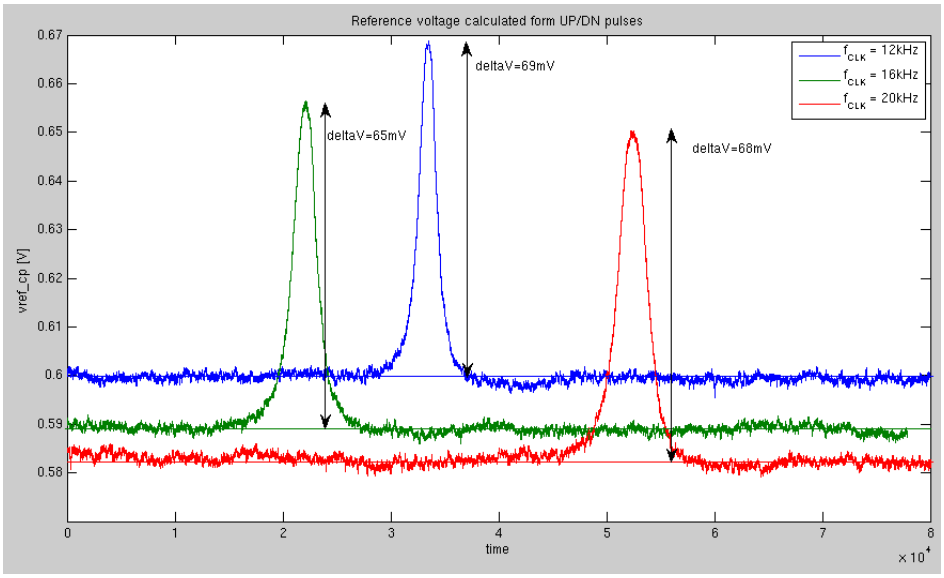

Figure 6.25: Comparison of the charge pump reference voltage between approaches with different clock frequencies

Figure 6.26 shows a comparison of approaches with the robot arm where the distance between the end position of the robot arm and the sensor plate was varied. If the robot arm comes closer to the sensor plate, the capacitance change is bigger. Thus, also the amount of generated up pulses and the change of the reference voltage are higher. It can also be seen that even at a distance of about 2 cm an approach could be detected.

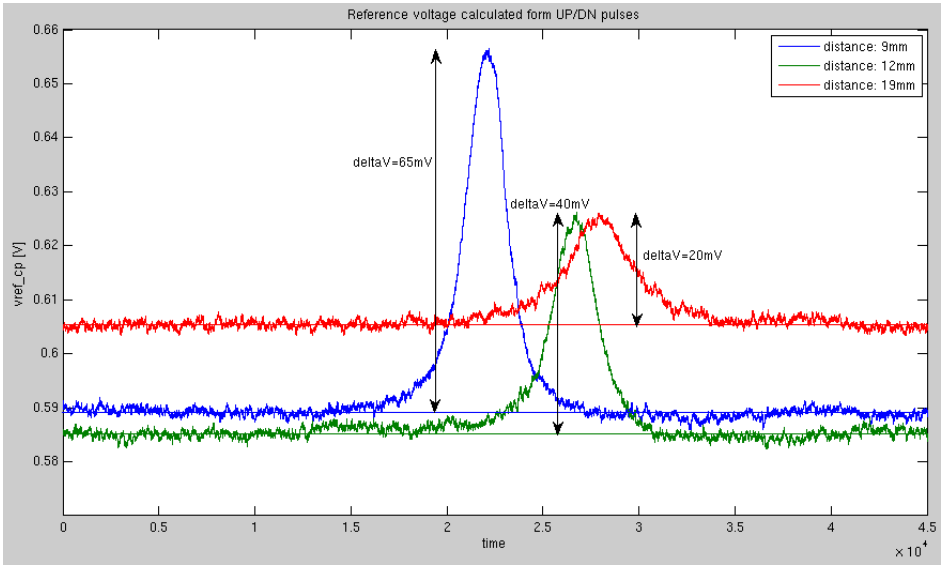

Figure 6.26: Comparison of the charge pump reference voltage between approaches with different distances to the sensor plate

Figure 6.27 shows a comparison of approaches with the robot arm while using different

reference capacitance values. The sensor plate and thus the sensor capacitance have been kept the same for the three measurements. It can be seen that the biggest change of the reference voltage is achieved by using the smallest reference capacitance value. This is the case because if the reference capacitance is smaller than the sensor capacitance, it is discharged faster. Thus, the charge pump reference voltage has to rise to a higher value to reach the equilibrium point where both comparators switch at approximately the same time. If the charge pump reference voltage level is higher than the middle point of the supply voltage ($> 0.9\,\mathrm{V}$), one up-step is smaller and therefore more up-steps are necessary to compensate for the capacitance change at the input.

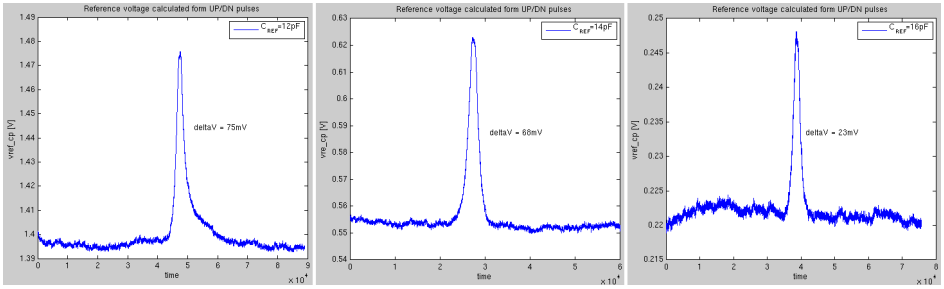

Figure 6.27: Comparison of the charge pump reference voltage between approaches with different reference capacitor settings

Figure 6.28 shows a comparison of approaches with the robot arm between the two different boards and a different sensor capacitance while using the same sensor plate. Here too, the reference capacitance was set accordingly. It can be seen that the sensitivity is smaller when a smaller input capacitance is used because the relative capacitance change caused by the approaching object is higher.

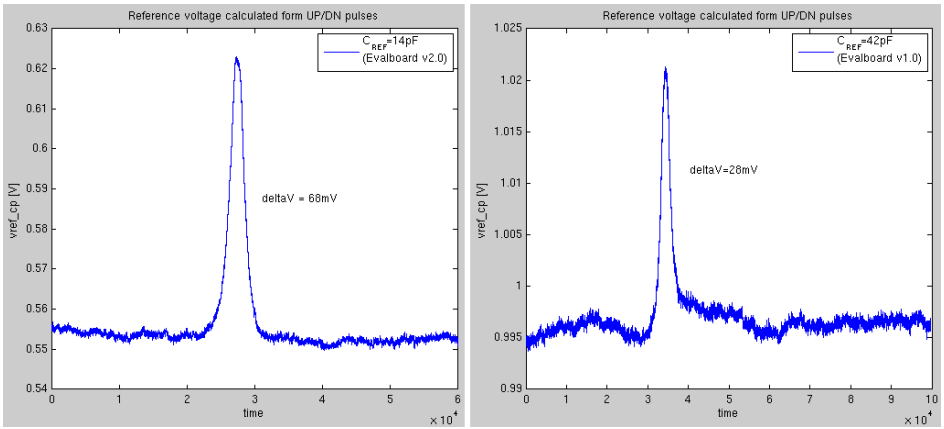

Figure 6.28: Comparison of the charge pump reference voltage between approaches with different boards

In figure 6.29 a comparison of approaches with a human hand is shown. It can be seen that the shape of the curve caused by the hand that approaches and touches the sensor plate looks very similar in the various measurements. The voltage difference is not always the

same because an approach with a real hand can not be repeated as uniformly as with a robot arm. An approximation without touching the plate in the end leads to a similar shape and voltage difference as the approach with the robot arm at about 15 mm distance to the sensor plate.

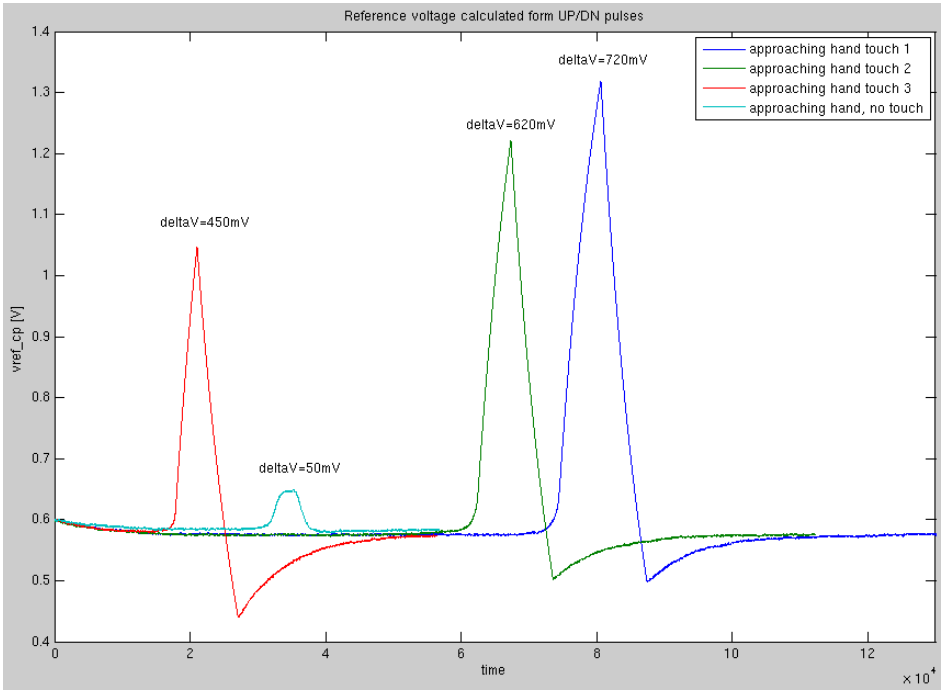

Figure 6.29: Charge pump reference voltage behavior at different hand approaches

6.4 Conclusion

Extensive measurements have shown that parts of the IC behave differently than expected from the simulations. Especially the charge pump behavior was different than in the simulations. If the system is configured in such a way that only up pulses occur, it is expected that the reference voltage reaches a voltage level of 1.8 V at some point. Measurements showed that this voltage level has never been reached, especially not when selecting the largest charge pump capacitor. This behavior could not be reproduced in simulations.

After some investigations it was found that the model of the capacitors that have been used in the charge pump was not correct. The gate leakage of the NMOS capacitors was not modeled in and therefore this ”erroneous” behavior was not seen during extraction and simulation. In chapter 7 this problem will be described in more detail.

It has been shown that the *Proxysense* chip is more sensitive than the already existing *PCA*8886. To reach an even higher sensitivity, the charge pump capacitors on the chip have to be replaced by another version without gate leakage. Furthermore, the focus has to be set on the improvement of the sensor plate layout. It has to be configured in such a way that a

high capacitance change can be achieved also with bigger distances between sensor plates and the approaching hand.

7 Follow-up Considerations

As mentioned above, the behavior of the chip was not exactly as expected. In the measurements a series of 64 or more consecutive up pulses could never be achieved. The maximum of consecutive up pulses was around twenty pulses in a row, and then at least one down pulse occurred in between. In the pre-tapeout simulations this behavior could not be seen. Therefore, the difference between the measurement setup and the simulations had to be investigated and new simulations had to be carried out. The findings thereof are described in the following sections.

7.1 Leakage

One of the blocks that were further investigated was the charge pump. A test bench for the charge pump, where up pulses were applied to it, was set up. In the measurements it could be seen that the reference voltage was not increasing further than about 1.2 V when only up pulses were applied. The same behavior was not experienced in simulations and could not be explained at first. After studying the modeling of the capacitor that has been used, it was discovered that the device has a voltage dependent gate leakage current, which is not included in the device model used in the simulations.

In figure 7.1 the voltage dependence of the leakage current in an NMOS GO1 capacitor can be seen. This graph is based on measurements that were performed by the in-house modeling group. In this case a 100 μm $\times$ 100 μm capacitor was used and it shows a leakage current of about 1 nA at 1.8 V. For this thesis larger capacities have been used and this would mean that a leakage current of about 4 nA to 30 nA, depending on the settings, would occur.

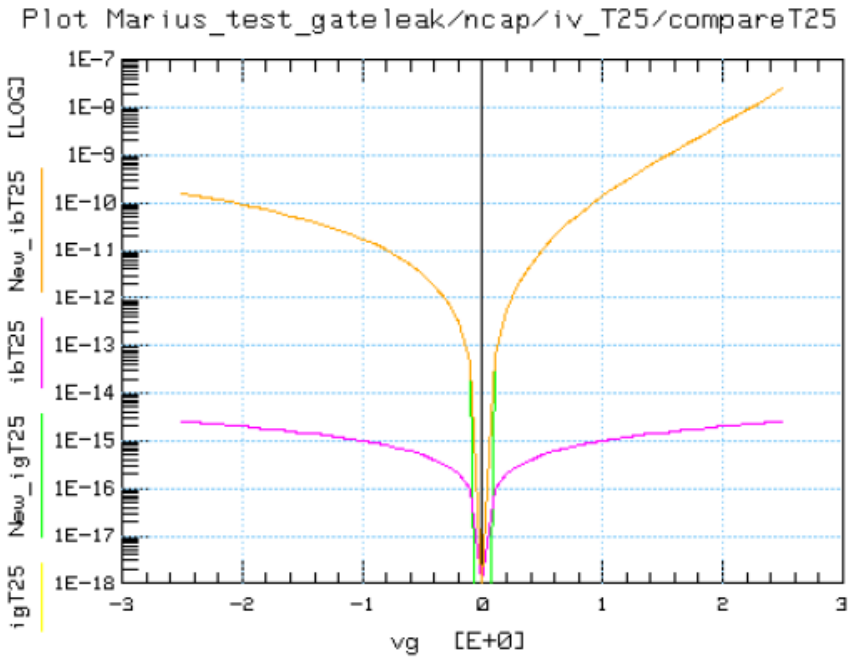

Figure 7.1: Leakage current of NPoly capacitor dependent on voltage level

After new models, which take account of the leakage behavior, were provided by NXPs internal modeling group, simulations were run to confirm that the expected results are achieved now. Figure 7.2 shows the test bench that was used to simulate the behavior of the voltage on the charge pump capacitors; first they were charged to 1.5 V and then the supply was disconnected.

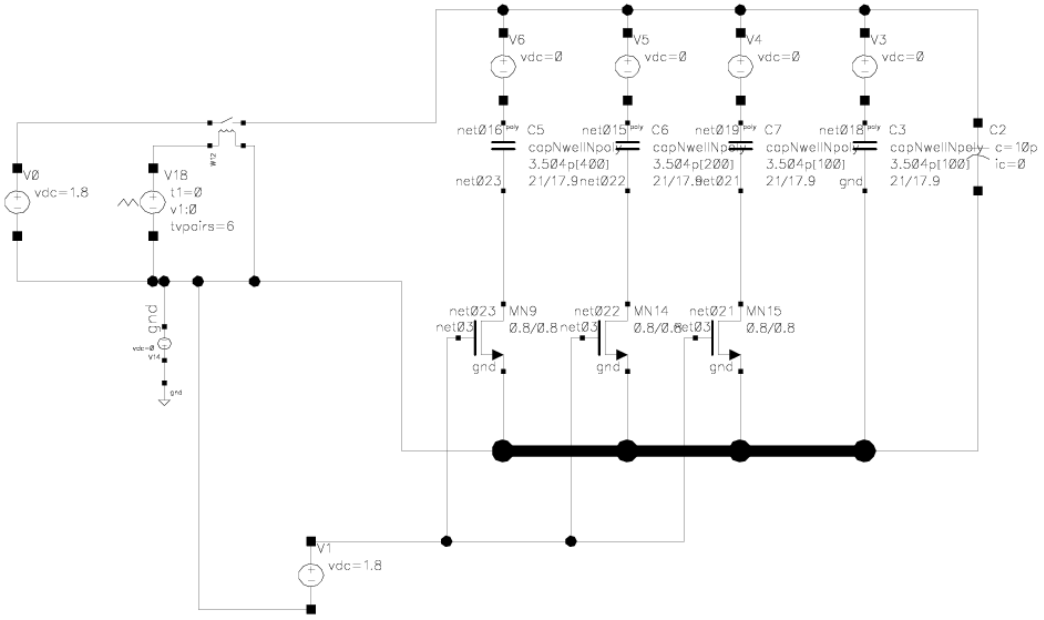

Figure 7.2: Test bench for simulating leakage behavior of charge pump

The simulation and measurement in figure 7.3 show the behavior of the charge pump capacitor after it is charged to 1.5 V and then disconnected from the supply. The old model shows that the charge pump voltage stays at 1.5 V as one would expect from a capacitor without leakage. When the gate leakage current is taken into account in the model, the capacitor discharges to about 180 mV within 20 s. This value matches also quite well with the measurements, where the capacitor is discharging to 240 mV in the same time. The slightly higher voltage in the measurements can be explained with non-leaking parasitic capacitances in the chip and on the board. In the zoomed out section of the voltage curve it is shown that within 62 μs, which is one clock period, the voltage decreases by about 64 μV. This is more than half of the amount that is added by one up pulse. This means that half of the charge that is added by one up pulse is leaking away. Hence, after a hand has approached, more up pulses are necessary to reach an equilibrium state again. This behavior can also be seen later in top level simulations with the new models.

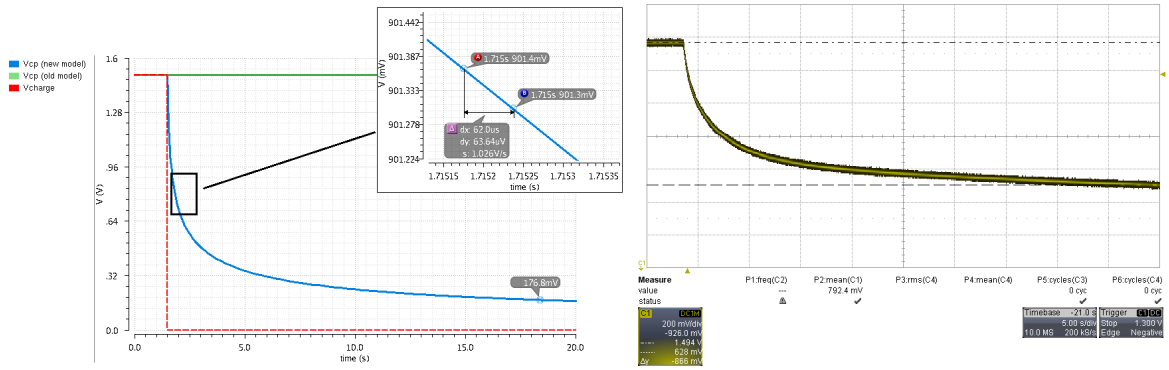

Figure 7.3: Comparison of new model, old model and measurement of voltage behavior on the charge pump capacitance after supply voltage is switched off

The simulation where only up pulses are applied to the charge pump was repeated as well. The comparison of the simulation with the old and new model is shown in figure 7.4. With the old model, where the gate leakage has not been modeled, the voltage rises always up to 1.8 V. With the updated model, depending on the capacitance value, it rises only up to 1.074 V at most.

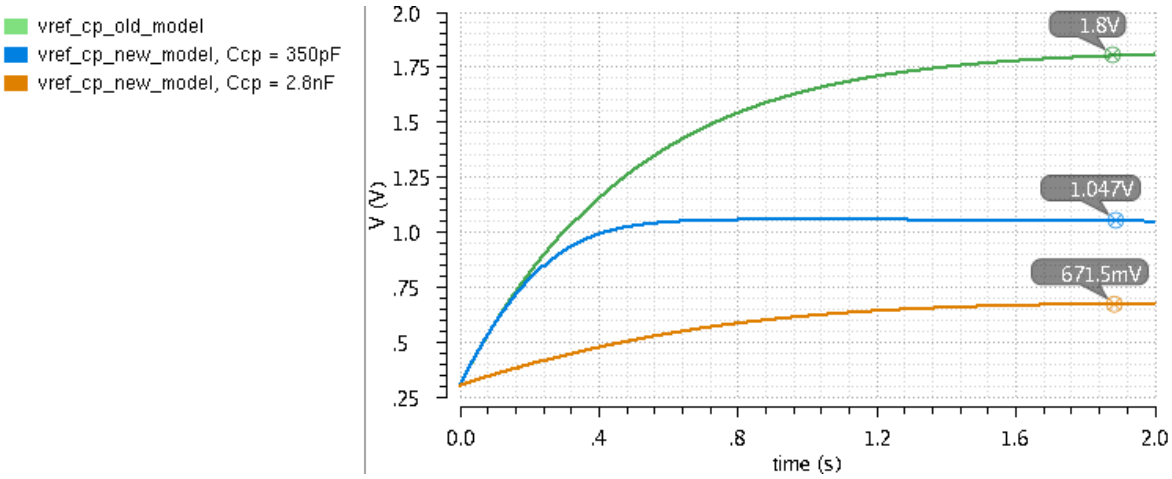

Figure 7.4: Comparison of reference voltage behavior when only up pulses are applied: Leakage model (C_{CP} = 350 pF), leakage model (C_{CP} = 2.8 nF), old model without leakage

To further compare the schematic simulations and the silicon, a measurement and a simulation of the leakage current were carried out for different capacitance values. The results of the simulation are shown in figure 7.5 and the results of the measurement in figure 7.6.

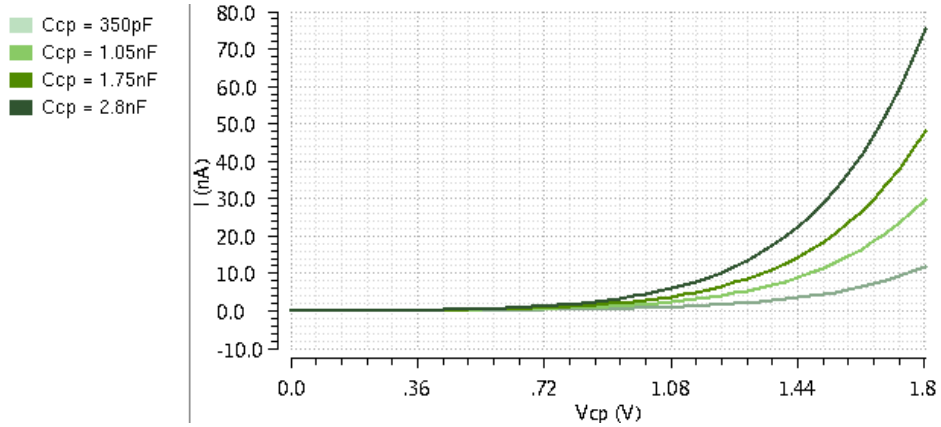

Figure 7.5: Charge pump leakage current (simulated) depending on C_{CP} setting

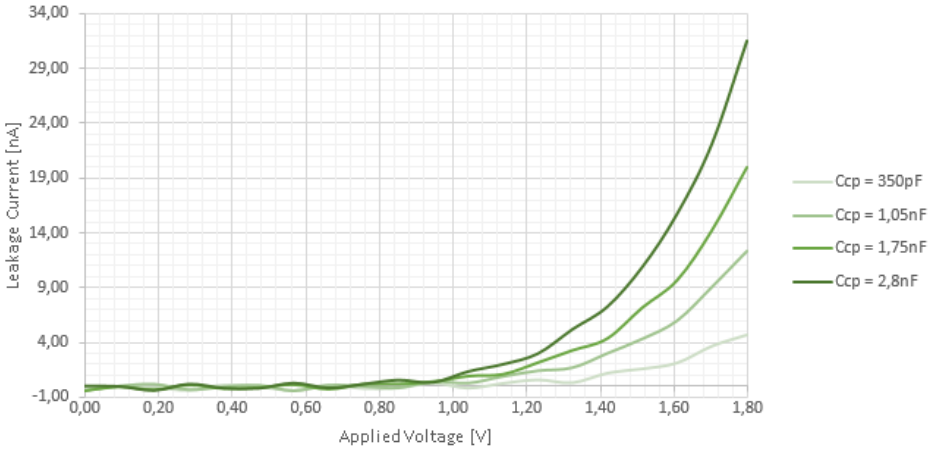

Figure 7.6: Charge pump leakage current (measured) depending on C_{CP} setting

Due to this leakage problem the top level simulations had to be re-run. The simulation results showed that the system should still be functional in case the reference voltage is set to a lower level in the equilibrium state (around 740 mV). This can be achieved by setting the sensor capacitor to a smaller value than the reference capacitor. In this case the leakage does not have a big influence anymore, since the leakage current is dependent on the voltage level. It is also dependent on the capacitor area, which is the dominating factor, therefore the smallest charge pump capacitor has been used for further measurements and simulations.

The first simulations have been run with a fast approach of capacitance, which means that in this case 70 fF where added to the sensor input within one us. This approach was also used to get a result in a reasonable time, because a transient top level simulation of 50 ms takes about tree days. In the simulation result shown in figure 5.9 in chapter 5 it can be seen that the amount of pulses generated in the simulation without leakage match quite well with the expected calculated numbers.

In figure 7.7 the result of the same simulation, using the updated models, is shown. It can

be seen that the amount of up pulses is now even higher than in the simulations with the old models. More up pulses are necessary to reach the same voltage level in the equilibrium state because the charge leaks away.

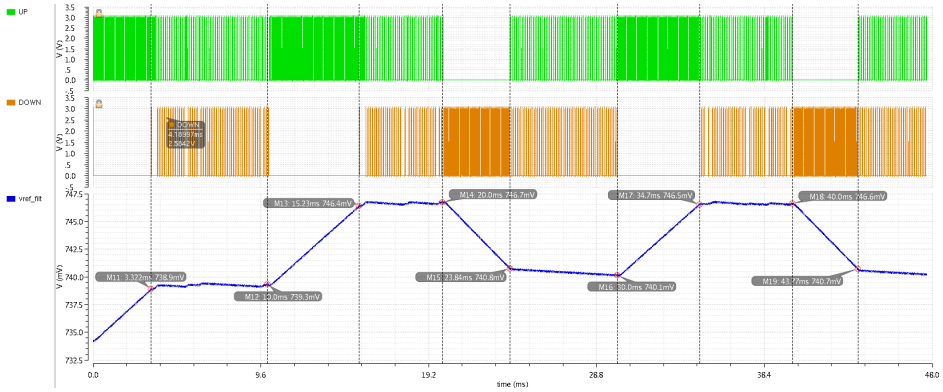

Figure 7.7: Top level simulation with leakage: fast approach, $\Delta C = 70\,\text{fF}$

To overcome the leakage issue, the capacitors could be replaced in the future with GO2 capacitors, which have a thicker gate oxide and thus no gate leakage. The behavior of the GO2 capacitors is the same as in the simulations shown for the old model.

Even having considered the findings mentioned above, it could not be explained why the behavior in the lab was different than in the simulations. Therefore, the noise of the power supplies in the lab were examined more closely and transient noise was added in the simulations. The outcome of this investigation is described in the next section.

7.2 Noise

The measurement setup was analyzed closely and it was seen that noise has not been considered in the simulations. Initially, it was planned to integrate LDOs in the chip, but for reasons of time they were left out in the first version of the test chip. Only decoupling capacitor were added on the VDD_1v8 domain. This means that there is no proper power supply rejection and therefore the noise of the power supply sources in the lab have a direct influence on the circuit behavior. Due to coupling between the supply lines and the reference voltages, the noise can also be seen there. Since the capacitance change caused by an approaching hand is very small, also the change in the discharge curve is very small. Therefore, a noise on the reference voltages can lead to a switching of the comparator at a different time than expected and thus lead to a wrongly generated up or down pulse. Figure 7.8 illustrates how the reference voltage and the sensor input voltage, including noise, could look like. Due to the noise there is a region where the comparator decision is uncertain, and false up or down pulses can be generated. If a smaller sensor capacitor is used, the input voltage will have a steeper slope and the region of uncertainty and therefore also the influence of the noise will be smaller.

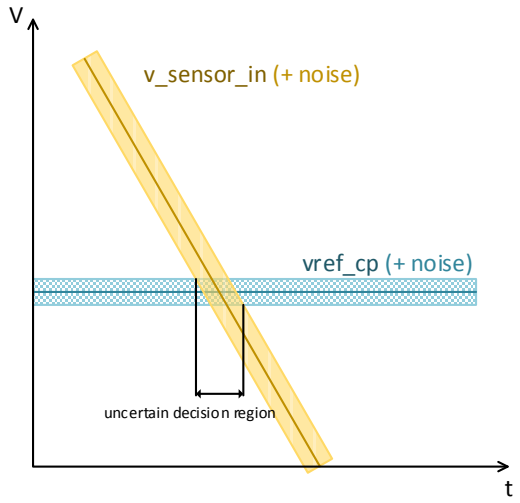

Figure 7.8: Uncertainty in comparator decision due to noise

A transient noise simulation was set up as shown in figure 7.9. Resistors were added to all three supply lines to add a certain level of noise, which was defined in the simulation setup. Additionally, coupling capacitors were added between the reference voltages, the clock and the comparator output, which represent the parasitic capacitance from the layout in the schematic.

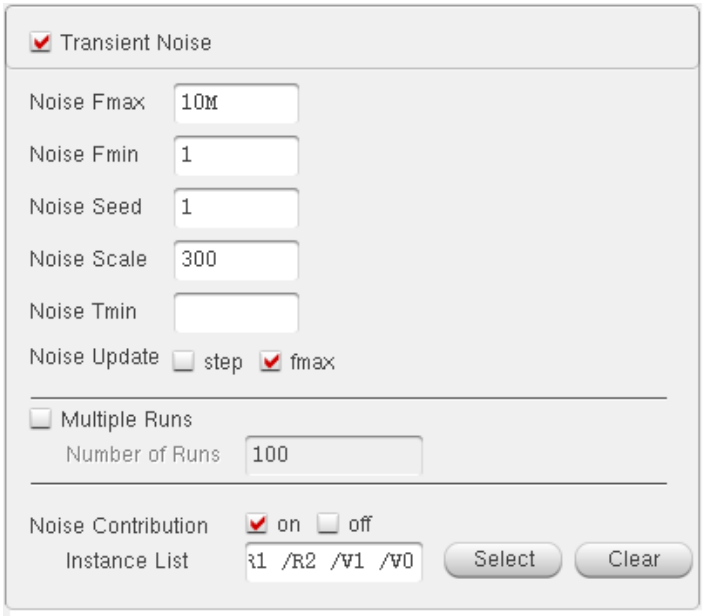

Figure 7.9: Settings for transient noise simulation

The simulations were repeated with these settings. Figure 7.10 shows the difference between the supply and reference voltages with and without noise.

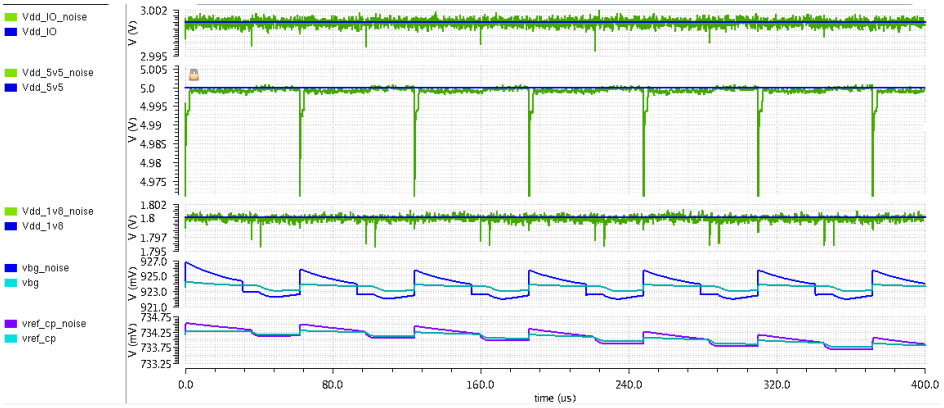

Figure 7.10: Supply and reference voltages with and without noise

In figure 7.11 the results of the top level simulation including leakage and noise are shown. However, the simulations still did not show any detection problems. Therefore, a closer look was taken at the approaching object's speed and how the sensor input capacitance is changed by it. These investigations are described in section 7.3.

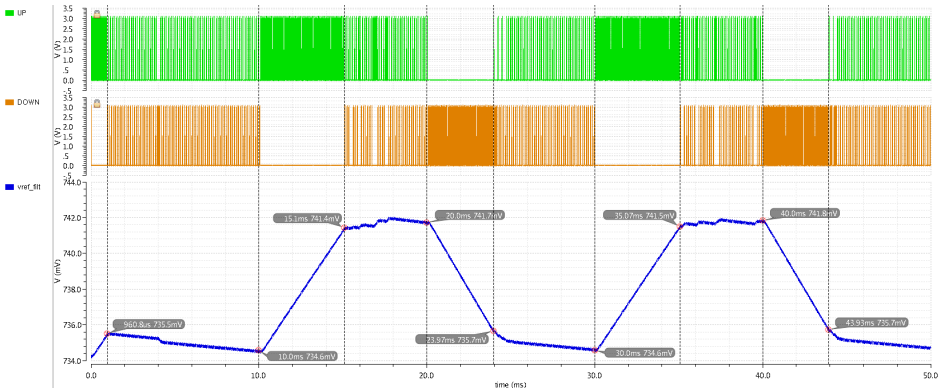

Figure 7.11: Top level simulation with leakage and noise: fast approach, $\Delta C = 70\,fF$

To lower the supply noise at the chip input, a different supply, for example a battery, can be used, or LDOs can be integrated into the chip. As a first measure LDOs have been included on an updated version of the evaluation board. Moreover, in a redesign of the chip the sensitive lines could be routed further away from the supplies and shielded coaxially.

In table 7.1 the results of the previously described simulations are compared to the estimated values for the occurring up and down pulses.

7.3 Approaching speed

The next step was to simulate and measure the capacitance change which occurred in the lab setup. With an LCR meter the capacitance of the sensor plate was measured while the

	pulses to reach equilibrium	approach at 10 ms	remove at 30 ms	approach at 30 ms	remove at 40 ms
	#UP pulses	#UP pulses	#DN pulses	#UP pulses	#DN pulses
no leakage + noise	45	54	119	58	116
leakage + no noise	53	84	61	75	60
leakage + noise	15	82	64	65	63
calculated	31	51	74	51	74

Table 7.1: Comparison of top level simulation results

approaching plate was continuously put closer to the sensor plate. Several points have been measured in this way, starting from a distance of 150 mm to a distance of about 9 mm. Since the distance was manually adjusted, the average of several measurements was taken.

The results of this measurement were transferred to an approximation curve, which was used in an approximation model for the schematic top level simulations. For this also the speed of the robot arm was taken into account. Table 7.12 shows the capacitance change at the measured distances and the corresponding time steps for different supply voltages of the robot arm.

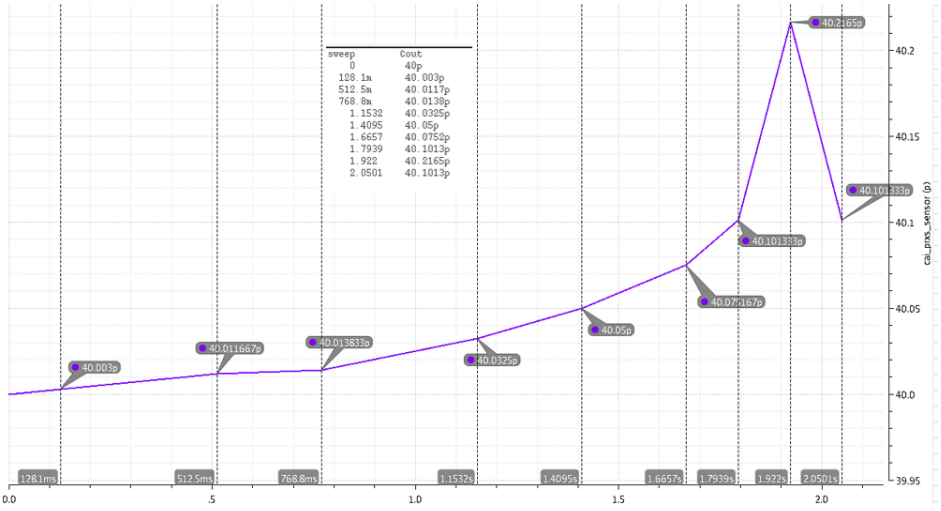

Figure 7.12: Measured curve of capacitance change, used as simulation input

Table 7.2 shows how the capacitance was added to the sensor input in further simulations. To mimic the exact approaching behavior with a robot arm speed of 0.08 $\frac{m}{s}$, a simulation run over 2 s had to be set up. It takes about six days to simulate a time of 100 ms when leakage is taken into account. Therefore, only the last step, the distance from 20 mm to 10 mm with a capacitance change of 114 fF, was used for further simulations.

The first simulation was carried out with the old transistor model without leakage and no

distance	average cap. change	Robot arm time steps (0.08 $\frac{m}{s}$)	Robot arm time steps (0.08 $\frac{m}{s}$)	Robot arm time steps (0.19 $\frac{m}{s}$)
160 *mm*	0 fF	0 ms	0 ms	0 ms
150 *mm*	3.0 fF	128.1 ms	75.6 ms	54.0 ms
120 *mm*	11.7 fF	512.5 ms	302.3 ms	216.0 ms
100 *mm*	13.8 fF	768.8 ms	453.4 ms	324.0 ms
70 *mm*	32.5 fF	1153.2 ms	680.1 ms	486.0 ms
50 *mm*	50.0 fF	1409.5 ms	831.2 ms	594.0 ms
30 *mm*	75.2 fF	1665.7 ms	982.4 ms	702.0 ms
20 *mm*	101.3 fF	1793.9 ms	1057.9 ms	756.0 ms
10 *mm*	216.5 fF	1992.0 ms	1133.5 ms	810.0 ms

Table 7.2: Measured values of capacitance change per distance, used as simulation input

noise was added to the power supply (see figure 7.13). It can be seen that there were still consecutive up pulses over a period of time of more than 4 ms, which means that more than 64 pulses occurred in a row when the charge pump reference voltage was forced to above 1 V. In the approaching phase also down pulses occur in between, but according to these simulations it would still be possible to detect an approximation. In the phase where the capacitance is removed again, pulses occur on both sides.

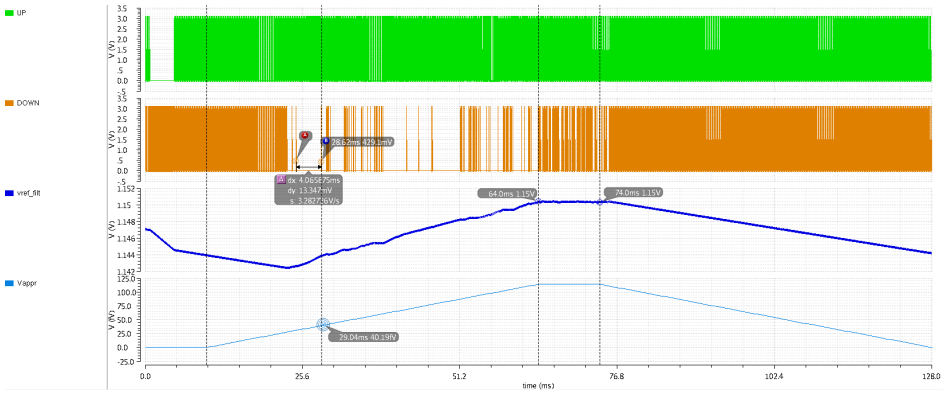

Figure 7.13: Top level simulation: slow approach, $\Delta C = 114$ fF, cntrl_cp=3

The reason for this is that due to the higher reference voltage, one down pulse leads to a bigger discharge step. Because of the leakage, it was not possible to force the reference voltage to a higher value in the lab measurements to confirm that the behavior is the same as in reality. Figure 7.14 shows the result of the same simulation with a lower reference voltage. Here, the opposite behavior can be observed, and it can be clearly seen that the capacitance has been removed.

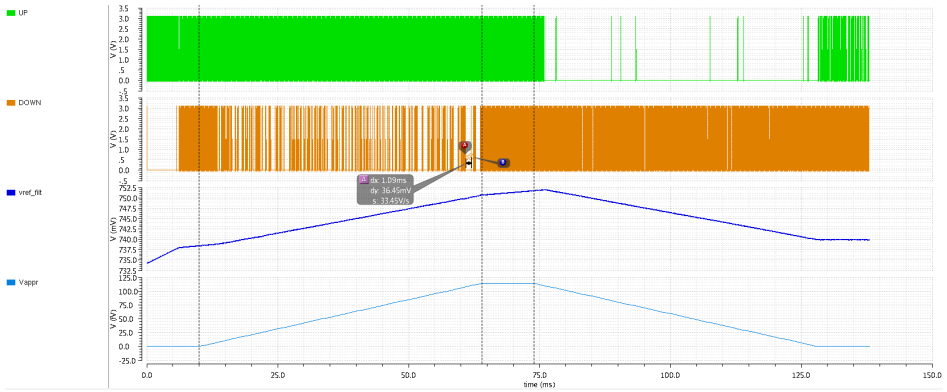

Figure 7.14: Top level simulation: slow approach, $\Delta C = 114\,\mathrm{fF}$, cntrl_cp=3

Figures 7.15 and 7.16 show the simulation results including leakage as well as leakage and noise. To emulate lab conditions, the capacitance has been increased gradually.

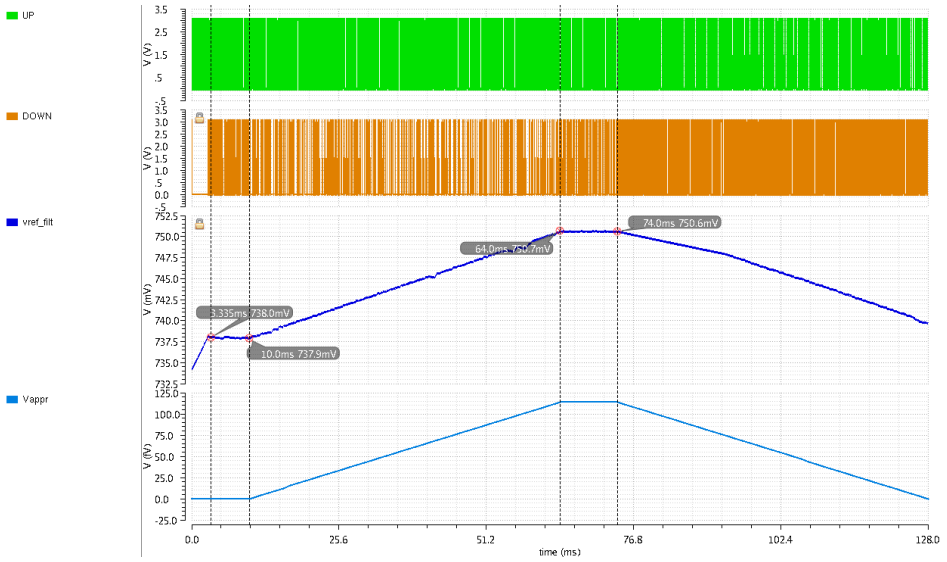

Figure 7.15: Top level simulation with leakage: slow approach, $\Delta C = 114\,\mathrm{fF}$

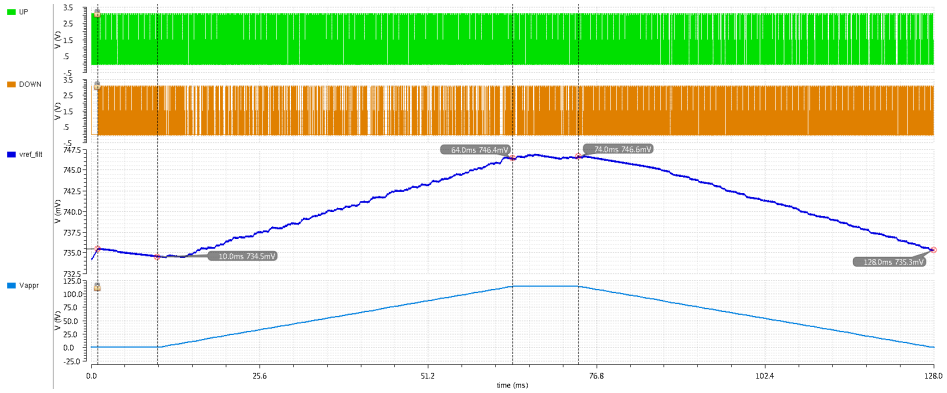

Figure 7.16: Top level simulation with leakage and noise: slow approach, $\Delta C = 114\,\mathrm{fF}$

Now, simulations and measurements produce similar results. In the slow approach simulations, including noise and leakage, as well as in measurements can be seen that the method of counting 64 up pulses in a row can not be used for detecting an approach. However, an increase of the charge pump reference voltage is still clearly visible. Therefore, a different post-processing concept, for example the use of a special filter, has to be developed to detect an approach.

8 Conclusion and Outlook

On system level one of the next steps would be to develop a high level model of the complete system in MATLAB®. From this model many findings and more detailed specifications for the analog as well as the digital implementation could be derived. For a fully integrated solution, the incorporation of a digital processing and control unit to create a fully integrated system and reduce the number of used pins, would be necessary.

Another step would be to integrate an array of capacitors that can be switched in small steps in the range of a few femtofarad. With this arrangement the capacitance increase, as it would occur when a hand approaches, can be simulated and the first validation and testing of the system could be done without an external sensor plate. Furthermore, the concept of power line communication could be investigated, to be able to send the output through the supply cables without the need for extra cables from the body control unit to the sensor chip.

To be able to cover the full input capacitance range, further measures can be taken with regards to the PCB. Firstly, the sensor input line can be made even shorter. Secondly, external decoupling capacitors can be increased to lower the influence of the supply noise. Additionally, different sensor configurations have to be investigated to a greater extend, which could be done with Momentum simulations at first.

Measurements in the laboratory show that the measured currents and voltages match quite well with the simulations. The overall behavior differs a bit from the expected one due to the factors described before.
Measurements have shown that it is difficult to find an appropriate setup to measure the sensitivity of the device in order to be able to compare it to that of the competitor's products. For future work, a new setup has to be developed to measure the sensitivity of the capacitive sensor. This new setup should be able to test different approaching characteristics as well as different sensor plates. Moreover, it should be automated with LabVIEW to make further measurements less difficult and to measure more samples, to investigate spread, in a shorter time. This also makes it easier to reuse the same setup for possible further derivatives of this chip and compare them among each other. To lower the influence of the measurement devices on the system, a voltage follower on the bandgap and reference voltage output, as has been added on the updated PCB, could also be integrated in the chip.

Furthermore, some improvements in the analog system, such as a smaller step size of the reference capacitor and a more linear behavior of the reference voltage, should be implemented. With these measures a more stable equilibrium state can be reached and thus a more stable output is created, which makes digital post-processing easier. One of the most

important improvements would be to replace the GO1 transistor in the charge pump with a GO2 transistor to eliminate the problem caused by the leakage current. Moreover, voltage regulators should be integrated in the chip to reduce the number of necessary external components and suppress the noise on the supply voltage. And lastly, the biasing of the separate blocks should be decoupled from the discharging of the sensor and reference capacitor. In this way the blocks can be biased ideally, without being influenced by the capacitance size and its need for a higher or lower discharge current.

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Appendix

MATLAB®script to calculate and plot the charge pump reference voltage from recorded up and down pulses:

```
function varargout = cai_prxs_plotVref(up, dn, ccp, vref_start, cref, csens)

    vdd5v5 = 5;
    vdd1v8 = 1.8;
    vbg = 0.9;
    Idischarge = 5*1E-6;
    ccp = ccp*1E-12;

    c0 = 50*1E-15;
    cref = cref * 1E-12;
    Csens = csens * 1E-12;

    if vref_start == 100
        dt = cref *(vdd5v5 - vbg)/Idischarge;
        vref(1) = vdd5v5 - Idischarge*dt/Csens;
    else
        vref(1) = vref_start;
    end

    for i = 1:length(up)

        if up(i) == 1
            vref(i+1) = (vref(i)*ccp + vdd1v8*c0)/(ccp + c0);
        elseif dn(i) == 1
            vref(i+1) = (vref(i)*ccp)/(ccp + c0);
        else
            vref(i+1) = vref(i);
        end
    end

    % nothing to return - plot
    if nargout == 0
        plot(vref)
        %hold all
        title('Reference voltage calculated form UP/DN pulses')
        xlabel('time')
        ylabel('vref\_cp [V]')
    else
       varargout{1} = vref;
    end
end
```

Figure .1: MATLAB®script for vref_cp plots

Schematic of the second version of the evaluation board with less sensor input capacitance, LDOs and voltage followers included on the board, and Test Station and Altera FPGA input removed:

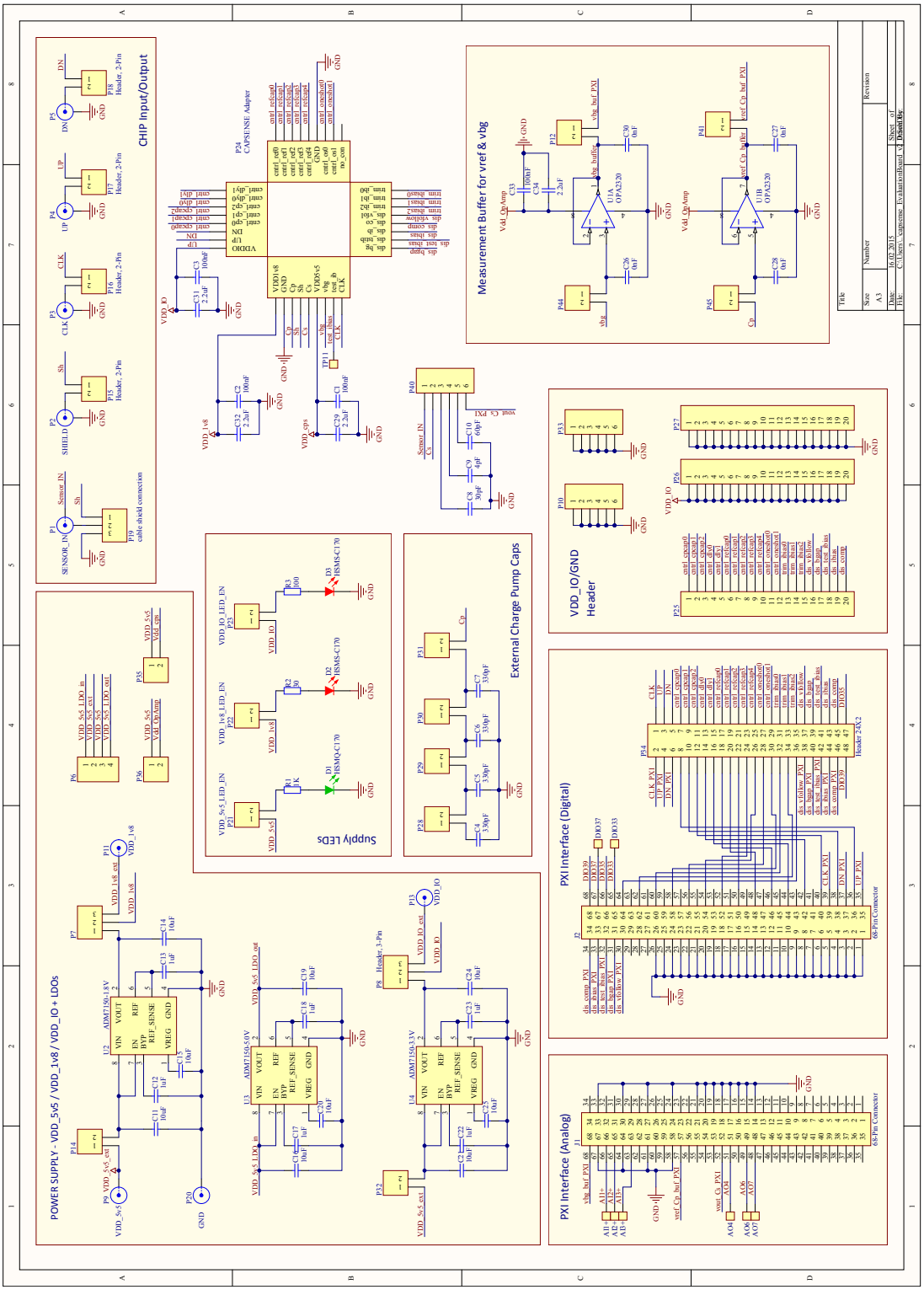

Figure .2: Schematic of the improved version of the evaluation PCB