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Low frequency noise measurements in MOSFETs

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Abstract

A low frequency noise measurement technique using an on chip amplification circuit is presented. The purpose is to have a fast, easy and reliable way of determining noise levels in transistors, which is resilient to external influences. Experimental data is gathered and compared with results from conventional noise measurement methods as well as simulation results from SPICE modelling. A good agreement is found. The analysed technology is CMOS 0.35 µm. The n-channel MOSFET transistor has a gate length of 1.2 µm and a gate width of 10 µm. The measurement technique is used to analyse the impact of gate oxide and gate contact implantation on noise levels. The performance of the measurement system in a noisy environment (processing) is tested. From the noise characterisation data of single transistors the volumetric trap density of the gate area is extracted.

Zusammenfassung

Die vorliegende Arbeit beschäftigt sich mit Niederfrequenz-Rauschmessungen in Transistoren. Die dafür angewandte Methode verwendet einen Wafer-integrierten Vorverstärker. Dies ermöglicht eine schnelle, einfache und zuverlässige Bestimmung der Rauschpegel. Das verstärkte Signal weist darüber hinaus eine gute Widerstandsfähigkeit gegenüber externen Einflüssen auf. Die gewonnen Messdaten werden mit den Ergebnissen konventioneller Rauschmessungen verglichen, so wie mit Simulationsergebnissen der SPICE-Modellierung. Es konnte ein gute Übereinstimmung gefunden werden. Die untersuchte Technologie ist CMOS 0.35 µm. Der n-Kanal MOSFET hat eine Gatelänge von 1.2 µm und eine Gatebreite von 10 µm. Die vorgestellte Methode wird dazu verwendet, den Einfluss von Gateoxid- und Polisillizium-Implantierung auf das Rauschniveau zu untersuchen. Das Leistungsverhalten des Messaufbaus in einer rauschintensiven Umgebung (Produktion) wird getestet. Aus der Charakterisierung eines einzelnen Transistors wird die volumetrische Störstellen-Dichte bestimmt.

Acknowledgements

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Contents

Chapter 1

Introduction

1.1 What is noise and why is it important?

Noise is the random fluctuation of a signal. A current will never have the exact same value over time due to various perturbations. Figure 1.1 provides an example. If noise becomes significant in comparison to the signal strength, it can be hard to distinguish between the two.

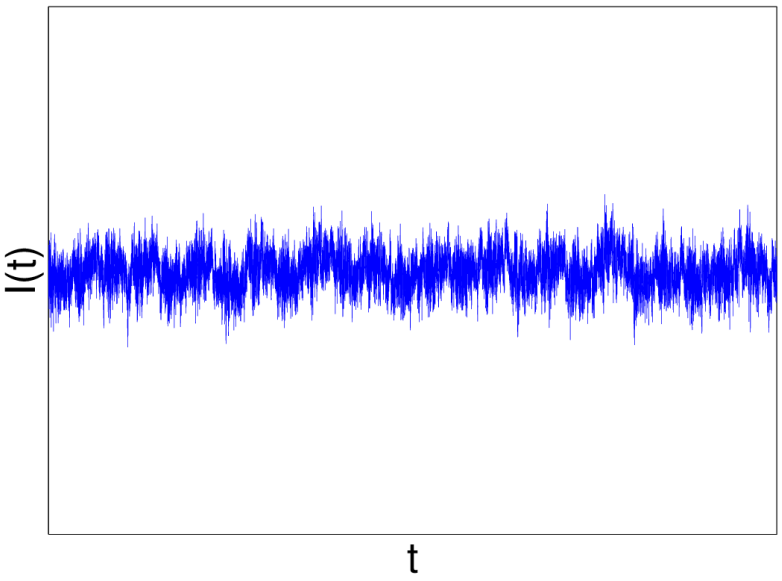


Figure 1.1: Current fluctuations over time.

Noise can originate from internal and external sources. Some examples of external sources are wireless lan, cell phones, vibrations, adjacent circuits, light, AC signals

from power source etc. External sources can be dealt with, by the use of proper shielding and filtering. For that reason they will not be subject of this work. The most common internal noise sources will be discussed in the upcoming chapter. Noise is a random perturbation of a signal and therefore a single event can't be predicted. For that reason it is conventional to take averages and use probability theory. A very useful way to look at noise is in terms of Power Spectral Density (PSD). It can be obtained by taking the square of the noise amplitude. Noise power is the Fast Fourier Transform (FFT) of the time series. One has to be aware that by squaring any phase information is lost and the original time signal can't be reconstructed. PSD gives the power distribution in frequency domain.

With gradual scaling down of CMOS devices, Low Frequency Noise (LFN) is playing a more and more important role. Not only the spatial dimensions are becoming smaller, also the number of carriers within the devices are becoming less. Since $1/f$ noise increases with the reciprocal of the device area, this can become a limiting factor for analog and digital circuits. Producing smaller devices is often connected with complicated manufacturing processes, which can lead to an increasing number of imperfections in the material. Traps play a major role in $1/f$ noise levels. LFN therefore also gives information about the quality of the devices and can also be used to monitor fabrication processes. It is important for people working in the field of microelectronics to have an understanding of noise processes to make better devices in the future.

1.2 Fundamental noise sources

Noise is the fluctuation of charge carriers flowing though a conducting material per unit of time. The average current in a piece of material with a length L is given by

$$\bar{I} = q\overline{N\nu_d}/L \tag{1.1}$$

with q the electron charge, N the number of free carriers and ν_d the drift velocity of the carriers. A bar above a variable indicates that the average is taken. Since ν_d and N can vary, equation 1.1 is rewritten as

$$I(t) = \sum_{i=1}^{N(t)} q\frac{\nu_i(t)}{L} \tag{1.2}$$

where ν_i is the drift velocity for an individual carrier and

$$N(t) = \overline{N} + \Delta N(t) \tag{1.3}$$

$$\nu_i = \overline{\nu_i} + \Delta\nu_i(t) \tag{1.4}$$

With this the current fluctuation can be written as

$$\Delta I(t) = \frac{q}{L}\overline{\nu_d}\Delta N(t) + \frac{q}{L}\sum_{i=1}^{\overline{N}}\Delta\nu_i(t) \tag{1.5}$$

The first term describes the number fluctuation of carriers and the second term the fluctuation of the carrier velocity. These are the 2 basic physical principals that can lead to current noise fluctuation in a material. Both principals can originate from different mechanisms. It is more common to speak about mobility fluctuation instead of carrier velocity fluctuation. They are directly connected through the electrical field:

$$\nu_i = E\mu_i \tag{1.6}$$

μ being the mobility (μ_i the individual carrier mobility). The following sections will take a closer look at the fundamental noise sources in terms of PSD [1].

Thermal noise

Thermal noise or white noise originates from random thermal motion of electrons in a material. The electrons are scattered randomly and the the average drift is zero. It can be mathematically easily described by equation (1.7) in terms of voltage and current noise.

$$S_I = \frac{4k_BT}{R} \text{ or } S_V = 4k_BTR \tag{1.7}$$

With k_B the Boltzmann constant, T the temperature and R the resistance. Even thermal noise appears to be white (same for all frequencies), it is physically not possible because the noise power would go to infinity. For that reason k_BT is replaced by a frequency dependent quantum correction factor when dealing with high frequencies. This factor is the Bose-Einstein function for non occupied high energy states.

$$S_I = 4\frac{hf}{e^{hf/k_BT} - 1}\frac{1}{R} \tag{1.8}$$

With h the Planck's constant. Since this thesis is dealing with low frequency noise exclusively, equation (1.7) will be used. Thermal noise sets the lower noise limit in an electric circuit with resistive elements. Nevertheless it is possible to optimize an electric circuit for low noise, using mainly reactive elements like inductances and capacitances,

which have no thermal noise share. Further the unused part of the bandwidth generates unnecessary noise and the bandwidth should be kept as small as possible [1].

Shot noise

Shot noise describes the fluctuation of current flowing across a potential barrier (like a p-n junction). Due the the discrete nature of electronic charge q (electrons) there can never be a continuous flow. Only a discrete number of charge carriers can pass the barrier in a certain time frame. This gives the current I. One can speak of Shot noise if the electrons cross the barrier independently and at random, which is a Poisson process. The created noise is given with a PSD shown in equation (1.9) [1].

$$S_I = 2qI \tag{1.9}$$

Generation-recombination noise

Generation-recombination (g-r) noise originates from traps, which randomly catch and release charge carriers. This causes a fluctuation in current. Traps are states within the forbidden band gap and exist due to various defects and impurities in the semiconductor and it's surfaces. G-r noise is only significant if the Fermi energy is close, within a few k_BT, to the trap energy level. Only then the time constants (capture τ_c and emission times τ_e) are about equal and the trap will not remain empty or filled for most of the time. The trap can be charged or neutral in it's empty state. The PSD of g-r noise is given by

$$S_N(f) = 4\,\overline{\Delta N^2}\,\frac{\tau}{1+(2\pi f)^2\tau^2} \tag{1.10}$$

With $\tau = (1/\tau_c + 1/\tau_e)^{-1}$ the trapping time constant. The shape of equation 1.10 is called a Lorentzian and is shown in figure 1.3. It will be important in the next chapter [1].

Random-Telegraph-Siganl (RTS) noise

RTS is a special case of g-r noise, in which the current is switching only between a few discrete levels in the time domain as shown in figure 1.2. If a trap releases an electron, the current rises by an discrete value and when it catches one the current drops by

the same amount. The time spend in the the higher τ_h and lower level τ_l are Poisson distributed and the PSD is given by

$$S_I(f) = \frac{4(\Delta I)^2}{(\tau_l + \tau_h)[(1/\tau_l + 1/\tau_h)^2 + (2\pi f)^2]} \tag{1.11}$$

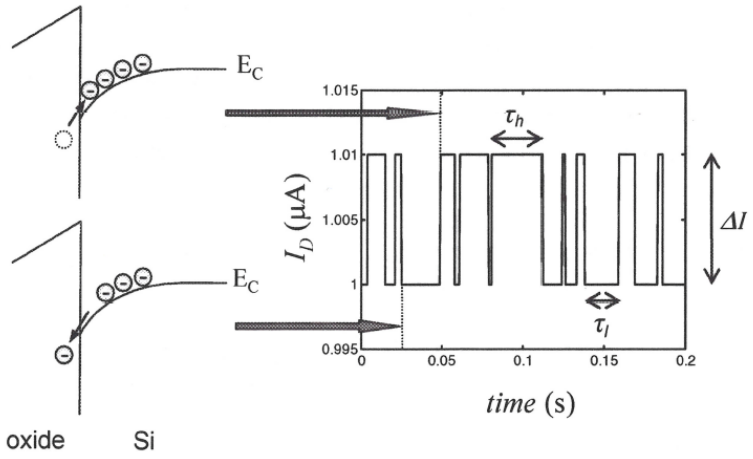


Figure 1.2: Schematic description of RTS noise [1].

The PSD of RTS and g-r noise are both of Lorentian shape, which is shown in figure 1.3. It consists of a plateau and drops with $1/f^2$. G-r noise can be seen as the sum of RTS noise processes with the same characteristic time constants. The interesting thing about RTS noise is that the contribution of single trap can be studied in the time domain. The change of current of many charge carriers is controlled by a single carrier and therefore a single electron can be studied. Since the traps are only active, if the trap energy level is close to the Fermi energy, parameters that change the Fermi energy, like temperature and transistor biasing, play an important role.

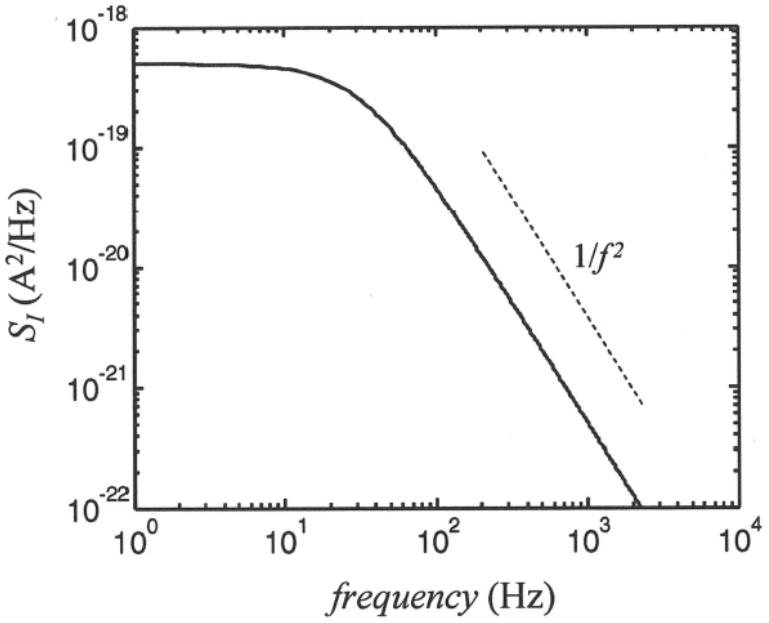


Figure 1.3: Laurentzian shaped PSD [1].

As mentioned RTS noise can only be observed if the number of traps involved is very small. Therefore a MOSFET with a small gate area (below 1 µm^2) is required [1].

Flicker or 1/f noise

A Fluctuation with a PSD behaviour like $1/f^\gamma$, with a characteristic exponent γ close to 1, is called Flicker noise, or $1/f$ noise. Typical γ values are between 0.7 and 1.3 [A^2/Hz]. The PSD can be written in the general form

$$S_{Id} = C_1 \left(\frac{I}{I_0}\right)^\beta \left(\frac{f_0}{f}\right)^\gamma \tag{1.12}$$

Where C_1 is a constant and β the current exponent. In upcoming chapters this model will be used for the fitting of noise data and the extraction of γ. For the fitting $I_d^\beta C_1 = C_2$ will be used. Flicker noise can be found in the low frequency part of the spectrum (10^{-5} to 10^7 Hz) in most conducting materials. We know from equation 1.5, that a fluctuation in current can either originate from mobility or number fluctuation of charge carriers. G-r noise from a large number of traps can produce flicker noise it

the time constants are distributed as

$$g(\tau) = \frac{1}{ln(\tau_2/\tau_1)\tau} \text{ for } \tau_1 < \tau < \tau_2\,,\ g(\tau) = 0 \text{ otherwise} \tag{1.13}$$

The factor $1/ln(\tau_2/\tau_1)$ is for normalization purposes. The superposition of many traps distributed like $g(\tau)$ gives

$$\begin{aligned} S_{tot}(f) = \int_0^{\inf} g(\tau) S_{g-r}(\tau) d\tau &= \frac{1}{ln(\tau_2/\tau_1)\tau} \int_{\tau_1}^{\tau_2} \frac{1}{\tau} \frac{B\tau}{1+(2\pi f\tau)^2} d\tau \\ &= \frac{1}{ln(\tau_2/\tau_1)} \frac{B}{2\pi f} [\arctan(2\pi f\tau)]_{\tau_1}^{\tau_2} \end{aligned} \tag{1.14}$$

Thus,

$$S_{tot} \approx \frac{B}{4ln(\tau_2/\tau_1)f} \text{ for } 1/2\pi\tau_2 << f << 1/2\pi\tau_1 \tag{1.15}$$

An example for the superposition of 4 Lorentzians is shown in figure 1.4. The Lorentzians add up to $1/f^\gamma$, with γ close to 1. It has to be mentioned that g-r noise can only be added together if the traps are isolated and don't interact.

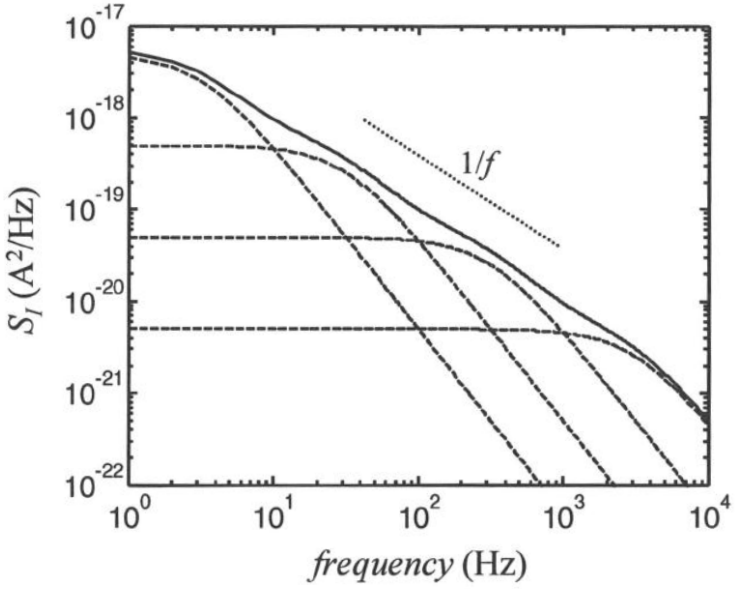


Figure 1.4: Superposition of 4 Lorentzians adds up to $1/f$ behaviour [1].

The second source of flicker noise is the mobility fluctuation. It was first described by Hooge by his empirical formula for the resistance fluctuation S_R:

$$\frac{S_R}{R^2} = \frac{\alpha_H}{fN} \tag{1.16}$$

With α_H the dimensionless Hooge parameter, which is a constant depending on the crystal quality. The factor 1/N comes from independent mobility fluctuations from each of the N conduction carriers. There has been a long discussion on which of the 2 mechanisms (number or mobility fluctuation) is the source of flicker noise. The truth seems to be that both contribute to the noise and which one dominates, is depending on the present situation. Parameters playing a role are: material, device type, operating conditions, sample variation etc. The Hooge model is accurate for explaining $1/f$ noise in metals in bulk semiconductors. In MOSFETs on the other hand, the current is confined to a narrow path under the gate oxide and traps seem to be the dominant noise source. It is important to know, that the Hooge noise model is an empirical model and therefore not based on physical models. [1]

In the classical Carrier Number Fluctuation (CNF) model, the drain current fluctuation arises from charge fluctuations at the Si-SiO_2 interface. This charge variation δQ_{it} can be explained by trapping of free charge carriers into slow oxide traps. δQ_{it} can be related to a flat band voltage variation through $\delta V_{fb} = \delta Q_{it}/(WLC_{ox})$. With C_{ox} being the oxide capacitance. For a better model the change of the charge mobility $\delta\mu_{eff}$ due to the interface charge variation is taken into account as well. With this the drain current fluctuation can be written like [2]:

$$\delta I_d = -g_m \delta V_{fb} - \alpha I_d \mu_{eff} \delta Q_{it} \tag{1.17}$$

With μ_{eff} the effective mobility and α the Coulomb scattering coefficient for electrons/holes. This leads to the normalized drain current and input gate voltage noise $S_{V_g} = S_{I_d}/{g_m}^2$ for strong inversion. The result is the Carrier Mobility Fluctuation (CMF) model [2]:

$$S_{I_d}/{I_d}^2 = (1 + \alpha\mu_{eff} C_{ox} I_d/g_m)^2 \left(\frac{g_m}{I_d}\right)^2 S_{V_{fb}} \tag{1.18}$$

and

$$S_{V_g} = S_{V_{fb}}[1 + \alpha\mu_0 C_{ox}(V_g - V_t)]^2 \tag{1.19}$$

With μ_0 the low field mobility, V_t the threshold voltage and $S_{V_{fb}} = S_{Q_{it}}/(WL{C_{ox}}^2)$ the flat band voltage noise. For comparison here the simpler Carrier Number Fluctuation

(CNF) model:

$$S_{I_d}/{I_d}^2 = S_{V_{fb}} \left(\frac{g_m}{I_d} \right)^2 \tag{1.20}$$

Total noise

The total noise of a system will almost always be a combination of different noise mechanisms. Figure 1.5 shows mixing of white noise, g-r noise and $1/f$ noise. At low frequencies $1/f$ noise or noise with a Laurentzian spectrum is more dominant. As it drops with increasing frequency, one can observe a transition to white noise, which sets the minimal signal limit.

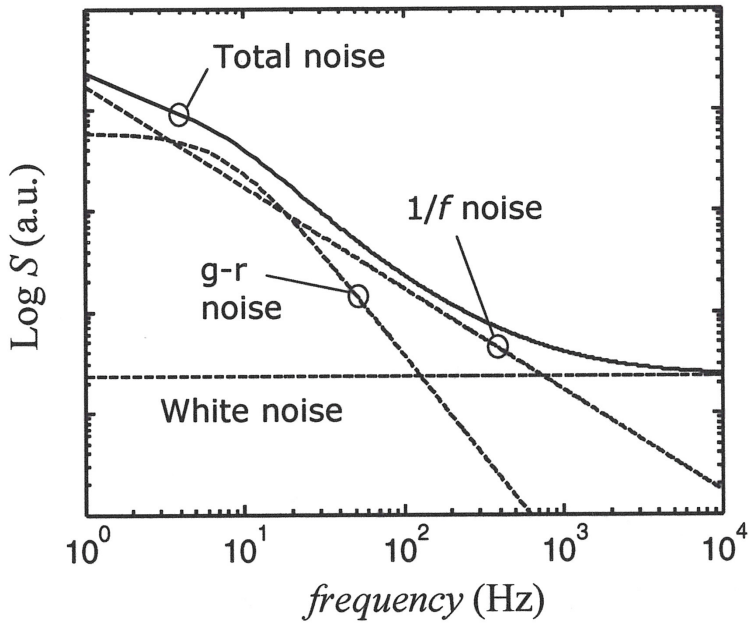


Figure 1.5: Different noise types add up to total noise [1].

1.3 Low Frequency Noise (LFN) measurements using an amplification circuit (noiseSLM)

The idea behind this thesis is to determine noise levels in transistors without the effort of doing a whole noise characterisation as described in chapter 2.1.3. This process should be done fast, easy and within a noisy environment like the production area

(machines that produce a high electric field, Wifi, mobile phones, etc.). The idea to realize this is to use an amplification circuit on chip, which boosts the signal to a level that is less susceptible to interferences. This device is located in the scribe line of the wafer, which is used for monitoring devices. When the wafer will be cut, the cutting will happen along these scribe lines. For that reason the amplification device used, is called "noise scribe line monitor" or short **"noiseSLM"**. The cut out blocks are called dies. Figure 1.6 shows a wafer, the white lines represent the scribe lines and the square a die. In chapter 2.1.2 a detailed description of the noiseSLM measurement set-up can be found.

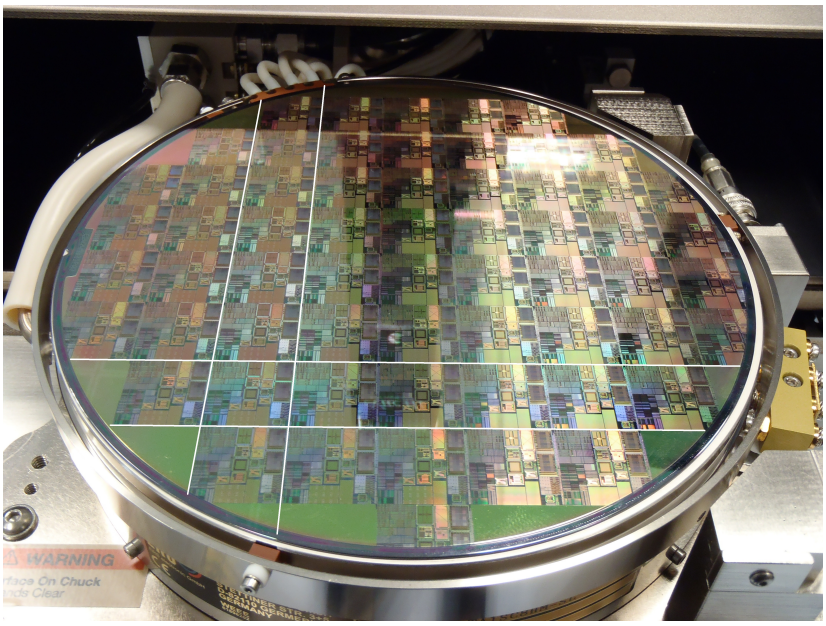


Figure 1.6: Wafer, the white lines are representing the scribe-line. The square formed by the scribe line is called a die.

The on-wafer amplification circuit

In this section the noiseSLM schematic, shown in figure 1.7, will be explained. The noiseSLM forms a noisy current source and becomes activated by applying a voltage between the pads **a** and **b**. At the top of the schematic a current mirror **cm** can be seen, it guaranties that the same current flows through both of it's paths. Next up are 2 cascodes **cs1** and **cs2** which reduce the supply voltage dependence of the circuit. This ensures that the created noise originates from the transistor and not from variations in the supply voltage. **M1** is the actual MOSFET transistor under test. Even though there are other transistors used in the circuit, this one has the smallest gate area (especially gate length) and therefore generates the most noise. The gates of the transistors **M8** and **M9** are connected with the gate of **M1** and are amplifying

the noise signal. During start-up a **M1** drain current of $I_d = 0$ would actually be valid working point. The working-point-correction structure **wpc** is build in to prevent that. Besides the contacts **a** and **b**, the noiseSLM also has a pad **psub** for substrate contacting and biasing. The shape of the structure on wafer with it's pad configuration is shown in figure 1.8

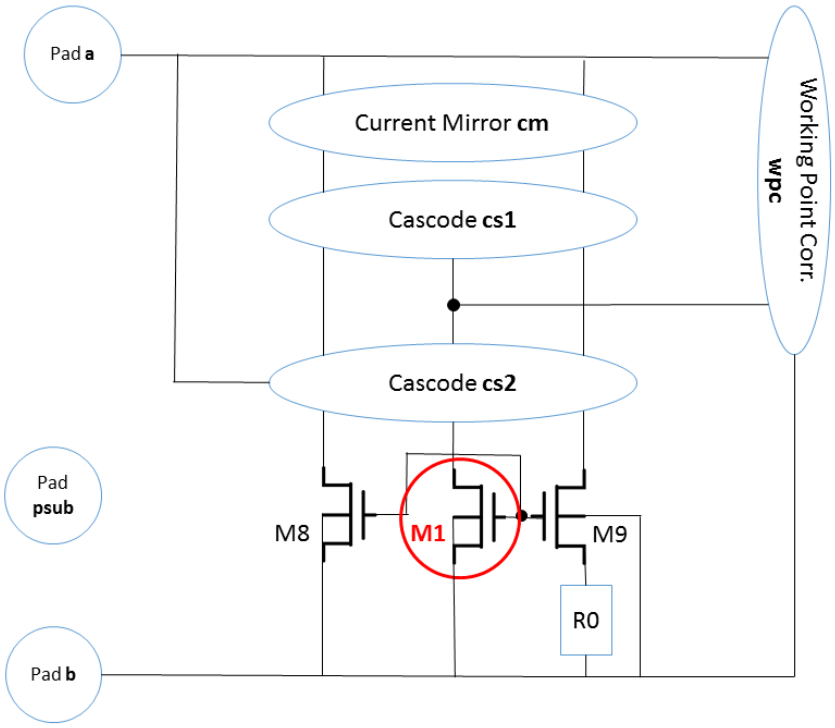


Figure 1.7: Schematic of noiseSLM

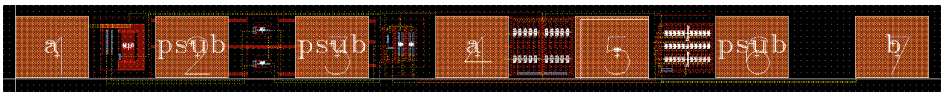


Figure 1.8: Pad configuration

Chapter 2

Measurements and Simulations

2.1 Measurement system

This chapter gives an overview of the used measurement systems and set-ups.

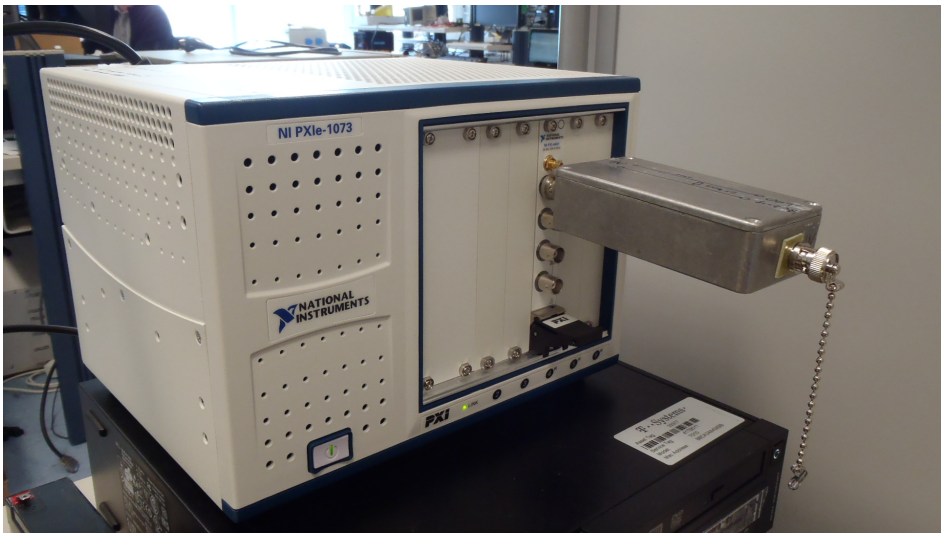
2.1.1 Analog-Digital-Converter (ADC)

Almost all measurements concerning the NoiseSLM have been done using an Analog-Digital-Converter (ADC) from National Instruments "NI PXI-4461". It has a resolution of 24 bit and the voltage range can be switched between ± 42.4 V and ± 316.0 mV up to a maximum resolution of ∼ 40 nV. The different ranges are important, since the noise data is sitting on top of a ∼ 7 V DC signal. The ADC collects the voltage variations over time and then Fast Fourier Transforms (FFT) it into a noise spectrum (Power Spectral Density (PSD) in [V^2/Hz]). The resulting spectrum is too broad to be useful and an averaging is done for smoothing

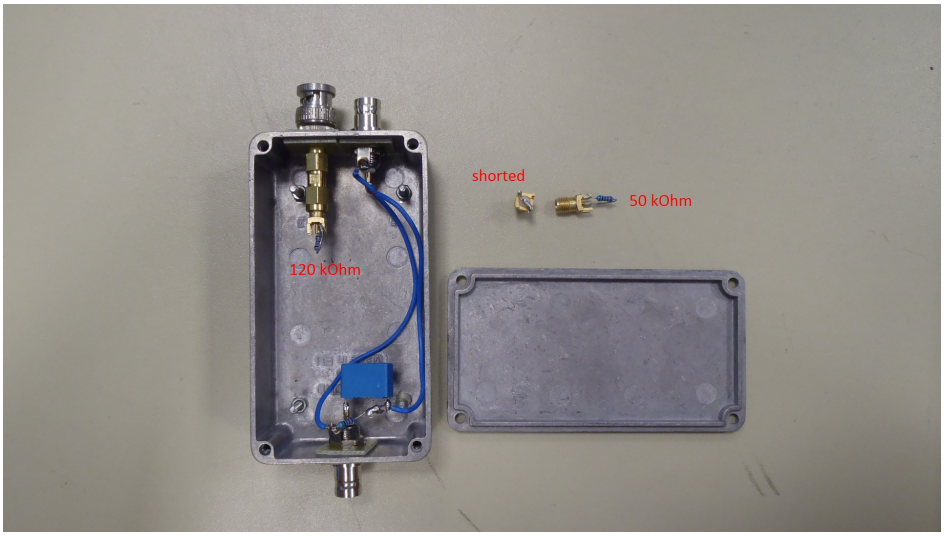
The calibration of the system was done using thermal noise measurements of metal film resistors. They have almost exclusively thermal noise S_{th} and no flicker noise share. Thermal noise is is mathematically very well defined and constant over all frequencies:

$$S_{th} = 4k_B T R \tag{2.1}$$

k_B is the Boltzmann constant, T the temperature and R the resistance. For the calibration a resistor with $R_1 = 120\,\mathrm{k}\Omega$, a resistor with $R_2 = 50\,\mathrm{k}\Omega$ and the background noise was measured. For the background noise the input (BNC plug) was shorted using a piece of wire soldered onto a socket. For the measurement the device under test was screwed tight into a metal box, to minimize interferences from outside. The box and the resistors can be seen in figure 2.1b.



(a) NI PXI-4461 with isolation box

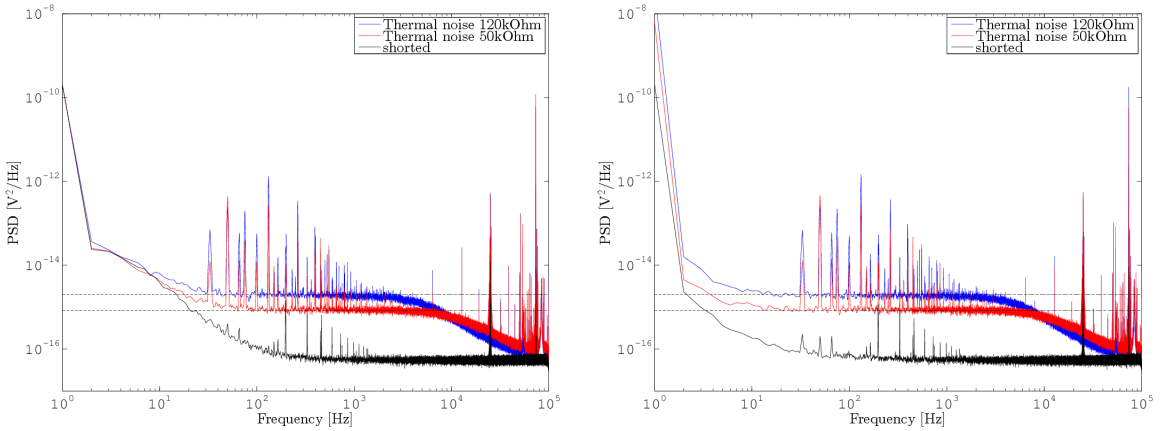


(b) Isolation box

Figure 2.1: Measurement equipment

The experiment was done with the ADC in AC and DC mode using the smallest input range of $\pm$ 0.316 V. You can see the results in figure 2.2. The dashed lines are the corresponding calculated values from equation (2.1) at 25 °C. For the recording of the spectrum a recording time of 1 second was chosen and an averaging number of 100. With these settings the measurement gives useful results and can be done within a reasonable time. A measurement time of 1 second obviously constrains the spectrum to frequencies bigger than 1 Hz. The ADC also has a Flicker noise share at low frequencies. One has to be careful not to mistake this with the noise of the device under test. Picking the AC mode lets the signal go through a high pass filter

and therefore cuts off the $\sim$ 8V DC value. This leads to a higher noise floor at low frequencies due to an additional device. The lower frequency limit for the AC mode with a measurement time of 1 second and an average of 100 times is 13 Hz, for DC mode 8 Hz. For bigger signals like the amplified signal from the noiseSLM the lower limit moves to even smaller frequencies. For that reason the lower limit of 10 Hz is chosen for both modes. The other end of the spectrum is limited by the maximum sampling rate which is 204.8 kS/s, which leads to a frequency cut off at about 5000 Hz as can be seen in the figures. Even though this value is true for the thermal noise is resistors, for noise measurements the cut-off frequency has to be taken into account. The cut-off frequency arises from the parasitic capacitances and resistors that form a low pass filter and therefore attenuate the signal above a certain frequency. For the noiseSLM this frequency is $\sim$ 1000 Hz. This leaves us with a usable frequency range of 10-1000 Hz for the noiseSLM measurements.
The lowest signal acquired with the ADC during all transistor noise measurements with 1 second acquisition time was $2.2E-10\,\mathrm{V}^2/\mathrm{Hz}$. This is raw data, not noise. The noise floor of the ADC at 10 Hz is about $1E-15\,\mathrm{V}^2/\mathrm{Hz}$ for 1 second data acquisition time. There is no danger for measurement data to interfere with the noise floor.



(a) Thermal voltage noise, measurement in AC mode.

(b) Thermal voltage noise, measurement in DC mode

Figure 2.2: Comparison between voltage noise measurements in AC and DC mode-

Figure 2.3 shows a recording over 30 seconds with an average number of 100. This corresponds to an acquisition time of 50 minutes With these settings, frequencies starting from 0.1 Hz can be analysed.

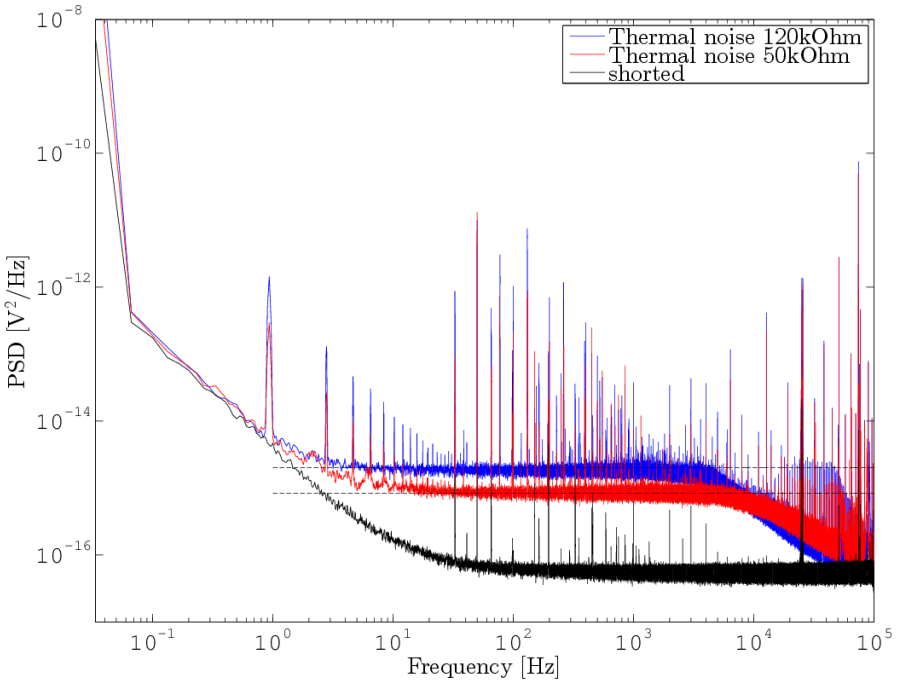


Figure 2.3: Thermal noise measurement in DC mode over 30 seconds and with 100 averages

2.1.2 NoiseSLM measurement set-up

Figure 2.4 shows the measurement set-up schematic for a noise measurement using the noiseSLM. The noiseSLM forms a noisy current source after the voltage source V is turned on. The created noise is proportional to the noise in the transistor under test. The current noise is then transformed into voltage noise over the resistor R and measured by a spectrum analyser or in the case of this thesis an ADC. The used resistor is a metal film resistor, since their Flicker noise is negligible. Following Ohm's law $U = RI$ the resistor acts as an additional amplifier for the ADC.

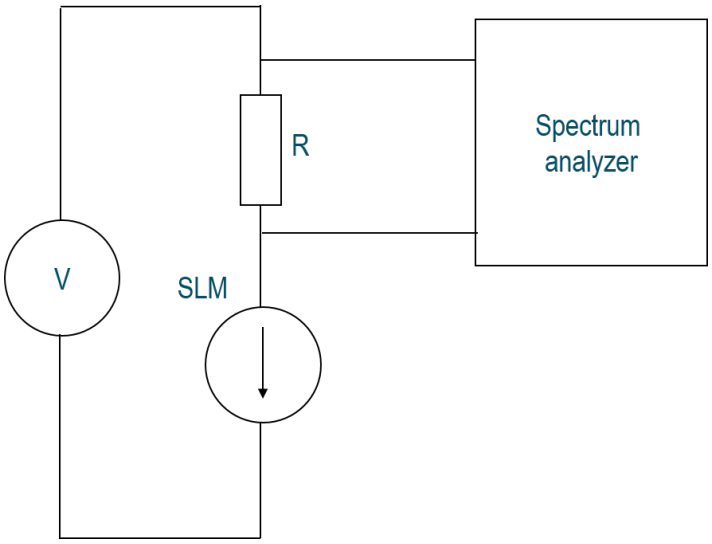


Figure 2.4: Measurement set-up

The measurements were done using a metal shielded prober figure 2.5, resting on a heavy stone plate with 4 gas suspended legs to prevent electronic and seismic interferences. Some interferences like the 50 Hz spike from the power grid are very hard to get rid of and will show up nevertheless. The chamber is flushed with nitrogen to prevent the wafer from reacting with air. The laboratory temperature is at a constant 25 °C. The prober temperature control is not used for the measurements, because it would lead to interferences. The heating is done electrically and would show up on the spectrum. The cooling is done by a cooling liquid, that is circulating through the wafer socket. Circulating ions in this liquid would also lead to electrical disturbances. The prober used for the noise characterisation in chapter 2.1.3 uses clean room air for the temperature control. This doesn't lead to any interferences. In the right picture, the wafer can be seen. The socket, the wafer is resting on, is called a chuck. The isolating hood is removed in this picture and the needle card can be seen on top.

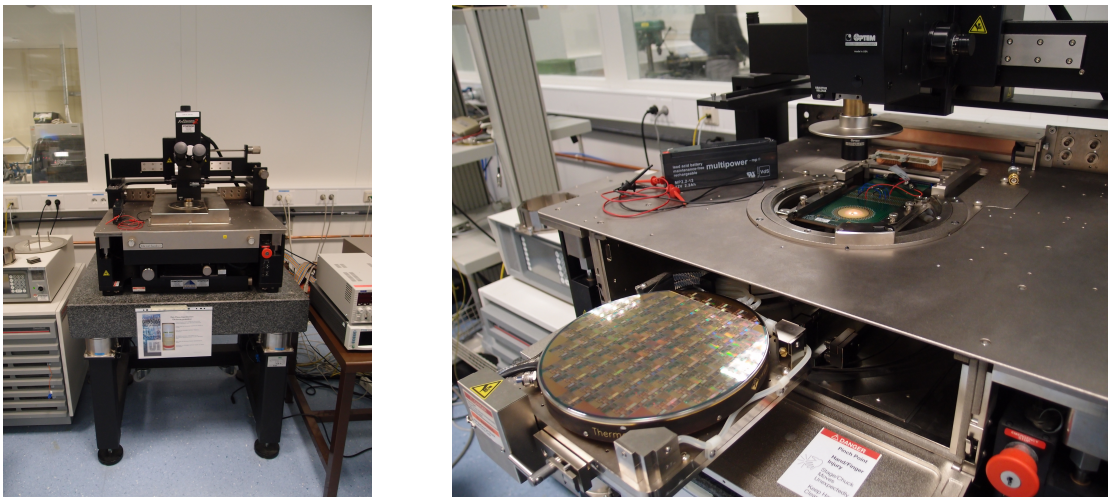


Figure 2.5: Prober (left) and Chuck (right)

The needle card is used to contact the pads on the wafer (figure 2.6). It puts the voltage across the noiseSLM and the substrate to ground. For the noiseSLM the resistor **R = 120 kOhm** mentioned above is soldered onto the board and the connection with the voltage source (lead battery 12V,2.2Ah) is made. A battery is chosen, because it has very little noise and is small enough to fit it in the metal casing. Some of the voltage drops over the resistor and the generated noise signal sits on top of a $\sim$ 7 V DC voltage. This signal is transferred to the ADC using a BNC cable with ground on the outer cylinder.

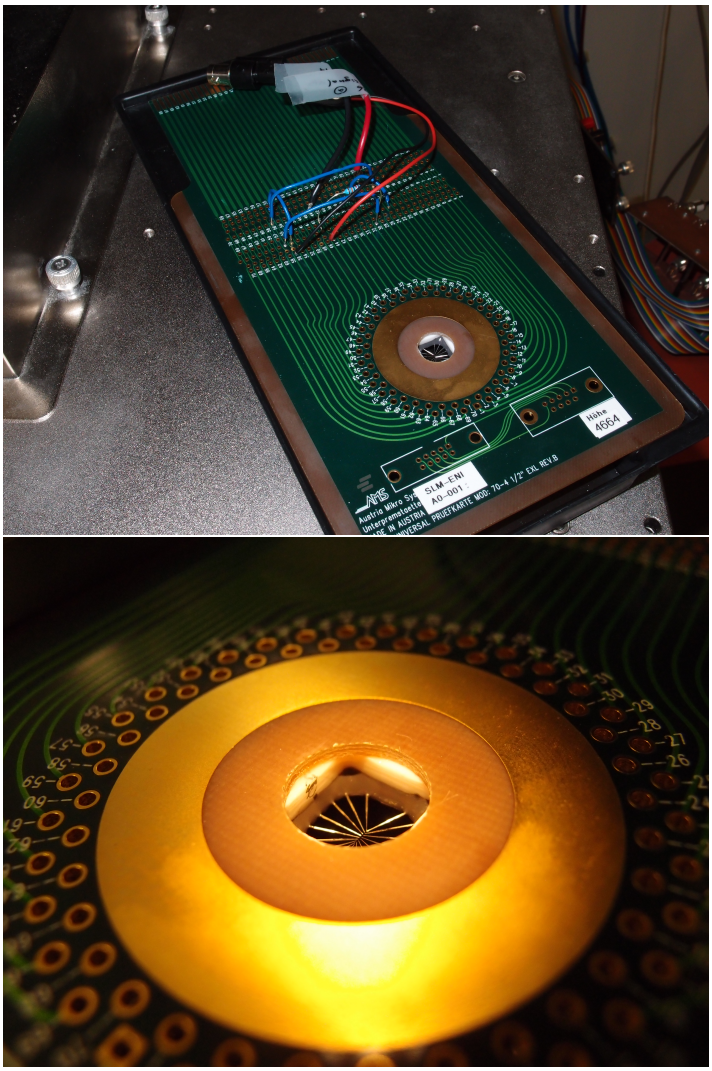
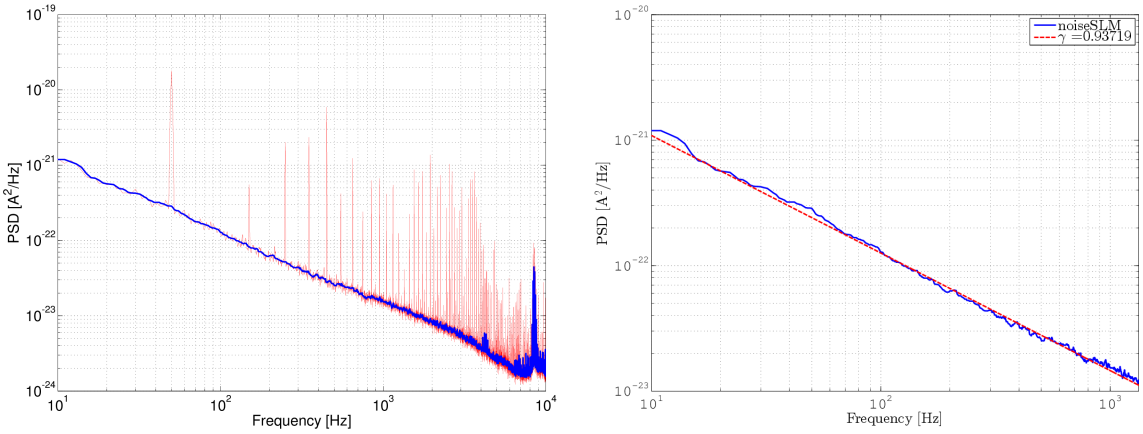


Figure 2.6: Needle card full view and close up

The prober location is set in an engineering laboratory where a wide variety of experiments are run. Therefore the data is affected by a lot of interferences. To get rid of those frequency spikes, the Matlab filtering function "medfilt1" with a filtering factor of n=20 is used. The data before and after the filtering is shown in figure 2.7a. The linear part of the modified spectrum is fitted according to the physical model equation (1.12) and the characteristic exponent γ is extracted in figure 2.7b. The presented data is already divided by the amplification factor of the circuit, therefore shows the noise of the transistor under test.



(a) Smoothing of acquired data

(b) Fitting characteristic exponent γ

Figure 2.7: NoiseSLM data treatment

2.1.3 LFN characterisation

In this section the noise characterisation measurement set-up for transistors that don't have an amplification circuit like the noiseSLM will be discussed. The transistor can be contacted on the wafer by micro-manipulators on source, gate, drain and body site. The transistor is identically build to the one in the noiseSLM. For the measurement body and the source are both grounded. The set-up is presented in figure 2.8. As a first step, the transfer characteristic, as described in chapter 2.1.4 is done. This ensures that the transistor is working properly and for picking the operating points for the noise characterisation. The operating points are forced by Source Measurement Units (SMU). To reduce any noise that might come from the SMUs, the signal goes through a Low Pass Filer (LPF) with a very low cut-off frequency. This makes sure, that they only give a flat DC signal. The source R_{source} and load resistor R_{load} set the impedance conditions for the device under test. The blocking capacitance has a large capacitance and forms a high pass filter together with R_{load}. This makes it possible for the system to measure noise spectra, starting from less than 3 Hz. The noise signal gets amplified by a Low Noise Pre-amplifier (LNA). A good LNA is important, since it sets the noise floor for the measurement (figure 2.9). The amplified signal is collected by a Dynamic Signal Analyser (DSA) and a Fast Fourier Transform (FFT) is done to transform the data from the time to the frequency domain. The resulting spectrum can be used for noise characterisation. [3]

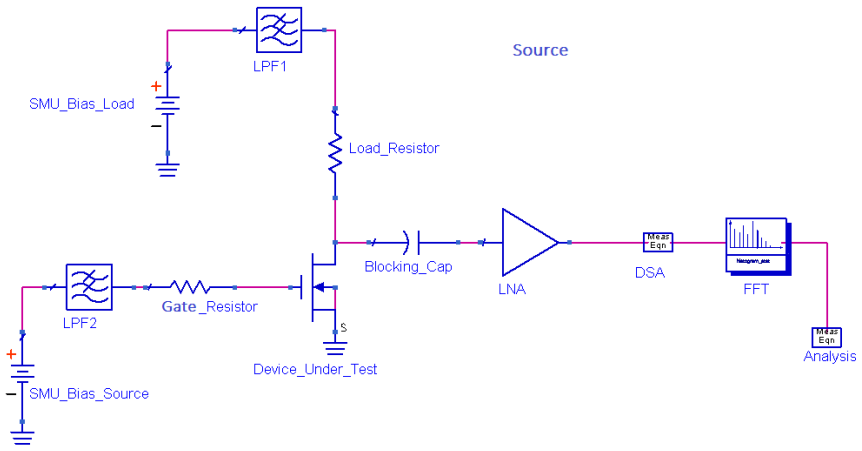


Figure 2.8: Measurement set-up for a LFN characterisation [3]

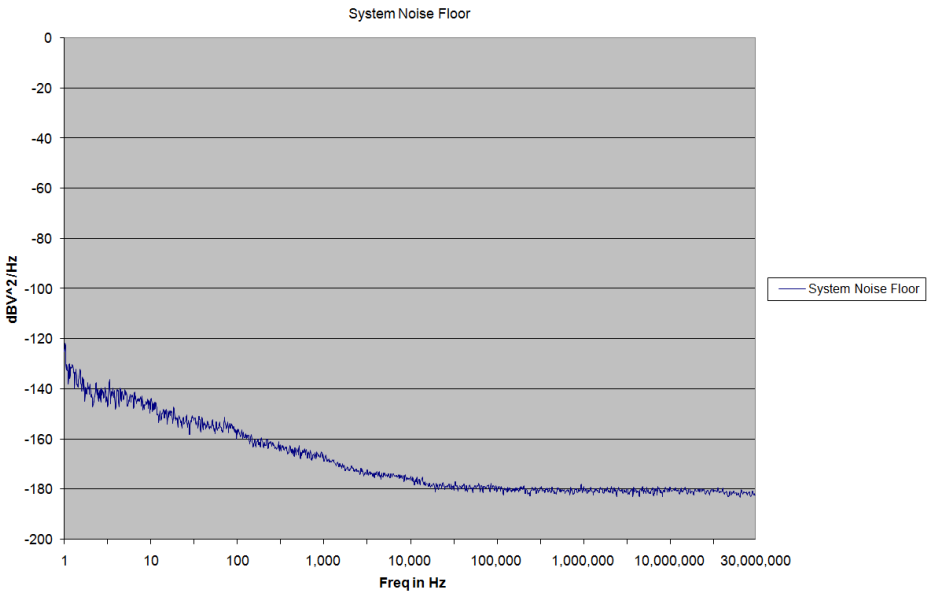


Figure 2.9: Noise Floor of measurement system [3]

Figure 2.10 shows the LFN of a Transistor without the amplification circuit. Below 100 Hz the signal is influenced by the bandwidth limitation and above 10 kHz roll-off is happening. Between $0.1 - 10\,\text{kHz}$ the data is useful and shows Flicker noise behaviour.

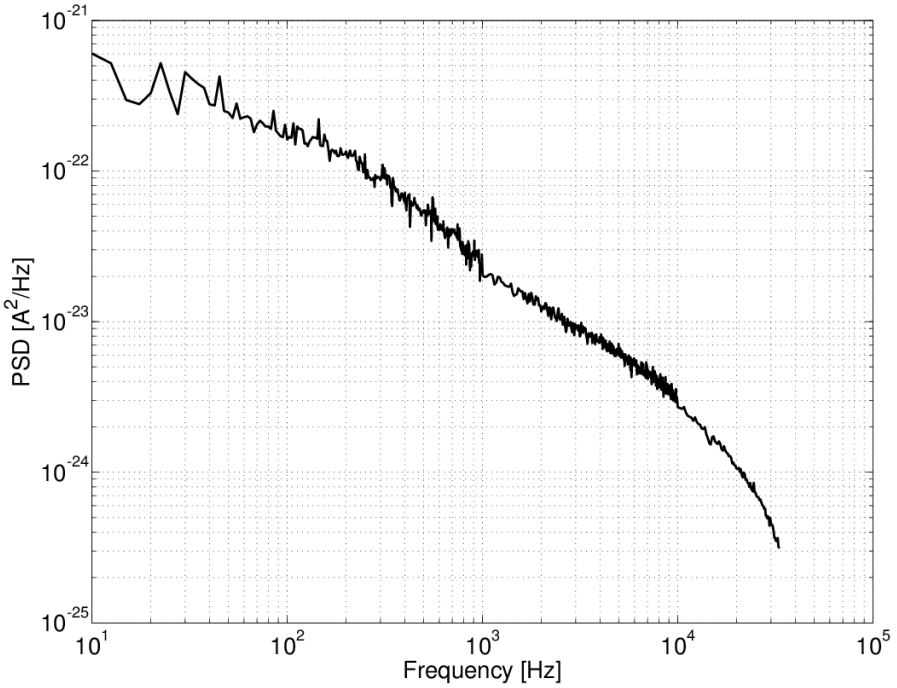


Figure 2.10: LFN spectrum

2.1.4 Methodology

This chapter describes the methodology used to characterise noise data from LFN measurements as described in chapter 2.1.3.

Transfer characteristics

In a transistor transfer characteristic the drain current is plotted as a function of gate voltage. It gives the transistor behaviour, for different applied gate voltages and a malfunctioning device can be identified. From the semi-logarithmic plot (figure 2.11) we can see that the transistor is working properly. Now the drain currents for the noise measurement are chosen. These points are taken between the saturation region and the start of the linear region. From the transfer characteristics we can also calculate the corresponding transconductance g_m from equation (2.2). g_m and I_d are plotted versus V_{gs} in figure 2.12. The little peaks in the g_m plot are a consequence of the limited amount of I_d and V_{gs} data points. In a measurement with a smaller step size, they wouldn't be visible.

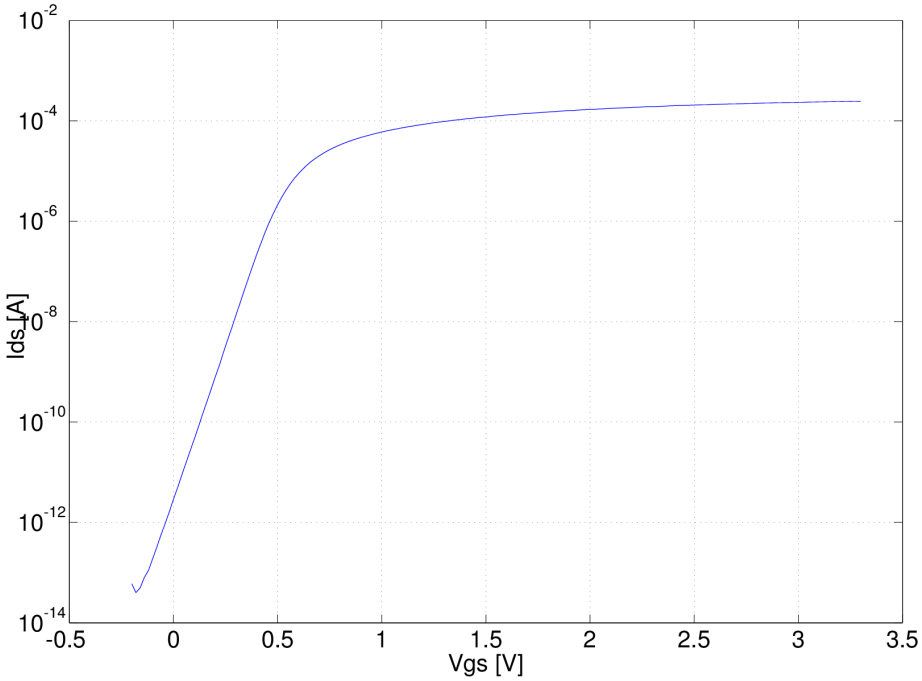


Figure 2.11: Transfer characteristic of transistor

$$g_m = \frac{\Delta I_d}{\Delta V_{gs}} \tag{2.2}$$

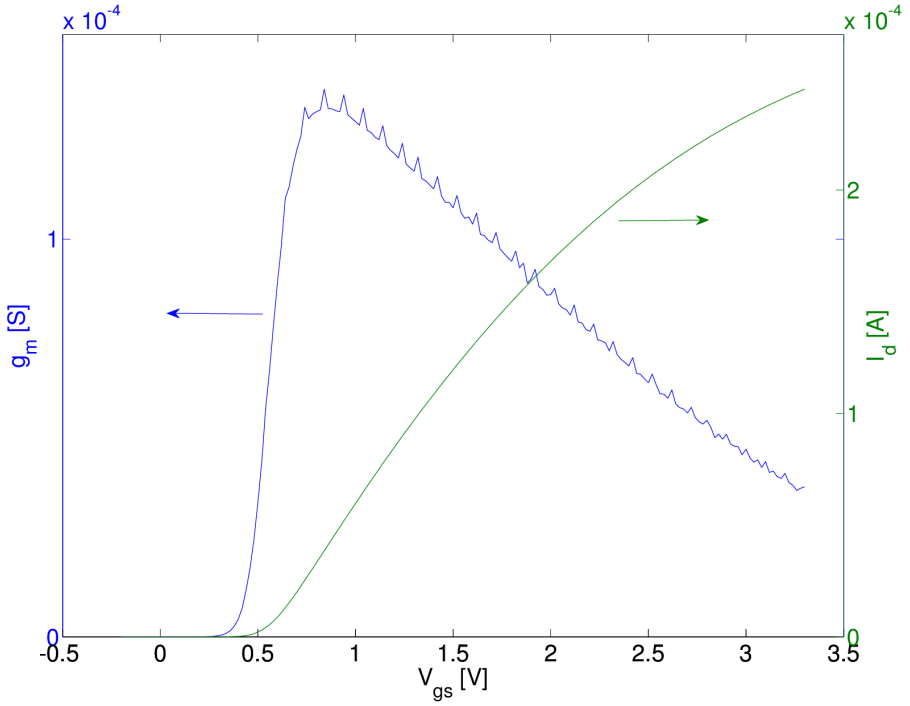
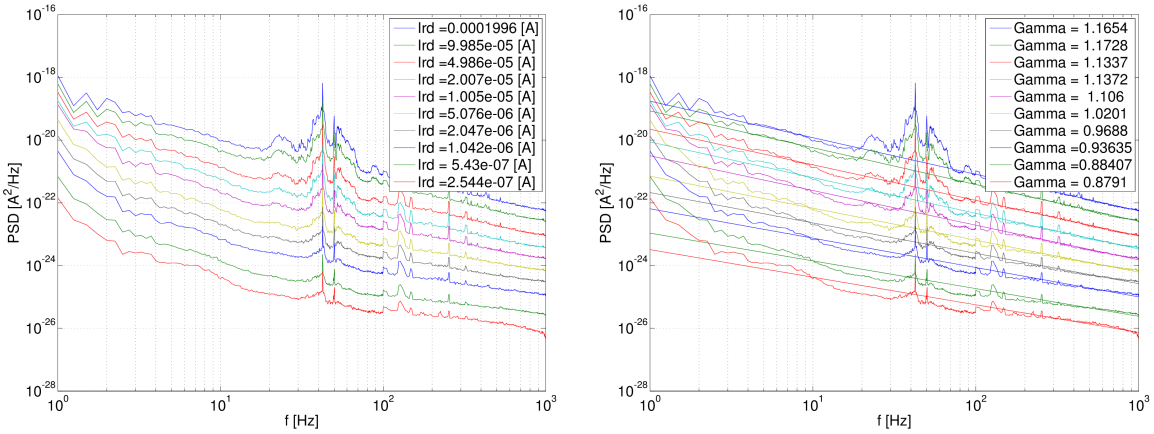


Figure 2.12: Transconductance g_m and drain current I_d versus gate-source voltage V_{gs}

Noise Data

In figure 2.13a the noise for ten drain currents, picked from the transfer characteristic, is shown. Following equation (1.12) a fit is put through the lines and the characteristic exponent γ is extracted. The biggest interferences spikes show around 50 Hz, for that reason this area is cut out from the fitting and only the regions from 2-20 Hz and 100-1000 Hz are considered. For the noise to be Flicker noise γ has to be close to 1 [2]. If it is not within these boundaries the physical mechanism behind the noise is not Flicker noise. The fit and the corresponding γ values are shown in figure 2.13b.



(a) Noise characteristics of 10 drain currents (b) Fitting characteristic exponent γ

Figure 2.13: nMOSi noise characteristic

Another way to ensure that the noise data is indeed Flicker noise is to plot the current noise S_{Id} times f^{γ} over frequency. The resulting lines (figure 2.14) have to be flat besides the interference peaks.

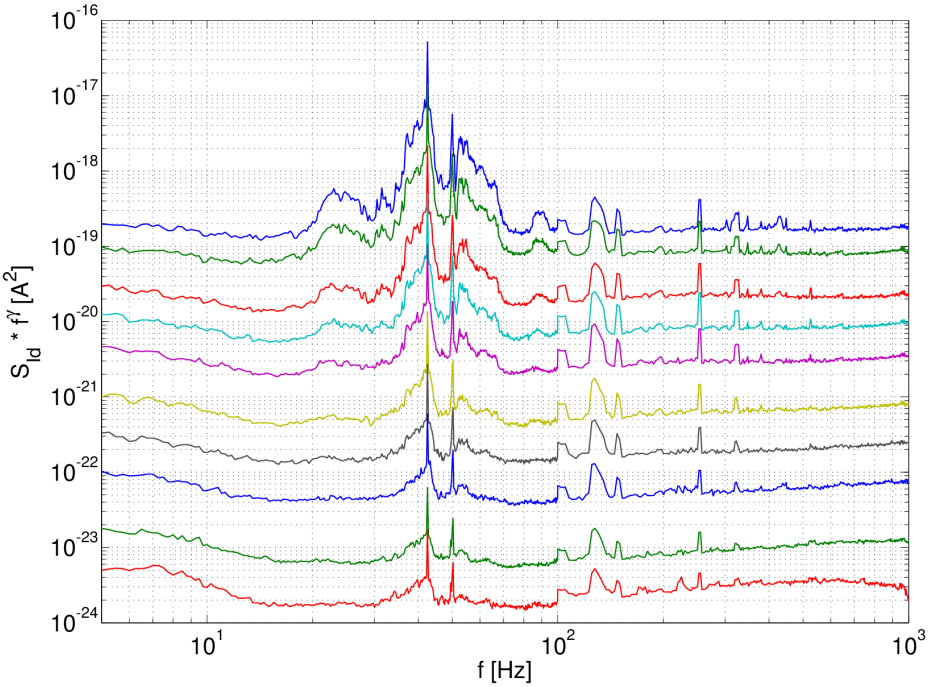


Figure 2.14: $S_{Id} * f^{\gamma}$

If the spectrum shows Flicker noise behaviour, the next step is to plot $f^{\gamma}S_{Id}/{I_d}^2$, with f $\sim$ 10 Hz versus I_{ds}. Since noise shows random fluctuations it is better to take the average value around 10 Hz. This can be done since the spectrum is about flat after being multiplied with f^{γ}. For the resulting plot, the physical noise model (Carrier Number Fluctuation, Carrier Mobility Fluctuation, Hooge) that fits the data the best has to be found.

2.2 NoiseSLM

This chapter covers the simulation of the noiseSLM, the measurement of the noiseSLM and the measurement of an identically constructed transistor without the noiseSLM circuit. The simulation is done using the program "Cadence". After looking at the noiseSLM at one wafer location, we will do 14 additional measurements on certain wafer sites for a variability analysis. The comparison of the simulation and the two measurements will be discussed at the end.

2.2.1 Simulation

The simulation of the noiseSLM was done using the the program Cadence. Cadence is an environment for designing, and simulating integrated circuits using SPICE (Simulation Program with Integrated Circuit Emphasis) models. The exact circuit layout of the noiseSLM can't be displayed here, but a schematic can be found in figure 1.7. The simulation was done at 100 Hz and then expanded over the full frequency range according to spice models. Figure 2.15 shows the current and voltage noise simulation, which are connected by $S_{V_g} = S_{I_d}/{g_m}^2$. The simulation was done using a resistor of 120 kΩ and a supply voltage of 12V. The transistor shows 1/f behaviour until it goes into saturation above 1000 Hz.

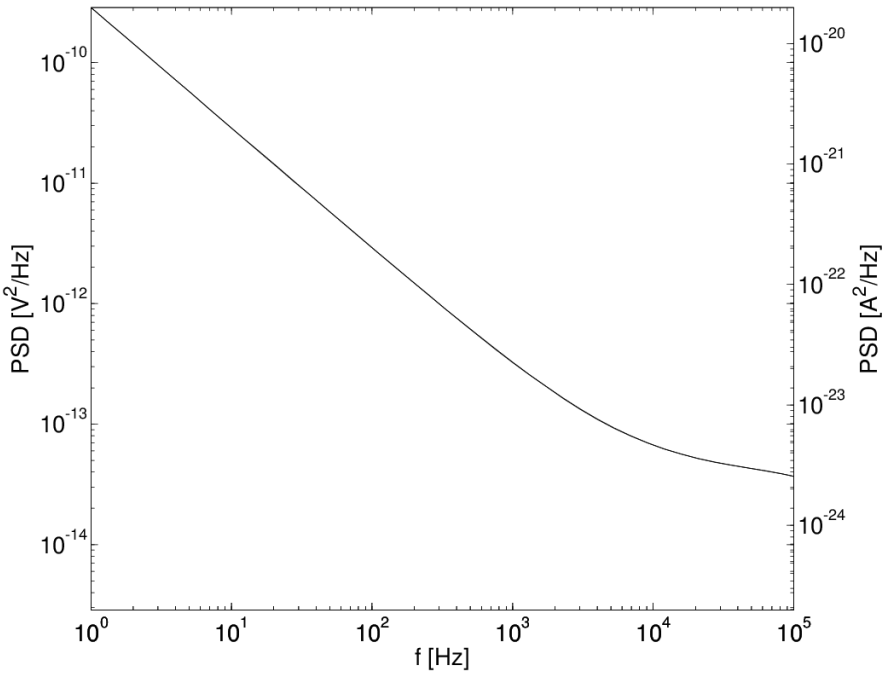


Figure 2.15: Simulation of current and voltage noise.

The simulation also yields the noise contribution of the individual parts making up the noiseSLM to the total noise. In table 2.1 this data is shown. We are only interested in the noise of the transistor M1 and therefore it's necessary that the majority of the noise is coming from this device. At 10 Hz: 95% of the noise is coming from M1, at 100 Hz: 94% and at 1 kHz: 85%. Above 10 kHz less than half of the noise is Flicker noise coming from M1 and the contribution is too small to give reliable data. Devices are labeled M for transistor and R for resistor. The table shows the flicker noise contribution **"fn"**, the drain-source resistance thermal noise **"id"** and the thermal noise of the resistors **"thermal"**. This explains nicely the saturation behaviour of the noise curve in figure 2.15. While Flicker noise is dropping like 1/f, thermal noise is constant over all frequencies and the curve saturates.

Table 2.1: Contribution to total noise

Frequency [Hz]	Device	Parameter	Noise Contribution [A/sqrt(Hz)]	% of total noise
1.00E+01	M1	fn	1.47E-09	95.20
	M8	fn	1.97E-10	1.71
	M0	fn	1.71E-10	1.29
	M5	fn	1.38E-10	0.84
	M4	fn	1.38E-10	0.84
1.00E+02	M1	fn	4.72E-10	94.14
	M8	fn	6.31E-11	1.69
	M0	fn	5.48E-11	1.27
	M5	fn	4.42E-11	0.83
	M4	fn	4.42E-11	0.83
1.00E+03	M1	fn	1.50E-10	84.83
	M1	id	3.04E-11	3.47
	M4	id	2.70E-11	2.75
	M5	id	2.70E-11	2.75
	M8	fn	2.01E-11	1.52
1.00E+04	M1	fn	4.74E-11	42.58
	M1	id	3.03E-11	17.43
	M4	id	2.70E-11	13.82
	M5	id	2.70E-11	13.82
	R0	thermal	1.44E-11	3.94
1.00E+05	M1	id	2.87E-11	29.18
	M4	id	2.55E-11	23.14
	M5	id	2.55E-11	23.14
	M1	fn	1.41E-11	7.04
	R0	thermal	1.36E-11	6.59

The noiseSLM has a build in amplification factor of 33.2. It has been extracted by inserting a small AC signal between the cascode cs2 and the transistor M1. The amplitude ratio between drain and source site gives the amplification factor. This can also be included in real noseSLMs for amplification factor measurements. The noise of transistor M1 without the amplification circuit has been simulated to compare it with the signal of the noiseSLM. The comparison is shown in figure 2.16. The single transistor is represented by the red line and the noiseSLM by the black bold line. The noiseSLM simulation is divided by the amplification factor for a better comparison (black dashed line). They are a good fit until about 1000 Hz, when the thermal noise of the noiseSLM components is starting to saturate the signal.

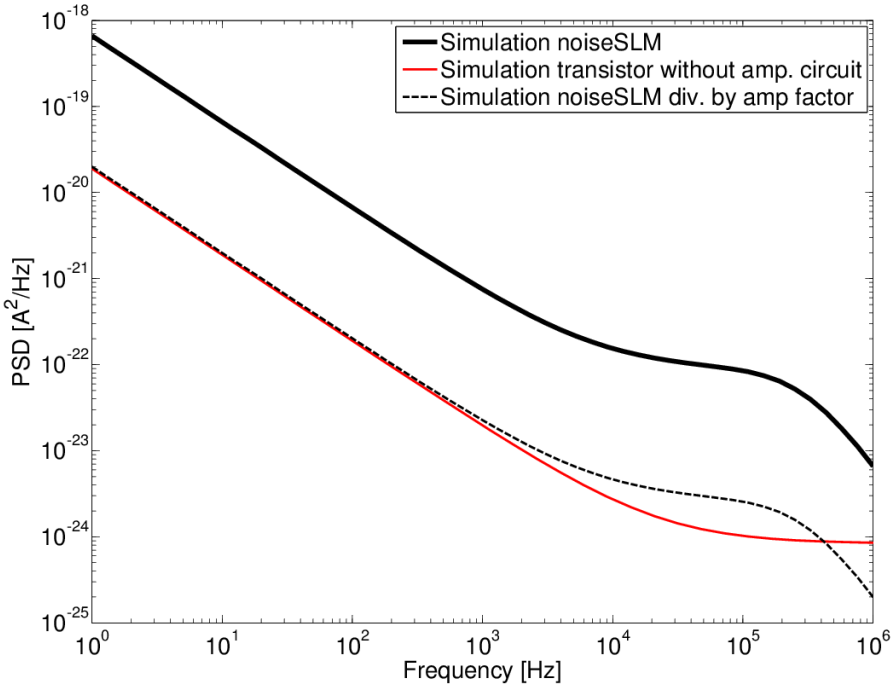


Figure 2.16: Comparison between a transistor without the amplification circuit (red line) with the noiseSLM simulation (black bold line). The noiseSLM noise was divided by the circuit amplification factor of 33.2 (black dashed line).

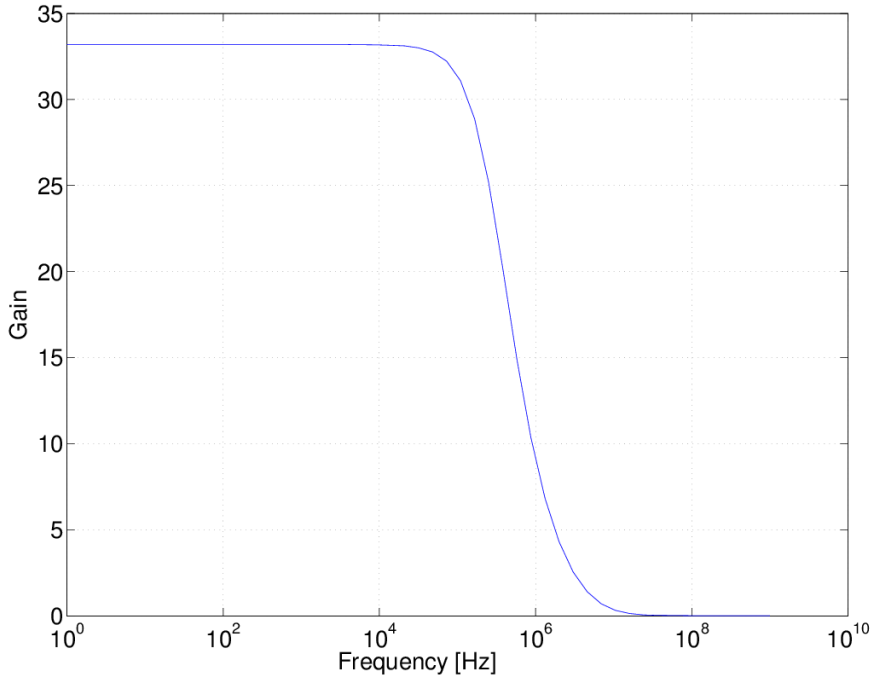


Figure 2.17: Gain is constant over the frequency rage of interest ($\ll$ 10 kHz).

The roll off above 100 kHz is a consequence of the parasitic capacitances and resistances in the transistors. It can be explained through the connection between the angular frequency ω and the first order gain H. In approximation shown in equation (2.3) [4].

$$H(\omega) = \frac{A_0}{|1 + \frac{i\omega}{\omega_0}|} \tag{2.3}$$

With ω_0 the constant angular frequency of the circuit and A_0 the constant gain factor. As long as $\omega \ll \omega_0 \Rightarrow H(\omega) = A_0$ and the gain is constant. For $\omega \gg \omega_0$ the equation becomes $H = \omega_0 A_0/\omega$ and drops with $1/\omega$. equation (2.3) is a first-order low-pass transfer function and explains the noise and gain drop above 100 kHz (figure 2.16 and figure 2.17). Since the spectrum is limited by thermal noise to frequencies $<$ 10 kHz and the gain is constant until $\sim$ 100 kHz, this is not the limiting factor.

The Power Supply Rejection Ratio (PSRR) gives the amount of noise from the power supply, that the circuit can reject. It is the ratio between output voltage change and power supply change of the circuit. The PSRR of the noiseSLM is $>$ 48 dB until 1 kHz. This gives a good screening against noise from the power supply. The PSRR over frequency is shown in figure 2.18.

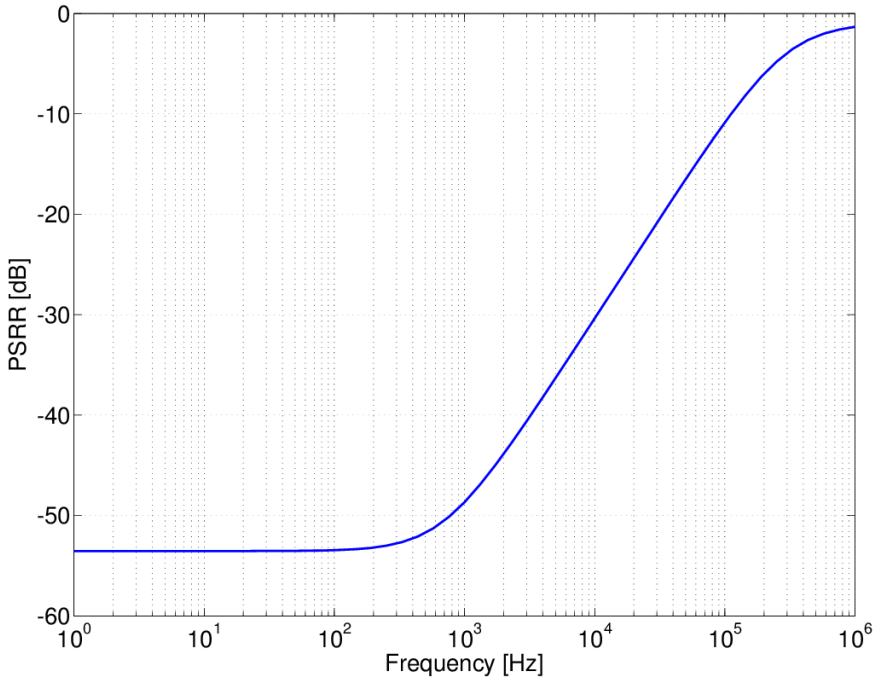


Figure 2.18: PSRR of the noiseSLM.)

2.2.2 Measurements

The measurement equipment and set-up for the noiseSLM is described in chapter 2.1.2. The noiseSLM n-channel MOSFET transistor has a gate length of 1.2 µm and a gate width of 10 µm. It is fully isolated from the rest of the wafer due to resting in an isolating well. The used technology is CMOS 0.35 µm and the gate oxide material is SiO_2. The analyzed frequency bandwidth is $10 - 1000$ Hz and the power supply is a 12V lead battery. Since the transistor is integrated in an amplification circuit, the operating point of the noiseSLM transistor M1 can't be measured, but from the simulation an estimation can be given. The values are shown in table 2.2. The following sections will present 1.) flicker noise measurements 2.) a comparison between noiseSLM measurement, noiseSLM simulation and single transistor noise characterisation and 3.)the occurring of RTS noise.

2.2.2.1 Flicker noise

Figure2.19 shows flicker noise in terms of PSD over frequency. The blue solid line shows data from a noiseSLM measurement. The data was fitted, which is represented by the red dashed line and the characteristic exponent *gamma* was extracted. $\gamma \approx 1$ and

the data form a nice straight line. This indicates that the traps are homogeneously distributed inside the gate oxide interface. There is no error showcased for single noise spectra, because the randomness of noise is bigger than the uncertainty of the measurement equipment. Instead an error will only be given for sets of measurements of the same device type in the form of standard deviation.

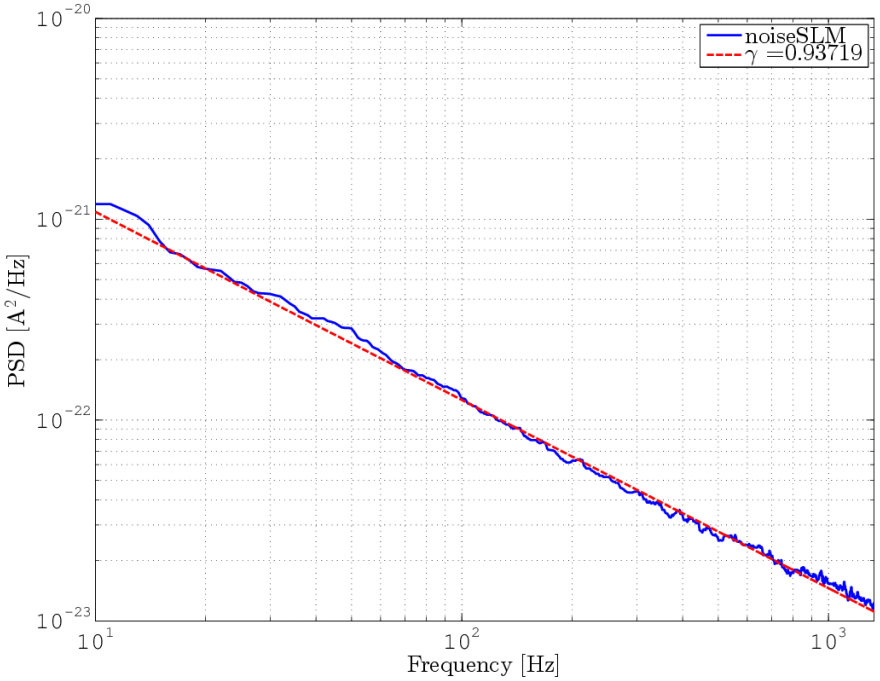


Figure 2.19: Flicker noise in PSD over frequency (blue solid line) with fit (red dashed line).

2.2.2.2 Comparison

Figure 2.20 compares averages of 11 noiseSLM measurements (blue solid line) and 12 single transistor LFN characterisations (cyan dashed line) in PSD over frequency. The single transistor LFN characterisation is plotted starting from 100 Hz due to bandwidth limitation, as explained in chapter 2.1.3. The characteristic exponent γ is extracted from fitting the noiseSLM data (red dashed line). Further the standard deviation and the noiseSLM simulation (black bold solid line) are plotted. Both averages show $1/f$ behaviour and match the simulation. This displays that the noiseSLM is working properly and can be used for noise level measurements in transistors.

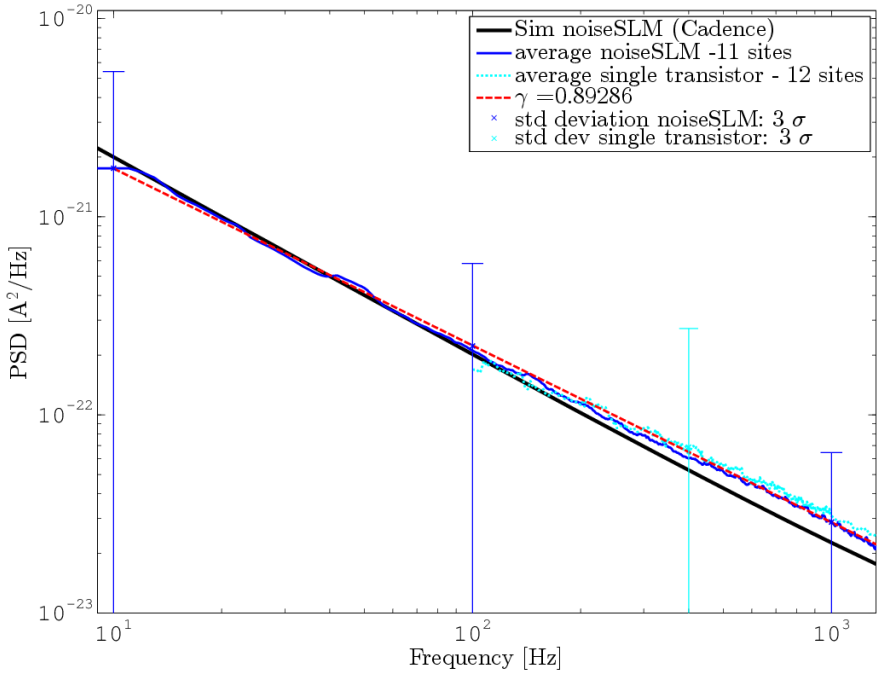


Figure 2.20: Flicker noise in PSD over frequency for the noiseSLM Simulation (black bold line), the average of 11 noiseSLM (blue solid line) with fit (red dashed line) and the average of 12 single transistor measurements. The standard deviation for noiseSLM and single transistor is shown as well.

The operating point of the single transistor should be the same, as transistor M1 experiences in the noiseSLM. Since the operating point of M1 can't be measured due to it's integration into the amplification circuit, the operating point was taken from the simulation. In the single transistor LFN characterisation V_{ds} is forced by an SMU and the values for I_{ds} and V_{gs} arise from the transfer characteristic. The simulation and measurement parameters are found in table 2.2.

Table 2.2: Transistor operating points for comparison

	V_{gs} [mV]	V_{ds} [V]	I_{ds} [µA]
M1 from Sim	570.8	3.0	3.1
Transistor (no amp circuit)	520.0 ± 1.7	3.00 ± 0.01	3.8 ± 0.02

When comparing noise data from different devices, it is best to compare averages. The noise in single devices might vary as shown in in figures 2.21 and 2.22. These 2 graphs show noise measurements of several devices in PSD over frequency (grey lines) as well

as the resulting average (black bold line). Figure 2.21 represents the noiseSLM and figure 2.22 the single transistor.

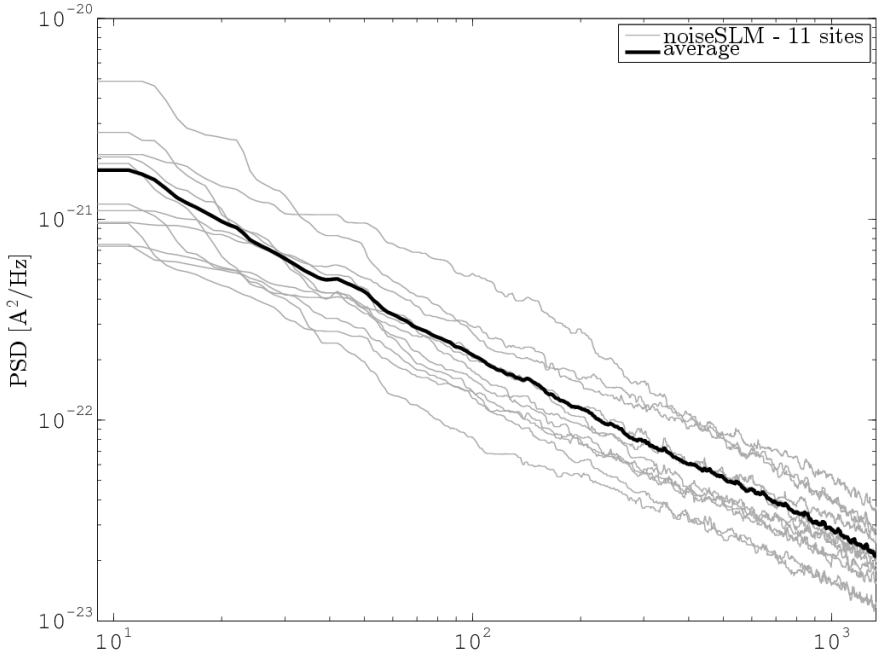


Figure 2.21: The average (black bold line) of 11 noiseSLM flicker noise measurements (grey lines) in PSD over frequency. The data shows $1/f$ behaviour.

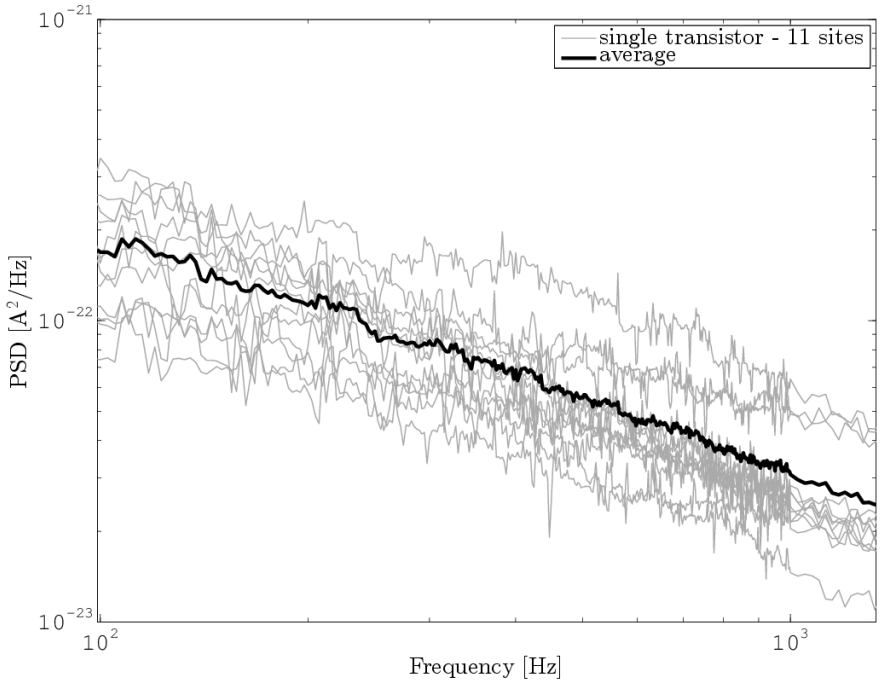


Figure 2.22: The average (black bold solid line) of 12 LFN characterisations (grey solid lines) in PSD over frequency. The data shows $1/f$ behaviour.

2.2.2.3 RTS noise

Not all measurement show characteristic flicker noise behaviour as shown in figure 2.19. This section will discuss spectra showing $1/f$ behaviour with strong RTS share. As explained in chapter 1.2, RTS noise gives a Lorentzian shape: flat plateau and then drop like $1/f^2$. Figure 2.23 shows flicker noise behaviour until $\sim$ 200 Hz with a γ_1 of 1.00 and then drops like a Lorentzian with $2\gamma_1 \approx \gamma_2 = 1.80$. A possible explanation for this behaviour is, that traps with a trapping constants τ_i smaller than a certain corner trapping constant τ_{corner} are homogeneously spread and therefore give a $1/f$ trend. Above τ_{corner} there is one dominant trap that determines the current fluctuation.

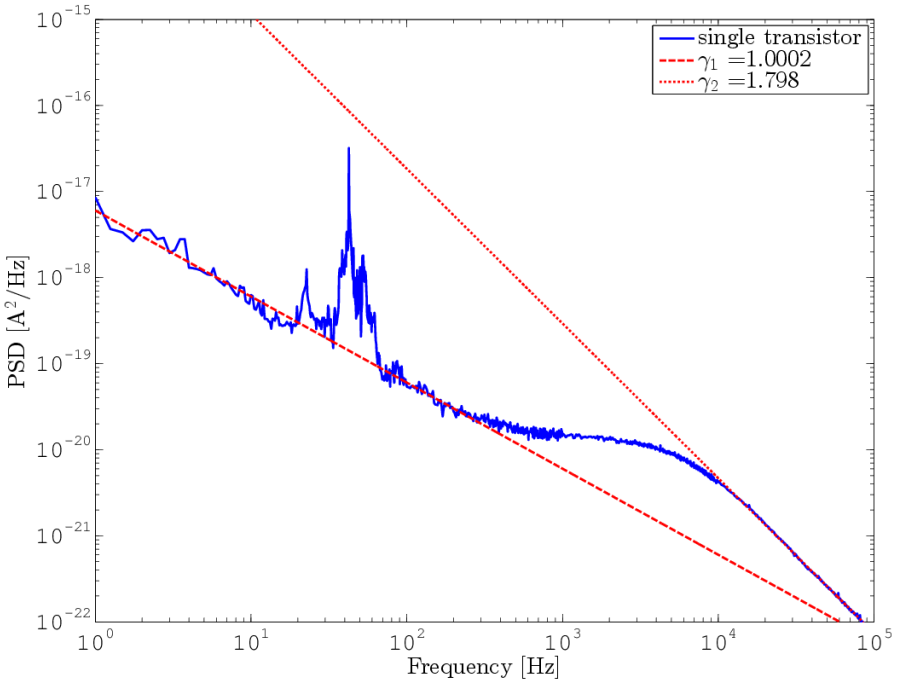


Figure 2.23: Flicker noise with RTS share.

The figures in 2.24 show time domain behaviour of flicker noise (left) and RTS noise (right). The data on the left was recorded using a high pass filter to erase the DC voltage, while the data on the right was gathered without. This has no effect on the behaviour shown here. The data comes from the noiseSLM and the voltage is measured over the 120 kΩ resistor R_1. The time domain fluctuation for flicker noise are more or less random, while the RTS signal shows switching between 2 voltage levels. The black arrows at the bottom show the time spend in the lower state τ_{low}. In average they should have the same length. The state spend in the higher state τ_{high} (red) is independent from τ_{low}, but again all red arrows should have the same average length. τ_{high} and τ_{low} represent the trapping and emission times, but it is impossible to tell which one is which. For that one has to know the responsible type of trap. The trap could be charged in it's empty state or charged in it's filled state.

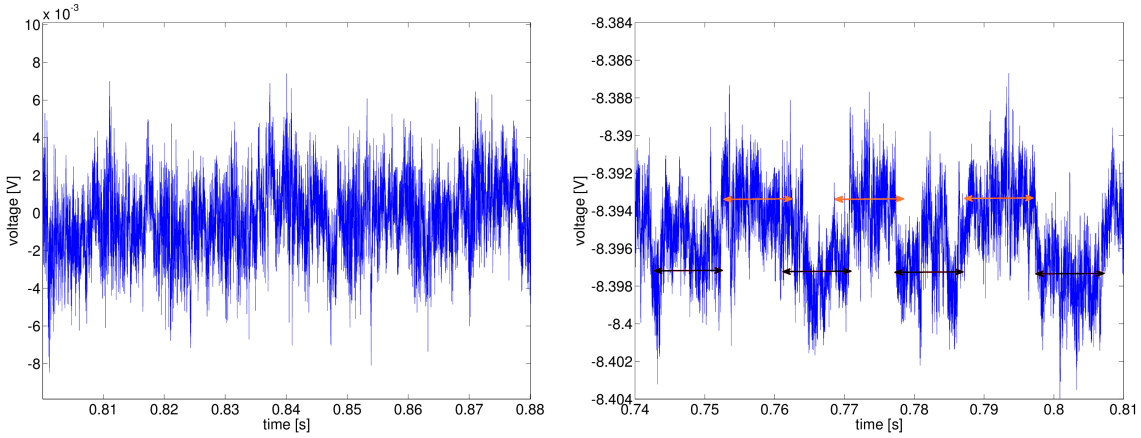


Figure 2.24: Time domain behaviour of flicker noise (left) and RTS noise (right).

Figure 2.25 shows the corresponding frequency domain spectra, calculated by taking a FFT. The measurement time is 1 second and the averaging number 100. The left graph shows flicker noise behaviour with a straight line, while the right one is taking the shape of a Lorentzian.

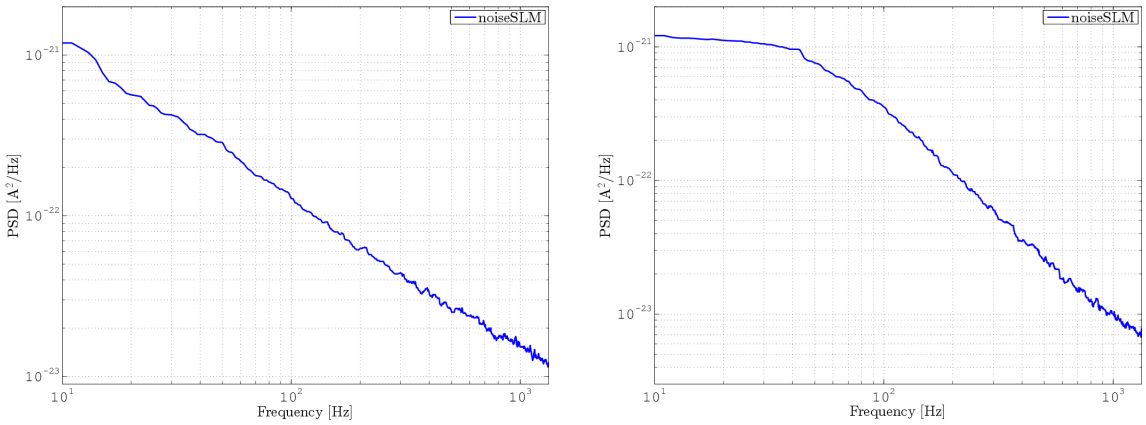


Figure 2.25: Frequency domain behaviour of flicker noise (left) and RTS noise (right) from the spectra shown in figure 2.24.

In the upcoming section "variability" a variety of wafer sites is measured and the average is taken. When taking the average of noise data one has to be careful, since RTS noise tends to add up to $1/f$ behaviour. In figure 2.26 7 sets of RTS noise data is shown. The black bold line represents their average, It forms a straight line with $\gamma \approx 1$. This shows that it's not possible to make statements about the noise mechanism by only looking at the average. For that reason all sets of data in the "variability" section

are checked beforehand and sets that are not flicker noise are discarded for the analysis. This is especially important in chapter 2.3, because the used models wouldn't be valid any more.

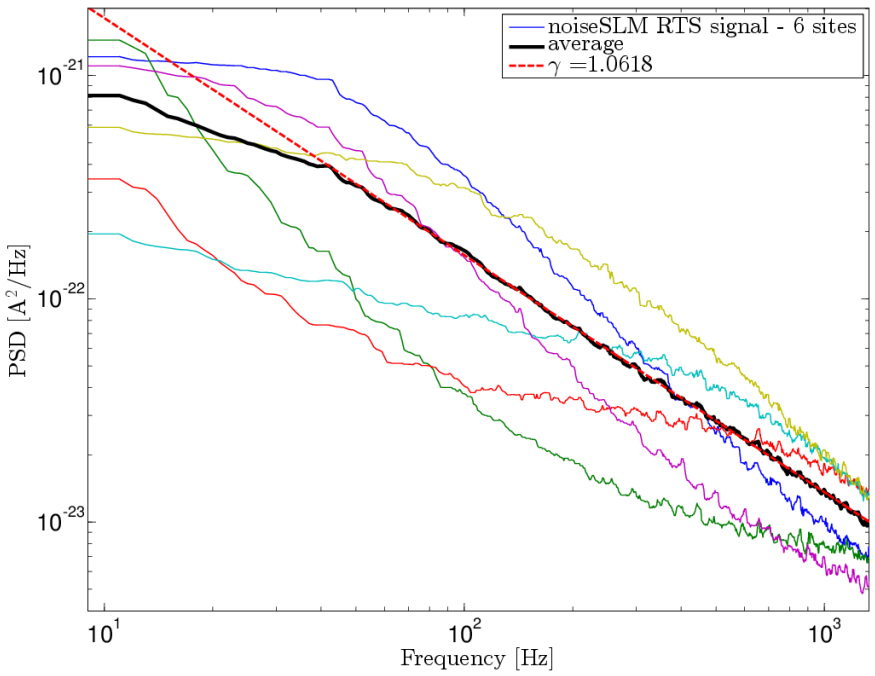


Figure 2.26: RTS noise sums up to $1/f$ behaviour.

As mentioned in the introduction, traps are only contribution to noise if the trap energy level is close to the Fermi energy. Only then capture and emission times are about the same and the trap is not empty or filled most of the time. The trap energy level is changing with the transistor biasing conditions. An example is given in figure 2.27. At an operating point of $V_{gs} = 2.06$ V, $V_{ds} = 3.00$ V and $I_{ds} = 999.08\,\mu$A, there is one dominant trap determining the current fluctuation. The result is RTS noise. By lowering I_{ds} one can see the RTS share becoming less and less significant until there is only flicker noise. This points out a weakness of the noiseSLM. Since the operating point is fixed, no statement can be made about noise levels at different biasing conditions. One has to be aware that the noiseSLM can not replace a LFN characterisation. It is a fast and easy tool for monitoring noise levels in first estimation.

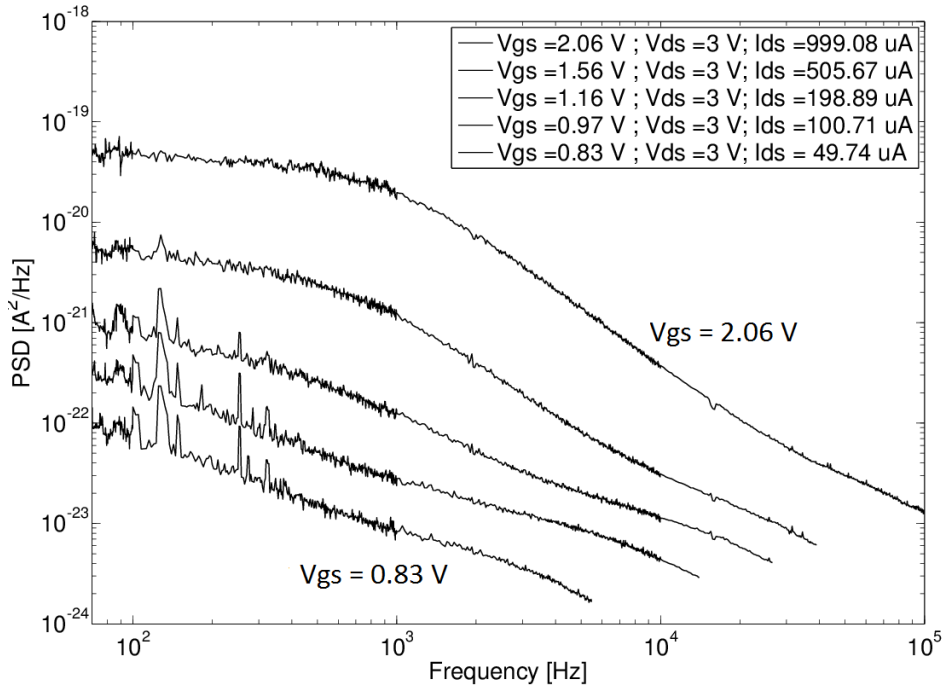


Figure 2.27: Trap behaviour for different bias conditions

2.2.2.4 The influence of implants on the noise level

This section will take a look at the variability plots of multiple noiseSLMs on the same wafer. The analysis is exclusively dealing with flicker noise, any deviation from that behaviour won't be considered. The measurement set-up is the same as described in chapter 2.1.2 and the frequency range of interest is $10 - 1000$Hz.

Each of the following figures represents a different wafer. Within each figure the noise data comes from different sites of the same wafer. The figures show the noiseSLM PSD over frequency (blue lines). The errorbars (red bars) in form of standard deviation are taken at 10, 100 and 1000 Hz. For each of the three frequencies the mean is taken and a fit is done. the noise level at each mean is marked. From the fit, the characteristic exponent γ is extracted.

The wafers analysed in this section have experienced 2 different noise-influencing treatments. The exact details of the treatments will not be discussed, but an overview of the processes is given. The first treatment is an implantation of material α into the amorphous polycrystalline silicon, to lower the number of traps at the gate oxide interface. The second treatment is an implantation of material β into the same area. The purpose of β is to form a better ohmic contact with the gate. The cross section of a MOSFET showing the location of SiO_2 and polysilicon can be seen in figure 2.28. Both treatments have been done for a fixed implantation energy and varying implantation dose. The abbreviations are shown in table 2.3. A rising index stands for an increasing implantation dose.

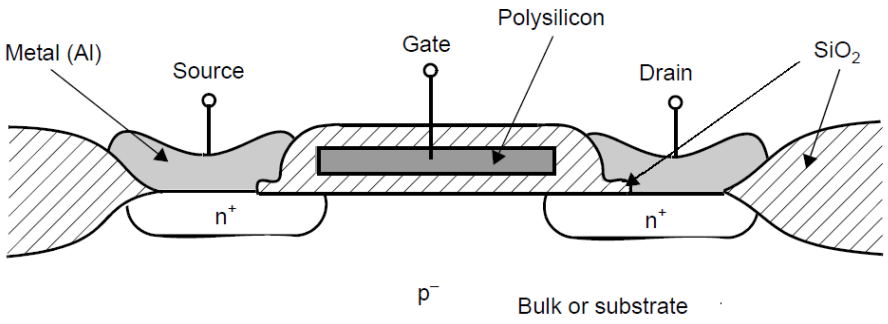


Figure 2.28: Cross section of n-channel MOSFET [4].

Table 2.3: Abbreviations for implant dose of material α and β. A rising index stands for increasing implantation dose.

	Gate-Oxide	**Polysilicon**
Implantation	$\alpha_1 - \alpha_4$	$\beta_1 - \beta_3$
No implantation	α_{no}	β_{no}

Table 2.4: Wafer treatment overview. The wafers are grouped by comparability and sorted by increasing noise levels. Direct comparisons are not divided by a horizontal line.

Wafer-Nr.	**Treatment**	**PSD @ 100 Hz [A^2/Hz]**
1	α_2 β_3	1.61E-23
2	α_1 β_3	2.87E-23
3	α_4 β_1	2.21E-23
4	α_3 β_{no}	4.29E-23
5	α_3 β_1	7.32E-23
6	α_{no} β_2	1.84E-22
7	α_{no} β_3	2.22E-22

Wafer 1 and 2 have the same β concentration in polysilicon, but different α concentration in the gate oxide (figure 2.29 top and bottom). The comparison shows that a slight concentration increase from α_1 to α_2 reduces the noise in the transistors. Wafer 3 has the highest concentration α_4 in the gate oxide and a low concentration β_1 in the polysilicon (figure 2.30 top). This results in the second lowest noise level, between wafer 1 and 2. Wafer 4 and 5 show the influence of the β implantation. While wafer 4 has no implant, wafer 3 has a low concentration (figure 2.30 bottom and 2.31 top). This low concentration implantation rises the noise level noticeably. This behaviour stays true for wafer 6 and 7 (figure 2.30 bottom and 2.32). There is no implantation of α and an increase from β_2 to β_3 raises the noise level.

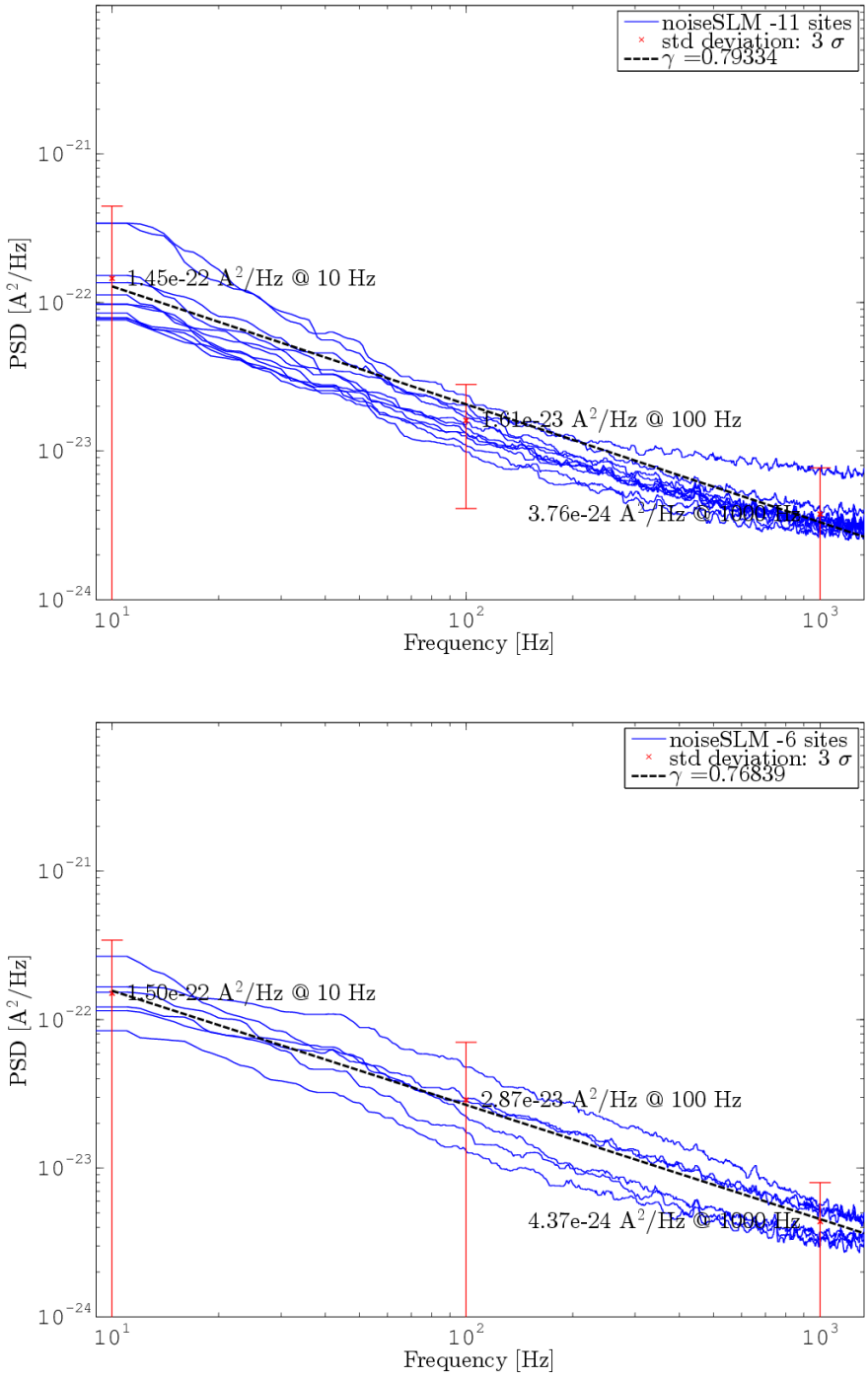


Figure 2.29: NoiseSLM Variability plot in PSD over frequency (blue lines) for wafer 1 (top) and 2 (bottom). The standard deviation of 3 σ is shown for 10, 100 and 1000 Hz (red bar). The characteristic exponent γ is extracted from fitting the average of the 3 frequencies (black dashed line).

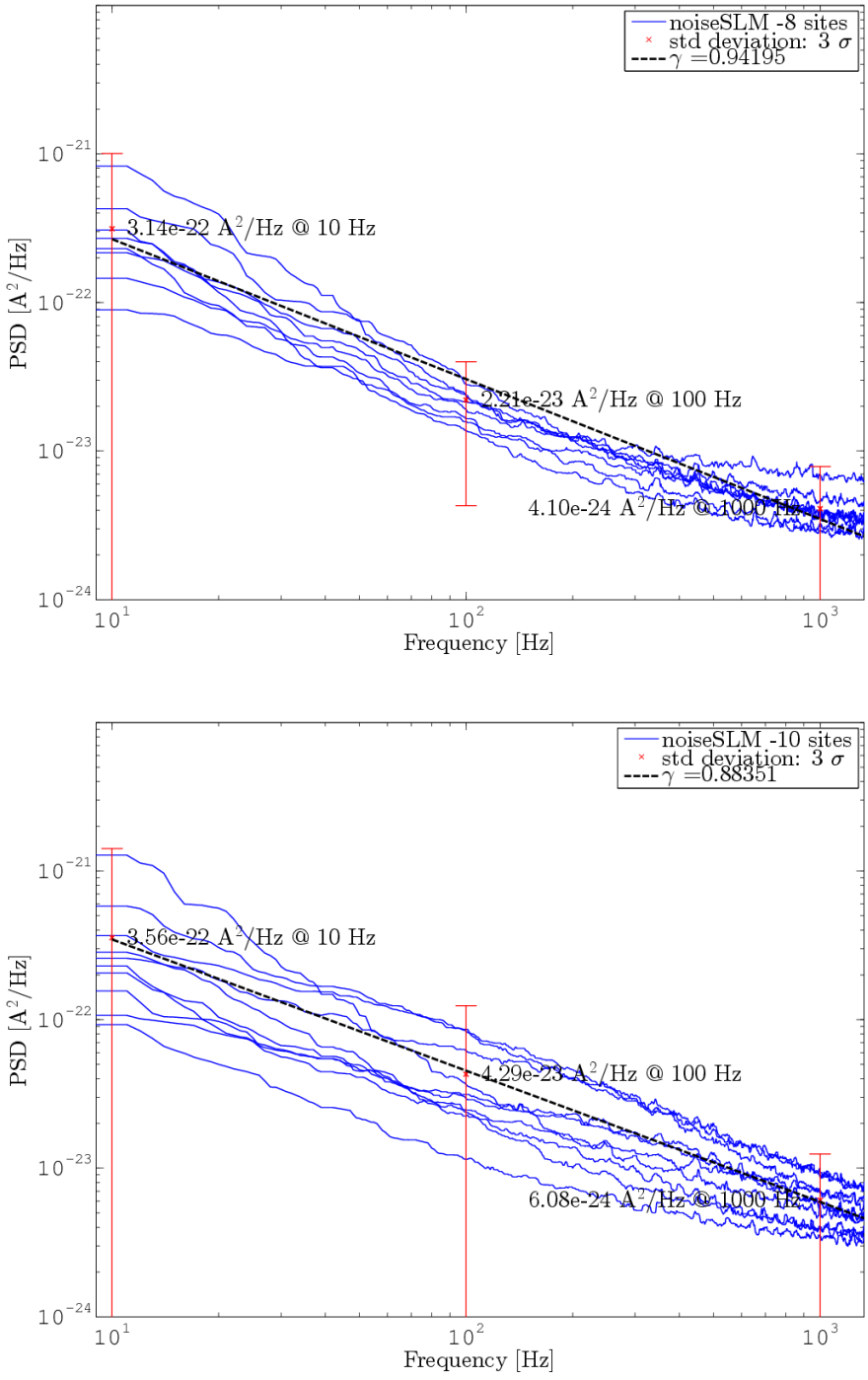


Figure 2.30: NoiseSLM Variability plot in PSD over frequency (blue lines) for wafer 3 (top) and 4 (bottom). The standard deviation of 3 σ is shown for 10, 100 and 1000 Hz (red bar). The characteristic exponent γ is extracted from fitting the average of the 3 frequencies (black dashed line).

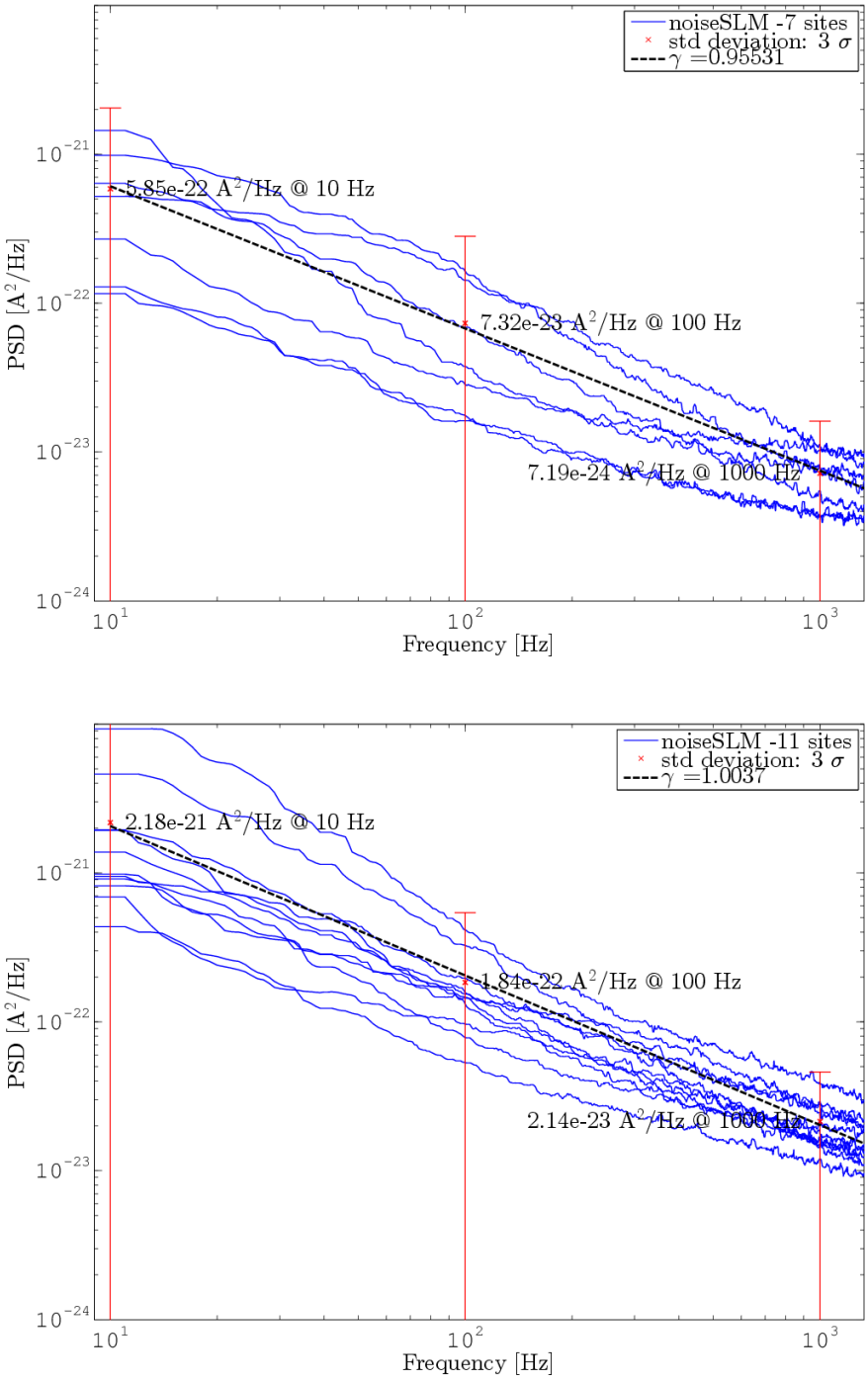


Figure 2.31: NoiseSLM Variability plot in PSD over frequency (blue lines) for wafer 5 (top) and 6 (bottom). The standard deviation of 3 σ is shown for 10, 100 and 1000 Hz (red bar). The characteristic exponent γ is extracted from fitting the average of the 3 frequencies (black dashed line).

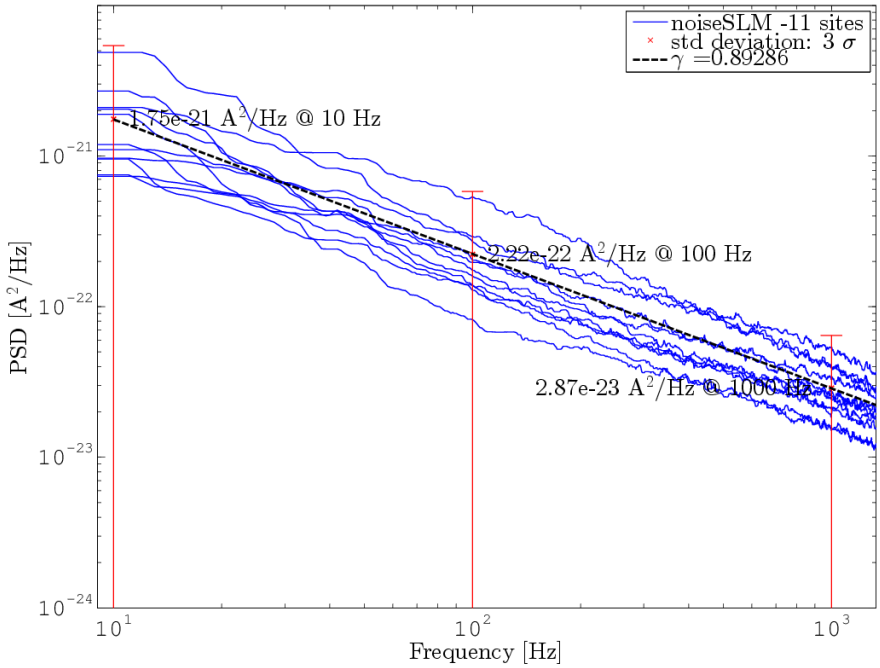


Figure 2.32: NoiseSLM Variability plot in PSD over frequency (blue lines) for wafer 7. The standard deviation of 3 σ is shown for 10, 100 and 1000 Hz (red bar). The characteristic exponent γ is extracted from fitting the average of the 3 frequencies (black dashed line).

The analysis of several wafers with different concentrations of material α in the gate oxide and material β in the polysilicon led to the conclusion that a rise of the α concentration reduces the noise, while an β increase rises the noise level.

2.2.2.5 NoiseSLM in process environment

This section discusses noiseSLM measurements taken in a process environment and compares them with results gained from the benchmark prober. For the prober used in the process environment no modified needle card can be used and the space under the coverage is too small to fit the battery. Therefore disturbance susceptible parts like the resistor, cables and power source have to be placed outside as shown in figure 2.33. This is not an optimal set-up, since the disturbances influence the noiseSLM and the ADC. Corrupted measurements will be discussed below. Besides that, the measurements were successful and led to believable results.

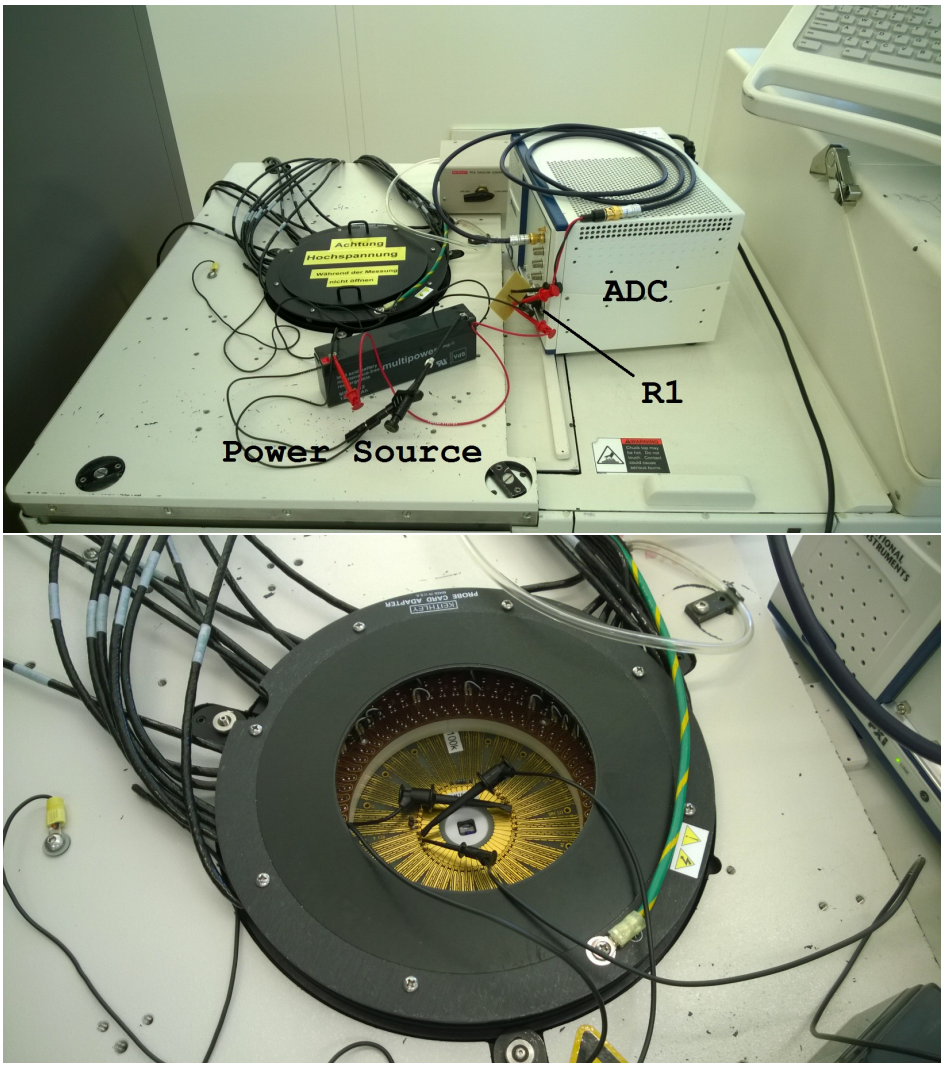


Figure 2.33: The top picture shows the measurement set-up for the process environment noiseSLM measurement. In the bottom picture a connection between needle card, ADC, resistor R_1 and power source is made through cable clamps.

Six noiseSLM measurements were taken, 4 were successful and 2 showed corruption due to external influences. The non-corrupted measurements show credible noise behaviour and are presented in terms of PSD over frequency in figure 2.34 (blue lines). The average of the 4 lines was taken at $10, 100$ and $100\,\mathrm{Hz}$ and fitted (black dashed line). The resulting γ can be found in the figure legend. The PSD value for each of the points can be found next to them. For a better comparison the expected value from the simulation is represented by the black bold line. The red bars indicate the standard deviation of 3 σ.

The corrupted measurements show a plateau in the frequency domain, followed by

an Lorentzian-like drop with γ values > 2.5 (figure 2.36). The time domain signal of the same data can be seen in figure 2.37. It shows switching between 2 voltage levels. This behaviour is superimposed, since the background noise measurement, without any needle contact, shows the exact same behaviour. The likely explanation is, that the ADC picks up a frequencies from a neighbouring machine through the unshielded cables. This external machine emits not continuously, therefore not all the measurements are influenced. The Lorentzian behaviour in figure 2.36 comes from a similar voltage level switching distribution as for RTS signals. A background noise measurement taken 30 minutes after the first one shows normal behaviour.

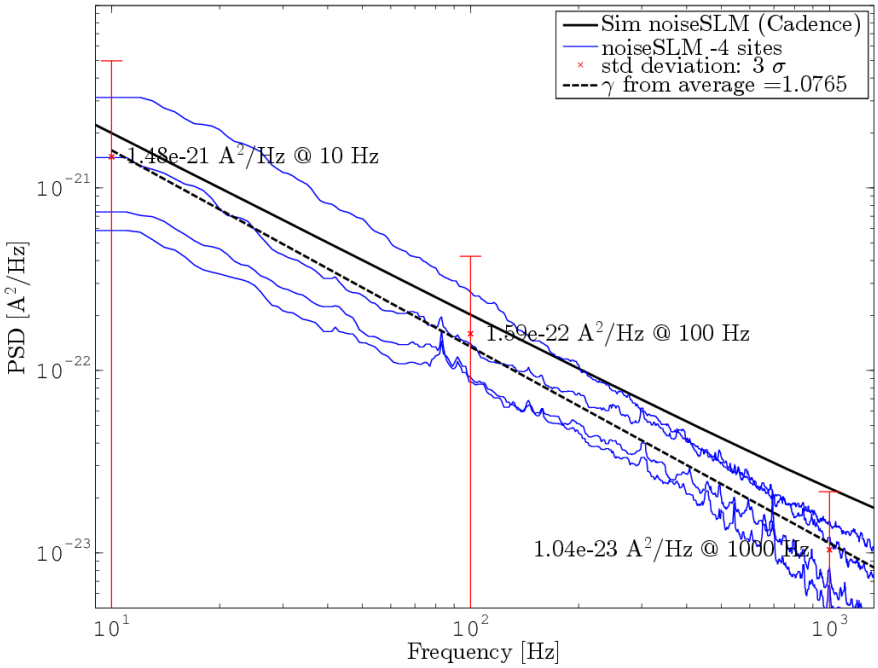


Figure 2.34: PSD over frequency for 4 noiseSLMs (blue lines), measured in the process environment. The standard deviation of 3 σ (red bars), as well as the characteristic exponent γ from the fit(black dashed line) is shown.

Figure 2.35 compares a noiseSLM measurement between the benchmark prober (blue solid line) and the process environment (blue dashed line). The same device is analysed. The results are in the same PSD range, but the process environment γ value taken from the fit is high.

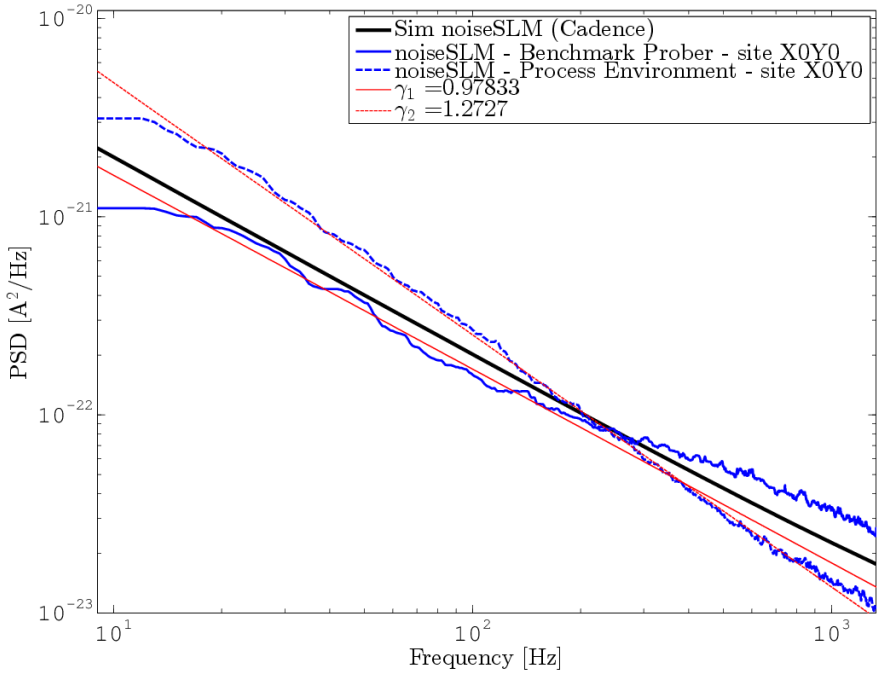


Figure 2.35: Comparison between the PSD behaviour of the same noiseSLM measured at 2 different locations (blue lines) as well as the simulation of the noiseSLM (black bold line). The γ values have been extracted from the corresponding fits (red thin lines).

The noiseSLM measurements in the process environment are working, but there are some optimisations necessary. The whole measurement set-up needs shielding against electrical disturbances to prevent corruption. The battery should fit within the prober, as well as the resistor R_1. All cables outside the prober need coaxial/triaxial shielding.

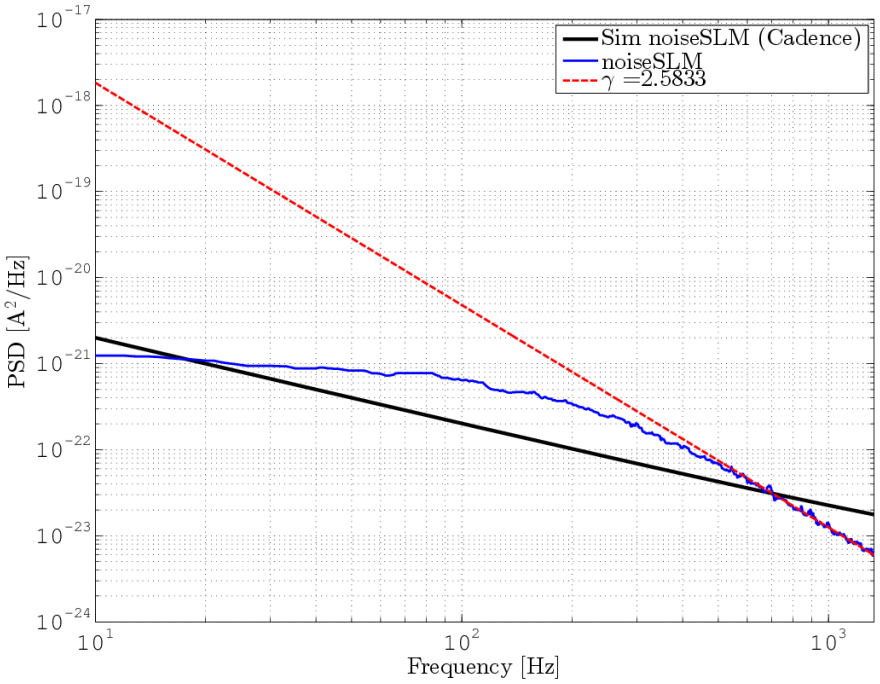


Figure 2.36: Process environment noiseSLM measurement in PSD over frequency (blue line). The noise spectra shows Lorentzian behaviour due to superimposed external frequencies.

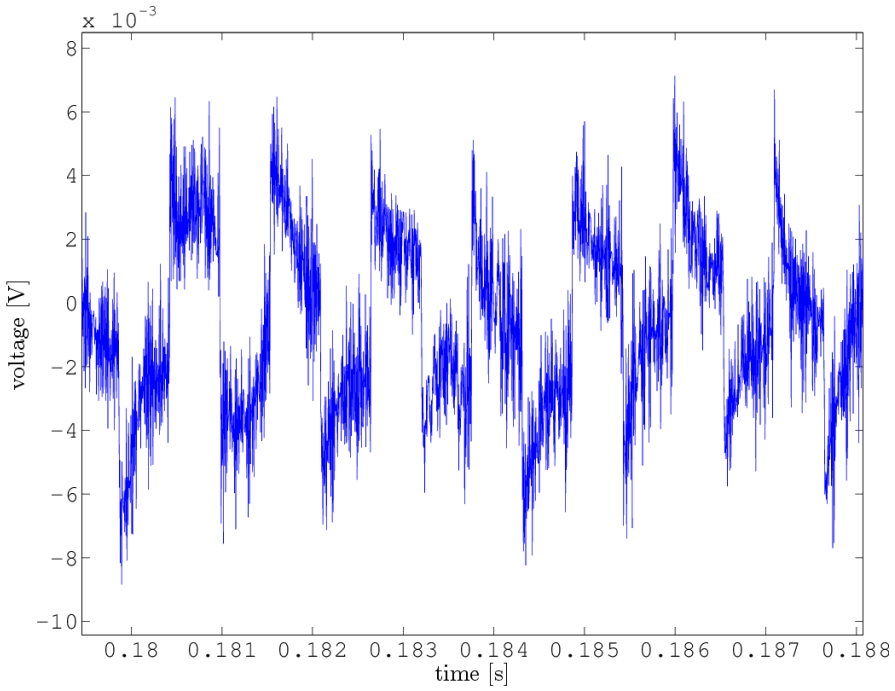


Figure 2.37: Time Domain signal in voltage vs. time from the data presented in figure 2.36. The data shows superimposed switching between 2 levels from external sources.

2.3 Noise as a characterisation tool

2.3.1 Extraction of volumetric trap density

In this section the procedure of extracting the volumetric gate trap density from isolated MOSFETs for different drain currents will be discussed following the methodology in chapter 2.1.4. The CMF model and the CNF model are explained in chapter 1.2. Ten drain currents on a single wafer site will be tested. The measurement set up is the same as in chapter 2.1.3. The drain-source voltage V_{ds} is kept constant at 3 V, the gate area has a length of $L = 1.2\,\mu m$ and a width of $W = 10\,\mu m$ and the temperature is $T = 27°C$. The used drain currents are:

$I_{ds} = 0.1996, 0.0998, 0.0998, 0.0499, 0.0201, 0.0101, 0.0051, 0.0020, 0.0010, 0.0005,$
0.0003 [mA]

And the resulting transconductance g_m:

$g_m = 0.6130, 0.4419, 0.3079, 0.1827, 0.1188, 0.0743, 0.0377, 0.0216, 0.0120, 0.0052$ [mS]

In figure 2.38 the noise data (solid line), the CMF model (dashed) and the CNF model (dotted) are compared. At smaller drain currents both models fit the data quite well. Only at higher drain currents the CNF model starts to smear off, while the CMF model is still keeping the same behaviour.

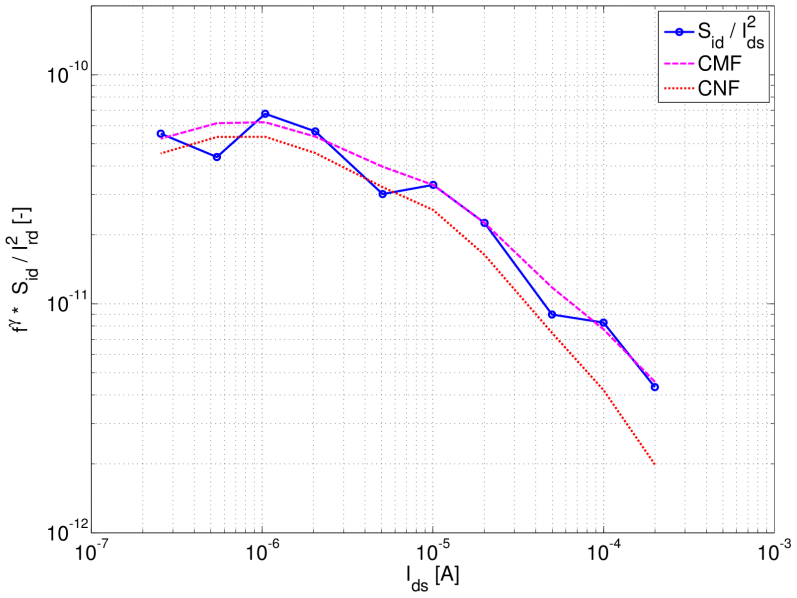


Figure 2.38: Comparison between data, CMF model and CNF model

From equation (1.18) one can see that the normalized drain current noise $S_{I_d}/{I_d}^2$ and $(g_m/I_d)^2$ are related through a constant factor. Therefore plotting them should give a straight line as can be seen in figure 2.39. In order to calculate the flat band threshold voltage V_{th} from equation (1.19) we take the square root. It shows the behaviour of a linear equation $y = kx + d$ as can be seen in equation (2.4).

$$\sqrt{S_{V_g}} = \sqrt{S_{V_{fb}}}\Omega\frac{I_d}{g_m} + \sqrt{S_{V_{fb}}} \tag{2.4}$$

With $\Omega = \alpha\mu_{eff}C_{ox}$. By fitting a line through the data points in figure 2.40 we can extract $S_{V_{fb}} = 1.44E-14$ [V^2/Hz] and $\Omega = 1.58E-4$ [cm^2/V].

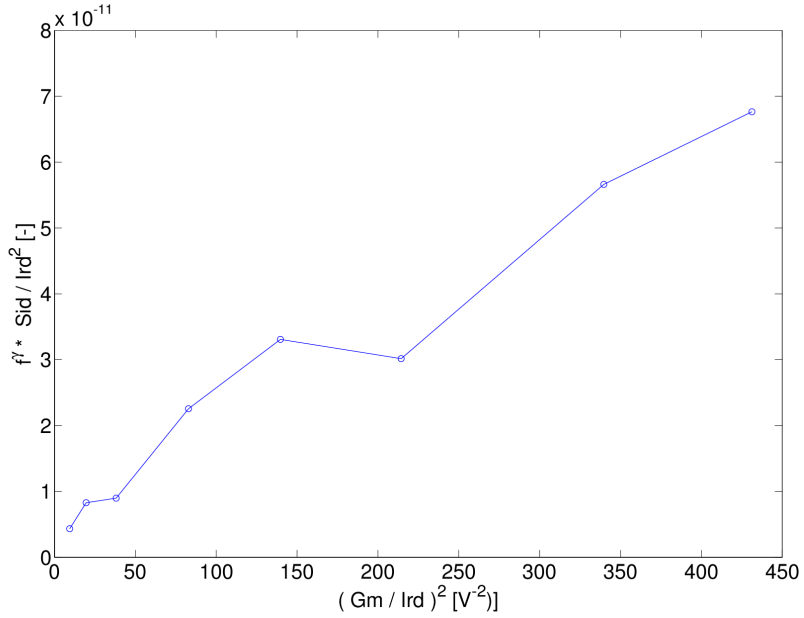


Figure 2.39: $S_{Id} * f^{\gamma}$ and g_m/I_{rd} are related through a constant

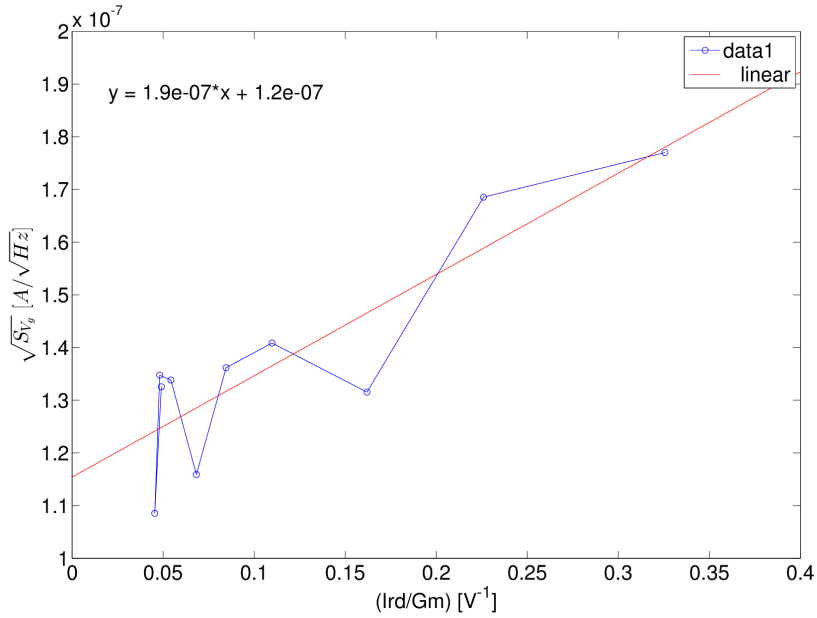


Figure 2.40: Extraction of Ω and $S_{V_{fb}}$

We can now calculate the volumetric trap density from:

$$S_{V_{fb}} = \frac{q^2 k_B T \lambda \mathbf{N_t}}{W L {C_{ox}}^2} \left(\frac{f_0}{f}\right)^{\gamma} \tag{2.5}$$

$\mathbf{N_t = 5.59E + 13\ [1/(eV\ cm^3)]}$ with $\gamma \approx 1$. λ is the tunnel attenuation distance (≈ 0.1 [nm]).

Chapter 3

Conclusion

For this work a low frequency noise measurement technique for transistors, using an on-chip amplification circuit was investigated. The noise of this circuit (noiseSLM) is determined by one significant transistor M1. M1 is a n-channel MOSFET with a gate length of 1.2 µm and a gate width of 10 µm. The technology is CMOS 0.35 µm. The gate material is polysilicon and the oxide material SiO_2. The analysis focuses on flicker noise.

The behaviour of the noiseSLM was simulated, using the program Cadence (chapter 2.2.1). This yielded the amplification factor of 33.2 , as well as the operating point of M1 ($V_{gs} = 570.8\,\mathrm{mV}$, $V_{ds} = 3.0\,\mathrm{V}$ and $I_{ds} = 3.1\,\mu\mathrm{A}$). The contribution of the single devices in the circuit to the total noise can be be found in table 2.1. From this the frequency range $10 - 100\,\mathrm{Hz}$ for the measurements was determined. Lower frequencies are too time consuming, while at higher frequencies M1 is not dominating the noise any more. It was ensured that the gain and the power supply reject ratio is constant for this frequency range.

The noiseSLM was measured and the resulting PSD spectra were compared with the PSD of single transistors (chapter 2.2.2.2). For the comparison of noise data, always the mean of several measurements was used, due to the random nature of noise. The noise behaviour of the noiseSLM and the single transistor are matching, showing that the noiseSLM is working properly. The NoiseSLM measurement and simulation are matching as well. The comparison of all three is presented in figure 2.20.

The occurrence of RTS noise was discussed and the data analysed in frequency and time domain (chapter 2.2.2.3). The danger of mistaking means of RTS noise as flicker noise was pointed out and an example is shown in figure 2.26. The activation and deactivation of a single trap, in dependence on bias conditions, is shown in figure 2.27.

The influence of implants on the transistor noise levels was investigated in chapter 2.2.2.4. Different concentrations of material α were implanted in the gate oxide and different concentrations of material β in the polisilicon. The influence of the implants on the noise levels can be found in table 2.4 and the according PSD spectra are in figures 2.29 - 2.32. Is was concluded that an increasing implantation concentration of material α in the gate oxide lowers the noise. An increase of material β raises the noise levels in the transistor.

The long term plan for the noiseSLM is to be integrated into the production line and give information about the noise levels right after production. For this reason a set of measurements were done in a process environment. They can be found in chapter 2.2.2.5. The results are compared with the ones from the benchmark prober in figure 2.35. Even the measurement in the process environment is working, there are still some issues to overcome. The used prober did not have enough space to fit vital parts of the measurement set-up. Therefore some unshielded parts were exposed to external influences which are showing up in the results. A better shielding of the system should solve the problem. The process environment measurements are shown and discussed in figure 2.34.

Chapter 2.3 explains how to extract the volumetric gate trap density from noise spectra. The measurements have been done, using a single transistor with the same dimensions and channel-type as M1 in the noiseSLM. The resulting volumetric oxide trap density is $N_t = 5.59\text{E}{+}13\,[1/(\text{eV}\,\text{cm}^3)]$. Further the parameters for the carrier number and carrier mobility fluctuation model were extracted. The models are plotted and compared with the experimental data in figure figure 2.38. For this transistor the carrier mobility model is a better fit, since the carrier number fluctuation model is deviating from the measurement data at higher frequencies.

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