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Design of a Precision Sine Wave Amplitude Detection Circuit

Master's Thesis

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Finally, I must express my very profound gratitude to my wife, Kathi, showing me unfailing support and continuous encouragement. The patience and understanding she had, is something I will never forget.

This accomplishment would not have been possible without them. Thanks to all of them.

Richard Pregetter

Abstract

This thesis documents the development of a precision sine wave detection circuit. The goal is to precisely measure the amplitude of a given sine wave signal in a noisy environment, as this solution will be used in an automated test environment and will extend the analog capability of the system already in place.
First, an analysis of the currently running test setup and the requirements for the measurement circuit are discussed. Different approaches are presented and compared to each other. An ADC based solution is then implemented by designing a prototype board that houses all necessary components. Important design features are described and considerations regarding the performance of the circuitry are explained. After discussing the signal processing that is implemented, the measurement results of the precision sine wave detection circuit are presented and the performance is evaluated. The result is an easily scalable module based approach that is able to capture low amplitudes in a noisy environment. By undersampling the input signal and using signal processing to determine the final result, the findings in this thesis are applicable to existing systems that feature an ADC and a microcontroller with rudimentary DSP capabilities.

Contents

1 Introduction

1.1 Defining a starting point

To start the research of the measurement module an analysis of the currently used setup is helpful. The amplitude measurement circuit will be part of the automated test environment at the NXP research and development site in Gratkorn (Austria) as well as manufacturing sites abroad. Those setups did include different approaches over their respective development cycles, which are taken into consideration

1.1.1 Description of the test setup

The test setup as used at the NXP site in Gratkorn is built around a J750 ATE platform. This is a complete solution for parallel testing of digital components such as microcontrollers, FPGA, and digital audio/baseband devices. It provides up to 1024 input/output pins that can be independently used with different timing and voltage resources. Digital signals can be read or written with up to 100 MHz and there is 16 Mbit vector memory for each pin available. This tester is mostly used for digital signals, but provides some analog features too.
The analog to digital converters available in the tester are able to capture DC values but are not suitable to convert time varying signals of higher frequencies. They open up possibilities to sample analog data but are not able to track high frequency signals of 13.56 MHz as needed for amplitude measurement of NFC carriers. The sampling frequency is too low to fulfill the Nyquist-criterion at this frequency and therefore the best solution is, to

sample for a given time and take the highest sample value captured. The time needed to reach a high accuracy through this approach is too much for repeated tests during production. It is also not sure, that even after a certain period the correct amplitude or peak value is detected. Therefore, this solution does not fulfill the standards that are needed in this test environment.
Two different approaches can be taken to set up a test routine that is both fast enough and has a suitable accuracy and dependability to fulfill the requirements that are discussed later on. One option would be external sampling, using an analog to digital converter for sampling and a DSP to calculate and forward the measured amplitude or peak values to the tester. The other option would be to capture the signal with an analog circuit that then provides a slowly changing voltage that represents the amplitude or the peak value. This output voltage effectively provides an envelope of the input signal, which can then be sampled by the ADC of the J750.
While running the test routines an external circuit provides the signals that should be measured. These are currently differential signals at the RX pins of the NFC chip under test. This input signal is generated either through a heavily filtered rectangular waveform provided by the J750 or through direct digital syntheses by an AD9834.

1.1.2 Peak-Peak measurement with the J750

As of now the J750 tester is used for peak-peak measurement directly. The sine wave is sampled and then compared to a pattern burst. Every time the sine wave is higher than the compare level, an error is logged. If too many errors occurred, the pattern level is increased. This is done in a successive approximation method until the number of errors reaches a predefined end value.
This method is slow and lasts several hundred milliseconds per device under test until completion and in addition reaches an accuracy of only 10%.

2 Requirements and Constraints

2.1 What is limiting the possible solutions?

When looking at the task of measuring the amplitude of a sine wave, it does not seem as a difficult undertaking. Oscilloscopes and frequency analyzers do it with accuracy that is suitable for most applications. The problem becomes more complex when there are stricter limitations to power consumption, measuring time, storage and computation resources, space and also user interaction. A sine wave could be measured with an oscilloscope, a computer to automate the process and test personal that reacts according to the result that is provided. This is not a suitable solution in case of testing during production.

As mentioned in the introduction, an automated test system is already in place and therefore the module that shall be integrated to measure the sine wave is restricted by different constraints.
In general, the space that can be used for the amplitude detection module is limited due to the mechanical mounting of the test board, the layout of the test board and the position of the module.
The tester that is used, a J750 from Teradyne, together with the hardware already connected to it, limits the number of pins that can be used to control the module. Supply current and voltages are also set by this system.

At last, the signal that shall be measured and the time that can be used to do so limit the possibilities further and will lead to a final set of possible solutions that will be discussed.

2.2 Constraints for this project

For possible solutions the limitations are discussed in the next sections. They will be split up and explained in detail to set a framework, which is used to find the best suitable approach.

2.2.1 Space constraints

The final circuit of the module shall be placed on a small PCB that is connected at a 90-degree angle towards the main PCB. This is done to provide each socket holding a device under test on the main PCB with a separate measurement circuit, to keep traces short, reduce the amount of switches needed and guaranty a low amount of load on the RX-pins at which the sine wave will be measured.
The PCB holding the amplitude measurement circuit has its connector to the main PCB on one of its long edges. The length of one socket on the main PCB defines this dimension because the module has to be mounted in parallel to the socket. The second dimension, as well as the height of the components, is limited due to the mounting mechanism of the main PCB. This leads to the maximum size of 30 mm x 20 mm x 5 mm (length x depth x height).
In addition to the outer dimensions, the layout is also restricted by the presence of another circuit on the backside of the module PCB. Components can only be mounted on the topside of the board and routing on the four existing layers is restricted by already existing traces and vias, although those can be moved as needed.

These limitations are true for the final layout. However, during the development process, a larger PCB with no restriction to size and layout can be used. For test purposes multiple solutions can be implemented on the same board. Additional space can be used for test points, alternative routing or extra components for filtering and decoupling. In the final product the space requirements shall be uphold and only one solution shall be implemented.

2.2.2 Supply constraints

For the supply of the circuit, the restrictions are given by the tester J750 and the running test setup. The tester itself can in the current setup provides $\pm 15\,V$ and $\pm 5\,V$ supplies. Those supplies are regulated, but need conditioning near the measurement circuit.
Existing and future circuits, which are powered by these supplies, limit the current that may be used by the module. For the $\pm 15\,V$ supplies $15\,mA$ can be used, for the $\pm 5\,V$ supplies $50\,mA$. In addition, the module shall have a way to power down, to reduce power consumption when the module is not needed.
The power is provided via the connector on the edge of the PCB.

2.2.3 Input Signal

An important limiting factor is the input signal. In this test setup, only a limited set of signals need to be measured.
The signal will vary from $50\,mV$ to $2\,V$ peak-peak and is provided via a differential signal-chain. Those values shall be measured with a precision of $\pm 2\%$ over the whole amplitude range. It should be noted, that the noise floor measured by the oscilloscope shows $15\,mV$.
The signal will vary at least between $400\,Hz$ and $15\,MHz$ but only the amplitude of the signal is relevant, no harmonics need to be considered, except if they falsify the measurement of the fundamental wave and this should be avoided. Even though the frequency of the input signal is in the MHz range, the samples of the amplitude measurement are only needed every ms.
No other characteristics of the sine wave are important right now and implementing additional features would force the start of a new project.

2.2.4 Environmental constraints

In addition to the above-mentioned limitations, the biggest concern is how the module will interact with signals provided to them. Restrictions are

necessary that dictate how the module influences the current test setup.
Heat dissipation is not a problem in this area and heat from the tester introduced to the module is also not high. Due to the test routines in manufacturing sites, the circuit shall be built around -40 to +125 degree Celsius components. During testing, the device under test, and therefore its surroundings are heated or cooled with airflow to simulate different ambient temperature.
Noise introduced from the module to the supply lines and its surrounding shall be kept as low as possible, but no limits are set. For the existing noise in this PCB area, no exact data is measured yet but high noise is expected.

2.2.5 Cost constraints

There are no constraints on the amount of money used during the development. This does not mean that new measurement equipment and high profile software will be acquired, but evaluation boards or low-cost software are not limiting factors.
The cost of the final circuit is also not an important factor if high priced components or boards with a higher number of layers are needed.

2.2.6 Connections

The characteristics of the I/O-pins for the J750 tester are not available, therefore, buffers for switches and clocks are necessary to use one output of the tester for multiple sites.
A clock can be provided by the tester, but because this clock is already used in multiple tests it has fixed frequencies of 25.66 MHz and 50 MHz. Integer subdivisions of those frequencies can also be generated.

2.2.7 Validation

The detection circuit shall be at first validated with a signal generator and oscilloscope. An alternative way has to be found to validate it in the final test

setup because there is no reliable way to determine if the sine wave generator in the setup is working properly without the detector and the other way around. For a validation, the module is tested with only one device under test. Multi socket functionality can introduce unforeseeable problems that could increase the development time and are therefore excluded from this thesis.
For validation, the test routine shall work isolated from any other tests. This will validate the module without the interference of any other test cycle or hardware.

2.3 General

Other than the before mentioned requirements, there are no restrictions to the approach of measuring the sine wave. One factor will be to keep the design simple to ease the development process. There is no need to complicate the design if the restrictions are met.
The circuit shall also avoid hardware trimming to achieve proper functionality, as the production of multiple boards shall be kept simple. However, the prototype board will use multiple additional passive components to disconnect certain parts of the circuit, introduce filters and impedance matching. This includes series and parallel components in supply lines, signal lines and between functional blocks of the circuit.
If possible the function of the module shall be independent of the J750 to use the same module on other testers.

3 Considering multiple approaches

3.1 Possible solutions

This chapter will discuss different solutions to measuring the amplitude of a sine wave. All requirements and limitations previously discussed will be considered. Most of the approaches were found in application notes and datasheets of general-purpose and some special-purpose components. If possible the proposed circuits are simulated to find suitable solutions without the need of developing prototypes. In most cases a simulation was not possible, as the manufacturers provide no suitable models, or the solution being microcontroller based. Only datasheets and application notes are used for discussion in these cases.

3.1.1 First simple circuits

First, some simple peak detection circuits, with increasing complexity are simulated. The first one consisting of a diode to rectify the input signal, that then loads the capacitor (3.1). If the input signal is higher than the voltage drop over the capacitor, the capacitor will be loaded. During the time, the input signal is lower than the voltage at the capacitor the diode inhibits the discharge of the capacitor. At least with a n ideal diode it would. The reverse leakage current of the diode, the parasitic resistance of the capacitor and input bias current of the operational amplifier all contribute to the discharge of the capacitor.
A resistor of 10 MΩ in parallel to the capacitor is to account for any impedance on the board. The AD8066 is chosen for an output buffer because it has a FET input that provides a low input bias current of typical 2 pA.

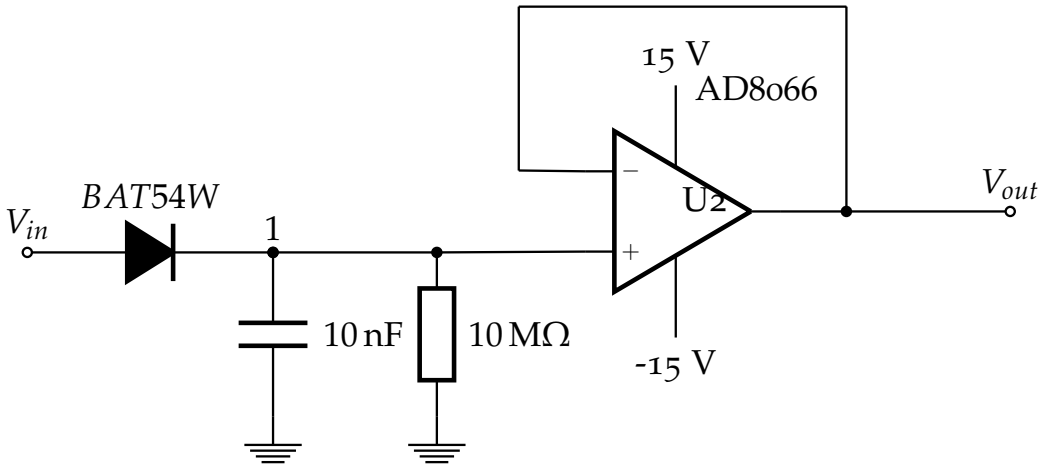

Figure 3.1: Simple peak detection circuit 1: As long as the input voltage is higher than the voltage over the capacitor current is charging the capacitor further. The input bias current of the AD8066 is lower than the current over the 10 MΩ resistor. Even though a low reverse current diode is chosen the capacitor is mostly discharged through the diode during the time the input voltage is below the voltage across the capacitor. In Addition, the forward voltage is too high, so that measurements at lower amplitudes are not possible.

Discharge of the capacitor is not the only drawback of this circuit. Due to the voltage drop of the diode, the forward voltage, the voltage over the capacitor never reaches the peak of the input signal. This offset error depends only on the diode and can vary depending on type.

The second circuit includes a feedback to compensate the voltage drop due to the diode (3.2). The negative input and therefore the node 1 is forced to the same level as the positive input. The amplifier increases the output to compensate for the forward voltage introduced by the diode.
When the input is lower than the voltage at the capacitor the output of the amplifier tries to drive the feedback to a lower value and therefore drives the output to the negative supply rail. Most of the current that discharges the capacitor flows through the diode depending on the reverse current of the part chosen.

In the third circuit, the reverse current of the diode is compensated by the introduction of a second diode in series with the first one (3.3). The feedback

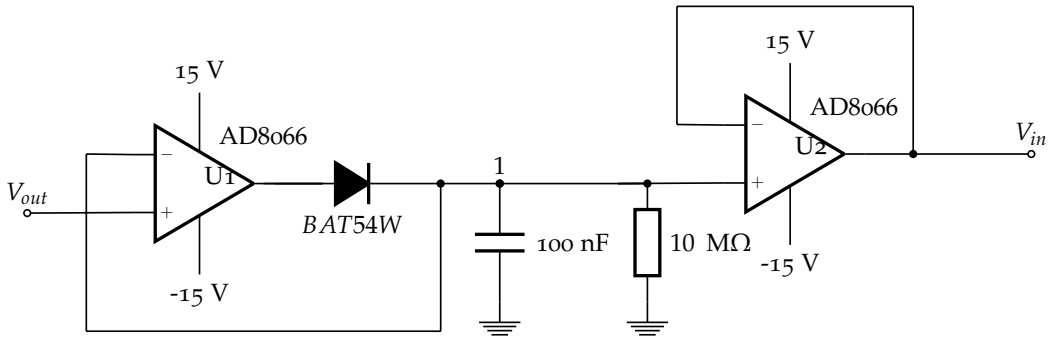

Figure 3.2: Simple peak detection circuit 2: The improvements in relation to the first circuit is, that the input amplifier compensates the forward voltage of the diode. The reverse current through the diode is still the biggest contributor to the discharging of the capacitor.

path of the input amplifier is still routed from node 1 to the negative input and the amplifier, therefore, increases its output to compensate the voltage drop of both diodes.
The output voltage of the output amplifier is the same as its positive and negative input. By connecting the output to the node between the diodes there is no voltage drop across the second diode. This means there is also no reverse current flowing through this diode and no current is discharging the capacitor through the diode.
The reverse current through the first diode is provided by the output of the output amplifier.

By introducing an input buffer and using a feedback loop from the output of the output buffer the requirements for those components rise. Both operational amplifiers need bandwidths that are high enough to accommodate the frequency range of the input signal. The slew-rate needs to be high enough to follow a 2 V peak-peak input signal with a sine wave of up to 15 MHz.
The maximum slope needed is the slope at zero crossing of the input sine wave with A being the amplitude and f being the frequency:

$$x = A \cdot cos(2\pi \cdot f \cdot t) \tag{3.1}$$

First derivation:

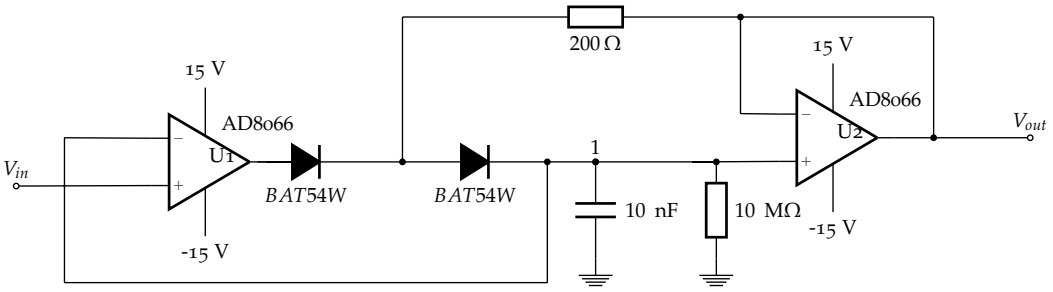

Figure 3.3: Simple peak detection circuit 3: By introducing a second diode and a feedback from the output amplifier, the voltage over the second diode is zero. Therefore no reverse current flow through the diode discharges the capacitor. The input amplifier compensates the voltage drop of both diodes.

$$\frac{\mathrm{d}x}{\mathrm{d}t} = -A \cdot 2\pi \cdot f \cdot sin(2\pi \cdot f \cdot t) \tag{3.2}$$

Maximum:

$$\left.\frac{\mathrm{d}x}{\mathrm{d}t}\right|_{max} = A \cdot 2\pi \cdot f \tag{3.3}$$

With $A = 2\,\mathrm{V}$ and $f = 15\,\mathrm{MHz}$:

$$\left.\frac{\mathrm{d}x}{\mathrm{d}t}\right|_{max} = 2\,\mathrm{V} \cdot 2\pi \cdot 15\,\mathrm{s}^{-1} = 188.5\,\mathrm{V\,\mu s}^{-1} \tag{3.4}$$

For the following simulations the AD8066 was used(*AD8065/AD8066 High Performance, 145 MHz FastFET Op Amps* 2010). With a bandwidth of 145 MHz and a slew-rate of $180\,\mathrm{V\,\mu s}^{-1}$ simulation result will show how the before mentioned circuits behave. The results were simulated in LT-Spice, using the spice models provided by the software and by Analog Devices.

The AD8066 is used for these simulations because it not only provides the bandwidth and slew-rate that is needed but also provides low input bias current of 2 pA and can deliver a reasonable high load current of up to 30 mA.

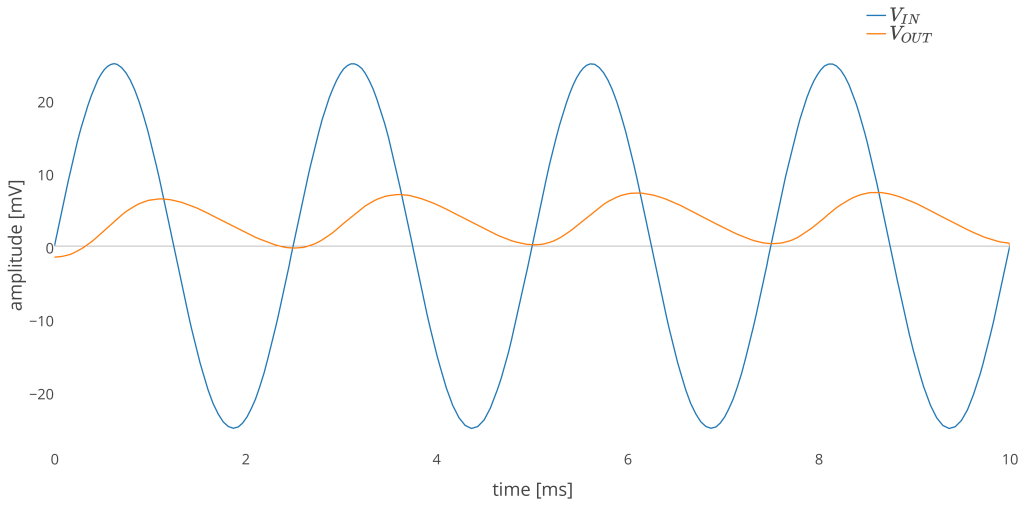

Figure 3.4: Simulation of Circuit1 (3.1): The circuit was simulated as shown in the schematic. A first a low frequency of 400 Hz with an amplitude of 25 mV was used as the input signal. The forward voltage of the diode prevents the 10 nF capacitor from being loaded

Circuit1 (3.1) can not be used with small signals down to 25 mV peak-peak, due to the voltage drop across the diode preventing the capacitor from being charged (3.4).
The red trace shows the input signal with an amplitude of 25 mV. The capacitor of 10 nF is not loaded, because the voltage drop of the diode exceeds the positive voltage swing on the input.

When simulating the second circuit(3.2), the same value for the capacitor was used. The current through the diode discharged the capacitor too fast(3.5). At [1] the peak value is not reached during the positive half-wave. Between the input maximums the output voltage droops [2] due to the reverse current through the diode. No reliable measurement is possible as long as the output swing is that high.

To reduce the influence of the current through the diode, a larger capacitor could be used but then the problem arises when simulated with a higher frequency(3.6). Still with a 10 nF capacitor at 4 MHz the slew rate of the

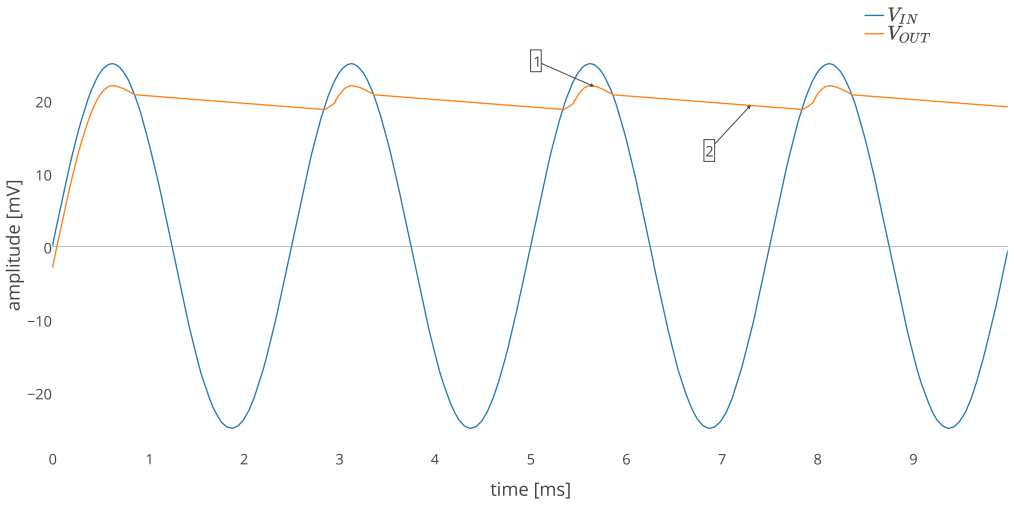

Figure 3.5: Simulation of Circuit2 (3.2): The input signal with 400 Hz and 25 mV is not able to load the 10 nF; capacitor during the positive half-wave to the maximum [1]. Between the peaks, the capacitor is discharged significantly [2].

AD8066 is not a problem, but the large capacitor can not be loaded during the time the input voltage is higher than the voltage at node 1. The current over the diode does not allow for a capacitor value that works at both high and low frequencies.

By using circuit3 (3.3) the problem of discharging over the diode should be solved. When using a 10 nF capacitor with a 400 Hz input signal, the output signal ripple is lower as with the previous circuit(3.7).

When increasing the input frequency to 4 MHz the output overshoots, probably due to the feedback circuit of the output amplifier.(3.8).

By increasing the input frequency further, the capacitor is not charged at all. This is again most certainly a problem of the feedback structure. The system is not fast enough to track those high frequencies(3.7).

This concludes the simulations of those simple peak detect and hold circuits. They were simulated with different values, but those presented here showed

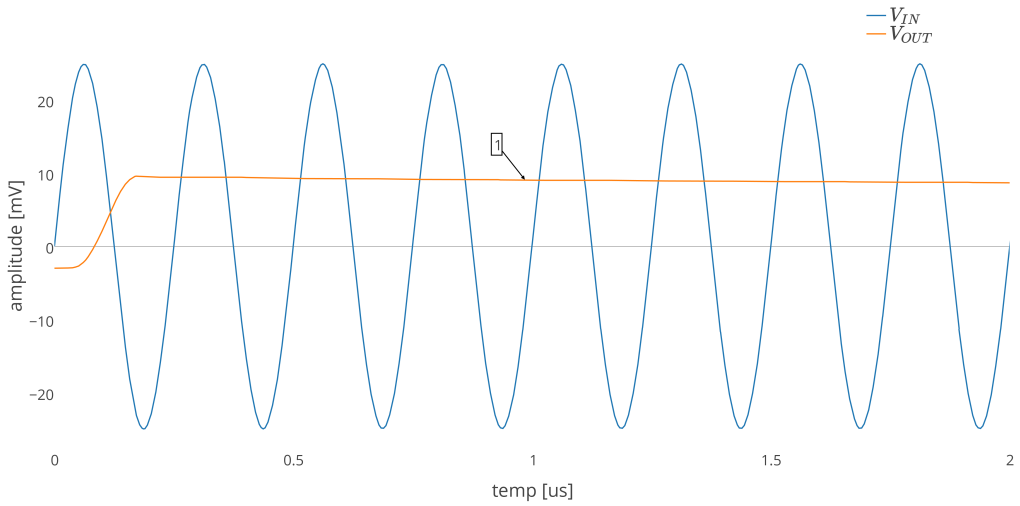

Figure 3.6: Simulation of Circuit2 (3.2): Frequency: 4 MHz, Amplitude: 25 mV, Capacitor: 10 nF; Between peak values the voltage droop is not significant, but the the maximum is not tracked [1]. Again the big capacitor prevents the circuit to work properly at high frequencies.

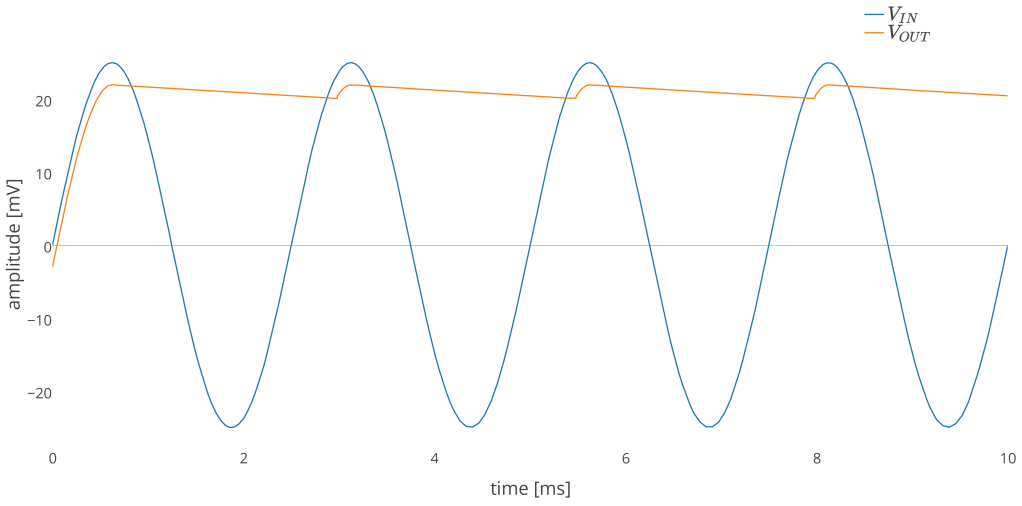

Figure 3.7: Simulation of Circuit3 (3.3): Frequency: 400 Hz, Amplitude: 25 mV, Capacitor: 10 nF; The reduced discharge current through the diode leads do a smaller voltage droop in between input signal peaks.

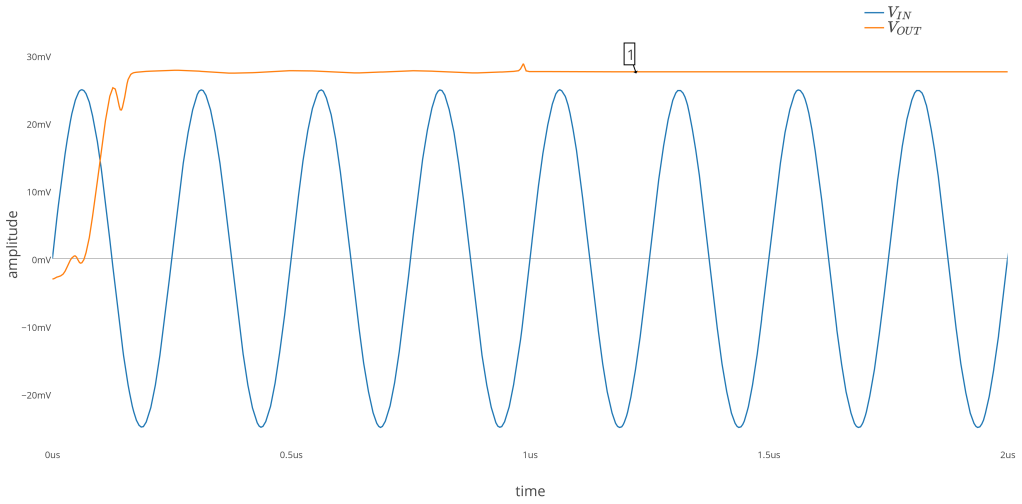

Figure 3.8: Simulation of Circuit3 (3.3): Frequency: 4 MHz, Amplitude: 25 mV, Capacitor: 10 nF; The over-shoot is probably due to the feedback circuit of the output buffer.

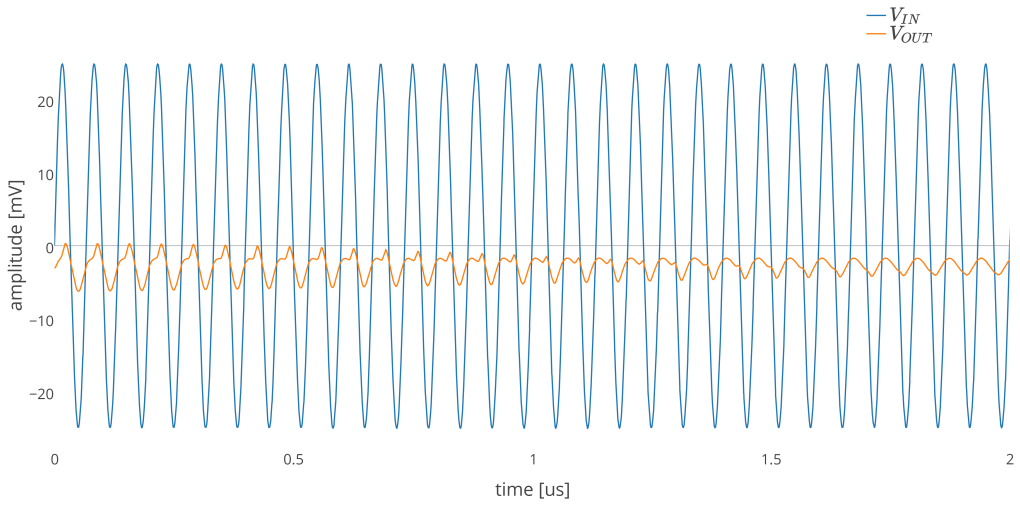

Figure 3.9: Simulation of Circuit3 (3.3): Frequency: 15 MHz, Amplitude: 25 mV, Capacitor: 10 nF; The output can not track the input at all. This is probably to the circuit structure in combination with the big capacitor.

the fundamental problems of those solutions. The minimal input amplitude was chosen here because it was the most critical in the simulations. The wide frequency range from which the input signal can be chosen prohibits the usage off one capacitor value for the whole range. In addition, there are problems when the frequency reaches high frequencies of 10 MHz and beyond. This can probably be explained by the fact that the feedback circuit is too slow to work correctly with the corresponding input signal.

3.1.2 Circuit as described in AD8033/34 datasheet

While looking for suitable operational amplifiers, that can be used to simulate the previous circuits a schematic in the AD8033 datasheet was found(*AD8033/AD8034 Low Cost, 80 MHz FastFET Op Amps* 2008). It is more complex than the solutions up to this point.

In the datasheet, the restriction to 1.4 V peak-peak is stated, because of the input protection diodes across the inputs. The AD8033 has a bandwidth

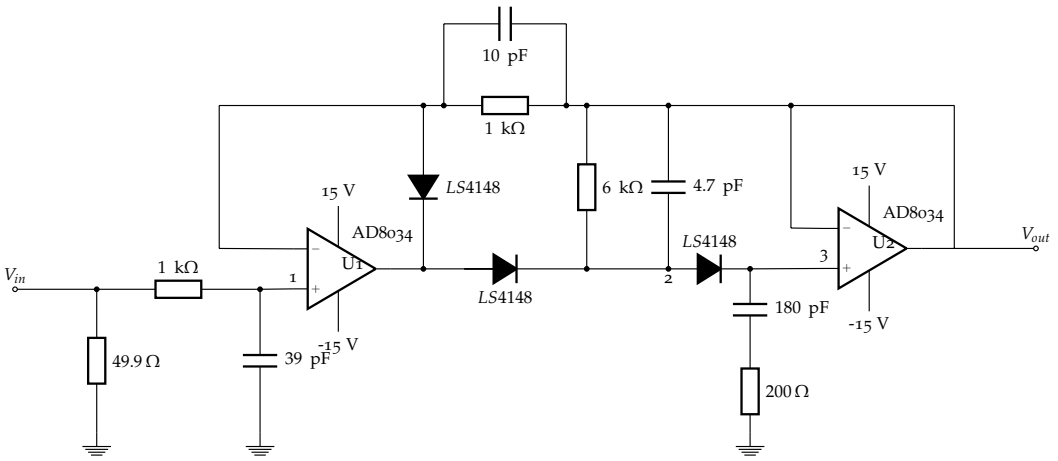

Figure 3.10: Detection circuit as described in AD8033 datasheet. A more complex feedback circuit is used to keep the reverse current through the diode low and to compensate forward voltage drop-off over the diode between node 2 and 3. A low-pass at the input is used to keep the input in a frequency range that allows the feedback circuit to work properly.

of 80 MHz but only a slew rate of $80\,\mathrm{V\,\mu s^{-1}}$. For simulation, the AD8066 was used. With a better slew rate of typical $180\,\mathrm{V\,\mu s^{-1}}$ this should lead to similar results with a broader range of input signals.

An input signal of 400 Hz and one of 1 MHz result in a tracking of the peak value that could be used as an input to the tester ADCs. With an amplitude of 25 mV the accuracy and ripple are better than the previously mentioned solutions. Even at a low frequency the drop of the voltage at node 3 between cycles is low enough to be sampled by a slow analog to digital converter and provide results that are accurate enough.
When increasing the input frequency further there are several problems that limit the functionality of this circuit. First, operational amplifiers with a high slew rate need to be used. The slew-rate needs to be not only high enough to follow the input signal, but also to provide the feedback signals fast enough.

Secondly, the low-pass filter at the input needs to be set to a cut-off frequency that does not attenuate the input signal. This does not hold true in the circuit as provided in the datasheet (3.10). As can be seen in in figure 3.13, labeled

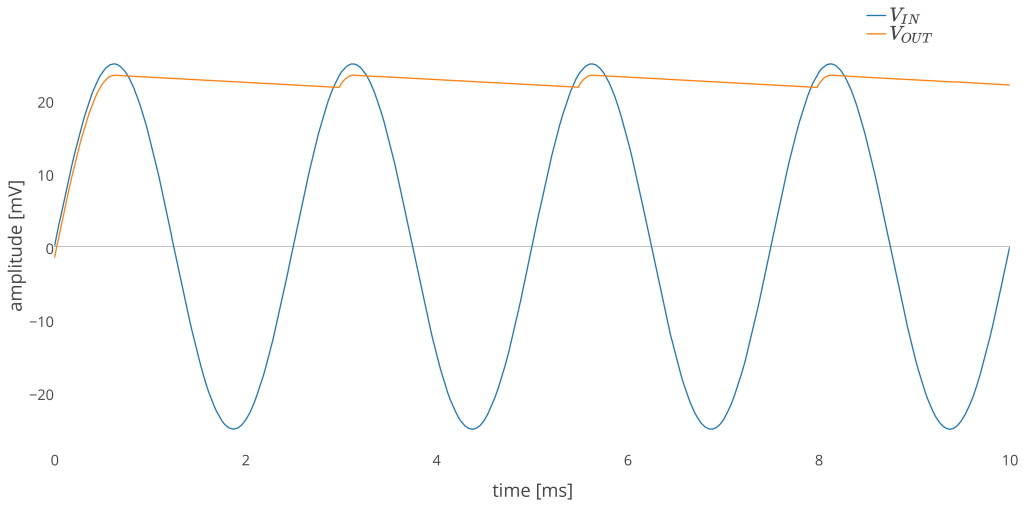

Figure 3.11: Simulation of circuit based on AD8033 datasheet (3.10): Frequency: 400 Hz, Amplitude: 25 mV; The output for low frequencies looks similar as the ones seen previously. Again the peak value is not reached, but the droop voltage is low enough.

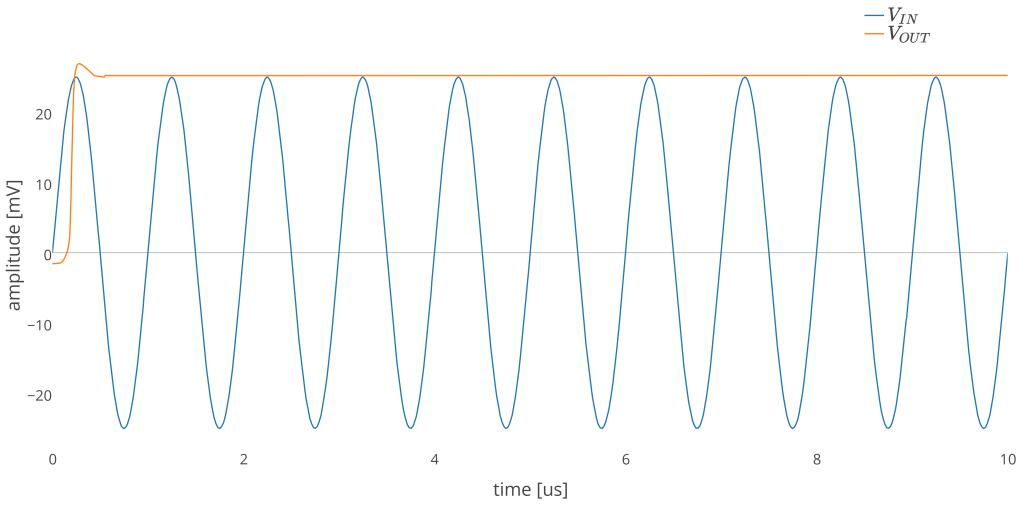

Figure 3.12: Simulation of circuit based on AD8033 datasheet (3.10): Frequency: 1 MHz, Amplitude: 25 mV; The circuit works good at this frequency, as the amplitude is tracked as desired.

"Filter1" the cut-off frequency is at 4 MHz, which directly affects the output signal.

By reducing the value of the capacitor in the input filter the cut-off frequency can be raised. The cut-off frequency is carefully chosen as described in the AD8033 datasheet:

"The rate of the incoming edge must be limited so that the output of the first amplifier does not overshoot the peak value of VIN before the output of the second amplifier can provide negative feedback at the summing junction of the first amplifier. This is accomplished with the combination of R1 and C1, which allows the voltage at Node 1 to settle to 0.1% of VIN in 270 ns." (*AD8033/AD8034 Low Cost, 80 MHz FastFET Op Amps* 2008)(p.19). Therefore after raising the corner-frequency of the input filter to 20 MHz by lowering the capacitor to 10 nF (3.13; Filter2), the results at the output of the circuit were not as expected(3.14).

Due to the complex nature of the feedback circuit, the limiting factors for maximum input frequency are the feedback paths that are used to keep the

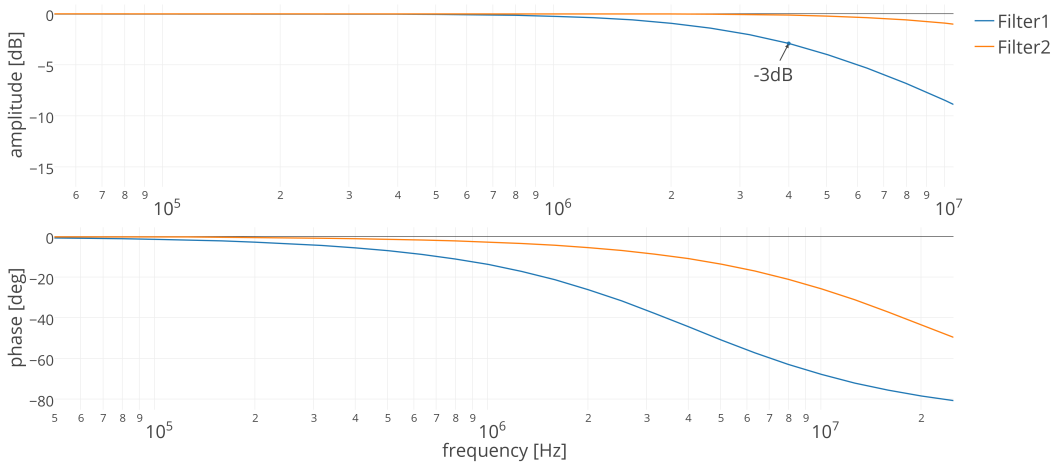

Figure 3.13: Bode Diagram for node 1 (3.10): Filter 1 is used as described in (*AD8033/AD8034 Low Cost, 80 MHz FastFET Op Amps* 2008) with R = 1 kΩ and 10 pF which lead to a −3 dB cut-off frequency of 4 MHz. For Filter 2 the values were changed to 500 Ω and 10 pF which increased the cut-off frequency to around 20 MHz

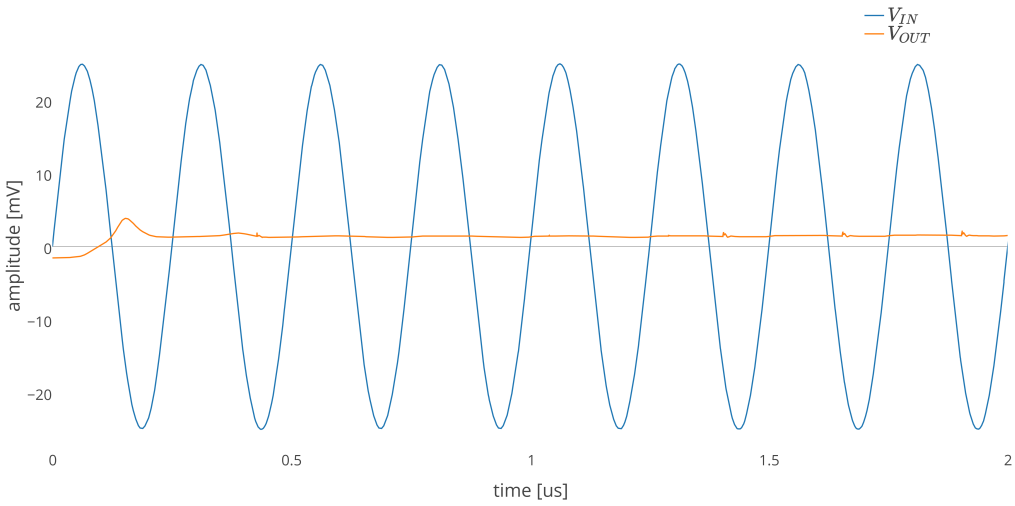

Figure 3.14: Based on AD8033 datasheet (3.10); When the input frequency is increased to 4 MHz the circuit is not working anymore. As described in the AD8033 datasheet the feedback circuit is not fast enough to provide the necessary feedback.

voltages over the series diodes near 0 V and hence reducing the effect of reverse current.
After simulating with different settings, the assumption is that with this topology an input signal of up to 15 MHz is not achievable.

3.1.3 Logarithmic Amplifier

Discrete circuits as discussed in the previous sections shared the problem, that they are either not suitable for high input frequencies of up to 15 MHz or could not be set up for the whole bandwidth in which input signals may reside.
This leads to integrated solutions that may have solved those issues and can be used in the test setup.

One solution is the product line of logarithmic amplifiers. Those are highly integrated circuits that are meant to be used in applications such as antenna power measurements, receiver signal strength indication and low-cost radar and sonar signal processing (*AD8307 Low Cost, DC to 500 MHz, 92 dB Logarithmic Amplifier* 2008).
Analog Devices and Texas Instruments provide components with similar functionality but different ranges and conversion rates. Most of them are designed for frequencies way above 15 MHz but some can be configured to work down to DC.

Logamps, as those components are commonly known as use a cascade chain of linear amplifiers with a typical gain of 10 dB to 20 dB. In the example in figure 3.15, taken from Eamon Nash, 2000 a circuit of a five stage version of a logamp is shown, each of the stages with a gain of 20 dB.
When a small continuous sine wave is fed to the input of the first amplifier it propagates through the cascade with each stage amplifying the signal by 20 dB. At one stage the signal will increase to a level that causes it to clip. This clipping has been set to 1 VDC in this example. In figure 3.15 this clipping happens in the third stage and every succeeding stage is also limited to 1 VDC. Each stages output is forwarded to a full-wave-rectifier and then summed up with all other stages outputs. These summed outputs

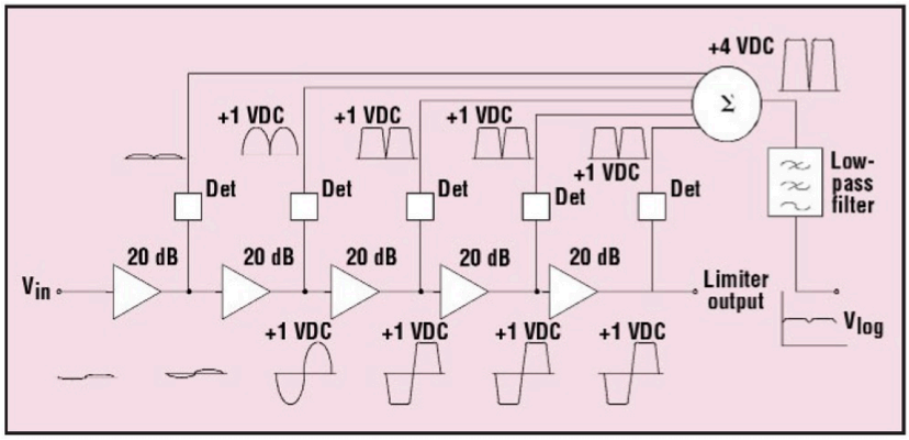

Figure 3.15: Example of a logamp as described in (Eamon Nash, 2000) Five gain stages with a gain of 20 dB each are used to successively amplify the input signal. The gain stages clip at 1 V to generate and the outputs of all gain stages are rectified and summed up to provide the output.

are filtered with a low-pass to remove ripple to produce the output of the logamp.

By reducing the input signal by 20 dB one gain stage less will be clipping, leading to 1 V less output at the end of the logarithmic amplifier. This means the slope, the input/output characteristic is 1 V per 20 dB or 50 mV dB^{-1}. Eamin Nash, n.d.(p.2)

Defining factors for logarithmic amplifiers are the slope as described, witch is the change at the output depending on the input, and the intercept. The intercept is the point at which the input/output graph crosses the 0 dB-axis.

In the case of the AD8307, these characteristics are set by external components by defining voltages at two input-pins of the device. Those voltages set the characteristics of the following equation:

$$V_{OUT} = V_Y \cdot log\left(\frac{V_{IN}}{V_X}\right) \tag{3.5}$$

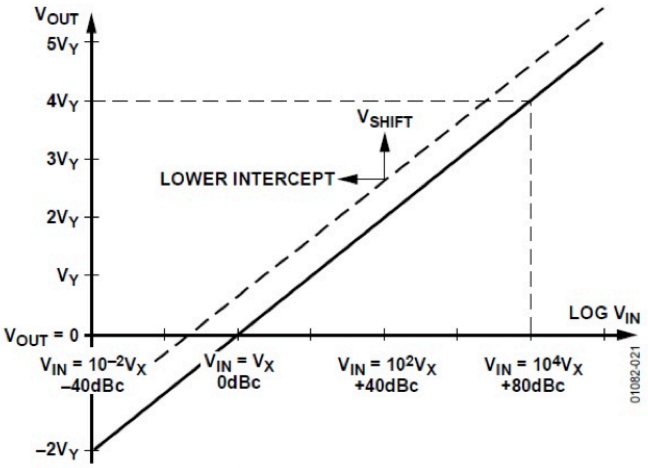

Figure 21. Ideal Log Amp Function

Figure 3.16: Input/output characteristic of a generic logarithmic amplifier as described in (*AD8307 Low Cost, DC to 500 MHz, 92 dB Logarithmic Amplifier* 2008)

The logarithmic characteristic fits well with the error limit which is $\pm 2\,\%$ over the whole voltage range and therefore increases with signal strength. Low external component count and small package size are additional reasons to consider the AD8307 as a solution for this amplitude measurement.

3.1.4 ADC and Microcontroller

Another possibility to acquire the amplitude of a sine wave is, sampling it with an ADC and calculating the needed parameter with a DSP or with the tester itself. This would allow for more parameters to be measured in future updates and reduces the errors that may be introduced when the analog signal has to be routed to the tester.

The limited number of usable pins on the tester that can be used for each module, eliminates the use of parallel data lines from an ADC to the tester. Contrary to this, ADC with serial data output are not available for

high frequencies. This limits this approach further and forces the use of undersampling.

Undersampling

Undersampling is a way to capture high frequency signals with the means of ADC that working with a lower sampling frequency. This can still fulfill the Nyquist criterion if the sampling frequency is twice the bandwidth of the signal. The signal will then be folded back to baseband between DC and half of the sampling frequency without overlapping with mirror frequencies. By carefully choosing the sampling frequency the shifted signal can be used as is. This requires that the lower boundary of the bandwidth of the signal is a multiple of the sampling frequency.

When looking at a single input frequency the bandwidth is minimal and the sampling frequency can be chosen quite low. Because the signal can have a frequency between 400 Hz and 15 MHz the bandwidth of the signal at the input can not be limited too much. Therefore even if the signal only consists of one frequency, when undersampled, it may superpose with distinct noise spikes. With a sampling rate of 100 kHz all frequency components will be shifted to the baseband between DC and 50 kHz.

The input signal may be low-pass filtered at 15 MHz, which leads to over 300 frequency representations that occupy the same baseband frequency spectrum as the wanted signal. All of them can falsify the measured amplitude. It is, therefore, important to have high resolution of the frequency representation to minimize the frequencies that occupy the same frequency bin.

Overview, Sampling and DFT

The number of samples taken to produce the frequency representation determines the accuracy of the amplitude by providing bins close to the frequency of the input signal. More samples to do the DFT lead to more

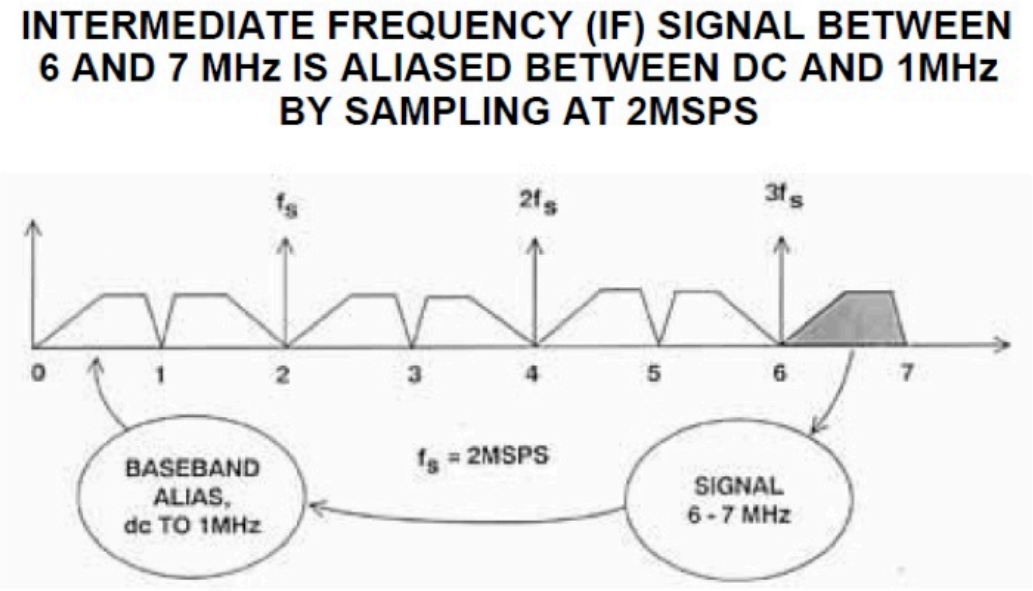

Figure 3.17: A representation of undersampling a signal from 6 MHz to 7 MHz. The lower boundary of the bandwidth, which is of interest is a multiple of the sampling frequency and the bandwidth of the signal does not exceed the Nyquist bandwidth. Therefore, the baseband representation shows the input signal from DC up to half the sampling frequency without overlap of other aliasing frequencies. (*Analog Devices Design Handbook Chapter 5 - Undersampling Applications* n.d.)

frequency bins, which lead to better resolution of the frequency representation. More distinct frequency bins in the frequency domain increase the possibility that the desired signal is near the lope of a bin.

For a sampling frequency of 100 kHz and an acquisition time of 10 µs, 100 samples can be measured. This leads to 100 frequency bins over twice the baseband of 100 kHz and a frequency resolution of:

$$\frac{100\,\mathrm{kHz}}{100 bins} = 1000\,\mathrm{Hz} \tag{3.6}$$

When increasing the acquisition time to 512 µs, 512 samples can be measured with a sampling frequency of 100 kHz. This leads to a resolution of:

$$\frac{100\,\mathrm{kHz}}{512 bins} = 195.3\,\mathrm{Hz} \tag{3.7}$$

In contrast, if the sampling frequency is increased to 1 MHz and the sampling time is 10 µs, with 1000 samples, the frequency resolution is the same as in the first example:

$$\frac{1000\,\mathrm{kHz}}{1000 bins} = 1000\,\mathrm{Hz} \tag{3.8}$$

By increasing the sampling frequency and at the same time the numbers of samples no higher resolution in the frequency domain can be obtained. Only by the increase of the acquisition time a better resolution can be achieved. There is a trade-off between acquisition time and frequency resolution. For best accuracy in the frequency domain, the maximum time available for sampling should be used.
Increasing the sampling frequency will, on the other hand, reduce the number of frequencies that overlap in the baseband. As described previously when sampling a signal with 15 MHz with 100 kHz sampling frequency, 300 frequencies share the exact same position in the frequency spectrum.

$$\frac{15\,\mathrm{MHz}}{50\,\mathrm{kHz}} = 300 \tag{3.9}$$

If the sampling frequency is increased to 1 MHz only 30 frequencies share the same representation.

$$\frac{15\,\text{MHz}}{500\,\text{kHz}} = 30 \tag{3.10}$$

In addition to the frequency resolution, there is another resolution that influences the accuracy of amplitude measurement. The resolution of the frequency representation depends also on the number of samples to calculate the discrete time Fourier transform.

Figure 3.18 shows the DFT of a 13.56 MHz signal that was sampled with 100 kSPS for 640 µs, which result in 64 samples. The frequency in the baseband that represents this signal after aliasing occurred is 40 kHz. Neither the actual frequency nor the amplitude can be derived from this representation. This is not because the frequency resolution is too low, but because the resolution of the representation, the DTFT is not high enough to show the individual bins.

To increase the resolution of the DFT, zero padding can be used. Additional samples with a value of zero are appended to the samples in time domain. These additional samples, even though they contain no additional information, lead to more calculated values of the DFT.

Time domain representation after sampling the input signal is a series of samples:

$$x[n] = \{x_0, x_1, \ldots, x_n\} \tag{3.11}$$

Using zero padding extends the series:

$$x_z[n] = \{x_0, x_1, \ldots, x_n, 0, 0, \ldots, 0\} \tag{3.12}$$

In figure 3.19 the effect to the frequency representation can be seen. The same input signal and the same sampling-rate and duration were used, but the resolution of the DFT increased. The individual bins can be seen in figure 3.19. Because calculating the DFT results in 64 bins in the frequency range of -50 kHz to 50 kHz and the negative frequencies not containing

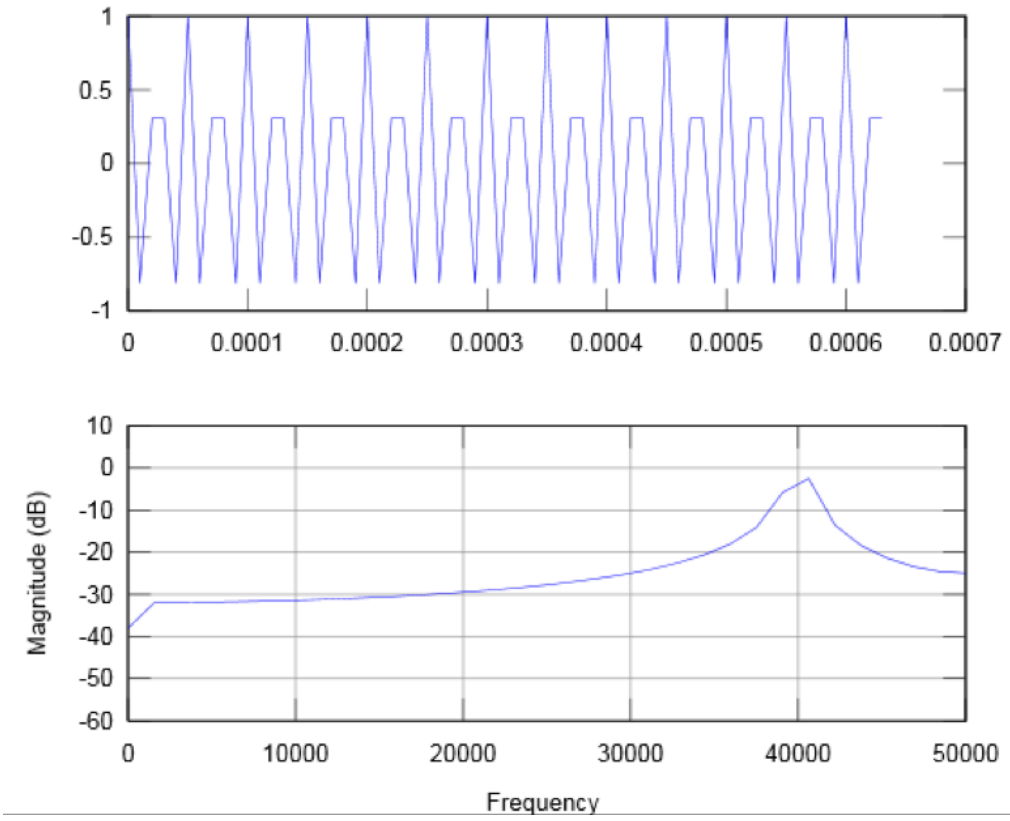

Figure 3.18: 13.56 MHz signal with full-scale amplitude is sampled with 100 kHz. The resolution of the frequency representation is too low to determine neither the frequency nor the correct amplitude of the input signal.

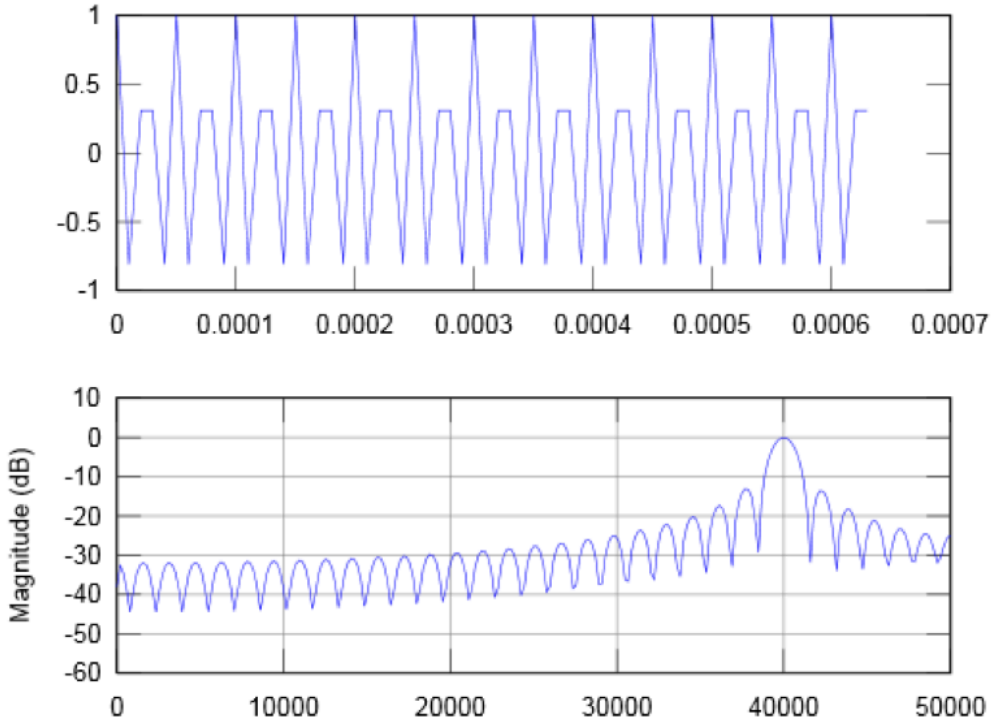

Figure 3.19: 13.56 MHz signal with full-scale amplitude and zero padded is sampled with 100 kHz The frequency resolution is the same as before but the resolution of the frequency representation was increased. All single frequency bins can be seen accurately. The input signal is represented exactly at the 40 kHz frequency bin and therefore, the amplitude is also accurate.

additional information only the positive frequencies are shown. The 32 bins in the figure show a bandwidth of 1.5625 kHz.

Zero padding can be used to get more values that represent the same frequency representation of the signal. It does not help to find the right frequency but it will help to find the accurate peak value of the presentation. The problem is, that if the frequency that is been observed does not lie on a bin the real amplitude is buried in the frequency representation. The best outcome can be achieved if the sine wave input frequency is on a bin.

To increase the accuracy of amplitude measurement with FFT, windowing can be used. This is a technique that is used on the time domain sample values. The different samples are multiplied with different values and therefore weighted. This can be seen as an interpolation in the frequency representation. The lopes are shaped differently after the windowing function is applied.

Applying a window is a multiplication of the sample values with the values of the windowing series $w[n]$ which has the same length as the input series:

$$x_w[n] = x[n] \cdot w[n] = \{x_0 \cdot w_0, x_1 \cdot w_1, \ldots, x_n \cdot w_n\} \tag{3.13}$$

It is important to note, that when using windowing and zero padding, the window functions has to be applied to the input series alone. After that zeroes can be appended as required.

For a given application, one has to choose from a multitude of window functions to acquire the best accuracy for the parameter that needs to be measured. As the amplitude is in this case the parameter of interest, the Flat-Top-Window can be used. The interpolation in the frequency domain leads to accurate amplitude values even in between frequency bins.

This is just a small summary of trade-offs and problems that are present when using undersampling or sampling in general to determine the amplitude of a sine wave signal.

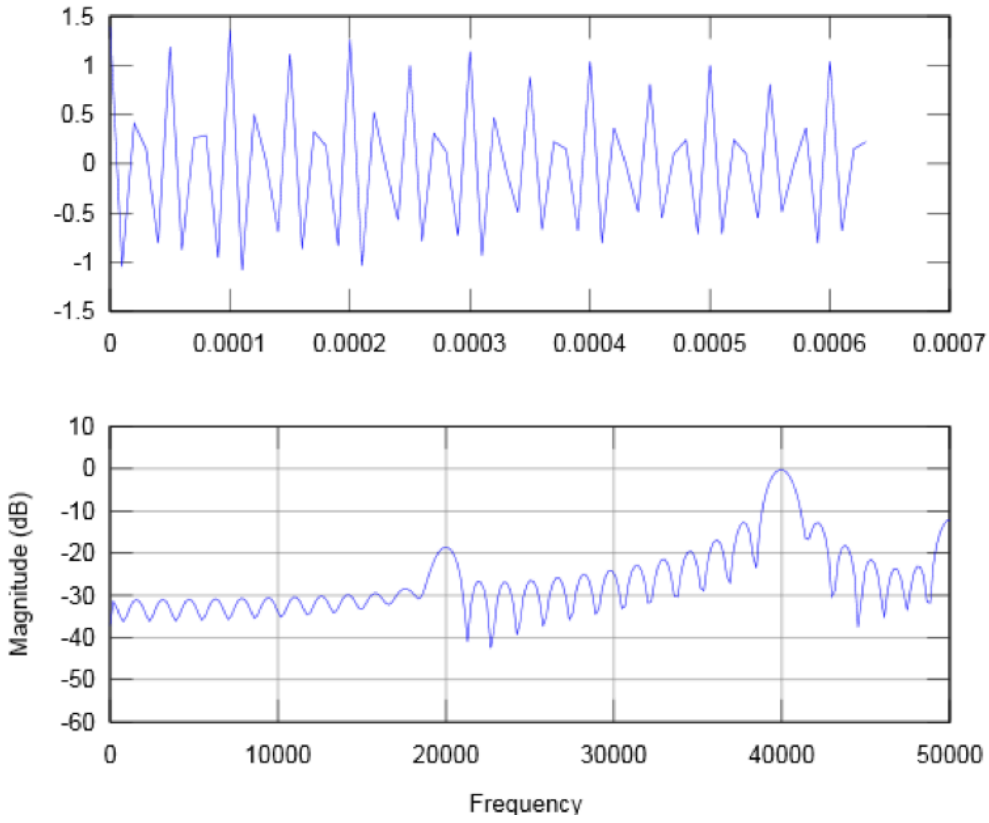

Figure 3.20: 13.56 MHz signal sampled with 100 kHz with zero padding and error frequencies

ADC selection

When sampling a signal the choice of the analog to digital converter is an important one to preserve crucial information in the input signal. Typically ADC has relevant parameters listed to show how the signal is influenced during conversion. Some of them are the signal to noise ratio (SNR), spurious free dynamic range (SFDR), differential linearity error (DNL), integral linearity error (INL) and effective number of bits (ENOB). These values are defined over a certain bandwidth usually the Nyquist-bandwidth of the ADC.

"Sampling ADCs are generally designed to process signals up to Nyquist (fs/2) with a reasonable amount of dynamic performance. As we have seen, however, even though the input bandwidth of a sampling ADC is usually much greater than its maximum sampling rate, the SFDR and effective bit (ENOB) performance usually decreases dramatically for full-scale input signals much above fs/2. This implies that the selection criteria for ADCs used in undersampling applications are SFDR or ENOB at the IF frequency, rather than sampling rate. The general procedure for selecting an ADC for an undersampling application is not straightforward. The signal bandwidth and its location within the frequency spectrum must be known. The bandwidth of the signal determines the minimum sampling rate required, and in order to ease the requirement on the antialiasing filter, a sampling rate of 2.5 times the signal bandwidth works well. After determining the approximate sampling frequency needed, select the ADC based on the required SFDR, S/(N+D), or ENOB at the IF frequency. This is where the dilemma usually occurs. You will find that an ADC specified for a maximum sampling rate of 10MSPS, for instance, will not have adequate SFDR at the IF frequency (72.5MHz in the example above), even though its performance is excellent up to its Nyquist frequency of 5Mhz. In order to meet the SFDR, S/(N+D), or ENOB 12 requirement, you will generally require an ADC having a much higher sampling rate than is actually needed."(*Analog Devices Design Handbook Chapter 5 - Undersampling Applications* n.d.)

Naturally there are more parameters that are important for the selection of the ADC. Supply range, power consumption, input range, input resistance and capacitance, common mode rejection ration, power rejection ratio are

all things that need consideration when choosing the ADC.

3.1.5 Microcontroller

As mentioned previously, tester inputs and outputs are limited and therefore ADC working with parallel data lines can not be used directly with the tester. The alternative would be data send via SPI communication, which would put a huge load onto the data bus and the tester itself. A different approach would be to send the data to a microcontroller that can also take over the calculation and send only the results to the tester. A good choice here would be I2C data bus, which would take only 2 pins of the tester to communicate with multiple modules. This solution would also provide parallel acquisition of multiple sites on one test-board, as well as easy scaling as long as the I2C-bus supports the number of external modules. Even then a second I2C-bus would easily increase the number of modules further. The microcontroller needs to have the capability to acquire data from the ADC, calculate a result and send it to the tester. In addition, power management of the module would be a good way to minimize power consumption.

3.2 Proposal

To conclude the selection of a method to measure the amplitude of a sine wave, the direction this master thesis will develop further and the solution, which will be implemented is proposed in this chapter. Later on, a prototype board will be developed and the acquisition of the final results will be simulated and also measured at the test setup.

Two solutions shall be implemented on one board. The core will be a microcontroller, to gather data, calculate the result, send it to the tester and control power consumption of the module. One solution will be an ADC and one a logamp.

Next, the relevant components are discussed and pros and cons are listed. This should give a suitable explanation why those components were chosen and what are the crucial decision points that led to this solution.

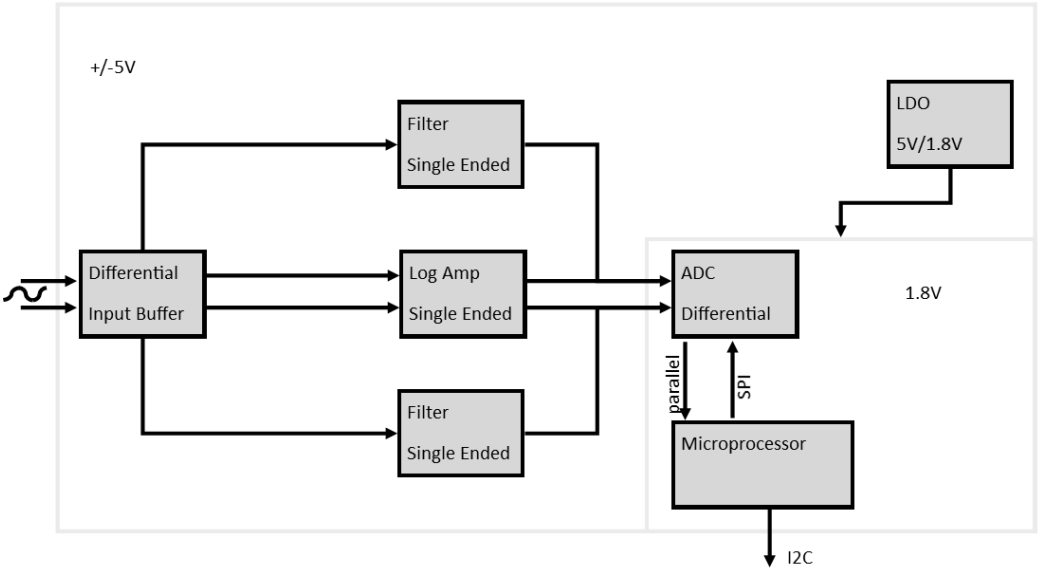

Figure 3.21: Block Diagram of the proposed prototype. The module uses a differential input buffer, to reduce the load the measurement circuit put onto the device under test. An optional low-pass filter is used to set the input bandwidth. Either the logamp or the ADC is used to acquire the data that is sent to the microcontroller. The result is sent to the tester using I2C-Bus. SPI communication can be used for ADC setup.

3.2.1 Logamp AD8307

Different logamps from different manufacturers are available but not all suit the special needs that come with the usage of such components at lower frequencies. Analog Device provides a description how to use most of their logamp products with low frequencies (Pilotte, 2005). This leads to the choice of the AD8307, which frequency extension is documented down to frequencies as low as 20 Hz. As shown in the datasheet (*AD8307 Low Cost, DC to 500 MHz, 92 dB Logarithmic Amplifier* 2008) the output is the logarithmic representation of the envelope of the AC input signal. How well the amplitude representation will work at low frequencies is not documented.

The small outline of the 8 lead SOIC, low external component count and

the low power consumption of 10 mA at a single supply of 2.7 V to 5 V are well-suited characteristics for the amplitude measurement module. In addition, an enable pin is present to reduce power consumption even further when not used. The differential input is rated with 1.1 kΩ, which requires the use of an input buffer to ensure the device under test is not loaded too heavily.

The stated applications are "conversion of signal level to decibel form", "network spectrum analyzers" and "true decibel ac mode for multimeters" (*AD8307 Low Cost, DC to 500 MHz, 92 dB Logarithmic Amplifier* 2008) and therefore fits the intended use reasonably well.

3.2.2 External ADC

For the second approach a suitable ADC is needed. This bares several problems as described in the chapter (3.1.4). ADC with sample rate up to 1 Msps are available with SPI data output. Storing this data at this rate requires a fast microcontroller. The alternative would be parallel data outputs, which require more input pins at the microcontroller. When using the minimal full-scale range of 2 V, which is needed to track the maximum input signal, a 12 bit ADC has a resolution of 0.5 mV. Therefore, a 14 bit or 16 bit should be preferred to provide additional accuracy and account for a possibly larger full-scale range.

The LTC2160 is a suitable ADC as the stated sampling rate if 25 MSps is the maximum sampling rate, but sampling down to 1 MSps is documented in the datasheet (*LTC2162/LTC2161/LTC2160 Low Power ADC* 20011). Furthermore the −3 dB bandwidth is 550 MHz and SNR, SFRD are rated up to 140 MHz. In addition, undersampling applications are clearly stated as use-cases for the LTC2160.

The component is working with 1.8 V single supply and a power consumption of 45 mW. The input range is 2 V and hence perfectly suitable for the amplitude measurement application.

Data output is parallel 16-bit data lines and clock encoding is done with an external clock source with minimal requirements. This means 16 pins of the

microcontroller are used for data input and clock encoding can be done by the microcontroller. Setup is done via register settings modified via SPI, but the device is also working stand-alone.

To reduce load on the tested circuit, an input buffer is required to provide the ADC with the needed input current.

3.2.3 Microcontroller

For the microcontroller, some requirements are already given. 16 input pins are needed for the data lines. Ideally, those data pins are located on one port for easy acquisition and storage. Additionally, SPI and I2C communication need to be supported. Supply voltage should be 1.8 V to match the supply voltage of the ADC.

The STM32L051C6 fits the above-mentioned requirements. It is an ARM Cortex M0+ processor featuring single-cycle hardware multiplication, extended mathematical functions and is running with up to 32 MHz with the internal oscillator. It is provided in a 7 mm x7 mm 48-pin LQFP package which results in small area used on the PCB. ARM processors are supported by the CMSIS (Cortex Microcontroller Software Interface Standard) that provides easy setup of the system and peripherals.

The 32-bit processor can handle the 16-bit data during multiplication and accumulation. Look-up table for trigonometric functions and square-root computation are also provided.

3.2.4 Differential Buffer

To reduce the influence of the measurement circuit on the device under test, a differential input buffer is needed. A high input resistance and a low input capacitance are desired, to reduce the load and minimize the influence of the measured signal to a minimum.

The LT6411 is an ADC-driver with a bandwidth of 650 MHz that is well suited to handle this task. A high slew rate and typical 500 kΩ input resistance as well as 1 pF input capacitance are the most important parameters of this component. Without the need of external components in the signal path in front of the input means, there is nothing that deteriorates those values.

3.2.5 Power Consumption

As a baseline, the estimated power consumption is shown in table (3.1). There will be 3 different power supply voltage levels. Symmetrical ±5 V supplies are used for the input stage as well as for an optional low-pass filter. This can also be used to reduce larger input amplitudes that are than processable by the ADC. The AD8307 is mutually exclusive with the ADC when calculating power consumption and is supplied with 5 V single supply.

The microcontroller, the ADC and the ADC-driver in front of the ADC are working with an 1.8 V single supply.

Part	Module	Current [mA]	Power Supply [V]
AD8132	Differential Buffer	10.7	±5
optional	Filter	15	±5
AD8307	Logamp	8	5
LTC2160	ADC	27	1.8
AD8132	ADC Driver	10	1.8
STM32L051C6	Microcontroller	5	1.8

Table 3.1: Components with estimated power consumption

4 Prototype Board Design

In this chapter an overview of the circuit design, component placement and layout will be given. The prototype board itself does not have strict size limitation as they are stated in the chapter (2.2), therefore, component choice and layout can be done with easier debugging in mind.

4.1 General Thoughts

Additional external components like resistors and capacitors will be included in the schematic and the layout to react on a multitude of problems during debugging. They will be used to detach certain stages of the signal chain from the power supply or bypass them entirely during measurements. Pads for larger capacitors near critical components will be provided to counteract unusual high ripple on the power supply lines. Also, additional components will be placed between stages of the signal chain that can be used to introduce low-pass filters or DC-decoupling if this is necessary.

Where possible bigger component sizes, 0603 or higher will be used for easier soldering and desoldering during debugging. Additional spacing should further simplify this process.

Test points should be introduced to essential connections that can otherwise not be measured easily.

4.2 Schematics

Schematics are done using EAGLE 6.5 and all figures that follow are exported directly. The different stages of the signal chain are depicted separately with connections between those stages are matched via their netname.

Differential routed nets can be forced by naming. The same name needs to be used for both nets with one ending on _*P* and one _*N*. This will force differential routing and allow for wire-length compensation during layout.

4.2.1 Input Buffer

The input buffer is connected to supply as described in the datasheet (*LT6411, 650MHz Differential ADC Driver/Dual Selectable Gain Amplifier* 2007). Every connection to positive and negative power supply is decoupled with a 470 pF capacitor to ground. In addition 4.7 nF and 1 µF capacitors are placed near the component for decoupling of lower frequencies on the supply. 0 Ω resistors are used to disconnect the part from the supply if needed.

Additional resistors are used to set the enable pin, as well as the common mode offset of the device. For the typical setup, both pins are tied to ground. The input configuration is chosen as described for a gain of 1.

C601 and C604 are used to decouple the input from the tested circuit if a different reference voltage is used. The input reference is set by R612, R613, R610 and R611. A low-pass filter can be introduced if needed but ideally, no external components are needed at the input to use the good input resistance and capacitance the part was chosen for.

4.2.2 Low-pass Filter

As discussed in the chapter (3.1.4) a low-pass filter with a cut-off frequency inside the bandwidth the input signal may occupy is not possible, a filter

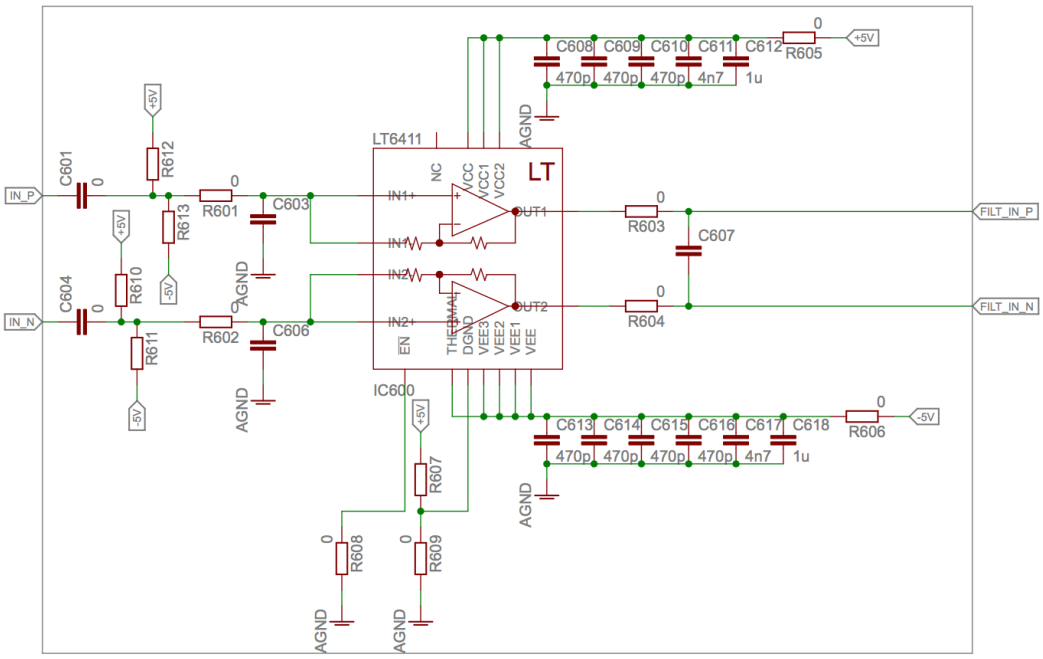

Figure 4.1: The LT6411 is used as the input buffer of the board. Ideally, no external components are used at the input to take advantage of the good input characteristics of the component. Extensive supply bypassing is used as described in the datasheet. Additional components at the output may be used if necessary.

can be used to reduce noise and error frequencies above the bandwidth. In figure (4.3) a 4th-order low-pass filter can be seen. It is build of two stages of 2nd-order Sallen-Key low-pass filter for each of the differential paths. Those filters were designed in Microchip Filter Lab and later trimmed for better amplitude response in the cut-off region. The Bode-plot of the filter stages can be seen in figure (4.2). One stage is designed with a resonance peak and steeper fall-off to increase the slope of the overall filter. The second stage has a slightly lower corner frequency that allows this stage to counteract the peaking of the previous stage. The stopband attenuation is $-25\,\mathrm{dB}$, which is most likely sufficient to reduce possible error-frequencies to a level where they do not pose a problem. Between $6\,\mathrm{MHz}$ and $15\,\mathrm{MHz}$, the amplitude response shows a variation between $1.5\,\mathrm{dB}$ and $-2\,\mathrm{dB}$. This error can be accounted for after acquisition of measured data.

If need be the filter can be modified to a slower cut-off above $15\,\mathrm{MHz}$, but a higher stopband attenuation. A better amplitude linearity in the passband could also be a parameter to tweak, but the design in figure (4.2) will be the starting point.

It is important to note, that offset errors of the operational amplifiers need to be accounted for. If needed a DC-blocking capacitor in the following stage has to be included to circumvent this problem. In addition, a voltage divider with output buffer is included if signals larger than the full-scale range of the ADC need to be measured. High accuracy resistors should be used here to reduce amplitude error. For each of the dual-channel operation amplifiers, decoupling capacitors are used for both, the positive and the negative supply. If needed, free pads for larger values are provided. Again $0\,\Omega$ resistors are used to detach the stage from the power supply. Additional resistors, used as jumpers, are included to bypass this stage and to route the signal to next stage, either the input buffer of the ADC or the logamp stage.

4.2.3 ADC Buffer and Level Shifter

The previous stages used a $\pm 5\,\mathrm{V}$ supply so accommodate for higher input signals and to reduce supply current needed by the $5\,\mathrm{V}$ power supply from

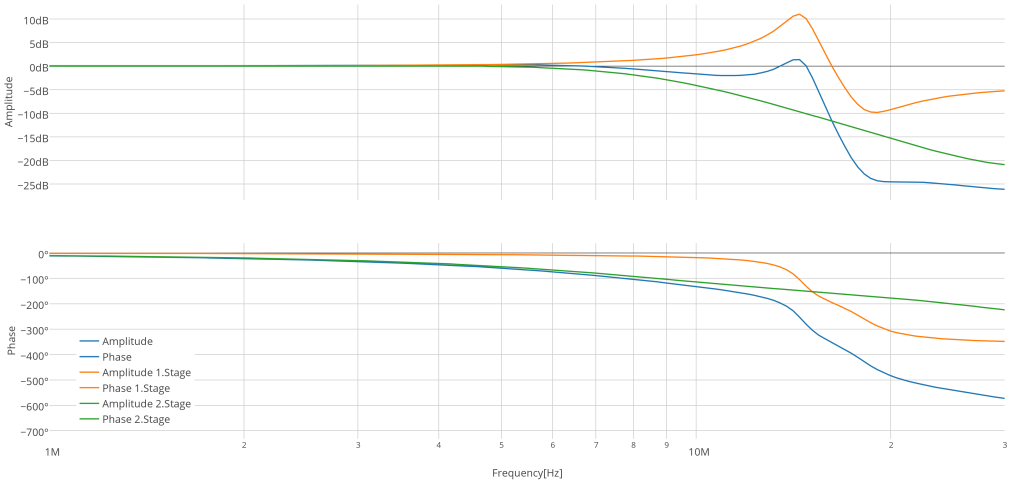

Figure 4.2: Bode-plot of the 4th-order low-pass filter with individual stages shown. The peaking at the corner frequency of stage one is reduced by using a lower corner frequency for the second stage. The overall amplitude response shows a sharp cut-off between 15 MHz and 20 MHz and a stop-band attenuation of around −25 dB.

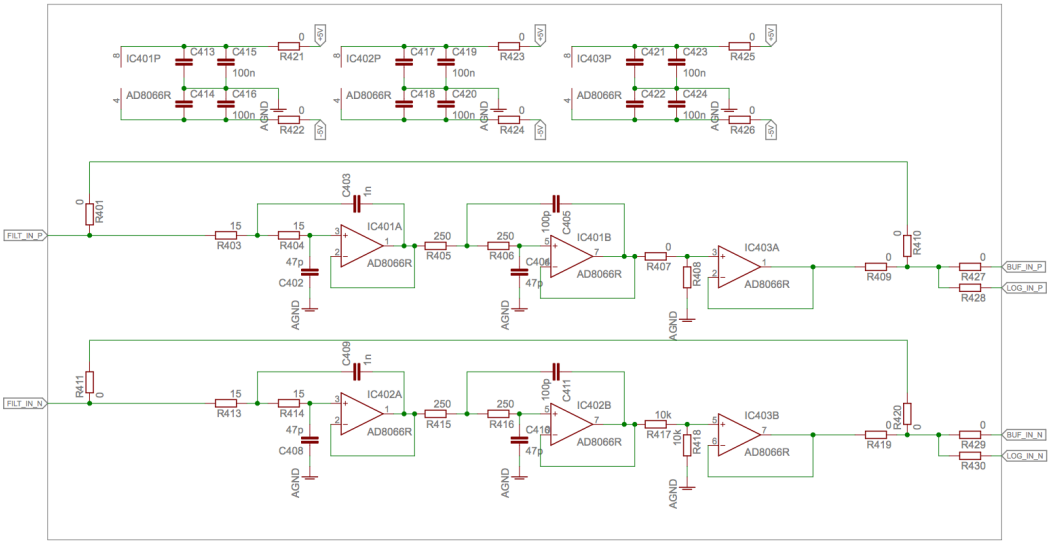

Figure 4.3: 4th-order low-pass filter is Sallen-Key setup that uses 2 dual-package operational amplifiers for the differential paths. To attenuate the signal a voltage divider followed with a buffer is used. A bypass is included to take the low-pass out of the signal path if not needed.

the J750. To convert the differential signal to an input that is compatible with the ADC, the AD8132 is used. It is used to shift the common mode voltage level to the reference voltage provided by the ADC.

At the input, C501 and C502 may be used as DC decoupling capacitors if a previous stage introduces an offset error. Both at the input and the output optional components for the filter are inserted. As described in the datasheet (*AD8132 Low Cost, High Speed Differential Amplifier* 2015) the resistors R507 and R508 may be needed to reduce high frequency ringing if a capacitive load is driven. The feedback path is set up as shown in the datasheet for a gain of 1. An additional parallel capacitor is included in the feedback to combat problems that may arise. Bypass capacitors at the supply pins and resistors to detach the component from supply are again included.

4.2.4 ADC

In the case of the LTC2160 the supply pins are again bypassed with 100 nF and resistors are again used to disconnect the ADC from the power supply during debugging. Additional bypass capacitors are needed at the VCM and the VREF pins to ensure the best functionality of the ADC.

The REFH and REFL pins need also external capacitors. In the datasheet (*LTC2162/LTC2161/LTC2160 Low Power ADC* 20011) the part MURATA LLA219C70G225MA01L is suggested. The pin spacing is the same as the one of the LTC2160 and therefore the part can be placed as close as possible to the ADC. At the ENC inputs the suggested components are included, but at first the ENC- pin will be tied to ground and the ENC+ will be directly connected.
At the input a filter structure as proposed in the datasheet on page 20 is used with a cut-off frequency at around 100 MHz DC block capacitors are included to take into account any offset errors that are introduced in the signal chain on either of the differential lines. Per definition the overall input signal is DC free. To set up the ADC either an SPI-bus or hardware setup may be used. All necessary pins can be connected to either ground or VDD or left be floating. This gives the option to test the ADC without microcontroller setup.

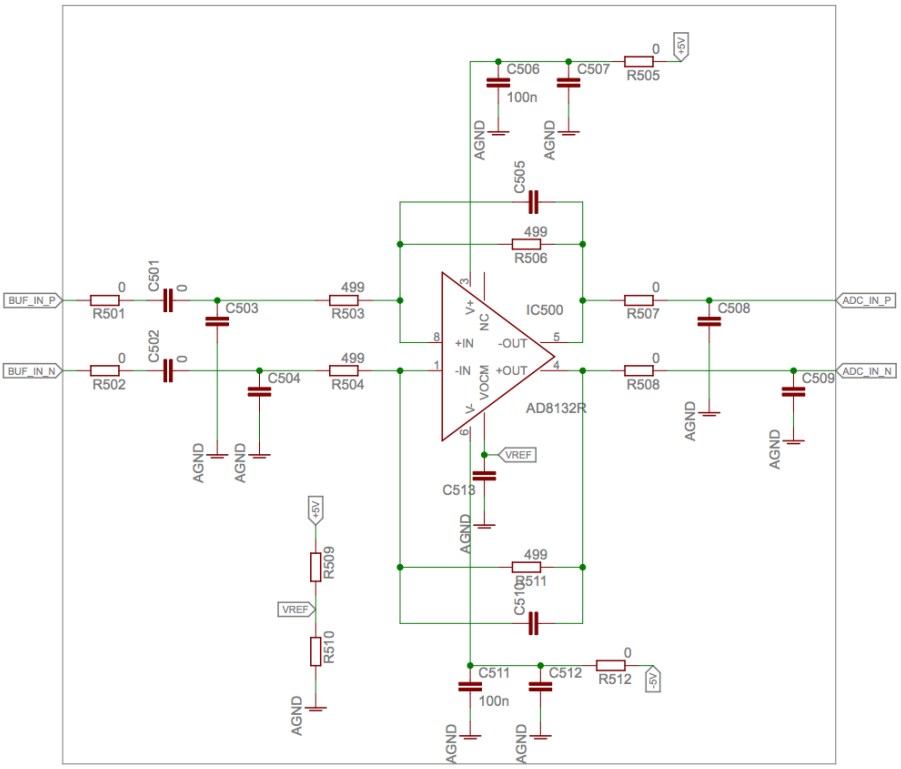

Figure 4.4: The AD8132 is used to shift the input level to the common mode voltage provided by the ADC. At the input and the output additional components are placed to use additional filters is needed.

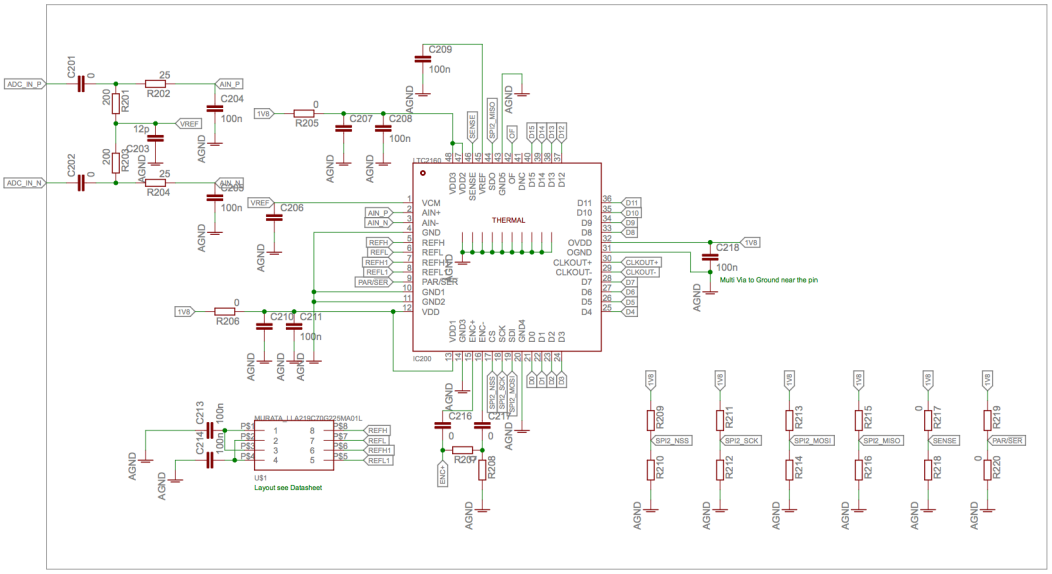

Figure 4.5: At the input of the ADC a low-pass filter with a cut-off frequency off around 100 MHz is suggested in the datasheet. Setup can be done by SPI communication as well as hardware settings. Both ways can be used due to external resistors that can be used to pull the corresponding pins to ground, VDD or left floating.

All data lines, including the overflow pin OF, are directly connected to the microcontroller but are also connected to test points to allow easy access.

4.2.5 Microcontroller

The STM32L051C6 is also set up similar to the previous components as described in the datasheet (*Access line ultra-low-power 32-bit MCU ARM®-based Cortex®-M0+* 2015). For reference, the schematic of the STM32Lo discovery kit (*Discovery kit for STM32Lo series with STM32L053C8 MCU* 2015) was used. Supply pins are again bypassed by 100 nF capacitors and resistors are included to detach the part from the power supply. This time, additional larger capacitors are placed farther away from the pins. External resistors are used to set the BOOTo pin to VDD so that the microcontroller will boot from the user provided code. 4.7 kΩ resistors are used as pull-ups

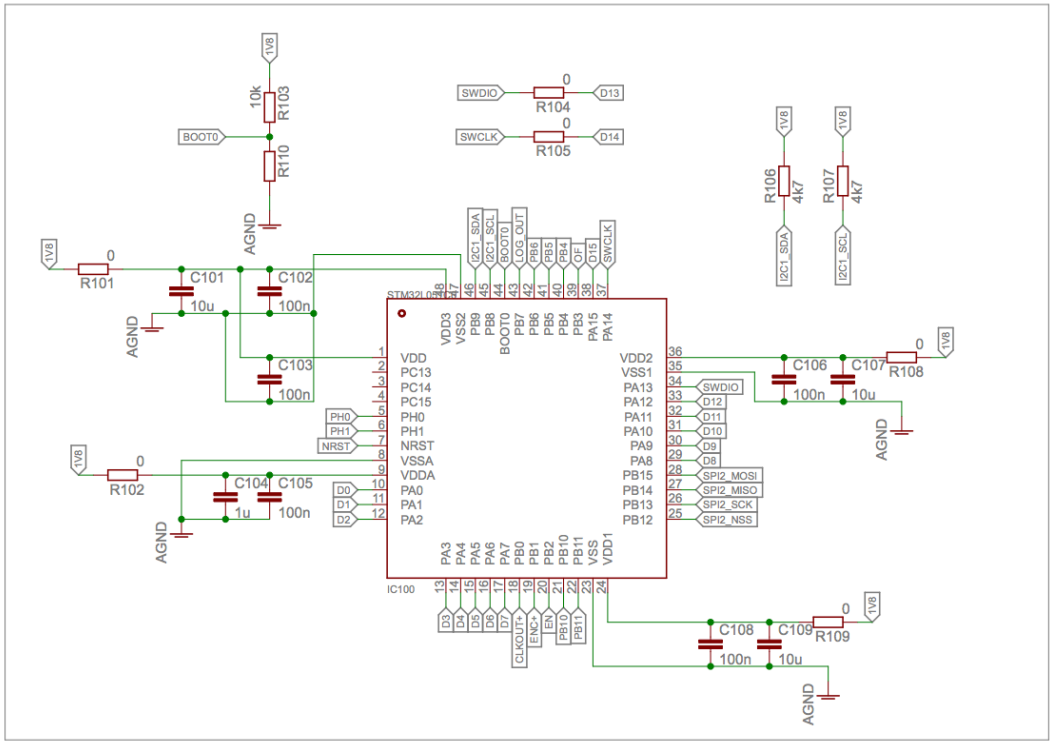

Figure 4.6: MicroController

for the I2C-bus connection to the J750. If higher speeds or high parasitic capacitance make it necessary these resistors will be switched to lower resistance values. During debugging and programming the PA13 and PA14 pins are used, which interferes with the 2 most significant bits of the parallel ADC data lines. Therefore during debugging R104 and R105 are not placed to prevent any problems. This reduced the full-scale range of the overall system during debugging. When simple programming is needed the resistors can be included because the ADC is not running during this time.

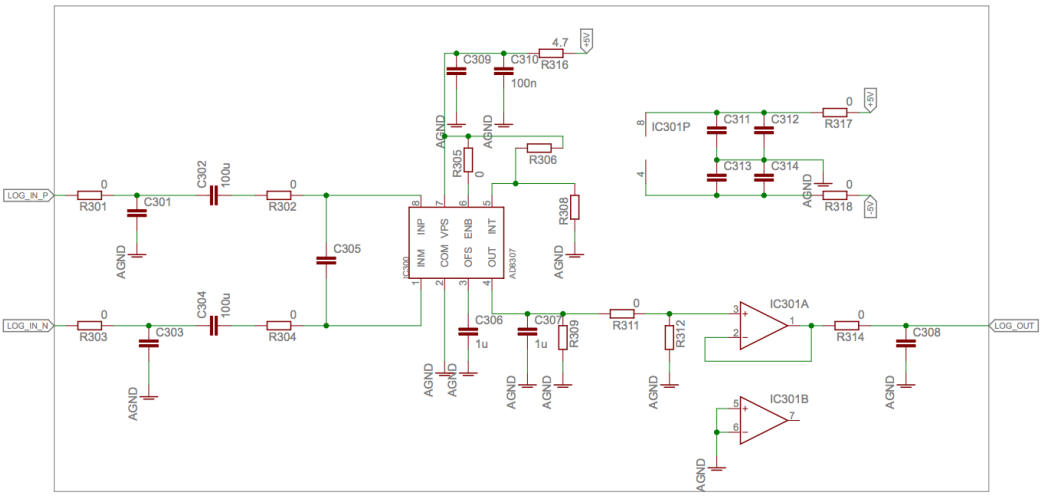

Figure 4.7: As an alternative measurement solution the logamp is setup as described in the datasheet. Low frequency extension is achieved by using a 100 MHz as a DC block at the input.

4.2.6 Logamp

The logamp, which is used as a backup solution is used mutual exclusive with the ADC. Therefore through hardware setup, either of those solutions is chosen. On the input, which is connected to the output of the 4th-order low-pass filter, external components are used if the input signal needs additional filtering. The 100 µF DC blocking capacitors are used to extend the low frequency response as described in the application note (Pilotte, 2005). R306 and R308 can be used to set the intercept of the logamp as it can be seen in the datasheet (*AD8307 Low Cost, DC to 500 MHz, 92 dB Logarithmic Amplifier* 2008). The ENB pin is set to VDD to enable the device and 1 µF capacitors are connected between pins OFS and OUT and ground. At the output, a voltage divider and a buffer are used to scale the output signal, so that it can be used as an input for the microcontroller. Again 100 nF bypass capacitors and series resistors are placed near supply pins.

4.3 Layout

During placement and layout, it was important to keep a clean differential signal path on the analog side of the ADC. Careful separation of digital and analog circuits was of high priority to reduce the influence of clock and data lines of the ADC on the analog input signal.

The top and bottom layer were used for signal routing to provide easy access in case of any problems during debugging and testing. Area that was not needed for routing was filled with ground areas, to provide shielding and a good connection to ground at every point in the circuit.
The second layer was used completely as a ground layer to provide further shielding of the supply in the third layer.

One key point was to support differential routing of the analog signal to the ADC as far as possible. Components that supported differential processing were used where possible and the 4th-order low-pass filter circuit is using the same layout for both signal lines.
In the end, a difference in length of the differential paths was less than 1 mil. A lot of additional components lead to a less ideal solution that could be improved after the design is proven.

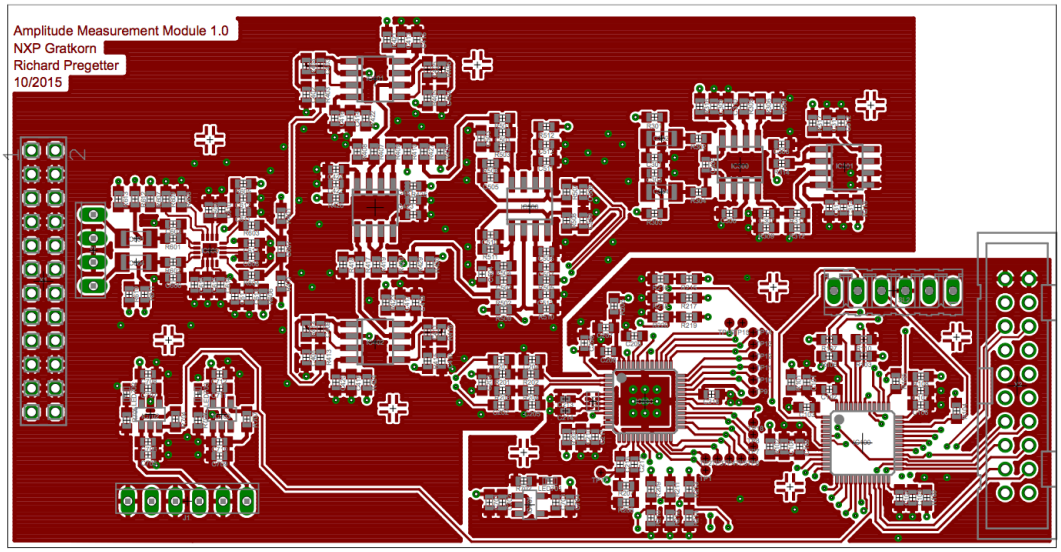

Figure 4.8: Top Layer

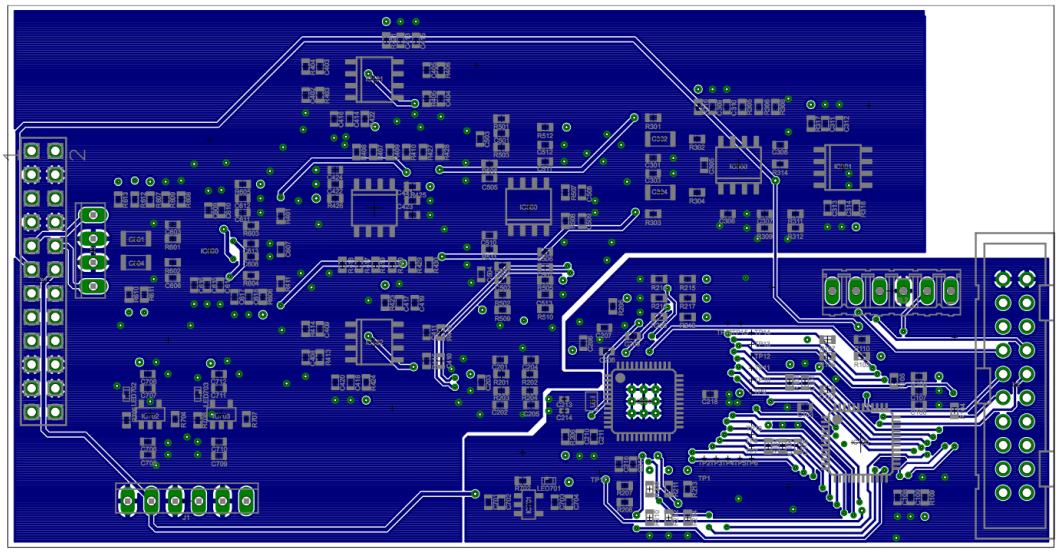

Figure 4.9: Bottom Layer

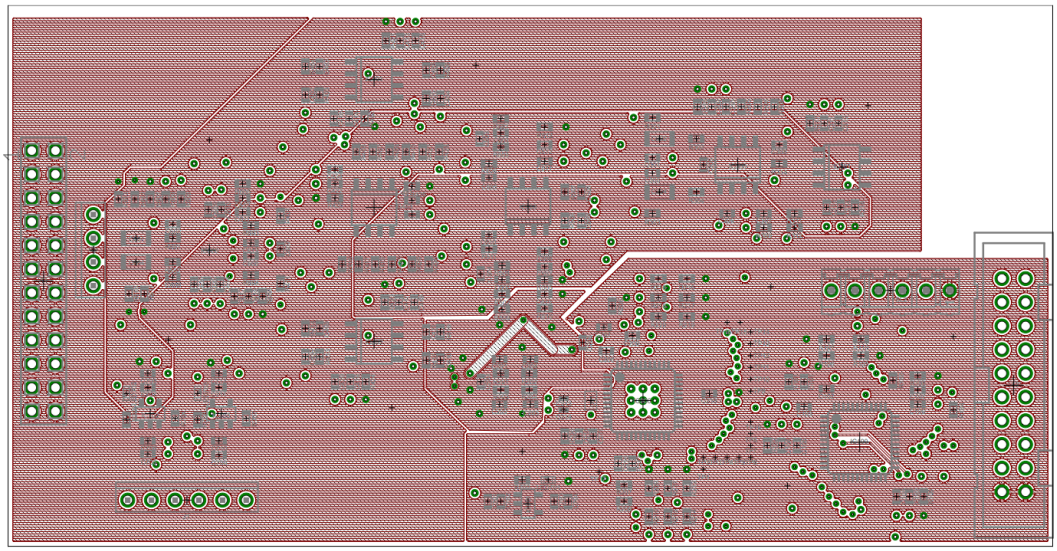

Figure 4.10: Supply Layer

5 Different solutions in Matlab

The use of an ADC with a microcontroller provides a lot of flexibility how to derive the actual amplitude of the input signal. By limiting the signal to a sine wave this property can be used to simplify the acquisition of said amplitude.

As a starting point, the calculation of an FFT would be sufficient. This will provide a frequency representation of the input signal. By definition, the input sine wave is the frequency with the highest amplitude. Therefore, after calculating the FFT, a search for the highest bin has to be done.

This shall be the worst-case scenario and less complex solutions will be simulated in Matlab to reduce calculation time of the result.

5.1 Limiting factors

The ADC with a sampling rate of roughly 1 MSps will sample the signal. This means that for signals higher than 500 kHz the input is undersampled and aliasing will occur. Information about the real input frequency will be lost and superposition of error frequencies can cause an error of the amplitude measurement.

Due to the fact that the frequency of the input signal is roughly known and is not the scope of the measurement the problem of undersampling is mostly negligible as long as the noise and the amplitude of error frequencies are not too high.

Ideally, the frequency could be measured as well if it is already roughly known. But due to multiple errors that influence this measurement the

actual frequency and the frequency that can be derived from the samples provided by the ADC can be different. Errors may be introduced by:

- Clock in the J750 that provides the clock for the DDS
- PLL of the DDS
- Internal clock of the microcontroller
- PLL of the ADC

To circumvent this problem the measurement shall not rely on knowing the exact frequency of the input signal.

Additional problems are caused if the input signal is low in frequency. The DFT will not provide good results when only a few periods of the signal are sampled. A different approach will be needed when measuring low input frequencies.

5.2 Worst case, 512 point FFT

To define a point to start with, a 512 point FFT is taken as the worst case scenario. The Fast Fourier Transform is an algorithm that is optimized to calculate the DFT of a signal. All frequency bins are calculated with this algorithm and afterward, the frequencies with the maximum amplitude is searched and taken as the result. Even though this algorithm is supported by the ARM Cortex M0+ other solutions will be looked at to reduce computation time and increase amplitude resolution. These different solutions will be compared with the 512 point FFT in Matlab with a model including additive white Gaussian noise and distinct frequencies that will represent error frequency introduced by other analog signals, or data and clock signals. Later the same algorithms will be used with a real signal taken from the RXP and RXN pins at the load board of the automated test environment. The signal is sampled by a 12-bit scope and therefore provides lower accuracy than the 16 bit ADC used with the prototype board.

5.2.1 Matlab Model

The signal generated in Matlab to test the different solutions is build up from a sine wave that is swept from 1 kHz to 499 kHz in 1 kHz steps. Added are distinct error frequencies and additive white Gaussian noise with -20 dB in reference to the input signal. See the table (5.1) for the error frequencies and the corresponding levels compared to the input.

Frequency[kHz]	Amplitude [dB]
40	-20
120	-14
240	-10
325	-26
400	-6

Table 5.1: Frequency and Amplitude of Errors used in Simulation

The final signal the different approaches are tried on is given by:

$$s = s_i + \sum s_e + AWGN(-20dB) \tag{5.1}$$

with s_i being the input signal and s_e being the distinct error frequency.

5.2.2 Simulation results for 512 sample FFT

The input signal is generated and the Flat-Top window is applied before using the FFT function in Matlab. In figure (5.1) the relative error in compared to the ideal amplitude of 0 dB over the frequency range of 1 kHz to 499 kHz is displayed. Spikes in the error can be seen when the input signal is close to a distinct error frequency. At 400 kHz the -6 dB signal leads to an amplitude error of up to 60% while the -26 dB error frequency at 325 kHz introduces an error below 10%.

Frequencies near DC and near half the sampling frequency at 500 kHz show a large error. These frequency bins are not usable for amplitude measurements and need to be avoided.

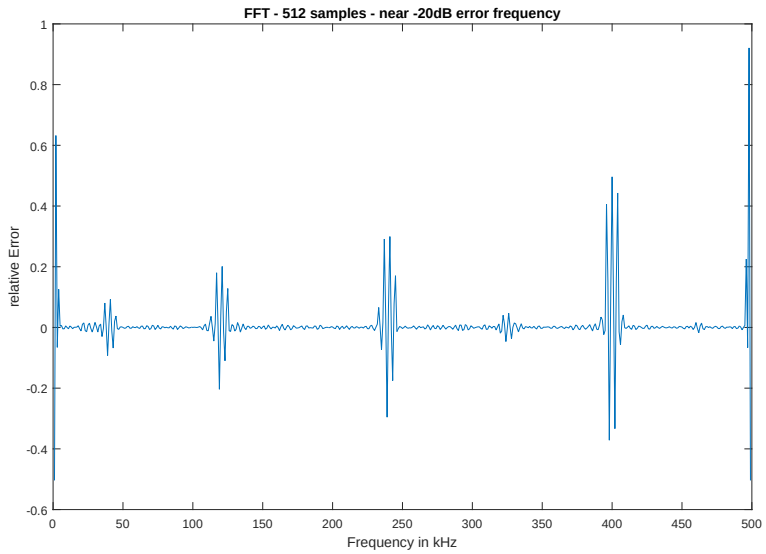

Figure 5.1: Error of FFT with 512 samples. The input signal is swept from 1 kHz to 499 kHz and the relative error compared to the ideal 0 dB result is displayed. Close to distinct error frequencies the amplitude error increases up to 60%.

In figure (5.2) a frequency range close to the error frequency at 40 kHz is shown. The error when no distinct error frequency overlaps with the input signal and only additive white Gaussian noise is present stays below 2%.

5.3 Iterative DFT with Görtzel algorithm

A first step to reducing computation time is to reduce the amount of sample to use to compute the FFT. This will reduce the frequency resolution and the problem near distinct error frequencies will be even more prominent as the same frequency bin will contain a larger span of frequencies.

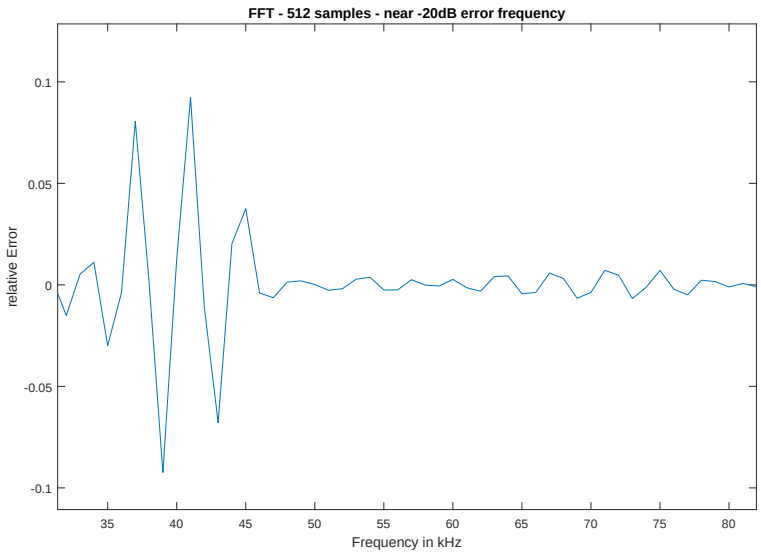

Figure 5.2: Error of FFT with 512 samples, near error frequency. The input signal is swept from 1 kHz to 499 kHz and the relative error compared to the ideal 0 dB result is displayed. When the input signal is near a distinct error frequency the amplitude error is above 2%. When only white gaussian noise is present the error stays below 2%

A way to prevent this is to use an FFT with a lower number of samples to find the frequency of interest and then calculate the amplitude at this frequency. The Görtzel algorithm is used to calculate the DFT at one frequency bin with a larger number of samples.

5.3.1 Quadratic curve fitting

To find the frequency of the input signal, which is per definition the frequency with the highest amplitude, quadratic curve fitting is used. Jacobsen, 1999

By using the frequency bin with the highest frequency bin and the two next to it, a parabola, a quadratic curve can be fitted, that will contain all three points and which maximum will be a closer estimate of the real frequency with maximum amplitude. The formula for a quadratic curve can be written as follows:

$$y = a \cdot (x + b)^2 + c \tag{5.2}$$

Three degrees of freedom can be calculated by three points of the curve. This can be used to compute the properties of the curve. Below is the formula provided by Jacobsen, 1999:

$$b_{dif} = \frac{y_{-1} - y_{+1}}{4 \cdot y_0 + -2 \cdot y_{-1} - 2 \cdot y_{+1}} \tag{5.3}$$

With b_{dif} being the difference of the newly estimated frequency from the current maximum frequency bin. b_{dif} is given as a fraction of the distance between two frequency bins and is in the interval of $[-0.5, 0.5]$. y_0 is the amplitude of the highest frequency bin. y_{-1} and y_1 are the amplitudes of the bins next to it.

An example of curve fitting is shown in figure (5.3)

5.3.2 Iterative frequency estimation

First, a 32 sample FFT and a search for the maximum frequency bin is done. Then a quadratic curve fitting is used to estimate the new frequency of interest. The Görtzel algorithm is then used with 128 samples to compute three frequency bins at the estimated frequency and next to it. A second curve fitting, to estimate the frequency more accurately, and a final use of the Görtzel algorithm with 512 samples provide the final result.

If the input frequency is known and accurate enough, the first step of the 32 sample FFT can be left out and the process can be started with calculating three frequency bins with the Görtzel algorithm and 128 samples.

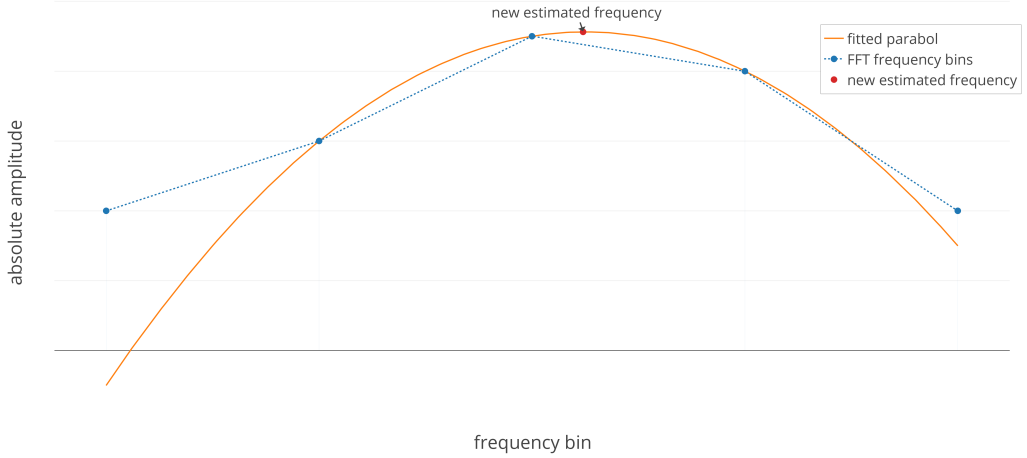

Figure 5.3: A low-resolution FFT is fitted with a quadratic curve using the maximum frequency bin as well the bins next to it. The peak of the parabola is at a frequency that is an estimate of the real peak in the frequency spectrum.

5.3.3 Simulation results for iterative DFT

The same model as before is used, and the Flat-Top window is applied before using the last calculation of the Görtzel algorithm. Up until this step, the frequency resolution is more important. Only the last calculation needs increased amplitude accuracy.

In figure (5.4) the relative error in comparison to the ideal 0 dB signal is shown in blue. In red the additional error in comparison to the 512 sample FFT can be seen. Increase in error is most notable near the large error frequencies at 400 kHz and 250 kHz. This is due to the fact, that the process of finding the right frequency results wrong estimates and the amplitude at the wrong frequency bins are calculated.

The additional error at error frequencies with lower amplitude or in frequency ranges with only additive white Gaussian noise is low or none at all as can be seen in figure (5.5) The additional error at error frequencies with lower amplitude or in frequency ranges with only additive white Gaussian noise is low or none at all as can be seen in figure (5.5)

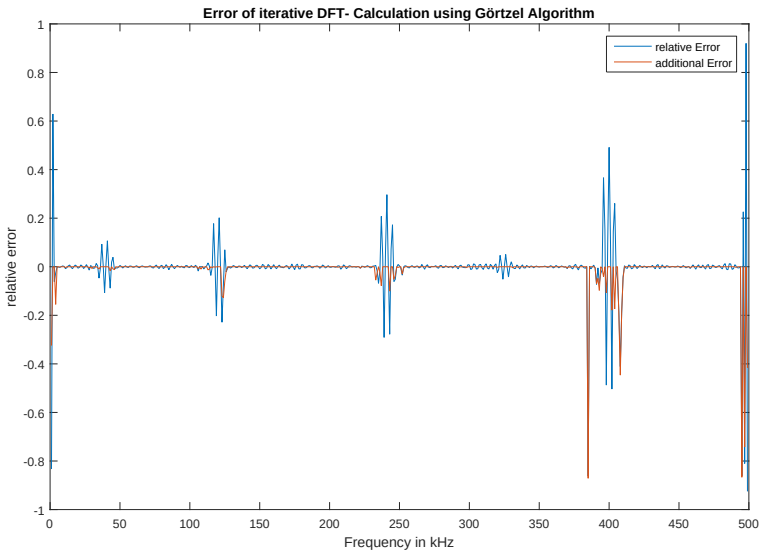

Figure 5.4: Error of iterative DFT with 512 samples, near error frequency. In blue the relative error compared to the ideal 0 dB signal is shown. In red the additional error of the iterative process compared to the 512 sample FFT shows a worse result mostly near high amplitude error frequencies.

5.4 Quinn-Fernandes Frequency Estimation

Another approach to finding the maximum frequency is the method by Quinn and Fernandes described by Kootsookos, 1999. A similar algorithm is proposed by Ta-Hsin Li, 1998, which introduces additional parameters to decrease the number of iterations the algorithm needs for a given accuracy.

The time domain input samples are used as the input for the following second-order all-pole filter:

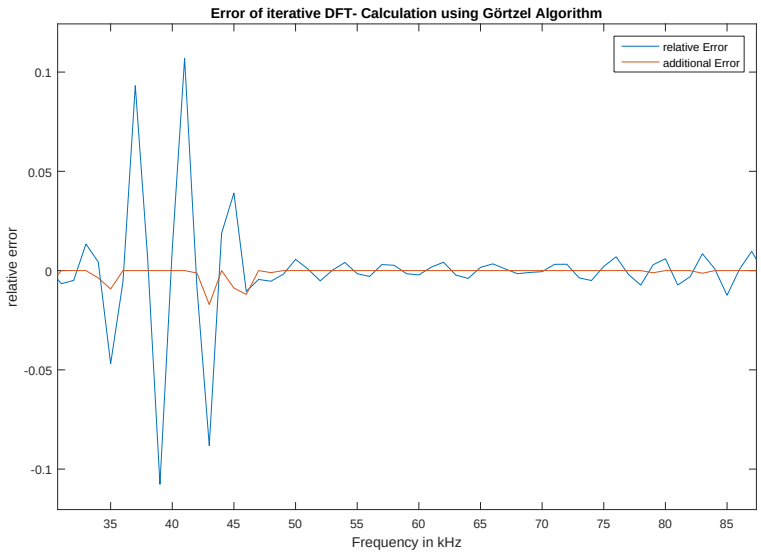

Figure 5.5: Error of iterative DFT with 512 samples, near error frequency. At lower amplitudes of the error frequencies and with only additive white Guassian noise, the results are almost the same as with the 512 sample FFT.

$$H(z^{-1}, a) = \frac{1}{1 + (1 + \eta^2) \cdot a \cdot z^{-1} + \eta^2 \cdot z^{-2}} \tag{5.4}$$

with

$$a = \cos(2 \cdot \pi \cdot f_{est}) \quad \text{and} \quad \eta \in [0, 1] \tag{5.5}$$

The output $y[n]$ with $x[n]$ being the time domain input samples

$$y[n] = x[n] + \left(1 + \eta^2\right) \cdot a \cdot x[n-1] + \eta^2 \cdot x[n-1] \tag{5.6}$$

is used in the least square estimator to compute the next estimated frequency:

$$a_{m+1} = \frac{\sum y_{t-1}(a_m) \cdot \{y_t(a_m) + y_{t-2}(a_m)\}}{2 \cdot \sum y_{t-1}^2(a_m)} \tag{5.7}$$

This calculated frequency estimate can be used in the next iteration of the algorithm. Closing further in on the real frequency. The use of 32 input samples, and 5 iterations with $\eta = 0.95$ showed good results in simulation. Important is the first guess of the frequency estimate in the first iteration. Due to the frequency being roughly known the first guess will not be off by much and the algorithm will work properly. After the frequency is determined the Görtzel algorithm is again used to calculate the amplitude at this frequency.

5.4.1 Simulation results for Quinn-Fernandes algorithm

In addition to the previous simulations, a first guess of the frequency is needed for the first iteration of the algorithm. This frequency is chosen as 95% of the real input frequency.

Figure (5.6) shows the absolute error of the Quinn-Fernandes algorithm in blue and the additional error compared to the 512 point FFT in red. For the most part, this is the same error we see for the quadratic curve fitting approach. The reason for this is that the error seen is mostly attributed to the Görtzel algorithm, which is used in both cases.

An increased error is observed at the 250 kHz and 420 kHz error frequencies. In the range above the error frequencies, a constant high error is displayed. Due to the first guess of the frequency as an input to the algorithm being below the error frequency, and the error frequency being close in amplitude to the maximum frequency, the algorithm estimates the error frequency as the frequency of interest. This suggests that the Quinn-Fernandes algorithm is vulnerable to distinct high error frequencies.

When looked closer at a distinct error frequency with lower amplitude the same picture as with the iterative DFT is drawn.

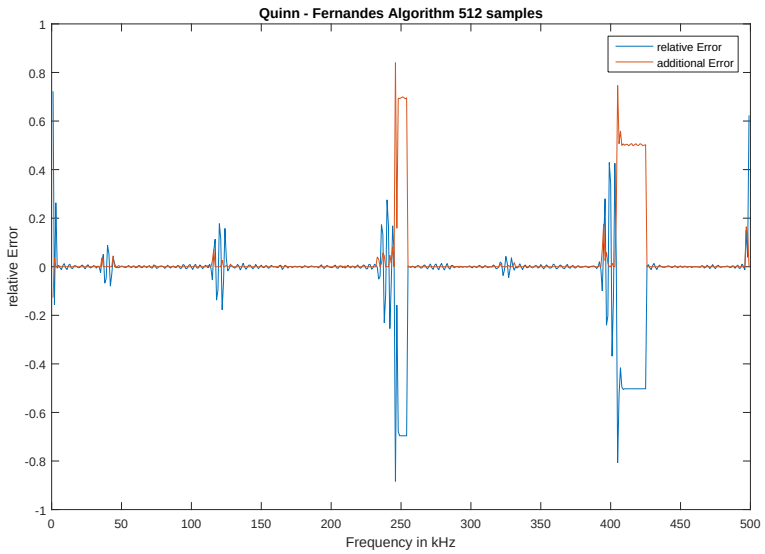

Figure 5.6: Error when using Quinn-Fernandes Algorithm. The additional error can be seen as with previous simulations. This is because the Görtzel algorithm when compared to the FFT causes it. An increase in error is observed near the distinct error frequencies with high amplitude. Here the Quinn-Fernandes estimates the maximum frequency falsely and therefore the wrong amplitude is calculated.

5.5 Jenq-Crosby amplitude estimation

Another way to acquire the amplitude of a sine wave is described by Y.C.Jenq and Crosby, 1988. The algorithm to estimate the amplitude directly is a root mean square calculation on the time domain samples, on which first a Blackman-Harris window was applied. In the end, the weighting of the window is compensated.

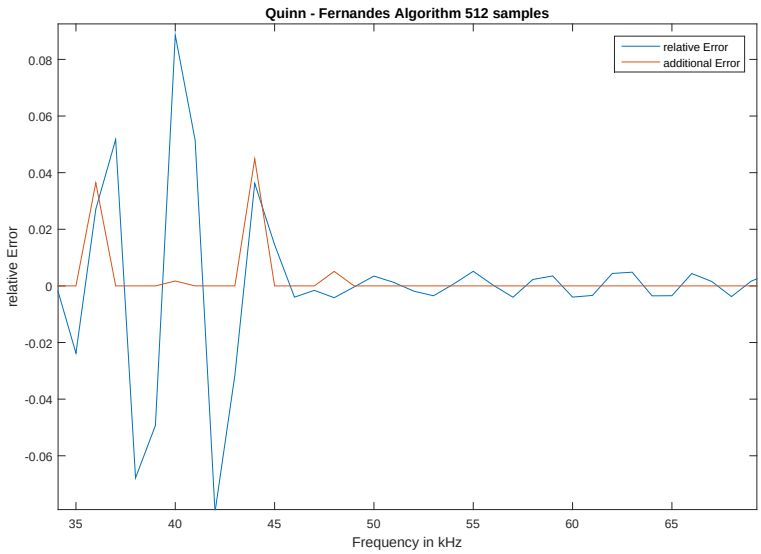

Figure 5.7: Error when using Quinn-Fernandes Algorithm, near error frequency with lower amplitude. The same results as with the iterative DFT are shown. Only the error introduced by the Görtzel algorithm is displayed.

$$A = \left(\frac{\sum_{k=0}^{N-1} w_k \cdot {s_k}^2}{2} \right)^{\frac{1}{2}} \cdot \left(\sum_{k=0}^{N-1} w_k \right)^{\frac{1}{2}} \tag{5.8}$$

With w_k being the coefficients of the window function and s_k being the input samples. The division by $\sqrt{2}$ is done to convert from RMS to an amplitude of a sine wave.

This solution uses only time domain samples and apart of the square root, which is only calculated once no intensive calculations are needed. On the other hand, the RMS calculation computes power and therefore noise and distinct error frequencies contribute to the final results more than in the

previous approaches. In a given environment this would be seen as an offset that can be compensated.

5.5.1 Simulation for Jenq-Crosby amplitude estimation

When looking at the absolute error of this amplitude estimation, a constant offset over the whole range is displayed as expected. Distinct error frequencies show an increase in error, but less than with previous algorithms.

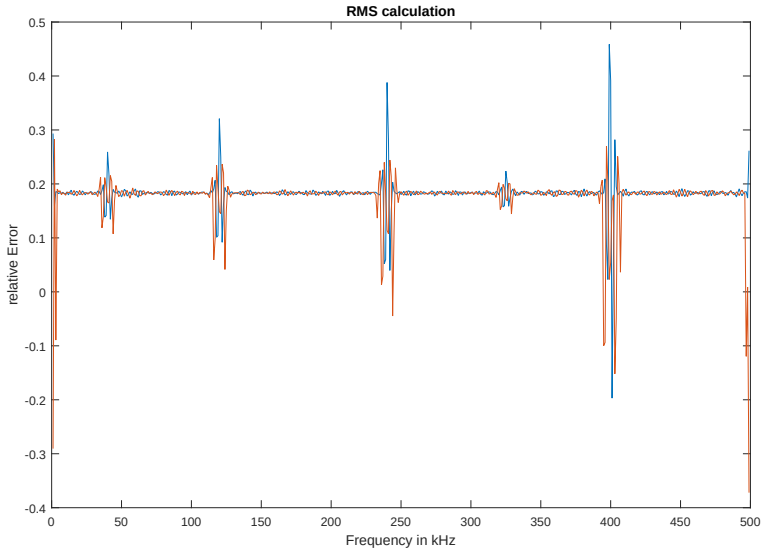

Figure 5.8: Error when using Jenq-Crosby amplitude estimation. A constant offset over the whole frequency range is displayed.

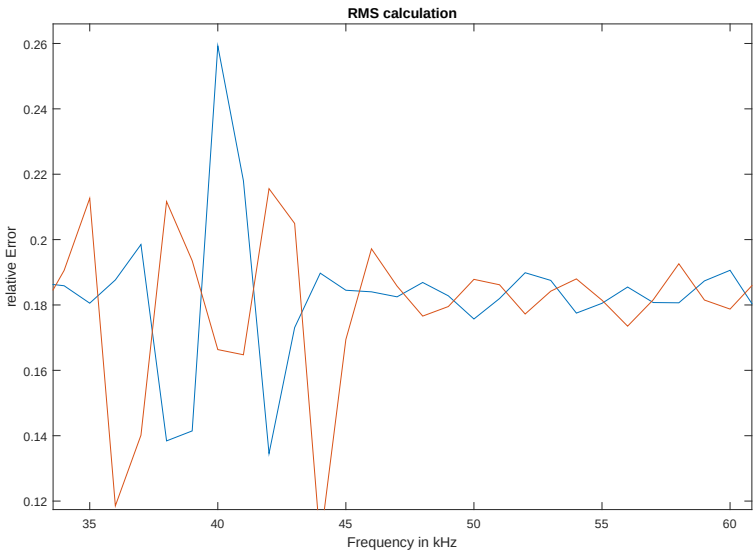

Figure 5.9: Error near error frequencies: Distinct error frequency near the input frequency do not influence the results as much as in previous

5.6 Real Data

After simulating the algorithms with a signal model including error frequencies and noise, real data is used to evaluate and compare their applicability.

The data was collected at the automated test environment, during a standard test setup, with a scope at 8-bit amplitude resolution. As an input frequency 13.56 MHz was chosen, as this will be one main use-case for the amplitude measurements module. The amplitude was measured with the scope as 14 mV. Samples with an interval of 1 µs were taken from the collected data to emulate 1Msps sampling. To get an overview how the signal will look after undersampling and with aliasing of all frequencies into the baseband

a 32768 point FFT was computed.

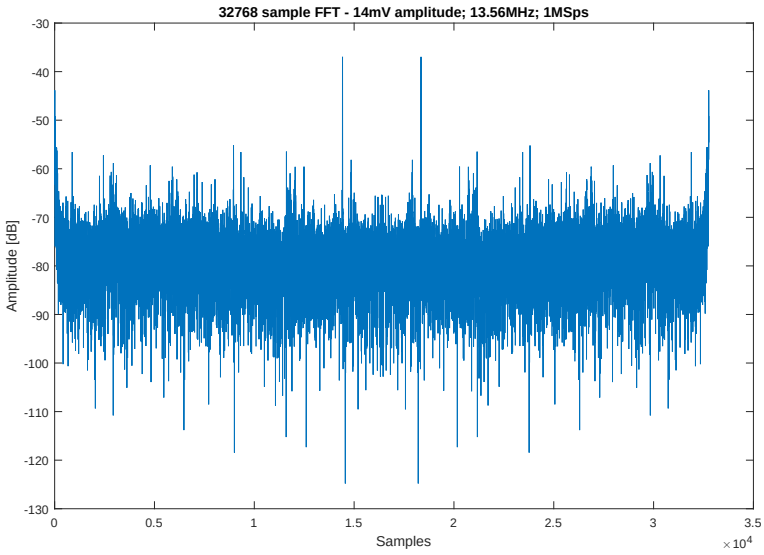

Figure 5.10: FFT of the measured signal at the automated test environment. 8 bit amplitude resolution and 1Msps. Every frequency is shifted to the baseband between 0 kHz and 500 kHz.

A difference of more than 20 dB is shown between the maximum frequency and the next highest one. This is a better environment than the on the algorithms were checked for in simulation.

5.6.1 Real data results

First an input signal with 13.56 MHz and 1000 mV was set, and measured with the scope at points of interest. The collected data was treated as

described above and then processed by the algorithms. Additional measurements with lower frequency and amplitude were done as well. The results are presented in the tables below.

For comparison, the peak-peak value is shown as well. This value was computed by taking the difference between the highest and the lowest of 65536 samples and divide it by two. As the true value, the maximum of an FFT of all those samples was chosen. All percentage errors were computed in regards to this value.

Solution	Amplitude [mV]	Error [%]
pp/2 65536 samples	987.5	5.43
65536 sample FFT	936.6	0
256 sample FFT	936.5	-0.01
Iterative DFT	936.5	-0.01
QF- Alg.	936.5	-0.01
RMS	936.1	-0.05

Table 5.2: Results for an input signal that was measured with 1000 mV and a frequency of 13.56 MHz by the scope. All three algorithms that use the FFT or the Görtzel Algorithm, showing same results as expected. The RMS based algorithm is also well in the limit of $\pm 2\%$.

Solution	Amplitude [mV]	Error [%]
pp/2; 65536 samples	73.2	515.49
65536 sample FFT	14.2	0
256 sample FFT	14.3	0.07
Iterative DFT	14.3	0.07
QF- Alg	14.3	0.07
RMS	20.1	41.55

Table 5.3: Results for an input signal that was measured with 40 mV and a frequency of 13.56 MHz by the scope. The three algorithms that are DFT based are inside the limit of $\pm 2\%$. At this low amplitude, noise (also from the scope) and distinct error frequencies contribute a lot to the RMS value.

For the 400 Hz input signal a lower sampling rate and a longer acquisition time was used. For 256 samples the acquisition time is 32.5 ms. In comparison to before, the error is larger for all simulated algorithms. This is probably due to the fact, that the baseband is roughly 4 kHz and more noise and distinct error frequencies occupy the same frequency bin due to undersampling.

Solution	Amplitude [mV]	Error [%]
pp/2 65536 samples	1044.0	4.12
65536 sample FFT	1002.7	0
256 sample FFT	1006.3	0.36
Iterative DFT	1006.3	0.36
QF- Alg	1006.3	0.36
RMS	1004.3	0.16

Table 5.4: Results for different solutions with a signal of roughly 1000 mV amplitude and a frequency of 400 Hz. In this case the RMS based value provides numbers, closer to the reference given by the 65536 point FFT than the other algorithms. It is not much effected by more frequencies being undersampled and therefore sharing the same frequency representation in the baseban.

Solution	Amplitude [mV]	Error [%]
pp/2 65536 samples	91.8	235.38
65536 sample FFT	39.0	0
256 sample FFT	37.8	-3.08
Iterative DFT	37.8	-3.08
QF- Alg	37.8	-3.08
RMS	41.6	6.67

Table 5.5: Results for different solutions with a signal of roughly 40 mV amplitude and a frequency of 400 Hz The superposition of multiple frequencies in shifted on the same frequency in the baseband, leads to a larger error with lower amplitudes. Neither algorithm leads to a results within the limits of $\pm 2\%$. For lower amplitudes the DFT base algorithms are better than the RMS base one, even for lower frequencies.

5.6.2 Suggestions for further improvements

This chapter shows different approaches to calculating the amplitude of the input signal in a model and for real data. The results look promising for a sampling rate of 1 Msps but are not inside the limits for a sampling rate of around 8 ksps. A better solution for lower frequencies needs to be found. Below 30 kHz, the amplitude accuracy of the DFT is diminished, due to being to close to the lower end of the baseband near DC.

The same problem is observed near half the sampling frequency, at the upper limit of the baseband. Here a change in sampling frequency can solve the issue. A rule set for the whole frequency range up to 15 MHz is needed.

6 Measurements

To judge the quality and reliability of the algorithm and the prototype board, measurements with the complete system were done. The algorithm of choice for these measurements is the previously discussed Quinn-Fernandes algorithm for frequency estimation, with a Görtzel algorithm at the estimated frequency afterward, to determine the amplitude.

In a first step, the measurements were done with a single-ended signal generator connected to the positive input of the prototype board, while the negative input is pulled to ground. The differential path of the signal chain is mostly unused in this case, but the signal generator can be used as a reference to judge the accuracy of the measuring system.
Next, measurements are done at the load board of the automated test environment, with the input signal set up by a standard routine used in a typical test case. The signal at the RX input pins of the device under test is connected to the differential input of the prototype board. The differential signal chain is used and the amplitude detection circuit is used in the environment it is intended for.

At first, the fourth-order low-pass filter is bypassed and will be only used if necessary. In both setups, with the signal generator, as well as at the automated test environment, external power supply is used. In addition, the implementation of the I2C communication on the digital tester was not done and therefore all measurements are done with the microcontroller in debugging mode. The results are read out with the notebook directly over the debugging interface.

6.1 Measurements with the Signal Generator

A single-ended signal generator was used to provide the input signal to the positive input of the prototype board while pulling the negative input to ground. The LT6411 input buffer provides a single ended signal on the positive differential line and ground on the negative one. Bypassing the fourth-order low-pass filter the signal is routed to the level-shifter at the input of the ADC. Here the single-ended signal is converted to a differential one, which is provided at the input of the converter.

While keeping the microcontroller in debugging mode, 256 samples are acquired and processed by the algorithm. The results are read out via the debugging connection to the notebook.
These results are captured and presented below in addition to the mean value, the standard deviation, and linear curve fitting.

In the upper half of the figures, five results are shown at each measurement point, including the mean value, as well as a linear regression, which shows linearity over the input amplitude. In the lower half, the error of the measurements compared to the mean value is displayed as box-plots. The standard deviation of those five measurements is also displayed.
Only low amplitudes are shown here, as higher amplitudes suffer less from inaccuracy caused by noise, distinct error frequencies from the board and quantization noise during analog to digital conversion.

At first measurements with 173 kHz, 700 kHz and 2 MHz are done, as those are typical use-cases. Amplitudes as low as 5 mV stay within the specified $\pm 2\%$ error limits.

6.1.1 Measurement for 173 kHz with Signal Generator

At 173 kHz the error for signals above 25 mV amplitude is well within the limits. Lower amplitudes than stated in the requirements show still good results, by staying inside $\pm 2\%$ down till 5 mV amplitude. This first measurement was done with an increased number of amplitude steps.

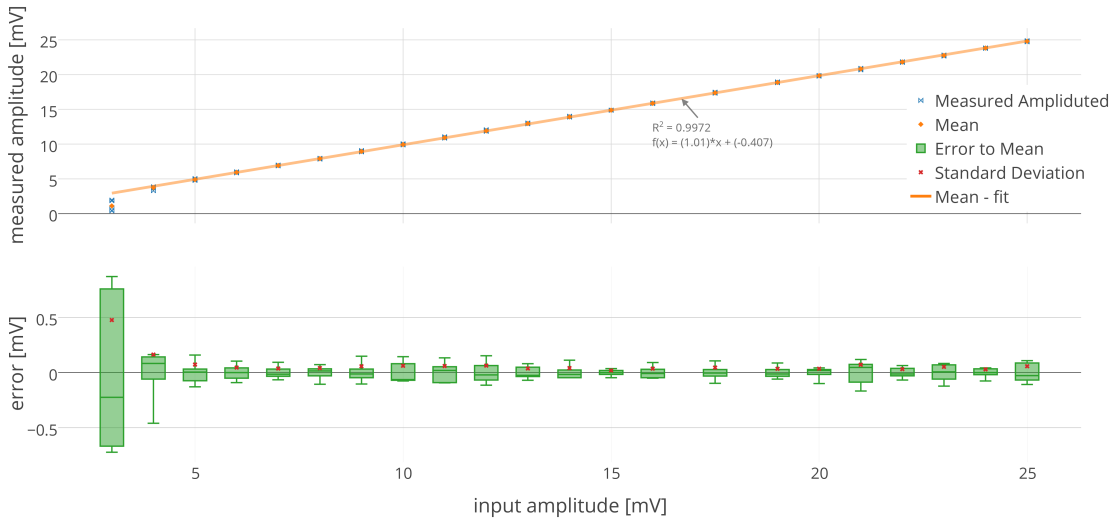

Figure 6.1: Measured data, mean value; error in regards to the mean value and the standard deviation are displayed. Higher input values lead to error well inside the specified error-limits of ±2%. Amplitudes as low as 5 mV are measured within the limits. The results increase linear with the input amplitude.

6.1.2 Measurement for 700 kHz with Signal Generator

The same measurements are done with an input frequency of 700 kHz. Similar results as before show that frequencies above the Nyquist frequency of 500 kHz, show the expected behavior when undersampled. The frequency estimation algorithm provides a result near 300 kHz. Due to the internal clock of the microcontroller being not ideal, the sampling clock is also not exactly 1 MHz. This results in a slight shift of the estimated frequency and gives good reason to the use of an estimation algorithm instead of using the set input frequency as the one, that is defining which frequency bin is calculated by the Görtzel algorithm. By slight changes in the sampling clock, the frequency representation of the input signal shifts as well. Using the estimation algorithm calculates the correct frequency of this representation and therefore makes sure, that the calculation of the amplitude yields the correct values

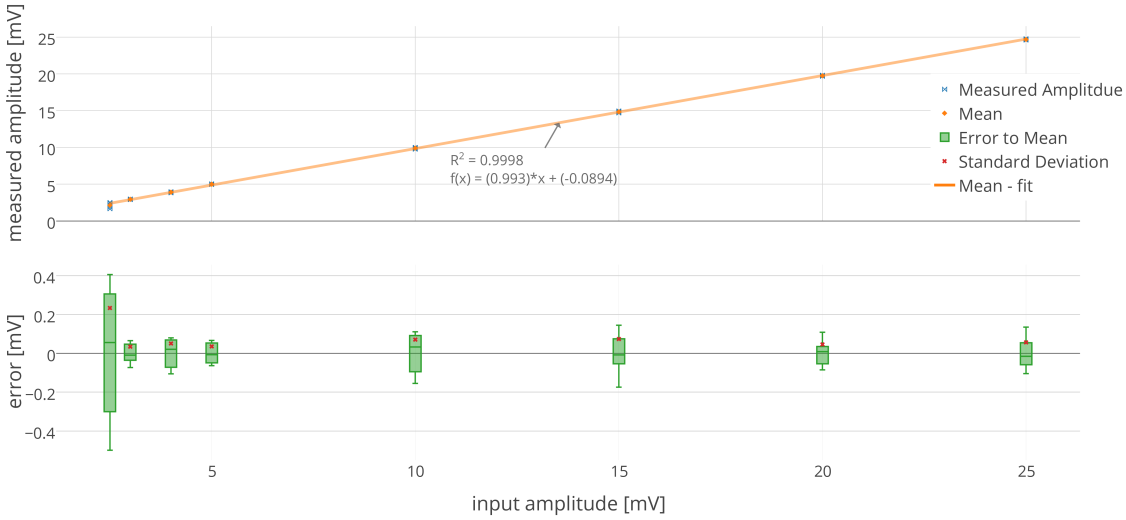

Figure 6.2: Measured data, mean value; error in regards to the mean value and the standard deviation are displayed. The undersampled signal shows similar results as the input signal in the baseband. Results even below 5 mV are accurate enough. The results increase linearly with input amplitude.

6.1.3 Measurement for 2 MHz with Signal Generator

A 2 MHz input signal is located exactly at an unusable frequency region when using 1 MHz as the sampling frequency. Therefore, the clock is changed to 1.143 MHz. This is done by not using 32 clock cycles of the internal 32 MHz clock of the microcontroller as the sampling period, but only 28 cycles. The input frequency is no longer aligned with the sampling frequency and usable results can be collected. Similar changes to the sampling clock need to be done at multiple input frequencies, which can be accomplished by using 3 different sampling frequencies.

Again, good results inside the limits are shown in figure (6.3). A different sampling clock and higher frequencies show no change in the behavior of the algorithm. Results down to 5 mV are usable.

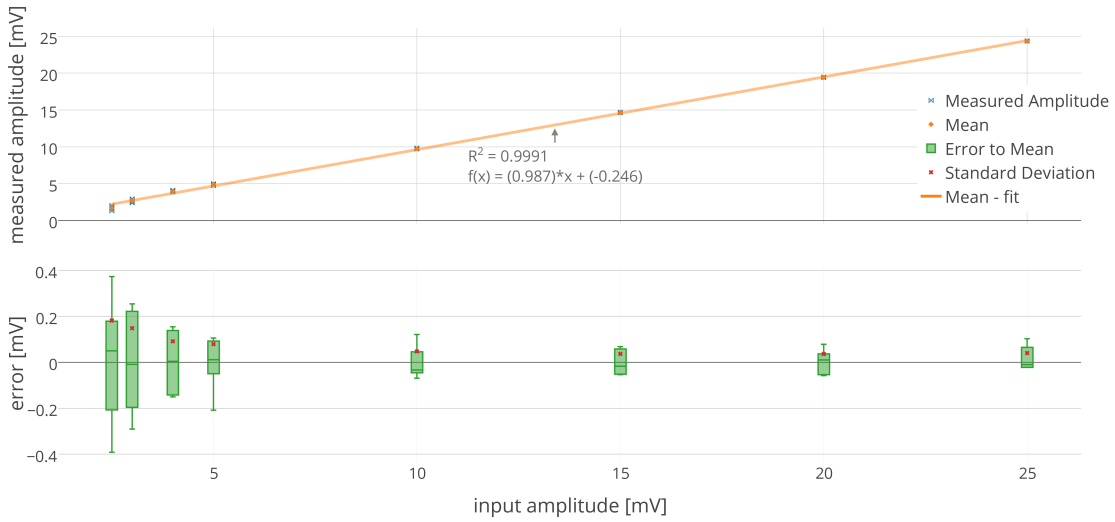

Figure 6.3: Measured data, mean value; error in regards to the mean value and the standard deviation are displayed. A different sampling clock and higher frequencies show no degradation of the measurements results.

6.1.4 Measurement for 13.56 MHz with Signal Generator

For 13.56 MHz, the most important frequency, as it is the carrier frequency of the NFC standard, results look less good. For all input amplitudes, the measurement error exceeds the limits of ±2%. The increase of the absolute error with the amplitude can be seen in figure (6.4) in the lower half. A linear fitting suggests a linear increase in error with the input amplitude. This can be seen as a constant relative error.
During the simulations, with higher noise and higher distinct error frequencies, this behavior was never noticed. With the absolute error not being constant it is also not caused by noise on the board or distinct error frequencies.

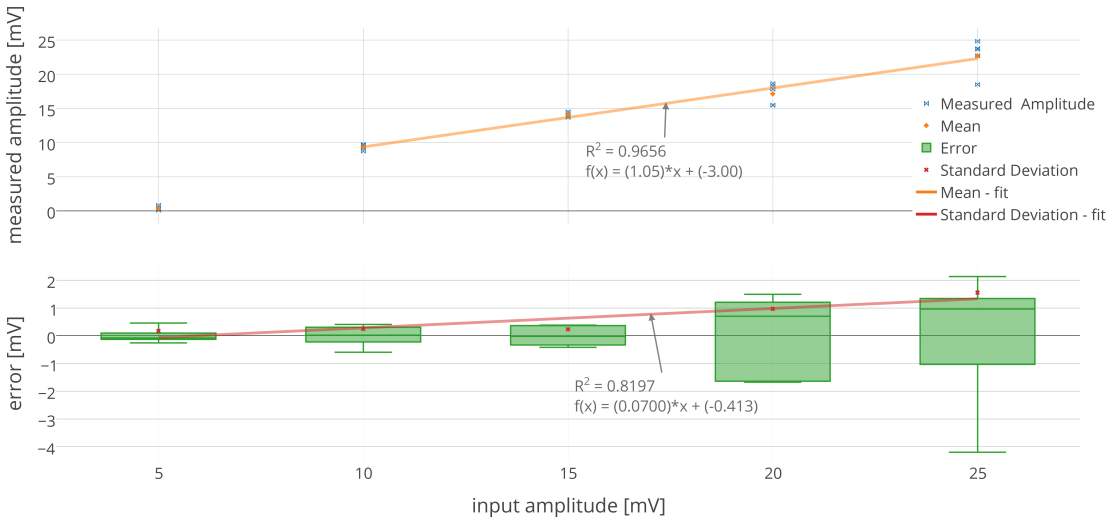

Figure 6.4: Measured data, mean value; error in regards to the mean value and the standard deviation are displayed. The error exceeds the error limits. A linear increase of the standard deviation with the input amplitude can be seen. Linearity of the mean value is still visible.

6.1.5 Measurement over bandwidth with Signal Generator

To investigate the error seen at 13.56 MHz further measurements were done for multiple frequencies. An input amplitude of 25 mV was chosen and measurements are done for every 1 MHz. An increase of the error with increasing input frequency is shown in figure (6.5). Simulations show, that with the same model of noise, input frequencies with the same frequency representation in the baseband, show the same results.
In addition, the sampled values provided to the algorithm in Matlab show the same errors, as the algorithm run on the microcontroller. All this suggests a problem during signal conditioning or during sampling. A measurement with the oscilloscope at the input of the ADC shows no attenuation of the signal up to 15 MHz.

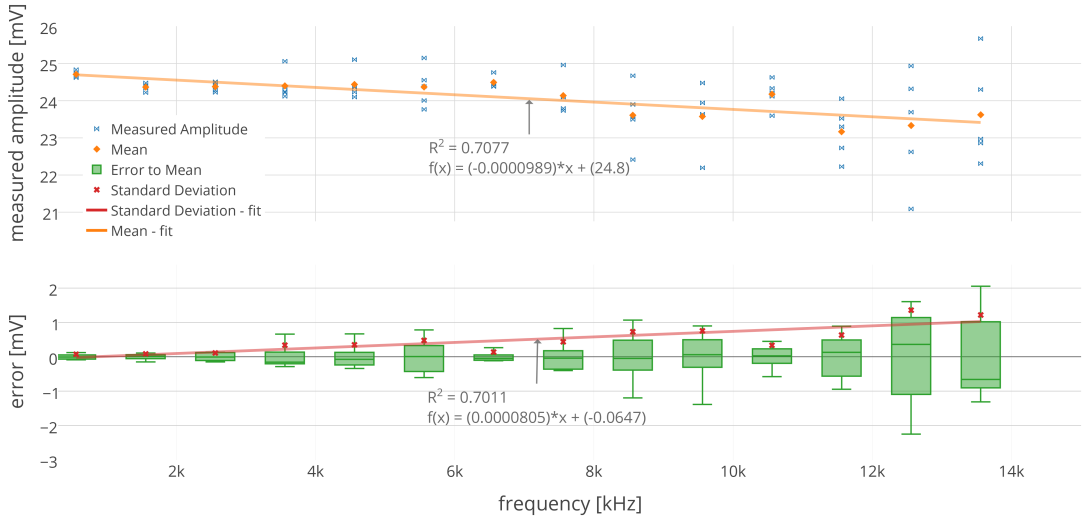

Figure 6.5: Measurement from 0.56 MHz to 13.56 MHz are displayed. The standard deviation of the error increases with frequency.

6.2 Sampling Jitter

From the measurements above, some characteristics of the error can be derived. The error is only noticeable with higher input frequencies. At lower frequencies, the error is within the limits of $\pm 2\%$.
For higher frequencies, the error increases with input amplitude as well as with input frequency. With the samples collected from the sampling process of the ADC, the same error is calculated with the algorithm in Matlab. In contrast, no error is shown when using samples taken with an oscilloscope and provided to either Matlab or the algorithm on the microcontroller. This removes the implementation of the algorithm with fixed-point calculation as the issue.

All these findings suggest sampling jitter as the cause for the error. It is the non-ideality of the sampling process due to clock jitter. The time deviation of the sampling clock causes an error in amplitude as it is depicted in figure (6.6). This error is present as noise at the signal frequency and is dependent

on the amplitude of the signal as well as on the frequency.

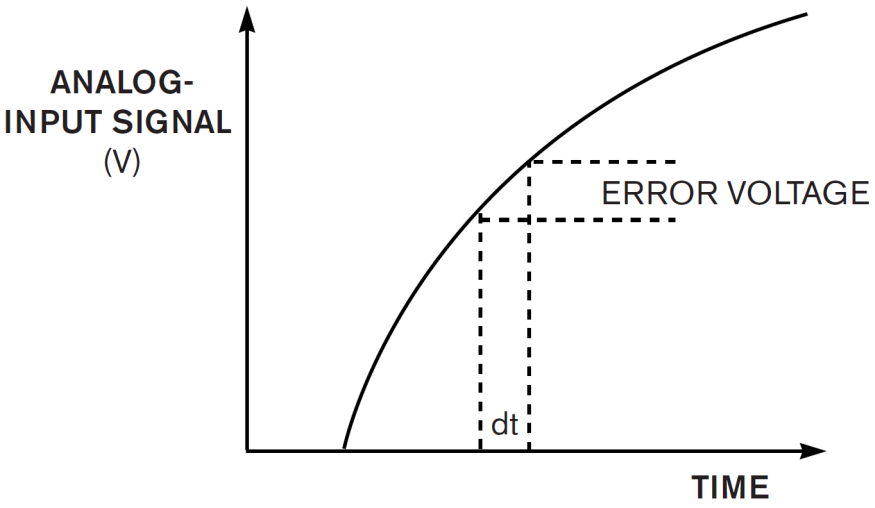

Figure 6.6: Deviation in sampling time leads to deviation in amplitude. A higher amplitude of the signal leads to more amplitude deviation and more noise. The error is dependent on the signal amplitude. The SNR of the noise is only dependent on the jitter and the input frequency, but not on the input amplitude.

Sampling Jitter causes noise with an SNR independent on the signal amplitude because a larger amplitude leads to time deviation causing larger deviation in amplitude.
Steeper flanks of the input signal lead to more deviation in amplitude with the same jitter. Therefore, higher frequencies lead to more jitter-noise.

The formula to calculate the SNR is given as

$$SNR_{Jitter}[dBc] = -20 \cdot \log\left(2 \cdot \pi \cdot f_{IN} \cdot t_{Jitter}\right) \tag{6.1}$$

with f_{IN} being the input frequency and t_{Jitter} being the clock jitter in seconds.

Independence of SNR (or linear dependence of the error itself) in regards to the amplitude and linear dependency in regards to the frequency are traits,

shared between sampling jitter and the error seen in the measurements above.

Due to the design, an output pin of the microcontroller without further conditioning provides the sampling clock for the ADC. This is poor design regarding sample jitter.
The specifications of the ADC were misinterpreted as the internal PLL of the ADC is not able to condition the clock as well as needed, contrary to the assumptions during design.
Improving the sampling clock jitter could be done by using an external clock generator for the microcontroller or by using a suitable external PLL.

6.3 Measurements with the J750 Automated test environment

Knowing the limitation due to sampling jitter, additional measurements at the automated test environment are done. The system is set up with a device under test on the load board while stepping through a typical test procedure that provides the input signal. Additional noise is expected on the load board, compared to the measurements with the signal generator.

The supply is provided by an external power supply and not by the J750 this leads to long power connections near digital signals and ground loops may introduce additional noise.
Development for the I2C communication on J750 was not possible due to limited time it was free to use. Measurements results are again read out via the debugging connection.

6.3.1 Measurements for 173 kHz

When generating frequencies below 2 MHz on the load board, a direct digital synthesizer is used. The settings were not calibrated for this particular load board and therefore the settings in the test program were taken as the

reference of the measurements. The results increase linearly with the input amplitude and the error is inside the limits of ±2%. In figure (6.7) the measurements down below 10 mV show usable results. Additional noise and distinct error frequencies from the load board do not show a significant increase in error.

Figure 6.7: Measured data, mean value; error in regards to the mean value and the standard deviation are displayed. The tester settings are not calibrated; the results increase linearly with the input. Amplitudes below 10 mV show errors inside the ±2% limits.

6.3.2 Measurements for 13.56 MHz

At last the measurements at 13.56 MHz are done. A clock provided by the J750 automated test environment is used to generate this input signal. This clock is filtered with a low-pass filter so isolate the fundamental frequency. The amplitude is not calibrated and the tester settings were taken as the reference.
The results scale linear with the input but the error is outside the limits as expected. This high error values are due to the sampling jitter of the ADC and are similar to what was seen with the signal generator.

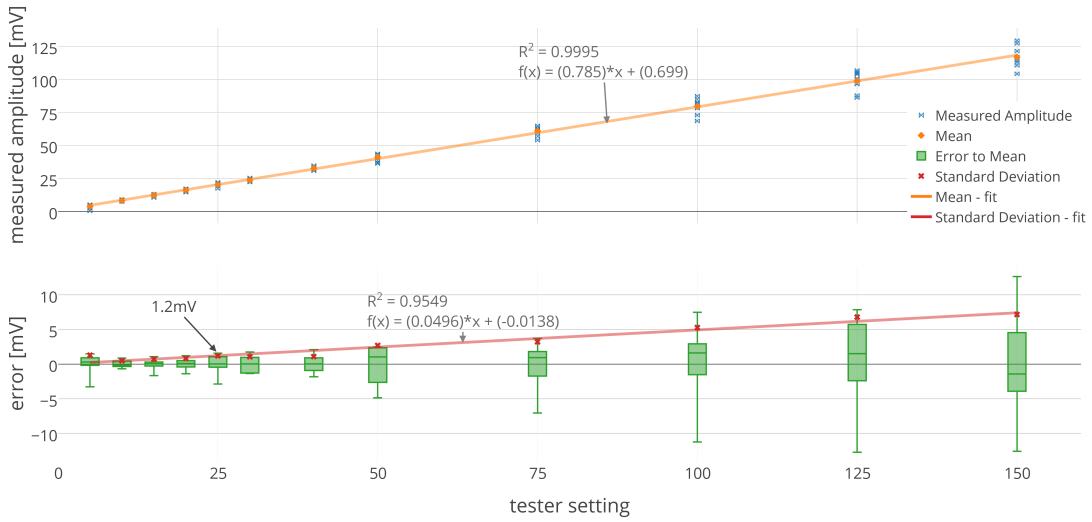

Figure 6.8: Measured data, mean value; error in regards to the mean value and the standard deviation are displayed. The error is outside of the limits of ±2%. This is due to the sampling jitter. The results are similar to the ones captured with the signal generator

6.4 Summary

Above measurements show, what the simulations already suggested. Undersampling is a viable strategy to measure the amplitude of a sine wave. The inaccuracy of the frequency is taken care of by, using frequency estimation as well as proper windowing of the input signal. The following table (6.1) shows a summary of the results of this chapter.

High percentage error at higher frequencies, independent of the amplitude is caused by high jitter on the sampling clock. Frequencies above 13.56 MHz provide results outside of the error limits. By improving the jitter on the sampling clock, the signal to noise ratio of the jitter noise is decreasing.

Frequency	Maximum Error @ 25mV	% Error @ 25mV	Lowest Amplitude within Limits
173 kHz	0.1 mV	0.4 %	5 mV
700 kHz	0.13 mV	0.5 %	5 mV
2 MHz	0.1 mV	0.4 %	10 mV
13.56 MHz	4.2 mV	16.8 %	-
J750 ATE			
173 kHz	0.6 mV	2.4 %	-
13.56 MHz	1.2 mV	4.8 %	-

Table 6.1: Summary of the measurement results with a signal generator and at the J750 ATE. The maximum error @25 mV is taking the maximum deviation form the mean value of 5 measurements. This value is then also represented in percentage. The lowest amplitude, which gives results within the error limits, is also stated if applicable.

7 Conclusion

This thesis shows the implementation of a precision sine wave measurement circuit. The approach described was evaluated in the lab as well as at the automated test environment where it is intended to be used. These are the results:

- **Undersampling**: Using an ADC with a sampling rate, that does not cover the signal bandwidth is feasible as long as only the amplitude is of importance. Frequency information can be derived by previous knowledge of the rough input frequency, and the exact sampling frequency.
- **Frequency estimation**: The frequency estimation algorithm is working in a real system as long as noise is not too high. The frequency bin at which the amplitude is calculated needs to be estimated, because neither the input frequency is know accurately nor the sampling frequency.
- **Implementation in fixed-point calculation**: The frequency estimation algorithm, as well as the Görtzel algorithm and associated windowing can be done with fixed-point calculation and 16 bit x 16 bit multiplication with a 32 bit result.
- **Low frequencies within error limits**: With a signal generator as well as on the J750 automated test environment, good results within the error limits are shown for low frequencies(up to 2 MHz).
- **Sampling Jitter**: High jitter of the internal clock and PLL of the microcontroller, which are used to produce the sampling clock for the ADC, prevent higher accuracy of frequencies up to 15 MHz
- **I2C communication**: I2C communication is set up on the microcontroller, but was not tested with the J750 ATE. The use of I2C leads to the easy scaling for use with multiple devices under test at once. Only

sending the results to the J750 will remove workload and increases test time.
- **Additional functionality**: The use of an ADC/microcontroller approach provides the possibility for future functionality.

This thesis starts with a simple, but not narrowly defined task to measure the amplitude of a given sine wave. At first, this sounds simple and quite a lot quick answers come to mind. This is when the first specifications show that even a seemingly simple assignment can have a lot of requirements that need to be fulfilled.
Form factor, power consumption, the provided voltage levels and the surroundings of the final circuit provide restrictions that need to be well defined and reduce the possible approaches. Even more influential is the definition of the range of possible input signals that may be provided to the measurement circuit.
A large bandwidth over almost 5 decades poses a challenge for non-adaptive solutions. In most cases a time constant, defined by a capacitance and a resistance of some kind is not easily chosen to support the full range of input signals from 400 Hz up to 15 MHz.

During all phases of this project, only a limited amount of time was available even though each of these chapters would have provided much more content to delve into. From the research on different solutions to PCB design, signal processing and finally the validation of the final circuit could all use much more work and it would be naive to say that the results provided in this thesis cover every aspect of all these topics in depth.
But what is shown is the development of a solution for the problem given, by starting with a broad look at different approaches, and providing a unique solution that was not documented in any of the found sources. A solution that provided not yet perfect results, but with a few tweaks can provide even better measurements than expected.

To extend the analog capabilities of the automated test environment at hand, the use of individual modules with I2C integration provides a system that can scale while removing load from the main system by only presenting the needed results instead of a data stream or requiring the sampling of an analog input signal. Distributed signal processing can also be used in

parallel further increasing speed of overall system.

To be used at the automated test environment, several improvements to the prototype board need to be made. This includes the removal of all components that are not needed in the end, like additional filter components, the 4th-order low-pass filter, the logamp backup solution as well as components and circuitry used detach or bypass single stages of the signal path.
After further investigation, it may be possible to remove the input buffer of the ADC by setting the common mode voltage of the overall input buffer to the level provided by the ADC.
Improving the sample clock will lead to good results at higher frequencies up to 15 MHz.

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