Highly Stable All CMOS Frequency Reference for SoC Wireless Sub-GHz Applications

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Submitted as thesis to attain the academic degree "Dr.techn." at the

Graz University of Technology

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Graz, July 2017

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Abstract

This thesis examines highly stable and fully integrated all CMOS frequency references based on LC oscillators (LCOs). Traditionally highly stable frequency references have been realised by means of quartz crystal oscillators. However, high requirements on size and cost have led to the development of silicon based frequency references which can be integrated in silicon. Different types of silicon based frequency references are available such as microelectromechanical systems (MEMS) based devices used for crystal replacement. Next to MEMS, also all CMOS frequency references are possible, e.g., RC oscillators (RCOs), LCOs. These devices are entirely realised in a standard CMOS technology, thus achieving the highest level of integration and the lowest possible size and cost. While RCO based all CMOS frequency references are widely used, they only have inferior frequency accuracy, compared to quartz crystals. However, newly emerged all CMOS frequency references based on LCOs can achieve much higher frequency accuracy, which is competitive to state-of-the-art MEMS oscillators and quartz crystals.

State-of-the-art all CMOS frequency references based on LCOs use frequency trimming for calibration and temperature compensation. However, trimming components such as varactors and switched capacitors exhibit either strongly non-linear or lossy behaviour and are consequently in this work considered to limit the achievable frequency accuracy. For that reason, a new concept for an all CMOS frequency reference has been developed in this work, which is based on a non-trimmable LCO. Instead of the analog frequency trimming, a fractional frequency divider is used to derive a variable frequency from the LCO. A calibration and compensation is performed via the fractional dividing ratio. The correct dividing ratio is determined by a compensation logic, using an integrated temperature and mechanical stress sensor as well as calibration data stored in an on-chip non-volatile memory (NVM). Shifting the calibration and compensation functionality from the analog to the digital side, this new concept is optimised for a high design robustness and frequency accuracy. Additionally, this concept inherently provides a field programmability of the required frequency due to the perfect linearity of the all-digital frequency generation.

In an all CMOS frequency reference, the calibration process is critical as the required calibration effort has to be as low as possible to be suitable for volume production. A simple calibration method for the process, voltage, and temperature (PVT) effects has thus been developed in this work, using only two temperature insertions. A high initial frequency accuracy of 52 ppm has been achieved with this calibration method, using devices from several different wavers. Next to PVT effects considered in previous work, in this thesis environmental effects due to electric and magnetic coupling as well as mechanical stress is taken into account. Theoretical considerations as well as measurements preformed in this thesis show, that after PVT and environmental induced frequency errors are compensated or minimised by suitable design measures, the highest portion of the remaining frequency errors can be attributed to mechanical stress. Mechanical stress compensation has thus been implemented in this work. Using the standardised stress analyses highly accelerated stress test (HAST) and high temperature operating life (HTOL),

similar to state-of-the-art LCO based all CMOS frequency references, an overall lifetime accuracy of 204 ppm has been estimated without the mechanical stress compensation. However, using the mechanical stress compensation, a significantly higher frequency accuracy of 136 ppm has been achieved.

Based on this new concept for an all CMOS frequency reference, a system on chip (SoC) transmitter has been developed within this work. It uses a phase-locked loop (PLL) to generate a variable frequency in the sub-GHz range. A custom-built differential current open drain power amplifier (PA) with Gaussian shaped current transitions is used to minimize harmonics. Next to diminishing injection pulling effects, which are critical for the employed concept, the reduced harmonics also simplify the required matching and filtering networks. An amplitude shift keying (ASK) and frequency shift keying (FSK) modulation can be performed via the PA as well as via the fractional dividing ratio, respectively.

Acknowledgments

This work has been carried out at the Institute of Microwave and Photonic Engineering at Graz University of Technology (Austria) in cooperation with the Cooperative Research and Exploration (CRE) department at Infineon Technologies Austria AG. The work was performed as part of the project "Kalium Home Monitoring" that has been funded by the Austrian Research Promotion Agency (FFG). During my thesis many people gave me support, whom I would like to thank in the following:

I sincerely appreciate the past years of supervision and promotion by my dissertation adviser Univ.-Prof. Dipl.-Ing. Dr.techn. Wolfgang Bösch, MBA. I would also like to thank my second examiner Prof. Dr.-Ing. Thomas Ußmüller.

Thanks to Dipl.-Ing. Gerald Holweg, head of the CRE department, for allowing me to be a part of his team. I would also like to thank him for creating the promoting and open-minded framework conditions.

Special thanks go to Dipl.-Ing. Dr.techn. Jasmin Grosinger, BSc. for collaboration on scientific publications, support, and guidance.

Thanks also to all my colleagues at the CRE department who enabled an inspiring and constructive working atmosphere. Many thanks go to the following colleagues which supported my work during the chip development: Johannes Schweighofer for digital design and general support, Michael Grassl for layout design, test, and measurements, and Sandra Wilfling for test and firmware development.

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Chapter 1

Introduction

Frequency references are required in many electronic devices serving as the ”heartbeat” of a circuit. Often, a highly stable frequency reference is deployed for applications requiring a high frequency accuracy [1]. A frequency reference can for instance be used as the clock signal of a digital system, a wireline communication, or a wireless communication. A high frequency accuracy is required for synchronous operation between different components of the digital system or between the transmitter and the receiver of the wireline communication. Also, for a wireless communication a high frequency accuracy is required for the carrier frequency signal on which the transmitted data signal is modulated.

Next to the requirements on the performance of a frequency reference, overall size and costs of an electronic system are important factors considered for the selection of the best suited frequency reference. This trend is in part driven by the development of miniaturized wireless sensor nodes required for the internet of things (IoT). A miniaturization and cost reduction can be achieved by the integration of all components of an electronic system on chip (SoC). Typically, in state-of-the-art SoCs an external quartz crystal frequency reference is often used as it cannot be integrated. This external quartz crystal limits the reduction in costs and size of electronic systems. As a consequence, lots of effort has been expended on replacing the quartz crystal with a silicon based frequency reference which can be integrated in silicon and is therefore smaller and cheaper [2].

Based on an integrated frequency reference a SoC wireless device can be developed that is highly miniaturized with a minimum number of external components and minimum costs required in many wireless sensor nodes for sense and control and IoT applications.

1.1 Highly Stable Frequency References

In many electronic systems a highly stable frequency reference is required. Depending on the respective requirements, several different performance characteristics must be considered for the choice of the best suited frequency reference. These characteristics comprise of the type of oscillator, quality factor (Q), operating frequency, frequency accuracy, phase noise,

jitter, costs, geometric factors like size and shape, operating temperature range, and power consumption. The most important characteristics are discussed in more detail in the following:

A frequency reference is generated by means of an oscillator which oscillates at a certain frequency, i.e., the operating frequency of the frequency reference can be a multiple of the oscillator frequency. The frequency of a frequency reference compared to the oscillator operating frequency from which it is derived can be equal, higher, e.g., using a phase-locked loop (PLL) [3], [4], or lower, e.g., using a frequency divider [5], [6].

Oscillators can be classified in different ways, based on their principal of implementation. According to [7], [8], oscillators can be classified based on their output signal shape into sinusoidal (harmonic) or non-sinusoidal oscillators. A sinusoidal oscillators produces a waveform which is very close to or exactly sinusoidal. A non-sinusoidal oscillator produces a square or a sawtooth waveform, e.g., a relaxation oscillator.

Oscillators can further be classified as negative resistance or feedback oscillators [8]. Negative resistance oscillators use an active device with a negative slope of its current-voltage characteristic. In CMOS oscillators a negative resistance is typically generated by means of a CMOS transistor and therefore characterised as a negative transconductance ($-g_{\mathrm{m}}$). Feedback oscillators are arranged as a loop with a positive feedback generated by an amplifier.

In [9], oscillators are classified in continuous-time and discrete-time, with discrete-time referring to oscillators which have a discrete number of states, e.g., a relaxation oscillator, or are implemented digital. Furthermore, in [9], continuous-time oscillators are separated into resonator based and non-resonator based types equivalent to negative resistance and feedback oscillators. Resonator based oscillators exhibit two types of reactive elements inductor (L) and capacitor (C), allowing to create a resonator in which energy can be stored over several oscillation periods. An equivalent behaviour could also be obtained with a mechanical resonator. Non-resonator based oscillators include only one type of reactive element with either a L or a C. A feedback as well as an additional resistor (R) is required for a non-resonator based oscillator.

A resonator based oscillator can be rated by means of its Q. As described in [9], a general characterisation of the Q for a resonator can be written as:

$$Q = 2\Pi \frac{\text{Total energy stored in the resonator}}{\text{Energy lost per cycle from the resonator}}. \tag{1.1.1}$$

The Q is defined as being proportional to the ratio between the energy stored in the resonator and the energy lost during one cycle. For an LC resonance circuit, also known as LC tank, the Q can easily be calculated using the values of the passive components L and C as well the losses represented as either a series resistor ($\mathrm{R_S}$) or a parallel resistor ($\mathrm{R_P}$). The Q for an LC oscillator (LCO) in a series and a parallel resonant circuit is defined by [9]

$$Q = \frac{1}{R_{\mathrm{S}}}\sqrt{\frac{L}{C}}, \quad Q = R_{\mathrm{P}}\sqrt{\frac{C}{L}}. \tag{1.1.2}$$

In oscillators, a high Q of the resonator is advantageous for noise minimisation. Typical values for the Q of a resonator based oscillator can range from low values of about 10-20 [10] for integrated LC tanks up to 10^6 for quartz crystals [11].

An important characteristic of a frequency reference is the operating frequency of its oscillator. According to [12], the frequency (f) is defined as the number of periods (ΔN) per time interval (Δt) or as the reciprocal value of the period time (T_P):

$$f = \frac{\Delta N}{\Delta t}, \quad f = \frac{1}{T_P}. \tag{1.1.3}$$

The frequency can also be stated as the angular frequency (ω) with the relation to f defined by [12]

$$\omega = 2\Pi f. \tag{1.1.4}$$

For a resonator based oscillator, the frequency is given as the resonance frequency (f_{res}). In an LC tank, the f_{res} depends on L and C according to [7]:

$$f_{\mathrm{res}} = \frac{1}{2\Pi\sqrt{LC}}, \quad \omega_{\mathrm{res}} = \frac{1}{\sqrt{LC}}. \tag{1.1.5}$$

In a mechanical resonator, the resonance frequency is given by the mechanical properties, e.g., the resonance frequency of a quartz crystal is given by the shape and thickness of the cut [8].

A very important performance criterion is the frequency accuracy which represents the maximum deviation of the ideal frequency, in this work also referred to as frequency error. The accuracy of a frequency reference is often defined as the relative deviation of the ideal specified frequency given in % or part per million (ppm). The corresponding relation is defined by [2]

$$f_{error}(\%) = \frac{\Delta f}{f_0}\cdot 10^2, \quad f_{error}(ppm) = \frac{\Delta f}{f_0}\cdot 10^6. \tag{1.1.6}$$

The frequency accuracy thereby refers to the mean long time frequency value neglecting short time variations. Depending on the application, different levels of accuracy are required ranging from ones of % down to sub-ppm accuracy. In order to meet the requirements for a specific

application, a frequency reference must not exceed the maximum tolerable deviation of the ideal frequency.

Next to the mean long time frequency error, also short time variations can occur in a frequency reference. These variations lead to two important performance characteristics referred to as phase noise ($\mathcal{L}$) and jitter (J). The phase noise is defined as the power spectral density (PSD) of the frequency signal over a 1 Hz bandwidth in relation to the overall signal power [9]. It is typically represented as the single side band phase noise at offset frequency f_o ($\mathcal{L}(f_\mathrm{o})$) in the unit dBc/Hz (dB carrier/Hz). In the time domain, short time variations of the frequency can also be represented as a time error referred to as jitter, i.e., the zero-crossing time of the wave signal deviates from the ideal moment in a stochastic manner [9]. Different definitions of jitter are well-established. The period jitter (J_P) defines the root mean square (RMS) period time deviation of the average period time. Aside from period jitter, integrated jitter is specified as a requirement for the frequency reference in many applications. As phase noise and jitter are related to each other, the contribution of phase noise to the jitter can be determined from the phase noise spectrum. Integrated jitter represents jitter, referable to a certain offset frequency range of the phase noise spectrum.

Depending on the performance requirements, different types of frequency references can be used. Traditionally, vacuum tube oscillators have been used as frequency references [13]. Later, the vacuum tube oscillator has been replaced by the quartz crystal oscillator, representing a highly stable frequency reference. Driven by costs, several types of silicon based frequency references have been developed, which provide a high frequency accuracy and are thus suitable for quartz crystal replacement. These frequency references include architectures based on microelectromechanical systems (MEMS) resonators (MEMS based frequency references) and on circuits entirely realised in a standard complementary metal-oxide semiconductor (CMOS) process (all CMOS frequency references) [2].

1.1.1 Quartz Crystal

A quartz crystal is an electromechanical device exploiting piezoelectricity and mechanical resonance as its principle of operation. It can be excited to an oscillation at the resonance frequency given by the geometry [14]. Also operation at harmonics of this resonance frequency is possible which is applied for overtone quartz crystals [15]. To maintain the resonance frequency given by the mechanical resonator, the quartz crystal needs to be housed in a hermetically sealed enclosure. In an open package the crystal resonator would otherwise be effected by mass loading from moisture and other contamination, leading to frequency drifts [16], [17]. The coupling of the mechanical resonator to an electric circuit is accomplished by means of the piezoelectric effect [14], [18]. Considering the high Q ranging from 10^4 to 10^6 [19], [11] a quartz crystal is a very stable frequency reference. For decades a quartz crystal was the only way to economically provide a highly stable frequency reference [1]. Still quartz crystals provide the highest performance for different characteristics relevant for a frequency reference.

Quartz crystals can have an inherently low temperature dependency depending on the cut angle and mode of operation [20]. Therefore quartz crystals can come as non-compensated crystal oscillators (XOs) with accuracy levels ranging from 20-100 ppm. Depending on the requirements also temperature compensated crystal oscillators (TCXOs) exist, providing even sup-ppm accuracy levels [1]. Due to the high Q quartz crystals can provide a high phase noise and jitter performance as well as low power operation [21], [22]. Despite the high performance quartz crystals come at reasonably low costs due to economy of scale. Therefore the quartz crystal is the state-of-the-art frequency reference prevalent in the frequency reference market [1].

In a typical architecture of an electronic system an integrated circuit (IC) is mounted on a printed circuit board (PCB). In order to provide this IC with a frequency reference a quartz crystal is mounted on the same PCB combined with two load capacitors. The usage of a quartz crystal consequently leads to additional required space on the PCB, additional passive components, as well as two additional dedicated pins from the IC. Figure 1.1 shows the typical arrangement of a quartz crystal in such a system on a PCB.

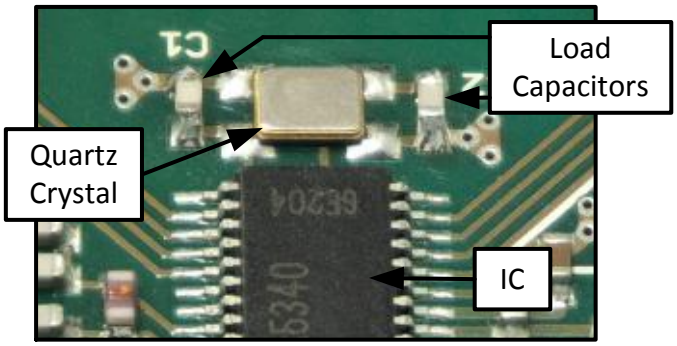

Figure 1.1: Infineons state-of-the-art wireless transceiver TDA5340 [23] mounted on a PCB including the quartz crystal and the two related load capacitors.

Over the last decades CMOS technology has scaled according to moor's law [24]. Transistors become smaller in newer CMOS processes and also the costs per transistor are reduced. This trend has a considerable influence on ICs with mostly digital functionality as the number of integrated transistors on a chip can be increased or the size of a chip can be reduced. Also analog and mixed signal ICs are affected by this trend leading to the need of miniaturization and cost reduction in modern SoCs [25], [26]. Therefore all the required analog and digital functionality must be integrated on a single chip with a minimum number of external components. Although the quartz crystal has also historically scaled in size it cannot hold path with the high requirements caused by CMOS scaling [1]. Physical limitations make further scaling difficult and the end of scaling is imminent [27]. Also a quartz crystal cannot be integrated in a CMOS process [1]. The high sensitivity to mechanical shock and vibration is another disadvantage of

a quartz crystal. Nevertheless quartz crystals have proven to meet customer requirements in performance and price and are therefore the state-of-the-art frequency reference [1]. In order to replace the quartz crystal with a silicon based (MEMS or all CMOS) frequency reference, the new technology not only has to come with the advantage of costs and miniaturization but also have to gain the customers acceptance.

1.1.2 Silicon Based Frequency References

The trend of scaling in size and the need for a high level of integration has caused the need for integrated frequency references [2], [27]. Lots of effort has therefore focused on the development of a silicon based frequency reference over the last decades. Such a silicon based frequency reference is realised in silicon and therefore can be integrated [1]. Silicon based frequency references can be further distinguished in silicon MEMS- and all CMOS frequency references [5], [2]. A silicon MEMS based frequency reference uses a mechanical micro resonator implemented in silicon which is used to derive an accurate frequency reference [28]. An all CMOS solution refers to a frequency reference which can entirely be integrated in a CMOS circuit using only devices which are inherently available in a CMOS process [5]. In order to compete with a quartz crystal a silicon based frequency reference needs to provide a high performance [1]. The major difficulty in such an integrated frequency reference is the high sensitivity to variations in process, voltage, and temperature (PVT) [2]. Additionally, ageing and environmental influences like moisture and mechanical stress must be taken into account.

MEMS based Frequency References

One possible approach for a silicon based integrated frequency reference is the exploitation of silicon MEMS. The development towards silicon MEMS based oscillators started in 1967 with the resonant gate transistor [29]. Since then lots of research has led to the development of integrated micro-mechanical resonators for replacement of quartz crystals [30], [27]. Nowadays a MEMS oscillator typically is based on a mechanical structure in silicon which forms a mechanical resonator and can be excited at its resonance frequency [28]. The coupling between a mechanical vibration and an electrical signal can be based on piezoelectricity [31] like in quartz crystals, but also electrostatic [30] and piezo-resistive effects [32] can be exploited. To create an oscillator the MEMS resonator must be combined with a CMOS circuit which constantly feeds power into the resonator and hence excites and sustains an oscillation. As a consequence MEMS oscillators mostly are implemented as a two-chip solution including the MEMS resonator die and an additional chip for the required CMOS circuit [28], [32]. In silicon MEMS resonators similar to quartz crystals a high Q is possible. However, since any surrounding air would dampen an oscillation and hence degrade the Q such resonators require a hermetic packaging which often is realised by means of a silicon cavity [28], [32].

Another difficulty of silicon MEMS resonators is the high temperature dependency of the Elasticity modulus [33] for silicon leading to a typical temperature coefficient of about -31 ppm/K for the resonance frequency [34]. A temperature compensation via the combination of materials with different temperature coefficients has therefore been developed [34], [35] and is used in some, but not all silicon MEMS based frequency references. Also manufacturing variations of the geometry leads to variations of the resonance frequency. As a consequence calibration and temperature compensation is required for MEMS based frequency references. Therefore most MEMS based frequency references use a fractional frequency synthesizer and an integrated temperature sensor as well as a digital polynomial temperature compensation to correct the temperature dependency and variations of the MEMS oscillator [28], [32]. The calibration data are stored in an non-volatile memory (NVM) which is also implemented on the CMOS chip. This approach enables a field programmability of such devices as a fractional frequency synthesizer can easily provide a wide range of output frequencies derived from the MEMS oscillator reference [28], [32]. Also, a very low drift of the resonance frequency has been demonstrated over the lifetime of MEMS oscillators, enabling high levels of frequency accuracy [36]. The frequency accuracy which can be achieved with such frequency references ranges from 100 ppm down to even sub-ppm levels [37]. Also low phase noise and sub-ps jitter performance is possible allowing MEMS based frequency references to compete in performance with their quartz crystal counter parts [3]. Next to the low costs of MEMS based frequency references also the lower sensitivity to mechanical shock and vibration is a considerable advantage over quartz crystals.

All CMOS Frequency References

An all CMOS frequency reference refers to a frequency reference which is entirely implemented in a CMOS process using only the components which are inherently available in this CMOS process [2], [5]. As a result, these type of frequency references can be implemented on a single silicon die which therefore leads to the smallest possible size and the highest possible level of integration [38]. Standard CMOS processes and packaging techniques can be applied enabling low cost and high reliability [2], [5]. The major difficulty of these type of frequency references is to overcome the high variations of the available CMOS devices depending on process, temperature, voltage, and ageing. Also environmental influences like moisture and mechanical stress must be considered [39], [38]. Furthermore the strongly non-linear behaviour of certain CMOS components makes the design of precision circuits difficult. Therefore a robust approach must be chosen which allows to achieve a high frequency accuracy despite the aforementioned difficulties.

A non-linear behaviour of the frequency determining components leads to a high influence of the absolute values of voltages and currents in a frequency reference. In contrast, if the frequency determining components are perfectly linear, absolute values are cancelled out and have no effect on the frequency. Generally in a CMOS process there are only the three passive

components R, L, and C available to provide a high linearity. Combinations of these three components are the most suitable means to create an accurate frequency in a CMOS circuit [2]. Implementations of RC oscillators (RCOs) as well as LCOs are therefore commonly known as all CMOS frequency references providing a high level of accuracy. A combination of R and L to derive a frequency would theoretically also be possible but is not done in integrated circuits for practical reasons. A combination of R and L would have similar properties than a combination of R and C with the disadvantage of the high chip area occupation of L. Lots of other implementations for CMOS oscillators not relying on the passive components R, L, and C are possible, but are not considered in this work as they typically are not suitable for a high frequency accuracy. An exception to this are recently developed electro-thermal frequency references which can provide a high level of accuracy [40]. In this type of frequency reference the well defined propagation of heat on a silicon chip is used to derive an accurate frequency. In this work the major focus lies on LCOs as they are the most accurate all CMOS frequency references currently known. For comparison RCOs as well as electro-thermal frequency references are considered briefly.

RC Oscillator

The RCO uses a time constant which is derived by the passive components R and C to generate a frequency reference. Several topologies are known for such RCOs. Common topologies include harmonic, ring, and relaxation RCOs [2].

Harmonic RCOs are based on linear amplifiers with a frequency selective RC feedback network [2], [41]. They therefore typically operate with sinusoidal (harmonic) signals. One common implementation of a harmonic RCO is the Wien-bridge oscillator [41], [42].

The RC-ring oscillator is a topology which uses a number of consecutive delay stages with feedback [43]. Similar to the ring oscillator realised with CMOS inverter stages each delay stage consists of an amplifying inverter stage [44]. When single ended inverting delay stages are employed an odd number of stages is required for oscillation. Also an even number is possible for a fully differential implementation of the delay stages. For the RC-ring oscillator an additional RC-delay stage is added to every delay stage acting as a phase shifter. As the time constant of that RC-delay is typically much greater than the delay of the inverting stage alone the overall delay of a stage is mostly given by R and C. Consequently such an RC-ring oscillator exhibits a much lower sensitivity to temperature and supply voltage in comparison to the ring oscillator. The period time of the oscillation is given by the delay time of one stage multiplied by the number of stages.

Another common approach is the RC relaxation oscillator [45]. This type of RCO uses the time required to charge a capacitor to derive a frequency reference. An oscillation can be achieved by having two threshold voltages and cyclically charge and discharge the capacitor between these thresholds [46], [47], [48]. Alternatively also an implementation with only one threshold voltage

can be realised. Therefore the capacitor is charged until the voltage exceeds the threshold and is then discharged in a very short time by means of a switch [45], [49]. In typical implementations these oscillators use a current source for charging and discharging the capacitor rather than a resistor. Nevertheless, as this current is typically derived by means of a resistor in the bias current circuitry such an oscillator is considered an RCO [2], [49].

The major challenge in RCOs is to overcome the large variations of integrated resistors and capacitors. A calibration is therefore required and can be implemented by means of a variable resistor or capacitor [46]. Also temperature effects must be considered via a careful design in order to get a high frequency accuracy over the required temperature range. Overall the frequency accuracy which can be achieved with RCOs is in the range of less than 1 % [50], [51]. In [4] an RCO with an exceptional accuracy of even ±85 ppm was demonstrated using an on-chip heater for calibration versus temperature. The major advantage of RCOs is the low occupied chip area as well as the low power consumption. A power consumption of only 120 nW was realised in [49] using a standard CMOS process. RCOs are therefore suitable for low power applications with relaxed requirements for frequency accuracy.

LC Oscillator

An LCO uses the passive components L and C to derive a frequency by means of electrical resonance. LCOs have been used as frequency references for over a century starting with vacuum tube oscillators in 1906 to be the first economical means to generate a continuous electrical oscillation [13], [42]. They are nowadays a well known type of oscillators in CMOS technology often used as voltage controlled oscillator (VCO)s in PLLs due to their superior phase noise performance in comparison to other oscillators available in CMOS technology [52], [53], [54]. However the operation of LCOs in a free running configuration is a very new approach for an integrated frequency reference that has emerged over the last years [55], [5]. Integrated LCO frequency references therefore use the standard devices L and C available in every CMOS technology. To achieve a high performance the operating frequency is typically chosen in the GHz range as integrated inductors cannot provide a sufficiently high Q at lower frequencies. Consequently also the power consumption of such oscillators is typically high lying in the range of 3.6-25.2 mW [5]. In LCOs, accuracy levels in the range of hundreds of ppm can be achieved which currently is the highest possible accuracy for an all CMOS frequency reference. Also, LCOs exhibit by far the best performance in terms of jitter and phase noise among the all CMOS frequency references [5]. LCOs have been commercialized for quartz crystal replacement in different applications including sub-GHz wireless [56], [57], [58]. As LCOs potentially can offer the highest performance of all frequency references available in CMOS technology they are considered the major focus of this work.

Electro-thermal Frequency References

As mentioned above, another class of frequency references realised as an all CMOS solution are electro-thermal frequency references. This type of frequency reference uses the thermal diffusivity as another physical property available in a standard CMOS process instead of relying on the passive components R, L, and C [40], [59]. The propagation of heat on a silicon chip over a geometric distance thereby corresponds to a time delay. Such an electro-thermal time delay is typically implemented via a heater and a temperature sensor placed in a defined distance. The time delay is given by the geometric distance and the thermal diffusivity of the silicon substrate. The thermal diffusivity of silicon is a material specific property [60]. It depends on the temperature and therefore makes temperature compensation mandatory for these devices. As the geometry is given by the lithographic manufacturing and the thermal diffusivity is a very well defined and reproducible property a very high accuracy can be achieved in a modern CMOS process. An accuracy of 0.2 % was reported in [40] even without any calibration. For devices calibrated with a single insertion at room temperature a frequency accuracy of 0.1 % was achieved. The power consumption of such electro-thermal frequency references is in the range of 2 mW [59] and therefore higher than for RCOs but slightly lower than for LCOs. Although electro-thermal frequency references can achieve a higher performance than RCOs they are confined only to research yet. Further improvements in performance particularly regarding the frequency accuracy are expected with technology scaling [59].

1.2 Scope of Work

In this theses the major goal is to develop a highly integrated frequency reference. As the work is focused on achieving a high level of integration an all CMOS solution is desired. This frequency reference should further be suitable for wireless data transmission. Therefore, the frequency accuracy as well as the phase noise are considered to be the key performance characteristics. In order to enable a wide-ranging applicability, a high frequency accuracy of 100 ppm as well as a phase noise, comparable to stat-of-the-art wireless sub-GHz transmitters are considered the basic requirements in this work. Previous work on highly stable all CMOS frequency references demonstrates LCOs to be the most promising devices compared to other all CMOS solutions. For that reason, this work is focused on an LCO based all CMOS frequency reference.

Furthermore, based on this all CMOS frequency reference, a device is developed which provides a wireless transmitter functionality. This wireless transmitter is designed for an operation in the sub-GHz frequency range. The device is realised on a single silicon die comprising of all the functionality required for a wireless transmitter. Therefore a SoC transmitter is implemented including the analog and radio frequency (RF) functionality to generate an accurate frequency reference as well as a modulated RF signal for wireless data transmission. Also, a digital core and a NVM is included for the storage of an application specific firmware as well as the

calibration data. Finally, this devise provides a wireless transmitter functionality with the highest possible level of integration, a low number of required external devices and hence lowest possible costs.

1.3 Related Work

The first research work presenting a fully integrated frequency reference based on an LCO was published in 2005 [61]. Meanwhile an abundance of research work has been published and also commercialized frequency references are available. They have been typically exploited as crystal replacement assembled in pin-compatible standard plastic packages [56], [5], [57]. Next to dedicated oscillator devices, also more complex systems have been commercialized based on this technology. Therefore an intellectual property (IP) macro [55] as well as a single silicon die frequency source [38] have been introduced for use in universal serial bus (USB) controllers and USB sticks [5]. Moreover a SoC wireless transmitter has been commercialised using an LCO as its frequency reference [58]. For these LCOs mentioned above there are several different system architectures which are briefly introduced and compared in the following.

1.3.1 System Architectures

The system architecture of state-of-the-art LCO based CMOS frequency references can be distinguished by means of their approach for temperature compensation. So far three different architectures are known referred to as passive and active temperature compensation [2] as well as the temperature-null approach [62]. Next to this known techniques also a combination is possible to profit from the respective advantages. In [5], a combination of passive and active temperature compensation has been described.

Passive Temperature Compensation

As illustrated in Sec. 2.2.1, in integrated LCO frequency references the temperature behaviour is dominated by the temperature dependency of the series resistor of the inductor leading to a negative temperature coefficient. In the same way a loss referable to a series resistor of the capacitor would lead to a positive temperature coefficient of the LCO frequency. For the passive temperature compensation a lossy component is thus deliberately introduced into the LC tank on the capacitor side to compensate the frequency drift caused by the lossy components of the inductor [38]. Figure 1.2 depicts a simplified realisation of an LCO frequency reference using a passive temperature compensation according to [38]. To achieve a calibration versus temperature, the frequency as well as the residual temperature coefficient must be adjustable. This is realised by means of a bank of switched trimming capacitors C_{TR}[X:0] (X+1 number of elements) as well as resistively degraded capacitors C_{TC}[Y:0], R_{TC}[Y:0] (Y+1 number of elements). The

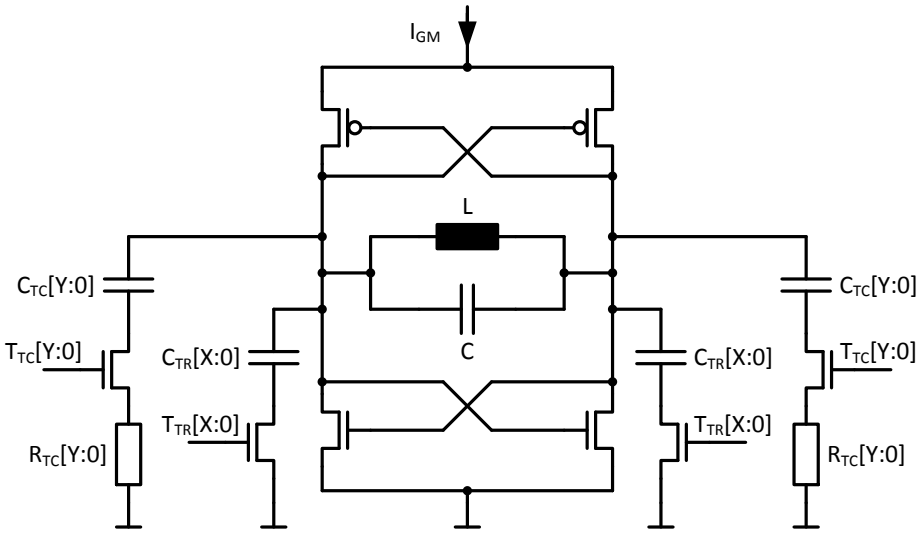

Figure 1.2: LCO frequency reference using passive temperature compensation as described in [38]. An array of capacitors C_{TR}[X:0] for frequency trimming and an array of resistively degraded capacitors C_{TC}[Y:0], R_{TC}[Y:0] for temperature compensation is implemented.

trimming capacitors C_{TR}[X:0] are used to compensate process variations and to adjust the frequency to the desired value. The resistively degraded capacitors C_{TC}[Y:0], R_{TC}[Y:0] are used to introduce loss in the LC tank on the capacitor site and thus to compensate the temperature characteristic of the LCO. As a result, a small frequency range of a few percent as well as a temperature compensation can be achieved for the free running LCO. A higher output frequency range can be covered by dividing the LCO frequency with a variable integer frequency divider. For the calibration process described in [38], first, the best suited dividing ratio is selected. Then, both, the programmable switches for the frequency trimming T_{TR}[X:0] and for the temperature compensation T_{TC}[Y:0] are adjusted using two temperature insertions, respectively. The advantage of this approach is the simple and power efficient system implementation. Only little digital functionality is necessary for configuration and also no additional temperature sensor is required. On the downside this passive temperature compensation can only be applied for the first-order temperature coefficient. A high initial frequency error caused by higher order effects of the LCO temperature characteristic remains. Also deliberately introduced losses unfavourably degrade the overall Q of the LC tank.

Active Temperature Compensation

Another possible architecture for LCO based CMOS frequency references is active temperature compensation. In such an architecture the LCO is arranged as a VCO using varactors for frequency tuning [10], [55], [63], [56]. The tuning range is kept to a rather small range, e.g.,

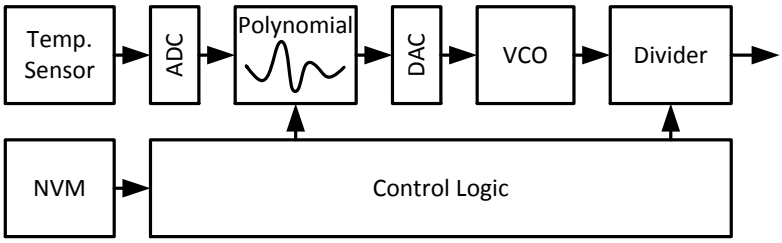

Figure 1.3: LCO frequency reference using active temperature compensation according to [10].

3 %. Figure 1.3 depicts a simplified realisation of an LCO frequency reference using active temperature compensation according to [10]. The device includes a temperature sensor as well as an analog to digital converter (ADC) to convert the measured temperature into a digital value. In order to compensate the temperature characteristic of the LCO, a digital polynomial is used, which adjusts the LCO frequency by means of an analog control voltage generated by a digital to analog converter (DAC). To extend the output frequency range also a variable integer divider is used. All the required configurations including the polynomial coefficients as well as the dividing ratio are stored in an on-chip NVM. For calibration, a suitable dividing ratio is selected. The digital value for the control voltage is adjusted to obtain the correct output frequency for several temperature points. A polynomial function is then fitted through this points to generate a constant frequency versus temperature. Also, a process sensor can be used to gather more information of the temperature characteristic or to reduce the number of necessary calibration points. The major advantage of this architecture is that due to the complex compensation logic a high initial frequency accuracy can be achieved [56]. Unfortunately, this leads to a high system complexity and to some extent also to a high power consumption. Also, a very accurate control voltage is needed for the varactors to cover a trimming range of a few percent while offering a frequency accuracy of tens of ppm. Besides, varactors degrade the LC tank in terms of linearity and Q, presumably leading to a higher frequency drift over lifetime.

Temperature Null Compensation

Another known architecture for temperature compensation in LCO frequency references is a phase shift technique referred to as temperature null [64] ,[62], [65]. In this architecture a variable shift of the sustaining amplifier's phase is used to perform the temperature compensation. Figure 1.4 depicts a simplified realisation of an LCO frequency reference using the temperature null approach according to [62]. This architecture uses a programmable phase shifter to adjust the phase of the sustaining amplifier. The phase of the sustaining amplifier affects the temperature characteristic of the LCO. For the correct phase, the temperature coefficient of the LCO equals zero. To obtain a variable output frequency, additional switched capacitors for tuning and an integer frequency divider is implemented. The calibration process described in [62]

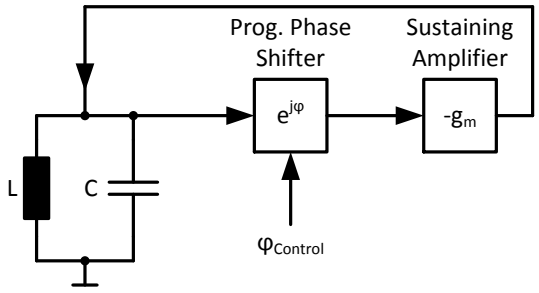

Figure 1.4: LCO frequency reference using the temperature null architecture according to [62]. The phase of the sustaining amplifier can be adjusted by means of a control word $\varphi_{\mathrm{Control}}$ to compensate for the temperature.

can be performed by a single point room temperature only calibration. Therefore, the output frequency is adjusted via the dividing ratio and the capacitive frequency trimming. The correct phase is adjusted for temperature null by modulating the temperature with an on-chip heating structure. Similarly to passive temperature compensation, the temperature null approach is simple and power efficient. It also comes with the drawback of a high initial frequency error versus temperature due to remaining higher order effects of the LCO temperature characteristic. An improved version of the temperature null approach is presented in [65] where the phase is additionally corrected versus temperature by means of an on-chip temperature sensor for a higher initial frequency accuracy.

1.3.2 Performance Comparison

Table 1.1 summarizes the most important parameters for all currently known LCO based frequency references. First published results came up as early as 2005 with research now continuing for over one decade. The devices are compared in terms of their architecture and technology feature size. It is also distinguished between devices published as research work and those which where commercialized with a datasheet available. The frequency range available for this devices ranges up to a couple of hundreds of MHz with the devices typically also covering a wide frequency range. Most of the compared devices achieve a very low period jitter in the range of single digit ps. The power consumption varies in the range of up to 20 mA with active temperature compensated devices dissipating slightly more power than passive compensated ones. Presumably, the most important parameter, the frequency accuracy is stated as initial accuracy referring to the accuracy versus temperature after the initial calibration, as well as an overall accuracy which refers to the value specified in the datasheet including all frequency drifts over the device lifetime. For research projects, typically the initial accuracy is given, while for commercialized devices only the overall frequency accuracy is available from the respective datasheet. As LCO frequency references are sensitive to ageing induced frequency drifts, the device ageing conditions over lifetime are also stated in the datasheet for the specified

frequency accuracy. From Table 1.1 it can be observed that devices designed in a smaller technology tend to achieve a better frequency accuracy. It can also be seen in Table 1.1, that LCO based frequency references are mostly deployed for a narrow temperature range of 0 - 70 °C .

Table 1.1: Comparison of state-of-the-art LCO based frequency references

Device / Ref	[61]	[55]	[63]	[66]	SI500 [56]	[38]	IDT3CN [57]	IDT3LV04 [5]	SWS3100 [67]
Year	2005	2007	2008	2008	2008	2010	2011	2011	2015
Architecture	active	active	active	active	active	passive	passive	passive+active	temp. null
Technology (nm)	180	350	250	250	130	130	130	130	180
Research / commercialized	R	C	R	R	C	C	C	C	C
Frequency (MHz)	528/66/50	12	25	0.5 - 480	0.9 - 200	6 - 133	4 - 133	-	1 - 133
Period jitter (ps)	7.4/21/33	6.78	2.75	6.5	1.5	-	5	-	3
Current consumption	5.1 mA @ 1.8 V	9.5 mA @ 3.3 V	18 mA @ 3.3 V	15 mA @ 3.3 V	9.7 mA @ 3.3 V	2 mA @ 3.3 V	1.9 mA @ 1.8 V	- -	7.6 mA @ 3.3 V
Initial accuracy	1 %	100 ppm	152 ppm	90 ppm	-	80 ppm	75 ppm	25 ppm	-
Overall accuracy	-	400 ppm	-	-	250 ppm	300 ppm	100 ppm	50 ppm	50 ppm
Ageing condition	-	-	-	-	10 years @ 85 °C	-	5 years @ 25 °C	-	1 year @ 25 °C
Temperature (°C)	0 - 70	-10 - 85	-10 - 80	0 - 70	0 - 85	0 - 70	0 - 70	0 - 70	0 - 70

1.3.3 Mechanical Stress Compensation

Previous research on highly stable all CMOS frequency references has mostly been focused on PVT compensation [2], [56], [57]. PVT effects can be compensated via the initial calibration. Consequently, as mentioned above, by means of several temperature insertions, the process and temperature induced frequency variations can be considered. The influence of the supply voltage can be minimised by means of an integrated low-dropout (regulator) (LDO) providing a constant internal supply voltage to the voltage sensitive LCO core circuit. However, even tough being mandatory for an all CMOS frequency reference, with PVT compensation alone only an inferior frequency accuracy can be achieved compared to quartz crystals. State-of-the-art LCO based all CMOS frequency references offer frequency accuracy levels in the range of 150-300 ppm. As many applications require a total frequency accuracy better than 100 ppm the levels achieved in state-of-the-art LCO based all CMOS frequency references are the major limiting factor for high volume markets.

Next to PVT effects which can be condensed as the frequency errors remaining after the initial calibration, ageing of the CMOS circuit, as well as electric interactions with moisture in the package can lead to frequency errors. Furthermore, mechanical stress has been mentioned to be responsible for frequency errors in LCO based all CMOS frequency references [38]. However, little attention has been paid to the order of magnitude and the exact underlying mechanism of mechanical stress induced frequency errors.

Mechanical stress is caused by the package as well as by different thermal expansion coefficients from the silicon die, the lead frame and the plastic mold compound [68], [69]. All these effects are irrelevant for a post-assembly calibration. However, the mechanical stress can also change over lifetime in a plastic package due to hygroscopic swelling, cure shrink, and soldering [70], [71]. In [38], effects referable to moisture have been found to be the major ageing mechanisms using a highly accelerated stress test (HAST), despite the Faraday-shield which prevents a direct electric interaction of the moisture with the LCO.

Figure 1.3 depicts the stress notation for a silicon die, with the x- and y-axes defined as being parallel to the chip edges. A typical silicon die exhibits specific geometric characteristics with the measures in x- and y-direction being much greater than the thickness (z-direction). Furthermore, packaged ICs are typically arranged in a laminar structure. As a result, mostly the in-plane stress components σ_{xx}, σ_{yy} occur and influence the behaviour of the CMOS circuit. Stress components other than σ_{xx}, σ_{yy} are less distinctive and occur mostly at the perimeter and at the corners of the silicon die [68], [72], [71].

Mechanical stress compensation has already been successfully applied for precision bandgaps and precision Hall effect based current sensors [71]. In [71], an on-chip stress sensor based on two types of n-well resistors with different piezo-coefficients is used for compensation. It has been found that mostly in-plane stress occurs and is relevant for the stress compensation. By designing all circuits with an L-shaped layout, an equal sensitivity to x and y in-plane stress σ_{xx}, σ_{yy} has been achieved, leading to the consideration of the relevant stress as a scalar

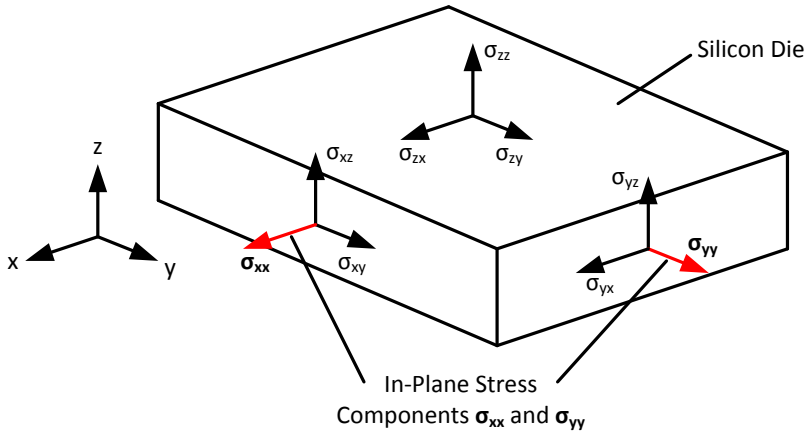

Figure 1.5: Stress notation for a silicon die: The specific geometric characteristics (z < x,y) as well as the laminar structure of typical packaged ICs makes in-plane stress (σ_{xx}, σ_{yy}) the relevant stress component influencing CMOS circuits.

$\sigma = \sigma_{xx} + \sigma_{yy}$. A stress sensor using L-shaped stress resistors has thus been implemented for stress compensation, significantly reducing stress induced errors.

The same approach is applied in this work to reduce stress induced frequency errors in an all CMOS frequency reference, potentially enabling a frequency accuracy better than 100 ppm.

1.4 Main Contributions

Previous work has demonstrated that LCO based all CMOS frequency references provide a high frequency accuracy in the range of 50 - 250 ppm and low phase noise. The major requirements for a sub-GHz wireless application can thus be fulfilled. However, several difficulties must be resolved in order to develop a wireless device, based on this technology.

As shown in Table 1.1, the frequency accuracy of the compared devices is stated over a narrow temperature range of only 0 - 70 °C or as the initial value after the calibration. However, for an LCO based all CMOS frequency reference, additional frequency errors over lifetime must be expected caused by different ageing effects. For an accurate estimation, suitable standard reliability tests must be performed in order to estimate the frequency accuracy which can be achieved under the conditions anticipated over the lifetime for such a device. For the commercialized devices presented in Table 1.1, this has been done. However, the lifetime conditions for the claimed frequency accuracy are stated in a lax way, only considering room temperature storage conditions.

The Silicon Labs SI500 [56] as well as the device presented in [38] are an exception to this. With harsh lifetime conditions stated for the SI500 [56] as well as suitable standard reliability tests presented in [38], a frequency accuracy of 250 ppm and 300 ppm has been achieved, respectively. In this work, it is assumed that all devices presented in Table 1.1 will have similar values for the frequency accuracy under harsh lifetime conditions.

Measurement results and estimations of the stress sensitivity of the LCO frequency presented in this work, reveal mechanical stress to be the major cause of frequency drifts occurring over lifetime. As mentioned in Sec. 1.3.3, mechanical stress can be package induced and caused by moisture (hygroscopic swelling), different thermal expansion coefficients, cure shrink, and soldering. Depending on the conditions, it can thus change over lifetime. Previous research has demonstrated mechanical stress compensation in Hall based current sensors to significantly reduce stress induced measurement errors.

In this work, for the first time the same concept is applied to an LCO based all CMOS frequency reference. The mechanical stress compensation significantly reduces frequency errors as estimated over lifetime by standard reliability tests including HAST and high temperature operating life (HTOL). Compared to the state-of-the-art, a significantly higher overall frequency accuracy of 136 ppm can thus be achieved in this work, considering harsh lifetime conditions.

In state-of-the-art LCO based CMOS frequency references, frequency trimming is combined with an integer frequency divider to cover a wide output frequency range. As the output frequency becomes higher, the dividing ratio has to become smaller. Consequently, for higher output frequencies, the trimming range of the LCO frequency must be accordingly higher leading to a higher portion of required switched capacitors or varactors. Switched capacitors or varactors, used for frequency trimming, degrade the LC tank in terms of linearity and Q. This will have adverse effects on the frequency accuracy and the phase noise performance.

For an LCO utilised in a simple frequency reference, a calibration to a single frequency might be sufficient. However, in state-of-the-art wireless sub-GHz devices a field programmability of the operating frequency is typically available. A typical implementation based on a quartz crystal uses a fractional PLL to generate the RF carrier frequency and thus allows to freely adjust the operating frequency in a wide range [23]. As a consequence, a field programmability is considered a basic requirement for this work.

So far, the Silicon Labs SI4010 [58] is the only device available which has solved the aforementioned problems. The exact implementation is not known, however a trimmed LCO in combination with a frequency divider is used. The SI4010 uses a sophisticated self calibration process to provide a field programmability and to operate over a wide frequency range. The self calibration process must be performed prior to every data package transmission, leading to a significant additional energy consumption.

In this work, an entirely new approach has been chosen based on a non-trimmable LCO. The LCO is combined with a fractional PLL to provide a variable output frequency. In comparison to

the state-of-the-art system architectures presented in Sec. 1.3.2, the temperature compensation is performed via the fractional frequency dividing ratio. An on-chip temperature sensor as well as a digital compensation polynomial are used to determine the correct dividing ratio. Additionally, as a consequence of the digital compensation, a field programmability of the desired frequency can easily be implemented due to the perfect linearity of digital frequency dividing. In contrast, the non-linear properties of analog frequency trimming as used in state-of-the-art LCO based all CMOS frequency references only allow to calibrate such a device to a single frequency.

In this work, a fully integrated all CMOS wireless SoC transmitter is implemented based on an this new approach. Mechanical stress compensation is used to achieve a frequency accuracy, significantly better than the presented state-of-the-art. The device achieves the highest possible level of integration, requiring no external quartz crystal and only a small number of external components for matching and filtering.

Chapter 2

Frequency Reference Concept and Design

As described in Chapter 1, currently costly and bulky quartz crystals are used as the preferred frequency reference. In order to reduce costs and size, several frequency references based on MEMS and CMOS oscillators have thus been presented in previous work for quartz crystal replacement. MEMS based frequency references are typically realised as a two chip solution using a MEMS and a CMOS die, which leads to additional costs. CMOS frequency references refer to devices entirely realised in CMOS. As they can achieve minimum size and costs, CMOS frequency references are considered the most desirable solution. Additionally, a CMOS frequency reference can directly be integrated in a SoC eliminating the need for an additional dedicated oscillator device [5].

This chapter deals with the concept and the design of an LCO based all CMOS frequency reference. In order to design an LCO for the specific requirements of a highly accurate frequency generation in a free running configuration, several difficulties must be taken into account. Next to the frequency determining devices L and C, also other effects can influence the frequency. Previous work shows that unwanted influences can arise from parasitic resistors in the LC tank, from the sustaining amplifier, and from the environment of the LCO [39], [38]. For a high frequency accuracy, all the possible influences must be considered and minimised by designing the circuit accordingly and by other suitable measures apart from the circuit.

For that reason, theortical considerations including CMOS technology scaling as well as several relevant frequency error mechanisms are presented in this chapter. The CMOS technology scaling is thereby regarded as the key enabling factor for this type of frequency reference. Next to other frequency error mechanisms, briefly discussed in this chapter, the LCO temperature characteristic, environmental effects of package and humidity, and mechanical stress are discussed in more detail using theoretical considerations as well as insights from previous research.

Based on the aforementioned considerations, a concept for an LCO based CMOS frequency reference has been developed. In contrast to the state-of-the-art system architectures presented in Chapter 1, for this concept, a new architecture is used, which is based on a non-trimmable LCO. This architecture is optimised for a robust design and thus for a high frequency accuracy.

Using the presented concept, the design of a highly stable LCO will be described under the consideration of the different possible frequency error mechanisms.

2.1 CMOS Technology Scaling

LCOs have been used as frequency references in a free running configuration for over 100 years [13]. Also, LCOs are often used as the VCO in integrated PLLs. However, only since 2008 [56], integrated LCOs are also available on the market used as frequency references in a free running configuration, even though all the required components comprising of inductors, capacitors, and the CMOS transistors are standard devices inherently available in every CMOS technology. In order to find the reason for that, certain properties of the integrated active and passive components must be taken into account.

Active components are strongly non-linear devices. They show a considerable temperature dependency and are prone to ageing. In contrast, passive components are excellent in terms of linearity, temperature dependency, and ageing. However, active components are required to fundamentally make a circuit work, e.g., by providing gain. Therefore, precise analog circuits are typically arranged in a way, so that the behaviour is mainly determined by passive components, whereas the active components, which are required for the functionality, have little influence. This concept is often used, e.g., in the feedback of operational amplifiers to provide a precise gain factor. The same concept is applied in precision oscillators. In RCOs the frequency is ideally given by the time constant determined by R and C only. In integrated LCO frequency references the same concept is pursued with the frequency given by L and C. Also, integrated LCO frequency references pursue this strategy where the frequency i designed to be a function of L and C.

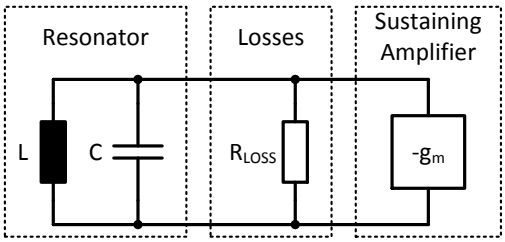

Figure 2.1: Simplified circuit of an LCO comprising of the LC tank, a parallel resistor R_{LOSS} that represents the losses, and the sustaining amplifier

Figure 2.1 depicts a simplified LCO circuit, comprising of the LC tank, a parallel resistor accounting for the losses, and a sustaining amplifier which is required to compensate the losses. The passive devices L and C determine the resonance frequency. An ideal sustaining amplifier would have no influence, except of providing a negative transconductance $-g_{\mathrm{m}}$. However,

in practice the sustaining amplifier consists of active components (transistors). Figure 2.6 shows a simplified architecture of an LCO including the transistors which form the sustaining amplifier. The transistors have an unwanted influence on the resonance frequency. As the Q of integrated LCOs is very low (10-20), the transistors of the sustaining amplifier must be designed accordingly large, which further increases their influence on the resonance frequency. Different parasitics in the equivalent circuit of these transistors can influence the resonance frequency. However, the gate capacitance of the transistors is considered the major influence. In general, such an influence can be cancelled out with the calibration. However, as the gate capacitance has a strongly non-linear behaviour, it varies with the LCO amplitude. This leads to a high sensitivity of the LCO frequency to ageing related drifts of the LCO amplitude, considerably limiting the achievable frequency accuracy.

In the following, the relation between this unwanted gate capacitance and the minimum transistor length (l) in a CMOS technology is illustrated.

In order to maintain a continuous oscillation, a negative transconductance $-g_\mathrm{m}$ must be provided by the sustaining amplifier. This is necessary to compensate the losses of the LC tank as indicated in Figure 2.1. The relation to be fulfilled is defined by

$$g_\mathrm{m} = \frac{1}{R_\mathrm{LOSS}}. \tag{2.1.1}$$

According to [73], the transconductance for the small signal behaviour of a transistor can be expressed as follows:

$$g_\mathrm{m} = \sqrt{2I_\mathrm{D} \cdot \mu \cdot C_\mathrm{ox} \cdot \frac{w}{l}}. \tag{2.1.2}$$

Next to the current (I) into the drain terminal I_D and the technology-specific parameters mobility (μ) and oxide capacitance per unit gate area (C_ox), the transistor dimensions, the transistor width (w) and l, have a significant influence on the transconductance. At the same time, the transistor dimensions w and l also greatly influence the gate capacitance. Several parasitic capacitors can be relevant for the gate terminal in a transistors equivalent circuit including the gate-source capacitance (C_gs), the gate-drain capacitance (C_gd), and the gate-bulk capacitance (C_gb) [73]. However, for simplicity only the gate-channel capacitance (C_gc) is considered according to:

$$C_\mathrm{gc} = C_\mathrm{ox} \cdot w \cdot l. \tag{2.1.3}$$

Using Equation 2.1.2 and Equation 2.1.3, a relation between the gate-channel capacitance C_gc and the transistor dimension l can be derived for a given negative transconductance $-g_\mathrm{m}$:

$$C_\mathrm{gc} \propto l^2. \tag{2.1.4}$$

As for a given $-g_\mathrm{m}$, w of the transistors can be scaled linearly with l (see Equation 2.1.2), the corresponding gate area and consequently the gate-channel capacitance C_gc scale quadratic with the transistor dimension l. The gate-channel capacitance C_gc as well as the LCO frequency sensitivity to ageing related LCO amplitude drifts thus scale quadratic with the l of the

transistors. As this sensitivity should be minimised, l is dimensioned as small as possible in a given technology.

As a result, the scaling of the minimum l in modern CMOS technologies can be considered as the key factor enabling the design of very accurate LCO frequency references with integrated low Q LC tanks. As mentioned in Sec. 1.3.2, a better frequency accuracy can be observed in Table 1.1 for devices designed in smaller technologies. The first reported high accuracy integrated LCO frequency reference [55] has been realised in a 350 nm technology. Further scaling of the transistor length l improves the accuracy, however, at some point, frequency errors based on other effects prevail. Most new designs and also the chips designed in this work are implemented in a 130 nm CMOS technology.

2.2 Frequency Error Mechanisms

In an all CMOS frequency reference based on an integrated LCO several mechanisms can lead to frequency errors. The major portion arises from variations of the LCO frequency caused by process variations of the capacitor. A minor influence is caused by the inductor which can be manufactured with much tighter tolerances. However, process variations are cancelled out at the initial calibration and are assumed to remain constant over the device lifetime.

Contrary, several other error mechanisms can change the LCO frequency over operating conditions and over the device lifetime. This error mechanisms include the temperature characteristic, magnetic and electric interaction of the LCO with its environment, mechanical stress, injection pulling, and ageing of the CMOS circuit.

The greatest of these effects is the LCO temperature characteristic which is described in more detail in Sec. 2.2.1. A temperature calibration method as well as measurement results are presented in Sec. 4.1.4.

Frequency errors caused by magnetic and electric field interactions of the LCO inductor with its environment are very unique problems, only relevant for LCO frequency references in a free running configuration. In a typical LCO based VCO applied in a PLL, such frequency errors are cancelled by the phase regulating properties of the PLL. In order to reduce frequency errors caused by magnetic interactions, magnetic shielding must be applied. The magnetic shielding structure applied in this work is presented in Sec. 2.4.4. In order to reduce electric field effects, a plastic package is used in this work which assures a consistent electric environment of the LCO inductor. Using a plastic package, a post-assembly calibration must be applied in order to reduce the package induced shift of the LCO frequency [38]. However, residual errors can arise from water absorption of the plastic package over the device lifetime [39]. An estimation of the frequency error caused by water absorption is presented in Sec. 4.2.

A significant frequency error can also arise as a result of mechanical stress. Mechanical stress can be caused by the packaging process. Applying a post-assembly calibration, however, this effect is cancelled out. Nevertheless, caused by soldering, mechanical stress of the package or the PCB, or simply by water soaking of the plastic package, the mechanical stress of the chip can change over the device lifetime [39]. As a consequence of the mechanical stress sensitivity of the LCO frequency, a considerable frequency error can thus occur over the device lifetime. A mechanical stress sensitivity estimation and measurements are described in more detail in Sec. 2.2.3 and Sec. 4.3, respectively. Furthermore, a mechanical stress compensation technique as a means for a reduction of the mechanical stress sensitivity is presented in Sec. 4.1.5.

As another mechanism, frequency errors can arise from electromagnetic interference. In a special case such an interference is caused by the output signal of the all CMOS frequency reference. For certain ratios between the LCO frequency and the output frequency considerable frequency errors can be caused by injection pulling. Injection pulling is investigated in more detail in Sec. 4.5.

Furthermore, ageing of the CMOS devices over the device lifetime can occur and can lead to frequency errors. Ageing mostly affects the active components, e.g., the CMOS transistors, as they experience very high electric fields as well as current densities. The CMOS devices, which potentially can affect the LCO frequency, are generally confined to the transistors of the sustaining amplifier. However, also reference currents and voltages can drift over lifetime as a result of ageing and can consequently lead to frequency errors. An investigation of the relevant parameters as well as the result of a high temperature accelerated ageing test is presented in Sec. 4.4.

2.2.1 LCO Temperature Characteristic

In integrated LCOs, several effects can have an influence on the temperature characteristic of the LCO frequency. A temperature dependency can arise from the passive components of the LC resonator including the inductor and the capacitor, but also from losses in the resonator, represented as lossy resistors. Additionally, the sustaining amplifier can show temperature dependent characteristics influencing the LCO frequency. Figure 2.2 shows an extended simplified equivalent circuit of an LCO. The lossy components are included and are split into losses referable to a parallel resistor R_{P}, and losses referable to series resistors R_{SC} and R_{SL} of the capacitor and the inductor.

The temperature characteristics of integrated capacitors and inductors are defined by material specific properties. The temperature coefficient of the capacitor is mostly given by the temperature coefficient of the permittivity of the exploited insulating material. For a metal-metal capacitor, a temperature coefficient (TC) of about 25 ppm/K is caused by a silicon oxide insulator. For the inductor, a very low positive temperature coefficient in the range of single digit ppm/K can be estimated, considering the change of geometry caused by the thermal

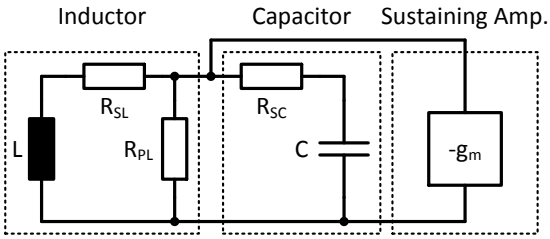

Figure 2.2: Extended simplified equivalent circuit of an LCO comprising losses in the LC tank and the sustaining amplifier to compensate these losses: The losses can be split in losses caused by series and parallel resistors having different effects on the LCO frequency.

expansion of silicon substrate. A thermal expansion coefficient of 2.5 ppm/K has been reported in [74]. In [75] a very low temperature coefficient of the inductance has been reported for integrated inductors. The influence on the LCO frequency caused by changes of the capacitor or the inductor can be derived from Equation 1.1.5 as:

$$\omega = \sqrt{1/(LC)} \rightarrow \frac{d\omega/\omega}{dL/L} = \frac{d\omega/\omega}{dC/C} = -\frac{1}{2}. \tag{2.2.1}$$

Accordingly, a combined LCO temperature characteristic of about -13.75 ppm/K can be estimated to be caused by the capacitor and the inductor, assuming a TC of 2.5 ppm/K for the inductor.

In [38], the lossy components of the LC tank have been identified as the primary mechanism for frequency drifts referable to the temperature. The inductor as well as the capacitor of the LC tank are composed of metal layers which exhibit a finite conductivity. Consequently, these components show losses which can be considered as series resistors as shown in Figure 2.2. Also parallel losses occur, but can be neglected for considerations of the temperature characteristics, as these losses are compensated by the sustaining amplifier with only little effect on the LCO frequency. The lossy series resistors R_{SC} and R_{SL} exhibit temperature coefficients ($R_{\mathrm{SC}}(T)$, $R_{\mathrm{SL}}(T)$) and consequently influence the resonance frequency of the LCO depending on the temperature (T). The corresponding relation is defined by [38]

$$\omega_0 = \sqrt{1/(LC)} \rightarrow \omega_1(T) = \omega_0 \sqrt{\frac{CR_{\mathrm{SL}}^2(T) - L}{CR_{\mathrm{SC}}^2(T) - L}}. \tag{2.2.2}$$

Typically, the losses in an integrated inductor are much greater than in an integrated capacitor. The effects of R_{SC} can thus be neglected for the subsequent considerations. The temperature characteristic can therefore be approximated by [38]

$$R_{\mathrm{SL}} \gg R_{\mathrm{SC}} \rightarrow \omega_1(T) \approx \omega_0 \sqrt{1 - \frac{CR_{\mathrm{SL}}^2(T)}{L}}. \tag{2.2.3}$$

Assuming a constant temperature coefficient of $R_{\mathrm{SL}}(T)$, Equation 2.2.3 implies a second order negative concave-down temperature characteristic of the LCO frequency.

For a well working temperature compensation, the temperature coefficient of the LCO frequency TC_{LCO} must be as small as possible. In the following, the TC_{LCO} is defined by

$$TC_{\mathrm{LCO}} = \frac{1}{\omega_0}\frac{d\omega_1(T)}{dT}. \tag{2.2.4}$$

Inserting Equation 2.2.3 into Equation 2.2.4, the influence of R_{SL} on the LCO frequency as well as an approximation for it can be defined as follows:

$$\frac{1}{\omega_0}\frac{d\omega_1(R_{\mathrm{SL}})}{dR_{\mathrm{SL}}} = -\frac{R_{\mathrm{SL}}C}{L\sqrt{1-\frac{CR_{\mathrm{SL}}^2(T)}{L}}} \approx -\frac{R_{\mathrm{SL}}C}{L}. \tag{2.2.5}$$

Under consideration of the temperature coefficient TC_{RSL} for the exploited conductive material of the inductor, $dR_{\mathrm{SL}}(T)$ can be substituted with dT according to

$$\frac{dR_{\mathrm{SL}}(T)}{dT} \approx TC_{\mathrm{RSL}}R_{\mathrm{SL}}. \tag{2.2.6}$$

Considering Equation 2.2.6 and Equation 2.2.5 as well as the definition of the Q of an LCO (Equation 1.1.2), a relation can be derived, indicationg a reciprocal and squared relation between the Q_{S} and the temperature coefficient of the LCO frequency

$$TC_{\mathrm{LCO}} = \frac{1}{\omega_0}\frac{d\omega_1(T)}{dT} \approx -\frac{TC_{\mathrm{RSL}}{R_{\mathrm{SL}}}^2C}{L} = -\frac{TC_{\mathrm{RSL}}}{Q_S^2}, \tag{2.2.7}$$

whereas Q_{S} refers to the portion of Q that is attributable to the series resistor losses in the inductor. In state-of-the-art CMOS LCOs, a Q_{S} in the order of 10-20 can be achieved [10]. A calculation example for a Q_{S} of 10 using copper with a relative temperature coefficient of $3.9\,10^{-3}$/K is shown in the following:

$$TC_{\mathrm{LCO}} = \frac{1}{\omega_0}\frac{d\omega_1(T)}{dT} \approx -\frac{3.9\ 10^{-3}K^{-1}}{10^2} = -39\ ppm/K. \tag{2.2.8}$$

With Q_{S} of 10, a temperature coefficient of -39 ppm/K can be achieved. Depending on the available metal stack, a Q_{S} of up to 20 can be achieved in CMOS LCOs which will results in a temperature coefficient of only about -10 ppm/K. For practical reasons, a slightly higher value can be estimated for the temperature coefficient caused by an additional influence of the sustaining amplifier. Further additional losses caused by the temperature coefficient of R_{SL} in the LC tank are compensated due to the automatic amplitude regulation described in Sec. 2.4.3 by providing a higher negative transconductance $-g_{\mathrm{m}}$ of the sustaining amplifier. As a result,

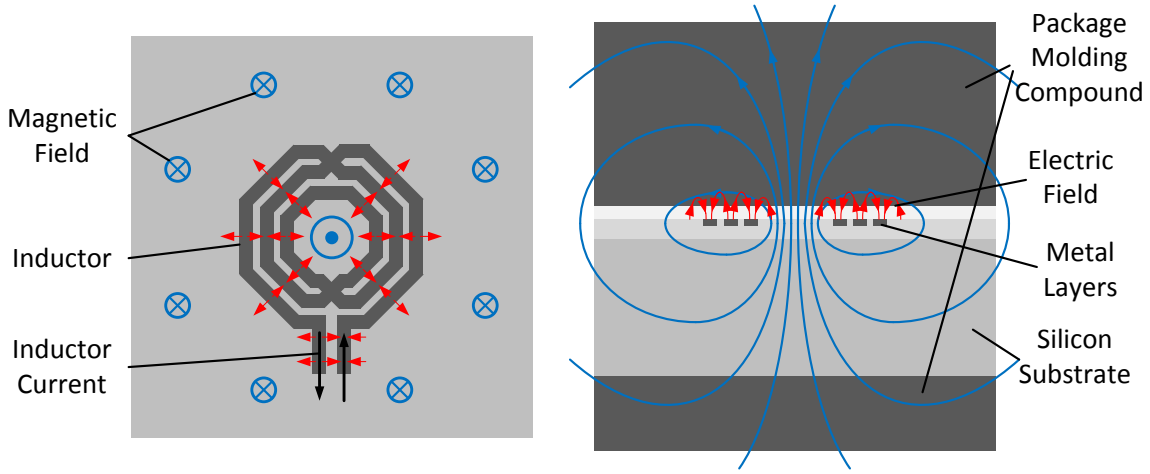

Figure 2.3: Top and cross-sectional schematic view of an integrated inductor and its electric (red) and a magnetic field (blue): The generated electric and magnetic fields spread out and interact with the inductors environment. As a consequence, the inductance is influenced by the inductor environment leading to an environmental sensitivity of the LCO frequency.

the effective capacitance of the sustaining amplifier will increase leading to an amplification of the temperature coefficient of the LCO frequency caused by R_{SL}.

Considering the aforementioned temperature effects of the LCO, it can be concluded that a portion of about -15 ppm/K of the temperature characteristic is referable to the inductor and the capacitor. This portion is caused by material specific properties and is thus assumed to be independent of process variations. However, the major portion of the temperature characteristics is referable to the losses in the series resistor R_{SL} of the inductor. As the value of R_{SL} exhibits strong process variations, also strong variations of the overall temperature characteristic of the LCO frequency occur, making it necessary to apply a sophisticated temperature calibration within LCO based frequency references, as shown in Sec. 4.1.4.

2.2.2 Environmental Effects of Package and Humidity

By applying a current to an inductor, a magnetic field is created. The created magnetic field spreads out into the environment as depicted in Figure 2.3 for an integrated inductor. This spread magnetic field interacts with the environment of the inductor. Based on the electrical characteristics, interactions occur referable to the permeability of the materials in the environment, as well as eddy currents for conductive materials. This interactions lead to a change of the electrical characteristics, influencing the effective inductance of the inductor. As a consequence, a dependency on the environment must be expected for the LCO frequency.

Next to the magnetic field spread, the inductor of the LCO also produces an electric field. In comparison, a relevant electric field only arises around the close environment of the inductor windings. Consequently, only in this area an interaction with the environment leads to significant LCO frequency errors. Furthermore, for a frequency error consideration only the electric field which spreads on top of the chip surface is of interest and is also shown in Figure 2.3. A similar electric field is formed on the substrate side of the inductor, however does not lead to a change of the LCO frequency over the device lifetime.

In typical applications for integrated inductors, electric or magnetic field interactions can be neglected. For VCOs in a PLL configuration, frequency errors are compensated via the phase regulation. In filter or matching applications, the tolerances typically exceed the environmental related variations by far. However, in a free running LCO used as a frequency reference, this interactions are very critical as frequency errors of hundreds of ppm can easily be caused by the environment [76]. An effective shielding measure is thus mandatory for a high frequency accuracy.

Measurement results presented in Sec. 4.2 and also in [76] indicate that, due to the electric and magnetic field spread of the inductor, a plastic package is required to ensure a consistent electrical environment with a constant permeability and permittivity. The plastic package assures a consistent electric behaviour by keeping away any contamination from the chip surface. However, the plastic package can absorb water from its environment, which in turn increases its effective permittivity. Due to the interaction with the electric field of the LCO, a parasitic capacitor is formed, which depends on the water content of the package. This effect leads to an LCO frequency error due to the electric field interaction induced by the water absorption of the package. An investigation of the LCO frequency sensitivity to water absorption of the plastic package is presented in Sec. 4.2. While the electric field can be sufficiently shielded from the environment by a plastic package coverage, the magnetic field can spread much further. Even the environment outside of the plastic package can influence the inductance. In [76], an effect on the LCO frequency induced by magnetic field modulation has been found in a distance of up to 1 mm to the chip surface. An additional shielding measure is thus mandatory for a high frequency accuracy. For this work, a magnetic shielding structure has been developed (see Sec. 2.4.4).

2.2.3 Mechanical Stress

The mechanical stress (σ) has a significant influence on integrated circuits including integrated oscillators (see Sec. 1.3.3). The stress sensitivity of the transistors [77] can have an influence, e.g., by altering the transconductance and consequently the frequency of a ring oscillator. Also, an RCO can have a significant stress sensitivity due to the piezo-resistive effect by influencing the RC time constant. In contrast, integrated LCOs are expected to be less stress sensitive, as the passive components L and C are not subject to piezo effects. Nevertheless, the LC tank resonance frequency is affected by alteration of the inductance and capacitance induced by the

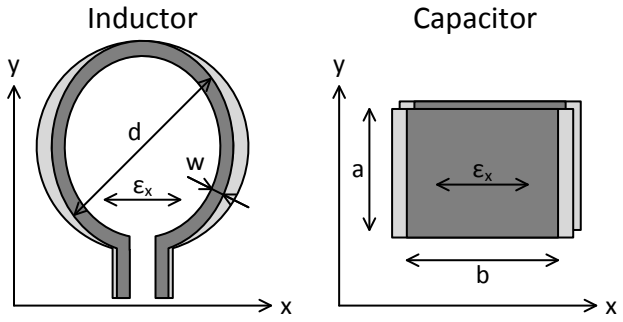

Figure 2.4: Strain of an integrated inductor and capacitor as a response to mechanical in-plane stress: The stress induced geometric deformation causes an alteration of the values of the inductor and the capacitor (the strain in the x-direction is shown exemplarily).

mechanical strain (ε). The strain induced deformation of an integrated inductor and capacitor is depicted in Figure 2.4. It is assumed, that all relevant measures scale uniformly as a response to in-plane stress, e.g., the relative change of w is proportional to the relative change of d as responce to strain ($w(\varepsilon) \propto d(\varepsilon)$). The corresponding influence on the values of L and C is elucidated in the following:.

$$L \propto d \rightarrow \frac{dL/L}{d\varepsilon} = \frac{1}{2}, \tag{2.2.9}$$

$$C \propto a \cdot b \rightarrow \frac{dC/C}{d\varepsilon} = 1. \tag{2.2.10}$$

As already shown in Equation 2.2.1, the relative change of the LCO frequency caused by changes of the capacitor or the inductor scales with $-1/2$. Considering the elasticity modulus (E) (relation between stress and strain [12]) with in-plane values of $E = E_{\mathrm{XX}} = E_{\mathrm{YY}} = 169\,\mathrm{GPa}$ for standard (100) silicon [33], an LCO frequency sensitivity to mechanical stress can be estimated according to:

$$\sigma = E\varepsilon \rightarrow \frac{d\omega/\omega}{d\sigma} = \frac{-0.375}{E} = -2.22\,ppm/MPa. \tag{2.2.11}$$

In ICs, assembled in standard plastic packages, mechanical stress can change over the lifetime, induced by hygroscopic swelling, high temperature ageing, and soldering. This change in mechanical stress can be in the order of up to 100 MPa [72] and can consequently lead to frequency errors ranging up to over 200 ppm. Additional errors can arise from the stress sensitivity of the sustaining amplifier, as the transistors are influenced by mechanical stress [76]. However, these effects are considered insignificant and are thus neglected in this work.

2.3 Non-Trimmable LCO Concept

An LCO is an electrical resonator and the components L and C are easily accessible. As a consequence a trimming of the resonance frequency can easily be accomplished by means of a

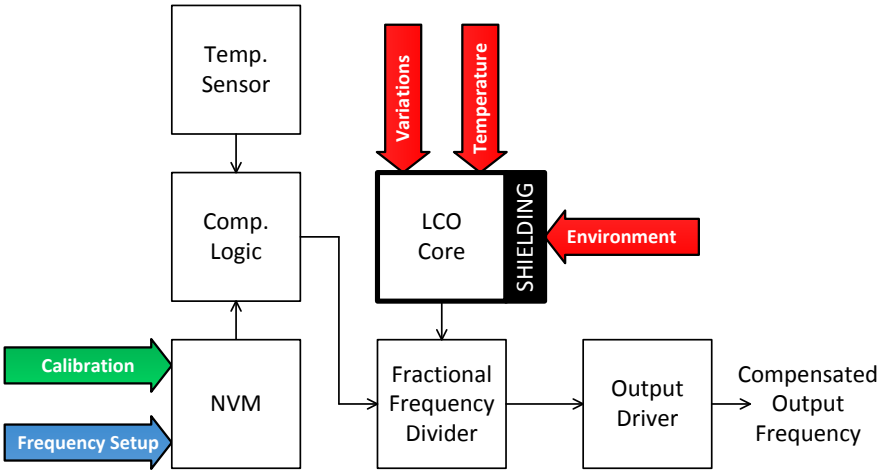

Figure 2.5: LCO frequency reference based on a non-trimmable LCO: A variable and temperature compensated frequency is derived by means of a temperature sensor, a compensation logic, and a fractional frequency divider.

variable capacitor. In all the system architectures for LCO based CMOS frequency references introduced in Sec 1.3.1, a trimming of the LCO frequency is therefore used for calibration and temperature compensation. In contrast, in mechanical resonators an electrical equivalent circuit can be generated composed out of the components L, C, and R. The components of this equivalent circuit are not directly accessible. Therefore, frequency trimming can only be accomplished via the electrical terminals of the mechanical resonator. Due to the high Q, most energy is captured in the resonator and only a low amount of energy can be exchanged trough the electrical terminals. As the Q is typically very high, trimming can only by accomplished for a very small range of a few tens of ppm for a quartz crystal or a few thousands of ppm for a bulk acoustic wave (BAW) resonator [78]. Therefore, in frequency references based on mechanical resonators, a fractional frequency synthesises, e.g., a fractional PLL is used as the preferred means to derive a variable output frequency from the fixed frequency of the mechanical resonator.

Although frequency trimming of LCOs is a well known technique for VCOs in PLLs, it comes with significant disadvantages for an LCO utilized in a free running configuration for a CMOS frequency reference. Frequency trimming either realised by means of a switched capacitor array or by a varactor leads to a degradation of Q as well as to an introduction of highly non-linear devices to the LC tank. Therefore, in this work, an entirely different approach is pursued for an LCO based all CMOS frequency reference. Figure 2.5 depicts the simplified system architecture implemented in this work. To avoid all the disadvantages of frequency trimming, this approach is based on a free running LCO, which is not trimmable at all (see Figure 2.5, LCO core). Instead, a variable output frequency can be generated using a fractional frequency divider. The frequency can be adjusted by means of the digital dividing ratio. As mentioned before, several unwanted influences affect the LCO frequency. Exemplarily, process variations,

temperature, and the LCO environment is shown in Figure 2.5. While environmental effects can be mitigated by means of shielding, other effects must be compensated. The correct dividing ratio is thus determined by a compensation logic under consideration of the calibration and frequency setup data as well as an on-chip temperature sensor. Instead of a calibration by means of frequency trimming, the frequency of the LCO is measured at several temperatures. A compensation polynomial is generated out of this measurements, which characterizes the LCO temperature behaviour. The correct output frequency is generated by an output driver stage under consideration of this compensation polynomial and a frequency setup value. The calibration and frequency setup data is stored in an integrated NVM.

This architecture constitutes an all digital approach, which leads to several advantages over an architecture using a frequency trimmed LCO. No lossy or non-linear trimming component is used in the LC tank which allows the design of an LCO for optimised robustness in terms of frequency accuracy. Also, due to the perfect linearity of digital frequency division, the frequency setup can be simplified. A separation between the calibration and the frequency setup of such a device is possible and allows for a field programmability, similarly to MEMS based frequency references described in Sec. 1.1.2. Also, a digital frequency setup and modulation is doable which facilitates the deployment in a wireless application. On the downside, this architecture leads to a higher system complexity and power consumption. Also, some impairments on the phase noise and jitter performance due to the fractional divider must be expected in comparison to an architecture using a frequency trimmed LCO (see Sec. 4.6).

2.4 LCO Based Frequency Reference Design

Figure 2.6 depicts the simplified block circuit diagram of the LCO core. In its core, the LCO consist of an LC tank composed of an inductor and a capacitor in a parallel arrangement. For simplicity, the lossy components are neglected. Different arrangements are possible for LCOs, nevertheless for this work a symmetric design has been chosen. Therefore, a symmetric voltage (V) signal is obtained at the nodes V_{LCOA} and V_{LCOB} of the LCO during operation. In order to excite and sustain an oscillation, a sustaining amplifier is implemented. The sustaining amplifier is realised with a negative transconductance amplifier $-g_{\mathrm{m}}$. In a differential LCO architecture this can easily be accomplished by means of a cross coupled transistor pair. For a high power efficiency, such a cross coupled pair is implemented in this work on the positive (-GM PMOS) and on the negative (-GM NMOS) supply side of the LC tank. The sustaining amplifier is powered via two pass devices on the positive and negative supply side. The pass devices can be arranged as a current or as a voltage source, respectively. In this work, the positive pass device is arranged as a current source and the negative pass device behaves like a voltage source.

Typically, in LCOs a simple current source can be used to power the sustaining amplifier. However, for highly stable self referenced LCOs an automatic amplitude control is required. The

sustaining amplifier can influence the LCO frequency by several mechanisms. This can occur via the gate-source capacitance of its transistors, by the parasitic pn-junction capacitance of the drain terminals, and also by harmonics of the current injected into the LC tank. This influences can considerably alter the LCO frequency and also make it sensitive to drifts of the supply voltage, the reference voltages as well as currents, and to a drift of device parameters referable to ageing. By applying automatic amplitude control, the LCO can be operated at an optimum power level to minimise these adverse effects. Therefore, a positive and a negative peak detector is implemented to detect the maximum and minimum voltage of the LCO terminals V_{LCOA} and V_{LCOB}. A reference voltage generator provides two reference voltages V_{RP} and V_{RN} which are aligned around half the supply voltage. Two regulators adjust the voltage source (negative pass device) as well as the current source (positive pass device) in such a way that the peak values correspond to the reference voltages.

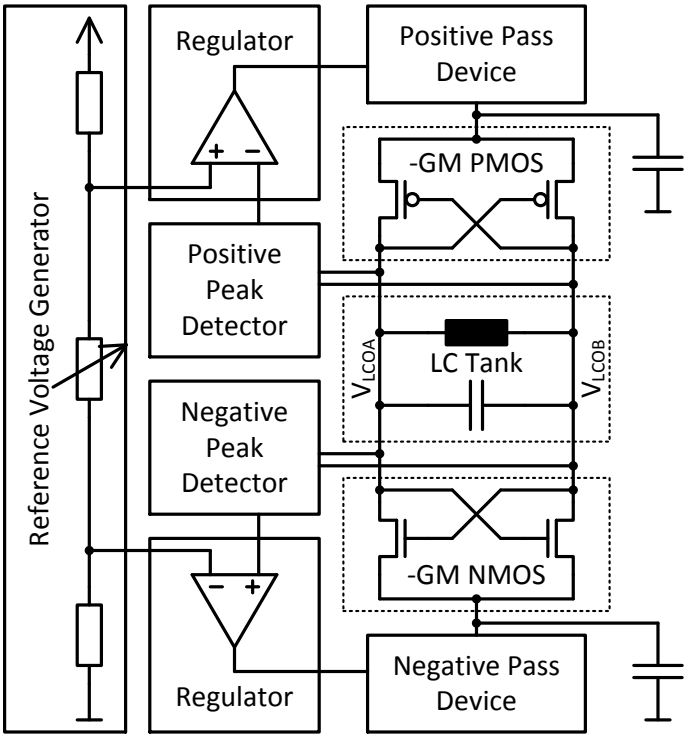

Figure 2.6: Simplified block diagram of the LCO core

2.4.1 Quality Factor Optimised LCO

In integrated LCO based frequency references, a high Q is crucial for the frequency accuracy and also for other characteristics typically relevant for oscillators like phase noise, jitter, and

power consumption. Addressing the frequency accuracy, the sustaining amplifier is considered the major unwanted influence which scales reciprocally with the Q. In contrast, for phase noise and jitter as well as robustness against interferences, next to the Q, also the overall energy in the resonator must be taken into account. In integrated LCOs, the Q is degraded by losses in the inductor as well as in the capacitor. However, the major portion of losses typically arises in the inductor, while the capacitor contributes only to little losses.

Integrated Inductor

In order to optimise an inductor for the deployment in an integrated LCO frequency reference, its behaviour as well as the corresponding influence on different performance characteristics must be considered. Figure 2.7 shows a detailed equivalent circuit of a typical integrated inductor with two terminals $\mathrm{L_A}$, $\mathrm{L_B}$. Several different parasitic elements are present. Next to parasitic capacitors which reduce the resonance frequency of the LC tank, also lossy resistive components can be found which degrade the Q. The limited conductivity of the employed metal layers leads to losses which are represented by the series resistor R_S. This series resistor constitutes the major loss mechanism of an integrated inductor at low operating frequencies. For high frequencies also other components of the equivalent circuit become more prevalent. The capacitive coupling to the substrate via the parasitic elements C_OX leads to electric fields in the substrate. As the substrate has a high permittivity and also a non-negligible conductivity, this effects are considered in the equivalent circuit of the integrated inductor as the capacitors C_SUB and the resistors R_SUB. In addition to the aforementioned lossy mechanisms, also the skin and proximity effects must be considered which lead to an increase of the series resistor R_S at high operating frequencies. Also, magnetically induced substrate losses occur which are not taken into account.

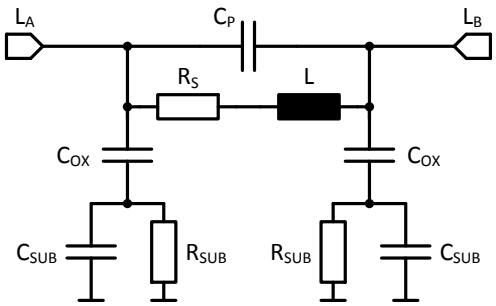

Figure 2.7: Detailed equivalent circuit of an integrated inductor

Most of the inductor losses arise in the parasitic series resistor. Therefore, in order to optimise the quality factor, it is very effective to operate the LCO at a high frequency. However, other mechanisms responsible for losses and also the technology specific maximum frequency of the

CMOS circuit limit the operating frequency. Typically, in LCO based all CMOS frequency references, the resonance frequency of the LCO is chosen in the range between 1 and 4 GHz [5]. For the LCO realised in this work, a frequency of roughly 3.1 GHz has been chosen. As the voltage of the LCO is given by the employed architecture and the transistors of the sustaining amplifier, the energy in the LC tank can only be influenced by the values of the inductor and the capacitor. No custom inductor has been designed as part of this thesis. Instead the best suited inductor has been selected from the available standard inductor library. This inductor has a rather small value of 1.65 nH. The corresponding Q of the LC tank is estimated to be around 10 for the first design (analog test chip, see Sec. 3.1). A version of the inductor, improved via an additional metal layer on top of the exploited metal stack has been used in the final design (SoC transmitter, see Sec. 3.2). The quality factor of the SoC transmitter is estimated to be around 13.

Integrated Capacitor

Integrated PLLs are frequently used in frequency synthesizers employing LCOs as VCOs. The trimming of the frequency is achieved by means of voltage controlled capacitors referred to as varactors. These varactors are strongly non-linear and also have a poor Q. Next to varactors, also capacitors with a fixed capacitance are used which offer a better Q. Several different types are typically available in a standard CMOS process [79].

The metal-metal capacitor also referred to as metal-oxide-metal (MOM) capacitor is the most common capacitor in a CMOS technology. It is formed by at leased two metal plates arranged on top of each other in the standard metal stack and uses the silicon oxide isolation between the metal layers as the dielectric material of the capacitor. This MOM capacitor offers a high Q but typically has a low specific capacitance per area. In another arrangement, this capacitor can also be implemented as a vertical-parallel-plate (VPP) capacitor which typically yields a higher specific capacitance per area. Another commonly used capacitor is the metal-insulator-metal (MIM) capacitor. This type of capacitor uses an isolating materiel between two metal plates which must be separately processed in additional fabrication steps. It offers a high Q and also a high specific capacitance per area, but unfortunately comes with additional costs and is not available in every standard CMOS process. In a process with a FLASH/EEPROM option, also a poly-poly capacitor is available which is formed between the inherently available two poly layers.

For the specific requirements of an LCO based all CMOS frequency reference, a capacitor is needed which offers a high Q as well as a high linearity. Consequently, varactors in general are ruled out. Nevertheless, the usage of varactors has been reported in LCO based all CMOS frequency references using an active temperature compensation architecture [10]. In such an implementation, only a small trimming range is required in comparison to a VCO typically employed in a PLL. The major portion of the capacitance can thus be realised with a highly linear capacitor and only a small varactor is used for frequency trimming and

temperature compensation. For the fixed capacitor used in active and passive temperature compensation architectures, thin-film (MIM) capacitors have been reported as the capacitor of choice [5].

Non-trimmable LC Tank Arrangement

Figure 2.8 shows the three-dimensional view of the LC tank arrangement as implemented in the SoC transmitter.A similar arrangement has been used in previous chips (analog test chip). The inductor can easily be recognized surrounded by a magnetic shielding ring described in more detail in Sec. 2.4.4. As no MIM capacitors are available in the employed CMOS process, the capacitor has been implemented in the standard metal stack as a MOM capacitor. The MOM capacitor is implemented using metal plates on top of each other in a cross coupled arrangement for a symmetric connection to the inductor. Additionally, an electric shielding is implemented using a shielding plate at the bottom and at the top of the capacitor, respectively. For the LC tank arrangement including the shielding, at least four metal layers are required. In the employed CMOS process, seven metal layers are available from which the metal layers 4-7 are used for the non-trimmable LC tank arrangement according to Figure 2.8. Additional three metal layers are available, allowing the area under the magnetic shielding ring and under the capacitor to be used for circuits and routing. For an area efficient implemented of the final chip, the sustaining amplifier has been placed under the capacitor and the area under the shielding ring has been used for decoupling capacitors of the supply voltage.

2.4.2 Sustaining Amplifier

As mentioned before, the losses in the LC tank must be compensated in order to sustain a continuous oscillation. This generally is accomplished by means of a sustaining amplifier which constantly feeds power into the LC tank. The same concept is also applied for oscillators realised with a mechanical resonator in quartz crystal or MEMS oscillators. The sustaining amplifier can also be considered as a negative resistor or the reciprocal negative transconductance $-g_{\mathrm{m}}$, which is connected to the parallel lossy equivalent resistor of the LC tank (see Figure 2.7). For a continuous oscillation, the reciprocal value of the negative transconductance $(1/-g_{\mathrm{m}})$ exactly matches the lossy equivalent resistor. The negative transconductance $-g_{\mathrm{m}}$ of the sustaining amplifier is therefore the characteristic, which is required for an operation of the LCO. Next to the required negative transconductance, the sustaining amplifier also exerts a number of unwanted effects on the LC tank influencing the resonance frequency. As described in Sec. 2.1, this effects include the non-linear parasitic gate capacitance of the transistors employed in the sustaining amplifier. Additionally, the non-linear transfer characteristics as well as all other parasitic capacitors of the transistors are critical. For given values of the inductor and the capacitor, the required negative transconductance and consequently the dimensions of the sustaining amplifier can be scaled reciprocally with Q of the LC tank. In the same way also

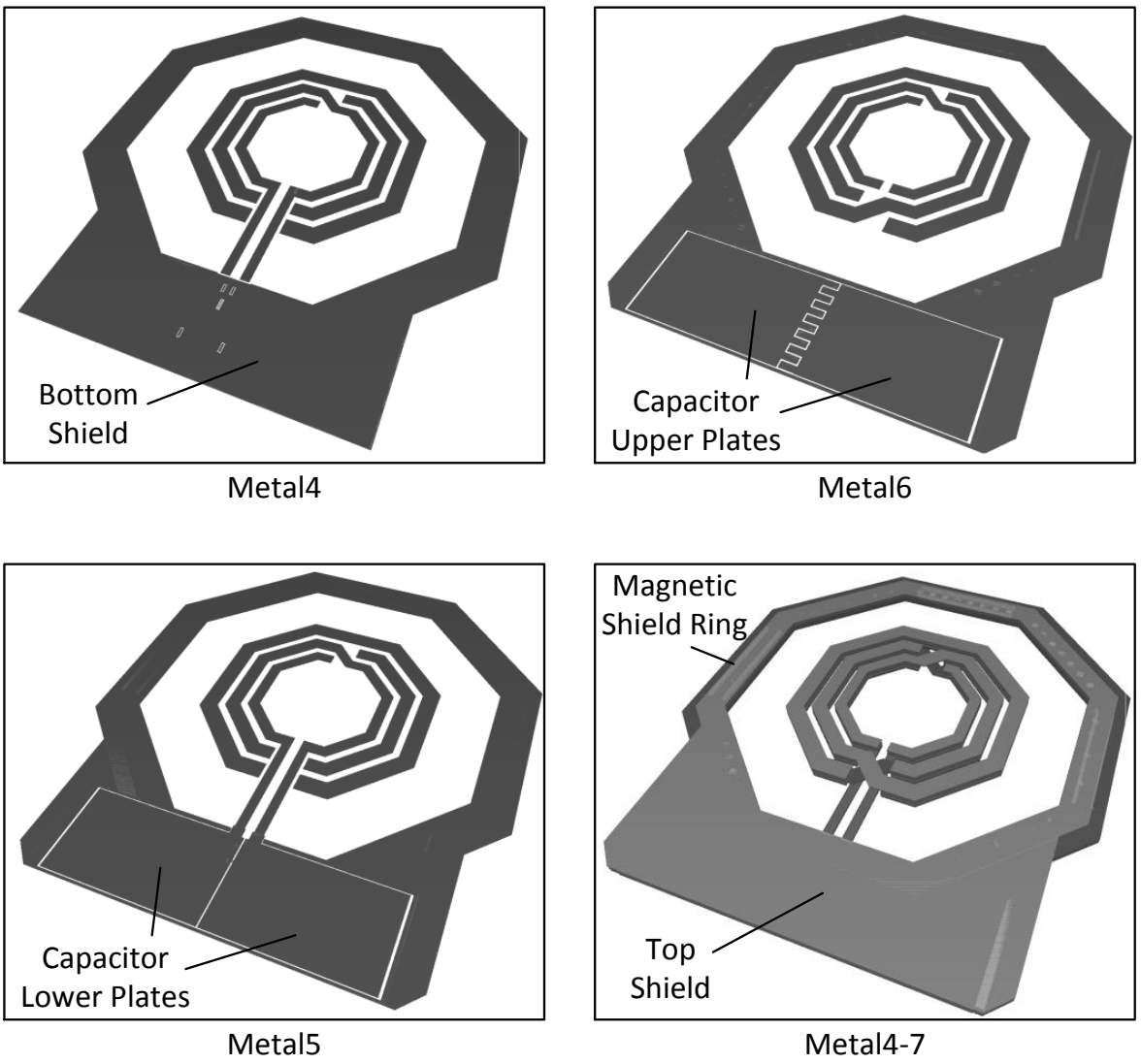

Figure 2.8: Three-dimensional view of the LC tank arrangement using MOM capacitors: The LC tank is implemented using the metal layers 4-7. An electric shield for the capacitor is implemented using the metal layers 4 and 7 at the bottom and top of the capacitor. Additionally, a magnetic shield ring is implemented which surrounds the inductor.

the unwanted effects of the sustaining amplifier scale. This unwanted effects typically can be neglected in oscillators based on mechanical resonators with high Q ranging from 10^3 to 10^6. As in comparison, the Q in integrated LCOs is extremely low (10-20), these effects must be considered as a major frequency error mechanism. The effect of the sustaining amplifier can be minimised by an optimised design as well as an automatic amplitude regulation. Therefore, in this design the dimensions of the transistors of the sustaining amplifier have been chosen to

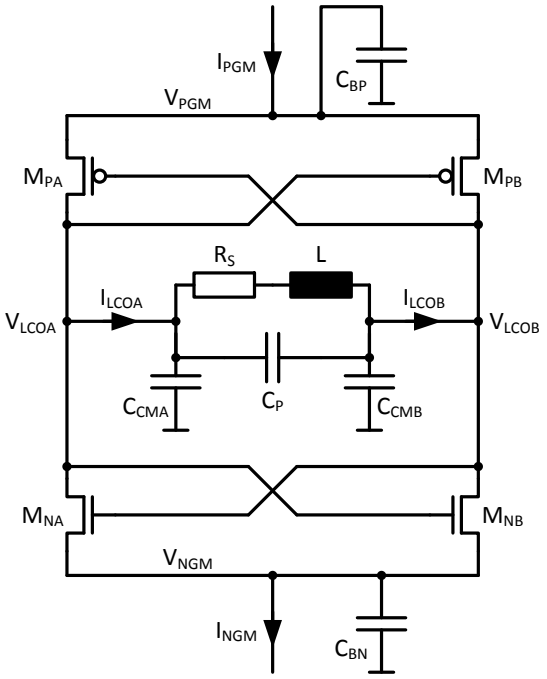

Figure 2.9: Circuit diagram of the LC tank and the the sustaining amplifier: The sustaining amplifier is implemented using two pairs of cross coupled transistors at the positive supply side (M_{PA}, M_{PB}) and at the negative supply side (M_{NA}, M_{NB}), respectively.

have a minimum length of 130 nm in order to keep the gate-capacitance as small as possible. Also, an automatic amplitude regulation is implemented to operate the sustaining amplifier at an optimum power level in terms of sensitivity to voltage drifts, the effective capacitance, and harmonics in the transfer characteristic.

A detailed section of the LCO core showing the LC tank and the cross coupled transistors is depicted in Figure 2.9. The LC tank is composed of the inductor L and its series resistor R_S, the capacitor split into a parallel capacitor C_P and two common mode capacitors C_{CMA} and C_{CMB}. For simplification only the series resistor R_S is considered for losses. The differential operating voltage V_{LCO} of the LCO is connected to the sustaining amplifier via the nodes V_{LCOA} and V_{LCOB}. The negative transconductance $-g_m$ is generated by means of the cross coupled transistor pairs. For a high power efficiency, such a cross coupled pair is placed at the positive (VDD) and negative (VSS) supply side, respectively. The sustaining amplifier is supplied via the tail currents I_{PGM} and I_{NGM}. This tail currents are regulated in such a way, that the LCO nodes V_{LCOA} and V_{LCOB} oscillate around half the LCO core supply voltage. During an oscillation, the sustaining amplifier injects harmonic currents into the tail current nodes V_{PGM} and V_{NGM}. While odd harmonic currents are cancelled in a symmetric differential arrangement, even harmonic currents remain and can lead to harmonic voltages at the tail current nodes. Therefore, additional capacitors C_{BP} and C_{BN} can be used to block even harmonic currents

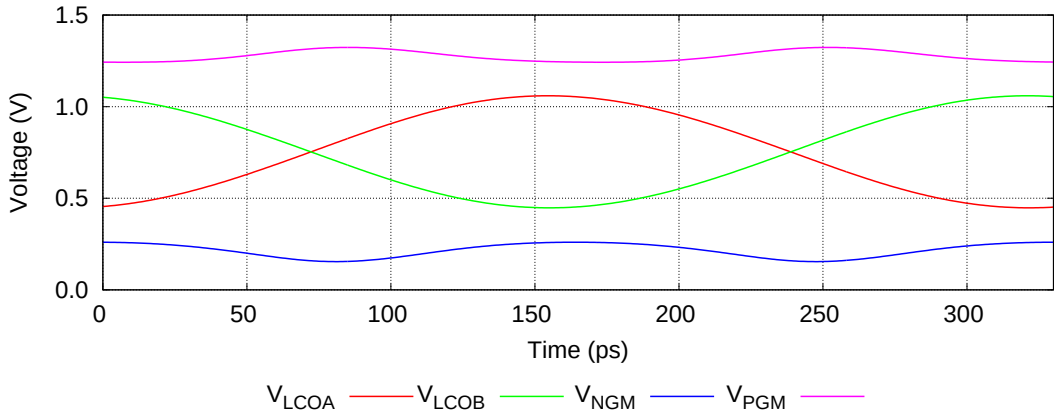

Figure 2.10: Transient voltage signals of the LCO core without blocking capacitors

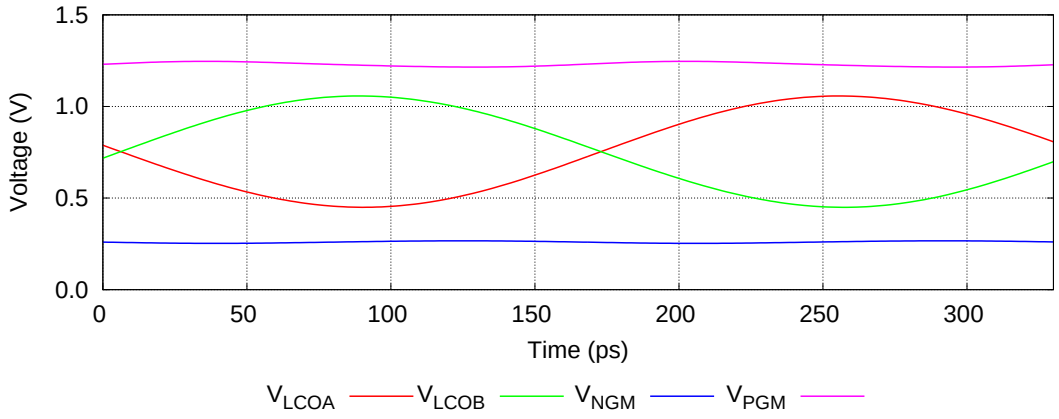

Figure 2.11: Transient voltage signals of the LCO core using blocking capacitors

injected into the tail current nodes of the sustaining amplifier. Figure 2.11 and 2.10 depict the simulated transient curves of the tail current nodes V_{PGM} and V_{NGM} with and without blocking capacitors, respectively. The results have been obtained using the simulator Spectre® from Cadence Design Systems, Inc.

In the following simulation results, the behaviour of the LCO core is investigated in terms of frequency, amplitude, and the usage of blocking capacitors. For further considerations and depicted simulation results, the following simplifications are applied to the analysis:

$$V_{\mathrm{LCO}} = V_{\mathrm{LCOA}} - V_{\mathrm{LCOB}}, \tag{2.4.1}$$

$$I_{\mathrm{GM}} = \frac{I_{\mathrm{PGM}} + I_{\mathrm{NGM}}}{2}, \tag{2.4.2}$$

$$I_{\mathrm{LCO}} = \frac{I_{\mathrm{LCOA}} + I_{\mathrm{LCOB}}}{2}. \tag{2.4.3}$$

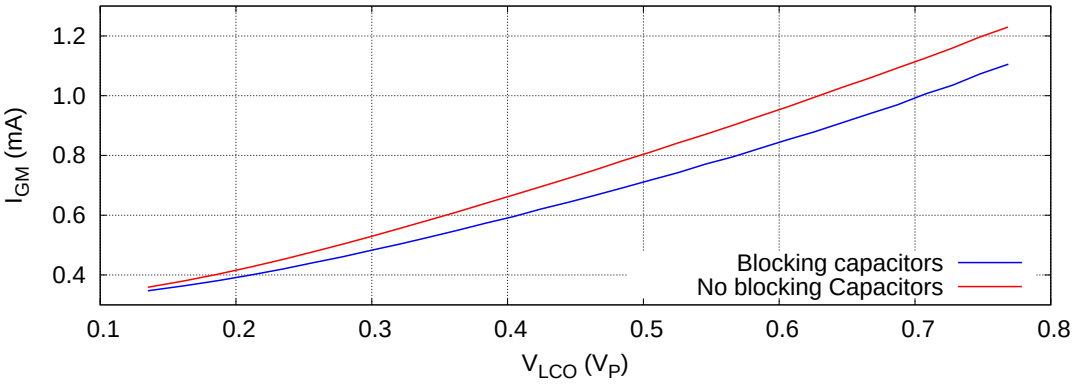

Figure 2.12: Simulated current consumption of the LCO core as a function of the amplitude. The blocking capacitors reduce the current for a given amplitude and hence improve the efficiency of the sustaining amplifier.

Figure 2.12 depicts the current consumption of the LCO core as a function of the LCO amplitude. The usage of blocking capacitors reduces the current consumption by means of a more efficient feeding of energy into the LC tank. In Figure 2.13, the LCO frequency is depicted as a function of the LCO amplitude. A significant reduction of the sensitivity is accomplished by the use of blocking capacitors. Furthermore, the point of the maximum frequency is shifted to higher values by the blocking capacitors. At the point of maximum frequency, the curve is flat and hence has no voltage sensitivity. This point is considered the optimum operating amplitude of the LCO. Using the blocking capacitors, the LCO can be operated with a higher amplitude, which is an advantage in terms of phase noise and sensitivity to interferences. Figure 2.14 depicts the LCO current I_{LCO} and the LCO voltage V_{LCO} over two oscillation periods for amplitudes ranging from 130 mV to 760 mV (V_{CON} ranging from 0 mV to 600 mV, see Sec. 2.4.3). The current I_{LCO} is shown with and without blocking capacitors, respectively. A negative transconductance required for oscillation, capacitive effects, and also harmonic portions can be observed. Due to blocking of even harmonic currents into the tail current nodes V_{PGM} and V_{PGM} of the sustaining amplifier, the harmonic portions can significantly be reduced by means of the blocking capacitors for an operation at the respective peak frequency (see Figure 2.13). Due
capacitors are used for the tail current nodes V_{PGM}, V_{PGM} of the sustaining amplifier in this work.

2.4.3 Automatic Amplitude Control

Automatic amplitude control is a commonly known technique used in resonator based oscillators to limit the amplitude or regulate it to an optimum level. As a consequence the sustaining amplifier can be operated at an amplitude where it provides high linearity and power efficiency.

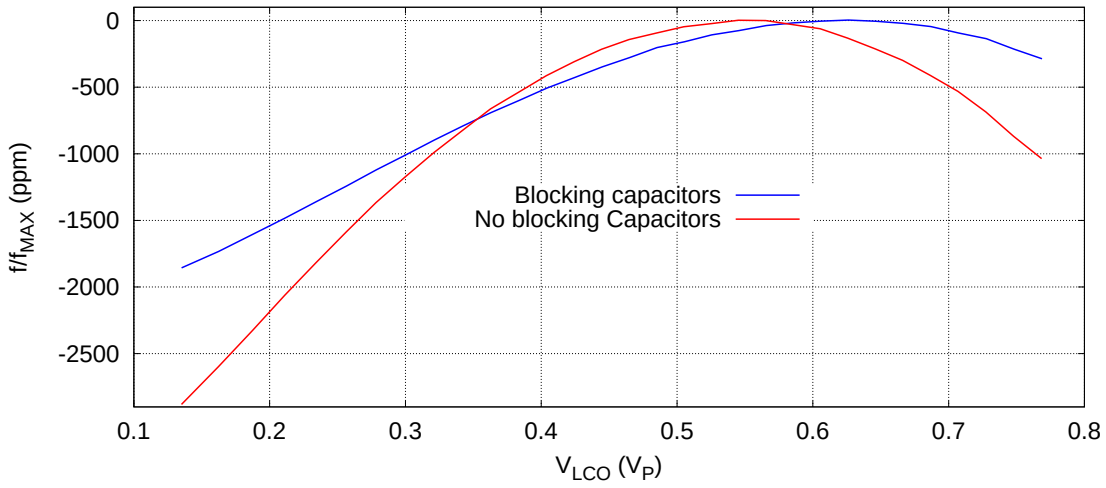

Figure 2.13: Simulated relative LCO frequency with respect to the maximum frequency as a function of the LCO amplitude simulated at 27°C. The blocking capacitors reduce the steepness of the curve and also shift the point of maximum frequency to a higher amplitude.

In comparison, a design without automatic amplitude control can be realised by simply powering the sustaining amplifier with a constant current. In such an implementation the current must be adjusted to a high value to assure an oscillation under consideration of possible process and temperature variations. As a consequence the amplitude of the oscillator will be limited only by the overdrive of the sustaining amplifier. This will lead to an unnecessarily high power consumption as well as to a degradation of the phase noise performance. Automatic amplitude control can thus be used to assure a minimum power consumption along with a high phase noise performance. In an integrated LCO frequency reference the frequency is strongly influenced by the operating amplitude. Figure 2.13 shows the frequency versus amplitude curve simulated for the LCO implemented in this work. A different shape of such a curve has been described in [55]. However, in this work the frequency of the LCO rises with growing amplitude to a maximum and goes down at even higher amplitudes. At its maximum, the curve is flat and therefore exhibits little influence of the amplitude in this region. The specific operating range around the maximum frequency cannot be reached by simply supplying the sustaining amplifier with a constant current. Instead, a tight control of the LCO amplitude must be realised with automatic amplitude control. Consequently, aside from aforementioned advantages, automatic amplitude control can also be applied to improve the frequency accuracy of an LCO based CMOS frequency reference.

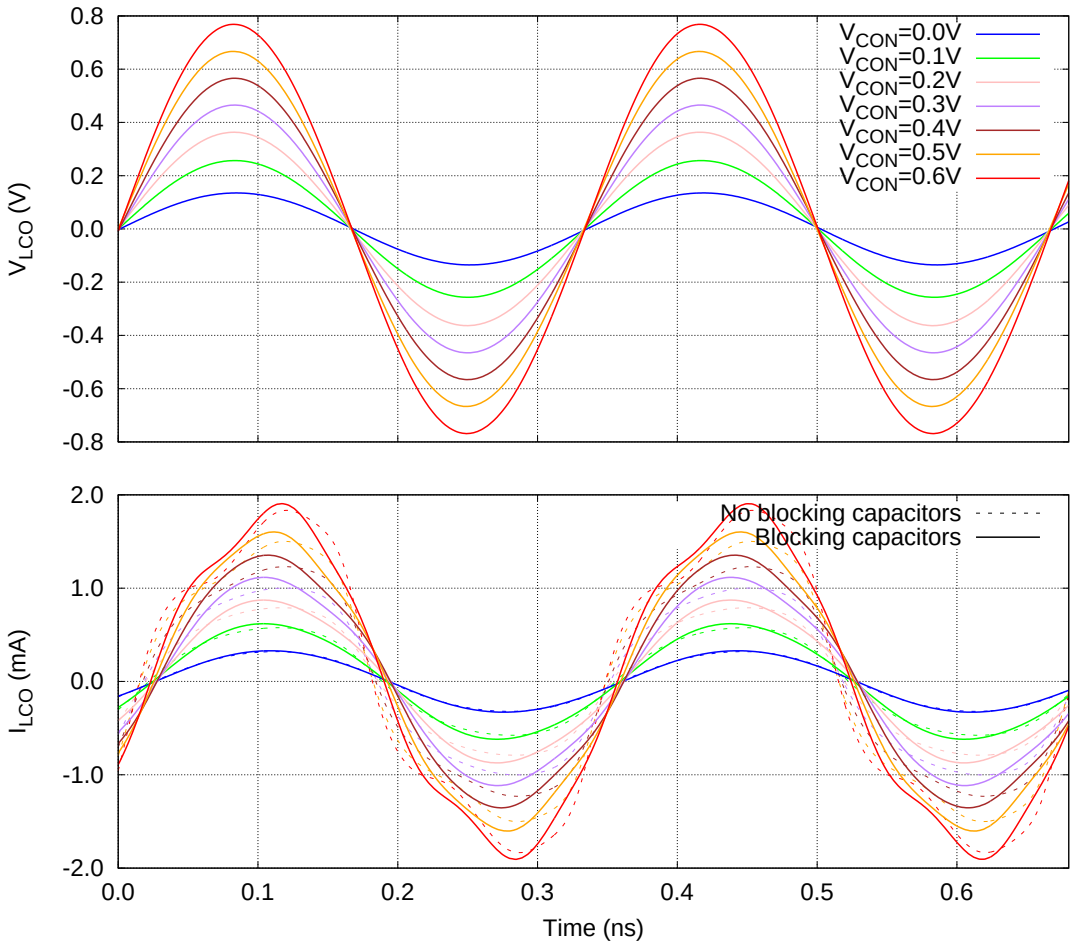

Figure 2.14: Simulated voltage V_{LCO} and current I_{LCO} plotted versus the time for different operating amplitudes with and without blocking capacitors, respectively. Next to the negative transconductance $-g_{\mathrm{m}}$ required for oscillation, also capacitive as well as harmonic portions can be observed. Due to the even harmonic voltages induced into the tail current nodes V_{PGM} and V_{NGM} of the sustaining amplifier, the harmonic portions are stronger pronounced without blocking capacitors.

Circuit Implementation

For the automatic amplitude control, a circuit has been implemented, which regulates the amplitude of the LCO to have a specified value. Figure 2.15 depicts the simplified circuit of the LCO core including all the sub blocks required for the automatic amplitude control. The biasing is implemented by means of several current mirrors operated at a bias current I_{B} of 500 nA. For a simplification, only the corresponding bias voltages V_{BP} and V_{BN} are shown. For an operation of the sustaining amplifier, a current source is implemented at the positive supply side (VDD) and a voltage source on the negative supply (VSS). A reference voltage

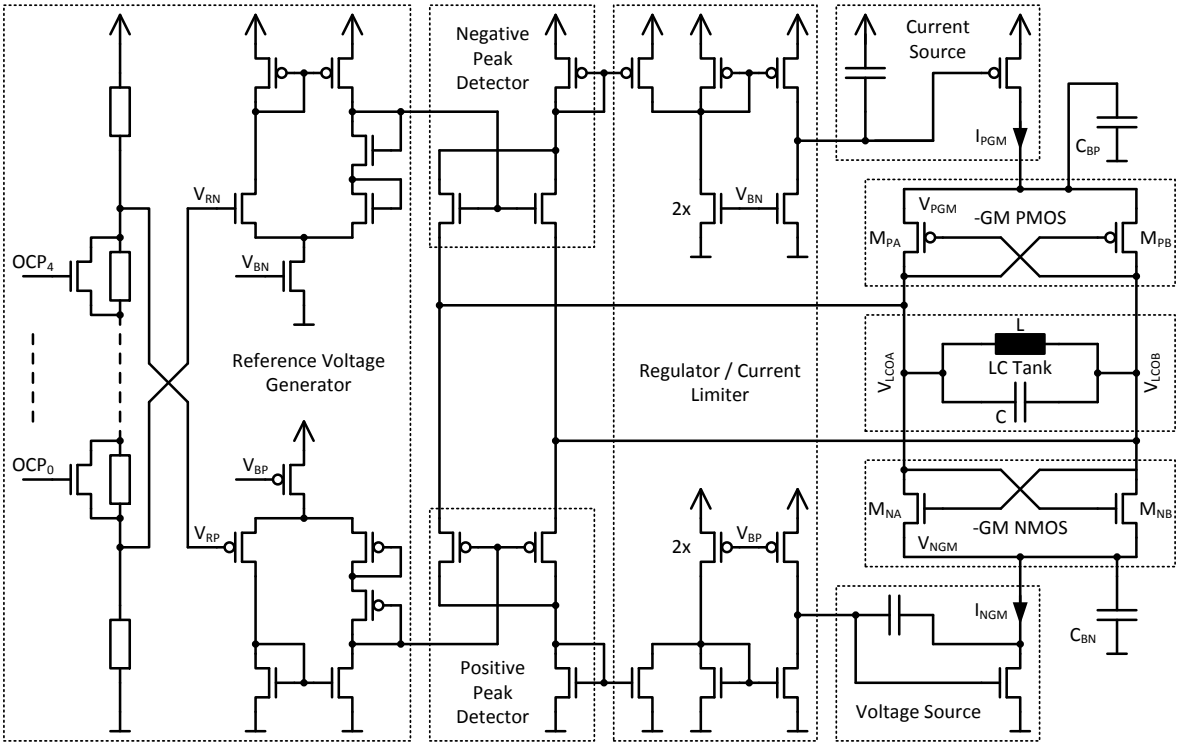

Figure 2.15: LCO core containing of all sub blocks for automatic amplitude control: In contrast to Figure 2.6, this schematic shows a detailed overview of each block. The positive and negative pass devices from Figure 2.6 are implemented as a current and a voltage source, respectively.

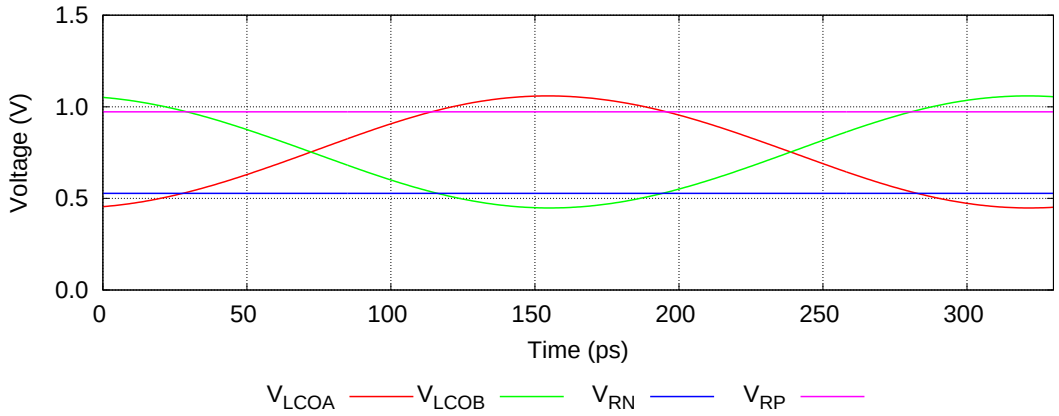

Figure 2.16: Simulated transient LCO and reference voltage signals over one period

generator stage provides two reference voltages V_{RP} and V_{RN}, which are aligned exactly around half the supply voltage. The differential voltage V_{CON} between V_{RP} and V_{RN} is programmable by means of a 5 bit binary code (OCP_4 - OCP_0) corresponding to a range of 0 - 600 mV. In

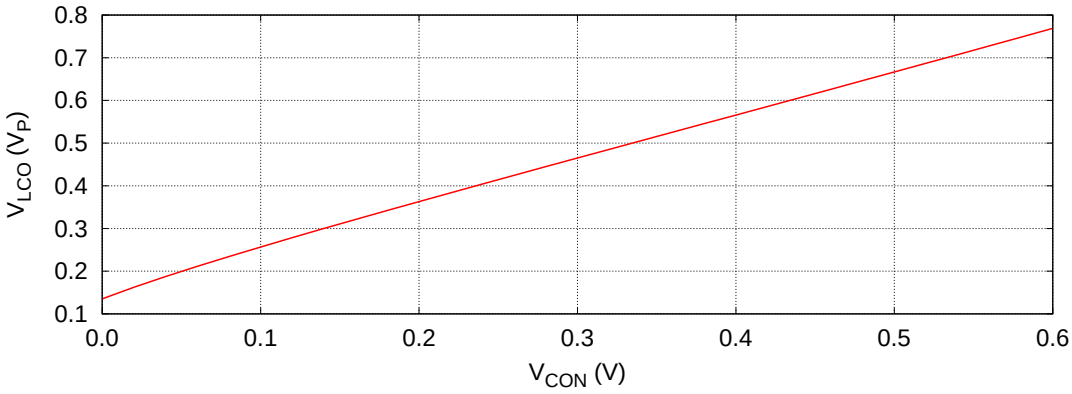

Figure 2.17: Simulated amplitude of the LCO voltage V_{LCO} as a function of the control voltage V_{CON}

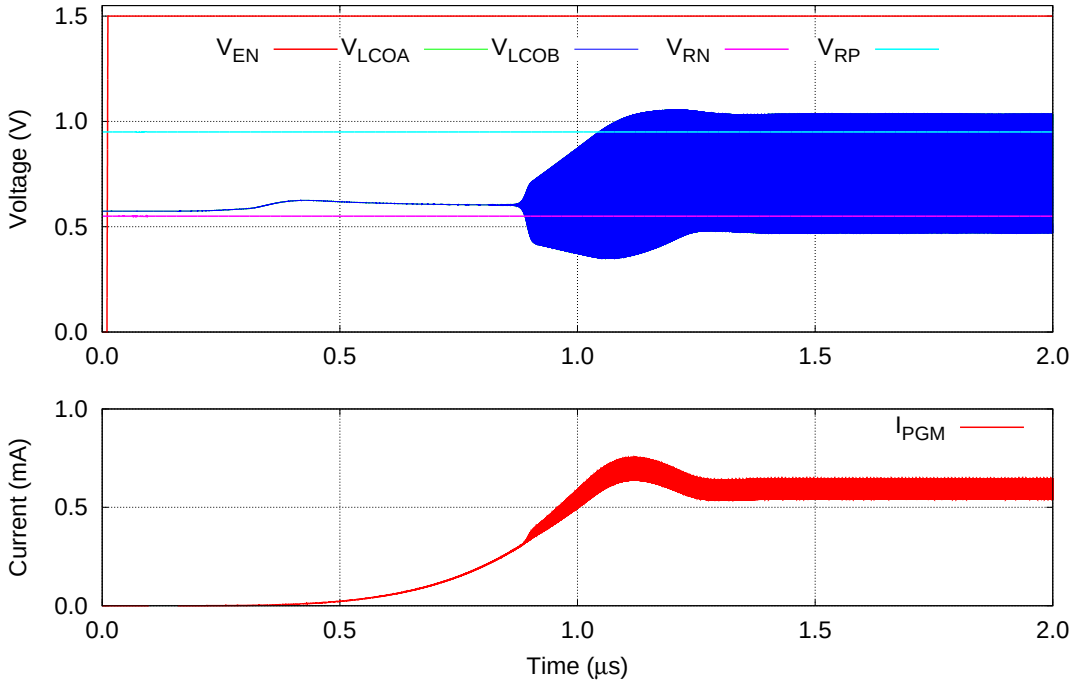

Figure 2.18: Simulated transient signals of the LCO core during start-up

order to regulate the LCO voltages V_{LCOA} and V_{LCOB}, their peak values are sensed by means of a positive and negative peak detector. Therefore, an additional circuit generates two corrected bias voltages using the reference voltages V_{RP} and V_{RN}. This voltages are then used to bias the transistors of the positive and negative peak detector. Those transistors are arranged in a common gate configuration and generate a current that depends on the positive and negative

peak values of the LCO voltages V_{LCOA} and V_{LCOB}. Subsequently, this current is mirrored into a folded current stage, which provides the functionality of a regulator as well as a current limitation to a maximum value of 1 x I_{B}. Finally, the limited output currents are fed into the current source on the VDD side and the voltage source on the VSS side. The regulator adjusts the positive and negative peak values of the LCO voltages V_{LCOA} and V_{LCOB} to equal the corresponding reference voltages V_{RP} and V_{RN}. Figure 2.16 shows the simulated transient voltages of the LCO and the reference voltages. The peak values slightly exceed the reference voltages, which leads to an offset between V_{CON} and the real amplitude of the LCO. Figure 2.17 depicts the amplitude of V_{LCO} as a function of the programmable control voltage V_{CON}. An amplitude for V_{LCO} between 130 - 760 mV is obtained over V_{CON} ranging from 0 - 600 mV. The transient start up of the LCO is depicted in Figure 2.18. The oscillation starts from noise once enough negative transconductance is provided by the sustaining amplifier and is then regulated to the adjusted amplitude. A start-up can be performed within 1.5 µs including the settling of the automatic amplitude control.

2.4.4 Planar Magnetic Shielding

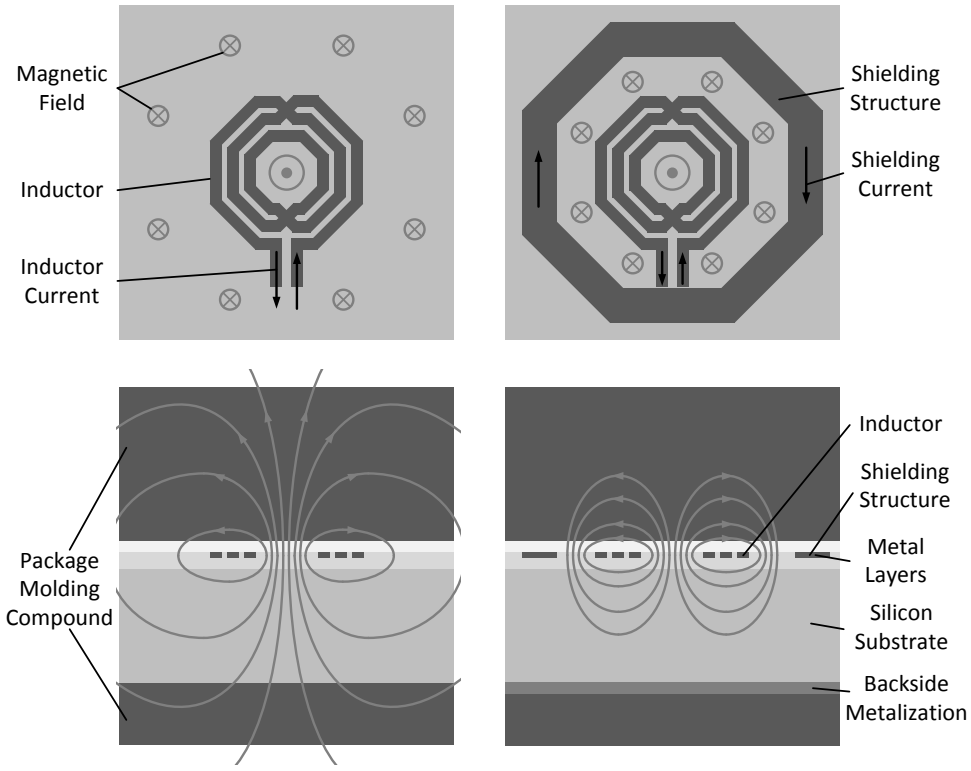

Figure 2.19: Top and cross-sectional schematic view of an unshielded (left) and a shielded (right) integrated inductor and the corresponding magnetic field spread

As elucidated in Sec. 2.2.2, magnetic field interactions of the inductor with its environment can lead to an alteration of the inductance and consequently to frequency errors. An effective shielding measure is thus mandatory for a high frequency accuracy. Figure 2.19 depicts the magnetic field spread for an unshielded integrated inductor. In previous work, two basic ways of environmental shielding for integrated inductors have been reported. In [38], a Faraday shield has been presented, which is post processed on the surface of an integrated LCO. This approach constitutes a very effective solution as it can shield both, the magnetic field and the electric field of the inductor. Moreover, advantages in terms of moisture sensitivity and mechanical stress have been reported. Unfortunately such a shielding option will lead to additional fabrication steps and costs as it is not available in a standard CMOS process. The other possible approach for environmental shielding is the use of a planar magnetic decoupling structure [80]. Such a decoupling structure is typically applied in LCO based VCOs to reduce magnetic coupling with other inductors on the same chip or to reduce the sensitivity to interferences. Similarly, in this work a planar magnetic decoupling structure is used for environmental shielding and consequently for a reduction of environmentally induced LCO frequency errors. A very similar shielding structure is also used in [56]. The implementation of such a shielding structure and the corresponding effects on the magnetic field spread is also depicted in Figure 2.19. The shielding structure consists of a conductive shielding ring which closely surrounds the inductor. It can be implemented in the standard metal stack and requires no additional manufacturing steps. The magnetic field, which is produced by the inductor, induces a counteracting current into the shielding ring. This current produces a magnetic field, which compensates the magnetic field of the inductor outside of the shielding structure. The residual magnetic field is contained in a small region around the inductor. By covering this sensitive region with the molding compound of the standard plastic package, a consistent electric behaviour can be maintained over the lifetime of the device. For the planar magnetic shielding, also the inductor and shielding ring dimensions are of importance as they also affect the magnetic field spread on top of the chip and as a consequence the required plastic package thickness on top of the chip surface. In this work, the inner diameter of the shielding ring amounts to 300 µm. According to measurements in [76], a minimum of 500 µm has been estimated for the required thickness of the plastic on top of the chip surface. The employed standard plastic package DSO-14 exhibits a thickness of 1.1 mm corresponding in a chip covering thickness of 700 µm. On the backside of the chip a shielding effect can be achieved by using a package with a lead-frame underneath the chip or alternatively by an aluminium metallisation [38].

2.4.5 Fractional Interpolating Frequency Divider

In this work, a free-running, non-trimmable LCO is used to provide a fixed frequency from which a variable output frequency can be derived using a fractional interpolating frequency divider. Influences on this fixed frequency given by process variations, temperature, and mechanical stress can be compensated via the fractional dividing ratio. A precise fractional dividing ratio is obtained via a modulated integer N/N+1 divider (N ranging from 1 to 16). The

corresponding phase error is corrected using an accumulator based phase correction logic and a phase interpolator with a high resolution in time of about 10 ps. The required dividing ratio is determined by a compensation logic applying a compensation polynomial for the temperature and stress compensation.

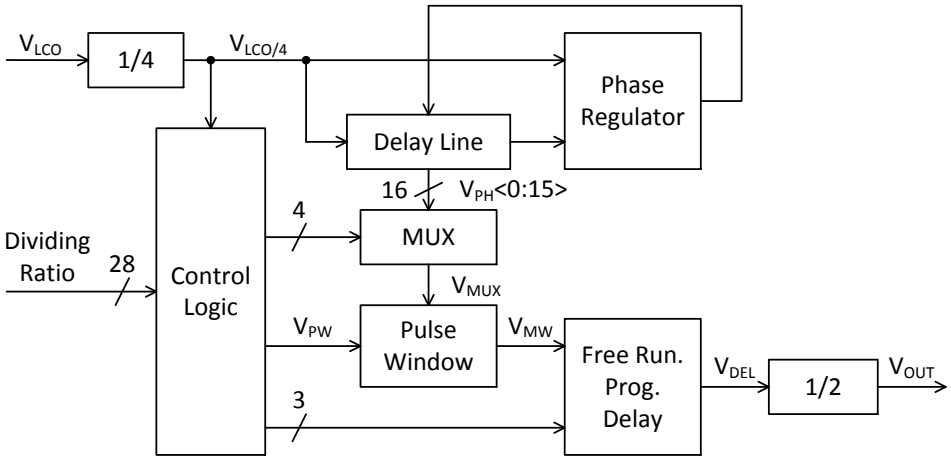

Figure 2.20: Block circuit diagram of the developed low jitter fractional interpolating frequency divider

Figure 2.20 shows the block circuit diagram of the fractional frequency divider. The simulated transient signals are depicted in Figure 2.21 for an LCO frequency of 3.15 GHz and an output frequency of 156.25 MHz. A high speed prescaler divides the differential LCO input signals V_{LCOA}, V_{LCOB} by a ratio of four ($V_{\mathrm{LCO/4}}$) to reduce the power consumption of the subsequent circuitry and to assure a proper operation of the standard logic devices, which are limited in their maximum operating frequency to about 1 GHz. The control logic consists of an integer divider, which is modulated by a phase accumulator for a fractional N/N+1 operation. Higher quantisation in time is achieved by a programmable delay, which is controlled from the seven most significant bits of the phase accumulator. The programmable delay is composed of an accurate multiphase interpolator and an additional free running programmable delay for higher resolution in time. The multiphase interpolator comprises a delay line, which is realised by several consecutive inverters and a phase regulator. An accurate delay time is achieved via the phase regulator by controlling the supply voltage of the inverters. Consequently, the input signal is divided into 16 different phasings (V_{PH} <0:15>) from which one can be selected by the multiplexer (MUX) (V_{MUX}) providing a time resolution of approximately 80 ps. A pulse window signal V_{PW} controlled from the integer divider generates a signal edge V_{MW} with correct phasing. Further scaling to a time resolution of 10 ps is accomplished with an additional programmable free running delay (V_{DEL}), which is matched to the delay line using the control voltage of the phase regulator. Finally, the signal (V_{DEL}) is divided by two to generate a rectangular reference

frequency V_{OUT} with accurate rising and falling edges.

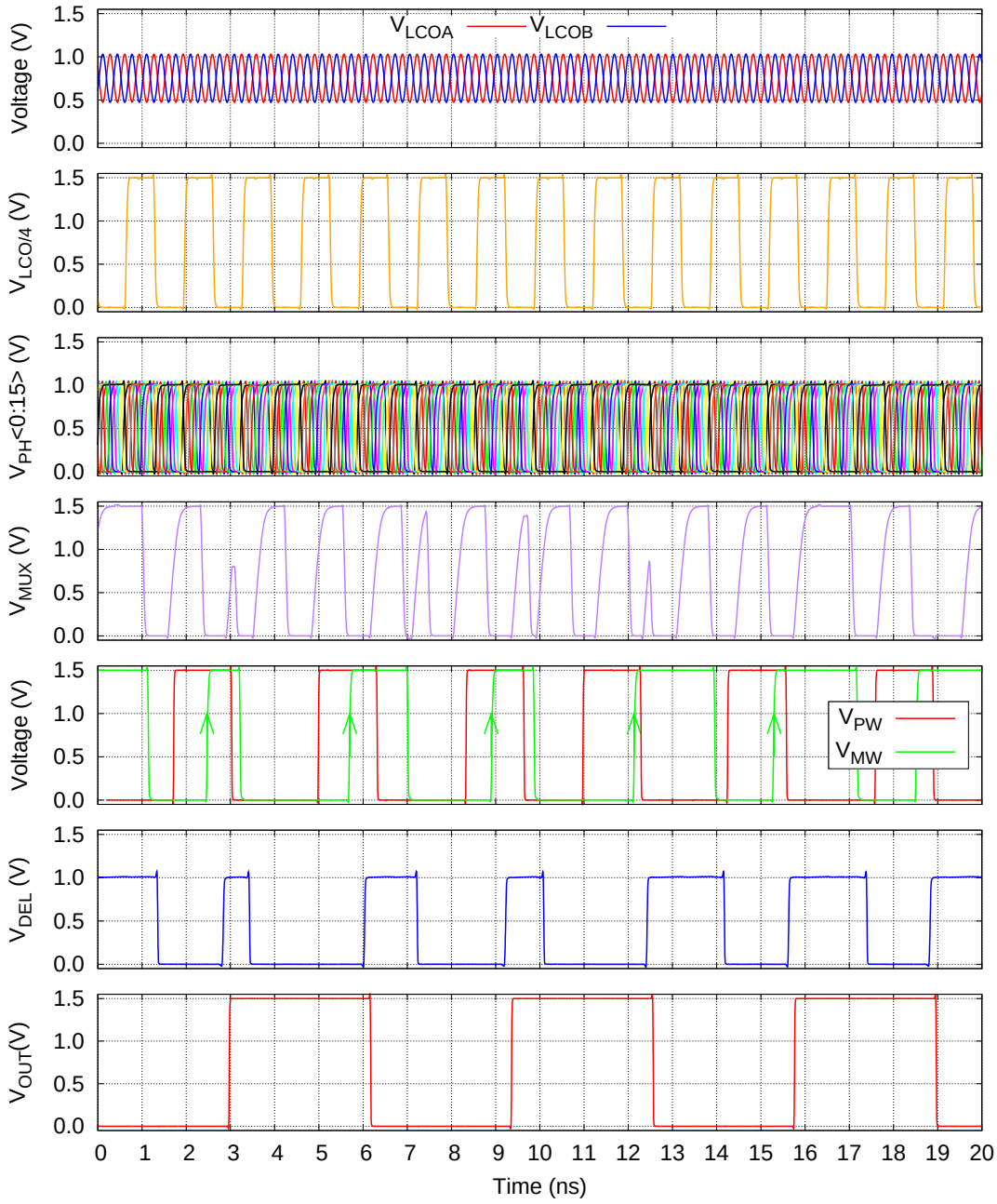

Figure 2.21: Transient signals of the fractional interpolating frequency divider

2.5 Summary

Chapter 2 presents the concept and the design of the all CMOS frequency reference, realised in this work. The ongoing CMOS technology scaling is considered as the enabler for highly stable all CMOS frequency references, explaining the emerging of this technology in resent years. As the transistor length influences the achievable frequency accuracy, this consideration is crucial for the design.

Furthermore, several frequency errors mechanisms are considered including PVT effects, typically relevant in CMOS design. The temperature characteristic is investigated in more detail, illustrating the important relation between the temperature coefficient of the frequency and Q of an integrated LCO. Additionally, several effects of specific interest for all CMOS frequency references are highlighted, including environmental effects related to the device package and humidity, as well as mechanical stress. Mechanical stress effects are considered in more detail with an estimation of the stress-strain induced sensitivity of the LCO frequency to mechanical stress. It is estimated in this work, that mechanical stress is the major cause of frequency errors in state-of-the-art LCO based all CMOS frequency references over lifetime.

Moreover, in Chapter 2, a new approach for an all CMOS frequency reference is presented. In contrast to state-of-the-art architectures, a non-trimmable LCO is used to derive an accurate frequency. Frequency trimming as used in state-of-the-art LCO based all CMOS frequency references, is realised by either using trimming capacitors (varactors) or switched capacitors. Either way, non-linear or low Q components are thereby introduced to the LC tank, degrading the performance and thus the achievable frequency accuracy. Instead of using analog trimming components, in this work, the frequency trimming is performed by means of a fractional frequency divider, shifting the compensation functionality from the analog to the digital side. Consequently, a better robustness of the design can be achieved. However, as a result a more complex overall system is developed, requiring a complex digital logic for frequency generation as well as for the compensation of process (initial calibration), temperature, and mechanical stress effects.

The design of the most important building blocks is described in detail in this chapter. The LCO core, although very simple, is considered the most important block of this work. The design is presented including the LC tank and the arrangement in the available metal stack. Furthermore, the sustaining amplifier is presented including an automatic amplitude control. Automatic amplitude control is required to operate the LCO at the optimal power level for minimised sensitivity to voltage drifts and is thus crucial for a high frequency accuracy. A planar magnetic shielding structure is implemented in this work, cancelling frequency errors which would otherwise be caused by magnetic field spread and coupling effects. Finally, the fractional frequency divider is presented, which is used for the non-trimmable LCO architecture in this work. The fractional frequency divider includes a programmable delay, which facilitates a time interpolation and thus a true fractional operation. As a result, a high time resolution of

10 ps can be achieved, allowing to generate a low jitter output frequency without the need of an additional PLL.

Chapter 3

Chip Architecture and Development

This chapter deals with the different test chips, which have been manufactured during the course of this work. The analog functionality is considered the major challenge for the design in this work. Continuous improvements have been implemented within the analog components with every further test chip, starting with a very simple proof of concept, mostly analog test chip. The final SoC transmitter device has a well-engineered analog core, including a highly accurate temperature sensor, a mechanical stress sensor, and a power amplifier (PA) specifically designed for the need of the CMOS frequency reference architecture. Furthermore, in the final SoC transmitter a complex digital core is implemented, which provides all the digital functionality that is required for an operation as a wireless transmitter or a single chip frequency reference (the digital design has not been perfomed as part of this work).

3.1 Analog Test Chip

The aim of the first test chip was to proof the concept of an all CMOS frequency reference based on a non-trimmable LCO with a manageable design effort. For that reason, an analog test chip has been manufactured, which was mostly focused on the critical analog functionality. The required digital functionality is intended to be performed by an external microcontroller. However, a high number of digital control signals (more than 200) are required. In order to reduce the number of required external pins, a serial peripheral interface (SPI) is implemented on the analog test chip. Later, two additional redesigned versions of the analog test chip have been manufactured, including several design improvements as well as a process sensor to get insights into the relation between process variations and chip behaviour.

3.1.1 Architecture

Figure 3.1 depicts the architecture of the analog test chip in combination with an external microcontroller. The analog test chip includes the non-trimmable LCO as well as the fractional frequency divider described in Sec. 2.3 and Sec. 2.4.5, respectively. Using these building blocks, an output frequency can be generated, which ranges up to about 180 MHz. In order to provide

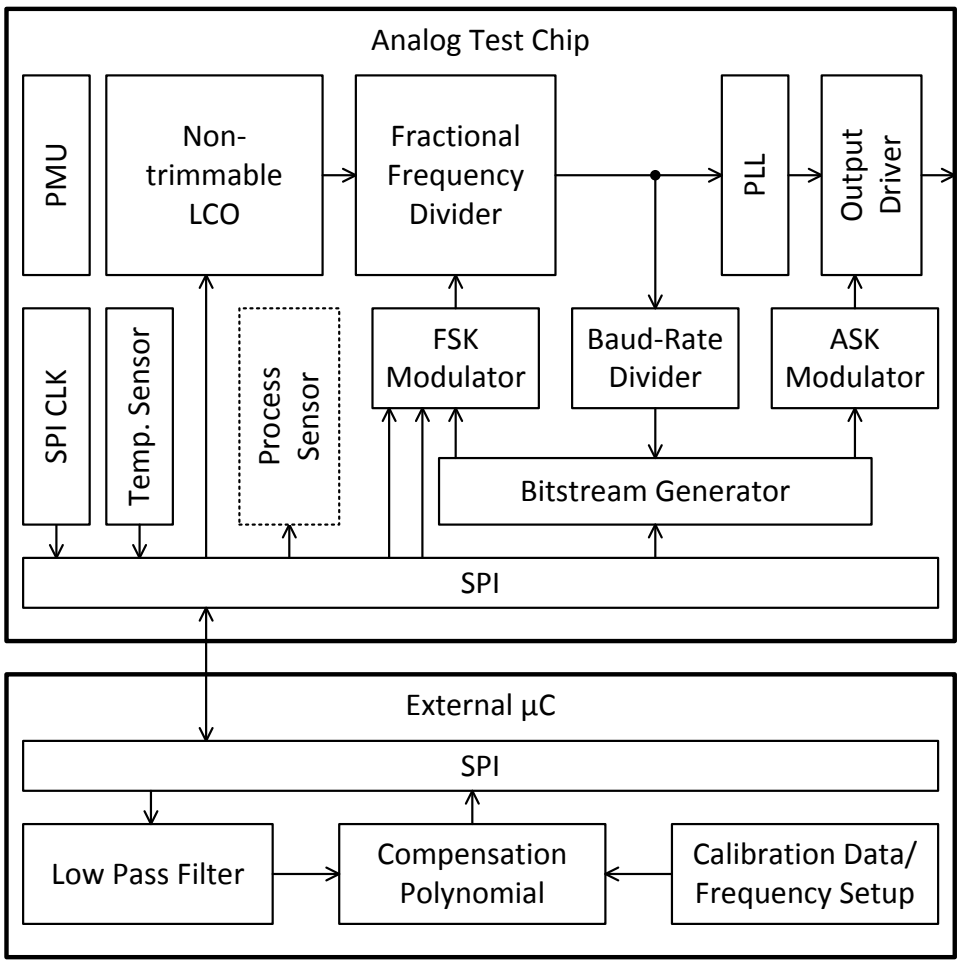

Figure 3.1: Simplified block diagram of the first analog test chip (the two redesigned versions of this analog test chip are also based on this simplified diagram): The devices are implemented as mostly analog test chips, containing an SPI as the only synthesized digital logic. An external microcontroller is required for operation, performing temperature compensation and configuration.

even higher frequencies, a PLL is implemented, which can be used to scale the output frequency of the fractional divider by a variable value to the power of two up to a maximum frequency of about 3 GHz. For the output driver, a simple CMOS push-pull stage is implemented, suitable for single ended and differential operation. Very short transistors with a channel length of 150 nm are used in the output driver to enable an operation at 3 GHz. A temperature sensor is also implemented for the compensation of the LCO temperature characteristic. The temperature sensor is realised using a pn-junction to create a temperature depending voltage. This voltage is measured using a successive approximation register (SAR) ADC with a temperature independent bandgap voltage used as the reference. In order to operate the analog test chip as a wireless transmitter, a simple bitstream generator is implemented using the analog design flow. It can

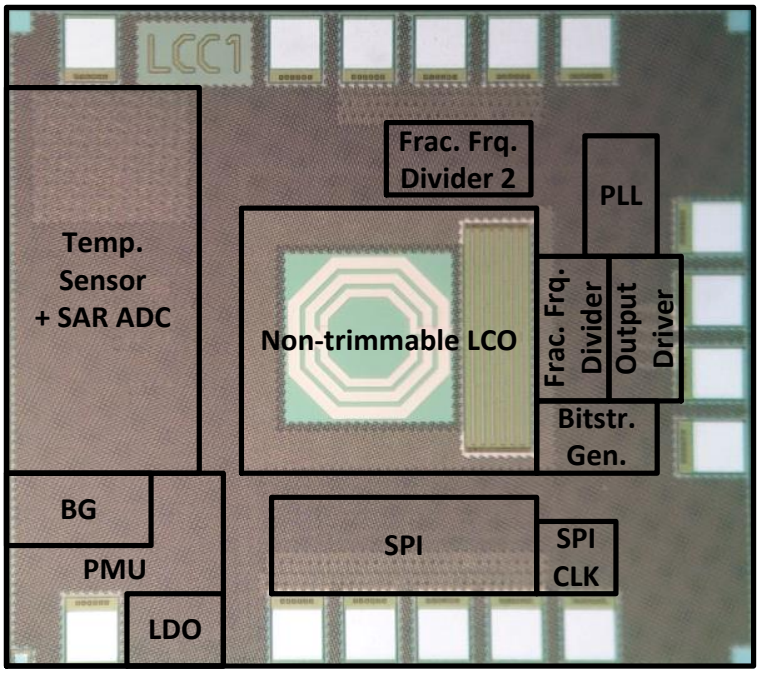

Figure 3.2: Chip photography of the analog test chip showing the location of the most important blocks: The chip has an area size of 0.8 mm by 0.9 mm and is manufactured in a 130 nm standard CMOS process.

generate sequences of up to 64 bits using non-return-to-zero (NRZ) or Manchester coding. The generated bitstream is used to switch the dividing ratio between two predefined values for frequency shift keying (FSK) modulation. For an amplitude shift keying (ASK) modulation, the output driver which functions as the PA is simply turned on and off. An accurate baud-rate is derived from the output frequency of the fractional divider using an integer divider. The available baud-rate resolution is thus limited depending on the dividing ratio. The analog test chip also includes a power management unit (PMU) with a bandgap voltage reference and several LDO voltage regulators. A minimum operation current of 1 µA can be achieved with all components turned off except of the SPI and the SPI clock.

The external microcontroller is connected to the analog test chip by the SPI, allowing a bidirectional data transmission with only four wires. The SPI is used for configuring and controlling the analog test chip. However, the fundamental task of the microcontroller is to perform the temperature compensation. For that reason, the temperature value is read by the external microcontroller. In a first processing step, the temperature value is low pass filtered using an infinite impulse response (digital filter) (IIR) low pass filter, realised as software of the microcontroller. This step is required to reduce noise, which would otherwise lead to phase noise at the output frequency of the analog test chip. As a further processing step, a temperature compensated raw value for the dividing ratio is calculated using a polynomial. The coefficients of the polynomial are considered as the calibration data of the analog test chip. They must be

determined for every analog test chip separately and are stored in the external microcontroller. The raw value of the dividing ratio is subsequently multiplied with the frequency setup value, which constitutes the configuration value for the desired frequency. Finally, the correct dividing ratio is written into the analog test chip, which then generates the desired output frequency, independently of temperature effects and process variations.

Figure 3.2 depicts the chip photography of the analog test chip as well as the location of the most important blocks. The LCO can be clearly seen in the centre of the analog test chip with its shielding ring closely surrounding the inductor. Although occupying a considerable portion of the chip area, the shielding ring is required in order to reduce interferences and magnetic coupling to the environment (see Sec. 2.4.4). A placement of the temperature sensor closely to the LCO is advantageous to reduce temperature differences due to heat dissipation and the corresponding temperature gradients. As the fractional frequency divider is considered a particularly critical block, a second instance is placed on the chip (see Figure 3.2, Frac. Frq. Divider 2), which can be operated with an external input frequency for test purposes.

3.1.2 Packaging

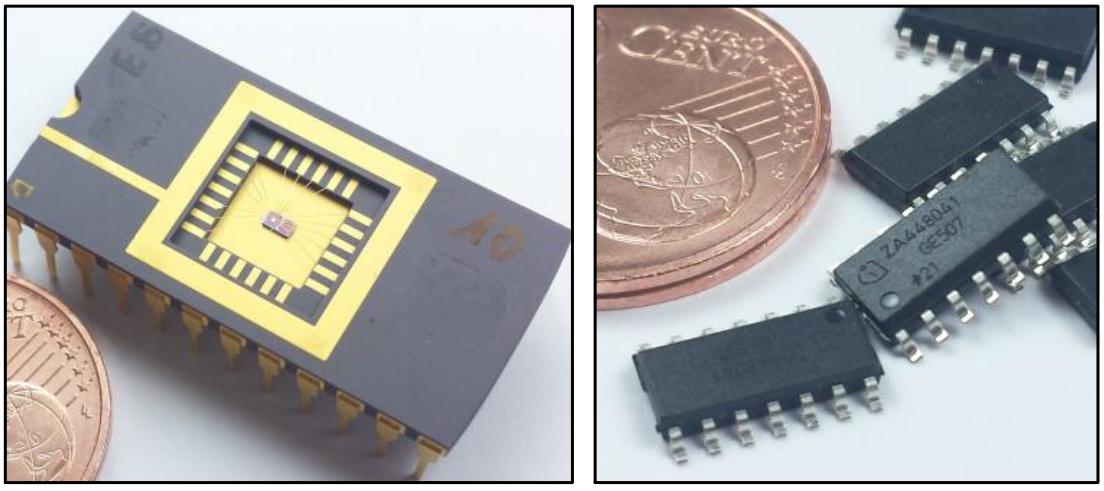

Figure 3.3: The left picture shows the analog test chip in an open ceramic package. Difficulties with contamination of the chip surface by water, freeze over, and dust lead to the need of a plastic package. The right picture shows the analog test chip packaged in a standard DSO-14 plastic package.

Devices for test and research purposes are typically tested in ceramic packages to reduce packaging costs. The analog test chip was therefore also first packaged in a ceramic package for functional tests. As known already, the LCO frequency reference is extremely sensitive to its close environment. Any contamination of the chip surface leads to a change of the LCO frequency caused by electric or magnetic interactions. Even a thin film of water, attributable

to condensation or freeze over constitutes a considerable problem. In order to avoid this environmental effects, the analog test chip has later been packaged in a standard DSO-14 plastic package. Using a plastic package, the chip surface is covered with the package mold compound, thus assuring a consistent electric behaviour of the close LCO environment. Figure 3.3 depicts the analog test chip packaged in the ceramic and in the DSO-14 plastic package.

3.1.3 Progression and Insights

After the thorough evaluation of the first analog test chip, the major building blocks have been found to be functioning. The first analog test chip thus helped gathering lots of measurement results and insights of the LCO based frequency generation technology.

However, also several design issues as well as deviations from the previous simulation results have been revealed. The measured temperature coefficient of the LCO frequency has been found to be higher than expected from the simulation results. This fact is attributable to the lower Q of the manufactured inductor in comparison to the simulation model. Additionally, a deviation of the temperature curve shape has been found for the measured LCO frequency with respect to the simulation model. It is assumed, that the cause of this deviation is the non-linearity of the temperature coefficient of the metal layers used for the inductor. Due to the SAR ADC architecture, a limited resolution and linearity as well as noise has been found for the temperature sensor. This issue has been resolved by using a very low cut-off frequency for the subsequent low pass filter. Due to the low cut-off frequency and the high amount of noise, only a poor performance has been achieved with a limited accuracy and a long response time to a change of temperature. Another design issue has been found with the frequency divider, which stopped working for temperatures higher than about 120 °C.

Two different redesigned analog test chip versions have been manufactured as successors of the first analog test chip. Despite several modifications, the basic architecture as well as the layout floor plan were taken over from the first analog test chip, in order to avoid a complete redesign of the layout. One major focus of the redesigned analog test chips has been to improve the Q of the LC tank. For that reason, the inductor has been extended by adding the aluminium top layer as an additional layer for a better overall conductivity. Additionally, the distance of the inductor shielding structure has been increased, which also leads to an improved Q. The frequency divider of the first analog test chip has been replaced in one version of the two redesigned analog test chips with an improved design, which works reliably up to 150 °C and also has a slightly reduced power consumption. Furthermore, a process sensor has been implemented including resistors, consisting of the metal layers which are used in the inductor. In order to gain insights into possible correlations of process variations and the LCO temperature characteristic, also diode connected transistors are available for NMOS and PMOS transistor types, exhibiting the same dimensions and orientation than the transistors used in the sustaining amplifier. In order to determine the influence of the chip coating on the moisture sensitivity, two different

coatings (polyamide and passivation) have been used for manufacturing. The redesigned analog test chips have been packaged in ceramic and in the DSO-14 plastic package in the same way as the first analog test chip.

3.1.4 Crystal-less Demonstrators

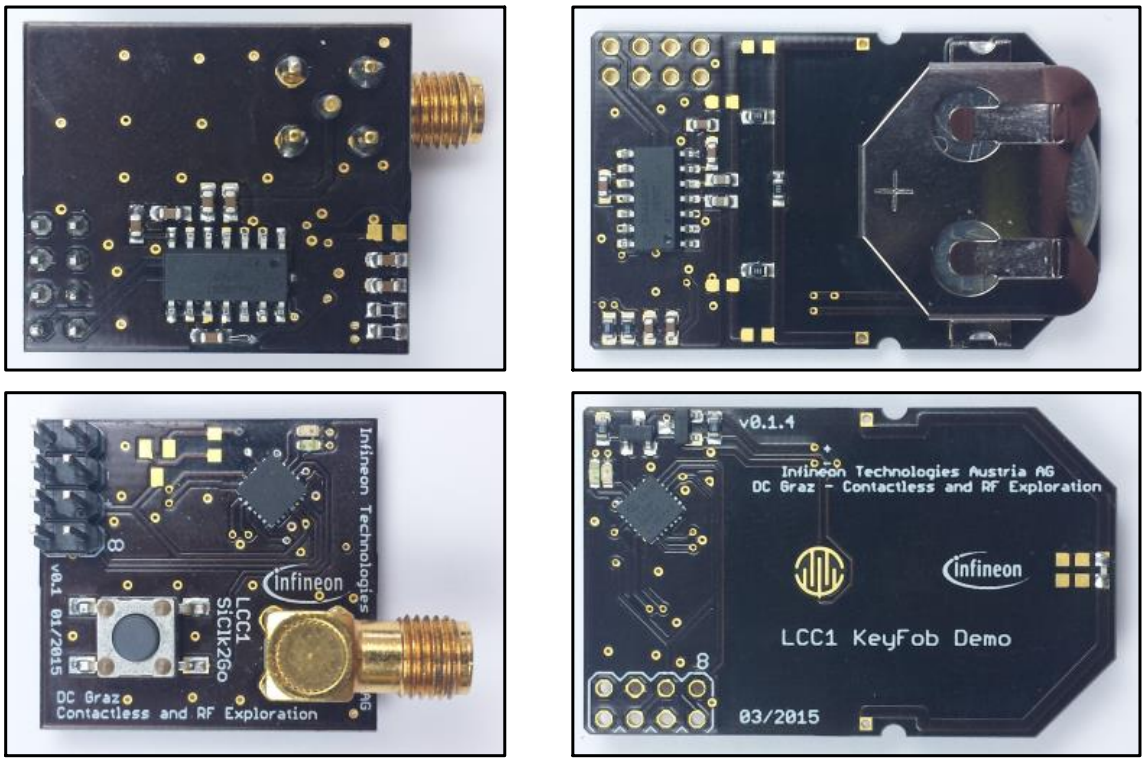

Figure 3.4: Demonstrators realised with the analog test chip. The left pictures show the top and the bottom side of a crystal-less frequency reference demonstrator. The right pictures show the top and the bottom side of a wireless key fob demonstrator. Both demonstrators employ the analog test chip, depicted in the top figures, as well as a microcontroller (XMC1100) depicted in the bottom figures.

Figure 3.4 depicts two demonstrators, which have been realised with the analog test chip. The first demonstrator that has been realised, represents a crystal-less frequency reference using the analog test chip and Infineons XMC1100 [81] as the external microcontroller. It is intended to demonstrate that crystal replacement is viable in applications with relaxed frequency accuracy requirements of about 250 ppm. The output frequency can be programmed arbitrarily between 1 MHz and 180 MHz.

The second demonstrator has been realised as a wireless transmitter in the form of a wireless

key fob. It also requires the XMC1100 as an external microcontroller due to the mostly analog architecture of the analog test chip. Additionally, some discrete components (MOSFETs and resistors) are required for the power management, as the XMC1100 cannot be configured to a sleep mode that is sufficiently low in power consumption for a battery powered device. Apart from this, the key fob has been realised with a minimum number of external components using a PCB antenna, which includes mandatory components as a balanced-unbalanced (balun) and a matching circuit. The key fob has been designed for an operating frequency of 433.92 MHz, which is a common frequency for such an application. A transmit power of 3 dBm has been achieved with a maximum supply current of 20 mA. The baud-rate has been adjusted to 5 kbps, using ASK modulation and Manchester coding. Using this configuration, compatibility has been demonstrated with the state-of-the-art transceiver TDA5340 [23]. Compatibility has also been shown for different baud-rates using ASK and FSK modulation at 315 MHz, 433 MHz, and 868 MHz. Although a functioning reception of the modulated carrier signal from the analog test chip has been shown, considerable out-of-band emissions have been observed. This comes from the fact that for ASK as well as for FSK only a harsh modulation is available, realised by simply turning the PA on and off for ASK and by switching between two frequencies for FSK.

3.2 SoC Transmitter

A further development of the analog test chip has led to a fully integrated SoC crystal-less wireless transmitter. The analog architecture is mostly based on the previous analog test chip. Next to the building blocks already implemented in the analog test chip, new analog components are implemented comprising of a highly accurate sigma delta temperature sensor as well as a mechanical stress sensor. The most important enhancement, however, is the complex digital core implemented to replace the external microcontroller, which was required for the operation of the analog test chip. Using this digital core, the SoC transmitter can be operated either as a crystal-less wireless transmitter or a single chip frequency reference.

3.2.1 Architecture

Figure 3.5 depicts the simplified block diagram of the SoC transmitter architecture. The block diagramm is separated into three different blocks including the analog core, the digital core, as well as the output stages.

Analog Core

Similar to the analog test chip, the SoC transmitter includes the non-trimmable LCO as well as the fractional frequency divider described in Sec. 2.3 and Sec. 2.4.5. With this configuration,

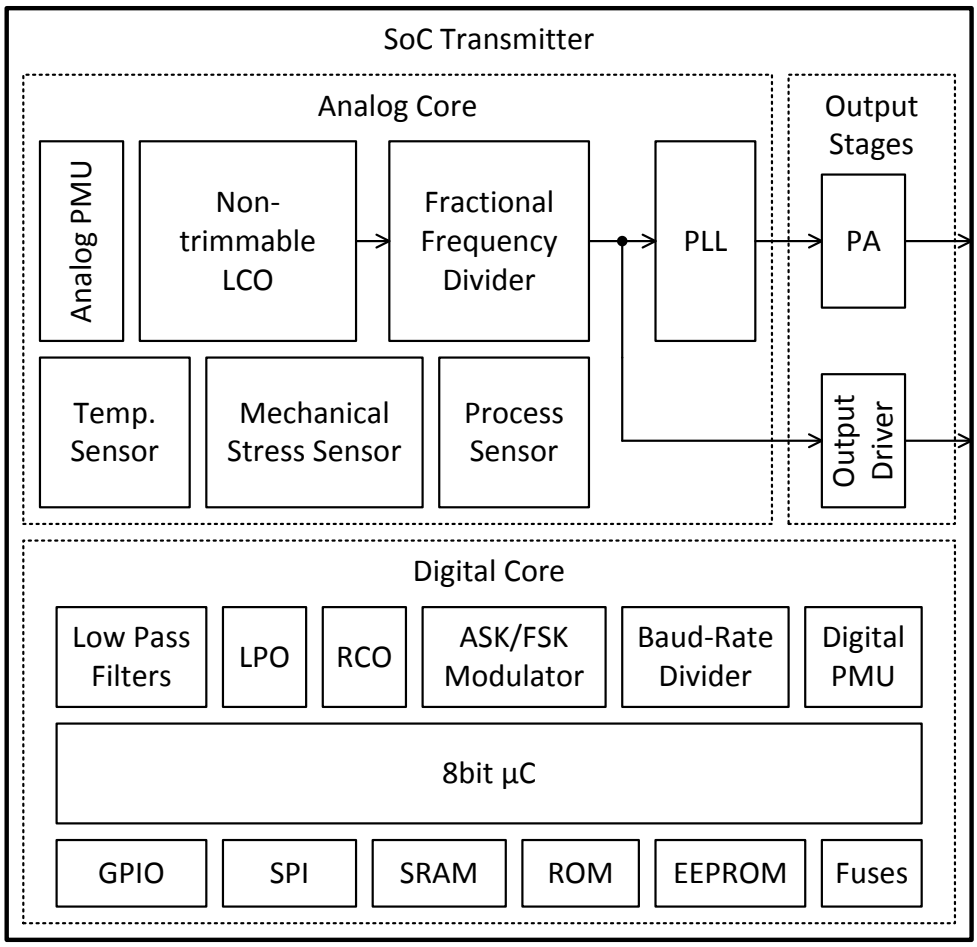

Figure 3.5: Simplified block diagram of the SoC transmitter: The device constitutes a SoC crystal-less wireless transmitter or a single chip clock source with a minimum number of required external components.

an output frequency ranging from 3 MHz to 180 MHz can be generated for an operation as a clock source. Additionally, a PLL is implemented, which allows scaling the output frequency of the fractional frequency divider by a value variable to the power of two. Using the PLL, a frequency in the range of 10 MHz to 1 GHz can be provided for a sub-GHz wireless transmitter operation. The analog core of the SoC transmitter furthermore comprises an analog PMU including a band-gap reference and several LDOs for the respective analog building blocks, a highly accurate temperature sensor, and a mechanical stress sensor. The most important analog blocks are in the following described in more detail in Sec. 3.2.2 to 3.2.5.

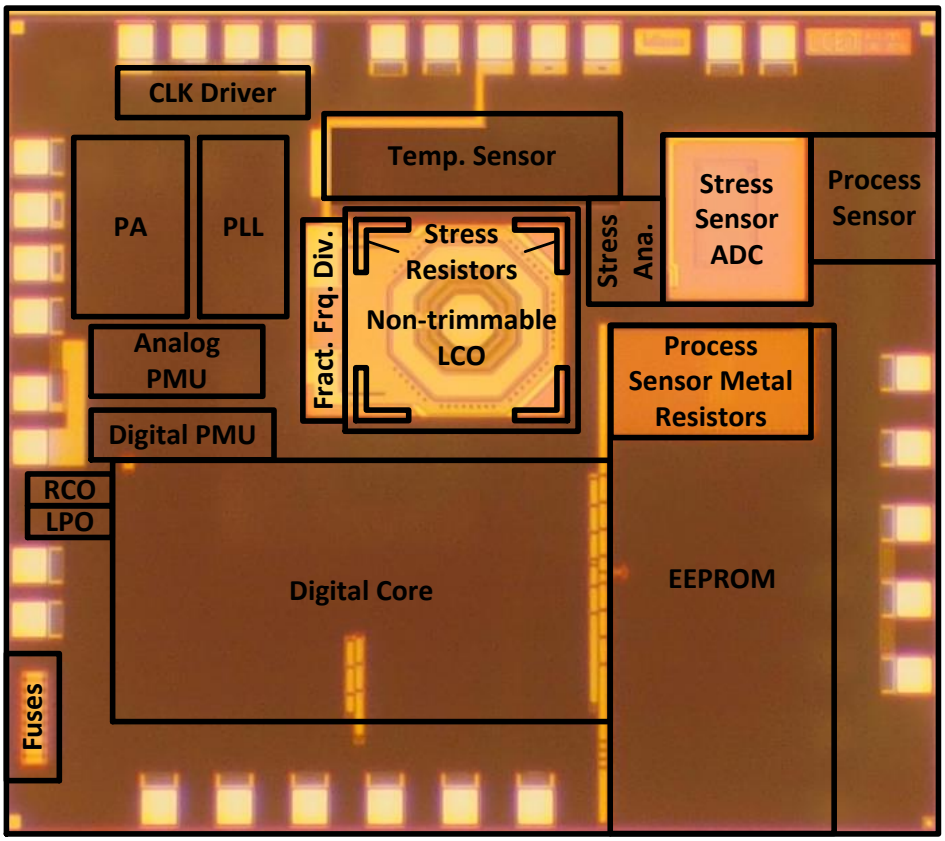

Figure 3.6: Chip photography of the SoC transmitter showing the location of the most important blocks: The chip has a size of 1.725 mm by 1.5 mm and is manufactured in a 130 nm standard CMOS process with EEPROM option. The components of the mechanical stress sensor are separated into the stress resistors, the analog circuitry (stress ana.) and the stress sensor ADC. Furthermore, the metal resistors of the process sensor are indicated.

Digital Core

The digital core of the SoC transmitter is based on an 8 bit microcontroller. It is designed to provide all the digital functionality required for temperature compensation as well as for the frequency generation and modulation for which the analog test chip required an external microcontroller. It is clocked by either a 70 kHz low power oscillator (LPO) or a 24 MHz RCO. Specific digital hardware is implemented for filtering and processing of the measured temperature as well as for the modulation in the wireless transmitter operation mode. The temperature and stress compensation is performed by means of a compensation polynomial, which is implemented as part of the firmware. For the data transmission, the digital hardware includes an ASK/FSK modulator. It supports sloping as well as Gaussian shaped transitions for NRZ and Manchester coding. FSK modulation is performed by altering the dividing ratio

of the fractional frequency divider. The high reconfiguration rate of the fractional frequency divider allows to operate at a high baud-rate of up to 500 kbps. For ASK modulation a fixed carrier frequency is used and the modulation is performed by altering the tail current of the PA (see Sec. 3.2.5). The output frequency of the fractional frequency divider, which is used as the reference frequency of the PLL is also used to derive the baud-rate by means of a baud-rate divider. The baud-rate divider uses a fractional-n architecture to generate a variable baud-rate. By this means, an accurate baud-rate can be generated with a high resolution better than 0.05 %. A read-only memory (ROM) is also implemented, including precast firmware-functions for start-up as well as the polynomial calculations required for temperature and stress compensation. Furthermore, an electrically erasable programmable read-only memory (EEPROM) is implemented for an application specific firmware as well as for the calibration data. After a reset, the application specific firmware is loaded into a dedicated address range of the static random-access memory (SRAM) from where it is subsequently executed. The calibration data including the configuration setup as well as coefficients for the compensation polynomials are also loaded into the respective special function register (SFR) as part of the start-up routine.

Output Stages

In the SoC transmitter, two different output stages are available comprising an output driver and a PA. The output driver is implemented as a CMOS push-pull stage for single ended or differential mode operation. It can be used to operate the SoC transmitter as a frequency reference for quartz crystal replacement. The PA is implemented for the operation as a wireless transmitter in the sub-GHz range.

Layout Design

Observations and measurements from the previous analog test chip revealed several critical effects, which must be considered in the layout design. The output stages can produce a considerable amount of harmonics resulting in interferences due to electromagnetic coupling. Additionally, the digital core produces distortions. In order to minimise interferences, the supply domains have been separated for the analog core, the digital core, as well as the PA and the output driver. Furthermore, temperature gradients caused by local heat dissipation can lead to considerable temperature differences across the chip. For an accurate temperature compensation the unaltered temperature must be measured for the non-trimmable LCO. The temperature sensor is thus placed close to the non-trimmable LCO, while the major heat dissipaters, including the PA as well as the analog and digital PMU, are placed distantly. Figure 3.6 depicts the chip photography of the SoC transmitter indicating the most important blocks.

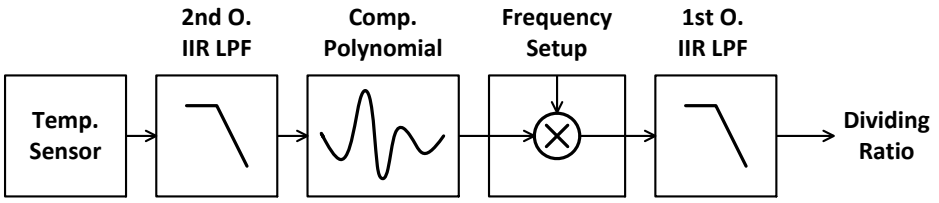

Figure 3.7: Simplified block diagram of the signal processing chain for the temperature compensation, comprising the sigma delta temperature sensor followed by the second order digital low pass filter (LPF), the compensation polynomial, and the frequency setup (realised via firmware) to provide the correct dividing ratio. The second LPF stage is implemented to provide an overall third order low pass behaviour.

3.2.2 Temperature Sensor

In order to obtain an accurate reference frequency, a temperature compensation is required. A temperature sensor has therefore already been implemented in the analog test chip. However, only a poor performance has been achieved with this temperature sensor, which limits the overall frequency accuracy of this device.

In order to achieve a better performance, a highly accurate temperature sensor is implemented on the SoC transmitter. This temperature sensor has not been designed as part of this work but was taken over as a complete IP block. It uses an architecture similar to [82]. Two substrate PNP transistors biased with different current densities are used to generate a voltage that is proportional to absolute temperature (PTAT) as well as a temperature independent bandgap voltage V_{BG}. A digital temperature value is generated by converting the PTAT voltage via a second order sigma delta ADC, while the voltage V_{BG} is used as the reference.

Figure 3.7 depicts a simplified block diagram of the signal processing chain for the temperature compensation. For further processing of the temperature, the 1 bit ADC output signal of the temperature sensor (Temp. Sensor) is low pass filtered using a second order digital IIR filter (2nd O. IIR LPF). While this digital value can be used to compensate the temperature characteristic of the LCO, any overlaying noise leads to a modulation of the frequency and as a consequence to phase noise. This effect is particularly critical as the above mentioned sigma delta ADC produces a high amount of quantization noise. The cut-off frequency of the second order IIR filter must thus be chosen accordingly low. Measurement results show that up to a cut-off frequency of 400 Hz, the phase noise due to quantization noise is lower than the phase noise produced by the LCO, and consequently no degradation occurs. While a 400 Hz cut-off frequency corresponds in a sufficiently fast temperature response, the initial settling time after turning the device on will correspond in an unnecessarily long start-up latency of up to 20 ms. To overcome this issue, the second order IIR filter is implemented with a variable

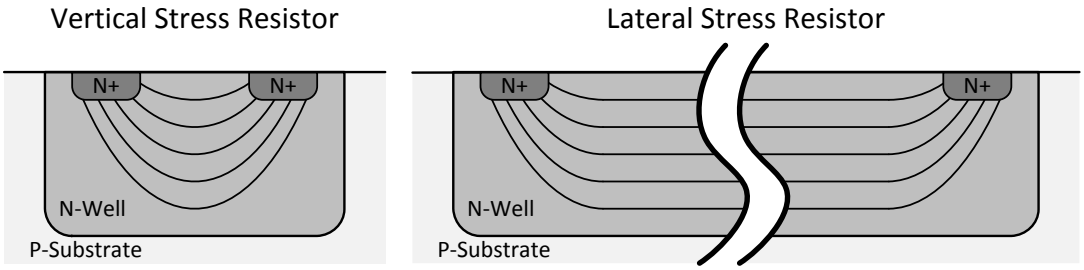

Figure 3.8: Cross section of n-well stress resistors (schematic): Lines of constant current density are sketched. A maximal vertical current flow is achieved using short n-wells of whom several are connected in series to form the vertical stress resistors. Long n-wells are used as lateral stress resistors.

cut-off frequency. In the first few milliseconds, the filter is adjusted to a high cut-off frequency of 3.2 kHz to achieve a fast settling time and is then switched to 400 Hz before the LCO is turned on. This implementation leads to a fast start-up within 5 ms, while not degrading the phase noise performance.

Theoretical considerations as well as a previous publication [5] imply that the LCO has a distinct second order temperature behaviour (see Sec. 2.2.1). Higher order effects also occur, but are less pronounced. A forth order polynomial has thus been implemented as part of the firmware, which is applied to the output signal of the first LPF stage. The compensated value constitutes a raw dividing ratio for a temperature-independent frequency. This value is subsequently multiplied with a frequency setup value to obtain the correct dividing ratio for the desired operating frequency. The frequency setup value is a digital value referable to a period time, as a multiplication is easier to implement than a division in the implemented microcontroller. Finally, the dividing ratio is low pass filtered with a further digital IIR filter (1st O. IIR LPF) to achieve a third order overall low pass characteristic.

3.2.3 Mechanical Stress Sensor

As elucidated in Sec. 2.2.3, a sensitivity of the LCO frequency to mechanical stress is expected for an LCO based frequency reference. In order to investigate the relation between mechanical stress and the LCO frequency, a mechanical stress sensor has been implemented on the SoC transmitter. The mechanical stress sensor is implemented using n-wells as piezo-resistive stress resistors. Two types of stress resistors are implemented with different current flow directions resulting in different piezo coefficients. Short n-well resistors are used to achieved an arc-shaped current flow leading to a high portion of current flow in the vertical direction of the chip. To form the vertical stress resistors R_{V} several of these short n-wells are connected in series. The lateral stress resistors R_{L} are realised using long n-wells corresponding in a mostly lateral current flow. Figure 3.8 depicts the cross section and the lines of constant current density of the two stress resistors implemented in the 130 nm standard CMOS process.

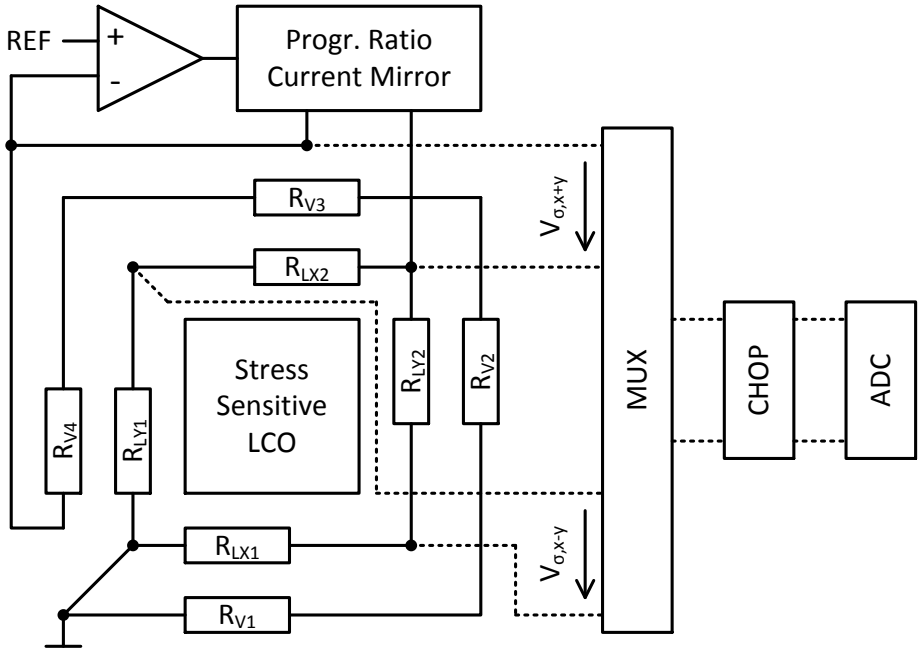

Figure 3.9: Stress sensor configuration: The lateral stress resistors R_{L} are arranged in a bridge configuration using the vertical stress resistors R_{V} as the reference. As a result, in-plane stress can be measured in x and y direction using only a single trimmed current mirror.

In order to determine the mechanical stress, the ratio between the vertical and the lateral stress resistors is measured. Therefore, the stress resistors are symmetrically arranged around the LCO according to Figure 3.9. As shown in Figure 3.6, a lateral and a vertical stress resistor is located at every corner of the LCO with x and y alignment, respectively (only two corners are shown in Figure 3.9). The vertical stress resistors are connected in series with a sensitivity to the sum of the in-plane stress $\sigma_{\mathrm{x+y}}$. The lateral stress resistors are implementation as a bridge. In order to measure the in-plane sum stress $\sigma_{\mathrm{x+y}}$, two coupled current sources are connected to the vertical and to the lateral stress resistors in order to transform the resistor ratio into the voltage $V_{\sigma,\mathrm{x+y}}$. Furthermore, the in-plane difference stress $\sigma_{\mathrm{x\text{-}y}}$ can be measured as the transverse voltage $V_{\sigma,\mathrm{x\text{-}y}}$ of the lateral stress sensor bridge. The voltage across the vertical stress resistors is regulated to a reference voltage V_{REF} for a defined sensitivity and also to account for non-linearities of the n-well resistors. The ratio of the two current sources can be trimmed to account for variations of the stress resistors. The two voltages $V_{\sigma,\mathrm{x+y}}$ and $V_{\sigma,\mathrm{x\text{-}y}}$ are converted into digital stress values using a MUX and an ADC. An additional chopping switch (CHOP) is used to reduce offset errors. As the same n-wells are used for the lateral and the vertical stress resistors, only a small difference between the temperature coefficients is present. Nevertheless, a temperature compensation is required for the ADC raw value of $\sigma_{\mathrm{x+y}}$ in order to obtain a temperature independent value for the sum stress. The digital value for $\sigma_{\mathrm{x+y}}$ can be used to compensate parameters with equal sensitivity to in-plane stress in x and y

direction. Furthermore, the digital value for $\sigma_{\text{x-y}}$ can be used to account for any differences of the sensitivity in x and y direction.

3.2.4 Ring Oscillator PLL

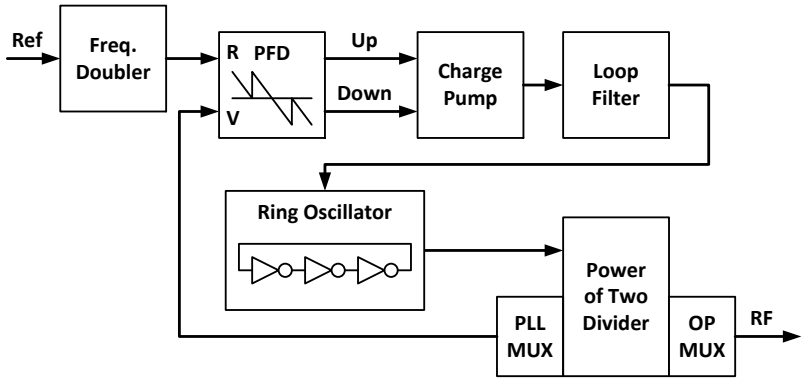

Figure 3.10: Block circuit diagram of the ring-oscillator PLL: The ring-oscillator frequency can be variably divided in power of two steps via the PLL MUX and the OP MUX to provide the PLL feedback and the RF signal within a wide frequency range.

The PLL is used to enable generating higher frequencies to cover the whole sub-GHz frequency range (see Figure 3.5, PLL), as the output frequency of the fractional divider is limited to 180 MHz. Figure 3.10 depicts the block circuit diagram of the PLL. The PLL comprises a frequency doubler at its input allowing operation at an effective reference frequency of up to 360 MHz. A fast phase frequency detector (PFD) is realised with a minimum turn on time of 300 ps to avoid dead zone errors. For a variable loop characteristic, a charge pump is implemented offering an adjustable current as well as a loop filter with a widely configurable loop bandwidth. The VCO in this PLL is realised by means of a ring oscillator. A PMOS transistor is used to convert the output voltage of the loop filter into the supply current of the ring oscillator. The VCO is followed by a power of two scalable frequency divider, which is used to generate the scaled PLL feedback frequency as well as the desired RF output frequency via the PLL multiplexer (PLL MUX) and the output multiplexer (OP MUX), respectively. The ring oscillator is designed for an operating frequency range of 1.3 GHz - 2.6 GHz and for a current consumption of about 1 mA at an operating frequency of 1.736 GHz for a divided output frequency of 868 MHz. Using a ring oscillator as the VCO comes with the advantage of a small chip area occupation and unlike LCO based VCOs with a low sensitivity to magnetic interactions. The phase noise of a ring oscillator is substantially worse in comparison with an LCO at low offset frequencies, while the phase noise at high offset frequencies can be sufficiently low for sub-GHz applications. Accordingly, the PLL must be operated with a high loop bandwidth.

3.2.5 Low Harmonic Distortion Power Amplifier

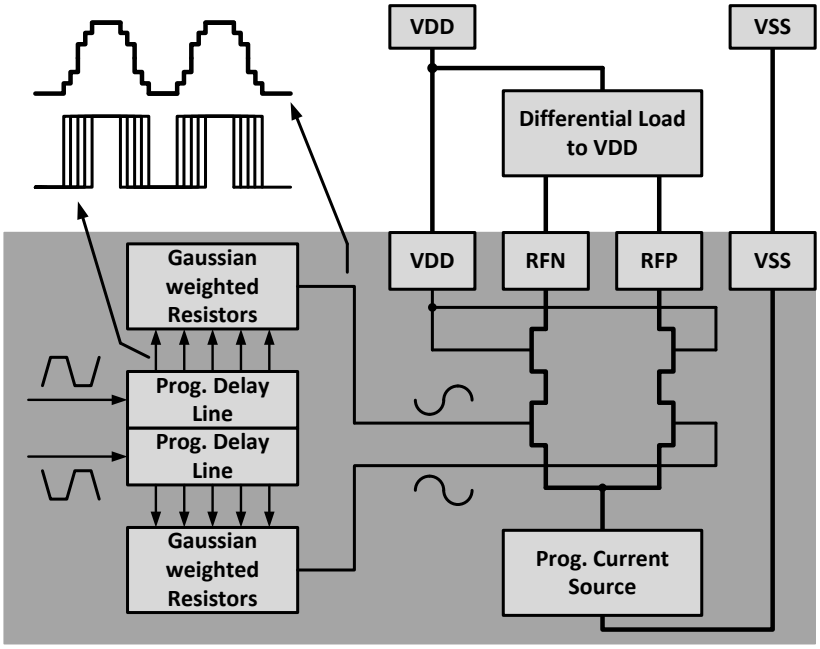

Figure 3.11: Block circuit diagram of the PA: A differential current architecture with Gaussian shaped transitions is used to reduce harmonics and interferences.

As mentioned before, in the SoC transmitter, a PA has been implemented for the operation as a wireless transmitter (see Figure 3.5, PA). During the course of the SoC transmitter design, it was found that under certain conditions an unwanted modulation of the LCO frequency occurs due to harmonic distortions of the output stage and that this modulation is a critical problem for the transmitter. This effect, referred to as injection pulling/modulation, is caused by harmonics in the current of the output stage or the PA, which lie exactly at/or very close to the LCO frequency. Based on magnetic coupling to the LCO inductor, these harmonics can lead to frequency errors for odd integer ratios between the LCO and the output frequency or to a modulation for ratios very close to odd integer values. There is a high probability for this effect to occur due to the fact that many different frequencies are available in the sub-GHz range and due to the fact that the non-trimmable LCO frequency varies due to process variations. Injection pulling/modulation also occurs in crystal based transmitters with LCO based VCOs [83], yet is less critical in a PLL configuration. If the realised chip is operated as a frequency reference, this effect can be neglected up to 180 MHz by using a limited slew rate of the output stage for typical impedance values of the load. However, a high slew rate is inevitable for higher output frequencies up to 1 GHz.

In order to reduce the injection pulling/modulation effect, a differential current based PA architecture has been chosen for implementation within the SoC transmitter. As a result,

the current is mostly influenced by the PA, while the load impedance has only a minor influence on the current transition shape. A differential current based architecture of the PA is also implemented in [58]. Figure 3.11 shows the simplified block circuit diagram of the PA implemented in the SoC transmitter. The output stage of the PA is implemented as a differential open drain stage powered by a programmable current source against VSS. The load must consequently constitute a differential impedance with respect to VDD. To reduce the voltage drop across the transistors an additional cascode is implemented. With this approach, a constant DC current through the PA is achieved which, thus produces little interference. Considerable interferences can in any case also be induced by harmonics from the differential current of the PA. This harmonics have been reduced by means of Gaussian shaping of the current transitions. A delay line is thus used, which generates five phasings for the RF carrier signal of the positive (RFP) and negative output current path (RFN), respectively. The five phasings are recombined via a Gaussian weighted resistor array, leading to Gaussian shaped voltage transitions on the differential current output stage. The shaped voltage signal is converted into the output current by the output stage. The gate capacitance in conjunction with the resistor array thereby acts as an additional LPF. In addition to counteracting injection pulling/modulation effects, a reduced amount of harmonics also simplifies the design of the antenna filter/matching network. A drawback of this implementation is that the Gaussian shaped current transitions lead to a slightly degraded PA efficiency in comparison to rectangular shaped output currents. For a trade-off between PA efficiency and harmonic distortion at the respective operating frequency, the delay line is adjustable corresponding in a rise/fall time in the range between 250 ps and 1.5 ns.

3.2.6 Packaging

Similar to the analog test chip, the SoC transmitter has first been packaged in ceramic for functional tests. Later, the SoC transmitter has also been packaged in a standard plastic package, in order to obtain measurement results, which comprehend all influences caused by the plastic package. These influences include the protection against environmental contamination or objects in the close vicinity of the LCO. Furthermore, package induced frequency errors are important, including water soaking and the related change of permittivity and mechanical stress. In the ceramic package, all available pins of the SoC transmitter can be connected. However, as only 14 pins are available in the employed DSO-14 standard plastic package only the most important pins can be connected. Correspondingly, all required pins are connected for the operation of the programmer interface, the PA, the clock source driver stage (only single ended), and seven general-purpose input/output (GPIO) pins. Figure 3.12 depicts the SoC transmitter in the DSO-14 standard plastic package.

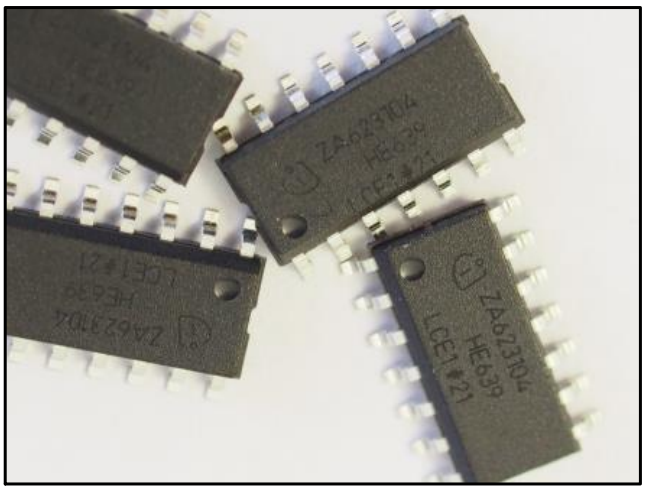

Figure 3.12: SoC transmitter packaged in a standard DSO-14 plastic package, providing operation as a wireless transmitter or a single ended clock source. Additionally, seven GPIO pins are available.

3.2.7 Evaluation Board and Demonstrator

For the SoC transmitter packaged in the DSO-14 standard surface-mount device (SMD) package, a wireless key-fob demonstrator as well as an evaluation board has been realised.

The wireless key-fob demonstrator is depicted in Figure 3.13. Similarly to the Silicon Labs SI4010 datasheet example [58], the antenna is implemented as a magnetic loop antenna on the PCB including the matching for the differential current power amplifier. In comparison to the demonstrator realised with analog test chip (see Figure 3.4), no external microcontroller and no external components for the power management are required. Hence, a complete wireless key-fob can be realised with the SoC transmitter using a minimum number of external components including only two capacitors.

Furthermore, an evaluation board has been developed (shown in Figure 3.13), which is suitable for the 50 Ω test equipment. Using this evaluation board, the SoC transmitter can be configured for an operation as a crystal-less wireless transmitter or a crystal-less frequency reference. It includes the matching and filtering network, realised with passive L, C components in order to provide a differential load of approximately 430 Ω to the PA of the SoC transmitter.

A simple arrangement of a 434 MHz ASK transmitter has been realised using this evaluation board. Figure 3.14 shows the transient graph for one transmitted data package. A baud-rate of 5 kbps and Manchester coding are used. The current consumption is also shown in Figure 3.14 in relation to the respective state of operation. At the beginning of the data transmission, the chip is started up from the deep sleep mode by an external interrupt. The firmware

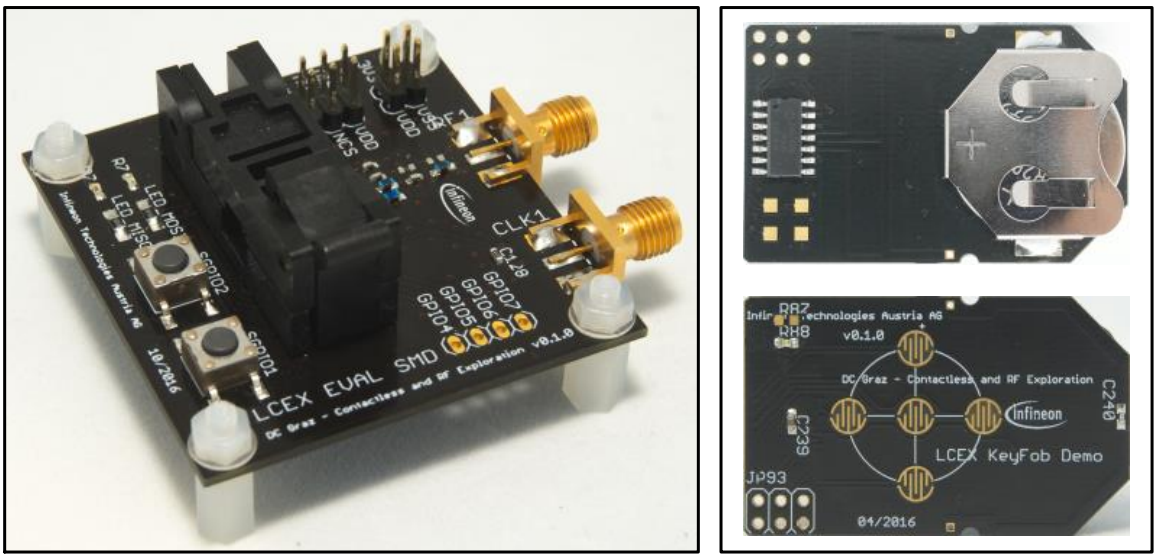

Figure 3.13: Evaluation/demonstrator board for the SoC transmitter in the DSO-14 standard SMD package: On the left side the evaluation board is depicted including a matching network for a sub-GHz wireless operation, a connector for an operation as a crystal-less frequency reference, as well as a programmer interface. On the right side the top and bottom of the wireless key-fob demonstrator is depicted, which is realised using only two external capacitors.

is then loaded from the EEPROM and subsequently executed. For this arrangement, the temperature sensor filters are settled for 6.5 ms. During the temperature settling time the current consumption is low with about 1.2 mA. Subsequently, the LCO and the PLL are turned on. The PLL lock is typically achieved within less than 10 μs and is then followed by the transmission of the data package. The overall current consumption for the RF carrier generation including the continuous temperature compensation amounts to about 8 mA. The transmit current consumption depends on the adjusted output power and can range up to 18.5 mA for the maximum power of 9.5 dBm (as shown in Figure 3.14). After the data transmission, the transmitter goes back to the deep sleep mode in which it consumes 500 nA. Using this test arrangement, compatibility with state-of-the-art sub-GHz receivers has been demonstrated in the lab with different baud-rates for ASK, FSK, and Gaussian frequency shift keying (GFSK) modulation.

3.3 Summary

In Chapter 3, the different test chips, manufactured during this work are presented. Two types of test chips have been manufactured including an analog test chip as well as a SoC transmitter. The architecture of both test chips is described briefly. The analog test chip is kept very simple

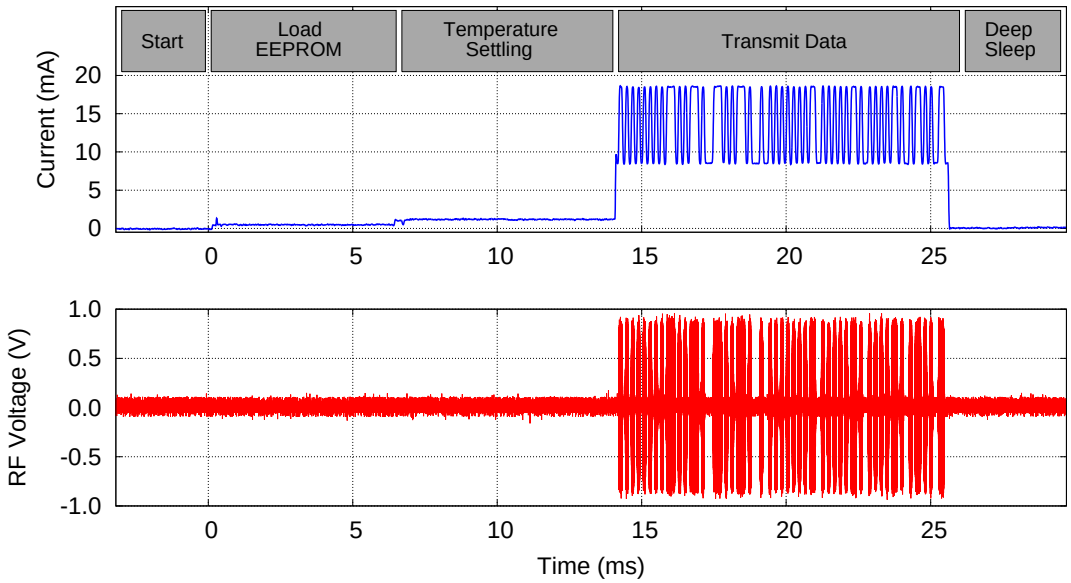

Figure 3.14: Transient plot of a data transmission event: The different states of operation as well as the current consumption are plotted for an ASK operation. Also, the RF-output signal is shown for an optimal matching at a 50 Ω load.

and is purely intended for a proof of concept of the analog building blocks realised with the new non-trimmable LCO architecture. It has been manufactured three times with improvements of the analog circuits in every chip generation. The respective progressions and insights gained with this test chip are highlighted in this chapter.

Based on the designed and optimised circuits of the analog test chip, the SoC transmitter has been developed. For the SoC transmitter, additional new building blocks have been included, which are required for the transmitter functionality. These building blocks comprise of a highly accurate temperature sensor, a mechanical stress sensor, a ring oscillator PLL, as well as a low harmonic distortion PA. They are specifically required for the non-trimmable LCO architecture used in the SoC transmitter. With the exception of the temperature sensor, this building blocks have been designed as part of this work.

Both, the analog test chip as well as the SoC transmitter have been packaged in standard plastic packages for a consideration of package induced effects and a realistic estimation of the overall lifetime behaviour. Also, evaluation boards and demonstrators have been developed, which are briefly presented in this chapter.

Chapter 4

Calibration Methods and Measurement Results

In general, for an all CMOS frequency reference, a calibration is required as process, temperature, and stress effects exceed the maximum tolerable frequency errors by far. Consequently, every device must be individually calibrated, in order to obtain an accurate frequency over the operating conditions. This chapter presents the specific calibration methods, which have been custom-built and applied to the analog test chip and the SoC transmitter.

Additionally, in this chapter several measurement results are presented. They include aforementioned effects, which can influence the frequency accuracy like environmental effects of the package, moisture, and the related mechanical stress (see Sec. 2.2). Considering these effects, the overall frequency accuracy achieved in this work is estimated by using suitable standard reliability tests. Furthermore, injection pulling and modulation as well as phase noise and jitter measurements are performed, which are relevant for a wireless operation.

4.1 Calibration Methods

For the calibration of an LCO based all CMOS frequency reference, several difficulties must be taken into account. As mentioned in Sec. 2.2, a post-assembly calibration is required in order to cancel frequency shifts which would otherwise be caused by the assembly process. A separate calibration for every device is consequently required. Nevertheless, this calibration process must be achieved with a minimum effort, as a complicated calibration process would lead to additional costs in volume production. The calibration effort rises with the required calibration time and complexity, e.g., the number of required temperature insertions. As in an LCO frequency reference the temperature behaviour is one of the major influences on the frequency, it is difficult to keep the number of required temperature insertions low. Due to the different chip designs, different calibration methods have been applied for the analog test chip and the SoC transmitter, respectively. As the analog test chip is only considered a proof of concept development with several design limitations (see Sec. 3.1), only a low importance has been placed on the development of the applied calibration method. Consequently, only a complicated calibration method has been realised, not suitable for volume production. In contrast, the design of the SoC transmitter allows to apply a calibration method, which only requires two

temperature insertions for the entire calibration. Next to the temperature characteristic of the frequency, all the other required parameters must be calibrated with the same two temperature insertions.

4.1.1 Calibration Parameters

During the calibration process, several parameters must be calibrated for the analog test chip and the SoC transmitter. Table 4.1 summarises the respective parameters and the applied calibration methods. The calibration of the analog test chip can only be performed by means of a full sweep over the entire operation temperature and is thus not suitable for a volume production. In contrast, the calibration of the SoC transmitter is realised in a way that is suitable for a volume production. The entire calibration of all required parameters can be performed with only using two temperature insertions at 0 °C and 70 °C. As a result, the development of the two point calibration methods has been more difficult, as the exact underlying mechanism of the temperature behaviour of the LCO frequency must be taken into account. Additionally, the calibration of the stress sensor is required for the SoC transmitter. The calibration methods for the parameters shown in Table 4.1 are described in detail in the following for the analog test chip and the SoC transmitter, respectively.

Table 4.1: Calibration parameters and respective methods for the analog test chip and the SoC transmitter

Parameter / Device	Oscillator amplitude	Frequency versus temperature	Mechanical stress	
			Stress versus temperature	Stress gain
Analog Test Chip	Single point calibration @ room temperature	Sweep over entire operating temperature range (-40 °C - 120 °C)	-	-
SoC Transmitter	Two point calibration (0 °C, 70 °C) + 1st order polynomial function	Two point calibration (0 °C, 70 °C) + 3rd order polynomial function (linearly scaled coefficients)	Two point calibration (0 °C, 70 °C) + 2nd order polynomial function (linearly scaled coefficients)	Calibration in the laboratory (same coefficients applicable to all devices)

4.1.2 Test Setup for Calibration

In order to apply the abovementioned calibration methods, several parameters must be determined for every device. For that reason, a custom-built test setup has been developed, which is suitable for the calibration and test of the analog test chip and the SoC transmitter. It allows to simulataniously measure the LCO frequency and to read various parameters from the chip including the temperature and the mechanical stress values measured on the device under test (DUT). The test setup is based on a microcontroller. It provides the SPI with which the DUT can be programmed and configured. The microcontoller is futher used to measure the LCO frequency using a counter. For the frequency measurement, the LCO chip is adjusted to a

fixed frequency dividing ratio of 100. Assuming an LCO frequency of approximately 3.15 GHz, the resulting output frequency amounts to about 31.5 MHz. The microcontroller measures the frequency by counting the edges of the output frequency signal over a defined counting time. A counting time of 10 ms and 100 ms has been used resulting in a frequency measurement resolution of about 3 ppm and 0.3 ppm, respectively.

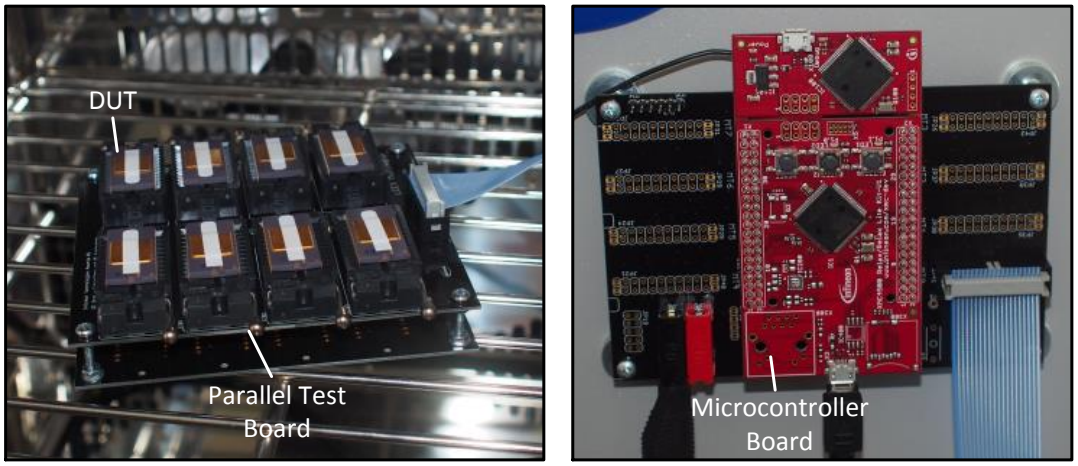

Figure 4.1: Test setup for temperature calibration and measurements: On the left side, eight SoC transmitter chips are placed in a parallel test board, which is located in the climate cabinet. On the right side, the microcontroller board outside of the climate cabinet is depicted, which is used for configuration and frequency measurements of the DUTs.

For a statistically significant statement, a high number of devices must be investigated resulting in a considerable measuring effort. In order to reduce this effort, the test setup has been extended to be suitable for a parallel operation. Figure 4.1 shows the test setup including a microcontroller board, as well as a parallel test board (only a version for devices packaged in ceramic is shown). Using this parallel test board, up to eight devices can be tested simultaneously.

It must be noted that the microcontroller is clocked by a quartz crystal. Any frequency error of the quartz crystal would thus lead to a frequency error of the calibrated devices. However, as the devices have all been calibrated and tested using the same microcontroller board, this error is cancelled out. Furthermore, only the LCO devices are placed in the climate cabinet while the microcontroller is always kept outside the climate cabinet at room temperature.

4.1.3 Oscillator Amplitude Calibration

As elucidated in Sec. 2.4.2, the LCO amplitude has a considerable influence on the frequency. For that reason, an automatic amplitude control circuit is implemented in this work, which allows the LCO amplitude to be adjusted using a digital control signal OCP. The automatic amplitude control is described in detail in Sec. 2.4.3. In order to provide the best possible frequency accuracy, every device must be calibrated to an optimum LCO amplitude. For the analog test chip, this has been performed as a single point calibration at room temperature. However, the optimum LCO amplitude also has a considerable dependency on the temperature. Therefore, a temperature compensation has been implemented in the SoC transmitter, allowing to operate the LCO at an optimal amplitude over the entire operating temperature range.

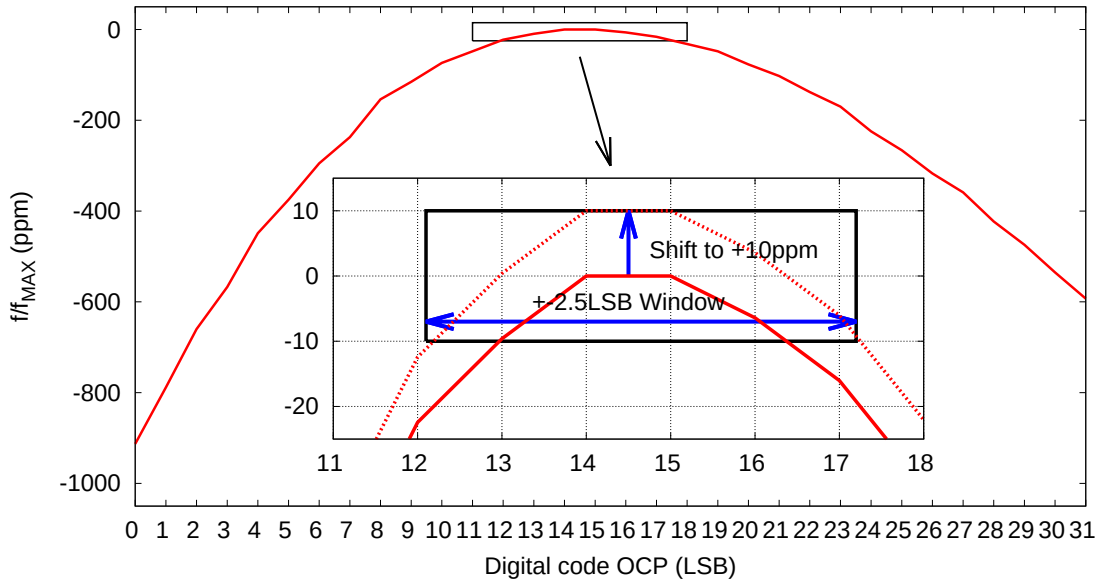

Figure 4.2: Measured relative LCO frequency as a function of the programmed OCP value with respect to the maximum frequency. The small subsection shows the calibration approach and the estimated frequency error referable to voltage drifts over lifetime.

The oscillator amplitude calibration is performed by means of a sweep of the LCO amplitude via the digital OCP value, which has a resolution of 5 bit. The maximum value of the frequency is considered the ideal operating point. An operation at this point leads to a minimised frequency sensitivity to drifts of the LCO amplitude over the lifetime of the device. Voltage drifts can be attributed to changes of bias currents and offset voltages of the automatic amplitude control circuitry or directly to a drift of the threshold voltage of the transistors in the sustaining amplifier. These drifts must be considered for the calibration.

An offset of the ideal operating amplitude of the LCO can also be regarded as an offset of the ideal digital OCP value. Figure 4.2 shows the relative frequency of the LCO as a

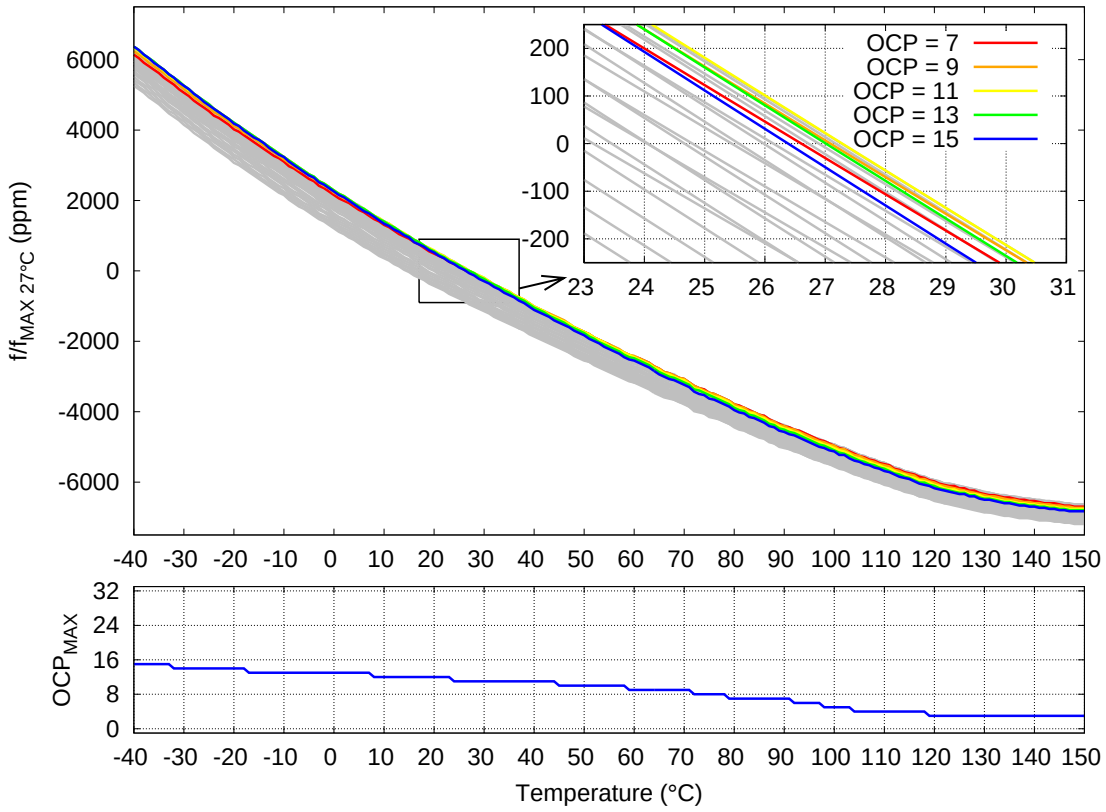

Figure 4.3: LCO frequency measured over the temperature for all possible OCP values ranging from 0 to 31: The OCP value for the respective maximum frequency versus temperature is depicted in the bottom.

function of the digital OCP value with respect to the measured maximum value. An offset of the ideal digital OCP value always leads to a negative frequency error when the maximum frequency is taken for the calibration of OCP. Therefore, an initial calibration to a slightly positive frequency error, i.e., 10 ppm can be applied to improve the frequency accuracy under consideration of voltage drifts over lifetime. Also, the temperature dependency of the ideal operating amplitude of the LCO must be taken into account for calibration. Figure 4.3 shows the relative LCO frequency versus temperature for a single device. The frequency has been measured for all possible OCP values ranging from 0 to 31 and has been normalized to the maximum frequency at 27 °C. Additionally, in Figure 4.3, the digital OCP value for the maximum frequency versus temperature is shown. A change of several least significant bit (LSB) can be observed versus temperature. Therefore, also a temperature calibration and compensation is necessary.

The detailed subsection of Figure 4.2 shows the frequency error around ±2.5 LSB offset of the OCP value corresponding in an error of -20 ppm to 0 ppm. An initial frequency calibration to +10 ppm allows the frequency error to stay within ±10 ppm for a maximum OCP offset

of ±2.5 LSB (see Figure 4.2, dashed line). The initial *OCP* calibration is performed by means of two temperature insertions at 0 °C and 70 °C for the SoC transmitter. A first order polynomial is fitted through this points for an amplitude compensation versus temperature. For the quantisation and calibration errors versus temperature, a maximum offset of ±1 LSB is expected. The residual headroom of ±1.5 LSB corresponding to 35 mV LCO amplitude error is expected not to be exceeded over the device lifetime.

4.1.4 Frequency Calibration versus Temperature

In order to obtain an accurate frequency over the operating temperature range, every device must be calibrated individually. As mentioned above, this calibration process must be feasible with a minimum effort, as a complicated calibration process would lead to additional costs in volume production. Due to the different chip designs, different calibration approaches have been applied for the analog test chip and the SoC transmitter, respectively.

Frequency Calibration of the Analog Test Chip

The analog test chip is calibrated by means of a full sweep over the entire operating temperature range, while the frequency as well as the digital value from the integrated temperature sensor are gathered. From the obtained curves, a calibration polynomial is determined for every device individually. A high initial frequency accuracy of 50 ppm over a temperature range of -20 °C to 85 °C is achieved with this approach depicted in Figure 4.4. However, a full temperature sweep is impractical for a high volume production. The attempt of applying a two-point calibration has failed due to the highly non-linear behaviour of the integrated temperature sensor.

Frequency Calibration of the SoC Transmitter

Compared to the analog test chip, in the SoC transmitter a more accurate temperature sensor is implemented, which allows applying a two point calibration approach.

As described in Sec. 2.2.1, the lossy components of the LC tank are the major components, determining the LCO frequency characteristic versus temperature. The inductor as well as the capacitor of the LCO are composed of metal layers, which exhibit a finite conductivity. Consequently, these components show losses, which can be considered as serial resistors R_{SL} and R_{SC}. The lossy components exhibit temperature coefficients and as a result lead to a temperature dependency of the LCO frequency (see Equation 2.2.2). As R_{SL} typically outweighs R_{SC}, the overall temperature coefficient is negative (see Equation 2.2.3). Considering a constant temperature coefficient of R_{SL}, Equation 2.2.3 implies a negative concave-down temperature characteristic of the LCO frequency. However, measurement results show a negative concave-up

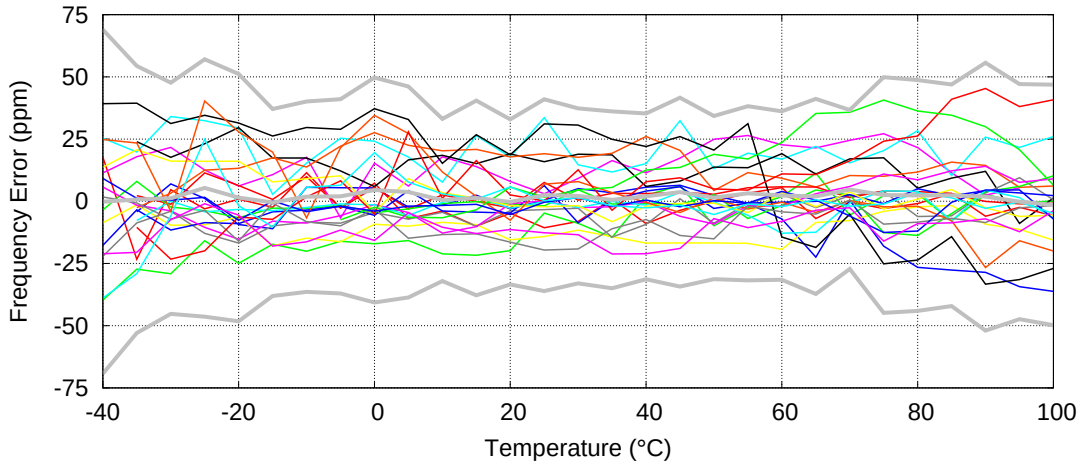

Figure 4.4: Measured frequency error versus temperature after initial calibration for 24 samples of the analog test chip: The grey lines indicate the average error and the $\pm 3\,\sigma$ limits.

temperature characteristic. For clarification, metal resistors have been implemented as part of the process sensor using the metal layers, which are also used for the inductor as a substitute for R_{SL} (see Sec. 3.2). The relative resistances, normalized to the resistance at 27 °C have been measured for the four metal layers used in the inductor and are depicted in Figure 4.5. A non-linear behaviour has been found with the temperature coefficient of R_{SL} decreasing at high temperatures. This finding explains the measured negative concave-up temperature characteristic of the LCO (see Figure 4.3).

As the relative temperature characteristic of R_{SL} varies very little but only the absolute value of R_{SL} varies strongly due to variations in the metal layer thickness, the corresponding temperature characteristic of the LCO varies in a very well defined way, which can be exploited for a simplification of the calibration process.

For the temperature compensation, similar to [10], a polynomial has been implemented in order to determine the dividing ratio $D(T)$ of the fractional frequency divider as a function of the temperature according to:

$$D(T) = C_0 + T \cdot C_1 + T^2 \cdot C_2 + T^3 \cdot C_3. \tag{4.1.1}$$

In order to enable a simplified calibration, a formula has been developed in this work, which resembles the underlying mechanism for the temperature characteristic referable to R_{SL} by linearly scaling the coefficients C_{RL1}-C_{RL3}:

$$D(T) = C_{\mathrm{AL0}} + C_{\mathrm{AL1}}(T \cdot C_{\mathrm{RL1}} + T^2 \cdot C_{\mathrm{RL2}} + T^3 \cdot C_{\mathrm{RL3}}) + T \cdot C_{\mathrm{LC}}. \tag{4.1.2}$$

Additionally, a portion of the temperature characteristic which is not related to R_{SL} is considered

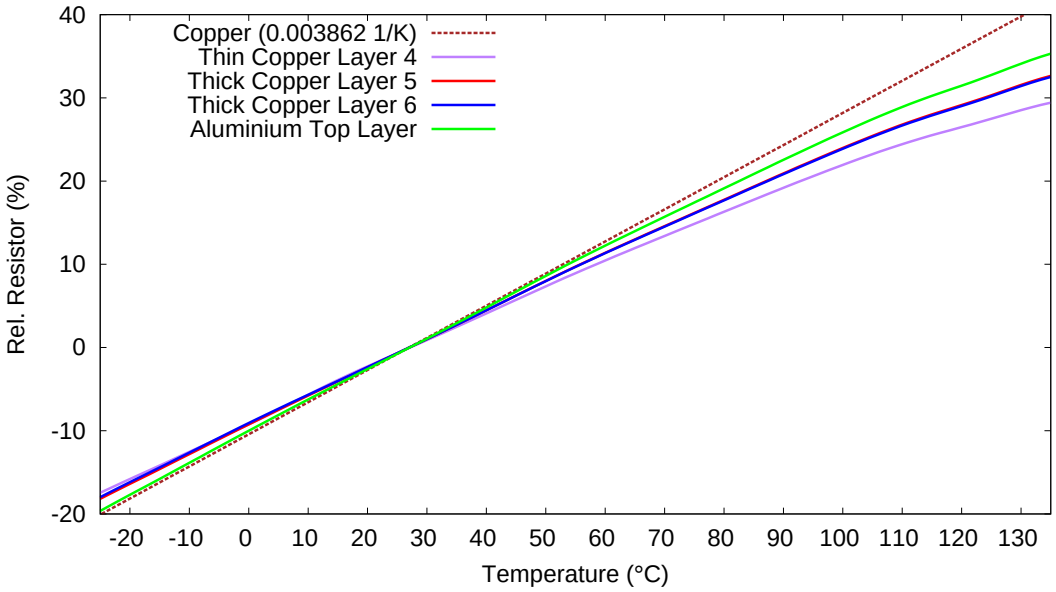

Figure 4.5: Relative resistances of the different metal layers that are used in the LCO inductor as a function of the temperature (the two thick copper layers 5 and 6 have an almost identical characteristic): The temperature coefficients are not constant, but instead decrease at higher temperatures. This behaviour explains the specific temperature characteristic of the LCO and can be exploited to simplify the LCO frequency calibration.

by the coefficient C_{LC}, e.g., the thermal expansion for the inductor or the temperature coefficient of the permittivity for the capacitor (see Sec. 2.2.1).

In Equation 4.1.2, the temperature characteristic referable to R_{SL} is implemented as a third order polynomial. Effects referable to L and C are considered only with a linear coefficient. The coefficients C_{LC} and C_{RL1}-C_{RL3} have been found experimentally using chips from different wavers. To determine C_0-C_3 of the final polynomial (Equation 4.1.1), only C_{AL0} and C_{AL1} must be determined for every single device individually, which can be accomplished by means of two temperature insertions, e.g., 0 °C and 70 °C. The calibration approach has been found to be very robust with the same coefficients applied to devices from four different wafers. Figure 4.6 shows the initial frequency accuracy of 28 devices in a ceramic package after the initial calibration. A high initial frequency accuracy of 52 ppm over a temperature range of -20 °C to 85 °C has been achieved. The initial average frequency error of about +10 ppm is caused by the aforementioned oscillator amplitude calibration.

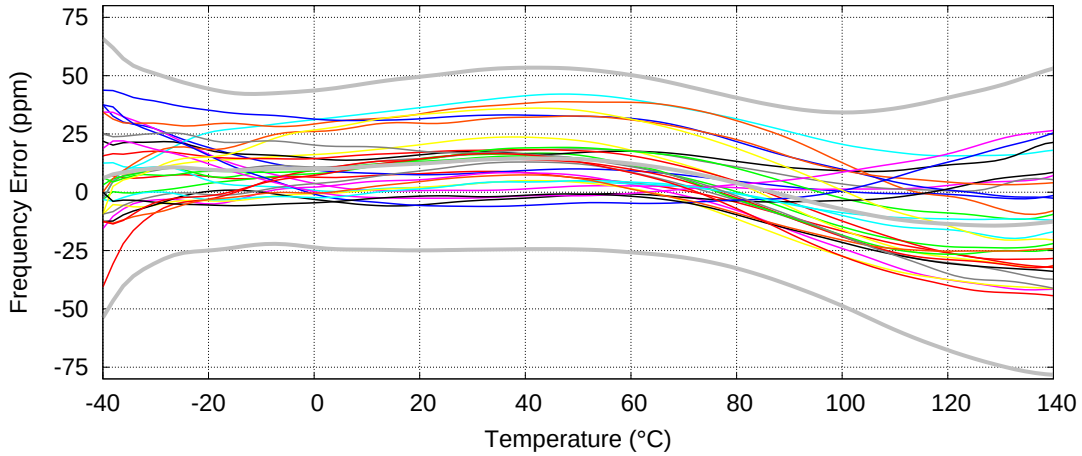

Figure 4.6: Measured frequency error versus temperature after initial calibration for 28 samples of the SoC transmitter: The grey lines indicate the average error and the $\pm 3\,\sigma$ limits.

4.1.5 Mechanical Stress Calibration

The design of the stress sensor implemented in the SoC transmitter is described in detail in Sec. 3.2.3. Two different types of stress resistors (lateral and vertical) are used, which exhibit different piezo coefficients. The different piezo coefficients allow to determine the mechanical stress by measuring the ratio between the stress resistors (see Figure 3.9). The resistor ratio is converted into a differential voltage between the lateral and the vertical stress resistors $V_{\sigma,\mathrm{x+y}}$ using a programmable current mirror. Furthermore, the resistors are divided in several subunits, which are equally arranged in x and y direction, allowing to measure the sum of the in-plane stress $\sigma_{\mathrm{x+y}}$. Additionally, the lateral stress resistors are implemented as a bridge. The difference between the stress in x and y direction $\sigma_{\mathrm{x\text{-}y}}$ can be measured as the transverse voltage at the bridge $V_{\sigma,\mathrm{x\text{-}y}}$. An ADC is used to convert the analog voltages $V_{\sigma,\mathrm{x+y}}$ and $V_{\sigma,\mathrm{x\text{-}y}}$ into raw digital values for $\sigma_{\mathrm{x+y}}$ and $\sigma_{\mathrm{x\text{-}y}}$ in order to facilitate a digital stress compensation.

All the components used in the stress sensor are sensitive to PVT effects, making a calibration necessary. In a first calibration step, the programmable current mirror is adjusted in a way so that the voltage drop across the vertical and the lateral stress resistors is equal and the voltage $V_{\sigma,\mathrm{x+y}}$ is zero. However, as only a limited resolution is available for the programmable current mirror, a small voltage for $V_{\sigma,\mathrm{x+y}}$ might remain.

As the vertical and the lateral stress resistors have a slightly different temperature coefficient, the digital value for $\sigma_{\mathrm{x+y}}$ also has a temperature dependency. A calibration versus temperature is thus required in order to compensate the temperature dependency. Therefore, every device is calibrated with two temperature insertions. A second order calibration polynomial is fitted through this two temperature points, which generates a compensation value using the integrated

temperature sensor. The polynomial value is subtracted from the raw digital values for σ_{x+y}. The corresponding result is a measure for the sum of the mechanical stress in x and y direction σ_{x+y}. The calibration versus temperature must be performed for every device separately. It is performed simultaneously with the LCO frequency calibration using the same two temperature insertions at 0 ℃ and 70 ℃. The stress calibration in a high volume production can thus be accomplished with a minimum additional calibration effort.

Next to the temperature calibration, a sensitivity calibration is required. The measured stress is used to compensate stress induced frequency errors in the LCO. A stress gain coefficient is thus required to scale the stress measured with the stress sensor for an exact compensation of the stress induced LCO frequency errors. Two different stress gain coefficients are used for σ_{x+y} and σ_{x-y}, respectively. The calibration of these stress gain coefficients is a very difficult process, as the devices must be exposed to mechanical stress to investigate its behaviour. However, a separate calibration for every single device is thus not feasible for a volume production. As the mechanism of stress induced frequency errors is highly reproducible (stress strain relation described in Sec. 2.2.3), the stress gain coefficients can be considered equal for every device. A single calibration of the stress gain coefficients has thus been performed once in the laboratory to be then used for all subsequently calibrated devices.

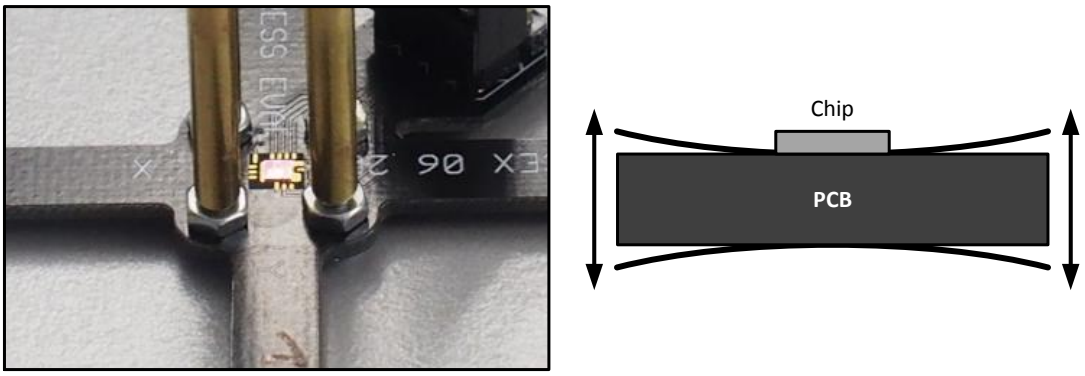

Figure 4.7: Stress sensor gain calibration: Mechanical in-plane stress is induced at the chip surface by means of bending. For that reason, the chip is glued to a PCB. The mechanical coupling allows to bend the chip by bending the PCB. The correlation between the stress induced response of the stress sensor as well as the LCO frequency is used for the calibration.

In this work, the stress gain coefficients have been calibrated by bending the DUT in x and y direction, respectively. Bending can be used to induce mechanical in-plane stress on the surface of the chip. A similar approach has been used in [72]. As depicted in Figure 4.7, a PCB with the SoC transmitter chip glued on the surface is utilised for that reason. Using a rugged glue, a high mechanical coupling is achieved between the chip and the PCB, which allows to bend the chip by bending the PCB. For the calibration, a simple method has been chosen. The

stress gain coefficients for σ_{x+y} and σ_{x-y} have been adjusted in a way, so that the frequency error induced by bending vanished. This calibration has been performed for several devices, showing only little difference in the stress gain coefficients. For the final calibration of the SoC transmitter in the DSO-14 plastic package, the average values are used as the stress gain coefficients for σ_{x+y} and σ_{x-y}, respectively.

4.2 Environmental Influence of Package and Humidity

By exposure to any moisture, a plastic package can soak water [70]. As described in Sec. 2.2 this leads to two major effects by which the LCO frequency can be influenced. One effect is the deformation of the water soaked package, inducing mechanical stress in the chip, which as a consequence leads to a change of the LCO frequency. The mechanical stress induced frequency error is investigated in detail in Sec. 4.3. The other effect is caused by the direct electrical interaction of the LCO with its environment, which changes the frequency as a result of a change of the environmental permittivity.

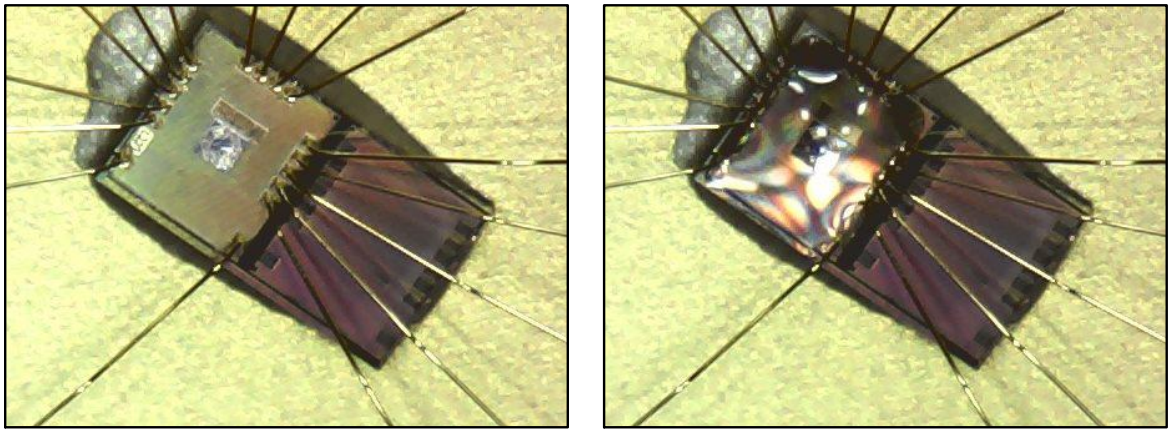

Figure 4.8: The left picture shows the analog test chip in an open ceramic package. The right picture shows the same chip with a drop of water placed on its surface. A shift of the LCO frequency is observed, which is used to assess the environmental sensitivity caused by electric field interactions.

As described in Sec. 2.2.2, the inductor of the LCO produces an electric field. This effect leads to an LCO frequency error due to electric field interaction induced by the water absorption of the package. In order to determine the LCO sensitivity to this effect, the chip surface has been exposed to water, which has a defined relative permittivity of 81. Figure 4.8 depicts the analog test chip in an open ceramic package with a drop of water placed on its surface. The frequency shift, which is caused by the drop of water, is considered a response to 100 % water. However, in a plastic package the water content is limited. In [84], a saturated moisture concentration of

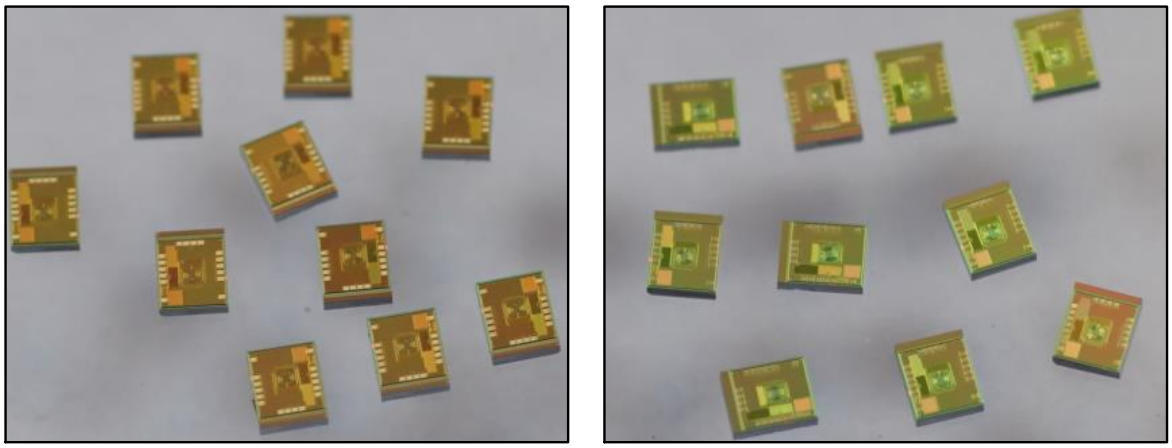

Figure 4.9: Bare die of the analog test chip with polyamide coating (brown) on the left and passivation coating (shiny green) on the right side

about 3 mg/cm³ is reported for various mold compounds corresponding to 0.3 %. The maximum frequency error caused by 0.3 % water is estimated using linear interpolation. Furthermore, the layers between the inductor and the chip surface have an influence on the electric field spread. For an improved Q, the inductor has been extended by the top metal aluminium layer for one version of the analog test chip (see Sec. 3.1) and for the SoC transmitter (see Sec. 3.2). This additional metal layer reduces the thickness of the silicon oxide insulator to the chip surface. Additionally, with polyamide and passivation two different chip coatings are available leading to different sensitivities. Figure 4.9 depicts the analog test chip manufactured with polyamide and passivation, respectively. Although the thicker polyamide coating can reduce the response to the water drop, it must be noted that the polyamide itself could potentially absorb water. This circumstance is not considered in this investigation as the test duration of only a few seconds is too short for the polyamide to absorb water. The measured frequency shifts as well as the estimated frequency error in a package is summarised in Table 4.2 for the different chip generations and coatings. It can be observed that the devices with an inductor design including the top aluminium layer show a higher sensitivity. Furthermore, the polyamid coating reduces the sensitivity. An acceptable frequency error of -51 ppm is estimated for the SoC transmitter with passivation coating, assuming a saturated moisture concentration of 0.3 %. However, in practice such a high moisture concentration is not expected to occur. A more realistic estimation of the frequency error caused by moisture can be obtained using the HAST (see Sec. 4.4).

4.3 Mechanical Stress

As described in Sec. 3.2.3, n-well stress resistors are used as piezo-resistive stress sensors. Two types of stress resistors are used (lateral and vertical) exhibiting different stress coefficients.

Table 4.2: LCO frequency error caused by humidity due to electric field interaction

Device	Analog Test Chip	Analog Test Chip	Analog Test Chip	SoC Transmitter	SoC Transmitter
Chip coating	Passivation	Passivation	Polyamide	Passivation	Polyamide
Inductor design	Cu	Cu+Al	Cu+Al	Cu+Al	Cu+Al
Frequency shift 100 % water (ppm)	-9300	-16500	-1730	-17100	-1810
Estimated max. frequency shift in package (0.3 % water) (ppm)	-28	-50	-5	-51	-5

In order to evaluate the functionality of the stress resistors, their stress sensitivity is of great importance. It is difficult to measure the stress sensitivity by applying stress with an absolute accuracy as described in [85]. For the sake of low costs, in this work a different method has been applied. As the lateral stress resistors have a very well defined in-plane current flow direction, the stress sensitivity can be estimated via the known doping density of the n-well. The relation between the stress sensitivity and the doping density is presented in [86]. Knowing the stress sensitivity of the lateral stress resistors, the sensitivity of the vertical stress resistors can be determined by comparing the relative response to stress without knowing the absolute value of the applied stress.

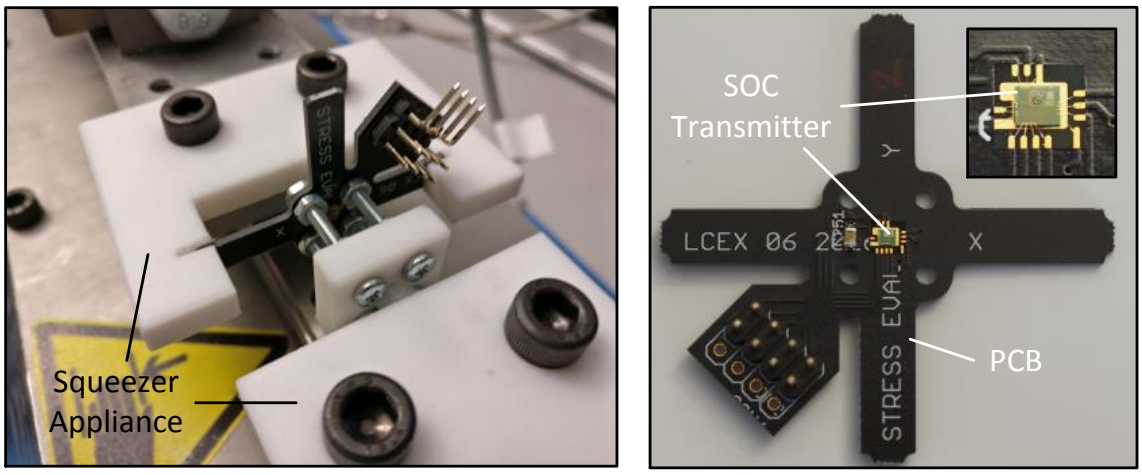

Figure 4.10: Apparatus for stress sensitivity measurements: On the right side a PCB is depicted, on which the SoC transmitter is bonded using a hard glue for a good mechanical coupling (the detailed subsection shows the chip and the bond wires). On the left side this PCB is depicted fixed in a squeezing appliance setup for bending the SoC transmitter by applying a defined force to the PCB.

For the stress measurements, several chips have been glued on a PCB (right side of Figure 4.10) with which in-plane stress can be induced by bending of the PCB as described in Sec. 4.1.5.

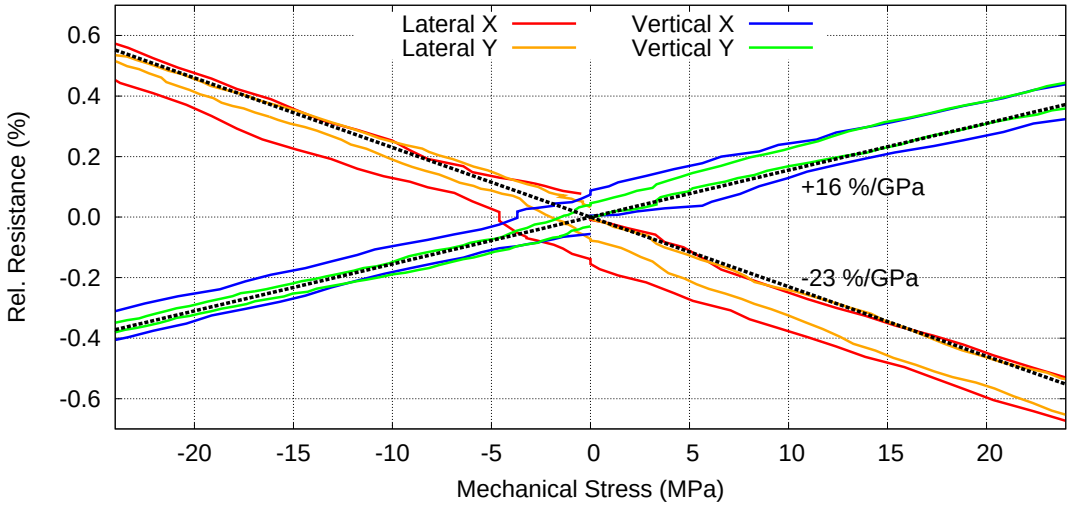

Figure 4.11: Relative change in resistance in response to stress for the lateral and the vertical stress resistors: Bending in x and y direction is applied to induce in-plane stress. The sensitivity of the lateral stress resistors is estimated with -23 %/GPa and allows determining the sensitivity of the vertical stress resistors with +16 %/GPa.

This PCB has been further fixed on a squeezer apparatus (left side of Figure 4.10) in order to apply an accurate and well reproducible force. It is assumed that a linear relation between the applied force and the in-plane stress exerted on the chip is prevalent. The measurements have been performed by applying a transient triangular force profile on the PCB. All the obtained measurement results are scaled to the known sensitivity of the lateral stress resistors. Furthermore, all the measurements are performed with bending in x and in y direction, respectively.

Figure 4.11 shows the relative change in resistance in response to stress for the lateral and the vertical stress resistors using x and y bending, respectively. With an estimated sensitivity of -23 %/GPa for the lateral stress resistors, a sensitivity of +16 %/GPa can be observed for the vertical stress resistors. No significant difference is found for x and y bending, however, a minor hysteresis-like behaviour is found (see Figure 4.11 at $\sigma = 0$), which is presumably caused by the glue connecting the chip with the PCB.

Several interesting parameters have been measured with the aforementioned apparatus using the lateral stress resistor as the reference. However, the measurements have been performed consecutively. After several bending procedures it has been observed that the applied force leads to different stress values. It is assumed, that the glue weakens with every bending procedure, leading to significant measurement errors. As a result, the measurements which are obtained with this method are considered not to be exact. Nevertheless, the results are important in order to gain insights into the cause of the mechanical stress induced frequency error. Figure 4.12 shows the sensitivity of the LCO frequency as well as the digital values for the sum and the

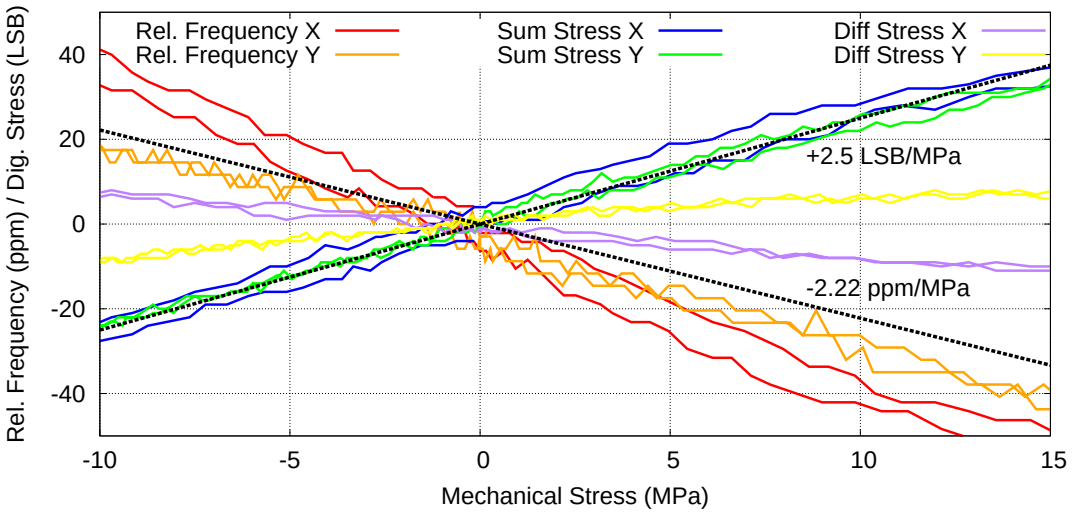

Figure 4.12: Relative change of the measured LCO frequency and the digital values for the mechanical stress in response to in-plane stress induced by bending: A sensitivity of 2.5 LSB/MPa is shown for the digital value of the stress sensor (black dashed line). For the LCO frequency sensitivity to the sum of the stress, a slightly higher value than the theoretically determined -2.22 ppm/MPa is found (black dashed line). Additionally, a small sensitivity to the difference of the stress is found.

difference of the mechanical stress in x and y direction $\sigma_{\text{x+y}}, \sigma_{\text{x-y}}$. A significant correlation between the applied stress and the digital value for $\sigma_{\text{x+y}}$ is found with about 2.5 LSB/MPa. Also a good correlation of the LCO frequency sensitivity has been found. However, a slightly higher sensitivity as the -2.22 ppm/MPa estimated in Sec. 2.2.3 has been found. Also, a slightly different response to mechanical stress in x and y direction is present.

The measurement results confirm, that the major underlying effect of the stress sensitivity of the LCO frequency is caused by the stress induced deformation, affecting the inductor and the capacitor as described in Sec. 2.2.3. The deviation from the theoretically determined sensitivity as well as the difference of the sensitivity in x and y direction is assumed to be caused by the transistors of the sustaining amplifier and the unsymmetrical arrangement of their LCO layout (see Sec. 2.4.2).

4.4 Standardised Reliability Tests

ICs can change their behaviour over lifetime. This effect is also referred to as ageing. In LCO based all CMOS frequency references, ageing can lead to drifts of the initially calibrated frequency [39]. For a statement of the overall frequency accuracy, which can be achieved with an all CMOS frequency reference, these drifts must be considered. Several standard reliability tests are applicable to perform accelerated ageing in ICs in order to predict their behaviour

over lifetime. Different effects can lead to frequency errors in an LCO based frequency reference as elucidated in Sec. 2.2. The functionality of the CMOS circuit can be altered by degradation effects. These effects are mostly relevant for active components (transistors) and are accelerated by high temperature or high operating voltages. Furthermore, package induced mechanical stress caused by moisture can influence the behaviour of the CMOS circuit. Depending on the IC, other ageing mechanisms might be relevant. High temperature ageing can also lead to cure shrink of the package mold compound and consequently to a change of the mechanical stress [71]. Furthermore, in an LCO based all CMOS frequency reference, moisture can influence the frequency by interaction with the electric field due to the high permittivity of water. A separation of the respective effects on the frequency is therefore difficult and has not been reported in previous work. In [38], moisture related effects have been found to be the major cause of frequency errors in an all CMOS frequency reference, significantly limiting the overall frequency accuracy. It has been stated that package effects are responsible for frequency drifts next to the CMOS circuit design. However, as in this work a mechanical stress sensor is implemented in the SoC transmitter, a separation between stress induced and other ageing related frequency errors is possible.

In order to estimate the lifetime induced frequency errors, several standardised reliability tests have been performed with the SoC transmitter. These tests include HAST*, HTOL, and a standard solder reflow profile. The results are summarised in Table 4.3. Additionally, the frequency accuracy versus temperature obtained with the SoC transmitter in a plastic package as well as versus the supply voltage range is stated. All tests have been performed with and without stress compensation, respectively. Consequently, the contribution of mechanical stress to frequency errors can be recognized in Table 4.3. As expected, the major portion of frequency drifts caused by HAST is attributable to mechanical stress effects. The same is true for frequency errors caused by soldering. However, against expectations, a high frequency error is caused by HTOL even with mechanical stress compensation. In [38], only a small frequency error was found to be caused by HTOL.

Similar to [38], each stress test is considered independent and includes a mean offset (μ) and a standard deviation (σ). The overall ($3\,\sigma$) frequency accuracy is estimated by determining the maximum value of all possible combinations of the offsets (μ) and calculating the root of the sum of each variance (σ^2). As a results, an overall frequency accuracy ($3\,\sigma$) of 204 ppm can be estimated without the stress compensation, which is comparable to state-of-the-art LCO based all CMOS frequency references. However, using the stress compensation, a significantly better overall frequency accuracy ($3\,\sigma$) of 136 ppm can be achieved.

* As the results of the HAST are not available at the current time, these results have been substituted by devices which have been stressed by storage in a glass of water for 96 hours. The induced stress is assumed to be comparable with the stress induced by a HAST.

Table 4.3: Frequency accuracy of the SoC transmitter with and without stress compensation

Test	Method/Conditions	No stress comp.		Stress comp.	
		μ (ppm)	σ (ppm)	μ (ppm)	σ (ppm)
Temperature	0 - 70 °C	-10	14	2	21
Supply voltage	1.8-3.6 V (cal. @ 3.3 V)	-1	2	-1	2
HTOL	1000 hr. operating life test at 125 °C	47	19	65	5
HAST	96 hr. unbiased	-34	4	-4	2
Solder reflow	260 °C profile	58	23	-4	7
Total	max($\lvert\mu\rvert$), σ	105	33	67	23
	$\lvert\mu\rvert + 3 \cdot \lvert\sigma\rvert$	204		136	

4.5 Oscillator Injection Pulling and Modulation

Injection pulling is another possible mechanism, which can lead to a frequency error in an LCO based frequency reference [87], [88]. In CMOS frequency reference devices, typically a push-pull output stage is used. Such an output stage produces a rectangular voltage signal with a high amount of harmonics. Mostly odd harmonics can occur but also even harmonics are present. If the ratio between the output frequency and the LCO frequency is an integer value, harmonics can occur, which lie exactly at the LCO frequency. This harmonics can lead to a frequency deviation referred to as injection pulling. Depending on the phase, the frequency deviation can be positive or negative. Also, for frequency ratios very close to an integer value, a frequency modulation can occur.

It must be noted that injection pulling in integrated LCO frequency references is mostly based on the magnetic interaction between the output stage and the LCO inductor. Hence, the load has a strong influence as it affects the current of the output stage.

Injection pulling has first been observed in the analog test chip. The analog test chip uses a CMOS push-pull output stage, which is designed using very short transistors in order to operate over the entire available output frequency ranging up to 3 GHz (see Sec. 3.1). As a result, this output stage has very short rise and fall times and consequently produces harmonics in the frequency range of the LCO. This is also true in the case when operating at low frequencies of about a few MHz.

In contrast, the SoC transmitter is realised with several design improvements to reduce injection pulling (see Sec. 3.2). Two different output stages are available. A CMOS push-pull output stage is implemented for an operation with dividing ratios down to 16 corresponding to an output frequency of up to 180 MHz. As a result of the much lower frequency compared to the analog test chip, the CMOS push-pull output stage can be implemented with a much longer rise and fall time, resulting in significantly reduced injection pulling effects. For higher frequencies

up to about 1 GHz, a PA is implemented with a differential current open drain architecture for reduced injection pulling effects.

In order to test the sensitivity to injection pulling, both frequency references, the analog test chip and the SoC transmitter, have been investigated using a frequency demodulator. Therefore, the DUT is operated with an integer dividing ratio. The measured frequency may has an offset caused by injection pulling. However, using an exact integer dividing ratio, a constant frequency is observed in any case by the frequency demodulator. By adjusting the dividing ratio to a value very close to the previous integer value, the injection pulling causes a modulation of the frequency. This modulation can be observed with the frequency demodulator. The positive and negative peak values are considered the maximum frequency error caused by injection pulling.

As an example, the measured modulated and unmodulated frequency is depicted in Figure 4.13 for the SoC transmitter using the custom-built PA. It is operated with the worst case odd integer dividing ratio of three, corresponding to a frequency of about 1.06 GHz. For the sensitivity test, the closest digital dividing ratio next to three has been chosen, resulting in a frequency deviation of 20 Hz. As a result of injection pulling the output frequency is modulated with three times this frequency deviation amounting to 60 Hz. An acceptable maximum frequency error referable to injection pulling of 5.8 ppm is obtained under worst case conditions using the highest possible frequency, the maximum current for the PA, and the minimum PA current transition time of 250 ps.

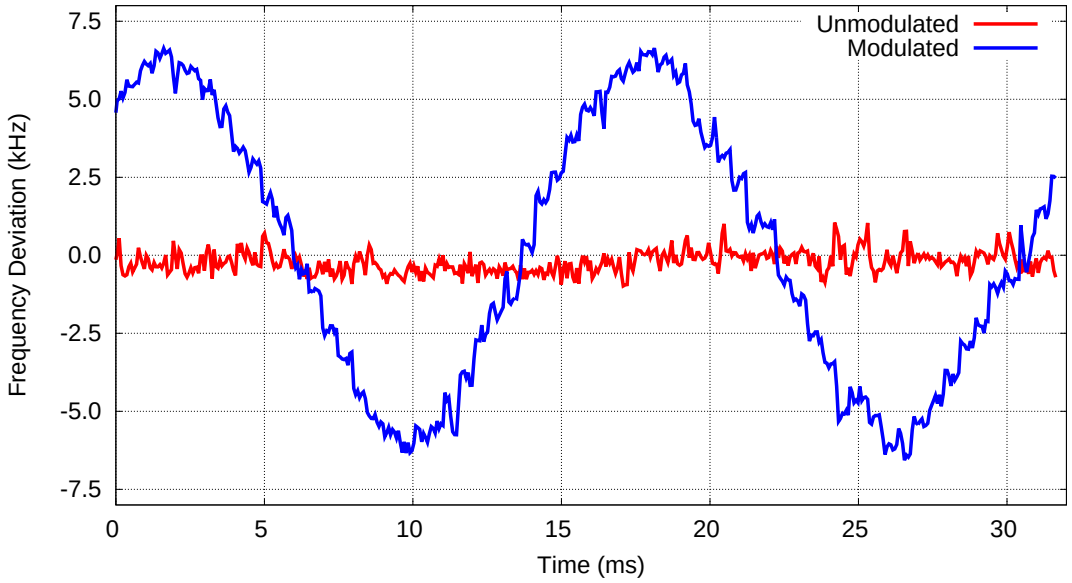

Figure 4.13: Transient plot of the frequency deviation from the 1.06 GHz carrier obtained by means of a frequency demodulator. For a dividing ratio of 3,000000059 a modulated and for a dividing ratio of exactly three an unmodulated carrier signal can be observed. Due to injection pulling, a maximum frequency deviation of 6.2 kHz was found corresponding to 5.8 ppm.

The above described injection pulling measurement has been repeated with the analog test chip for integer dividing ratios from 2 - 23 corresponding to a frequency range of 137 - 1575 MHz. Injection pulling measurements for the SoC transmitter have been performed using the CMOS push-pull output stage* for integer dividing ratios from 16 - 33 corresponding in a frequency range of 92 - 191 MHz and with the differential current PA for integer dividing ratios from 3 - 10 corresponding in a frequency range of 315 - 1050 MHz. The results are depicted in Figure 4.14 as frequency deviation in ppm as a function of the integer dividing ratio. Due to different designs, the LCO frequencies of the analog test chip and the SoC transmitter are slightly different. However, the corresponding influence on injection pulling effects can be neglected. Figure 4.14 shows a significantly reduced sensitivity to injection pulling in the SoC transmitter compared to the analog test chip, which is considered to be attributable to the aforementioned design differences of the respective output stages.

* A 50 Ω load has been used for the injection pulling measurements of the analog test chip and the SoC transmitter using the CMOS push-pull output stage. Additionally, a parallel capacitance of about 15 pF is added by the respective test board.

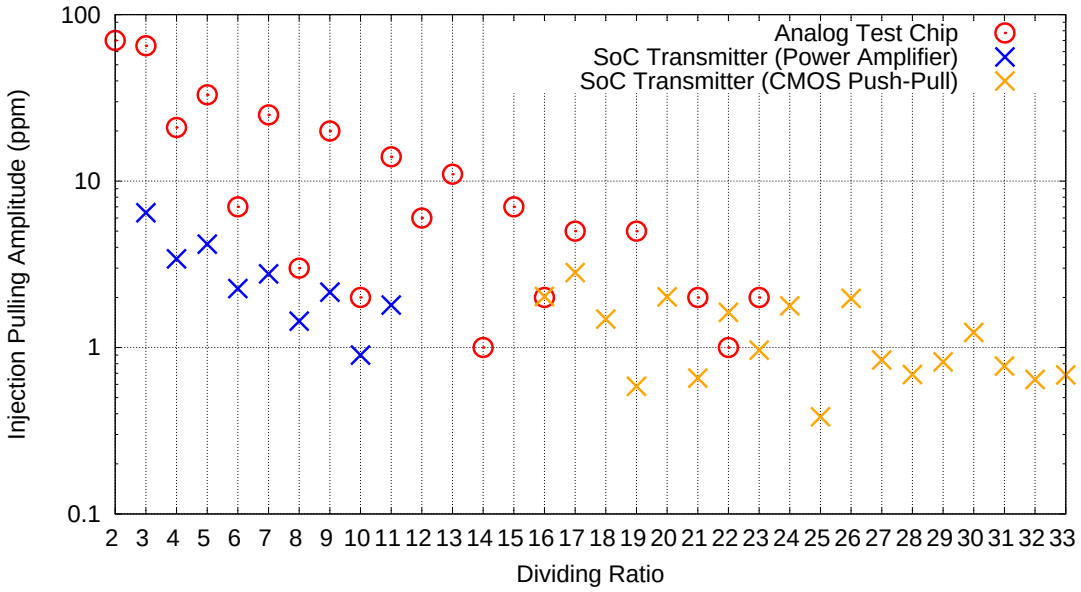

Figure 4.14: Measured injection pulling amplitude as a function of the dividing ratio: The values are measured for the analog test chip as well as for the SoC transmitter. Using a low harmonic differential current PA, injection pulling effects can be significantly reduced in the SoC transmitter for high frequency operation (low dividing ratios).

For an operation as a sub-GHz transmitter, injection pulling can be critical even under usage of the low harmonic differential current PA. However, in practice, an odd integer dividing ratio is never obtained for the frequency range between 868 MHz and 960 MHz considering the frequency variations of the LCO. Also, for lower frequencies of up to 434 MHz, a higher PA current transition time can be used, so that injection pulling effects are further attenuated.

4.6 Phase Noise and Jitter

Phase noise and jitter are important parameters for a frequency reference. As elucidated in Sec. 3.2, the SoC transmitter developed in this work generally supports two operating modes. It can be operated as frequency reference for frequencies up to 180 MHz or as a wireless sub-GHz transmitter for frequencies up to about 1 GHz using the integrated PLL.

During an operation as a frequency reference, the output frequency is generated using the fractional frequency divider (see Sec. 2.3). As a consequence, a considerable amount of phase noise is added to the LCO phase noise by the fractional frequency divider. Figure 4.15 displays the single side band (SSB) phase noise PSD measured at an output frequency of 100 MHz. The phase noise at low offset frequencies of the carrier is dominated by the LCO phase noise scaled

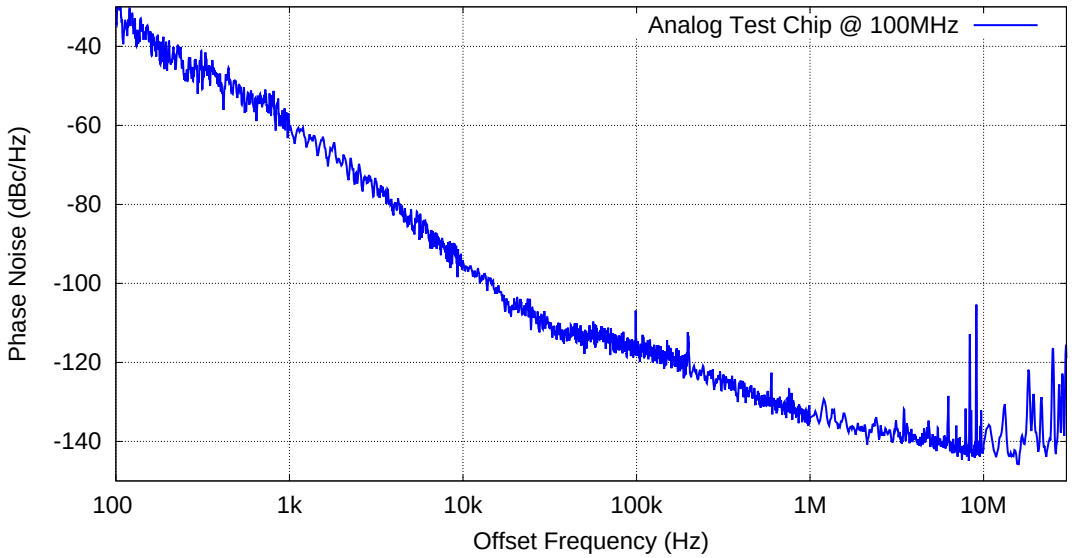

Figure 4.15: SSB phase noise PSD measured at a 100 MHz carrier: spurious tones occur and degrade the phase noise performance at high offset frequencies

to the respective output frequency. An additional phase noise is introduced by the fractional frequency divider referable to a quantisation jitter as well as a mismatch and jitter from the delay line, which is used for the phase interpolation in the employed fractional frequency divider architecture (see Sec. 2.4.5). This phase noise occurs at high offset frequencies of the carrier in the shape of spurious tones in the spectrum and as increased noise floor. The corresponding integrated RMS jitter measured over a bandwidth of 12 kHz to 20 MHz amounts to 4.7 ps. Apart from phase noise, the period jitter is an important characteristic value for different timing applications. Figure 4.16 shows the jitter histogram measured at 100 MHz. The period jitter has been measured at different dividing ratios and can range from 3 ps for integer dividing ratios up to 12 ps in the fractional operation mode. The RMS period jitter of 12 ps is higher than in related LCO frequency reference devices (see Sec. 1.3.2), which are employing integer dividers. As expected, the fractional divider used in this work comes along with a degraded but still acceptable period jitter performance.

For an operation as a wireless sub-GHz transmitter, additionally to the fractional frequency divider the phase noise is influenced by the PLL characteristic. As the phase noise scales with the carrier frequency, the phase noise has been measured at the highest frequency typically used in sub-GHz applications amounting to 868 MHz. Furthermore, different PLLs are implemented in the analog test chip and the SoC transmitter, respectively. Figure 4.17 shows the measured SSB phase noise PSD of the SoC transmitter at a carrier frequency of 868 MHz. The loop bandwidth of the PLL has been adjusted to 3.2 MHz for an optimal performance. At low offset frequencies, the phase noise is determined by the LCO phase noise, while for higher offset frequencies above the PLL bandwidth, the ring oscillator based VCO produces additional

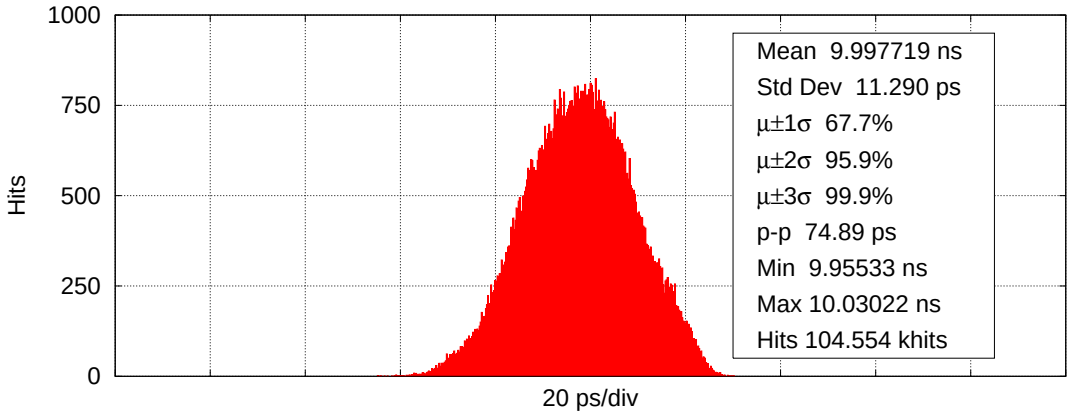

Figure 4.16: Period jitter histogram measured at 100 MHz; depending on the dividing ratio different period jitter values and also non-Gaussian distributions can be observed

phase noise. For comparison reasons, the phase noise of the analog test chip is also plotted. Furthermore, the data sheet values of the phase noise are plotted for the SI4010 and for the TDA5150. At an offset frequency of 10 kHz, a low phase noise of -80 dBc/Hz is achieved with the SoC transmitter, which is comparable to the quartz crystal based transmitter TDA5150. Also, at low offset frequencies in comparison to the analog test chip an improvement has been achieved due to the additional aluminium top metal layer used in the inductor of the SoC transmitter (see Sec. 3.2). The significantly lower phase noise in comparison to the LCO based transmitter SI4010 is assumed to be attributable to the nonexistent lossy trimming components of the exploited architecture of the SoC transmitter (see Sec. 2.3). In the range between 10 kHz and 1 MHz a phase noise performance is achieved, that is similar to the SI4010 and significantly better than the TDA5150. For offset frequencies higher than 1 MHz, the SoC transmitter and the analog test chip achieve only a low phase noise performance, which is caused by the high phase noise of the ring oscillator based VCO as well as the required high loop bandwidth.

4.7 Summary

Chapter 4 presents the methods, which have been applied for the calibration of the analog test chip as well as the SoC transmitter, realised in this work. For a high volume production, the key requirement to the calibration process is to keep the calibration effort low. Compared to the design of the all CMOS frequency reference chip, the development of such a calibration method can also be considered a challenging task. A test setup has been developed for automatic cali+bration and measurement, as a high number of devices must be tested to obtain a statistically significant result.

The analog test chip has been calibrated, using a temperature sweep over the entire operating

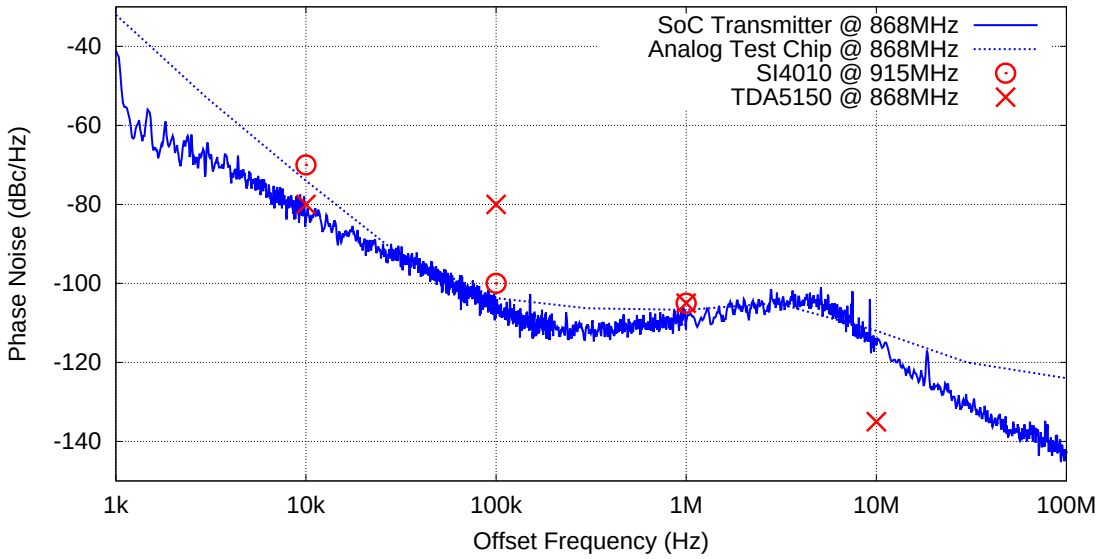

Figure 4.17: SSB phase noise PSD at a carrier frequency of 868 MHz measured for the SoC transmitter and the analog test chip: For comparison reasons, the datasheet values for the phase noise of the Silicon Labs SI4010 [58] device and the Infineon TDA5150 [89] device are shown in the figure.

temperature region. However, such a calibration method is impractical and not suitable for a high volume production. As described in Sec. 4.1.4, measurement results using a process sensor revealed that the temperature characteristic of the LCO frequency varies in a well defined way. Based on this knowledge, a calibration method has been developed, which only requires two temperature insertions. Using this two temperature insertions, the calibration of all required parameters, including the oscillator amplitude, the LCO frequency versus temperature, and the mechanical stress compensation can be performed. The calibration method has been applied to the SoC transmitter, yielding a high initial frequency accuracy of 52 ppm. As a result, a minimization of the required calibration effort can be achieved, suitable for a high volume production.

Furthermore, Chapter 4 presents, several measurement results. Measurements, investigating the sensitivity to environmental effects caused by package and humidity are separately investigated to mechanical stress. It has been demonstrated, that the major portion of moisture and package induced frequency errors is attributable to mechanical stress rather than to other related effects. This finding is confirmed using the standard reliability tests HAST and HTOL. Several calibrated devices have been exposed to this two standard reliability tests. The results are summarised in Table 4.3 with the stress compensation turned on and off, respectively. Similar to previous work [38], HAST has led to the highest frequency error when the stress compensation is turned off. However, a significant reduction of this error can be achieved with the stress compensation.

Finally, based on the standard reliability tests and the initial frequency accuracy, the overall frequency accuracy over lifetime is estimated. Similar to state-of-the-art LCO based all CMOS frequency references (250-300 ppm) [38], [56], an overall frequency accuracy of about 204 ppm can be achieved without stress compensation. Using the stress compensation, however, an overall frequency accuracy of 136 ppm can be achieved, which is significantly better than state-of-the-art.

Chapter 5

Conclusion and Research Summary

A highly stable frequency reference is required in many electronic devices. Traditionally such frequency references have been realised using a quartz crystal. However, high requirements on size and cost have led to the development of silicon based frequency references for crystal replacement. Previous work focused on MEMS based integrated frequency references. However, MEMS based frequency references are typically realised as a two chip solution using a MEMS resonator and an additional application-specific integrated circuit (ASIC), which contains the required CMOS circuit. Recent work has demonstrated LCO based all CMOS frequency references to achieve very high frequency accuracy, competitive to quartz crystals. This new technology for all CMOS frequency control has no need for a mechanical resonator and therefore achieves the highest possible level of integration. However, as LCO based all CMOS frequency control is a rather new technology, only little research has been done offering a huge potential for further improvements.

This thesis examines LCO based all CMOS frequency references for quartz crystal replacement to miniaturise the size and to reduce the costs for SoC devices. Next to state-of-the-art architectures for this technology, a new architecture is presented in this thesis. Throughout the course of this theses, several test chips have been manufactured based on this architecture. The final device constitutes a SoC transmitter suitable for a sub-GHz wireless operation. For the SoC transmitter, a calibration method has been developed, suitable for a high volume production. Furthermore, a mechanical stress sensor is used in order to reduce mechanical stress induced frequency drifts over lifetime.

Chap. 1: Introduction

This chapter deals with highly stable frequency references commonly used in electronic devices. Next to the quartz crystal a comprehensive overview of state-of-the-art silicon based frequency references is given in this chapter, including MEMS based frequency references and all CMOS frequency references. All CMOS frequency references refer to devices entirely realised in a standard CMOS technology. They can further be separated in RCO and LCO as well as electro thermal frequency references. This thesis is focused on LCO based all CMOS

frequency references as they can provide the highest frequency accuracy. Consequently, a more detailed overview is given for this particular technology, comprising the introduction of the different architectures as well as a performance comparison of the state-of-the-art. Furthermore, mechanical stress compensation is introduced, which has been successfully applied in previous work on integrated Hall based current sensors and potentially can also improve the frequency accuracy of LCO based all CMOS frequency references.

Chap. 2: Frequency Reference Concept and Design

This chapter relates to the concept and design of an LCO as a frequency reference for quartz crystal replacement. Starting with a consideration of CMOS technology scaling as an enabler for the LCO based all CMOS frequency reference technology, this chapter further includes a theoretical consideration of different frequency error mechanism, which are relevant for the design. In previous work, only PVT effects have been considered for the CMOS design. Next to process variations, the major relevant effect considered in this chapter is the LCO temperature characteristic. Additionally, in LCO based all CMOS frequency references several rather unique effects must be taken into account, including environmental effects like magnetic or electric interaction between the LCO inductor and the environment of the chip. Furthermore, mechanical stress caused by the package and humidity can have a significant influence on the LCO frequency.

Optimised for a high frequency accuracy, a new approach for an LCO based all CMOS frequency reference is introduced, on which this theses is based on. It uses a non-trimmable LCO and a fractional divider in order to provide a variable and temperature compensated reference frequency. As no lossy and non-linear trimming components are required, a very robust design can be created based on this approach. Additionally, this approach inherently provides a field programmability of the reference frequency making it suitable for a wireless operation.

For the chip realization based on the non-trimmable LCO approach, a comprehensive overview of the design and the theoretical considerations relevant for the design is given. The most important parts of the circuit are presented in more detail including the free running LCO, the sustaining amplifier, the automatic amplitude control, as well as the fractional interpolating frequency divider.

Chap. 3: Chip Architecture and Development

Several test chips have been manufactured as part of this theses. This chapter specifically deals with the architecture and the development of these chips. As a first prototype for proof of concept, an analog test chip has been developed. In order to keep the development effort for this chip low, the main focus has been on the critical analog components. The required

digital functionality has therefore been performed using an external microcontroller. Three versions of this analog test chip have been manufactured including continuous optimisations of the analog components. Based on the insights of the analog test chip, a SoC transmitter has been developed, which includes a digital core for all the required digital functionality. Furthermore, a mechanical stress sensor has been implemented on the SoC transmitter as previous measurements with the analog test chip showed mechanical stress to be the major frequency error mechanism. The SoC transmitter is fully integrated in a standard CMOS process and therefore achieves the highest possible level of integration with a minimum number of required external devices.

Chap. 4: Calibration Methods and Measurement Results

This chapter deals with the calibration process and measurement results for the analog test chip and the SoC transmitter. A simple calibration process is mandatory, so that it can be applied with minimum costs in a high volume production. The frequency calibration of the devices versus temperature is particularly critical, as the LCO has a very strong temperature dependency including higher order effects. However, considering the mechanism underlying the temperature characteristic, a two point calibration method has been developed for the SoC transmitter. Measurement results show this calibration method to be very robust achieving a high initial calibration accuracy of 52 ppm. Furthermore, as a good correlation has been found between the LCO frequency and the mechanical stress measured by the stress sensor, in this theses a mechanical stress compensation for an integrated LCO based all CMOS frequency reference is demonstrated for the first time. For that reason, a calibration method has been developed for the stress sensor including a temperature compensation for every device separately, which can be performed with the same temperature insertions as for the temperature compensation. Additionally, the calibration for the sensitivity of the LCO frequency to mechanical stress has been performed. As the same sensitivity is expected for every device, this sensitivity only has to be determined once and can then be used for every device. Additionally to the calibration parameters and the corresponding measurement results, this chapter presents measurement results for several interesting parameters and effects including, environmental influence of package and humidity, ageing related frequency drifts, injection pulling and modulation, and phase noise and jitter.

Future Work

The SoC transmitter presented in this thesis constitutes an example for miniaturization and cost reduction. Although previous work like the Silicon Laboratories SI4010 chip [58] already offer a crystal less wireless transmitter functionality, a more robust solution has been achieved in this thesis by shifting some of the functionality from the analog to the digital side. Instead of analog frequency trimming and a sophisticated self calibration process as it is applied in the

SI4010, a fractional PLL is used in the SoC transmitter to generate a variable and temperature compensated frequency.

However, in order to increase the performance of the presented prototype, further improvements have to be done in the future. A CMOS process offering thick metal layers with several μm of copper will allow the design of a high Q-inductor. Such a design will decrease the temperature coefficient of the LCO frequency, consequently simplifying the calibration process and improving the frequency accuracy.

Although the mechanical stress compensation significantly improves the overall frequency accuracy to 136 ppm, the desired value of 100 ppm has not been achieved in this work. Considering Table 4.3, it can be observed that an overall frequency accuracy well under 100 ppm would be achievable without the HTOL induced frequency error. Further investigations concerning the sensitivity to HTOL will consequently be performed in the future.

In the SoC transmitter, a power consumption similar to the SI4010 and slightly higher than in state-of-the-art quartz crystal based devices [89] has been achieved. For future work, a similar approach with a sigma delta fractional divider instead of the fractional interpolating frequency divider could help to obtain a power consumption closer to the quartz crystal based devices.

In addition, a further development of a fully integrated SoC crystal-less transceiver is feasible as the transmit functionality demonstrated in the SoC transmitter is considered to be more critical and thus no obstacles are expected for the implementation of a receiver.

Symbols and Acronyms

$-g_{\mathbf{m}}$ negative transconductance

$C_{\mathbf{gb}}$ gate-bulk capacitance

$C_{\mathbf{gc}}$ gate-channel capacitance

$C_{\mathbf{gd}}$ gate-drain capacitance

$C_{\mathbf{gs}}$ gate-source capacitance

$C_{\mathbf{ox}}$ oxide capacitance per unit gate area

E elasticity modulus

I current

J jitter

$J_{\mathbf{P}}$ period jitter

Q quality factor

T temperature

TC temperature coefficient

T_P period time

V voltage

ΔN number of periods

Δt time interval

$\mathcal{L}$ phase noise

$\mathcal{L}(f_{\mathbf{o}})$ single side band phase noise at offset frequency f_{o}

μ mobility

ω angular frequency

σ mechanical stress

ε mechanical strain

f frequency

$f_{\mathbf{res}}$ resonance frequency

l transistor length

w transistor width

ADC analog to digital converter

ASIC application-specific integrated circuit

ASK amplitude shift keying

balun balanced-unbalanced

BAW bulk acoustic wave

C capacitor

CMOS complementary metal-oxide semiconductor

DAC digital to analog converter

DUT device under test

EEPROM electrically erasable programmable read-only memory

FSK frequency shift keying

GFSK Gaussian frequency shift keying

GPIO general-purpose input/output

HAST highly accelerated stress test

HTOL high temperature operating life

IC integrated circuit

IIR infinite impulse response (digital filter)

IoT internet of things

IP intellectual property

L inductor

LCO LC oscillator

LDO low-dropout (regulator)

LPF low pass filter

LSB least significant bit

MEMS microelectromechanical systems

MIM metal-insulator-metal

MOM metal-oxide-metal

MUX multiplexer

NRZ non-return-to-zero

NVM non-volatile memory

PA power amplifier

PCB printed circuit board

PFD phase frequency detector

PLL phase-locked loop

PMU power management unit

ppm part per million

PSD power spectral density

PTAT proportional to absolute temperature

PVT process, voltage, and temperature

R resistor

RCO RC oscillator

RF radio frequency

RMS root mean square

ROM read-only memory

SAR successive approximation register

SFR special function register

SMD surface-mount device

SoC system on chip

SPI serial peripheral interface

SRAM static random-access memory

SSB single side band

TCXO temperature compensated crystal oscillator

USB universal serial bus

VCO voltage controlled oscillator

VPP vertical-parallel-plate

XO non-compensated crystal oscillator

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