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Development of a Post-Silicon Laboratory Verification Environment for an Automotive Batterymanagement IC

MASTER'S THESIS

to achieve the university degree of

Diplom-Ingenieur

Master's degree programme: Electrical Engineering

submitted to

Graz University of Technology

Supervisor

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Institute of Electronics

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Graz, Jannuary 2015

AFFIDAVIT

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Acknowledgments

Special gratitude belongs to Prof. Peter Söser from the TU Graz Institute of Electronics, for always finding the time when I needed a piece of advice, and for always giving me constructive feedback.

I would also like to thank Infineon Technologies Austria AG for giving me this unique opportunity to work on my thesis on a real application. I also want to thank the whole team of the Power Train Systems department for giving me the support and all the enriching discussions that helped me to gather a better understanding of electronics and battery management in electric vehicles.

My sincere gratitude here is dedicated to Ing. Karl Felber, who is part of this team at Infineon. He has always been a great mentor to me and taught me many important practical things from his huge experience in the field and beyond.

Finally, I want to express my deepest thanks to my whole family and especially my parents Rosemarie and Anton Hofinger, who have always supported me throughout my life. Without their help it would not have been possible for me to start my second course of studies in the city of Graz, which have greatly enriched my life.

Abstract, Kurzfassung

Abstract - English

One of the most important parts of an electric vehicle is the battery with its associated battery management system. Infineon Technologies Austria has developed an Integrated Circuit (IC) that dramatically eases the effort of building such a battery management system needed to supervise and balance the battery cells. In addition to its high precision, this IC offers the possibility of transferring energy between cells called "Active Balancing" with only a few external parts. This allows an extension of the driving range compared to standard "Passive Balancing", which is also supported.

Before an IC can be put into mass production, the correctness of its implemented functionality must be sufficiently verified. It is therefore necessary to operate the IC in an application-like environment with the desired modes of operation, and to check its behavior against various test scenarios.

In the scope of this master thesis a verification environment was created that allows functional and application-like verification measurements to be conducted on the TLE8000QK IC. The core of this environment, as well as of this thesis, is the so-called Verification Board, which can be seen on page 151. This provides all the required modes of operation for the IC and allows various kinds of measurements to be conducted, with both internal and external equipment.

After a first introduction to the topic, this thesis starts with the gathering of requirements for the verification environment. This is based on the IC's specification and on findings from the verification of a previous test chip.

The main part of this thesis then focuses on the actual implementation, starting with the investigations and upgrades of previously insufficient external equipment. Then the development of a "High Precision Battery Simulator" (HPBS) will be shown in detail. Its development was also used to test various concepts for achieving high accuracy, which were later used for the verification board. This device is a galvanically insulated cell with a typical accuracy of 180 µV in a temperature range from 5 °C to 45 °C and very fast reaction to load changes up to ±50 mA. The last part of this thesis focuses on the implementation of the actual verification board, with its numerous functions needed for the verification of the TLE8000QK.

The verification environment presented in this thesis has already been used to successfully conduct hundreds of verification measurements of the IC.

Kurzfassung - German

Einer der wichtigsten Bestandteile eines elektrisch angetriebenen Fahrzeugs ist die Batterie mit dem dazugehörigen Batteriemanagementsystem. Infineon Technologies Austria hat einen IC entwickelt, der den Aufwand zum Bau eines solchen Batteriemangementsystems wesentlich vereinfacht. Neben seiner hohen Präzision bietet dieser IC die Möglichkeit des "Active Balancing", das Energietransfer zwischen den Zellen mit nur wenigen externen Bauteilen ermöglicht und somit die Reichweite gegenüber dem ebenfalls unterstützten "Passive Balancing" erhöht.

Bevor ein IC in die Massenproduktion übergeführt werden kann ist es notwendig, dass die korrekte Umsetzung der Funktionen anhand von Musterexemplaren ausreichend verifiziert wird. Dazu ist es notwendig, den IC in einer applikationsnahen Umgebung in den verschiedenen geplanten Betriebsmodi zu betreiben und sein Verhalten in diverse Test-Szenarien auf Korrektheit zu analysieren.

Im Rahmen dieser Masterarbeit wurde daher eine Verifikationsumgebung geschaffen mit deren Hilfe funktionelle und applikationsnahe Verifikationsmessungen am TLE8000QK IC durchgeführt werden können. Der Kern dieser Verifikationsumgebung ist dabei das so genannte Verifikationsboard, das den Hauptteil dieser Arbeit darstellt. Dieses ermöglicht unterschiedlichste Arten von Messungen sowohl mit internem als auch externem Equipment, sowie die Bereitstellung der unzähligen Betriebsmodi, die dieser IC bietet.

Nach der Einleitung widmet sich diese Arbeit dem Bestimmen der Anforderungen für die Verifikationsumgebung, die sich durch die Spezifikation des ICs, sowie aus Erfahrungen bei der Verifikation eines vorangehenden Testchips ergeben.

Der Hauptteil dieser Arbeit widmet sich der eigentlichen Umsetzung. Dabei wird zuerst auf das Upgrade bisher nicht ausreichenden externen Equipments eingegangen. Im nächsten Schritt wird die Implementierung eines Präzisons Battteriesimulator Prototyps (HPBS, Seite 55) gezeigt. Dessen Entwicklung wurde zum Test diverser Konzepte zur Erzielung hoher Präzision verwendet, die später ebenfalls auf dem Verifikationsboard zum Einsatz gekommen sind. Er bildet eine galvanisch getrennte Zelle und bietet eine typische Genauigkeit von weniger als 180 µV in einem Temperaturbereich von 5 °C bis 45 °C sowie äußerst schnelle Ausregelung bei Lastsprüngen bis ±50 mA. Der letzte Teil dieser Arbeit bietet einen Einblick in die Entwicklung des eigentlichen Verifikationsboards mit seinen unzähligen Funktionen, die zur Verifikation des TLE8000QK umgesetzt wurden.

Durch die hier vorgestellte Verifikationsumgebung konnte bisher bereits mehrere hundert Verifikationsmessungen des TLE8000QK erfolgreich durchgeführt werden.

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1 Introduction

This chapter provides an introduction to the necessity of battery management for electric vehicles, specifies the role of the IC under test in a Battery Management System (BMS) and introduces to the main tasks of this thesis.

1.1 History

Fully electric vehicles are a possible candidate for future transportation systems, as they provide highly energy efficient means of transportation with hardly any emissions. Although a research boom has started in the recent past that brought some electric vehicles already to mass market[1], it is hard to believe that they have been around since the beginning of the automotive industry.

At the beginning of the 20th century, battery driven vehicles were more common and more robust than their counterparts with combustion or steam engines. They even were the first to reach the speed limit of 100 $^{km}/_{h}$ in 1899 [LL12]. But within the following decades, the scene changed completely as the infrastructure improved and the call for driving longer distances became louder. With the low energy density of batteries compared to that of oil, huge and heavy batteries would have been necessary to yield the same distances, as can be seen in figure 1.1. Furthermore, combustion engines had greatly improved, also with the invention of electric starters, and oil had become cheaper in the USA.
Soon the combustion engine became the standard for traveling and traction vehicles, whereas battery driven electric drive vehicles were only in use for special tasks like mining cars. [LL12; Sul04a; Sul04b; Dav97]

This picture remained quite constant until oil prices started to grow tremendously at the end of the 20st century. Car manufacturers again started to put more effort into the development of hybrid and fully electric vehicles. Although the energy density of batteries is still low compared to gasoline, it has already increased multiple times since 1900. Lithium Ion batteries have approximately 5 times the energy density of Lead-acid batteries [PI08, page 366]. Other material mixes, like the lithium-sulfur battery, are promising candidates for even higher energy densities in the future. Combined with highly efficient motors, power electronics

[1] For example Nissan Leaf, Renault Zoe, Ford Focus Electric, BMW i3, Mitsubishi i, Tesla Model S, Smart electric drive, VW e-Up!, and others

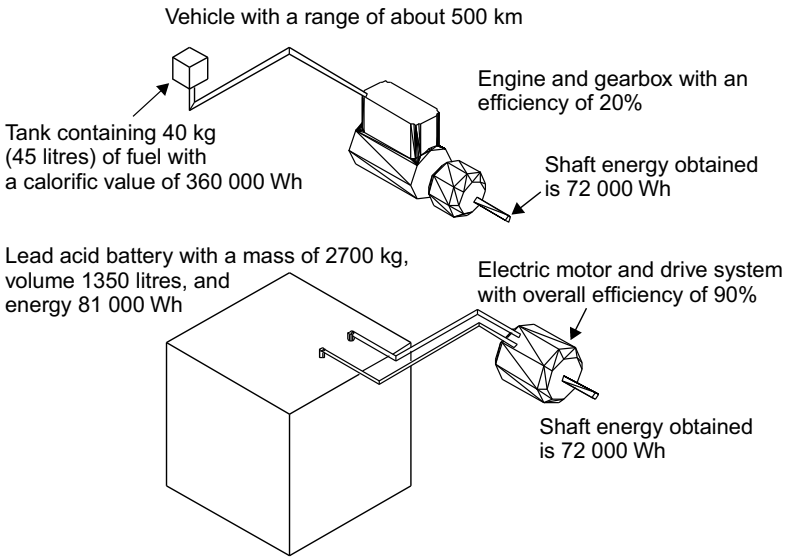


Figure 1.1: Electrical and petrol vehicle for 500km range [LL12, Figure 1.3]

and intelligent systems, that allow, e.g. regenerative braking, Lion Batteries are already in use for electric and hybrid cars today.

1.2 The need for Battery Management Systems (BMS)

But these new battery materials have drawbacks as well. Excessive care is necessary to prevent over- or undercharging, as this will lead to damages or, in extreme cases, even to thermal runaway with the risk of fire. As most applications require a huge amount of battery cells to provide the necessary energy, the effort to control and protect these batteries can grow tremendously as well.
For this reason battery management systems (BMS) have become an important and integral part of modern electric drive vehicles. Figure 1.2 shows such a BMS inside a typical power path of an electric vehicle.

Such a power path consists of an electric motor/generator with a power inverter, a charger, and the battery cells with sensors and supervisory circuitry. As previously stated, a huge number of batteries needs to be used to provide the energy needed for longer driving distances, and to deliver sufficient power for the motor. The commonly used way of connecting these battery cells is to stack them in series, to gain an increased stack voltage. This has various reasons.

First of all, whilst handling each cell separately could allow for individual and therefore optimal charging and discharging procedures, it also leads to uneconomic costs, volume and weight for the needed chargers and other electronic circuitry. Parallel or series connections allow the use of a single charger for multiple battery

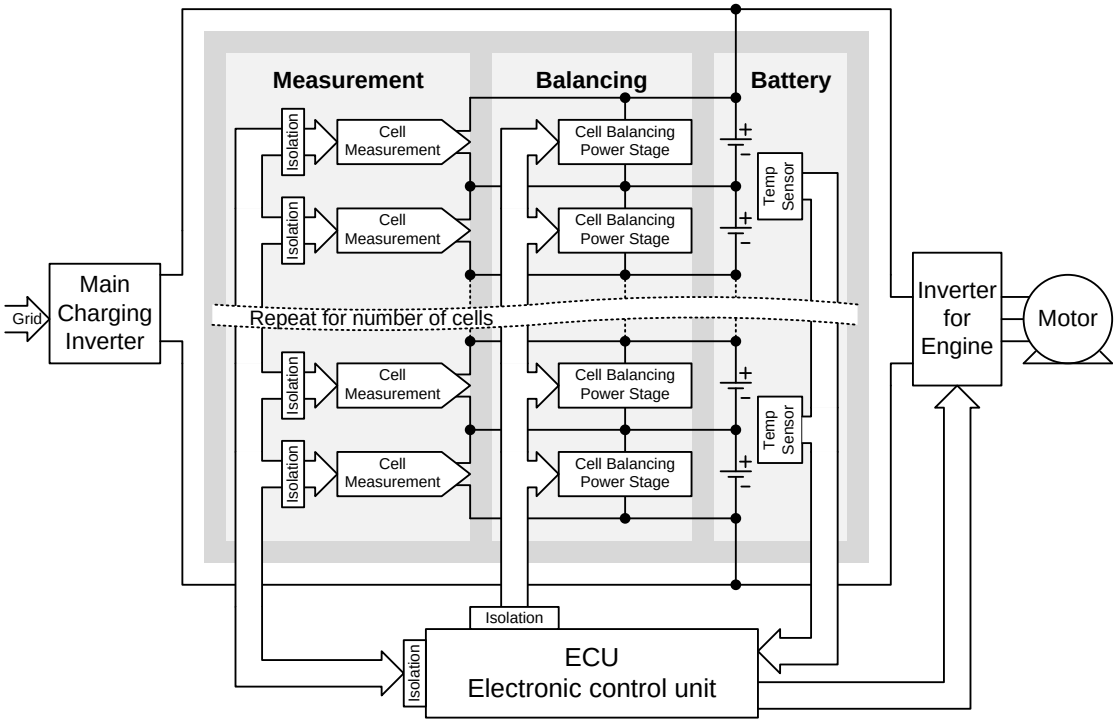


Figure 1.2: Example of a typical power path inside a battery-powered vehicle

cells at the same time.

Another point to consider is that a single battery cell has a relatively low voltage compared to needs of an electric drive engine that would be powerful enough to drive a vehicle. This means that, although a pure parallel connection of cells would theoretically be possible, it is not of practical interest as it would demand enormously high currents throughout the wiring and the inverter for the engine. These extremely high currents would lead to higher resistive power losses, as these scale with the square of the current. Hence stacking cells in series is common practice as it brings the stack voltage closer to that of the engine and lowers resistive losses, which yields a higher overall efficiency.

1.3 Balancing

However, this higher efficiency does not come without cost. As the battery cells are not completely identical, charging them in series with the same current does not necessarily bring them to the same cell voltage. Cells with higher capacity will end up with lower cell voltages than cells with slightly lower capacities. Furthermore, some cells will have a higher self-discharge rate than others. This means that not only the voltage of every single cell needs to be measured, but also some kind of balancing between the cells is necessary to allow full charging and discharging of

the stack, without the risk of damage or hazards.

Balancing, in practice, means that if only a single cell reaches its maximum rated voltage during charging, some portion of this cell's energy is being removed, to allow a continuation of the charging process until all cells reach their maximum limit. The simplest way of balancing is to dissipate the excess energy into heat using a resistor. This is called "Passive Balancing".

A more sophisticated way of balancing, called "Active Balancing", transfers this excess energy from the nearly full cell to the other, emptier cells, using switch-mode power-supply technology, which makes charging more energy efficient. Another benefit that comes with Active Balancing is the possibility of recharging nearly empty cells from other still full cells during discharge. This allows to draw as much energy out of a battery pack as possible. During driving, energy-saving technologies, like active-braking, switch between charging and discharging multiple times, hence often benefiting from every improvement in the charging process. This means that Active Balancing has the potential to increase the overall energy efficiency and therefore extending the vehicles driving range. More information on balancing in detail will be given in chapter 2.2.2. For more general information about various balancing techniques please refer to [Kai10],[BR09],[LMZ13] or [Ber01].

In general various electronic circuits are needed to achieve the required measurement, balancing and supervision tasks. These circuits can be built with multiple discrete standard parts, if no specialized devices are available. But it is also possible to build so called application specific integrated circuits (ASICs) that already contain most of the needed circuits. This also helps to minimize the overall system and assembly costs, because less parts are needed, which also helps to keep error possibilities small. But it requires that a high number of parts is being needed, so that mass production helps to spread the high development costs across all ICs.

1.4 The TLE8000QK Battery Management IC

The TLE8000QK is an Integrated Circuit (IC) that provides multiple features needed to build such an Active or Passive Balancing BMS in automotive applications with minimized hardware effort, as can be seen in figure 1.3. It is designed as a front end to allow a single microprocessor to control, supervise and balance up to several hundreds of battery cells. It incorporates cell voltage measurement, active and passive cell balancing front ends, temperature measurement, multipurpose inputs and outputs as well as an isolated communication interface needed to allow the base controller to communicate with multiple TLE8000QK ICs throughout the battery stack. Furthermore, this IC provides a patented Active Balancing technique that allows increasing battery capacity of a typical battery by approximately 15% [Inf] compared to standard Passive Balancing methods.

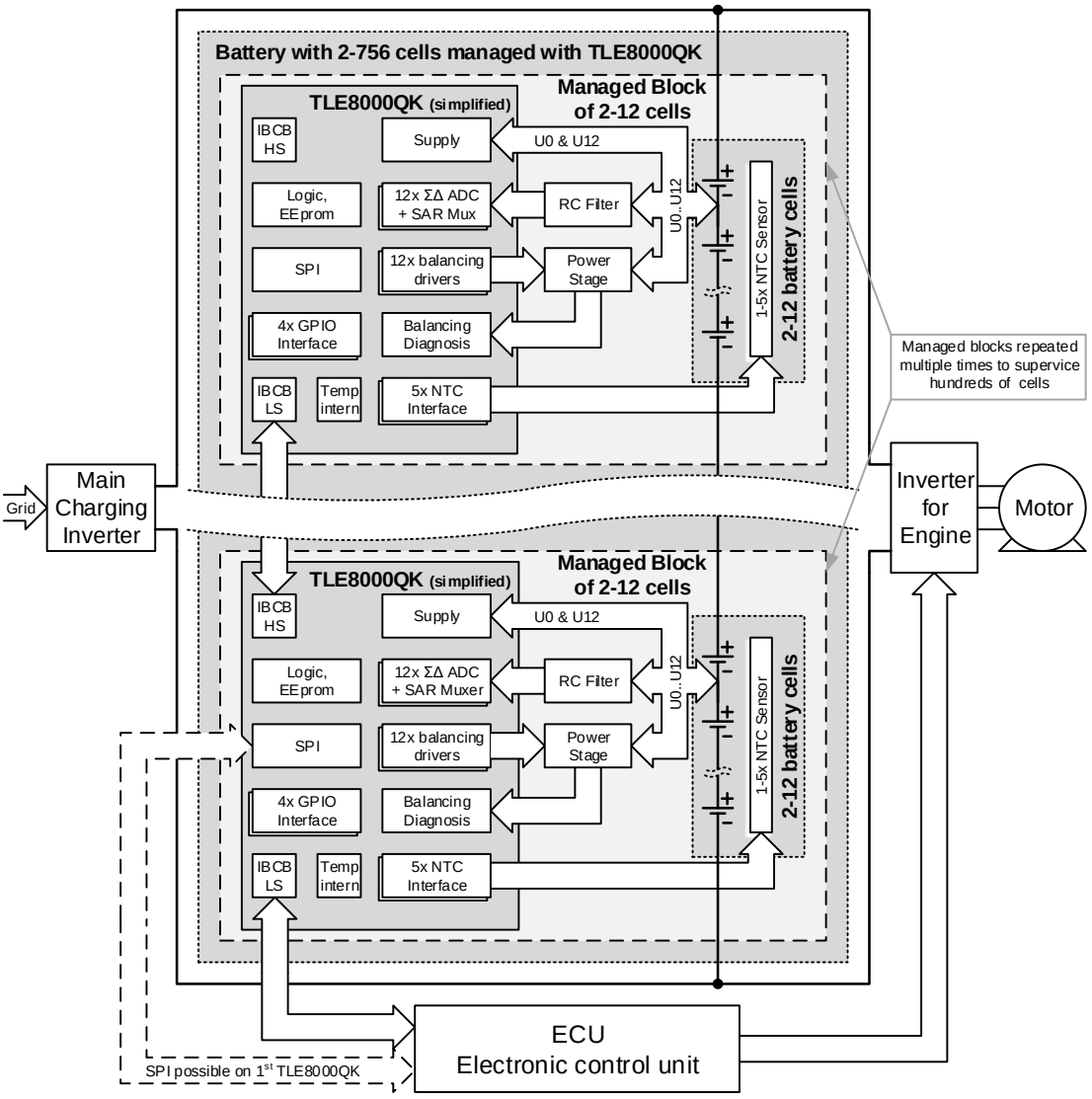


Figure 1.3: Example of a BMS with the TLE8000QK IC

1.5 Motivation

The above-mentioned TLE8000QK IC is a key element in simplifying the design of Active Balancing circuits for automotive batteries. It therefore has the potential to increase the usable energy of current battery technologies. This makes longer ranges possible or batteries with present-day ranges cheaper.

One important step in the development process of such an IC is to verify that all its embedded functions work as intended by concept and design, before it is put into mass production. This verification has to be done against all the conditions the IC has been designed for. Therefore such verification steps include simulation of operating states under varying environmental changes as well as simulation of specified fault conditions.

To perform all of the required verification work, special equipment is needed. Such equipment includes, for example, thermal forcing systems, verification boards with test circuits for IC communication, Active and Passive Balancing, and much more.

The tasks of this thesis therefore ranged from analyzing the type of equipment needed, comparison against existing equipment, acquisition, to the development of new equipment where necessary. The main emphasis here laid on the development of a so called main verification board that enables high accuracy measurements of the IC in various operation modes in application like conditions.

2 Requirement gathering for the verification environment

In this chapter the requirements for the verification environment are gathered and necessary tasks to implement are being defined. At the very beginning frequently used terms, like verification or testing, are defined and described in more detail. Then the gathering of information is done by first analyzing the IC to be verified as well as the equipment that was available during the start of this thesis project. At the end of this chapter, a short list summarizes the tasks for the implementation of the verification environment. The next chapter (3) will then describe the actual development of the verification environment as well as its outcome.

2.1 General introduction to the development of the verification environment

As the topic of this thesis is to develop a verification environment, one needs a clear understanding what is meant by verification and verification environment.

2.1.1 Terminology

Throughout different and closely related disciplines the same term may be defined with different meanings. The term verification, for example, may range from a pure simulational process, where it already overlaps with the design process, all the way to a real world measurement process that already overlaps with the process of testing.

This section will therefore define important terms like “verification” or “testing” before a typical verification environment can be described in the next section.

2.1.1.1 Differentiation between verification and testing

Verification

In the context of this thesis, verification in general shall be defined as the process of investigating if a Device under Test (DUT) behaves as intended by concept and

design and as declared in the specification. In contrast to testing, the process of verification not only tests specific functional blocks or parameters, but also the interaction of blocks in application-like conditions. However, as verification is a time-consuming process needed to find design or concept failures, it is done with a low number of already tested DUTs for each IC type.

Verification typically involves testing and/or simulating of all relevant functionality of the DUT under all expected environmental conditions. For further differentiation this term can be divided into pre- and post-silicon verification.

Pre-silicon verification

Before a chip's design data is sent to production, correct functionality can already be pre-verified to some extent. This can be done either in a virtual environment using simulation techniques, or even under partly real world conditions using special rapid prototyping boards with e.g. FPGAs. The advantage of such pre-silicon verification techniques is that bugs found can easily be fixed, as the production data is still changeable.

This technique is often used in digital logic design, where simulation times are shorter than in analog designs and prototyping systems with FPGAs can easily be built. But, especially in analog or mixed-signal designs, simulation-based pre-silicon approaches have to use simplified models of the IC under development to reach reasonable simulation times. And even though simplified models are used, simulations of processes that last fractions of a second in real world may take hours or even days to simulate. Therefore, only a subset of all the relevant cases may be able to be simulated in time.

Post-silicon verification

Once a new IC-type has gone through the production process for the first time, the correct functionality of this type has to be fully tested and verified before it can be released to mass production. In contrast to pre-silicon verification, the IC can now be evaluated under true real-world conditions without any simplifications given in the simulations. Especially, for larger systems this can lead to faster results than it would be possible with simulations. Having the real IC also allows its behavior to be analyzed under true application or application-like conditions. This often reveals parasitic aspects that have not been thought of, or have not been covered sufficiently within the models and have therefore not been represented by the simulations.

However, post-silicon verification also has limits, as not all signals can be accessed as in a simulation due to physical restrictions. Furthermore, bugs found at this late stage are more expensive to correct, as fixing them means to rebuild at least part of the masks needed for the production process.

Once a specific IC type is sufficiently verified, the design itself is considered correct and can be released to the next level in the mass production procedure. As each IC is basically a copy of the proven design, one only needs to ensure that the copy was manufactured correctly. This is done by individual analyses of each part against hardware defects, which is called testing.

Testing

In contrast to the previous verification process, testing is done on all ICs in the high production volumes. It is therefore required to keep a high test coverage at a lowest possible testing time. Fortunately, it does not have to be done on the entire IC as a system, as the concept is already verified, but rather on the individual building blocks that later create the functionality. This greatly reduces testing effort and time which is directly related to the cost of each IC.

For testing to be effective, it is necessary to ensure that:

- all building blocks involved in the ICs behavior are identified
- all identified blocks are verified to work correctly
- the block interaction is verified as well
- there is no cross coupling between blocks that prohibits independent testing
- the blocks are designed in such a way that no failure condition is undetectable by independent testing

2.1.1.2 An example of verification and testing

A good example to see the difference between verification and testing can be given on an IC implementing a digital state machine. Such a state machine normally consists of memory blocks as well as transition logic blocks. The memory blocks save the current state as well as other important data, whereas the logic blocks actually calculate the transition conditions.

During the verification process the memory and the logic blocks are first tested independently, to see if they were manufactured correctly. Then the actual verification starts that checks if the interaction of these blocks works. Various verificational tests have to be done to ensure that all states work correctly, can be reached in the intended manner, and that no unwanted states occur. This can be time-consuming especially if also faulty conditions have to be checked.

Once the verification has proven the design to work in all relevant conditions on selected samples, separate testing of the IC building blocks is used to ensure all mass produced ICs follow the design. In the testing case the internal memory blocks are tested independently of the logic functions to reduce test cases and

speed. For this, the memory blocks are being brought into a special scan-path mode, where all memory blocks are combined to form a giant shift register. This principle is used in, e.g., in the concept of scan-path testing [Sös10, page 135].

In summary, the concept of verification and testing follows the following idea: If it is known that the independent blocks a,b,c and d work, because they were tested, and it is known through previous verification that if a,b,c and d work a specific functionality is given, then it can be assumed, that the functionality is given in this particular IC although it was only tested but not verified.

2.1.2 The scope of this work

The scope of this work is to build a verification environment for the TLE8000QK IC, that allows to do reproducible verification work for nearly all required verification tasks. Furthermore, the environment shall support manual as well as partly-automated measurements under controlled and reproducible conditions. It shall also be expandable for similar types of ICs possibly upcoming in the near future.

Although this verification environment shall provide most features needed to do laboratory post-silicon verification on this IC, it is not required to provide absolutely all the functionality needed for a complete verification solely with this environment. For example, very specialized verification topics like EMC compliance tests, fully automated parameter tests or pure application tests can be omitted here, as they will be covered by separate environments, which are currently under development by other teams.

The following shall give an example, on how a typical verification environment may look like.

2.1.2.1 Description of a typical verification environment

In general a verification environment is a setup of specialized equipment needed to do the verification measurements. Figure 2.1 shows a block diagram of a typical setup used in the department of Power Train Systems of Infineon Technologies Austria. The main parts are a verification board with the DUT itself, various measurement equipment, equipment that simulates application and environmental conditions, communication interfaces and a Host PC.

Verification Board:

The core part of such a setup is a verification board that connects to the DUT either directly with a testfixture or indirectly via a DUT-board. The complexity of such a board differs widely, from a simple interface board to complex designs

2.1.2. The scope of this work

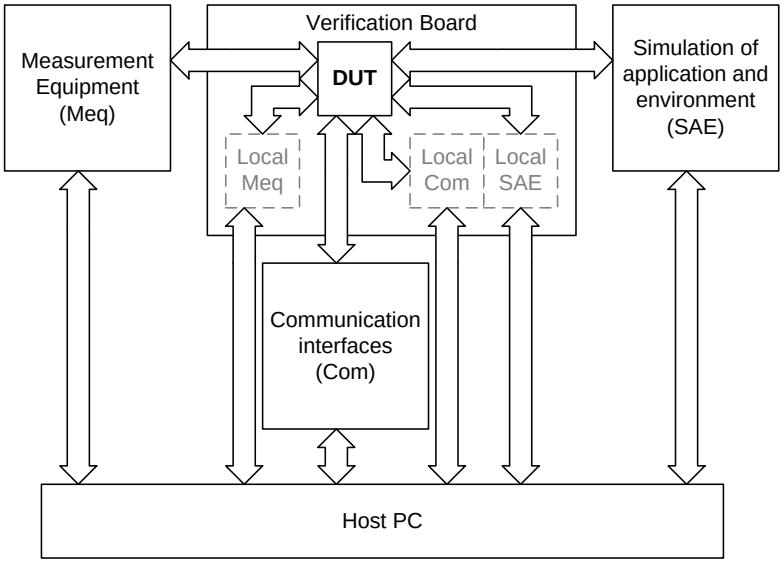


Figure 2.1: Blockdiagram of a typical verification environment

that already contains parts of specially developed measurement equipment or application related circuitry.

Measurement equipment

Typical measurement equipment includes electrical measurement systems like voltmeters, oscilloscopes, protocol analyzers, and so forth. But also physical quantities such as pressure or temperature can be of interest.

Simulation of application and environment

Especially, for ICs that were designed for certain applications it is necessary to verify the behavior under real-world application or application-like conditions. To do so the application might need to be simulated to allow investigations on specific conditions. Such simulation equipment may differ depending on the physical quantity to simulate. So for example inductors can be used as a replacement for electromagnetic actuators, or special controllable resistors to simulate temperature sensors. But also varying environmental settings such as pressure or temperature may be relevant directly and need to be applied to the device.

Communication interfaces

To enable communication with the DUT, all relevant interfaces have to be provided. This may range from simple direct inputs or outputs to high speed serial interfaces in various combinations.

Host PC

All of the abovementioned parts have to work together to be able to simulate various application-like conditions for the DUT. This can be controlled either manually on each piece of equipment separately, or remote via a host PC, depending on the equipment. The use of a host PC as an interface to the verification environment gives the opportunity to log and replay all manual steps as well as to completely automate verification tasks where needed.

As a result tests that might need to be redone multiple times but for example under varying temperature conditions can be redone much faster and even more reliable in an (semi-)automated way.

2.2 Investigations on the IC functions to verify

This section now focuses on the function the IC provides, as these need to be verified within the verification environment.

Please be aware that all presented numbers and data are based on preliminary values which were available during the development of this thesis. Those preliminary values were used to develop the verification environment, but do not necessarily have to be valid for the TLE8000QK on the date this thesis was published.

2.2.1 Overview of the TLE8000QK functions to verify

The first step in the development process was to get familiar with the IC the verification environment shall be designed for. Before each key feature of this IC will be presented and analyzed in detail, a short overview is given as a starting point.

Figure 2.3 shows the internal block diagram of the TLE8000QK IC in version A11. As already mentioned briefly in the introduction (chapter 1) this IC can be used in conjunction with a single micro controller to build up a BMS with very low additional hardware effort. Every single TLE8000QK is able to measure and provide the interface to balance a battery block containing 2 to 12 serially connected cells. In addition, a multiple of these managed battery blocks, each containing a TLE8000QK, can be connected in series to form battery stacks with even higher voltages of, e.g., some 400 V, as can be seen in figure 2.2. Although this results in completely different base potentials for the TLE8000QK IC inside each block, no active isolation components like opto-couplers or digital isolators are needed to allow communication between all the ICs. This is possible through a patented interface called “Inter Block Communication Bus” (IBCB), which uses simple passive capacitors as isolation interface.

2.2.1. Overview of the TLE8000QK functions to verify

Besides these basic functions, each TLE8000QK also provides additional features, needed in typical BMS applications. These include an interface for up to 5 NTC-temperature sensors, an internal temperature sensor, 4 general purpose input/outputs (GPIO), various diagnostic and safety functions as well as many other features that will all be discussed and analyzed in the next section. For further and even more detailed information than can be given in this thesis, please refer to the datasheet of the IC [AG13].

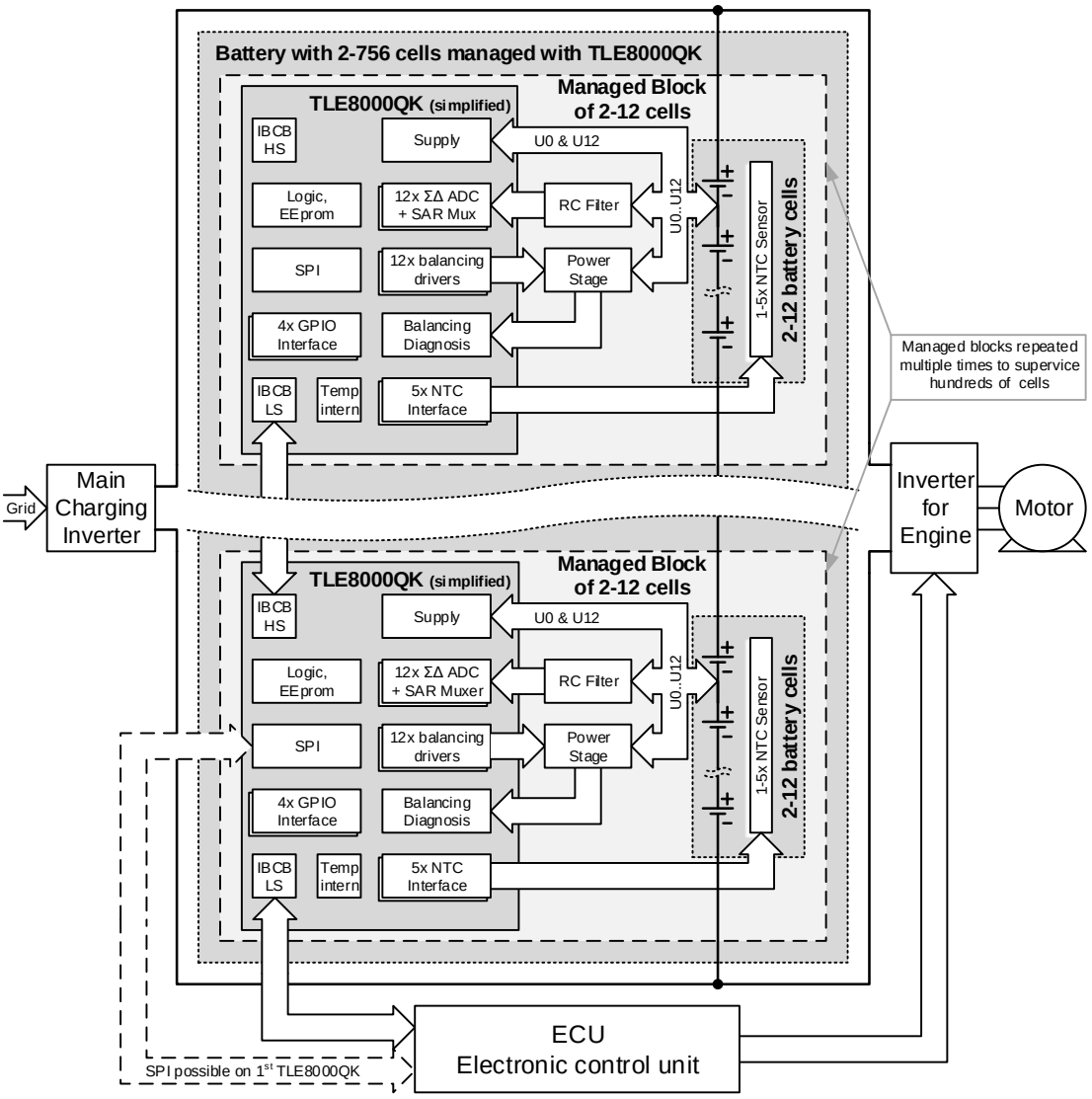


Figure 2.2: Stacking of multiple TLE8000QK ICs for high power applications like electric vehicles.

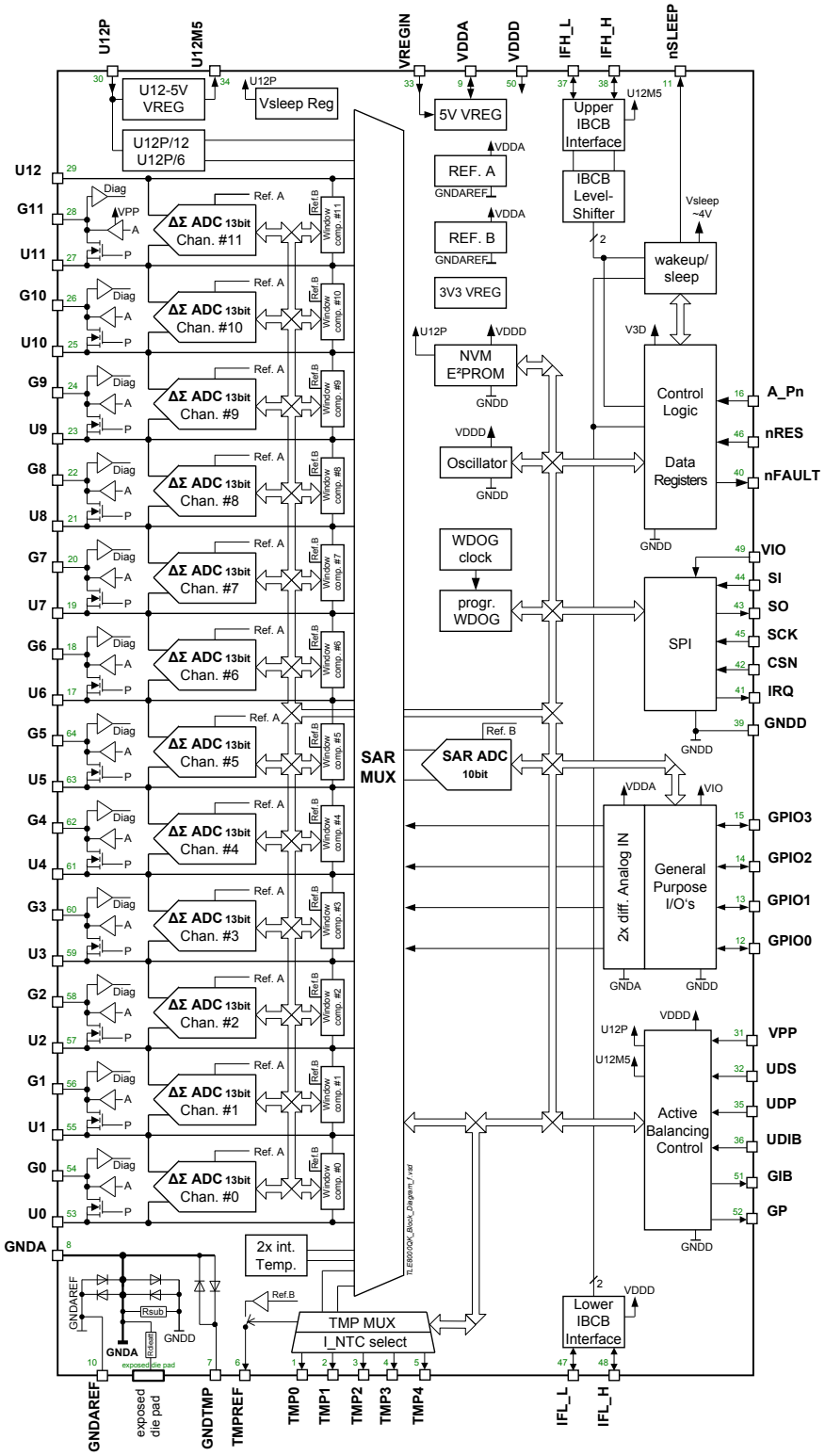


Figure 2.3: Preliminary overview of the TLE8000QK IC in version A11

2.2.2 Balancing interface

The balancing interface of the TLE8000QK is one of the core functions of this IC. It already provides many features needed to simplify Active as well as Passive Balancing designs. This means that balancing itself is done and supervised directly by the TLE8000QK, but configuration and activation of the energy transfer is still in control of the main BMS micro controller that commands the TLE8000QK.

The balancing hardware inside the TLE8000QK consists of 12 nearly identical stages that allow either Passive or Active Balancing. Each stage features a power MOSFET for Passive Balancing, and a MOSFET-driver stage for Active Balancing as well as diagnosis circuitry, as illustrated in figure 2.4. Furthermore, there is an additional sensing stage that can supervise the Active Balancing process and adjust switching times if needed.

As Active and Passive Balancing rely on completely different external hardware, the mode selection is also defined by external hardware in form of a pull-up or a pull-down resistor. This resistor is connected to the A_Pn pin of the IC and read out only once during startup.

2.2.2.1 Passive Balancing:

In standard Passive Balancing configuration, the external power stage can be as simple as a single power dissipation resistor per cell (see figure 2.4, left half).

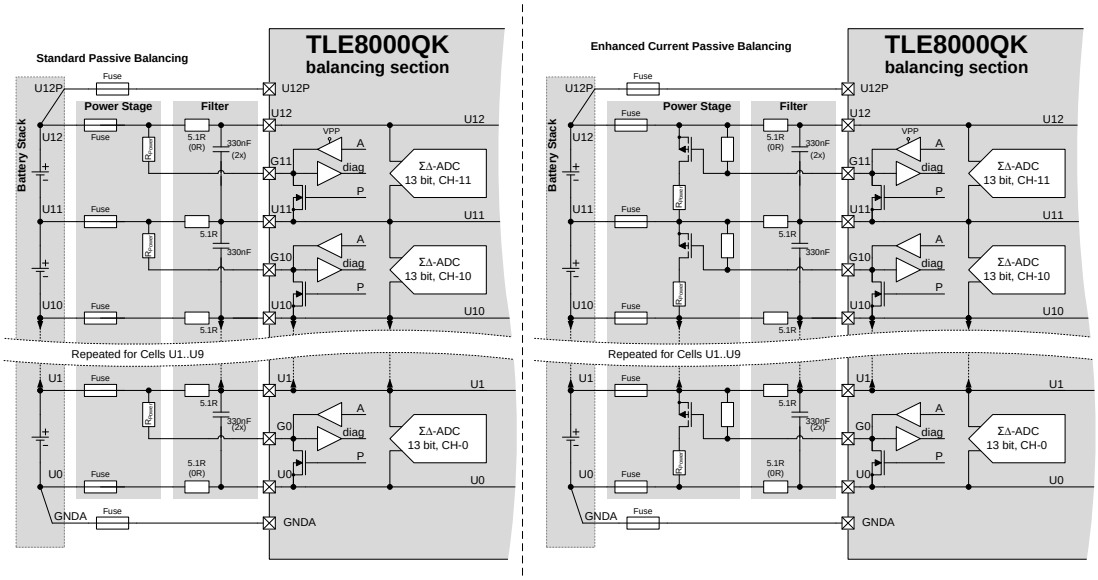


Figure 2.4: Passive Balancing; left: standard low current; right: high current

These resistors are placed between the Gx pins of the IC and the next higher cell voltage connection point. Each Gx pin - and so the balancing resistor - is

internally connected to the lower cell voltage connection point through a power MOSFET switch. These MOSFETs are each able to draw up to 200 mA and can be controlled completely individually. If for any reason, this balancing current should not be sufficient, external P-MOSFETs with pull up resistors can be used to drive even more powerful dissipation resistors, as can be seen in figure 2.4 on the right half.

If the TLE8000QK has started up in Passive Balancing mode, a diagnostic circuitry is enabled, that checks for various fault conditions on the Gx pins. These contain typical failures such as open load or short circuit cells.

2.2.2.2 Active Balancing

Introduction:

For Active Balancing configuration, a more complex power stage is needed. However, the TLE8000QK simplifies the effort needed to drive this stage. The basic idea is to build up a flyback converter[1] that allows energy transfer between single cells and the connected 2 to 12 battery cells. This can be achieved by having a special transformer with the primary side consisting of one coil connected to the whole battery stack, whereas the secondary side utilizes multiple coils that are each connected to their corresponding single cells. External MOSFETs are used to control the current flow in and out of the transformer coils to allow the power transfer between the different cells.

The MOSFETs as well as the transformer are simple external parts, whereas the complex driver and control circuitry is provided by the TLE8000QK. An illustration of the concept of such an Active Balancing circuitry is given in figure 2.5.

Active Balancing modes: Top, Bottom, Pre-charge bottom or Interblock

In Active Balancing mode, the TLE8000QK supports multiple balancing modes, allowing energy flow in several directions. This allows to support various charging and discharging scenarios.

- "Bottom Balancing" [ERF11] for example, can be used during charging to ensure to get as much energy as possible into the whole stack. This is done by moving energy with the main transformer out of the whole stack into a single partially charged cell.
- "Pre-charge Bottom Balancing" is a special version of the above, allowing to charge cells that are too empty to provide a minimum voltage to operate the integrated driver stage for the power MOSFETs. In this mode the cell

[1] A flyback converter is a simple kind of isolated DCDC converter that uses a transformer for energy storage as well as voltage transformation. For further explanations and examples please refer to standard literature, such as [TS09]

2.2.2. Balancing interface

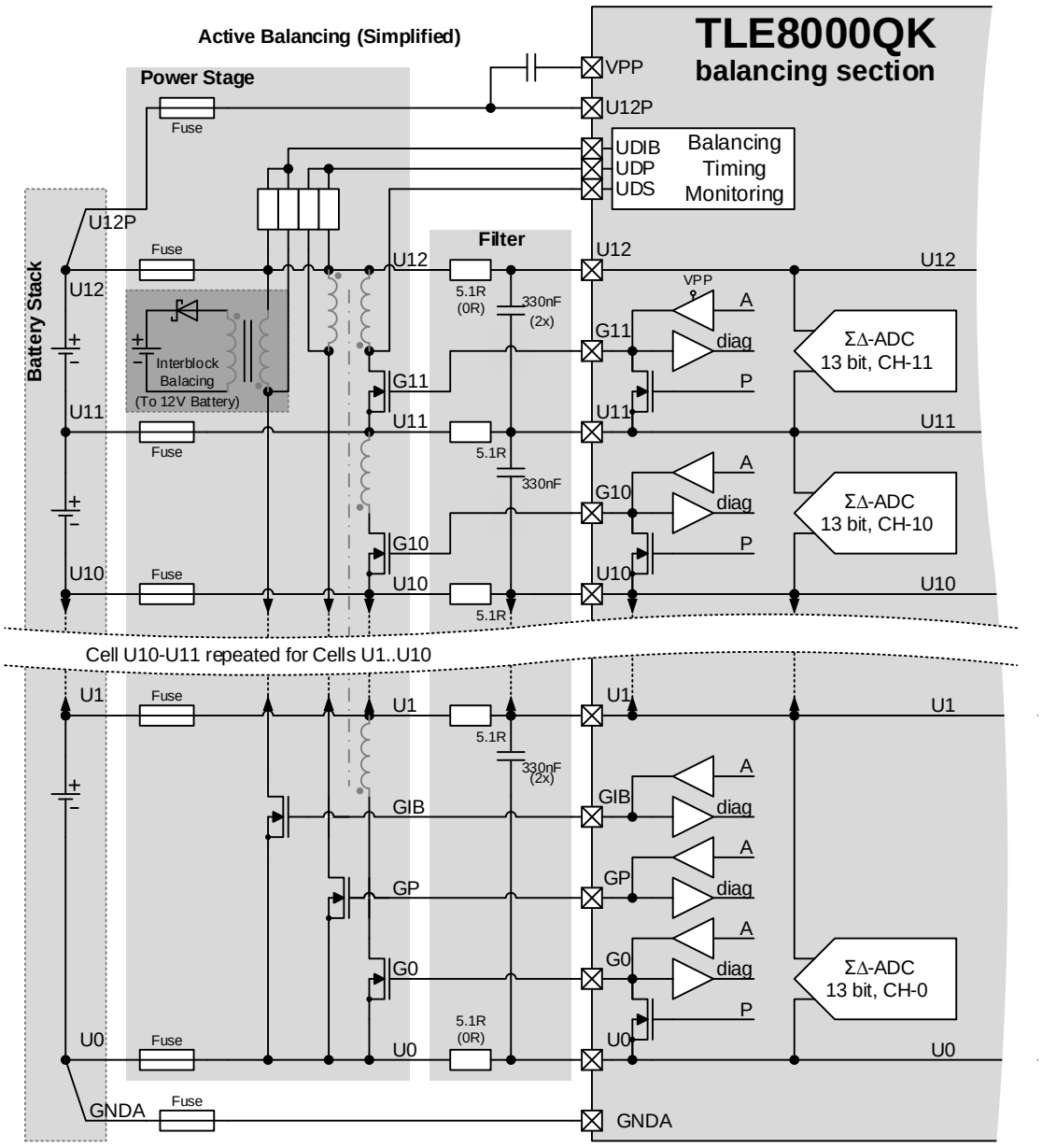


Figure 2.5: Simplified Active Balancing circuitry

with the lowest cell voltage throughout the stack gets automatically charged most, as the current runs through the bulk diode of the power MOSFET.

- "Interblock Balancing" allows to transfer energy from the battery stack to a completely different battery or battery stack. This can be necessary to prevent overcharging a battery that consists of multiple balanced stacks that are all connected in series. A possible target to transfer the energy to can be, e.g., the secondary battery providing 12V or 48V for consumer electronics in the vehicle. This requires an additional transformer, with high voltage insulation capabilities.

- "Top Balancing" [ERF11] can be used to retain as much energy out of the stack as possible during discharge. This is done by moving energy out of a single, not yet empty cell, to the whole stack using the main transformer.

As the basic concept for all these Active Balancing modes is based on a flyback design, the energy transfer always takes place in a two-step process. First, the transformer is being energized by connecting one side to either a single cell or the whole stack via a power MOSFET. Then this MOSFET turns off, which results in a reversed induction voltage, which forces the current to flow on the opposite coils of the transformer.

In standard Top or Bottom Balancing, this de-energizing current flow is running through a power MOSFET that is being controlled by TLE8000QK to act as an active rectifier for highest power conversion efficiency. In Interblock Balancing this secondary current flow is being rectified by a passive diode only. This is also true for Pre-charge Bottom Balancing, where the reverse diodes of the secondary MOSFETs are used, to allow current flow. This however, reduces the amount of energy reaching the battery in Pre-charge mode, due to losses in the power MOSFETs reverse diode.

Active Balancing timing and safety features

As in any DCDC converter design, timing is key to achieve correct function of the flyback converter. This is especially true since MOSFETs are used as active rectifiers to achieve high efficiency. Depending on the phase of the energy cycle, too long On-times of the MOSFETs can have various negative effects. In the first phase of charging, an oversized On-time will bring the transformer's ferrite core to a saturation condition. This will further result in excessively increased currents than can even damage parts of the circuitry. In the second phase of discharging, a too long On-time will result in re-energizing the transformer again once the original energy was effectively transferred. This is not even unwanted, but also highly counterproductive to the desired balancing behavior as it moves energy back and forth, lowering overall efficiency.

To avoid problems that may occur due to incorrect timing setup, the TLE8000QK controls some timing settings fully automatically and supervises user settable timings. The IC is able to do this by analyzing the transformer voltages in comparison to U12. During correct operation these voltages follow a deterministic pattern, which enables the IC to correct timing violations immediately. The voltage measurement points can be seen in figure 2.5.

For example, the user is able to set the transformer charging time, which corresponds to the amount of energy transferred. If this time is set too long, the transformer starts to run into saturation and changes its voltage patterns. As soon as this is detected by the IC, it turns off the charging and reports an error. The discharge time on the other hand is fully controlled by the IC's sensing

capabilities and doesn't even allow user adjustment.

If multiple of these energy transferring balancing cycles are needed, they normally start as soon as the preceding cycle has finished, which ensures highest speed. The IC also features the possibility to use a longer, but fixed time interval for the start of such a cycle. This eases EMC design as fixed switching frequencies are easier to handle with filters.

Other standard safety features available in Active Balancing mode include 'Short-to-Bat' or 'Short-to-Ground' detection for the gates of the MOSFETs.

For more information about safety, timing, or the actual used waveforms, please refer to the datasheet of the TLE8000QK IC [AG13].

2.2.3 Measurement capabilities of the TLE8000QK

2.2.3.1 Overview

The TLE8000QK, being designed to be a front-end for a micro controller, does not only provide a balancing interface, but also various possibilities to measure different physical quantities important in a BMS. To do so it features 12 dedicated precision ΣΔ-ADCs for cell voltage measurement as well as a standard SAR-ADC for additional measurements. As the SAR-ADC is used for a variety of tasks it incorporates a multiplexer that allows routing to different measurement targets on, or off the chip. The 12 dedicated precision ΣΔ-ADCs are referred to as the primary ADC (PADC), whereas the multiplexed standard SAR-ADC is referred to as the secondary ADC (SADC).

The chip also features internal safety functions that constantly supervise some of the measured quantities. It is able to either flag warnings that can be checked by the micro controller or even, for example, automatically abort balancing processes if specific limits are exceeded.

2.2.3.2 Primary ADC (PADC) - Cell voltage Measurement

As cell voltage measurement is absolutely critical in a BMS, the TLE8000QK provides two independent ways of measurements. The standard measurement method uses the PADC and allows simultaneous high precision measurements on all cells.

For safety reasons it is also possible to qualitatively re-check those precision results with the medium precision SADC if desired. This allows detection and reporting of defects to any of the ADCs. To ensure safety, the PADC and SADC even rely on completely independent voltage references.

Primary ADC (PADC) Details:

The PADC's high precision ΣΔ-ADCs allow fast and simultaneous measurements on all battery cells, which can be triggered to start synchronously across the whole battery stack.

Besides its resolution of 13 Bit, it also features a relatively high DC accuracy of 1.5 mV. The input range is 0 V to 4.8 V which results in an LSB of approximately 586 µV. The conversation time is approximately 3.4 ms

As the ΣΔ-ADC principle relies on fast, precise switching and comparison of voltages with an LSB as low as 600 µV, the verification of the correctness of such precise behavior requires careful design and huge effort on both, equipment and setup. This is especially true if the gained results shall not only be "in specification" or "out of specification", but also reveal the root cause.

2.2.3.3 Secondary ADC (SADC) - multipurpose measurements

Besides the possibility to independently re-check the cell voltage measurements of the PADC, the SADC allows measurements of:

- up to 5 external NTC temperature sensors
- two internal temperature sensors
- up to 2 differential external voltages on the GPIO pins
- the voltage reference for the PADC, for cross reference checks
- other important chip voltages

Secondary ADC (SADC) - Details:

The SADC is a 10 bit SAR-ADC with dedicated multiplexer. The voltage range of this ADC will change automatically from 2.5 V to 5 V depending on the selected multiplexer position and signal source. For an FSR of 2.5 V the LSB results to roughly 4.9 mV. The conversion time is approximately 16 µs.

2.2.3.4 Cell voltage monitor

For safety reasons, the chip features a cell voltage monitor that supervises if the cell voltages remain within user definable limits. This is done by cyclic measurements of the cell voltages with the SADC and comparing them against the stored values. If these limits are reached, overvoltage or respectively undervoltage flags are set accordingly and balancing is stopped automatically.

2.2.3.5 Temperature measurement interface

To allow for temperature measurements with the SADC, the TLE8000QK features a special NTC-sensor frontend. This frontend allows measurement of up to 5 external NTCs using switchable precision current sources. It also provides automatic measurement range selection by increasing or decreasing the corresponding sense current. Furthermore, typical failures like overtemperature, short circuits or open wires can be detected and flagged automatically.

Besides this interface for external NTCs, the TLE8000QK also features 2 internal temperature sensors. One is located next to the 5 V regulator, and the other near the voltage reference of the PADC.

For more information about measurement capabilities of the TLE8000QK IC please refer to the ICs datasheet [AG13].

2.2.4 Communication interfaces

The TLE8000QK IC features multiple communication interfaces. Those include simple input output pins to flag special events as well as a standard SPI interface and a special communication bus, allowing communication between a single micro controller and multiple TLE8000QK ICs.

2.2.4.1 Inter Block Communication Bus - IBCB

The inter block communication bus (IBCB) is a differential, daisy-chainable point to point bus system with one master and up to 63 slaves. It allows command transfer and wakeup propagation throughout multiple TLE8000QK ICs residing on different base potentials within the high voltage battery stack. In contrary to standard isolated communication approaches, where opto-couplers, digital isolators or transformers are used, this interface solely relies on cheap passive capacitors for isolation. It allows for high speed communication with up to 1 MBit. In case of failure, DC isolation is still provided up to the voltage rating of the used capacitors.

Typical setup and Mastermode

A typical communication setup can be seen in Figure 2.6. To allow daisy-chaining the IC has two IBCB interfaces, one on the top side, and another on the bottom side. As the IBCB-interface is a special interface normally not present in standard micro controllers, the TLE8000QK can act as SPI to IBCB translation device if it is run in the so called “Master Mode”. However, this is only possible for the topmost or bottommost TLE8000QK and is decided during the startup sequence and the following enumeration procedure.

Physical and protocol layer

On the physical layer the bus uses differential voltage signaling, designed to work with standard twisted pair cables. As this is an asynchronous bus system each slave device needs to synchronize itself onto the incoming messages on the fly. This is ensured by a synchronization field at the start of each message.

There are different kinds of messages. Some are designed for a master to single slave communication. Others are designed to allow sending of broadcast messages to all slave devices at once, or to retrieve failure information from all slaves in one go. All of these messages are secured with cyclic redundant codes (CRCs) to ensure data integrity over the whole daisy chained bus system.

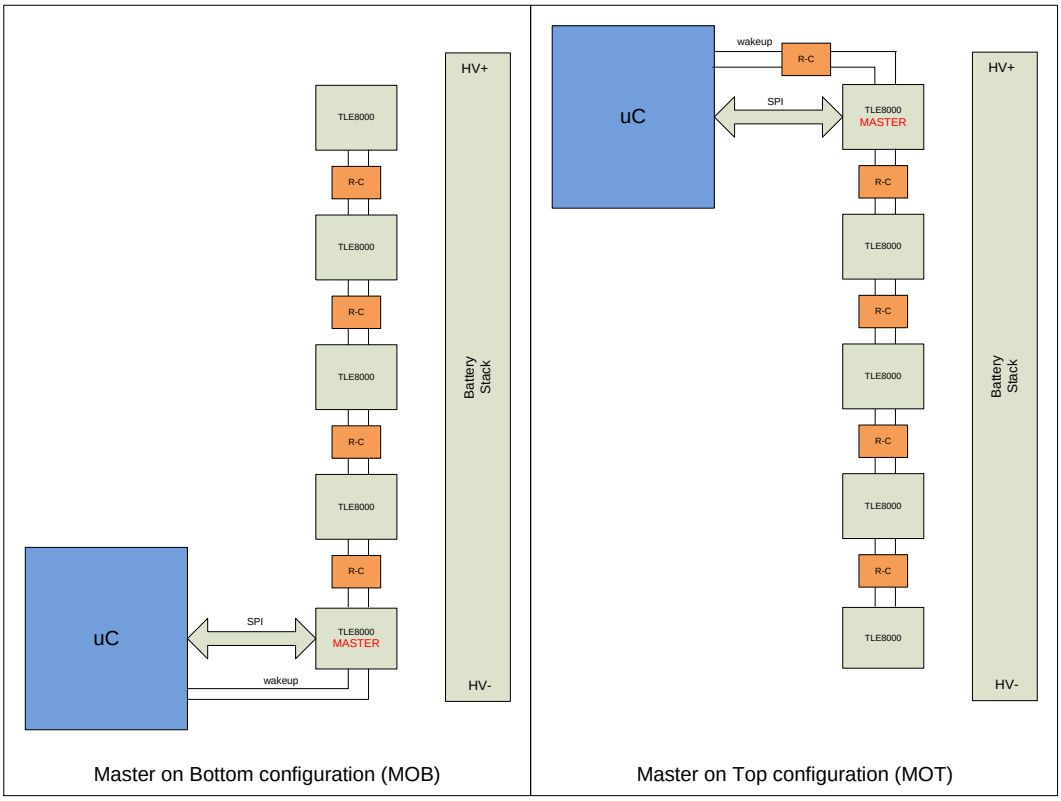


Figure 2.6: Standard daisychain configurations for the IBCB-interface. Source: [AG13, Fig15 & 16]

Wakeup sequence

In standard configuration a TLE8000QK IC will reside in sleep condition until a valid wakeup sequence is detected at one of its IBCB-interfaces. This feature results in power savings if the IC is currently not used. The wakeup sequence consists of a minimum of 8 differential pulses of $\geq 10\,\mu s$ pulswidth. This sequence can be generated, e.g., by toggling two output pins of the micro controller. Once the IC detects this sequence, it enables its internal voltage regulator as well as

the NSLEEP pin and starts to power up. Furthermore, the IC generates another wakeup sequence at the opposite IBCB-interface, to wakeup other possibly connected TLE8000QK ICs.

Redundant IBCB Connection possibility

Since the decision to define the master IC in the chain can be made every time the IC is woken up from sleep mode, it provides a possibility to change communication from the bottom to the top side with only slightly increased hardware effort as can be seen in Figure 2.7. This redundancy in the communication path provides safety in case of damage to the bus wire.

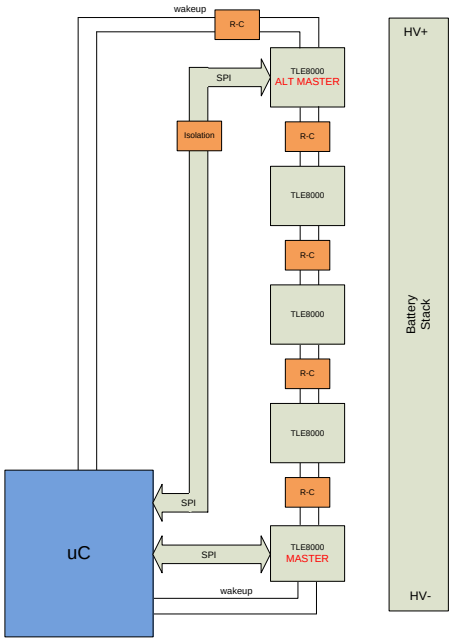


Figure 2.7: IBCB - Redundant Daisy Chain configuration

2.2.4.2 SPI

The TLE8000QK incorporates a standard serial peripheral interface (SPI) that allows full duplex communication with the micro controller. It requires 4 signal wires and supports fully user selectable data rates up to a maximum of 8 MBit/s. The size of a communication frame is 32 Bit. Although the communication is fully duplex, which means that communication to and from the IC happens simultaneously, the answers received are always delayed by exactly one communication cycle. This is very common in SPI communication, as the execution of a command inside the IC is only possible after receiving and decoding the full command. This requires an additional communication cycle at the end of a data transfer to receive the last commands answer. Although this seems like a drop in data rate of 50 %,

the percentage of additional communication overhead decreases with the amount of commands to be sent. So when high throughput is necessary, the overhead becomes minimal.

As stated in the IBCB section, this SPI interface is enabled for the TLE8000QK in master mode only.

2.2.4.3 Direct IOs

The TLE8000QK IC features various input output (IO) lines for fast response to special events. For example the IRQ pin indicates if new information is available in the IBCB communication register. The nFault pin indicates if one of the maskable failure conditions has occurred.

For more information about communication capabilities of the TLE8000QK IC please refer to the ICs datasheet [AG13].

2.2.5 Supply possibilities

The TLE8000QK features different supply paths for high voltage functions such as balancing and IBCB communication, as well as for low voltage functions such as logic, measurements or SPI communication. The low voltage domain can be supplied from the high battery voltage using an internal linear regulator as well as any type of external regulator. This provides the possibility to use simple supply concepts as well as more complex designs allowing higher efficiency and accuracy due to less chip heating (figure 2.8).

2.2.5.1 High voltage supply domain

The high voltage side of the chip is designed to be directly supplied by the connected battery cells. The supply range for GNDA to U12P reaches from 10 V to 60 V, whereas a cell count ranging from 2 to 12 cells is supported. This allows the IC to operate with a wide range of battery technologies that feature different cell voltages.

IC functions supplied from this supply path are for example the balancing drivers, the cell monitoring, or the PADC input stages. These functions include an internal charge pump on the VPP pin, needed to efficiently drive the MOSFET of the highest cell in the stack in Active Balancing mode. The IC also includes a linear regulator for the IBCB highside communication present at the U12M5 pin.

As the IC is supplied directly from the same battery it is supposed to measure, its own supply current can affect measurement accuracy. To avoid such unwanted loss

of accuracy the IC supports completely different paths for supply and measurement, namely on U12 and U12P as well as U0 and GNDA. This can be used for a Kelvin connection where measurement and supply currents use different tracks and are only connected directly at the battery stack that needs to be measured. With this technique voltage drops from supply currents can be minimized to a level that does not affect the results any more. In cases where the specified 1.5 mV DC accuracy with 13 Bit resolution is not required, those lines can be combined as well.

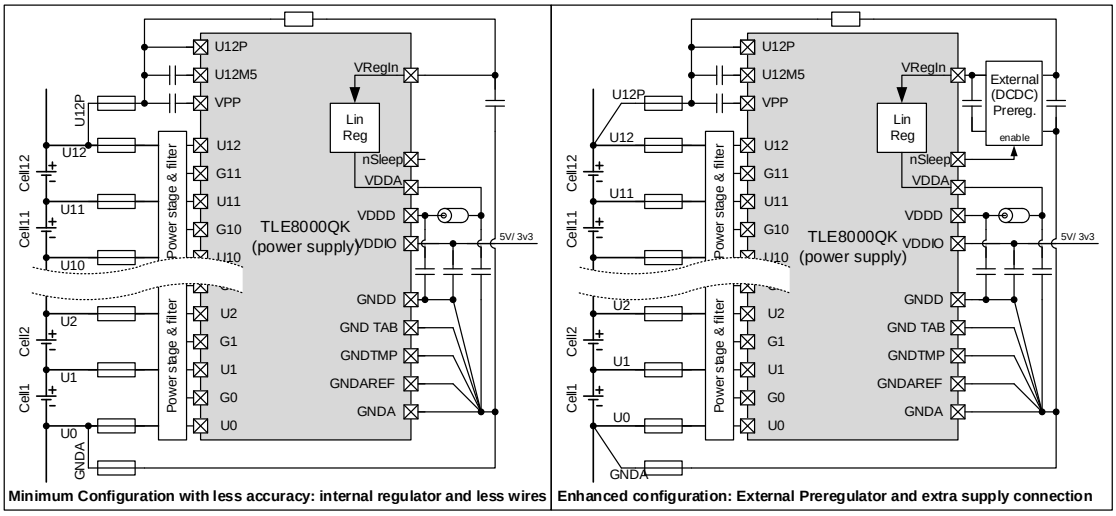


Figure 2.8: Different supply possibilities for TLE8000QK ICs

2.2.5.2 Low voltage 5 V supply domain

The supply voltage for the 5 V domain is normally derived from the same supply as the high voltage domain. As the requirements on a BMS can vary broadly, the IC also supports multiple ways of generating this voltage.

Internal voltage regulator

The cheapest way is to use the internal linear regulator to create the needed 5 V supply directly from the battery voltage. However, depending on the actual battery voltage, the resulting power losses might already reduce accuracy and Passive Balancing capabilities. A simple way to reduce these power losses is to introduce a series power resistor between the battery stack and the linear regulator input. This setup can be seen in figure 2.8 on the left side.

External regulator

Another possibility to further reduce internal power losses is to generate the 5 V by an external DCDC regulator. In contrast to the standard linear regulator,

which converts the excess voltage into heat, the DCDC-regulator transforms the voltage, resulting in a higher overall efficiency. A side effect of DCDC converters is the introduced switching noise on the supply voltage. Depending on the level of introduced noise, this can lead to reduced accuracy, if non-sufficient filtering techniques are being used.

Internal regulator with external pre-regulator

If both high efficiency and high accuracy are needed, both methods can be combined. In this case the external DCDC regulator produces an already decreased input voltage for the internal linear regulator. This reduces internal power losses of the internal regulator that is used to reduce the voltage spikes of the DCDC. Such a setup is recommended and can be seen in figure 2.8 on the right side.

For more information about power supply of the TLE8000QK IC please refer to the ICs datasheet [AG13].

2.2.6 Other not yet mentioned IC features

2.2.6.1 Watchdog

To ensure correct operation, and to allow automatic abortion of balancing in case of failure, the TLE8000QK contains a hardware watchdog. This is an internal safety circuitry with a counter that needs to be reloaded periodically by the main micro controller. If this counter is not reloaded in time, the IC will abort all operations and go back to sleep mode.

2.2.6.2 Ability to withstand hotplug conditions

In contrast to standard electronic circuits that have a single power supply, which can be connected via a single switch, the TLE8000QK is supplied by a stack of multiple battery cells, which cannot be turned off. This means that connection to the target has to be established whilst voltage is already present, which is called “hot-plugging”. The TLE8000QK supports connection to the battery cells in a random sequence. As a result any standard or combinations of standard connectors can be used. There is no need for special connectors with forced connection order.

2.2.7 Block functions to verify

All the previously presented chip functionality is designed for direct customer usage. These functions, which are also specified in the datasheet, need to be verified.

2.2.7. Block functions to verify

But these are not the only functions that need verification. Most of these functions are based on building blocks, which can be accessed directly and separately in special testmodes that are not accessible to end users. During the verification process it is often necessary to verify these blocks in a separate way. This can for example be the case, if this block is used inside a state machine and where their outputs are not directly visible to the end user.

For all these tests, special testmodes are needed that require special external circuitry and security codes. However, as these are confidential, no further information may be given in this thesis.

2.3 Previous verification setups - Improvement requests

Now that the IC-functions to verify are known, the next step in the development process was to gather improvement requests from previous verification setups.

Before the development of the TLE8000QK IC, a testchip had been built to investigate many of the concepts later used in the TLE8000QK. As this testchip also had to run through a verification process, a previous setup existed at the start of this thesis. Besides standard equipment like sources, multimeters, oscilloscopes or thermal forcing systems this previous setup already contained a simple verification board, a battery simulator and a capacitor array allowing high current rise times for Active Balancing.

The following section describes parts of this previous setup, as well as knowledge gained needed for improvements.

2.3.1 Verification board X11

The verification board for the previous testchip will from now on be called X11 board. It was intended to be a simple interface board, providing typical hardware and interfaces for the DUT. All connection to onboard hardware was made purely manually through either solder jumpers or mechanical jumpers. This allowed to easily apply external equipment to the DUT whilst completely avoiding side effects of still connected onboard circuitry.

The board was in fact a combination of two boards, as can be seen in Figure 2.9. One board was an already existing general purpose FPGA board, which provided a PC interface as well as free programmable digital interfaces and standard analog inputs and outputs. The other board was the actual verification board, providing the application specific hardware.

The hardware of the X11 verification board included

- interfaces to 2 external battery simulators
- capacitor buffered resistor ladders that could be used instead of the battery simulator
- 12 power resistors for Passive Balancing
- an interface matrix allowing to manually connect the resistors ladder and the power resistors to the DUT in various combinations
- various power supply possibilities for the DUT

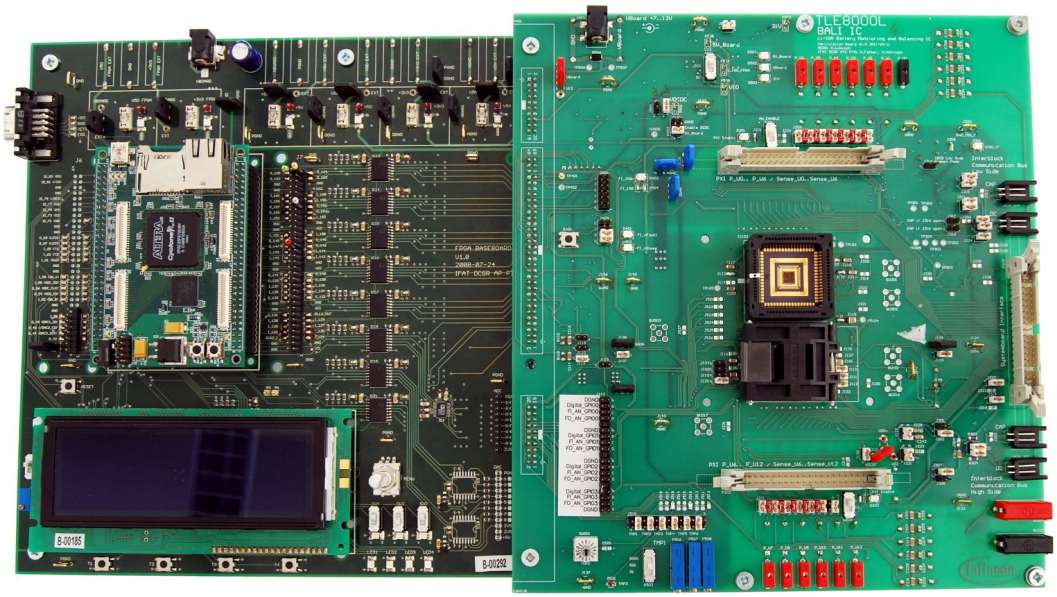


Figure 2.9: General Purpose FPGA Board with X11 board

- various analog resistors to manually investigate the behavior of the NTC sensor of the testchip
- basic connection hardware for the IBCB, SPI and other digital interfaces
- multiple LEDs and switches to interface with the DUT's direct inputs and outputs
- a jumper matrix allowing to connect analog or digtial signals to the GPIO interface
- other minor circuitry, not yet mentioned needed for proper operation of the DUT

Improvement requests for the new verification board:

Although this simple concept was successfully and heavily in use for the verification of the testchip, an advanced concept was needed for the verification of TLE8000QK. The following list presents parts of the old concept that needed improvements:

- The preparation for each different verification setup was a long lasting manual process. Much care had to be taken to avoid mistakes creeping in. Furthermore, the actual setup was hard to reproduce, as it solely relied on manual notes given by the verification engineer.

  ⇒ The new verification board shall minimize the possibility for wrong setups. It shall also provide at least semi-automatic setup of verification tasks, as well as ways to detect specific setups.

- Some IC functions changed basically from the testchip to the TLE8000QK. This led to a completely different pinout compared to that of the testchip, which made the old verification board incompatible with the new TLE8000QK. Also future derivates of the TLE8000QK might have different packages and therefore different footprints.

  ⇒ The new verification board shall provide a flexible concept that allows easy adoption to new footprints and variants, without the need for a completely new verification board.

- Although the old board was designed for good analog performance, the full accuracy could not be reached easily. This was due to various reasons, involving both testchip and board design. The new TLE8000QK supports even a higher resolution with an updated concept that allows for further accuracy improvements if the external circuitry was designed accordingly.

  ⇒ The new verification board shall provide enhanced analog accuracy, as well as differential measurement possibilities to verify this accuracy. Steps necessary to achieve this enhanced accuracy include further separation of supply and measurement paths for the DUT as well.

- Measurements done with the old verification board always needed a bunch of external equipment, which decreased accuracy because of the huge amount of wiring and connection points. It also increased the possibility for setup failures, e.g. by wiring failures.

  ⇒ The new verification board shall contain more onboard measurement options to allow for smaller setup requirements. This shall also increase reproduceability of measurement results.

2.3.2 Other boards

Besides the main X11 board also other boards where available in this setup. The following shortly describes the most important of these.

2.3.2.1 BMS board

For demonstration purposes a battery management system (BMS) board with the testchip had been developed by a group of application engineers. Figure 2.10 shows such a board in version 7.0. This board allows for Passive as well as Active Balancing applications, depending solely on the assembly. It features connectors allowing high currents to the battery, as well as various others for communication or NTC measurement.

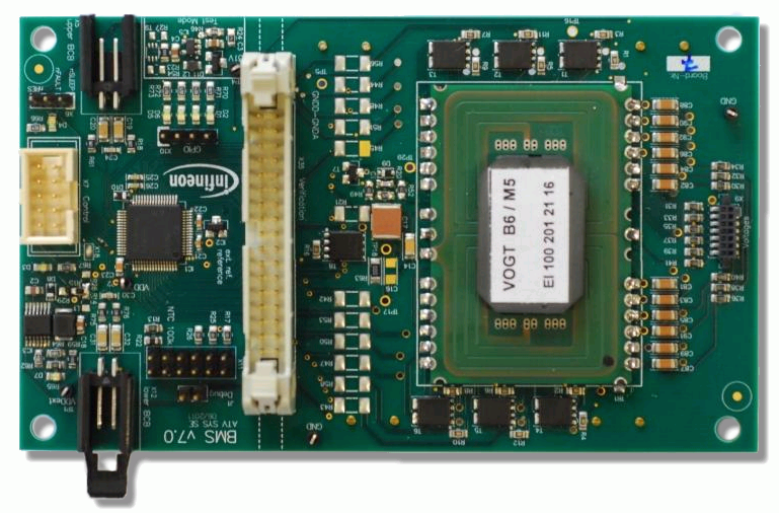


Figure 2.10: BMS-board 7.0; Assembled for Active Balancing

Improvement requests

To allow for increased efficiency as well as improved measurement accuracy, the developer group of that board decided to update the main battery interface of the BMS boards concurrently with the anyway necessary upgrade from the testchip to the TLE8000QK.

The new verification environment shall therefore be built in such a way that it supports this upcoming 8.x series of the BMS board. Coordination with design team will be necessary.

2.3.2.2 ESD boards

To allow measurements on the ESD behavior of the IC a so called ESD board had previously been built. This board follows very strict design guidelines to minimize parasitic effects during ESD stress tests. It basically provides an interface for an ESD gun to all DUT pins that reside in a testfixture. These connections are designed to be as similar for each pin as possible.

Improvement requests

As the testchip and the TLE8000QK use the same IC-package the same ESD board can be used. Therefore, nothing needs to be updated here.

2.3.3 Measurement equipment

The measurement equipment used can be divided into two main groups. The first group is used for (quasi)-static measurements allowing high precision and accuracy results for DC or slow changing voltages.

The second group is required to measure fast changing signals. However, high accuracy (voltage) measurements are often not possible with this kind of equipment.

2.3.3.1 (Quasi)-static measurement Equipment

The present available equipment involves various kinds of meters allowing to measure physical quantities such as voltage, current, resistance and more, over various orders of magnitude. This is de facto standard, therefore only those measurement capabilities that are special will be discussed in detail.

Measurement of battery voltages

The testchip as well as the TLE8000QK claim to allow high accuracy measurement of up to 12 battery cells. This has to be verified by comparison with measurement results from high accuracy equipment under calibration control.

For comparison measurements in the old setup, a Keithley 2000 high accuracy multimeter was used in combination with a NI-PXI 2569 relay multiplexer card inside a PXI measurement system. After various measurements an uncertainty of multiple hundred µV up to mV concerning the repeatability of this setup was discovered. This was assumed to come from a combination of factors like the high count of contact points throughout the measurement path, as well as the high cable length and noise source present inside the PXI system near the relay cards.

Requests for the new verification platform: A new setup shall be created that allows for simpler and also more reliable reference measurements. This new setup should also use some kind of multiplexer, but with a significantly reduced amount of connection points and cable length, allowing accuracy measurements with a single voltage meter.

2.3.3.2 Dynamic measurement equipment

The dynamic equipment involves various types of waveform recorders and oscilloscopes equipped with active and passive current and voltage probes as well as dedicated logic probes. Nearly all measurement tasks necessary during testchip verification were able to be fulfilled satisfyingly with the existing equipment. However, there were problems measuring fast low voltage signals.

Both, the testchip and the TLE8000QK, are able to measure voltages very accurately. But, as the measurement takes some time, the cell voltages applied to the chip have to be stable during this time period. Otherwise the chip will measure the average of the signal plus that of any disturbance present during the measurement time. It is therefore necessary to ensure that the applied voltages are sufficiently stable, especially if battery simulators are used.

Furthermore, as the chip uses a ΣΔ-ADC concept, the input voltage is not measured continuously during this period but sampled multiple times at a high sample rate. This measurement process itself creates periodic voltage drops on the input pins that have to be recharged by the external filter capacitors. If the external circuitry and filtering is designed and applied appropriately, accurate measurements are possible. The verification of this is not an easy task and relies on accurate and quantitative measurement of these fast voltage drops down to the sub millivolt range.

Request for further improvements

The verification of the testchip revealed that measurement of those high speed and low voltage signals, were hardly or even in some configurations even not possible with the presently available equipment. Verification therefore solely relied on measurements of second order effects which turned debugging into a difficult and long lasting process. Therefore, new ways to close this measurement gap should be investigated.

2.3.4 Equipment for simulation of environmental conditions

2.3.4.1 Standard environment simulation equipment

Besides the already mentioned boards and measurement equipment, some equipment that allows to generate the environmental conditions of application scenarios is also available.

This equipment involves for example, various voltage or current sources, temperature forcing and other needed equipment.

Improvement requests:

The standard equipment worked well for the verification of the testchip and other ICs. No need for updates have been reported.

2.3.4.2 Battery voltage simulation

To allow for higher accuracy and higher currents than possible with the resistor ladder of the X11 board a PXI battery simulator is available. It consists of 12 independent programmable voltage sources, each capable of driving up to 300 mA with parallel current sinks allowing for 0 mA to 100 mA in 16 steps.

To support even higher peak currents, e.g., for Active Balancing, a capacitor array had previously been built. It houses up to 5 super-capacitors per cell, each 3 F, coming to a total of 15 F per cell.

Figure 2.11 shows the final state of this equipment at the end of this thesis as no original images before the modifications are available. Therefore, the upgrade to fit the new BMS platform are already visible in this configuration.

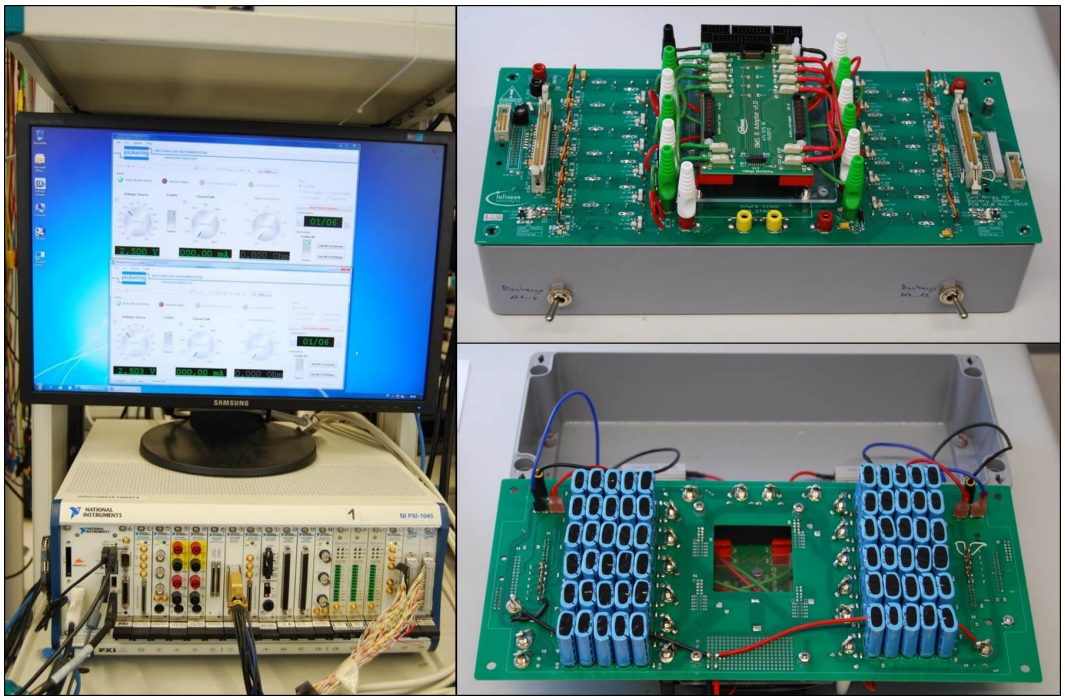


Figure 2.11: Battery simulator setup, left PXI with battery simulator, right top: capacitor array with flexible interface for BMS8.x or BMS7.x, right bottom: capacitor array opened with $5 \cdot 3 = 15$ F per cell

Pickering PXI battery simulator

The battery simulator available at the start of this thesis consists of two Pickering PXI cards with Model No. 41-752. This cards each offer 6 isolated and independent programmable voltage sources with additional current sinking capability. The output voltage can be set with a resolution of 14 Bit (approximately 430 µV) and offers an accuracy of ±20 mV + ±2 % of the desired set value.

This accuracy further decreased as soon as output current was drawn out of the simulator. Therefore, extensive effort had previously been needed to re-adjust the setting of the battery simulator if accurately set voltages were needed. This involved a rather complex automatic recalibration setup that re-tuned the output voltage once the IC was in place and operating.

Requests for battery voltage simulation: To ease future verification an improved way of applying precise voltages shall be possible. This new setup shall support the following features:

- higher resolution than the current setup and the TLE8000QK IC's resolution
- increased accuracy; minimum the accuracy of, or preferable better than the resolution of the TLE8000QK IC
- support either multiple cells, or allow stacking inside a chain with the existing battery simulator
- fast response to dynamic load changes. The current battery simulator shows significant voltage drops as soon as the IC's current consumption rises by some 10 mA due to a start of an ADC measurement.
- fully programmable via a PC or directly from the verification board

Requests for the super capacitor array

The super capacitor array had originally been designed without a Kelvin connection for the highest and the lowest cell. It furthermore features an interface to a BMS board for the testchip that was replaced by an improved BMS interface for the TLE8000QK.

The array shall therefore be updated to support the new interface as well as the Kelvin connection. (Figure 2.11 already shows the updated capacitor array)

2.4 Short summary of tasks to implement

To conclude this chapter, this short list summarizes the necessary tasks for the new verification environment on one single page.

- Build a new verification board that allows the verification of the TLE8000QK IC. This board shall allow to verify all the chip functions for the TLE8000QK described in section 2.2 and fulfil the requirements that arise from the X11 board in section 2.3.1. Those mainly involve:
  - Incorporate a concept that allows usage of bare ICs in various packages, as well as the BMS-board
  - Provide all standard means of communication (SPI, IBCB, direct IO)
  - Allow a setup to further investigate IBCB communication, preferable on one board
  - Allow investigations on Active and Passive Balancing
  - Allow all standard modes of power supply
  - Provide automatic ways to setup the board's configuration to avoid the error prone manual setup procedures of the X11 board
  - Ensure reproduceability by both automatisms and identification possibilities
  - Allow for high accuracy measurements of the TLE8000QK's Ux pins during ADC measurement
  - Allow for high accuracy measurements with the other TLE8000QK functions like NTC, GPIO,...
  - Allow for interfaces to external equipment
  - The board shall be extensible for possible future derivates of the TLE8000QK
- Investigate and provide new ways to measure the battery cell voltages more accurately
- Investigate and provide new ways to measure the dynamic low voltage signals more accurately
- Investigate and provide new ways for battery voltage simulation
- Update all boards to be compatible with the upcoming BMS-board version 8.x

3 Development and Implementation of the verification environment

While the previous chapter derived all needs for the verification environment to build, this chapter concentrates on the actual development process. It starts with the update of the measurement equipment. Then the new setup and boards for the simulation of environmental conditions will be presented. In this section the development of the HPBS will be exercised in detail and measurement results will be presented. It demonstrates in general how board development processes have taken place during the project phase of this thesis. The following section presents the main verification board. Due to the complexity of this board the focus will shift from complete description of all circuitry to the concept and final realization. Insights on the design process will only be given on some exemplary and important circuitry. Finally an overview of the software will be given and exemplary measurement results of the total verification environment will be presented.

3.1 Improvements for the measurement equipment

As the analyses of the old verification setup had shown, it was necessary to update some of the measurement equipment. Therefore, one of the first steps was to investigate if the other equipment also available at the Power Train Systems department would be suitable or if enhanced devices needed to be built or acquired.

3.1.1 Improvements on the static measurement equipment

As mentioned earlier the old setup for measuring the battery cell voltages needed an update to allow for better repeatability. Therefore, both, the used voltage multiplexer setup as well as the voltmeter had to be investigated, to see where accuracy and repeatability gains could be reached.

3.1.1.1 Comparison of existing voltmeters

The voltmeter type used in the previous setup was a Keithley K2000 type. According to the datasheet the absolute gainable accuracy mainly depends on the

range used as well as on the actual value to be measured. But it also depends on the integration time of the voltmeter, and may be increased, if the integration time is a synchronized multiple of power line cycles (PLC). It furthermore decreases with elapsed timespan between the measurement and the last calibration.

Based on the values given in the K2000's datasheet, the uncertainty may be calculated by the following equation.

$$\mathsf{Error} = \mathsf{Range} \cdot \mathsf{uncertainty}_{\mathsf{Range}} + \mathsf{InputVoltage} \cdot \mathsf{uncertainty}_{\mathsf{Reading}} \tag{3.1}$$

$$\mathsf{Error} = 10\,\mathrm{V} \cdot 5\,\mathrm{ppm} + 5\,\mathrm{V} \cdot 30\,\mathrm{ppm} = 200\,\mu\mathrm{V} \tag{3.2}$$

The following comparison tables (table 3.1 and 3.2) perform the above calculations for all relevant multimeters available at the start of this thesis at Power Train Systems. The range chosen for this comparison, is the lowest possible range that allows measurements from 0 V to 5 V. DC Common Mode Rejection Ration (CMRR) was 140 dB for all voltmeters shown and could therefore be neglected in the error calculations.

	Values from the datasheet					Calculated	
	Range	Range failure	Reading failure	Resolution	PLCs needed	Input Voltage	error
	[V]	[ppm]	[ppm]	[µV]	[cnt]	[V]	[µV]
Keithley K2001	20	4	24	10	10	5	**200**
Keithley K2000	10	5	30	10	10	5	**200**
Keithley K2700	10	5	30	10	10	5	**200**
Agilent 34410A	10	5	30	10	100	5	**200**
HP/Agilent 3458A	10	0.05	8	0.1	10	5	**41**

Table 3.1: Voltmeter accuracy comparison; lowest range used allowing 0 to 5 V measurements; Based on **1 year** calibration interval

	Values from the datasheet					Calculated	
	Range	Range failure	Reading failure	Resolution	PLCs needed	Input Voltage	error
	[V]	[ppm]	[ppm]	[µV]	[cnt]	[V]	[µV]
Keithley K2001	20	4	18	10	10	5	**170**
Keithley K2000	10	5	20	10	10	5	**150**
Keithley K2700	10	5	20	10	10	5	**150**
Agilent 34410A	N.A.	N.A.	N.A.	N.A.	N.A.	N.A.	N.A.
HP/Agilent 3458A	10	0.05	4.1	0.1	10	5	**1**

Table 3.2: Voltmeter accuracy comparison; lowest range used allowing 0 to 5 V measurements; Based on **90 day** calibration interval

Results for the voltmeters:

The calculations for the comparison show an interesting result. Although the voltmeters are from different vendors and use different ranges, all except for the far more expensive HP/Agilent 3458A allow for the exact same maximum accuracy after 1 year of 200 µV as well as same resolution of 10 µV. One could therefore assume that these instruments all rely on a similar kind of internal reference and ADC, especially since they are all in a similar price range.

These results can now be compared with the requirements for the measurement of the TLE8000QK IC. The resolution of the TLE8000QK is 586 µV, whereas the accuracy shall reach ±1.5 mV. This means, in terms of resolution, that each LSB of the IC can be measured with a 58x higher resolution with the above standard meters which should be more than sufficient for precise measurements of the ADC's linearity. Furthermore, the accuracy of the voltmeters is 7.5 times higher than that of the DUT and approximately 3 times higher than the DUT's LSB.

For special measurements the Agilent 3485A would provide even higher resolution and accuracy, but this should only be necessary in rare cases. Therefore, sufficient repeatability should be given with all voltmeters, as long as the measurement path with the multiplexer doesn't introduce additional random error sources.

3.1.1.2 Alternatives for the existing voltage multiplexer

Since the previous section showed that the voltmeter of the old setup should have been sufficient, the relay multiplexer will be investigated next to see where improvements to the repeatability of the X11 verification equipment can be made.

Original setup

As mentioned earlier the old setup used a NI-PXI 2569 relay card, as well as various cables and connectors with a single voltmeter for the measurements of all the cells. The relay card is a multipurpose type and features 100 independent single-pole single-throw (SPST) relays. Accessing the relays required multiple connectors and long cables in the previous configuration, which is non-ideal as each connection point is a possible error source. This was especially true since the old setup also relied on an IDC type connector that was later replaced by a spring probe adapter to access the voltage pins as close to the DUT as possible.

In total a cell voltage signal had to pass through 2x12 electrical connection points,[1] numerous solder joints, series resistors and approximately 2x4.8 m of cable to con-

[1] This also included the relay and the spring probe. Without the spring probe but with the IDC connector a total of 2x11 connections result. The factor x2 is because the signal has to go back and forth.

nect each cell from both sides to the voltmeter. This offers possibilities for multiple error sources to alter the measurement results.

Error sources and possibilities for improvement

As the measurement accuracy and resolution target is in the sub mV range, many different error sources can easily sum up in the measurement path, if insufficient care is taken. Such error sources include, e.g., thermoelectric contact voltages, voltage shifts caused by unintended currents sharing parts of the measurement path, disturbances either coupled capacitively or inductively, amongst others.

Voltage shifts: Although the measurement current of the voltmeter is negligible, which means that it will not create measurable voltage drop across the measurement path itself, other currents might still run across parts of this path creating significant voltage drops. Such errors can be reduced by decreasing the track length that is shared with the other currents, e.g., the supply current of the IC, and by connecting the pure sensing lines as close to the points of interest as possible. In the new verification environment all boards used for accuracy measurements with the TLE8000QK shall therefore provide a dedicated cell voltage measurement connector interfacing to the best fitting sensing points. This also reduces the need for needle spring probes. Further separation from supply and measurement current path of the IC will also have to be implemented, which is anyway generally intended for the new TLE8000QK-Design.

Thermal EMF: In the range of 1 mV and below contact voltages (also referred to as thermal EMF = thermal electromagnetic forces) can start to play a role as well. This is especially true since in this case, as the DUT's temperature will be forced by external equipment, which can lead to significant temperature gradients as well as excess air flows on the surrounding PCB and connectors. Literature research revealed thermal voltage coefficients of multiple typically used materials that can be seen in table 3.3. An extreme example of the huge range is the comparison of a clean copper to copper connection with 0.2 µV/K to that of copper to copper oxide with 1000 µV/K. Other notable values are those of solder 5 µV/K and that of a typical metal film resistor with 20 µV/K.

Giving an exact estimation to which extent these thermal voltages will affect accuracy is difficult as it depends on multiple factors such as geometry of the solder joints and its surroundings, thermal power to be transported, possibilities for the thermal voltages to cancel out and so on. In general the effects scale with the amount of parts and joints incorporated in the measurement path, which means that the old setups accuracy could already have suffered from these effects, but this was not verified in detail.

Paired Materials	µV/K (Qab)
Copper-Copper	<0.2
Copper-Cadmium/Tin Solder	0.2
Copper-Gold	0.3
Copper-Silver	0.3
Copper-Brass	3
Copper-Lead-Tin Solder	5
Copper-Aluminum	5
Copper-Nickel	10
Copper-Kovar	40
Copper-Copper Oxide	>1000
typical metal film resistor	≈ 20
typical carbon composite resistor	≈ 400

Table 3.3: Thermoelectric potentials of various material combinations, upper part from [Kid12],[KC03], lower part from [RCD02] and [Lin91b, page 7]

However, there are simple countermeasures that can be taken for the new system to minimize the effects even under great thermal load.

- Decrease the number of thermoelectric active parts to a minimum. This includes electrical connection points as well as solder joints or parts like resistors or solder jumpers.
- Decrease thermal gradients across sensitive parts. Either take the part out of thermal active area and/or equalize thermal potential around the part by thermal copper masses surrounding the part.
- Allow thermal voltages to cancel out. As the errors occur on both wires of the measurement path, they have the possibility to cancel throughout the loop. But for this to happen effectively, the paths have to be as symmetric as possible and lie on the same thermal gradients. It may even be beneficial to introduce dummy parts to increase symmetry and therefore allow for better cancellation, as proposed by [Wil01]. But this technique may only be used in special cases where layout conditions allow for thermal matching.
- Use relays with low thermal EMF, dedicated for low voltage measurements. Such types are often double-pole single-throw (DPST) or double-pole double-throw (DPDT) relays, which means that they feature two contacts per relay, both with similar EMF values that more easily cancel out throughout the measurement path [Nat10].

Noise and other disturbances: Another source of inaccuracies can come from coupled noise and disturbances. Disturbances can come from multiple sources like

switched currents or directly via the mains, and couple through various methods. The most common coupling effects are direct ohmic, capacitive, magnetic and electromagnetic.

Direct ohmic coupling may occur if large currents create voltage shifts across the ground resistance, which causes a ground shift that is also seen by the signal to measure. This can happen on a small scale on a single PCB if the power and signal grounds are not sufficiently routed. It can also occur on a larger scale if multiple measurement devices are used that are all grounded on different mains positions and also on the PCB allowing induced currents to flow in this loop. To prevent such situations, ground loops should be avoided by connecting all devices at a single ground point only. For the later example this can be achieved using isolating transformers and single ground connections on the PCB to measure. If such a transformer is not available, the effect may be at least reduced by decreasing the loop size and area and therefore the possibility to capture disturbances, by e.g. connecting all grounded devices at closely related mains outlets.

As the voltmeter itself measures differentially and features very high common mode rejection, it should not cause ground loops. However, it may still see disturbances that are caused by ground loops formed by other equipment. However, this kind of noise is often synchronous to the mains, which allows for adapted filtering by choosing a voltmeter integration time of multiple power line cycles (PLC).

The indirect ways of coupling are capacitive, magnetic and electromagnetic. The intensity of the disturbance depends on the power of the noise source as well as the coupling factor from the source to the target. In an application the reduction of such disturbances mainly relies on filtering and shielding techniques as no influence on the disturbance sources, like inverters, is possible. In a laboratory environment there can also be the possibility to partly turn of some of these sources as well.

So for the battery cell voltage measurement this means that filtering and shielding from unwanted disturbance sources should be used wherever possible. The cables for the measurement path shall also be as short as possible and put as far away from sources of disturbance as possible to keep coupling minimal. And furthermore all not needed equipment for the specific measurement task shall be turned off to keep disturbance levels low.

Mismatches between static and dynamic values: Another important factor to notice is the different measurement timing of the multiplexed voltmeter and that of the TLE8000QK. This means that both devices will only be able to gain similar results if the voltages are truly the same during both measurement cycles. Although this sounds simple in the first place, one has to keep in mind that the battery simulator used to supply the TLE8000QK is an active device and may show dynamic effects, when it has to provide the transient supply current to the IC during the measurements. This means that both, the voltmeter and the IC

may yield different, but both correct results, as the voltages RMS value may differ between the measurement cycles of the DMM and the TLE8000QK. The equipment necessary for proofing of such dynamic stability will be introduced in the next section on page 44.

Outcome for the improved multiplexer setup

To improve repeatability and to reduce all the above mentioned unwanted effects as good as possible, the following improvement steps were performed during the development of the new verification environment.

All newly designed boards in chapter 3.3 that may be used for voltage measurements now feature the small voltage measurement connector of the BMS7.x board. This type is far more compact than the previously used IDC series (figure 3.1), and therefore allows for better thermal equalization. Furthermore, all power lines that might draw currents during measurements were further separated from the cell voltage measurement connector's sense lines to reduce voltage drops.

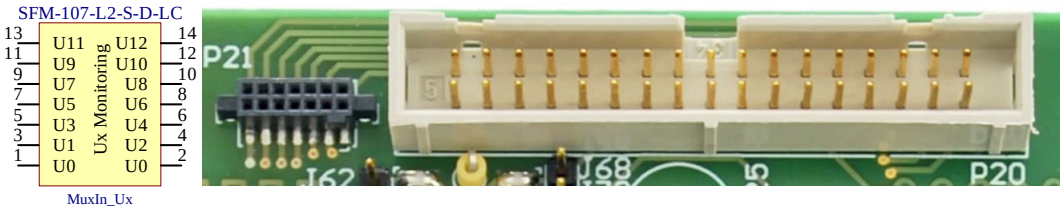


Figure 3.1: Connector for battery voltage measurement. Left: Pinout; Middle: new connector; Right: old connector

A new compact relay multiplexer (see page 139) was built onto the main verification board, which allows usage of all of the previously mentioned voltmeters with every verification board. It uses DPDT relays that have a thermoelectric potential rated at $<10\,\mu V$ [AXI11]. This multiplexer uses the same voltage connector as all new boards and allows simple connection using short 1:1 cables.

Alternatively also one K2700 Multimeter carrying a special relay card was prepared to measure the cell voltages.

In total there are now only 2x6 mechanical contacts in the measurement loop, which is half the old value, and the cable length was greatly reduced. Also the connections are now more compact, which allows for further thermal equalization within the return path.

3.1.2 Improvements for the dynamic measurement equipment

3.1.2.1 Detailed analyzes of existing problems

Measurement difficulties

As previously mentioned it was necessary to measure the cell voltages at the input of the TLE8000QK whilst it performs measurements, to find out if differences in the results arose from suspected dynamic input changes. In particular there were two effects in consideration that needed to be quantified.

The first possible effect to investigate was the stability of the applied voltages throughout the whole PADC conversion process. This results in a required time-frame, for an oscilloscope to see the whole event, of approximately 5 ms. The vertical accuracy should be better than at least half an LSB of the TLE8000QK whilst providing a resolution of minimum 10 times the IC's LSB. So the accuracy should be better than roughly 300 µV and the resolution better than 50 µV.

The second effect concerned the periodic high frequency voltage drops that will occur at the switched capacitor input of the ΣΔ-ADC. Those voltage drops and possible oscillations are normal for any kind of switched capacitor input stage. They result from the parasitic inductances and resistors that slow down recharging from the external filter capacitor. However, the task was to quantize these drops and their decay time to ensure that the input voltages settle before the actual comparison step of the ΣΔ-ADC takes place. The timespan for such phenomena to see is approximately 1 µs whilst still maintaining an accuracy better than the half LSB of the TLE8000QK.

These dynamic measurements are the most challenging in the low voltage area for the TLE8000QK IC and therefore dictate the specification for the equipment here.

Original setup

The original setup that was previously used to start these investigations consisted of an Agilent Infiniium 54831D type oscilloscope in combination with standard compensated 1:10 passive probes. The oscilloscopes minimum full scale range (FSR) is 40 mV with a resolution of 8 Bit. This results in an LSB of 1.5 mV using the 1:10 probes.

As the probes are standard single ended types, any ground related noise will directly result in a measurement error at the particular channel. Improvements can be made if a second probe measures this ground noise directly at the point of interest and the oscilloscope cancels out this error using digital subtraction. However, this technique is only effective if the signal to remove is bigger than the noise floor at the oscilloscopes bandwidth of interest. So if the signal is lower than this noise

floor, ground related noise sources can hardly be removed, especially for single shot measurements.

Even though the oscilloscopes specification is very coarse, some first results for estimation purposes of slow disturbances had previously been possible with the use of heavy oversampling and filtering as well as the use of excessive averaging of multiple measurement events. But, the needed oversampling and the high filtering effort prohibited similar measurements for the higher frequency switched-capacitor input noise. Also the improvements by the excessive use of averaging have to be seen skeptical as misleading results may occur if jitters are too big, or if other signals are present that are not purely random and not statistically unbiased.

Possibilities for further improvement

There are multiple ways to improve the previous setup.

- Oscilloscope: Although the previously used oscilloscope features all kinds of digital signal processing possibilities, its analog performance in the low voltage area is rather poor compared to the current needs.

  ⇒ Use an oscilloscope that is better suited for low voltage measurements, with a lower noise floor and lower voltage for the LSB.

- Preamplifier: The voltage levels are so small that the signal can't be seen through the noisefloor of the oscilloscope.

  ⇒ The small transient voltage changes can be pre-amplified before they enter the oscilloscopes input structure that adds additional noise.

- Single ended vs. differential Measurement: In the old setup two probes are needed for a differential voltage measurement. These are sampled at different input channels, with different noise results, before they can be subtracted. This requires higher efforts to remove this overall noise with averaging or filtering.

  ⇒ Analog, true differential probes can be used instead. Some types even feature internal preamplifiers.

- Decrease averaging jitter: The resulting quality of averaged measurements largely depends on the quality of the trigger signal.

  ⇒ Provide a synchronization pulse that can be used for low jitter triggering of the actual signal to measure. This has to be provided directly by the IC in a dedicated factory testmode that has to be required from the team of IC designers.

3.1.2.2 Selection of the new equipment

The search for improved equipment for these dynamic measurement tasks was far more difficult than expected. Whilst many devices are available on the market for high speed measurements, only few seem to be available for dynamic low voltage measurements. Most differential probes or amplifiers seem to be designed for either high voltage measurements in power converters, or for high speed measurements of voltage levels more related to digital logic than for low voltage analog systems. The search therefore included investigations on existing equipment at Power Train Systems as well as getting in contact with the most important manufacturers of dynamic measurement equipment. The following section shows parts of the evaluation steps that were conducted to choose proper equipment.

Oscilloscopes

Comparison of oscilloscope parameters: The oscilloscope is the core part for these dynamic measurements. Its measurement and signal processing capabilities mainly determine the overall achievable results. Therefore, many different oscilloscopes on the market or already available at Power Train Systems were compared in terms of their low voltage capabilities.

At the time this search was conducted only one oscilloscope was found on the market that allowed for significantly better results than the already acquired types. This type, built by LeCroy, features a 12-Bit ADC with low noise input, as well as extensive signal processing capabilities. Table 3.4 shows the parameters of the available oscilloscopes at Power Train Systems as well as this improved type.

During the gathering of the information for this table also an interesting fact was discovered. Although all oscilloscopes provide the same low voltage ranges with 1 mV/div, 2 mV/div and 5 mV/div most of them stop analog amplification already at 5 mV/div and simply display a digitally zoomed version at lower values. However, this results in an extremely poor signal noise ratio for low voltage signals.

As the LeCroy HRO oscilloscope is the only type that uses a native 12-bit ADC, it is able to provide a 16 times better resolution and quantization noise than would be possible with the other types even if they would have had the same FSR in the first place. However, one has to keep in mind that resolution is one thing, but especially when it comes to low voltage measurements the results reachable are typically at least one magnitude worse than a LSB because of noise and disturbances.

Noise floor comparison: The noise floor depicts how much amplitude a signal needs to have so that it can be differentiated clearly from noise in a single shot measurement. This makes it very important for low voltage measurements. It also defines how much filtering or averaging effort is needed to reveal signals below this noise for slow or repetitive signals.

3.1.2. Improvements for the dynamic measurement equipment

	Available types					Other
	Agilent Infiniium 5000 MSO54831D	Agilent Infiniium 7000 MSO7034A	Agilent Infiniium 8000 MSO8104A	Le Croy Wavemaster 8600A	Tektronix MSO4000 MSO4034B	LeCroy HRO 12-bit HRO 66zi
Horizontal System						
Sampling rate 4CH [Gs/s]	2	2	2	10	2,5	2
Analog Bandwidth[MHz]	600	250	1000	6000	350	600
Vertical System						
DC Gain Accuracy [%]	1.25	2	1.25	1.5	1.5	0.5
Min range [mV/div]	1	2	1	2	1	1
Min analog range [mV/div]	5	4	5	10	1	1
Min FSR [mV]	40	64	40	80	10	8
ADC resolution [Bit]	8	8	8	8	8	12
Calculated values						
Number of discrete steps	256	256	256	256	256	4096
LSB 1:1 Probe [µV]	156	250	156	313	39	2
LSB 1:10 Probe [µV]	**1563**	**2500**	**1563**	**3125**	**391**	**20**

Table 3.4: Comparison of oscilloscope parameters

Unfortunately most manufacturers do not specify the noise levels in their datasheets, which makes comparison difficult. Therefore, measurements were conducted between the three most suitable oscilloscopes out of the previous table. The measurements with the LeCroy HRO were conducted with a temporary evaluation device. The results can be seen in figure 3.5.

The measurement setup was the following.

- CH1 of each oscilloscope was directly connected to ground via a 50 Ω resistor. CH2 was connected to the 1:10 probe supplied with the oscilloscope and shortened to the ground directly at the probes tip.
- The measurement was performed twice per oscilloscope, but with different Bandwidth-limit (BWL) settings. First, the lowest analog filter setting offering at least 150 MHz was chosen, to fit the measurement setup requirements. The second time the 20 MHz filter, available on any state of the art oscilloscope, was selected, to provide true 1:1 comparability.
- All digital post-processing functions like filtering or averaging were turned off to give true comparability of the input signal quality. Only the statistic functions were activated, to calculate RMS and peak to peak values of the noise floor.

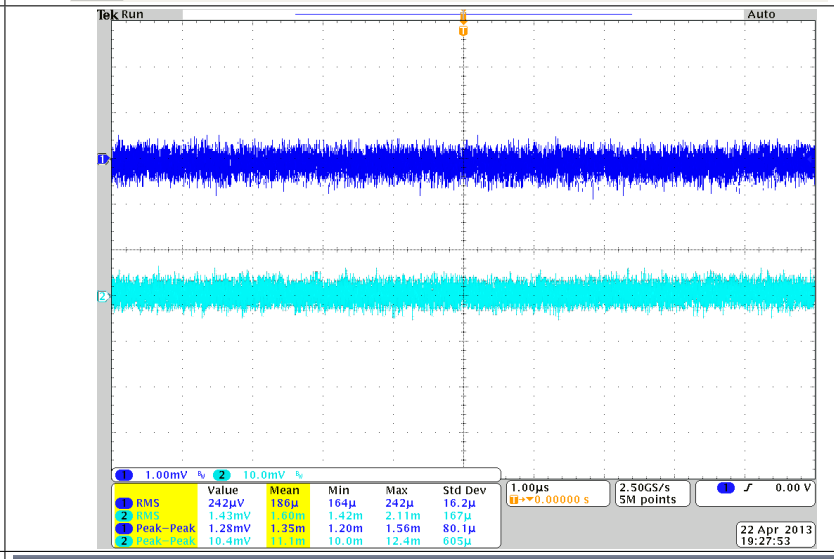
Agilent MSO8104A BWL: 1 GHz Single shot uncertainty 1:10 Probe: ≈26 mVpp	
Tektronix MSO4034B BWL: 250 MHz Single shot uncertainty 1:10 Probe: ≈11.1 mVpp	
LeCroy HRO 66zi BWL: 200 MHz Single shot uncertainty 1:10 Probe: ≈5.4 mVpp	

Table 3.5: Oscilloscope noise floor. Lowest BWL > 100 MHz selected, similar to desired application. 6 mm ≙ 1 mV (CH1), or 10 mV(CH2)

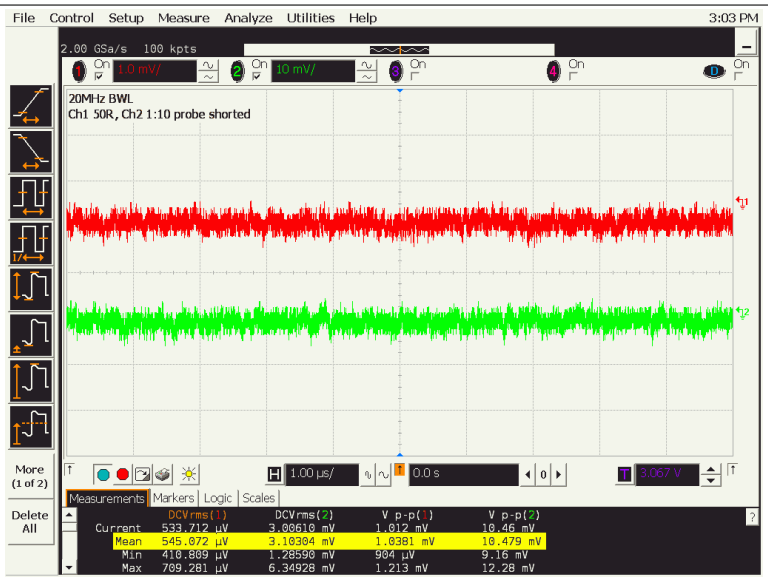
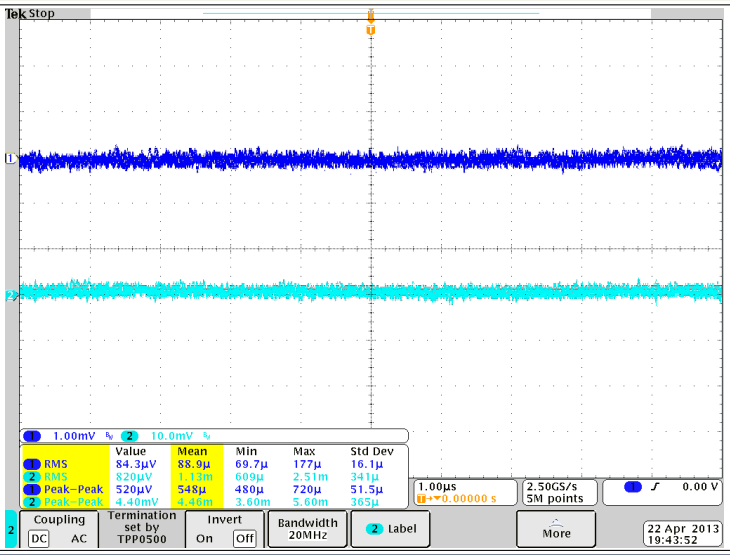
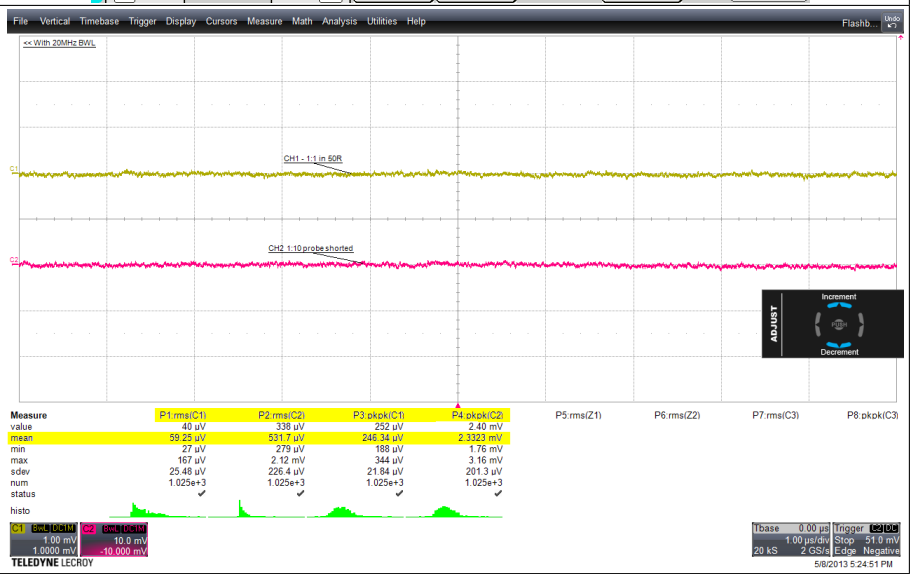
Agilent MSO8104A BWL: 20 MHz Single shot uncertainty 1:10 Probe: ≈10.5 mVpp	
Tektronix MSO4034B BWL: 20 MHz Single shot uncertainty 1:10 Probe: ≈4.5 mVpp	
LeCroy HRO 66zi BWL: 20 MHz Single shot uncertainty 1:10 Probe: ≈2.3 mVpp	

Table 3.6: Oscilloscope noise floor. BWL = 20 MHz (out of application) selected to allow better comparability. 6 mm ≙ 1 mV (CH1), or 10 mV(CH2)

The measurements in the figures 3.5 and 3.6 show that there is significant difference between these oscilloscopes in terms of noise floor. The LeCroy HRO has approximately a 5 times lower noise floor than the Agilent,[2] and also a 2 times lower noise floor than the Tektronix type. However, this alone is still not sufficient, which means that still additional measures like low noise differential pre-amplification or digital signal processing have to be taken.

The later is the discipline where the LeCroy really outperforms the competitors. Whilst the Agilent type with its poor analog performance would provide sufficient signal processing power, the Tektronix type that has improved analog performance immediately slows down to nearly unusable processing times if the needed signal processing options are enabled. So the LeCroy is the only type that provides sufficient analog measurement and digital post processing power. This was proven multiple times during various test measurements that are not further described in this document for sake of brevity.

Comparison of differential pre-amplifiers and differential probes

As already mentioned earlier, differential measurement of the signals of interest is absolutely necessary in the low voltage domain. Differential amplifiers and probes offer improved possibilities as they continuously perform the subtraction before the input and quantization noise of the oscilloscope come into play.

However, just like with the oscilloscope, most manufacturers offer products that are optimized for high speed or high voltage rather than for low voltage measurements. These unsuitable types often include fixed attenuation settings, no amplification >1 and a very high FSR. Preferred types on the other hand should feature a bandwidth of minimum 100 MHz, a setting with no attenuation but amplification instead, and add only little noise to the original signal of interest.

Intensive search, and various requests to different manufacturers came up with only two different pieces of equipment that could be suitable for the measurement tasks. Interestingly both were again found at LeCroy.[3] The first item is the DA1855A, a standalone differential pre-amplifier, whereas the second device the AP033 is a differential probe with internal pre-amplifier. The basic specification for both devices is given in table 3.7 and the common mode rejection ratio (CMRR) vs. frequency characteristics can be seen in figure 3.2.

The most suitable low voltage setups for both devices are highlighted. This is where no attenuation is used and amplification is at the highest possible value of 10 for both devices.

[2] This Agilent scope is a similar type to the one used in the X11 verification.

[3] Interesting side note: The DA1855A is based on a pre-amplifier design developed by the company Preamble that was founded by former Tektronix staff. Preamble was acquired by LeCroy in 1997.

3.1.2. Improvements for the dynamic measurement equipment

DA1855A (with 1:1 Probe)					
Attenuation	[1]	**1**	1	10	10
Gain	[1]	**10**	1	10	1
Total Gain	[1]	**10**	1	1	0,1
Common Mode Range	[±V]	**15.5**	15.5	155	155
Differential Mode Range	[mV]	**50**	500	500	5
Maximum Differential Offset	[±V]	**1**	10	10	100
AP033					
Attenuation	[1]	**1**	1	10	10
Gain	[1]	**10**	1	10	1
Total Gain	[1]	**10**	1	1	0.1
Common Mode Range	[±V]	**4.2**	4.2	42	42
Differential Mode Range	[±mV]	**40**	400	400	4000
Maximum Differential Offset	[±V]	**0,4**	4	40	40

Table 3.7: Parameter comparison of AP033 and DA1855A

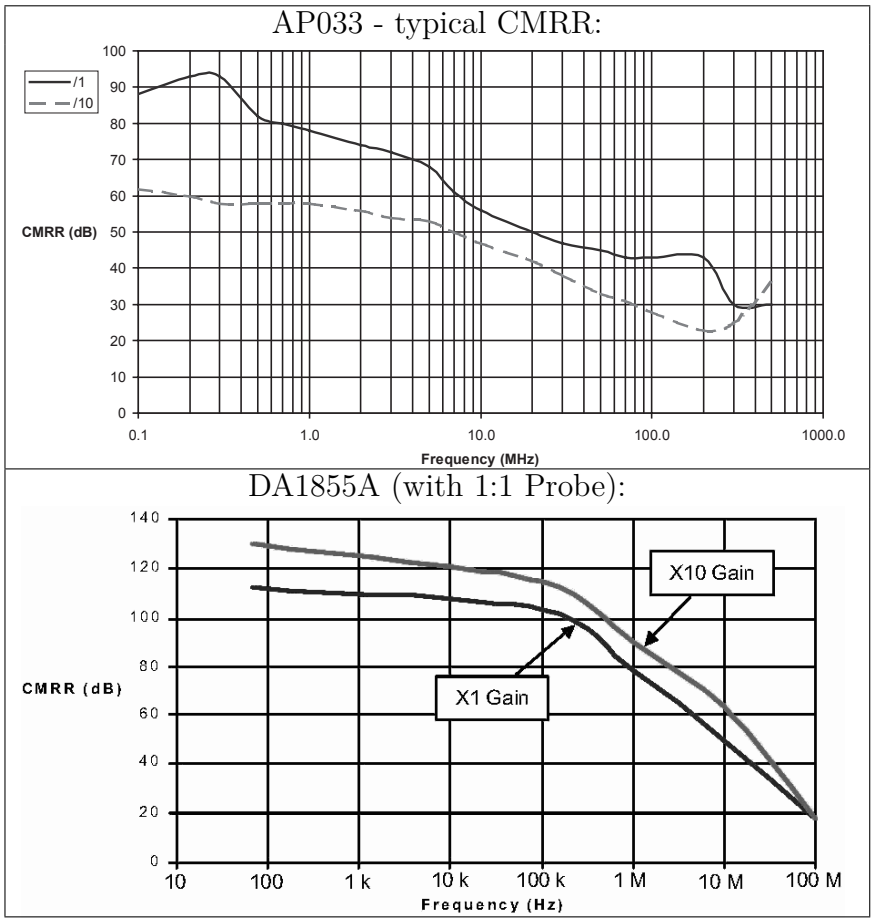


Figure 3.2: Typical CMRR curves for AP033 and DA1855A

As can be seen both devices share similar setup possibilities like variable attenuation by 1 or by 10 and variable amplification also by 1 or 10. Furthermore, both devices also have a similar differential FSR at the range of interest. However, the DA1855A features a nearly 4 times higher common mode range and a 2.5 times higher differential offset range than the AP033.

Evaluation results: Both devices were ordered for evaluation purposes. Various tests were conducted to examine which device would better suite the measurement tasks and if the investment would be justified. Those tests included for example:

- Measurements with shorted inputs to estimate input noise.
- Measurements with various standard signals.
- Measurements with small amplitude standard signals, created by a precision frequency generator and scaled down by a low noise voltage divider.
- Measurements on BMS boards with the previous X11 testchip to see results in application like conditions.

For sake of brevity, only a single exemplary comparison measurement (figure 3.3) will be presented here, whereas a summary of outcomes from the other tests will be given later on.

Figure 3.3 shows the results for a low voltage sinusoidal signal that was created by a precision frequency generator and a capacitively compensated resistive voltage divider. The divider was built up on a breadboard PCB and shielded with adhesive copper tape. The input signal was provided via a BNC socket that was directly soldered to the copper tape to avoid external disturbances. The resulting sinusoidal signal had a peak to peak amplitude of approximately 160 µV.

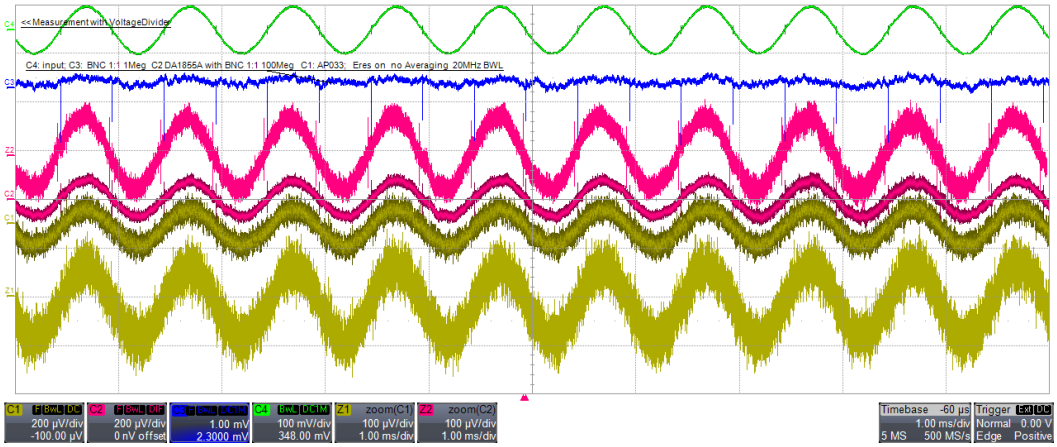


Figure 3.3: Comparison of differential measurement equipment. C1 = AP033 (yellow), C2 = DA1855A (red), C3 = std. 1:10 probe (blue), C4 = Vout Frequency generator

3.1.2. Improvements for the dynamic measurement equipment

The original undivided signal was measured with a standard 1:10 probe on channel 4 (C4, green). Channel C3 (blue) shows single-ended measurement results from the oscilloscope connected to the divider via a 1:1 BNC cable. The results in C2 (red) are from the DA1855A whereas those from C1 (yellow) are from the AP033. The signals Z1 and Z2 are just zoomed-in versions of the differential measured signals displayed in C1 and C2.

All low voltage measurement channels (C1-C3) were set up identically on the oscilloscope. As this particular test was done at a low frequency, the BWL was set to 20 MHz. Furthermore the enhanced resolution mode (ERES), which is basically a digital lowpass-filter in combination with oversampling, was turned on to further reduce the noise level. The conditions in this setup can be seen as nearly optimal, as in real applications a lot of additional disturbances will show up.

Although this setup provides nearly optimal conditions and a minimum of digital filtering is already present on all channels, hardly any signal can be seen if the oscilloscope is used without the use of differential pre-amplifying devices (C3). On the other hand the pre-amplified differential measurements on C1 and C2 are still noisy but they reveal the expected sinusoidal signal with similar results. This perfectly illustrates the necessity for differential measurement, pre-amplification, as well as digital processing, like filtering when investigating low voltage signals.

As can be seen the DA1855A shows approximately half the noise of the AP033. However, more effort was necessary to setup the DA1855A correctly, as it is more prone to earth related noise than the AP033. This is especially true if ground points are not taken with sufficient care, and the earth of the supply is not located as close as possible to the earth of the oscilloscopes supply.

Summary of evaluation results: The following results where gained through multiple comparison tests that were taken under various conditions:

Although figure 3.3 might suggest something different, dynamic voltage measurements in the range of 1 mV and below are not an easy task even with the appropriate equipment. Especially if it comes to signals in the MHz range, where noise is generally higher and less samples per second remain for oversampling or digital filtering. However, it is principally possible with both devices, although each device has its own pros and cons.

It is therefore absolutely crucial for the repeatability of a particular measurement, that all parameters of the setup are documented. This includes settings like BWL, coupling, combination of gain and attenuation, etc., as many parameters can have a direct impact on the measurement result. Otherwise analysis of the data can become misleading and measurement results may not be reproducible. Therefore, the usage of the devices together with a LeCroy oscilloscope is strongly recommended, as it allows automated documentation and recalling of all used settings.

In general the DA1855A provides more options, than the AP033. Such features include for example more analog input filters, 2 input resistance values to select from or a zero compensation that can be used whilst the probes are connected to the target. It also features a mode with ultra-low AC-coupling frequency, allowing precision AC-coupled measurements at lowest frequencies. Furthermore it also features better technical data than the AP033, in any case except for the maximum input frequency. This includes, e.g., the 3 times higher input common mode range, the approximately half input noise or the better CMRR. On the other hand the AP033 is cheaper and easier to setup and operate.

3.1.2.3 Proposed solution for dynamic measurements

The recommended setup consists of a LeCroy 64/66Zi HRO oscilloscope and a DA1855A differential pre-amplifier. This combination allows for lowest possible input noise, which is essential for single shot measurements and also for reduced effort if averaging is necessary. It furthermore allows for best adjustment to the actual measurement task, with the wide variety of setup possibilities of both devices. The possibility to let both devices interact and automatically store the used settings with the measurement data ensures repeatability.

Figure 3.4: Proposed solution for dynamic measurements: The LeCroy 64/66Zi HRO oscilloscope and the LeCroy DA1855A differential amplifier

If it is not possible to acquire this combination due to budgetary concerns, the AP033 might be used instead of the DA1855A. It is still suitable for this task, but it provides less options, slightly higher noise levels and lower CMRR.

Although the combination of the AP033 or the DA1855A with the Tektronix MSO4034B oscilloscope might seem like a cheap alternative, it is not recommended. This is due to the higher noise levels and the low signal processing capabilities of this oscilloscope. In conducted test scenarios the low processing speed and the minimal signal processing capabilities made the already tedious measurement task even more cumbersome. Also the missing storage possibility for the front-ends settings introduces an unnecessary source of setup and documentation errors.

3.2 Changes to environment simulation equipment

As already mentioned in chapter 2.3.4.1 most parts of the equipment used for generating application-like conditions of the old setup for the testchip were still usable for the TLE8000QK. This includes the power supplies, the thermal forcing system etc.

However, the main battery simulation equipment needed multiple updates because the PCB connector used with BMS 7.x boards for the testchip had changed to a new improved version. Therefore, all PCBs that are to be used with the new BMS 8.x design had to be updated (e.g., the updated capacitor array on page 34).

Furthermore, the accuracy of the currently used battery simulator did not meet the requirements. Therefore, a precision battery simulation device was needed.

3.2.1 High precision battery simulator - HPBS

One of the most stressed features of the TLE8000QK IC, besides the balancing itself, is its high DC measurement accuracy. Previously, much effort was necessary to recalibrate the Pickering Battery Simulator to allow verification of high accuracy measurements. This had to be redone for each voltage set-point, as the simulator only offered ±20 mV ±2 % of accuracy. Each calibration run included significant wait times to allow for drift effects to settle[4]. It was also revealed that the existing battery simulator was not able to hold the desired voltage constant enough over the measurement cycle of the TLE8000QK IC.

So there was the need for a more suitable battery simulator for these accuracy setups. This device should require only little or preferable no calibration effort and should emulate at least one single cell of the existing battery simulator in the chain, with a high precision cell. Multiples of these cells should also be usable to build a simulated precision battery stack.

After a short market review it was decided to build this device in house, as most devices at that time focused on higher currents and less on accuracy. Another main reason was that this also opened the possibility to use it as a platform to verify some accuracy design concepts for the main verification board on a small scale, before it was due for building. These included for example grounding techniques, power supply filtering as well as special OpAmps. It even allowed to test the usability of implementation techniques like layout replication, or parallel work in the PCB design environment (page 81). Using this opportunity was highly desirable as reaching the aimed accuracies for the verification board is a non-trivial task and timing constraints didn't allow for a second version of the main verification board.

[4]Those drift effects occurred with multiple setups, including various load current settings, minimum and maximum capacitive load etc.

3.2.1.1 Requirements

In a standard application scenario the TLE8000QK IC will be powered out of the battery pack's cells it is intended to measure. Although the voltage measurement itself is hardly loading the cells directly via the sense pins, the chip consumes more power during the measurement cycle. Hence, the IC is not only the measurement device but also a dynamic load for the battery simulator. Although this is not a problem in a real application, as the batteries input resistance is low and the chips supply current runs on separate tracks, it can be a problem with a battery simulator. The aim of this design was therefore to provide the high accuracy needed for repetitive voltage measurements even, with dynamic load currents from the TLE8000QK.

The requirements for this new high precision battery simulator (HPBS) therefore concluded into the following specification:

- Provide output voltages with roughly a magnitude better resolution than that of the TLE8000QK. This results to a resolution target of 60 µV or lower.
- The DC accuracy must at least be better than the 1.5 mV of the TLE8000QK IC. Preferably it should be better than half the TLE8000QK LSB, which results to 300 µV.
- The design should work stable with capacitive loads in the low µF range, to be usable with typical application circuitry.
- The battery simulator shall be built fully galvanically insulated, to allow free placement within a stack of battery- or battery simulator cells.
- The concept has to be extensible and affordable enough, to allow construction of a 12 channel precision device on the long run.
- Need for calibration shall be maximum once per day, compared to the once per measurement for the existing simulator.
- Even during load conditions the output voltage shall be stable enough to allow for precision measurements. This means that the resulting changes shall be less than half an LSB of the TLE8000QK. As the chip was still in development during the time the HPBS was built, the load currents for the simulator were defined in such a way that they were more than twice as high as expected by simulation results of the chip under worst case conditions.
  - The simplest load condition is specified as the cell voltage measurement current alone which was defined to 50 µA. This means the chip is not supplied from the HPBS during this measurement.
  - The second load condition is specified as measurement and chip supply at the same time. For this setup the load current is defined as the 50 mA

plus the 50 µA via the measurement path.

3.2.1.2 Difficulties in reaching high accuracy

Although in the worst case an accuracy of better than 1.5 mV would already be acceptable, an accuracy of less than 300 µV with a 5 V output or in other words better than 60 ppm or 0.006 % should be aimed for.

Although special OpAmps are available that offer extreme low offset or gain errors, the overall sum of deviations of every single part in the circuit has to be good enough to achieve this high accuracy target. Therefore, each part is only allowed to contribute to a fraction of the overall error.

This results in a huge design restriction as most common OpAmp circuits depend on the matching of external passive parts to achieve high accuracy. A market survey showed that even with single chip resistor arrays, relative matchings better than 100 ppm are hard to get and values in the 10 ppm range are too expensive. Therefore, most analog circuits like adders or subtractors cannot be used as they would introduce an unacceptable amount of error just from their dependency on passive components.

As a result the circuitry of the HPBS had to be designed in such a way that the accuracy depends on as little passive components as possible.

3.2.1.3 Basic concept

The basic concept of the HPBS can be seen in figure 3.5. The idea is to combine a powerful but inaccurate output driver with a precision control operational amplifier to gain a highly accurate and still powerful output stage for a precision source. In this case the source is an extremely accurate DAC connected to a calibrateable precision reference.

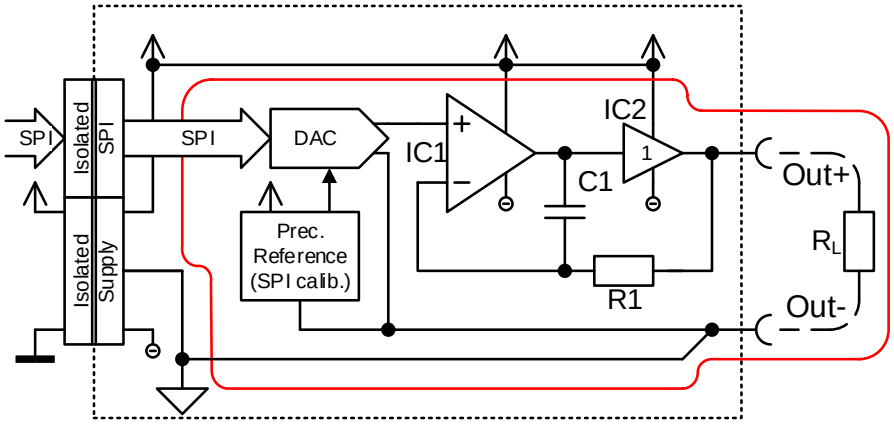


Figure 3.5: Basic concept of the HPBS control circuit

The idea for the controlled output stage is rather simple but powerful and can be found in similar forms in other sources like [Jim07]. The control circuitry basically forms an inverting integrator circuit, that sums up all the deviations until the output driver's output matches that of the source. Once equilibrium is reached the integrator's capacitor stores the output driver's offset voltage and compensates for it. Therefore, the DC precision is not depending on the power stage any more, but is mainly defined by the more accurate operational amplifier and by the DAC's output accuracy.

Although this concept seems simple at the first glance, reaching accuracies below 1 mV is a task that requires great care along the design process. Therefore, the concept as well as all main parts involved will be analyzed here in detail. However, as the developed force-sense concept is basically just an add-on to this base circuitry, it will first be left out from this analysis and introduced on page 86 onwards.

Mathematical analyzes of the circuit

In this section the basic mathematical equations will be derived to proof the above statements. Figure 3.6 shows an annotated version of the core control loop of the HPBS.

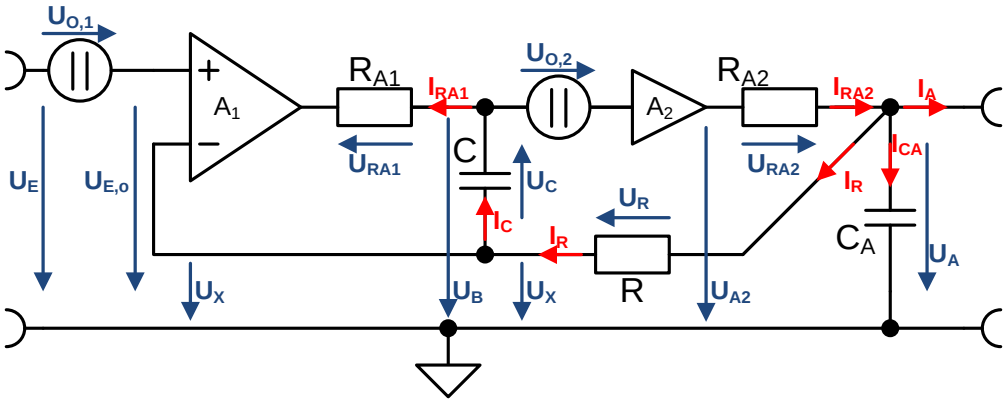


Figure 3.6: HPBS annotated for calculation

In this version of the drawing some non-idealities like the finite gain or output resistance are shown. The arrows show the convention for current directions used for the following equations.

3.2.1. High precision battery simulator - HPBS

First of all some basic dependencies are being derived from the schematic:

$$U_{E,o} = U_E - U_{o,1} \tag{3.3}$$
$$U_R = U_A - U_X \tag{3.4}$$
$$I_R = I_{R,A1} = I_C \tag{3.5}$$
$$I_{CA} = sC_A U_{CA} = sC_A U_A \tag{3.6}$$
$$I_R = \frac{U_R}{R} = \frac{U_A - U_X}{R} \tag{3.7}$$
$$I_{R,A2} = I_{CA} + I_R + I_A = sC_A U_A + \frac{U_A - U_X}{R} + I_A \tag{3.8}$$

Then two equations for U_X are being derived, so that they can later on be joined via the use of U_X.

$$\begin{aligned} U_B &= (U_{E,o} - U_X)A_1 + I_R R_{A1} \\ &\vdots \\ U_X &= U_{E,o} - \tfrac{U_B}{A_1} + \tfrac{U_A - U_X}{R}\tfrac{R_{A1}}{A_1} \\ \Rightarrow\ U_X &\left(1 + \tfrac{R_{A1}}{A_1 R}\right) = U_{E,o} - \tfrac{U_B}{A_1} + U_A \tfrac{R_{A1}}{A_1 R} \end{aligned} \tag{3.9}$$

$$\begin{aligned} U_X &= U_B + U_C = U_B + \tfrac{I_C}{sC} \\ &\vdots \\ U_X &= U_B + \tfrac{U_A - U_X}{sCR} \\ \Rightarrow\ U_X &\left(1 + \tfrac{1}{sCR}\right) = U_B + \tfrac{U_A}{sCR} \end{aligned} \tag{3.10}$$

These equations still contain the unwanted internal variable U_B. Therefore, an additional equation is needed that expresses U_B without the introduction of new variables. It can be derived from the dependency of U_B from the output voltage. However, in an intermediate step U_{A2} has to be calculated first.

$$U_A = U_{A2} - I_{R,A2} R_{A2} \tag{3.11}$$
$$\begin{aligned} &\vdots \\ U_A &= U_{A2} - \left(sC_A U_A + \tfrac{U_A - U_X}{R} + I_A\right) R_{A2} \\ \Rightarrow\ U_{A2} &= U_A \left(1 + sC_A R_{A2}\right) + \tfrac{U_A - U_X}{R} R_{A2} + I_A R_{A2} \end{aligned} \tag{3.12}$$

$$U_{A2} = (U_B - U_{o,2})A_2 \tag{3.13}$$
$$\begin{aligned} &\vdots \\ U_B &= \tfrac{U_{A2}}{A_2} + U_{o,2} \\ \Rightarrow\ U_B &= \tfrac{U_A}{A_2}\left(1 + sC_A R_{A2}\right) + \tfrac{U_A - U_X}{A_2 R} R_{A2} + I_A \tfrac{R_{A2}}{A2} + U_{o,2} \end{aligned} \tag{3.14}$$

Now, this equation for U_B (3.14) is inserted into the equations for U_X (3.9 and 3.10). After grouping all terms the following intermediate results are given:

$$U_X \left(1 + \frac{R_{A1} - \frac{R_{A2}}{A2}}{A_1 R}\right) = U_{E,o} + U_A \left(\tfrac{R_{A1} - \frac{R_{A2}}{A2}}{A_1 R} - \tfrac{1 + sC_A R_{A2}}{A_1 A_2}\right) - \tfrac{I_A R_{A2}}{A_1 A2} - \tfrac{U_{o,2}}{A1} \tag{3.15}$$

$$U_X \left(1 + \frac{1}{sCR} + \frac{R_{A2}}{A_2 R}\right) = U_A \left(\tfrac{1}{A_2} + \tfrac{sC_A R_{A2}}{A_2} + \tfrac{R_{A2}}{A_2 R} + \tfrac{1}{sRC}\right) + \tfrac{I_A R_{A2}}{A2} + U_{o,2} \tag{3.16}$$

Combining the above equations (3.15 and 3.16) eliminates U_X. The result is a formula that allows calculation of the output voltage U_A with regards to all the other input values.

$$\frac{U_{E,o}+U_A\left(\frac{R_{A1}-\frac{R_{A2}}{A2}}{A_1R}-\frac{1+sC_AR_{A2}}{A_1A_2}\right)-\frac{I_AR_{A2}}{A_1A2}-\frac{U_{o,2}}{A1}}{\left(1+\frac{R_{A1}-\frac{R_{A2}}{A2}}{A_1R}\right)}=\frac{U_A\left(\frac{1}{A_2}+\frac{sC_AR_{A2}}{A_2}+\frac{R_{A2}}{A_2R}+\frac{1}{sRC}\right)+\frac{I_AR_{A2}}{A2}+U_{o,2}}{\left(1+\frac{1}{sCR}+\frac{R_{A2}}{A_2R}\right)} \tag{3.17}$$

Intermediate result and assumptions: To ease further calculations, a first assumption is made. For most low to modest frequencies the output resistances R_{A1} and R_{A2} will be low whereas the factor A_1R will be huge. Therefore, the term $\frac{R_{A1}-\frac{R_{A2}}{A2}}{A_1R}$ may be neglected with hardly any impact on the result. This allows for a more compact equation for U_A.

$$\frac{U_{E,o}+U_A\left(0-\frac{1+sC_AR_{A2}}{A_1A_2}\right)-\frac{I_AR_{A2}}{A_1A2}-\frac{U_{o,2}}{A1}}{(1+0)}\approx\frac{U_A\left(\frac{1}{A_2}+\frac{sC_AR_{A2}}{A_2}+\frac{R_{A2}}{A_2R}+\frac{1}{sRC}\right)+\frac{I_AR_{A2}}{A2}+U_{o,2}}{\left(1+\frac{1}{sCR}+\frac{R_{A2}}{A_2R}\right)}$$

$$\vdots$$

$$\Rightarrow U_A=\frac{(U_E-U_{o,1})\left(s+\frac{1}{CR}+\frac{sR_{A2}}{A_2R}\right)-\left(U_{o,2}+I_A\frac{R_{A2}}{A_2}\right)\left[s+\frac{1}{A1}\left(s+\frac{1}{CR}+\frac{sR_{A2}}{A_2R}\right)\right]}{\left(\frac{s}{A_2}+\frac{s^2C_AR_{A2}}{A_2}+\frac{sR_{A2}}{A_2R}+\frac{1}{RC}\right)+\left(s+\frac{1}{CR}+\frac{sR_{A2}}{A_2R}\right)\left(\frac{1+sC_AR_{A2}}{A_1A_2}\right)} \tag{3.18}$$

Estimations and properties: Although equation 3.18 seems rather complex some basic properties can already be seen. For example, the different behavior for input voltage changes compared to that for disturbances like $U_{o,2}$ or I_A. Furthermore, some estimations can be made if the orders of magnitude of some of the parameters are taken into account.

As first estimation the DC behavior will be investigated. At DC the amplification A_1 will be extremely high whereas the parameter s will tend to zero. Therefore, also the terms $1/A_1$ or especially s/A_1 can be neglected.

$$\begin{aligned} U_{A,DC} &= \lim_{s\to 0}\frac{(U_E-U_{o,1})\left(s+\frac{1}{CR}+\frac{sR_{A2}}{A_2R}\right)-\left(U_{o,2}+I_A\frac{R_{A2}}{A_2}\right)[s+0]}{\left(\frac{s}{A_2}+\frac{s^2C_AR_A}{A_2}+\frac{sR_{A2}}{A_2R}+\frac{1}{RC}\right)+0} \\ &= \frac{(U_E-U_{o,1})\left(0+\frac{1}{CR}+0\right)-\left(U_{o,2}+I_A\frac{R_{A2}}{A_2}\right)\cdot 0}{\left(0+0+0+\frac{1}{RC}\right)} \\ \Rightarrow U_{A,DC} &= U_E-U_{o,1} \end{aligned} \tag{3.19}$$

The result of the estimation shows that this circuit truly follows the input voltage U_E except for the integrators offset. Even if the amplification factor A_2 of the output buffer is only roughly equal to 1, or the output current is not equal zero this circuit will tend to reach the input voltage.

The only value that cannot be accounted for is the input offset voltage of the first amplifier $U_{o,1}$, which states the difference between U_E and U_{E1}. It is therefore essential to use an amplifier with adequate offset behavior.

But equation 3.18 can also be used to estimate the behavior at higher frequencies. Here the quadratic s terms in the denominator, that all contain $s^2 C_A R_{A2}$, soon become dominant. This basically illustrates the dampening effect of the output drivers finite resistance and the load capacitor, which means that fast changes of, e.g., U_E take some time to be fully reflected on the circuits output.

On the other hand C_A helps to dampen the impact of fast load current (I_A) changes on the output voltage, if highest frequencies are taken into account. This can be seen from the I_A part of equation 3.18, if terms that become small at high frequencies are neglected.

$$\begin{aligned} U_{A,I_{A,fast}} &\overset{s\uparrow\uparrow}{\approx} \frac{-\left(I_A \frac{R_{A2}}{A_2}\right)\left[s + \frac{s}{A1}\left(1 + \cancel{\frac{1}{sCR}} + \frac{R_{A2}}{A_2 R}\right)\right]}{\frac{s^2 C_A R_{A2}}{A_2} + \frac{s^2 C_A R_{A2}}{A_1 A_2} + \frac{s^2 C_A R_{A2}}{A_1 A_2}\frac{R_{A2}}{A_2 R}} \approx -\frac{I_A\left[1 + \frac{1}{A_1} + \frac{R_{A2}}{A_1 A_2 R}\right]}{sC_A\left[1 + \frac{1}{A_1} + \frac{R_{A2}}{A_1 A_2 R}\right]} \\ &\approx -I_A X_{CA} \end{aligned} \tag{3.20}$$

This means that the current related output changes at highest frequencies mainly depend on the output capacitors reactance. Therefore, bigger capacitors will further reduce the first fast voltage drop that the output buffer could not handle due to its limited speed.

But this positive damping effect does not come without a downside. Because of the quadratic $s^2 C_A R_{A2}$ term, the system is now able to oscillate. Sufficient care has therefore to be taken in the design process to prevent such oscillations as will be discussed on page 73 onwards.

3.2.1.4 Selection of the main control parts

Results for part selection: Now that a basic understanding of the circuit behavior is given, suitable parts can be searched for, to simulate and build it. This is always an iterative process, as the overall system depends on the performance of each single part. Therefore, if a single part in the chain isn't available as desired, the whole system might need to be redesigned. It was therefore highly anticipated to use parts with standard footprints and pinouts, which allow for simple later exchange if necessary.

For the integrating amplifier the preceding estimations mean that an amplifier is needed with extremely low input offset voltage, and at the same time high amplification over a large as possible bandwidth. The output buffer on the other hand should provide low output resistance, high current drive capability and fast response time. Also, a sufficiently accurate voltage reference and a DAC are needed to fulfill the required accuracy target.

The main integrating OpAmp

As previously stated the circuit's output accuracy is mainly defined by the main integrator's OpAmp. For example, to achieve the wanted high levels of A_1 over a wide frequency range, the OpAmp has to have both, a high DC amplification (A_0) as well as a high gain bandwidth product (GBWP). The higher the GBWP-value the broader the frequency range that the OpAmp provides a high value for A_1.

As far as the offset is concerned, there are two major groups of amplifiers that can be taken into consideration. First, there are "standard" precision amplifiers, which might be trimmed at factory to achieve the requirements. Such types claim to reach offsets in the 100 µV range, or some even below. However, this value is most likely only typical and sums up with other error sources like from part to part variation, common mode, or temperature effects. For example, many newer OpAmps on the market feature Rail-to-Rail Inputs and Outputs (RRIO). Although this can be very useful, it requires a more complex input stage, which in turn is harder to compensate for [Wal08], especially over the whole common mode voltage or temperature range. So it often happens, especially with RRIO types that the initially specified offset voltage in the datasheet would meet the target, but as soon as the change of the offset voltage is accounted for over the whole desired input range, the OpAmp reveals a magnitude worse offset, and is therefore not usable[5].

There is also a second group of OpAmps that actually uses various techniques to actively cancel the offset on the fly. OpAmps featuring such technologies are often called "chopper", "chopper-stabilized", "zero-drift", or "auto-zero" operational amplifiers, depending on the manufacturer and the actually used cancellation technique. The basic ideas are very similar, and the following will explain some of the used concepts. For the rest of this thesis the term "self-zeroing" will be used to refer to any kind of OpAmp that uses one of the multiple ways to reduce offsets by some automatic technique.

Short explanation of offset canceling techniques in OpAmps: One of the first self-zeroing techniques[6] was the so called chopper amplifier [Wal09],[Tho05], which used modulation to allow DC amplification with the use of an AC amplifier, which can not show DC offsets. This means that the DC signal is first modulated to AC, then amplified, and afterwards synchronously demodulated and filtered (figure 3.7). As the amplifier only needs to amplify AC signals, its own DC offset can easily be blocked by a simple capacitor. However, as this is a switched technique, the bandwidth is very limited, and filters are needed to avoid aliasing effects.

[5] For example the AD8615 is specified to have a typical offset voltage of 23 µV and a maximum offset voltage of 65 µV. However, if the full common mode range is taken into account this immediately increases to 500 µV, even at room temperature! It was therefore necessary to carefully investigate the datasheets from all manufactures to reveal the true possible offsets for this application. This drastically reduced the amount of possible candidates.

[6] Chopper and Chopper-stabilized amplifiers were already used around the 1940s in tube amplifiers, for example in the so called Goldberg configuration. [Joh08]

3.2.1. High precision battery simulator - HPBS

Another very basic idea is to periodically disconnect and internally short the amplifiers inputs and directly measure its offset at this simulated zero input voltage. This offset voltage is then stored inside a capacitor and fed back to the offset compensation of the amplifier (figure 3.8). However, this has to be done periodically which also builds up a switched system [Rez00a; Rez00b].

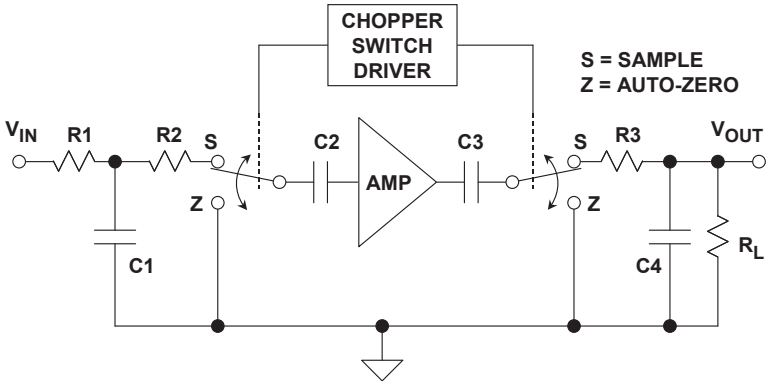


Figure 3.7: Principle of a Chopper Amplifier [Wal09]

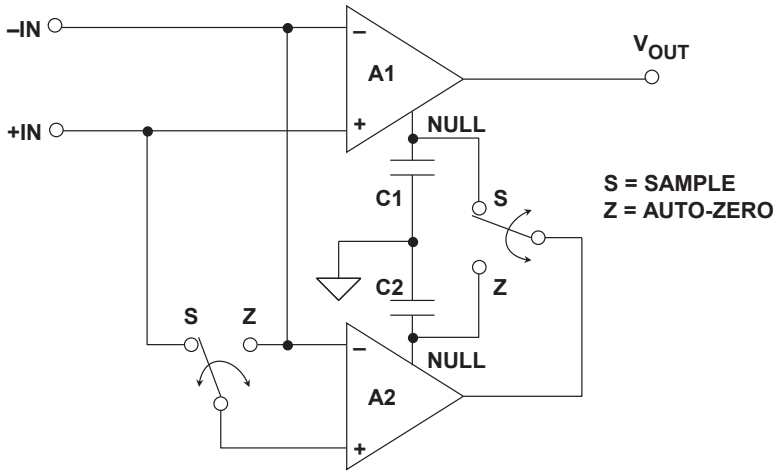


Figure 3.8: Principle of an Auto-Zero Amplifier [Wal09]

As a result most of these techniques initially offered a very limited frequency range. Todays more advanced technologies therefore combine multiple of these self-zeroing concepts with standard OpAmps to allow continuous operation, DC accuracy, and high frequency amplification all at once. This is possible due to the high integration possibilities in todays CMOS technologies, which allow building of complex systems including the control logic inside a single chip at reasonable cost [Tho05, page 22]. In a chopper-stabilized amplifier, for example, a sufficiently filtered chopper amplifier is used for low frequency amplification, whereas a standard amplifier is used for higher frequencies. It is also possible to use a self-zeroing amplifier to tune a standard amplifier, until its input terminal voltages are exactly equal. The list of possibilities is huge, and each manufacturer favors its own patented approach.

But there are also drawbacks arising from such more advanced compensation techniques. First of all, the devices become more complex and therefore more expensive. Beyond that, all technologies include some kind of switching, which introduces disturbances [Tho05, page 24,26]. And even although every manufacturer tries to minimize such switching noise as good as possible, coupling to the inputs or output of the amplifier can never be fully avoided.

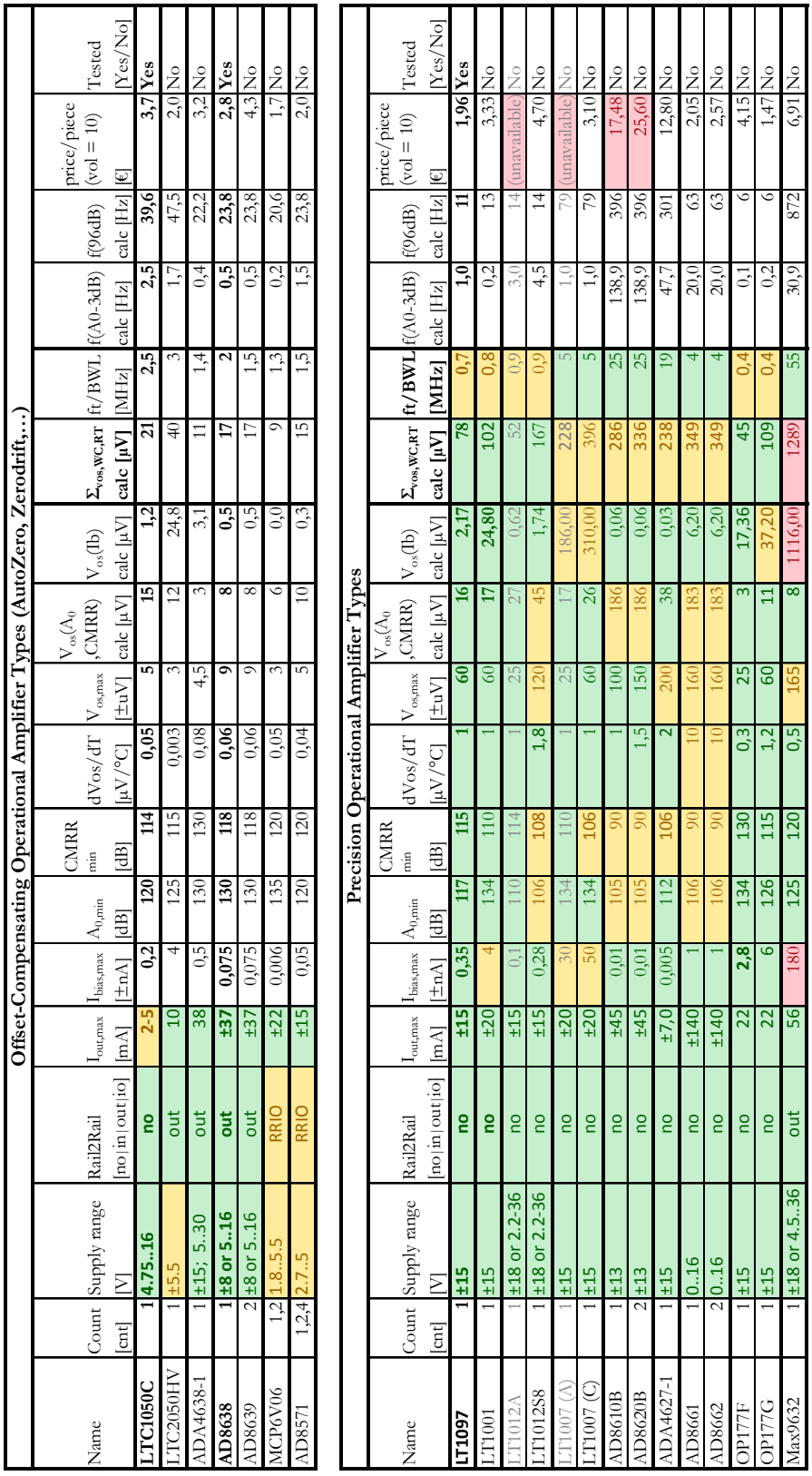
Actual amplifier selection: The requirements for possible candidates are:

- A maximum offset voltage, including deviations originating from A_0 and I_b well below the overall target of 300 µV, to provide sufficient headroom for errors of the DAC and reference. This often means that the specified typical offset values has to be better than ≈100 µV, as can be seen in table 3.8.
- A_0 of around 100 dB which corresponds to less than 50 µV additional offset for DC signals.
- GBWP or transit frequency of around 1 MHz, preferably higher, to have A_0 up to a highest possible frequency range
- SOIC-8 footprint with a standard pinout, to allow later exchange for even further performance upgrades.
- Supply voltage range should support sufficient overhead to provide enough drive strength even at high common mode values
- The single ended input voltage range has to be 0 V to 5 V.
- The differential input voltage range has to allow −5 V to 5 V.[7]
- Although the device will be operated at 25 °C in the laboratory, it shall work in a range from 5 °C to 45 °C to account for expected excess air currents from nearby equipment like temperature forcing systems.

With these requirements the available databases of OpAmp manufacturers were searched. Although most self-zeroing OpAmps had outstanding specification values, hardly any information was given about switching noise in the time domain. Therefore, the search was not only conducted over the self-zeroing types but also across the conventional types, to provide a fallback option just in case of need. From all the checked OpAmps the most promising parts and their datasheet parameters are summarized in table 3.8. Because of the necessity for pin compatibility, this table only contains devices that are (also) available in a SOIC-8 package with standard footprint, at least for their single opamp version.

[7] This criteria prevents the usage of many otherwise perfectly suitable parts, like e.g. AD8675. Because, if either the input or the output voltage changes rapidly currents would start to flow across the internal protection structures of the OpAmp.

3.2.1. High precision battery simulator - HPBS



Offset-Compensating Operational Amplifier Types (AutoZero, Zerodrift,...)

Name	Count [cnt]	Supply range [V]	Rail2Rail [no | in | out | io]	$I_{out,max}$ [mA]	$I_{bias,max}$ [±nA]	$A_{0,min}$ [dB]	$CMRR_{min}$ [dB]	dVos/dT [µV/°C]	$V_{os,max}$ [±uV]	$V_{os}(A_0,CMRR)$ calc [µV]	V_{os}(Tb) calc [µV]	$\Sigma_{vos,WC,RT}$ calc [µV]	ft/BWL [MHz]	f(A0-3dB) calc [Hz]	f(96dB) calc [Hz]	price/piece (vol = 10) [€]	Tested [Yes/No]
LTC1050C	**1**	**4.75..16**	**no**	**2-5**	**0,2**	**120**	**114**	**0,05**	**5**	**15**	**1,2**	**21**	**2,5**	**2,5**	**39,6**	**3,7**	**Yes**
LTC2050HV	1	±5.5	out	10	4	125	115	0,003	3	12	24,8	40	3	1,7	47,5	2,0	No
ADA4638-1	1	±15; 5..30	out	38	0,5	130	130	0,08	4,5	3	3,1	11	1,4	0,4	22,2	3,2	No
AD8638	**1**	**±8 or 5..16**	**out**	**±37**	**0,075**	**130**	**118**	**0,06**	**9**	**8**	**0,5**	**17**	**2**	**0,5**	**23,8**	**2,8**	**Yes**
AD8639	2	±8 or 5..16	out	±37	0,075	130	118	0,06	9	8	0,5	17	1,5	0,5	23,8	4,3	No
MCP6V06	1,2	1.8..5.5	RRIO	±22	0,006	135	120	0,05	3	6	0,0	9	1,3	0,2	20,6	1,7	No
AD8571	1,2,4	2.7..5	RRIO	±15	0,05	120	120	0,04	5	10	0,3	15	1,5	1,5	23,8	2,0	No

Precision Operational Amplifier Types

Name	Count [cnt]	Supply range [V]	Rail2Rail [no | in | out | io]	$I_{out,max}$ [mA]	$I_{bias,max}$ [±nA]	$A_{0,min}$ [dB]	$CMRR_{min}$ [dB]	dVos/dT [µV/°C]	$V_{os,max}$ [±uV]	$V_{os}(A_0,CMRR)$ calc [µV]	V_{os}(Tb) calc [µV]	$\Sigma_{vos,WC,RT}$ calc [µV]	ft/BWL [MHz]	f(A0-3dB) calc [Hz]	f(96dB) calc [Hz]	price/piece (vol = 10) [€]	Tested [Yes/No]
LT1097	**1**	**±15**	**no**	**±15**	**0,35**	**117**	**115**	**1**	**60**	**16**	**2,17**	**78**	**0,7**	**1,0**	**11**	**1,96**	**Yes**
LT1001	1	±15	**no**	±20	4	134	110	1	60	**17**	**24,80**	**102**	**0,8**	0,2	13	3,33	No
LT1012A	1	±18 or 2.2-36	no	±15	0,1	110	114	1	25	27	0,62	52	0,9	3,0	14	(unavailable)	No
LT1012S8	1	±18 or 2.2-36	no	±15	0,28	106	108	1,8	120	45	1,74	167	0,9	4,5	14	4,70	No
LT1007 (A)	1	±15	no	±20	30	134	110	1	25	17	186,00	228	5	1,0	79	(unavailable)	No
LT1007 (C)	1	±15	no	±20	50	134	106	1	60	26	310,00	396	5	1,0	79	3,10	No
AD8610B	1	±13	no	±45	0,01	105	90	1	100	186	0,06	286	25	138,9	396	17,48	No
AD8620B	2	±13	no	±45	0,01	105	90	1,5	150	186	0,06	336	25	138,9	396	25,60	No
ADA4627-1	1	±15	no	±7,0	0,005	112	106	2	200	38	0,03	238	19	47,7	301	12,80	No
AD8661	1	0..16	no	±140	1	106	90	10	160	183	6,20	349	4	20,0	63	2,05	No
AD8662	2	0..16	no	±140	1	106	90	10	160	183	6,20	349	4	20,0	63	2,57	No
OP177F	1	±15	no	22	**2,8**	134	130	0,3	25	3	17,36	45	0,4	0,1	6	4,15	No
OP177G	1	±15	no	22	6	126	115	1,2	60	11	37,20	109	0,4	0,2	6	1,47	No
Max9632	1	±18 or 4.5..36	out	56	180	125	120	0,5	165	8	1116,00	1289	55	30,9	872	6,91	No

Table 3.8: HPBS OpAmp selection table for low offset and high speed. Values are at room temperature. Single CH devices are pin compatible (SOIC-8). Types in use in this thesis are highlighted bold.

As datasheets are not standardized, the way parameters are given either as minimum, typical, or maximum value, as values or as graphs, linear or in decibel varies widely. It was therefore tried to find the most comparable values across all the datasheets, which means that the presented values may sometimes actually be calculated out of multiple parameters from a single datasheet to make it comparable with the others. In general all parameters reflect room-temperature values but under worst case conditions, like full voltage range. Some other parameters were also calculated and are marked with the add-on "calc" next to their unit. For example, the offset voltage caused by the OpAmps input current $V_{OS}(I_b)$ across the expected 6.2 kΩ output resistance of the DAC (see table 3.11) is also calculated. This is, e.g., the reason why the otherwise exceptional MAX9632 cannot be used for this application.

From all the devices presented in table 3.8, two were selected to conduct further simulations with. Namely the LTC1050 which is a Zero-Drift type and the LT1097 which is a conventional precision type amplifier. Each device provides the best compromise in its type between overall accuracy, speed and price.

The output driver

In order to emulate the fast transient response of a battery cell, the output driver has to react extremely quickly on load changes and provide sufficient current. Although the output capacitor is helping to level out the fastest load changes, it also means that the output driver has to be stable with capacitive loads. Furthermore, the output resistance of the buffer as well as its acceptable supply voltage range also have large impacts on how fast the output capacitor can be recharged, once it was altered by the load current.

The LT1010: The LT1010 is a very fast buffer IC, and although its design is nearly 30 years of age, it is one of the few buffer ICs available, that is by itself stable with driving capacitive loads in the µF range. In fact its datasheet explicitly states "Isolate Capacitive Loads" as one of the typical applications [Lin91a]. It provides up to ±150 mA of continuous output current and a maximum transit frequency of 20 MHz. However, this transit frequency steadily decreases with increasing load capacitance.

Other important specification values are an offset voltage of 150 mV maximum and an output resistance of 10 Ω. This makes it very clear why a precision OpAmp is needed to achieve the required DC accuracy.

MAX9550/MAX9551 - VCOM Driver: Then there is another type of output drivers for large capacitive loads. It was designed especially for the needs in LCD panels where liquid crystals are placed between electrodes that form a capacitor. By changing the polarity of voltage applied to the electrodes the crystals can be

rotated. To avoid unnecessary aging of the device it is necessary to keep the crystals on average free of DC voltages. If the common side of all pixels is held at ground level (VCOM = 0 V), the switching side of the pixels would need to provide positive and negative voltages to rotate the crystals back and forth. As an cheaper alternative it is also possible to shift VCOM to the middle of the supply rail and use simple switches that switch the other electrode between the positive supply and ground.[Ogi09]

But it is essential that VCOM can be calibrated exactly and highly automated at the LCD panel factories. Therefore, a voltage buffer is needed, that is stable with the high capacitive loads on the VCOM line. Furthermore, this virtual supply rail has to be very stable against the high current transients that occur from the high speed pixel switching [Cor05].

As a result many specialized ICs have been created for this purpose by many manufacturers. Unfortunately only a few types are available for orders with low volumes. Most of these, especially newer generation ICs, already incorporate many more functions specialized for LCD panels, like the DAC needed in front of the VCOM driver. This is a problem as these DACs do not provide the required accuracy or resolution, and are most likely directly connected to the VCOM driver internally. Therefore, only the MAX9551 remained as suitable candidate that is currently available in small quantities[8].

The MAX9551 is a dual channel[9] VCOM driver designed to provide up to ±800 mA of peak and ±55 mA of continues current. The huge difference in dynamic and static current already shows that this device is especially designed for capacitive loads, where it greatly outperforms the LT1010. Also the typical offset of 1 mV with a maximum of 10 mV over the whole temperature range is closer to the desired application. Furthermore, the datasheet tells that internally an operational transconductance amplifier (OTA) is used in such a way that its transconductance increases with increasing output current. This allows for very fast settling times on the one hand, but provides the problem that an additional not further described internal feedback loop is present, that might collide with the planned external feedback loop, which could cause instabilities. Therefore, simulation results were planned to show if these occurred, and how much improvement could be gained in comparison to a standard LT1010 device.

3.2.1.5 DAC and Reference selection

There is an extremely high number of DACs available on the market today. However, as soon as superior DC performance is desired, the majority of the devices render useless as they come combined with internal buffer amplifiers and references

[8] The MAX9651 is a pin compatible higher current version of the MAX9551. It was not available at the time of testing, but may be of interest for future designs.

[9] The MAX9550 is the not available single channel version of the used MAX9551.

with accuracies and stability factors far off the desired target. It was therefore necessary to search for two independent devices. A truly DC accurate DAC with unbuffered outputs, and a sufficiently capable voltage reference IC.

DAC selection - the LTC2641

Just like with all the previous components also here all major suppliers were searched for a suitable part. As all DACs tend to have non-idealities like non-linearity or gain errors in the order of several LSB, it was necessary to search for devices with at least 16 Bit (76 µV) of resolution, to keep the effective deviations in volt minimal. Fortunately a de facto standard SOIC-8 pinout could be identified that is supported by many manufacturers for this class of unbuffered DACs.

The finally chosen device is of the LTC2641 family, which offers a 16 Bit version in this SOIC-8 footprint and also an additional drastically cheaper DFN (Dual Flat No-lead) - Package with 12 Bit, 14 Bit and 16 Bit of resolution. As this package is extremely small it allows for a PCB Layout that combines both packages, giving a cheap precision solution with a high count of second source possibilities[10].

Voltage reference selection

The voltage reference is one of the key parts that define the overall accuracy of the HPBS to build. Currently, there are numerous precision reference ICs available from a variety of manufacturers that allow high accuracies off the shelf. However, reference ICs with an initial accuracy of less than ±1 mV are difficult to get and only a few types are available with values down to ±0.5 mV. A reason for this may come from the soldering stress that easily causes voltage shifts in the range of several 100 µV according to [Cor10]. As manufacturers typically only specify the accuracy of the device prior to soldering, paying for higher initial accuracies would therefore be rendered pointless.

Therefore, reaching higher accuracies depends on calibration as well as the stability of the used reference against, e.g., thermal or long-term drift effects. Table 3.9 shows a selection of possible high accuracy reference candidates. The largest contribution to the remaining drift factor is by far the temperature coefficient. As this factor is highly non-linear and normally only specified in a far greater range than intended to be used with the HPBS, additional manual readouts from the typical temperature deviation graphs were also added where available.

While the LTZ1000A definitively leads the performance in table 3.9 it is also the device with the highest overall implementation effort. It is therefore mainly used in absolutely highest accuracy equipment, where price is on second order, like in

[10] Other device families that could be used instead are DAC883x, AD55x1, MAX5541 or the MAX541

	Ref5050ID	AD586B	ISL21009B	**MAX6250AC**	**Max6350C**	VRE3050JS	LTZ1000A
Vref [V]	5	5	5	**5**	**5**	5	7,2
Underlying principle	Bandgap	B. Zener	FGA	**B. Zener**	**B. Zener**	B. Zener	Heated B. Zener
Init. accuracy @25°C, no load [%]	0,05	0,049	0,01	**0,02**	**0,02**	0,01	7
Temp coef, full range,max[ppm/°C]	3	5	3	**2**	**1**	0,6	0,05
Noise 0.1-10Hz [µVpp]	15	4	4,5	**1,5**	**3**	3	1,2
long-term stab [ppm/√kHr]	100	15	10	**20**	**30**	6	0,3
Iout max [±mA]	25	45	10	**15**	**15**	15	n.a.
Load regulation [ppm/mA]	30	20	4	**6**	**6**	12	n.a.
Settling time [µs]	200		100	**10**	**10**	2	n.a.
Line regulation [ppm/V]	1	20	18	**30**	**7**	35	n.a.
Package	SOIC8	SOIC8	SOIC8	**SOIC8**	**SOIC8**	SOIC8	TO-99
Price @ 10 pieces	€ 3,91	€ 10,50	€ 9,60	**€ 9,58**	**€ 10,55**	€ 94,40	€ 55,00
Trimm input [Yes/No]	Yes	Yes	Yes	**Yes**	**Yes**	Yes	Yes
Typical trimm range [±mV]	5	300	125	**25**	**25**	5	n.a.
Calc Initial Offest [µV]	2,5mV	2,45mV	0,5mV	**1mV**	**1mV**	0,5mV	200mV
Max Coef Temp Dev. (±20°C) [µV]	600	1000	600	**400**	**200**	120	14,4
Temp dev. from graph (±20°C) [µV]	400	1000	500	**80**	**80**	100	14,4
Error after 1000H [µV]	500	75	50	**100**	**150**	30	2,1
Error after 1Day 24H [µV]	77	12	8	**15**	**23**	5	0
Max temp dev. (±20°C)+ 1Day [µV]	677	1012	608	**415**	**223**	125	15
Typ temp dev. (±20°C)+ 1Day [µV]	477	1012	508	**95**	**103**	105	15

Table 3.9: Selection of various highest precision reference ICs

the HP/Agilent 3458A 8 1/2 digit multimeter[11]. It is even recommended for space programs [RLJ97] and at least in 2005 it was still rated as one of the best electronic reference ICs [Har05]. Although this is beyond the needs for the HPBS it gives an indication on what is possible.

As can be seen from table 3.9, the MAX6250 and MAX6350 were selected because of their overall good performance at still reasonable price. Although the MAX6350 shows better worst-case results, the MAX6250 had to be used in the demonstrator prototype due poor supply of the other and is therefore used for all further calculations. Despite the difference in the maximum temperature related offset changes, the typical characteristics (figure 3.9) are around 80 µV or 0.4 ppm/°C for both devices in the target temperature range of 5 °C to 45 °C.

Recalibrateable reference circuitry

As the accuracy target is 300 µV (half a TLE8000QK LSB) in-system calibration is inevitable. All the references presented in table 3.9 allow for later calibration. But one has to be very careful not to degenerate the good performance of these references with an improperly designed external trimming. Furthermore, as many of HPBS devices should be usable at the same time, a digital controllable trim mechanism was highly desired over manual potentiometer trimming.

[11] More information about the LTZ1000 circuitry inside the HP/Agilent 3458A can be found, e.g., under http://www.prc68.com/I/HP3458DVM.shtml or http://www.prc68.com/I/HP3458DVM

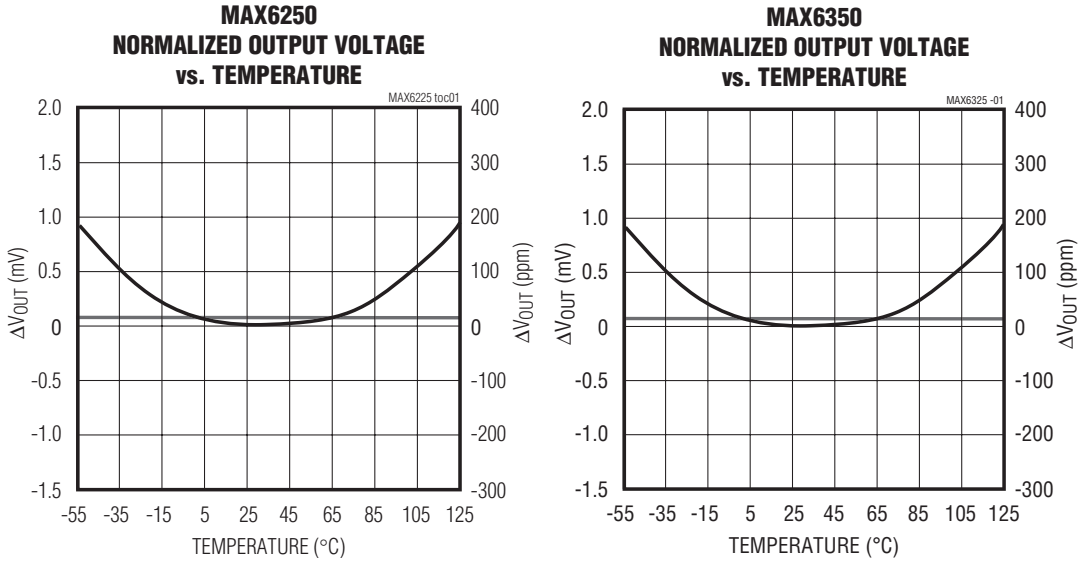


Figure 3.9: Typical temperature related offset changes for MAX6250 and MAX6350 (source = datasheet)

The trim circuitry in figure 3.10 limits the trim range to reduce any drift effects of the external components at the trim pin. The "matched" resistors in the schematic are 10 kΩ Vishay PRA100 types, which share the same ceramic substrate providing optimal thermal matching. The digital controlled potentiometer is a MAX5481 type with 10 kΩ and 1024 resistor taps, which was one of the highest resistor counts available for digital potentiometers. Although these parts have temperature coefficients of 1 ppm/°C and 5 ppm/°C, they only affect the trim input with its worst case range of ±50 mV. Therefore, their coefficients become scaled down to ∼ 0.05 ppm/°C, which hardly affects the references stability.

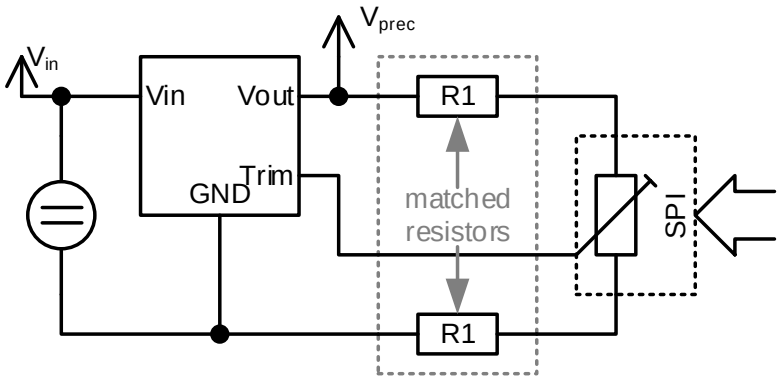


Figure 3.10: Digital in circuit calibration of a reference IC with temperature compensation

For the used MAX6250 reference this results in a reduced worst case trim range of around ±17 mV, with trim steps of approximately ±33 µV. This means that a reference can be calibrated to 5 V within ±17 µV!

3.2.1.6 Error budget

Now that the part selection process is done, a complete error budget can be calculated. Since the system relies on a calibration process, the error budget will focus on the remaining errors after calibration. Although the voltage reference could be calibrated alone, it can also be used to calibrate the HPBS's overall full scale output deviation. This is also the expected use case, as the final version of the HPBS will reside in a housing allowing only access to the analog overall output.

Unfortunately providing a truly representative error budget is difficult as many device parameters are often only specified for a fixed operation range that differs from the target operational range. Furthermore, many parameters are non-linear which precludes simple scaling to the desired range. Especially worst case assumptions therefore often have to use unnecessary larger and unrealistic values, just because no specific values or graphs are given for the region of interest. The detailed error budget calculation in table 3.11 on page 72, therefore tries to explicitly state over which area which values are valid, as this is also strongly depending on the manufacturer and datasheet.

Table 3.10 shows the combined results of the error budget, as well as the expected drift over time. As a result from the very sparsely specified parts, it was not possible to get a realistic worst case estimate over the temperature range (5 °C to 45 °C) but only over an almost twice as large temperature range (0 °C to 70 °C), which is clearly overestimated even for a worst case consideration.

		typ 25°C	typ 5-45°C	WC 25°C	WC, (0..70°C)
Fresh calibrated Reference	[µV]	16	16	16	16
Ref changes from Temp	[µV]	0	90	0	410
Ref changes from DAC codes	[µV]	2	2	14	14
DAC uncertainties	[µV]	38	40	153	184
Deviations from integrator LT1097	[µV]	14	33	79	228
Deviations from integrator LT1050C	[µV]	2	21	21	37
Sum for all with LT1097	**[µV]**	**70**	**181**	**263**	**852**
Sum for all with LT1050	[µV]	59	168	205	661
DAC Step Size	[µV]	76,3	76,3	76,3	76,3
BALI A11 LSB	[µV]	586	586	586	586

Long-term stab [ppm/√kHr]=	20	1Hr	10Hr	24Hr	1Week	1Month	1 Year
Time	[Hr]	1	10	24	168	744	8760
Deviation over Time	[µV]	3	10	15	41	86	296

Table 3.10: Top: Summary of the error budgets results for the HPBS
Bottom: Expected deviations over time for HPBS

However, the error budget for a typical HPBS device could be made just for the really expected temperature range, as more typical curves are given in the datasheet. As measurement results on page 81 and 88 onward will show, the typical values here are still somewhat pessimistic compared to gained measurement results.

	Integrator - LT1097S8		typ, 25°C	WC,0..70°C	WC, 25°C	WC,0..70°C
starting points	Offset drift over Temp	[µV/°C]	-	0,2	-	1,4
	A0 RL = 10k	[V/mV]	128	126	117	110
	CMRR	[dB]	130	128	115	108
	Input Bias Current	[nA]	0,05	0,075	0,35	0,57
	Input Offset Current	[nA]	0,06	0,075	0,35	0,57
	=> Input Current IO+ IB/2	[nA] calc	0,08	0,11	0,53	0,86
	Expected input resistance	[kOhm]	6,2	6,2	6,2	6,2
calc	Offset	[µV]	10	20	60	130
	=> dV from Offset drift	[µV]	0	8	0	56
	=> dV from A0, & CMRR	[µV]	3,6	4,5	16,0	36,6
	=> dV from i_in * Rin	[µV]	0,5	0,7	3,3	5,3
∑	Total Offset, OPAmp	[µV]	14	33	79	228
	Integrator - LTC1050		typ, 25°C	typ -40..85°C	WC, 25°C	WC,-40..85°C
starting points	Offset drift over Temp	[µV/°C]	-	0,01	-	0,05
	A0 RL = 10k	[dB]	160	160	120	120
	CMRR	[dB]	130	110	114	110
	Input Bias Current	[nA]	0,010	0,150	0,075	0,150
	Input Offset Current	[nA]	0,020	0,200	0,125	0,200
	=> Input Current	[nA] calc	0,020	0,250	0,138	0,250
	Input Resistor integrator (estim.)	[kOhm]	10	10	10	10
calc	Offset	[µV]	0,5	1,75	5	11,25
	=> dV from Offset drift	[µV]	0,0	0,4	0,0	2,0
	=> dV from A0, & CMRR	[µV]	1,6	15,9	15,0	20,8
	=> dV from i_in * Rin	[µV]	0,2	2,5	1,4	2,5
∑	Total Offset, OPAmp	[µV]	2	21	21	37
	DAC - LTC2641CS8-16		typ, 25°C	typ 0..70°C	WC, 25°C	WC,0..70°C
starting points	Resolution	[Bits]	16	16	16	16
	=> Step Size	[µV]	76,3	76,3	76,3	76,3
	R,Refin min	[kOhm]	15	15	11	11
	Reference input current max	[mA]	0,3	0,3	0,5	0,5
	Gain Error drift over Temp	[ppm/°C]	0	0	0	0
	Zero Error drift over Temp	[ppm/°C]	0,05	0,05	0,05	0,05
	Maximum INL	[LSB]	0,5	0,5	2	2
	output resistance	[kOhm]	6,2	6,2	6,2	6,2
calc	=> dV from INL	[µV]	38,1	38,1	152,6	152,6
	=> dV from Gain Error drift	[µV]	0	0	0	30
	=> dV from Op Input current	[µV]	0,1	1,6	0,9	1,6
∑	Total Offset, DAC	[µV]	38,3	39,7	153,4	184,1
	Voltage Reference - MAX6250ACSA		typ, 25°C	typ 5..45°C	WC, 25°C	WC, (0..70°C)
starting points	Output voltage	[V]	5	5	5	5
	Temp Coeff. (from Graph for typ. val.)	[ppm/°C]	-	0,4 + 0,05	-	2,05
	Load regulation 0<I<15mA	[ppm/mA]	1,0	1,0	6,0	6,0
	Output Voltage Noise (0.1H-10Hz)	[µVpp]	3,0	3,0	3,0	3,0
	Trimmrange	[±mV]	50,0	50,0	50,0	50,0
	Reduced trimrange	[±mV]	16,7	16,7	16,7	16,7
	Dig trim poti count	[Bit]	1024	1024	1024	1024
	=> Step size	[µV]	32,6	32,6	32,6	32,6
calc	=> Max dev after trimming	[±µV]	16,3	16,3	16,3	16,3
	=> Temp drift	[µV]	0	90	0	410
	=> dev from DAC current changes	[µV]	1,7	1,7	13,6	13,6
∑	Total Offset, Ref. after calibration	[µV]	18	108	30	440

Table 3.11: Detailed Error Budget for HPBS

Furthermore at room temperature even a worst case device should reach the aimed target of 300 µV. For the aimed temperature range of 5 °C to 45 °C most devices should also reach this limit, as indicated by the typical case shown in the error budget. Even those that fall under the wide temperature worst-case estimation, would still provide a higher accuracy than the DUT. However, as the HPBS devices to build are going to pass manual quality checks anyway, a worst case device will be detected and the part responsible for the deviation can therefore be replaced.

3.2.1.7 Detailed setup and simulations of the control loop

Now that the parts to use are defined, the control loop can be designed. As already stated on page 67, the MAX9551 buffer has an internal gain that on purpose increases with the output current. While this is beneficial for capacitive loads, the non-linearly increasing curve complicates control system design.

Setting up non-linear control systems is usually done by use of non-linear control theory using e.g. Lyapunov stability, but this would require detailed knowledge of the internal non-linear functions of the part. As these are not provided by the manufacturer, one can still linearize the system in an appropriate operation point (which is inherently done in Spice AC simulations) and continue with the linearized system, provided that the region around this specific point is stable. To ensure stability, one has to make sure, that movements away from this operation point, which would require a new linearization, are still stable with the designed control loop.

The HPBS's loop therefore has to be designed for a minimum load that needs to be present to provide at a lower limit for the minimal current and hence gain.

Output buffer characteristics vs. load

Figure 3.11 shows the frequency behavior of both the LT1010 and the MAX9551 under various load conditions. These include different load resistors of 0.1 kΩ, 1 kΩ and 10 kΩ and capacitors 0.1 µF, 1 µF, 10 µF and 100 µF. The outcome is further condensed and shown in figure 3.12 that shows the dependency of the buffers -3 dB bandwidth with the loads. This figure very well illustrates the negligible impact of output load currents on the LT1010, versus the MAX9551's high dependency.

As the typical load will be 1 µF this results in a −3 dB cut-off frequency of 23.1 kHz for the LT1010 and 41.6 kHz for the MAX9551, under worst case load.

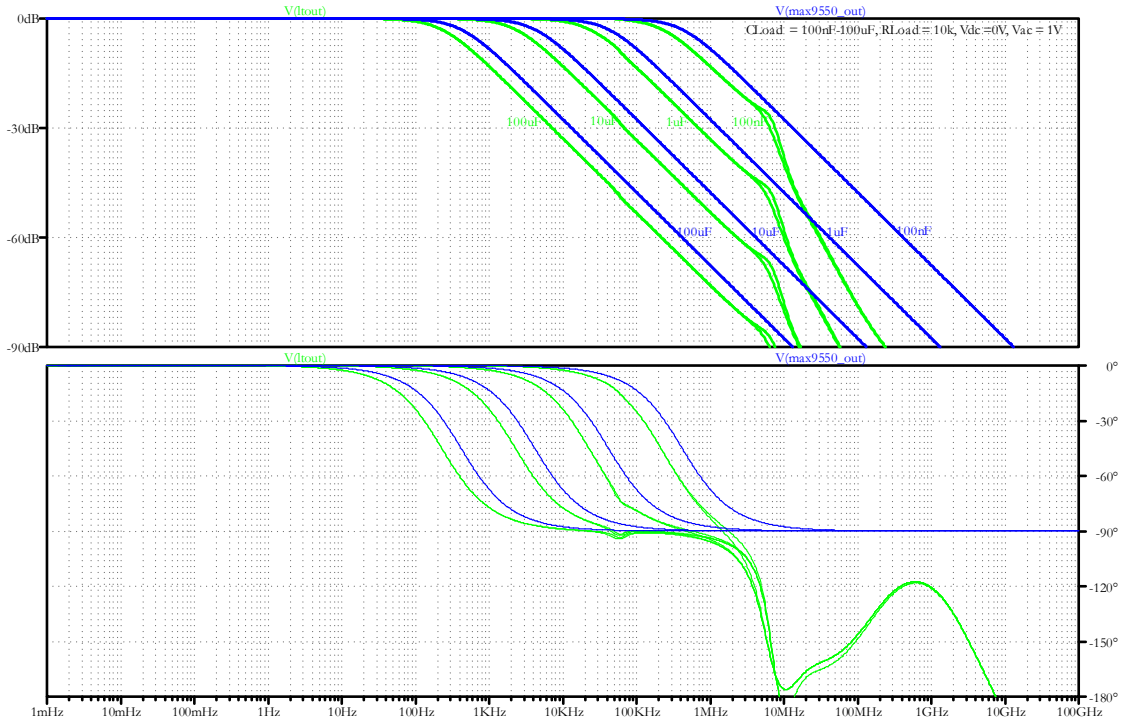


Figure 3.11: LT1010 and MAX9551 vs. frequency with various capacitive loads

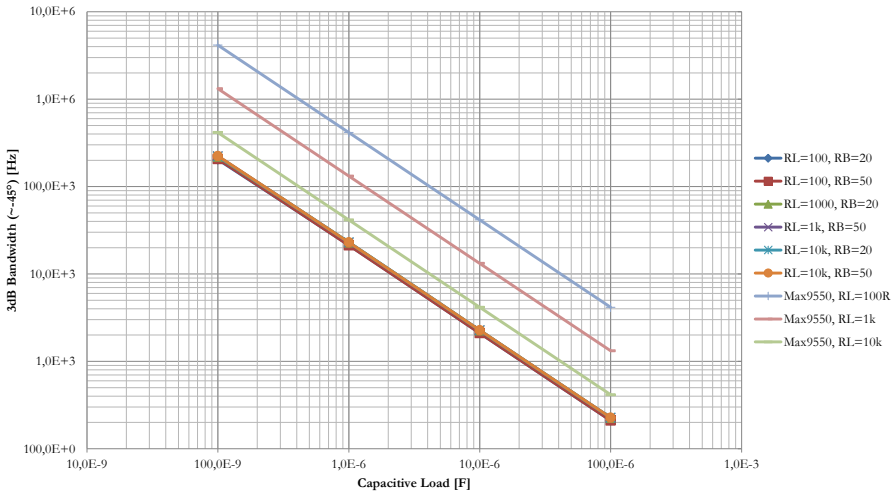


Figure 3.12: HPBS- Driver bandwidth versus load capacitance and load resistance

Integrator design

Based on these bandwidth values the integrator can be designed. The design idea hereby is to set the +3 dB point of the integrator directly onto the -3 dB point of the buffer to achieve approximately $(-90° - 45°) = -135°$ of phase, giving $\approx 45°$ of phase margin at the resulting 0 dB point. In general the +3 dB frequency of an integrator is $f_{+3dB} = 1/2\pi RC\sqrt{2}$ which results in RC combinations in the low $k\Omega \cdot nF$ range for this application.

3.2.1. High precision battery simulator - HPBS

To show impacts of various parameter combinations on the real circuit, parametric simulations for the LTC1050 and the LT1097 can be seen in figure 3.13. Although both OpAmps give similar results, the plot still reveals an interesting detail.

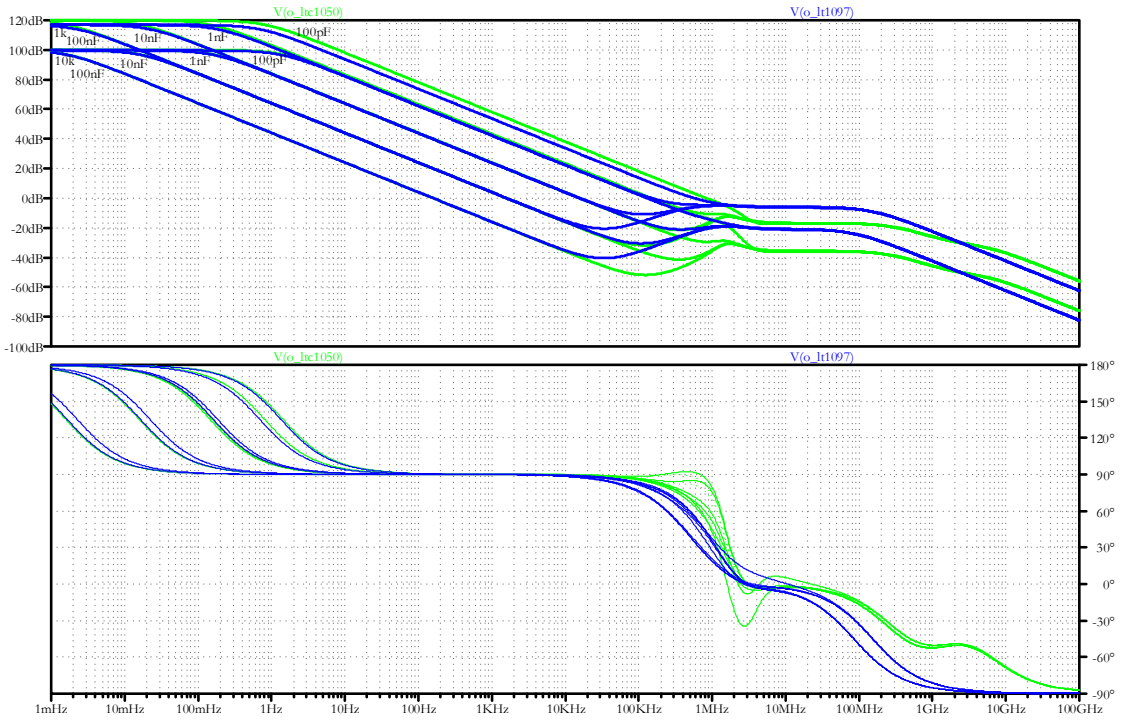


Figure 3.13: Integrator with various RC values; green LTC1050, blue LT1097

In the low frequency range, the circuit built with a 10 kΩ resistor settles at 100 dB, whereas the 1 kΩ settles at 120 dB. This result is due to the limited parallel resistance across the integrators capacitor. Although capacitors themselves can reach parallel resistances in the high GΩ range and above [Roe12], the limiting factor is most likely the PCB, with its non-ideal insulation resistances. Here a value of 1 GΩ was assumed which should be low but realistic for assembled boards soldered with a No-Clean flux[12] [ZAP06]. As a result the value for the integrator resistor should be lower than 10 kΩ to not affect overall DC accuracy. Also the cleanness of the board is an important factor to keep the initial accuracy up over lifetime. This can be further improved by adding protective coating.

Figure 3.14 shows the f_{+3dB} dependency of the integrator capacitor for 1 kΩ and 10 kΩ. With 1 kΩ these would result in 4.9 nF and 2.7 nF for the two amplifiers as a starting point. This was later optimized by simulations of the transient behavior to 4.7 nF for the LT1010 and 1.5 nF for the MAX9551 configuration.

[12] According to [ZAP06; Chr14] PCB surface resistances below 100 MΩ are failures after IPC J-STD-004A. Typical values under test conditions, and temperature are in the low GΩ range

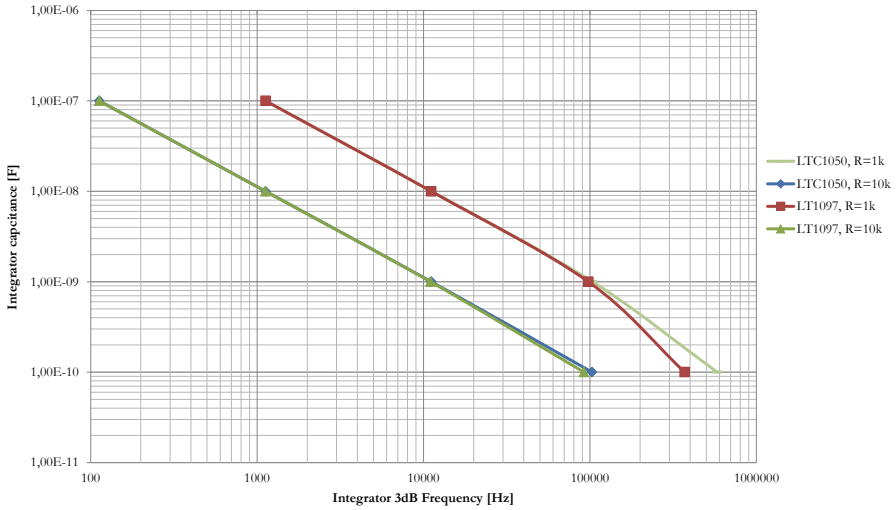


Figure 3.14: Integrator +3 dB frequency vs. integrator capacitor and resistor

Open loop simulations

Figure 3.15 shows the resulting frequency plot for the optimized circuit. As the integrators behave relatively similar, only the LTC1050 version is shown here. As can be seen the final bandwidth of the LT1010 design results in 20.7 kHz and that of the MAX9551 to 52.6 kHz. Both designs feature roughly 40° of phase margin, and should therefore be stable in closed loop configuration.

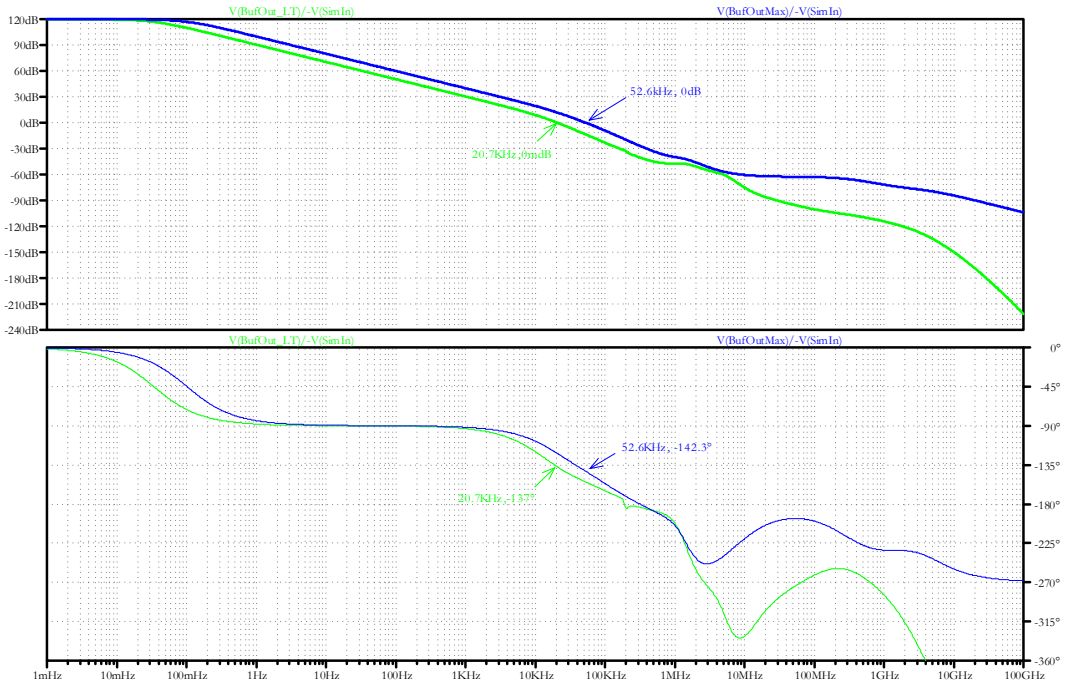


Figure 3.15: HPBS- open loop frequency response, Blue = Integrator + LT1010 buffer; Green = Integrator + MAX9550 with lowest bandwith

Closed loop - transient behavior

The transient response of both circuits under first a 50 µA and then a 50 mA load jump is given in Figure 3.16. As can be seen the time to reach the ±300 µV limit is multitudes shorter with the MAX9551. Furthermore the initial voltage drop at the load-jumps is also magnitudes smaller with the MAX9551.

These results for the MAX9551 are quite exceptional. It only needs around 2 µs at the 50 mA load-jump to recover to within the ±300 µV border.

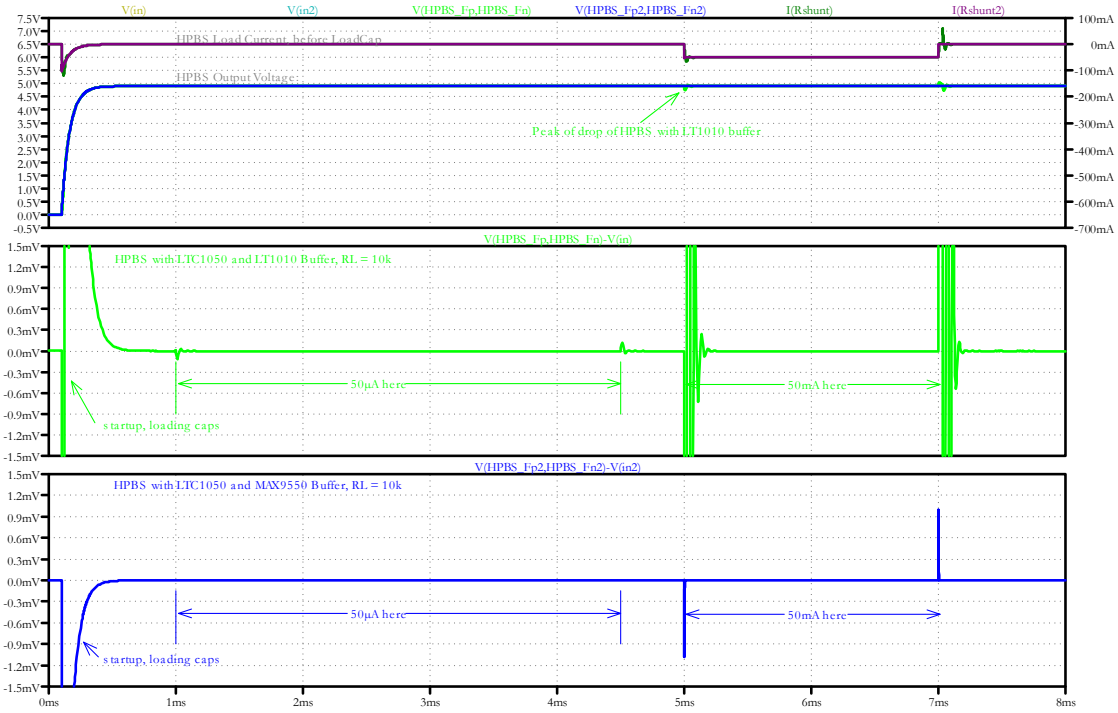


Figure 3.16: HPBS- transient response comparison, Top: Load current and Output voltage LT1010 Buffer, Bot.: MAX9551 Buffer

3.2.1.8 Supply

As a real battery cell is galvanically independent, the HPBS also needs to provide an isolated supply for the parts. Such supplies can easily be realized with fully assembled DCDC modules. Unfortunately, such DCDC converters also introduce noise, ripples and spikes on the output voltage. Sufficient filtering and post regulation is therefore key for high accuracy equipment.

Texas Instruments offers linear regulators that are especially designed for post DCDC converter regulation. These devices of the TPS7A49xx and TPS7A30xx series offer a very high bandwidth, which is needed to reduce the high frequency ripple of DCDC converters. However, highest frequency noise spikes are hard to come by with active components alone. Therefore, a common approach is to

passively filter the DCDC output voltage sufficiently enough so that the resulting lower bandwidth spikes can then be come by with the post regulators.

For this purpose the supply concept, illustrated in a simplified way in figure 3.17, was chosen. Here each DCDC is first separately filtered with a dual stage LC filter that uses ferrite beads and common mode chokes as inductors. Each post regulator is furthermore connected via a low frequency ferrite bead and locally decoupled with capacitors at its inputs.

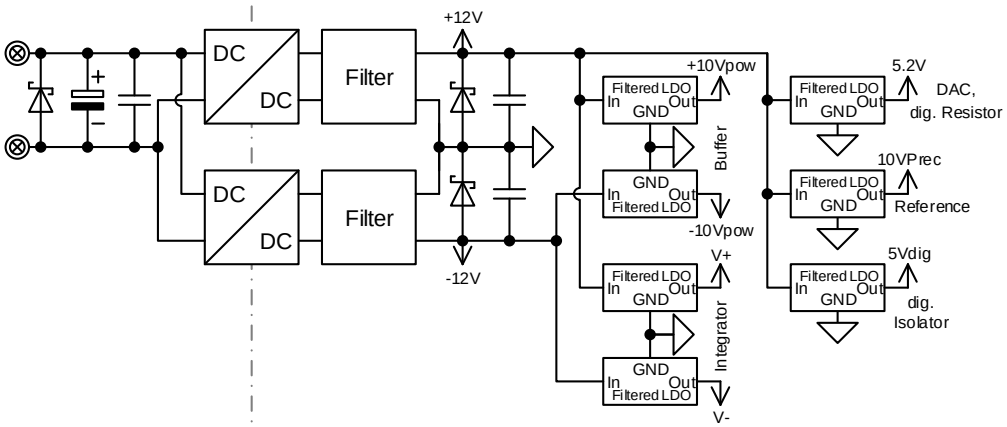


Figure 3.17: Concept of the isolated low noise power supply for the HPBS

To avoid disturbances spreading from non-filtered areas into already clean ones, the PCB layout was designed in such a way, that the supply currents run over dedicated stages that are also regionally separated. Thus the disturbances and noise steadily decreases along this path, before it reaches the core control parts.

As this board was designed to verify concepts, there are separate linear regulators for each part type, to allow independent adjustment of output voltage and provide highest supply voltage decoupling. It is furthermore possible to separately disconnect each regulator and, e.g., use a combined supply for the integrator and the buffer. This also allows to easily do performance tests with various parts of different vendors as well as cost optimizations before a higher number of HPBS cells is to be built.

3.2.1.9 First prototype implementation

Force-sense concept vs. proof of concept

Although all previous calculations and simulations showed very positive results, it was clear that a final HPBS will require a force-sense concept to deliver its full performance all the way to the DUT. Without such a force-sense concept the device would only be usable when it is more or less directly connected at the load point with a lowest ohmic connection possible.

Due to the tight schedule for the main verification board it was urgently necessary to get real world test results for the so far developed concepts, like the recalibration of the reference IC, the usability of self-zeroing OpAmps, etc.. It was therefore decided to build the first prototype of the HPBS without a fully developed force-sense concept. However, this missing part was later added successfully to the first prototype and will be discussed on page 86 onwards.

Intermediate prototype

Figure 3.18 shows the first prototype of the HPBS as it was initially implemented. This prototype was designed to fit both the LT1010 and the MAX9551 as well as the LTC1050 and LT1097. As the combination of the MAX9551 and LTC1050 showed best simulation results, this assembly option was selected for the first HPBS to be assembled and is shown in the image below.

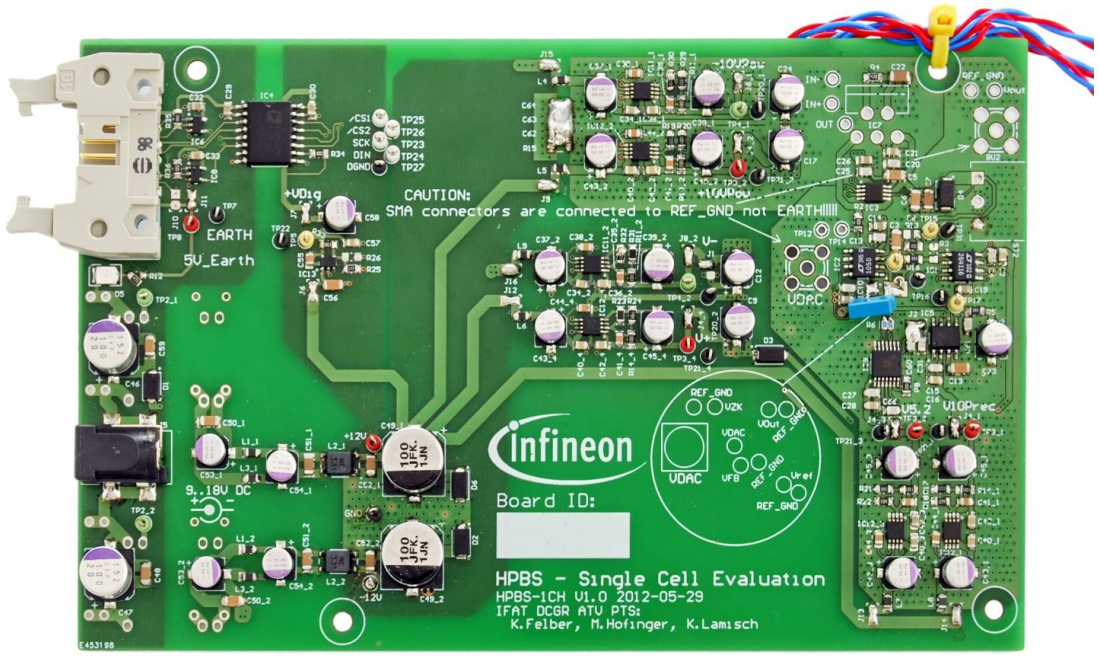


Figure 3.18: High precision battery simulator, first prototype with MAX9551

Partitioning and grounding concept

As the integrator compares the DAC's output voltage to the buffers output, it is necessary to keep groundshifts between those devices as small as possible. The idea was therefore to put these devices as close as possible to the HPBS output so the load current induced ground voltage differences can be kept as low as possible. Furthermore, it was desired to ensure that the load return current was kept out from sensitive areas near the reference or the DAC.

The ground plane was therefore split into different regions that only interconnect near the output to form a starpoint there, as can be seen in figure 3.19. The word star point can be misleading in this case, as it is in fact a star-area near the output connector where all GND planes join on multiple layers with heavy usage of cooper and vias to keep the resistance as low as possible. All ground return paths join there and run back to the supply combined.

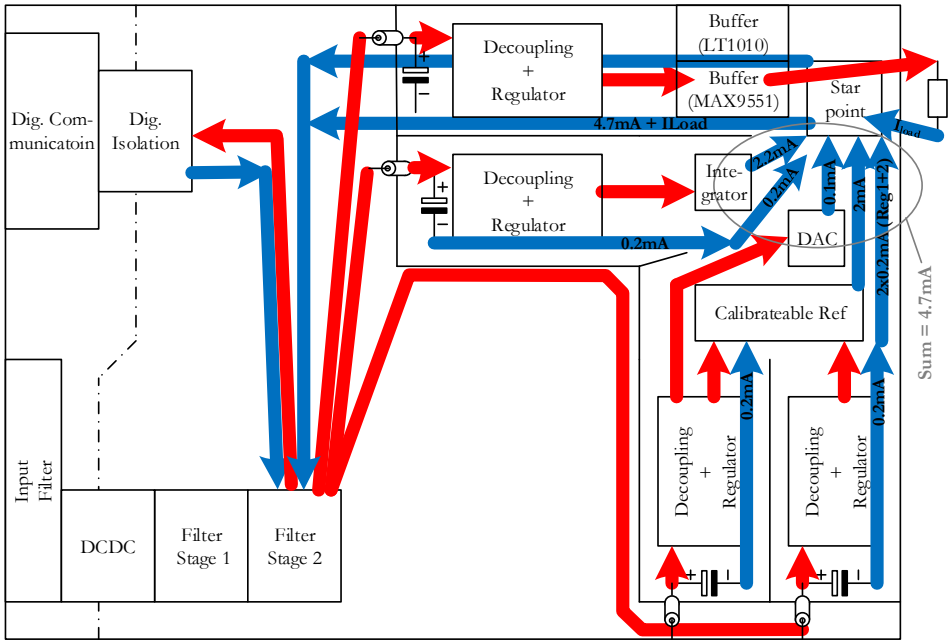


Figure 3.19: Course grounding concept of the HPBS. Supply current values are static worst case values for the whole temperature range

This leads to an interesting effect during fast transient load currents. As all devices now share the same current return path as the output buffer, the whole area near the output is therefore commonly shifted against the ground at the DCDC sources. This in turn leads to an indirect drop of the supply voltage of the according voltage regulators for the control devices. To dampen this effect, serial ferrite beads with a high impedance already in the high kHz range were used together with multiple local capacitors to decouple the linear regulators from the DCDC sources.

Another side effect of this single ground return path is, that the DC return-current of the control devices, like the DAC, or reference, now also has to flow over the star point to get back to the source. But these devices have only very little and mostly static supply current demands of around 4.7 mA even under worst case conditions and temperature range. The area where these currents flow under the critical parts is around 20 mm wide and 30 mm long, which gives only around 0.3 mΩ since the ground plane runs on 3 parallel planes in this area. The resulting offset caused by the control parts should therefore be negligible.

Other layout considerations

To ensure lowest ohmic ground connections throughout the board, ground polygons were used on all layers and stitched together with heavy use of vias. This also helps to equalize temperature and keep thermal gradients across all parts low, which in turn is key to avoid deviations cause by thermoelectric voltages.

This PCB also provided a good opportunity to test practical implementation strategies such as layout replication and SubVersion (SVN) based version control for PCB design before the main verification board had to be built.

It was for example possible to copy the schematic and PCB layout of the voltage regulators and to later use it again as building blocks for the main verification board. This can be seen in the right half of image of HPBS (figure 3.18). These are the decoupled regulators as illustrated in the boards grounding concept in figure 3.19. This blocks and parts of the filter gave a perfect opportunity to test the layout replication capabilities of the PCB tool, which was highly needed for the main verification board.

3.2.1.10 First test results

For the first tests of the HPBS the DCDC modules were left unassembled and an external low noise power supply was used. This was left open as last step, so that each section could be investigated independently.

A HP/Agilent 3458A 8 1/2 digit high precision multimeter was used for the calibration of the device. Both, the multimeter and the HPBS were turned on and then left running for several minutes, to ensure thermal equilibrium before starting the calibration procedure. The control of the HPBS was realized with an Aadvark USB-to-SPI interface controller and a tiny LabVIEW™ application specially written for this task.

Load current tests, without force-sense

It was clear that each mΩ of wire resistance would directly influence the performance as this version did not yet include the force-sense concept. Therefore, the load was connected via the shortest possible way to the HPBS, resulting in less than 3 cm wire length. The left curves in figure 3.20 represents the measurement results at the point of the load, whereas in the right picture directly at the PCB's output connector.

Even with this smallest possible wire length the deviation is almost in the range of an LSB of the TLE8000QK. However, the measurement results directly on the PCB's output connector show that the HPBS itself is extremely accurate and that the deviations truly only occur due to the wire resistance. This once again makes the need for a force-sense concept obvious, as otherwise the device would only be

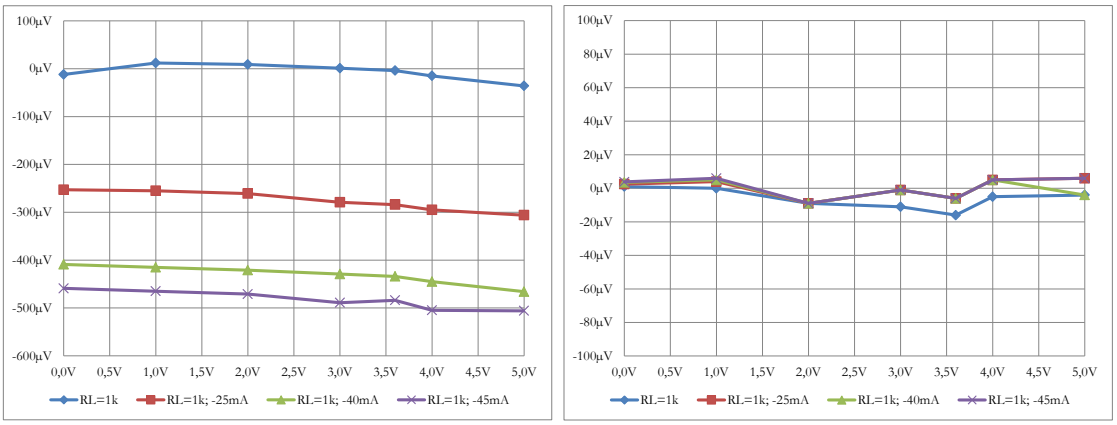


Figure 3.20: HPBS LTC1050 without force-sense vs. various loads. Left: Measured at load, Right: Measured directly at PCB

usable for low current loads with thick and short connection wires. Luckily, as page 86 will show, the final force-sense concept only required minimal changes to this first demonstrator.

Test over the temperature range

One of the next very important tests was the behavior over the temperature range of the HPBS and especially the reference IC with the external trimming. For this reason a THERMONICS T-2500 temperature forcing system was used to provide a well-controlled environment. The tests shown in figure 3.21 were run at 5 °C, 15 °C, 20 °C, 25 °C, 30 °C and 50 °C air temperature. The actual recorded temperature was sensed by monitoring the PCB ground plane near the voltage reference.

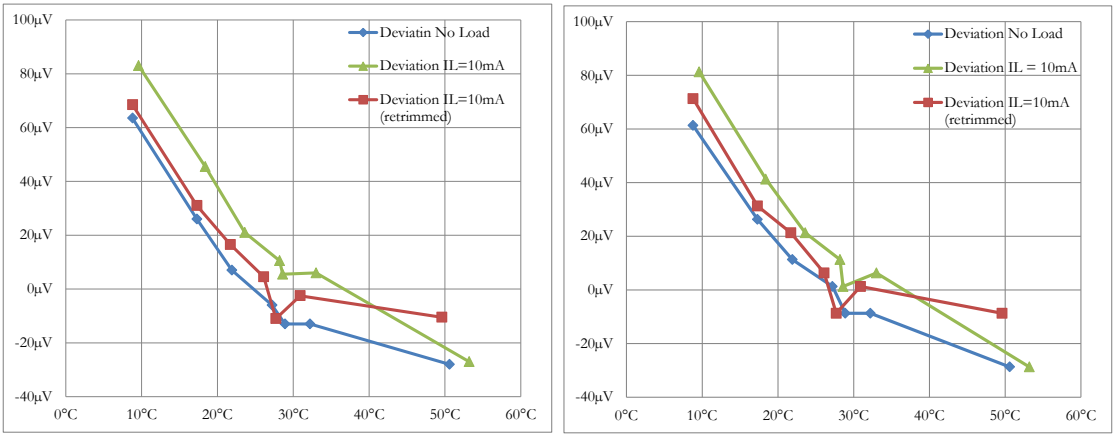


Figure 3.21: HPBS accuracy deviations over Temperature, Left: Vref(T), Right: VOut(T) with LTC1050

As can be seen both the HPBS output and the reference voltage show nearly identical results. The reference is therefore the main factor in the thermal stability

of the HPBS, just as predicted by the error budget. The reason for the sharp edge near 25 °C may come from, e.g., thermal hysteresis effects, as these two values were conducted at the start and at the middle of the measurement sequence but both at 25 °C.

Considering worst extrema the temperature related drift sums up to ∼110 µV. Although this is slightly higher than what was expected for a typical voltage reference IC alone in the error budget on page 71, it is also better than what was expected for the overall HPBS. This measurements result in a total temperature drift of just 0.55 ppm/°C over the intended operating temperature range!

However, it has to be noted that extreme temperature gradients, for example applied with freezing spray on one side of the PCB, can temporarily cause serious shifts up into the low mV range. Therefore, shielding with a metal housing should be anticipated to prevent extreme temperature gradients from hitting sensitive parts. Also sufficient heating up times have to be observed to allow initial temperature gradients to settle.

LTC1050 switching noise

After the previous static measurements the dynamic tests were started. These tests revealed the true amount of switching noise residue of the LTC1050, as can be seen in figure 3.22.

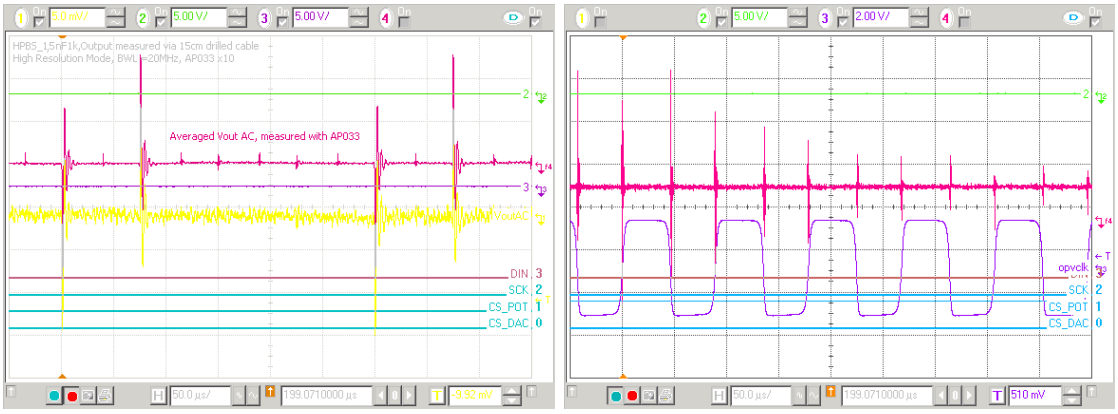


Figure 3.22: LTC1050 switching disturbances directly at the IC. Left: Disturbances on the output ≈ 20 mVpp, Right: OpAmp clock pin vs. disturbance

Although the average voltage seems to be stable, the peak to peak disturbance still reaches unacceptable values in the 20 mVpp range. The right measurement graph shows that these peaks directly correlate with the clock frequency of the LTC1050, which was therefore considered as the rootcause for these disturbances.

DCDC noise and noise reduction

Finally the DCDC modules were connected to retrieve results on their induced disturbances. Figure 3.23 compares the HPBS's DCDC noise directly at the converters output to that behind all filter stages at the high bandwidth regulators output.

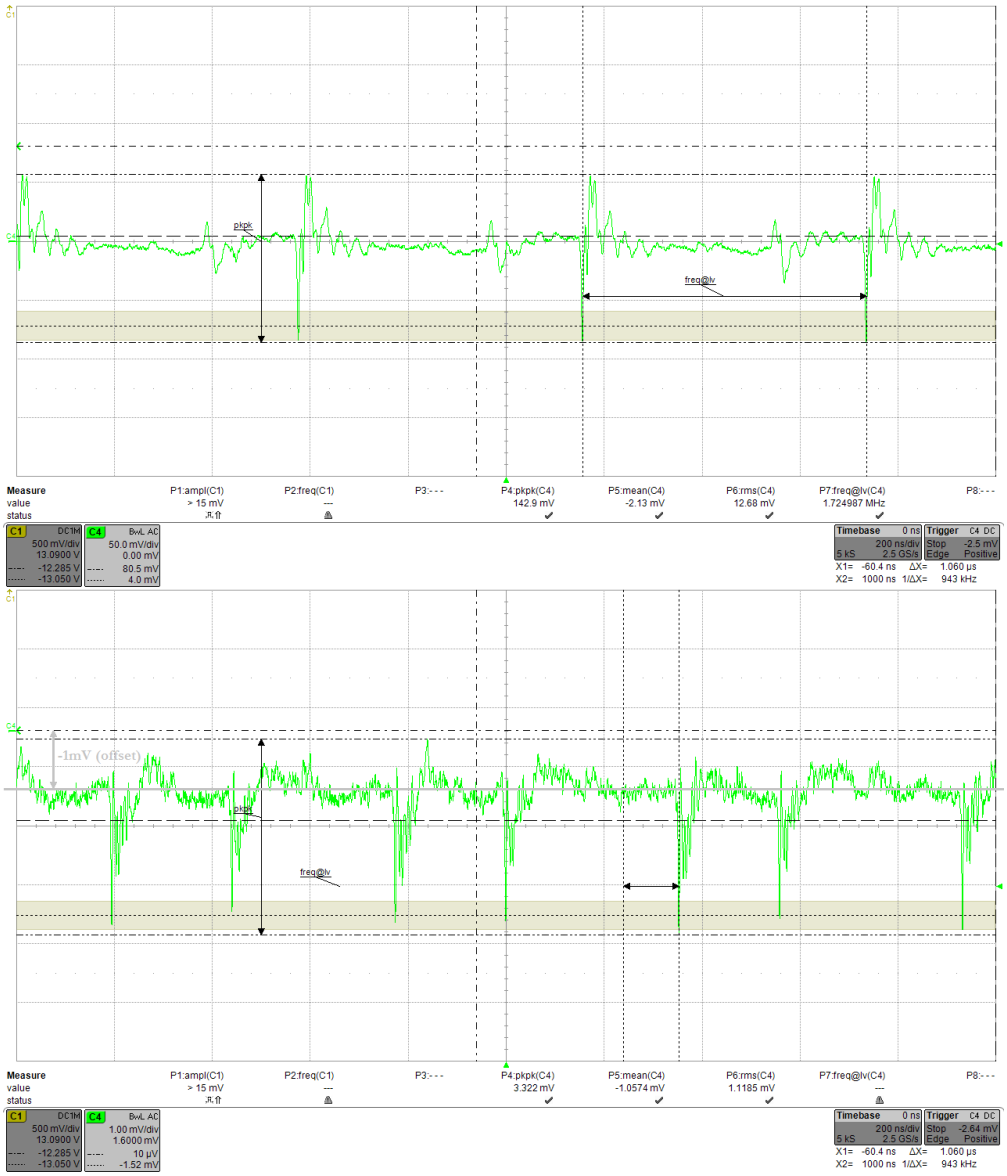


Figure 3.23: HPBS DCDC disturbances comparison.
Top: at the DCDC converter output ≈140 mVpp;
Bottom: passed the filters and the filtered regulators ≈3 mVpp

As can be seen the initial 142 mVpp were reduced down to roughly 3 mVpp. Although this is a reduction by almost 50 times, it is still a significant remaining ripple. The biggest portion of this ripple voltage is due to very high frequency

spikes with a repetition rate of 1.7 MHz. It can be expected that the ADC's input filter with roughly 48 kHz pass-bandwidth should be able to further reduce the ripples to acceptable levels. As the figure shows, the difference in the average and the RMS value of the DCDC related noise is around 100 µV. The HPBS is normally calibrated with a true RMS precision multimeter like the HP/Agilent 3458A. The difference measured with the TLE8000QK's PADC, which measures averaged filtered voltage, should therefore also be in the 100 µV range. However, since the implemented DCDC filtering is not yet fully optimized, there is still room left for further improvement.

Intermediate outcomes and implications for the further development steps

Even though the timing constraints prohibited further extensive tests, already some valuable implications for the design of the verification board and the next steps of the HPBS could be retrieved.

First of all, despite the extreme DC performance of the LTC1050, there is still a significant switching related distortion on the output. As this was not mentioned in the LTC1050 datasheet it can be expected that this behavior may be found with other self-zeroing OpAmps as well. Such types should therefore only be used with sufficient filtering and/or in cases where such disturbances are not expected to cause errors. They may still be used, for example, in front of integrating ADCs, as these types only count the average voltage of the OpAmps, which still has an exceptional performance.

Secondly reaching accuracies below 1 mV on custom PCBs is achievable, provided sufficient care is taken throughout the whole design process. And as figure 3.20 perfectly illustrates, these accuracies can be achieved even without a force-sense concept as long as the load currents and the wiring resistances are sufficiently low. This means that for pure sensing and measurement tasks the current concepts should be sufficient, whereas for forcing tasks a dedicated force-sense concept is highly recommended.

Finally the overall concept of the HPBS works satisfyingly. This means that no greater pitfalls were overseen in the design process and all selected components work together as anticipated. This can be best seen in figure 3.21, as there are hardly any differences between the deviation of the reference and that of the overall system, which implies that hardly any additional error sources were introduced. Therefore, the parts and the design methodology of this concept are suitable for the main verification board as well.

3.2.2 Upgrades to the first HPBS prototype

With the previous mentioned results the implementation of the main verification board was started. The following upgrades were therefore applied after the main verification board's implementation was finished.

Force-sense implementation

One of the first steps in the upgrade was the implementation of the already mentioned force-sense concept.

Single side force-sense: As most analog circuits like subtractors rely on external passive components, which are not available with sufficient precision, different concepts had to be looked at. Figure 3.24 shows a very simple modification to the original concept that allows to sense the positive output voltage directly at the load.

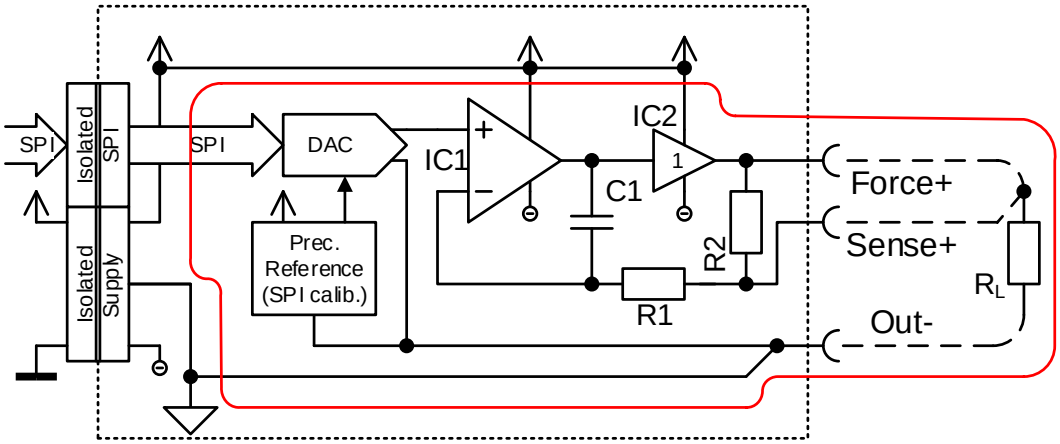


Figure 3.24: Force-sense concept for the +Output

The idea is to split the feedback resistor into two parts. Both together still connect to the output buffer on the HPBS's PCB. The point between those two resistors is used as a sense contact for the load. If this sense pin is connected to the load, the internal resistor is being shorted, forcing the control loop to regulate to the loads positive terminal.

On the one hand, resistor R_2 has to be in a range that is sufficiently greater than the expected wire resistance, to avoid supply currents running over its wires. On the other, the resistor R_2 has to be small enough, so that the feedback loop is not altered to strongly between using and not using the sense line.

A positive side effect of using the resistor R_2 instead of leaving it out completely is, that voltage ripples on the sense line due to wire inductances are being damped,

improving overall stability even with wires applied. Simulations revealed that the initial short time voltage drop slightly increases to ≈5 mV, due to the simulated wires (100 mΩ and 50 nH) but the overall drop between the positive side of the load and the PCBs GND quickly returned to ≈23 µV. Of course the static drop over the Out⁻ wire still depends on its resistance and the current load current.

Double force-sense: Applying a force-sense concept for the Out⁻ line requires somewhat more effort, due to the lack of usable arithmetic analog circuitry.

The easiest remaining concept uses the push/pull capability of the output driver. Therefore, the same force-sense circuit can be used again for the negative path as can be seen in figure 3.25.

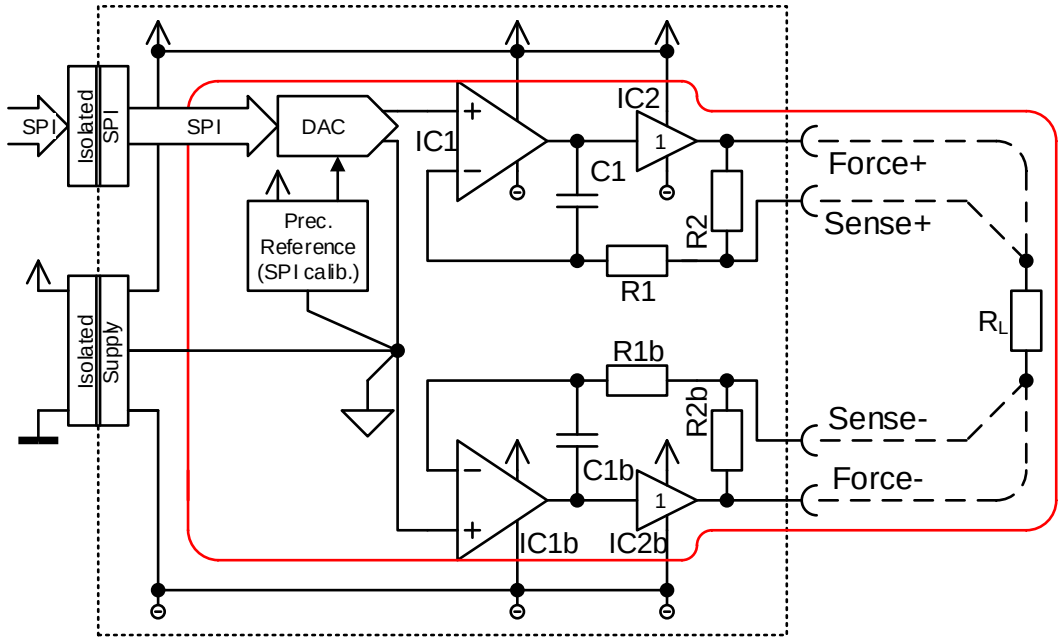


Figure 3.25: Force-sense concept for the + and -Output

This allows to directly sense the DAC's GND potential and create a matching virtual-ground return point for the load. The cost for this increased precision is additional power consumption, as now also a second buffer IC is needed. Furthermore, as two regulating systems are now working on the same load it increases the chance for system instabilities.

For this reason, additional simulations were conducted, again assuming around 100 mΩ of series resistance and 50 nH inductance per wire. As can be seen in figure 3.26 the initial voltage drop now increases to around 18 mV but returns to a static offset of ≈ 45 µV after only around 20 µs.

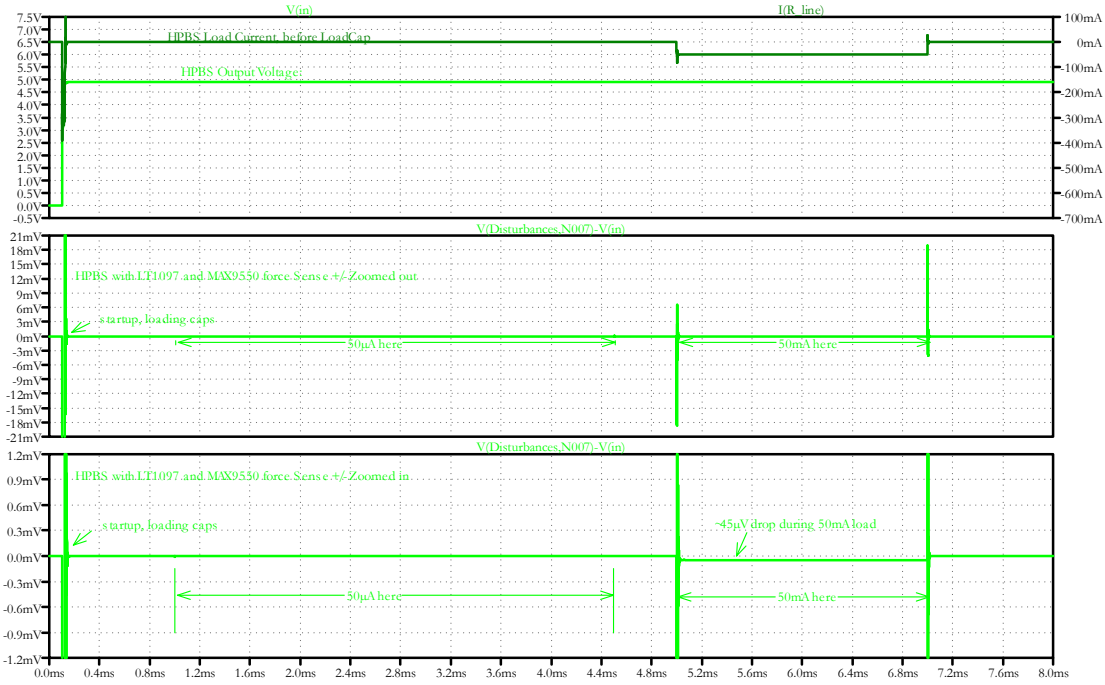


Figure 3.26: Transient simulation results for double force-sense

3.2.2.1 Measurements results of the upgraded prototype

Based on these promising simulation results the HPBS prototype was upgraded in several steps. After integration of R_2 and first positive results with the single force-sense concept, the LTC1050 was replaced by the LT1097 to eliminate the LTC's switching disturbances. As the LT1097 has a higher noise floor, the output capacitance was further increased to 2 µF, which lowered the noise level and hardly changed the load jump behavior or stability.

At this point several measurements were conducted to compare the behavior with and without the sense feedback. Then an add-on PCB with an additional LT1097 in integrator configuration was attached to the second buffer inside the MAX9551. This integrator was then connected to sense the DAC's ground potential, as depicted in the concept-figure 3.25. Of course, this retrofitting is far from an optimal layout, but the basic principle should be observable, although with expected less dynamic performance than for example, in the single force-sense version, that has a near optimal layout.

For the various following tests, standard HIRSCHMANN MKL 0,64/25 series cables where used. These have a length of around 25 cm each, fit standard 0,64 pins in a 2.54 mm grid, and a cross section of 0.25 mm^2. These cables were used on both sides of the load.

Testing against static loads

Single Force-Sense: Figure 3.27 shows the static behavior of the HPBS in the configuration with the single force-sense concept and the 25 cm cables.

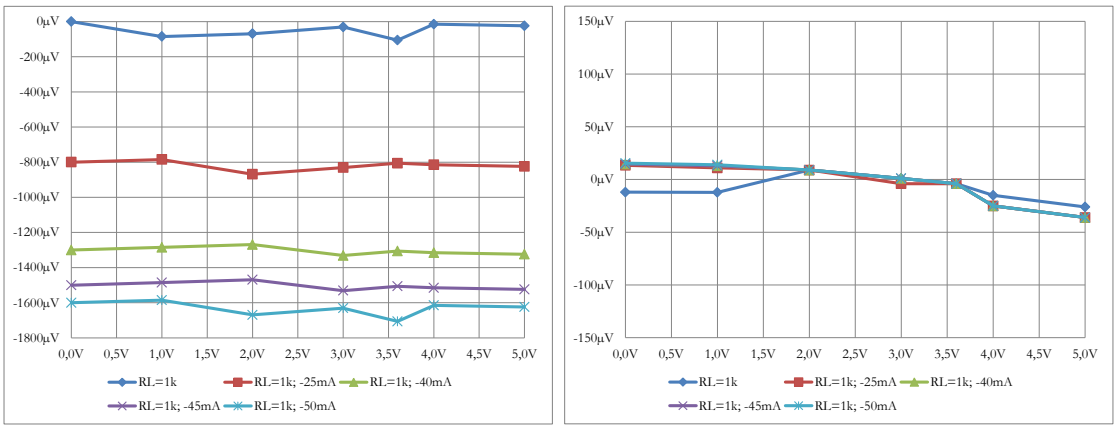


Figure 3.27: HPBS with LT1097, single force-sense applied to the positive pin of load only, with 25 cm of cable on both sides. Left: Differential changes at the load; Right: Changes vs. HPBS ground

As can be seen on the right side of the graph, the deviations between the positive side of the load and the GND plane of the HPBS are in the range of around ±30 µV. Of course, this degenerates quickly as soon as the voltage drops on the Out^- Out^+ line are taken into consideration as well. However, considering the fact that this line is very thin and completely uncompensated, this can easily be improved by usage of heavier wire and elimination of the plug contacts on the HPBS side, where direct soldering may be a better option.

The single force-sense concept might therefore already be useable, provided that realistic load current are around half the HPBS maximum load capability of 50 mA and better wiring is used at least for the GND side, which should be feasible.

Double Force-Sense: If these conditions cannot be met, the double force-sense concept has to be used, as it provides far better static performance as can be seen in figure 3.28.

Although the negative sense integrator was just added onto the HPBS with an add-on PCB, these static results are extremely good. Even though in total 50 cm of wiring with standard non-precision contacts were used, the total maximum deviation is still less than 100 µV, compared to the initial calibration.

However, it has to be noted that, due to the use of both output drivers in a single package, twice as much power is dissipated. Therefore, the 50 mA output current, plus the current from the 1 kΩ static load can only be provided for roughly one minute, before the over-temperature-shutdown turns off the MAX9551. The

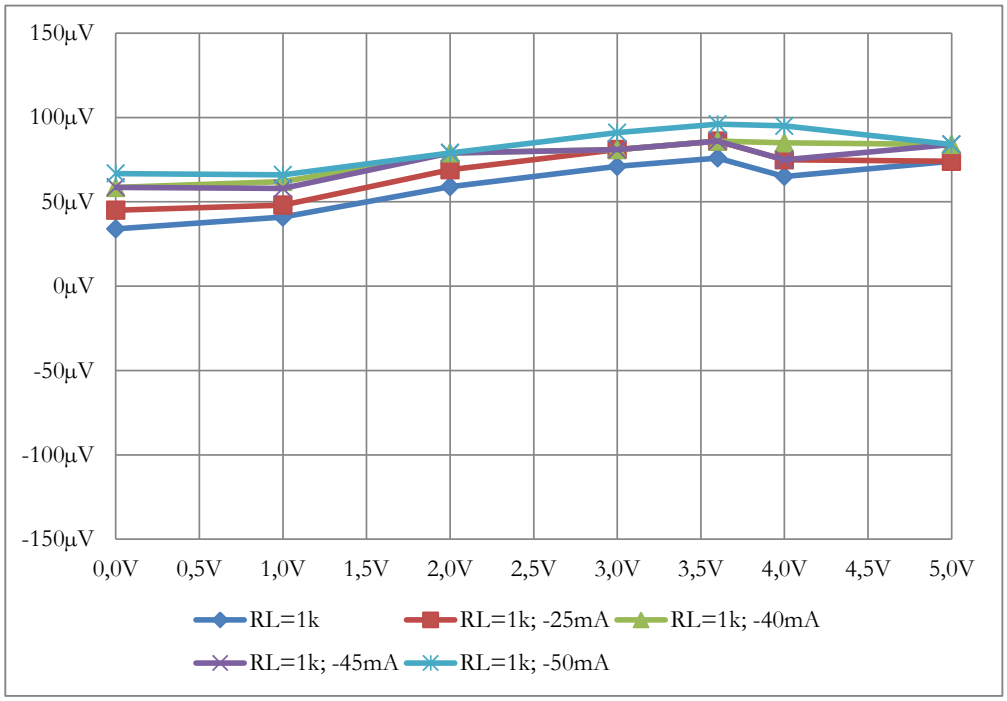


Figure 3.28: HPBS with LT1097, double force-sense applied at load with 25 cm of cable on each side

maximum static load current observed in the double force-sense configuration that did not turn off the MAX9551 was 45 mA.

Testing against dynamic loads

For the dynamic test, a resistive load of around 110 Ω was periodically connected to the HPBS via a BS170 MOSFET transistor and a 1 kΩ was connected statically. As the tests were conducted at 5 V this results in a load jump of roughly 5 mA to 50 mA.

Load steps and noise: Figure 3.29 compares the load jumps results versus the different force-sense configurations. As can be seen on the right side of all figures, the noise of the HPBS output increases with increased output load and is around ±750 µVpp at its maximum. This noise is statistically independent and can be reduced with proper filtering and averaging on the oscilloscope. The result of this filtering is shown on the left side in the function f1 trace.

All measurements were conducted with AC coupling and therefore only show the changes due to the loadjump, not the total offset. Please also notice the different scaling of the vertical axis throughout the graphs.

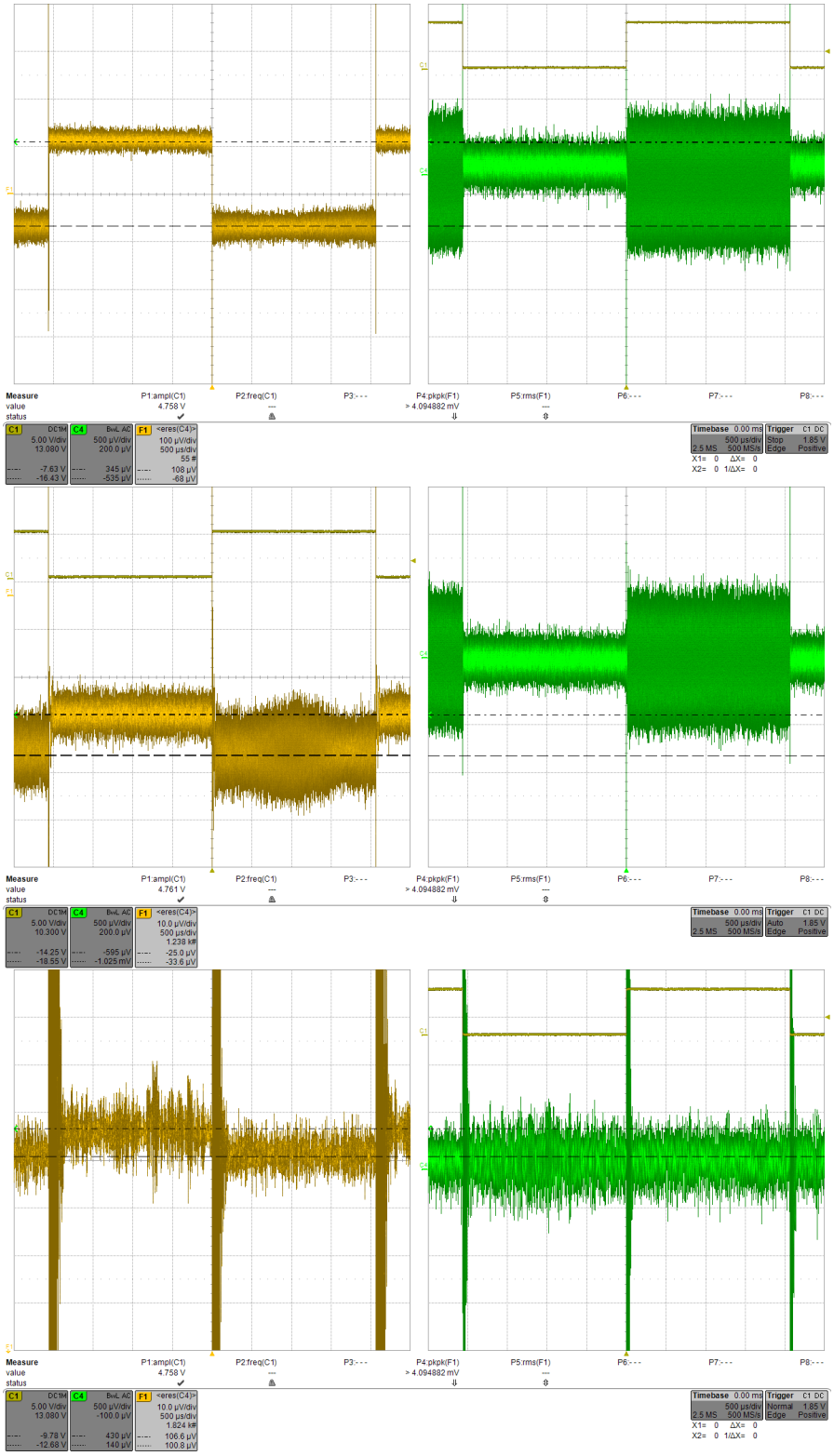


Figure 3.29: HPBS comparison of dynamic load behavior.
Top: No force-sense, measured vs. HPBS-GND, short cables;
Middle: Single force-sense, measured vs. HPBS-GND, 25 cm cables;
Bottom: Double force-sense, measured across load, 25 cm cables
Attention, mind the different scaling factors!

The topmost graph shows the result of the HPBS without the force-sense concept applied, but with the minimum wires. Even with very short and thick wires this gives around 200 µV of offset.

The graph in the middle represents the single force-sense concept. Here the 25 cm cables were used on both sides. As the lower side offset strongly depends on the actual cable length used, the measurement was conducted only between the topside of the load and the GND of the HPBS, to better reveal the capabilities of the Out^+ force-sense. The offset on the Out^- side, can be added as determined by the static measurements, under consideration of the actual desired cable length. But as can be seen, there are hardly any dynamic changes, besides the offset, compared to the version without force-sense. Please note that the vertical scaling of the filtered and averaged function f4 in this graph was increased by a factor of 10!

The bottommost graph finally shows the version with the add-on PCB for the double force-sense. Here the voltages are differentially measured directly across the load. Interestingly, the output noise behavior changes and doesn't increase with the load current any more, now that two buffers work against the same load. It can also be seen that the dynamic performance is by far not as fast as with the previous configurations. As the dynamic performance is also less than expected by the simulations, it may at least partly be a result of the usage of an add-on PCB compared to the optimized layout for the previous tests. But even with this rough setup and the force-sense applied over real cables, the system remains stable.

Load step settling time: Figure 3.30 compares the settling time of the single force-sense versus that of the double force-sense concept in case of a load jump.

The single force-sense is very dynamic and manages it to settle to within ±300 µV in approximately 1 µs. The initial voltage drop during this short time period is just about 6 mV. These values match up very well with what was expected based on the simulations.

The double force-sense on the other hand shows a small dampened oscillation with a maximum of ±17 mV. It needs around 70 µs to settle within the ±300 µV borders. Here much better results were expected from the simulation than were revealed in the real world results.

Although this is not as good as anticipated, the error on the TLE8000QK's ADC conversion should still be negligible as the average of the oscillation should almost cancel out. Even for a worst case assumption of a one-sided triangle waveform the resulting drop would be negligible, as can be seen by the following calculation.

$$U_{drop,WC} = \frac{17\,\text{mV} \cdot 70\,\text{µs}}{2 \cdot 3600\,\text{µs}} = 165\,\text{µV}$$

Anyhow, it may be expected that at least a part of this oscillation behavior may

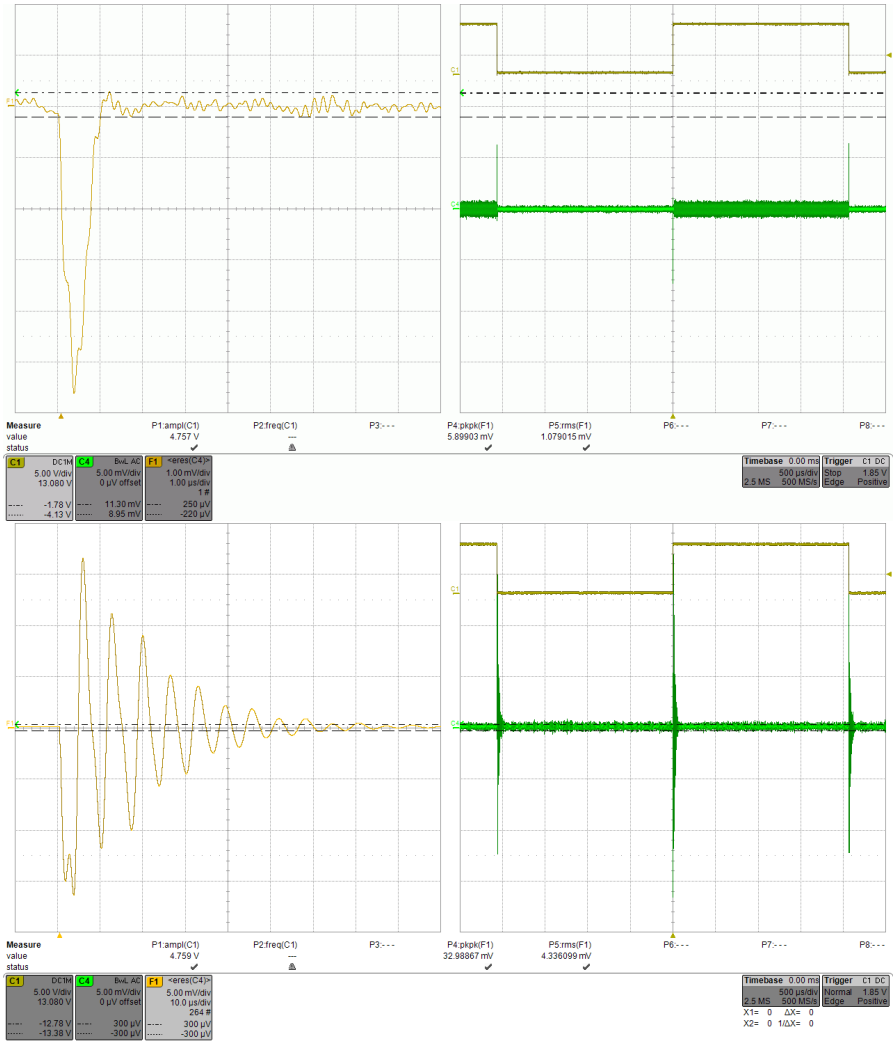


Figure 3.30: HPBS load jump settling time.
Top: Single force-sense, measured vs. HPBS-GND, 25 cm cables;
Bottom: Double force-sense, measured across load, 25 cm cables
Attention, please mind the different scaling factors!

be further improvable with a board initially designed for double force-sense, that doesn't require any add-on PCBs.

3.2.2.2 Summary and outlook for the HPBS

During the development phase of the HPBS many devices and techniques needed for accuracy PCB design could be tested. One of the core parts is a reference with digital re-calibration, that in total showed a temperature drift of only 110 µV from 5 °C to 45 °C, or in other words 0.55 ppm/°C.

A single force-sense technique was implemented on the first prototype, that allows

extremely fast load regulation for the positive load side, even with 25 cm cables applied. The remaining offset in this configuration mainly depends on the negative return path resistance and the load current. This system is therefore very interesting for every application that needs a high speed and high accuracy load driver located on the same ground plane as the load.

Also a double force-sense technique was added to the prototype. This allows to compensate static voltage drops on the cables to the load to under 100 µV. Even though the dynamic performance is not as fast as with the single force-sense implementation, it still manages to settle a remotely connected dynamic load to within ±300 µV in around 60 µs. As this double force-sense concept is not yet optimized, neither in the PCB nor the control loop design, further improvements can be expected.

Finally, the created HPBS features a greatly improved accuracy and requires decreased calibration intervals compared to the original simulator. It can be used as a single high precision battery simulating cell, or even in combination with multiple HPBS cells or other battery simulators, due to its galvanic insulation.

3.3 Main verification board

The development of the main verification board was the most important and intense part during the project phase of this thesis. It had to provide the main interface to the DUT and simulate all necessary environmental behavior to allow proper verification of the IC's functions.

Due to the high number of different circuitry needed, and the tight time frame given, this development was conducted as a team process. The core development team consisted of 2 people (Karl Felber and the author) during concept phase. During schematic entry and PCB-layout implementation at times up to 3 additional co-workers were assisting in entering and especially layouting the circuits in parallel. The work therefore not only included technical aspects, but also many organizational tasks to synchronize the whole development team.

The outcome is a verification board (images are on page 151, figure 3.72) with a shape slightly bigger than a sheet of A3 format paper, housing around 2700 components described on 55 disparate schematic sheets, which are often used in multiple instances, and conclude into around 105 total pages of schematics.

The design process for the circuitry on this board was similar to that of the HPBS. It also followed the steps: idea, concept, literature research, basic calculations, part search, further calculations, detailed manual schematics, schematic PC entry, coarse layout concept, coarse part arrangement in the PCB-layout, refining the layout concept, and final layout. Often multiple loops had to be run in this design process, as problems arose due to, e.g., lacking accuracy of needed parts.

Throughout the board development process, many design ideas already discussed in the previous section (3.2.1), were re-used to allow for highest accuracy. Because of this repetition and the huge amount of different circuitry developed, only some circuits of the verification board will be described in detail. However, the concepts and results will be presented for most circuits.

3.3.1 Basic concept and overview

Before the concepts of the various parts are being discussed, a short and narrow overview of the whole verification board will be given here as a starting point. An illustration of this concepts can be seen in figure 3.31, which will be later broken down into more detailed concept blocks.

As can be seen, there are two main parts that interconnect via various circuitry. The one part is the DUT itself, whereas the other is an FPGA module that contains specially programmed logic to interface with the DUT and the verification board.

It can also be seen that the DUT is placed onto a dedicated PCB with only a minimum amount of external circuity. This area represents either a special DUT-

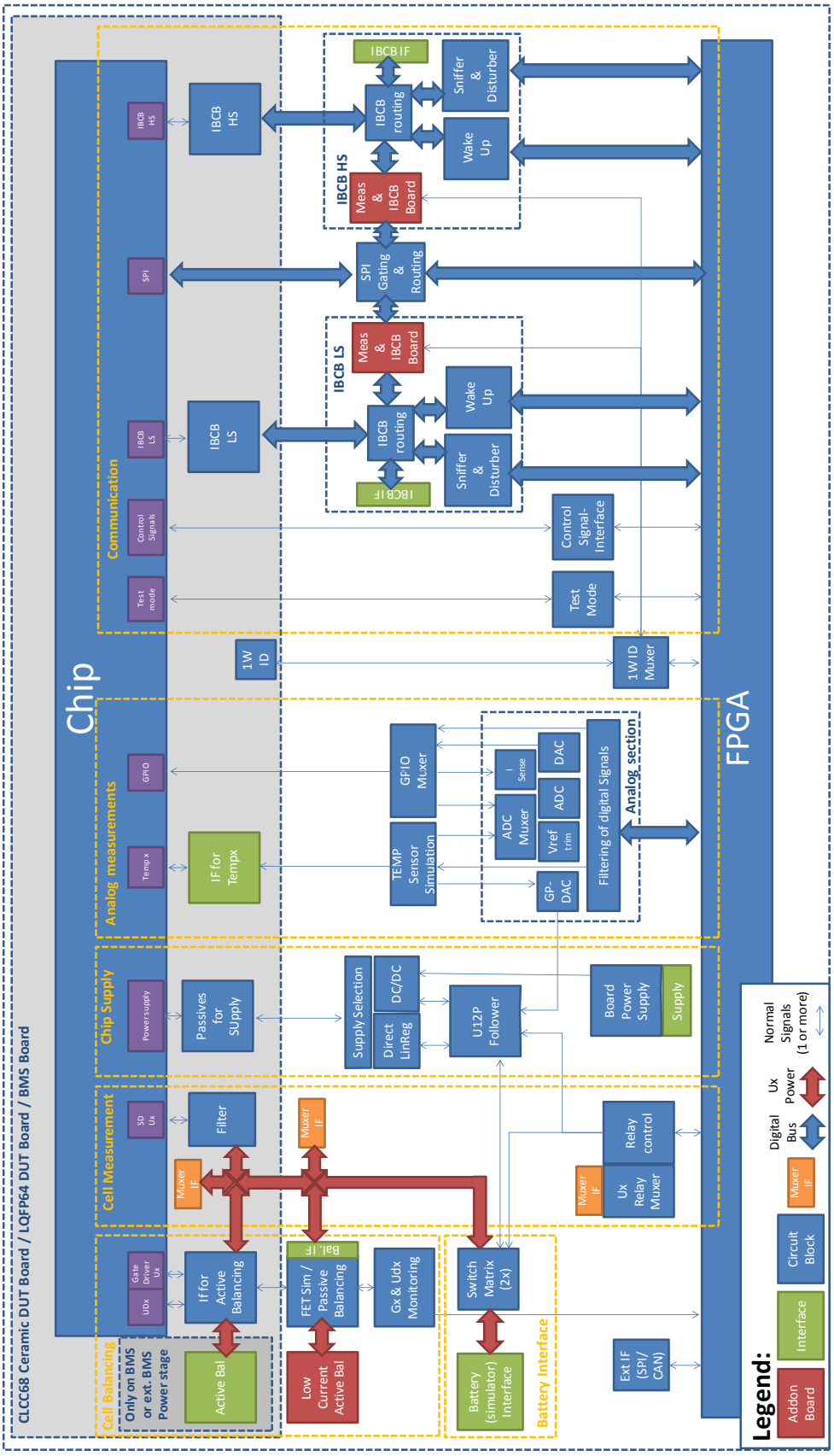


Figure 3.31: Simplified concept graph of the verification board. Be aware that some parts and many connections are omitted to gain simplicity

board or a battery management system board (BMS), that can be mounted directly onto the verification baseboard. The baseboard is the main board that contains all the circuitry and interfaces, to give the FPGA full control over the DUT's environment.

The circuitry on the baseboard can be grouped in the following blocks that will be described in the next section:

- Communication with one or multiple DUTs:
  This block contains circuitry, to allow all the different communication modes the DUT provides. It also provides slave devices to communicate with, communication routing, logging, sniffing, disturbing possibilities, and more functions needed to verify the correct behavior of the communication interfaces.

- Active and Passive Balancing:
  The verification board allows multiple ways to do Active or Passive Balancing. These range from configurable low current on-board modes of balancing, to high current off-board possibilities in conjunction with a BMS 7.0 power stage. Furthermore, there is direct feedback of balancing diagnosis lines into the FPGA to allow for advanced diagnosis.

- Battery simulation and interfacing:
  The center of this block is a relay multiplexer, which allows independent connections to battery cells as well as providing short or open loop conditions. The battery cells can also either be simulated on-board or off-board, or even be external Li-Ion batteries.

- Battery measurement:
  As cell voltage measurement is one of the key features of the TLE8000QK, the board is designed in such a way that accuracy measurements are possible throughout the board and its add-ons. To ensure this accuracy, every important piece of equipment is fitted with dedicated measurement interfaces, to allow for cross checks. Also various partition and layout concepts were used to ensure highest accuracy.

- Various modes of chip power supply:
  The baseboard is able to provide all supported modes of power supply for the DUT in a fully remote controllable way. This further includes power routing, and decoupling to unload the battery simulators from the chip's supply current, to support accuracy measurements.

- Analog board functions:
  There are many analog circuits on the baseboard that allow for example simulation of temperature sensors, generation of input voltages for the GPIO pins, or measurement of various chip voltages of interest. This section also creates numerous bias voltages and currents needed throughout the board.

- Other onboard circuitry:
  Other baseboard circuitry contain for example the general board supply, numerous interfaces for external devices, an ID system to identify which specific add-on boards are connected, and various control logic and relays.

Although the mentioned blocks of the verification board can nicely be grouped on paper, they are highly interconnected with others in reality. This means that each decision taken for a single block directly interferes with the others, which led to multiple iteration loops during the development phase. For this reason, also the descriptions given here, will present influences between different blocks as well.

3.3.2 DUT Boards / BMS Boards and coarse supply concept

To allow for future pinout changes as well as a direct connection to application-specific boards, a flexible interface concept was needed for the DUT connection. A technique that was successfully in use with other projects utilizes a so called DUT-Board. This means that the testfixture connecting to the DUT resides on a separate board that is placed on top of the main verification baseboard.

The benefit from this separation is the possibility to adopt a cheap DUT-Board to changing needs whilst leaving the expensive baseboard unchanged. Such changes can for example be as simple as different testfixtures for different DUT packages or adoptions to IC-pinout changes. On the other hand, also more complex changes, like extensions for wafer prober station adapters, or additional hardware for special applications can be handled with the very same and unchanged baseboard.

However, there are drawbacks from this technique as well. It clearly introduces overhead like additional connection points, with all its failure possibilities, as well as additional wiring that otherwise would not have been necessary. It therefore depends on the requirements if such a concept can be used and if countermeasures are needed to compensate for the wiring overhead.

The requirements for such a DUT-Board concept were the following:

- Allow connection possibilities for DUTs in a CLCC-68 and a LQFP64 package via testfixtures, and also directly soldered LQFP64 package as well.
- Allow connection possibilities to DUTs mounted on a BMS 8.0 board.
- Use reliable electric contacts with low mechanical insertion force.
- Provide possibilities for external temperature forcing with simultaneous temperature sensing.
- Allow some form of connection to a DUT located on a wafer prober station.
- Provide high analog performance (deviations in the sub mV range only). This also involves an adequate grounding concept.

- Provide the dedicated voltage measurement connector described on page 43.
- Allow for fast switching for Active Balancing.
- Provide direct access to all chip pins for special measurement tasks like leakage current measurements.
- Provide the possibility to disconnect each chip pin separately from the baseboard for special measurement tasks.
- Provide an SPI connection routed for highest speeds to allow for SPI timing verification.

As in most electronic design tasks, no solution can be found that is perfectly fitting for every requirement, as some will always be in direct contrast to others. For example, all the required connectivity options will always be in contrast to the request for minimum connections and wiring length optimal for Active Balancing.

3.3.2.1 General decisions for the DUT-Board concept

To provide a good compromise for the most important requirements, some decisions concerning the partition had to be taken.

- First of all no high current Active Balancing will be done directly on the baseboard, nor on the DUT-Board. As the high current levels and rise times provide extremely high requirements on compactness and wiring, all the other requirements would be unfulfillable. However, there will be a possibility to do a high current Active Balancing with the DUT-Board in combination with a slightly modified BMS 7.x powerstage residing directly on a super capacitor array or a battery. Therefore, only moderate gate driving and diagnosis currents need to flow from the DUT-Board to the power-stage. But the baseboard will provide a possibility for an Active Balancing setup with reduced currents, which utilizes a transformer with higher inductances, as well as standard Passive Balancing. More information about the Active Balancing will be given in the balancing section starting on page 113.
- There will be two connector panes on the verification board. One dedicated for the BMS 8.x board and another for the actual DUT-Board. As both have different sizes they can relatively simple be interconnected. This reduces the amounts of necessary connection points and wiring for the BMS board to a minimum.
- The filter stage for the ADC inputs has to be present on each DUT-Board to provide the input currents needed for the switched capacitor structures as close to the IC as possible. These input lines will therefore have the highest priority in wiring in the DUT-Board design, to achieve the needed accuracy.

- A special mechanical adapter for thermal forcing will be manufactured to keep the forced area at a minimum. In this way all test-pins to the DUT are still available, and only the chip resides in the area with forced temperature.
- Some form of identification of each DUT-Board shall be possible. This will be necessary for documentation and reproducibility of the measurements. This will be described in more detail starting on page 141.

The outcome of this design process can be seen in figure 3.32.

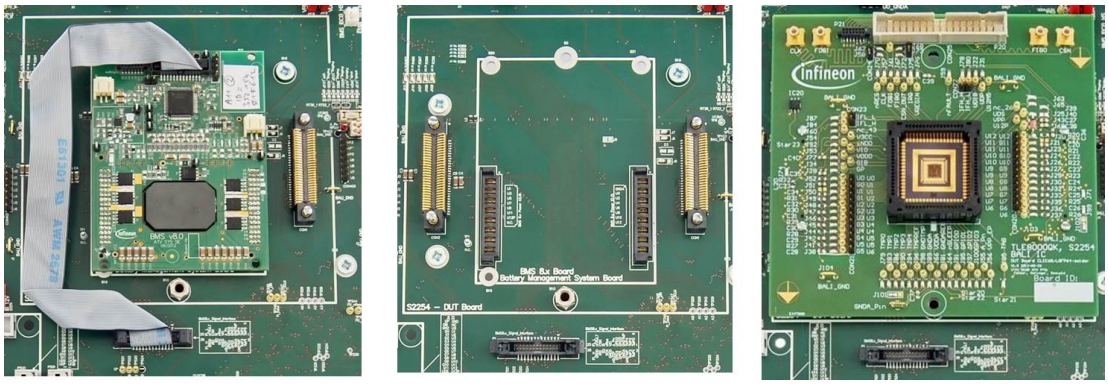


Figure 3.32: DUT-Board interface on baseboard. Left: with BMS 8.0 Board. Middle: no Board populated. Right: CLCC-68 DUT-Board

3.3.2.2 Connection to the DUT-Board or BMS-Board

In the center of figure 3.32 the connectors on the baseboard can be seen, without any board connected to it. The left image shows this area populated with a BMS 8.0 board, whereas in the right image the standard configuration with one of the various DUT boards can be seen. In this case a DUT-Board for ceramic CLCC-68 packages is shown, allowing direct access to the die, as can be seen in the image.

The left- and rightmost connectors (figure 3.32 middle image) are Samtec FSI-130-10-L-D-E-AD board-to-board types, with low-connection-force. They provide a total of 120 contact pins, which connect to gold plated landing pads on the DUT-Board's bottom side. This allows to bring all pins of the IC down to the baseboard. It also offers the possibility to have multiple ground pins for shielding and optimal HF-return paths.[13] Therefore, all signals were arranged in a way that keeps their current return paths minimal and minimizes cross coupling to other signals. Signals with critical requirements, like the cell voltages are routed with two pins per signal. Those pins therefore allow for higher currents, lower deviations due to electrical contacts and best routing possibilities, for optimal HF return current paths, as can be seen in figure 3.33. This means for example that all ground related signals like SPI etc. are placed next to GND pins, whereas for

[13]The Samtec Connector itself is rated up to GHz range for both, single and differential ended communications, which is even beyond the needs in this work.

example the push/pull gate driver signals are located near their next higher and lower cell voltage lines as those are their reference levels, which can be seen in figure 3.34.

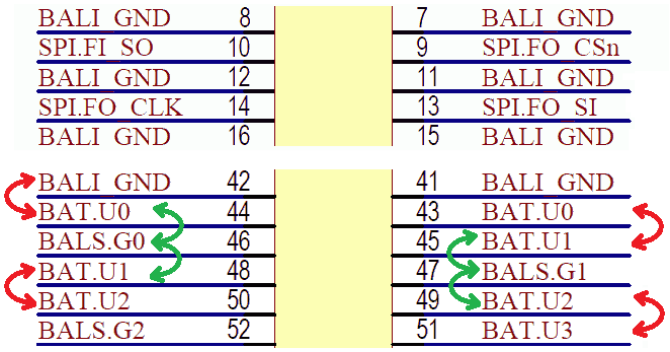


Figure 3.33: Example of HF-optimized pinout. Top: Ground related signals next to Ground. Bottom: Red arrows: Ux pins are locate next to Ux+1. Green arrows: Gx pins are embedded between Ux and Ux+1 pins

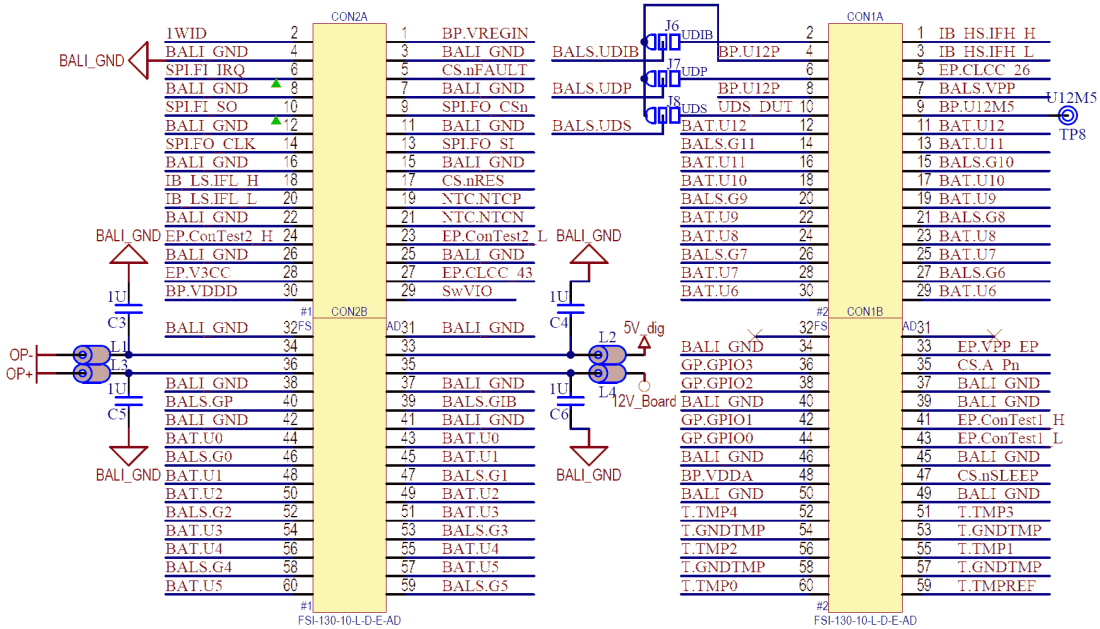


Figure 3.34: DUT-Board to baseboard connection

The two central vertical 8-pin connectors (figure 3.32 middle image) are also special types from Samtec, the high current UPS-08-04-01-L-V, that provide an extremely low DC-resistance of around 1 mΩ. They were chosen as the power connectors for the BMS 8.0 board, to keep power losses low for Active Balancing.

The horizontal aligned connector on the bottom (figure 3.32 middle image) is the data connector for the BMS board that provides the SPI and other verification relevant signals to the BMS-board. It is a standard miniature IDC connector

with 0.65 mm pitch size and is normally connected via a flat ribbon cable to a BMS-board, as can be seen on the left image.

3.3.2.3 Details for measurement accuracy and interconnections

In the verification process it is often necessary to measure dynamic signals with an oscilloscope as close to the IC as possible. It is also required to have the possibility to disconnect all external circuitry from the DUT to allow special measurements, of for example leakage currents. For this reason, each IC-pin on the DUT-Board is equipped with a testpin and a solder jumper (normally closed), as can be seen in figure 3.35. As these testpins also have to be accessible with temperature forcing equipment in place, an additional wiring length of 2 cm is introduced. Although this is not a problem for most signals, it can become critical for power supply pins or the accuracy of the Ux pins. Therefore, an additional footprint is provided for the decoupling capacitors, as close to the IC pins as possible on the bottom side of the PCB (normally unpopulated). The importance of this wiring could impressively been seen in the first design step of the DUT-Board for the ceramic package.

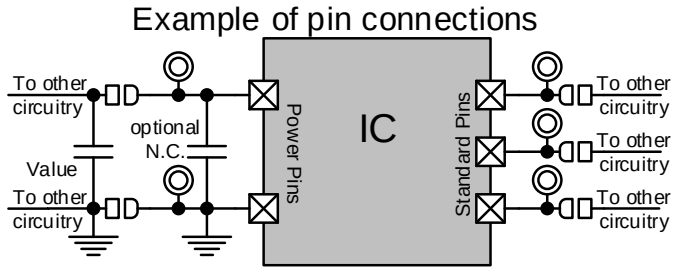


Figure 3.35: IC-pin connection concept, utilizing testpins and solder jumpers

Example of wiring importance on the first revision of the ceramic DUT-Board

The pinout of the TLE8000QK IC features 2 blocks of each 6 ADCs on two opposite sides of the chip package. This results in a special position for the middle cell voltage U6, as it is only present on one chip pin on one side, although it is internally connected to ADC 5 and 6. Therefore, also the external filter circuit coming from both sides needs to be connected to the U6 line. This however results in the fact that at least one of these filter capacitors has a longer PCB routing length to the pin than the other. As the thermal forcing equipment needs some spare space around the DUT's testfixture, there is also an additional longer distance of the filter from the IC on both sides. This combination plus a non-perfect routing in the very first design step of the ceramic CLCC-68 DUT-Board immediately altered the accuracy matching of the U6 ADC channel by around 8 LSB in comparison to the Automated Test Equipment that was used to test and calibrate the chip![14]

[14]Fully matching the accuracy results of the tester and the verification board to the last bits, required multiple measurement sessions, to identify remaining parasitics on both boards, even

Figure 3.36 illustrates this first revision of the ceramic DUT-Board with the layout imperfection, to better give an impression on how demanding the overall design process was. There are various highlighted sections that show the current loop

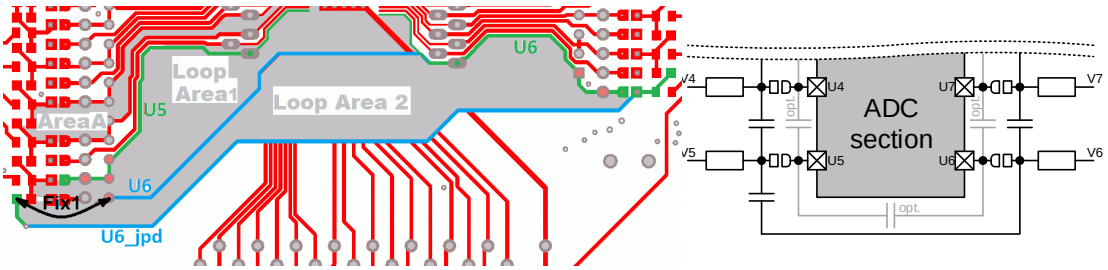


Figure 3.36: Layout impact on the filter capacitors connected between U5 and U6 in an unoptimized first layout step

areas for the filter capacitors. "Area A" (∼1.2 cm^2) shows the loop for the ADC that measures on the pins U3, U4. This area represents the typical optimized loop for all ADCs, except the one connected to U5 and U6. As the loop inductance corresponds to the loop area one should always try to keep this area minimized. The outer bound of "Loop Area 1" (∼3.7 cm^2) plus "Loop Area 2" (∼5.8 cm^2) shows the initial implemented loop area for the unoptimized ADC channel. As this area is approximately 8 times greater than "Area A" it is clear why the loss of accuracy was only present on this particular ADC channel. In an intermediate improvement step the loop area was reduced by adding a wire on the two points indicated by "Fix 1". This reduced the loop area roughly to one-third and the deviation to around 2 LSB. Adding the decoupling capacitor on the footprint of the bottom side completely removed the deviations on these first boards.

For the next versions of DUT-Boards the loop area was further optimized which removed the deviations, whilst allowing to keep the capacitors on the top-side and out of the thermal hot spot.

3.3.2.4 Details on the temperature forcing concept

Simulation of ambient temperatures at Power Train Systems is often done with a Thermonics T-2500 temperature forcing system. This instrument features a moveable shroud that can be put around the DUT to force a correctly tempered air flow around it. The shroud can be exchanged with various sizes, but all available types are too big to leave the probing testpoints on the outside without massively increasing the critical wires between the filter and the ADCs. It was therefore decided to design a mechanical Teflon adaptor to reduce the size of the shroud opening down to a workable minimum.

with the new oscilloscope and differential equipment.

A conceptual drawing and a picture of the actual manufactured adaptor can be seen in figure 3.37. Unfortunately this kind of thermal forcing equipment creates high temperature gradients, as only one part of the PCB is heated, which can cause thermal EMF. One can therefore only try to thermally optimize the PCB in such a way, that the biggest gradients occur in areas where they cause the least side effects. If the analog voltage performance checks have to be done against temperature, using the small application boards inside thermal controlled racks will result in more reliable results, as gradients can be minimized.

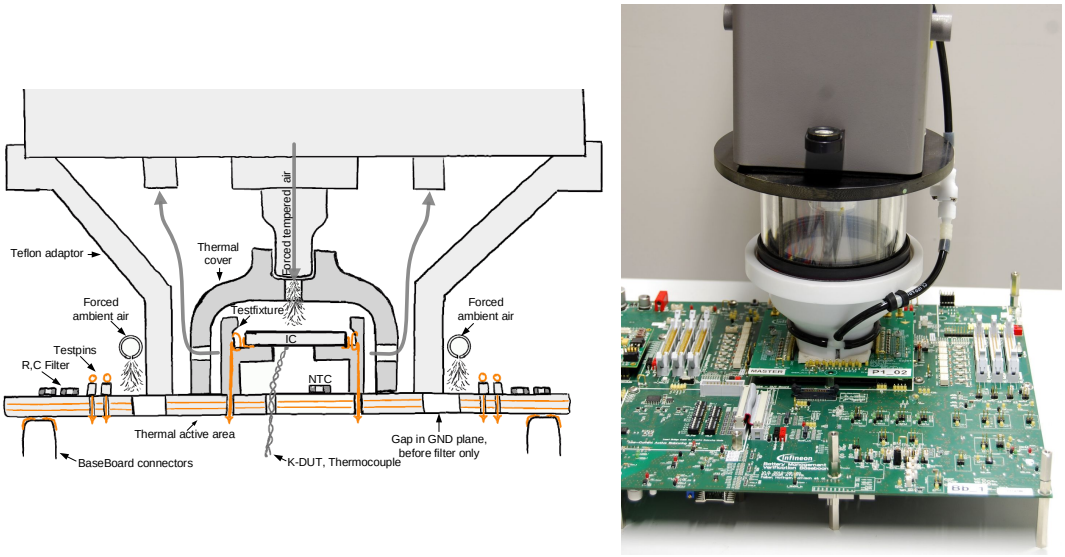


Figure 3.37: Left: Concept for thermal forcing adapter; Right: Realization

However, some ideas were realized in the DUT-Board concept, to try to move the gradients away from the most crucial spots. In general materials with high thermal masses and good conductivity may be used to equalize certain areas, whereas materials with low thermal conductivity can be used to isolate other parts.

The idea was to surround the RC filters with a multilayer ground plane that has some isolation gaps towards the temperature forced center of the PCB. The good conductivity of the copper underneath the critical parts shall therefore equalize the temperature around the filter components and keep gradients and therefore thermal induced voltages low. All incoming traces that connect to RC filter must first pass massive parts already above this equalization plane, that cannot create series thermal voltages, like testpins or pinheads as they are connected in parallel. As these parts already reside above the plane they act as a kind of thermal drain for the incoming thermally active traces, which helps to decrease their temperature difference to the local plane. Of course this is only possible for the differential Ux pins, as other ground related signals could be affected by the increased ground return path by this technique.

To faster reduce the temperature gradient from the adapters inside to the outside, a so called purge air flow is present around the adapter, that uses air with ambient

temperature. The overall goal is to keep most of the gradient close to the border of the adapter and away from the parts of the filter or the electrical contacts.

But as said before, such a DUT board will always be far bigger than an actual application board due to the needed connectivity. Ultimate performance tests will therefore always have to rely on the small application boards and thermal chambers.

3.3.2.5 Probe station interface concept

It is sometimes of interest to measure, or force signals that are only present inside the DUT and do not have connections to pins, as they are not required during normal operation. The TLE8000QK therefore features testmodes, which are also used during the initial test program and allow, e.g., re-routing of some dedicated highly important signals to external pins. And there is even another more direct method to allow access to such signals. In this case miniature contact pads are added to such a signal in the layout process. These pads are too small for standard bond wires, but they can be contacted with special probe needles if necessary. Of course this is only possible with partially opened DUTs that allows direct access to their bare die. Furthermore, a so called wafer probe station is needed, that provides a vibration-cushioned table, a microscope and high precision micro-manipulators carrying the probe needles.

As this equipment has very limited available space, it is not possible to put a whole verification board there. Therefore, some way of remote operation is required for the verification environment, to be ready if the need arises. One possibility that was already tested uses a slightly modified DUT-Board with a manually added on-board voltage divider and various extension cables to the baseboard for communication.

Although this simple setup can be used for urgent cases, figure 3.38 shows an improved concept that would allow more options and a sturdier prober access. The idea here is to use an extension cable, with an adaptor board on both sides between the base- and the DUT-Board. This allows to still use all the baseboards functions, and the different DUT-Boards on the probe station. Of course the cables introduce additional parasitics like series resistances and capacitances. But normally measurements that require a wafer prober don not aim on accuracy but more on some basic block functions.

The proposed adaptor board would provide the landing pads for the DUT-Board's Samtec connector on the bottom and the according solder pads on the topside directly connected to it, as well as connectors for extension cables. As a result a single type of PCB would be sufficient on both sides of the cable.

Furthermore, this PCB could feature footprints for additional parts like decoupling capacitors or bypassable logic buffers, that can be used to counterbalance some of

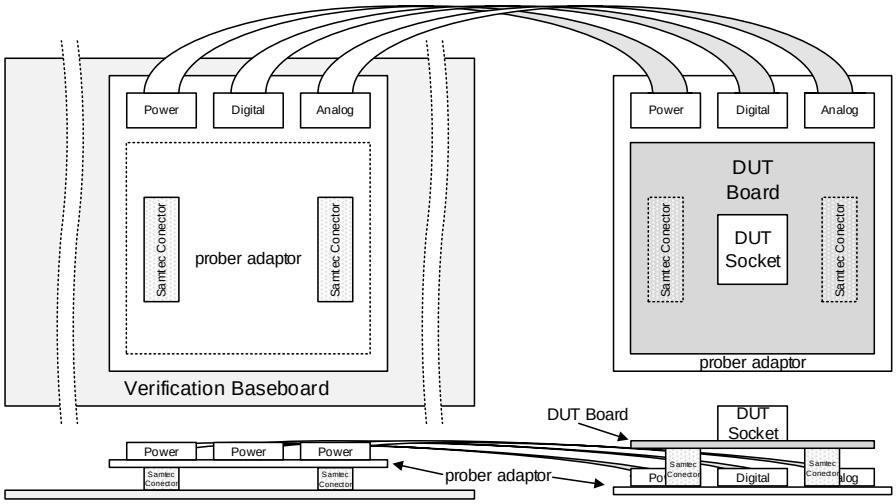


Figure 3.38: Probe station interface concept

the effects of the extension cables. But as the DUT-Board already features most of the bypass capacitors, and communication speeds can be kept low on demand, the effort for the implementation of this improved adaptor should overall be minimal. It therefore provides a good possibility for a future upgrade to the existing modified DUT-Board currently used to interface to the probe station.

3.3.3 TLE8000QK supply concept

The supply concept was one of those design objects that is highly interconnected with all the other parts of the baseboard. It therefore needed many iterations before a satisfying solution could be found. One difficulty was to support all the chip's supply modes, even with different external powers supplies as only one 12 channel battery simulator was available at the time. At the same moment the need for better repeatable automatic setups, as well as increased accuracy was needed to be achieved.

In a real application the chip's supply current will always come from a battery in the end, but here additional possibilities needed to be provided as well. For example, it is also of interest to allow for different energy sources for the low voltage and the high voltage domain. This provides a possibility of unloading the 12 channel battery simulator from the chip's supply current for accuracy measurements.

3.3.3.1 High voltage power supply - Battery emulation

As the low voltage domain of the TLE8000QK can be either completely separate or derived from the high voltage side it is beneficial to consider all high voltage supply possibilities first.

3.3.3. TLE8000QK supply concept

It is obvious that a 12-ch battery simulator per baseboard would give the most degrees of freedom to the verification engineers. However, there is only one such device available and there are many tasks where a much simpler and also cheaper setup is fully sufficient, like for pure digital or non-accuracy related tests. For all those tests, a simple resistor ladder with one or two stacked DC sources may be used instead.

To give a better overview of the realized high voltage supply possibilities, figure 3.39 illustrates them all in the same graphic. External high voltage supplies are grouped with colors to better see associated parts. The more opaque a color or the thicker a line, the more current can be provided via this path. Basically each colored option is primarily intended to be used alone, but there are some combinations that can be of interest. Two integral parts of this supply concept are the relay matrix and the interconnection area, which will be discussed before the supply possibilities will be presented in more detail. The high voltage supply is split into two blocks. A low side ($U_0 \ldots U_6$) and a high side ($U_6 \ldots U_{12}$), similar to the chip's separation of the ADC channels and best visible in figure 3.40.

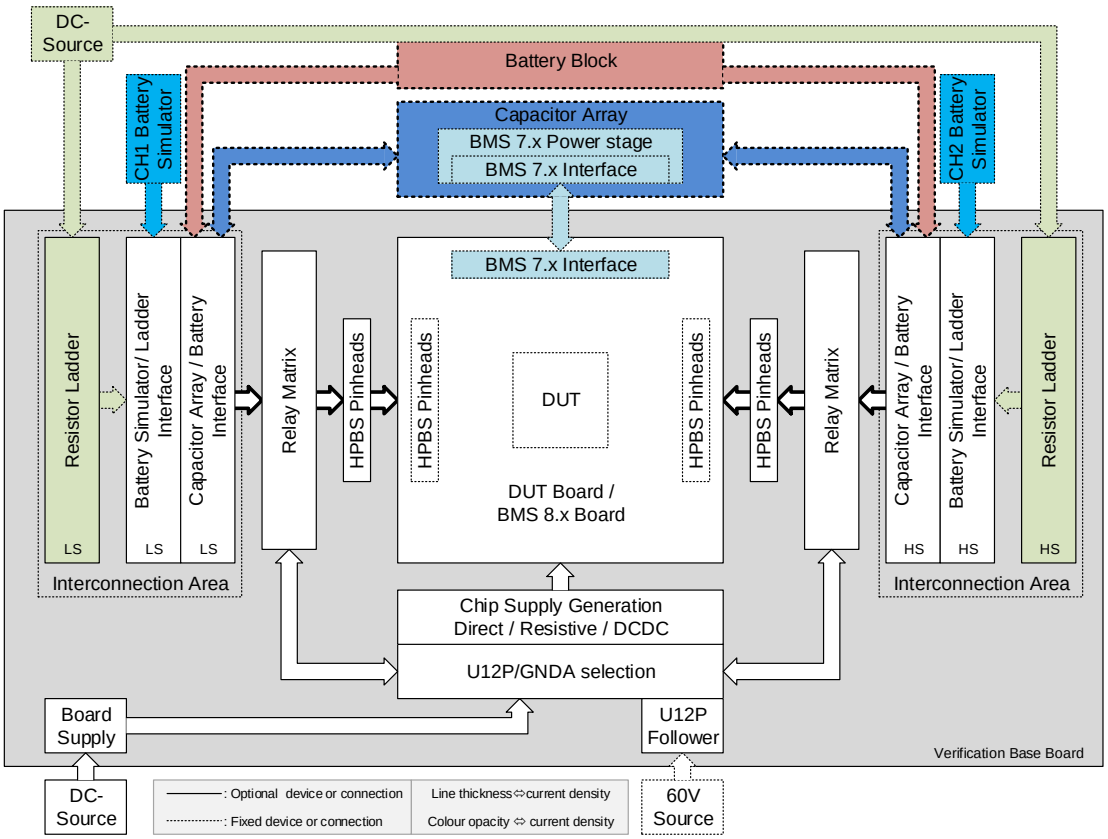


Figure 3.39: Coarse DUT-Board high voltage power supply concept

Relay matrix

For many parts, like the 12-Ch Battery simulator that was built for 12 cells, it is not sufficient to just turn off a single channel to disconnect it from the DUT if less cells are needed. This would mean that components like output capacitors would still stay connected that are just not present in a real application. It therefore has to be possible to actively establish and break the connections somewhere on the baseboard. On the X11 board this had to be done with around 30 separate jumpers that needed to be set manually, which led to an error prone setup procedure.

The new baseboard uses a relay matrix (figure 3.40), that can be controlled by the main FPGA, which allows to store and reload setup configurations. It allows independent disabling, enabling, or shorting for each individual channel. Furthermore, it provides two additional paths for U12 and U0, namely U12P_BAT and GNDA_BAT, to allow for the mentioned separate connection of the chip's supply from the measurement path.

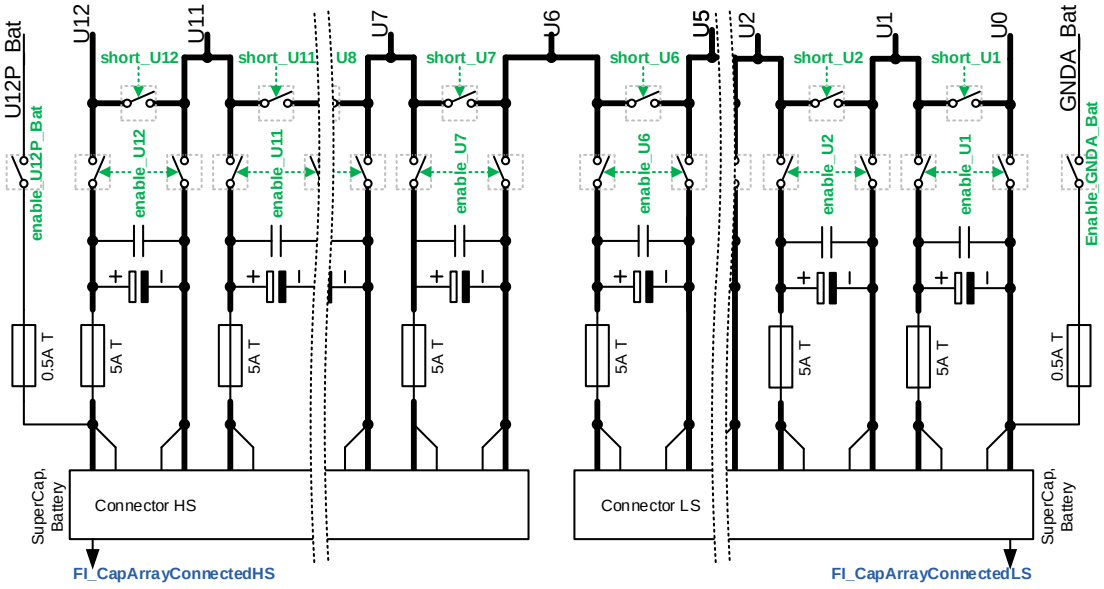


Figure 3.40: High voltage power supply: relay matrix detail
green: Relay driver, blue: FPGA digital portexpander

The relays used are highly reliable signal relay types (Axicom IM06DGR) that offer up to 5 A of continues current, while still having less than 10 µV of thermoelectric potential. More information about this special relay series will be given on page 122, although on the IM26GR which is the 2 A, ultra-sensitive variant of it.

Interconnection area

Another important part of this concept is the connection area, as illustrated in figure 3.39. Although it follows a rather simple idea, it very effectively offers a way to utilize the various supply possibilities, and even combinations whilst reducing

manual setup effort. It consists of 3 times the battery simulators 40-pin IDC connector per side (6 cells), although with different wiring attached to it.

The interface closest to the DUT-Board in the middle, is the power connector which connects to the relay matrix via highest possible copper usage on multiple PCB layers, to keep the resistance low. It is intended to be used with the high possible currents of either the capacitor array or an external battery. In theory it has the same pinout as the battery simulator, but it is used differently. Here even the sense lines have the same copper area as the power lines, as they can also be used for power flow from a real battery to the board. At least if the externally connected capacitors or battery cells are connected properly, which results in 4 parallel wires and contacts per Ux signal, and therefore lowest achievable resistance.

The connector in the middle is the true battery simulator interface and is wired 1:1 to the connector dedicated for the battery. However, this connection uses slightly less copper, as otherwise the power connector would have needed to accept thinner track widths.

The outermost connector is directly connected to a resistor ladder and is not wired to the other two. It can be used instead of the battery simulator by simply inserting a 1:1 IDC cable between the middle and the outer connector. This can be seen in figure 3.72 on page 151. To supply the ladder an additional external DC source is required as depicted in figure 3.39 on page 107.

As the original battery simulator interface uses a 37 pin SUB-D to 40 pin IDC connector cable, 3 pins are unused. Those pins were utilized to implement an automatic detection of the currently used setup (figure 3.41). So it is possible to independently detect whether the resistor ladder and/or the capacitor array and/or battery are connected. This can be logged by software to allow reproducible results.

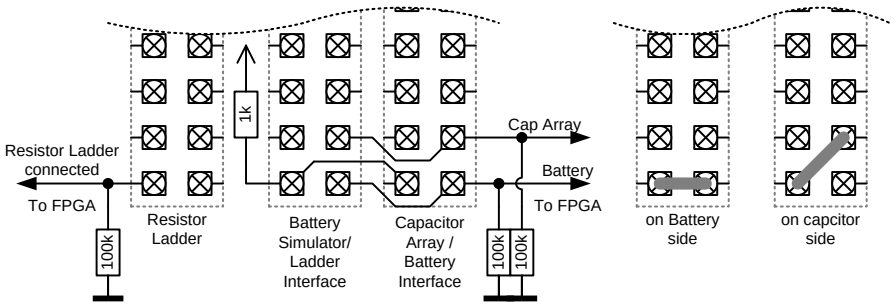


Figure 3.41: Connection area, automatic detection circuit

Most relevant supply possibilities

Resistor ladder: This is the simplest possibility to provide the high voltages to the DUT. As the relay matrix already allows to short or enable individual

channels, the manual connection effort is reduced from the around 30 jumpers on the X11 board to simple insertion of two IDC cables in the new baseboard. Each cell of the resistor ladder consists of resistors with 100 Ω in parallel with 10 µF and 100 nF capacitors. It features two banana plug connectors for the lowest 6 cells and 2 for the highest 6 cells, to provide the voltage with either one or two external DC-sources.

Battery simulator: The Pickering 2x 6 channel battery simulator can easily be added to the middle connector of the connection area. The relay matrix allows to easily disconnect a specific cell, which provides the possibility to use another type of cell emulation, like the HPBS instead.

Capacitor array: The capacitor array can be added to virtually any of the other supply possibilities to allow for higher peak currents during Active Balancing. It should therefore be added to the center-most connectors.

Battery: Batteries can be connected instead of the capacitor array as well. Fuses are provided on the baseboard, however it strongly depends on the mounting method for those external batteries, if additional fuses should be placed close to the cells to protect the needed wiring. One simple but also practical solution may be to use a small PCB equipped with 6 battery holders per side that can directly be fitted onto the IDC connector. This would keep the wires extremely short, and could avoid the need for extra fuses (dc-resistance) depending on the actual realization.

Reverse supply via the BMS 7.x power stage + DUT-Board: One very special supply mode arises for the high current Active Balancing mode. In this mode the power does not come in via the connection area but from the BMS 7.x interface on the DUT-Board. More information on this will be given in the Active Balancing section on page 113 onward. An image of such a connection can be seen in figure 3.44 on page 115.

Hotplug simulation: As all supplies are normally routed via the relay matrix, it is possible to simulate so called hot-plug situations with the baseboard. A hot-plug event happens when the application board is connected to the pre-assembled batteries, which has to happen whilst the battery voltage is present. In a normal application environment the connection order of the board's contacts to the battery stack is random. To simulate serially connected batteries, solder jumpers are provided that allow a serial connection in front of the relays, as real batteries would also be connected in series. The relays can then be activated with various programmed patterns to simulate random hot-plug events.

3.3.3.2 Low voltage chip supply concept

As already described in section 2.2.5 the chip is intended to work with a variety of supply possibilities. However, all of these supply modes normally draw their power solely out of the battery. Whilst this is hardly any problem with real batteries, the chip's supply current, which increases during ADC measurements, can already alter the accuracy of the 12 cell Pickering battery simulator enough to affect the chip's measurement results.

In order to avoid any unwanted impact on accuracy, additional supply modes were added to the verification board. Figure 3.42 depicts the realized concept. It provides the verification engineer with the complete freedom to choose any means of supply for the chip either from the battery or external, as appropriate for the intended test.

Ferrite beads, in combination with decoupling capacitors, were inserted between many sections of the supply path. This was done to ensure that ripple currents, and the resulting ripple voltages remain in the areas where they cause the least effect, and prevent them from propagating to the sensitive Ux lines.

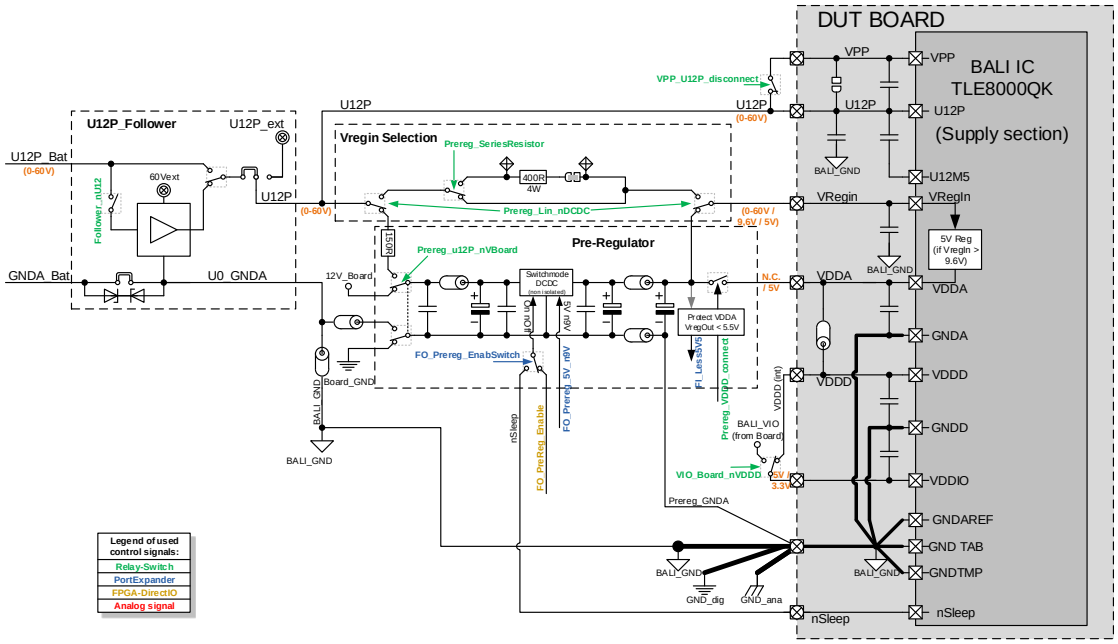


Figure 3.42: Baseboard - Chip power supply

The signal-name colors used in the diagram represent the way the FPGA is connected to the devices. Green indicates that the control happens through an FPGA controlled relay driver IC that will be talked about on page 140. Orange represents fast direct digital connections to the FPGA via a level-shifter, whereas blue means that the signal is connected to the FPGA via a lower speed port expander (page 142). Red represents analog signals, both driven or sensed by analog circuitry that

will be explained in section 3.3.6. This color-scheme was already used in figure 3.40 and will be further used for various detailed concept graphs of the baseboard.

U12P-follower

The first part in this supply concept is the U12P follower circuit. Every other part is powered via this stage and it allows three operation modes. First, it allows to use power directly from the Kelvin connection points at the battery/battery-simulator interface without any change. Secondly, there is an externally supplied decoupling circuit, that prevents loading the battery simulator with the chip's supply current. It is built around a loaded linear regulator, which is intended to follow the U12P voltage, although with limited accuracy which is sufficient for most cases. Finally, there is also a possibility to completely bypass the follower and the battery, using an external power supply as well.

Vregin selection

In the simplest supply option, the chip's linear regulator is directly connected to U12P, to create the 5 V level that is provided at the VDDA pin. As the excess voltage is turned into heat, the board provides the possibility to add a series resistor right in front of the regulator. One part of the regulated output-power is directly consumed by the analog part, which is internally connected to VDDA. The other part is consumed by the digital chip logic connected to VDDD. To prevent digital supply spikes entering the analog domain, a ferrite bead at the VDDA-VDDD interconnect and decoupling capacitors to the respective GNDs are used.

Pre-regulator

It is also possible to provide the 5 V supply for the chip with an energy efficient external DCDC regulator as can be seen in figure 3.42. In this mode the Vregin needs to be disconnected from the battery and connected together with VDDA to the 5 V signal. However, as any DCDC converter creates voltage ripple on its output, this may affect the accuracy of the IC.

Therefore, it is also possible to use the external DCDC as a pre-regulator for the internal regulator. This results in a high energy efficiency, combined with reduced voltage ripples. A good compromise uses for example 9.6 V as the DCDC's output voltage, which feeds the chip-internal linear regulators for post regulation.

In a normal application, only one of these supply possibilities is present. But on the verification board each has to be possible. For reasons of simplicity, the same DCDC converter was used, but with a switchable feedback ratio to select the output voltage to either 9.6 V or 5 V. This however, creates the danger of applying 9.6 V to the VDDA pin, which would destroy the DUT's analog circuitry. To prevent chip damage from a wrong setup combination, a safety circuit was

added to the VDDA relay that prevents connection, if the DCDC is setup for 9.6 V. Additionally it continuously measures the DCDC's output voltage with a comparator, and prevents the relay from closing if the voltage is beyond 5.48 V. To avoid unwanted switching of the relay, a Schmitt-trigger circuit was built with a hysteresis of around 400 mV.

To keep the amount of required external voltage supplies at a minimum, the pre-regulator can also be directly supplied from the verification board supply.

3.3.4 Balancing

As mentioned in the DUT-Board section, finding a workable solution for the balancing circuits was difficult as the needs are in great contrast to many other needs for the verification board. Although the passive variant works with moderate currents, the high current Active Balancing requires for switching periods in the µs range and peak currents of up to 20 A. This results in very high current rise-times, which require an optimized, dense layout, like on the application board. The verification board on the other hand needs to be flexible and allow many different measurement setups that may require additional connectors or parts. But every additional wiring, connector or solder-jumper increases the chance for unwanted voltage drops or other side effects like ringing.

It was therefore decided to split up the Active Balancing into different types and define the tasks that shall be possible with the verification board and what is better suited for other equipment.

- High current Active Balancing:
  Active Balancing with full application-like current. These high currents do not need to run on the verification board, as the BMS-Board 8.x, which was built in parallel by another engineering group, should be ready in time. However, different options for doing Active Balancing with a fully accessible IC (which normally requires a DUT-Board or similar) needed to be investigated.
- Low current Active Balancing:
  The verification board should still provide a way of doing Active Balancing although with reduced current, to allow full control of the DUT. The focus would be on the verification of the DUT's fault diagnosis and timing behavior, e.g., in Auto-Balancing mode of the chip.
- Test of the Active Balancing gate drivers:
  There are special testmodes that allow individual testing of the Active Balancing gate drivers. The verification baseboard shall allow to do both static and dynamic tests.
- Passive Balancing:
  Passive Balancing should be fully supported.

3.3.4.1 High current Active Balancing

The concept for this mode uses a modified BMS 7.x power stage that is directly mounted onto the battery or capacitor array (figure 3.43). Thus, the area that carries the high power currents is kept minimal. Only the control signals (Gx), feedback signals (UDx) and the relatively low chip supply current are exchanged to the connected verification board.

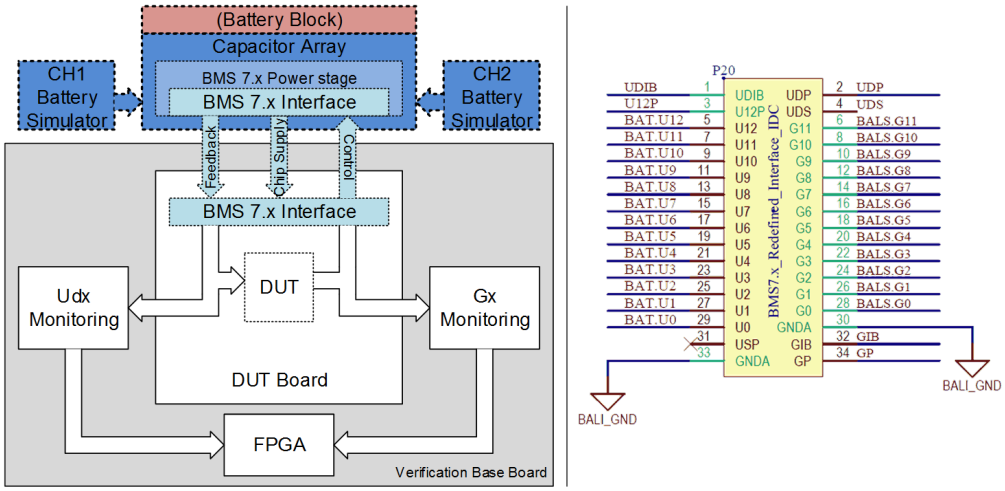


Figure 3.43: Left: Concept for high current Active Balancing;
Right: Modified BMS 7.x connector

To keep the wiring and the number of connections also for these signals at a minimum, the interface is located directly on the DUT-Board. As an effect the whole high voltage chip supply does now come from the opposite side in this mode.

The BMS7.x connector was updated (indicated by the green names) to allow best signal integrity with the new chip version. This means, that similar to the DUT-Board connector, each signal is located next to its high frequency return path. As this is a standard IDC connector, it is used with flat ribbon cables that interleaves the pins of both sides, according to the pin numbers. Some modifications had to be done to the BMS 7.x stage as well, as the Kelvin connections U12P and GNDA had not previously been available. Also the UDIB signal had to be attached manually from the power stage to the connector.

An image of such a high current Active Balancing setup can be seen in figure 3.44, where the verification baseboard with the attached DUT-Board is connected to the capacitor array[15] that houses a modified BMS 7.2 power stage, It can also be seen that the original mounted X11-IC has been removed from the power stage, leaving the LQFP-64 footprint empty.

[15] In this particular image a capacitor array with low capacitance is used only for illustration. Typically a 15 F array would be used for high current Active Balancing.

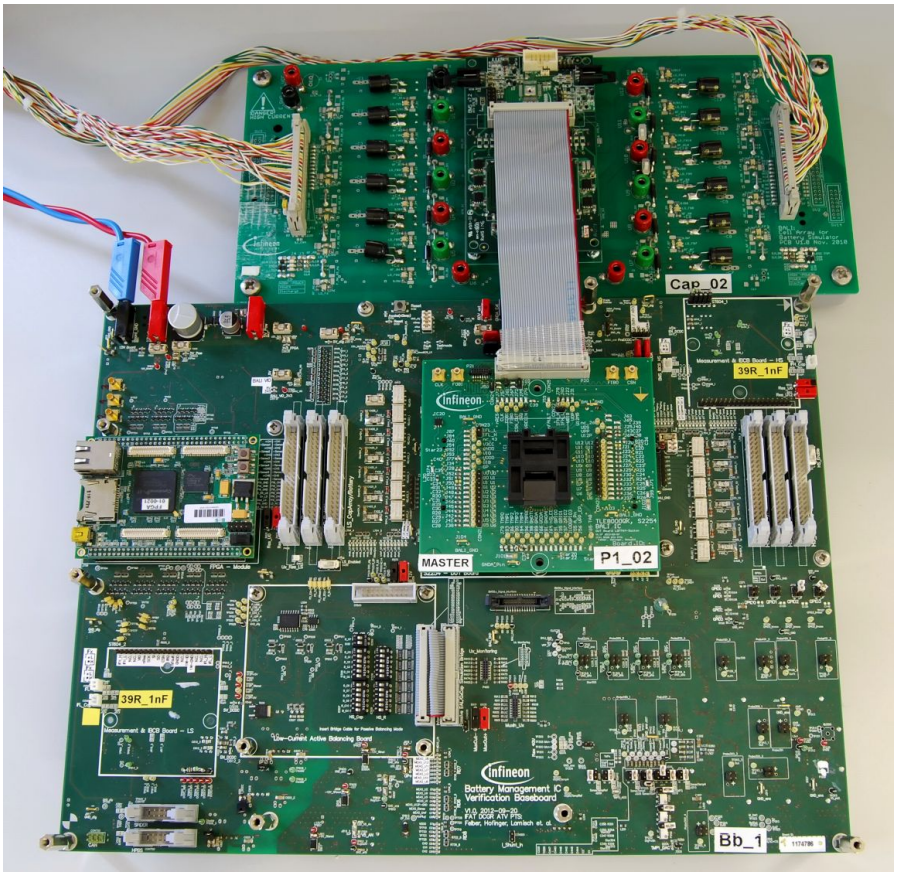


Figure 3.44: Verification setup for high current Active Balancing using the modified BMS 7.x power stage on a capacitor array

3.3.4.2 Low current Active Balancing and timing analyses

As decided a special version with reduced balancing currents needed to be possible on the verification board, as a fallback option. However, the hardware necessary for this implementation had to bring as little impacts on measurement accuracy for normal measurements as possible. There are basically two ways of reducing the average current, that both are possible with the built verification board.

Reduced on-time Active Balancing with the BMS-Board

This version uses a very simple approach, that was easy to implement and can be used for very first analyses. A standard BMS 8.x board is used but with limited on-times for the balancing power transistors. This keeps the balancing currents below 1 App with limited side effects.

Although this effectively reduces the current, it still has the same fast current transients, which can easily induce voltages in sensitive areas. The wiring was therefore realized by usage of HF-optimized paths with high copper usage on mul-

tiple layers, all the way from the decoupling capacitors of the relay matrices to the BMS-Board. Furthermore, additional capacitor footprints were added underneath the BMS interconnect areas, that can be populated if needed.

Low current Active Balancing with the DUT-Board

Nevertheless, to do a full verification of the automatic timing behavior, longer timings periods and better measurement interfaces are necessary as well. For this reason an option for additional low current balancing was implemented on the baseboard. It uses a transformer with increased inductances that allows application related timings, low currents and current slopes at the same time.

Since this required a new power stage, it offered the possibility to add all the diagnosis connectors and circuitry that were only of interest for verification and could not be added to the application board. As multiple power stages had already been tested with the X11 chip, it was clear that probably many different power stages could be of interest for the future as well. It was therefore decided to put this power stage on an extra add-on board that can be fitted directly onto the baseboard. The baseboard on the other hand should offer the diagnosis circuitry for functional and timing tests, which can be used to analyze this power-stage.

The diagnosis circuitry can be seen in figure 3.45, that also shows all Active and Passive Balancing, as well as gate driver testing possibilities of the baseboard. For the ground related gate drivers, comparators with settable thresholds are used, whereas the UDx section uses fixed thresholds and galvanic isolation. All diagnosis signals can therefore be measured relative to ground, which allows usage of standard oscilloscope logic probes. Furthermore, all signals are feed to the FPGA, which allows usage of automatic testing algorithms as well.

The low current Active Balancing's external add-on board has not yet been built, since verification with the BMS 8.0 board, as well as the high current Active Balancing approach that uses the BMS 7.x power stage ran extremely smoothly and were already sufficient. It can however be built and added to the main verification board at any time if the need arises for future derivatives of the chip.

Passive Balancing and gate driver strength tests

Besides these Active Balancing interfaces and diagnosis functions, the baseboard directly incorporates passive components to do further testing on the gate drivers. For Passive Balancing, power resistors are provided and for dynamic tests of the gate drivers capacitors are also available, that can be enabled via simple DIP switches. On the ground related gate pins, the Active Balancing diagnosis circuitry can also be used to measure timings directly with the FPGA, since the thresholds can be selected freely via a DAC.

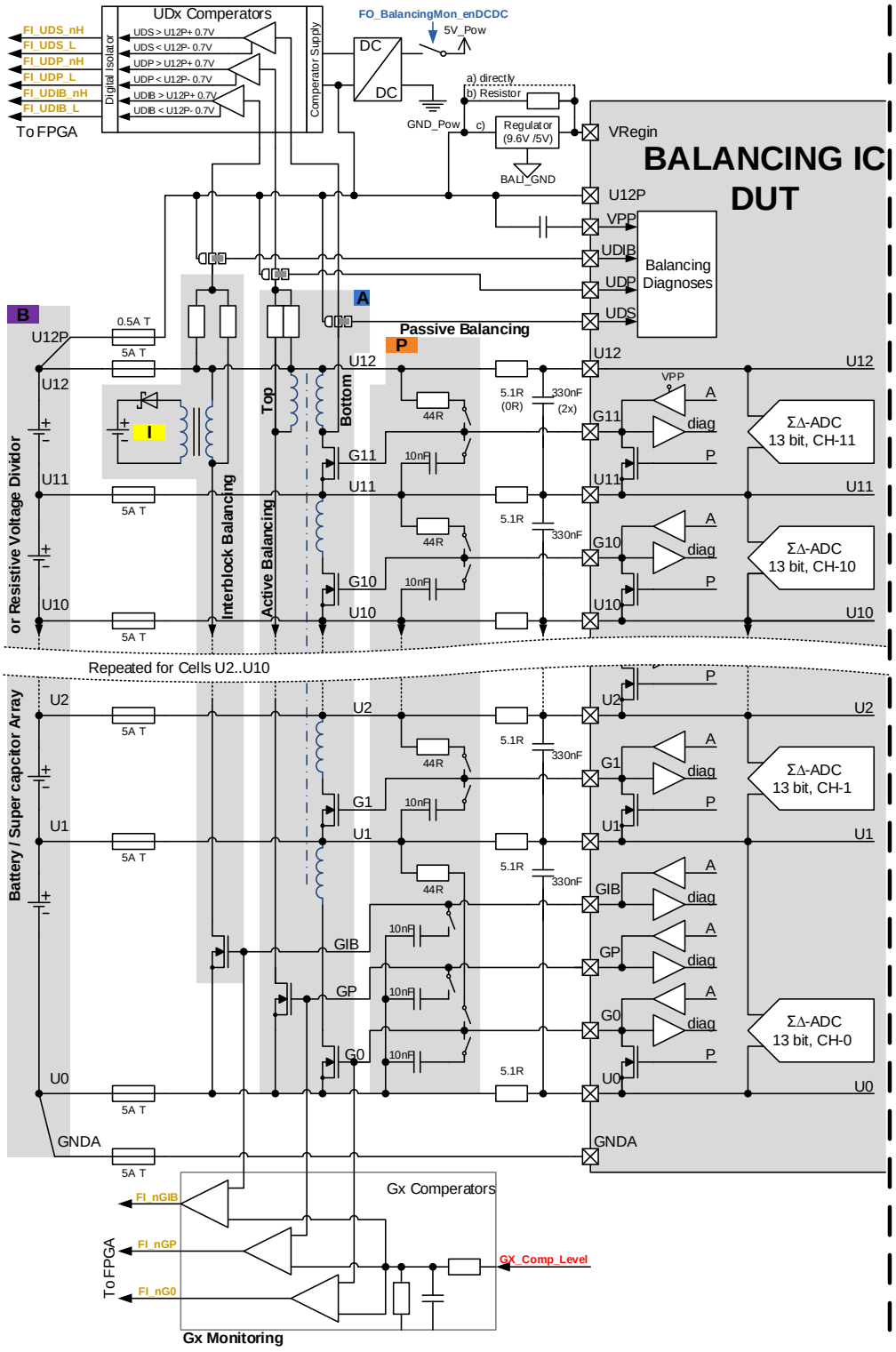


Figure 3.45: Balancing: Showing all possibilities at once with added supervision circuitry

To minimize the number of connections and to prevent the passive components to be still connected during Active Balancing, a similar approach to the connection of the resistor ladder had been chosen (figure 3.46).

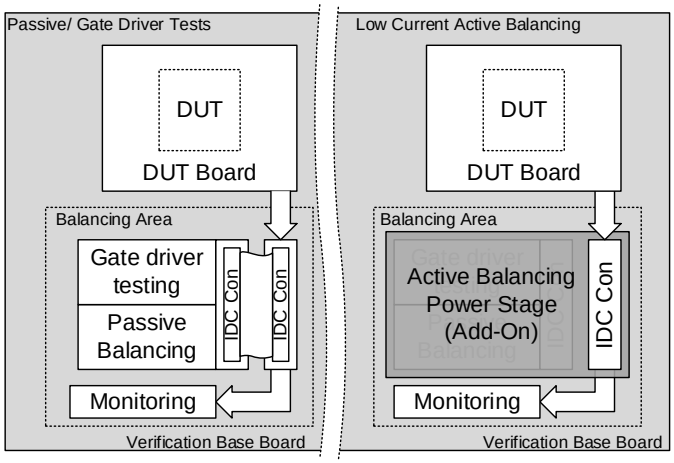


Figure 3.46: Interconnection concept for low current Active vs. Passive Balancing[16]

This means that all the passive components are present on the baseboard, but have to be connected to the DUT via an IDC cable. The presence of this cable can again be detected with the FPGA. It is therefore possible to warn the user within the software in case of erratic setups.

The same connector and the same PCB area is again used to connect to the low current Active Balancing subprint. This means that the usage of this subprint inherently prevents the passive components from being still connected, thus eliminating this otherwise potential error source.

3.3.5 Communication with the DUT- SPI and IBCB

Another very important feature of the chip is its communication capability. The verification baseboards concept was therefore designed in such a way, that it not only provides single-chip SPI communication, but also inter-chip IBCB communication in various configurations within multiple chips, without the need to always use several baseboards.

It furthermore had to provide a way that allows the chip on the DUT-Board to be used in the different communication modes the TLE8000QK provides. For example “Master on Top” (MoT), “Master on Bottom” (MoB). The master is the device the micro controller communicates to via SPI, and does the conversion between SPI and IBCB bus. The last device in an IBCB chain is called final node, whereas all devices in between are referred to as normal slaves.

To fulfill these requirements additional TLE8000QK devices have to be available on the verification board. If the TLE8000QK on the DUT-Board shall be usable as master and as slave, it also has to be possible to re-route the main SPI to one of the other devices as well.

3.3.5.1 Realized IBCB concept

Figure 3.47 shows the realized IBCB communication concept of the baseboard. Before the parts are described in more detail, a short overview is given here first.

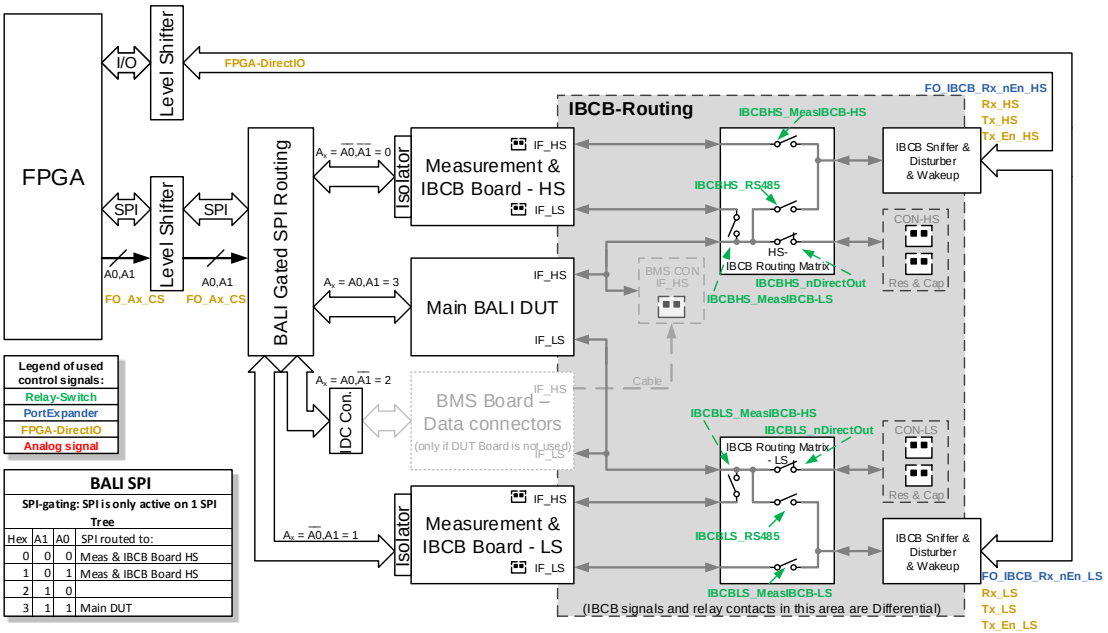


Figure 3.47: IBCB concept and routing

The communication system consists of the main DUT residing on the DUT-Board or BMS-Board and two additional TLE8000QK ICs, of which one can be connected to the top and the other to the bottom IBCB interface of the main DUT. Those additional chips are mounted on so called “Measurement and IBCB Boards” that provide basic SPI and IBCB interface, that can also be rerouted. Additionally a so called “IBCB Sniffer Disturber and Wakeup” (SDW) circuitry is also present for the low and high-side interface. A multitude of different connections can be established in a fully FPGA controllable way. This also allows to prevent bad connections by software. For example, simultaneous connection of both the HS and the LS interface to the SDW would otherwise lead to a short circuit of the interfaces.

The IBCB Sniffer, Disturber and Wakeup circuitry (SDW)

The SDW is a bidirectional communication structure that in essence resembles the hardware level of a very basic IBCB interface. A simplified view of this circuit is given in figure 3.48.

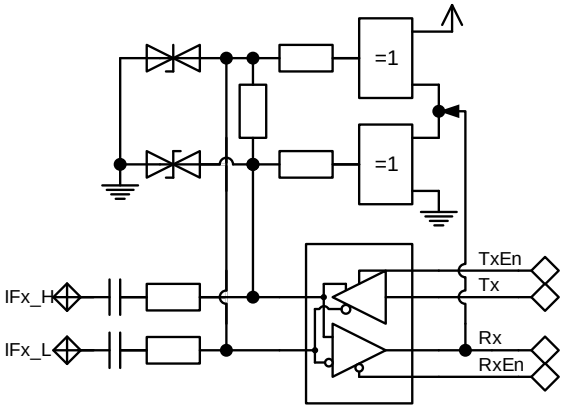


Figure 3.48: IBCB - Simplified Sniffer Wakeup and Disturber circuit

The circuit consists of a standard RS485 driver with a busholder circuit and some passive parts. Its single ended side is in direct control of the FPGA, which allows it to sniff or disturb ongoing communication. In theory, even a complete IBCB device could be resembled with the FPGA's logic blocks, which could be used by the designers to do real world analysis of code changes.

To wakeup the chip from sleep mode, differential pulses with dedicated length can be generated on the IBCB bus by the SDW circuit. Once the TLE8000QK recognizes this pattern on one side of its interface, it recovers from sleep mode and regenerates the pattern on the other interface to wakeup the next connected chip. To wakeup a complete chain of TLE8000QK ICs the pulses therefore only need to be applied to either the topmost or the bottommost device and they will propagate autonomously throughout the chain. Since the output of the SDW is capacitive decoupled, the SWD circuit can also be rerouted and used at different common mode voltage levels.

As long as the SWD is solely used in wakeup mode, only the transmission stage is used. As soon as sniffing and disturbing is desired the busholder and the receiver come into play.

Because of the capacitive decoupling, which removes the potential difference between the SWD and the TLE8000QK, no differential DC logic signals can remain at the receivers input. Therefore, a busholder with XOR gates was built, that feeds back the already received signal and allows to store the last bus state. However, as the busholder tries to keep the last bus state constant, it has to be connected loosely to the receiver, so that true communication is still able to change the buses state.

Measurement and IBCB board

As the additional TLE8000QK ICs have to be of the same type as the DUT they also need to be exchangeable, to allow for future design steps. However, there is no need to add two additional complete DUT-Boards, as the only interfaces needed here are IBCB, SPI, and power supply.

The idea was to build a very small special addon-board that removes the need for testfixtures and allows for future possible pinout changes. Furthermore, this board can be used for other special verification tasks as well, if it provides a standalone mode. Such tasks are for example, building extremely long IBCB chains to verify bus correctness or doing ADC verification with emphasis on solder or temperature stress. Figure 3.49 shows a 3D draft for such a Measurement and IBCB board.

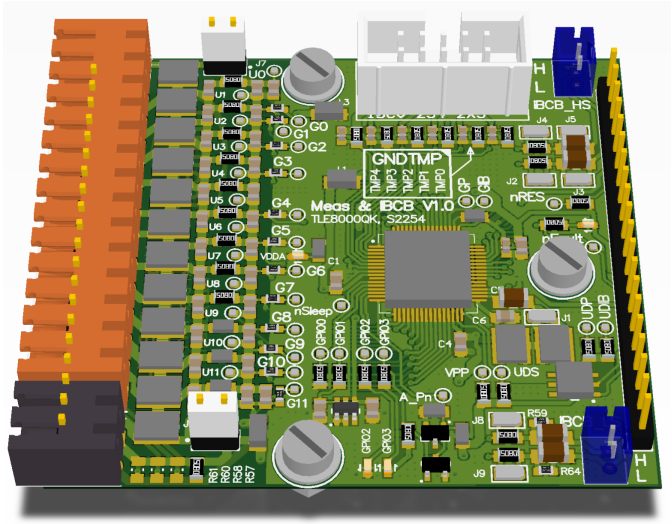


Figure 3.49: Measurement and IBCB Board - 3D visualization

As this board is designed for verification of dedicated functions only, not needed parts for balancing, etc., can be omitted, which keeps the area small and the wiring minimal. For communication tests in IBCB chains or on the verification board, a simple resistor ladder can be populated, to ease power supply. For measurement applications, connectors can be used instead to connect the board to batteries or simulators.

IBCB routing

To allow this multitude of communication scenarios it was necessary to reroute the IBCB lines in a highly reproducible manner. Although the IBCB connections carry digital information, the waveforms differ from standard logic signals, even if they were related to a single ground. Also the fact that many IBCB messages contain protocol depending direction changes between the master and the slave prohibits the use of standard off the shelf semiconductor devices as routing devices. So the

only true alternative was to use relays. As the IBCB signals base frequency is around 1 MHz, the switching device had to allow a minimum of 10 to 100 times this frequency to not unintentionally alter the original waveform.

A possible candidate are so called signal relays, which are common in telecommunication electronics. The Tyco IM signal relay series that is also in use for the power as well as the Ux sensing relay matrix is a miniature signal relay type of the 4th generation [Axi], which provides compact size and low parasitic effects. For example, all parasitic capacitances [AXI11] (between any contact and even the coil) have a maximum rating of 2 pF or less and an isolation resistance of $\geq 1\,\mathrm{G\Omega}$. Also at 100 MHz insertion loss is only 0.03 dB and contact isolation is still 37 dB, which is sufficient for this particular application.

SPI signaling

To allow the main DUT to become a slave device in upward or downward direction, the SPI needs to be routable to the other two TLE8000QK ICs so that either one of them can become a master. In difference to the IBCB, these SPI signals have pure logic levels with dedicated directions. But, because each TLE8000QK resides on a different common mode voltage level, galvanic isolating couplers are needed. A good choice for such tasks is the ADUM140x Quad-Channel Digital Isolator series [Ana12] from Analog Devices. These devices use magnetic air core transformers to transfer the signals from one galvanic side to the other. As they incorporate control and reconstruction logic with CMOS logic level compatible IO structures, they can easily be connected to other CMOS devices. They work from DC up to 1 Mbps, 10 Mbps or 90 Mbps depending on the grade, and provide a good alternative to classical optocoupler based approaches.

The SPI bus basically allows to connect to multiple ICs in parallel, with the use of chip-select lines that tell each IC when it shall listen to the communication. As each of the TLE8000QK ICs has to have access to this SPI bus to act as a master, a simple parallel connection would have resulted in high speed lines that basically travel across the entire verification board. Hence, also parasitic effects from this digital communication, like spikes would also have been spread out over the whole system. Since the verification board should allow voltage measurements in the range below 1 mV such disturbances had to be avoided. Unfortunately the FPGA board provided too few pins to allow routing of complete separate buses. Therefore, a signal gating approach was chosen as can be seen in figure 3.50.

Signal gating basically means that the there are certain barriers in the signal path that prevent signals to propagate beyond this barrier if it is for any reason desired (compared to clock gating[17] in CMOS ICs).

[17] Clock gating is a very simple but powerful way of reducing power consumption that is often used inside low power CMOS ICs. This means that inside these ICs, the clock signal is prevented

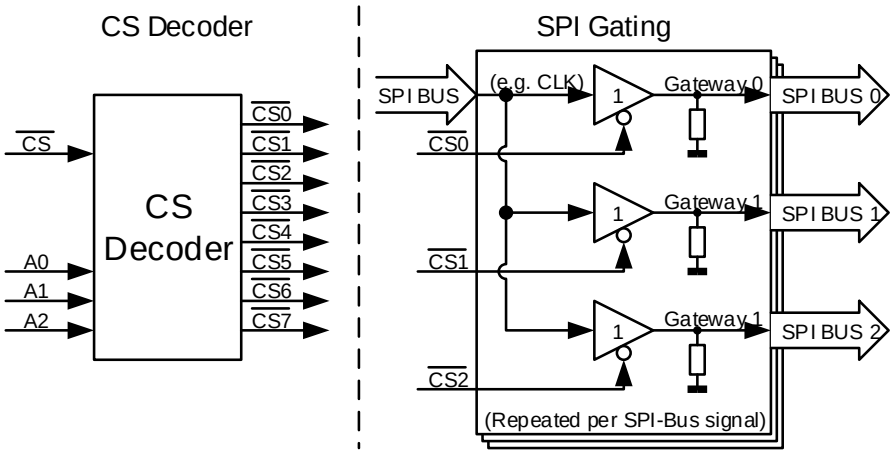


Figure 3.50: Signal gating - concept view

Gating can be done with various semiconductor devices. For example if OR-gates are used, the output will stay at logic high as soon as a single input goes to logic one. The logic part that is used defines the "sleep" voltage level. Alternatively simple logic buffers with output enable can also be used (figure 3.50), allowing to choose the recessive state of the output with pull-up or -down resistors. As always this flexibility comes with the cost of more required (in this case passive) parts.

Here in this context gating was utilized to split the SPI bus system into 4 independent branches. This can be seen in the conceptual overview figure 3.47 on page 119). The active SPI branch is only connected to the TLE8000QK configured for Master mode. As the gating semiconductors are located close to the FPGA, the noisy PCB sections are kept minimal and in a non-critical area.

3.3.6 Onboard analog equipment

Most of the other, not yet presented board functions require a great deal of circuitry for high analog performance. As these often make use of the baseboards analog core functions, these will be described here first. Those analog core functions contain for example a high precision ADC converter with a specially designed input multiplexer, a tuneable voltage reference, an 8 channel general purpose DAC, 4 high precision DACs[18], various amplifiers and a dedicated filtered power supply.

The general idea of all the analog board functions was to provide a compact system to cover many common verification topics, to reduce setup dependencies and failures resulting from false setups. For many measurements the analog circuits therefore need to measure with high precision and repeatability in order to reduce

to enter dedicated areas that are currently not needed, which stops their synchronous operation and lowers their current consumption [Pri14].

[18]The 4 high precision DACs will be explained in the GPIO section

the effort for external equipment to a minimum. At best only a single precision multimeter should be needed to do a few cross checks to ensure the accuracy of the system is still within the specified limits.

Mulitplexed precision ADC

The baseboard has to fulfill different requirements for ADC conversion. On the one hand there are slow speed signals that have to be measured with high DC accuracy. Examples are battery voltages or chip internal references[19] used for the TLE8000QK's ADCs with an accuracy in the 1.5 mV range and a resolution of 586 µV. On the other hand there are also fast changing signals, like the chip's NTC measurement waveforms. Here, the chip's SADC is used with a much coarser resolution of around 2.4 mV, but the signals need to be sampled within maximum 100 µs and that at a few dedicated points in time to allow verification of, e.g., correct voltage settling.

So while the conversion speed of 100 µs and a resolution of 16 bit (8x the PADC's resolution) with an 5 V FSR is a common target for today's ADCs, accuracies of better than ±1.5 mV are far more difficult to achieve. Especially since a 3 to 10 times better accuracy of the measurement system compared to the measurement target would be desirable. Therefore, the first step in the development process was a survey over the most promising ADC manufacturers to retrieve the current possibilities.

Although no search preference on ADC technology was present during the survey, the candidates found to fulfill the requirements almost exclusively used either classic SAR-ADCs or low speed ΣΔ-ADCs. Once all the error sources, like CMRR, gain error, INL, etc. were summed up only few types of ΣΔ-ADCs of the previously around 50 candidates were able to truly provide the high DC accuracy. As these devices are extremely oversampled they provide way more resolution than would be necessary. On the other hand these ΣΔ-ADCs only provide very low resulting conversion rates, which would also prevent most of the candidates from being usable in all cases. However, one series from Texas Instruments remained that uses a higher order for the ΣΔ-ADC to achieve both, high accuracy and speed.

The ADS1259-ΣΔ-ADC was a promising device on the market for this high range of applications. The setup of the ADC can be changed via software commands, which enables the user to choose between low speed with highest accuracy (10 SPS with 24 bit) or high speed with reduced accuracy (14.4 kSPS with 16 bit). Figure 3.51 shows the conceptual graph from the datasheet.

As can be seen from the figure, both the measurement input as well as the reference input are differential types. Furthermore, a calibration engine can be seen, which

[19] those references are available from the outside in special testmodes only.

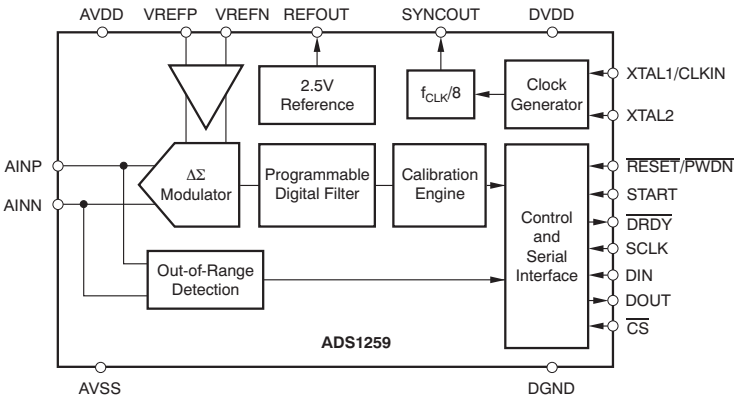


Figure 3.51: ADS1259 Industrial, 14 kSPS, 24 bit Analog-to-Digital Converter [Tex11]

allows to calibrate for offset and full scale errors, provided that both signals can be applied to the inputs. This chip also features inherent 50 Hz and 60 Hz noise suppression for its low speed conversation types. All of the above is necessary to achieve the high specified accuracy values. For example, the offset error is stated as ±250 µV and the Gain error as ±0.05 % before calibration, and as ±1 µV and ±0.0002 % afterwards.

The mulitplexed input stage for the ADC was required to feed the different signals to the ADC, as it only provides a single differential input. Figure 3.52 shows a conceptual graph of the ADC with the created mux input structure.

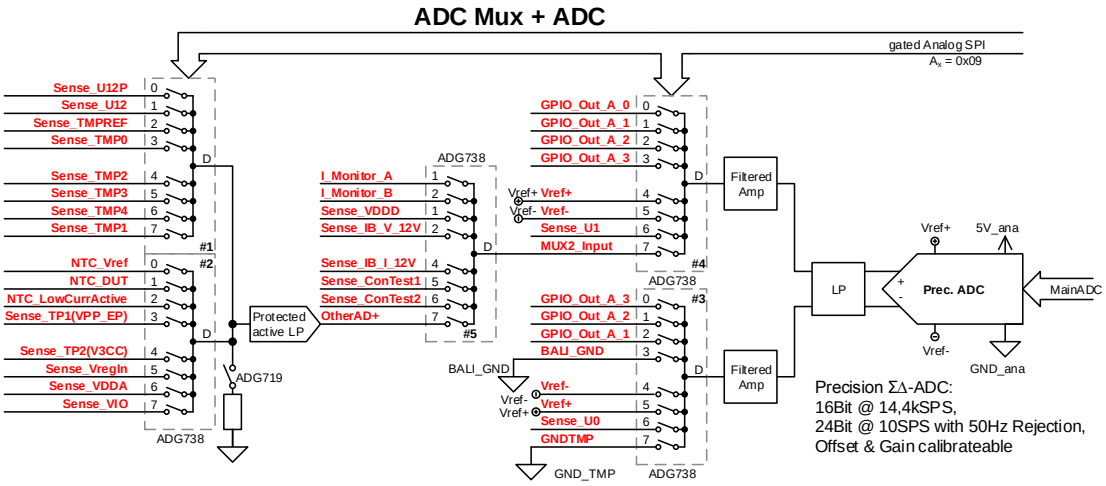


Figure 3.52: Precision ADC with multiplexer and filter stage

The shown switches are all electronic, either of the ADG738 or ADG719 type. These devices only differ in the count of switches, and control logic but feature same

electrical properties. Whilst the 8 switch devices are controlled via a daisychained SPI bus[20], the single switch variant is controlled directly via a logic signal. The parameters of these parts are exceptional, at least for the needs of the signals during this thesis project. They provide a bandwidth of 200 MHz, a maximum leakage current of ±0.25 nA, a maximum parasitic capacitance of 27 pF, Off-state isolation of 87 dB at 1 MHz and switching times of under 10 ns.

The only disadvantage in this application is the On-resistance of typically 2.5 Ω. In the worst case it can reach values of 4 Ω, with a flatness over the voltage range of 1.2 Ω and channel to channel mismatch of 0.4 Ω. If one takes the ADC's input resistance (500 kΩ) into account, these resistors form a parasitic voltage divider (if the filtered OpAmp is bypassed). Although constant values can be eliminated with the calibration routine the mismatch and flatness values dictate the bottom line for accuracy. So the error factor results in

$$\text{Error}_{uncalibrated} = \frac{2R_{max}}{R_{in}+2R_{max}} = \frac{2{\cdot}4\,\Omega}{500\,\text{k}\Omega+2{\cdot}4\,\Omega} = 16\,\text{ppm}$$

$$\text{Error}_{flattnes} = \frac{2R_{flat}}{R_{in}+2R_{flat}} = \frac{2{\cdot}1.2\,\Omega}{500\,\text{k}\Omega+2{\cdot}1.2\,\Omega} = 4.8\,\text{ppm}$$

$$\text{Error}_{mismatch} = \frac{2R_{mm}}{R_{in}+2R_{mm}} = \frac{2{\cdot}0.4\,\Omega}{500\,\text{k}\Omega+2{\cdot}0.4\,\Omega} = 1.6\,\text{ppm}$$

In the calibrated case this corresponds to around 19 ENOB (Effective Number of Bits) or 8 µV for a full scale value. Of course this is only the additional error from the filter, and does not contain any other error source in the signal chain like from OpAmps. It is also only valid for the first row of the multiplexers input, as the others even add more series resistance. Furthermore, there has to be a possibility to bring the reference voltage, as well as a clean 0 V signal to this stage, so that the calibration routine can be executed. Therefore, the signals that require the most accuracy, are the ones that need to be connected to the first multiplexer stage, closest to the ADC's input.

The leftmost multiplexer stage in figure 3.52 is buffered by a fast filtered amplifier, designed in such a way that its dynamic accuracy is still sufficient for NTC-waveforms. More information about the different signals will be given in the dedicated NTC-measurement section on page 136.

The filtered amplifiers located between the ADC's passive filter and the multiplexer, are active filters that are currently not populated but bypassed. All board signals that are brought to the ADC section are bandwidth-limited by dedicated filtered amplifiers, so the additional active filter should not be needed. It is rather meant as a backup, in case that the self-zeroing amplifiers, used in some precision filters, might cause problems, due to their switching noise. The needed OpAmps for the active filters in front of the ADC would have to be fast and accurate enough to not alter the NTC-measurement signals and the DC-precision of the ADC at

[20] The numbers in the figure with the preceding # sign indicate the number in the SPI daisy chain

the same time. This requirement is hard to reach with standard parts, but as these filtered amplifiers are between the first multiplexer section and the ADC, their offsets errors could possibly even be calibrated for, as long as their common mode errors are low, which widens the list of possible candidates again.

The circuit of this filtered amplifier can be seen in figure 3.53. It was built in a very versatile way, and is used as a building block at various points throughout the board.

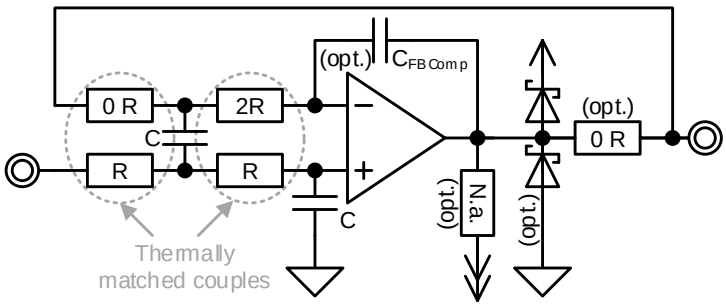


Figure 3.53: Versatile configureable Sallen-Key low pass OpAmp circuit

Therefore, the same schematic and layout could be re-used for every task needed on this board by simply using different parts. This also allows to easily make later changes to the parts used, as the verification board had to work on the first run, preventing bigger changes. Therefore, only OpAmps available in standard footprints and pinouts were used. For precision DC signals, the AD8638/AD8639 (see page 65) self-zeroing OpAmps were used, as they feature little switching noise and only 75 pA input leakage current. For the fast NTC signals, the OPA350 was used that will be discussed on page 133 in more detail.

The first thing to mention about this circuit, is that it basically is a modified Sallen-Key [TS09, page 812] low pass filter. Depending on the populated parts, a protection to the OpAmp is possible if needed. The input side is simply protected by the series resistor and the internal clamping diodes of the OpAmp. Additional clamping diodes at the inputs were avoided, as their capacitance and leakage currents would easily destroy required accuracies. As the output normally has to be low resistive, the 0 Ω resistor can be exchanged to the maximum tolerable value for the actual application. The additional Schottky clamping diodes at the output assists the internal low power diodes. The feedback loop was closed behind the diode and the resistor to allow the OpAmp to compensate for possible deviations. An additional feedback capacitor allows improved feedback, in case of instabilities due to, e.g., capacitive loads. To allow lowest DC offsets, the parts at the inputs were made very symmetric both in schematic and layout. This allows for thermoelectric potentials to cancel out as well as for voltages induced by leakage current.[21]

[21] Highest ohmic sources, which are also amplified on this board, use special amplifier types

Also the supply of the OpAmp was made changeable via solderjumpers. This allows usage of dual and single supply types. To counterbalance the effect of the increased supply track lengths, each OpAmp is supported with its own shortest connected decoupling capacitors. In the case of a single supply OpAmp, the normally not assembled (n.a.) resistor can be used to allow the output stage to truly reach 0 V by building a bias to the negative supply rail.

Trimable precision voltage reference

As the ADC's internal voltage reference accuracy is not sufficient for the needs on the baseboard, an external type was needed. With the HPBS design of this thesis a trimable voltage reference had already been built and tested (see page 69). Due to its excellent results it was reused for the baseboard, although with slight further improvements.

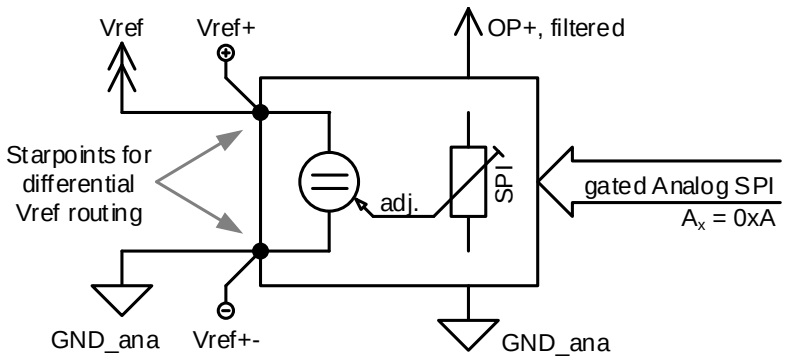


Figure 3.54: Trimmable precision voltage reference; Nominal 5.0000 V, Trimmrange = ±10 mV, Trimmstep ≈ 20 µV to 30 µV

Test measurements on the HPBS revealed that, although the design is sufficiently stable over the tested temperature range of ±20 °C, it can be sensitive to temperature gradients. Since such gradients are dangerous for any low voltage analog measurement, it was decided to cover the ADC, the multiplexer and the reference with a solder-able metal shielding box (see figure 3.72), that prevents gradients from unwanted airflow. Combined with high copper usage on multiple PCB layers, stitched together by vias, the high thermal conductivity of the metal shielding helps to minimize remaining gradients effectively. Besides this thermal aspect, the metal box also shields against any unwanted voltage noise. Along this and other minor layout improvements, a temperature sensing NTC was placed close to the voltage reference IC, to allow detection of remaining temperature changes.

with extremely minimal input leakage currents to avoid offsets due to the resulting input resistance imbalance on the + and - inputs.

General purpose DAC

The general purpose DAC (figure 3.55) is used for the creation of some general

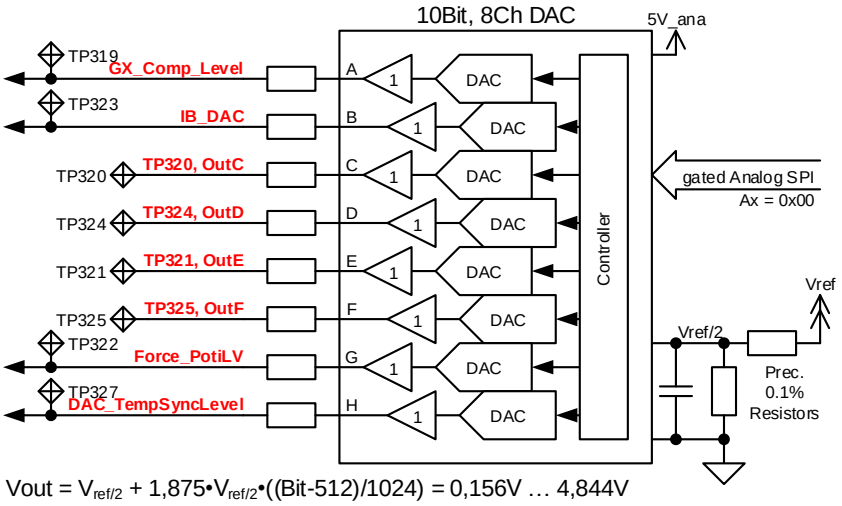


Figure 3.55: General purpose, low precision DAC

coarse analog voltages, like for set-points of voltage comparators. It features 8 buffered outputs than can be varied from 0.156 V to 4.84 V with a resolution of 10 bit [Ana98]. The internal reference is extremely coarse, and was therefore replaced by a connection to the board's 5 V reference. As the DAC needs 2.5 V at its buffered reference input, a voltage divider was used. Using reasonable cheap 0.1 % 10 kΩ standard resistors was already sufficient for this general purpose part. Even with the considered maximum input leakage current of 1 µA over temperature the original accuracy of 8 % was easily improved. Especially since the typical value at room temperature is around 1 nA.

Current sense amplifier

Figure 3.56 shows the onboard current sense amplifier, which was re-used from a previous verification environment. It is built around an AD8227 instrumentation amplifier, that allows for simple gain selection and input ranges up to ±40 V, although this is beyond its own supply voltage. However, once the circuit is used beyond its own supply limit, the normally extremely low input current rises from the nA range up to ±500 µA. In general, this circuit is meant to be used for rough tracking of current values of for example the DUT's low voltage supply during automated measurements. So it is more about plausibility checks than accuracy. The circuit consists of two amplifiers with predefined settings and sensing resistors that can be used for different ranges. There are multiple connection points and solder jumpers to allow flexibility. There is even a possibility to combine both amplifiers by using a diode for highest range flexibility, although this reduces

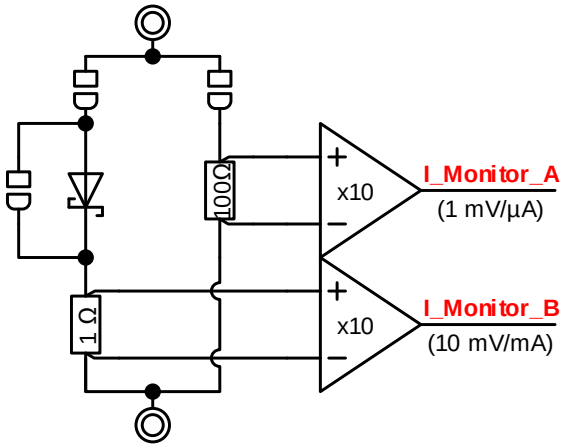


Figure 3.56: Configurable current sense amplifier

accuracy on both ends once one of the amplifiers reaches its minimum or maximum sense limit.

Gated and filtered digital communication

To allow the high flexibility of the analog section, many digital control lines and buses had to be routed into an area, where high accuracy is needed and only low disturbance levels are allowed. It was therefore necessary to provide a communication concept that reduces cross coupling to a minimum. Once again a balance between a widespread single bus, coupling noise in the analog area, and a non routeable high number of separate buses had to be found.

The realized solution (figure 3.57) uses a modified version of the gating approach presented on page 122.

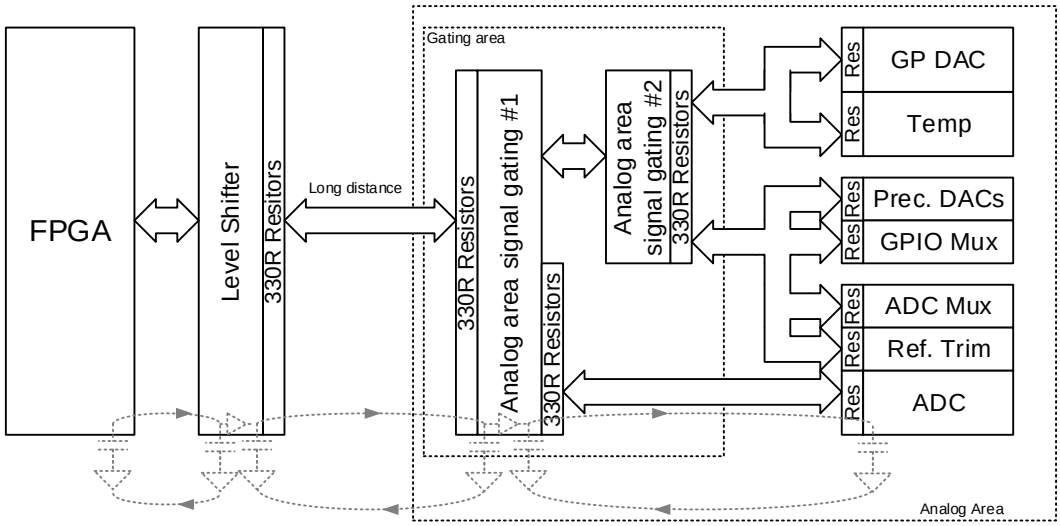


Figure 3.57: Analog area SPI gating

In this version series resistors were used on the digital buses and control signals to limit the rise and fall times, and so the capacitive coupling of fast transients to a minimum. The resistors were calculated using estimated values for the parasitic trace and input capacitances and a data rate of 1 MBps. All parts in the gating circuitry are manufactured in CMOS technology, which offers very low input currents. This helps to keep static voltage drops across the series resistors low and therefore the safety margin high. Furthermore, the logic level thresholds of CMOS are also better suited for this application, than for example that of TTL devices.

These gating devices were placed close to the start-point-area that connects the analog and the digital GND planes, as can be seen in figure 3.69 on page 147. Furthermore, buffers were added at this section for all the non SPI digital signals that were not already covered by the gating concept. All these devices are powered by a filtered and heavily capacitively decoupled supply that originates from the analog supply, to ensure that also static digital levels are quiet. This ensures that all the control signals entering the analog area have lowest noise levels. As these devices also feature very little static supply currents, hardly any impact on the analog ground level is expected.

Furthermore, areas were grouped according to accuracy and similar usage, to reduce the routing effort for the buses. As the baseboards ADC has the highest accuracy requirements it is the only device in the analog section that has a dedicated bus on its own. This ensures every other bus communication in the analog section is completely quiet once the ADC conversion is running. The ADC bus itself is also carefully routed on an outer layer with shielding lines to the side. These lines are stitched with vias to the ground plane underneath that is kept free of interruptions. This ensures a shortest possible HF current return path for the communication, away from the sensitive analog lines.

The next communication group contains devices that are connected to highly sensitive signals that do not need communication during ADC measurements, but probably before or after. For example the ADC-multiplexer needs to be set up sufficient time before triggering the ADC, to allow the analog input signal to settle. As this group of communication lines is separated by gating from the rest of the board, it can be kept completely quiet during the actual conversion process.

The third group consists of devices that have modest accuracy requirements, but may require faster changes. This bus is routed at the outer edge of the analog section, away from the sensitive core parts.

Now that the core parts of the analog section are known, circuits that use them will be described, starting with the GPIO interface.

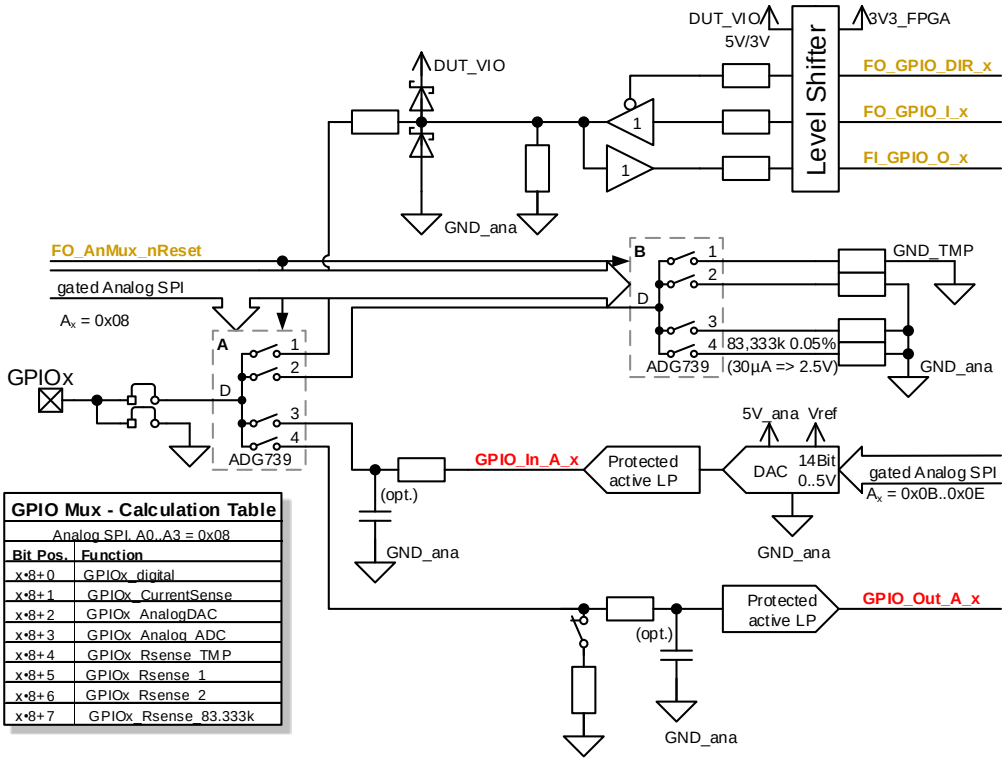
3.3.7 GPIO interface

The TLE8000QK's GPIO interface is very versatile and can be used as digital input/output or even as analog input. In the analog mode the GPIO pins are used as pairs to allow differential voltage measurements. Each pair can independently be configured to use the digital or analog mode. Internally both pairs are linked to the 10 bit SADC, although with different FSR settings. On the GPIO0-GPIO1 pair the FSR setting is 2.5 V whereas GPIO2-GPIO3 uses 5 V. This results in an LSB of around 2.44 mV or 4.88 mV respectively.

In the digital mode each line is independently configurable as in- or output. Furthermore, the voltage levels are defined externally for the whole group via the VIO pin voltage.

Furthermore, there are special testmodes, not available to any customer, which allow internal highest precision signals to be routed out of the IC's GPIO interface for verification purposes.

To allow verification of the IC's GPIO pins, the baseboard also needs to provide a versatile circuitry as a counterpart. Figure 3.58 shows the concept that is realized for each GPIO pin to allow full analog and digital IO configuration.



GPIO Mux - Calculation Table	
Analog SPI, A0..A3 = 0x08	
Bit Pos.	Function
x•8+0	GPIOx_digital
x•8+1	GPIOx_CurrentSense
x•8+2	GPIOx_AnalogDAC
x•8+3	GPIOx_Analog_ADC
x•8+4	GPIOx_Rsense_TMP
x•8+5	GPIOx_Rsense_1
x•8+6	GPIOx_Rsense_2
x•8+7	GPIOx_Rsense_83.333k

Figure 3.58: GPIO multipurpose interface, present on each GPIO pin

The switch located closest to the DUT's pin is an ADG739 type, which basically is a derivative of the ADG738 that was used at the ADC muxer. It comes with 2x4

combined switches instead of the 1x8 in the ADG738 and features nearly the same properties which makes it perfectly suited for the purposes at the GPIO interface.

Digital GPIO interface section

The upper part of figure 3.58 shows the digital interface to the FPGA. It uses logic buffers with an output disable feature, to allow bidirectional digital communication. These buffers are supplied by either 5 V or 3.3 V. To allow FPGA-DUT communication with the different supplies, fast 74LVC8T245 type level-shifters are in use in front of these buffers.

Analog GPIO interface section

The remaining sections are for analog measurements and provide current and voltage measurement capabilities as well as the creation of analog signals.

The DAC used for these signals is of the same type as on the HPBS design, although here the cheaper variant with only 14 bit resolution is in use. This still allows an LSB of 0.31 mV which is 8 times higher than the LSB of the SADC. As this DAC is unbuffered one external buffer is needed per device. Like for most buffers on this board, the versatile configurable active filter circuit from page 127 was used for this purpose. This also keeps the used bandwidth and therefore noise levels at a minimum.

The active filter on the bottom of figure 3.58 allows to check the accuracy of the applied DAC voltages. Furthermore, it is needed to buffer chip internal testmode signals to an appropriate impedance level for the board's ADC.

The measurement of chip internal reference currents is also possible in testmode with this section. For this function precision resistors at the second multiplexer can be activated. To avoid uncontrolled oscillations, once the filter is disconnected from the GPIO pin, a pull-down resistor is available. This resistor can be disconnected to prevent accuracy deviations on high impedance sources.

3.3.8 NTC Simulation

The TLE8000QK's TMP interface is designed to measure the resistance of external NTC sensors. It uses current sources to create a voltage drop across the external NTCs. This drop is then measured by its internal SAR-ADC. The base reference for these current sources can either be derived from a fixed internal value, or set with an external precision resistor. This resistor has to be connected to the TMPREF pin, where the chip applies accurate 2.5 V to it, to derive the intended reference current. To allow a wide input range, as needed for the measurement of non-linear NTCs, the chip switches between 4 current sources that copy the

reference current with different scaling factors to the output. Depending on the size of the resistance to measure, the best fitting current source is selected by an internal state machine that decides based on the last measurement result. The scaling factors of the available current sources are 8, 4, 1 or 0.25. Once the measurement is finished, the SAR-ADC readout and the used scaling factor are stored together in the corresponding "Temp Result" registers of the IC.

All this allows the customer to adopt the chip to a wide range of usable NTCs. Table 3.12 shows the 4 ranges over some possible configuration examples, where the 40 µA column is the standard for the internal reference and the 33 kΩ and 100 kΩ columns represent the maximum allowed external reference resistors.

	Increasing Reference Resistance (Decreasing Reference Current)→					
	Reference:	33k→75,8 µA	60 kΩ-0,1%	60 kΩ→41.7 µA	60 kΩ+0,1%	40 µA	100 kΩ →25 µA
	Detected as short cicuit						
← Increasing Resistance	Lower End	129 Ω	234 Ω	234 Ω	235 Ω	244 Ω	391 Ω
	Range 1	↕	↕	↕	↕	↕	↕
	Higher End	4093 Ω	7434 Ω	7441 Ω	7449 Ω	7751 Ω	12402 Ω
	Lower End	3964 Ω	7200 Ω	7207 Ω	7214 Ω	7507 Ω	12012 Ω
	Range 2	↕	↕	↕	↕	↕	↕
	Higher End	8186 Ω	14868 Ω	14883 Ω	14898 Ω	15503 Ω	24805 Ω
	Lower End	7928 Ω	14400 Ω	14414 Ω	14428 Ω	15015 Ω	24023 Ω
	Range 3	↕	↕	↕	↕	↕	↕
	Higher End	32742 Ω	59472 Ω	59531 Ω	59591 Ω	62012 Ω	99219 Ω
	Lower End	31711 Ω	57599 Ω	57656 Ω	57714 Ω	60059 Ω	96094 Ω
	Range 4	↕	↕	↕	↕	↕	↕
	Higher End	216563 Ω	393356 Ω	393750 Ω	394144 Ω	410156 Ω	656250 Ω
	Detected as open load						

Table 3.12: TLE8000QK temperature ranges versus reference currents

To allow proper verification of, e.g., correct measurement range selection or linearity, a simulated NTC resistor would be the device of choice. However, due to this wide covered resistance ranges, it is nearly impossible to provide a single solution with adequate resolution and accuracy over the whole area. After various concept iterations a set of solutions was found that can be used to independently cover the relevant verification topics.

The basic idea is to use multiple simulation approaches, each suited best for particular verification topics. Since all temperature channels are built identically inside the chip it is feasible to use different approaches for different pins. However, it is still left possible to exchange the simulation approaches using external cabling, if uncertainties or specific setup requests would arise.

Preceding accuracy considerations

As the 10 bit SAR-ADC is used for the NTC resistor measurements, the resolution corresponds to 1024 values or 977 ppm. The external resistors used for the

verification must have a better accuracy than the IC. Preferably it should be even better than its resolution, as this would mean that measurement results should be equally reproducible over all boards. However, in order to have accuracies superior to the chip's resolution, resistors rated even better than a 0.05 % class with lowest thermal coefficients would be needed, which are extremely expensive. On the other hand, resistors with a rating of 0.05 % and a temperature rating of 10 ppm/°C are still in a feasible price range.

Assuming a worst case ±20 °C temperature rise on the board area near the resistors and a worst case deviation from the rated value would result in an inaccuracy of 900 ppm, which compares to around 1 LSB of deviation in a worst case scenario. In general the varying resulting LSB value per range in Ω should also be considered, as can be seen in table 3.13.

	Decreasing Reference Current)→				
	Reference:	33 kΩ	50 µA	40 µA(62.5 kΩ)	100 kΩ
LSB [Ω]	Range 1	4,0 Ω	6,1 Ω	7,6 Ω	12,2 Ω
	Range 2	8,1 Ω	8,1 Ω	15,3 Ω	24,4 Ω
	Range 3	32,2 Ω	32,2 Ω	61,0 Ω	97,7 Ω
	Range 4	257,8 Ω	257,8 Ω	488,3 Ω	781,3 Ω

Table 3.13: Resulting temperature resolution in Ω for each measurement range

TEMPREF - Reference selection possibilities

The first pin considered here in detail is TEMPREF. For verification purposes it has to be possible to provide the allowed extreme values as well as a typical one that creates a current near the internal reference for comparison purposes. Also (near) short-circuit or open-load conditions should be possible to simulate. Furthermore, various values for capacitive decoupling have to be possible as well. Figure 3.59 shows the realized concept for this pin.

The connections to the various passive devices can be established via the already presented ADG738 SPI controlled matrix switch. Its low parasitics allow it to be used to connect the high precision resistors. For example its worst case leakage current of 1 nA corresponds to a 100 µV error at the highest 100 kΩ resistor. On the other extreme, the worst case value of 5 Ω for the on-resistance correspond to 152 ppm at the 33 kΩ resistor. However, although the device is rated for 200 MHz and the typical value for R-on is around 1.2 Ω, additional capacitor footprints are located directly on the DUT-Board, close to the DUT, to provide the possibility for improved capacitor placement if necessary.

For comparability measurements of the NTC sensing capabilities, a rather complex approach was necessary, to be able to nail down error sources like accuracy loss due to insufficient settling times. As the measurements are done autonomously

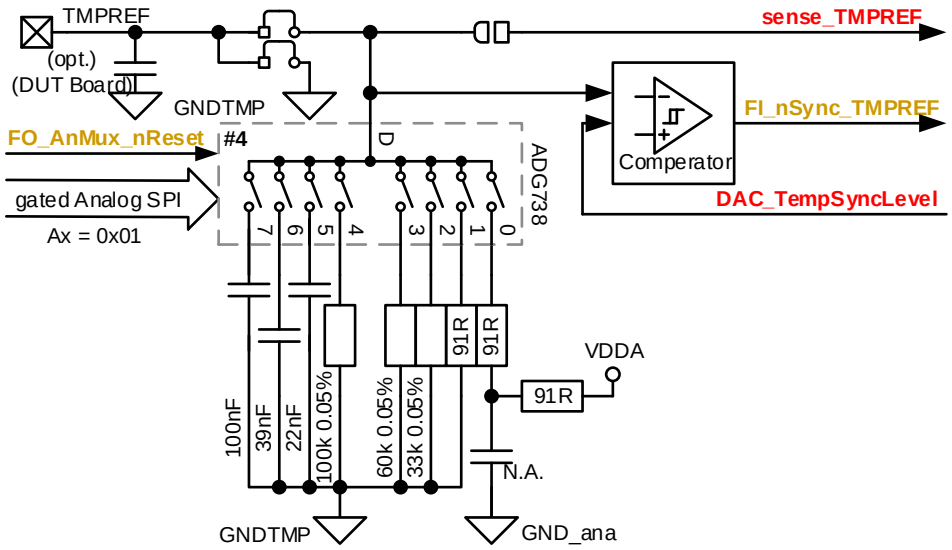


Figure 3.59: TEMPREF pin - Reference selection possibilities

by the IC, supervision has to be locked to the DUT's timing. The idea is to synchronize the boards ADC to the exact sampling times of the NTC measurement, to verify sufficient signal settling.

Reaching this synchronism requires short sampling times of around 100 µs or less, which can easily be achieved with the 14.4 kSps of the boards ADC. Also the required buffer, which is located in the analog multiplexer section (figure 3.52, page 125) has to be sufficiently fast and accurate, although the timing is not as critical as for the ADC, as the input signal is present around 1 ms before the ADC's measurement triggers. However, as the input signal waveform is a rounded rectangle slowly matching the final value more and more accurately, the OpAmp has to match the accuracy down to the 977 ppm, which is around 60 dB. Therefore, the required OpAmp has to have an open loop gain reserve of at least 60 dB in the 10 kHz range, and an offset failure of less than 1 mV.

After a search over all major vendors the OPA350 was found to be the device of choice. It has a worst case offset of 1 mV and is unity gain stable while providing 38 MHz of bandwidth. This results in a corner frequency of 38 kHz for the desired 60 dB gain reserve. All the other important parameters like closed loop output impedance, input currents, CMRR, etc. are also exceptional for this application.

TMP4 - Precision and synchronization

To allow synchronization, both the TEMPREF and the TMP4 pin are supervised with an additional comparator, as can be seen in figure 3.60. The comparator is built as inverting Schmitt-trigger, which allows to have the hysteresis backlash of the output come to the inverting input instead of the true comparison non-inverting input, which has to be left unloaded.

The resistor was chosen with 2.7 kΩ to always force the internal measurement into range number 1 with the highest output current, regardless of the reference current setting.

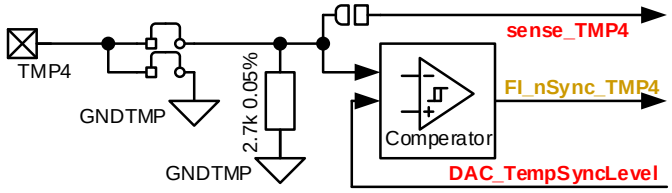


Figure 3.60: TMP4 unbiased precision resistor with sync generation

TMP3, TMP2 - External NTC and manual resistor simulation

The realized circuits for TMP4, TMP3 and TMP2 (figure 3.61) are all basic passive variants, to provide manual alternatives to the automated measurement setups. TMP2 simply provides a standard connector for an external real NTC, with the possibility of ADC supervision. TMP3 provides a chain of precision potentiometers with 10 turns each. By the use of simple jumpers, each variable resistor can be quickly bypassed and capacitors added.

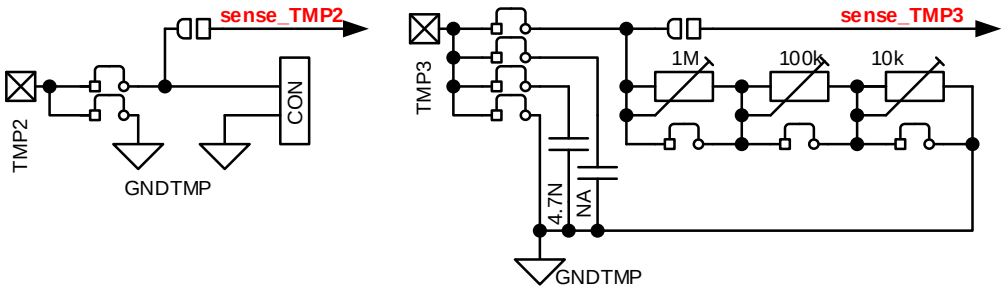


Figure 3.61: TMP2 external NTC; TMP3 manual potentiometers

TMP1 - Enhanced digital potentiometer

The concept for the TMP1 pin uses a very flexible enhanced digital potentiometer as can be seen in figure 3.62. In contrast to most other circuits on the baseboard, the idea focuses more on resolution than on accuracy. This is based on the fact that at the time this project was conducted, no simple electronic resistors were available, that could even closely deliver the required accuracy. Furthermore, construction of a fully configurable precision resistor matrix would have been beyond any feasible effort, due to the high resistor range needed to cover. But even with the lower available absolute accuracy, stability combined with high resolution allows to do extensive automated verification test on correctness of the internal state machine.

The typical accuracy of programmable resistors available at the time was around 20 % with often just 256 steps. Extensive search revealed that a few new parts

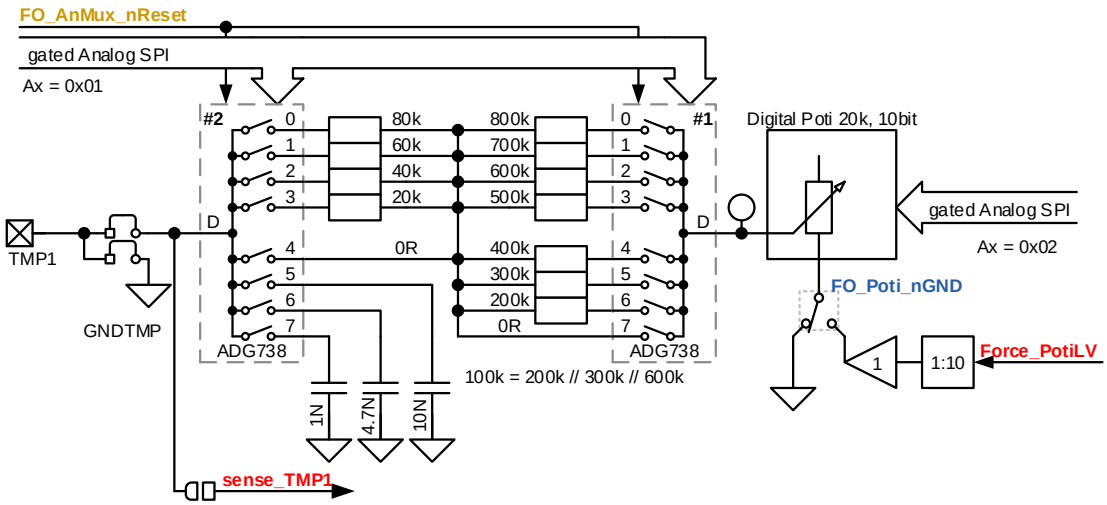


Figure 3.62: TMP1 enhanced digital potentiometer allowing values between 0 Ω and 800 kΩ with 19.5 Ω resolution and around 1 % accuracy

called "Digital Rheostat" were just made available from Analog Devices, providing 1024 different resistor values with, for on chip resistors, astonishing precise 1 % of absolute accuracy. The device of choice is an AD5270 in the 20 kΩ variant, which is the smallest of this series. Comparing the device's LSB value of around 19.5 Ω with table 3.13 one can see, that this is still higher than the LSB of the lowest DUT's measurement range, but at least always lower for the ranges 3 and 4. In the second range the devices LSB nearly matches those of the DUT, for the lower reference current values.

However, as these ranges require higher maximum resistance than the electronic resistor can provide on its own, a simple range extension was added, which uses a combination of standard 1 % resistors[22,23] and matrix switches. With this extended range, resistor values between 0 Ω and 800 kΩ can be reached with a 19.5 Ω resolution. Of course the user has to be aware that, especially in higher resistive regions, the absolute accuracy is worse than 1 % due to leakage currents[24].

To allow an even finer setting point for the ranges 1 and 2, the base-point-potential of the rheostat can be shifted. This voltage shift is created by the general purpose DAC, scaled down by a factor of 1:10 and then buffered with the standard active lowpass buffer, populated with a fast OPA350. Although this does not change the resistance, it alters the reading of the DUT's SADC that is used for the measurement. This allows to make fine changes at the range borders to verify the correct operation of the DUT's automatic range selection.

[22] For simplicity, only resulting resistor values are shown in figure 3.62 although most values are built of two standard values.

[23] The 100 kΩ value can be reached by parallel activation of 200 kΩ, 300 kΩ and 600 kΩ

[24] The maximum input leakage current of the digital rheostat is around 50 nA over temperature, which can produce non negligible offsets in the highest ohmic regions.

TMP0 - Precision resistors

The circuit for TMP0 (figure 3.63) focuses on accuracy verification again. It provides the highly accurate 0.05 % resistors that were selected in such a way, that each value forces the DUT into a particular measurement range. There is however an exception for range 2, as the DUT's ranges were designed to get best accuracies with the non-linear NTC resistors. This results in the fact, that no single resistor value exists that will always force the state machine to this range, at least not for all possible reference current values. Therefore, two precision resistors (7.68 kΩ and 13 kΩ) were used that have to be chosen according to the currently used reference value to ensure a forcing into range 2.

To allow highest precision with minimal parasitics, relays were used for this circuit instead of ADG electronic switches. Especially for the low value resistors, the worst case on resistance of up to 4 Ω of the ADG switches would already have compromised the accuracy, whereas the 50 mΩ of the IM26G relay leaves enough headroom for wiring resistances.

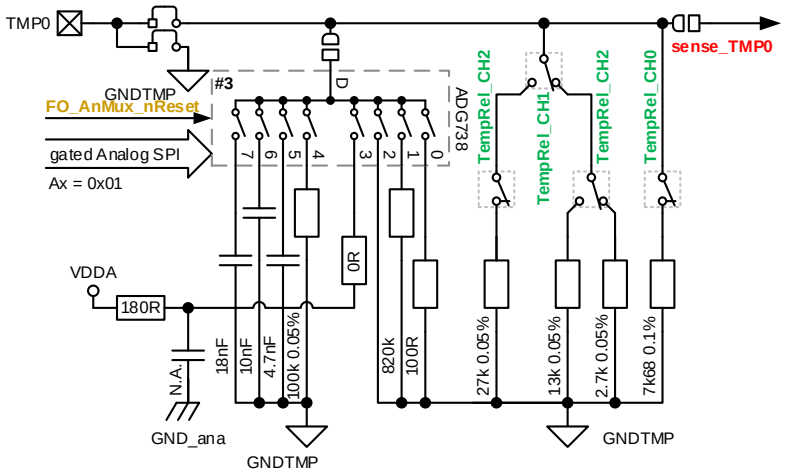


Figure 3.63: TMP0 - switchable precision resistors

3.3.9 Onboard measurement relay multiplexer and relay control

As already mentioned in section 3.1.1.2 an alternative to external voltage multiplexers was also implemented on the verification baseboard (figure 3.64). The idea is, that only a single precision multimeter shall be needed together with the verification board's differential multiplexer to measure all battery cell voltages. To ensure proper setup and board calibration the multiplexer also allows measurement of the board's reference voltage, the total stack voltage and also provides an additional interface for a current sensing resistor.

For versatility reasons, the relays that measure the battery cells are not directly routed to the voltages present on the baseboard but to the voltage measurement connector illustrated in figure 3.1 and discussed on page 43. The connection to

the actual measurement point is realized with a short 1:1 cable[25]. This allows the multiplexer to measure the baseboard, directly on a DUT-Board, or even on an application board connected to a real battery.

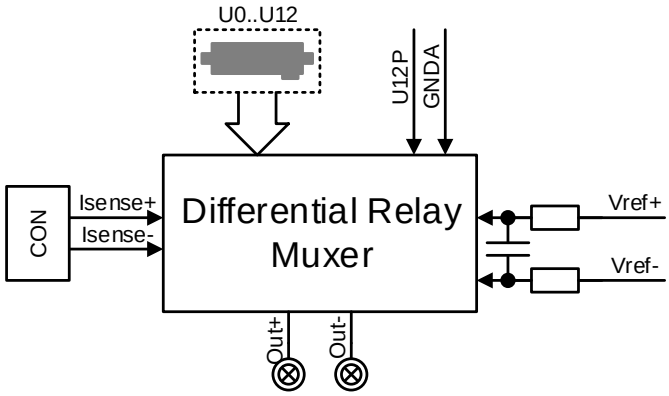


Figure 3.64: Differential 15 channel relay multiplexer

Relay control

Although the measurement multiplexer uses 15 relays, this is only a fraction of the total 60 relays used throughout the board. To control this huge number of relays, Infineon's TLE7240 or so called SPIDER[26] IC was used. This device is an intelligent, SPI controlled, 8-channel low-side switch, intended as relay driver. It is daisy-chainable, features on-chip diagnostic and protection functions as well as the ability to actively clamp the switch-off energy of inductive loads. This means that freewheeling diodes can be omitted when driving inductive loads like small signal relays. Therefore, when the relay turns off and the interrupted current causes an induced voltage, the driver acts similar to a zener diode and turns on again once the induced reverse voltage reaches 41 V. As a result the magnetic field inside the relay decreases rapidly, which allows faster switching times compared to standard diode based freewheeling approaches [Inf11].

To keep overall current consumption at a minimum, ultra-sensitive 12 V IM26 relay types were used across the board, except for the relay matrix (page 107) of the IC's high voltage power supply that uses IM06 types. These result in a maximum current of

$$I_{tot} = 24\frac{12\,\mathrm{V}}{1029\,\Omega} + 36\frac{12\,\mathrm{V}}{2880\,\Omega} = 430\,\mathrm{mA}$$

which is nearly 4 times less compared to the $\sim 1.7\,\mathrm{A}$ needed for the standard 5 V types. Furthermore, the relay supply and return ground path were routed on dedicated tracks, preventing the static return currents from entering sensitive analog regions. To avoid large loops for the return currents of the digital control signals, they were routed as a dedicated bus with their according supply and ground paths underneath or to the sides.

[25] The 1:1 cable for the multiplexer is a Samtec TFSD-07-28-G type
[26] SPIDER = SPI relay DrivER

3.3.10 Board identification system

One of the main reasons for the need of the various automation-, setup-detection and measurement options of the verification board, was to provide a reliable way of saving and storing measurement setups to improve repeatability compared to the previous X11 board. Therefore, most of the remaining parts that still might need to be adjusted for various measurements, like solder jumpers, decoupling capacitors or balancing transformers were put onto sub-prints like the DUT-Board, to avoid modifications to the baseboard. As a result different sets of, for example, DUT-Boards may be built over time to fit different needs.

It is therefore very important to provide a safe way of tracking each particular combination of boards that was used for a verification task. This also allows to trace back which measurements were conducted with which setup. As a result, detection of problems like degenerated contacts or parts even allows to track down possible influences on previous measurement setups. Each board is therefore equipped with a chip-based unique identification number.

Figure 3.65 shows the basic identification bus that was implemented on the baseboard. To allow unique identification and low wiring effort, DS2431 EEproms

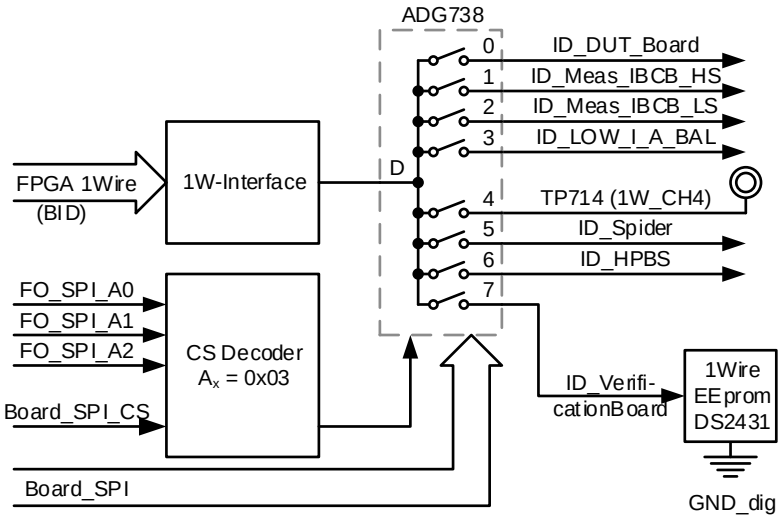


Figure 3.65: Identification concept using 1-Wire eeproms devices

with an 1-Wire bus system were chosen as ID devices. These devices power themselves "parasitically" from the single bus-wire. Each device contains a unique factory programmed and unalterable 64 Bit identification number that is needed for addressing, as the bus normally allows a connection of multiple devices to the same bus wire. Additionally each device offers 1024 Bits of user programmable non-volatile data memory, allowing storage of, for example, 128 ASCII text characters, providing space for short descriptions. Although 1 single data/supply wire would have been sufficient for this bus, a multiplexer was used to allow routing to dedicated board positions, to avoid potential misinterpretations of setups.

Overall this 1-Wire devices offer a very flexible and reliable way of providing an ID system with minimal hardware effort.

3.3.11 Digital board control signals and signal protection

While figures 3.47 (page 119) and 3.57 (page 130) concentrated on the communication path between the FPGA and the DUT, or the FPGA and the analog section, figure 3.66 now shows the remaining signals that are necessary to control the board's hardware that was presented so far.

As was explained on page 111, a color scheme was used to indicate the kind of the signal used throughout the schematic concept diagrams of the baseboard. Figure 3.66 now shows where these control signals originate. The only exception are the red analog signals that always originate in the analog section. Of course, as mentioned earlier, all digital control signals that are used inside the analog area, additionally also have to pass the gating area (page 130) for proper noise filtering.

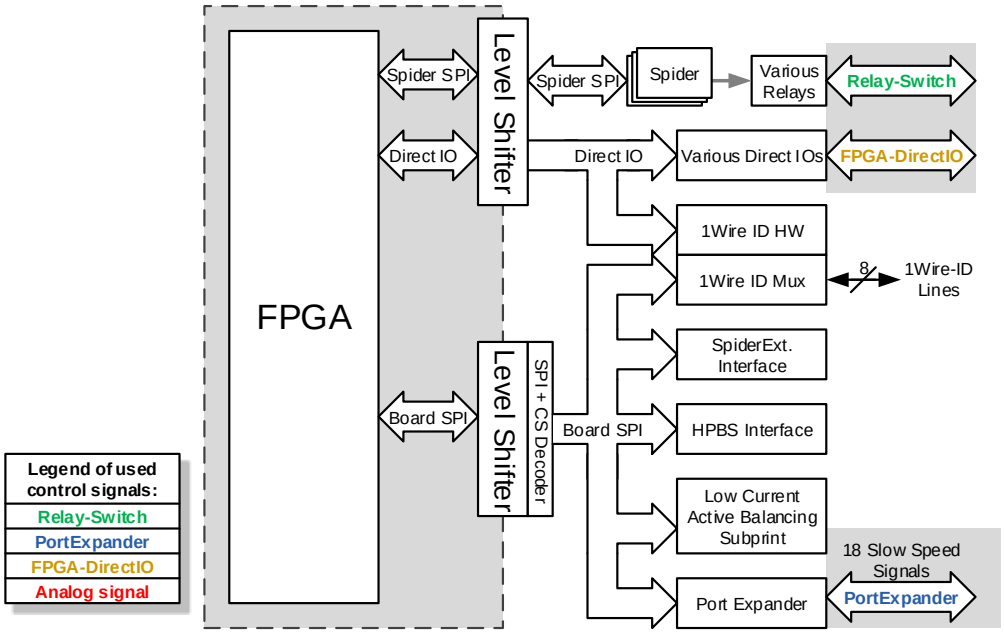


Figure 3.66: Digital Board control signal flow

The majority of the signals in figure 3.66 come from the various board circuitries and are directly connected to the FPGA through level-shifters. Then there is a so called Board-SPI bus, which connects to various board parts and connectors for external equipment like the HPBS. As these parts are all located in non-critical board areas, the expense for SPI gating could be omitted here and only separate chip select lines had to be routed.

One part connected to this bus is the MAX7301, a so called Port I/O Expander. This device provides additional input and output pins to the FPGA, but of course,

with reduced speed performance compared to the direct FPGA connection. As a result, this device was often used for slow speed tasks like sensing the connection state of, e.g., the battery simulator interface (see figure 3.41 on page 109), which typically only changes once per setup.

The relay driver is different, as it actually doesn't provide digital signals but relay driver output stages. The relay controlling SPIDER blocks are daisy-chained and placed across the board on locations where most relays can be reached best.

3.3.11.1 Signal Protection

The FPGA module is a very powerful but also expensive part. It was therefore desired to have a protection concept that protects it from board failures as well as defective DUTs. As can be seen in the figures 3.47, 3.57 and 3.66, all the signals connected to the FPGA pass through level-shifters. A protection technique applied to these level-shifters therefore effectively builds a protection barrier between the FPGA and the rest of the board. This also allows to use layout replication techniques with the level-shifters ICs to keep the effort minimal.

Figure 3.67 depicts the protection concept used. It is a standard concept that can, e.g., be found in [Wil12, page 251] combined with an active clamping circuit on the voltage supply. It uses fast BAT54 clamping diodes that redirect signal voltages levels that are outside the supply voltage range towards the supply. To avoid excessive currents, series resistors are used to limit the current.

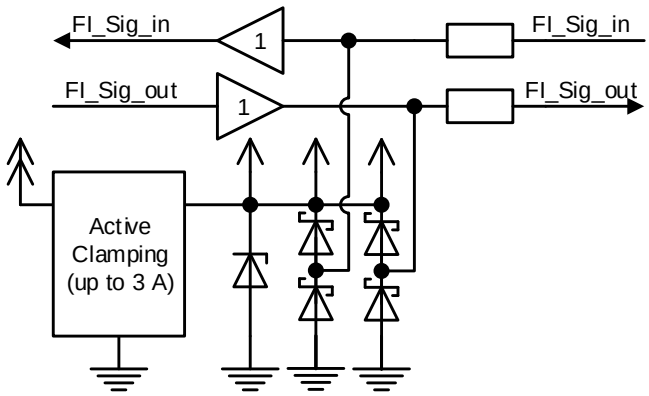


Figure 3.67: Protection concept with active clamping on the voltage supply

The maximum input voltage of the 74LVC8T245 level-shifter ranges from $-0.5\,\mathrm{V}$ to $6.5\,\mathrm{V}$ regardless of the supply voltage, as long as a maximum of $50\,\mathrm{mA}$ allowed clamping current is observed. This gives sufficient headroom for the BAT54 to handle the maximum expected over-voltage condition of $60\,\mathrm{V}$, which is the highest voltage present in the system. In such an event the $330\,\Omega$ series resistor would limit the current to the $5\,\mathrm{V}$ supply to roughly

$$I_{max} \approx \frac{U_{fail} - U_{supply} - U_{diode}}{R} \approx \frac{60\,\mathrm{V} - 5\,\mathrm{V} - 0.7\,\mathrm{V}}{330\,\Omega} \approx 165\,\mathrm{mA}$$

The used BAT54 from NXP is capable of permanently taking up to 200 mA with a 0.7 V (typical rating) series voltage drop. Therefore, the remaining input voltage at the level-shifter results in 5.7 V. Unfortunately no maximum rating for the forward voltage is given for the 200 mA value, but even a twice as high value would fit the limit given by the level-shifter.

Supply protection - Active Clamping

This protection concept requires that the supply circuit is capable of sinking multiples of these failure currents in parallel, which is not a very common property among voltage supply regulators. As the level-shifters are supplied via a normal linear regulator, the only existing sink path is through the load devices on the supply. This means that the supply voltage would rise as soon as the current from the over-voltage protection path becomes dominant over that of the load devices. It is therefore necessary to prevent the supply voltage from growing to a value that could actually damage the supplied parts. Otherwise the "protection" circuit could lead to a collateral damage of a multitude of parts throughout the board.

To resolve this issue an active clamping circuitry is connected to the boards supplies. It features a very steep current to voltage curve that is fine-adjustable, which makes it superior to the only coarsely specified zener diodes, which are only present as backup. This allows it to hardly draw any current for a normal supply voltage range, but steadily increase it up to 3 A within only a few 100 mV of over-voltage. As this active clamping circuit is proprietary no further details may be given here.

Reduced signal slew rate

Of course, adding additional parts in the digital signal path does add parasitics too. The BAT54 for example adds additional 10 pF to the signal line. Also the series resistance and the parasitic trace capacitance further increase the rise and fall times.

A signal with probably the worst count of parasitics is for example the clock of the Board SPI. Here the FPGA has to drive 5 input gates over a long track length that is estimated to be around 30 cm. In the worst case, each gate has 10 pF and the track corresponds to roughly 24 pF. But as this is an output signal, at least the parasitic BAT54 capacitance is directly driven and can be omitted from the calculation, as it does not lay behind the series resistor.

$$t_{10\%-90\%} \approx 2.2\tau = 2.2\,(330\,\Omega \cdot (5 \cdot 10\,\mathrm{pF} + 24\,\mathrm{pF})) \approx 52\,\mathrm{ns}$$

As a result this SPI bus may only be operated up into the low MHz range, but this actually matches the requirements very well. A reduced slew rate of all digital signals is a positive side effect of this protection circuitry, which helps avoiding digital noise from coupling to sensitive other lines.

Additional protection for Hot-Plug-testing and against user errors

As already described on page 110, the board allows to simulate hot plugging of the DUT to the batteries. Although the chip is designed to be Hot-Plug resistant, this is something that has to be proofed first. Therefore, not only the FPGA but also many board parts should be protected against possible side effects from damaged ICs. Furthermore, it is possible that user errors, like short circuits with probes to adjacent IC pins etc. may occur over the lifetime of the board.

As a result the previously presented protection concept was applied to many circuits that directly interface with the DUT. This can, e.g., be seen in the already shown concept graphs of the GPIO interface (figure 3.58) or the filtered OpAmp (figure 3.53).

3.3.12 Board power supply and floorplan

Whilst section 3.3.3 concentrated on the supply of the DUT itself, this part now focuses on the supply of the surrounding board electronic. The coarse concept for this board supply can be seen in figure 3.68. The general idea here was to provide voltages as free of disturbances as possible, whilst still requiring only a single external power supply for all the board functions. Therefore, all the supplies are filtered and locally supported by heavy usage of bypass capacitors. Where applicable, the DCDCs were also filtered on the ground side to keep the higher frequency noise spikes as local as possible.

Whilst the higher frequency currents can be kept locally, it is inevitable that the high DC content of the ground return currents spreads across the GND plane. Since the board is supplied by a single supply one can only try to optimize the layout in such a way, that most of the currents run in areas, where they cause the least harm. The supply concept in figure 3.68 has therefore to be looked at in parallel with the floorplan in figure 3.69.

The analog section

The floorplan shows that the analog section is placed on a dedicated ground plane in the right lower corner of the board and that it is supplied by glavanically isolated and additionally filtered DCDC modules. This ensures that none of the other high supply return currents is allowed to run into the analog section. The analog section is directly connected to the GND plane of the DUT by use of the highest possible amount of copper to keep ground shifts low. The remaining currents between the DUT and the analog area should only be related to leakage, and to the actual measurement currents. Furthermore, many measurement signals that run from the DUT into the analog area are done differentially, which compensates ground related errors at least for these signals.

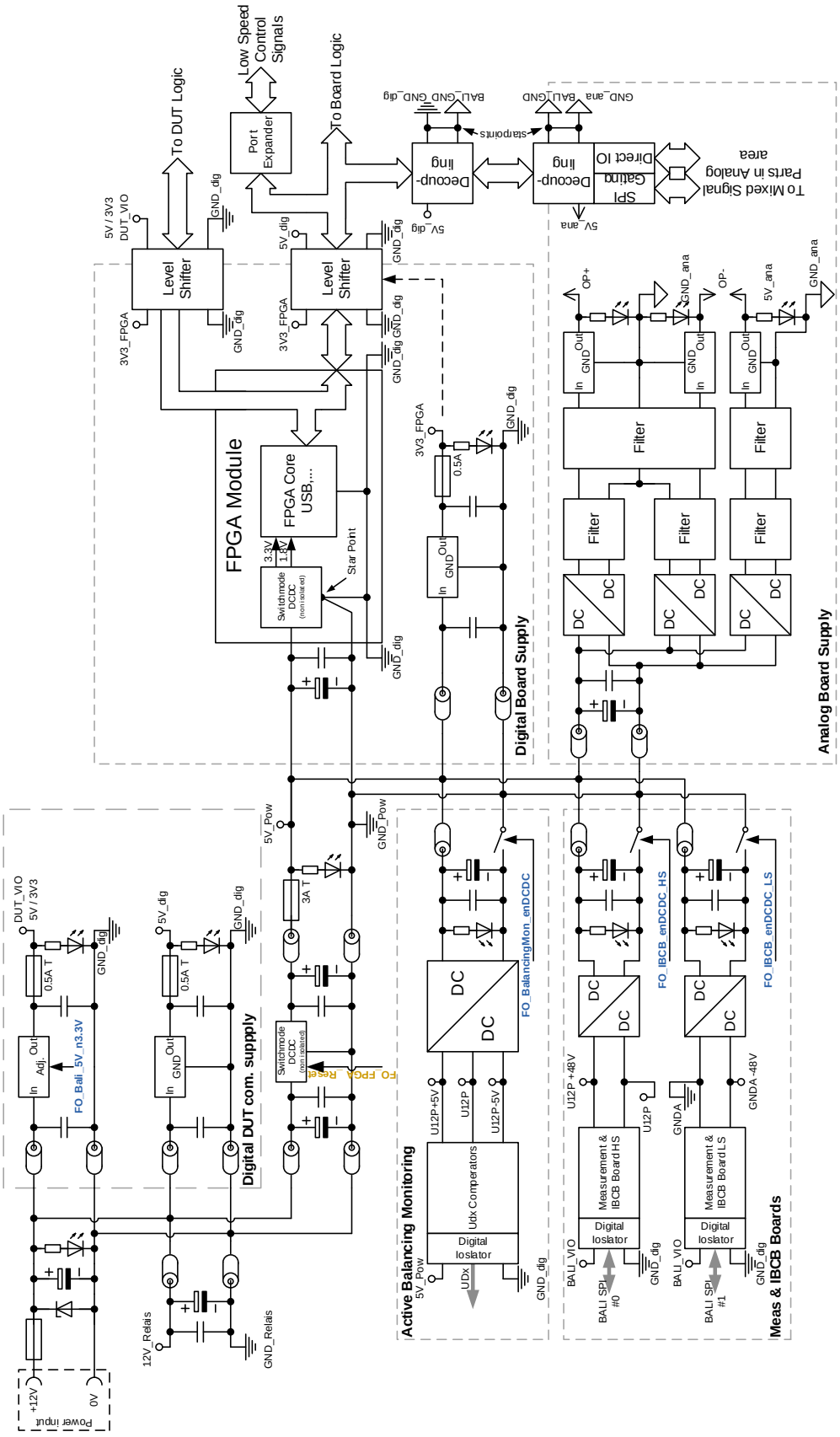


Figure 3.68: Supply concept for the board voltages, excluding the DUT supply

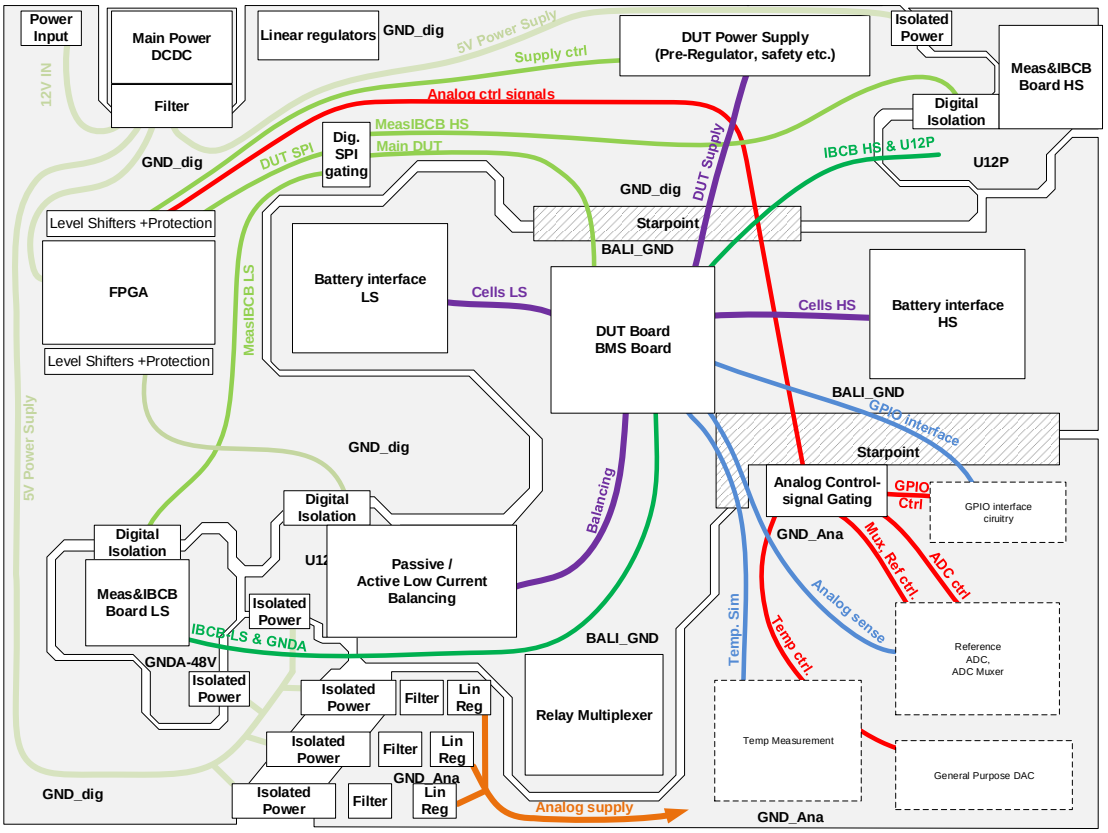


Figure 3.69: Floorplanning concept, not to scale

However, measurements were done on the final board to evaluate the voltage differences between the ground planes of the DUT and the analog area. For this purpose, a DC current was forced between the mounted DUT-Board and a GND testpoint near the ADC of the analog area. The voltages were measured on close-by Kelvin connections. For a current of 100 mA, which is far exceeding the expected currents here, the total voltage drop comes down to 180 µV. But, most of this voltage drop (160 µV) was created across the inevitable electric DUT-Board contacts, which means that only 20 µV are created across the star point area. As the expected ground currents for the DUT-Board should directly result from the chip's power supply, the true voltage shift should even be less than this 160 µV.

But one has to be careful with the design of the return path of the digital control lines from the analog section, as they now have to run over different ground planes. These lines therefore also have to be routed across the star-point areas to keep the current loop and the corresponding inductance low. And as previously mentioned (figure 3.57), these digital signals feature 330 Ω series termination resistors on both ends to keep digital transient current spikes as low as possible.

The DUT section

The next section of interest is the DUT area itself. Just like with the analog section, it is highly desired to keep non DUT related ground return currents away from the DUT's GND area. As the analog section is supplied with isolated DCDCs, the only remaining entry-point is the digital ground plane. Therefore, the only significant static ground return currents flowing across this start-point-area should come from the inevitable DUT's supply, which is located in the digital area.

To avoid deviations between the battery interfaces and the DUT, the connectors as well as the interconnection area were placed on the DUT's ground plane. Furthermore, the balancing area also resides on this plane. As both connections shall allow for low current Active Balancing, the tracks were routed with high copper usage on multiple layers. The PCB stackup was chosen in such a way, that smallest overall return loops result for each of the 12 Ux and Gx channels.

The digital section

The digital section is the area with highest tolerance to ground shifts. Therefore, the DCDC modules and linear regulators were placed here. As the FPGA module's current consumption is in the ampere range, it was placed close to the board's supply and the main power DCDC. Those parts remain in the upper left corner of the PCB, which is the exact opposite side to the analog area.

Furthermore, the main 5 V power rail and its return were routed like a low resistive bus from this area to the more remote DCDC modules. As a result the high DC return ground currents should stay very local in this upper left corner.

The measurement and IBCB boards

As described in section 3.3.5.1, "Measurement and IBCB boards" can be added to the baseboard to allow inter chip communication using only one single baseboard. Each of these boards resides on its own supply that is either above or below the potential of the baseboard. As their signals and supplies are referred to their corresponding ground levels, they also got their own ground planes that reside on U12P and GNDA-48 V level.

The UDx sensing area

The same is true for the UDx sensing comparators (figure 3.46, page 118) of the Active Balancing section. Therefore, also here a separate relative "ground" plane was created that resides on U12P potential. This provides shortest possible ground return paths for the comparators that all reside on this high voltage level.

3.3.13 Software: LabView, Matlab and FPGA

The programming of the software is not directly considered a part of this thesis, although it was also partly done by the author. Therefore, only a very basic overview is given here.

The FPGA features multiple logic modules that directly access the board's hardware, or stimulate the DUT's watchdog by cyclic SPI communication. It can execute single commands requested from the PC, and also small sequences that can even be triggered and paused by hardware events or timer-based in the µs level.

On the PC side the board control can either be done script based using MATLAB or manually via a GUI written in LABVIEW™ that can be seen in figure 3.70.

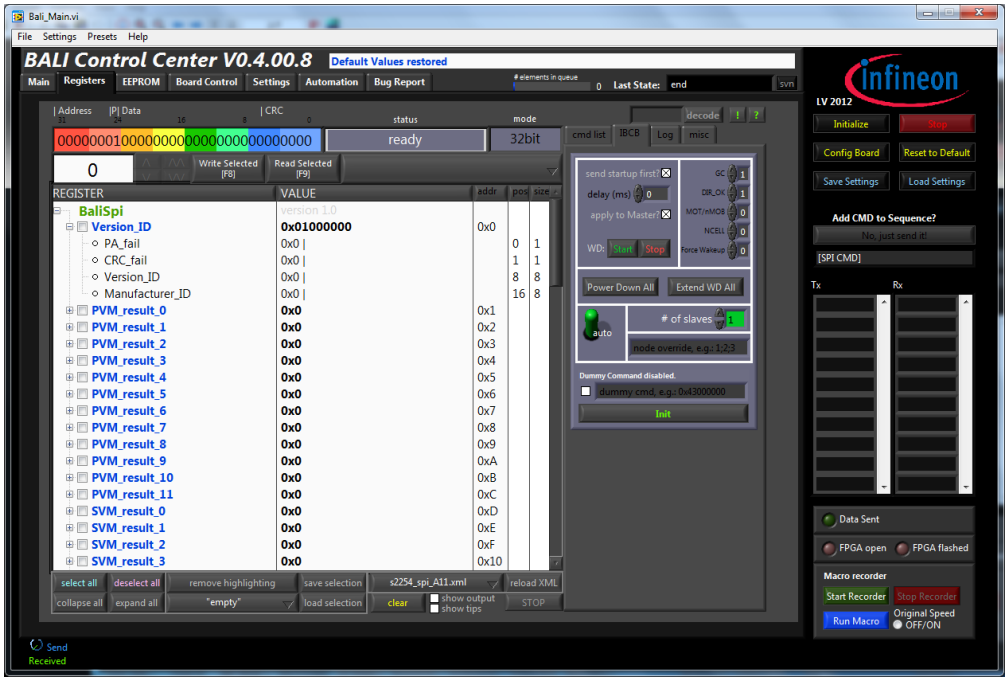


Figure 3.70: User interface for the main verification board

The GUI currently shows a tree that represents the registers of the TLE8000QK and allows direct access to them. It furthermore gives control to the most important board functions in a simple way for manual control. It also features a macro recorder, which allows replaying specific manually entered tasks. This GUI is mainly used for quick setups, where programming and testing of scripts would introduce more time overhead than they might return.

However, for more complex automated tasks, the direct programming of MATLAB scripts is recommended as it gives more degrees of freedom compared to the GUIs simple macro recorder.

3.3.14 Outcome - final verification board

Finally this section presents the outcome of the whole design process. In figure 3.72 a photograph of the verification board can be seen from the top and the bottom-side. Figure 3.71 illustrates the most important connectors on the top-side, which helps to identify special regions on the real board.

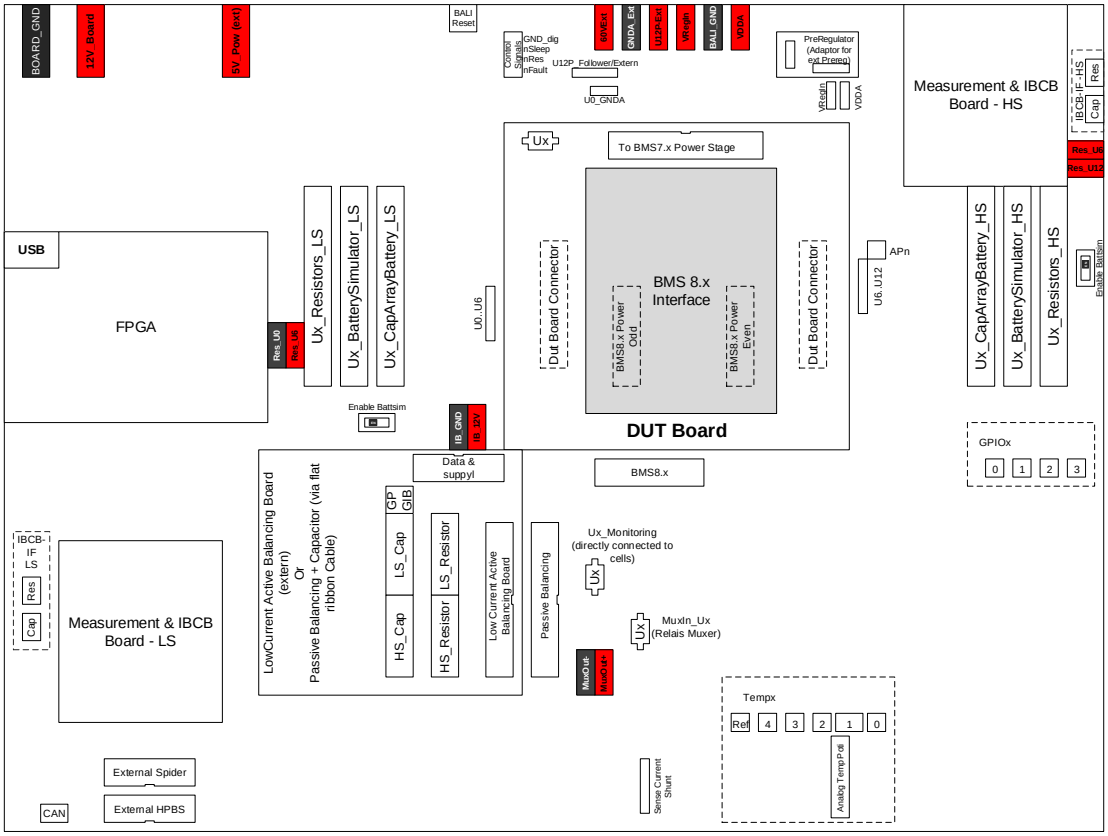


Figure 3.71: Verification board, most important top-side connectors

The upper photograph shows a board that is populated with a ceramic CLCC68 DUT-Board, housing an opened TLE8000QK IC, which allows the bare die to be seen. On the left side the FPGA module is inserted. Directly below and above this module the protection diodes of the level-shifters can be seen.

As can be seen in the middle and to the right, the IDC flat ribbon 1:1 connectors are inserted between the battery simulator and the resistor ladder input. In this configuration only one 12 V supply for the board and one 12 V to 60 V supply for the DUT are required to conduct many verification tasks that do not require the high currents or accuracy of a battery simulator.

To reduce the risk of short circuits, due to accidentally dropped probes, etc., the majority of parts were mounted on the bottom side of the board. Furthermore, all vias were covered with the electrically insulating solder mask.

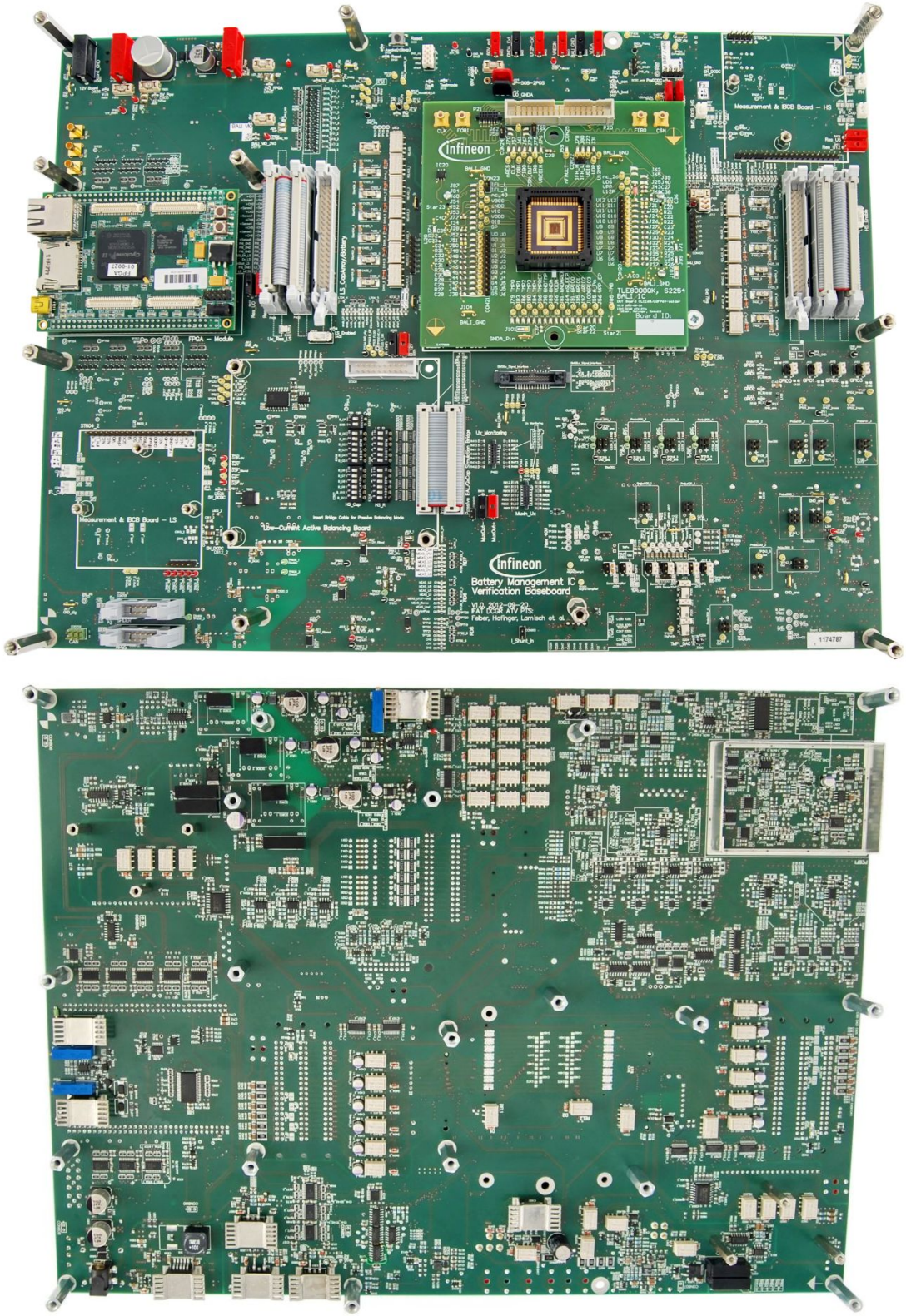


Figure 3.72: The main verification board with a DUT Board. Notice the opened ceramic chip residing on the testfixture on the DUT board.
Top: Top-side of the board, Bottom: Board flipped vertically

On the bottom side of the PCB the metal that houses the analog core parts can be seen. It was opened for this illustration, to show the densely packed precision analog circuitry.

3.3.15 Exemplary measurements with the verification board

This section will present two exemplary measurements, which were conducted with the created verification environment.

Low frequency voltage drop between U1 and U0

Figure 3.73 shows a measurement of the input voltage drop between the DUT's U1 and U0 input pins during the whole duration of the DUT's Ux measurement.

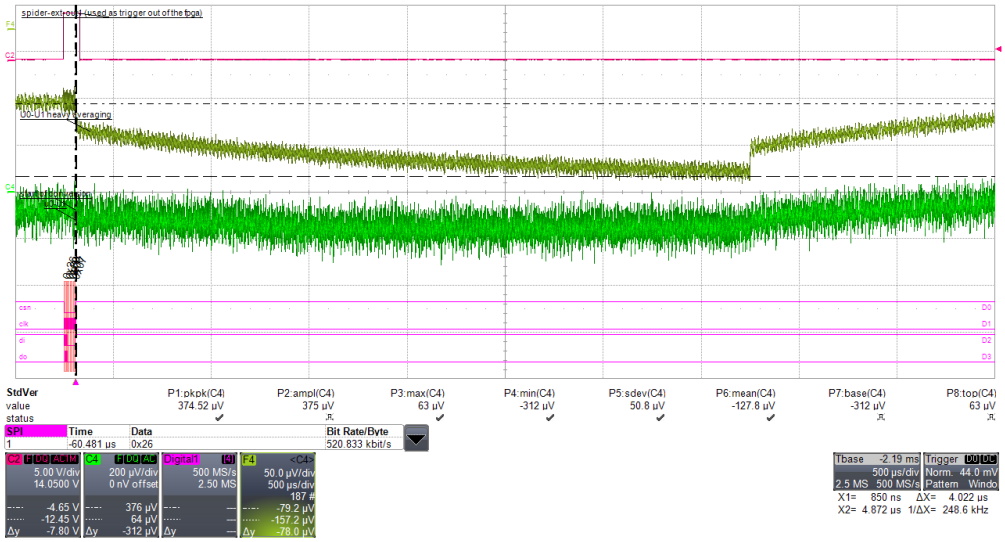


Figure 3.73: Voltage drop at the U1,U0 input pins during a measurement cycle.

As previously explained, the input currents of the DUT's ADCs cause a voltage drop across the series filter resistors. Due to a cancellation effect the resulting current only runs through the lowest and highest cell whilst the others only draw the resulting mismatch current of the adjacent cells. Therefore, the highest voltage drop can be expected at the outermost cells. Figure 3.73 shows that the drop on the lowest cell is only around 75 µV and therefore well below the LSB of the TLE8000QK. This corresponds to an input current of roughly 15 µA which matches up with the typical expected value for room temperature. It can therefore be seen that no other side effects than the expected voltage drop are present here.

Although heavy averaging was used on the oscilloscope's function channel F4, the single shot of C4 (20 MHz BWL + digital 4 MHz filter) shows the very low noise level present on the board, of around 200 µVpp up into the MHz range.

High frequency voltage drop between U1 and U0

Now that it was seen that the low frequency drop is well in the expected range, the high frequency behavior also needs to be checked. Figure 3.74 shows the remaining input voltage ripple between the DUT's U1 and U0 input, while its PADC and SADC are running. This time both, the AP033 and the DA1855A, were used but without applying digital filtering to avoid altering the appearance of the fast voltage transients.

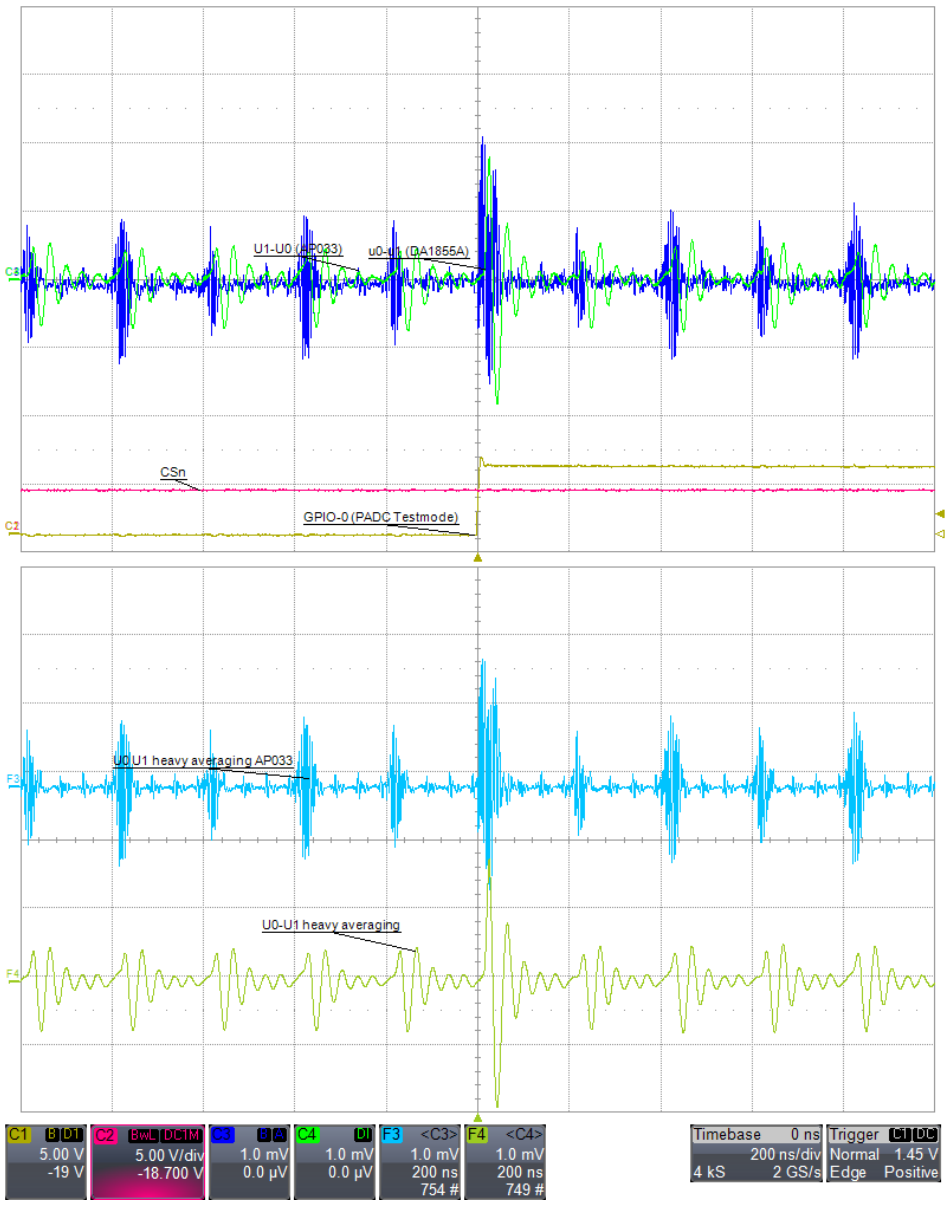


Figure 3.74: ADC related switching noise at the U1,U0 input pins

As result from the learnings during the investigation of the dynamic measurement equipment with the previous testchip (section 3.1.2.1), a special testmode

was added to the TLE8000QK. This mode forces the chip to create a synchronization pulse during the PADC conversion, to allow low jitter averaging with the oscilloscope.

The top part of the image shows a single shot result next to the synchronization pulse. The lower part shows the average of multiple hundred captures. Curve F3 illustrates that there are different types of periodic spikes. First, there is an alternating pattern of a lower and a slightly higher pulse. These correspond to the two different ADCs inside the chip, which both use a switched capacitor input structure that is activated at different times. Then there are smaller but faster spikes that correspond to each edge of the chip's internal digital clock.

As can be seen even the small digital spikes come into the range of a PADC LSB. It is therefore crucial that the sampling points for each bit of the ADC are placed between the digital clock pulses, which is ensured by the design of the IC. In between these pulses the input voltage shows little disturbances well under the level of an LSB of the chip.

4 Conclusion

During this thesis a verification environment for functional and application-like verification of the TLE8000QK IC was created. This environment consists of various equipment for making measurements and for simulating environmental conditions, and a special verification board that allows simulation of various application-like conditions for the DUT.

Existing measurement equipment was analyzed and alternatives for insufficient devices were proposed in section 3.1.2. As a result the recommended dynamic measurement equipment was ordered by the company and later successfully used in the verification process. This equipment and the evaluation phase during this thesis contributed to further improvements of the overall accuracy of the IC. Due to the high flexibility of this equipment it also greatly eased the verification of the differential "Interblock Communication Bus" (IBCB).

Furthermore, a demonstrator for a "High Precision Battery Simulator" (HPBS) was built (section 3.2.1). This device was also successfully used to test concepts for the main verification board prior to its implementation. It contains a recalibrateable voltage reference, that features a voltage drift of only around 110 µV in a temperature range of 5 °C to 45 °C, which corresponds to 0.55 ppm/°C. Furthermore, this demonstrator can be used with different force-sense concepts.

The HPBS's single-side force-sense concept achieves a very fast load regulation time of only 1 µs to within ±30 µV for the force-sensed positive load pin compared to the HPBS's ground, at a ±50 mA load jump. Of course the voltage deviations still depend on the shift between the loads negative pin and the HPBS's ground. This concept may therefore be very interesting for many applications in which all circuits remain on the same low resistive ground plane and a very fast load regulation combined with high accuracy is required.

The double-side force-sense concept of the HPBS allows regulation of static loads of up to ±50 mA over a total length of 50 cm of standard 0.25 mm^2 cables to around 100 µV accuracy, as showed on the implemented prototype. The load regulation time is slower than that of the single-side force-sense concept, but still manages to return the load change to under ±300 µV within 70 µV. As this concept is demonstrated using a retrofitted PCB, it can be expected that further improvements are still possible using a future optimized PCB.

The core part of the verification environment is the main verification board, housing some 2700 active and passive components while having a size slightly larger

than an A3 format paper. It works with different DUT packages as well as the BMS-Board and allows the verification of each functional block of the TLE8000QK. As nearly all functions of the verification board can be changed independently, like for example the chip's supply or communication modes, virtually all application-relevant scenarios can be emulated by the board's hardware.

Currently the available software allows usage of many functions important for verification. There are, however, some automated and semi-automated verification functions that are not yet implemented in the software. Other priorities during the actual verification work led to a postponement of the software development for these automated functions, such as the automated settling measurement of the NTC section. Although they were not used for the first version of the chip, they can still be useful for the verification of future derivatives of the TLE8000QK.

Nevertheless, the repeatability of measurements could be greatly improved compared to the verification environment of the previous testchip, because of the automatic setup and setup identification capabilities of the board. This is also true for the accuracy, as all the built equipment in this thesis, either on the verification board or on the HPBS was designed for highest accuracy from the ground up.

As a result, the verification board and the total environment have already been successfully in use for hundreds of verification measurement tasks.

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Used abbreviations and acronyms

AC	Alternating current
ADC	Analog to Digital Converter
BMS	Battery Management System
BMS-Board	Battery Management System Board, a special board with all the necessary electronics to measure and balance battery cells
Bottom Balancing	Bottom Balancing, transferring an energy portion out of the whole stack to a single cell. For more information see chapter 2.2.2.2
BWL	Bandwidth limit, the maximum unfiltered frequency range that can be measured with an oscilloscope
CMOS	Complementary Metal Oxide Semiconductor, a process for building highly integrated semiconductors
CMRR	Common mode rejection ratio. A figure of merit of an amplifier that states how much error it creates in differential signal amplification, if an common mode voltage is present at both differential inputs
DAC	Digital Analog Converter
DC	Direct current
DCDC	A DCDC converter is a device that transforms voltage from one DC potential to another
DPDT	Double Pole Double Throw specifies that a relay has two switching elements that each can switch an input to two different outputs
DPST	Double Pole Single Throw specifies that a relay has one switching element that can switch an input to two different outputs
DUT	Device under test, here most likely the TLE8000QK IC
DUT-Board	A PCB that holds a testfixture that actually connects to the device under test. For more information see chapter 3.3.2
EMC	Electromagnetic compatibility
ESD	Electro Static Discharge
FPGA	Field programmable gate array. A special customizable IC that can be fully programmed on the logic level and even allows embedding of microprocessors and more
FSR	Full scale range. The maximum voltage range that can be measured with an ADC
GBWP	Gain-bandwidth product, a figure of merit that allows the calculation of the frequency dependency of the gain a complete OpAmp-circuit. For more info see page 62
GND	Ground, or 0V Potential

GPIO	General purpose input output, a special interface on the TLE8000QK IC that allows analog measurements as well as digital input and output of signals
HPBS	High precision battery simulator, a piece of equipment that was developed during this thesis. See page 55
IBCB	Inter Block Communication Bus, a patented serial and daisychainable communication interface
IC	Integrated Circuit
Interblock Balancing	Interblock Balancing, transferring an energy portion of the whole stack to a completely different block. For more information see chapter 2.2.2.2
IRQ	Interrupt request pin on the TLE8000QK
LSB	Least significant bit
MOSFET	Metal Oxide Semicondutor Field Effect Transistor
nFault	inverted failure indication pin on the TLE8000QK
NTC	Negative Temperature Coefficient (Resistor), a cheap kind of temperature sensor
OpAmp	Operational amplifier, a special electronic circuit that provides huge amplification and is used for control activities.
PADC	The Primary ADC of the TLE8000QK, featuring full resolution and accuracy
PCB	Printed circuit board
Pre-charge Bottom Balancing	Pre-charge Bottom Balancing, transferring an energy portion out of the whole stack to the lowest charged cell, solely using the MOSFET's bulk diode. For more information see chapter 2.2.2.2
PXI	PCI eXtension for Instrumentation; a measurement platform based on PCI and founded by National instruments; for more information see http://www.ni.com/pxi
SADC	The secondary ADC of the TLE8000QK, featuring reduced resolution and accuracy
SAR-ADC	Successive approximation register ADC
$\Sigma\Delta$-ADC	Sigma Delta ADC, a special kind of oversampling ADC provides reduced input noise and inherent linearity
self-zeroing	In this thesis self-zeroing relates to any kind of OpAmp that uses some form of automatic offset compensation technique
SPI	Serial Peripheral Interface; a fast serial interface used to connect ICs
SPST	Single Pole Single Throw specifies that a relay has one switching element that can connect or disconnect an electrical contact.
Top Balancing	Top Balancing, transferring an energy portion out of a single cell to the whole stack. For more information see chapter 2.2.2.2
X11 board	The verification board for the X11 testchip, preceding the TLE8000QK, a description can be found in chapter 2.3.1

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