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# Investigation and Drift Minimization of Electrical Parameters caused by Mechanical Stress in High Performance Analog Semiconductor Devices

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# Abstract

Mechanical stress can lead to a drift of the electrical characteristic of integrated analog circuits. This work deals with the main causes for mechanical stress in integrated circuits and the underlying effects. A technique is developed to measure the electronic characteristics of analog chips in a near chip scale package under predefined mechanical stress. This technique is applied to test various types of integrated circuits. For the sake of comparison, the behavior under mechanical stress is further studied by finite element modeling.

*Mechanische Spannung kann zu einem Drift des elektrischen Verhaltens integrierter analoger Schaltungen führen. Diese Arbeit behandelt die Hauptursachen für mechanische Spannungen in integrierten Schaltungen und die zu Grunde liegenden Effekte. Es wurde eine Technik entwickelt, um das elektrische Verhalten von Analogchips in einem „Near Chip Scale Package“ unter definierter mechanischer Spannung zu messen. Diese Technik wird an verschiedene integrierte Schaltungen angewandt. Weiters wurde das Verhalten unter mechanischer Spannung für Vergleichszwecke mittels Finite-Elemente-Modellierung untersucht.*

# Contents

# List of Figures

# List of Tables

# List of Acronyms

**ASIC** application-specific integrated circuit

**BJT** bipolar junction transistor

**CMOS** complementary metal-oxide-semiconductor

**CSP** chip scale package

**CTE** coefficient of thermal expansion

**DAC** digital to analog converter

**DIL** dual in-line

**DUT** device under test

**EP** exposed pad

**fcc** face-centered cubic

**FEM** finite element method

**FET** field-effect transistor

**IC** integrated circuit

**LSB** lowest significant bit

**MEMS** microelectro-mechanical systems

**MLF** MicroLeadFrame®

**MOS** metal-oxide-semiconductor

**MSB** most significant bit

**op-amp** operational amplifier

**PCB** printed circuit board

**PEM** plastic encapsulated microcircuit

**POR** power on reset

**PTAT** proportional to absolute temperature

**QFN** quad-flat no-leadspackage

**SMD** surface-mount device

**SO** small outline

# 1. Introduction

Accuracy plays an important role in analog devices. A few operation conditions of monolithic analog devices are changing the behavior in an unwanted way. The focus in this work is the influence of mechanical stress on the properties of circuits manufactured on silicon wafers in the H35 process, a 0.35 µm complementary metal-oxide-semiconductor (CMOS) process produced by ams AG. The underlying effects are the piezoresistive and piezojunction effect. Both are well studied. They are associated with a mechanical stress in first and second order. During the fabrication of a microchip and its use many more or less controllable sources for a load on the silicon die occur and end up in a complex mixture. Previous experiments described in the literature use a sensitive setup with a single silicon beam or stripe to simulate such stresses on the electronic component on the silicon surface [1, 2, 3]. One aim of this work was the development of a method to characterize the produced chip in a near chip scale package (CSP) in terms of stress sensitivity.

The structure of this work is divided into three parts. The first part is a theoretical description of voltage references, reasons for stress in semiconducting devices and the physical description of the underlying effects. The second part of this work deals with the used method to characterize a semiconductor device with regard to its sensitivity to mechanical stress. The last part lists the findings with a test chip made in a 0.35 µm CMOS process by ams AG tested with the mentioned method.

# Part I.

# Theoretical background and modeling

# 2. Voltage reference

The generation of fixed reference voltage is important to realize many functions of analog circuits. An accurate, temperature-independent voltage source is essential for the performance of modern analog integrated circuits (ICs). The amplified or non amplified output of such reference voltage sources is used for example to set an operating point, as setpoint in a control system or as reference in a digital to analog converter (DAC) [4, p. 496]. In this chapter we will discuss the application-relevant case of a reference to scale the digital input value of a DAC to an analog output signal. Particularly relevant is the influence of the reference voltage accuracy on the precision of the device. A unipolar DAC refers the maximum digital value to the reference voltage minus the voltage of the lowest significant bit (LSB). The implementation of a stable voltage source depends on the application of the device. A very simple concept to produce a temperature-compensated reference voltage makes use of a Zener diode. This technique is inappropriate for low supply voltages because of the Zener voltage in the range of 6 V to 8 V. A more favorable concept for small fixed output voltages and therefore suitable for small supply voltages is called bandgap reference, because of the output in the range 1.2 V, close to the extrapolated energy bandgap voltage of silicon [4, p. 504].

## 2.1. Concept of bandgap reference

There are many ways to realize a voltage reference circuit. In 1971 Robert Widlar already published some design concepts, which can be used to construct a voltage reference device with bipolar junction transistor (BJT) in a monolithic way [5]. The principle of this circuits are based on bipolar transistors as shown in Fig. 2.1.

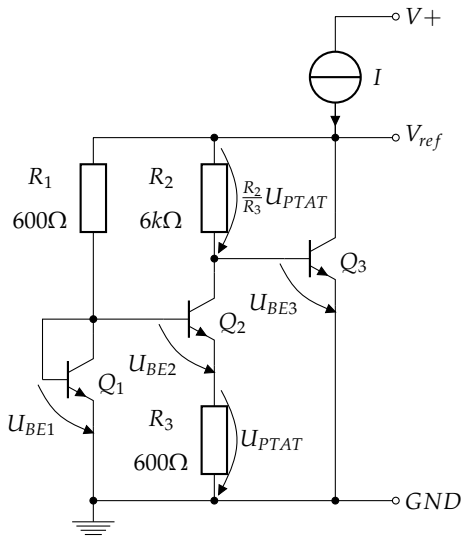



Figure 2.1.: Bandgap design by Robert Widlar [5].

The concept worked out by Widlar is a voltage with a positive temperature coefficient $U_{PTAT}$ added to a diode forward voltage of the transistors base-emitter diode $U_{BE}$ with a negative temperature coefficient as shown in Fig. 2.2. The forward voltage is not a strictly linear. Below 150 °C it is slightly convex. It is a theoretical concept that the forward voltage equals to the bandgap voltage at zero temperature, because there are no charge carriers at this temperature [6, p. 98]. The voltage $U_{PTAT}$ which is proportional to absolute temperature has to be amplified with a factor $n$ because of the low temperature coefficient. The diode forward voltage $U_{BE}$ with a negative temperature coefficient in a bandgap circuit comes from a BJT with shorted base and collector. The temperature characteristic of this transistor behaves like a diode and can be described with the

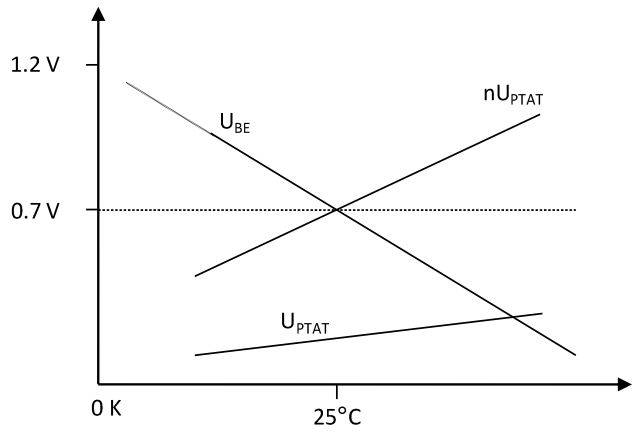



Figure 2.2.: The principle of a bandgap circuit with the amplified $U_{PTAT}$ and the $U_{BE}$ with negative temperature coefficient [6, p. 97].

Shockley diode equation

$$U_{BE} = U_T(T) \ln\left(\frac{I_F}{I_S(T)} + 1\right). \tag{2.1}$$

$U_T$ is the thermal voltage, $I_F$ is the forward current and $I_S$ is the saturation current. Both the thermal voltage and the saturation current are depending on the temperature $T$. Together with the equation for the saturation current

$$I_S = I_S(T_0) \exp\left[\left(\frac{T}{T_0} - 1\right) \frac{U_G(T)}{U_T(T)}\right] \left(\frac{T}{T_0}\right)^3 \tag{2.2}$$

we can calculate the negative temperature dependence of the forward voltage $U_{BE}$ [7, p. 55f.]:

$$\left.\frac{dU_{BE}}{dT}\right|_{I_F=const} = \frac{U_{BE} - U_G - 3U_T}{T} \overset{T=300\,\mathrm{K}}{\approx} -1.7\,\mathrm{mV\,K^{-1}}. \tag{2.3}$$

$U_G$ is the bandgap voltage in silicon and equals to 1.12 V at room temperature. For a silicon diode the current-dependent forward voltage is in the range of 0.7 V and $U_T$ equals to 25 mV at room temperature. This linear behavior is valid in a wide operation range of temperature.

The PTAT (proportional to absolute temperature) voltage comes from the voltage difference of two transistors driven at different current densities:

$$U_{PTAT} = U_{BE1} - U_{BE2} = \frac{kT}{q} \ln\left(\frac{I_{S2} I_{C1}}{I_{S1} I_{C2}}\right) = \frac{kT}{q} \ln\left(\frac{A_2 I_{C1}}{A_1 I_{C2}}\right). \tag{2.4}$$

The difference of the current densities is realized with different junction areas $A_i$ or different current levels $I_{Ci}$. This can be done with a different number of transistors which are parallel, or like in Fig. 2.1 with a high ratio of resistor $R_2$ with respect to $R_1$. The current density of the transistor $Q_2$ is 10 times lower than the current density of the transistor $Q_1$. The PTAT voltage drops over the resistor $R_3$. The voltage across $R_2$ is also proportional to $U_{PTAT}$ and together with the base emitter voltage of transistor $Q_3$ we get the temperature compensated reference voltage [5]:

$$U_{ref} = \frac{R_2}{R_3} U_{PTAT} + U_{BE3}. \tag{2.5}$$

A few years later Paul Brokaw came up with an optimization of the Widlar Bandgap [8]. His concept was more practical. The reference voltage is available at a low impedance point. This fact improves the stability. Both concepts make use of bipolar junction transistors. Also the simplest CMOS process used for analog ICs offers well characterized BJTs. Brokaw's concept for a bandgap reference circuit in a CMOS process is shown in Fig. 2.3. $n$ is the ratio of the emitter area $A$ of transistor $Q_2$ and transistor $Q_1$. There are three options to run transistor $Q_2$ at lower current density than transistor $Q_1$:

1. with a larger emitter area of $Q_2$, $n > 1$ and $R_1 = R_2$
2. with different resistor values $R_2 > R_1$ and $n = 1$
3. or with $R_2 > R_1$ and $n > 1$

A larger emitter area (case 1) is realized with a higher number of parallel transistors. The feedback of the operation amplifier forces the voltage drop of $U_{R1}$ and $U_{R2}$ to be

equal. The reference voltage is given by [4, p. 530]:

$$U_{ref} = I_2(R_2 + R_3) + U_{BE2} = \frac{R_2 + R_3}{R_3} U_T \ln\left(n\frac{R_2}{R_1}\right) + U_{BE2}. \tag{2.6}$$

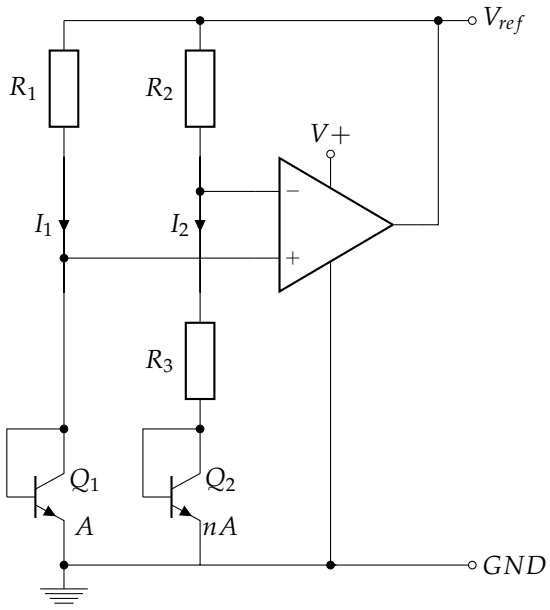



Figure 2.3.: CMOS bandgap [4, p. 529].

## 2.2. Accuracy of analog circuits

The accuracy of reference voltages has a direct effect on the precision of the whole device. This means that it is important to characterize bandgap reference circuits and relate their accuracy with the resolution of the digital to analog converter [9]. The accuracy is specified in percent or as an absolute value of the output voltage. The resolution of a DAC is specified by the physical number of bits. It is necessary to relate the resolution of the converter with the accuracy of the bandgap reference, to specify

the accuracy of the whole device. The maximum analog output value of the DAC is $U_{ref} - U_{LSB}$. The number of states $N$ is equal $2^n$ for an $n$-bit converter. This means that the accuracy of the DAC is specified by:

$$\Delta U_{DAC} = \frac{100\%}{N-1} = \frac{U_{LSB}}{U_{ref} - U_{LSB}} 100\%. \tag{2.7}$$

It can make sense to dimension the converter according to the accuracy of the voltage reference. If the voltage reference has an accuracy of 0.5 %, a 8-bit DAC is sufficient.

# 3. Stress in integrated circuits

Interfaces and packages are essential to connect a microchip to the environment and to protect the device from environmental conditions. These processes are simply named as packaging or assembly. In the literature this step is specified as 1st level in the production line of an electronic device [4, p. 198ff.]. Unfortunately the assembly can change the behavior of the devices. One effect is the mechanical stress on the silicon die itself. The steps during the assembly may vary depending on the used package type and the stress can be compressive or tensile (so-called packaging stress see Section 3.1). The use of chip scale packages (CSPs) and near CSPs have experienced substantial growth in the last decades because of their small outline, the thin profile, the low lead frame inductance, and the low process costs. One common near CSP type is the quad-flat no-leadspackage (QFN). There are different names depending on the manufacturer of this type of package. MicroLeadFrame® (MLF) is a registered trade name of Amkor Technology® for such type of packages. The process steps described in this chapter are related to MLF packages. Today plastic encapsulated microcircuits (PEMs) are very common in fact of their low price. The chip is packed in a transfer mold process. A drift of the chip parameters caused by packaging stress can be compensated by pre-trimming after the device production.

The assembly is not the only source for generation of stress. The 2nd level in the production line is to merge the chip level devices together to an electronic module on a

printed circuit board (PCB). The soldering process during the production is also a main source for stress. The difference of the coefficients of thermal expansion of the solder and the chip lead frame cause this so-called solder stress (see Section 3.2).

During the lifetime of the device, environment conditions like temperature or moisture can also lead to a change of the internal mechanical stress. Plastic encapsulation materials are non-hermetic. This means that moisture can diffuse into the bulk of the package. The chip is protected by a passivation layer, but the package itself can swell, caused by moisture. This leads to a change of the mechanical stress.

For the sake of completeness also other sources for mechanical stress should be listed, even if they have no relevance because they are not changing the parameters during the lifetime of the device. The production of ICs is a multilayer technology. Material deposition, doping, and oxidation at different process temperatures lead to a layered structure with an inbuilt stress. This can be reduced by a thermal annealing process.

## 3.1. Packaging stress

Gluing is the common used method to join the chip to the lead frame. The big advantage is the low temperature compared to joining it in a soldering process. Epoxy resin adhesives are widely used. The chemical mechanism of this type of adhesives is polymerization followed by curing (hardening via cross-linking). Adhesives based on epoxy resin can have different curing temperatures. Epoxy resin used to attach dies to the lead frame have high curing temperatures around 180 °C for 30 minutes. The different thermal expansion coefficients lead to a thermal stress [4, p. 211ff.]. This so-called in-plane stress in a MLF package is tensile and in the range of 10 MPa [10].

The connection of the chip to the package leads takes place in the bonding process. The oldest and most popular bonding method is wire bonding. The contact of the bond wire and the metallization of the chip are realized by introducing energy into the interface. Thermal and ultrasonic methods are commonly used. This flexible wire connection does not produce a residual stress in the die. Wire bonding is used for many package types and also MLF packages. For the sake of completeness we should also mention flip-chip bonding and tape-automated bonding. The chip is connected up side down with small solder balls and an under-filler to the lead substrate in the flip-chip bonding process. Tape-automated bonding is also a method to connect all pins in one step directly with conductors in a plastic film. Flip-chip and tape-automated bonding can introduce stress in the die.

The encapsulation of the chip (potting) is the final assembly step. Today 99 % of all chips are encapsulated in plastic (non-hermetic) packages. The improved encapsulation materials and the process combined with improved die passivation make the usage of hermetic packages like metal and ceramic obsolete. Metal and ceramic packages can only be found in niche applications in high temperature environment or for high frequency devices. The most common used material for the mold compound is epoxy resin. Some applications may also use polysiloxanes, polyimide, and polyurethanes. There are pre-mold and post-mold plastic packages [11]. Pre-molded packages are more expensive due to the higher number of process steps. Due to the cavity between the die and the upper shell of such packages, stress on the chip can be avoided when the two pieces are put together with an adhesive. The mold compound for a post-molded package is delivered as billet and joint with the die on the lead frame in a transfer mold process. The high pressure and the curing shrinkage produce a residual stress in the die. The considered MLF packages in this work are post-molded epoxy resin packages. The mold compound around the die is shown in Fig. 3.1. This so-called volumetric package stress in a MLF package is compressive and in the range of 50 MPa [10]. If we consider

the flat geometry of this type of package the component of the volumetric stress parallel to the surface is much higher than the component perpendicular to the surface.

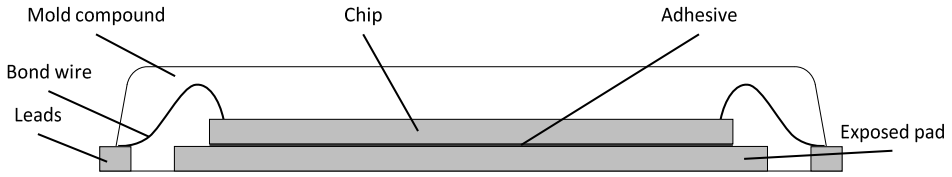


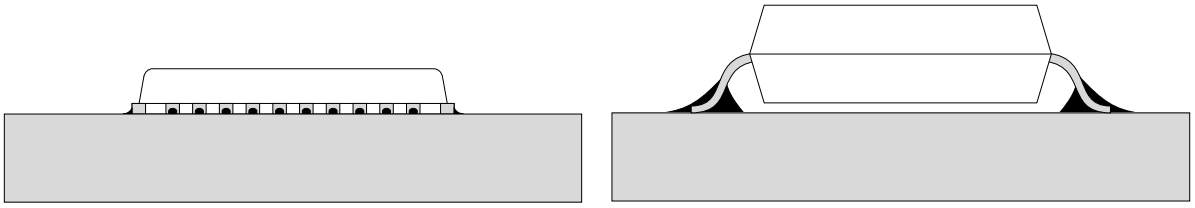

Figure 3.1.: Chip mounted on leadframe, bonded and packed in MLF package.

Due to their properties, epoxy resins cannot be used without additions. The epoxy mold compound contains filler particles. The filler reduces the coefficient of thermal expansion (CTE) and rises the thermal conductivity of the mold. Amorphous silica is a typical filler material and also used in MLF packages. Those particles are solid in the mold and have a much higher elastic modulus compared to the epoxy resin. This leads to a high local stress on the active surface of the die around such particles. In the literature this is called the local stress component, whereas the curing stress of the mold compound is denoted as the global stress component [12, 13].

## 3.2. Solder stress

A MLF packaged IC is directly mounted to the printed circuit board (PCB) during a reflow solder process. The lead frame and the plastic mold are put together to build a planar surface where the leads do not extend out of the package side. The first invented surface-mount device (SMD) package type was a modification of the dual in-line (DIL) package. This so-called small outline (SO) package type has “gull wing” leads instead of vertical leads like in through-hole mounted devices [4, p. 217]. Even if this package

needs a larger area on the PCB than MLF packages, the connection is more flexible and prevents a transfer of mechanical stress to the package and to the IC. The flexible mounted SO package is compared with the MLF package on a PCB in Fig. 3.2. For reasons of heat dissipation and mechanical stability MLF packages generally have a big exposed die attach paddle or simply called exposed pad (EP). In Fig. 3.1 one can see how the silicon die is attached to this pad. The other side of the EP gets soldered to the circuit board. There is a mismatch of the CTE of the copper lead frame and the solder. A residual stress occurs after the cooling phase. This effect associated with the reliability of soldered joints is well studied [14, 15]. The large area and the bad reproducibility give rise to randomly distributed solder voids and stress in the die [16].



(a) MLF package mounted on PCB. (b) SO package mounted on PCB.

Figure 3.2.: Comparison of MLF package and SO package mounted on a PCB, the elastic pins can absorve solder stress.

### 3.2.1. Estimation of solder stress in near CSP with exposed pad

Figure 3.2a shows how the chip is mounted to the exposed pad. The device underlies an additional force due to the higher thermal strain of solder compared to copper [17]. The thermal strain $\varepsilon_{th}$ produced by the CTE mismatch $\Delta\alpha$ between the two materials during a temperature change of $\Delta T$ is given by:

$$\varepsilon_{th} = \Delta T \Delta \alpha. \tag{3.1}$$

This is a rough estimation because the CTE and elastic modulus of solder materials are both strongly depending on the temperature. With the material properties in Table 3.1 we can calculate the strain difference $\varepsilon_{th}$ of 0.12 % between copper and solder after solidification of the solder and cooling to room temperature.

Table 3.1.: Important material parameters in solder processes [18, 19].

| | |
|---|---|
| **Oxygen-free electronic copper** | |
| CTE | 17 $\frac{\mu m\,K}{m}$ (at 20 °C to 200 °C) |
| Elastic modulus | 117 GPa |
| **Lead-free solder ($Sn_{96.5}Ag_{3.0}Cu_{0.5}$)** | |
| CTE | 23 $\frac{\mu m\,K}{m}$ (at 80 °C) |
| Elastic modulus | 80 GPa ( at 40 °C) |
| | 40 GPa (at 100 °C) |
| Solidus | 217 °C |

This approximation is good enough to define the requirements for a setup to apply a simulated solder stress to a semiconductor device. The real solder stress is expected to has a high random distribution due to variations of solder thickness, incomplete coverage of the EP with solder, and the spatial location where solidification starts.

The thermal expansion $\Delta l_i^{th}$ of the copper and the solder are given by:

$$\Delta l_{Cu}^{th} = \alpha_{Cu} l \Delta T; \qquad \Delta l_{So}^{th} = \alpha_{So} l \Delta T. \tag{3.2}$$

The difference of the thermal expansion leads to a force $F_i$ and an elastic elongation $l_i^{el}$ between the layers as given by:

$$\Delta l_{Cu}^{el} = \frac{F_{Cu} l}{E_{Cu} A_{Cu}}; \qquad \Delta l_{So}^{el} = \frac{F_{So} l}{E_{So} A_{So}}. \tag{3.3}$$

$E_i$ is the elastic modulus of the materials and $A_i$ the area of the layers. This simple model is based on the equilibrium conditions:

$$F_{So} = -F_{Cu}; \qquad \Delta l^{el}_{Cu} + \Delta l^{th}_{Cu} = \Delta l^{el}_{So} + \Delta l^{th}_{So}. \tag{3.4}$$

Equations (3.4) are valid if the bulk of the PCB is large enough to avoid bending and if pealing forces between the layers can be neglected. The stress in the copper layer results to:

$$\boxed{\sigma_{Cu} = \frac{\Delta T E_{Cu}(\alpha_{So} - \alpha_{Cu})}{1 + \frac{E_{Cu}A_{Cu}}{E_{So}A_{So}}}} \tag{3.5}$$

Equation (3.5) can be used to estimate the magnitude of the solder stress. This is necessary to define the requirements of the presented test procedure in Part II to simulate solder stress.

In general, the thickness of the PCB copper and the lead frame can vary depending on the package type.

**Example:** The solder stencil, the lead frame of an MLF, and the copper layer of the PCB exhibits a thickness of 125 µm, 250 µm, and 35 µm respectively. The resulting stress in the copper amounts to −22 MPa with Eq. (3.5). If we assume the mean elastic modulus of copper and silicon for a double cross section area we can calculate a mean stress of −13 MPa in the copper silicon compound and a stress of −15 MPa in the silicon.

## 3.3. Mechanical properties of silicon

On the one hand, the increasing accuracy requirements make it important to understand the mechanical properties of silicon and its impact on with the electric behavior. On

the other hand, there is a growing field of applications for microelectro-mechanical systems (MEMS). In this case a high influence of the electric properties under load is desired.

Crystalline silicon has a diamond structure. So it belongs to the group of cubic crystal structures which exhibits a fcc lattice with a two atomic base at $(0,0,0)$ and $(\frac{1}{4},\frac{1}{4},\frac{1}{4})$. This is the reason for the anisotropic behavior of silicon. The compliance tensor has three independent coefficients and can be put in a matrix equation according to Voigt notation:

$$\begin{bmatrix} \epsilon_{xx} \\ \epsilon_{yy} \\ \epsilon_{zz} \\ \epsilon_{xy} \\ \epsilon_{yz} \\ \epsilon_{zx} \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{12} & 0 & 0 & 0 \\ S_{12} & S_{11} & S_{12} & 0 & 0 & 0 \\ S_{12} & S_{12} & S_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & S_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & S_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & S_{44} \end{bmatrix} \times \begin{bmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \tau_{xy} \\ \tau_{yz} \\ \tau_{zx} \end{bmatrix} \tag{3.6}$$

The values for the compliance tensor, taken from [20], are listed in Table 3.2.

Table 3.2.: Coefficients of the compliance tensor for monocrystalline silicon taken from [20].

| | $[10^{-10}\,\mathrm{Pa}^{-1}]$ |
|---|---|
| $S_{11}$ | 0.768 |
| $S_{12}$ | −0.214 |
| $S_{44}$ | 1.260 |

It is also common to use the stiffness tensor which is the inverse of the compliance tensor. The advantage of the compliance tensor is that we can easily see the elastic modulus $E_{[100]} = \frac{1}{S_{11}}$ and the Poisson ratio $\nu_{12} = -\frac{S_{12}}{E_{[100]}}$.

The values of Young's modulus for most important directions are [21]:

- $E_{100} = 130\,\text{GPa}$
- $E_{110} = 169\,\text{GPa}$
- $E_{111} = 188\,\text{GPa}$

In this work also polycrystalline silicon devices are used. There is a variation of the elastic modulus of polycrystalline silicon reported in the literature [22, 23, 24]. In this work we use the value of 169 GPa and the Poisson ratio of 0.22 according to the work of Sharpe [23].

# 4. Stress influence on semiconductor device

In Chapter 2, the circuit of a bandgap was introduced and it was described how for example a change in the reference voltage influences the accuracy of a DAC. Solder and package stress were discussed in Chapter 3. The parameters of the components used in a bandgap circuit underlie a stress-induced change and this leads to a drift of the reference voltage. This chapter deals with the piezojunction and piezoresistive effect and their influence on the behavior of polysilicon resistors, BJT, and metal-oxide-semiconductor (MOS) field-effect transistors (FETs).

## 4.1. Polysilicon resistor

The known equation of the resistance

$$R = \rho \frac{l}{A} = \rho \frac{l}{wt} = R_s \frac{l}{w} \tag{4.1}$$

can be used to describe the change in electrical conduction during mechanical load. The geometry of the structure is included with the length $l$ and the cross section area $A$. $t$ denotes the thickness and $w$ the width. For thin layers with uniform thickness

the sheet resistance $R_s$ is commonly used instead of the specific electrical resistivity $\rho$. The unit of the sheet resistance is "ohm" ($\Omega$), but it is common to use the unit "ohms per square" ($\Omega/\square$) to indicate that it is also a specific value [4, p. 266]. There are two different known effects influencing the resistance of any resistor if a mechanical load is applied. On the one hand, there is a change in length and width of the structure. The change of the resistance due to the geometry is the basic for strain gauges made of metallic foil. William Thomson (Lord Kelvin) already found this effect in 1857 [25]. On the other hand, there is a change in the specific resistivity (or sheet resistance) of the material. Depending on the type of the material this effect can overcome the geometric effect. In semiconductor materials this so-called piezoresistive effect is hundred times larger than the effect arising from the change of the dimensions. It was discovered by Charles Smith in 1954 [26].

The piezoresistive effect is based on the change of the mobility $\mu$ and the charge carrier density $n$ and $p$ in semiconductor materials. The conductivity $\kappa$ is given by:

$$\kappa = \frac{1}{\rho} = q(n\mu_e + p\mu_p) \approx qp\mu_p \tag{4.2}$$

Although the mobility of holes is three times lower than the mobility of electrons, the dominant value in the equation is the concentration of the majority charge carriers, because the majority charge carrier concentration can be $10 \times 10^{10}$ times higher than the minority charge carrier concentration. For a p-type polysilicon resistor the holes are the majority carriers and their concentration determines the resistivity [27].

The relative change in resistance per mechanical strain $\varepsilon$ is called the gauge factor $G$. The stress $\sigma$ in $z$-direction can be converted with the elastic modulus $E$ in a strain $\varepsilon_z = \sigma E$. With the strain and the current direction being parallel in the longitudinal case and the gauge factor of an anisotropic material like monocrystalline silicon yields to:

$$G_l = \left(\frac{\Delta R}{R\varepsilon_z}\right)_l = 1 + \nu_x + \nu_y + \frac{\Delta\rho}{\rho\varepsilon_z} \tag{4.3}$$

The transverse gauge factor is related to the current direction perpendicular to the direction of the mechanical strain and is given by:

$$G_t = \left(\frac{\Delta R}{R\varepsilon_z}\right)_t = -1 + \nu_x - \nu_y + \frac{\Delta\rho}{\rho\varepsilon_z}. \tag{4.4}$$

$\nu_x = -d\varepsilon_x/d\varepsilon_z$ and $\nu_y = -d\varepsilon_y/d\varepsilon_z$ are the Poisson ratios in Eq. (4.3) and (4.4).

Polycrystalline silicon is made out of grains with random orientation or with preferred orientation. The Poisson ratio is the same for all directions, if we assume a random distribution of the grain orientation the gauge factors simplifies to:

$$G_l = 1 + 2\nu + \frac{\Delta\rho}{\rho\varepsilon}; \qquad G_t = -1 + \frac{\Delta\rho}{\rho\varepsilon} \tag{4.5}$$

with the Poisson ratio $\nu$ for polycrystalline silicon.

A lot of research has been done in the 1970s and 1980s to characterize polycrystalline silicon strain gauges [28, 29, 30]. In the end a model to describe the behavior of such polysilcon devices in terms of grain size, texture and doping level has been developed [31]. This model considers diffusion and thermionic emission in polysilicon as the dominant mechanism for charge transport. Depending on the doping level it is necessary to consider the grain boundary in the theory to calculate the gauge factor. The conductivity in polysilicon is given by:

$$\rho = \frac{L - (2w - \delta)}{L}\rho_g + \frac{2w + \delta}{L}\rho_b \tag{4.6}$$

$\rho_g$ is the grain resistivity and $\rho_b$ the barrier resistivity. The morphology is included by the grain size $L$, the boundary thickness $\delta$, and the depletion region $w$. It was shown that the grain boundary is insensitive to strain in high doped polysilicon and can therefore be neglected [31].

The relationship between the change of the resistivity and the stress in an anisotropic material like silicon is described with the tensor equation:

$$\frac{\Delta\rho_{ij}}{\rho_0} = \pi_{ijkl}\sigma_{kl}. \tag{4.7}$$

$\pi_{ijkl}$ is the piezoresistive tensor and $\sigma_{kl}$ is the stress tensor. We use the Voigt notation to convert Eq. (4.7) to a matrix equation given by:

$$\frac{1}{\rho}\begin{bmatrix}\Delta\rho_{xx}\\ \Delta\rho_{yy}\\ \Delta\rho_{zz}\\ \Delta\rho_{xy}\\ \Delta\rho_{yz}\\ \Delta\rho_{zx}\end{bmatrix} = \begin{bmatrix}\pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0\\ \pi_{12} & \pi_{11} & \pi_{12} & 0 & 0 & 0\\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0\\ 0 & 0 & 0 & \pi_{44} & 0 & 0\\ 0 & 0 & 0 & 0 & \pi_{44} & 0\\ 0 & 0 & 0 & 0 & 0 & \pi_{44}\end{bmatrix} \times \begin{bmatrix}\sigma_{xx}\\ \sigma_{yy}\\ \sigma_{zz}\\ \tau_{xy}\\ \tau_{yz}\\ \tau_{zx}\end{bmatrix} \tag{4.8}$$

The coordinate system which is used here is aligned with the crystal-axis coordinate system. In this case the longitudinal piezoresistive coefficient is given by $\pi_{11}$ and the transverse by $\pi_{12}$. Smith measured the piezoresistive coefficients in lightly doped silicon [26]. The material for polysilicon resistors is usually heavily doped. The investigations, done by Matsuda [1], instead describe the piezoresistive coefficients in heavily doped silicon (see Table 4.1).

Table 4.1.: Piezoresistive coefficients for heavily doped silicon by Matsuda [1].

| carrier concentration [$\mathrm{cm}^{-3}$] | | $1 \times 10^{17}$ | $5 \times 10^{17}$ | $8 \times 10^{18}$ |
|---|---|---|---|---|
| | | | $[10^{-10}\,\mathrm{Pa}^{-1}]$ | |
| p-type | $\pi_{11}$ | 0.0 | −0.6 | −0.4 |
| | $\pi_{12}$ | 0.2 | 0.1 | 0.3 |
| | $\pi_{44}$ | 11.9 | 11.2 | 9.7 |
| n-type | $\pi_{11}$ | −8.4 | −7.7 | −6.5 |
| | $\pi_{12}$ | 4.3 | 3.9 | 3.3 |
| | $\pi_{44}$ | −2.0 | −1.4 | −1.2 |

We can also relate the stress to the relative change in the conductivity $\kappa$ with the same

piezoresistive tensor:

$$\frac{\Delta\kappa_{ij}}{\kappa_0} = -\pi_{ijkl}\sigma_{kl}. \tag{4.9}$$

Any rotation of the crystal-axis coordinate system is taken into account by a transformation of the piezoresistive tensor [32]. The transformation for the longitudinal and transverse piezoresistive coefficient is given by

$$\pi_l = \pi_{11} + 2\left(\pi_{12} + \pi_{44} - \pi_{11}\right)\left(l_1^2 m_1^2 + l_1^2 n_1^2 + m_1^2 n_1^2\right) \tag{4.10}$$

and

$$\pi_t = \pi_{12} + 2\left(\pi_{11} - \pi_{12} - \pi_{44}\right)\left(l_1^2 l_2^2 + m_1^2 m_2^2 + n_1^2 n_2^2\right), \tag{4.11}$$

respectively. $l_i$, $m_i$ and $n_i$ are the coefficients of the rotation matrix

$$\begin{bmatrix} x' \\ y' \\ z' \end{bmatrix} = \begin{bmatrix} l_1 & m_1 & n_1 \\ l_2 & m_2 & n_2 \\ l_3 & m_3 & n_3 \end{bmatrix} \times \begin{bmatrix} x \\ y \\ z \end{bmatrix}. \tag{4.12}$$

The crystal-axis coordinate system is represented by $x$, $y$, $z$ and transformed to the coordinate system of the piezoresistor $x'$, $y'$ and $z'$.

The same applies for the transformation of the coefficients of the compliance matrix $S_{ij}$ with the transformation:

$$S'_{ij} = S_{12} + \left(S_{11} - S_{12} - \frac{1}{2}S_{44}\right)\left(l_i^2 l_j^2 + m_i^2 m_j^2 + n_i^2 n_j^2\right) \tag{4.13}$$

and

$$S'_{ii} = S_{11} + \left(S_{44} + S_{12} - 2S_{11}\right)\left(l_i^2 m_i^2 + l_i^2 n_i^2 + m_i^2 n_i^2\right). \tag{4.14}$$

We can now use the transformed values to define a general expression for the gauge factor with:

$$G_{l,t} = 1 - \sum_j \frac{S'_{ij}}{S'_{ii}}(1 - \delta_{ij}) + \frac{\pi_{l,t}}{S'_{ii}} \tag{4.15}$$

In the Eq. (4.13), (4.14) and (4.15), $i = 1$ in case of longitudinal stress and $i = 2$ in case of transverse stress.

Independent of the grain size, by assuming a random orientation of grains, one can calculate the relative change of the resistivity per unit strain of polysilicon from the piezoresistive coefficients of monocrystalline silicon by averaging over all orientations

$$\langle \pi_{l,t} / S'_{ii} \rangle = \left. \frac{\int_{\theta=0}^{\pi/2} \int_{\phi=0}^{\pi/4} \left( \frac{\pi_{l,t}}{S'_{ii}} \right) d\theta d\phi}{\int_{\theta=0}^{\pi/2} \int_{\phi=0}^{\pi/4} d\theta d\phi} \right|_{\psi=0} . \tag{4.16}$$

This value is the relative change of the resistivity per unit strain, in contrast to the piezoresistive coefficient which is the relative change of the resistivity per unit stress. The values according to this model are appropriate as long as the effect of grain boundaries can be neglected [33]. $\langle \pi_l / S'_{11} \rangle$ and $\langle \pi_t / S'_{22} \rangle$ are the expected values observed during the mechanical load experiment with a polysilicon resistor (see part III). The calculated values of polycrystalline silicon are shown in Table 4.2 and can be converted in the piezoresistive coefficients of polysilicon with the elastic modulus. The MATLAB source-code for the calculation is shown in the appendix. The ratio $\langle S'_{ij} / S'_{ii} \rangle$ characterizes the elastic properties of polysilicon and can be calculated with an equation similar to 4.16.

Table 4.2.: Relative change of the resistivity per unit strain for heavily doped polycrystalline silicon.

| carrier concentration [cm$^{-3}$] | | $1 \times 10^{17}$ | $5 \times 10^{17}$ | $8 \times 10^{18}$ |
|---|---|---|---|---|
| p-type | $\langle \pi_l / S'_{11} \rangle$ | 6.3 | 5.3 | 4.8 |
| | $\langle \pi_t / S'_{22} \rangle$ | $-2.2$ | $-2.3$ | $-1.7$ |
| n-type | $\langle \pi_l / S'_{11} \rangle$ | $-6.9$ | $-6.1$ | $-5.2$ |
| | $\langle \pi_t / S'_{22} \rangle$ | 4.5 | 4.0 | 3.4 |

For a more precise description considering also the morphology of the grains, the

model has been extended by French [31] with an additional coefficient for $\langle \pi_l / S'_{11} \rangle$ and $\langle \pi_t / S'_{22} \rangle$.

## 4.2. Bipolar junction transistor

A mechanical stress influences the charge transport. This effect can also be observed in bipolar junction transistors (BJTs). It is called the piezojunction effect and was discovered by Harry H. Hall [34]. A detailed description was done in the end of the 1990s and at the begin of the 2000s by a group in Delft. They formulated a relation between this effect and the piezoresisitve effect [27] and also determined the coefficients of the piezojunction tensor [35, 36]. Later they found the relation for the stress-induced change of a reference voltage generated with bandgap reference circuits [37].

The BJTs used in bandgap circuits with connected base and emitter act as a diode. We focus on such devices because their drift can influence the behavior of an analog circuit as discussed in Section 2.2. The current of a transistor connected as diode is described by [38]:

$$I_C = I_S \left[ \exp \frac{q U_{BE}}{k_B T} - 1 \right] \overset{I_C \gg I_S}{\approx} I_S \exp \frac{q U_{BE}}{k_B T} \tag{4.17}$$

with the saturation current $I_S \approx 1\,\mathrm{pA} \ldots 1\,\mu\mathrm{A}$ , the elementary charge $q$, the base emitter voltage $U_{BE}$, the Boltzmann constant $k_B$ and the temperature $T$. At moderate current level, $(-1)$ can be neglected in Eq. (4.17) [7, p. 6]. We already discussed this Shockley equation in Chapter 2.

The saturation current is the relevant quantity in the equation with respect to stress influence. $I_S$ of a PNP-transistor can be described with:

$$I_S = k_B T \frac{A_E (pn)_0^n \mu_p^n}{W N_D} = k_B T \frac{A_E}{W} p_0^n \mu_p^n. \tag{4.18}$$

$A_E$ is the emitter base junction area, $W$ is the width of the base and $(pn)_0^n \mu_p^n$ is the product of the charge concentrations in the n-base and the mobility of the holes in the n-base. $A_E$ and $W$ remain constant at moderate stress level and $n_0$ is equal to the donor concentration $N_D$. Only the change of the product $p_0^n\ \mu_n^p$ is influenced by stress. As done with the resistivity we can define an expression for the conductivity in the base of the bipolar transistor as given by:

$$\kappa_p^n = \frac{1}{\rho_p^n} = q p_0^n \mu_p^n. \tag{4.19}$$

The first-order piezojunction coefficients $\xi_{ijkl}$ and second order piezojunction coefficients $\xi_{ijklmn}$ are related to the change of the minority conductivity:

$$\frac{\Delta I_S}{I_S} = \left[\frac{\Delta \kappa_p^n}{\kappa_{p,0}^n}\right]_{ij} = -\xi_{ijkl}\sigma_{kl} + (\xi_{ijkl}^2 - \xi_{ijklmn})\sigma_{kl}\sigma_{mn}. \tag{4.20}$$

In the PNP transistor $\kappa_p^n$ is the product of the hole mobility in the n-region and the hole concentration. The first- and second-order piezojunction coefficients for vertical BJT on a $(100)$ wafer and a stress in $[011]$ direction are listed in Table 4.3.

Table 4.3.: First- and second order piezojunction coefficients for vertical BJT on a $(100)$ wafer and stress in $[011]$ direction (taken from [39]).

| | first-order | second-order |
|---|---|---|
| | $[10^{-10}\,\mathrm{Pa}^{-1}]$ | $[10^{-18}\,\mathrm{Pa}^{-1}]$ |
| pnp | 1.43 | −0.73 |
| npn | 4.55 | −0.30 |

The focus of this work is on vertical transistors on a $(100)$ wafer. The current direction is in the $[100]$ direction. The stress can be applied in the direction $[011]$ and $[01\bar{1}]$. Both directions lead to a transverse stress. With Eq. (4.17) we can relate the relative change

of the base emitter voltage to the relative change of the saturation current given by:

$$\Delta U_{BE} = -\frac{k_B T}{q} \ln\left(\frac{\Delta I_S}{I_S}(\sigma) + 1\right). \tag{4.21}$$

Figure 4.1 shows the non-linearity of the effect and the higher magnitude for the vertical NPN transistor.

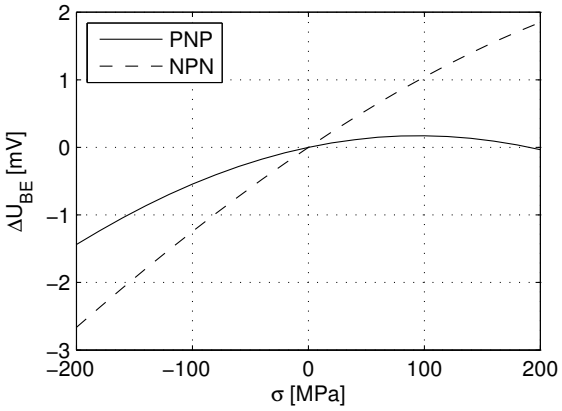



Figure 4.1.: Calculated change of the base emitter voltage by stress in vertical NPN and PNP transistor on a $(100)$ wafer for stress in $[011]$ direction based on the finding of Creemer and French [35].

The voltage with the positive temperature coefficient in a bandgap circuit is generated by two bipolar junction transistors driven at different current densities. The relative change of the saturation current can be related to a change of the PTAT voltage with:

$$\Delta U_{PTAT} = \frac{k_B T}{q}\left[\ln\left(\frac{\Delta I_{S1}}{I_{S1}}(\sigma) + 1\right) - \ln\left(\frac{\Delta I_{S2}}{I_{S2}}(\sigma) + 1\right)\right] \tag{4.22}$$

The stress-induced change of the saturation current only causes a drift of the signal if both transistors are exposed to a different magnitude of stress. Therefore, it is important to realize both transistor arrays in a common-centroid layout [4, p. 357] (a method to arrange devices around a symmetry center) in order to avoid drift by a gradient of stress.

## 4.3. MOS transistor

This section focuses on an enhancement-mode metal-oxide-semiconductor (MOS) field-effect transistor (FET) in saturation region. This is valid for a n-channel MOS transistor with connected drain and gate. In this case the condition $U_{DS} > U_{GS} - U_{Th}$ is valid. The drain source voltage $U_{DS}$ is always higher than the difference of gate source voltage $U_{GS}$ and threshold voltage $U_{Th}$. The saturation behavior with neglected channel length modulation is described by [4, p. 122ff.]:

$$U_{GS} - U_{Th} = U_{DS'} = \sqrt{\frac{2LI_{DS}}{WK_{n/p}}}. \tag{4.23}$$

$I_{DS}$ is the drain source current and the amplification factor is given by:

$$K_n = \mu_n \frac{\varepsilon_{Ox}}{d_{Ox}}; \qquad K_p = -\mu_p \frac{\varepsilon_{Ox}}{d_{Ox}} \tag{4.24}$$

for n- and p-channel devices respectively. The geometry is described by the channel length $L$ and the width $W$.

The stress induced change of the amplification factor can be described by the piezoresistive effect. Compared to the polysilicon resistor in Section 4.1 the MOS transistor has a monocrystalline structure. If the transistor is driven in inversion, the inverse charge carrier type represents the majority type for the current flow. The change of the threshold voltage and the geometry can be neglected [40, 3]. The relation between the mobility and the piezoresistive coefficients is given by:

$$\frac{\Delta K_{n/p}}{K_{n/p}} = \left[\frac{\Delta\mu}{\mu_0}\right]_{ij} = -\pi_{ijkl}\sigma_{kl}. \tag{4.25}$$

By means of Eq. (4.25) the relative change of $U_{DS'}$ reads:

$$\frac{\Delta U_{DS'}}{U_{DS'}} = \frac{1 - \sqrt{\frac{\Delta K_{n/p}}{K_{n/p}} + 1}}{\sqrt{\frac{\Delta K_{n/p}}{K_{n/p}} + 1}} \approx -\frac{1}{2}\frac{\Delta K_{n/p}}{K_{n/p}}. \tag{4.26}$$

Table 4.4.: Longitudinal and transverse piezoresistive coefficients in lightly doped silicon [26] and a MOS inversion layer [3] with the current direction in [011].

| | | lightly doped silicon | MOSFET inversion layer |
|---|---|---|---|
| | | $[10^{-10}\,\mathrm{Pa}^{-1}]$ | |
| p-type | $\pi_l$ | 7.2 | 6.0 |
| | $\pi_t$ | −6.6 | −3.8 |
| n-type | $\pi_l$ | −3.2 | −4.9 |
| | $\pi_t$ | −1.8 | −2.1 |

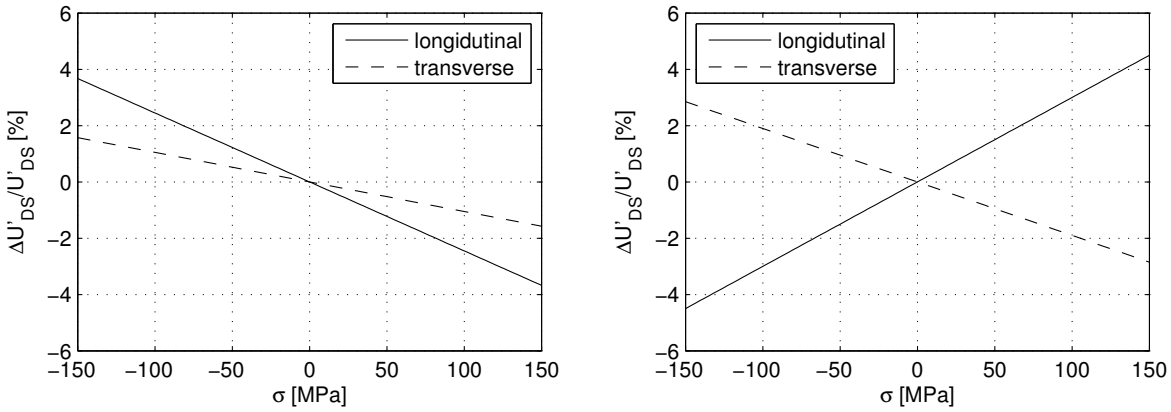
It is sufficient to consider only the linear term in this equation.

The longitudinal and transverse piezoresistive coefficients for monocrystalline silicon with stress applied in [011] direction can be derived from the values measured by Smith [26]:

$$\pi_l = \frac{\pi_{11} + \pi_{12} + \pi_{44}}{2}; \qquad \pi_t = \frac{\pi_{11} + \pi_{12} - \pi_{44}}{2}. \tag{4.27}$$

The piezoresistive effect in the inversion layer in a MOSFET shows small deviations from the observation of a lightly doped material. A more precise study was done by Gallon et al. [3]. The longitudinal and transverse coefficients in the inversion layer and lightly doped silicon are compared in Table 4.4.

The calculated graph of the relative source drain voltage change can be seen in Fig. 4.2. For a compressive stress (i.e. negative stress) in the nMOS transistor the relative change of $U_{DS'}$ increases for both the longitudinal and the transverse case. The increase is stronger for the longitudinal stress. In the pMOS transistor the relative change of $U_{DS'}$ is positive for a compressive transverse stress and negative for a longitudinal compressive stress.




(a) nMOS transistor

(b) pMOS transistor

Figure 4.2.: Calculated relative change of the drain source voltage by stress in an n-channel MOS transistor (a) and a p-channel MOS transistor (b) based on Gallon et al. [3].

# Part II.

# Experimental procedure

# 5. Definition of requirements

As already mentioned in Chapter 3 different causes lead to a mechanical stress in the microchip. The complex manner of the occurring stress in the integrated device and its complex interaction with the device behavior requires a method to evaluate the stress robustness of the whole chip design experimentally. To investigate the relation between stress and the electrical parameter, a measurement method is needed to apply a controlled changeable anisotropic stress to the active layer of the device. The focus of this work is directed on ICs in MLF packages. The applied test stress should simulate solder stress and packaging stress. We look for a method to analyze such devices. The requirements can be summed up as follows:

- Stress level in the range of 100 MPa to 200 MPa
- The focus is on compressive stress
- Minimal preparation effort to analyze a chip in MLF package

The method of choice is a cantilever beam (see Fig. 5.1). The beam is a standard printed circuit board with a mounted chip in a MLF package. Due to the large area of the soldered joint between the EP and the copper it is possible to apply a stress in the active layer of a device under test (DUT) by bending the beam. The beam is fixed at one end. A certain displacement is done with a forcer mounted on a linear positioning stage. Although the applied stress is uniaxial, it reasonably well simulates the stress created

during the device production as specified in Chapter 3. Especially the solder stress, which is normal to the die surface, is comparable with the stress applied with the beam method.

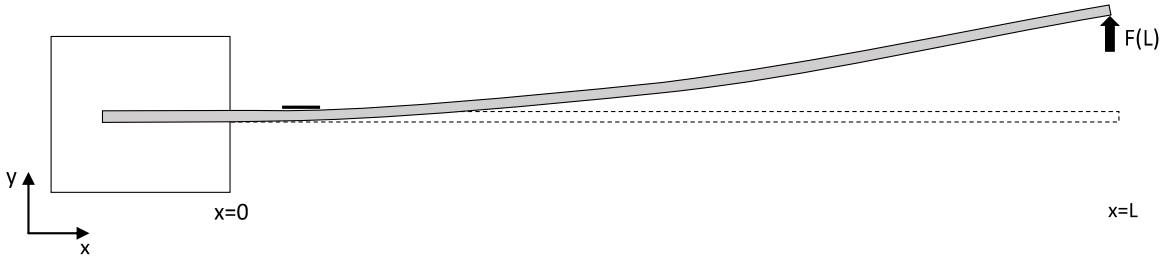



Figure 5.1.: Cantilever beam with one fixed end at $x = 0$ and a force $F$ at the position $x = L$.

# 6. Stress in the cantilever beam

There are many different approaches to investigate a beam structure under mechanical load. The accuracy of the obtained solution is depending on the complexity of the method. In this section we will start with the simplest approach, the Euler-Bernoulli theory. How a detailed solution is obtained with a computational method is shown at the end of this chapter.

## 6.1. Simple beam theory

The Euler-Bernoulli beam theory allows the description of a cantilever beam with a load at the end [41, p. 242ff.]. The applied force to a structural element supported or fixed at one or two ends causes a moment bending the element. This so-called bending moment $\vec{M}$ is given like any torque by:

$$\vec{M} = \vec{r} \times \vec{F}. \tag{6.1}$$

$\vec{F}$ is the force and $\vec{r}$ is the position vector in this equation. We take a closer view on a structure shown in Fig. 5.1. The point force $F_y(L)$ at the end of the beam generates the bending moment according to:

$$M(x) = F_y(x - L). \tag{6.2}$$

It is zero at the point of the force $x = L$ and has its maximum at the fixed end at $x = 0$. To calculate the stress at a certain distance away from the neutral axis, the geometric shape of the beam is described with the second moment of area:

$$I = \int_A y^2 \, dA = \frac{bh^3}{12} \tag{6.3}$$

with rectangular cross-section geometry of width $b$ and height $h$. Now the material parameter of the beam has to be considered. The static bending of the beam is described by the differential equation:

$$\frac{d^2}{dx^2}\left(EI\frac{d^2w(x)}{dx^2}\right) = q(x). \tag{6.4}$$

The deflection is denoted with $w(x)$ and related to the load $q(x)$. The product of the elastic modulus $E$ and second moment of area yields the flexural stiffness $D$.

A point load is taken into account by the Dirac delta function $\delta(x - L)$. If the elastic modulus and second moment of area are independent of $x$, Eq. (6.4) gets simpler. Together with the conditions of continuity at the boundary we end up with the differential equation system:

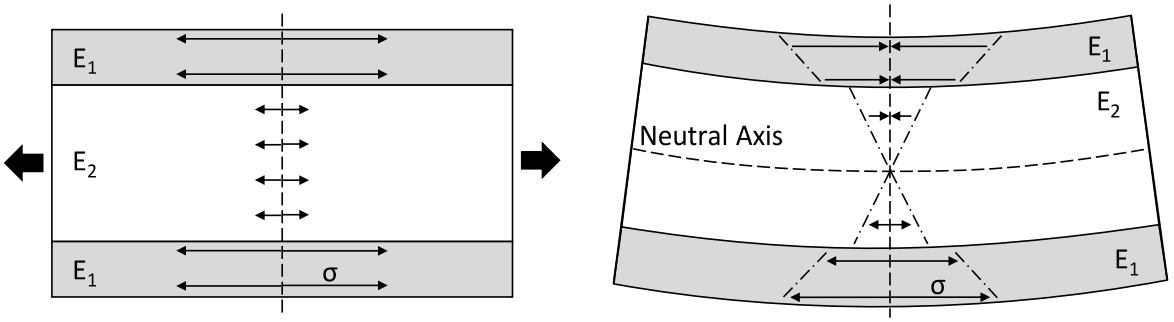
$$\begin{gathered} EI\tfrac{d^4w(x)}{dx^4} = F_y\delta(x-L) \ ; \\ \\ w(0) = 0; \quad \tfrac{dw(0)}{dx} = 0; \\ \\ \tfrac{d^2w(L)}{dx^2} = 0; \quad \tfrac{d^3w(L)}{dx^3} = 0. \end{gathered} \tag{6.5}$$

The solution of the differential equation is given by:

$$w(x) = \frac{F_y x^2(3L - x)}{6D}. \tag{6.6}$$

We are interested in a local stress at a certain position $x$ at the surface of the beam depending on the deflection at the end of the beam $w_L$. This is given by:

$$\boxed{\sigma(x) = \frac{F_y h(x-L)}{2I} = \frac{3w_L Eh(x-L)}{2L^3}}. \tag{6.7}$$




(a) Tensil stress (b) Bending stress

Figure 6.1.: Comparison of stress in a multilayer structure with different elastic moduli.

**Conclusion for a chip analysis technique:** The deflection at the end of the beam is named displacement in the following. Equation (6.7) can be used for a first estimation of how the beam has to be shaped to meet the specified requirements in Chapter 5. A high stress is required to come in the range of a few hundred MPa and, therefore, the device under test (DUT) is to place next to the fixed end. The stress is proportional to the elastic modulus and the height of the beam. The elastic modulus is limited by the available materials for PCBs. In this work we will use FR-4 (standard compound material for circuit boards) with a thickness of 3 mm.

## 6.2. Multilayer beam theory

The local stress on a beam has been described in Section 6.1. In this section we take a closer view on how the stress is transferred through different materials to the active layer of the DUT placed on the beam. The stress at a certain point can be calculated analytically, but one has to consider the different elastic moduli of the materials. If an axial load is applied to a sandwich material as shown in Fig. 6.1a, the strain $\varepsilon$ is the same in every layer, but the stress $\sigma$ is determined by the elastic modulus $E_i$ of the

material $i$. The elastic moduli of the bend beam materials used in this work are listed in Table 6.1. The approximation used in this section is summarized as "Engineering sandwich beam theory" [42]:

- Shear stress in all layers is neglected.
- No change in thickness takes place.

Table 6.1.: Elastic moduli of materials used in the beam structure [19, 21]

| Material | $E$ [GPa] |
|---|---|
| Copper | 115 |
| FR-4 | 22 |
| Silicon [110] | 170 |

The first problem in the analysis of beam bending is to figure out the neutral axis. For a symmetric geometry the neutral axis is in the middle of the beam. Figure 6.1b shows a segment of a bended sandwich-structured beam. The position $x$ and radius $\rho$ of the neutral axis of the beam determine the strain. The radius is given by:

$$\rho = \frac{1}{M(x)} \sum_i E_i I_i. \tag{6.8}$$

We have to sum over all materials with different elastic moduli $E_i$. The sum of the products $E_i I_i$ is the equivalent to the flexural stiffness $D$ of the sandwich structure. To describe a sandwich structure it is necessary to carry out the integral for each section separately or to recalculate the second moment of area with the parallel axis theorem by means of:

$$I_i = \frac{b_i h_i^3}{12} + y_i^2 A_i. \tag{6.9}$$

In this case $y_i$ denotes the position of the area centroid, $b_i$ is the width, $h_i$ is the height and $A_i$ is the cross-sectional area of the $i$-element of the beam.

Table 6.2.: Force for a 20 mm displacement of the beam at $x = 190\,\text{mm}$.

| Method | $F$ [N] |
|---|---|
| Calculated | 21.1 |
| Measured | $22 \pm 2$ |

The solution of the differential equation for the sandwich structure in analogy to Eq. (6.5) is given by:

$$w(x) = \frac{F_y x^2 (3L - x)}{6 \sum_i E_i I_i}. \tag{6.10}$$

For the measurements in this work we are interested in the compressive stress in the active layer of the chip. We can calculate it by means of the equation:

$$\boxed{\sigma_j(x) = \frac{E_j y}{\rho} = \frac{E_j y F_y (x - L)}{\sum_i E_i I_i}}. \tag{6.11}$$

**Calculation of the mechanical stress created with the cantilever beam technique:** The findings of the multilayer beam theory can be used to calculate the stress in the active area of the DUT during a test with the cantilever beam. The beam consists of FR-4 material (thickness 3 mm) with a 35 µm thick copper layer on the top and bottom surface. The distance between the fixed end to the forcer is 190 mm and the width 30 mm. The center of the chip is placed 18 mm away from the fixed end in the middle of the beam. The lead frame of the chip is 250 µm in thickness and the size is 4.7 mm × 4.7 mm. The die has a height of 250 µm and a size of 4.1 mm × 4.1 mm. The calculated stress in silicon for $x = 18\,\text{mm}$ is plotted in Fig. 6.2 up to a displacement of 20 mm and a beam length of $L = 190\,\text{mm}$. The required force for the displacement can be calculated with Eq. (6.6). The calculated value and the measured value are listed in Table 6.2.

## 6.3. Simulation of stress in a multilayer beam

An improved calculation of the stress at a position in the beam is achieved by the so-called "Linear sandwich theory". In contrast to the "Engineering sandwich beam theory", this theory takes into account the shear-stress in the core. This can lead to a better solution. The finite element method (FEM) is the state of the art in structuring mechanics and applicable for many more complex problems. So a FEM software package is the approach of choice to extract a detailed solution.

To get used with the working steps during a FEM analysis, a short overview should be given here. The starting point for the simulation is a structural model. This model contains the geometries of the structure and it is the base to generate the FEM-grid. A beam can usually be simplified as a two dimensional problem by an $xy$-cutting-plane through the center of the beam. The width comes in again by relating each point in the grid with the corresponding width. The last step in the pre-processing is the consideration of the boundary conditions [43]. One has to consider the different scale of the beam, in the range of millimeters in thickness and centimeters in length, as well as the scale of the chip, in the range of micrometer in thickness and in the range of millimeters in length. The very thin layer of adhesion between the chip and the lead frame as well as the solder with a few micrometer between the lead frame and the PCB are neglected. The simulation was done with a larger grid for the beam to find the boundary conditions for the chip simulation. The simulation of the structure of the lead frame and die was done with a finer grid. The stiffness tensor and Euler–Bernoulli beam theory lead to a equation system we can solve for finite elements of the structure. The simulation in this work has been carried out with the simulation software package COMSOL Multiphysics®.

We can compare the solution of the simulation with the analytic calculation from

Section 6.2. The plot is related to the stress at the center of the active area of the die. As we can see in Fig. 6.2 the FEM simulation ends up with a smaller stress. The reason is the neglected shear-stress in the sandwich theory. The simulation was also carried out for a die encapsulated in a mold compound. The stress for a beam displacement of 20 mm at $L = 190$ mm causes a compressive in-plane stress of an absolute value of 110 MPa in an encapsulated die and an absolute value of 130 MPa in a die without mold compound. This leads to a strain in the silicon surface of $-0.07\,\%$ in the encapsulated case and $-0.08\,\%$ in the case without mold.

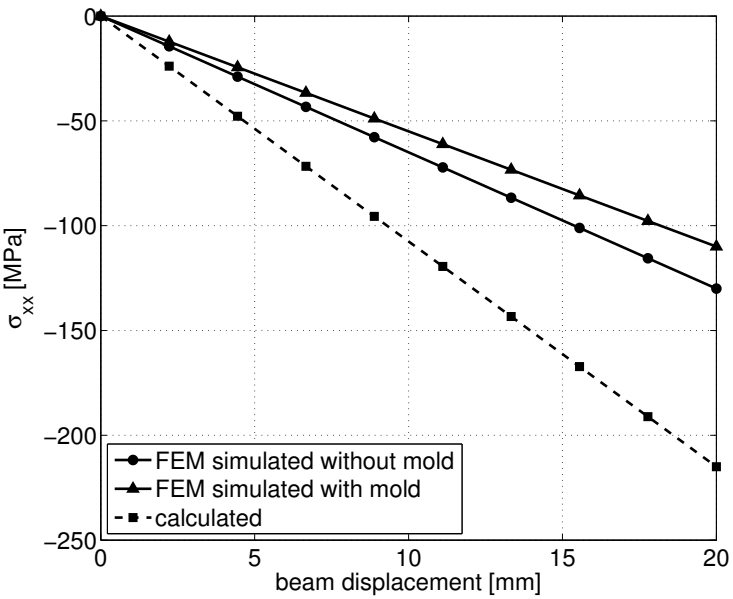
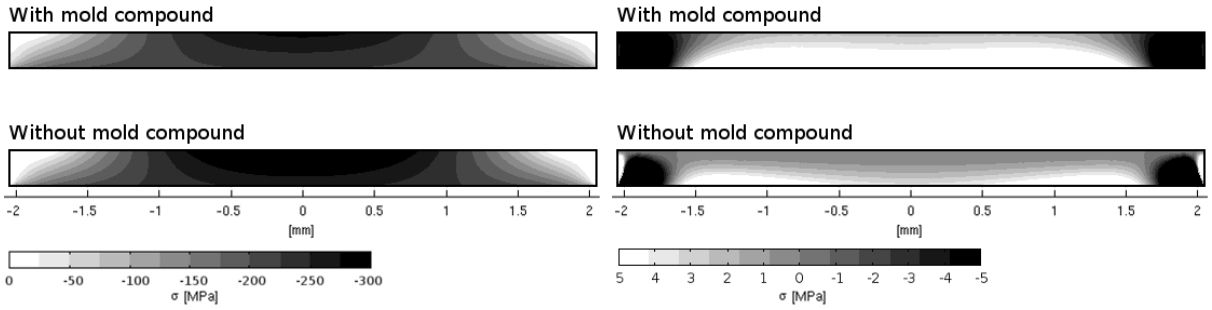



Figure 6.2.: Calculated and simulated stress in the center of the active area of the silicon die located on the beam at $x = 18$ mm during displacement.

The benefit of the simulation is that one can extract a whole stress profile of the chip. We can do this for the planar stress and also for the stress perpendicular to the surface of the die. The planar stress is maximal at the center of the die as one can see in Fig. 6.3a. There is a region next to the edge of the die, where a high change of the planar stress is present. This stress gradient can lead to a mismatch if matched structures are placed in

this region.

The change in thickness is not neglected in the simulation and this causes a small stress (in the range of $\pm 5\,\mathrm{MPa}$) perpendicular to the surface. This stress is constant on the surface if the simulation is done without mold. The simulation with mold shows a small compressive stress on the edge of the die as one can see in Fig. 6.3b. As already mentioned in Chapter 3, filler particles can lead to a local stress perpendicular to the surface. This means that in practice randomly distributed stress fields can occur around such particles.




(a) In plane stress.

(b) Stress perpendicular to the surface.

Figure 6.3.: Stress profile during bend test with a displacement of $50\,\mathrm{mm}$.

# 7. Test chip for mechanical stress study

In the previous section we discussed the stress and its distribution occurring in a near CSP mounted on a cantilever beam. In this section the used application-specific integrated circuit (ASIC) and the setup for the evaluation is presented.

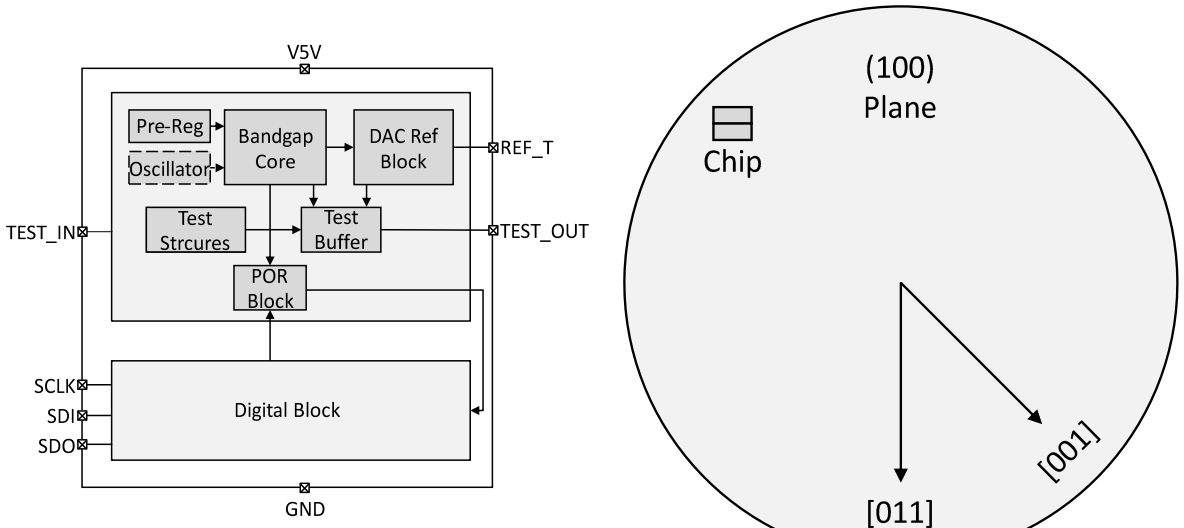



Figure 7.1.: (a) Block diagram of the test chip, (b) orientation of the test chip and the crystallographic directions on the wafer.

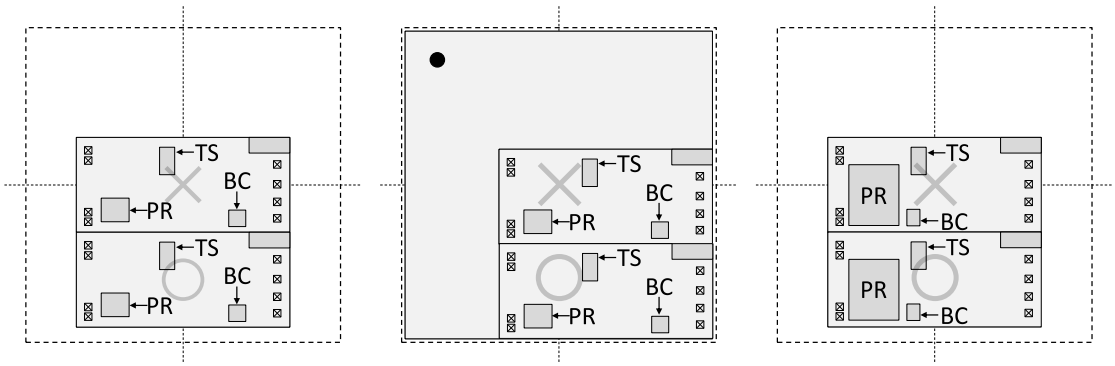
The test chip is produced in the H35 process by ams AG. The block diagram is illustrated in Fig. 7.1a. There is an analog block containing a bandgap circuit as well as analog test

structures. The digital block together with the digital input offers options to choose the test signals. The output voltage is routed with a test buffer to the test output. Two different test chips have been produced in the further work, which we name test chip 1 and test chip 2. Test chip 2 makes use of an oscillator for the improved bandgap core with an auto-zero offset cancellation. The pre-regulator block generates a reference voltage of 3 V. This voltage is given to the bandgap core. The bandgap voltage is amplified to 4.5 V in the DAC reference block. The bias currents required for the test structures are also generated from the pre-regulator with a current mirror circuit. A power-on reset block is included in the design. The POR signal is generated when both supply voltage and bandgap output are in the required range. This signal is given to the digital block. The test structure block includes (see also Fig. 7.3, below):

- a polysilicon resistor,
- a diode connected nMOS transistor,
- a diode connected NPN bipolar junction transistor, and
- a differential operation amplifier.

When the necessary enable signal for each test structure is given, the structure is biased as shown in Fig. 7.3d and the voltage or current can be measured through the TEST_OUT pin. The test buffer is used to measure the voltage output of a structure or a reference voltage specified with the digital block. The buffer offset can also be measured by a given signal from the digital block. By activation of a given test structure, a bias current is delivered to the structure and the voltage drop can be measured. The polysilicon resistor offers the additional possibility to measure the current through it.

The standard wafers used in the H35 process and in this work are aligned with the surface to the $(100)$ plane as shown in Fig. 7.1b. The cutting is done in the $[011]$ and $[0\bar{1}1]$ direction.




(a) Test chip 1, die size: 2400 µm × 2777 µm

(b) Test chip 1, die size: 4100 µm × 4100 µm

(c) Test chip 2, die size: 2400 µm × 2777 µm

Figure 7.2.: Placement of the die on the lead frame of the pre-molded package. In each case, there is one chip at the center of the package marked with a cross and one chip at the edge of the package marked with a circle. PR=pre-regulator, TS=test structure, BC=bandgap core.

The test chips have a size of 1200 µm × 2777 µm and two of them are together on one die, resulting in size of 2400 µm × 2777 µm as shown in Fig. 7.2a and Fig. 7.2c. Further specimens with an additional region of silicon outside the actual area of the IC have been produced from test chip 1. Therefore, the test structure of one chip (marked with a cross) is surrounded by silicon and placed in the center of the die with a total size of 4100 µm × 4100 µm shown in Fig. 7.2b. The dies are glued to a pre-molded MLF package and encapsulated with a glob top (encapsulation method usually used in chip-on-board technology). Figures 7.2 shows also how the dies are placed on the area of package lead frame. The grey area is the size of the silicon. The dashed line marks the area of the exposed pad. One chip of the die is located at the center of the package (marked with a cross) and one chip is located at the edge of the package (marked with a circle). The placement of the test structures, the pre-regulator, and the bandgap core are also shown in the picture.

The chip is soldered on the beam in two different orientations, i.e., with the chip long side parallel to the beam axis, or twisted by 90° with the chip long side perpendicular to the beam axis. Table 7.1 provides an overview of the different test chip arrangements in the package and the orientation of the package on the beam.

Table 7.1.: Different arrangements of the test chip in the package and on the cantilever beam.

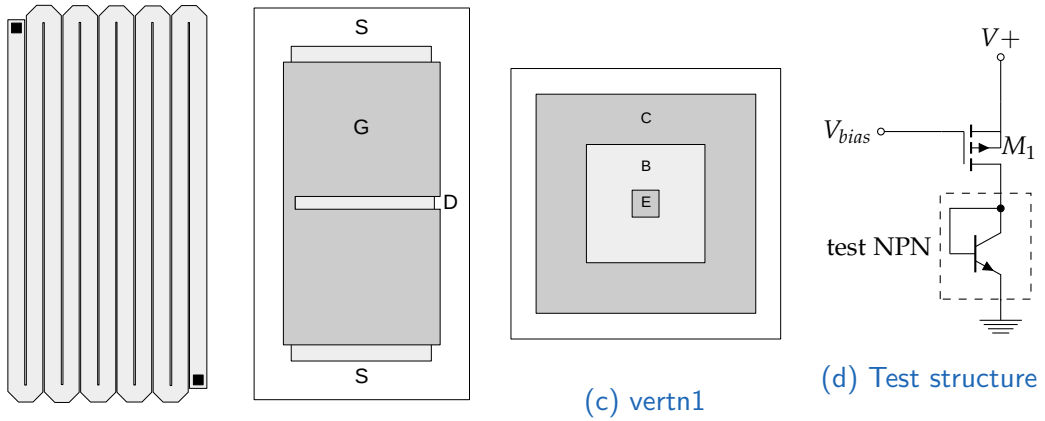
| Orientation | Position on EP | Die size |
|---|---|---|
| 90° | Center region (marked with cross) | Small, 2400 µm × 2777 µm |
| 0° | Edge region (marked with circle) | Big, 4100 µm × 4100 µm |

## 7.1. Test stucture: Polysilicon resistor

The resistor is fabricated in the poly2 layer [44] of the H35 process with a sheet resistance of 50 Ω/□. The resistor value is 14 kΩ and it is made out of n-type polysilicon. It has a meander geometry as one can see in Fig. 7.3a and a total length of 1.05 mm. The width of the trace is 4 µm. Transverse stress is perpendicular to the current direction and longitudinal stress is parallel to the current direction.

## 7.2. Test stucture: nMOS transistor

The nMOS transistor has two gate areas. The length of each channel is 10 µm and the width is 2 × 10 µm. The top view is shown in Fig. 7.3b. The behavior under stress can also be split into transverse and longitudinal.




(a) rpoly (b) nmosim (c) vertn1 (d) Test structure circuit

Figure 7.3.: Test stuctures of test chip 1 and test chip 2.

## 7.3. Test stucture: NPN bipolar junction transistor

The NPN bipolar junction transistor is a circular arrangement of emitter, base and collector. The main current direction of this vertical transistor is perpendicular to the plane. The top view is shown in Fig. 7.3c.

## 7.4. Bandgap circuit

Test chip 1 and test chip 2 are equipped with two different bandgap cores. The position of the bipolar junction transistor of the bandgap is marked in Fig. 7.2. The bandgap is similar to the CMOS bandgap discussed in Chapter 2. The current level is stabilized with an additional p-channel MOS transistor. The circuit is shown in Fig. 7.4. Bandgaps of this type require a startup circuit. A pre-regulator supplies the bandgap circuit with a voltage of 3 V. The BJT in the bandgap core is a vertical NPN. Test chip 1 has a transistor ratio of 32:128 and test chip 2 has a transistor ratio of 12:96. The bandgap of test chip 2 is equipped with an auto-zero offset cancellation.

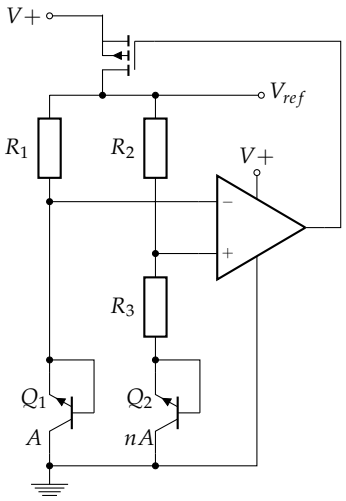



Figure 7.4.: CMOS bandgap of test chip 1.

Depending on the application (discussed in Chapter 2) it may be necessary to amplify the output voltage of the bandgap circuit for further use. The amplifier of the test chip (DAC reference block) is dimensioned to amplify an input voltage of 1.232 V to an output voltage of 4.500 voltage, which corresponds to an amplification $\beta$ of is 3.652 V.

# 8. Measurement setup

The test chip is soldered with a reflow process to the circuit board. Lead solder proved to be more suitable than lead-free solder. The beam with the mounted test chip is integrated in a measurement setup as shown in Fig. 8.1. The operation of the chip and the setup is controlled by means of a LabVIEW program. The beam is connected with two interface boards. The digital board enables the communication with the setup computer to bring the chip in each test mode. The analog signals are routed to the digital voltmeter. The current measurement can be done by means of an external resistor with a value of 10 kΩ. The bending force is applied with a precision translation stage.

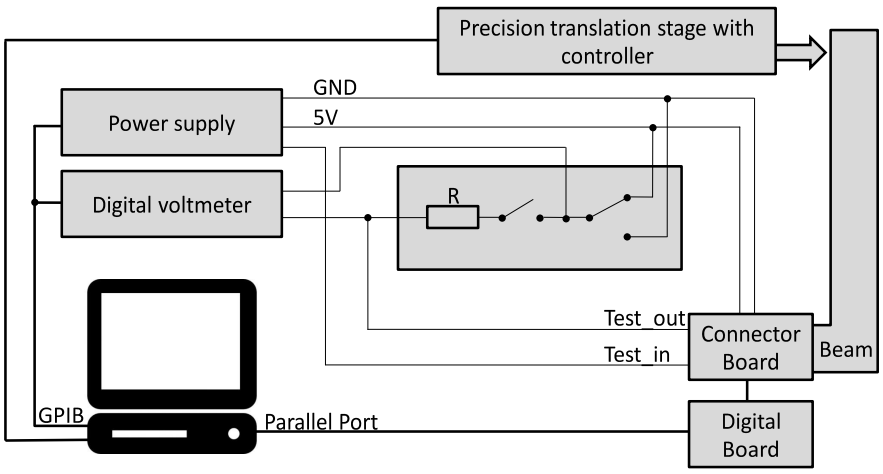



Figure 8.1.: Setup for automatic stress measurement.

The temperature was not controlled separately. The measurement was done in a laboratory with air conditioner and lasted approximately two minutes for one sample. The low power consumption together with the big copper plane of the beam ensures that the temperature remains constant during the measurement.

# Part III.

# Experimental results and discussion

# 9. Experimental evaluation of stress distribution

The beam method defined in Chapter 5 was used to characterize a test chip. In this part we will discuss details of the findings. The polysilicon resistor of the test chip underlies the linear piezoresistive effect. Therefore, it is a appropriate device to measure the in-plane stress at the silicon surface.

At first it is necessary to correlate the piezoresistive effect with the absolute stress deduced from the test with the beam method. The result should be comparable to the piezoresistive effect in literature as discussed in Section 4.1 in order to verify the calculation and simulation in Chapter 6.

Furthermore, the measurements can be used to make a statement about the stress distribution on the surface and may allow a comparison of different die sizes. This will lead to rules for the layout to prevent high stress at critical blocks of the device like the bandgap core. The test chips, which are presented in Chapter 7 were placed on a PCB beam and integrated in the the measurement setup described in Chapter 8. Figure 8.1 shows the setup. The beam deflection is set with a precision translation stage which is controlled from a LabVIEW program. The parameter (current and voltage) of the DUT can be measured for each deflection of the beam.

## 9.1. Correlation with theoretical description

As shown in Fig. 7.2b, one of the test structure areas (marked with a cross) is in the center of the die. In Chapter 3 the linear behavior of the polysilicon resistor for moderate stress level was characterized. The relation between stress and relative change of the resistivity is given by Eq. (4.6). Therefore, this device becomes suitable to investigate a relative uniaxial stress level in the plane of the chip surface. Together with the result of the stress simulation in Section 6.3 we can calculate the piezoresistive effect of the polysilicon resistor of the test chip from the data taken during the beam bending test. The simulation shows a compressive stress in the center of the die (at the position of the polysilicon resistor) of $-110\,\mathrm{MPa}$ for a beam with the described geometries during a displacement of 20 mm. With the elastic modulus (in Section 3.3) for silicon in the [110] direction, the equation for the elastic regime $\varepsilon = \sigma / E$ yields a strain of $-0.065\,\%$. The test was done with two orientations of the test chip on the beam to measure the transverse and the longitudinal piezoresistive effect.

With the Poisson ratio $\nu = 0.22$ of polycrystalline silicon and Eq. (4.5) we can calculate the relative change of the resistivity per unit strain

$$\left(\frac{\Delta\rho}{\rho\epsilon}\right)_t = \left(\frac{\Delta R}{R\epsilon}\right)_t + 1; \tag{9.1}$$

$$\left(\frac{\Delta\rho}{\rho\epsilon}\right)_l = \left(\frac{\Delta R}{R\epsilon}\right)_l - 2\nu - 1. \tag{9.2}$$

The results are shown in Table 9.1. The measurement of the polysilicon resistor is described more detailed in Section 10.3.

The piezoresistive effect in n-type polysilicon was calculated from the piezoresistive coefficients in monocrystalline silicon in Section 4.1. It should be possible to compare the calculated piezoresistive effect in Table 4.2 with the measured piezoresistive effect in Table 9.1 under the assumption that stress provided from the simulation is in accordance

with the real stress applied with the beam method. The longitudinal value $(\Delta\rho/\rho\epsilon)_l = -6.9$ calculated from the literature for a carrier concentration of $1 \times 10^{17}\,\mathrm{cm}^{-3}$ is equal to the measured value in Table 9.1. There is a small deviation of the transverse value calculated from the literature of 4.5 and the measured value of 4.2. The reason for this may be the morphology of the grains, which is neglected in the calculation, or the meander shape of the resistor (the transverse stress is longitudinal at the turn of the meander and vice versa as one can see in Fig. 7.3a). Furthermore, the carrier concentration of the polysilicon resistor on the test chips was not measured separately. However, this agreement of the measured relative resistivity change per unit strain and the calculated one is an indicator that the real stress in the die matches with the simulation in Section 6.3.

Table 9.1.: Resistivity change of the polysilicon resistor per unit strain.

| | |
|---|---|
| $\left(\frac{\Delta\rho}{\rho\epsilon}\right)_t$ | 4.2 |
| $\left(\frac{\Delta\rho}{\rho\epsilon}\right)_l$ | -6.9 |

## 9.2. Distribution of stress on the chip surface

The die attached to the beam has two equal test structures. The uniaxial stress is applied alongside the beam. No stress is applied perpendicular to the long side of the beam. In Fig. 9.1 the chip is shown in the two possible orientations on the beam. The 0° figure shows the chip orientation for the transverse measurement and the 90° figure shows how the chip is orientated for the longitudinal measurement. In the 0° position $\Delta R/R$ and, therefore, the stress at maximum displacement of the beam is almost the same for both test structures marked with a cross and a circle. Whereas a different $\Delta R/R$ as a measure for stress prevails in the two test structures in Fig. 9.1, if the chip is in the

90° orientation. We have seen the stress distribution already in the simulation result in Fig. 6.3a. The simulation shows, that the stress is about 25 % smaller 1 mm away from the center of the die, than in the center. The measurements of $\Delta R/R$ at the different places is in good accordance with the stress distribution in the simulation result.

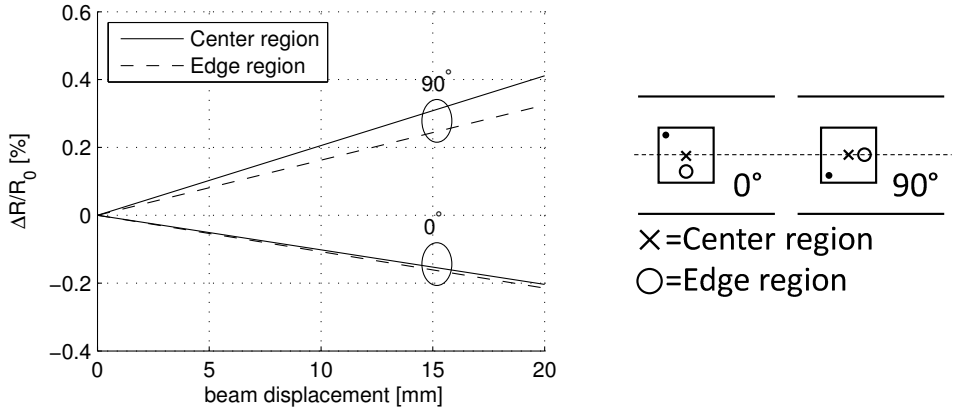
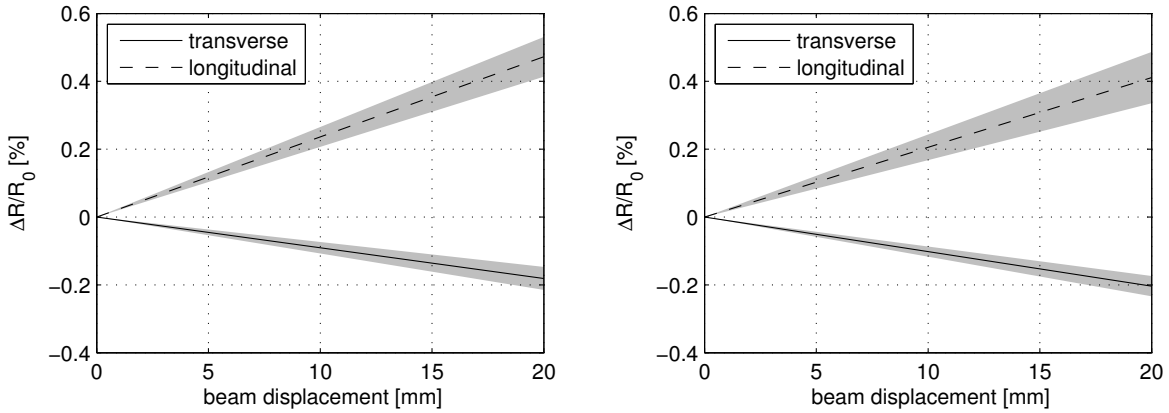



Figure 9.1.: Comparison of the relative change of the resistance by different position on the die surface and orientation on the beam, for 4100 µm × 4100 µm die size.

## 9.3. Comparison of different die sizes

In the previous sections the qualitative stress level in the die with a size of 4100 µm × 4100 µm has been described. The same test was also done with dies with a size of 2400 µm × 2777 µm. The location of the die on the EP was similar to that of the big die. Figure 7.2a shows the exact location of the small die and Fig. 7.2b shows the exact location of the big die with the test structure in the center of the package (marked with a cross). Figure 9.2a shows the longitudinal and transverse change of the relative resistance of the small die and Fig. 9.2b shows the relative resistance changes of the big die during the bend test.

The transverse resistance change is 20 % higher in the small die than in the big die. This means there is a higher stress present in the resistor at the edge of the small die than in the resistor at the center of the big die at the same position on the EP. This can be due to the higher stress (because of a smaller flexural stiffness) in the center of the exposed pad which is transmitted to the resistor at this position. Also the thickness of the glob top is higher in the center of the die and the long side of the chip is better enclosed.




(a) Die size: 2400 µm × 2777 µm

(b) Die size: 4100 µm × 4100 µm

Figure 9.2.: Stress-induced change of the polysilicon resistor in the center of the package during beam displacement. The grey-shaded indicates the standard deviation of the measurement. Comparison of small die (a) and big die (b).

# 10. Experimental evaluation of electronic components and circuits

It was shown in the previous chapter with the measurements of the polysilicon resistor that a certain stress can be applied with the beam method presented in 5. The compressive stress and its distribution is in accordance with the simulation in Section 6.3. The test chip described in Chapter 7 contains further test structures and two different bandgap circuits. The signals of the test structures are routed to a buffer. At the beginning of this chapter it will be shown that this buffer is not influenced by mechanical stress during the test. The other sections in this chapter deal with the influence of stress on the bandgap cores and test structures.

The investigation of the test structures only focuses on test chip 1, because the test structures of both test chips are equal. With respect to the stress-induced change of the bandgap voltage, a comparison of test chip 1 and test chip 2 will be performed.

## 10.1. Buffer offset during bend test

The test signals in the test chip can be routed to the test buffer. The buffer ensures that the test structures are not electrical loaded too high during the measurement. The signal

is available at a low impedance point. The buffer is implemented with an operational amplifier (op-amp). The offset of the buffer was in the range of $\pm 4\,\mathrm{mV}$ for all samples . During the bend test the buffer offset change was below $\pm 100\,\mu\mathrm{V}$. The range and an exemplary graph of the buffer offset is shown in Fig. 10.1.

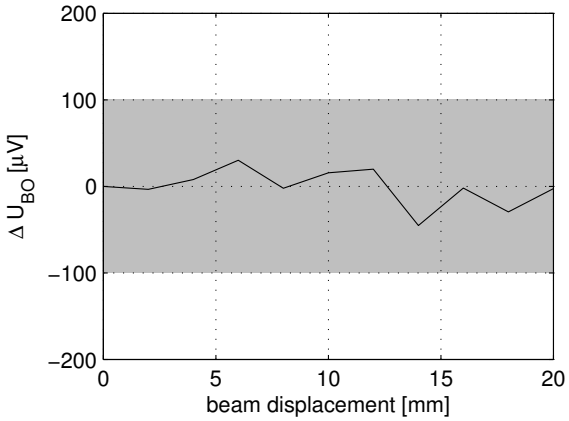
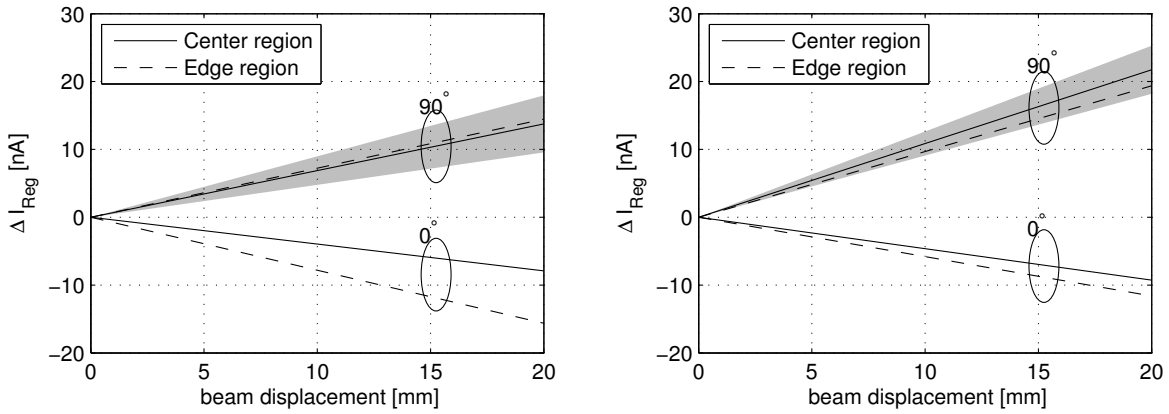



Figure 10.1.: Buffer offset of one exemplary sample of a chip in the center with a die size of $4100\,\mu\mathrm{m} \times 4100\,\mu\mathrm{m}$ (solid line). The grey area is the range of minimum and maximum change during the bend test of all samples.

## 10.2. Pre-regulator current

The bias current for the test structures is derived from the current in the pre-regulator in four stages. Although it is not possible to measure the current through the test structure we can measure this pre-regulator current. The measured value of the pre-regulator current was $I_{Reg} = (1.65 \pm 0.03)\,\mu\mathrm{A}$. The measured influence of the stress on the pre-regulator current was linear. The effect tends to be smaller in the big die in the center region as shown in Fig. 10.2.




(a) Die size: 4100 µm × 4100 µm

(b) Die size: 2400 µm × 2777 µm

Figure 10.2.: Stress-induced change of the pre-regulator current during stress in big die (a) and small die (b). A graph for the chip in the center of the package and for the chip at the edge of the package is shown as specified in Figure 7.2.

## 10.3. Polysilicon resistor under mechanical stress

The bias current for the polysilicon resistor is generated from the pre-regulator with a current mirror. We measured both the current and the voltage drop at the resistor, in order to calculate the change of the resistor. The test was done with five samples measured in longitudinal direction and five samples in transverse direction. The voltage drop $U_R$, current $I_R$, and calculated resistance $R$ through the unstressed resistor are measured as follows:

- $U_R = (1.14 \pm 0.02)\,\mathrm{V}$
- $I_R = (82 \pm 2)\,\mu\mathrm{A}$
- $R = (14.0 \pm 0.2)\,\mathrm{k\Omega}$

The variation of 1.5 % the resistance is typical for polysilicon resistors.

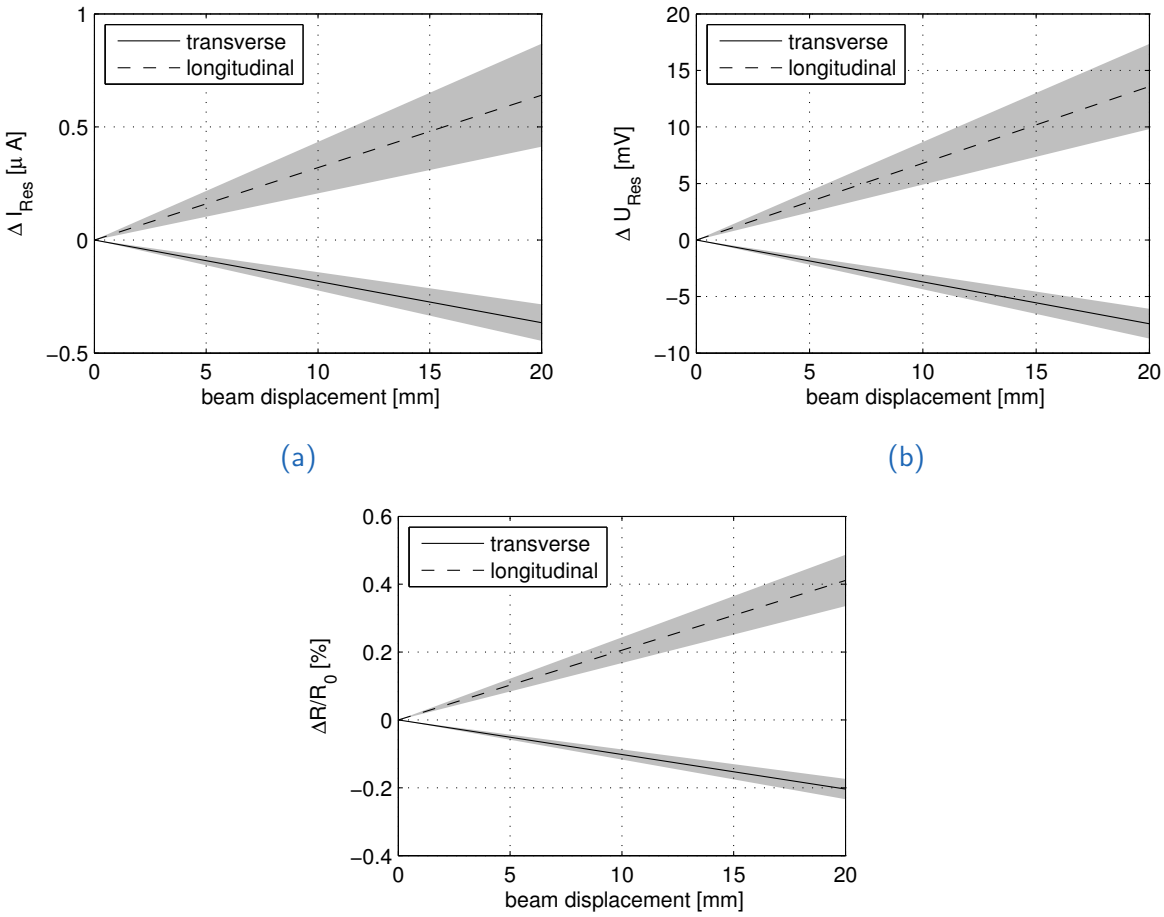



Figure 10.3.: Stress-induced change of the polysilicon resistor (c), the current through the resistor (a) and the voltage drop (b) during beam displacement.The grey area marks the standard deviation of the measurement. Die size: $4100\,\mu\mathrm{m} \times 4100\,\mu\mathrm{m}$.

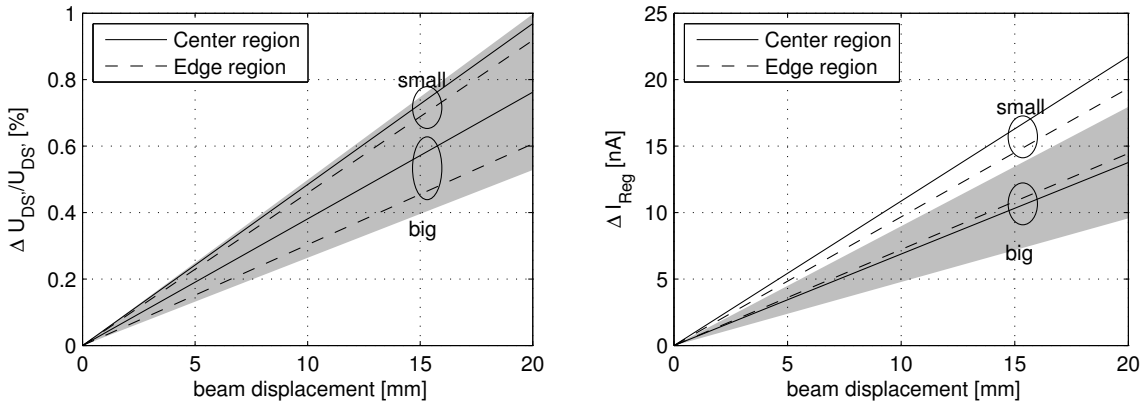
As one can see in Fig. 10.3a the current change $\Delta I_{Res}$ shows a distinct variation with the stress. With the voltage drop over the resistor and Ohm's law $R = U/I$ we can calculate the resistance. The relative change of the resistance is shown in Fig. 10.3c. The gauge factors are defined by Eq. (4.5). The part of the longitudinal gauge factor coming from geometric variation is given with $1 + 2\nu$ and yields 0.56 in polysilicon. In transverse case the geometric part is simply equal to $-1$. By dividing the relative change of the resistance by the strain ($-0.065\,\%$ at beam displacement of 20 mm) we get a transverse gauge factor of 4.0 and a longitudinal gauge factor of $-6.5$ which is much higher than the geometric part of the gauge factor usually observed in metallic strain gauges. The transverse piezoresistive effect is positive and the longitudinal effect is negative.

## 10.4. MOSFET under mechanical stress

The current for the n-channel test MOS transistor is generated from the pre-regulator bias current through a p-channel MOS transistor (see Fig. 7.3d). If a stress is applied to the die not only the mobility in the test transistor is changed but also the mobility in the p-channel MOSFET is changed as described with Eq. (4.25). This causes an error in the measured signal. The current is proportional to the mobility. The mobility in the p-channel MOS transistor increases with compressive stress in the longitudinal direction and decreases in the transverse direction. The bias current is proportional to the mobility in the p-channel MOS transistor. The compressive stress in the n-channel MOS transistor causes an increase of the voltage drop as shown in Fig. 4.2a if we consider the drain current as constant. The measured signal is a sum of the mobility change in the test MOS transistor and a stress-induced change in other devices in the circuit.

We discussed how to relate the drain-source voltage to the change of the mobility and

introduced the difference of $U_{DS'} = U_{DS} - U_{Th}$ in Section 4.3. The threshold voltage of the n-channel MOS device is 0.7 V. The drain-source voltage $U_{DS}$ without stress was $(1.137 \pm 0.005)$ V. Figure 10.4a shows a comparison of the longitudinal relative change of $U_{DS'}$ during the beam displacement in the small and the big die in the center and the edge region of the package as shown in Fig. 7.2a and Fig. 7.2b. The trend is a higher relative change of $U_{DS'}$ in the dies with the size of 2400 µm × 2777 µm than in the dies with a size of 4100 µm × 4100 µm.




(a) (b)

Figure 10.4.: Comparison of relative change of $U_{DS'}$ (a) and pre-regulator current (b) for longitudinal stress. Small means the 2400 µm × 2777 µm dies and big means the 4100 µm × 4100 µm dies, the grey area is the standard deviation of the samples with the big dies at the center region.

As already mentioned the difference cannot be exclusively attributed to the position of the test structure but may also arise from the position of the pre-regulator and of current mirror MOSFETs (see Fig. 7.3d) which produce the bias current for the test structures. The current through the test MOSFET cannot be measured but it is derived from the pre-regulator current in four stages. The pre-regulator current for the same groups is shown in Fig. 10.4b.

During the transverse measurement (not shown) the effects more or less cancel out, as residual signal randomly a decrease or an increase in the same group of samples occurred during the measurement.

## 10.5. Bipolar junction transistor under mechanical stress

The theoretical change of the base emitter voltage during a uniaxial stress is not linear (see Fig. 4.1). There is a first and second order piezojunction coefficient. The second-order coefficient is smaller by orders of magnitude than the first-order coefficient of the NPN transistor. Therefore, the stress-induced voltage change is nearly linear but it depends also on the initial tension. As discussed in Section 10.4 there is also an influence coming from the bias current generated from the pre-regulator. Unfortunately it is not possible to make any new statements about the the BJT test structure with the measurement (not shown).

## 10.6. Experimental evaluation of a bandgap circuit

To analyze the bandgap circuit we start with the pre-regulator voltage, which we can measure separately. The pre-regulator voltage in the unstressed chips was different for test chip 1 and test chip 2. We measured:

- Test chip 1: $U_{Reg} = (2.69 \pm 0.01)V$
- Test chip 2: $U_{Reg} = (2.99 \pm 0.01)V$

Depending on the chip orientation the measured voltage change was negative or positive and in the range of $-4.5\,\mathrm{mV}$ to $4.5\,\mathrm{mV}$. It is not expected that this small change of the supply voltage can change the bangap reference voltage.

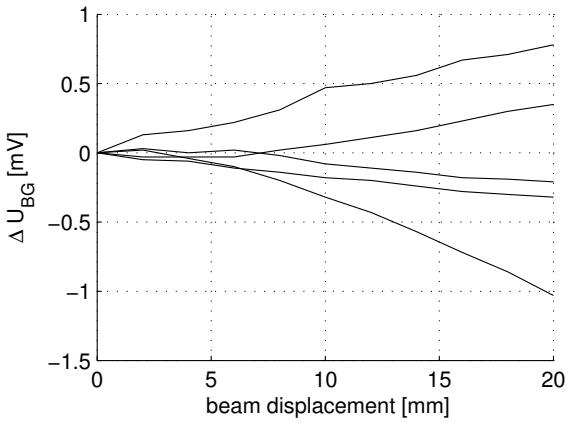


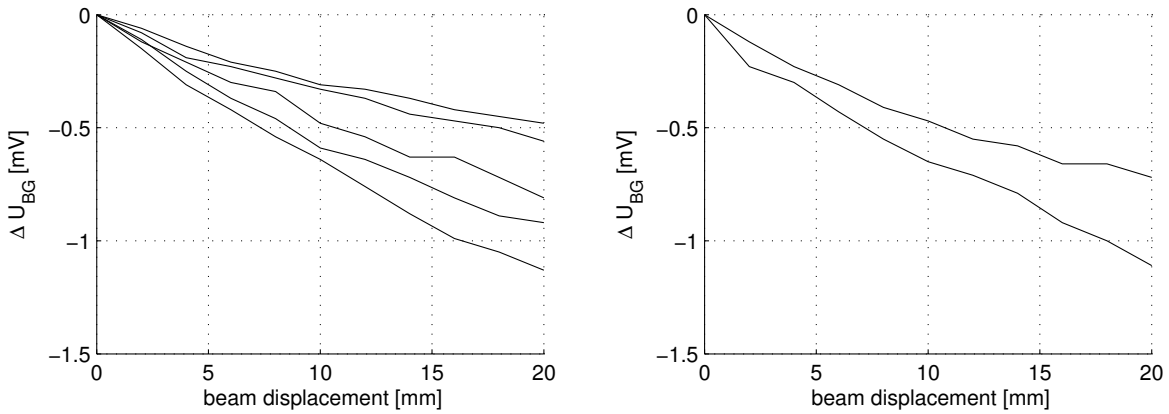

Figure 10.5.: Stress-induced reference voltage change of the bandgap circuit during bend test for 5 samples of test chip 1, 4100 µm × 4100 µm, at 90° in the center region.

The bandgap voltage itself shows a similar behavior as we discussed in the Section 4.3 for the piezoresistive effect in MOS transistors 10.4. There is a superposition of many effects. Together with random effects owing to the sample preparation, this results in both positive and negative trends in the same group of samples. As example Fig. 10.5 shows the voltage change of the bandgap circuit during bend test of five samples of test chip 1 with a size of 4100 µm × 4100 µm at 90° chip orientation in the center region of the die. This test reveals a random positive or negative trend of the bandgap in the range of ±1 mV.

The two BJT arrays of the bandgap core mentioned in 4.2 are matching structures (i.e. structures for which low paired tolerances are desired). If the same stress prevails in the two transistor arrays of the bandgap core, Eq. (4.22) yields $\Delta U_{PTAT} = 0\,\mathrm{V}$. In this case the stress-induced voltage change of the bandgap is given by Eq. (4.21) as shown in Fig. 4.1. An asymmetric design or local stress can lead to random voltage changes different from $\Delta U_{BE}$.

The piezojunction effect in the vertical BJT transistor is the same for the two tested orientations of the chip on the beam because the stress is applied either in the [011]

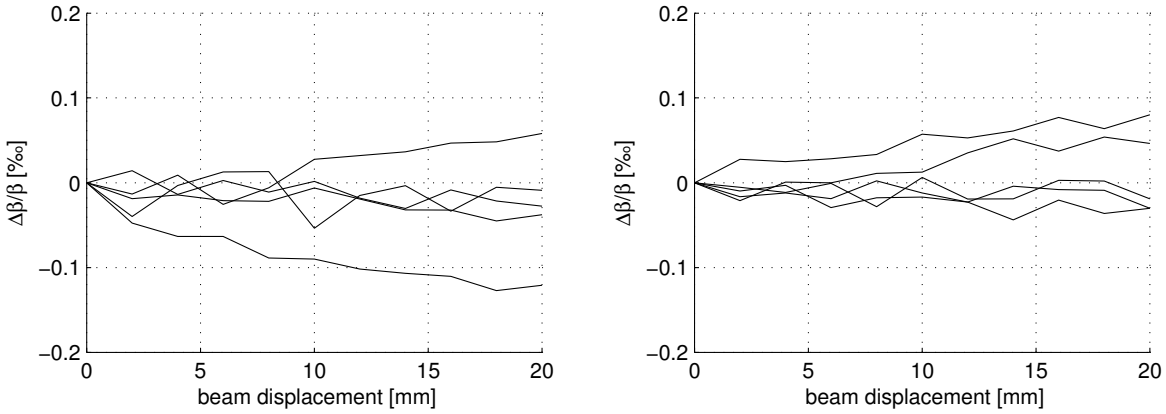
direction or in the $[0\bar{1}1]$ direction. Both directions are perpendicular to the current flow. Indeed, we expect the same stress-induced variation (due to the piezojunction effect) of the bandgap for the two orientations, if we assume the same stress in the bandgap core for both orientations and if all other effects are small enough. The bandgap circuit of test chip 2 showed the predicted behavior. This can be due to the auto-zero offset cancellation as mentioned in Chapter 7. The comparison of the measurements at different chip orientations is shown in Fig. 10.6.




(a) Orientation: 0° (b) Orientation: 90°

Figure 10.6.: Stress-induced change of the bandgap voltage during stress in test chip 2 in the center region with a die size of 2400 µm × 2777 µm in 0° orientation (a) and 90° orientation (b).

During the bend test we also recorded the variation of the amplified reference voltage. The amplification in the unstressed case was $3.65 \pm 0.01$. The relative change of the amplification $\Delta\beta/\beta$ during the test was between 0.2 ‰ and $-0.4$ ‰. Figure 10.7 shows the change of $\beta$ in five samples of test chip 1 with a size of 4100 µm × 4100 µm in the center region.




(a) Orientation: 0°

(b) Orientation: 90°

Figure 10.7.: Stress induced change of the amplification $\beta$ during stress in test chip 1 in the center region with a die size of $4100\,\mu\text{m} \times 4100\,\mu\text{m}$ in 0° orientation (a) and 90° orientation (b).

# 11. Summary

From the investigation of the influence of mechanical stress on the properties of analog integrated circuits, one expects insight into the piezoresistive and piezojunction effect as major causes for electro-mechanical coupling. From an empirical point of view these effects are well studied. The types of stress sources which occur during the production are depending on the used package type. This work focuses on near chip scale package (CSP) with exposed pad. Two main stress sources prevail. Hydrostatic pressure - one main source - is introduced during the transfer mold process of packaging (see Section 3.1). A drift caused during this early state of production can be compensated by trimming. The second main source for mechanical stress is the solder process (see Section 3.2). The different thermal expansion of the copper lead frame and the solder combined with the large area of the exposed pad causes a high compressive stress in the active chip surface in the range of $-10\,\mathrm{MPa}$. The solder stress is randomly distributed and depends on the process parameters. Solder is a ductile material. This means that the solder stress can underlie a relaxation. A robust design in terms of mechanical stress is the only option to prevent a drift during this so-called 2nd level in the production line.

In the present work we focus on the reference voltage of a bandgap circuit (see Section 2.1). A stress induced-change of such reference voltage has an effect on the precision of the entire device (see Section 2.2). The base-emitter voltage $U_{BE}$ of a diode-connected

bipolar junction transistor (BJT) with negative temperature coefficient and a voltage proportional to absolute temperature (PTAT) are combined in such a circuit to reach a temperature stable reference voltage. A CMOS bandgap circuit is realized with two BJTs and an operational amplifier. The matching components have to be placed in a common-centroid arrangement to avoid a change of the PTAT voltage caused by a stress gradient. Combined with an auto-zero offset cancellation only the stress-induced change of $U_{BE}$ (discussed in Section 4.2) remains. It is recommended to use vertical PNP transistors with the lowest piezojuction coefficients to reduce the stress-induced change of the base-emitter voltage. Two types of a bandgap circuit are compared in this work with an evaluation technique to investigate the stability of the reference voltage under mechanical stress (see Section 7.4).

In this work an evaluation method was develped using a printed circuit board in the shape of a bend beam with the chip mounted on the surface (see Chapter 5). With this technique it is possible to apply a uniaxial stress via the exposed pad to the active area of the integrated circuit. The range and distribution of stress were studied by finite element modeling (see Section 6.3). It is observed that the highest compressive in-plane stress is created in the center of the die in the range of $-110\,\mathrm{MPa}$ during the test with the bend beam. Towards the edge a region with a high stress gradient was found. The component normal to the surface is small compared with the component perpendicular to the surface. From this point of view, it is recommended, to place matching structures in the center of the chip in order to avoid a different stress-induced variation of parameters.

Two test chip in different arrangements were evaluated with this technique mentioned above. The major results are as follows:

- By means of evaluation of a polysilicon resistor on the test chip, results of FEM simulations could be confirmed (see Section 9.1). The piezoresistive effect in

polysilicon was derived from the effect in monocrystalline silicon (see Section 4.1). The resistor proved as a valuable tool to evaluate in-plane stress on the die.

- As also shown in the simulation, the measured in-plane stress applied through the exposed pad of the chip has a maximum in the center and is lower at the edge region (see Section 9.2).
- The evaluation of two different die sizes reveals a higher relative change of the resistance as a measure for the stress in the small die (see Section 9.3).
- The offset of the test buffer on the test chip showed no significant stress-induced change during the measurement and does not influence the measurement of the test structures (see Section 10.1).
- A stress-induced change of the pre-regulator current (used to bias the test structures) was measured. This was not considered during the design of the test chip and had a negative effect on the measurement of the test structures (see Section 10.2).
- It was not possible to confirm the piezojunction effect and the piezoresistive effect in the MOS transistor with the present measurement, because a stress-induced change of the bias current was not available as a measurable signal (see Section 10.4 and 10.5).
- A comparison of bandgap circuits with and without auto-zero offset cancellation demonstrated the potential of a stress stable design (see Section 10.6). The stress-induced change of amplification of the bandgap voltage to a reference signal of 4.5 V was between 0.2 ‰ and −0.4 ‰ during the bend test.

This findings can be seen as rules for a stable design in respect of mechanical stress and for a layout to prevent high stress (or a stress gradient) at critical blocks of an integrated circuit.

# Appendix

# Matlab code piezoresistive coefficients

```
%Calculation of the piezoresistive coefficents in polysilicon
%   Autor: Paulus List
%   12/2/2015
%--------------------------------------------------------------------------

%complience matrix polysilicon J. J. WORTMAN
s=zeros(6,6);
s(1:3,1:3)=-0.214*10^-10;
s(1,1)=0.768*10^-10;
s(2,2)=0.768*10^-10;
s(3,3)=0.768*10^-10;
s(4,4)=1.26*10^-10;
s(5,5)=1.26*10^-10;
s(6,6)=1.26*10^-10;

%p-type Matsuda
pi11=-6.5;
pi12=3.3;
pi44=-1.2;

%n-type Matsuda
% pi11=-7.7*10^-10;
% pi12=3.9*10^-10;
% pi44=-1.4*10^-10;

% %p-type Smith
% pi11=0.7*10^-10;
% pi12=-0.1*10^-10;
% pi44=13.8*10^-10;

%calc pi_d for every Theta and Psi
Theta=linspace(0,pi/2,100);
Phi=linspace(0,pi/4,100);
Psi=0;
pi_l=zeros(100,100);
pi_t=zeros(100,100);
sii_t=zeros(100,100);
```

```
sii_l=zeros(100,100);

%Phi=const in column
for i=1:100
    for j=1:100
        dcm = angle2dcm(Phi(i), Theta(j), Psi);
        pi_l(i,j)=pi11+2*(pi44+pi12-pi11)*(dcm(1,1)^2*dcm(1,2)^2+...
            dcm(1,1)^2*dcm(1,3)^2+dcm(1,2)^2*dcm(1,3)^2);
        pi_t(i,j)=pi12+(pi11-pi12-pi44)*(dcm(1,1)^2*dcm(2,1)^2+...
            dcm(1,2)^2*dcm(2,2)^2+dcm(1,3)^2*dcm(2,3)^2);
        sii_l(i,j)=s(1,1)+(s(4,4)+2*s(1,2)-...
            2*s(1,1))*(dcm(2,1)^2*dcm(2,2)^2+dcm(2,1)^2*dcm(2,3)^2+...
            dcm(2,2)^2*dcm(2,3)^2);
        sii_t(i,j)=s(1,1)+(s(4,4)+2*s(1,2)-...
            2*s(1,1))*(dcm(1,1)^2*dcm(1,2)^2+dcm(1,1)^2*dcm(1,3)^2+...
            dcm(1,2)^2*dcm(1,3)^2);
    end
end

%norm
Y_n=ones(100,100);
for i=1:100
    int_n1(i)=trapz(Phi,Y_n(i,:));
end
int_n2=trapz(Theta,int_n1);

%transverse
Y_t=pi_t./sii_t;
for i=1:100
    int_t1(i)=trapz(Phi,Y_t(i,:));
end
int_t2=trapz(Theta,int_t1);
pis_mean_t=int_t2/int_n2

%longitudinal
Y_l=pi_l./sii_l;
for i=1:100
    int_l1(i)=trapz(Phi,Y_l(i,:));
end
int_l2=trapz(Theta,int_l1);
pis_mean_l=int_l2/int_n2

%ratio of transverse and longitudinal
pis_mean_l/pis_mean_t
```

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