Gerald Schwarz

Development of a Parallel and Time Interleaved Multi-Channel Capacitance Measurement System

Diploma Thesis

Graz University of Technology

Institute of Electrical Measurement and Measurement Signal Processing
Head: Univ.-Prof. Dipl.-Ing. Dr. techn. Georg Brasseur

Supervisor: Dipl.-Ing. Dr.techn. Markus Neumayer
Cosupervisor : Dipl.-Ing. Matthias Flatscher, BSc.

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Abstract

Capacitive sensing is a versatile and simple technology for various sensing applications and is applied in many fields of technology. In the recent years, numerous examples for capacitive sensors can be found for applications in the field of consumer electronics. This trend has lead to a variety of integrated capacitance measurement ICs for simple realization of these sensors. Making use of these ICs for industrial sensing application is a suitable approach in order to reduce the instrumentation effort. Due to their origin, several of these integrated solutions offer rather low acquisition rates. This limits their use for sensing applications, where high acquisitions rates are required. Also, some modern applications of capacitive sensing require the simultaneous measurement of several capacitances, which often can not be handled by integrated solutions sufficiently. Extended hardware efforts are required, e.g. switching circuits, to realize multiple measurements. Given a signal acquisition system, the techniques of parallel measurement and time interleaved measurement are known approaches to increase the overall measurement rate. Hereby, several units of the same acquisition system are used simultaneously for the parallel and sequentially for the time interleaved measurement technique, to achieve higher measurement rates. This thesis investigates the concept of realizing a multi-channel capacitive measurement system using existing ICs by means of parallel and time interleaved measurements. Different measurement methods are analyzed with respect for applicability of parallel and time interleaved measurements. For a selected IC a circuit concept to realize both techniques is developed and discussed. The feasibility of the approach is demonstrated by means of measurements on a prototype.

Keywords: multi-channel capacitive sensing, parallel capacitive measurement, time interleaved capacitive measurement.

Kurzfassung

Die kapazitive Messtechnik hat sich für viele Anwendungen als bewährte Sensortechnik etabliert. Besonders im Bereich der Consumer-Elektronik entstanden viele Anwendungen für diese Sensorik. Dies führte auch zur Entwicklung mehrerer dezidierter Mess-ICs für kapazitive Messaufgaben. Eine Verwendung dieser ICs für neue messtechnische Aufgaben ist anzustreben, um den Entwicklungsaufwand zu reduzieren. Viele der entwickelten Mess-ICs besitzen jedoch geringe Messraten. Dies schränkt deren Anwendbarkeit für Applikationen mit höheren Abtastraten ein. Ebenso erfordern manche Messaufgaben, die gleichzeitige Erfassung mehrerer Kapazitäten. Auch dies kann mit vielen fertigen ICs nur zum Teil realisiert werden. Zur Erhöhung der Erfassungsrate sind bei ADC Systemen die Techniken der Parallelisierung und des Time-Interleaved-Samplings bekannt. Bei dieser Methode werden mehrere ADCs genützt, um im Parallelbetrieb mehrere Signale gleichzeitig zu erfassen. Im Time-Interleaved-Betrieb erfassen mehrere ADCs das gleiche Signal sequenziell, um eine höhere Abtastrate zu erreichen. In dieser Arbeit wird die Möglichkeit zur Parallelisierung und zum Time-Interleaved-Betrieb von kapazitiven Mess-ICs untersucht. Für eine ausgesuchte IC-Familie wird ein Konzept für ein kapazitives Mehrkanal-Messsystem erarbeitet. Messungen an einem Prototypen zeigen die Realisierbarkeit der vorgeschlagenen Verfahren.

Schlüsselwörter: Kapazitives Mehrkanal-Messsystem, kapazitive parallele Erfassung, kapazitive Time-Interleaved Sensorik

Contents

Abstract iii

1 Introduction 1

1.1 Introduction to Capacitive Measurement 1
1.2 Multi-Channel Capacitive Measurement Systems - An ECT Example 1
1.3 Aim of this work 4
1.4 Outline of this Thesis 4

2 Capacitance Measurement 6

2.1 Measurement of Capacitances 7
2.2 DC-Circuits 8
2.3 Oscillator Circuits 9
2.4 AC-Circuits 10
2.5 Switched-Capacitor Capacitance to Digital Converter 12
2.6 Differential Capacitive Voltage Divider 14
2.7 Tuning of a LC-Resonance Circuit 16
2.8 High-Precision Time Measurement 17
2.9 Measurement of Differential Charges 19
2.10 Summary of Capacitance Measurement Circuits 21

3 Capacitive ΣΔ-Converter 23

3.1 The ΣΔ-Analog-to-Digital-Converter 23
3.1.1 Oversampling 26
3.1.2 Noise Shaping 27
3.1.3 ΣΔ-Analog-to-Digital Converter 29

3.1.4 Realization of a ΣΔ-ADC in Switched-Capacitor Technology 30
3.2 Prototype Board for Parallel SC-ΣΔ-CDC Measurement 32
3.3 Simulation of a SC-ΣΔ-CDC with External Excitation 34
3.4 Summary 40

4 Design of Parallel and Time Interleaved Measurement Hardware 41
4.1 Measurement Setup 41
4.2 Hardware Features, Resolution and the Sampling Rate of the MAS6510 . . . 43
4.2.1 Application of External Excitation for the MAS6510 45
4.3 Supporting Circuitry for the Parallel Measurement System 47
4.3.1 Excitation-Signal Amplifier 47
4.3.2 Synchronization of Excitation and Measurement-Cycles 50
4.3.3 Parallel Communication 51
4.4 Measurement Hardware for Time Interleaved Charge-based Capacitive Measurements 52

5 Measurement Results 56
5.1 Characterization of the Parallel Measurement System 57
5.1.1 Analysis of the Results of the performed Measurements 57
5.1.2 Comparison of individual Measurement Channels 60
5.2 Characterization of the Time Interleaved Measurement Circuit 66
5.2.1 Comparison of the Results for the Measurement of the Individual Channels in Time Interleaved Mode 67
5.3 Test on an Example ECT-System 73

6 Discussion 76
6.1 Capacitive Measurement Technologies 76
6.2 Parallel Measurement Approach 77
6.3 Time Interleaved Measurement Approach 77
6.4 Conclusion 78

Bibliography 79

List of Figures

1.1 Schematic ECT Sesnor array 2
1.2 Schematic reassembling of one capacitance measurment configuration for an ECT sensor array 2

2.1 Schematic circuit of a capacitance measurment circuit in grounded mode . . 7
2.2 Schematic circuit of a capacitance measurment circuit in floating mode . . . 8
2.3 DC capacitance circuit 8
2.4 Basic RC-oscillator circuit 9
2.5 Synchronous full-wave demodulator circuit 10
2.6 High-impedanc eand low-impedance AC-amplifier 11
2.7 High-impedance amplifier block diagramm proposed by [12] 12
2.8 Low-impedance amplifier block diagramm with a tuneable input stage proposed by [12] 12
2.9 Block diagramm of swicthed-capacitor ΣΔ-CDC 13
2.10 Signal graphs of a switched capacitor CDC 13
2.11 Schematic circuit of a capacitive voltage divider 15
2.12 Signal graph of a capacitive voltage divider 15
2.13 Schematic cirucit of a LC-oscillator measurement circuit 17
2.14 Schematic circuit of a precision time measurement capacitance meter 18
2.15 Signal graph of a discharge time measuement circuit 18
2.16 Schematic circuit for a differential charge measurement 20
2.17 Signal graph of a differential charge measurement system 20

3.1 Analog-to-digital converter 24
3.2 Generic quantizer circuit and model of quantization error 24

3.3 Analog-to-digital circuit with oversampling 26
3.4 ΣΔ-modulator circuit 27
3.5 Filtering of a stochastic process with PSD 28
3.6 Discrete time ΣΔ-analog-to-digital circuit model 29
3.7 Block diagramm of swicthed-capacitor ΣΔ-ADC 31
3.8 Prototype board for AD7745 32
3.9 Graph of 800 subsequently measured data points with external excitation . . 33
3.10 Block diagramm of simulated swicthed-capacitor ΣΔ-CDC with external excitation source 35

4.1 Schematic parallel capacitive measurement system 42
4.2 Schematic diagram of MAS6510 44
4.3 Internal excitation signal graphs of the differential charge measurement system for external clock 45
4.4 Schematic test circuit for the external excitation of a MAS6510 46
4.5 Biased DC-amplifier 48
4.6 Signal graph of one external excitation signal used for trigger synchronization 50
4.7 Circuit providing the synchronization trigger signal 50
4.8 Schematic time interleaved capacitance measurement system 53
4.9 N-time current multiplier 54
4.10 Picture of the manufactured prototype board 55

5.1 Picture of parallel measurment setup 57
5.2 Measurement example for channel 3 with a test capacitance of 17.91 pF and $U_{\mathrm{exc}} = 67.4\,\mathrm{mV}$ 59
5.3 Comparison of all channels in parallel measurement mode for a test capacitance of 17.91 pF 60
5.4 Comparison of all channels in parallel measurement mode for a test capacitance of 26.45 pF 61
5.5 Depiction of the relative number of outliers of all channels in parallel measurement mode for a test capacitance of 17.91 pF 62
5.6 Combined results for all measured test capacitances for channel 3 62

5.7 Combined results for all measured test capacitances for channel 3 with the focus on small exciation voltages 63
5.8 Combined results for all measured test capacitances for channel 3 in dependance of the capacitive difference 64
5.9 Combined SNR for all measured test capacitances for channel 3, in dpenedance of the capacitive difference 65
5.10 Picture of time interleaved measurment setup 66
5.11 Comparison of all channels in parallel measurement mode for a test capacitance of 17.91 pF 68
5.12 Comparison of all channels in parallel measurement mode for a test capacitance of 26.45 pF 69
5.13 Depiction of the relative number of outliers for all channels in parallel measurement mode for a test capacitance of 17.91 pF 70
5.14 Combined results for all measured test capacitances for channel 3 70
5.15 Combined results for all measured test capacitances for channel 3, focused on small exciation voltages 71
5.16 Combined results for all measured test capacitances for channel 3, for capacitive difference 71
5.17 Combined SNR for all measured test capacitances for channel 3, for capacitive difference 72
5.18 Measurement setup using the ECT-test pipe 73
5.19 Example results of an ECT-test measurement using the full parallel measurement 74
5.20 Example results of an ECT-test measurement using the full time interleaved measurement setup 75

1 Introduction

1.1 Introduction to Capacitive Measurement

In recent years, the technology in the field of capacitive sensing has advanced tremendously. Capacitive sensor interfaces are nowadays used widely in industry and costumer electronics. Consumer electronics favor the potential to miniaturize capacitive senors, in particular distance and contact senors, e.g. for touch screens in mobile phones and computer tablets. In industrial applications, capacitive sensors are favored for the measurement of humidity, distances, acceleration and angular displacement etc.. The advantages of robustness against environmental interferences, simplicity in application and contactless measurement favor their use. The measurement of capacitive senors is performed using either a charge-based approach [1] or an AC-approach [2]. Based on this two principles numerous circuits for measuring have been developed.
In the following section, multi-channel capacitive sensing systems on the example of Electrical Capacitance Tomography ECT are described.

1.2 Multi-Channel Capacitive Measurement Systems - An ECT Example

Multi-channel capacitive measurement systems offer the ability to determine a large number of measurement capacitances simultaneously. Multi-channel capacitive measurements are needed in applications, where a single capacitance measurement is not sufficient for further processing. Such applications range from oil level sensing in two stroke machines [3] to the detection of congregations of ice on overhead power lines [4].

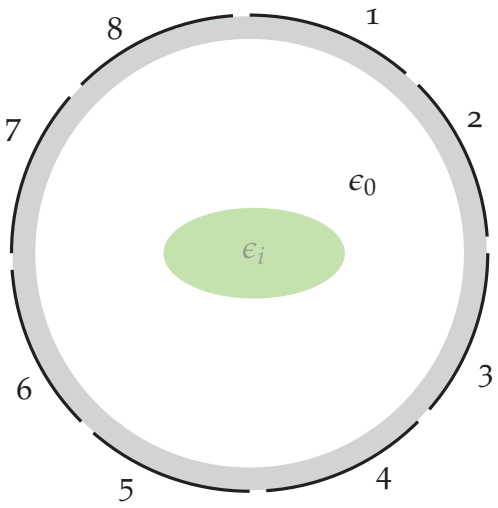

Figure 1.1. Schematic array of sensor electrodes for an ECT system with eight electrodes.

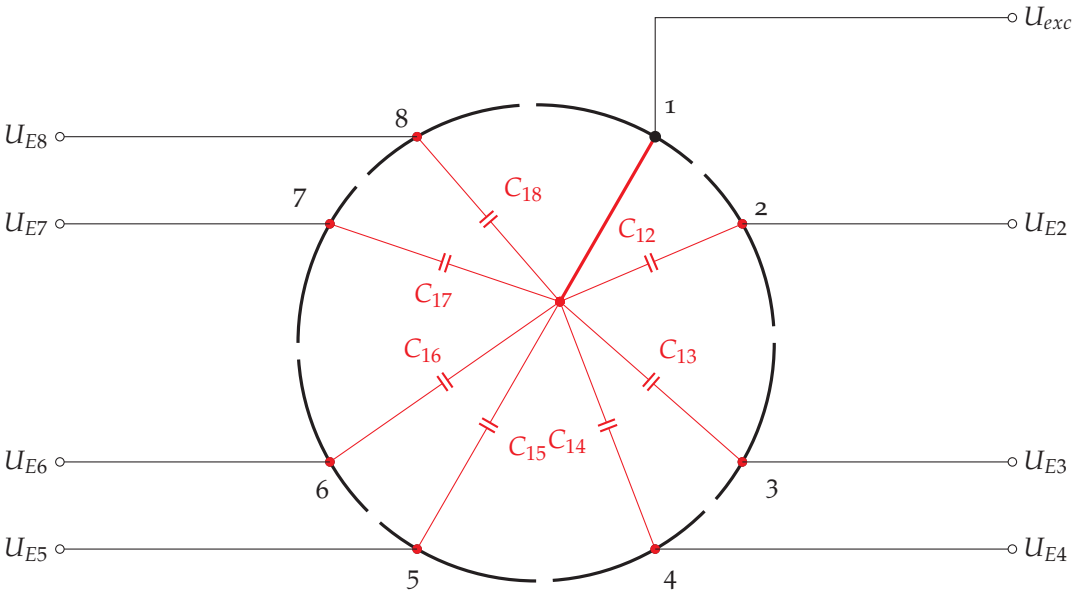

Figure 1.2. Schematic reassembling the capacitances of one measurement configuration of an array of sensor electrodes.

A special application of capacitive sensing is Electrical Capacitance Tomography (ECT). It can be referred to as a multi-capacitance measurement system. It is formed by a set of electrodes mounted on a tube [5]. An exemplary illustration for an ECT-sensor with $n = 8$ electrodes is depicted in figure 1.1. The capacitances formed between the electrodes are determined by the material distribution inside the gray pipe. Capacitive measurements can be used to reconstruct the spatial dielectric properties inside this tube from capacitive

measurements. For typical ECT-systems, the number of electrodes varies between $n = 8$ to $n = 16$ [6]. A large number of electrodes is required to achieve a considerable result for the reconstruction result. The reconstruction of the dielectric properties can be used to monitor the material distribution inside the tube [7] [8]. As illustrated in figure 1.2, for an n electrode ECT-sensor, $(n-1)$ coupling capacitances can be defined between one electrode and the remaining $(n-1)$ electrodes. Following this scheme a total number of $(n-1)^2$ measurement capacitances can be defined. However, due to symmetry reasons only $\frac{n(n-1)}{2}$ independent measurement capacitances can be obtained. In one measurement cycle one electrode is connected to an excitation source and the remaining electrodes are connected to low impedance current measurement circuits [9] [10]. In order, the displacement currents are measured. In the next cycle, the excitation source is switched to the next electrode and the current measurements are repeated, until each electrode was connected once to the excitation source. This approach has the advantage, that $(n-1)$ measurement capacitances can be measured in parallel for each excitation. Thus, all capacitances can be measured after n cycles. This principle has been proposed for various ECT-systems [11] [12]. As for any sampling system, the measurement rate has to be high enough to capture the dynamics of the process. Due to the large number of measurements for an ECT-system, fast measurement schemes are required [13] [14]. Parallel measurement strategies are already a concept to increase the measurement rate, in order to capture the same information about the same volume [14], i.e. the material distribution inside the sensor. Dedicated ECT hardware is specifically designed to meet all these requirements. However, designing such hardware takes a considerable effort. To use commercially available ICs would be preferable.

The feasibility to realize ECT-systems using of the shelf capacitance measurement ICs has already been demonstrated [15] [16]. However, most available ICs do not provide enough measurement channels to realize a typical ECT-system by means of a single chip solution. Elaborate hardware concepts, e.g. switch matrices, have to be designed in order to realize the measurement system. As reported in [16], measurements have to be performed sequentially, rather than in a parallel mode, which reduces the acquisition rate.

1.3 Aim of this work

In this thesis, two concepts to increase the measurement rates for capacitive multi-channel measurements using of the shelf measurement ICs are proposed. For fast acquisition of several measurement capacitances, the feasibility of a real parallel measurement mode using several ICs is investigated. In order to measure a single capacitance with an increased acquisition rate, the concept of time interleaved sampling, using several of the shelf ICs is suggested. The two measurement approaches use several units of the same acquisition system (of the shelf measurement ICs) simultaneously for the parallel and sequentially for the time interleaved measurement method.
To summarize, the following questions are addressed in this work:

- Is parallel capacitive measurement possible using of the shelf measurement ICs?
- Is time interleaved measurement of a single capacitance possible using of the shelf measurement ICs?
- What prerequisites are necessary to implement both approaches?

1.4 Outline of this Thesis

In this work, a parallelized approach for a multiple capacitance measurement system and a time interleaved approach for a single capacitive measurement system is developed, to increase the overall measurement rate. This work is structured as follow:

1. **Chapter 2** reviews methods for the measurement of capacitances and provides a selection for the most promising methods.
2. **Chapter 3** investigates an approach for parallelization of a ΣΔ-modulator based capacitive measurement system. In measurements and simulations conducted, the limitations of this technique are presented.
3. **Chapter 4** covers the specification of the measurement hardware for parallel and time interleaved measurements and the subsequent realization of the measurement hardware.
4. **Chapter 5** presents the measurement results obtained for the implemented hardware, for the parallel and time interleaved measurements. The system will be tested in a

specified measurement arrangement, in order to derive its measurement characteristics.

5. **Chapter 6** discusses the findings in this work, providing a conclusion of the results and presenting possible future work based on this thesis.

2 Capacitance Measurement

Capacitive sensing aims to evaluate measurement capacitances for the purpose of gaining knowledge about a quantity, which offers a certain sensitivity with respect to the desired measurand [17], i.e. capacitance. In this work the focus is set to the measurement circuitries to determine capacitances formed by capacitive senors. Initially in this chapter, two measurement configurations for capacitances are described. Further, methods are described in detail and investigated towards their applicability for parallel and time interleaved measurements. Concluding, a summary of the presented methods is given and based on this, the most promising method is chosen.
In total, seven categories of working principles for the measurement of capacitances have been identified:

- DC-circuits [17].
- Oscillator-circuits [17].
- AC-circuits [12], [17].
- Switched-capacitor circuits using $\Sigma\Delta$-modulation [11].
- Differential capacitive voltage dividing circuits [18].
- Detuning of a LC-resonance circuit [19].
- High precision time measurement circuits [20].
- Differential charge measurement circuits [21].

In order to measure an arrangement of capacitances in parallel, it is required to externally provide the excitation of the network. This avoids interferences between the single capacitances and a connection of multiple individual excitation outputs. In addition, it has to be considered that the activation of each individual circuit has to be done simultaneously for the parallel measurement. So far the requirements for the parallel measurement system can

be stipulated as follow:

- External common excitation of the measurement device.
- Simultaneous activation of measurement cycle.

The following subsections cover each principle in more detail. Before the measurement methods are presented, general challenges and considerations regarding capacitive measurements are described.

2.1 Measurement of Capacitances

In this section two modes are explained, how a measurement capacitance C_X can be connected and the reason for measuring will be discussed. The two types are:

- Grounded mode.
- Floating mode.

The mode distinguishes, how the measurement capacitance C_X is connected to GND. Firstly, in figure 2.1 the configuration for the grounded measurement mode is illustrated. In the grounded mode, the capacitance to be determined is connected to ground potential on one side and to the measurement circuitry on the other side. Parasitic capacitances due to connectors and cables are summarized by C_{S1}, which is depicted in figure 2.1. These are denoted as stray capacitances and are defined to alter the effective capacitance to be measured. An disadvantage is the restriction on circuit design for this mode.

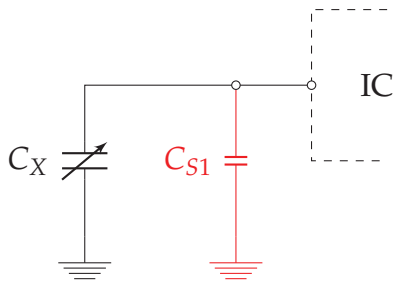

Figure 2.1. Schematic circuit of a capacitance to be measured in a ground referenced setup.

Secondly, in floating mode the capacitance to be determined is connected to a source and to the measurement circuit. This introduces at both connection points the stray capacitances

mentioned afore. A simplified circuit is presented in figure 2.2. It can be observed, that the properties of the source as well as the input stage of the IC have a considerable effect on the circuit. The advantage of this mode is the greater number of methods to be applicable. However, the two stray capacitances have a greater effect on the measurement capacitance.

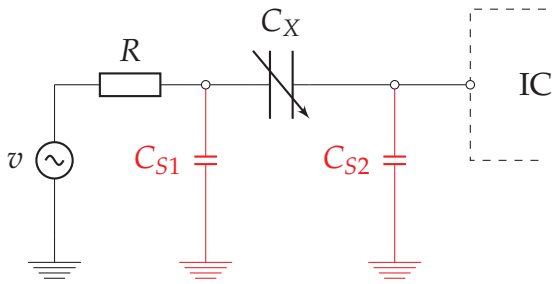

Figure 2.2. Schematic circuit of a capacitance to be measured in a floating setup.

Generally, the floating mode is preferred, because it allows to minimize the effects of the stray capacitances using a proper measurement circuit design. Subsequently, the initially found capacitance measurement methods are described.

2.2 DC-Circuits

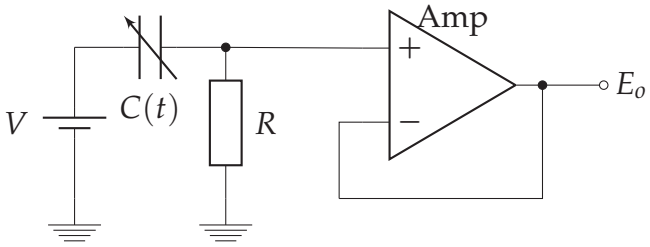

Figure 2.3. DC capacitance measurement circuit (rarely used due to restriction to measure only dynamic changes in capacitance).

DC measurement circuits are circuits to determine changes of the measurement capacitance [17]. A principle circuit is depicted in figure 2.3. It consists of a high input impedance amplifier *Amp* in combination with a source charging the capacitance $C(t)$ over the resistor R, which is connected to the amplifier input. As the charge is nearly constant, the output relation can be derived as:

$$E_0 = \frac{Q}{C} = \frac{C_{avg}V}{C}, \tag{2.1}$$

with Q being the charge on the capacitor C and C_{avg} the average capacitance in idle state, when the frequency of changes of $C(t)$ is greater than $1/RC$. The output E_0 will vary reciprocal to the capacitance applying $Q = CV$. It is important, that the time constant RC must be greater than the time between consequential measurements, to avoid losses induced by settling charges.

2.3 Oscillator Circuits

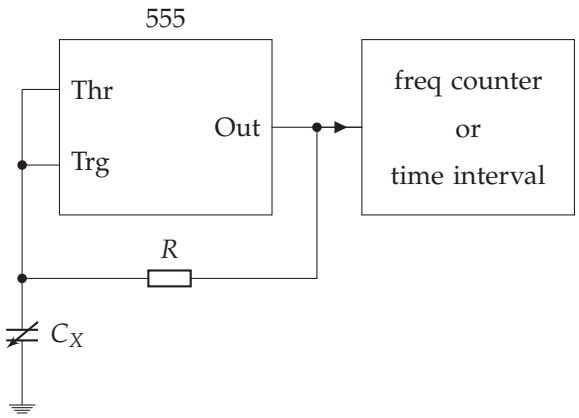

Figure 2.4. Basic circuit for an RC-oscillator using an 555-Timer IC.

Oscillator circuits transduce the measurement of capacitances to a time or frequency measurement. These can be divided in *RC*-oscillators and *LC*-oscillators. A very simple *RC*-oscillator circuit is displayed in figure 2.4. It reassembles a Schmitt-trigger with a *RC*-feedback-circuit. An advantage of this circuit is, that it is unaffected by supply voltage variations. Furthermore, it can be extended with an analog switch that temporarily replaces C_X with a reference capacitance to calibrate the circuit, to increase the overall accuracy. The output frequency can be measured using a frequency counter or a time interval measurement. In chapter 2.7 one integrated solution for a *LC*-oscillator CDC is described in more detail.

2.4 AC-Circuits

AC-circuits apply a high frequency signal in the range of 10 kHz to 1 MHz to a network of known impedances and the capacitance under test. A principle circuit is presented in figure 2.5. In this circuit, the AC-voltage is applied to two capacitive impedances, forming a voltage divider. Subsequently, the divided voltage is amplified and applied to a synchronous demodulator and a subsequent low pass filter. This measurement circuit is termed a synchronous full-wave demodulator with positive and negative half cycles contributing to the resulting DC signal at the output. The output signal is proportional to $\frac{C_X}{C_X+C_1}$.

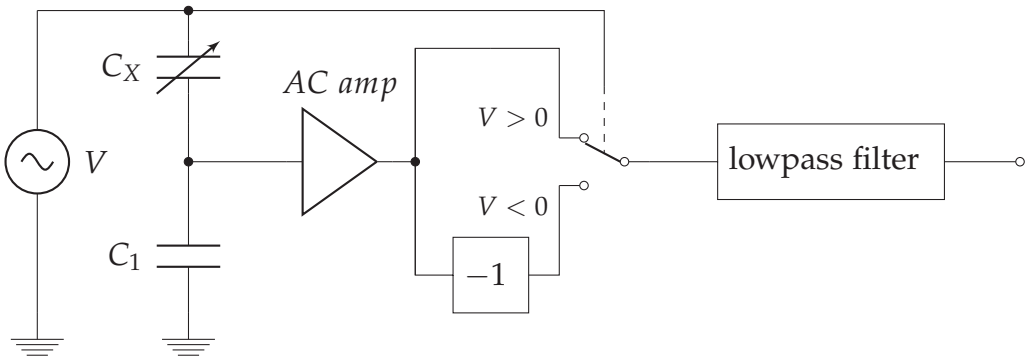

Figure 2.5. Schematic synchronous full-wave demodulator circuit.

In contrast to the DC-circuit, the AC-circuit allows for different evaluation principles to determine C_X. The AC-amplifier circuit principle can be realized in two different ways. The high-impedance amplifier and the low-impedance amplifier principle, respectively. Both types are shown in figure 2.6, the high-impedance amplifier in figure 2.6 a) and the low-impedance amplifier in figure 2.6 b).

The high-impedance amplifier generates an output signal depending to the ratio of the capacitance to be determined C_X and the stray capacitance C_S. The low-impedance amplifier transduces the displacement current through C_X to an output voltage proportional to the current. Subsequently it can be stated, that the high-impedance-type is highly affected by the stray capacitance C_S, whereas the second circuit shows no affection. Therefore high-impedance-amplifiers require additional circuitry to reduce these effects.

In the following, the two circuit variants will be discussed in more detail. Further information can be found in [12]. A high-impedance Receive/Transmit amplifier block diagram is

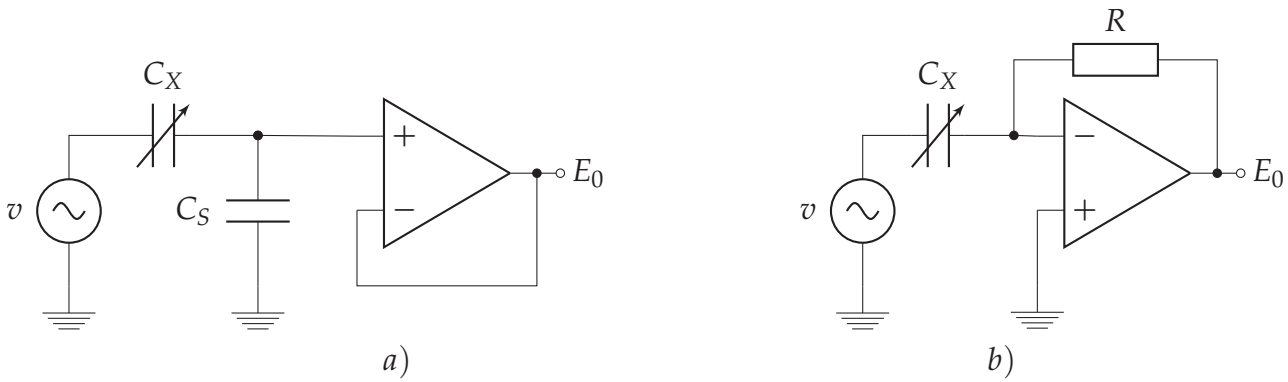

Figure 2.6. Principal circuit of high-impedance and low-impedance AC amplifier for capacitance measurement.

shown in figure 2.7. The circuit consists of an input stage, a demodulator stage, a transmitter stage controlled by a micro processor and the capacitance to be measured in floating mode. To determine the value of the inter-electrode capacitance C_X, the potential of an ideally floating electrode is measured, using the high-impedance amplifier. Circuit analysis revealed for the high-impedance amplifier a strong influence to the stray capacitance C_{S2}, due to the formation of a capacitive voltage divider by C_{S2} and C_X.

The low-impedance receive/transmit amplifier block digram with a tuneable input stage is shown in figure 2.8. In contrary to the high-impedance-approach, the sensing electrode is kept on virtual ground. Following the displacement current of the capacitance to be quantified, is converted by the low-impedance amplifier into a voltage signal, which is proportional to the inter-electrode capacitance C_X.

Furthermore circuit analysis showed, that the low-impedance amplifier with a tuneable resonance circuitry (L and C_{var}) implemented reduces the sensitivity to electromagnetic interferences, due to the narrow frequency characteristics. C_{var} allows to tune the resonance frequency of the input stage to match the excitation frequency. In addition, this characteristics reduce the noise bandwidth and therefore increase the signal-to-noise ratio. This leads to a higher effective resolution, compared to the high-impedance amplifier stage.
Concluding, a low-impedance approach is the preferable variant for AC-circuits, due to an enhanced effective resolution provided by the increased SNR and reduced sensitivity to stray capacitances connected to the amplifier input.

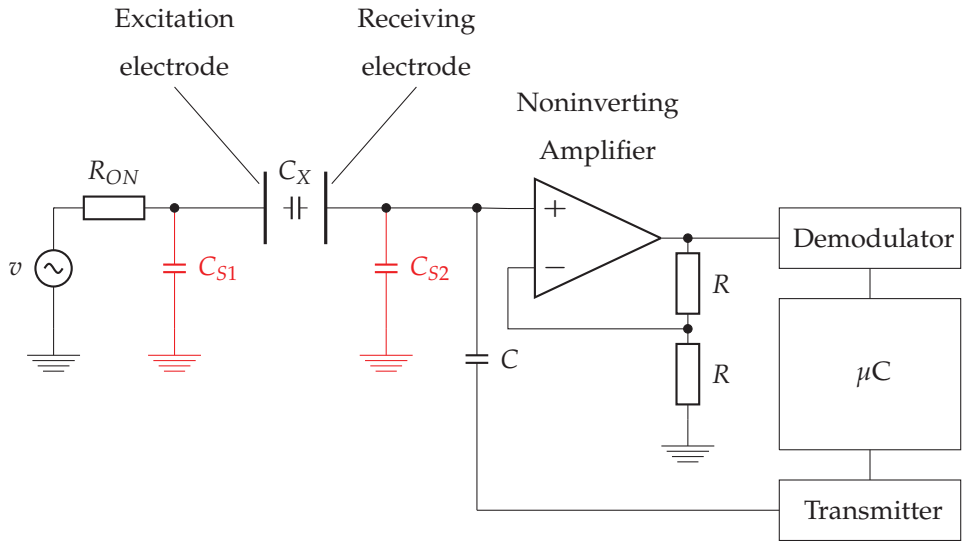

Figure 2.7. High-impedance ampilfier block diagramm front-end circuitry proposed by [12].

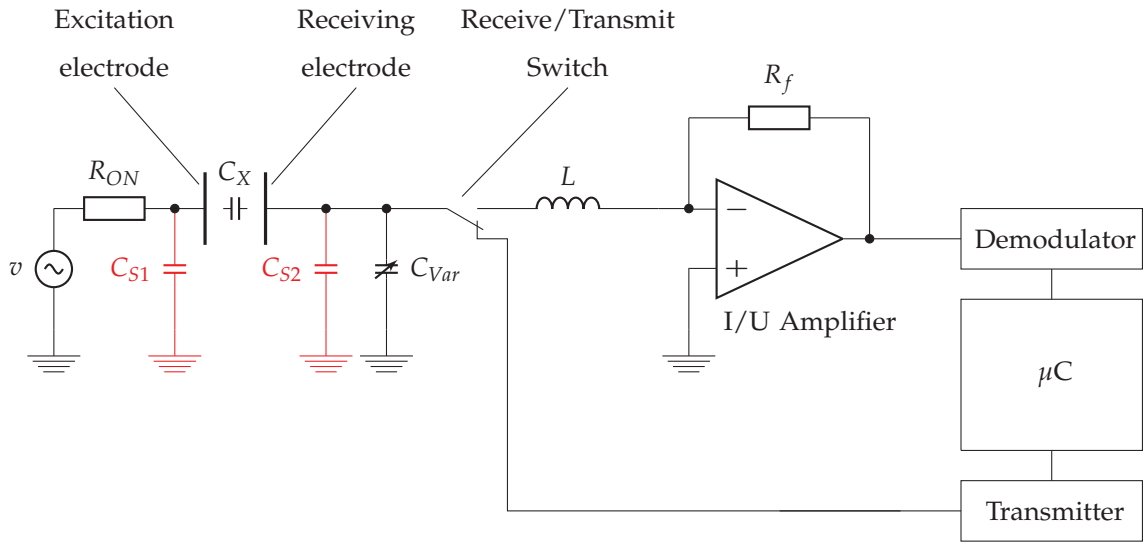

Figure 2.8. Low-Z ampilfier block diagramm front-end circuitry with a tuneable input stage proposed by [12].

2.5 Switched-Capacitor Capacitance to Digital Converter

The switched-capacitor capacitance to digital converter (SC-CDC) is based on the switched-capacitor charge-balancing ADC circuit proposed by [1]. The basic idea of this method is to repeatedly accumulate a defined amount of charge $q_{\text{in}} = C_{\text{in}}U_{\text{a}}$ over the conversion interval of n reference cycles and extract m-times a reference charge of q_{ref} from the capacitor. This concept is namely referred to as $\Sigma\Delta$-modulation and will be described detailed in chapter 3.

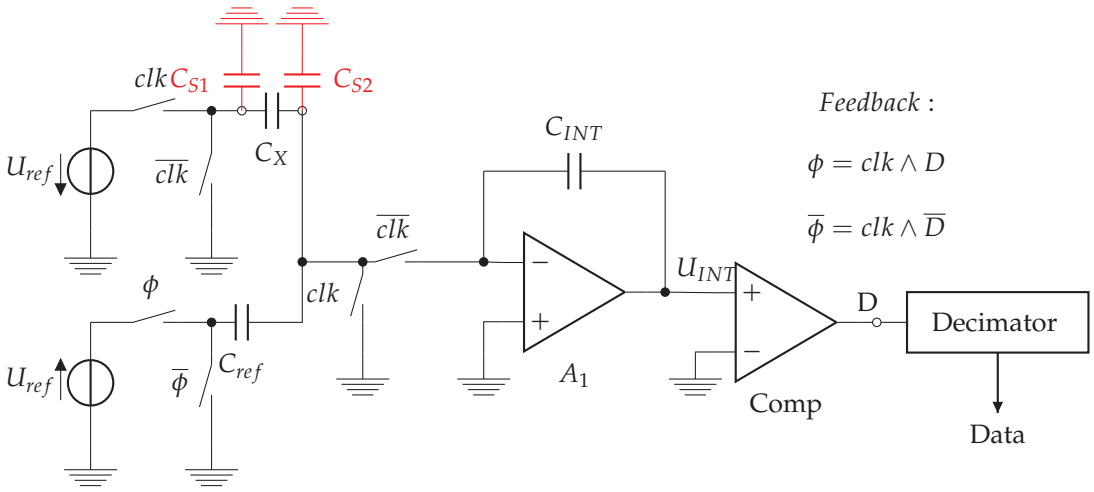

Figure 2.9. Block diagram of a ΣΔ-CDC for the measurement of floating feed-through capacitances. The stray capacitances of connecting cables are shown in red [1].

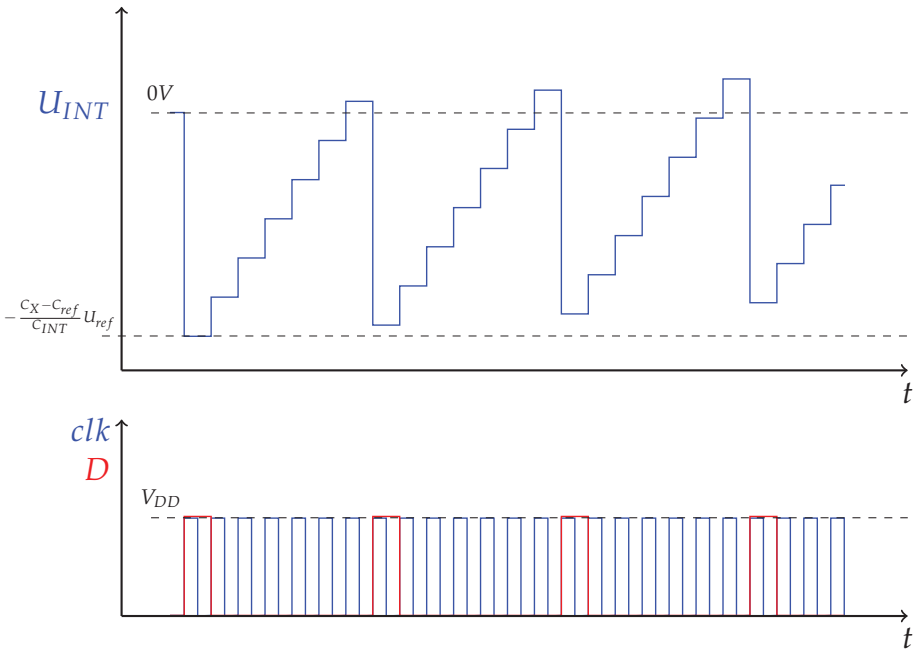

Figure 2.10. Signal graphs of a switched capacitor CDC based on ΣΔ-modulation [1].

Figure 2.9 shows the block diagram of a switched-capacitor ΣΔ-CDC. The signal graphs for the circuit are illustrated in figure 2.10. For the description of the working principle of the SC-ΣΔ-CDC, let us assume that for $t = 0$, the output of the integrator is negative and the comparator output is '0'. With every rising edge of the clock-signal *clk*, the capacitor C_X is charged to U_{ref}. At the falling edge of *clk* the charge stored in C_X is transfered to C_{INT} and is charged to $C_X U_{ref}/C_{INT}$. The charging processes is repeated until the output voltage of

the integrator surpasses 0 V and toggles the comparator output to '1'. In the subsequent charging phase C_{ref} is charged to $-U_{ref}$ and therefore the total charge of $(C_X - C_{ref})U_{ref}$ is transferred to C_{INT}. Afterwards further charges can be accumulated in C_{INT}.
The output stream of D consists of '1's and '0's and represents the number of discharge events occurred in one measurement cycle. The ratio of digital '1's in relation to the number of clock cycles equals the ratio of C_X/C_{ref}. This principle is applied in the integrated circuits AD7745-7747 and AD7150 manufactured by Analog Devices Inc [25].
One advantage of this principle is, that it is hardly affected by the stray capacitances C_{S1} and C_{S2}. C_{S1} is short circuited in the $\overline{clk}$ phases and charged in parallel otherwise and C_{S2} is short circuited during clk phases and otherwise kept on virtual ground of the integrating amplifier. The resolution of this type of CDC can be increased by applying the same methods used for ΣΔ-ADCs and the resulting bitstream D supersedes an additional ADC for conversion. The disadvantage is, that the switches introduce injected charges into the capacitor C_{INT} altering the result.

2.6 Differential Capacitive Voltage Divider

The Capacitive Voltage Divider (CVD) circuit has a similar working principle as the previous type of capacitance measurement circuit. The schematic circuit of a CVD is shown in figure 2.11. The capacitive sensors are referenced to ground potential.
The signal graphs for one measurement are depicted in figure 2.12. Initially both capacitances C_X and C_{HOLD} are uncharged. The switch $\phi_1 = 1$ is closed and $\phi_2 = \phi_3 = 0$ are opened, the internal capacitance C_{HOLD} is charged to V_{SS} and the external capacitance $C_X||C_S$ to V_{DD}. This is termed as precharge phase. Subsequently, the two capacitances are connected via $\phi_3 = 1$ (closed), the other switches are opened and the charges are allowed to settle. This phase is denoted as the acquisition phase. In the next step the ADC samples the voltage held by C_{HOLD}, denoted as conversion phase. After the first sample, the capacitances are charged to the opposite voltages and the process of settling and subsequent conversion are conducted, performing a second sample. If the external capacitance is larger than the internal ($C_X > C_{HOLD}$), the signal changes and the resulting graphs diverge as depicted in figure 2.12. The settling voltage after the first acquisition phase decreases and increases in

the second acquisition phase, resulting in diverging settling voltages. The voltage difference is denoted as ΔU. Typically V_{SS} is set to GND potential. Hence, in each charge phase one capacitance is charged and the second is discharged.

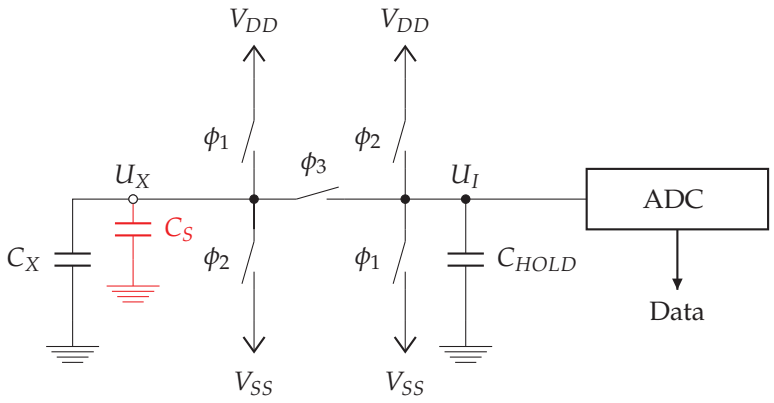

Figure 2.11. Schematic circuit of a capacitive voltage divider circuit.

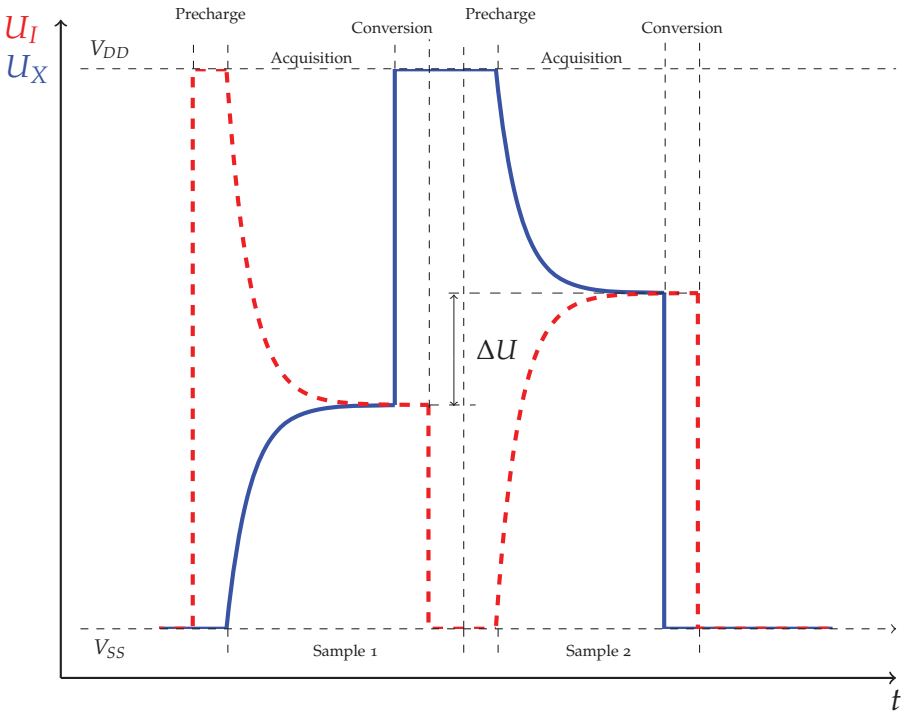

Figure 2.12. Signal graph of one conversion cycle of a capacitive voltage divider [18].

Given the total charge after precharging:

$$Q_{tot} = (C_X + C_S)U_X + C_{HOLD}U_I, \tag{2.2}$$

the settling voltage can be specified as the total charge divided by the total capacitance, the sum of C_X and C_{HOLD}:

$$U_{set} = \frac{C_{HOLD}U_{I,0} + (C_X + C_S)U_{X,0}}{(C_X + C_S) + C_{HOLD}}, \tag{2.3}$$

with $U_{X,0}$ and $U_{I,0}$ the voltages provided for the capacitances during the precharge phase. With $U_1 = U_{set}(U_{X,0} = V_{SS}, U_{I,0} = V_{DD})$ and $U_2 = U_{set}(U_{X,0} = V_{DD}, U_{I,0} = V_{SS})$ the differential result yields:

$$\Delta U_{ref} = U_2 - U_1 = (V_{DD} - V_{SS})\frac{(C_X + C_S) - C_{HOLD}}{(C_X + C_S) + C_{HOLD}}. \tag{2.4}$$

Introducing a change of the external capacitance $C_X = C_{X,old} + \Delta C$ the differential voltage results in:

$$\Delta U_{ref,\Delta C} = U_2 - U_1 = (V_{DD} - V_{SS})\frac{(C_X + \Delta C + C_S) - C_{HOLD}}{(C_X + \Delta C + C_S) + C_{HOLD}}, \tag{2.5}$$

and finally the CVD-signal can be calculated by subtracting (2.4) from (2.5), resulting in the normalized CVD-signal:

$$\frac{\Delta U_{ref,\Delta C} - \Delta U_{ref}}{(V_{DD} - V_{SS})} = \frac{CVD}{(V_{DD} - V_{SS})} = \frac{2C_{HOLD}\Delta C}{((C_X + \Delta C + C_S) + C_{HOLD})((C_X + C_S) + C_{HOLD})}. \tag{2.6}$$

Advantages of this method are a low dependency on V_{DD} and little hardware requirements needed due to the differential approach.
This method is implemented by MicroChip, Inc. in the *AN1478* [18].

2.7 Tuning of a LC-Resonance Circuit

LC-resonance circuits exploit the change of resonance frequency, when capacitive or inductive loads are applied to resonance circuits. In figure 2.13, a schematic circuit for capacitive measurement is displayed. This circuit was presented in sensing distances between two conducting surfaces building up the capacitance to be determined [19].
A circuit driver is tuned with an external LC-circuit to the desired operating frequency. The measurement capacitance C_X is connected in floating mode in parallel to the *LC*-circuit. The stray capacitances C_{S1} and C_{S2} are connected on both ends of the *LC*-circuit.

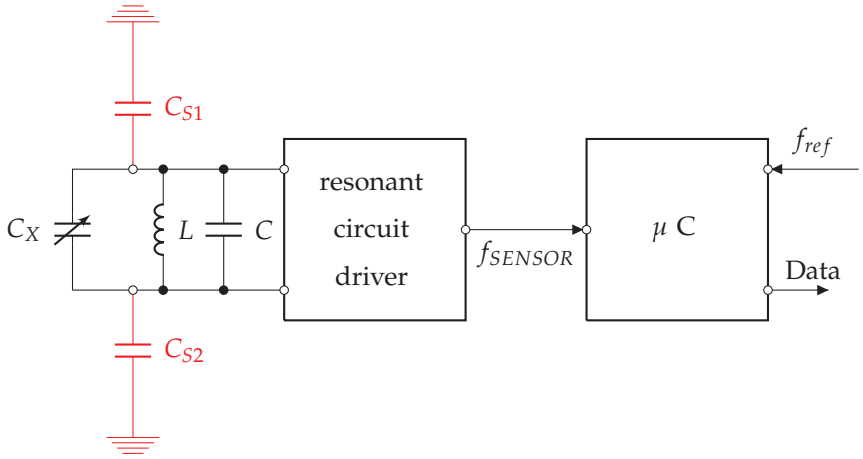

Figure 2.13. Schematic measurement circuit of LC-Oscillator capacitance meter [19].

The sensor capacitance can be determined with:

$$C_X = \frac{1}{L\,(2\pi f_{SENSOR})^2} - C, \tag{2.7}$$

with L and C the reactive components used for initial resonance frequency selection. An advantage of this circuit is, that a very high resolution or a very high sampling rate with moderate resolution can be achieved. In addition, a large dynamic range of capacitances can be measured and an insensitivity to injected charges is provided.
This measurement principle is implemented in the *FDC2x1x*-Series circuits manufactured by Texas Instruments, Inc. [19].

2.8 High-Precision Time Measurement

Time measurements can be applied to determine the charge or discharge time of a measurement capacitance. In the following, a method is described, that uses time measurements of only the discharge time of a capacitor/resistor networks to determine an unknown capacitance. Figure 2.14 illustrates a schematic circuit applying this method. In detail, a high resolution time measurement, using a Time-to-Digital-Converter (TDC) is performed. The discharge time of the measurement capacitance over a specified resistor is determined, until a predefined voltage threshold is reached. The discharge time of the sensor capacitance is measured and compared to the discharge time of an internal reference capacitance of known value. The ratio of time constants measured is directly proportional to the ratio of

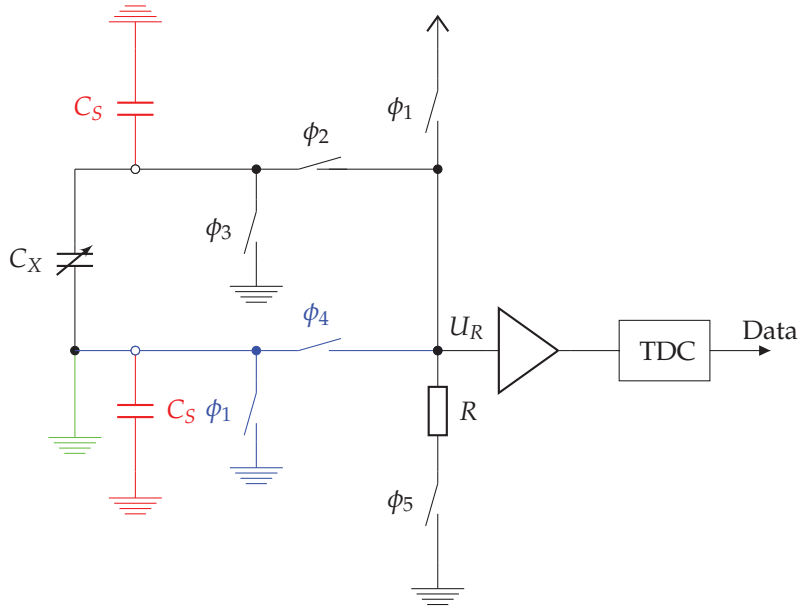

Figure 2.14. Schematic circuit of a precision time measurement [20].

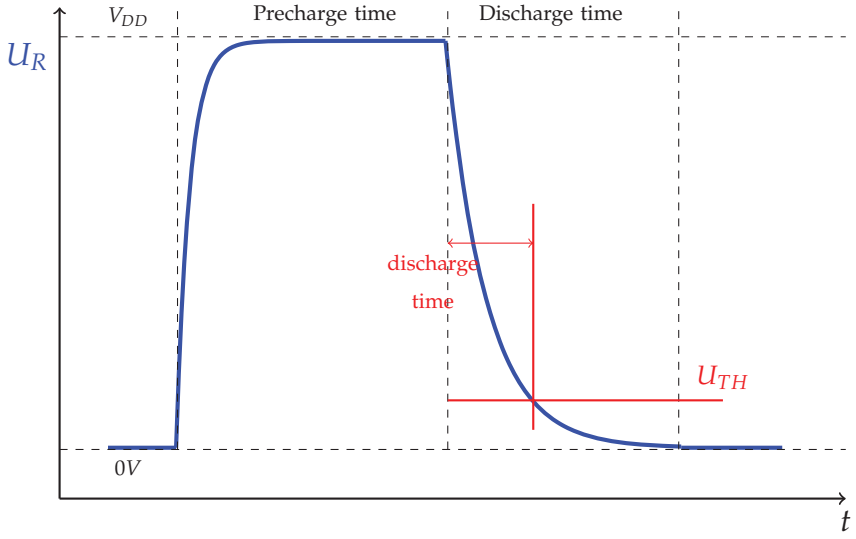

Figure 2.15. Signal graph of one measurement cycle of the discharge time measurement [20].

capacitances and ends up with $\tau = R\,C$ [20] to:

$$\frac{\tau}{\tau_{ref}} = \frac{C_X}{C_{ref}}. \tag{2.8}$$

This method can be applied to measurement capacitances in floating mode or grounded mode, figure 2.14 illustrates the grounded mode in green or the floating mode in blue. The signal graph of one measurement cycle is presented in figure 2.15. The sensor capacitance C_X is charged over the closed switches $\phi_1 = 1$ and $\phi_2 = 1$, during the precharge phase.

The time measurement starts with the discharge of the measurement capacitance, denoted as discharge phase. The switches $\phi_2 = 1$ and $\phi_5 = 1$ are closed, discharging the sensor capacitance C_X over R. The TDC measures the time needed for the RC-network to discharge, until the threshold voltage U_{TH} is reached. Using this measured time, the time-constant of the network is computed and the sensor capacitance can be calculated using (2.8). ϕ_3 is needed for initial calibration purposes.

Advantages of this method are the high resolution provided by the TDC and the fact, that the measured network is compared to an internal reference capacitance. Measurement influences like charge injection and stray capacitances can be accounted for using reference measurements. In addition the sensors can be connected in grounded or floating configuration. This method is implemented in *PCap* integrated circuits manufactured by Precision Measurement Technologies, Inc. [20].

2.9 Measurement of Differential Charges

The method of differential charges determines the measurement capacitance by comparing it to a known reference capacitance and sensing a remaining differential charge. In the following, the measurement method is described that determines a measurement charge by measuring the differential charge. The method uses the relation $Q = CU$, stating that capacitances store a defined amount of charge, when charged to a given voltage. Hence, the difference of two capacitances can be characterized by the measurement of the charge difference of these two. A circuit, which applies this method is displayed in figure 2.16.
A signal graph for the differential measurement is presented in figure 2.17. Given are the two symmetrical voltage sources U_+ and U_- referenced to ground. These charge the capacitances C_X and C_R to the voltage $|U_{ref}|$ with ϕ_1 closed. This is termed as charging phase. The amount of charge stored on each capacitance is $Q_i = C_i|U_{ref}|$. In the subsequent settling phase, the magnitude of the voltage sources is set to $U_+ = U_- = 0\,V$. Simultaneously, the switch ϕ_1 is opened and the charges of the two capacitances settle. The majority of the charges stored, compensate each other. The remaining charge is transfered to C_{INT} and forces the charge amplifier to create the output voltage U_{out}. This process follows the

relation:

$$\Delta q = Q_X + Q_R = C_X U_r ef + C_R(-U_{ref}) = U_{ref}(C_X - C_R). \tag{2.9}$$

The output voltage can be formulated as:

$$U_{out} = -\Delta q C_{INT}. \tag{2.10}$$

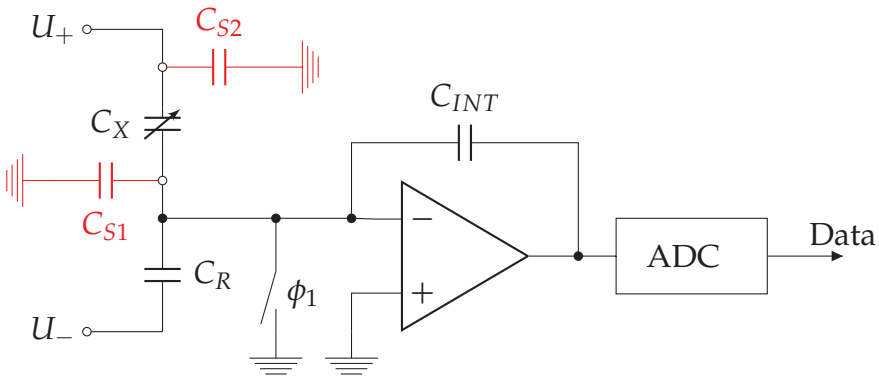

Figure 2.16. Schematic circuit for a differential charge measurement for determining a capacitance using a differential capacitive layout [21].

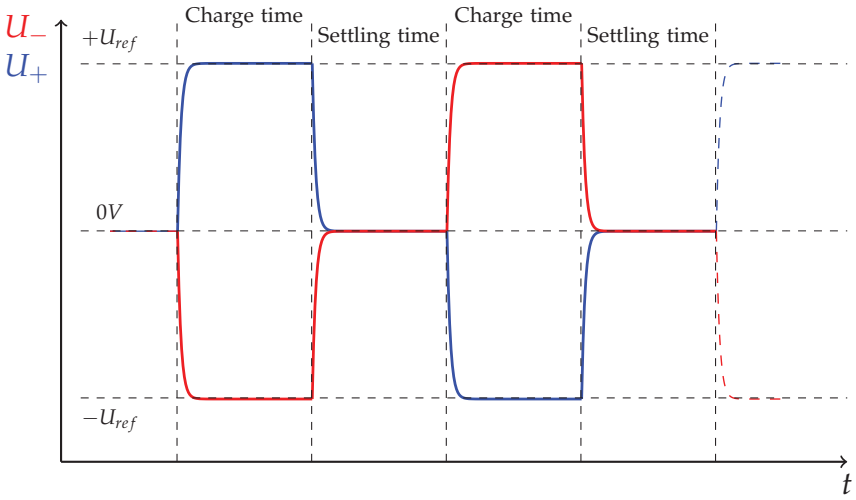

Figure 2.17. Signal graph of a differential charge measurement system for determining a capacitance [21].

This method has the advantage, that the stray capacitance C_{S1} is held to the virtual ground potential of the charge amplifier input during the charging phase. Also the stray capacitance C_{S2} has no influence.

Injected charges in the switches for the generation of U_+ and U_- and in the input stage

can have a significant influence on the differential charge transfered. Changing the polarity of U_+ and U_- and subtracting the result from the first cycle compensates for this and increases the sensitivity by a factor of 2. This method is implemented in the *MAS6510* series of MicroAnalogSystem Oy, [21].

2.10 Summary of Capacitance Measurement Circuits

The array of capacitances formed by an example ECT can be visualized as a network of capacitances, displayed in figure 1.2. Based on this schematic circuit, any measurement principle applied for ECT requires three key features. First, the ability to conduct measurements in parallel of an interconnected array of capacitances. Second, a high tolerance on stray capacitances. Due to the small changes in the sensor capacitances, stray capacitances can have a strong influence on the results of the measurements. Finally, this measurement setup does not allow for a simple parallel measurement using individual measurement ICs with internal excitation and measurement interfaces. Therefore, any applied measurement method needs to work with a common external excitation of all capacitances, as provided in [12]. This requires the measurement circuit to operate with capacitances in floating mode. Concluding, an overview of the applicability of the presented methods is given in table 2.1. In the table, the previously described methods are compared in terms of sensitivity to stray capacitances and sensor mode. Furthermore, if the method allows to operate the ICs in parallel. Given the summary presented, three methods match the prerequisites of parallel measurement ability, resistance to stray capacitances and operating in floating mode:

- AC-circuits.
- Switched-capacitor-CDC.
- Differential charge measurement.

There was no integrated solution found of AC-circuits designed for capacitive sensing. As a result, in this work the switched-capacitor-CDC using ΣΔ-modulation was chosen. The following section covers ΣΔ-modulators for the application of ADCs and switched-capacitor-CDCs based on this principle.

Table 2.1. Comparison of the presented capacitive measurement principles towards application in a multi-channel capacitance measurement-system.

principle	parallel circuit ability	stray cap. sensitivity	sensor mode
AC-Circuits	yes	tolerant	floating
SC-CDC	yes	tolerant	floating
Diff CVD	no	intolerantyes	grounded
LC-Osc. detuning	no	intolerant	fl./gr.
High-Pr.Time m.	no	intolerant	fl./gr.
Diff. charge m.	yes	tolerant	floating

3 Capacitive ΣΔ-Converter

As a result of the analysis of different capacitive measurement ICs, the ΣΔ technology has been selected as a promising candidate for creating a multi channel capacitive measurement system. In this chapter we will investigate the feasibility of this approach.
In a comparison of analog-to-digital-converter technologies and their performance in [22], it was found that ΣΔ-converter cover a wide range of sampling bandwidth up to 10 MHz or resolutions up to 35 bits and were only in wide band applications replaced by standard-Nyquist converters. This wide range of application is due to the principles used in ΣΔ-converters such as noise-shaping and oversampling.
In this chapter we will first review the principle of the ΣΔ-approach and how it can be used for capacitance measurements. We will then show first measurements for a parallel measurement system and analyze the approach.

3.1 The ΣΔ-Analog-to-Digital-Converter

Analog-to-digital-converters are systems that convert analog signals, which are continuous in time and magnitude, into digital signals that are discrete in time and magnitude. These systems contain at least, a sampling unit and a quantizer. In addition, most converters include an anti aliasing filter (AAF) to prevent the aliasing effect. Detailed information on the topic of aliasing is available in literature, for example [23]. A general circuit with an AAF is shown in figure 3.1.
The anti-aliasing-filter limits the pass bandwidth of $x_{\mathrm{a}}(t)$ to half of the sampling rate $f_{\mathrm{b}} = \frac{f_{\mathrm{S}}}{2}$, giving $x_{\mathrm{f}}(t)$. The sample-hold unit samples the signal with the sampling frequency f_{S}. After the sample-hold unit the signal is given by $x_{\mathrm{s}}(n) = x_{\mathrm{f}}(n \cdot \frac{1}{f_S})$. in order $x_{\mathrm{s}}(n)$ is quantized using N bits to the digital signal $Y_{\mathrm{d}}(n)$.

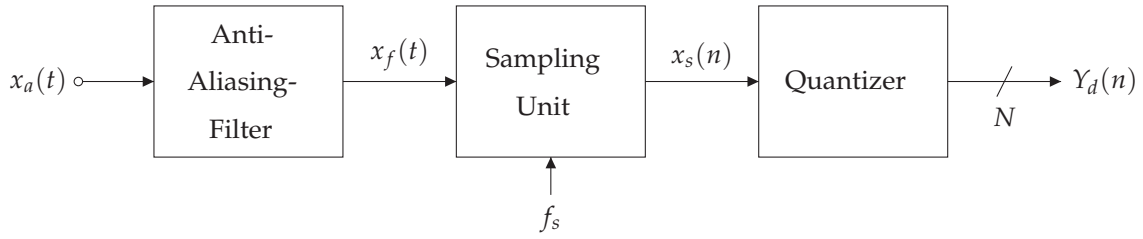

Figure 3.1. Analog-to-digital converter [22].

Two basic operations can be identified in analog-to-digital conversion, sampling and quantization. In detail, sampling performs a time discretization and quantization performs a magnitude discretization of the analog signal. It can be distinguished between converters, which perform sampling at minimum rate $f_\mathrm{S} = f_\mathrm{N}$ and those sampling at higher rates. f_N is denoted as the Nyquist-frequency and defined as $f_\mathrm{N} = 2f_\mathrm{b}$, with f_b the signal bandwidth. Converters sampling at minimum rate are termed Nyquist-converter. Converters, which sample at higher rates, are termed oversampling-converters.

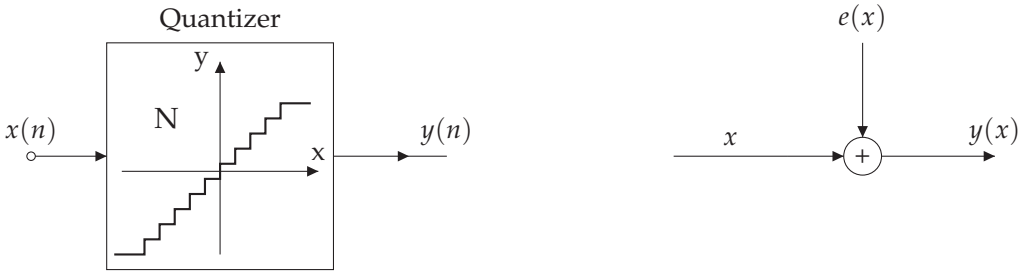

Figure 3.2. Generic N bit quantizer circuit and model of quantization error [22].

Quantization maps the continuous valued signal to a finite number of 2^N discrete levels, introducing an error termed quantization error $e(x)$. The resolution of an ADC is denoted as N in bits. The error is given as the difference between quantized signal and the input signal $e(x) = y(x) - x$, as figure 3.2 illustrates. The error is bounded inside the output-full-scale range of a quantizer Y_FS by half the quantization interval Δ, with $x < X_\mathrm{FS}$, and X_FS being the input-full-scale range. The interval Δ is defined as $\Delta = Y_\mathrm{FS}/(2^N - 1)$. Assuming randomly changing samples for an ideal quantizer, the quantization error can be modeled as a zero mean random process with uniform probability density function (PDF) in the range of

$\pm\Delta/2$. Subsequently the power associated with the quantization error can be expressed as:

$$\overline{e^2} = \sigma^2(e) = \int_{-\infty}^{+\infty} e^2 PDF(e) de = \frac{1}{\Delta}\int_{-\Delta/2}^{+\Delta/2} e^2 de = \frac{\Delta^2}{12}. \tag{3.1}$$

The power density function is defined as the Fourier-transform of the autocorrelation function, which is known as the Wiener-Khinchin-theorem [23]:

$$S_{xx}(e^{j\omega}) = \sum_{m=-\infty}^{+\infty} r_{xx}[m] e^{-j\omega m}. \tag{3.2}$$

Assuming uncorrelated samples for the quantization error, the PSD is constant for the frequency range $[-f_S, +f_S]$, which is the property of white noise. This allows to express the associated power as follow:

$$\overline{e^2} = P_Q = r_{ee}[0] = \int_{-\infty}^{+\infty} S_E(f) df = S_E \int_{-f_s/2}^{+f_s/2} df = \frac{\Delta^2}{12}, \tag{3.3}$$

which yields for

$$S_E(f) = \frac{\overline{e^2}}{f_S} = \frac{\Delta^2}{12 f_s}. \tag{3.4}$$

Equation (3.4) shows that the magnitude of the PSD of the quantization error decreases when the sampling frequency increases. In general the reduction in SNR contributed by the quantizer through the *in-band quantization error power* P_Q is calculated in (3.3). Concluding, the *Dynamic Range* (DR) of an ADC can be calculated by the power ratio of a sinusoidal signal with maximum amplitude to the in-band noise power P_Q. With the maximum input amplitude achievable at half the full-scale input range $X_{FS}/2$:

$$P^{out}_{X_{FS}/2} \cong \frac{(Y_{FS}/2)^2}{2} \cong \frac{(2^N\Delta/2)^2}{2} = 2^{2N-3}\Delta^2, \tag{3.5}$$

results in a DR of:

$$DR = \frac{P^{out}_{X_{FS}/2}}{P_Q} = \frac{3}{2}2^{2N} \implies DR|_{dB} = 6.02N + 1.76, \tag{3.6}$$

with N the number of bits. Equation (3.6) is a measure of quality of ADCs, also known as Signal-to-Noise-Ratio (SNR). To furthermore increase the accuracy of analog-to-digital conversion, ΣΔ-converters apply two basic concepts to decrease the in-band quantization error power, termed *Oversampling* and *Noise Shaping*.

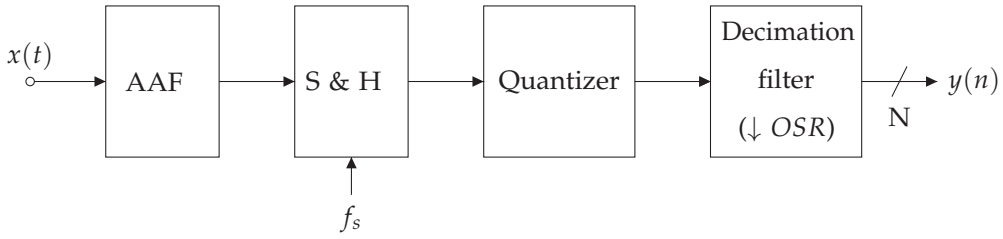

Figure 3.3. Analog-to-digital circuit with oversampling and decimator [22].

3.1.1 Oversampling

Sampling a signal faster than at Nyquist-rate is termed oversampling and is expressed in the Oversampling ratio (OSR). An example circuit is displayed in figure 3.3, extending the basic structure with a decimation filter. After the quantization process, the decimation filter reduces the signal rate to the Nyquist rate. The OSR is defined as the ratio of sampling frequency to Nyquist frequency:

$$OSR = \frac{f_s}{f_N} = \frac{f_s}{2f_b}. \tag{3.7}$$

The increased sampling frequency enlarges the spectral distance of the signal aliases to the signal band after sampling. The power of quantization noise remains constant, the magnitude of the PSD is reduced. The decimation filter limits the frequency range of the quantization noise to $[-f_b, +f_b]$ by filtering, yielding to the in-band power of the quantization noise of:

$$P_Q = \int_{-f_b}^{+f_b} S_E(f)df = \int_{-f_b}^{+f_b} \frac{\Delta^2}{12f_s}df = \frac{\Delta^2}{12OSR}, \tag{3.8}$$

Subsequently, the dynamic range for oversampling converters cane be denoted as:

$$DR = \frac{P^{out}_{X_{FS}/2}}{P_Q} = \frac{3}{2}2^{2N}OSR, \tag{3.9}$$

and can be expressed in dB as:

$$DR|_{dB} = 6.02N + 1.76 + 10\log_{10}(OSR). \tag{3.10}$$

Thus, sampling at higher frequencies in combination with the decimation filter improves the effective resolution of analog-to-digital converters. This can be further improved by noise shaping.

3.1.2 Noise Shaping

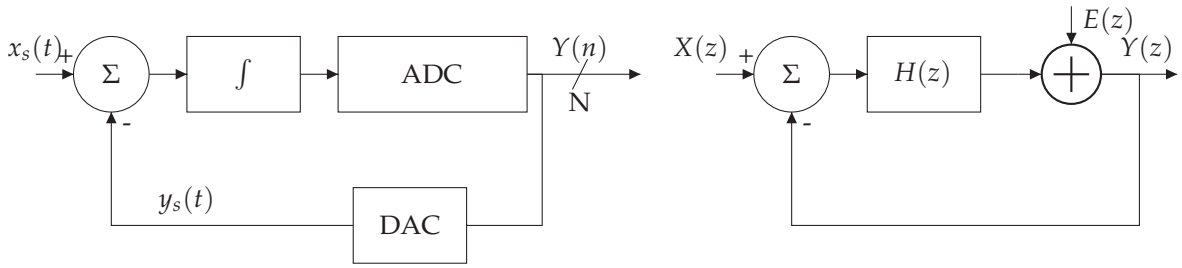

Figure 3.4. ΣΔ-modulator circuit consisting of a feedback loop for the purpose of noise shaping, the analog circuit is displayed on the left and the discrete time circuit is depicted on the right [22].

The approach to further increase accuracy is to reduce the power of the quantization error inside the signal band. This technique is termed noise shaping, which is realized by a ΣΔ-modulator. The circuit of a 1^{st}-order ΣΔ-modulator and its discrete time model are illustrated in figure 3.4. Noise shaping is achieved by means of converting back the quantized signal to an analog signal. This signal then serves as a feedback for the input signal. Based on this schematic circuit, the output signal $Y(z)$ consists of the filtered input signals $X(z)$ and $E(z)$. The input signal $X(z)$ and the noise input $E(z)$ are filtered with the filter transfer functions $H_{X\to Y}$ and $H_{E\to Y}$ accordingly. The output signal can be denoted as follow:

$$Y(z) = H_{X\to Y}X(z) + H_{E\to Y}E(z). \tag{3.11}$$

The filter transfer function for the input signal is termed Signal-Transfer-Function (STF) and for the noise input Noise-Transfer-Function (NTF):

$$STF(z) = H_{X\to Y}, \qquad NTF(z) = H_{E\to Y}. \tag{3.12}$$

Hence, the output can be rewritten as:

$$Y(z) = STF(z)X(z) + NTF(z)E(z). \tag{3.13}$$

The transfer functions are defined as:

$$STF(z) = \frac{H(z)}{1+H(z)}, \qquad NTF(z) = \frac{1}{1+H(z)}. \tag{3.14}$$

Hence, the signal and the quantization noise are affected by different transfer functions. The transfer function $H(z)$ represents the integrator within the ΣΔ-modulator and is given

by:

$$H(z) = \frac{1}{z-1}. \tag{3.15}$$

This gives for the transfer functions:

$$STF(z) = z^{-1} \rightarrow |STF(z)| = 1, \qquad NTF(z) = 1 - z^{-1}. \tag{3.16}$$

Equation (3.16) states, that the input signal passes the modulator delayed. The noise input $E(z)$ is filtered by a high pass filter. Considering solely the noise input for the output signal, it can be written:

$$E_{e\rightarrow y}(z) = (1 - z^{-1})E(z). \tag{3.17}$$

In discrete-time domain (3.17) yields to:

$$Y_e(n) = e(n) - e(n-1). \tag{3.18}$$

The result in (3.18) shows, that the 1^{st}-order ΣΔ-modulator performs a subtraction of two consequential noise samples. This hardware architecture can be repeated to form higher order ΣΔ-modulators. This results for the filtered noise at the output in:

$$E_{e\rightarrow y}(z) = (1 - z^{-1})^L E(z). \tag{3.19}$$

Hence, the NTF can be written as:

$$NTF(z) = (1 - z^{-1})^L, \tag{3.20}$$

with L denoting the order of the ΣΔ-modulator. The STF remains constant for higher order of the modulators:

$$|STF(z)| = 1. \tag{3.21}$$

To account for the effect of filtering of a stochastic process, the spectral power is described.

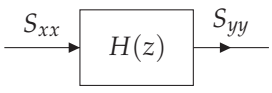

Figure 3.5. Filtering of a stochastic process with PSD.

The effect of filtering of a stochastic process is schematically displayed in figure 3.5 and ends up to:

$$S_{yy} = |H(z)|^2 S_{xx}. \tag{3.22}$$

Hence, the spectral power of the modulator output can be calculated as:

$$|NTF(e^{j\theta})|^2 = |1 - e^{-j\theta}|^{2L} = 2^{2L} sin^{2L}\left(\frac{\theta}{2}\right), \tag{3.23}$$

with

$$\theta = \frac{2\pi f}{f_s}. \tag{3.24}$$

Combing oversampling and a ΣΔ-modulator, the ΣΔ-ADC is realized.

3.1.3 ΣΔ-Analog-to-Digital Converter

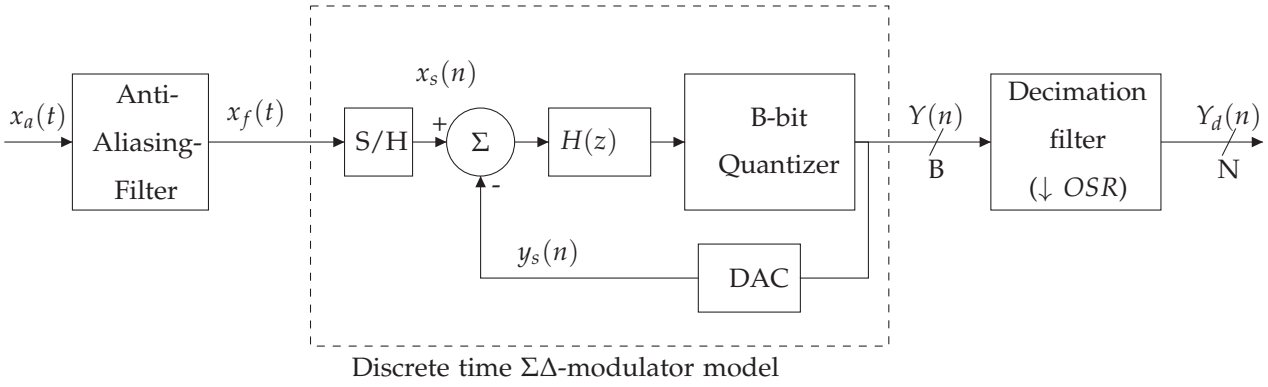

Figure 3.6. Discrete time ΣΔ-analog-to-digital circuit model.

Based on the general ADC scheme shown in figure 3.1, a basic scheme of an ΣΔ-ADC can be derived, consisting of three main blocks, an anti-aliasing-filter, the ΣΔ-modulator and a decimation filter, shown in figure 3.6. In order for the circuit to work as a ΣΔ-modulator, two properties have to be fulfilled. The input signal must not be affected and the noise transfer function must act as a high pass filter:

$$|STF(z)| = 1, \qquad NTF(z) = TF_{HP}(z). \tag{3.25}$$

The anti-aliasing-filter restricts the bandwidth of the signal provided to the ΣΔ-modulator. The modulator performs the analog-to-digital conversion and forms the quantization error,

while leaving the input signal unaffected. Subsequently, the modulator generates a digital bit stream at the sampling rate f_S with a word length of B bit. The concluding decimation filter reduces the sampling rate of the data stream to f_N and increases the SNR.
In order to quantify the benefit of ΣΔ-ADCs, the DR is calculated. Since the input signal is not affected by the modulator, the input power remains the same as for the Nyquist-ADC (3.6). The spectral power of the modulator output is calculated using the result from oversampling (3.7). Hence, the spectral power of the modulator output results in:

$$|NTF(e^{j\theta})|^2 = 2^{2L} sin^{2L}\left(\frac{\pi f}{f_b OSR}\right). \tag{3.26}$$

For a large OSR, the spectral power of the transfer function inside the signal band ($f \leq f_b$) is negligible and P_Q yields with the decimation filter applied to:

$$P_Q = \int_{-f_b}^{+f_b} \frac{\Delta^2}{12 f_s} |NTF(f)|^2 df \approx \frac{\Delta^2}{12} \frac{\pi^{2L}}{(2L+1)OSR^{2L+1}}. \tag{3.27}$$

Using (3.6) and (3.27), the dynamic range of ideally oversampled and noise shaped converter ends up to:

$$DR = \frac{P_{X_{FS}/2}^{out}}{P_Q} \approx \frac{3}{2} 2^N \frac{(2L+1)OSR^{(2L+1)}}{\pi^{2L}}, \tag{3.28}$$

and can be expressed in dB as:

$$DR|_{dB} \approx 20\log_{10}(2^N - 1) + 1.76 + 10\log_{10}\left(\frac{2L+1}{\pi^{2L}}\right) + (2L+1)10\log_{10}(OSR). \tag{3.29}$$

The number of bits is denoted as N, the order of the ΣΔ-modulator as L and the oversampling ratio as OSR. The ΣΔ-principle introduces additional terms to ADCs to the overall equation for the DR, compared to (3.10). The first term shows the gain contributed by noise shaping, whose gain is decreasing with higher orders of noise shaping. The second term shows the contribution due to oversampling.
After specification of performance metrics for ideally ΣΔ-analog-to-digital-converters, the practical implementation of these will be covered.

3.1.4 Realization of a ΣΔ-ADC in Switched-Capacitor Technology

ΣΔ-analog-to-digital-converters are implemented using two main topologies, the switched-capacitor (SC) approach described in [1] and the continuous-time (CT) approach described

in [24]. The SC-approach is preferably used due to the fact, that this topologies can be easily produced. A 1^{st}-order ΣΔ-ADC in SC technology is depicted in figure 3.7.

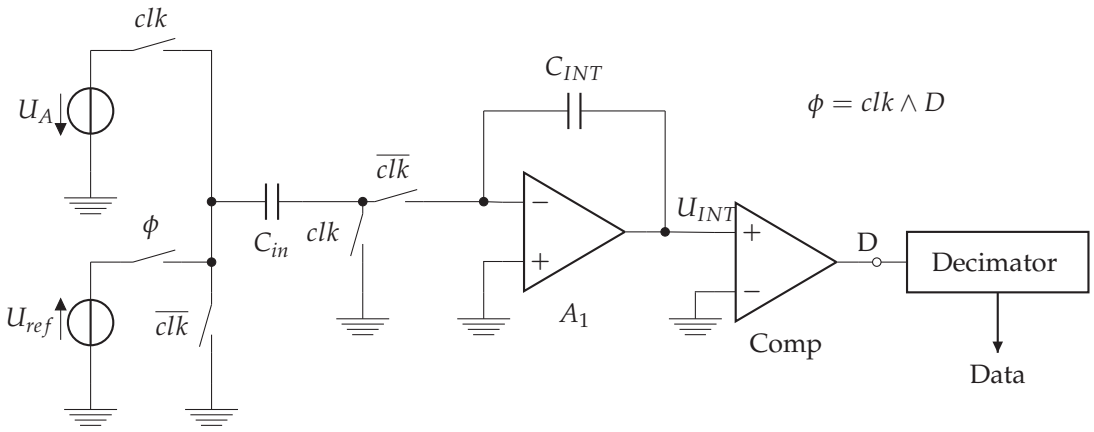

Figure 3.7. Block diagram of a ΣΔ-ADC.

For describing the function of the circuit, let us assume that U_{ref} is a DC-voltage and U_{A} is varying slowly with respect to *clk*. In addition, we assume $U_{\text{INT}} < 0$ for the initial time point.

In the following the subsequent steps of one measurement cycle are described. Starting in the *clk*-phase, the capacitance C_{in} is charged to U_{A}. The charge stored in C_{in} is $q_{\text{in}} = C_{\text{in}} U_{\text{A}}$. In the subsequent $\overline{clk}$-phase, the charge q_{in} is transfered to C_{INT}. This increases U_{INT} by $\frac{q_{\text{in}}}{C_{\text{INT}}}$.

After numerous charging and transferring cycles, U_{INT} exceeds 0 V. In the subsequent *clk*-phase, C_{in} is charged to $U_{\text{A}} - U_{\text{REF}}$, with $U_{\text{REF}} > U_{\text{A}}$. In the following $\overline{clk}$-phase, charge in the quantity of $(U_{\text{A}} - U_{\text{REF}})C_{\text{in}}$ is extracted from C_{INT}. This decreases U_{INT} to < 0 V. After N *clk*-cycles, D represents the number of discharge events. The ratio of $\frac{U_{\text{A}}}{U_{\text{REF}}}$ is equal the ratio of $\frac{D}{N}$.

The easy implementation of SC-technology is the main reason for the wide application, accepting the large number of steps required for one measurement. An advantage of the SC approach, is the simple adaption to measure other quantities such as capacitances. This adaption requires two changes. Firstly, the unknown voltage is replaced by the reference voltage with positive sign $U_{\text{A}} = U_{\text{ref}}$. Secondly, the capacitance is replaced with a reference capacitance and a measurement capacitance is added. This yields to the circuit described in

chapter 2.5. This circuitry allows to exploit the advantages and flexibility of ΣΔ-modulators for the measurement of capacitances. The integrated circuit AD7745 manufactured by Analog Devices Inc. was used in a prototype board produced.

3.2 Prototype Board for Parallel SC-ΣΔ-CDC Measurement

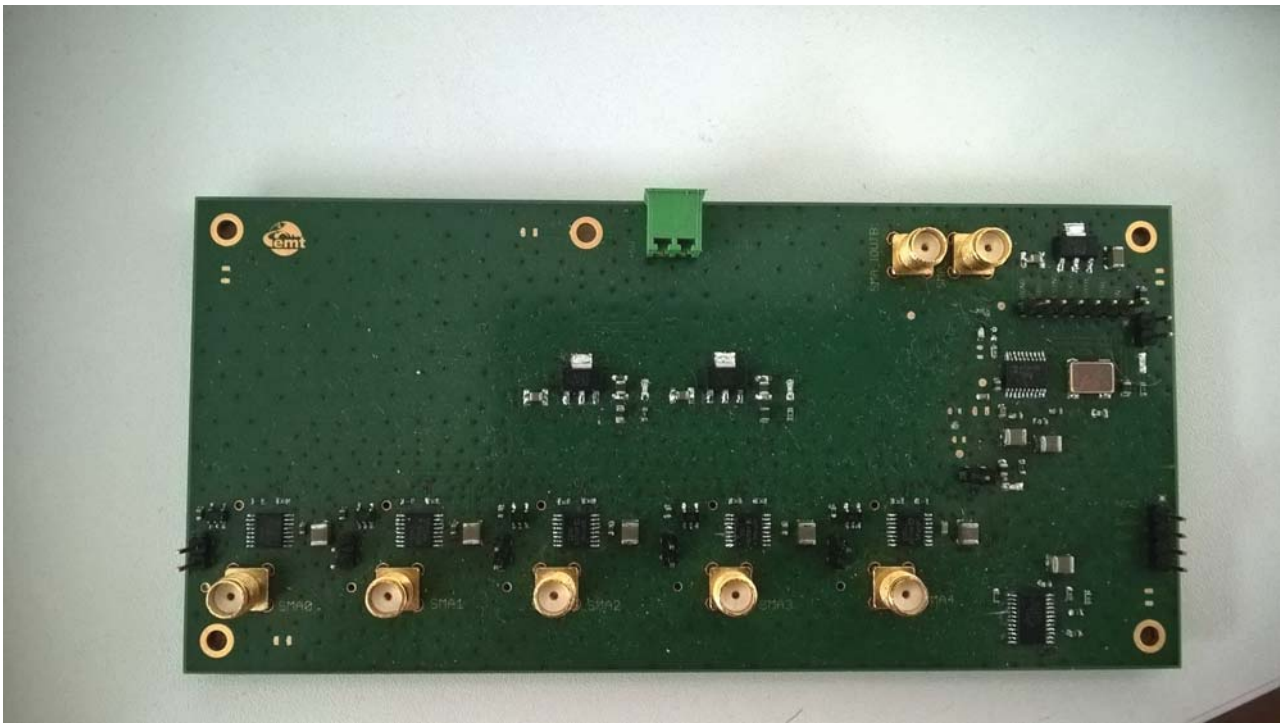

Figure 3.8. Prototype board for the detailed measurement of AD7745 towards external excitation.

As a result of chapter 2, the SC-ΣΔ-CDC AD7745 was identified as a possible solution to perform parallel multi-channel capacitance measurements. For the purpose of testing the SC-ΣΔ-CDCs, the prototype board illustrated in 3.8 was developed. The board is designed in order to have access to all pins of interest for the purpose of testing parallel measurements. The prototype board consists of five individual AD7745 with an externally provided buffer for the sensor excitation source and individual connectors for the buffered source and the measurement input. All five CDCs are connected to an 8-channel I^2C-switch PCA9548A. In addition, a SPI-controlled digital signal generator AD5932 was implemented for the

purpose of providing a common external on-board excitation source.
The AD7745 is designed to operate individually. It internally generates an excitation signal to perform stand alone capacitance measurements. In order to perform parallel multi-channel measurements, a common external excitation source in necessary. The aim of this prototype board is to analyze the AD7745 provided with an external excitation source to drive parallel measurements of a multi-channel capacitance measurement system. For this purpose, the common excitation signal frequency is set to the internal ΣΔ-modulation frequency $f_{\text{text,exc}} = 32\,\text{kHz}$ of the AD7745, specified in the data sheet [25].

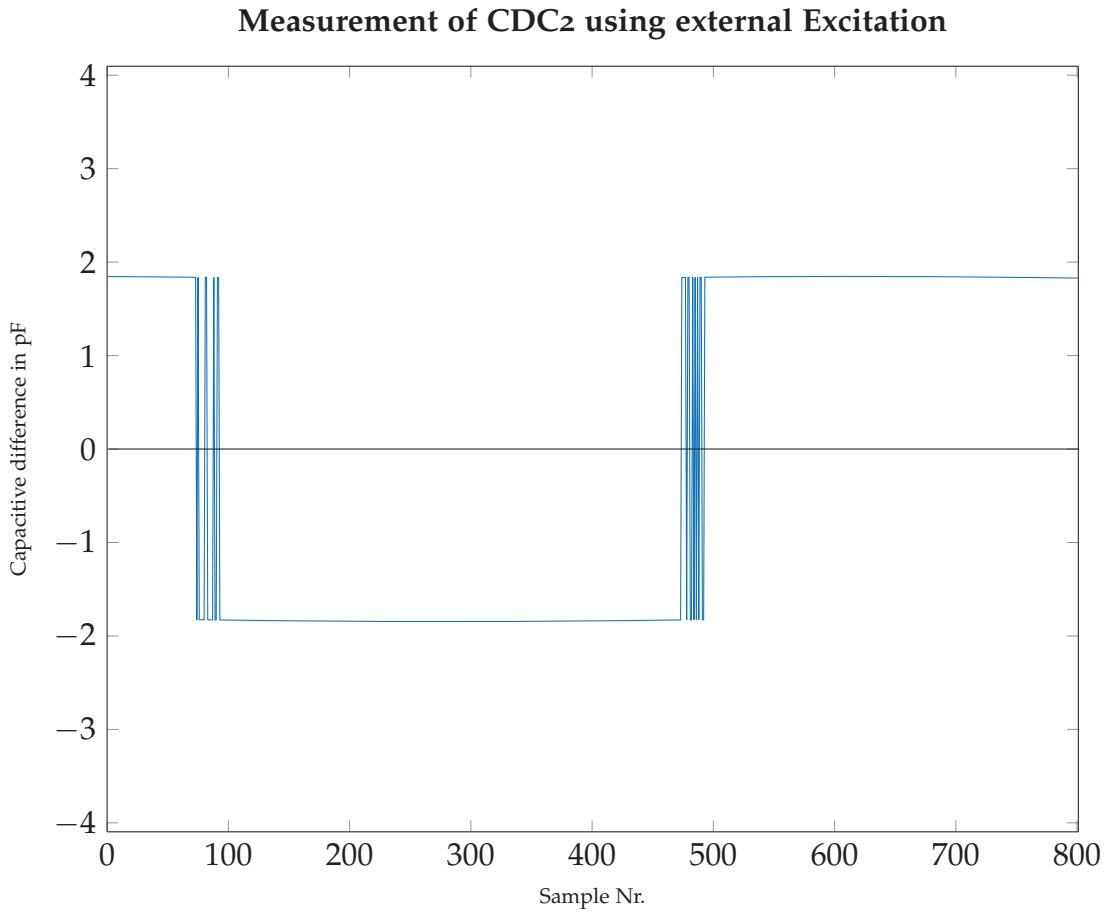

Figure 3.9. Signal graph of 800 consecutive data points measured with CDC2 applying external excitation.

For the first experiments with external excitation a reference capacitance of $C_{\text{ref}} = 1.8\,\text{pF}$ is used. The result gained for a sequence of 800 measurements of one example CDC for a known reference capacitance is presented in figure 3.9.

As can be seen, the CDC measurements lead to the used reference capacitance for about 50 % of the number of measurements. However, the unexpected negative results show an issue about the applicability of this concept. The behavior can be explained by the external excitation signal. The internal structure of the CDC allows to perform differential measurements of two capacitances and the internal excitation source can be set to logically invert the excitation signal. Considering this details of the hardware, the measurement results appear to alternate in sign. However, when the individual internally provided excitations signal is used, this effect is not observed. Subsequently, the external excitation source is suspected as source of error.

Table 3.1. Comparison of the excitation frequencies measured from all five devices.

CDC0	CDC1	CDC2	CDC3	CDC4
32 018 Hz	32 056 Hz	32 063 Hz	32 118 Hz	32 097 Hz

Hence, the internal modulation frequencies of the individual ICs were determined. The results gained are listed in table 3.1. The modulation frequency is subject to variation and differ from the common external excitation frequency. It is suspected that these small variations of the excitation frequency are the reason for the unexpected measurement results.

In order to verify that the source of error is the variation of the modulation frequency, a simulation is conducted. In the following section the simulation of a 1^{st}-order ΣΔ-CDC is described.

3.3 Simulation of a SC-ΣΔ-CDC with External Excitation

Based on the results gained of the measurement of the AD7745 prototype board, the behavior shall be verified by means of simulation. For the simulation the model in figure 3.10 is used. This model is extended with an external clock source and a reset switch to define a start point for the integrator circuit. The aim of the simulation is to investigate for the effect of an external excitation, which runs asynchronous to the internal. The simulation

is conducted in MATLAB/Simulink (The MathWorks, Natick, MA), using the Simscape-extension, which provides the features for simulation of physical networks, such as electrical circuits.

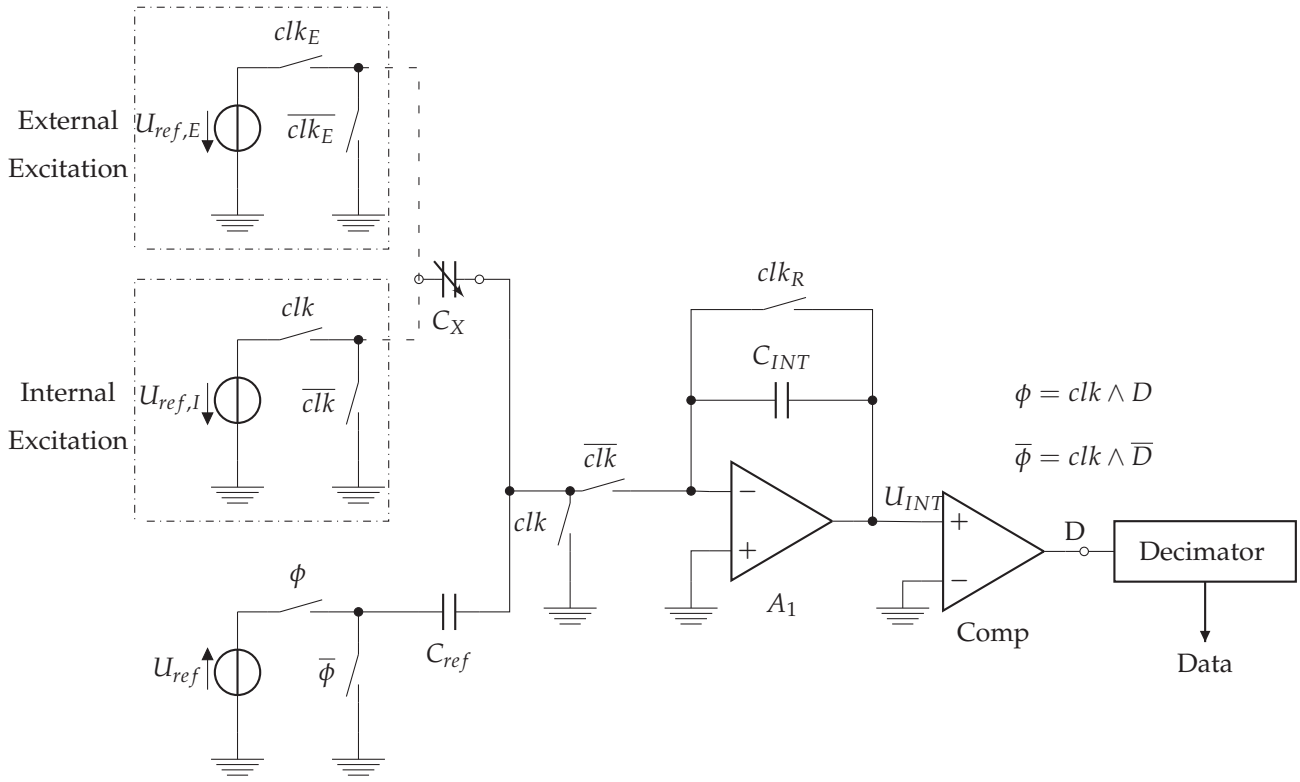

Figure 3.10. Block diagram of a ΣΔ-CDC for the simulation of the system behavior of floating feed-through capacitances with an external excitation source.

In the simulation, a 1st-order 1 bit ΣΔ-Modulator with an OSR of 32 is used. The integrating amplifier and the comparator are modeled with their ideal properties. They have no input currents or offset voltages. Further, they posses an infinite Slew rate, current output and no bandwidth limitation. In order to have a defined output of the comparator at the time steps, a Sample/Hold-unit triggered with the rising edge of *clk* succeeds the comparator in the simulation. The capacitances are modeled with an in series resistor of 0.01 Ω and C_{INT} and C_{ref} have a capacitance of 8 pF each. The variable capacitance C_{X} is set to 2.12 pF. The input reference voltage U_{ref} is set to 1 V. The clock sources are specified in order to have 32 clock cycles of charge transfer, before a reset pulse is formed to discharge C_{INT}. The external clock clk_E is modeled to differ 0.5 % of the internal clock source *clk* for improved visibility. Nevertheless, the results do not change for smaller differences.

The results are presented in figures 3.11 to 3.13. The top graph displays the clock signals of the circuit, controlling the switches. Below the reset clock is depicted. In the high-phase of the reset clock, the feedback capacitor C_{INT} is short circuited and discharged. The middle row shows the output signal of the comparator. In the reset phase, the output signal of the comparator is corrupted, due to numerical limitations of the simulation program. The fourth row illustrates the subsequent S&H-unit and it can be observed that the numerical errors of the simulation are suppressed in the output signal. In the bottom line the graph of the integrator output is presented. This graph illustrates the stepwise charging and discharging of the feedback capacitor. When $U_{\mathrm{INT}} > 0$ the comparator toggles the output to '1'.

The results of the first simulation conducted are displayed in figure 3.11. In this simulation the internal excitation is used to verify the functionality of the model. In the subsequent simulations an external excitation is used, one with synchronous start and one with asynchronous start.

The overall result of the first simulation for one simulated cycle, $D = 9$ '1's in 32 cycles, results in:

$$C_{test} = \frac{D}{N} \cdot C_{INT} = \frac{9}{32} \cdot 8\,\mathrm{pF} = 2.25\,\mathrm{pF}. \tag{3.30}$$

Due to considerably short decimation filter, the result gained differs from the predefined value in the simulation of $C_{\mathrm{test}} = 2.12\,\mathrm{pF}$. The difference is within the range of the resolution $\Delta C = \pm\frac{8\,\mathrm{pF}}{32} = \pm 0.25\,\mathrm{pF}$. With a prolonged decimation filter the simulation results improve accordingly.

It can be stated that the simulation conducted, works to depict the working principle of a simple ΣΔ-CDC correctly. Hence, this simulation will be used to determine the effects of asynchronous excitation of a ΣΔ-CDC.

Figures 3.12 and 3.13 illustrate the findings of the simulation with excitations with a relative frequency difference of 0.5%. In addition to the internal clock, the external clock is depicted in the first row in red. In figure 3.12 both clocks start synchronously and in figure 3.13 both clocks start asynchronously.

Comparing the integrator output from figures 3.11 to 3.12, it can be observed, that the

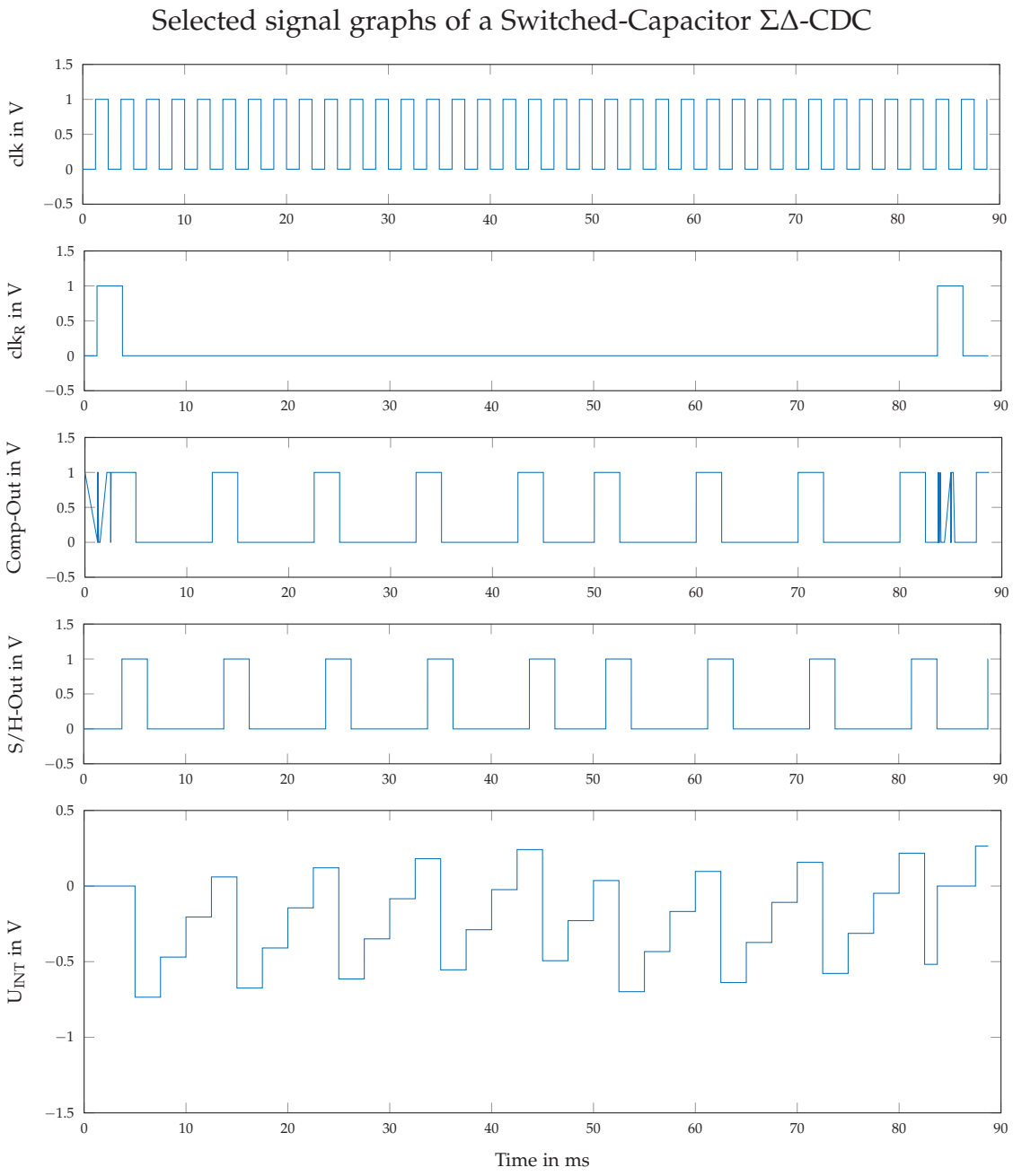

Figure 3.11. Signal graphs of the simulation of the ΣΔ-CDC for the correct excitation frequency. The signal graphs are displayed accordingly to figure 3.10.

discharge step and the subsequent charge phase do not coincide. This gap increases observably over the span of one measurement cycle as the clock cycles are diverging. However, so far the behavior is not changed, given the same result as previously simulated with synchronous excitation. The result is calculated in (3.30).

Figure 3.13 shows the results obtained with asynchronously started clock signals, depicted in

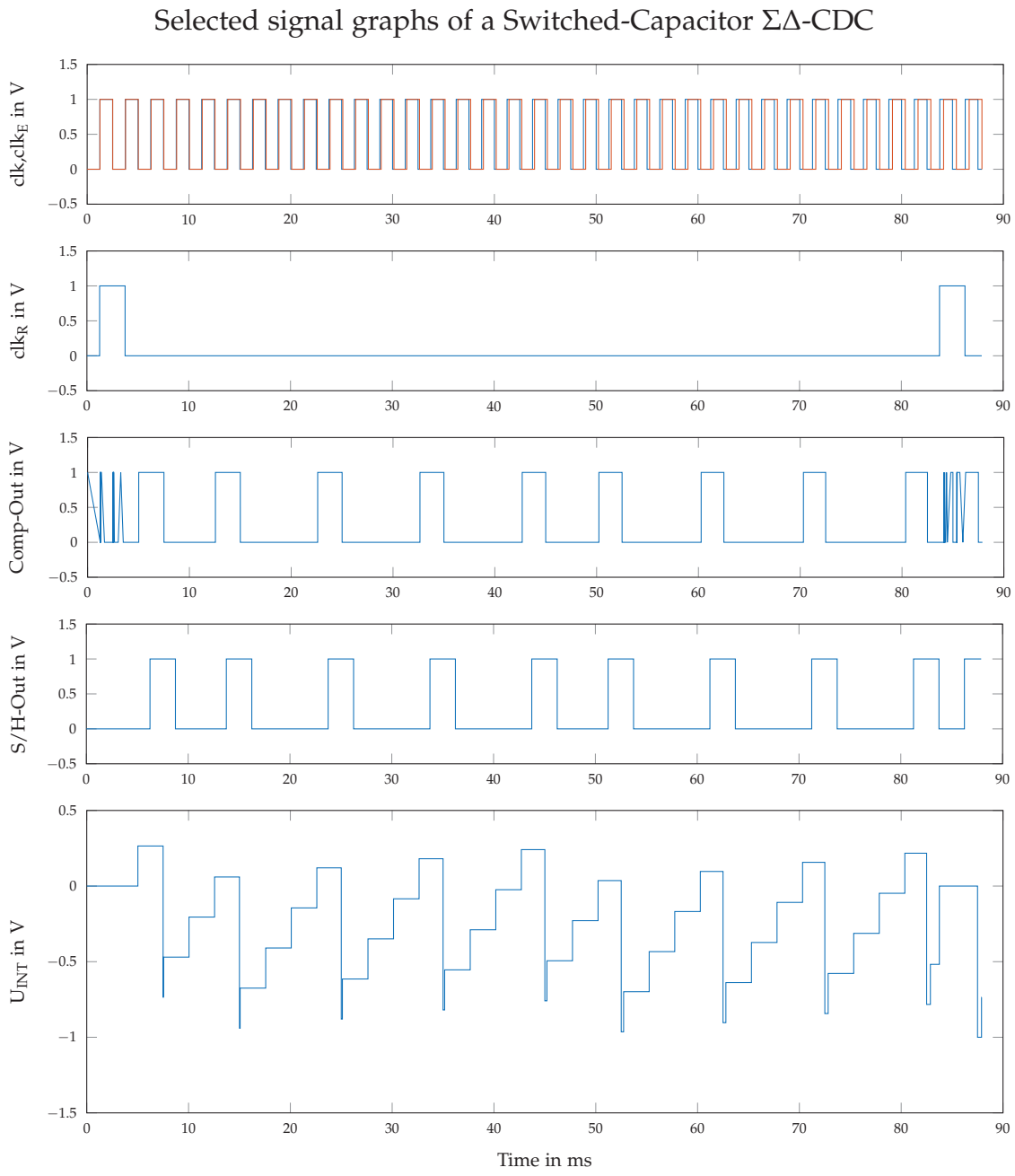

Figure 3.12. Signal graphs of the simulation of the ΣΔ-CDC for the incorrect excitation frequency with synchronous start of the clocks. The signal graphs are displayed accordingly to figure 3.10

the top row. In contest to the results gained previously, the integrator is steadily discharged after an initial extraction of charge. This happens until the end of the cycle, when the feedback capacitance is reset. Hence, the comparator is never activated in this cycle and the

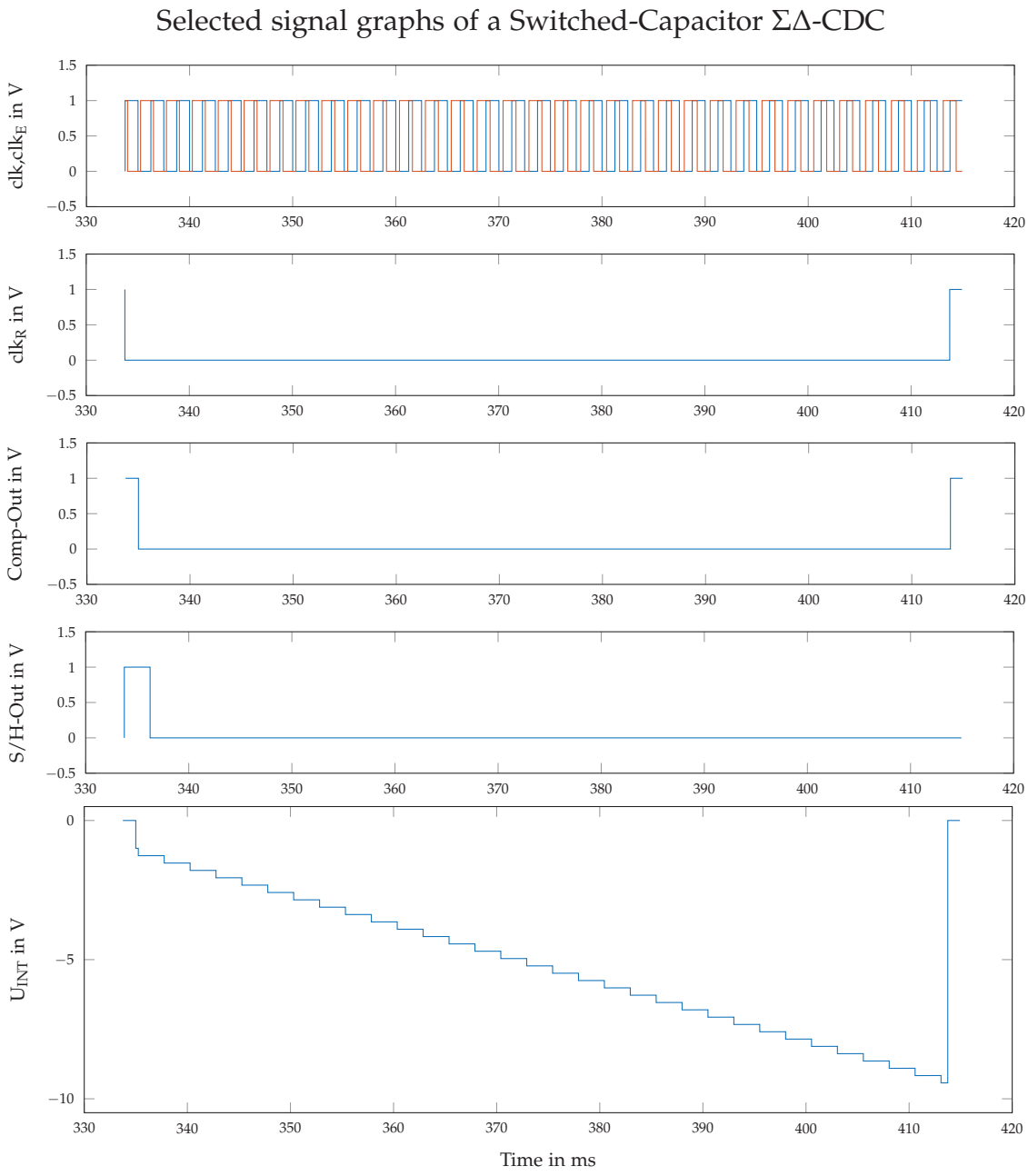

Figure 3.13. Signal graphs of the simulation of the ΣΔ-CDC for the incorrect excitation frequency with asynchronous start of the clocks. The signal graphs are displayed accordingly to figure 3.10

result gained is $D = 1$.

$$C_{test} = \frac{D}{N} \cdot C_{INT} = \frac{1}{32} \cdot 8\,\text{pF} = 0.25\,\text{pF}. \tag{3.31}$$

The result in (3.31) expresses the finding gained, if internal and external clock are nearly asynchronous. This result differs strongly from the previous ones as well as from the actual capacitance simulated.

Concluding it can be said that any difference between external excitation frequency and internal modulation frequency, introduces an alternating behavior of valid and corrupted measurements. This coincides with the measurements conducted in chapter 3.2.

3.4 Summary

Summing up the findings of all simulations and experiments conducted, offset in the excitation frequencies introduce a destabilizing effect, that prohibits a stable run with external excitation. In order, it can be stated that the ΣΔ-principle requires a fully synchronized excitation source to perform consistently. Therefore, application in a parallel measurement system would only possible with a master clock to synchronize all switch-overs of all individual circuits. Sadly no ΣΔ measurement IC allowing an external excitation was found among the product lines of IC manufacturers. In addition, another prerequisite could be derived for parallel measurement:

- Ability to synchronize internal and external excitation.

Concluding it can be stated, that the AD7745 is not usable for the purpose of this work, since no synchronization and hence parallelization can be realized.

Reviewing the measurement principles presented in chapter 2, another principle would be available, differential charge measurement systems. One integrated solutions was found, which allows the IC to be provided with an external master clock signal for all internal processes, named *MAS6510*. This IC does not use the ΣΔ principle. Hence, the measurement principle is changed to differential charge measurement and the MAS6510 is used further on. In the next chapter, the IC itself is described and the additional circuitry required to implement the parallel measurement hardware is specified.

4 Design of Parallel and Time Interleaved Measurement Hardware

As a result of the findings of the previous chapter, the ΣΔ approach is given up. In chapter 2 one other measurement principle was found promising to fulfill the prerequisites:

- Differential charge measurement.

For completeness the requirements derived to realized a parallel measurement system are recapped:

- External common excitation of the measurement system.
- Simultaneous activation of the measurement cycle.
- The necessity to synchronize internal measurement and external excitation.

The search for integrated circuits brought the *MAS6510* as a promising candidate to meet these requirements. This IC allows to have the internal processes clocked by an external master clock. Furthermore, the circuit supports the SPI-Bus, which allows to use multiple receivers simultaneously. The feasibility to use the IC with a common external excitation still has to be verified.
In this chapter, the structure of the system setup for parallel and time interleaved measurement is discussed, the features of the *MAS6510* are presented and requirements for additional hardware circuits are specified.

4.1 Measurement Setup

The schematic for the parallel measurement setup is depicted in figure 4.1. The measurement system consists of N sensor front ends with N individual measurement devices (MAS6510)

as part of the capacitive measurement system. The system is controlled by a micro controller, namely the STM32F407 micro processor. Programming, testing and data post processing is performed via a Desktop PC over a USB-connection. The microprocessor is programmed with ChibiStudio, an Eclipse based editor for programming real-time operating systems on microprocessors [26].

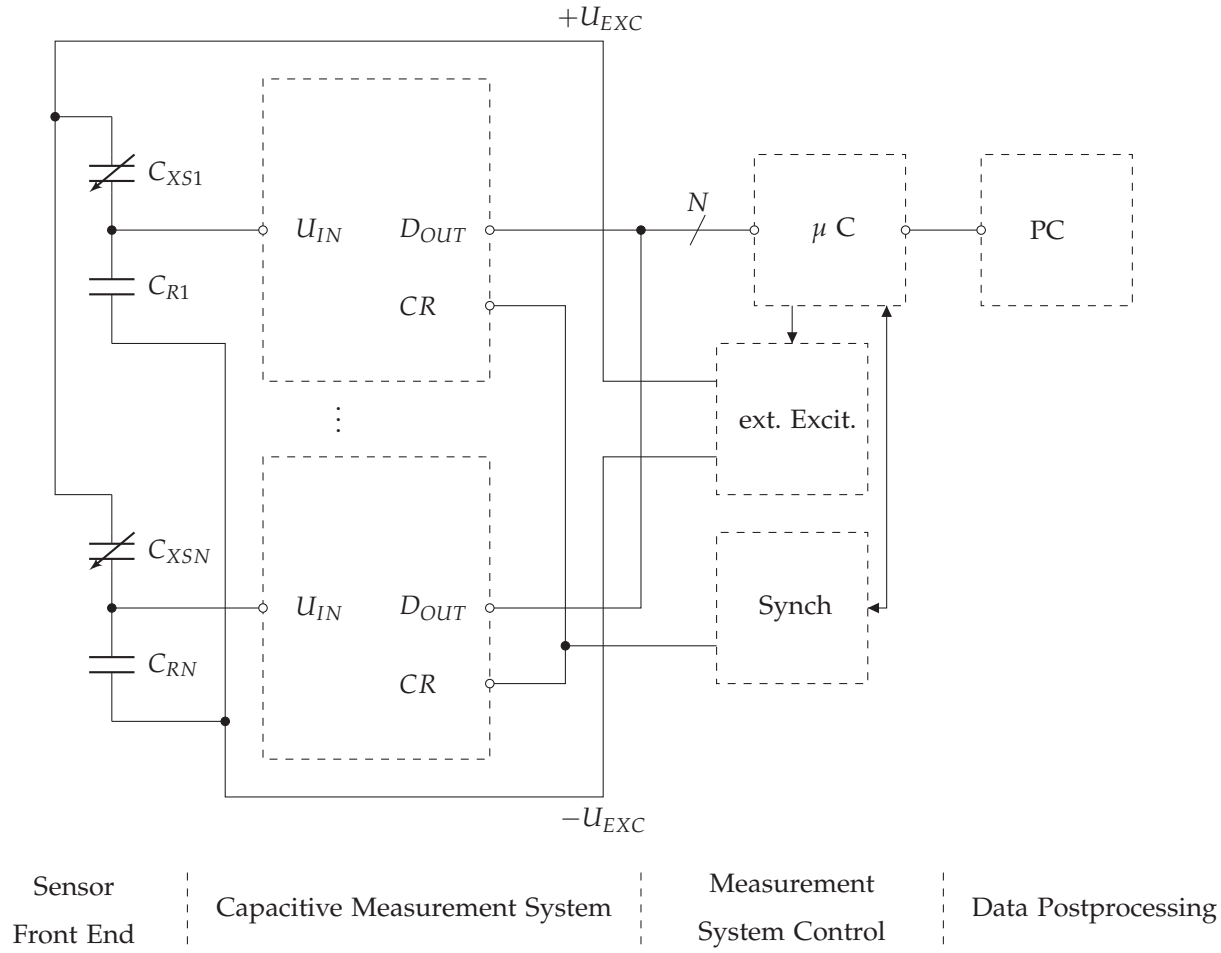

Figure 4.1. Schematic block diagram of the proposed parallel charge-based capacitive measurement system consisting of a sensor front end, N capacitive measurement devices, a micro controller for the control of the system and a PC for data post processing.

The sensor front end consists of the capacitances to be determined C_{Xi} and a reference capacitances C_{Ri} for each channel. In the example of ECT, the former are composed of a common transmitter electrode connected to the excitation source and the individual receivers to the measurement device, as seen in figure 1.2. The latter can be chosen according to the desired dynamic range of capacitances to be measured.

The capacitive measurement system consists of the equal number of *MAS6510* as capacitances to be measured. The integrated circuits communicate with the micro controller via *SPI*-bus.
Communication via SPI allows to send commands simultaneously from the master device to all receiving ICs. This enables to perform fully synchronized parallel measurements without additional circuitry. In this setup, the common excitation source is designed to be controlled by the micro controller, to facilitate the overall design. The final component is the synchronization unit. Its purpose is to synchronize the measurement cycles of the individual devices with the external excitation source.
The micro controller communicates over a serial interface with the PC. Data post processing and communication is handled by MATLAB scripts.
After the setup is defined, the requirements for the additional circuitry have to be derived. Hence, the hardware features of the *MAS6510* are described and based on these, the requirements for the additional circuits are specified.

4.2 Hardware Features, Resolution and the Sampling Rate of the MAS6510

MicroAnalogSystem Oy is the manufacturer of the MAS6510/12 [21]. It implements the differential charge method to measure capacitances and can be operated with an external master clock source. In this subsection, a short review of the important features of this chip is given and the necessities derived for the implementation of the measurement system are provided.
The full integrated circuit is depicted in figure 4.2. It provides a sensor interface for the measurement of the connected capacitances including analog-to-digital-converter, a controlling CPU and a peripheral interface for communication and signaling with other circuits. The IC is operated with a supply voltage of $V_{DD} = 1.8\,\mathrm{V}$ to $3.6\,\mathrm{V}$.
The sensor interface of the MAS6510 contains a signal generator in the MUX unit for the positive and the negative excitation voltage. The capacitances are connected between the pins *CS* - *CC* and *CR* - *CC*. At *CS* the positive internal excitation voltage is provided and

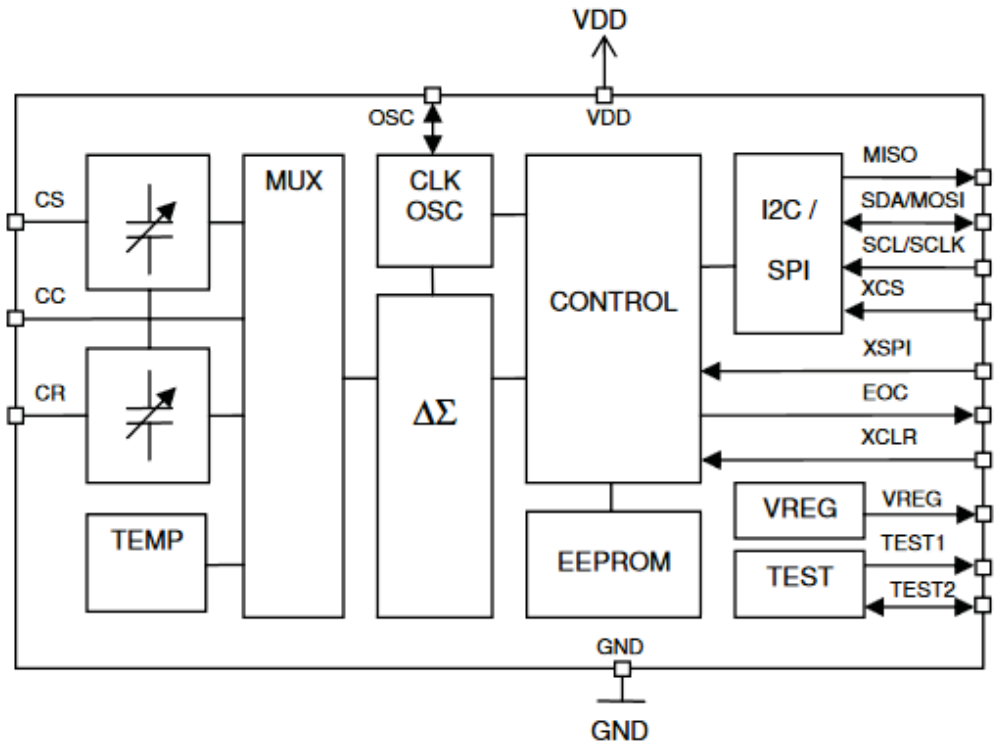

Figure 4.2. Schematic block diagram of the MAS5610 [21]).

the negative voltage at *CR*. The differential charge between the connected capacitances is measured via *CC* and converted, using the internal ΣΔ-ADC. For adjustment of the measurement range, internal capacitance matrices are connected from *CR* to *CC* and *CS* to *CC*, respectively. The most important feature for the purpose of this work is, that the ΣΔ-ADC can be set to use on an external clock-source connected at *OSC*.

All measurements performed by these chips, map the difference of the two connected capacitances into a full output scale range of 0 to 262 144, or 18 bit with an acquisition time of 5.8 ms and a range of 0 to 16 777 216 or 24 bit with an acquisition time of 82.6 ms. The range of output has to be adjusted by the excitation voltage in the range of 0.033 V to 1.407 V, selectable via serial-interface. The calculation of the actual value has to be performed by the micro-processor. To perform exact measurement, a calibration has to be conducted.

The control CPU is connected to an EEPROM, which allows certain measurement parameters to be loaded automatically at startup. All measurement parameters are stored in internal registers of the CPU and are accessible via serial-interfaces.

This device supports two types of serial-interfaces, namely the Inter-Integrated-Circuit-

Bus (I^2C) and the Serial-Peripheral-Interface-Bus (SPI), which are selected over $XSPI$-Pin. Additionally, the EOC-pin signals when a conversion is in progress or finished and the $XCLR$-pin allows to reset the chip. At $VREG$ a voltage regulator output is provided. $TEST1$ and $TEST2$ show internal signals not intended for any application.
Finally, it has to be investigated and specified, which characteristics an external excitation source has to posses and how the actual composition of the excitation signal is. These questions are investigated in the following section.

4.2.1 Application of External Excitation for the MAS6510

Prior to the application of an external excitation, the switching cycles of the chip are determined.
For this purpose, a test-IC is provided with an external clock-source, the master clock. It is connected to OSC and the internal excitation signals at CS and CR are observed. Figure 4.3 illustrates the findings. The signal switches of the excitation signal are performed internally at every rising edge of the clock-signal. Hence, the excitation frequency can be determined with $f_{EXC} = \frac{f_{osc,ext}}{4}$. In addition, it is noted that all excitation signals, as well as the sensing signal at CC, are biased to $V_{DD}/2$. This allows to maximize the signal amplitudes in a single-sided supply.

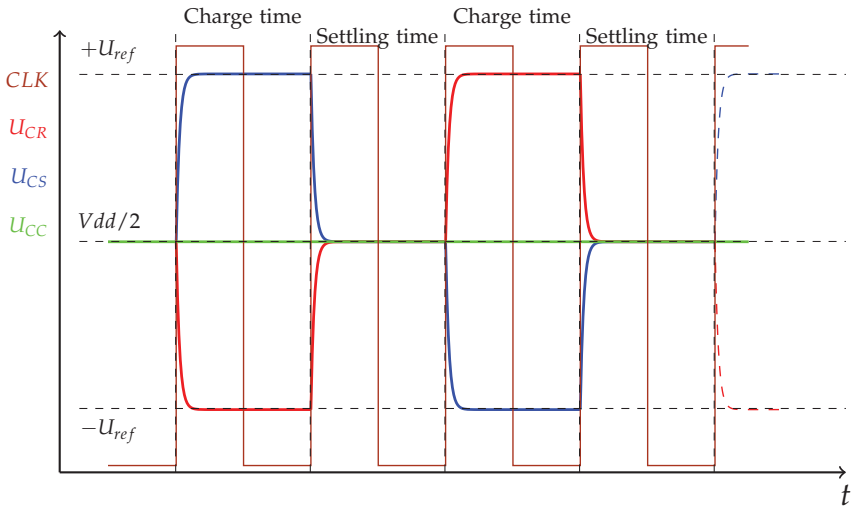

Figure 4.3. Internal excitation signal graphs of the differential charge measurement system with external clock-signal.

After the identification of the signal graph of the excitation source, it has to be verified, if the result can be reproduced by applying an external excitation source. A test setup was developed to compare both configurations. The schematic block diagram is shown in figure 4.4. A couple of test capacitances C_S and C_R are connected in turns to the internal and the external excitation source. For the external excitation, the internally generated signals are reimplemented using the Digital-to-Analog-Converters (DAC) provided in the STM32F4. The two DACs can be configured such that a provided sequence of digital values are converted. These values are sequentially updated at every rising or falling edge of an external trigger source, the master clock source.

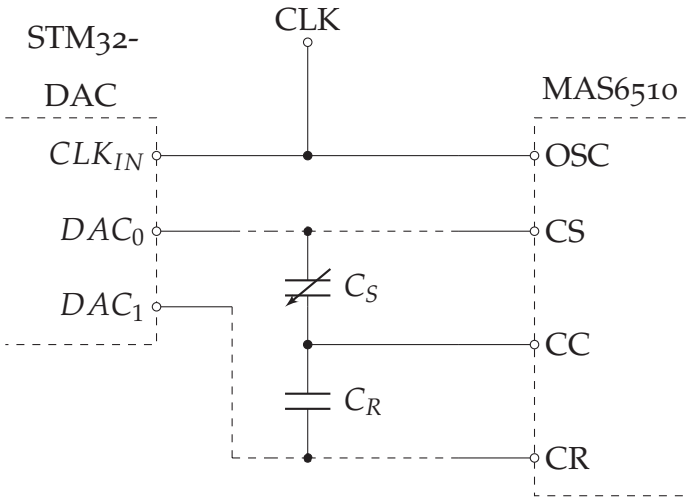

Figure 4.4. Schematic test circuit for the external excitation of a MAS6510 using edge triggered DACs of a STM32F4-Discovery-Board.

It could be confirmed, that the application of the remodeled excitation signal gives the same results as the application of the internally generated signal. However, the three different voltage levels contained by the excitation signal require proper synchronization to coincide the excitation and the measurement cycle.
Concluding, it can be stated that this CDC-solution meets the requirements stipulated at the beginning of the chapter. Hence, the operation characteristics of the *MAS6510* are presented:

- Excitation Bias voltage at CC, CR, CS: $U_B = \frac{V_{DD}}{2}$.
- Excitation voltage max amplitude at CR, CS: $U_{amp} \approx \pm\frac{V_{DD}}{2}$.
- Excitation/Measurement frequency: $f_{EXC} = \frac{f_{osc,ext}}{4}$.

These settings define the requirements for the supporting circuitry, which are specified in the next chapter.

4.3 Supporting Circuitry for the Parallel Measurement System

In the previous section it was shown, that the MAS6510 works proper when provided with an external excitation signal. The differential charge principle allows to increase the sensitivity of the differential circuit by means of increasing the amplitude of the excitation signal. In order, an amplifier is required to scale the excitation signal. Furthermore, a circuit is necessary to synchronize the external excitation source cycle and the internal measurement cycle. Lastly, an interface is required to perform receptions simultaneously. The following three features have to be realized for the parallel measurement system:

- External excitation source with variable signal amplitude.
- Synchronization of the excitation and the measurement-cycles for multiple CDC-circuits.
- Parallel communication between the microprocessor and the CDC-circuits.

Initially, the supply voltage of the board has to be defined. Two supply nets are specified:

- Analog supply: $U_{\text{sup}} = \pm 15\,\text{V}$, by an external supply.
- Digital supply: $V_{DD} = 3.3\,\text{V}$ derived from the analog supply.

4.3.1 Excitation-Signal Amplifier

It was discussed in section 2.9, that the amplitude of the excitation-voltages defines the sensitivity of the differential capacitance measured. Hence, two symmetrical amplifiers have to be realized to increase the amplitude of the excitation source and increase the sensitivity of the measurement system. Therefore, a excitation signal amplifier is connected in between the source and the measurement capacitances, displayed in figure 4.5.
The input signal of the amplifier is provided by the DA-convertes of the STM32F407 microprocessor. The output voltage of the DACs is limited by the supply voltage of the

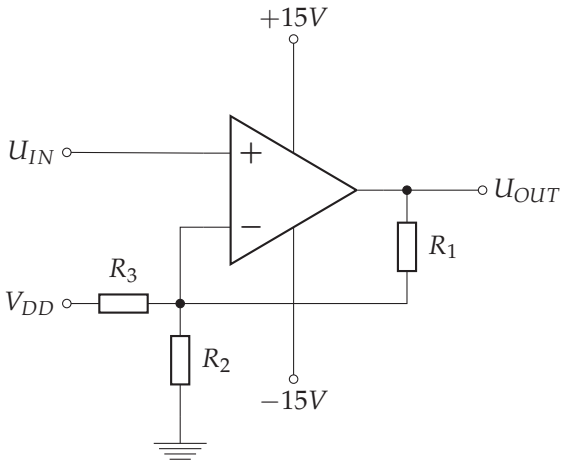

Figure 4.5. Schematic circuit of the biased DC-amplifier used in this work.

microprocessor, specified with 3.3 V and with a rather poor current driving ability of the chip. As stated in [27], the electrical load of the DAC-output has to be > 5 kΩ and the capacitive load < 50 pF, to drive the set voltage level. In order to maximize the signal output of the DAC, a bias voltage of $U_B = \frac{V_{DD}}{2}$ is introduced, allowing a maximum signal amplitude of $U_{amp,max,DAC} \approx \frac{V_{DD}}{2}$. This yields to the amplifier input requirements:

- Input voltage range: 0 V to 3.3 V.
- Input signal range: $U_B = 1.65\,\text{V}$, with $U_{amp,max,IN} \approx 1.65\,\text{V}$.
- High-input resistance $R_{in} \gg$.

The output requirements of the circuit are specified by the MAS6510 input requirements. A crucial parameter is the bias voltage of $U_B = 1.65\,\text{V}$ @ $V_{DD} = 3.3\,\text{V}$. The requirements for the operational amplifier are a high slew rate and a high gain-bandwidth product. Further, are a low output resistance and a sufficient current driving ability required to handle the fast charge and discharge processes of the connected capacitances. The maximum output amplitude of the excitation amplifier is limited by the analog supply voltage and the positive output bias voltage $U_{amp,max,OUT} = U_+ - U_B$. Hence, the minimum gain of the amplifier can be calculated. Summarized the output specifications for this circuit are:

- Output signal range: $U_B = 1.65\,\text{V}$, with $U_{amp,max,OUT} = 15\,\text{V} - 1.65\,\text{V} = 13.35\,\text{V}$.
- Low-output resistance: $Rout \ll$.

- Minimum amplification of: $V_{min} = \frac{U_{amp,max,OUT}}{U_{amp,max,IN}} = \frac{13.35\,\mathrm{V}}{1.65\,\mathrm{V}} \cong 8.1.$

The amplifier depicted in figure 4.5, is a circuit, which can provide the required functionality. The output voltage of this circuit is calculated as:

$$U_{OUT} = U_{IN}\left(1 + \frac{R_1}{R_2||R_3}\right) - V_{DD}\frac{R_1}{R_3}. \tag{4.1}$$

First, the resistive voltage divider is specified. To achieve $U_{\mathrm{OUT}} = U_B$ for $U_{\mathrm{IN}} = U_B$ the two values are applied to (4.1), resulting in:

$$\frac{V_{DD}}{2} = \frac{V_{DD}}{2}(1 + \frac{R_1(R_2 + R_3)}{2R_2R_3}) - V_{DD}\frac{R_1}{R_3}. \tag{4.2}$$

Simplified, this gives:

$$\frac{R_1}{R_3} = \frac{R_1(R_2 + R_3)}{2R_2R_3}, \qquad \rightarrow \qquad R_3 = R_2. \tag{4.3}$$

The resistors were set to $R_2 = R_3 = 20\,\mathrm{k\Omega}$. For the gain of the amplifier, the maximum output and input voltage are inserted in (4.1). With $U_{\mathrm{OUT}} = U_{\mathrm{SUP},+}$ and $U_{\mathrm{IN}} = V_{DD}$ this ends up to:

$$U_{SUP,+} = V_{DD}\left(1 + \frac{2R_1}{R_3}\right) - V_{DD}\frac{R_1}{R_3}. \tag{4.4}$$

Equation (4.4) can be reformulated to:

$$R_1 = R_3\frac{U_{SUP,+} - V_{DD}}{V_{DD}} = 20\,\mathrm{k\Omega}\frac{15\,\mathrm{V} - 3.3\,\mathrm{V}}{3.3\,\mathrm{V}} = 70.909\,\mathrm{k\Omega}. \tag{4.5}$$

Based on the result gained in (4.5), $R_1 = 82\,\mathrm{k\Omega}$ was chosen due to availability of precision resistors with this properties. The requirements for the operational amplifier can be summarized as follow:

- High current drive ability.
- High gain-bandwidth-product.
- High slew rate.
- Low output resistance.

The THS4631 operational amplifier satisfies this prerequisites. It has a high slew rate of $S = 1\,\mathrm{kV/\mu s}$, a considerably high gain bandwidth product of $GBP = 210\,\mathrm{MHz}$ and a high current driving ability of $I_{OUT} = 95\,\mathrm{mA}$.

The offset-voltages are calibrated using test measurements to assure the correct output bias-voltage levels.

4.3.2 Synchronization of Excitation and Measurement-Cycles

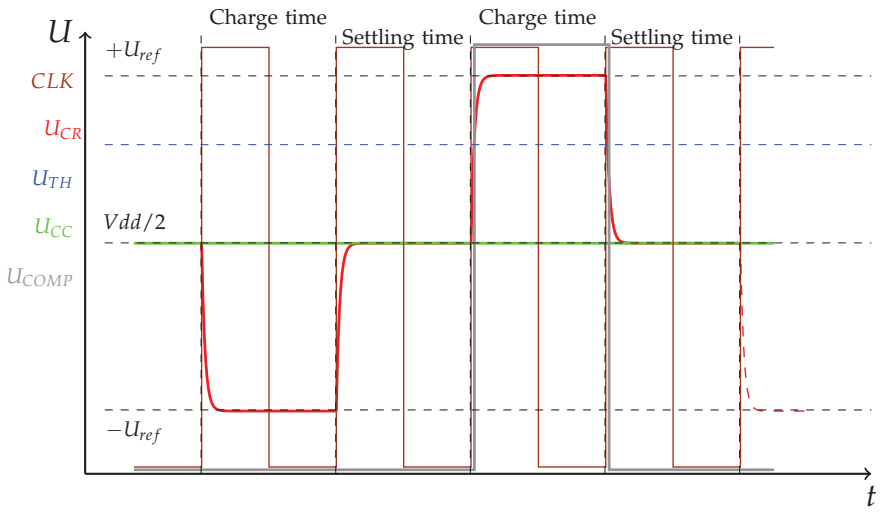

Figure 4.6. Signal graph for the differential charge measurement system with external excitation and external clock-signal used for trigger synchronization.

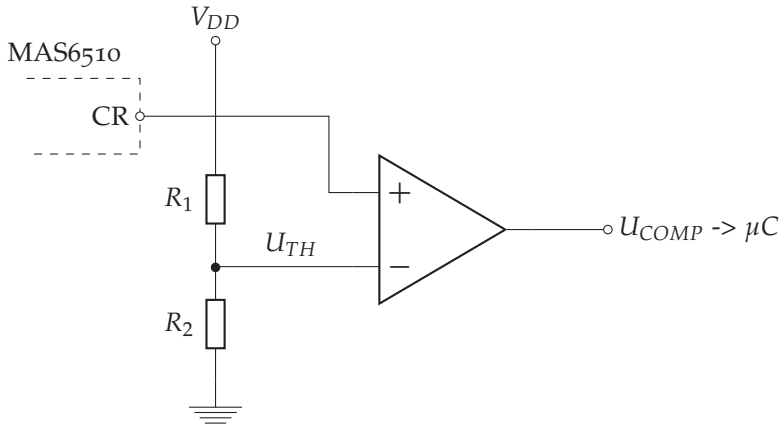

Figure 4.7. Depiction of the circuit for detecting the correct measurement cycle of the CDC-chip and providing a trigger signal for the micro controller.

When using an external clock, the CDC-chip provides an internal synchronization routine itself to synchronize with the external clock-signal. This phase is used by the micro controller to detect the correct measurement cycle to synchronize the excitation signal to the measurement cycle. Due to the three voltage levels of the excitation signal, a threshold sensor is required to detect the positive charging phase. The signal graph is depicted in figure 4.6 and the corresponding circuit in figure 4.7. For this purpose a preselected

comparator acts as threshold sensor of the internal excitation signal provided on the pin CR of the MAS6510.
In the internal synchronization phase, it is aimed to detect the positive charging phase of the measurement cycle, when U_{CR} reaches its positive charging phase. The rising edge of the comparator circuit is used to trigger an interrupt in the micro processor program to enable the DA-converter. The threshold voltage is set to $U_{TH} = 2\,\mathrm{V}$, to suppress false positive trigger events. The resistors are selected to $R_1 = 12\,\mathrm{k\Omega}$ and $R_2 = 20\,\mathrm{k\Omega}$ accordingly. A TLV3501 is used for the comparator providing an ultra-fast response time of 4.5 ns and common mode tolerance up to V_{DD}. Furthermore, an operational voltage in single supply of $V_{DD} = 2.7\,\mathrm{V}$ to $5.5\,\mathrm{V}$ is provided with a rail-to-rail CMOS-push-pull-output, directly providing digital compatible signals.

4.3.3 Parallel Communication

In order to perform fully parallel measurement, the measurements need to be started at the same time. For the selected CDC MAS6510, the measurement is started when a specific register is set via the I^2C-Bus or SPI-Bus. This option does not require a full-duplex communication with multiple devices, but has the necessity to send one command from one master device, the microprocessor, to all CDC-chips. The transmission of the data in the opposite way can be performed sequentially.
Considering the I^2C-Bus, the communication is performed over a 2-wire interface, consisting of a clock-line and a data-line. Communication is performed in half-duplex mode. Due to this, only one device on the bus can send data at a time. The selection of a chip is accomplished by sending the individual device address and subsequently the actual data. In general this bus does not support multiple receivers on the line, due to conflicts in the device-addresses. In the case of the MAS6510 chips, they feature two addresses for the I^2C-Bus, a hardware programmed static address for all chips and a software programmable address is saved in the internal EEPROM. As a consequence each of the chips would have to be configured with a unique device address prior to application in the measurement system or a considerable amount of circuitry implemented additionally.
The supported SPI-Bus would allow a full-duplex communication interface with two data

lines, one for each direction. On the other hand, an external signal needs to be applied to the Chip-Selection-Pin (CS), to signal the device to start receiving or transmitting. This is also denoted as a serial-4-wire interface, compared to the previous as 2-wire-interface. However, the CS-pins allow to individually select one, or multiple devices to receive when selected. As it is required in this approach, the result is that all devices are selected, receive the same data at the same time and start the measurement at the same time.
Therefore, the SPI-Bus is selected, using multiple CS-Lines with the drawback of one additional wire for every additional device. A general reset-line connects all devices to provide a defined initial status of all devices.
For additional experiments using the external clock source for all CDCs, three possible generators are provided, two of these on the prototype board. Firstly, an external clock generator can be connected via SMA-connectors. Secondly, a highly stable, crystal oscillator with digital buffered output of 1 MHz. Lastly, one of the CDCs can provide its internal oscillator clock for the remaining devices. In this configuration, an additional buffer amplifier is used to assure that the load of the internal oscillator is kept low.

4.4 Measurement Hardware for Time Interleaved Charge-based Capacitive Measurements

In the previous parts of this chapter, techniques for the parallel operation of the MAS6510 have been suggested. A parallel measurement mode is an effective way to increase the measurement rate, when measuring multiple capacitances. For achieving an increased measurement rate for an individual capacitance, so called time interleaved measurements can be conducted.
The idea of time interleaved measurement is to increase the overall temporal resolution of one capacitance by the temporally delayed measurements using individual measurement circuits. In detail, after a specifiable delay, but shorter than one measurement cycle, another measurement is started. This would allow to reduce the time between samples resulting in an improved temporal resolution.
Due to the principle of the MAS6510, additional circuitry is required to perform this

operation. To enable to measure one capacitance with multiple MAS6510, the charges that are transfered, have to be delivered to each IC. In order to do this, the discharge currents during each measurement phase are amplified and each MAS6510 is provided with the same amount of charge. In order an additional circuit is required. Figure 4.8 presents the suggested setup. This is an extension of the previously discussed circuit.
To realize the current amplification, a biased current multiplier circuit was designed, as displayed in figure 4.9. It consists of a biased charge amplifier with N outputs, providing a current with the same magnitude, but opposite phase at each output.

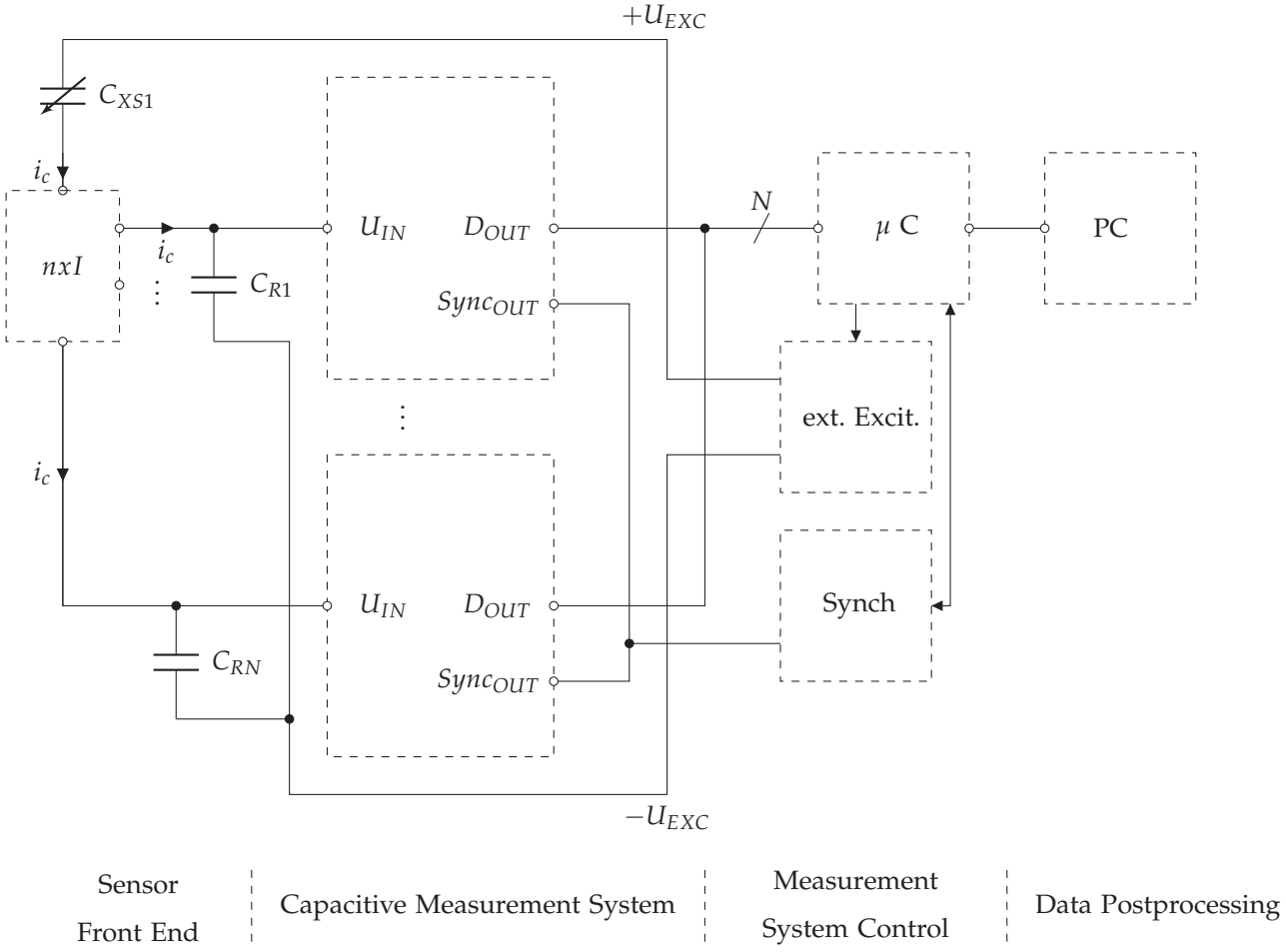

Figure 4.8. Schematic block diagram of the proposed time interleaved charge-based capacitive measurement system consisting of a sensor front end, N capacitance measurement devices, a micro controller for the control of the system and a PC for data post processing.

The resistors at the positive input of the amplifier set the bias voltage of the output voltage. In order to be connected to the MAS6510, the bias voltage is set to the bias voltage of the

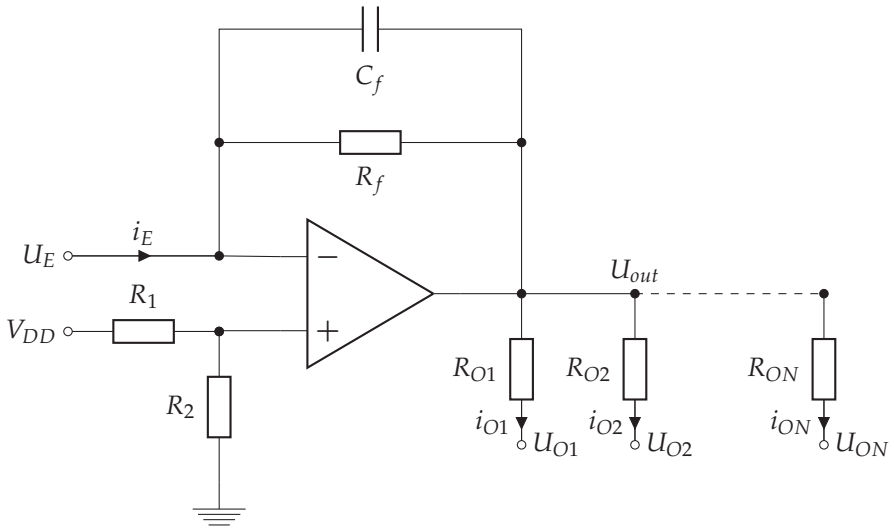

Figure 4.9. Circuit of a N-time current amplifier.

MAS6510. The resistors are set to $R_1 = R_2 = 20\,\mathrm{k\Omega}$ to provide $V_{DD}/2$. The output voltage U_{out} is calculated as:

$$U_{out} = \frac{V_{DD}}{2} - R_f \cdot i_E, \tag{4.6}$$

and gives for each output current:

$$i_{Oi} = \frac{U_{Out} - U_{Oi}}{R_{Oi}}. \tag{4.7}$$

With the output voltage $U_{Oi} = \frac{V_{DD}}{2}$, this simplifies to:

$$i_{Oi} = -\frac{R_f}{R_{Oi}} \cdot i_E. \tag{4.8}$$

In order to replicate the individual currents precisely, the resistors are selected $R_f = R_{O1} = \cdots = R_{ON} = 100\,\mathrm{k\Omega} \pm 0.01\,\%$. For stable operation, this circuit requires a feedback capacitance. Without the feedback capacitance, the circuit oscillates at the frequency set by the feedback resistor and the stray capacitances. For the calculation of the stray capacitance, the circuit is operated initially without feedback capacitor. The oscillating frequency is determined as $f_{osc} = 80\,\mathrm{MHz}$. Then C_S can be computed by:

$$C_S = \frac{1}{2\pi R_F f_{osc}} = 19.9\,\mathrm{fF}, \tag{4.9}$$

With the results determined for C_S in (4.9), the minimal feedback capacitance is calculated:

$$C_F \geq \frac{1 + \sqrt{1 + 4C_S \pi R_F GBP}}{2\pi R_F GBP} \geq 15.15\,\mathrm{fF}, \tag{4.10}$$

with GBP being the Gain-Bandwidth-Product of the operational amplifier. Equation (4.10) is provided in the manual of THS4631 [28]. The resulting feedback capacitance using the cut-off frequency can be calculated as:

$$C_F = \frac{GBP}{f_c^2 2\pi R_F} - C_S \tag{4.11}$$

The cut-off frequency is chosen to $f_c = 10\,\text{MHz}$, which results in $C_f \cong 2.7\,\text{pF}$ using (4.11). The feedback capacitance was set to $C_F = 3.3\,\text{pF}$, due to availability of proper capacitors.

The manufactured prototype board with all circuits discussed in this chapter, is presented in figure 4.10. It consists of the hardware selectable oscillator circuit block, two DC-amplifiers for the excitation signals provided by the microprocessor, one synchronization circuit, five CDC sensors connected via SPI-Bus, the current-multiplicative circuit and the power supply.

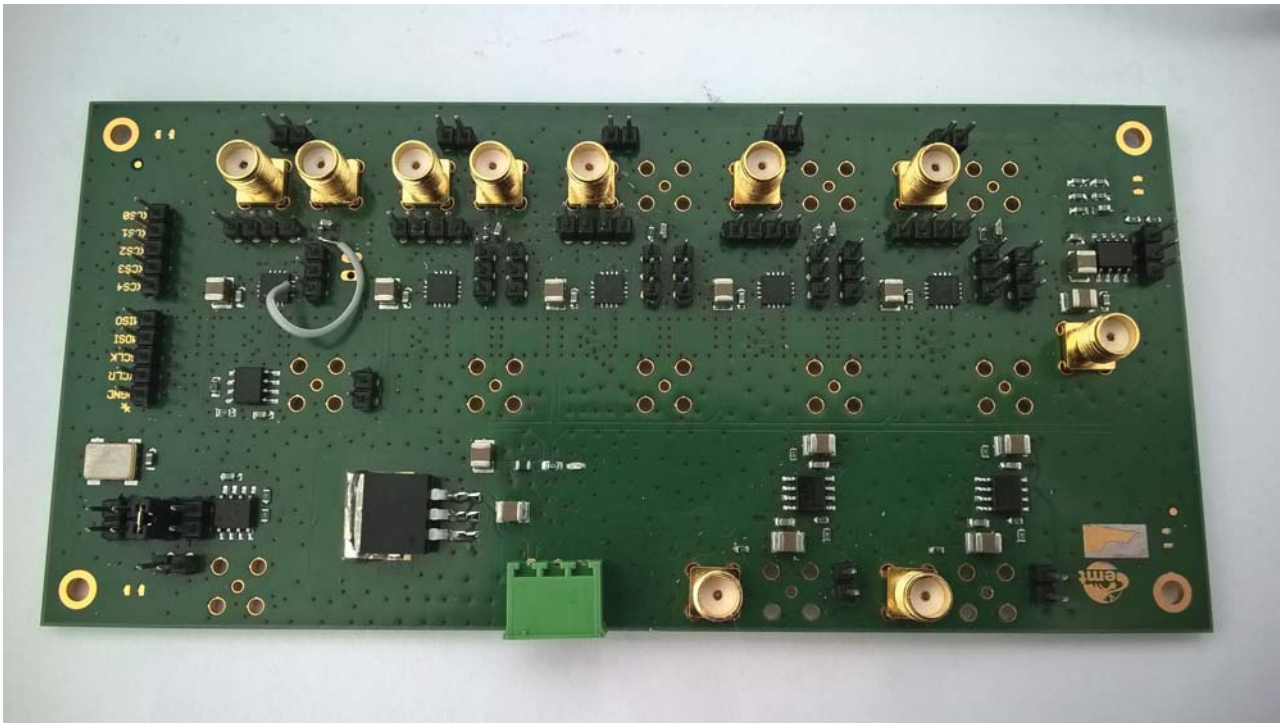

Figure 4.10. Picture of the manufactured prototype board with all the circuit components described before.

5 Measurement Results

In order to verify and characterize the proposed circuits, a number of measurements are conducted and presented in this chapter. Those are used to quantify the circuit to aspects as:

- Resolution regarding excitation voltage.
- Resolution regarding difference of capacitances.
- Linearity regarding excitation voltage.
- Linearity regarding difference of capacitances.
- Noise of each measurement channel.
- Temporal resolution of the interleaved circuit.
- Outliers of each channel.

The MAS6510 does not provide the capacitance values to be measured directly, but provides a ratiometric evaluation given by [21]:

$$Q_{AVE} = \frac{1}{2} + \frac{C_S - C_R}{C_{REF}} \frac{U_S}{2U_R}. \tag{5.1}$$

In (5.1), C_S and C_R are the external connected capacitances and C_{REF} the internal reference capacitance. U_{S} is the amplitude of the excitation signal and U_{R} the internal reference voltage for the ADC. The internal reference values are $C_{\mathrm{REF}} = 6\,\mathrm{pF} \pm 10\,\%$ and $U_{\mathrm{R}} = 264\,\mathrm{mV}$. In order to compare the measured results with the expected results, the ratios determined by the MAS6510 are presented throughout this chapter.
In the following, each channel is characterized individually in the parallel and the time interleaved measurement setup.

5.1 Characterization of the Parallel Measurement System

5.1.1 Analysis of the Results of the performed Measurements

In this chapter the results acquired with the MAS6510 in the parallel setup are analyzed. The test capacitances used in the setup, the reference capacitances soldered on the board and the measured signal are determined.
In order to fully characterize the developed measurement system, test measurements with different test capacitances are performed. Each test capacitance is determined with a precision LCR-measurement-bridge. Since a capacitive difference is measured, a test capacitance is soldered on the prototype board and measured accordingly. The measurement setup is presented in figure 5.1.

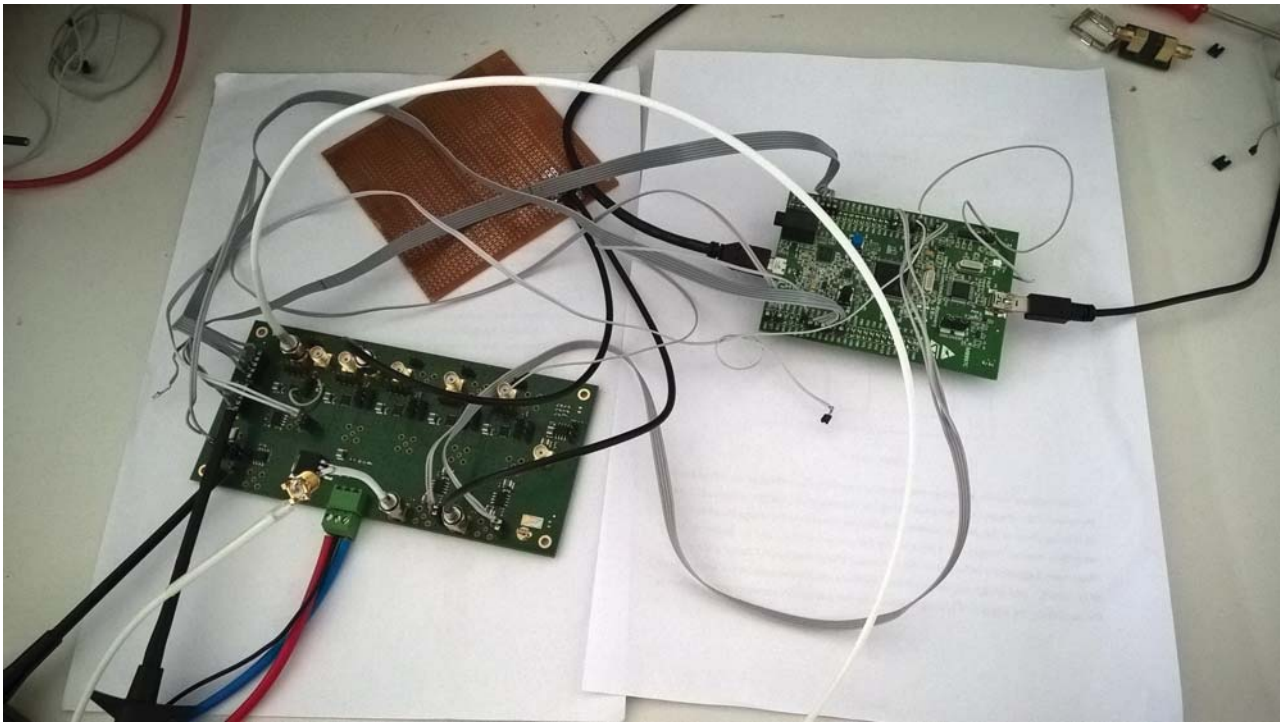

Figure 5.1. Picture of the parallel measurement setup, with channel 4 under test and the micro controller-board, respectively.

The testing of the excitation voltage is performed by means of test measurements with selected excitation voltages. In order to determine the range of measurement, the amplitude of the excitation source is increased from 0 V to the maximum applicable voltage to remain in the measurement range of the MAS6510. Therefore, for each measurement channel each

test capacitance is connected in turns and one measurement conducted for each amplitude of the excitation source in range. In total, seven different test capacitances are tested with a corresponding number of excitation voltages for each channel in parallel measurement mode.

For the specification of the measurement noise, 1500 subsequent measurements are conducted of each channel with all available settings of excitation voltage and test capacitances. The noise is calculated, after accounting for measurement outliers.

Prior to the measurements, the soldered reference capacitances for each channel were measured, using a HAMEG HM8118 LCR-Bridge (HAMEG Instrumentation, Mainhausen, Germany). The results are shown in table 5.1:

Table 5.1. Table with the measured reference capacitances of each measurement channel

Reference capacitance	Value
C_{R0}	23.82 pF
C_{R1}	23.60 pF
C_{R2}	23.45 pF
C_{R3}	24.38 pF
C_{R4}	27.52 pF

It is already observable from table 5.1, that channel 4 clearly has a larger reference capacitance than the other channels. The effect of this should be observable in the following diagrams for characterization of the parallel measurement system. The test capacitances used are noted in table 5.2. In a first test, a test capacitance from table 5.2, an excitation amplitude and a channel to be measured are selected. Exemplary the test capacitance is selected with $C_{\text{Test}} = C_{\text{T3}} = 17.91\,\text{pF}$ and the excitation amplitude with $U_{\text{exc}} = 67.4\,\text{mV}$. Channel 3 is selected as channel under test. The results gained for this configuration are presented in figure 5.2. The sequence of measurements show a proper result for the selected measurement setup. Unfortunately, outliers are observable as well. It is suspected that the synchronization fails in cases of outliers. Investigating this assumption, a short series of measurements were conducted and the signal graphs of excitation cycle and measurement cycle compared using an oscilloscope. The result confirms the assumption, that a miss in

Table 5.2. Table with the measured test capacitances for each measurement.

Test capacitance	Value
C_{T1}	7.46 pF
C_{T2}	12.32 pF
C_{T3}	17.91 pF
C_{T4}	22.55 pF
C_{T5}	26.45 pF
C_{T6}	34.29 pF
C_{T7}	48.76 pF

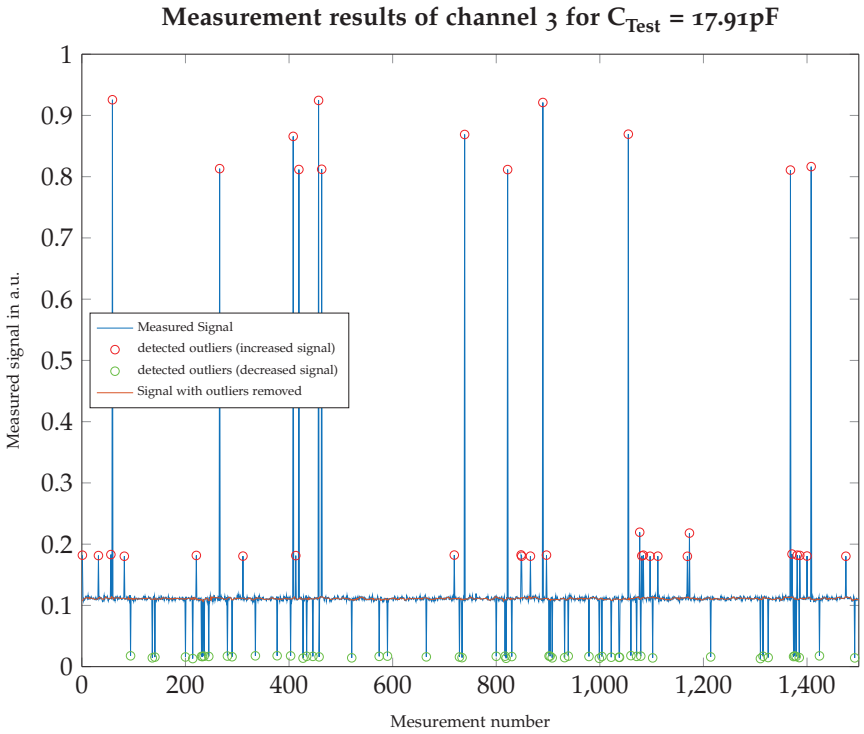

Figure 5.2. Measurement example of channel 3 with a test capacitance of 17.91 pF and $U_{exc} = 67.4\,mV$. With the measured points in blue, the detected outliers in red and green circles and the signal with outliers removed in brown.

synchronization results in this outliers. Two reasons are assumed to introduce the miss synchronization observed:

- Interrupt handling time jitter [29].
- Change in the measurement cycle of the MAS6510, due to internal processes.

The low incidence of the outliers allow to remove them by means of filtering. Hence, a median-filter of 7^{th}-order is applied to remove the outliers for the characterization of the measurement system. However, this is no permanent solution to the problem of outliers and the sources of the outliers have to be determined and accounted for specifically.

5.1.2 Comparison of individual Measurement Channels

In this section, the results are compared to verify the expected linear behavior stated in (5.1). In order, the results are presented for various excitation voltage applied and different capacitive differences used. The capacitive difference is determined by the test capacitance and the reference capacitance, $\Delta C = C_T - C_R$. The results presented are the calculated mean value of the filtered results and the corresponding confidence interval of $\pm\sigma$.

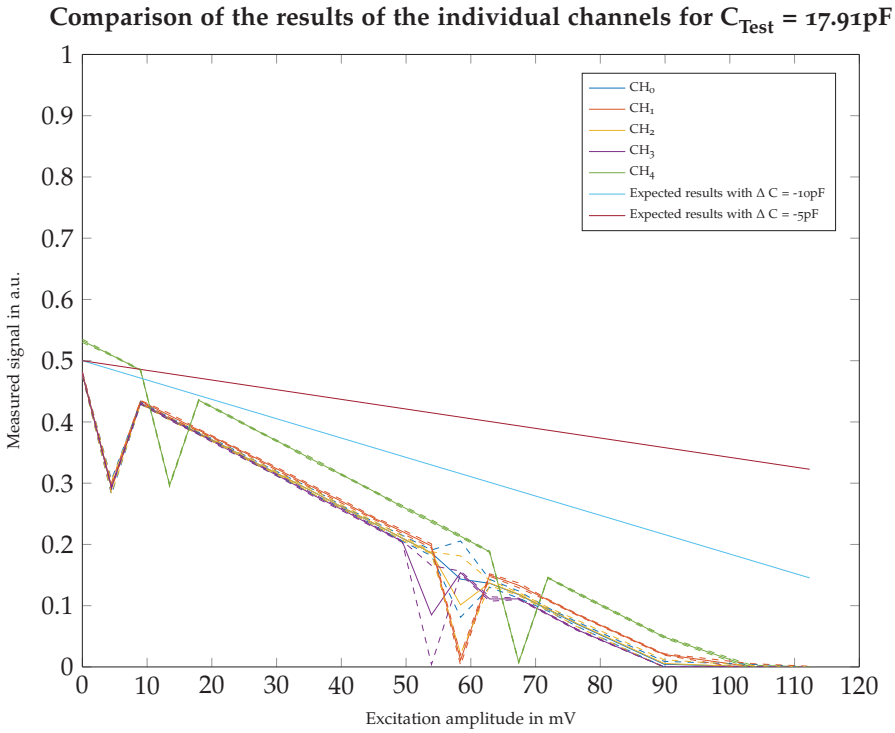

Figure 5.3. Comparison of the results of all five measurement channels for a test capacitance of 17.91 pF and a reference capacitance of ~ 24 pF.

In figure 5.3 one exemplary result for all five channels is presented. The test capacitance used in figure 5.3 is $C_{T3} = 17.91\,\text{pF} < C_{REF} \sim 24\,\text{pF}$. The solid lines show the calculated mean value of the 1500 subsequent measurements and dashed lines the σ-neighborhood

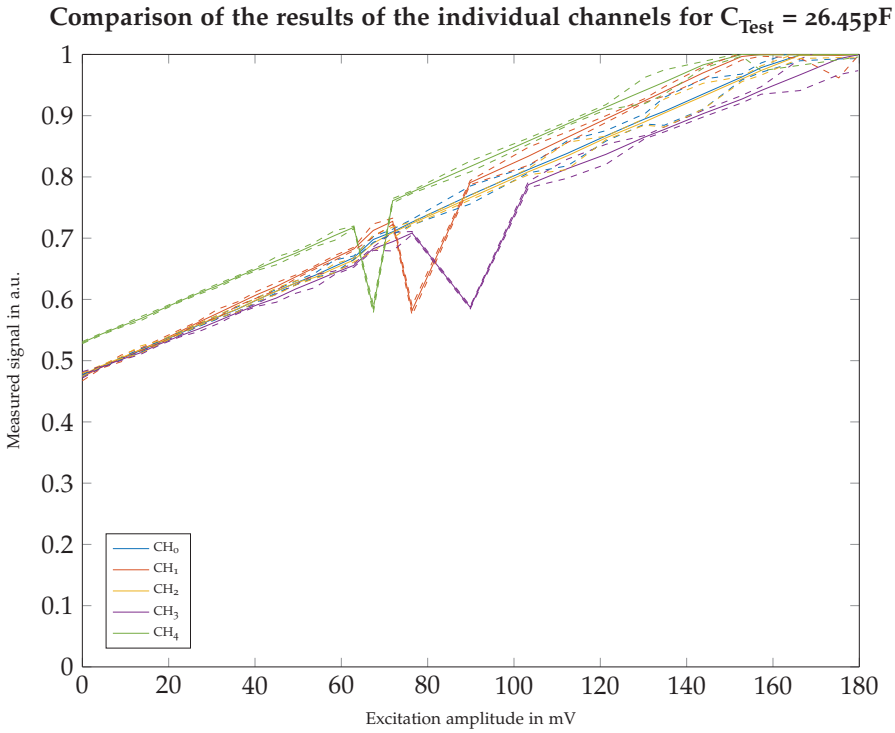

Figure 5.4. Comparison of the results of all five measurement channels for a test capacitance of 26.45 pF and a reference capacitance of $\sim 24\,\text{pF}$.

of the mean value. In addition, the expected results by (5.1) for a capacitive difference of $\Delta C = -5\,\text{pF}$ and $\Delta C = -10\,\text{pF}$ are displayed. It is observable, that the expected result of a decreasing output signal with increasing excitation amplitude is acquired. However, two differences are observable:

- The measured results decrease faster than expected.
- Channel 4 in green starts above 0.5, which is expected to occur for positive differences only.

Figure 5.4 depicts the results gained for the test capacitance $C_{T5} = 26.45\,\text{pF} > C_{REF} \sim 24\,\text{pF}$. The results show again the expected trend, an increase in the relative output with increasing excitation amplitude when a positive capacitive difference is measured. For channel 4 the capacitive difference is negative and a decreasing trend expected. However, a positive trend was acquired. Hence it has to assumed, that the measured value of the reference capacitance is not correct.

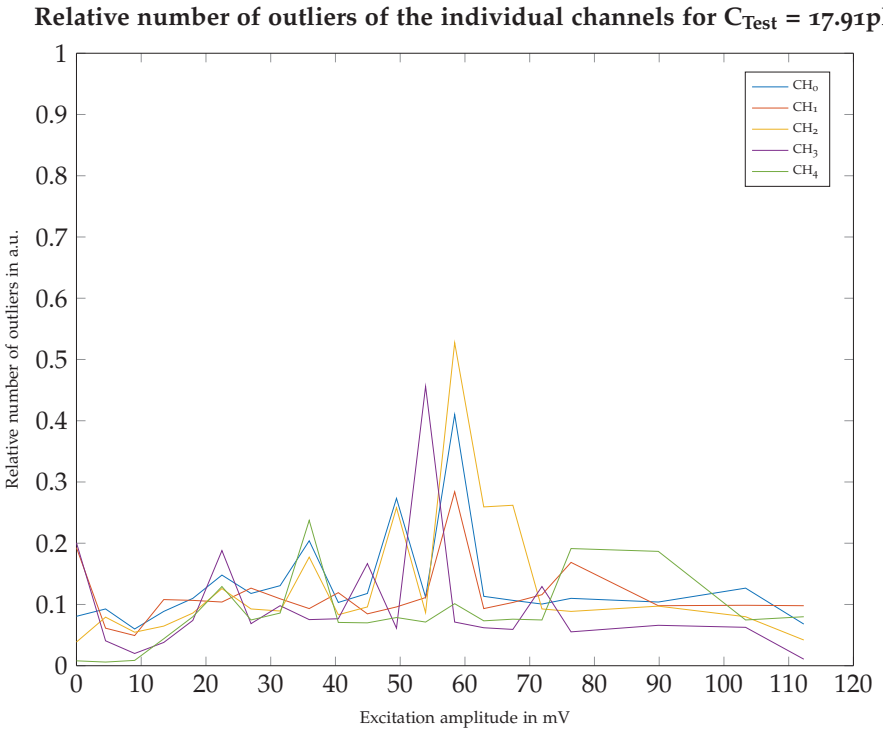

Figure 5.5. Depiction of the relative number of outliers of all five measurement channels for a test capacitance of 17.91 pF and a reference capacitance of $\sim$ 24 pF.

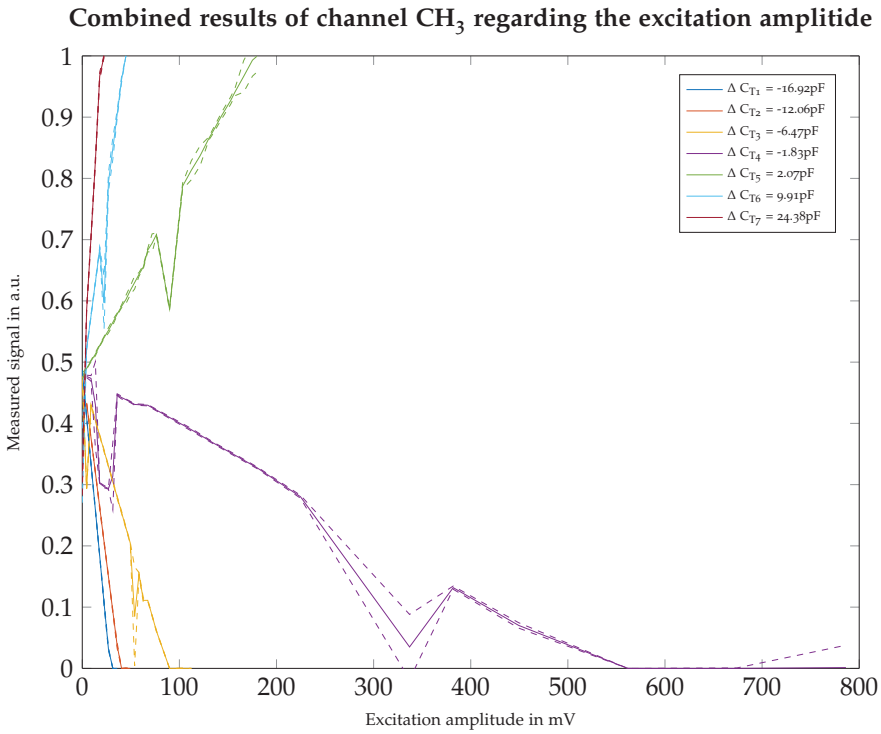

Figure 5.6. Depiction of combined results of all test capacitances measured for channel 3.

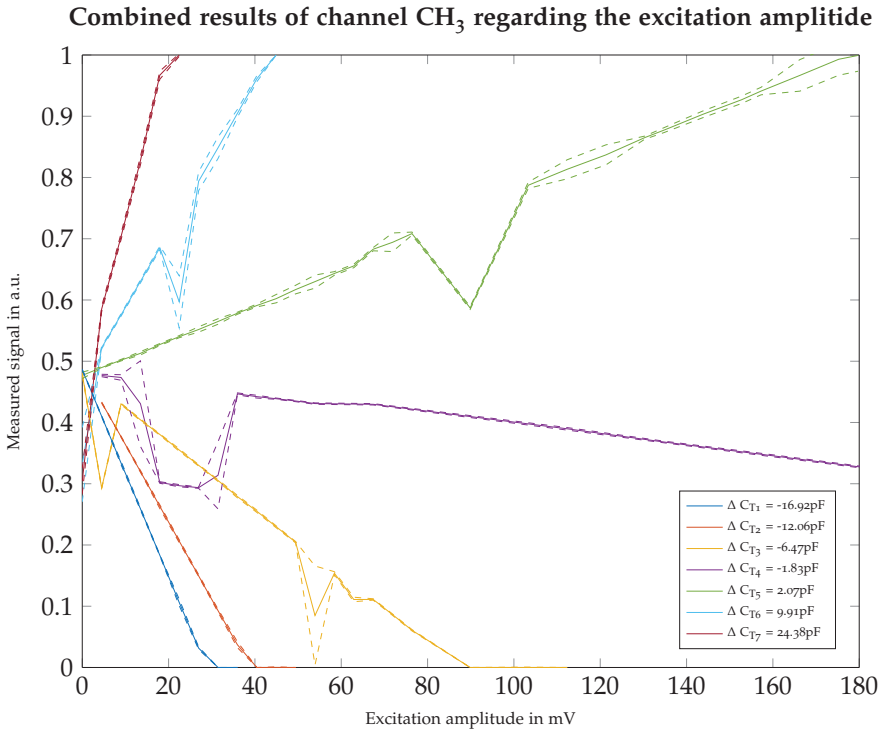

Figure 5.7. Depiction of combined results of all test capacitances measured for channel 3 with the focus is on small voltages.

In both figures discontinuities from the linear trend, in the range of 50 mV to 110 mV, can be observed. It is assumed that the reason for this discontinuity is due to an increased number of outliers that occurred at that specific excitation voltage. Hence, the number of detected outliers for all channels plotted over the excitation voltage is displayed in figure 5.5. The results gained, confirm the assumption that at the discontinuities a higher number of outliers occurred than regularly, $\sim 45\,\% \gg \sim 12\,\%$. With this high number of outliers, the median-filter is not capable of calculating a valid result.

An overview of all performed measurements for channel 3 are presented in the figures 5.6 and 5.7. In these figures all measured capacitive differences applied are presented. Figure 5.7 displays the results gained for excitation voltages < 180 mV in more detail. It can be observed, that the results measured confirm the linear relation between excitation voltage and measured result for all test cases for channel 3. Furthermore, it can be confirmed, that the sign of the difference of capacitances measured, determine the direction of the change of results for a given excitation voltage. In figure 5.7, a susceptibility to errors can be observed,

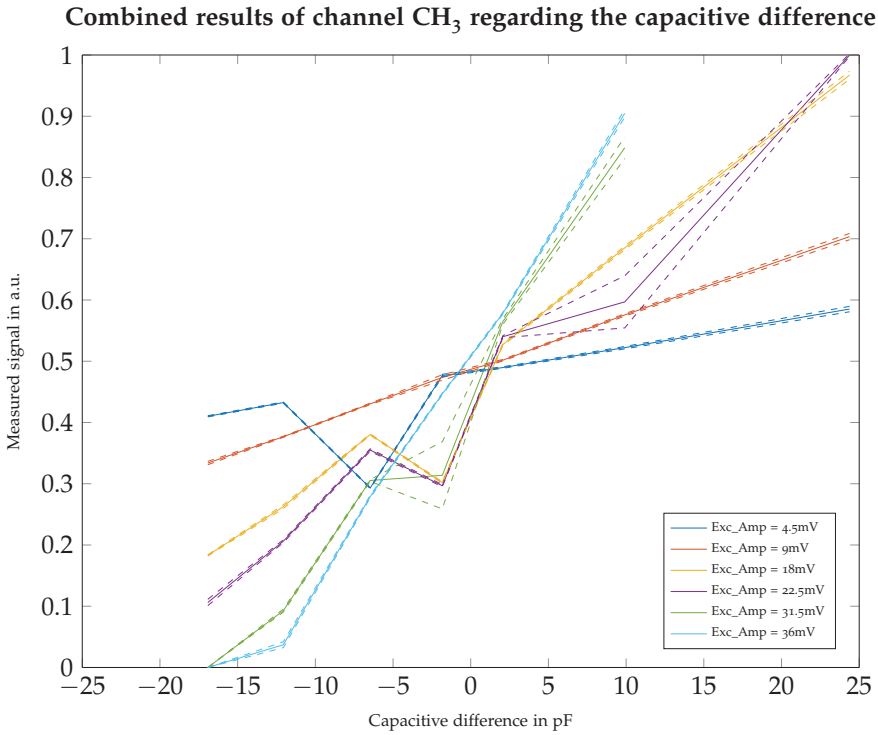

Figure 5.8. Depiction of combined results of selected excitation amplitudes for all capacitive differences measured with channel 3.

when small excitation voltages are provided with $U_{\mathrm{EXC}} < 40\,\mathrm{mV}$.

In figure 5.8 a clear linear relation between the capacitive difference and the conversion result is observable. However, a susceptibility to errors can be observed for small capacitive differences. As a measure of quality the SNR is estimated as follow:

$$SNR = 20log_{10}\left(\frac{\mu}{\sigma}\right). \tag{5.2}$$

The Signal-to-Noise-Ratio is approximated using (5.2) of the results given, presented in figure 5.9. The observed SNR with $\sim 40\,\mathrm{dB}$ is rather poor compared to the expected SNR of $\sim 92\,\mathrm{dB}$. The poor SNR can be explained by the very small excitation voltages used in this test. It is expected, that with the use of higher excitation voltages the SNR improves considerably.

Concluding, the results confirm, that there exists a linear relation between the excitation voltage and the conversion results and between the capacitive difference applied and the conversion result. However, it was observed that the small excitation voltages make the system susceptible to errors. Further, the synchronization methods proposed, are not

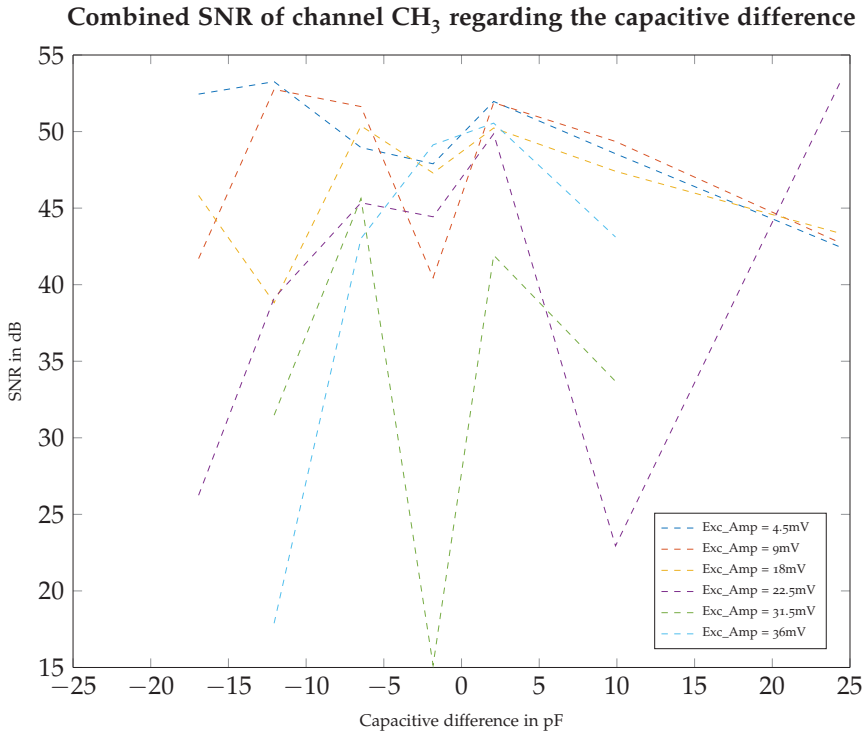

Figure 5.9. Depiction of combined SNR of selected excitation amplitudes for all capacitive differences measured with channel 3.

sufficient enough for stable operation of the parallel measurement system. In addition, the micro processor can not guarantee a fixed time to response to interrupt calls. Therefore, a synchronization circuit is desirable to reduce the number of outliers considerably. In the next section the characterization of the proposed time interleaved measurement system is described.

5.2 Characterization of the Time Interleaved Measurement Circuit

In this section the time interleaved measurement circuit is characterized. The measurement setup is presented in figure 5.10.

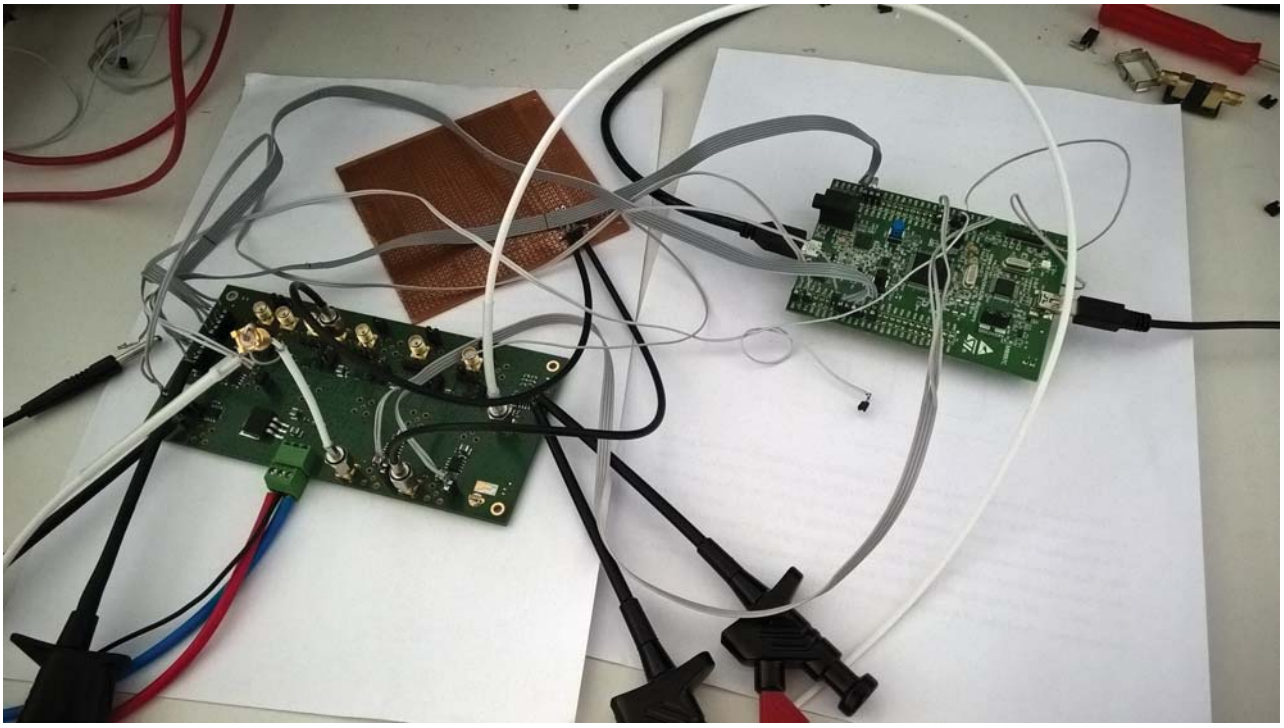

Figure 5.10. Picture of the time interleaved measurement setup, with channel 4 under test, with the micro controller-board all connections respectively.

For the test of this measurement setup, the capacitances determined in section 5.1.1 are used. In this section, all five channels are investigated in time interleaved mode for measuring the same capacitances measured in parallel setup to determine influences in the time interleaved operation mode.

One change has to be made prior to the measurement in time interleaved mode. The current amplification circuit proposed in figure 4.9, introduces an additional phase of $-180°$. In order to compensate for this phase shift, an equal phase shift was introduced to the negative excitation source via software.

The temporal delay between the individual measurement channels is programmed to the micro processor and has an initial delay of three measurement cycles, which is required

for synchronization of the excitations source and the subsequent measurement channels. Thereafter, all remaining channels have the smallest possible delay of one measurement cycle, with one cycle requiring four rising edges of the underlying clock source. With a clock of $f_{\text{clk}} = 200\,\text{kHz}$, the inter-channel-resolution is $t_{\text{int}} = 20\,\mu\text{s}$. Sequential measurements of one capacitance require typically $t_{\text{meas}} = 5.8\,\text{ms}$.
In the following the results for the individual channels are presented. The filter proposed in section 5.1.1 is applied accordingly.

5.2.1 Comparison of the Results for the Measurement of the Individual Channels in Time Interleaved Mode

In this section the individual results of the full time interleaved circuit are presented. The proposed current amplifier with five outputs is investigated. For comparison of the individual channels of the time interleaved system, a single capacitance is measured. All individual results of the different channels are plotted to be compared against each other. The temporal delay between the activation of the individual measurements is set to the minimum of $t_{\text{INT}} = 20\,\mu\text{s}$, or one excitation cycle.

For comparison of the results with the parallel measurement system, the test routines performed for the parallel system, are repeated. In detail, the test capacitances are connected between the excitation source and the proposed current amplification circuit. In order, the displacement current is amplified and provided to the individual CDCs.
The results are expected to have the opposite trend of the parallel measurement system, due to the phase shift introduced in the excitation sources. Furthermore, it is investigated if the actual time interleaved approach gives proper results.
In figure 5.11, the results for the test capacitance $C_{\text{Test}} = 17.91\,\text{pF}$ are displayed. In addition, the expected output values of the MAS6510 for $\Delta C = -5\,\text{pF}$ and $\Delta C = -10\,\text{pF}$ are depicted. Comparing the measured and the predicted results, the linear trend is clearly observable. In figure 5.12 the results for the test capacitance $C_{\text{Test}} = 26.45\,\text{pF}$ are presented. Both graphs show the expected linear behavior regarding the excitation voltage. However, the difference in the progress of the trends differ between measured and predicted output and

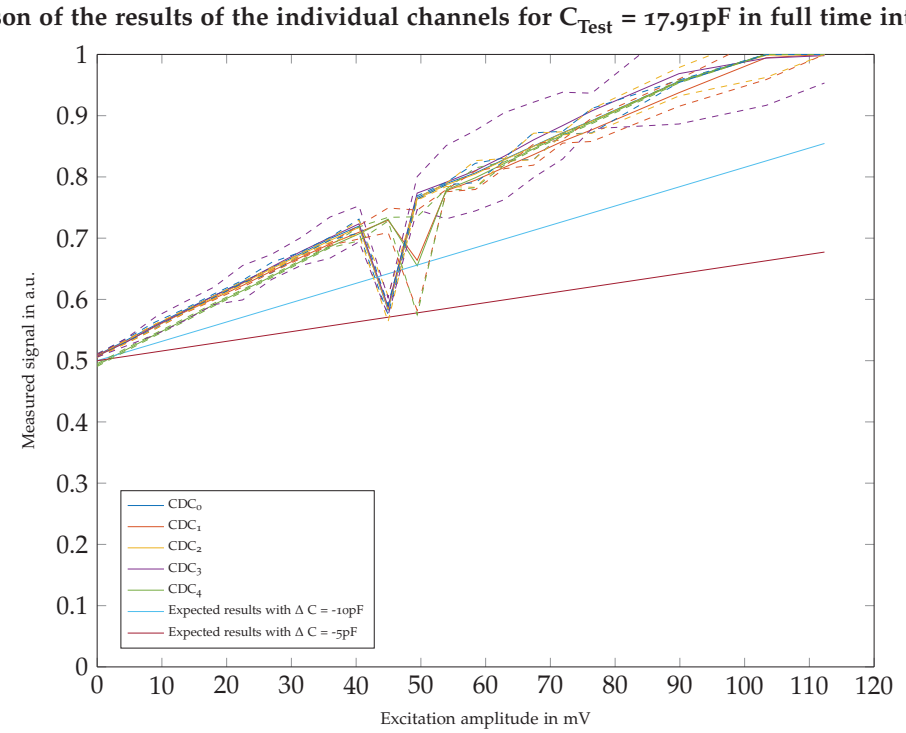

Figure 5.11. Comparison of the results of all five measurement channels for a test capacitance of 17.91 pF and a reference capacitance of $\sim$ 24 pF.

a discontinuity of the linear trend is seen. It is assumed that this issues are similar to these noted in the previous chapter for the parallel measurement system. In addition it can be observed, that the confidence interval σ of channel 3 is considerably elevated. Those of the remaining channels are only marginally increased. With respect to the results for the parallel measurement system, the trends for the time interleaved, show the same linear trend for increased excitation amplitude.

Figure 5.13 depicts the number of outliers occurred in the measurements. The discontinuities of the linear trend in time interleaved mode are introduced by an elevated number of outliers, as presented in the previous chapter for the parallel measurement system.

In figures 5.14 and 5.15 the results of channel 3 for individual measurement are displayed. The linear trend regarding the capacitive difference connected is prominent. However, it can be observed, that for higher excitation amplitudes the noise increases and the observed mean does not occur to be stable, in comparison to the results of the parallel setup in figures 5.6 and 5.7. It is assumed, that the amplifiers are operating at their limits, when high excitation amplitudes are set. Further, for increasing excitation amplitudes the noise

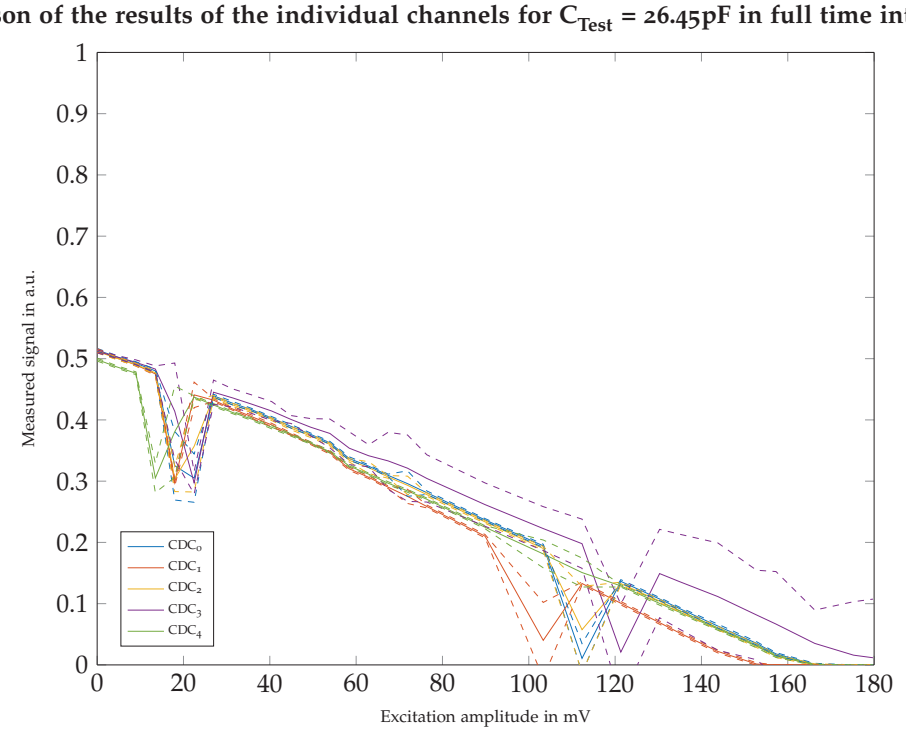

Figure 5.12. Comparison of the results of all five measurement channels for a test capacitance of 26.45 pF and a reference capacitance of $\sim$ 24 pF.

increases indicated by the elevated σ-interval and the unsteady progress of the mean. The results presented in figure 5.16 display the linear trend expected regarding the capacitive difference connected. Clearly observable are the enlarged confidence-intervals. These elevated confidence intervals end up in a considerably reduced estimation for the SNR. The reduced SNR can be observed in figure 5.17. When reviewing figures 5.11 and 5.12 it can be seen, that channel 3 has the highest confidence intervals of all 5 channels measured in this section. This may indicate a problem of this CDC in the time interleaved operating mode. Concluding it can be stated that the time interleaved approach can be applied to further improve the measurement rate of a single capacitance using a multi-channel capacitance measurement system. The SNR indicates for the application shown, that the system yields proper results.

Relative number of outliers of the individual channels for C_{Test} = 17.91pF in full time interleaved mode

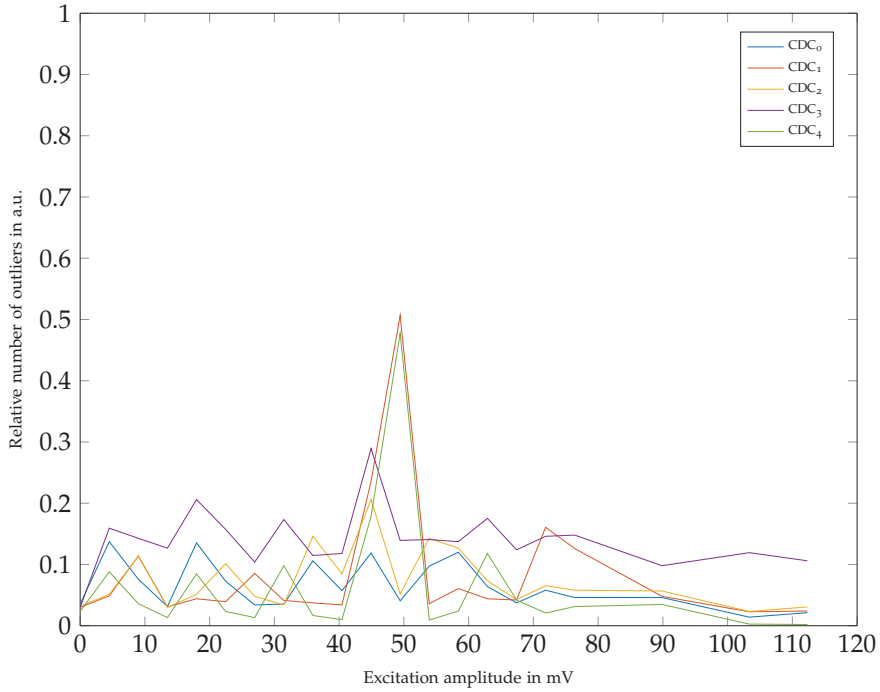

Figure 5.13. Depiction of relative jitter events of all five measurement channels for a test capacitance of 17.91 pF and a reference capacitance of $\sim$ 24 pF.

Combined results of channel CDC_3 regarding the excitation amplitide in full time interleaved mode

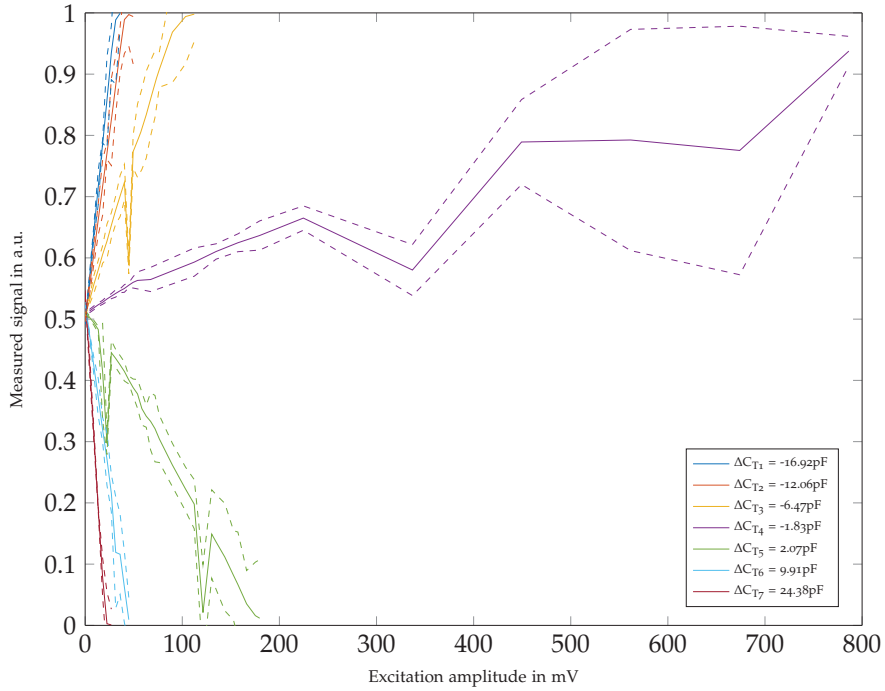

Figure 5.14. Depiction of combined results of all test capacitances measured for channel 3.

Combined results of channel CDC_3 regarding the excitation amplitide in full time interleaved mode

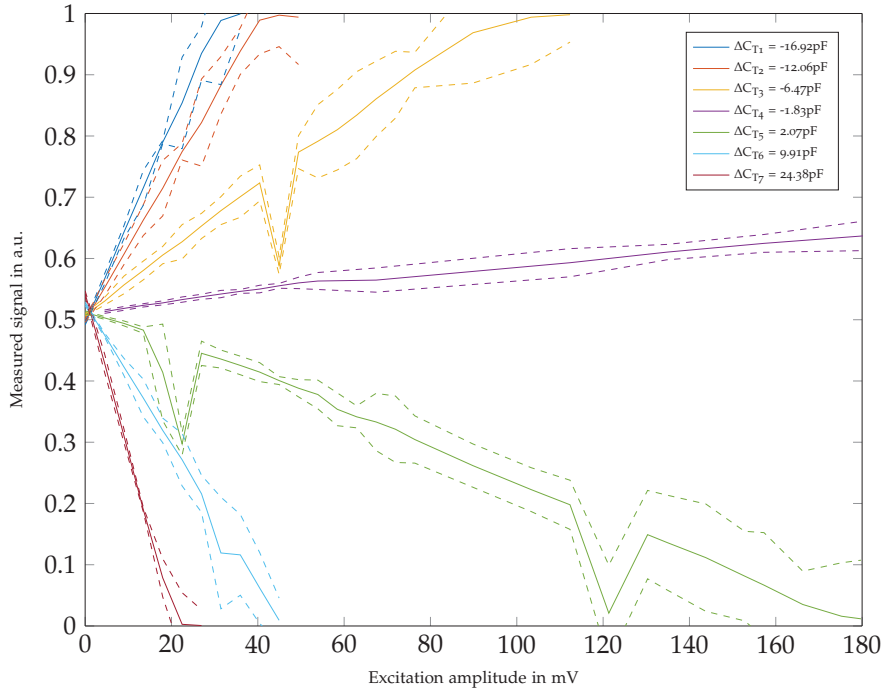

Figure 5.15. Depiction of combined results of all test capacitances measured for channel 3. The focus is on small voltages.

Combined results of channel CDC_3 regarding the capacitive difference in full time interleaved mode

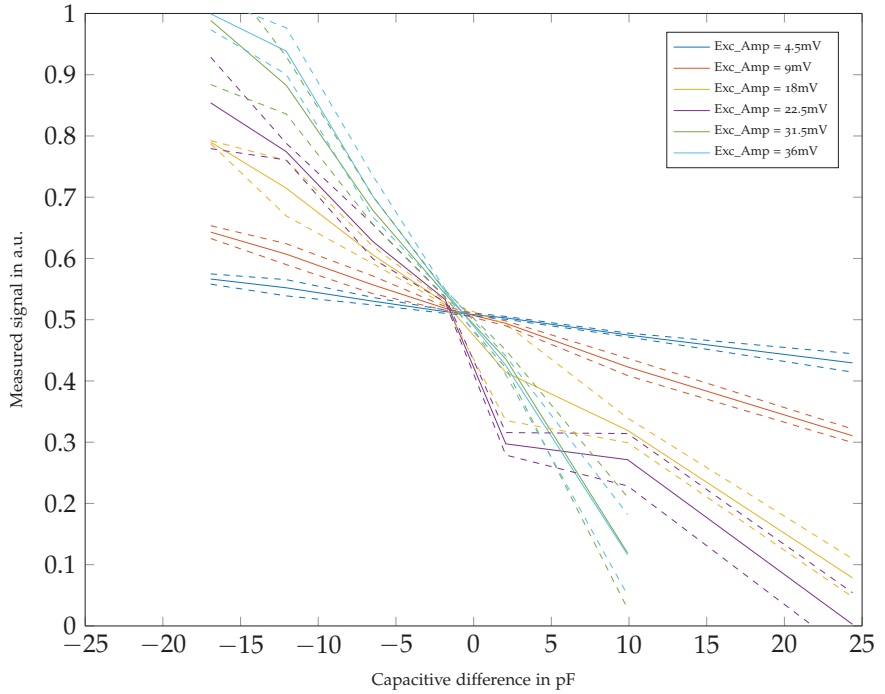

Figure 5.16. Depiction of combined results of selected excitation amplitudes for all capacitive differences measured with channel 3.

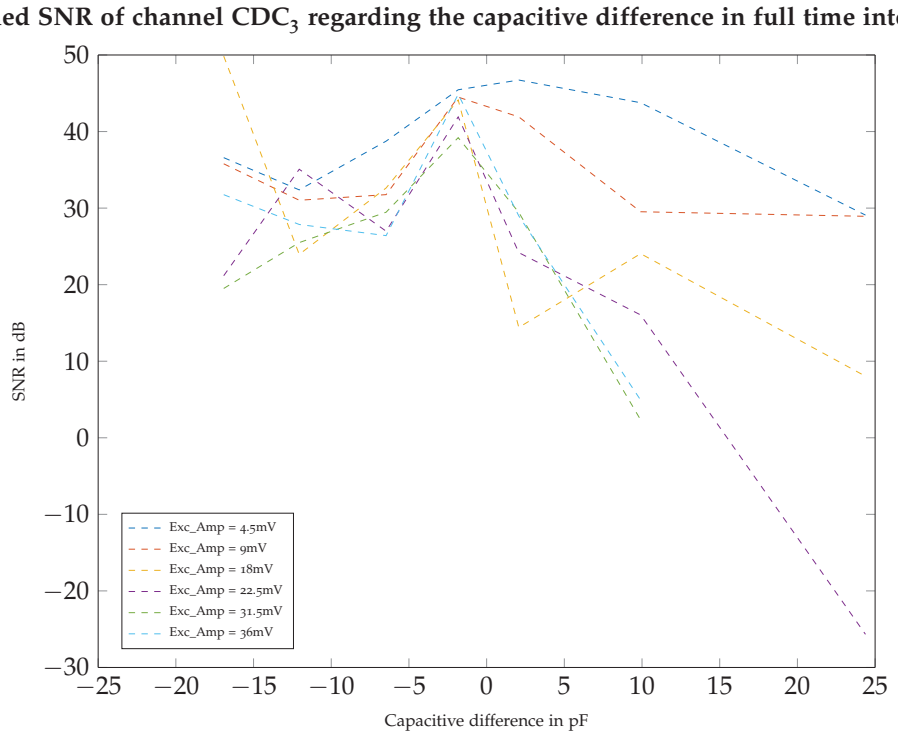

Figure 5.17. Depiction of combined SNR of selected excitation amplitudes for all capacitive differences measured with channel 3.

5.3 Test on an Example ECT-System

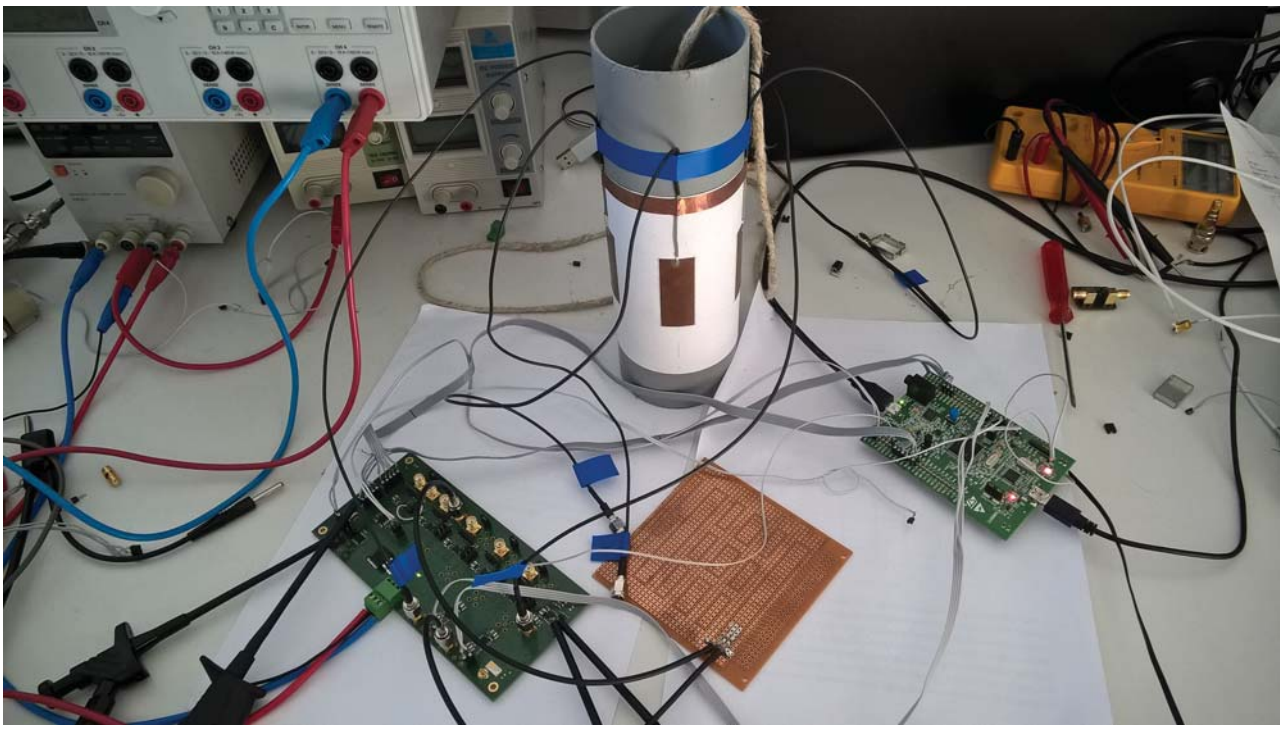

Figure 5.18. Measurement setup of the ECT-test pipe with an array of five sensor electrodes with electrode 5 as excitation/sender and the remaining four as receiver.

In addition to the characterization of the measurement system, a test measurement of both circuits on an actual ECT-test system is performed. It consists of four sensing capacitances, which are provided by five copper strips surface mounted on a Poly-Ethlyene pipe with 75 mm inner diameter and a wall thickness of 2 mm. The cross section of the pipe with the mounted sensor electrodes and the connecting cables to the prototype board, is depicted in figure 5.18.

For this measurement setup only four of the five implemented measurement circuits are required for the measurement of the five electrode ECT-array, due to the fact that one electrode is connected to the common external excitation source. The reference capacitances C_{R1} to C_{R4} have to be replaced due to the reduced capacitances that are expected. The capacitances are equally set to the lowest discrete available capacitance of $C_{R1} = C_{R2} = C_{R3} = C_{R4} = 0.47\,\text{pF}$ and the amplitude of U_{exc} is maximized regarding the sensor output to 2.5 V.

Mesurement results of one cycle of rising and lowering the PE-cylinder in the ECT-tube in parallel setup

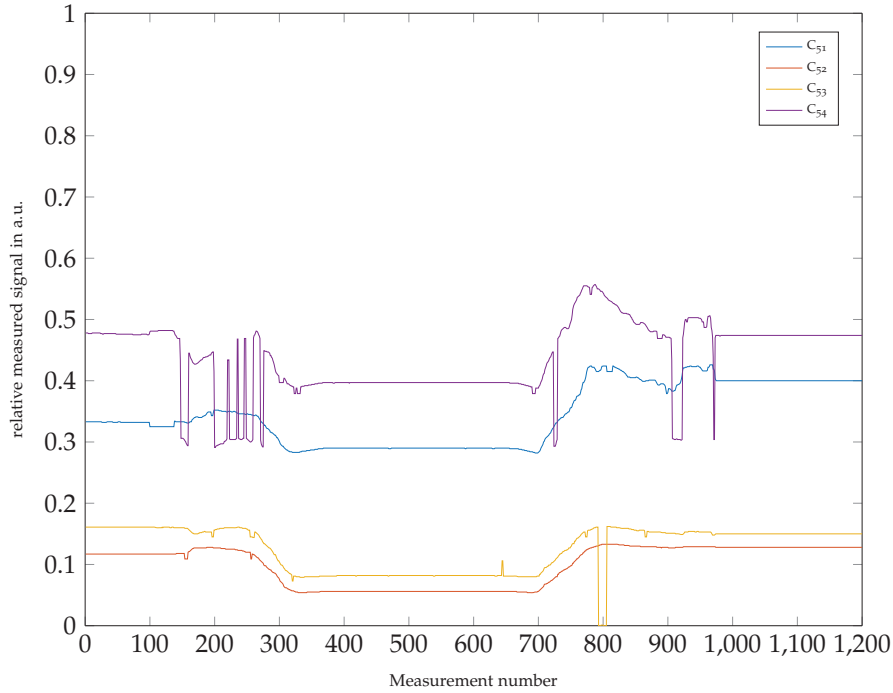

Figure 5.19. Signal graphs of all 4 capacitances of an 5 electrode ECT measured using the full parallel measurement.

For the experiment are in total 1200 points sequentially acquired and the median filter is applied, as proposed in section 5.1.1. During the experiment a cylinder of polyethylene is lowered into the tube and risen back up again by hand. The cylinder has an outer diameter of 4.5 cm and fills the tube almost entirely. The filtered result for the parallel measurement setup is shown in figures 5.19. The result of the time interleaved measurement is presented in figure 5.20. Both figures show proper sensitivity to the rather small changes of the capacitance in the ECT-system. For the test of the parallel measurement system, it is clearly observable that the setup starts with the PE-cylinder inside the tube with an elevated output result. When the cylinder is pulled outside of the tube the capacitance decreases. In order the capacitive difference increases and the output decreases. The signal graphs run in parallel during the trial. At the end, when the cylinder is lowered back in to the tube the output increases back accordingly to the initial value.

The trial of the time interleaved setup performs observably as well as the parallel. The electrode C_{51} depicted in the previous setup is used in this trial as capacitance to be determined. The values increase when the cylinder is pulled out of the tube and decrease

Mesurement results of one cycle of rising and lowering the PE-cylinder in the ECT-tube in time interleaved setup

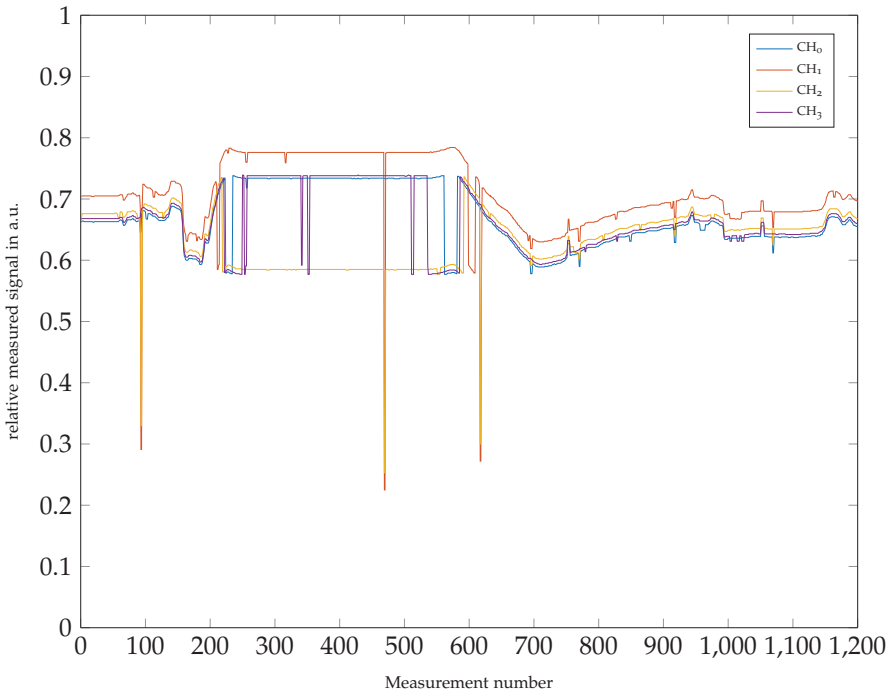

Figure 5.20. Signal graphs of one ECT electrode measured using the full time interleaved measurement setup using 4 channels.

when the cylinder is lowered back down. An offset between channel 1 and the others is observable. The reason for the seemingly parallel operation of the interleaved system is the considerable short temporal delay between the individual channels. compared to the overall measurement time of $6\,\text{ms}x1200 \cong 7.2\,\text{s}$ and the slow change in capacitance due to the manually induced movement. Although, a median-filter is applied, outliers occur in the filtered output signal. This indicates, that the filter order is set too low. Further can be seen in figure 5.20, that the output of channel 2 drops considerably when the cylinder is lifted, although the other channels reaming unchanged. It is assumed, that this effect is due measurement setup of the ECT-tube.

Concluding it can be stated, that the measurement systems works for the measurement of an ECT-system.

6 Discussion

In this chapter the findings of the previous chapters are discussed. In the first section the analysis of the available measurement technologies is discussed. In the following section, the parallel measurement setup is reviewed and in the last section the time interleaved approach. Finally, a conclusion of this work is given and possible future work topics presented.

6.1 Capacitive Measurement Technologies

In chapter 2 the currently available ICs for measuring capacitive senors are analyzed. The results found, indicate three promising commercially available circuits. The further investigation of $\Sigma\Delta$ technologies showed, that charge-based capacitance measurement methods require two main features:

- Applicability of external excitation.
- Synchronization with an external master clock.

The MAS6510 is at the time of this work the only available IC containing the features required and the implemented in the measurement system. The MAS6510 introduces the magnitude of the excitation voltage as additional degree of freedom, equation (5.1) shows the applied relation. This feature allows to adapt the range of measurement easily. However, this introduces a new source of error when providing the external excitation source.

6.2 Parallel Measurement Approach

The findings presented in section 5.1.2 show, that the parallel measurement approach can be used to improve the measurement rate of a multi-channel capacitive measurement system. The linear relation regarding excitation voltage and difference of the connected capacitances was confirmed. The tests performed, showed that the overall system performs proper and the proposed circuitry work as expected. The observation of a rather high rate of outliers of $\sim 15\,\%$, shows that the synchronization circuit has to be further improved. The two probable sources identified as source of the problem are:

- The software program of the micro controller.
- The unknown internal routines of the MAS6510.

As a solution to the problem of synchronization, the following future approaches are proposed:

- The use of a second micro processor to separate the generation of the external excitation and the control of the measurements.
- The use of a FPGA to implement the synchronization independently from the micro processor that is used.

6.3 Time Interleaved Measurement Approach

The results presented for time interleaved measurements in section 5.2 displayed a promising outcome. It could be shown that time interleaved capacitive measurements could reduce the interval between measurements to $t_{\mathrm{INT}} = 20\,\mu\mathrm{s}$. The circuit proposed to amplify the discharge current, showed promising results. The phase shift introduced by this setup has no observable influence on the results. Though, it could be observed that the time interleaved setup is more prone to these outliers observed than in the parallel configuration. Further, the noise is considerably higher and in order the achievable SNR reduced.

6.4 Conclusion

In this work two approaches to increase the measurement rate of a capacitive multi-channel measurement system were investigated. These two are parallelized and time interleaved capacitive measurement. The designed and manufactured prototype showed that these two approaches yield good results by means of acceleration of the overall measurement. The parallel approach indicates, that a greater number of measurement circuits than the five used in this thesis are possible to integrate, to further increase the measurement rate. The time-interleaved approach yielded proper results and allowed to accelerate the measurement up to an interval between measurements of $t_{\mathrm{INT}} = 20\,\mu\mathrm{s}$. Further work is focused on the improvement of the synchronization of excitation cycle and measurement cycle.

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