MASTER THESIS

BELOW GROUND OPERATION AND ZERO STANDBY CURRENT FOR A MONOLITHIC HALF BRIDGE IN AUTOMOTIVE APPLICATION

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Graz, February 2017

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Abstract

"Below Ground" Operation und Null Standby Strom für eine monolithische Halbbrücke in Automotiven Anwendungen

In den heutigen Automobilen ist der Einsatz von Elektronik nicht mehr wegzudenken. Der Funktionsumfang in den Automobilen wird immer größer und die Funktionen werden immer mehr durch die Elektronik gesteuert. Ein großen Teil der Funktionen wird hierbei von Gleichstrommotoren angetrieben, angefangen von Lichtsteuerung über Scheibenwischer und verstellbaren Rückspiegel, bis hin zur Türverriegelung. Diese Gleichstrommotoren werden von sogenannten Halb- beziehungsweise Vollbrücken angesteuert. Bis dato wird der Großteil von Halb- bzw. Vollbrücke aus integrierten diskreten Lösungen realisiert, um damit Gleichstrommotoren zu steuern. Einer der Gründe liegt darin, das speziell beim Ausschalten von Motoren, welcher in seiner Ersatzschaltung aus einem induktiven Teil besteht, sich eine negative Spannung einstellt. Somit verändert sich das Verhalten integrierter Bauteile wie MOS Transistoren. Ziel dieser Arbeit ist es, das Verhalten anhand einer monolithischen Halbbrücke zu verstehen, die Operation im Labor nachzustellen und den Baustein im Test (DUT) zu charakterisieren. Weiters ist das bestehende Schutzkonzept im Design so zu verbessern, das es mit Null Standby Strom ohne Einschränkung die Schutzfunktion erfüllt.

Below ground operation and zero standby current for a monolithic half bridge in automotive applications

Nowadays, the use of electronics in modern cars has become inconceivably important. The functional amount in modern cars is getting constantly higher and more and more functionality is getting controlled by electronics. A great part of these functions is covered by DC motors, for example headlight levelling, wiper, electric mirror and door lock. These DC motors are getting controlled by so called half- or full bridges. For controlling motors up to now, there are only integrated discrete solutions for half- or full bridges at the market. One of the reasons therefore, is the switching behaviour of the DC motor, especially in the case of switching off. In the equivalent circuit of the motor we have an inductive part, which produces a negative voltage if switching off the DC motor. Therefore, the behaviour of integrated devices, like metal oxide semiconductors (MOS) transistors is different. The goal of this master thesis is to understand the below ground operation in a monolithic half bridge and characterisation of the device under test (DUT) in the lab. Furthermore, to improve the design of the existing protection function, it should be fully functional with zero standby current.

Statutory Declaration

I hereby declare that,

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- I have not used sources or means without citing them in the text; any thoughts from others or literal quotations are clearly marked.
- the enclosed Master Thesis is the same version as the version evaluated by the supervisors.
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Acknowledgement

Try not to become a man of success,
but rather to be a man of value

(Albert Einstein)

Die Zukunft ist zuversichtlich für diejenigen,
die an ihre Träume glauben und dafür arbeiten

This master thesis was written in cooperation with the company Infineon Technologies Austria AG in Villach, within the body power department.

I want to express my special appreciation and thanks to my company supervisor Mrs. Dipl.-Ing. Francesca Romano from Infineon Technologies Austria AG, for very constructive proposals and discussions, that have contributed to the success of this work.

I also want to enunciate a big thank-you to my colleagues and to the whole Body Power department Villach at Infineon Technologies for the really good working atmosphere and for giving me the opportunity to write my Master Thesis.

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Last but not least, I want to say thanks to my friends within the Dynamobauzeichensaal (DSZ). It was a pleasure to be a member in this community, without the Dynamobauzeichensaal Z have never made this experience and I have never meet new friends, thank you.

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Chapter 1

Introduction

1.1 Motivation

The amount of ICs in the automotive area is enormous and is still increasing, especially when it comes to newer innovations, ICs are preferred. If the development of the next years is taken into account, electronic cars and autonomous driving are getting more attractive in the automotive area.

A higher part of these ICs are power transistors and concerning the power transistors, high current capability and energy efficiency is a key topic. Because of the vertical technology, SMART ICs are suitable for such requirements. Therefore, higher voltages and energy capability is possible. Especially in modern cars where relays, fuses, switches and many more applications are expiring from the technological point of view, SMART power ICs are getting more popular. Because of the increasing amount of SMART ICs in automotive applications, it is evident that there will be new innovations to enter the market. Considering the TAM (Total available market), the SMART ICs are the biggest market inside the automotive area and it is progressively moving to a higher integration. In 2015, the semiconductor TAM in the automotive area was 34 Billion Dollars and the CAGR (compound annual growth rate) between 2011 and 2015 was 8 percent. Therefore, this is a clear indication that the amount of SMART POWER ICs for automotive applications is growing.[2]

Typical application areas for power transistors in automotive applications are shown in figure 1.1.

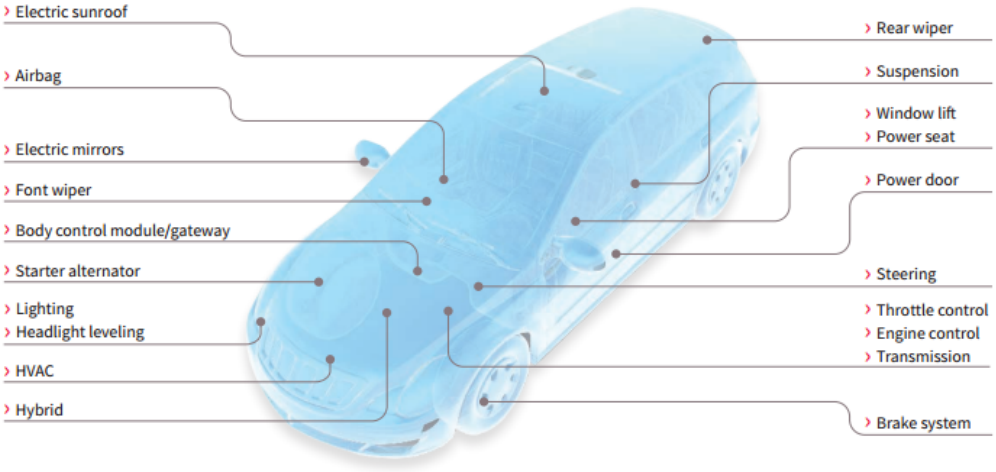


Figure 1.1: *Application of power transistor in automotive area [3]*

In principle, every application shown in figure 1.1 is from the electrical point of view a load, which can be controlled with a power transistor. As every application has its own function, for example high beam or reverse light, they also have their own electrical characteristic and behaviour. In the case of high beam, there is a 55 watt bulb and in the case of the reverse light there is a 21 Watt bulb. This leads to the fact that a power transistor has its own robust design for a certain functionality in the automotive area that can be controlled.

1.2 Research Goal - Task Definition

In this master thesis, which is an innovation project, the focus lies on the existing product test chip (PTC). The existing PTC is a monolithic Half-Bridge, which is basically a highside switch (HSS) and a lowside switch (LSS) in SMART Technology. This Master thesis is separated in two parts.

The first part basically, is the characterisation of the existing PTC in the laboratory. In more detail, this means the characterisation of the LSS and its behaviour in below ground operation. This includes the setup definition for the different characterisation scenarios, as well as the post processing for the characterisation data.

The second part includes the concept and design for the next PTC, which should work with zero standby current in off state. Up to now, the PTC works with a standby current of 3uA, which is needed because the protection function in case of the below ground operation has to be functional. In the next PTC the protection has to work with the target of zero standby current.

Chapter 2

Fundamentals

This chapter covers the basic information about the technology and circuit theory for automotive applications, which is needed as basic understanding for further considerations.

2.1 Voltage Requirements in Automotive Applications

In figure 2.1, the static and transient voltages in a 12V battery car net are illustrated. It can be seen that voltages within a car net can be 60V and above and therefore electronic circuits and especially integrated circuits, have to be designed to withstand these high voltages. Therefore, most SMART power technologies are rated for 60V.

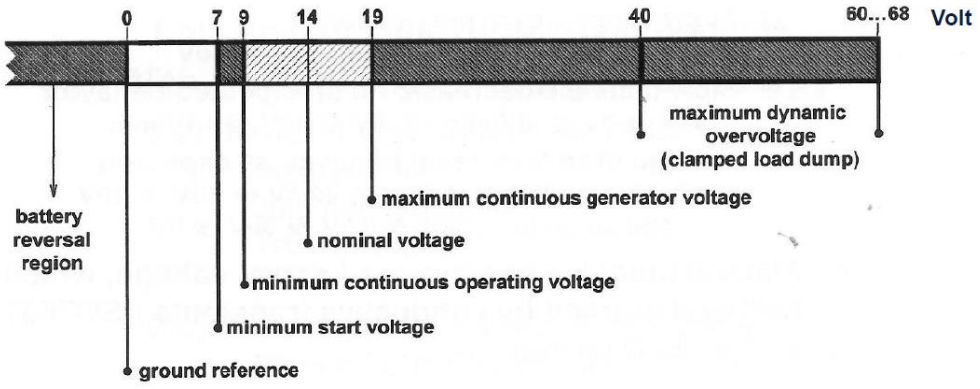


Figure 2.1: *Voltage requirments in automotive applications [4]*

2.2 Smart Power Technology

Integrated circuits can be analog, digital or power electronics. According to the requirement, there exist three different technologies: bipolar, MOS or power technologies. SMART offers the integration of these three technologies, which can be analog and digital circuits combined with the power stage on one single chip. In the literature, this is also called BCD technology. The name BCD has been created in the mid-eighties to classify the family of mixed technology processes, which allow to integrate into a single chip Bipolar, CMOS and DMOS transistors, forming a new power IC class, called SMART power IC [1]. The SMART part of the SMART power IC adds the protection and the diagnostic function to the power transistor. In SMART power technologies, an integrated power device is used, which is called double-diffused MOS (DMOS) transistor. Depending on its needs in application, the DMOS can be implemented in a vertical or lateral structure, where vertical and lateral defines how the current is flowing, in a geometric manner.

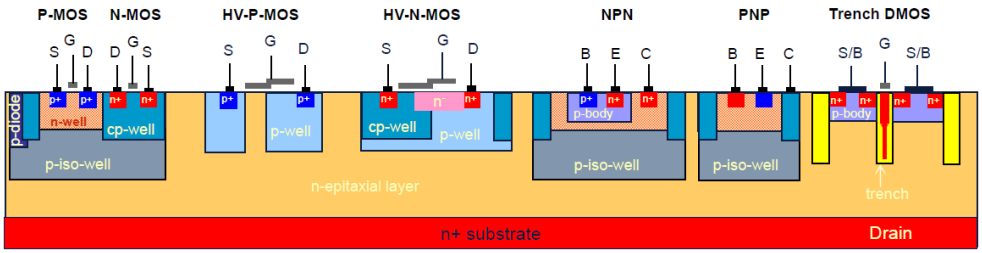


Figure 2.2: *Cross section overview of the SMART power technology [4]*

2.2.1 Vertical DMOS Transistor

In this section the vertical trench DMOS is explained, as it is commonly used in that kind of SMART power applications. The cross-section in Figure 2.3 illustrates a concept of a basic vertical DMOS, with the drain directly connected to substrate, which gives a lower contact resistance to the supply line. A big advantage of the vertical approach is, that the current flows vertically through a channel from the substrate, which allows very high current densities, and this at comparatively low area effort. As Figure 2.2 shows, the DMOS is arranged with vertical trench gates.

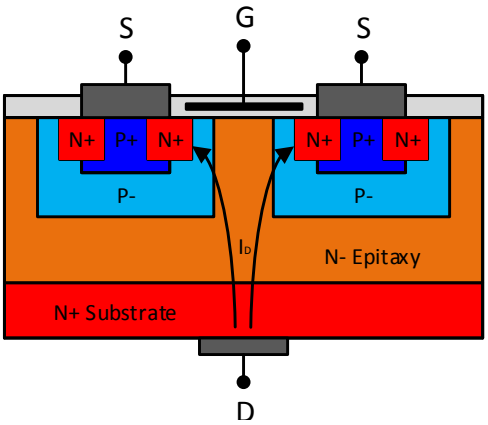


Figure 2.3: *Cross section of a vertical DMOS power transistor [5]*

The main drawback of the vertical structure with drain connected to substrate is given, because it is only possible to integrate one DMOS, without sharing the drain [1]. The substrate has to be connected to a positive supply voltage (according self isolation) and therefore, the drain of the DMOS is fixed to the positive supply voltage, as seen in figure 2.4. In the case of automotive applications the supply voltage is the battery in the car.

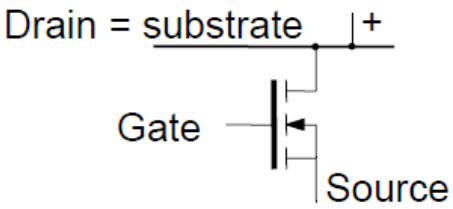


Figure 2.4: *Drain of the DMOS is fixed to the positiv supply voltage [4]*

2.2.2 Lateral DMOS Transistor

In this section, the lateral DMOS, which is also called NLDMOS (**N**-channel **L**ater DMOS), is explained. As already mentioned, in section 1.3, the difference between vertical an lateral DMOS is how the channel is formed. The cross-section in figure 2.5, illustrates a concept of a basic lateral DMOS. In the cross-section, the identification of an HV MOS transistor is given by the ndrift region.

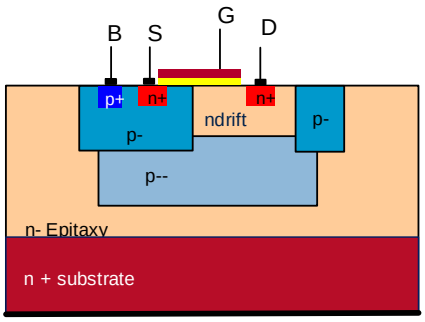
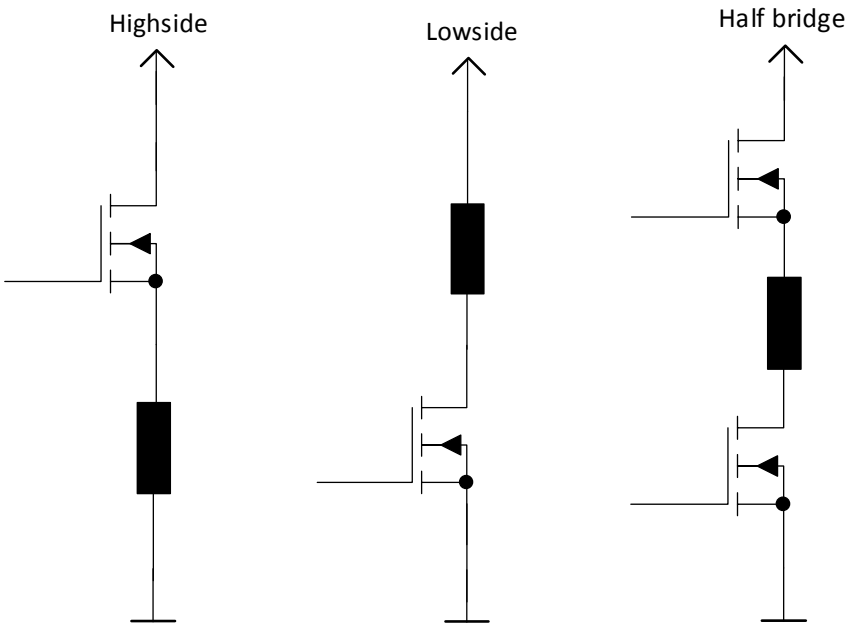


Figure 2.5: *Cross section of a lateral DMOS power transistor*

The drawback of the lateral structure, is the increasing DMOS area to withstand the increasing voltages, especially the ndrift region is getting larger, which leads to a higher on-resistance.

2.2.3 Circuit topologies power transistor

With the power transistors explained in the section 2.2.1 and section 2.2.2, it is possible to have three circuit topologies with respect to the load and supply voltage, which are shown in figure 2.6.



(a) *Highside switch* **(b)** *Lowside switch* **(c)** *Halfbridge*

Figure 2.6: *Power transistors circuit topologies*

The circuit topology (a) in figure 2.6, is called highside switch (HSS). Although a p-channel MOS (PMOS) would be more suitable for this kind of application, the n-channel MOS (NMOS) is used, because of its higher mobility of the charge carrier. The DMOS is located between the power supply and the load, which in the case of short-circuit to ground, the load does not get destroyed. That is a benefit only because of its topology. However, for switching on the DMOS, the gate potential has to be higher than the supply voltage, which needs an additional control block, called charge pump. The highside switch is used for switching resistive loads or bulbs.

The second circuit topology (b) in figure 2.6, is called lowside switch (LSS). Here, the DMOS is located between the load and the ground potential. The potential of the drain contact is close to the ground potential, depending on the DMOS on-resistance. Because, the DMOS is connected to the ground potential, it is only necessary to reach the threshold voltage of the DMOS at the gate contact to switch on the DMOS. The topology in lowside switch configuration is used to drive loads such as inductances.

The circuit topology on the right side (c) in figure 2.6, is called Half-Bridge. Here, the load is in between the highside switch and the lowside switch. In the case of a Half-Bridge, loads are mostly motors, because it is possible to drive the motor in forward and reverse direction with this Half-Bridge topologies.

In the following chapters, the focus of explanation is on the Half-Bridge and especially its monolithic implementation and upcoming challenges.

Chapter 3

Half bridge in SMART Power Technology

This chapter presentes a general overview of a Half-Bridge and an H-Bridge (Full-Bridge) in SMART power technology, as well as the switching behaviour of motors. Furthermore, the topic is more in detail about the monolithic half bridge in SMART power technology, which is the main topic of this master thesis.

3.1 H-Bridge Configuration

The schematic shown in figure 3.1, is called H-Bridge or Full-Bridge and is basically the combination of two Half-Bridges, as shown in the dashed rectangle. As explained in chapter 2.1.3, the load is in between the highside switch and the lowside switch and from the theoretical point of view it can be assumed, that the highside switches and lowside switches in both Half-Bridges are equal. But in practice, because of process variation, there is a mismatch between the Half-Bridges. If a look is taken to the highside switch, this transistor is well suited for Vertical SMART technology, which means that the drain of the highside switch is fixed to the positive supply voltage. On the other hand, the drain of the lowside switch is connected to the source of the highside switch, which clearly indicates that the realization of the lowside switch in vertical SMART technology is not possible, if used on the same silicon die.

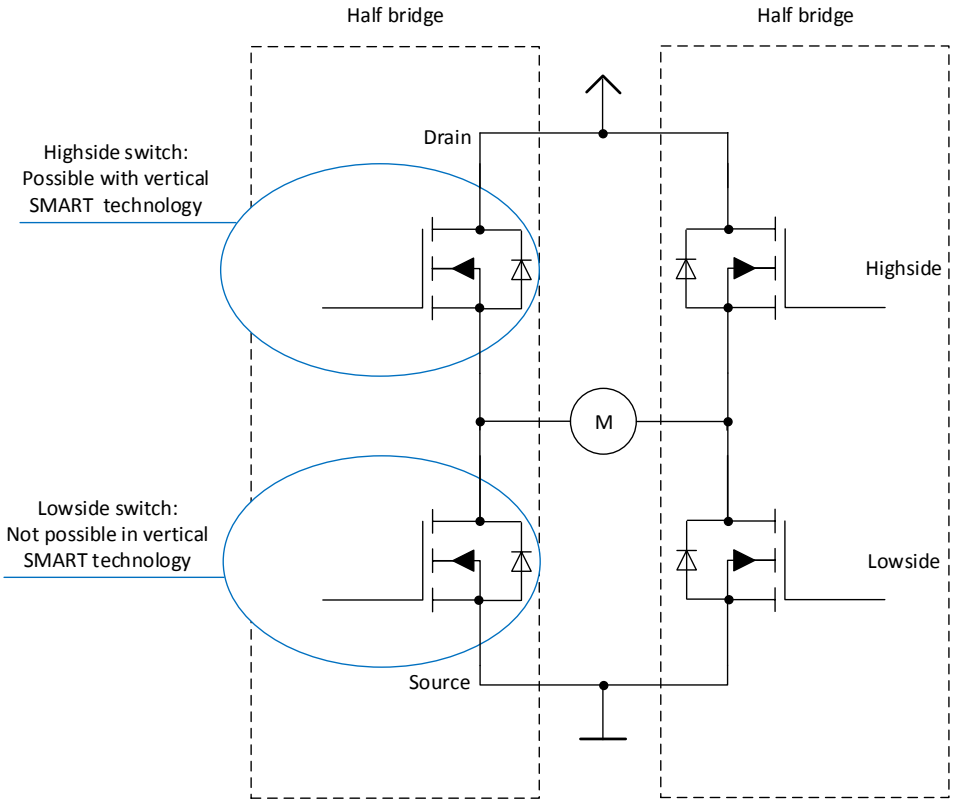


Figure 3.1: *Schematic of a H-Bridge configuration*

As shown in figure 3.1, it is possible to drive the motor in forward and reverse direction. Therefore, we need a relationship between the electric part, represented by the highside switches and the lowside switches and the mechanical part, which presents the motor. This relationship is given by the Lorentz force.

$$\vec{F} = I \cdot (\vec{l} \times \vec{B}) \tag{3.1}$$

$\vec{F}$...Force $[N]$

I...Current $[A]$

$\vec{l}$...Conducter length $[m]$

$\vec{B}$...Magentic flux density $[T]$

For the rotation of the motor, either in forward or in reverse direction a torque is needed, which is represented in the relationship of the power. From the electrical point of view, the

torque is represented by the current, so for the equation 3.3, the current is proportional to the torque.

$$P = \vec{M} \cdot \vec{w} \tag{3.2}$$

$$where \qquad I \approx \vec{M} \tag{3.3}$$

$$P ...\text{Power} \quad [W]$$
$$\vec{M} ...\text{Torque} \quad [Nm]$$
$$\vec{w} ...\text{Angular} \quad \text{speed} \quad [rad^{-1}]$$

In figure 3.2, the current flow for forward and reverse direction of the motor is illustrated. Per definition that switching on the highside switch M1 and the lowside switch M4, the motor is rotating in forward direction, as well as switching on the highside switch M2 and the lowside switch M3, rotates the motor in reverse direction.

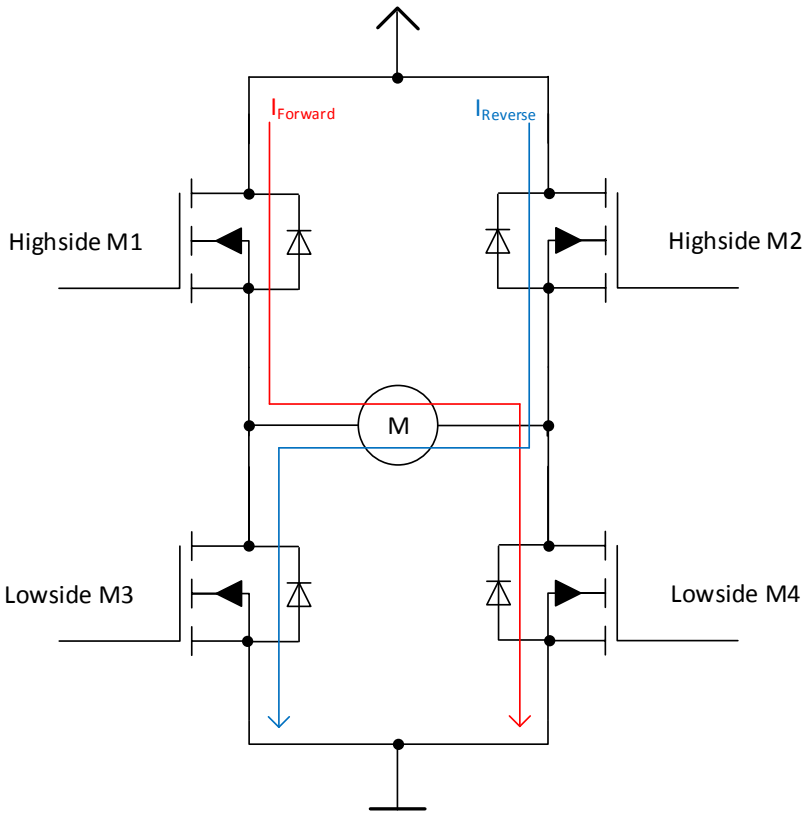


Figure 3.2: *Current flow for forward and reverse direction of the motor*

As previously discussed, the knowledge of the components and how to build a Half-Bridge and H-Bridge in concept, is given. Furthermore, how the current is flowing to provide the required rotation direction, either forward or reverse, of the motor was explained. In the next step, a short discussion about the electrical behaviour of the motor is necessary. In figure 3.3, the equivalent circuit is illustrated, which consists of an ohmic part, an inductive part and a voltage induced part. V_{ind} describes the induced voltage via a conductor which moves through a magnetic field. The higher the velocity of the movement through the magnetic field, the higher is the induced voltage. In case of the motor, the coil moves through the generated magnetic field, which induces the voltage V_{ind}. The voltage V_{ind} is depending on the angular speed and is also called electromotive force (EMF). For further considerations, the voltage V_{ind} can be neglected.

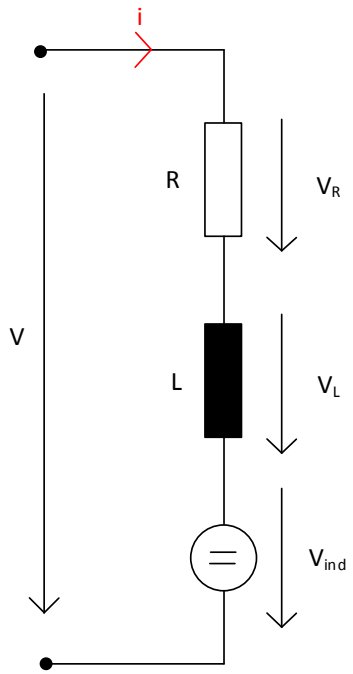


Figure 3.3: *Equivalent circuit of a DC Motor*

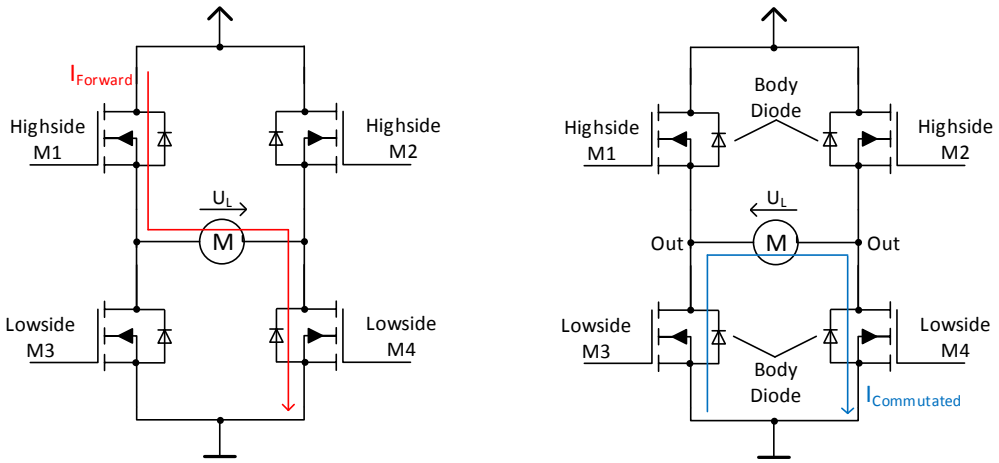
$$V = V_R + V_L + V_{ind} \tag{3.4}$$

$$V = i \cdot R + L \cdot \frac{di(t)}{dt} + V_{ind} \tag{3.5}$$

For further considerations, the behaviour of the inductive part, especially when switching the motor is important. An inductance is basically an energy storage device. The energy which, is stored in an inductance is given by the formula 3.6.

$$E = \frac{L \cdot I^2}{2}[J] \tag{3.6}$$

The H-Bridge configuration and the case of a forward direction, are illustrated in figure 3.4 (a). The current is flowing through the motor and through its inductive part, which generates a voltage V_L and stores energy, as formula 3.6 describes. When the current flow in forward direction stops, the energy stored in the inductance cannot disappear, as the law of conversation of energy says. The energy stored in the inductance, has to be dismantled and this happens because the inductance acts like a voltage source with opposite sign, illustrated in figure 3.4 (b). Therefore, the out node, shown in 3.4 (b), becomes a negative potential, which means a voltage below ground. If this negative voltage reaches the 0.7 V (Silicon) of the Body Diode, then this is biased in forward direction and the current will flow through it. This is how the stored energy in the inductance gets dismantled in an H-Bridge. The current $I_{Commutated}$ is flowing over the Body Diode of M3 and the Body Diode of M2 as long as the negative voltage is that negative to keep the PN - Junction of the Body Diode in forward direction.



(a) *Forward current* **(b)** *Commutated current*

Figure 3.4: *Current flow in forward direction and for the accumulate current*

Basically, the charging and discharging current via the inductance is defined by formula 3.7 and formula 3.8. Concerning the discharging phase, after 5T there are still approximately 2% remaining of the initial charge current.

$$charge: \qquad i(t) = \frac{V}{R} \cdot (1 - e^{\frac{t}{T}}) \tag{3.7}$$

$$discharge: \qquad i(t) = \frac{V}{R} \cdot (e^{\frac{t}{T}}) \tag{3.8}$$

$$where \qquad T = \frac{L}{R} \ [s] \tag{3.9}$$

3.1.1 State of the art of H-Bridges in SMART Power technology

As already mentioned in figure 3.1, the highside switch can be realised in SMART vertical technology but the lowside switch cannot be realised in SMART vertical technology, concerning a monolithic half - bridge. Therefore, for the lowside switch, a high voltage mosfet device is used. It is possible to combine all four power transistors in one package, which is shown in figure 3.5. It can be seen that the two highside switches, marked in figure 3.5 as high-side-Smart-FET, share the same piece of semiconductor and both lowside switches, marked in figure 3.5 as low-side-MOSFET, are separated on their own piece of semiconductor.

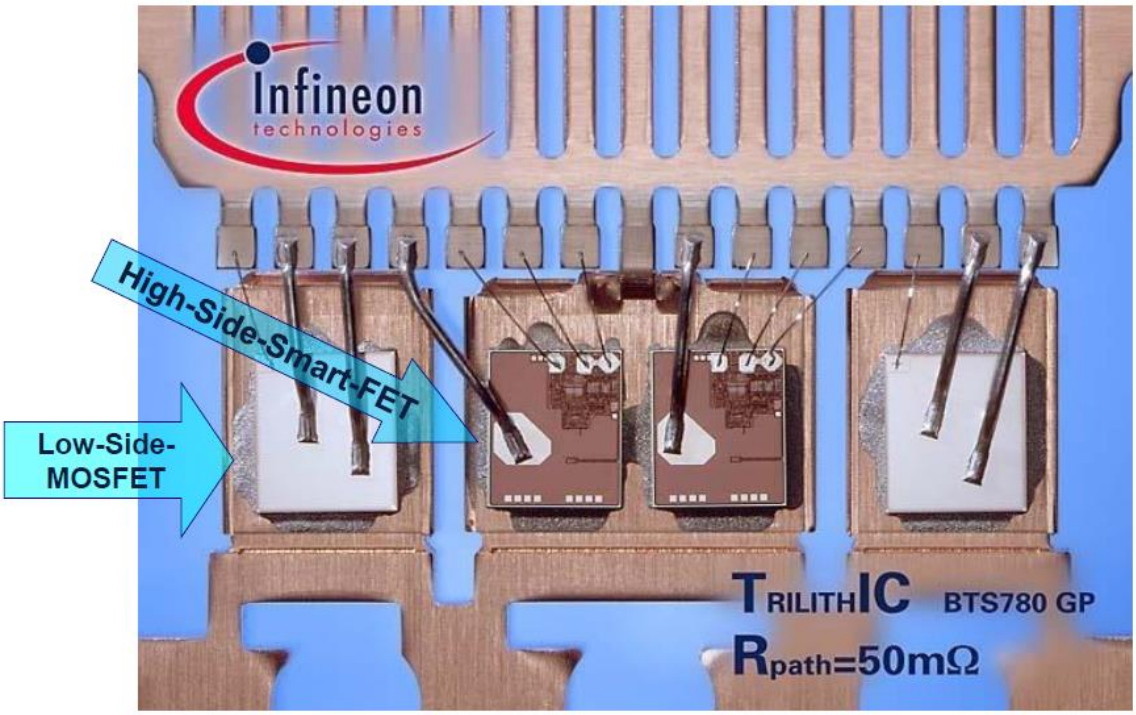


Figure 3.5: *Trilithic H-Bridge [4]*

3.2 Monolithic Half-Bridge

In the previous chapter 3.1, the H-Bridge configuration was explained, as well as the behaviour of the inductive part of the motor, when the supply voltage is on or off. So far, these considerations are for discrete highside and lowside switches. In the next step the Monolithic Half-Bridge and its challenges are explained. A short addition concerning the discrete description, as earlier explained, the highside switches are well suitable for vertical SMART technology. Therefore, it is possible to combine the two Highside switches within a H-Bridge on a single Semiconductor (DIE), where the Lowside switches are realized separately.

For the Monolithic Half-Bridge, the highside switch and the lowside switch are on the same Semiconductor (DIE), as shown in figure 3.6, within the blue dashed rectangle. Therefore, the highside switch is realized in vertical SMART technology and the lowside switch is realized in lateral SMART technology. The same is valid for the second Half-Bridge, shown in figure 3.6 with the dashed symbols.

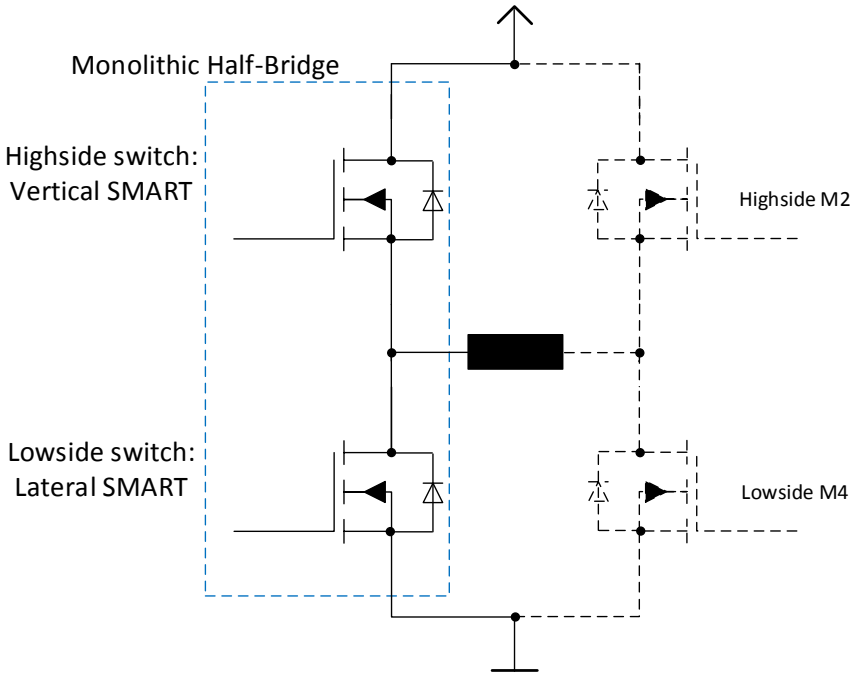


Figure 3.6: *Monolithic Half-Bridge*

In figure 3.7, the cross-section view of the monolithic Half-Bridge concept is shown. On the left hand side of 3.7, the lateral DMOS with the ndrift region for higher voltage capability is shown. On the right hand side of figure 3.7, the vertical trench DMOS is illustrated, its drain contact is located at the backside and it is only isolated from the lateral DMOS via p- and n- junctions.

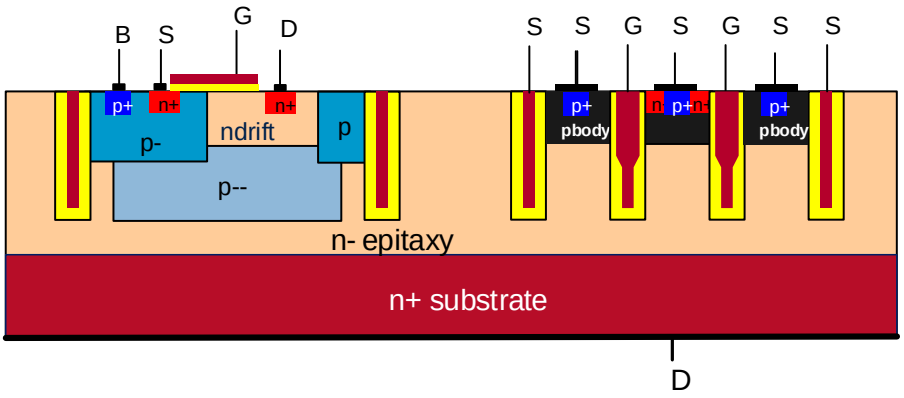
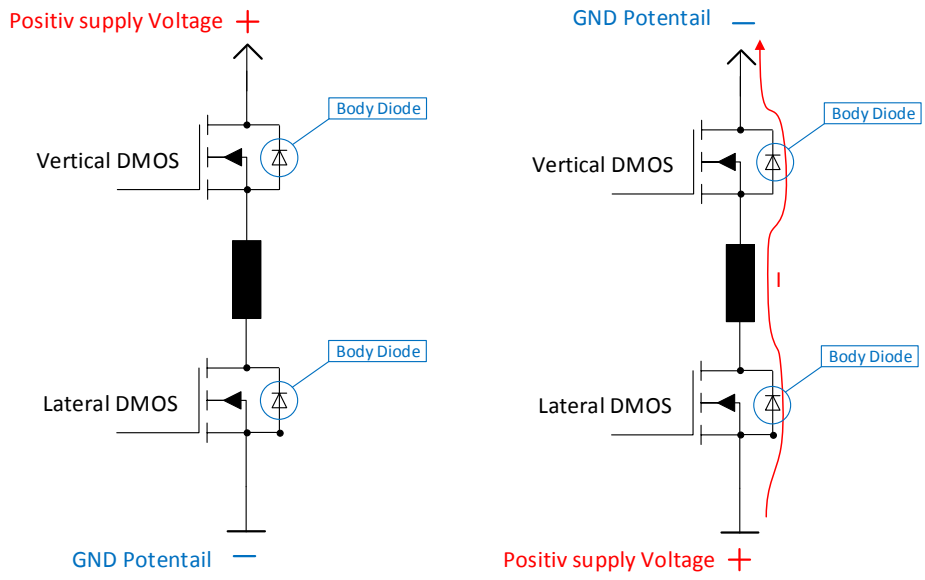


Figure 3.7: *Crosssection view of a Monolithic Half-Bridge*

3.2.1 Parasitic NPN Bipolar Transistor

As just mentioned, the lateral DMOS and the vertical DMOS are isolated from each other via p- and n- junctions, which is called self - isolation. Self isolation is the simplest implementation and is used in any MOS process. Isolation of neighbouring components is only done by applying the correct voltages to the terminals in respect to the substrate or well connection. The SMART power self isolation processes are based on a n-substrate p-well CMOS approach. It is neccasary to apply a positive voltage to the n-substrate to allow isolation of p-type devices.[4]

An example for self - isolation concerning the monolithic Half-Bridge is shown in figure 3.8. Illustrated in the figure 3.8 (a), is the correct applied car battery, where the positive voltage is connected to the drain contact of the vertical DMOS and the ground potential is connected to the source of the lateral DMOS. This configuration ensure self - isolation concerning the body - diode. Although, it is possible that the car battery gets connected wrongly, this scenario concerning self - isolation is shown in figure 3.8 (b). It can be seen that the positive voltage is connected to the source contact of the lateral DMOS and the ground potential is connected to the drain contact of the the vertical DMOS. Therefore, the body - diode of the lateral DMOS and the vertical DMOS is in forward direction and a current I can flow. In this configuration, self - isolation is not ensured, because the applied voltages are not correct connected.



(a) *Self Isolation ensured* **(b)** *Self Isolation violated*

Figure 3.8: *Example of self isolation concerning the battery voltage*

A closer look to the cross-section view of the lateral DMOS, clearly identifies the challenge as shown in figure 3.9: the parasitic body diode and the parasitic substrate diode. At the lateral DMOS, the bulk and source are connected, which always leads to a diode between the source and the drain contact, called the body diode. Thus, the substrate in the SMART technology is n - doped, which results in another parasitic diode, called the substrate diode between the source and substrate. As earlier mentioned, the substrate is basically fixed to the positive supply voltage, which needs to ensure self isolation.

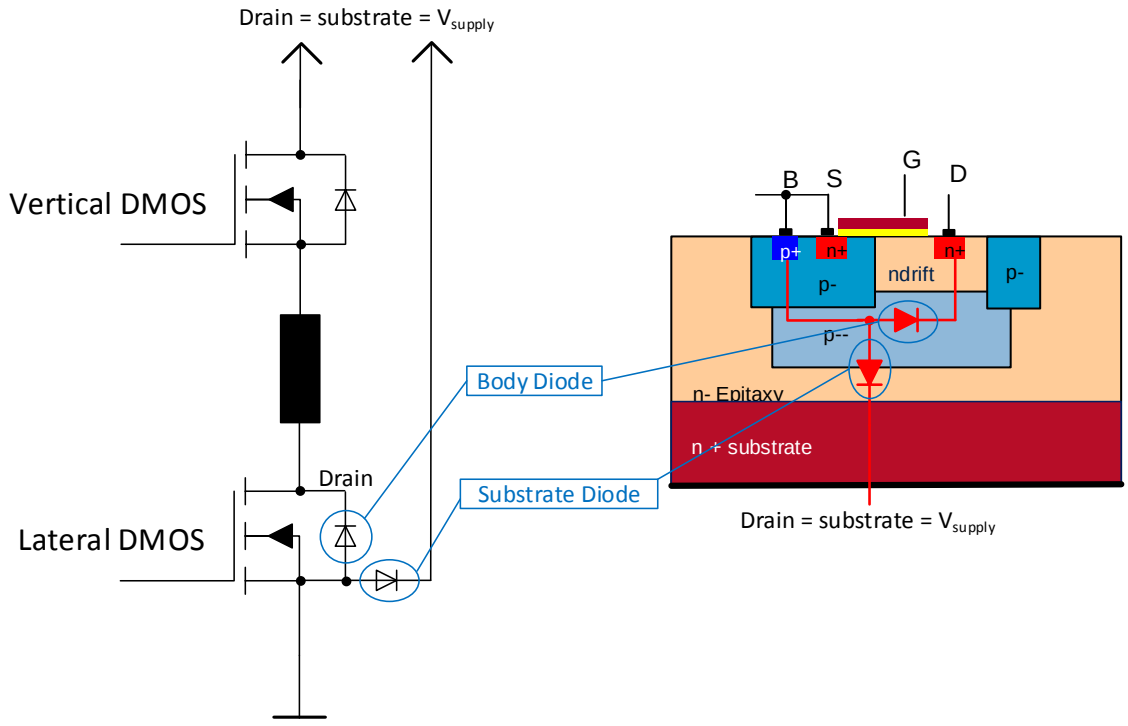


Figure 3.9: *NLDMOS parasitic Diode*

The observation of these two parasitic diodes, the body diode and the substrate diode, lead to the fact that they are forming a parasitic NPN bipolar transistor. The concept is illustrated in the cross-section view of figure 3.10. Here in particular, the challenge of the Monolithic Half-Bridge is visible, because it has a parasitic NPN bipolar transistor with its emitter contact connected to the drain contact of the lateral DMOS, which is basically the output of the Half-Bridge. Its collector contact is connected to the substrate, which is fixed to the supply voltage.

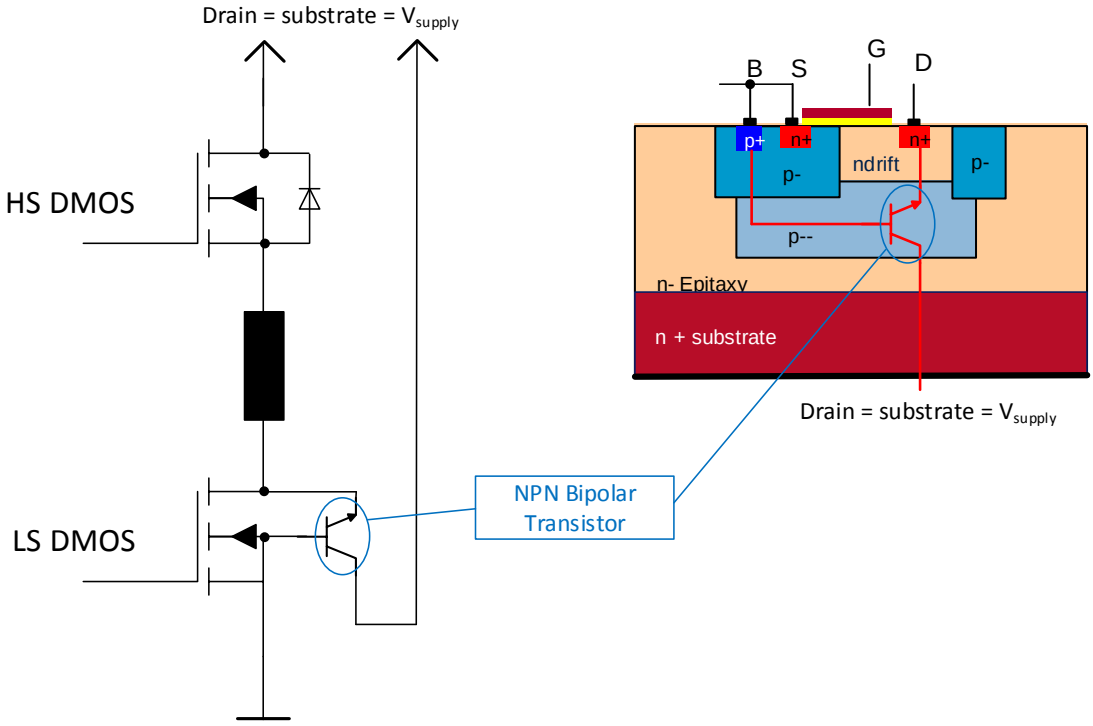


Figure 3.10: *NLDMOS parasitic NPN Bipolar Transistor*

In the formulas 3.10, 3.11, 3.12, the mathematical description for the Bipolar transistor is listed. Where V_{BE} is the base emitter voltage, V_T is the thermal voltage, which is approximately 26mV at room temperature and I_S describes the saturation reverse current, which is depending on the emitter area A and the technology constant I_0.

$$Collector \quad current: \qquad I_C = I_S \cdot e^{\frac{V_{BE}}{V_T}} \cdot (1 + \frac{V_{CE}}{V_A}) \tag{3.10}$$

$$Base \quad current: \qquad I_B = \frac{I_S}{\beta} \cdot e^{\frac{V_{BE}}{V_T}} \tag{3.11}$$

$$Gain: \qquad \beta = \frac{I_C}{I_B} \tag{3.12}$$

$$where: \qquad V_T = \frac{kT}{q}, \qquad I_S = I_O \cdot A \tag{3.13}$$

k...Boltzman constant $[\frac{J}{K}]$

T...Temperature $[°C]$

q...Elementary $charge$ $[C]$

The circuitry shown in 3.10, is sophisticated when it comes to switching off the load, especially in case when switching an inductive load within its discharging phase. Therefore, the lateral DMOS and its parasitic NPN transistor have to be characterised and its behaviour in case of the inductive discharge phase, like a motor load, can be understood. First of all, the consideration of the behaviour of the parasitic NPN transistor in a theoretical view should be mentioned. To force the same conditions like an H-Bridge in forward direction, the schematic in figure 3.11 is given. Considering, the HS DMOS is switched on and the LS DMOS is switched off, that a current I_L, which is defined by the load resistance R_L at a certain supply voltage V_{Supply} is flowing. This generates a voltage drop V_{RL} and V_L over the resistor R_L and the inductance L. Because of the very small R_{ON} of the HS DMOS, the V_{DS} of it is in the range of mV. Therefore, the bridge out node is nearly the supply voltage V_{Supply}. Now considering, that after a certain time the HS DMOS switches off, the inductance becomes a voltage source with an opposite sign, as illustrated in 3.12. Therefore, the bridge out node becomes a potential, which drops below ground. When it reaches the V_{BE} of 0.7V below ground, the base emitter diode of the parasitic NPN transistor is biased in forward direction, which leads to the commutate current I_{COM}, at the clamped V_{BE} voltage of 0.7V. Due to the fact that the

base emitter diode is already biased in forward direction, the parasitic NPN transistor is getting active, which provides an additional current path from the substrate I_{SUB}.

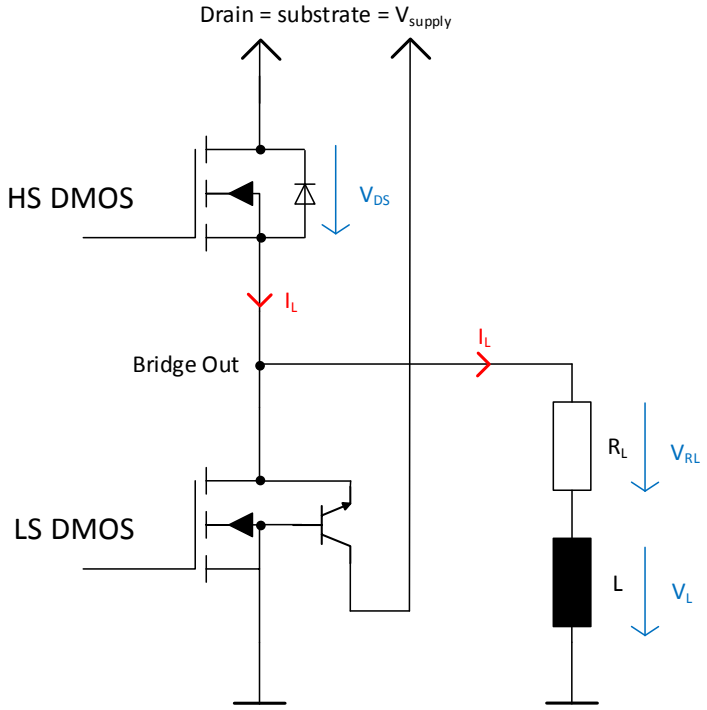


Figure 3.11: *HS DMOS switched on*

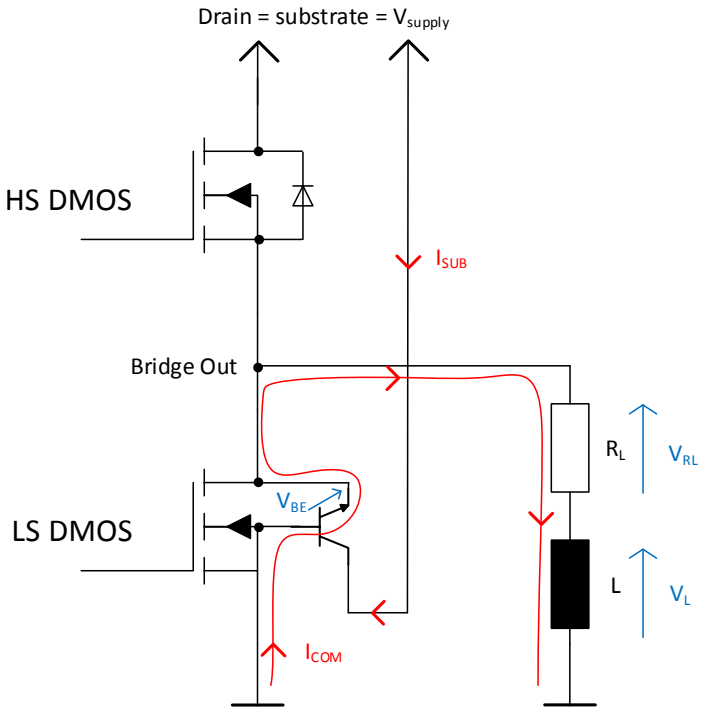


Figure 3.12: *HS DMOS switched off*

Chapter 4

Lab characterisation of the Monolithic Half-Bridge

As previously noted, this master thesis is based on an already available product test chip (PTC). The implementation of the lateral DMOS was a former master thesis [6]. In this chapter the characterisation of the existing PTC, also the lateral DMOS and specially its parasitic NPN transistor in the laboratory, is covered. Therefore, the behaviour of its current robustness, energy capability and the behaviour of temperature are evaluated.

4.1 Stand - alone lateral DMOS

In order to ensure only the characterisation of the lateral DMOS and its parasitic NPN transistor, without any influence from the HS DMOS, the semiconductor fabrication plant (FAB) provides product test chips, where only the lateral DMOS is implemented, called stand-alone lateral DMOS. This means, that the gate, source and drain are accessible to connect via the pins from the package, as seen in figure 4.1.

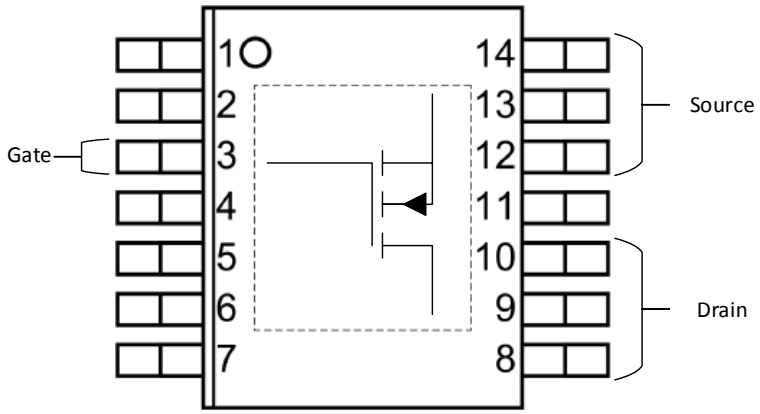


Figure 4.1: *IC Package of the stand-alone NLDMOS*

4.1.1 Setup defintion for stand - alone characterisation

As mentioned, the characterisation of the stand - alone lateral DMOS is required. Therefore are correct setup, which performs with the same requirements as the Half-Bridge is needed. This setup is implemented with the circuitry shown in figure 4.2. The important behaviour is the off phase, when the inductance generates the negative voltage and the Bridge Out note gets below ground potential. Therefore, a discrete single HS switch is used to provide the load current I_L, which will be set by the load resistor R_L. Another point to mention is, to ensure the lateral DMOS is switched off, the gate and the source of it are connected. Therefore, the gate source voltage V_{GS} is in fact zero, thus there will be no channel generated, where the current is flowing. In the final setup, for the off phase, the current can flow only via the base emitter diode when the bridge out node is below the V_{BE} of 0.7V. In addition, the current I_{VS} from the substrate is provided when the parasitic NPN transistor gets active, which is the case when the base emitter diode is active. For this reason, and to characterize the parasitic NPN transistor the currents in the circuitry can be expressed as:

- $I_L = I_{EMITTER}$
- $I_{GND} = I_{BASE}$
- $I_{VS} = I_{COLLECTOR}$

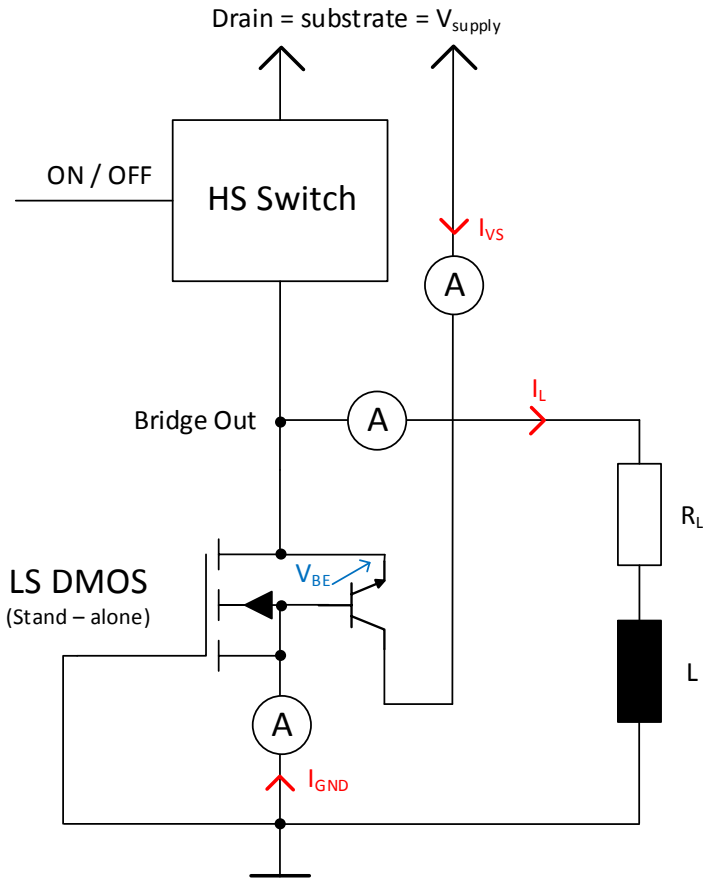


Figure 4.2: *Characterisation setup of the stand - alone NLDMOS*

4.1.2 Activation of the parasitic NPN transistor

As in the previous section mentioned, the NLDMOS in stand - alone configuration will not switch on, this means there will be no channel, in which the current can flow. Therefore, the current can only flow via the body diode, which leads to the activation of the parasitic NPN transistor. This behaviour is illustrated in figure 4.3. It can be seen, that the V_{OUT} node gets below GND and if its reaches the diffusion voltage of approximate 0.7V, the body diode is in forward direction, which leads to an increasing base current I_{Base} for the parasitic NPN transistor. Further, if the PN - junction of the body diode is already dismantled, the parasitic NPN transistor is active, which can be noticed with the increasing of the collector current $I_{Collector}$. The decreasing load current, which basically is the emitter current $I_{Emitter}$, leads to a decreasing V_{OUT}, until the current is completely accumulated. During the decreasing of the V_{OUT}, the amount of the collector current $I_{Collector}$ gets zero, because the V_{OUT} drops below the diffusion voltage. Although, after the parasitic NPN transistor is inactive, there is a base current I_{Base}, which equals the load current, which is basically the emitter current $I_{Emitter}$. The reason, that I_{Base} and $I_{Emitter}$, in the phase where the parasitic NPN transistor is inactive, are equal, is because the only current path in the circuit to accumulate it, is via the body diode. For the sake of completeness, as it can be seen in figure 4.3, the V_{OUT} signal is trimmed in x-direction. This is only because figure 4.3, should illustrate the starting of the off phase concerning the inductive part of the motor, where the inductance generates a negative output voltage V_{OUT}. This negative voltage is the trigger for the activation of the parasitic NPN transistor, therefore figure 4.3, shows a zoom of the output voltage V_{OUT}.

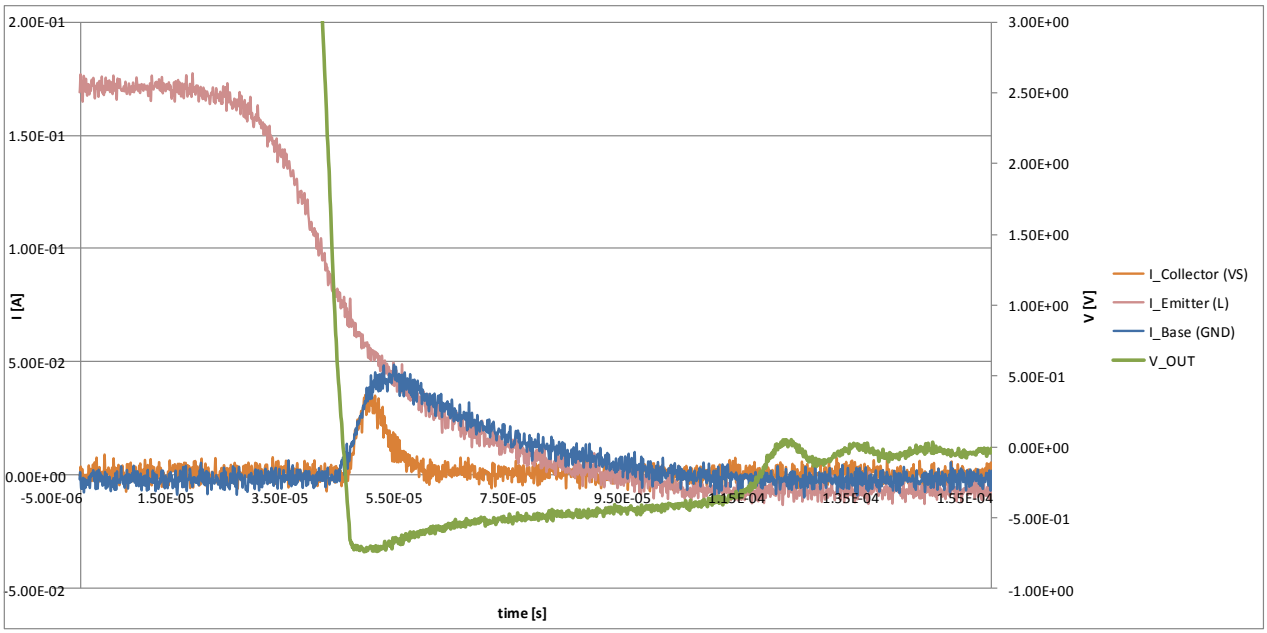


Figure 4.3: *Active parasitic NPN transitor*

4.1.3 Parasitic NPN Transistor characterisation

For the input and output characterisation of the NPN transistor, a setup, as illustrated in figure 4.4 is required. Therefore, the stand-alone NLDMOS circuitry, to characterise the parasitic NPN transistor turns out as shown in figure 4.5. Both schematics are in grounded emitter circuits. In the stand-alone schematic shown in figure 4.5, the gate is shorted to the source, therefore, gate and source have the same potential and the NLDMOS does not switch on. For this reason, the schematic in figure 4.5, has the same behaviour as the schematic in 4.4. Therefore, it is possible to characterise the parastic NPN transistor in the same way such as single NPN transistor. For the input characteristic a constant V_{CE} is given and the base emitter voltage V_{BE} gets sweeped, the result turns out the threshold voltage V_{TH} of the parasitic NPN transistor. On the other hand, for the output characterisation a constant base current I_B is given and the collector emitter voltage V_{CE} gets sweeped. For different base currents I_B, these turns out, in which of the three regions the bipolar transistor is working, these regions are the active region, the cut-off region and the saturation region.

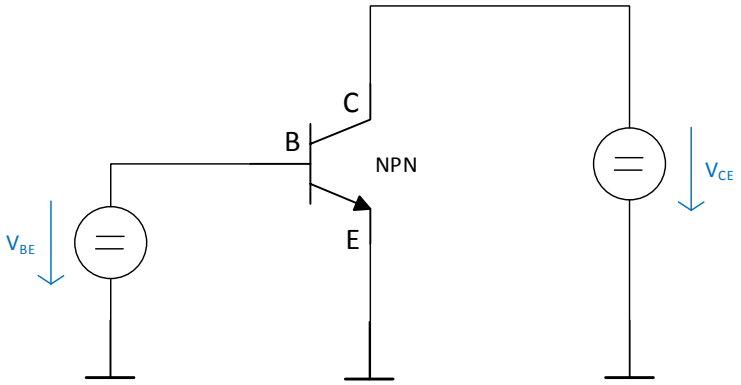


Figure 4.4: *Input and output characterisation of a NPN transistor*

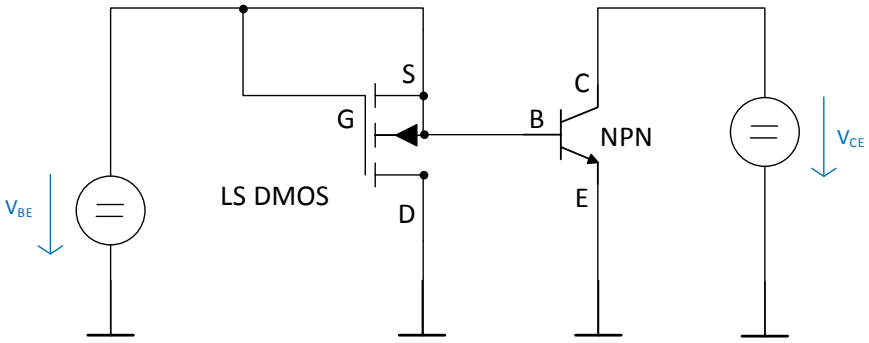


Figure 4.5: *Stand-alone NLDMOS schematic for the parasitic NPN characterisation*

In figure 4.6, the input characteristic of the parasitic NPN transistor is shown, it can be recognized that the threshold voltage V_{TH} is around 370mV. As mentioned in figure 4.6, the measurement has its limitation because of the parameter analyser. This is because the parameter analyser has only one channel with current limitation of 1A and all other channels has a current limitation of 100mA. Furthermore it can be seen in figure 4.7, the output characteristic of the parasitic NPN transistor, which shows nicely the active region, the cut-off region and the saturation region.

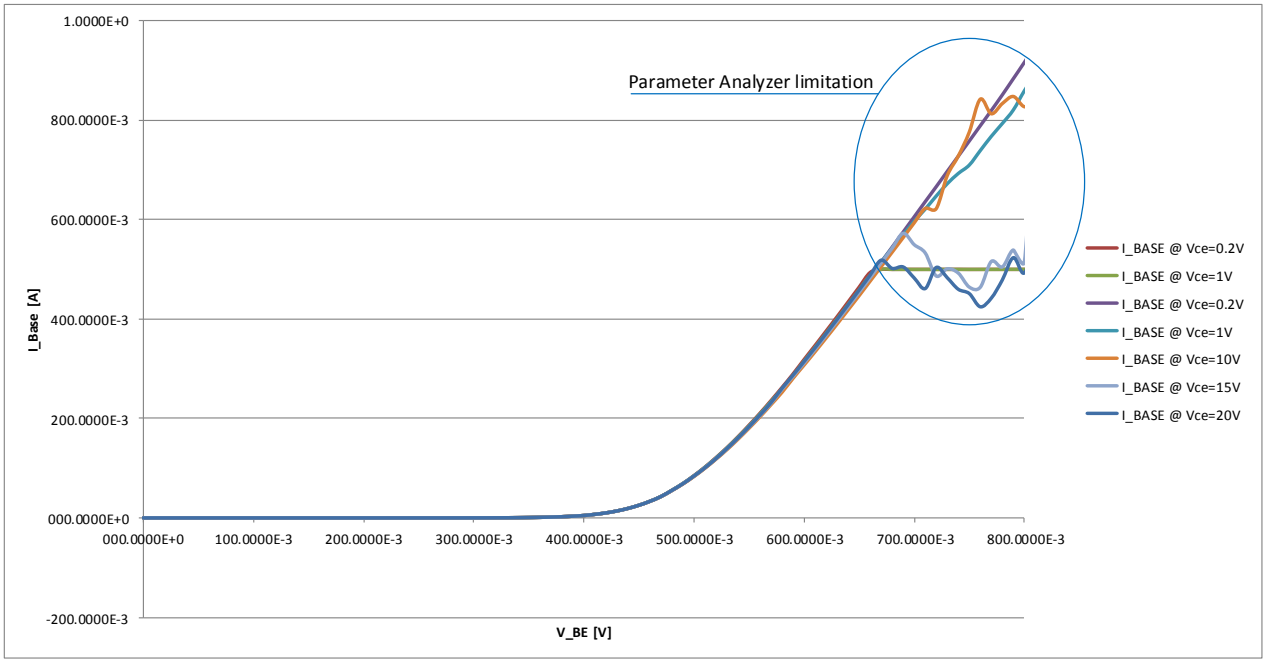


Figure 4.6: *Input characterisation of the parasitic NPN transistor*

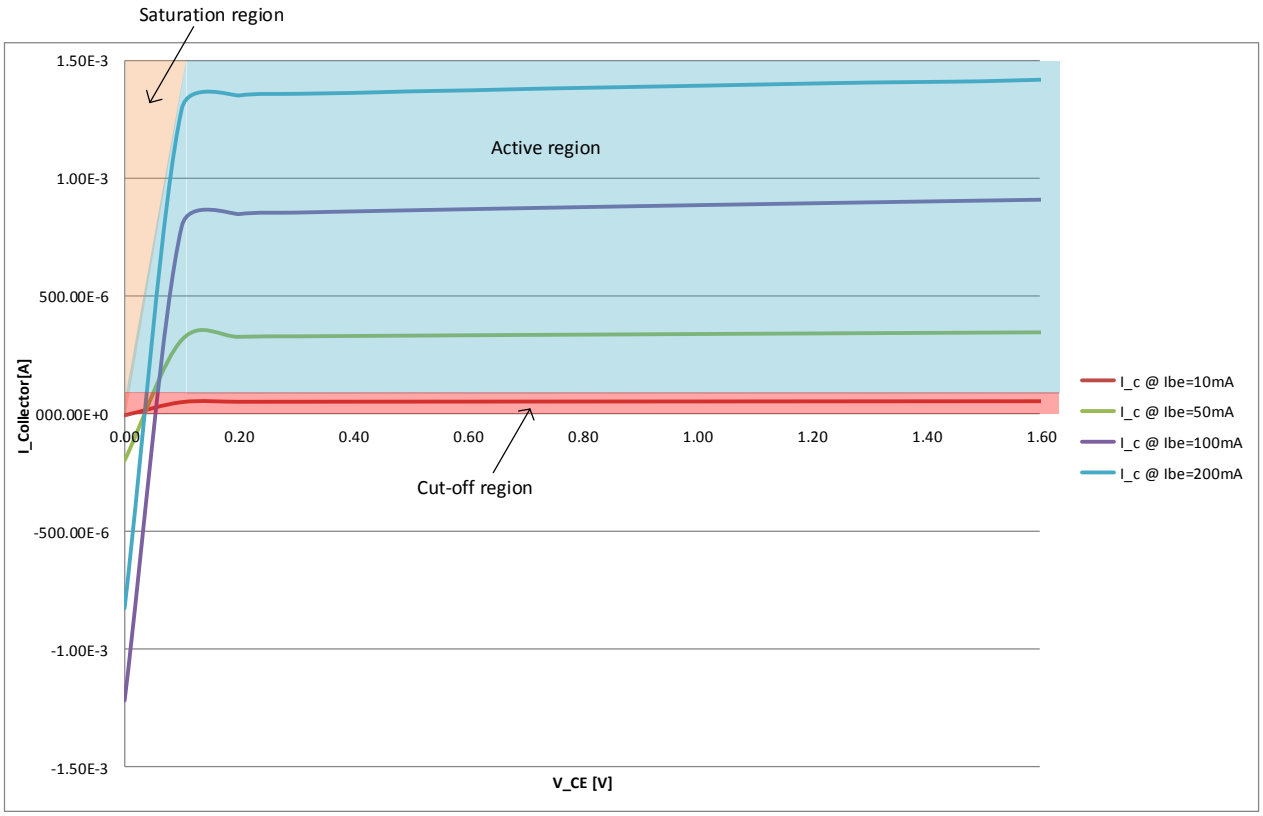


Figure 4.7: *Output characterisation of the parasitic NPN transistor*

In the input characteristic and the output characteristic it can be seen, that for example the value for the V_{TH} is lower as expected. This is because, in the stand - alone setup, the gate and the source contact are shorted, means V_{GS} of zero volt. Although, there is a leakage current flowing, via the NLDMOS channel, which is part of the base current of the parasitic NPN transistor. Therefore, the value of the V_{TH} in the input characteristic and the regions in the output characteristic are lower as expected. Due to the reason, the gate and source connection were done in the circuit design, it was not possible to release that connection. This means, the stand - alone IC was fabricated with a gate to source connection.

In figure 4.8, the gummel plot of the parasitic NPN transistor is shown. The gummel plot is a further characterisation where the collector current I_C and the base current I_B in logarithmic scale, versus the base emitter voltage V_{BE} is shown. The gummel plot gives informations about the gain $_\beta$, series resistance and leakage currents of the transistor. For the characterisation in this master thesis, the information about the gain $_\beta$ is important. In 4.8, it can be observed that around 600mV base emitter voltage V_{BE}, the collector current I_C and the base current I_B are running approximately parallel.

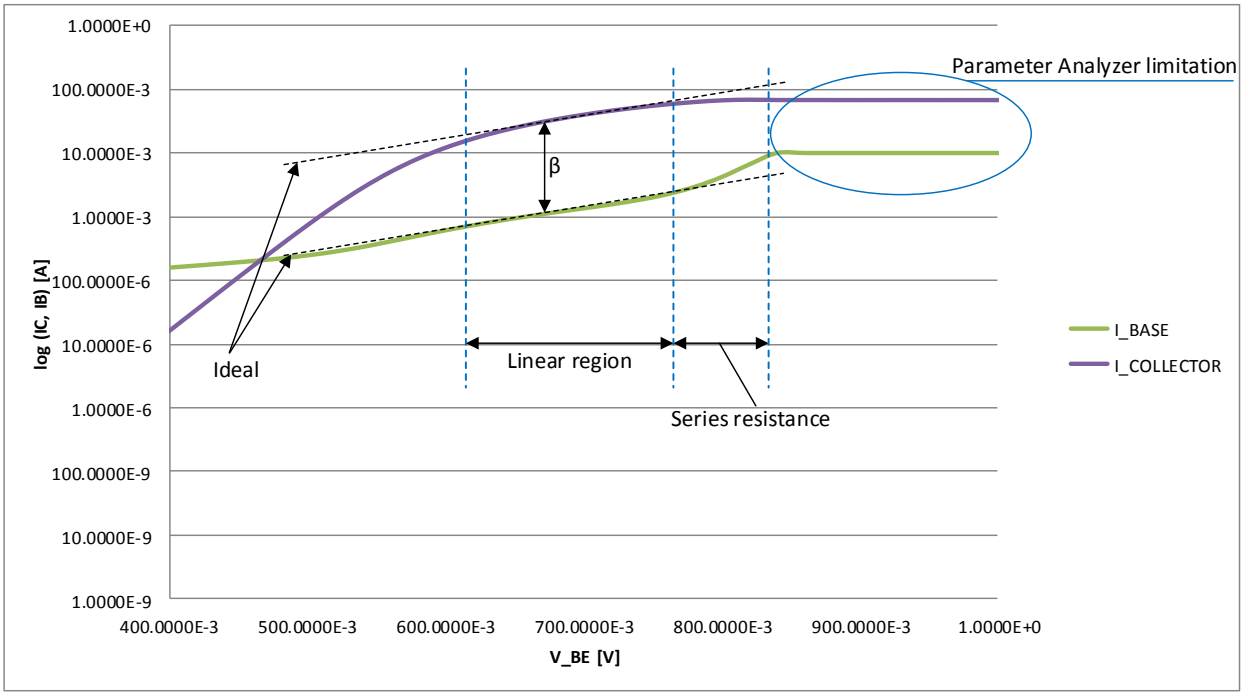


Figure 4.8: *Gummel Plot of the parasitic NPN transistor*

Figure 4.9, shows the gain extracted from the gummel plot and calculated with the formula shown in 4.1. With increasing base emitter voltage V_{BE}, the gain is also increasing to a maximum, which is a gain around 30. A comparison to a bipolar transistor which should be designed with a certain gain, its gain should be around 100. After the peak of the gain, is decreasing, because the transistor region turns more into active region, the current is not significantly increasing. This is also seen in 4.8, at around 820mV base emitter voltage V_{BE}, where the collector current I_C and the base current I_B run together.

$$\beta = \frac{I_C}{I_B} \tag{4.1}$$

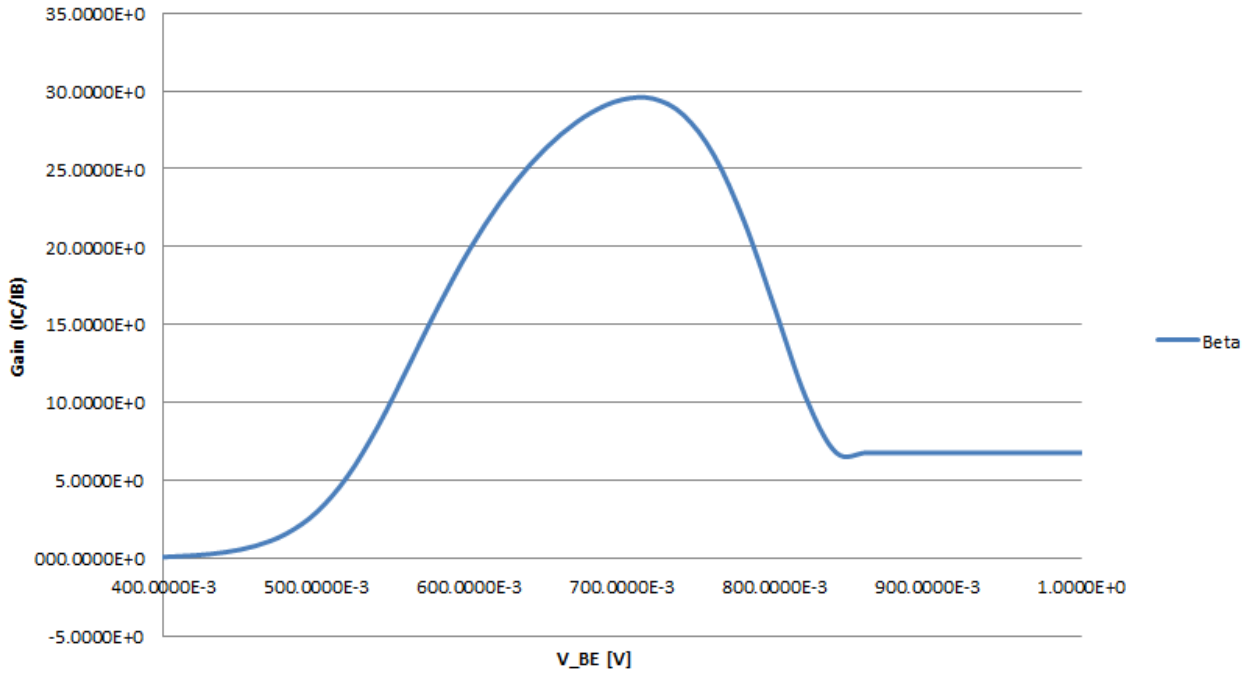


Figure 4.9: *Gain of the parasitic NPN transistor*

4.1.4 Energy capability of the Parasitic NPN Transistor

As already mentioned, especially the switching off phase of an inductive load is the phase where the characteristic has to be done. Therefore, another characterisation which has to be done is the energy capability of the parasitic NPN transistor. The energy capability

is important when an inductance is part of the circuit. In the case of this master thesis, it is a motor in automotive application but it can also be a long wire, for example in a truck. The inductance defines the time to commutate the current, which is essential for the energy calculation. In the case of the monolithic Half-Bridge, there are basically two energy parts. The first energy is given by the inductance of the motor and the second is given by the power supply, if the parasitic NPN transistor gets active. Both energy parts has to be accumulated, the inductance has its energy as long as the current is not zero and the power supply provides energy as long as the parasitic NPN transistor is active.

The setup definition is illustrated in figure 4.10, for the energy capability of the parasitic NPN transistor the V_{CE} and the complete current across the parasitic NPN transistor, is required. The resulting current I_L, is basically the sum of the current which gets driven by the inductance, as well the additional current from the supply. Basically, the energy in a circuit can be calculated as shown in formula 4.2 and in the case of the parasitic NPN transistor this results in formula 4.3. Starting with formula 4.2, it can be insert in formula 4.4, which turns out formula 4.5, where its derivative with respect to time chancels and results in formula 4.6. Therefore, for the energy calculation of the parasitic NPN transistor the formula 4.7 which results in formula 4.9 was used. The product of V_{CE} and I_L in every point, which is basically the power P, multiplied by the time difference over the whole switching off phase.

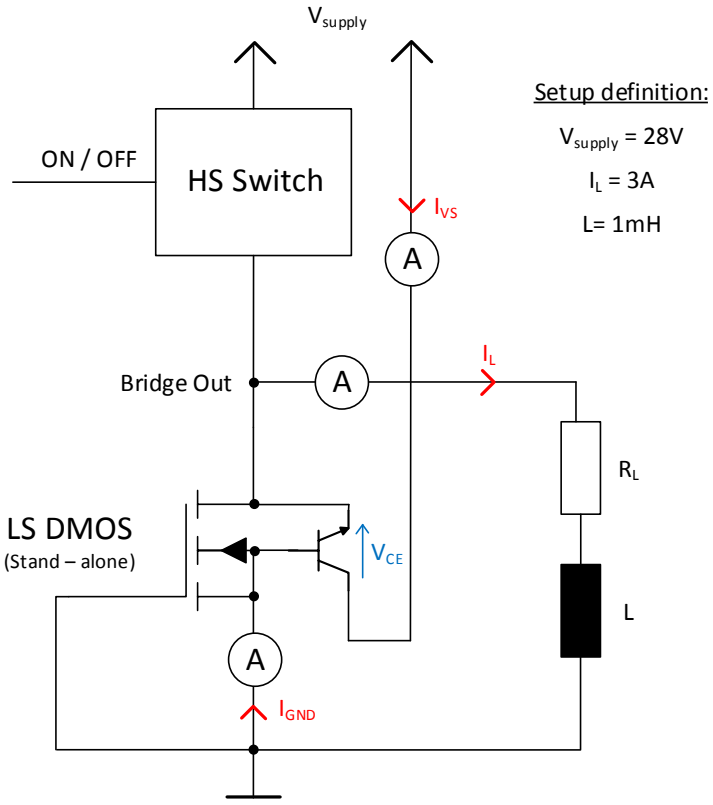


Figure 4.10: *Characterisation setup for the energy capability*

$$E = \int_{t1}^{t2} v(t)i(t)dt \tag{4.2}$$

$$E = \int_{t1}^{t2} v_{CE}(t)i_L(t)dt \tag{4.3}$$

$$P = \frac{dE}{dt} \tag{4.4}$$

$$P = \frac{\int_{t1}^{t2} v(t)i(t)dt}{dt} \tag{4.5}$$

$$P = v(t) \cdot i(t) \tag{4.6}$$

$$E = (V \cdot I)\Delta t = (V_{CE} \cdot I_L)\Delta t \tag{4.7}$$

$$E = P\Delta t \tag{4.8}$$

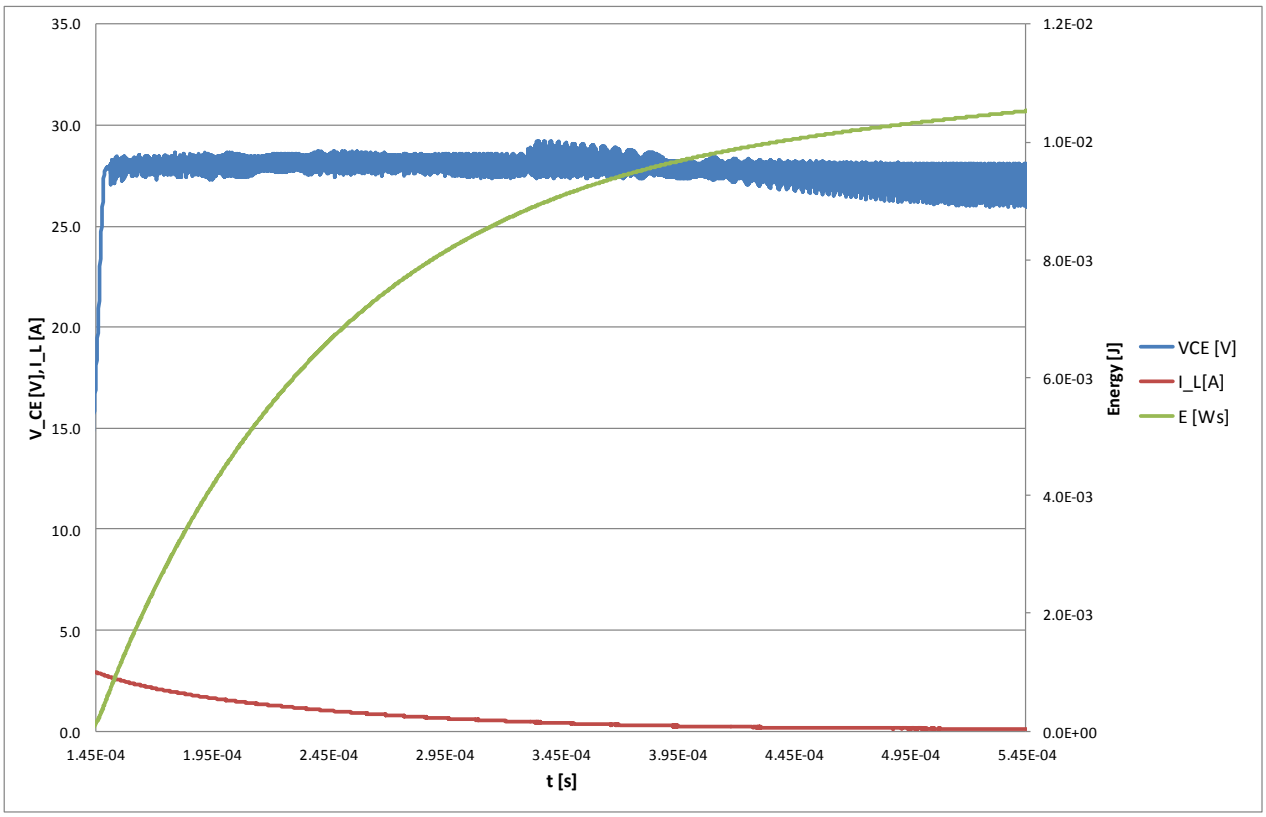


Figure 4.11: *Energy curve for the setup shown in Figure 4.10*

In figure 4.11, it can be seen, that the energy E is increasing over the time as long as there is a commutated current from inductance and as well as from the voltage supply. At the beginning, there is a steeper slope of the decreasing I_L, therefore the energy slope has a steeper increase. If the current I_L gets smaller, also the shape of the energy slope gets smoother, and the energy curve have a saturation where the total amount of energy E dissipated in the circuitry is seen. In figure 4.11, with setup from 4.10, the total amount of energy dissipated E in the circuitry from figure 4.10 is nearly:

$$E = 11mJ \tag{4.9}$$

In addition, shown in table 4.1 and figure 4.12, the dissipated energy of the parasitic NPN transistor with a fixed inductance of 1mH and different load currents I_L is shown. As already mentioned, the energy in a case of a motor is depending on the inductance L and the current I_L, a higher inductance and a higher current leads to a longer commutated current. Also the energy in the closed circuit is increasing, until that time the device under test (DUT) gets destroyed,therefore, the product design has to ensure that this point will never be reached for the target application. For the application concerning this master thesis, the current for the target application is around 3A and the total amount of energy is around 11mJ, as already mentioned in formula 4.9.

Table 4.1: *Energy characterisation summary*

Parameter	Symbol	Value					Unit
Commutated current	I_L	0.5	3	5	7	10	A
Collector Emitter Voltage	V_{CE}	25.1	28	28	28.2	28.2	V
Operation Temperature	T_{amb}	25	25	25	25	25	C
Total Energy	E	0.74	11	28	29	49	mJ

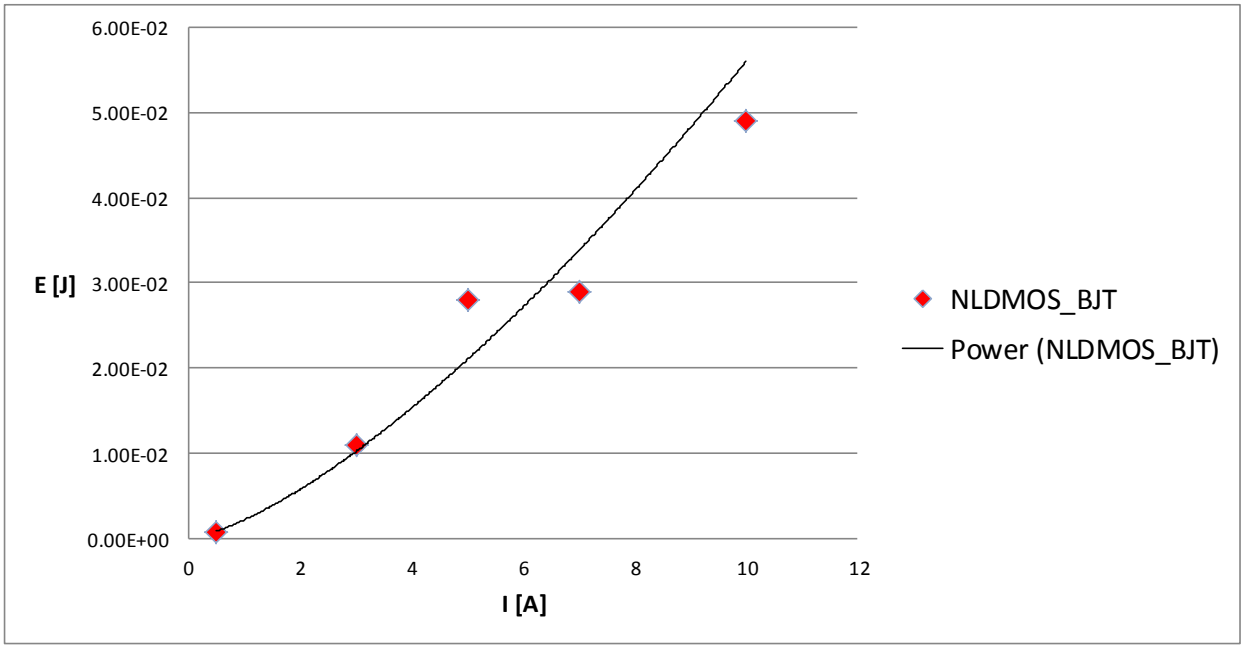


Figure 4.12: *Energy curve with different current I_L*

4.2 Product Test Chip

As seen in chapter 4.1, the characterisation of the parasitic NPN transistor where done. In this chapter, the already existing product test chip gets characterised and its protection concept concerning the activation of the parasitic NPN transistor. For the product test chip, the complete functional Half-Bridge is available, this means the highside switch as well as the lowside switch is implemented and fully functional, as shown in figure 4.13.

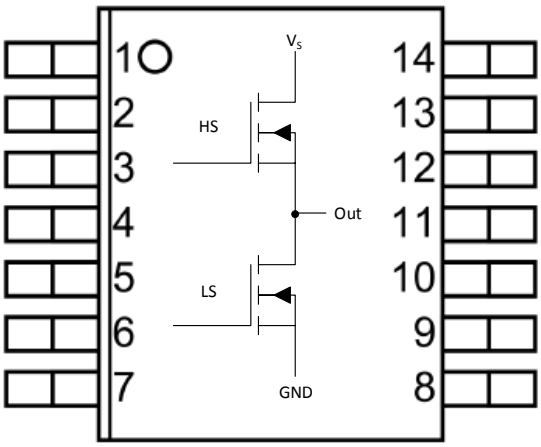


Figure 4.13: *IC package overview of the product test chip*

4.2.1 Below GND protection

Illustrated in figure 4.14, is the setup for the characterisation of the product test chip. By switching on the highside DMOS the current I_{Load}, as illustrated in 4.14, is flowing and will charge the inductance. By switching of the highside DMOS, the inductance acts like a voltage source with opposite sign, as already mentioned. So the output voltage V_{out}, gets below GND. To characterise this behaviour for the product test chip and in especially concerning the protection function, it is necessary to measure the load current I_{Load} as well as the ouput voltage V_{out}.

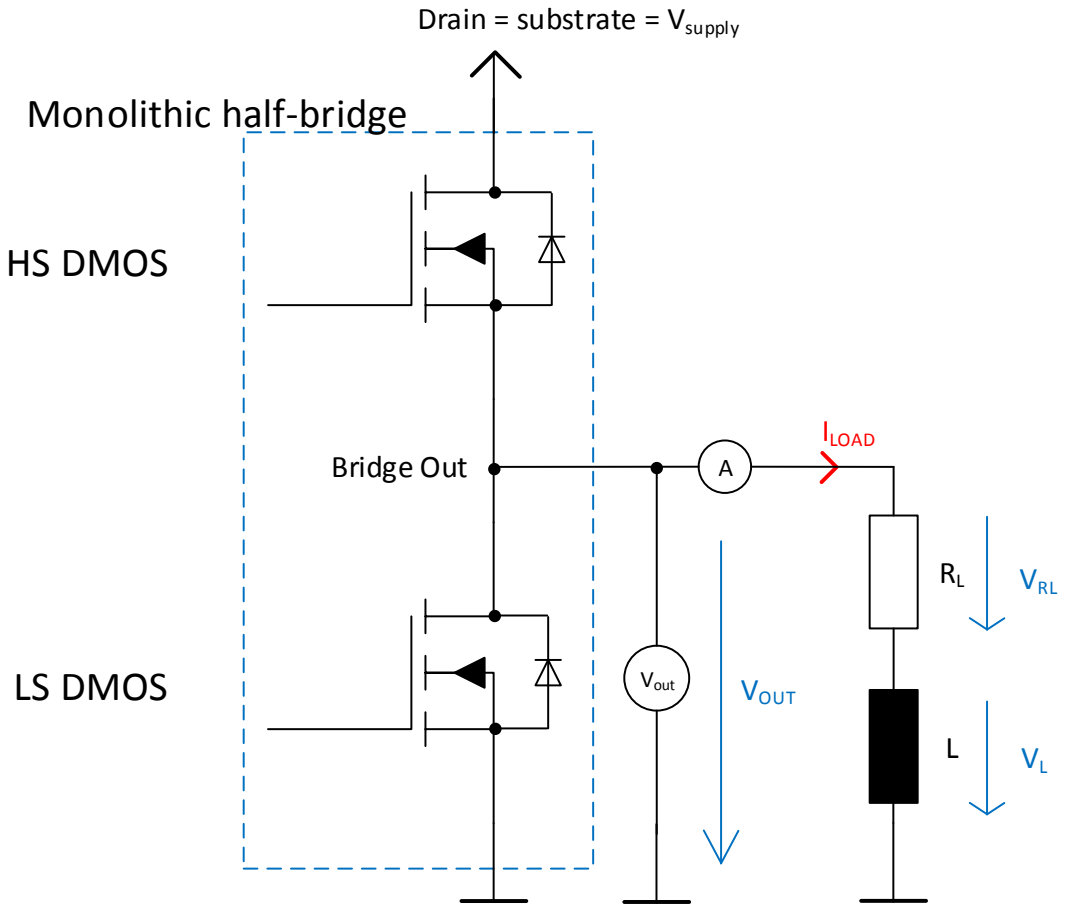


Figure 4.14: *Setup for the product test chip characterisation*

As already mentioned, the product test chip has a protection concept against the activation of the parasitic NPN transistor, which is called below GND protection. For the explanation of the below GND protection, consider figure 4.15. As already explained, in the switching off phase of the motor, because of its inductance part, the V_{out} node gets a negative voltage, means below GND, as long as a current is present. This can be seen in 4.15. The accumulated current, illustrated as I_{Load} has its exponential behaviour in the discharge phase and the output voltage V_{out}, gets below GND. At the first glance it will notice, that the output voltage V_{out} is oscillating, but this behaviour, identifies the activ below GND protection. A closer look to the detail plot 4.17, will show in which way this protection is working, a more detailed explanation is made in chapter concept development and design. As pointed out earlier, the below GND protection has to be fully functional in off mode, therefore, this product test chip has a stand-by current of 3uA.

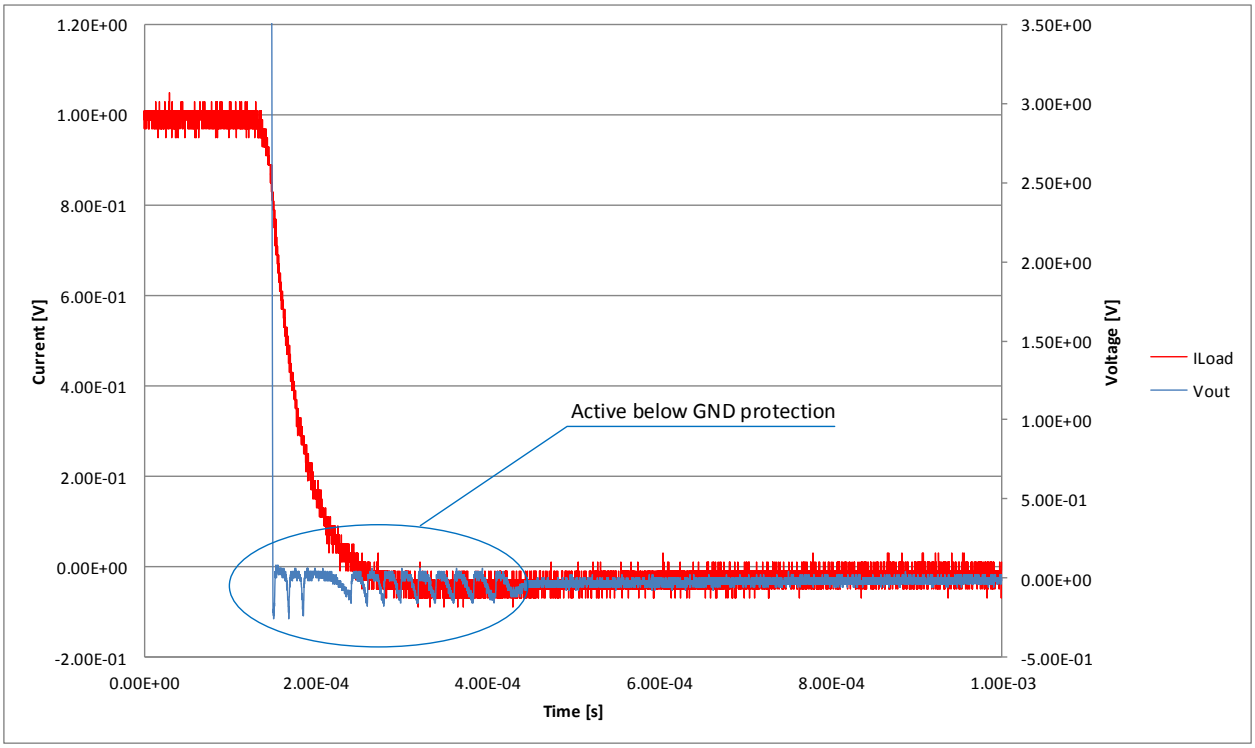


Figure 4.15: *Illustrated protection against the activation of the parasitic NPN transistor*

Basically, in the case, where the output voltage V_{out} node gets below GND, the NLDMOS gets switched on. The detection of the below GND voltage is realized with a comparator, illustrated in figure 4.16. At the spike 1 in figure 4.17, its seen that the output voltage V_{out} gets below GND, at the threshold of the comparator, the NLDMOS gets switched on. Therefore, the current can accumulate via the channel of the NLDMOS and not via the body diode any more, which was the main root cause for the parasitic NPN transistor activation. If the NLDMOS is switched on, its V_{DS} is much smaller, compared to the diffusion voltage of the body diode, which is basically the base emitter diode of the parasitic NPN transistor. The reason for the small V_{DS} is, because the NLDMOS has a very low resistance R_{DS}. Therefore, the V_{out} node approaches to the resulting V_{DS}. Although there is still a higher amount of current in the circuit, which has to be accumulated. So, the comparator switches off at a different threshold voltage, what means, that the V_{out} note is decreasing (see figure 4.17), and drops again below GND to the point, where the comparator switches on again. This happens as long the current is not zero and a negative voltage will be generated that the comparator can detected it and switch on the NLDMOS to accumulate the current via the channel of the NLDMOS. If the current is that small, that also the negative voltage does not activate the comparator, the NLDMOS does not get switched on any more. Which must be stated, is that the below GND comparator has two threshold voltages, one for switching on the NLDMOS and the

second for switching off the channel of the NLDMOS. This means, that the comparator has a hysteresis.

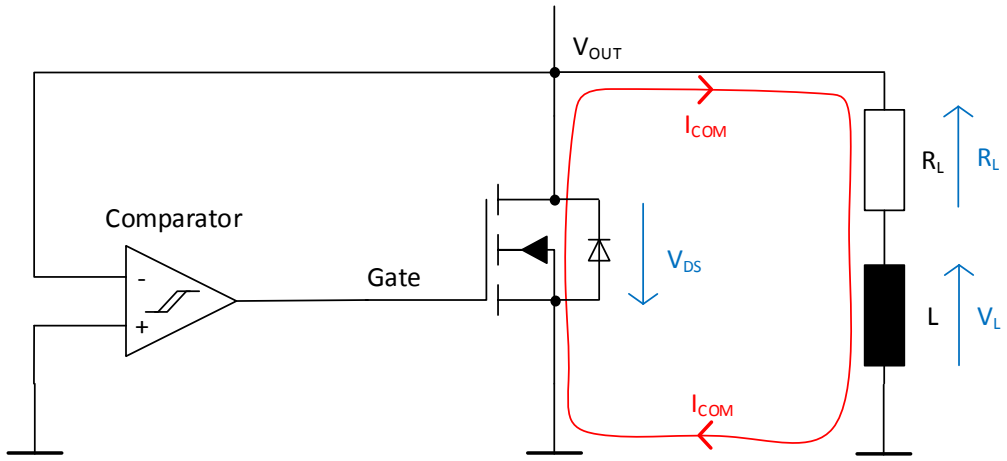


Figure 4.16: *Below GND protection concept*

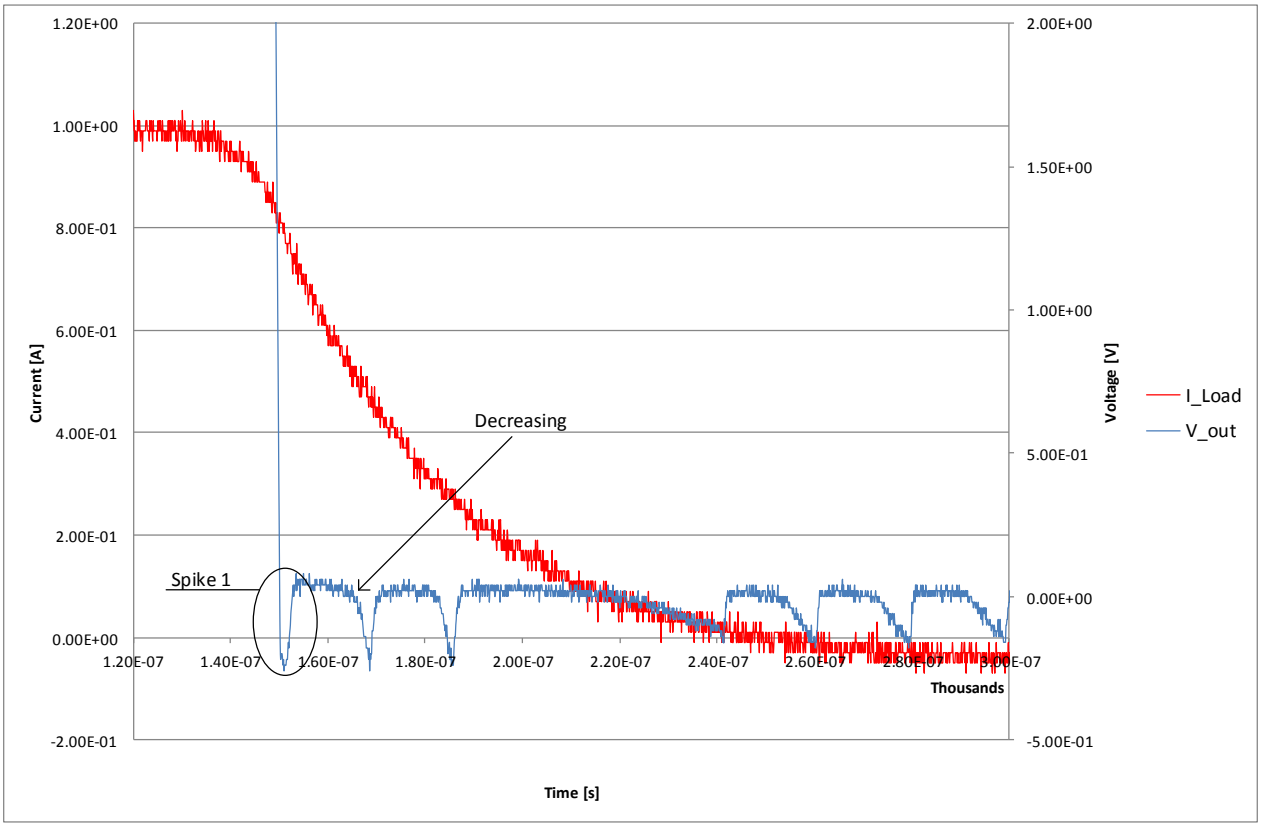


Figure 4.17: *Detailed illustration of the below GND protection*

4.2.2 Temperature behaviour

Semiconductors as diodes and bipolar transistors, are sensitive against temperature changing, therefore the changing temperature has influence on the voltage and current behaviour. The reason therefore is, that the charge carriers collide more often with increasing temperature and this leads to a less charge carrier mobility. Although, for a bipolar transistor this means, with increasing temperature, more charge carrier are available, which leads to a higher conductivity and a higher reverse current. In addition, with increasing temperature the resistance in forward direction gets smaller, which leads to a decreased threshold voltage. For this reason, it is necessary to evaluate the temperature dependency of the parasitic NPN transistor and further, the influence of the temperature dependency has on the below GND protection. The application consideration in this master thesis, is for automotive applications. Therefore, semiconductors in automotive application has to be fully functional from -40°C to 150°C. Primary, the relation between the collector current I_C, the base emitter voltage V_{BE} and its dependency of the temperature matters. The reason therefore, is the temperature dependency of the saturation reverse current I_S and the thermal voltage V_T (26mV at room temperature).

$$I_C(V_{BE}, T) = I_S(T) \cdot e^{\frac{V_{BE}}{V_T(T)}} \cdot (1 + \frac{V_{CE}}{V_A}) \tag{4.10}$$

$$V_T(T) = \frac{kT}{q} \tag{4.11}$$

$$I_S(T) = I_S(T_0) \cdot e^{(\frac{T}{T_0(T)} - 1)\frac{V_G(T)}{V_T(T)}} (\frac{T}{T_0})^{x_{T,I}} \tag{4.12}$$

k...Boltzmann constant $[\frac{J}{K}]$

q...Elementary charge $[C]$

$x_{T,I} \approx 3$

V_G...Bandgap voltage (0.7V of Silicon) $[V]$

V_A...Early voltage $[V]$

Basically, the temperature dependency of the bandgab voltage V_G is very small that it can be negligible. For more information about the temperature dependency in MOS transistors, consider [7].

In the case of the parasitic NPN transistor the base emitter diode, which is basically the body diode of the NLDMOS, is the trigger for the activation of the parasitic NPN transistor. Therefore the temperature dependency of the base emitter voltage was characterized, in practice and also in the literature, the temperature dependency of the base emitter voltage is written in formula 4.13. But this is not the absolute real value, as shown in formula 4.14, but for the characterisation in this master thesis, -2mV/K where used.

$$\frac{dV_{BE}}{dT} = -2\frac{mV}{K} \tag{4.13}$$

In figure 4.18, the temperature dependency with two constant I_C currents is illustrated and it can be seen the difference in the V_{BE}, furthermore, the common V_{BE} is the point where the temperature reaches the absolute zero ($-273°C$).

$$\frac{dV_{BE}}{dT} = \frac{V_{BE} - V_G - 3V_T}{T} \approx -1.7\frac{mV}{K} \tag{4.14}$$

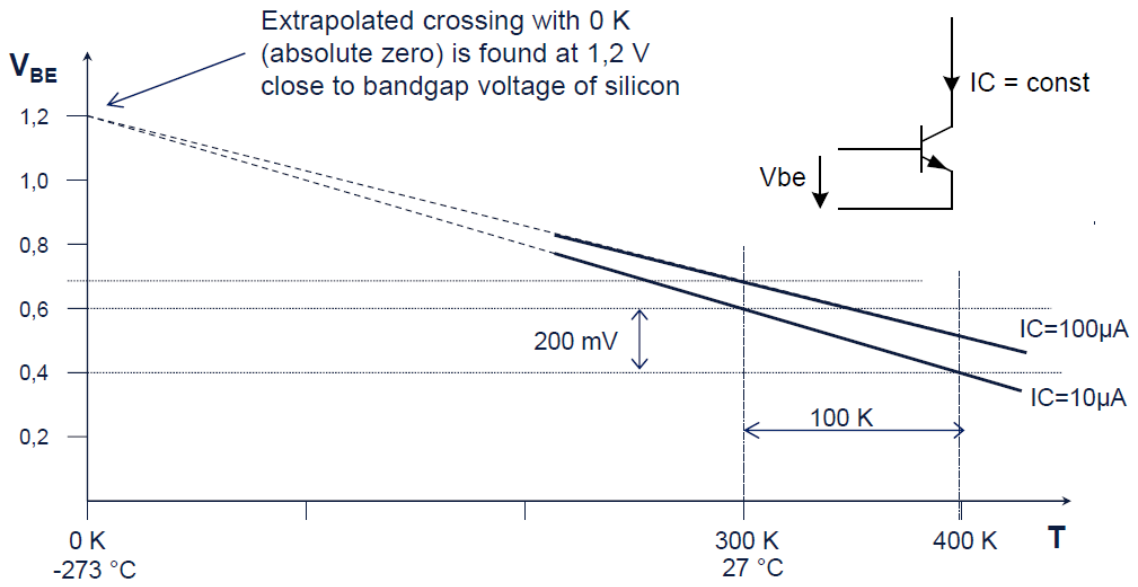


Figure 4.18: *Base Emitter voltage in dependency of the temperature [4]*

As already mentioned, the V_{BE} decreases with -2mV/K, so it has a negative temperature coefficient, this means, that the parasitic NPN transistor gets active with a lower V_{TH} at hot temperature. There is another drawback, which depends also on temperature like the V_{BE}. If the below GND protection switches on the channel of the NLDMOS, it has a channel on - state resistance, called R_{DS}, and a resistor is also temperature dependent, it has a positive temperature coefficient. The temperature dependency is illustrated in formula 4.15, where the consideration of the linear temperature coefficient is sufficient and the second order effect can be neglected.

$$R(T) = R_0(1 + TC1 \cdot \Delta T + TC2 \cdot \Delta T^2) \tag{4.15}$$

$$R_0 ... \text{Resistance at room temperature} \, [\Omega]$$
$$TC1 ... \text{Linear temperatur coefficient} \, [K^{-1}]$$
$$TC2 ... \text{Quadratic temperatur coefficient} \, [K^{-1}]$$
$$\Delta T = (T - T_0)$$

Taking the observation, of the negative temperature coefficient, from the V_{BE} of the parasitic NPN transistor and the positive temperature coefficient, of the channel resistance R_{DS} from the NLDMOS, into account. There is a criteria which has to be fulfilled against the activation of the parasitic NPN transistor at hot temperature, shown in formula 7.1.

$$V_{DS} < V_{BE} \tag{4.16}$$

$$where: \qquad V_{DS} = I_{DS} \cdot R_{DS} \tag{4.17}$$

To see, how the values concerning the temperature dependency are changing, the following calculations where done.

$$Room\ temperature: \qquad 300K = 26.85\,^{\circ}\text{C} \tag{4.18}$$

$$Hot\ temperature: \qquad 423.15K = 150\,^{\circ}\text{C} \tag{4.19}$$

The V_{BE} decreases with -2mV/K, which turns out that the threshold voltage V_{TH} for hot temperature (150°C) is 246.3mV lower. For a 0.7V (Silicon) at room temperature, this turns out at hot temperature:

$$V_{TH(HOT)} = 453mV \tag{4.20}$$

On the other side, the channel resistance R_{DS} of the NLDMOS is increasing with increasing temperature, at hot temperature (150°C). The measurements and calculations at 150°C turning out an R_{DS} of 44.2mΩ. With the temperature coefficient of 0.00657K^{-1} [8] as well as the resistance at room temperature R_0, which is basically the resistance R_{DS} at room temperature and which is 25mΩ, it is possible to calculate the resistance at 150°C. Therefore, formula 4.15 this turning out:

$$R(150\,^{\circ}\mathrm{C}) = 25m\Omega(1 + 0.00657K^{-1} \cdot (150\,^{\circ}\mathrm{C} - 27\,^{\circ}\mathrm{C})) = 45.2m\Omega \tag{4.21}$$

As seen, the calculation in 4.21, with 45.2mΩ and the measurements from the lab with 44.2mΩ, equals very well. For further considerations the value of 44.2mΩ where used. Consider the criteria which is shown in 4.16, two examples with a different current I_{DS} are shown in formula 4.22 and 4.23.

$$V_{DS(HOT)} = I_{DS} \cdot R_{DSHOT} = 3A \cdot 44.2m\Omega = 132.6mV \tag{4.22}$$

$$V_{DS(HOT)} = I_{DS} \cdot R_{DSHOT} = 10A \cdot 44.2m\Omega = 442mV \tag{4.23}$$

For the equation 4.22, the criteria 4.16, with a I_{DS} of 3A at 150°C, is fulfilled.

$$132.6mV < 453mV \tag{4.24}$$

For the equation 4.23, the criteria 4.16, with a I_{DS} of 10A at 150°C, is theoretically fulfilled. But in practice, there is a scattering, which can violate the criteria. Furthermore also the current can be higher, especially the stalling current to break down the motor and this can also violate the criteria.

$$442mV < 453mV \tag{4.25}$$

Chapter 5

Concept and Design Development

In the previous chapter, the existing product test chip was characterized, especially its behaviour concerning the below GND event. In more detail this means, the parasitic NPN transistor in stand - alone configuration and the below GND protection in the existing product. This chapter will cover the second part of this master thesis, which is mainly the development of the existing protection function with zero stand - by current. For this reason, the first step was to create the concept in a way, where the requirement can be fulfilled, without any limitation in the below GND protection.

5.1 State Diagram

Figure 5.1 shows the state diagram of the concept of the below GND protection. First of all, it has to be mentioned, that in zero standby condition, there is no internal supply voltage V_{DD} available. Therefore, as shown in the state diagram 5.1, there are two parts to fulfil the below GND protection. The first part, framed in the green dashed line, ensures that the NLDMOS gets immediately switched on, if the output voltage V_{OUT} node gets below GND. This is needed, because if there is no internal supply voltage V_{DD} available, there is no protection function available. Therefore, the immediately activation of the NLDMOS is needed to accumulate the current through the NLDMOS channel. The reason, why this is occurring only once, at the same time, the internal supply voltage V_{DD} for the below GND comparator will be generated and therefore the below GND comparator can handle the below GND event. In the second part, framed in the blue dashed line, the trigger event is the same as for the first part. If the output voltage V_{OUT} node gets below GND, this generates an internal supply voltage V_{DD} for the below GND comparator, which has the same function as in the existing product test chip. Particularly mentioned should be the delay block, which is necessary to keep the internal supply voltage V_{DD} for a certain time at a certain voltage level, that the below GND comparator and can sense the output voltage V_{OUT} and work correctly. Therefore, the second part framed in the blue dashed line is self generating, as long there is a below GND event. Because, if the below GND comparator have its internal supply voltage V_{DD}, after the first below GND event, it generates its internal supply voltage V_{DD} itself, with every occurring below GND event. Furthermore, the zero standby current is fulfilled, because there is only a supply current needed in case of the activation of the below GND protection. In the next chapters, a detailed explanation of the blocks, shown in figure 5.1, is given.

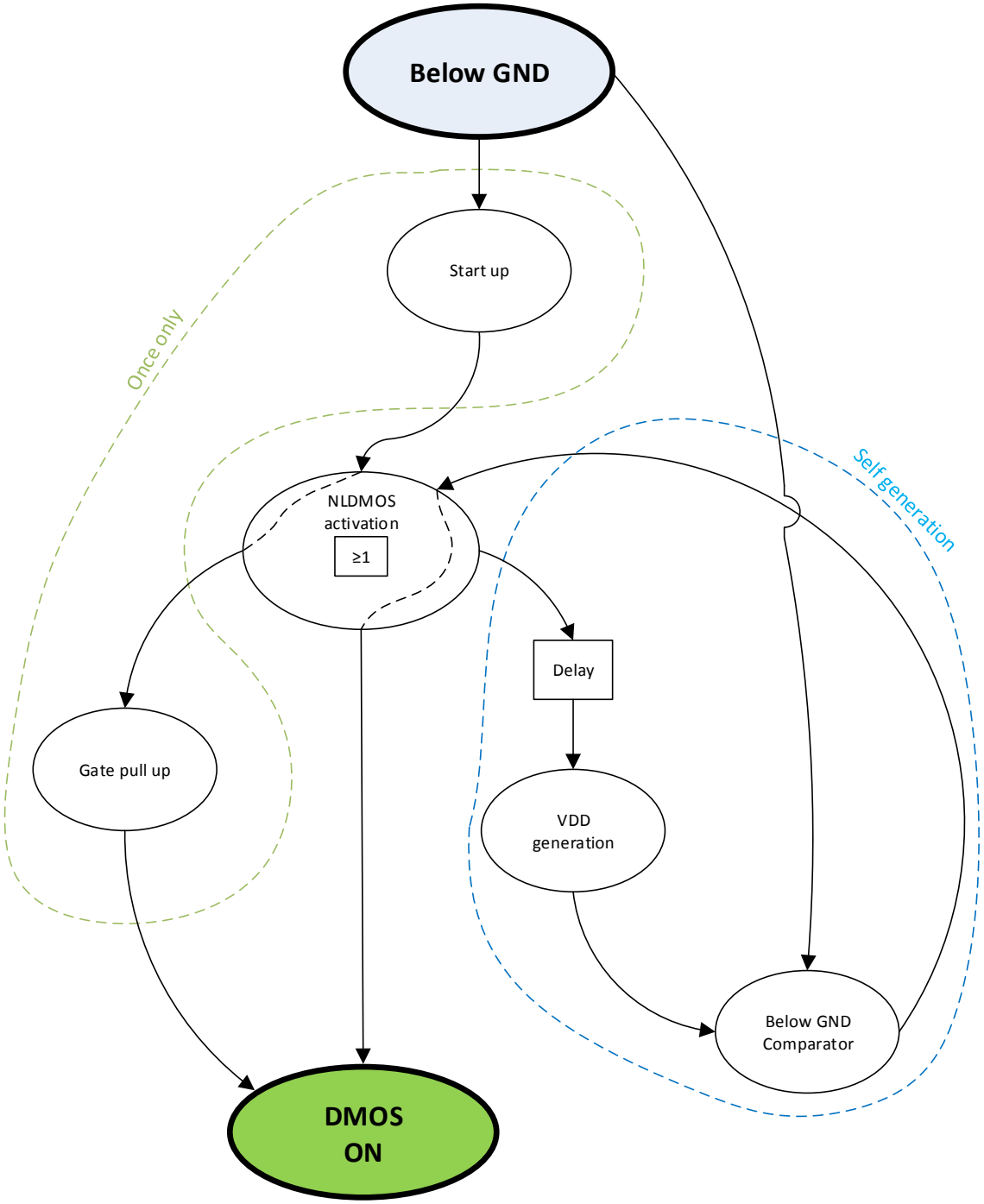
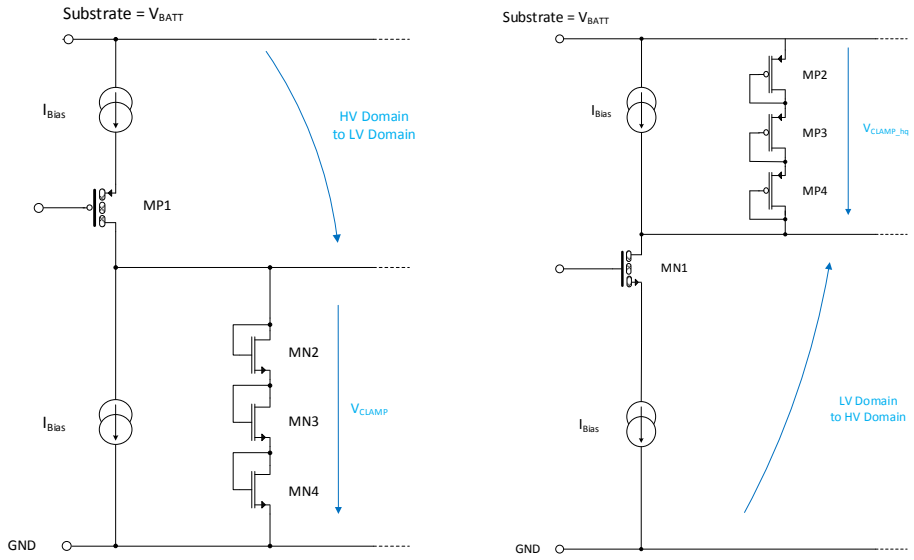


Figure 5.1: *Concept state diagram for the below GND protection with zero stand-by current*

5.2 Voltage Domain

First of all, as already mentioned, there is no internal supply voltage V_{DD} in the range of 3.3V available. However, the battery voltage, which is fixed to the substrate, is available constantly and as already noted in chapter 2, the voltages in a 12V battery car net, can reach 60V an more. Therefore, high voltage (HV) devices are needed to withstand voltages above 7V or separate the low voltage (LV) devices from the high voltage, also called high voltage domain and low voltage domain. For the sake of completeness, there is also a medium voltage domain, which is in between 3.3V and 7V, but for the design in this master thesis no medium voltage devices where needed. For the reason, that there is no V_{DD}, a shift between the high voltage domain and the low voltage domain is needed.



(a) *Changing from HV domain to LV domain* **(b)** *Changing from LV domain to HV domain*

Figure 5.2: *Changing within the voltage domains*

5.3 V_{OUT} Sensing Circuit

To detect a below GND event, a circuitry which senses the output voltage V_{OUT} is needed. In figure 5.3, the transistor MN1, together with the current source I_{REF}, acts as a source follower which is switched on if the output voltage V_{OUT} gets negative. If the V_{OUT} gets negative, the sense V_{OUT} node, which is basically the source contact of MN2, follow the V_{OUT} signal. Because of the reason, the source of MN2 follows the negative voltage of the V_{OUT}, its generates a V_{GS} and at the threshold voltage of MN2, it get switched on. Therefore, the HV PMOS current mirror gets activated and a current I_M can flow and will be mirrored. The NMOS transistor MN3, MN4 and MN5 are basically the clamping chain, in MOS diode configuration. The transistor MP2, the current source I_M and the clamping chain, shift the voltage from the high voltage domain to the low voltage domain and clamp the wakeup_l node to the clamping voltage V_{CLAMP}, which is approximately 3.3V.

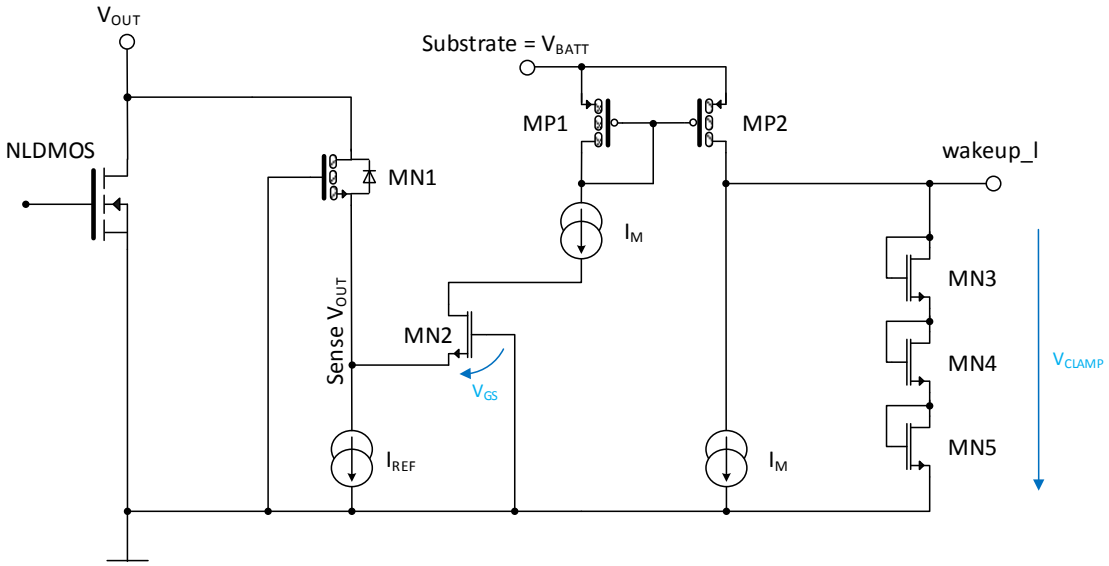


Figure 5.3: *V_{OUT} sensing for activating the start up*

Shown in figure 5.4, is the sense V_{OUT} which follows the actual ouput voltage V_{OUT}, further the wakeup_l node, which is basically the clamping voltage V_{CLAMP} of the MOS diode chain. What should be noted is, that the time between the detection of the below GND event and a low V_{CLAMP}, is lower than 1us. Which leads to the fact, that within this time interval, the NLDMOS has to switch on and the internal V_{DD} has to be generated.

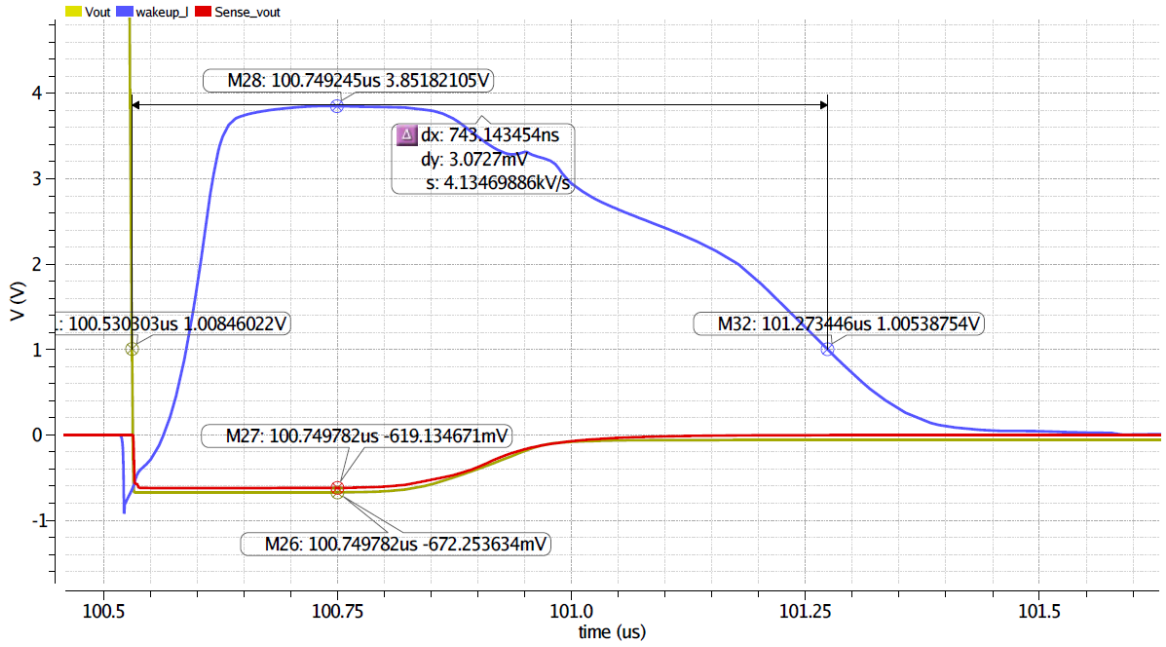


Figure 5.4: *V_{OUT} sensing plot*

5.4 NLDMOS Gate Pull - Up

A main difference in the design of a highside switch and a lowside switch is, that the lowside switch does not need a charge pump to control the gate of the DMOS. Because the source of a lowside switch is connect to the GND potential, it is only necessary to reach the V_{TH}, of the transistor to switch it on. Thus, the miss of the V_{DD} is still present, the immediate pull up of the Gate to switch on the NLDMOS, is implemented with a levelshifter, to switch between the HV domain and the LV domain, as shown in figure 5.5.

The wakeup_l signal is generated by the start up activation shown in figure 5.3, which will switch on the transistor MN1 and MN2. By switching on MN1, the Start_up_hq node gets pulled down and gets clamped by the three PMOS diode voltages V_{CLAMP_HQ}, below substrate voltage, which is the battery voltage. The Start_up_hq is a high side signal, characterised by the "hq", which is used to switch on the high voltage PMOS MP1. As already mentioned, the time interval for the start up sequence is less then 1us. In figure 5.6, the signals of the start up circuit are shown. It can be seen, that with the signal wakeup_l, the Start_up_hq node gets pulled down and the Gate potential of the NLDMOS is increasing.

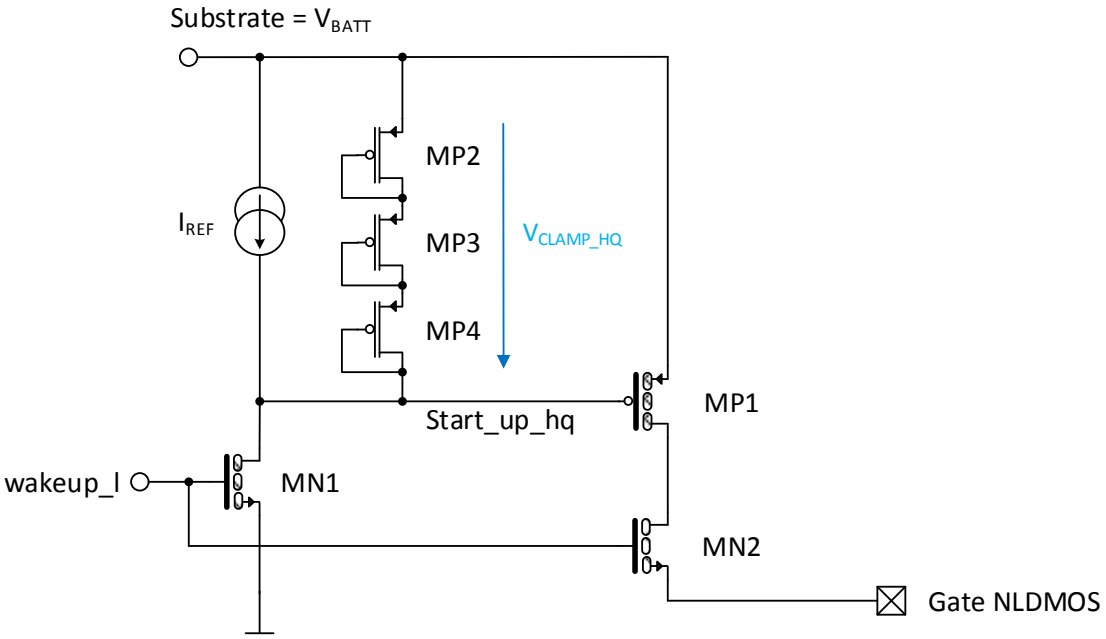


Figure 5.5: *Pull up circuit for the Gate of the NLDMOS*

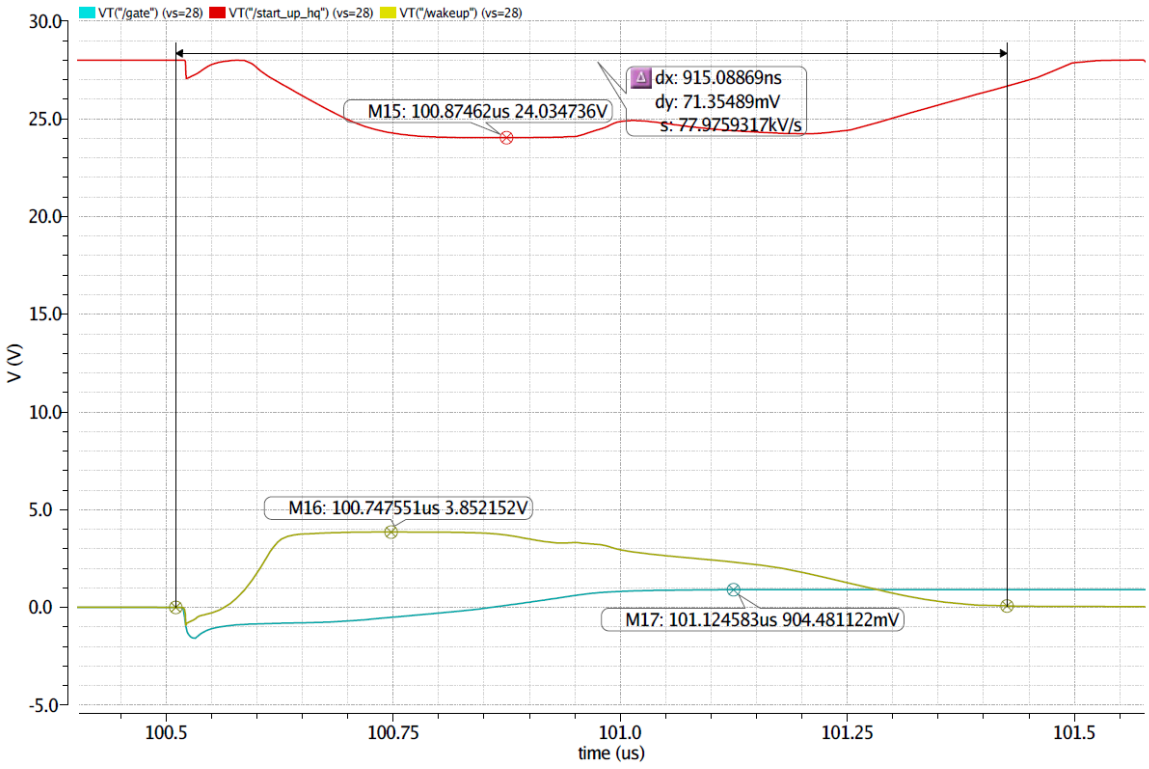


Figure 5.6: *Plot of the Gate pull up circuit*

5.5 Internal Supply Voltage (V_{DD}) Generation

For the V_{DD} generation, the below GND event is the actual trigger, but the V_{DD} generation is separated into two trigger events. The first was already discussed, it is the wakeup_l signal from the V_{OUT} sensing circuit, shown in chapter 5.3. The second trigger will be generated from the below GND comparator. In figure 5.7, the concept of the V_{DD} generation is shown, where within the green dashed line the first trigger signal (wakeup_l) and within the blue dashed line the second trigger, which is the blgnd_l signal from the below GND comparator are shown. As it can be seen, both signals, the wakeup_l and the blgnd_l, act as an input for the levelshifter to generate the Start_up_hq signal, therefore the levelshifter even includes an OR - decision. As already mentioned, the wakeup_l signal is used to switch on the NLDMOS immediately and furthermore in the short time interval where the wakeup_l is active, it initials the internal supply V_{DD}, as shown in figure 5.7. This activation of the internal supply voltage V_{DD} via the wakeup_l happens only once. If the V_{DD} is active, the below GND comparator is able to sense the output voltage V_{OUT} and switch on the NLDMOS controlled and furthermore it generates the signal blgnd_l, which sets the trigger for the internal supply voltage V_{DD} generation. Also seen in figure 5.7, a delay circuit block is implemented. The reason therefore is, if the below GND comparator has to work autonomous as long as the output voltage V_{OUT} is below the threshold voltage of the below GND comparator, it needs a V_{DD}. If no delay circuit block would be implemented, the below GND comparator would only work, only as long the first trigger (wakeup_l) is active, and it would not be possible to switch on the NLDMOS again. Therefore, the time delay of the delay circuit block, has to be set to the value that the below GND comparator has its V_{DD} to sense the V_{OUT}. So it can detect a below GND event and generate the second trigger (blgnd_l) as well as switch on the NLDMOS. Therefore, this process is self generating as long the V_{OUT} is below the threshold of the below GND comparator.

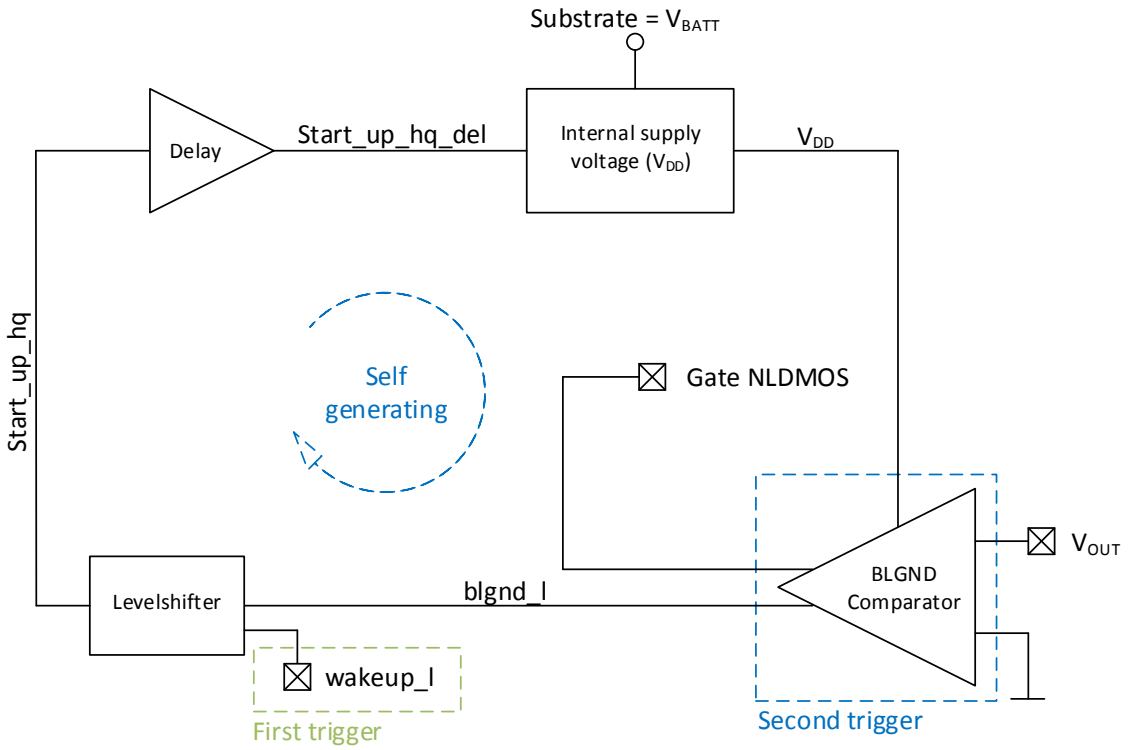


Figure 5.7: *Concept of the V_{DD} generation*

In figure 5.8, the signals of the V_{DD} and its trigger signals wakeup_l and blgnd_l are shown. It can be seen, that the delay signal Start_up_hq_del, which is generated by Start_up_hq, is longer active in terms of time, to ensure the active V_{DD}. Further, it can be noticed, that the wakeup_l signal is only once active for a short amount of time, but in this short amount of time it is possible to immediately pull up the gate of the NLDMOS and generate the internal supply voltage V_{DD}.

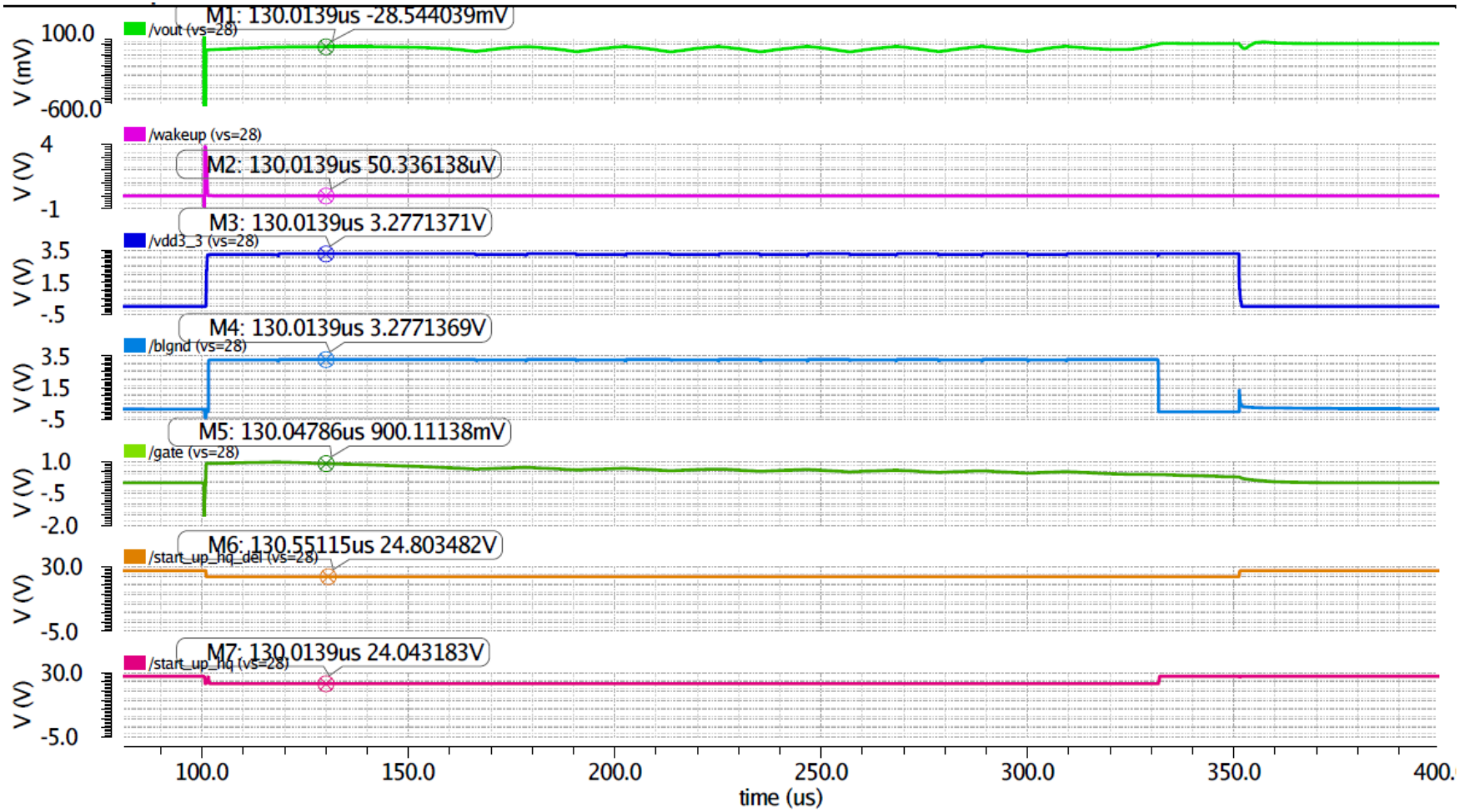


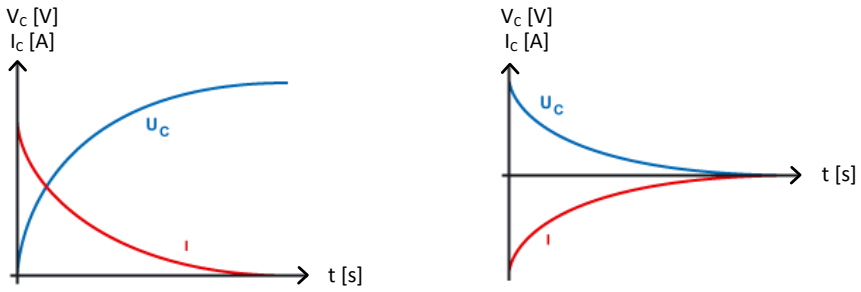
Figure 5.8: *Plot of the V_{DD} with its trigger signals*

5.5.1 Delay Circuit Block

As in the previous chapter already mentioned, the delay circuitry is needed to keep the internal supply voltage V_{DD} active for a certain time, where the below GND comparator is active and is able to sense the output voltage V_{OUT}. In other word this means, the V_{DD} has to stay at a certain level, for a defined time, therefore the delay is realised with a capacitor.

5.5.2 Switching behaviour of a Capacitor

In this section, a short treatment of the switching behaviour of a capacitor, especially the charging and discharging phase, is given. In figure 5.9, the ideal charging behaviour of a capacitor is shown. Figure 5.9 (a), shows the charging phase, with the increasing voltage and the decreasing current, and figure 5.9 (b), shows the discharging phase with its decreasing voltage and decreasing current.



(a) *Voltage and current curve of charging a capacitor [9]*

(b) *Voltage and current curve of discharging a capacitor [9]*

Figure 5.9: *Charging and discharging behaviour of a capacitor*

Figure 5.10, shows the time dependency of the charging- and discharging- voltage of the capacitor. The time constant can be calculated as shown in formula 5.1 and as in literature explained, after 1T the capacitor voltage is 63% of the voltage applied and after 5T the capacitor is nearly full charged or discharged. The voltage and the current in a capacitor can be calculated as shown in formula 5.2 and formula 5.3. Basically, the charging as well as the discharging of a capacitor is depending on the current applied. The quotient of voltage and current results in the resistance, which together with the capacitor, is defining the time dependency of the charging and discharging of a capacitor. For example, the internal resistance of an ideal voltage source is zero and the internal resistance of an ideal current source is infinity. If this considerations will be applied in formula 5.1, this will results in a Tau of zero. Which means the capacitor is infinitely fast charged or discharged and this is not possible, because nothing is infinitely fast.

$$T = R \cdot C = \frac{U \cdot C}{I} \tag{5.1}$$

$$i(t) = C \cdot \frac{dv(t)}{dt} \tag{5.2}$$

$$v(t) = \frac{1}{C} \cdot \int_{t1}^{t2} i(t)dt \tag{5.3}$$

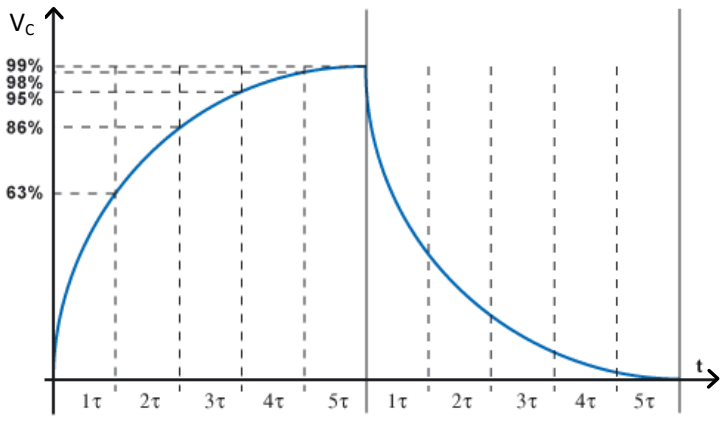


Figure 5.10: *Time dependency of the charging and discharging phase [9]*

5.5.3 Delay Circuit

In figure 5.11, the schematic of the delay circuit is shown, the signal Start_up_hq should have a delay, which is the input and activation of the internal supply voltage V_{DD}. If the PMOS MP1 is switched on, the capacitance C_{DEL} get charged with the constant current source I_{Charge} up to the voltage V_{Clamp}. If the threshold Voltage V_{TH} of the transistor MN1 is reached, it will be switched on and clamps the signal Start_up_hq_del to the voltage $V_{Clamphq}$. If the signal Start_up_hq gets disabled, or below the threshold voltage of MP1, the value of the capacitance C_{DEL} and the discharge current $I_{Discharge}$ have to be set to a value, that the voltage V_{Clamp} never gets below the threshold voltage of MN1, until the next Start_up_hq signal is switching on the transistor MP1. This process, is repeating as long as the below GND comparator is detecting an output voltage V_{OUT} and is finished if the output voltage V_{OUT} is above the threshold of the comparator. After the process is finished, the capacitance C_{DEL}, gets discharged via the current source $I_{Discharge}$. Therefore, to fulfil the delay, a capacitance of 1pF was chosen.

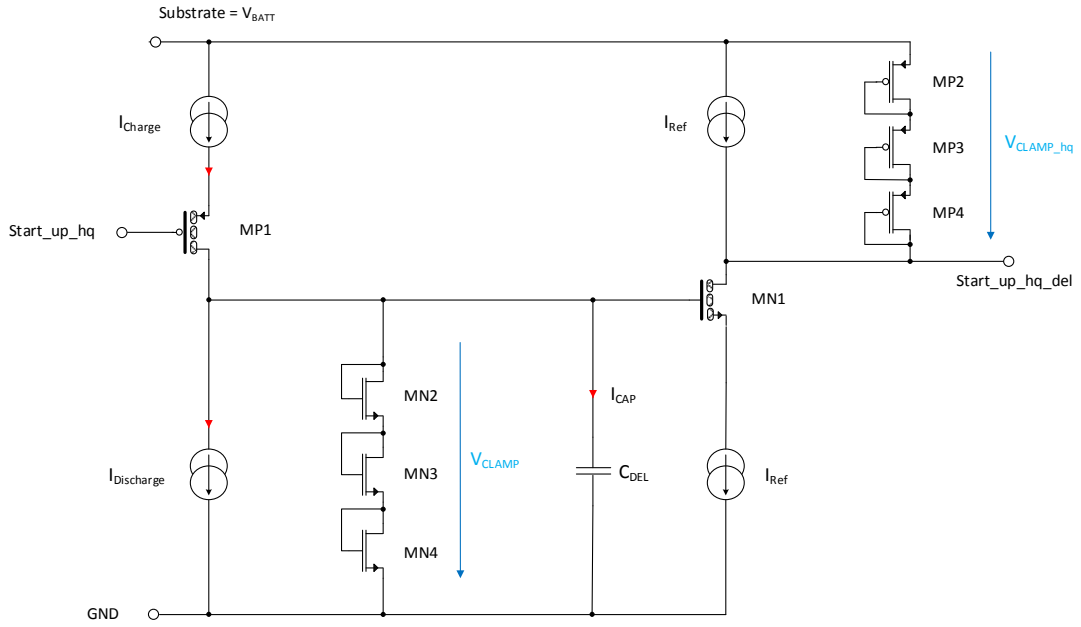


Figure 5.11: *Schematic of the delay circuit*

Illustrated in the plot 5.12, is the charging of the delay capacitance C_{DEL} and the discharging of the delay capacitance C_{DEL}. In the charging phase, it can be seen, that the current is decreasing until the capacitance is charged to the defined voltage. In the discharge phase of the delay capacitance, the current I_{cap} starts immediately with a negative sign to discharge the capacitance, but only to the value of discharging current $I_{discharge}$ from current source, therefore the values of the I_{cap} and $I_{discharge}$, are nearly the same, apart

from the sign. Via the current source $I_{discharge}$, the delay capacitance can be discharged by a defined current, which defines the delay time.

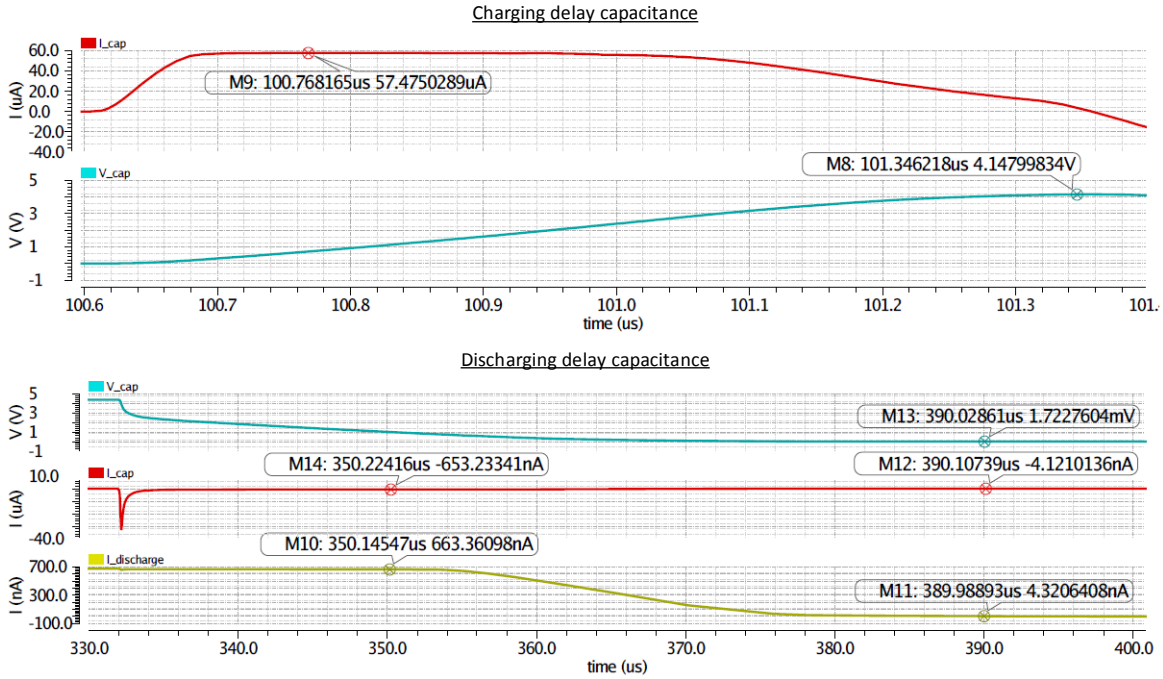


Figure 5.12: *Plot of the charging and the discharging phase of the delay capacitance*

5.5.4 Internal Supply Voltage Circuit

As in the previous section described, the delay circuit is necessary to keep the delay signal Start_up_hq_del at a certain level for a defined time, that the internal supply voltage is active. In this section the internal supply voltage block is described, figure 5.13, shows the schematic of the V_{DD} block. If the Start_up_hq_del switch on the transistor MP1, the potential of node_a is clamped to the voltage V_{Clamp}, which is basically three diode voltages above GND, depending on MN2, MN3, MN4. The need of the capacitance C_S, is basically to ensure a stable clamping voltage V_{Clamp} at node_a, furthermore, this leads to a stable gate potential at MN5, which is node_b. The potential of node_b is another diode voltage above V_{Clamp}, thus the transistor MN1 is a high voltage device, it has a higher threshold voltage, therefore the voltage at node_b is around 4.9V. This is necessary, because, if the transistor MN5 gets switched on, its source, get pulled up to V_{DD}, this is approximately 3.3V. To ensure that MN5 is always in saturation, the gate voltage was set higher, to ensure a V_{GS}, above the threshold voltage V_{TH}. Of course, if the transistor MN5

get switched on, the channel has a resistance, R_{DS}, which leads to a voltage drop. The internal supply voltage V_{DD}, is defined by the voltage drop over the channel resistance.

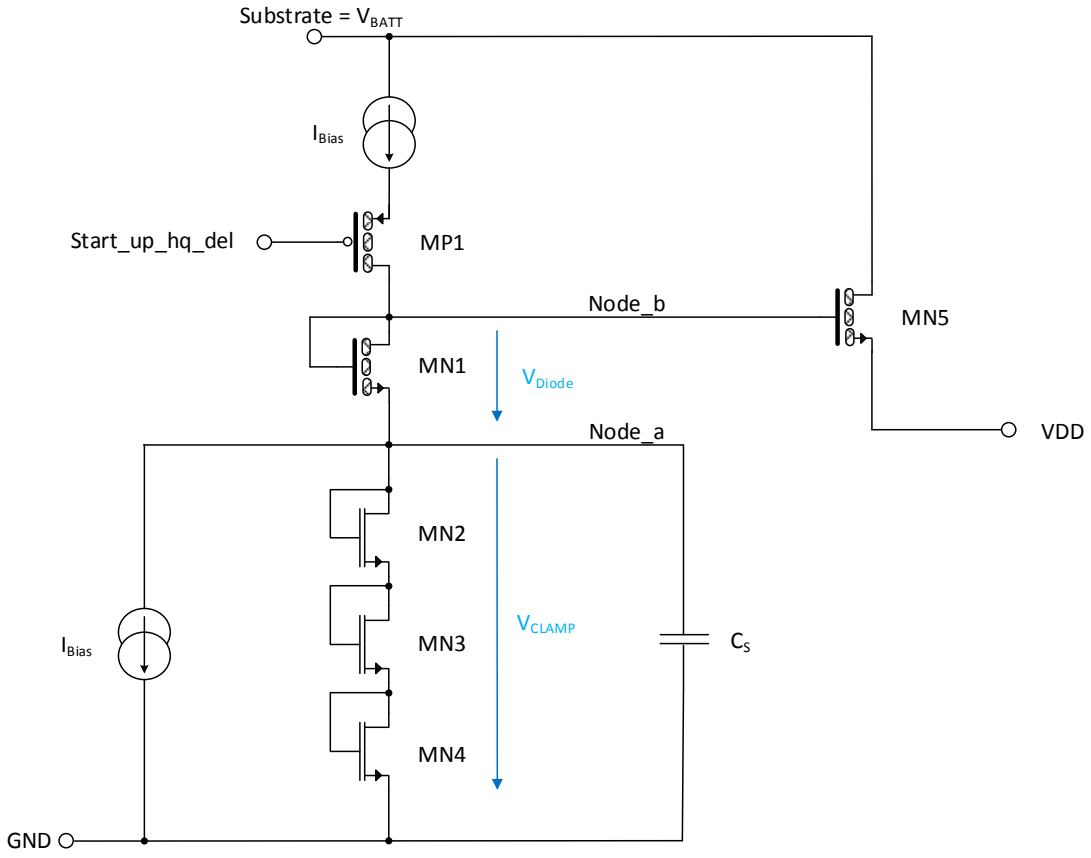


Figure 5.13: *Schematic of the internal supply generation*

Illustrated in figure 5.14, is the plot of the V_{DD} generation block. It can be seen, that the V_{DD} is active, as long as the signal Start_up_hq_del is active. In addition, the voltage of node_a and the voltage of node_b are shown. Which also can be noticed, is that the V_{DD} has a small variation in its voltage value. The variation occurs because at the lower value of the V_{DD}, the below GND protection is active and this leads to a higher internal current consumption.

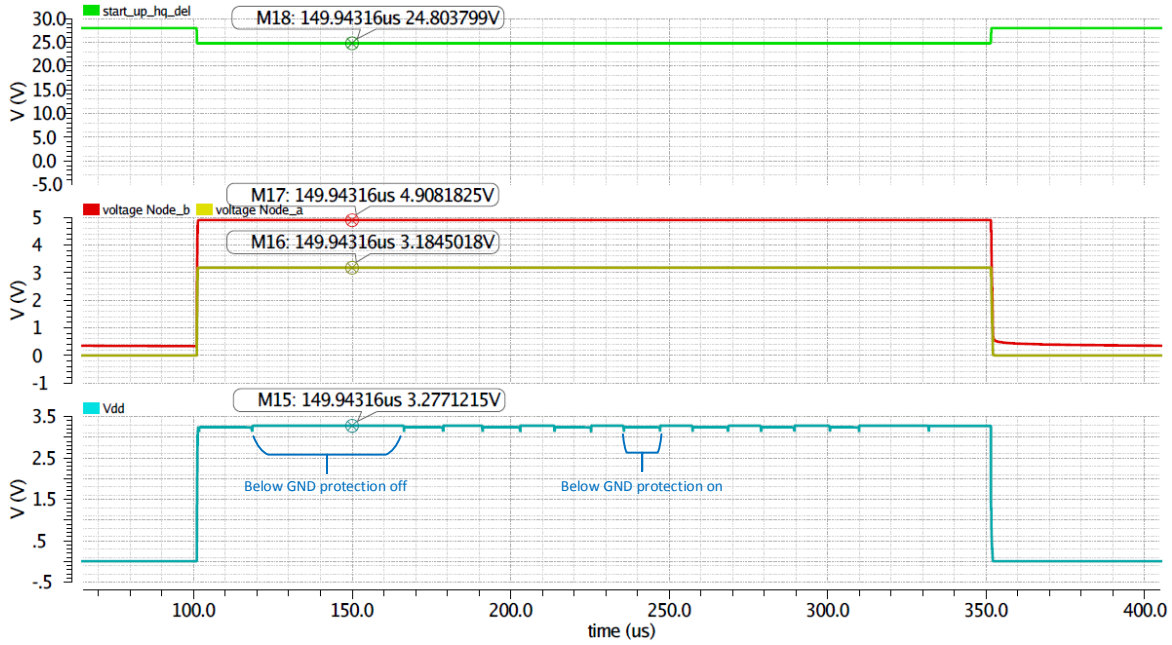
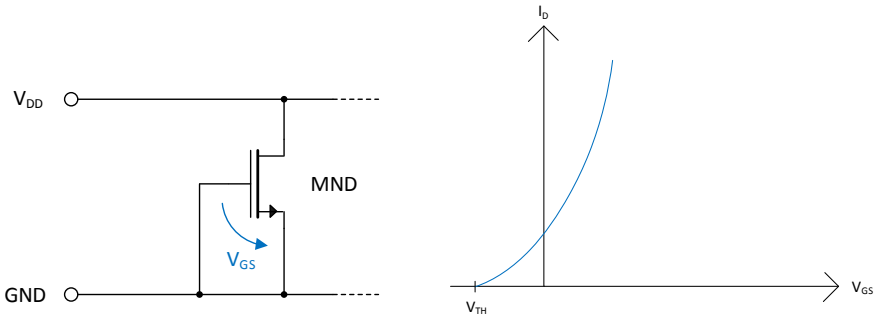


Figure 5.14: *Plot of the internal supply voltage generation*

5.6 Below GND comparator

As already mentioned, the start up circuit, which generates the signal wakeup_l , is the major initiator and the first trigger for the activation of the protection and the generation of the internal supply voltage V_{DD}. If the below GND comparator has its V_{DD}, it is actually the main block for the below GND protection, therefore, this chapter covers the functionality of the below GND comparator.

In figure 5.16, the schematic of the below GND comparator is shown. The output voltage V_{OUT}, is sensed via the input transistors MND1, MND2 and MND3. The transistor MN1 is a high voltage blocker, as the name already says, MN1 is used to block the high voltage from the low voltage devices. The input stage, which are the three transistors MND1, MND2, MND3, are N-channel depletion transistors, which means, they have a negative threshold voltage V_{TH}. This means, at a zero gate source voltage V_{GS}, the transistor is already switched on and a current is flowing. In figure 5.15 (a), the schematic of a single depletion transistor is shown, where, the gate source voltage V_{GS}, is zero. Furthermore, in 5.15 (b), the input characteristic is illustrated, where it can be seen that the depletion transistor has a negative threshold voltage and that at zero V_{GS}, a current is flowing.



(a) *Schematic of the depletion transistor* **(b)** *Input characteristic of the depletion transistor*

Figure 5.15: *Depletion transistor behaviour*

Thus, the depletion transistor has a negative threshold voltage, it is quite useful for the below GND detection. A closer look to the schematic in figure 5.16, shows that if no below GND event is detected, the depletion transistor MND1 has a constant current of 1uA, because its gate is connected to GND. Thus, there is no below GND event, also the depletion transistors MND2 and MND3 have constant current, in the branch of MND2 a current of 900nA is flowing and in the branch of MND3 100nA are flowing. Therefore the input stage has a constant current consumption of 2uA. Furthermore, considerations are showing, if there is no below GND event, that transistor MP4 is on, because its gate is pulled down. This leads to the activation of MN2, which is pulling down the gate of the NLDMOS with the current source $I_{DISCHARGE}$. Furthermore, if MP4 is switched on, the MN3 is also switched on and pulls the below GND trigger signal to GND, which means the output voltage is not below GND potential.

Let's assume, the output voltage gets below GND potential and as already mentioned, the depletion transistor MND1, MND2, MND3 have a negative threshold voltage. Therefore, the transistor MND2 and MND3, which are sensing the output voltage V_{OUT}, getting more to the point where they get switched off by the decreasing of the output voltage. In fact, this also leads to a decrease in the current flow through transistor MND2 and MND3. But, the amount of the current consumption, which is 2uA, has to stay the same. Therefore, via the depletion transistor MND1 has to flow the rest of the current. Further, if MND2 and MND3 are switched off, also MP4 is switched off, this further leads to the fact that MN2 switches off and MP5 switches on, which charges the gate of the NLDMOS to switch it on. Furthermore, if MP4 is off, this leads to the fact, that MP6 is switched on, which sets the below GND signal to high, means to V_{DD}. Via the feedback path, MP3 gets switched off, this path is basically for the hysteresis. Here also the trigger for

the self generation of the internal supply voltage V_{DD}, can be seen, which is basically the below GND signal.

To set the needed threshold of the comparator, which is a negative one, the matching of the depletion transistors MND1, MND2, MND3 has to be balanced. This can be achieved with the correct width of the depletion transistor MND1, MND2, MND3 or also by setting more equivalent devices in parallel. In the case for the below GND comparator, there MND1 are 5 equivalent devices in parallel, for MND2 are 6 equivalent devices in parallel and for MND3 there are 3 equivalent devices in parallel.

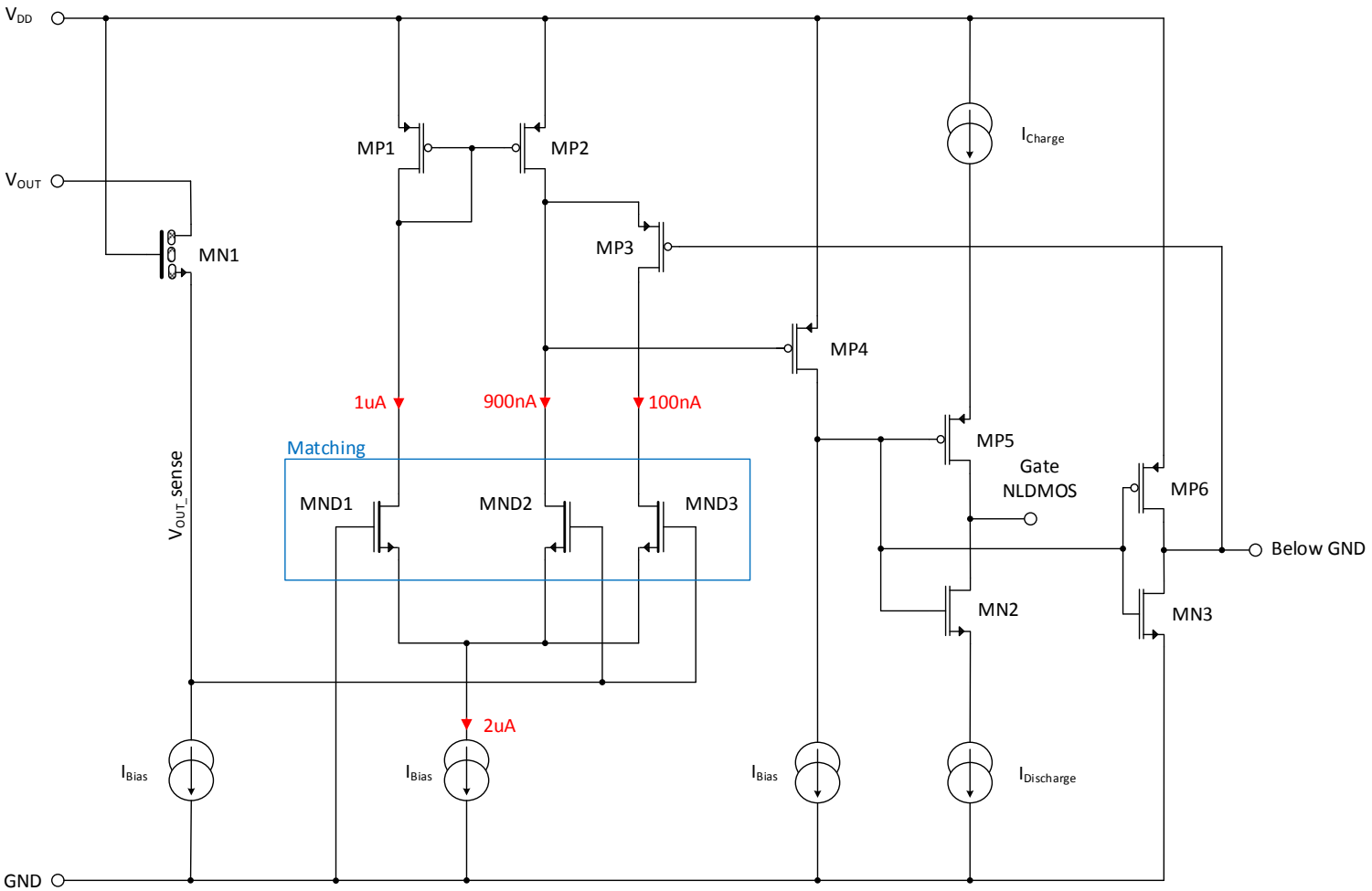


Figure 5.16: *Schematic of the below GND comparator*

To illustrate the behaviour of the below GND comparator a single test bench only for the below GND comparator was made. With the test bench it is possible to set the threshold of the comparator as well as the current consumption of the comparator. For the understanding of the behaviour, the sweep of a slow (3ms) output voltage V_{OUT} where used.

Figure 5.17, shows the plot of the current consumption by the changing of the output voltage V_{OUT}. It can be seen, that above the threshold voltage of the below GND comparator, the current consumption is 1uA via MND1, around 900nA via MDN2 and 100nA via MND3. If the threshold of the below GND comparator is triggered, this leads to a increasing current via MND2 and a decreasing current in MND2 and MND3 and it can be observed that the total current stay the same. The same behaviour can be observed, if the output voltage V_{OUT}, is increasing, this leads to a decreasing current via MND1 and a decreasing via MND2 and MND3.

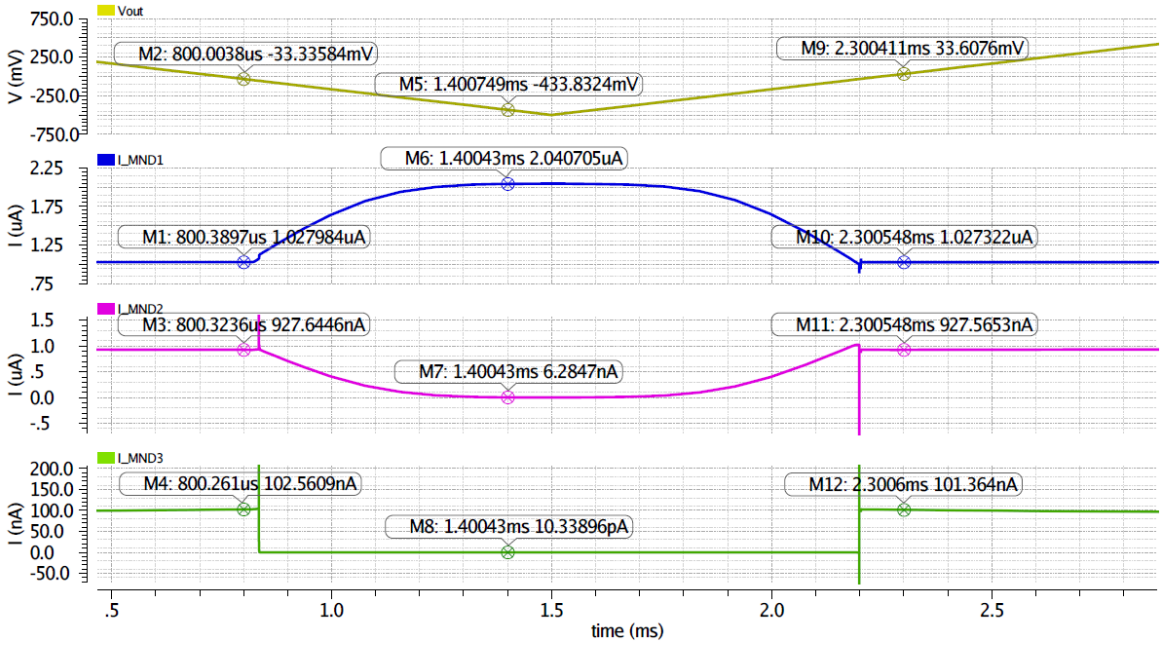


Figure 5.17: *Current consumption of the input structure of the below GND comparator*

As already mentioned, the below GND comparator has a hysteresis, which is needed to sense the output voltage V_{OUT}, over the whole discharge phase of the inductance. Basically, the hysteresis is defined via an additional current path from the transistor MP3. If the transistor MP3 is not active, which means the below GND signal is not active, the additional current can flow. On the other hand, if the output voltage V_{OUT}, gets below the threshold of the below GND comparator, the below GND signal is active, which switch off the transistor MP3 and therefore this current path is not active any more.

Figure 5.18, shows the threshold of activating the below GND signal, which is in the range of -56mV of the output voltage V_{OUT}. Furthermore, in figure 5.19, the threshold of deactivating the below GND signal is shown, which is in the range of -34mV of the output voltage V_{OUT}.

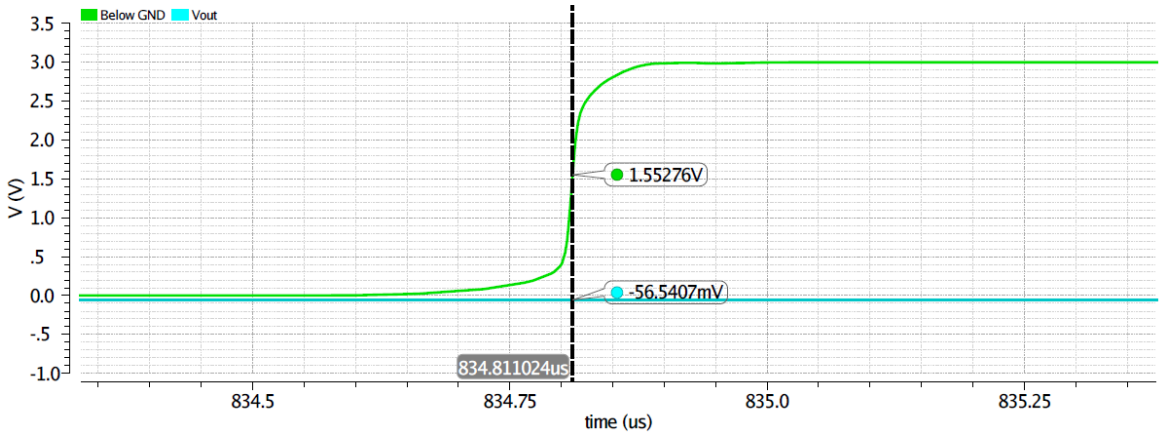


Figure 5.18: *ON threshold of the below GND comparator*

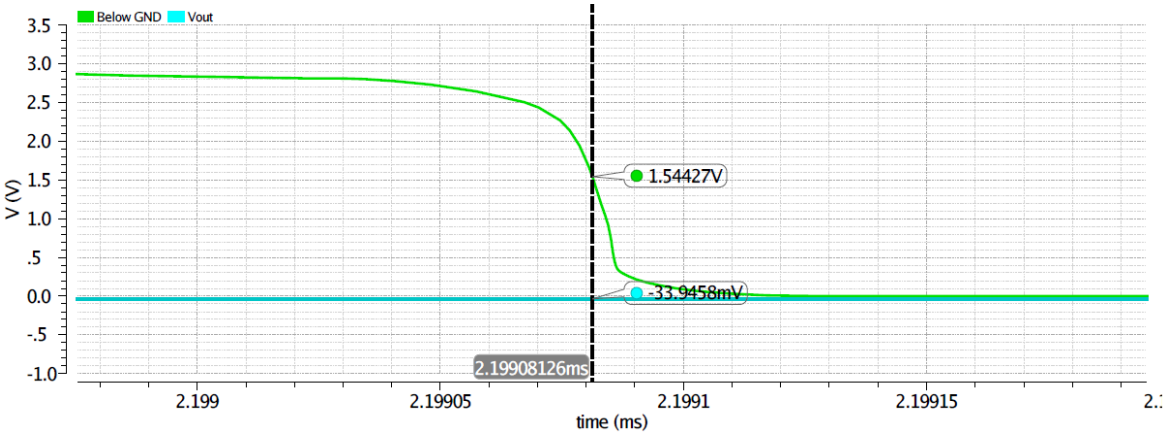


Figure 5.19: *OFF threshold of the below GND comparator*

For the sake of completeness, figure 5.18 and figure5.19, shows the ideal signal behaviour in a test bench. The test bench is needed to set the correct thresholds of the comparator, as well as the charging and discharging current for the gate of the NLDMOS. In the real application, this events happening much faster as in test bench.

Another implementation which has be done is, that in the already existing product test chip the oscillating in the output voltage, which is basically the hysteresis of the below GND comparator, can be seen or measured by the costumer. This behaviour of the output voltage is not wanted and not nice for the output voltage signal.

Therefore, another below GND comparator was implemented, which has a lower hysteresis. This leads to a lower oscillating in the output voltage signal. Both comparator are sensing the output voltage V_{OUT}, to ensure they do not disturb each other, they have a different hysteresis, illustrated in figure 5.20. As seen, the comparator for the internal supply voltage generation have a greater hysteresis than the comparator for the NLDMOS activation. This is needed to ensure the internal supply voltage are already active that the second comparator can work correct. Therefore it can be said, that the comparator for the NLDMOS activation is interleaved within the comparator for the internal supply voltage generation. The concept of these implementation is illustrated in figure 5.21. It can be seen, that the first below GND comparator, highlighted in the blue dashed rectangle, is used to generate the internal supply voltage V_{DD}. Where the second below GND comparator, highlighted in the green dashed rectangle, is used for the activation of the NLDMOS to accumulate the current via the transistor channel.

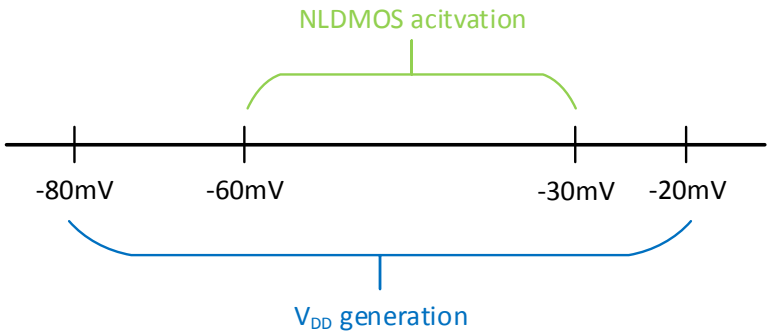


Figure 5.20: *Hysteresis of both below GND comparators*

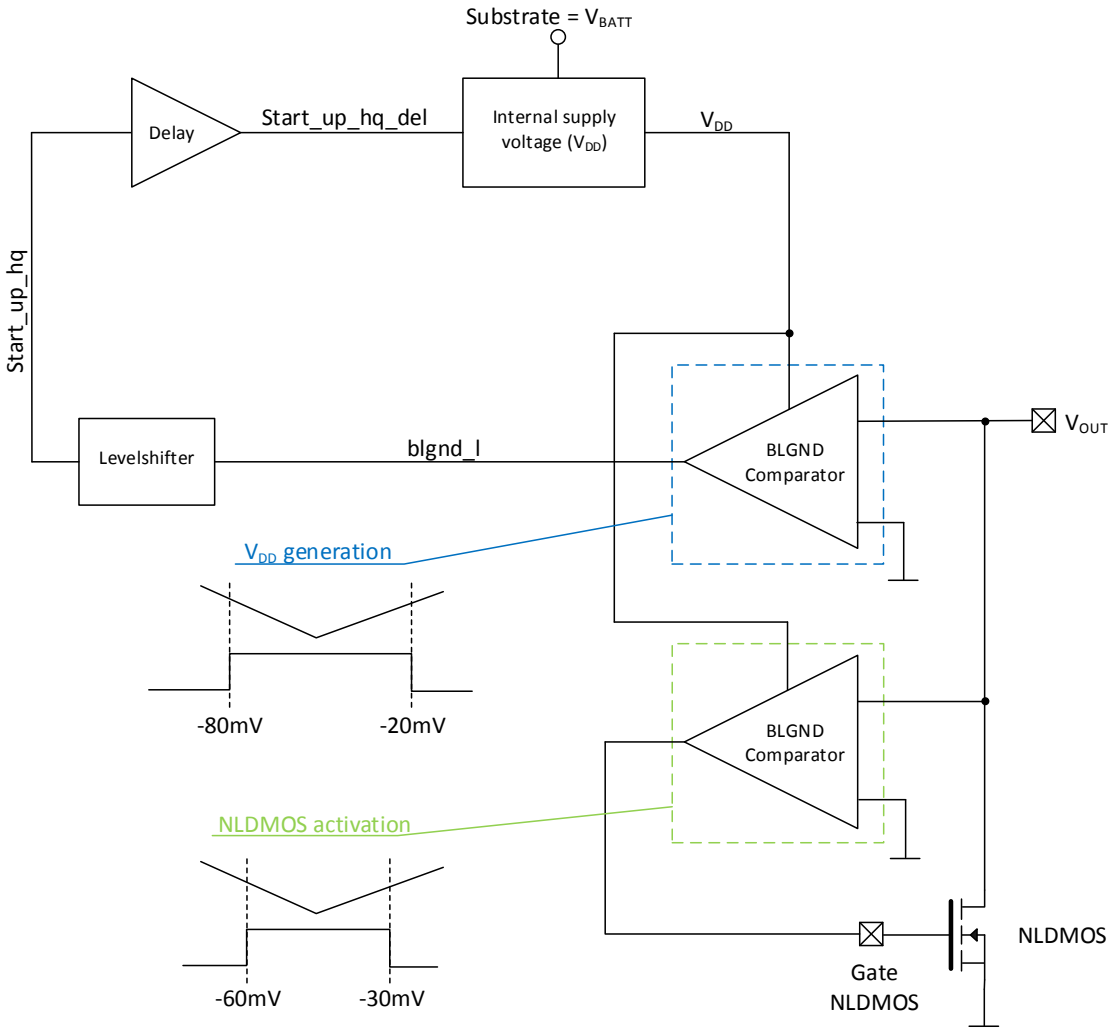


Figure 5.21: *Concept of the implementation of the second comparator to reduce output oscillating*

To understand why it is possible to reduce the oscillation of the output voltage, another look to the schematic of the below GND comparator, show in 5.16, is necessary.

By the activation of the below GND, the transistor MP5 get switched on, which leads to the charging current I_{CHARGE} for the gate of the NLDMOS to switch it on. If there is no below GND signal active, the transistor MP5 is off, but the transistor MN2 is switched on, this discharges the gate of the NLMDOS via $I_{DISCHARGE}$. This leads to the fact, that the charging and discharging of the gate of the NLMDOS happens controlled. In figure 5.22, it can be seen, that at the threshold of the comparator the below GND signal gets high, the controlled charging via I_{CHARGE} switches on the NLDMOS, which can noticed by the increasing gate voltage V_{GATE}. Furthermore, in 5.23, the discharging with the current $I_{DISCHARGE}$, happens at the second threshold of the below GND comparator, which switches the NLDMOS off, this can be also noticed by the decreasing gate voltage V_{GATE}.

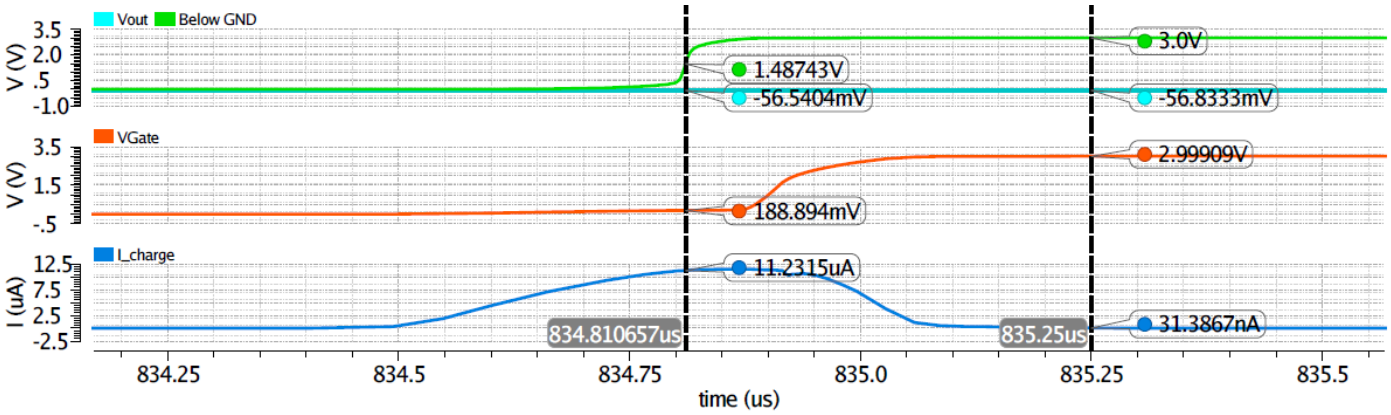


Figure 5.22: *Activating of the NLDMOS via the controlled* I_{CHARGE}

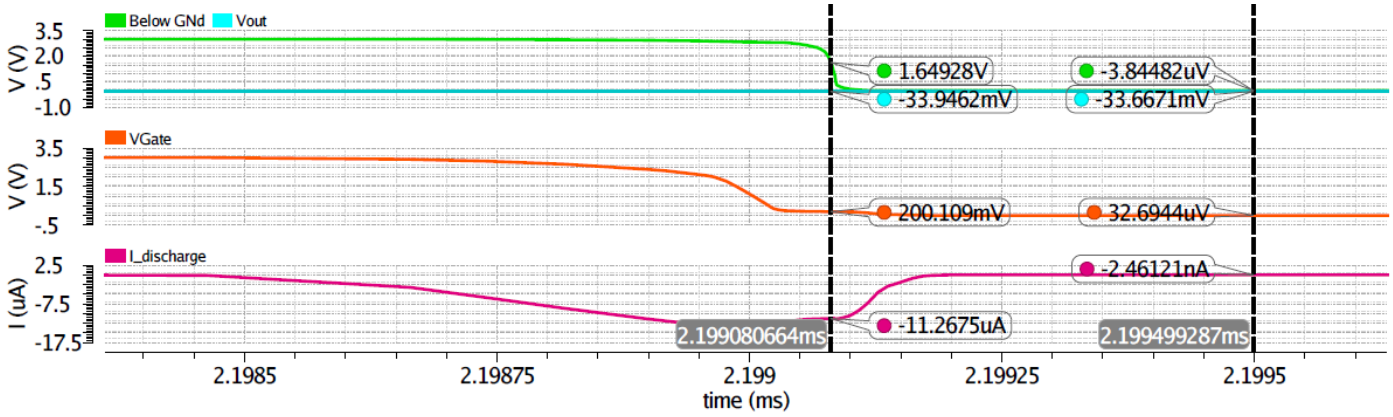


Figure 5.23: *Deactivating of the NLDMOS via the controlled* $I_{DISCHARGE}$

5.6.1 Current consumption

The main task of the concept and development, was to implement a circuit design, that the below GND protection have to work with zero standby current but it should fulfil the protection function. Therefore, the consideration of the complete current consumption of the circuit design is necessary. This is done by sensing the current from the substrate, because, as at the beginning of this work already mentioned, the substrate, which is basically the backside of the integrated circuit and fixed to the drain contact of the vertical DMOS is always available. This leads to the fact, if there is no below GND event detected from the below GND comparator, the complete current consumption have to be zero. Only if, the threshold of the below GND comparator is reached, it activates the protection circuit, which leads to a current consumption. The signals are illustrated in plot 5.24, marked with the left blue arrow is the phase where the below GND is not active, because there is no below GND event detected by the below GND comparator, there is no current consumption, described in the plot as $I_{Substrate}$. If there is a below GND event detected by the below GND comparator, the below GND protection is getting active, and a current consumption can be noticed, described with the green brace in the plot. Thus, the current gets accumulated via the channel of the NLDMOS also the output voltage is decreasing, until the point where the output voltage is smaller than the threshold of the below GND comparator. Therefore, the below GND comparator is not active and this leads again to a zero current consumption, marked with the right blue arrow in the plot.

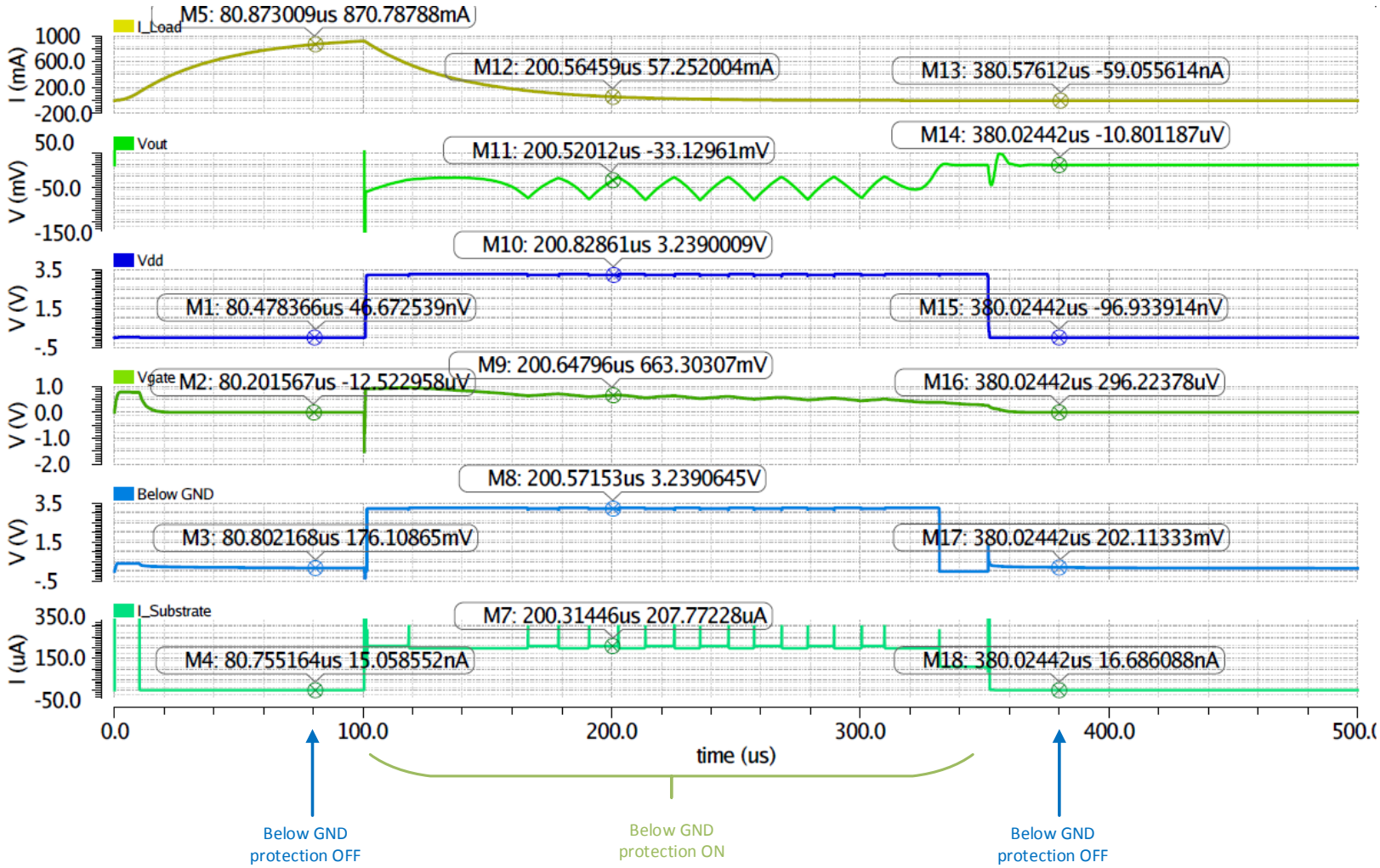


Figure 5.24: *Plot of the current consumption of the below GND protection*

Chapter 6

Comparison existing design versus this design

Due to the reason, that for the first part of this master thesis, which was the characterisation of the NLMDOS and its parasitic NPN transistor, there was no new implementation, the comparison refers only to the design part of the master thesis.

The goal of the design part, was to find a concept for the below GND protection, which should fully functional with zero stand by current. As in the previous chapter shown, this goal was achieved, compared to the already existing test chip, this has a current consumption of 3uA to 5uA.

Furthermore, as already mentioned in the existing test chip, the below GND comparator has a greater hysteresis, which lead to the fact that the output signal V_{OUT}, has a oscillating behaviour, which is not wanted. Therefore, a second below GND comparator was implemented. The two below GND comparator have its own hysteresis, the first below GND comparator is used to generate the internal supply voltage V_{DD}, that the below GND protection is working. The second comparator is used to switch on the NLDMOS via a controlled current source, that it is possible to accumulate the current via the NLDMOS channel. Due to the fact, the charging and discharging happens controlled, the current and the hysteresis could set to a lower value to reduce the oscillating of the output voltage signal.

Chapter 7

Conclusion & Outlook

7.1 Conclusion

Due to the fact, that this master thesis is based on an already existing test chip, it was possible to get a detailed consideration about the behaviour, especially concerning the below GND event. The first part of this master thesis, focus on the NLDMOS and its activation of the parasitic NPN transistor. Therefore, it was possible to characterise the parasitic NPN transistor and especially define the boundaries concerning the current capability and its temperature dependency. Due to the fact, that at higher load currents and hot temperature (150°C) the criteria in formula 7.1 will be violate, it would be possible to increase the NLDMOS area A. This will lead to a lower on-state resistance R_{DS}, as formula 7.2 shows and this will turning out a lower V_{DS} voltage.

$$V_{DS} < V_{BE} \tag{7.1}$$

$$R = \rho \cdot \frac{l}{A}[\Omega] \tag{7.2}$$

$$\rho ... Specific\ resistance\ [\Omega \cdot mm^2 \cdot m^{-1}]$$

$$l ... Lenght\ of\ the\ resistor\ [m]$$

$$A ... Area\ of\ the\ cross-section\ [m^2]$$

The requirement, that the below GND protection should work with zero stand - by current was achieved. Furthermore, the reduction of the oscillation output signal V_{OUT}, which cause by the hysteresis of the below GND comparator, could be reduced, by implementing a second below GND comparator.

Concerning the application, investigations about the switching behaviour in H-Bridge configuration is needed. Because, it is necessary to understand the full system in the automotive application, these could include:

- Definition of the load impedance
- Current in stall conditions
- Switching cycles of the DC - motor
- Temperature at the place of the DC - motor

Within the below GND comparator, the input structure are implemented with depletion transistors. They are used, because they have a negative threshold voltage and the below GND comparator should detect a negative voltage. Therefore the depletion transistor fit very well. But, there are also other circuit topologies, which make it possible to sense a negative output voltage. One example would be a folded cascode, with PMOS as input structure, the advantage with the folded cascode is, the input can go below 0V, but where the gain, bandwidth and gain-bandwidth are defined as for a single stage amplifier.

7.2 Outlook

The outlook for DC - motors, a difference between the DC - motors and the DC brush less - motors must be made. Considering the lifetime and switching cycles, DC brush less - motors are preferred, because they have no sliding contacts. Another drawback of the DC - motor is generates electromagnetic emission, which have to filtered. This electromagnetic emission happens, because between the switching of the brushes and the commutator, there will be sparks between those two components, which generates electromagnetic emission. Therefore, DC brush less - motors are more common in the automotive industry.

For the power transistor and the realisation in H-Bridge configuration, research and new innovations are always present. Therefore, a paper research on the IEEE explore turning

out a few interesting and innovative ideas. The first paper is about the 3D integration for DMOS transistors:

Electronic power systems follow the general trend of miniaturization and functional density. 3D technologies provide an interesting response if adapted to power specifications. This paper presents an H bridge of four power MOS transistors (DMOS)assembled to a through silicon via (TSV) last passive silicon (Si) interposer [10].

Another paper, shows the emerging trend of H-Bridged in electric vehicles:

This paper presents a hybrid cascaded H-bridge multilevel motor drive control scheme for electric/hybrid electric vehicles where each phase of a three-phase cascaded multilevel converter can be implemented using only a single DC source and capacitors for the other DC sources [11].

A general overview about the total safe operation area (SOA) of a lateral DMOS transistor is discussed in another paper. It is shown that the transistors are subjected to different kinds of stresses, yielding a combination of electrical and thermal degradation and/or failure modes. A methodology to build the total SOA for LDMOS transistors is highlighted and is experimentally verified on a 40-V LDMOS implemented in a 0.7um Smart Power technology [12].

Negative voltages in power stages of junction-isolated Smart Power ICs turn on parasitic bipolar transistors and inject minority carriers into the substrate, which can affect the functionality of the chip. In order to indicate inadmissible substrate currents and to evaluate protection measures, these parasitic transistors have to be included into a postlayout simulation [13].

Bibliography

[1] Murari B., Bertotti F. and Vignola G. A., *"Smart Power ICs - Technologies and Applications"*. Springer, 1996, Berlin, ISBN 3-540-60332-8

[2] Cuomo A., Grimme P., Papa C., *"Fireside smart power"*. Semicast research, 2010, (01.12.2016)

[3] Infineon, *"Automotive power selection guide"*. Infineon Technologies AG, Munich, Germany, November 2016

[4] Zitta H., *"Smart power and high voltage circuits"*. Documents from lecture 439.220 Smart power high voltage circuits, TU-Graz, WS2014

[5] Mayer D., *"Smart power high-side driver design for a power line protection circuit"*. Master Thesis at FH-Kärnten in cooperation with Infineon Technolgies AG, Villach, September 2014

[6] Lamacchia C., *"Low-Side Driver Integrated Circuit for a Half-Bridge in Automotive Applications"*. Master-Thesis at politecnico di torino in cooperation with Infineon Technologies AG, Villach, 2013/2014

[7] Bedrich J. Hosticka, K.-G. Dalsas, D. Krey, G. Zimmer, *"Behavior of Analog MOS Integrated Circuits at High Temperatures"*. IEEE JOURNAL OF SOLID-STATE CIRCUITS, pp. 871 - 874, 1985

[8] G.P. Zhigal'skii, B.K. Jones, *"The Physical Properties of Thin Metal Films"*. Taylor & Francis, 2003 ISBN 0-415-28390-6, London

[9] Elektronik Kompendium, *"Charge/Discharge of a capacitor"*. http://www.elektronik-kompendium.de/sites/grd/0205301.htm (01.01.2017)

[10] J. Charbonnier, M. Assous, J.P. Bally, A. Plihon, T. Hilt, A. Hassaine, T. Mourier, C. Brunet Manquat, R. Franiatte, J. Guillaume, C. Hartler, J. Siegert, F. Schrank, K. Pressel, H. Gruber, *"3D Integration for power MOS H bridge power application"*. ams

AG, 8141 Premstaetten, Austria Infineon Technologies AG, 93049 Regensburg, Germany, Austria , IEEE Electronic System-Integration Technology Conference (ESTC), Electronic ISBN: 978-1-5090-1402-6, 2016

[11] Zhong Du, Leon M. Tolbert , John N. Chiasson, Burak Ozpineci, Hui Li, Alex Q. Huang, *"Hybrid Cascaded H-bridges Multilevel Motor Drive Control for Electric Vehicles"*. Semiconductor Power Electronics Cener, The University of Tennessee, Oak Ridge National Laboratory, Center of Advanced Power Systems, IEEE Conference Publications, pp. 1-6, 2006

[12] P. Moens, G. Van den bosch, *"Characterization of Total Safe Operating Area of Lateral DMOS Transistors"*. IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY, pp. 349-357, 2006

[13] J. Oehmen, M. Olbrich, L. Hedrich, E. Barke, *"Modeling Lateral Parasitic Transistors in Smart Power ICs"*. IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY, pp. 408-420, 2006

List of Abbreviations

MOS	— **M**etal **O**xide **S**emicondictor
NMOS	— **N**-Channel **MOS**
PMOS	— **P**-Channel **MOS**
CMOS	— **C**omplementary **MOS**
DMOS	— **D**ouble-Diffused **M**etal-**O**xide-**S**emiconductor
NLDMOS	— **N**-channel **L**ateral **D**ouble-Diffused **M**etal-**O**xide-**S**emiconductor
MOSFET	— **M**etal **O**xide **S**emicondictor **F**ield-**E**ffect-**T**transistor
LV-	— **L**ow-**V**oltage
HV-	— **H**igh-**V**oltage
BJT	— **B**ipolar **J**unction **T**ransistor
BCD	— **B**ipolar **C**MOS **D**MOS
IC	— **I**ntegrated **C**ircuit
BLGND	— **B**elow **GND**
V_{BATT}	— **B**atterie **S**upply **V**oltage
V_{DD}	— **D**rain **S**upply **V**oltage
V_{DS}	— **D**rain **S**ource **V**oltage
V_{CE}	— **C**ollector **E**mitter **V**oltage
V_{BE}	— **B**ase **E**mitter **V**oltage
V_{IND}	— **I**nduced **V**oltage
V_{TH}	— **T**hreshold **V**oltage
V_{OUT}	— **O**utput **V**oltage
V_{CLAMP}	— **C**lamping **V**oltage
I_{COM}	— **C**ommutate **C**urrent
I_{CHARGE}	— **C**harging **C**urrent
$I_{DISCHARGE}$	— **D**ischarging **C**urrent

Gnd — **Grou**nd
TAM — **T**otal **A**vailable **M**arket
CAGR — **C**omponent **A**nnual **G**rowth **R**ate
PTC — **P**roduct **T**est **C**hip
HSS — **H**igh **S**ide **S**switch
LSS — **L**igh **S**ide **S**switch
LDD — **L**ightly **D**oped **D**rain
EMF — **E**lectro **M**agnetic **F**orce
MN — **M**OS **N**-channel
MP — **M**OS **P**-channel
MND — **M**OS **N**-channel **D**epletion
DC — **D**irect **C**urrent
TSV — **T**hrough **S**ilicon **V**ia
Si — **S**ilicon
SOA — **S**afe **O**peration **A**rea