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Printed Copper as Wafer Metallization: Material Characterization - Process Development - Technology Integration

Dissertation

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Abstract

The thesis at hand is a summary of research activities towards a new type and deposition method of a power metalization for power semiconductors. A power metalization on a semiconductor device is a metalization layer that is supposed to take up and dissipate heat pulses generated by the device upon operation. It ensures its functionality is therefore an important building block of a reliable power semiconductor device. In recent years, copper has become increasingly important in fulfilling this role, since it can be deposited electrochemically, making thick copper power metalizations economically attractive compared to aluminum, which has to be deposited in a time and cost extensive PVD process. Electroplated copper has a higher thermal capacity as well as a higher electrical and thermal conductivity than aluminum, but thick copper layers also can cause severe problems in manufacturing and reliability issues during the lifetime of the device due to the CTE mismatch of copper and silicon (17.6 vs. 2.5 ppm, respectively). This creates enormous interlayer stresses during temperature changes, resulting in wafer or chip bow and leading to a rupture of the layers after a certain amount of temperature cycles.

One way to overcome this issue is to introduce porosity into the copper metalization layer, which according to literature [1] reduces the Young's modulus of the layer and as a consequence leads to less strain to the device. There are numerous methods to deposit porous copper layers, but hardly any is suitable for semiconductor devices, which have very tight limitations towards temperature, pressure and especially possible contaminations. Printing of copper pastes that can be transformed into metallic layers is one elegant method of deposition, which offers several advantages like having a high throughput and direct structuring capability as well as being an already established deposition technique on wafer level. Those aspects contribute to the high cost efficiency of this method and therefore make it very interesting for high volume products.

This thesis will put the required processes into context of semiconductor manufacturing. It will give an overview on characterization methods of chemical and mechanical properties of raw materials and processed layers. The method of deposition will be refined and complemented by various post-treatment processes like structuring or electrical interconnection. The specific requirements of power semiconductor devices of different voltage classes will be compared to the properties of printed copper. The overall goal of those efforts is to evaluate the opportunities and assess the risks of the implementation of such materials into selected semiconductor technologies.

Zusammenfassung

Die vorliegende Dissertation beinhaltet eine Zusammenfassung von Forschungsaktivitäten zu einer neuen Art von "Power-Metallisierung" und der hierfür verwendeten Abscheidemethode auf Leistungshalbleitern. Eine Power-Metallisierung auf einem Halbleiterbauelement ist eine Metallisierungsschicht, welche vom Bauteil durch Schaltverluste erzeugte Wärmeimpulse aufnimmt und ableitet. Sie gewährleistet dessen einwandfreie Funktion und ist dadurch ein wichtiger Baustein eines jeden zuverlässigen Leistungshalbleiters. In den letzten Jahren hat die Bedeutung von Kupfer bei der Erfüllung dieser Rolle kontinuierlich zugenommen. Kupfer kann galvanisch abgeschieden werden, wodurch die ökonomische Abscheidung von dicken Metallisierungsschichten erst ermöglicht wird, während hingegen Aluminium in einem kosten- und zeitintensiven PVD Verfahren aufgebracht werden muss. Andererseits verursachen dicke Kupferschichten auch ernstzunehmende Probleme im Verarbeitungsprozess sowie in der Zuverlässigkeit im Laufe der Lebensdauer der Bauteile, da Kupfer und Silizium deutlich unterschiedliche thermische Ausdehnungskoeffizienten aufweisen (17.6 gegenüber 2.5 ppm). Dies erzeugt starke Spannungen am Interface zwischen den beiden Materialien, was zu einer Durchbiegung des Wafers bzw. des Chips führt, und im Laufe der Lebensdauer nach einer großen Anzahl von Temperaturzyklen zu einem Einreißen der Kupferschicht führt.

Eine Möglichkeit dieses Problem zu adressieren ist die Einführung von Porosität in die Kupferschichten, wodurch sich laut Literatur [1] der Elastizitätsmodul der Schicht reduziert, was zu weniger Spannungen am Bauteil führt. Eine Vielzahl an Methoden zur Abscheidung von porösen Kupferschichten ist bekannt, jedoch eignen sich die wenigsten hiervon für die Anwendung auf Halbleiterbauelementen, da diese nach strikten Einschränkungen bezüglich der verwendeten Temperaturen und Drücke verlangen, sowie sehr sensibel gegenüber Kontaminationen sind. Das Drucken von Kupferpasten, welche durch geeignete Prozesse in metallische Kupferschichten überführt werden können, stellt eine elegante Abscheidungsmethode dar. Eine Reihe von Vorteilen wie der hohe Waferdurchsatz, direkte Strukturierbarkeit sowie das Vorhandensein von geeignetem Equipment tragen zur Kosteneffizienz dieser Methode bei, wodurch sie sich für die Anwendung in Volumensprodukten empfielt.

Diese Dissertation wird die für die Herstellung benötigten Prozesse in Bezug zur Herstellung von Halbleiterbauteilen setzen. Sie wird einen Überblick über die Charakterisierungsmethoden der chemischen und mechanischen Eigenschaften von Rohmaterialien und prozessierten Schichten geben. Die Abscheidungsmethode wird verbessert und durch diverse Folgeprozesse wie Strukturierung oder elektrische Anbindung ergänzt werden. Die speziellen Anforderungen von Leistungshalbleiter-Bauelementen unterschiedlicher Spannungsklassen wird mit den Eigenschaften geprinteter Kupferschichten verglichen

werden. Das übergeordnete Ziel dieser Arbeit war eine Evaluierung der Vorteile und der Risiken der Implementierung dieser Materialien in die Halbleiterfertigung.

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Thank's to Barbara's efforts printed copper started to become interesting for several applications for which it previously did not qualify due to it's low conductivity. Barbara's optimizations of the furnace process gave us a huge boost, and her structured and organized style of working changed the way we were addressing problems. Also she contributed a lot to the understanding of the material behavior.
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Deutsche Fassung:
Beschluss der Curricula-Kommission für Bachelor-, Master- und Diplomstudien vom 10.11.2008 Genehmigung des Senates am 1.12.2008

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I declare that I have authored this thesis independently, that I have not used other than the declared sources / resources, and that I have explicitly marked all material which has been quoted either literally or by content from the used sources.

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Date Signature

Abbreviations

4PPM	**4** **P**oint **P**robe **M**ethod
BEOL	**B**ack **E**nd **O**f **L**ine
BSM	**B**ack **S**ide **M**etal
CTE	**C**oefficient of **T**hermal **E**xpansion
DCB	**D**irect **C**opper **B**onded
DMA	**D**ynamic **M**echanical **A**nalysis
DoE	**D**esign **o**f **E**xperiment
DSC	**D**ifferential **S**canning **C**alorimetry
EBSD	**E**lectron **B**ack- **S**catter **D**iffraction
ECD	**E**lectro- **C**hemical **D**eposition
EDX	**E**nergy **D**ispersive **X**-Ray spectroscopy
EFO	**E**lectric **F**lame- **O**ff
FAB	**F**ree **A**ir **B**all
FAV	**F**ormic **A**cid **V**apor
FEOL	**F**ront **E**nd **O**f **L**ine
FIB	**F**ocused **I**on **B**eam
FSM	**F**ront **S**ide **M**etal
FT-IR	**F**ourier **T**ransform **I**nfra- **R**ed spectroscopy
GC	**G**lass **C**arrier
GC-MS	**G**as **C**hromatography **M**ass **S**pectrometry
ICP-MS	**I**nductively **C**oupled **P**lasma **M**ass **S**pectrometry
IGBT	**I**nsulated **G**ate **B**ipolar **T**ransistor
IML	**I**ntrinsiq **M**aterials **L**td.
LDI-MS	**L**aser **D**esorption **I**onization **M**ass **S**pectrometry
MEMS	**M**icro **E**lectrical **M**echanical **S**ystems

MOSFET	**M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor
MSDS	**M**aterial **S**afety **D**ata **S**heet
μCT	micro **C**omputer **T**omography
PEG	**P**oly **E**thylene **G**lycol
(PE-)PVD	(**P**lasma **E**nhanced) **P**hysical **V**apor **D**eposition
PCB	**P**rinted **C**ircuit **B**oard
$R_{DS(on)}$	**R**esistance **D**rain **S**ource **on**
SEM	**S**canning **E**lectron **M**icroscopy
SNIT	**S**ilicon **NIT**ride
TDS	**T**hermo **D**e**S**orption
TGA	**T**hermo **G**ravimetric **A**nalysis
TMAH	**T**etra **M**ethyl **A**mmonium **H**ydroxide
TOF-SIMS	**T**ime **O**f **F**light **S**econdary **I**on **M**ass **S**pectrometry
VdPM	**V**an **d**er **P**auw **M**easurement

Chapter 1

Introduction

The thesis at hand has been written in the EPPL project (n° 325608), co-funded by grants from Austria, Germany, The Netherlands, France, Italy, Portugal, ECSEL member states and the ECSEL Joint Undertaking. The upcoming introduction will give a brief overview on the current situation in semiconductor industry, nowadays challenges in the field of metalization and the reasons why some of those challenges might be addressed by porous materials.

1.1 Copper in Semiconductor Manufacturing

Ever since in the history of semiconductor manufacturing, the decrease in size of the devices was one of the major drivers for innovation. This is being accomplished mainly by introducing new designs of semiconductor transistors, beginning with the first integrated circuit device introduced by Jack Kilby in 1958 [2] and leading to modern logic circuits, most prominently the CMOS (complementary metal oxide semiconductor) technology and power semiconductors like insulated gate biploar transistors (IGBTs), metal-oxide-semiconductor field effect transistors (MOSFETs) and a vast number of specialized varieties of those. By decreasing the size of the chips, the density of transistors is increasing, which leads to several challenges including heat dissipation. A semiconductor device generates heat upon switching, and with the high power fluxes of more than one hundred kilowatts per square centimeter as approached by modern IGBTs [3], the heat dissipation of power semiconductors is becoming the focus of research.

These problems have been addressed by optimizing the design on the one hand, while decreasing the silicon thickness on the other hand, as well as integrating new materials. Currently in power semiconductor industry, there is a transition from aluminum to copper metalization due to the higher electric and thermal conductivity of copper, as well as its higher heat capacity. [4] The introduction of copper metalization creates several challenges, since copper unlike aluminum tends to form silicides when being in direct contact with silicon. Those silicides can cause cracks and shortcuts in the semiconductor devices upon operation, which is a major reliability issue. [5] To avoid the formation of copper silicides, one or more barrier layers have to be introduced at the interface between copper and silicon. A barrier for copper is a metallic layer with good conductivity but poor solubility of copper atoms, for example alloys of tungsten and titanium [6], titanium nitride or tantal nitride [7]. Such barrier layers, as well as the copper layer itself, cause a huge mechanical stress to the device, since the coefficient of thermal expansion (CTE) of those layers are different from that of silicon. Copper, although having a smaller CTE than aluminum (17.4 vs. 23.1 ppm), has a higher contribution to wafer bow than aluminum due to it's higher yield strength, as can be seen in figure 1.1 taken from literature [8]. The term wafer bow describes the degree to which a wafer is deviating from its originally flat shape. It is typically a problem for many production tools and wafer handlers and hence needs do be confined in narrow specification limits by thorough design of the devices.

1.2 Copper induced Stress in Thin-Wafer Technology

With the copper thickness being relatively small compared to the overall thickness of the wafer, the resulting wafer bow can be contained within acceptable limits. Of course, the reduction of the silicon thickness is inevitable for reducing the $R_{DS(on)}$, the resistance of the device when current is flowing through it. The $R_{DS(on)}$, which is the resistance between drain and source in "on" state, in a DMOS type semiconductor device is the sum of six internal resistances within the device, including the resistance of the drift region. [9], [10] Equation 1.1 lists the contributors to the $R_{DS(on)}$ according to literature [10].

$$R_{DS(on)} = R_n + R_{Ch} + R_{acc} + R_{JFET} + R_{drift} + R_{drain} \tag{1.1}$$

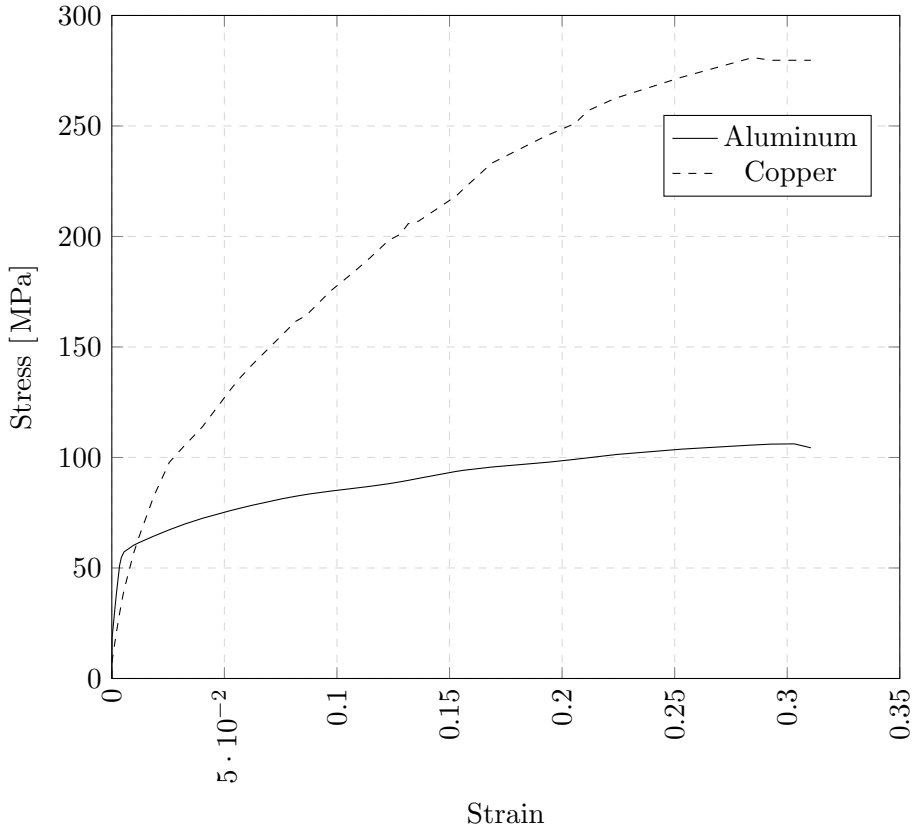


FIGURE 1.1: Strain curve of copper and aluminum under tensile stress, taken from literature [8].

The R_{drift}, which is the resistance of the drift region accounts for 95% of the $R_{DS(on)}$ and is dependent on the resistivity (influenced by the doping level) and the thickness of the drift region. [11] The other contributors to the $R_{DS(on)}$ are the lateral resistance of the n-source R_n, the resistance of the MOS channel R_{Ch}, the resistance of the region where the electrons are leaving the MOS channel R_{acc} (the abbreviation is due to the electron accumulation effect occurring in that region), the resistance of the n^- region separating the DMOS cells R_{JFET} and the resistance of the highly doped drain region R_{drain}.

A schematic illustration of the different contributors can be found in figure 1.2. The $R_{DS(on)}$ is one of the main contributors for losses in power semiconductors (others would be e.g. the resistances of the interconnections and the package), which means that the reduction of the on-resistance of silicon devices is greatly contributing to the efficient use of energy.

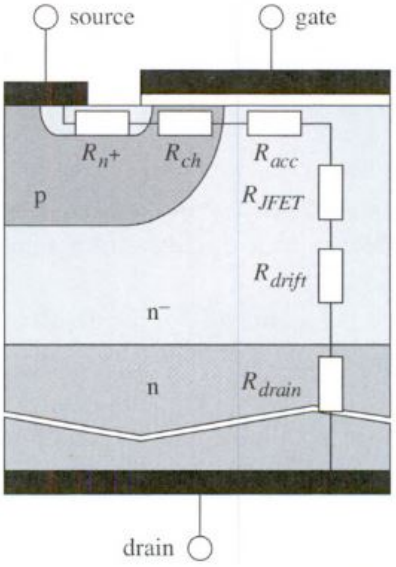


FIGURE 1.2: Main contributors to the $R_{DS(on)}$ in a vertical DMOS FET, picture found in [10].

In order to reduce the $R_{DS(on)}$ to an absolute minimum, two measures are being undertaken: First, the doping of the substrate is being adjusted to fit the requirements of the application. High voltage devices typically use substrates with a resistivity of 20 mΩcm, whereas low voltage devices use highly doped substrates with a resistivity as low as 5 mΩcm [12]. Secondly, the thickness of the drift region is being reduced to an absolute minimum [13]. The required thickness of the drift region W_D to block a maximum applied voltage V_{max} is given by equation 1.2 found in literature [14].

$$W_D = \sqrt{\frac{2\varepsilon_s V_{max}}{qN_D}} + L_P \tag{1.2}$$

It is equal to the sum of the diffusion length L_P and the width of the diffusion depletion layer, with qN_D as the charge carrier density and ε_s being the permittivity of the substrate. As a rule of thumb, silicon devices have a reverse voltage blocking capability of 10V per μm silicon, i.e. to build a vertical MOSFET device which needs to switch 50V, the minimum thickness of the drift region is as low as 5 μm.

Besides its purpose as a heat sink, thick copper metalizations are therefore also used for a second reason: During the manufacturing of the devices in back-end, the final chips have to be picked up from the dicing foil to be placed into the package, the so called 'die attach'. This pick-up process consists of a needle array pushing the chips up from

below the dicing foil, which causes the edges of the chips to be released from the foil due to the rigidness of the chip. Since silicon becomes flexible when being thinned town to thicknesses below approximately 50μm, this edge release is not possible with thinner chips and hence the chips can no longer be picked. Therefore, since the decrease of silicon thickness is inevitable for increasing the performance of next generation semiconductor devices, the overall thickness needs to be kept constant by introducing a thick, rigid conducting layer: copper. This concept is currently realized in MOSFET chips for low and medium power densities, where silicon thicknesses below 40 μm are today state of the art, but with the final goal of 5 μm on the horizon.

Another issue that is accompanied with the deposition of thick copper layers is occurring upon operation of the device. Semiconductor devices are often interconnected to the outside-world by wire-bonding the front-side to the lead frame. Those bond wires can either be attached by ultrasonic bonding or by additional heating of the wire by so called thermosonic bonding. The interface of the bond wires with the copper metalization layer is strongly affected by the thermo-mechanical stress due to the high temperature changes in the die during switching, which by time can lead to a lift-off of the bond wires [15]. In order to reduce the interface stress, so-called stress relief structures are known to literature [16]. Layers with a low stiffness and the same coefficient of thermal expansion as the substrate are proposed as such structures [16]. The introduction of a thick, soft front-side metal as buffer layer which might therefore reduce the damage inflicted to it by the bonding process, also acting as a kind of spacer between the site of impact of the wire and the barrier interface. For this application, bulk copper does not seem suitable due to its comparably high hardness [17] and its different CTE, again leading to wafer bow. The altered mechanical properties of porous copper on the other hand might offer advantages for this purpose, as will be discussed in this thesis.

1.3 Stress-Reduction by Grain-Size Adjustment

In order to avoid the various afore mentioned problems of thick copper metalizations, the most prominent being

1. the wafer bow during manufacturing,

2. the chip bow during die-attach as well as

3. the deformation of the chip during operation with the resulting reliability problems,

it is necessary to engineer or design the copper material in order to exhibit less stress to the silicon device. Basically, there are two possible approaches to address this issue: The first one is the modification of the properties of electroplated copper layers by changing the deposition parameters and electrolyte additives in order to achieve smaller grain size. The theoretical background for this approach can be found in the Hall-Petch relation: Adjacent grains usually have a different crystallographic orientation [18], [19], [20]. Upon plastic deformation, slip or dislocation motion have to take place at the grain boundaries. Due to the different orientation, a dislocation moving along a grain boundary has to change its direction when passing onto another grain. Also, the atomic disorder in the grain boundary region will cause a discontinuity of slip planes [21]. Those two effects result in a negative proportional relation between grain size and yield strength, as it is depicted in the Hall-Petch equation 1.3, where d is the grain size of the material, σ_0 is a friction stress that opposes dislocation motion and k_y is a material constant which is virtually temperature insensitive. The value of k_y indicates the sensitivity of the materials yield strength to grain size [21].

$$\sigma_y = \sigma_0 + k_y d^{-1/2} \tag{1.3}$$

The grain size of electroplated copper can be controlled by altering the deposition parameters like current density, applied current signal, temperature or bath composition [22]. By applying very high current densities, grain sizes even in the range of nanometers can be achieved, resulting in materials with very interesting mechanical properties [23]. One important reason why the approach of reducing the grain size by increasing the current density during deposition is not applicable to semiconductor devices is grain growth by annealing and self annealing. Since the semiconductor device will turn hot upon operation, the copper grains will receive enough energy to reduce the amount of grain boundaries and hence come to a lower energetic state. This effect will even occur while storing the devices at room temperature [24], [25]. A device that changes its properties during operation is of course inacceptable for the customer. Recently, efforts to stabilize the small grain size by alloying nano sized copper with other metals

like zirconium, which is predicted to significantly reduce the grain boundary energy of copper by segregation were undertaken [26]. Since this process requires annealing of the copper at 1000 °C, it is not applicable to semiconductor applications, as it would need to be applied in the back-end of line. The standard process flow of semiconductor device fabrication is divided into the FEOL (front-end of line), the BEOL (back-end of line) as well as the back-end. [27] Within the FEOL, the electrical properties of the basic material are modified by doping by ion implantation or diffusion, followed by high temperature furnace steps. The following BEOL processes introduce metalization and passivation steps required for the interconnection of the semiconductor device to the package. In the back-end, the devices are assembled into the package by different specific techniques of interconnection and encapsulation. A common first-layer metal[1] in many semiconductor technologies is aluminum [28], having a melting point of ca. 660 °C. Also, diffusion of dopants is undesired by this point of manufacturing, but the standard p-doping element boron has already significant diffusion rates at temperatures below 1000 °C [29]. Additionally, standard passivation and insulation materials applied in the BEOL, e.g. polyimide or epoxide have a limited thermal budget of typically around 400 °C.

1.4 Stress-Reduction in Porous Materials

The second approach, which will be reviewed within this thesis, deals with the development and implementation of a completely novel deposition method to generate porous copper metalization layers. Porous materials are widely used in other branches of industry like automotive, aerospace, ship building, sporting equipment and various others for their interesting combinations of physical and mechanical properties. [30]. Examples for such properties would be high stiffness in combination with low specific weight, gas permeability, high surface to volume ratio or comparably high thermal conductivity [31], [32], [33], [34].

To single out the optimal method for the particular application, it is first necessary to define the properties that should be provided by the material. Since the porous material should serve as a heat sink, its capability to store and conduct thermal energy is of utmost

[1] Especially in highly integrated devices, often the chip metalization comprises of several layers of metal. The first-layer metal is connecting the silicon to the metal interconnection layers above.

importance. In metals, heat is conducted predominantly by electrons, which are by the factor 2-3 faster than phonons. Hence, the electrical conductivity is interconnected with the thermal conductivity, a fact that is represented in the Wiedemann-Franz law [35]. The electrical conductivity (or more common its inverse value, the electrical resistivity) is important not only due to its relation to the thermal conductivity, but also due to the fact that the interconnection of the chips to the leadframe is typically done by wire-bonds on the metalization. Hence, the current needs to flow through the porous copper which creates demand for low ohmic resistivity. Simulations have shown that e.g. IGBT applications require electrical resistivities of maximum 3× bulk resistivity, which would be around 5 $\mu\Omega$cm. This would give a minimum thermal conductivity of 135 $\mathrm{Wm^{-1}K^{-1}}$.

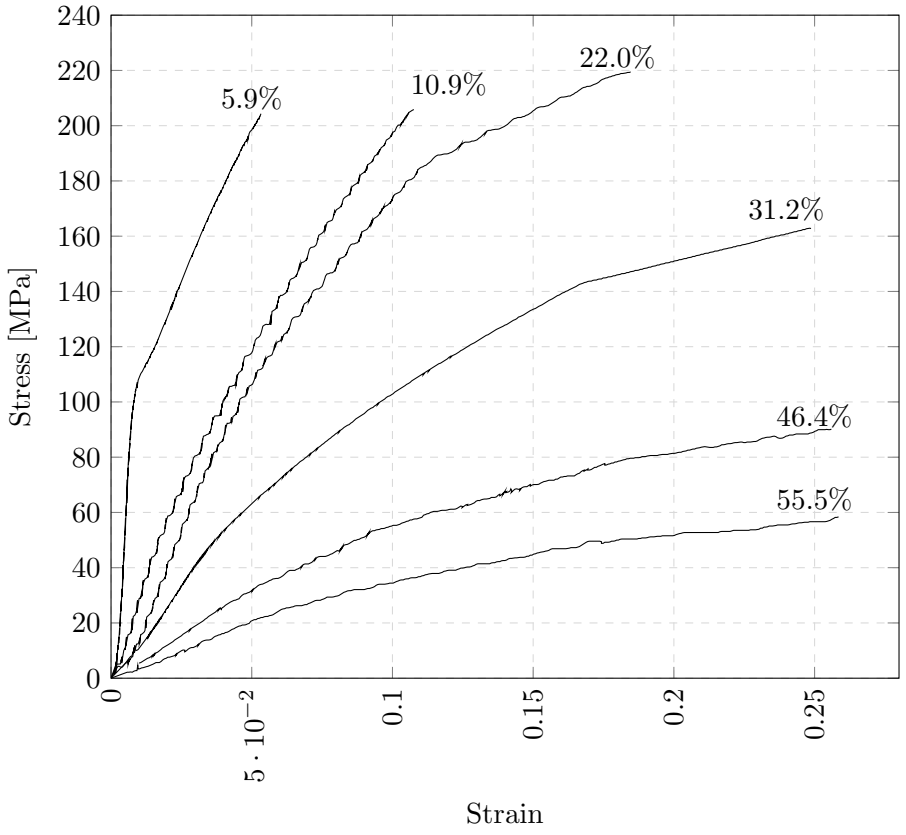


FIGURE 1.3: The stress strain curves of porous coppers with 5.9 to 55.5% original porosity under quasi-static compression condition, taken from literature [1].

On the positive side, the loss in conductivity and thermal capacity that is to be expected from porous materials must be compensated by superior mechanical properties. The thermo-mechanical stress, that is excerted by the metalization layer onto the silicon substrate and creates the wafer bow, should be as low as possible. Current thick copper metalizations exhibit stress of up to 200 MPa to the wafer. Here it is very hard to say

how much stress is still acceptable, since it is dependent on the technologies as well as on the manufacturig tools. Typically, the stress of the front-side metal needs to be balanced with the stress of the back-side metal to gain an overall flat chip, as it is required during packaging of the chip. This balancing is very difficult and can always only be done for a particular temperature range. The stress of metal foams can be effectively reduced by introducing porosity: Figure 1.3 shows stress-strain curves of porous coppers with porosities of 5.9-55.5% under quasi-static compression conditions. It can be seen that the stress curve is flattening upon an increase of porosity [1]. As will be later discussed in section 2.4.2, the thermo-mechanical stress is connected to the Young's modulus over the porosity independent CTE, so the stress reduction must be caused by a reduction of the modulus. Porosity, according to Gibson and Ashby [1], [36], is the single most structural characteristic of a cellular material which influences the Young's modulus. Figure 1.4 shows experimental data compared to theoretical predictions of Gibson's and Ashby's closed-cell model, reprinted from literature [1]. As can be seen in figure 1.4, the relative Young's modulus is strongly affected by the introduction of even small amounts of porosity.

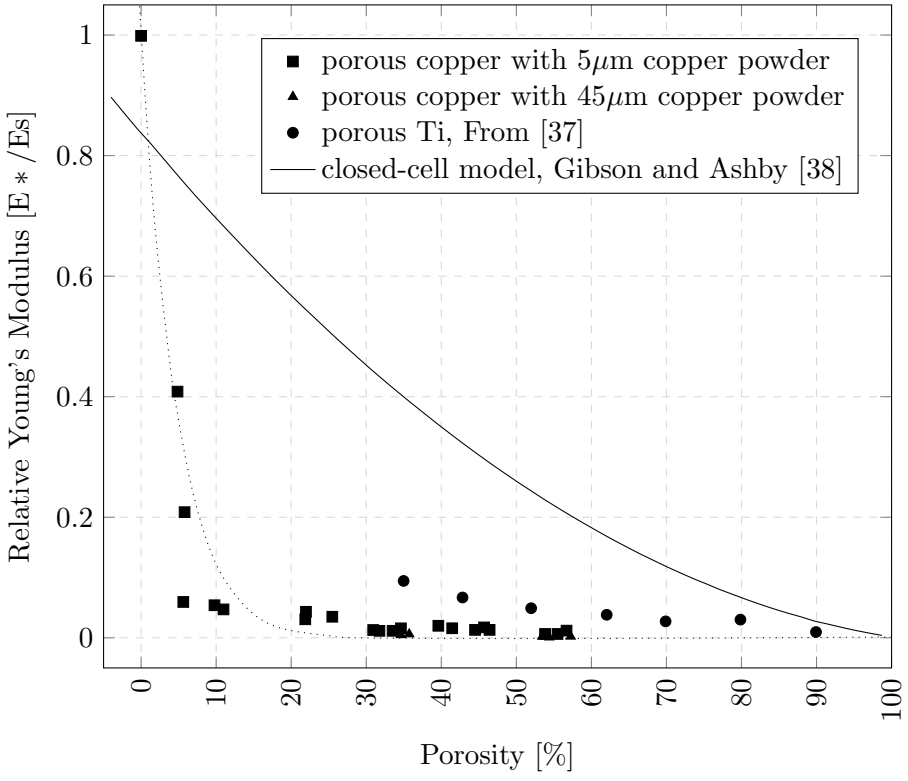


FIGURE 1.4: The Youngs modulus of porous metals normalized by the Youngs modulus of solid metal against porosity, taken from literature [1].

1.5 Manufacturing Methods for Porous Metals

The data shown in figure 1.4 was acquired mostly on sintered copper powders, but the manufacturing procedures which can produce porous materials are numerous and include exotic methods like foaming liquid metals with gas or extruding of polymer/metal mixtures. Figure 1.5 gives a short overview on the different types of source materials and methods according to [30].

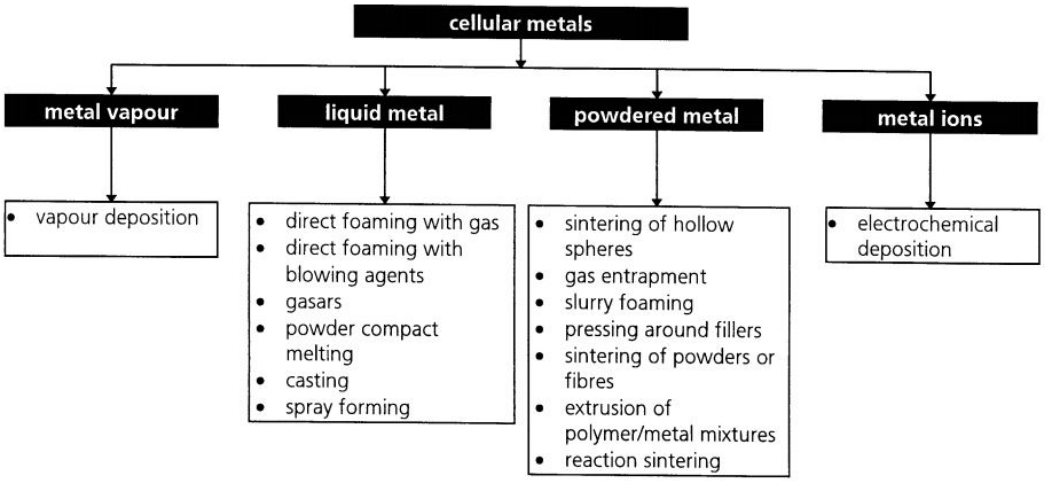


FIGURE 1.5: Different manufacturing methods for cellular metals [30].

It is clear that not all of those methods will be applicable to semiconductor applications, since e.g. copper melts at 1084 °C, a temperature that would as previously discussed severely damage any device, so any deposition method that includes liquid metals can not be used. Metal foams deposited by vapor deposition typically have very low densities, which can be interesting for applications where a high surface area is needed, but is not suitable for serving as a heat sink on power semiconductors due to the low specific thermal conductivity of highly porous metals. Besides the deposition from metal ions, the only remaining method of interest would be the deposition by sintering of metallic powders.

Handling of powders in a cleanroom environment is difficult, especially in case of critical materials like copper. Therefore only a limited amount of methods are suitable for this task.

1.5.1 Plasma Deposition

A plasma deposition tool for copper and other metal and polymer micro-powders that is suitable for semiconductor manufacturing is known to the scientific community in form of the patented PlasmaDust process by Reinhausen Plasma GmbH [39], but the method bears the inherent risk of spreading copper particles in the production environment. In this process, the surface of the particles is activated by a plasma of an inert or reductive gas, which enables the formation of a solid state connection between the particles and a surface they are sprayed on (see figure 1.6). By varying the deposition parameters, the material properties could be adjusted, giving layers with either high or low porosity [15].

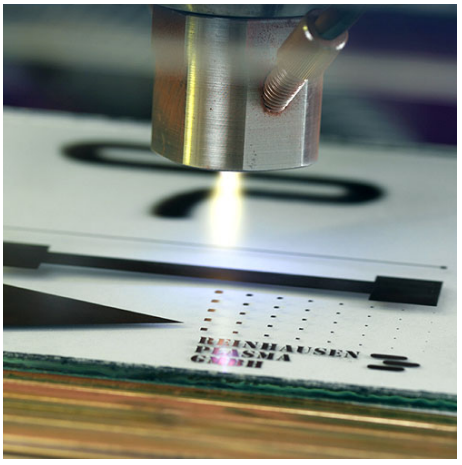


FIGURE 1.6: PlasmaDust deposition, picture taken from [39].

One of the most striking negative aspects of this technique - besides the sophisticated high-tech equipment with all its challenges and the inherent contamination risk - is the slow deposition rate. During the deposition process, the plasma torch has to scan the wafer line by line, and in order not to exceed a critical temperature during deposition, the propagation speed of the torch would need to be carefully controlled, thus limiting the amount of material that could be deposited within one run.

1.5.2 Printing of Copper Pastes

A more elegant way to handle copper powders is binding them in an organic matrix in order to prevent contamination and bring them into a form in which they can be applied by printing.

Printing on wafer level itself is not a new idea: In 2001 International Rectifier announced the introduction of a new package type, the DirectFET^{TM}. The DirectFET^{TM} package was designed for flip-chip applications [40] and uses a process sequence of a two step printing process combined with a lithographical structuring on to the front-side of a MOSFET chip. First, a screen printing process is applied, which deposits a polymer insulator on the chip. After the photolithography step, in which the pads are opened in this polymer mask, a solder paste is printed onto the pads in a stencil printing process. The chip is then glued into a metal package with a conductive silver glue, which is the drain contact. All contacts are therefore on the same side, which enables interconnection of the die to the PCB by soldering, making wire bonding unnecessary [41]. Figure 1.7 displays two already packaged DirectFET^{TM} chips. The brown polymer and the solder-paste pads are easy to spot on the front side, which in this package points into the direction of the printed circuit board where it will be attached. Since usually the back-side of the chip is attached to the PCB, this particular design is called 'flip-chip'.

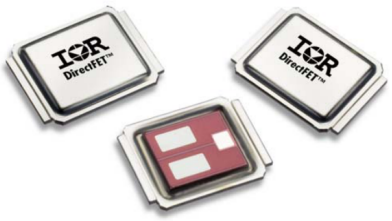


FIGURE 1.7: International Rectifier package type DirectFET^{TM} with printed solder paste and epoxid passivation. Picture found online at [42].

Solder paste printing is currently the most common productive printing process that is used within the semiconductor and electronics industry, be it on wafer level or on printed circuit boards. Most stencil printing equipment is therefore optimized to process solder materials, which means that e.g. the stencils, the cleaning agents and the stencil coatings are designed to provide optimal compatibility with common commercial solder pastes. Since copper pastes are very differerent from solder pastes in their composition, the standard materials and processes used for printing need to be adapted to the different chemical and rheological behavior of these pastes.

Copper pastes for screen or stencil printing applications have their origin in the emerging printed electronics industry. First applications in form of printed circuit boards used the high deposition speed and direct structuring capability of printing techniques to gain a cost advantage, but soon also novel and innovative applications like functional

wear or flexible electronic devices on plastic substrates were developed. As forecast by IDTechEx, today's (2016) market size of $26.54 billion is expected to more than double to $69.03 billion in 2026 [43]. The market is currently in a transition phase from silver to copper for reasons of cost saving, which is being enabled by new low-temperature curing methods.

1.6 Thesis Overview

Introducing printed copper pastes into semiconductor manufacturing requires work in three different but interconnected fields: characterization of material properties, finding the optimal processing conditions and integrating those processes into the workflow of an existing or new technology. The interdependencies of these three fields and how they are embedded into this thesis is illustrated in figure 1.8: The chip technology for which the paste is to be used on has certain technology requirements like resistivity, wafer bow, the size and shape of the structures or the pad thickness. Knowing the material properties of layers generated by standard processes from thorough material characterization and considering technology specific restrictions like temperature limitations, it needs to be verified that the technology requirements are fulfilled. If this is not the case, processes need to be developed that are compatible with the technology and provide materials with the required properties. This feedback loop generally needs to be cycled several times until the material properties match the technology requirements, so that technology integration, i.e. the integration of the developed processes into the process flow of the technology can be pursued.

The thesis at hand is therefore containing chapter 2 dealing with the characterization of the raw materials, the pastes, before processing, as well as with the investigation of the cured layers, especially explaining the characterization methods. Some of the general technology requirements of next generation semiconductor devices towards metalization layers are mentioned in chapter 1, especially in 1.7, others will be discussed in chapter 3, next to the related process adaptations. Chapter 3 also contains detailed information on the developed processes, as well as proposed ways for technology integration. As finally will be discussed in chapter 4, those processes could not be optimized to a stage in which a full 1:1 integration would be feasible, but will need further development effort

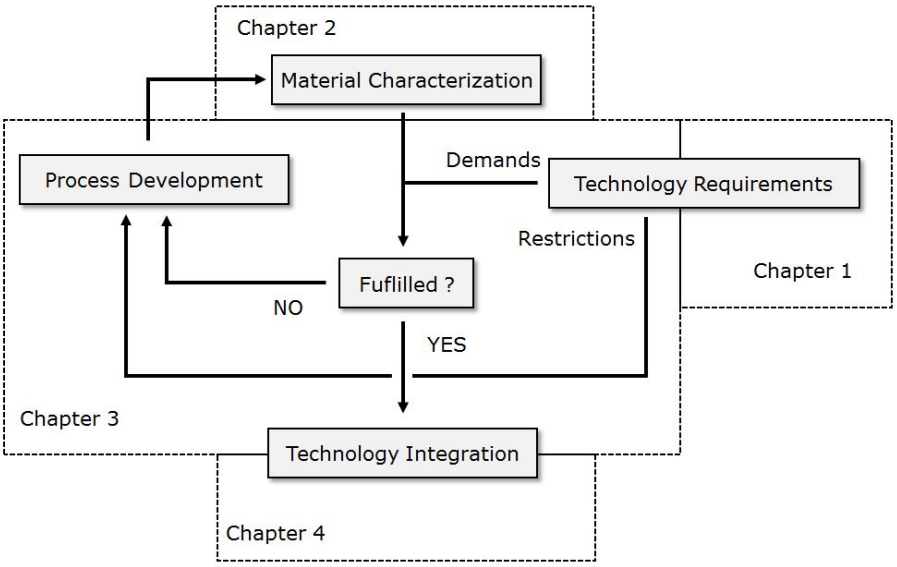


FIGURE 1.8: Schematic illustration of the thesis structure.

that will go beyond this thesis. Nevertheless, as documented in section 4.3, a variety of new processes could be developed, providing a toolbox for future work on this topic.

1.7 Issues in Question

There is a number of open questions which will determine whether there is an application of printed copper pastes in power semiconductor manufacturing or not. The following list will give an overview on the most important key issues and specify where or whether this information can be found within this thesis.

Resistivity vs. Thermo-mechanical Stress

The resistivity of porous metal layers is higher than of bulk material. If the resistivity is too high, the use of copper instead of aluminum becomes unattractive. Therefore, the resistivity must be decreased down to a level on which it is still acceptable for the respective technology. On the other hand, increasing porosity reduces the thermo-mechanical stress leading to wafer bow. A proper compromise in this trade-off needs to be found in order to maintain the mechanical advantages of the material while reducing the loss of conductivity to an acceptable level.

Resistivity: Section 2.1

Thermo-mechanical stress: Section 2.4

Oxidation Stability

Open-porous materials could be prone to oxidation: Oxygen could readily enter the porous network and oxidize it from the inside to the outside, hence increasing the rate of degradation compared to bulk material. The oxidation characteristics of the materials therefore must be studied.

Results: Section 2.5.1

Structuring

Many Infineon technologies that use thick copper layers are using very small die sizes. Such dies can be separated by sawing streets as thin as 50 μm or less, which is hard to realize with stencil printing. Hence, methods to structure porous copper layers must be developed.

Overview on the different methods: Section 3.2
Method for structuring fine sawing streets: Section 3.2.3

Interconnection

Pad metalization serves not only the purpose of heat removal, but is also the interface of the chip to the outside world. Therefore, the metalization must be capable of being used together with standard interconnection techniques like wire bonding and soldering. In case of wire bonding, problems might arise from the fact that the hardness of a porous layer is typically lower than that of bulk material [44]. In case of soldering, the open porous network could be quickly soaked with solder paste upon a reflow process, which would increase the rate of formation of an intermetallic layer and use up the whole copper pad. These risks need to be studied and evaluated carefully.

More details on the different interconnection processes, their requirements and their compatibility with porous copper layers can be found in section 3.4.

Details on wire-bonding: Section 3.4.2
Details on soldering: Section 3.4.3

Characterization

Porous metalizations are a completely new field of study within semiconductor industry. For future implementation of such materials, tight quality control of the raw materials as well as the final layers is necessary. There is few to no knowledge on the characterization of porous materials, which needs to be generated.

This information can be found in chapter 2, in which section 2.3.1 contains analysis results on the raw material.

Cross-Contamination

Copper is a very critical material in semiconductor manufacturing, since it can easily migrate through silicon-oxide passivation layers and cause shortcuts. Therefore, cross contamination needs to be avoided at any cost. The proper handling of copper printing pastes in a cleanroom environment needs to be studied and safe working procedures need to be developed.

A description of the deposition process will be given in section 1.8, whereas a risk assessment can be found in section 3.1.

Adhesion

Layers have to adhere to each other. As obvious as this rule may seem, sufficient adhesion should not be taken for granted. Due to residues from prior manufacturing steps, oxidation or the presence of surface contaminations the adhesion of printed structures needs to be carefully evaluated on every single surface of interest.

Consequences of insufficient adhesion will be reviewed in section 3.4.2.

Economical Aspects

One of the major arguments for printed wafer metalizations besides their beneficial physical properties is the cost factor. Due to the nature of the deposition method, very thick (50-100 μm) layers can be deposited for the same process cost than thin layers. This is an enormous advantage especially when creating heat sinks.

As this topic is considered confidential, it will not be not reviewed within this thesis.

Reliability

Due to the lower (thermo-)mechanical stress that is inflicted to the devices from porous materials in comparison to their bulk counterparts, one might expect the device in the field will be stressed less and hence should offer improved reliability. On the other hand, the pores might be predetermined breaking points, and the increased surface might lead to increased corrosion rates.

Section 2.5.2 gives an overview on the efforts to obtain reliability data.

1.8 General Process Description

Before going into detail on these issues, for a better understanding of the upcoming chapters the general process-flow of copper paste printing will be discussed here. The process block can be divided into five separate steps, i.e. five different tools are required. Figure 1.9 gives a schematic illustration of the five steps.

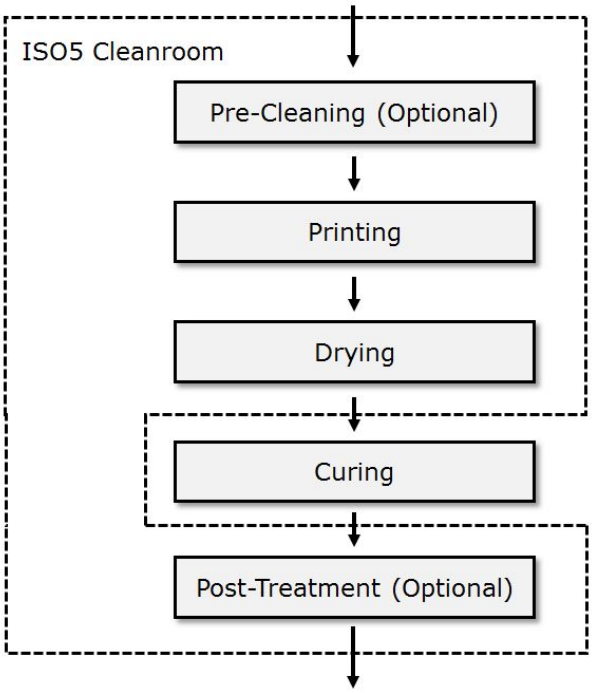


FIGURE 1.9: Schematic illustration of the general process flow of the paste metalization block.

At the beginning of the process block, the wafers are covered with a layer stack of PVD deposited barrier layer metals and a copper seed layer[2]. Examples for such stacks can be found in table 3.9 or table 3.10. Depending on whether the copper paste is to be applied to the front-side or the back-side of the wafer, the wafers are either in thick state, stabilized with a TAIKO-ring[3] or thinned and stabilized with a glass-carrier.

Figure 1.10 shows a sketch of the cross-section of the three different wafer types. Thick wafers and TAIKO-ring wafers are printed on the front-side, whereas the glass-carrier stabilized thin wafer is printed on the back-side, i.e. the wafer depicted in 1.10c would need to be flipped. The glass-carrier (pointed area) is attached to the wafer front-side

[2]The term seed layer is originated in the galvanic deposition method for copper, which requires a seed layer onto which the copper atoms are being deposited.

[3]A TAIKO-ring stabilized wafer consists of a large active area in the center of the wafer, which is thinned down to the desired thickness, and a 2-3 mm thick ring of 400-600 μm Si-thickness around the active area.

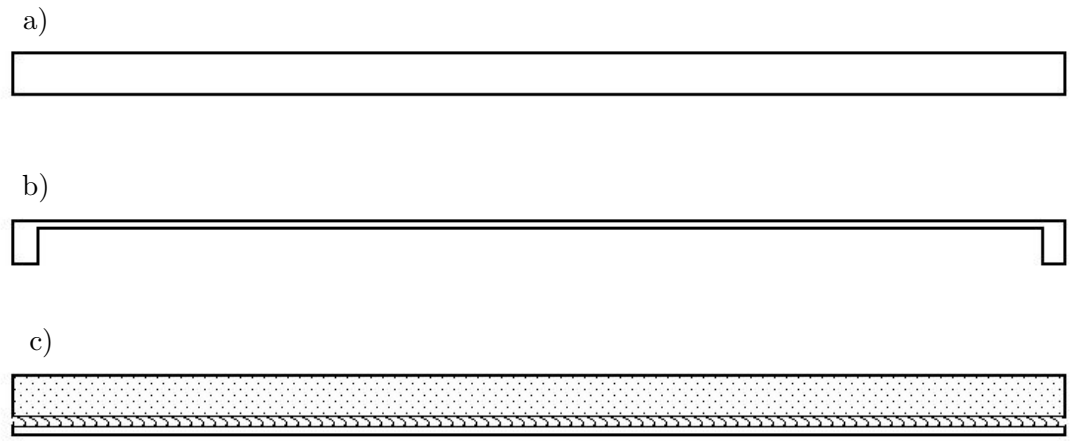


FIGURE 1.10: Different types of wafers: a) thick wafer, b) thin wafer stabilized with TAIKO-ring, c) thin wafer stabilized with glass-carrier (dotted area). The wafer front-side is always up, i.e. in case of c) it is pointing towards the glass-carrier.

with a glue (dashed area), which has a limited thermal budget, as will be discussed in section 3.3.4.

Depending on the application, a pre-cleaning step (plasma or wet-chemical) might be necessary to remove residues from previous processing steps. The printing is done on a DEK Horizon i02 shown in figure 1.11, which is connected to a WaferMate 200 wafer handler. The system is capable of printing 150, 200 and 300 mm wafers, although the wafer handler can only supply wafer sizes up to 200 mm. Larger wafers need to be inserted manually into the interface between the printer and the handler.

FIGURE 1.11: Used printing equipment DEK Horizon i02 with WaferMate 200 wafer handler from CHAD Industries.

The printing process itself can be divided into the wafer handling, the wafer alignment, the actual printing and the stencil-cleaning phases. During the handling steps, the wafer handler takes one wafer from the cassette, moves it to a pre-aligning stage where the wafer is centered and rotated to a defined notch orientation and then places it on the so called printer pallet, which is located in the interface between the printer and the handler. The printer pallet consists of a vacuum chuck that holds the wafer in place and a shim, which is a metal plate with a wafer-size whole in the middle. The shim is surrounding the wafer, serving as mechanical support during the printing process, as can be seen in figure 1.12. Once the handler is communicating to the printer that the wafer is in place, the printer pallet is moved into the DEK printer, where a camera is aligning the stencil to the alignment-marks on the wafer with a precision of $\pm 25\,\mu$m. The wafer is then lifted and brought into contact (or close proximity) with the stencil. A stencil is a metal (e.g. stainless steel or nickel) mask with defined openings, through which the copper paste is pressed by a moving squeegee. It passes over the wafer once or up to four times, depending on the predefined settings. More on the printer settings will be discussed in section 3.2.1. The wafer is then lowered from the stencil with a defined speed and removed from the printer towards the handling station, where it is placed in the cassette again. The printer will then perform a stencil back-side cleaning sequence, which will be described in section 3.2.1.1.

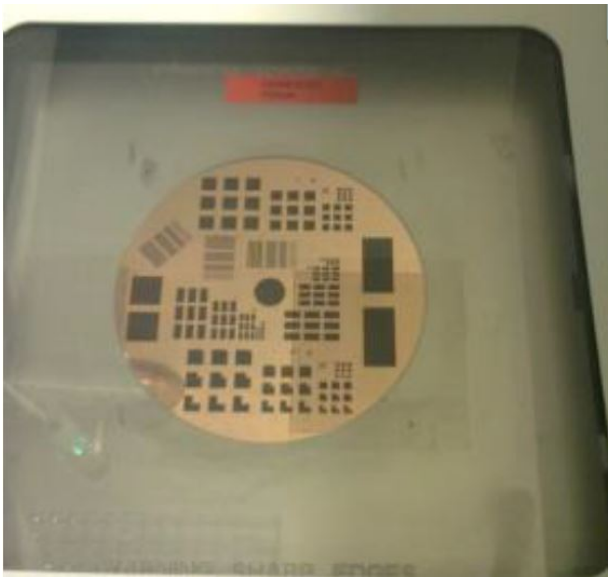


FIGURE 1.12: Wafer with test structures on the printer pallet, surrounded by the shim.

As soon as the last wafer has been printed, the cassette is removed from the wafer handler and inserted into a drying furnace. In this furnace, the organic solvents of the paste are

removed by evaporation at 60 °C for typically 30 minutes. As indicated in figure 1.9, the wafers are then being removed from the clean-room, since the curing furnace is located in the maintenance area. This is due to the experimental nature of this metalization block and would need to be changed for a productive application. The curing process is performed at 200-400 °C under formic acid, as will be discussed in detail in section 3.2.3.

The wafers are then being returned to the clean-room where they either undergo a sequence of post-treatment processes or are directly forwarded to the next operation on the respective work-route[4]. A post-treatment might for example be necessary in case of special structuring methods, as will be discussed in section 3.2.2 or section 3.2.3.

[4] A work-route is a kind of blueprint that contains all the required operations for a specific semiconductor technology to be manufactured.

Chapter 2

Characterization

The basic material for generating porous copper layers by printing techniques is the copper paste. Such pastes are commercially available on the market since the first years of this century. Copper is becoming an alternative to silver in printed electronics applications due to its lower price. On the other hand, the tendency of copper to oxidize and the high resistivity of copper oxides is demanding for special manufacturing techniques and particle coatings. Copper pastes are therefore high-tech products, and the exact composition and production conditions of such is a well-kept secret of the paste manufacturers.

To introduce printed copper pastes into semiconductor manufacturing, it is crucial to understand the behavior of these pastes under processing conditions in order to optimize the final product properties. Since the amount of information that is provided by the manufacturers was regarded insufficient, analyses were done to find out more about the components and their relative amount in the paste formulation. Especially the behavior of the organic components of the paste during the curing process is of crucial importance, since the complete removal of all organics from the copper matrix is important for many reasons. The term curing refers to the transition of the loose copper particles embedded in a binder system into a porous copper network by the formation of sinter necks due to heat impact. This topic will be dealt with in detail in section 3.3.

Once the curing furnace treatment is done, a porous copper network has formed as a final product of the process. The physical properties of this porous copper layer are most important for the technology integration and hence need to be characterized. Examples

for important physical properties are the porosity, the electric and thermal conductivity, the surface roughness and the thermo-mechanical stress. It is expected that there is an interdependence of those parameters with each other: layers of very high porosity might have a lower electrical conductivity, whereas they exhibit lower thermo-mechanical stress. Especially those two properties are in the center of attention, since the lower resistivity compared to aluminum was one of the major reasons for the introduction of Copper into the semiconductor industry, while the thermo-mechanical stress is a key property in manufacturing (wafer and chip bow) and in reliability. Different technologies might emphasize the importance of one of those two properties to a different extent, which is why it is important to understand how they are connected, how they can be influenced and which other parameters might be affected.

The material characterization cannot be considered isolated: As discussed in section 1.6 of the thesis introduction, it is in a constant feedback loop with process development, since the material properties are the output parameters of the processes applied to the paste. Hence, whenever the process is changed, the material properties will change. This is especially important to mention when dealing with new pastes. When a new paste is characterized in order to determine whether it offers a benefit over old materials, this paste is usually processed with the process parameters gained from optimizing the old materials, but of course, different pastes require different processing conditions in order to achieve optimal results. One of the major output parameters was always the specific resistivity, as it is easy to measure and of high importance for every technology. It is possible that a new paste that is compared to an old one by using a furnace process that has been optimized for the old one will not outperform its predecessor, although it would do so after optimizing the process. Process optimization is usually done by a design of experiment (DoE), which requires a large experimental setup to investigate the influence of each of the many possible process parameter settings. Material characterization again is the operation, that generates the response parameters of such a DoE.

Some of the experiments described in this chapter were performed by research partners or expert engineers at Infineon Technologies, who are typically embedded in the FA (failure analysis) teams of different company sites. The respective person or institution will be mentioned for each experiment.

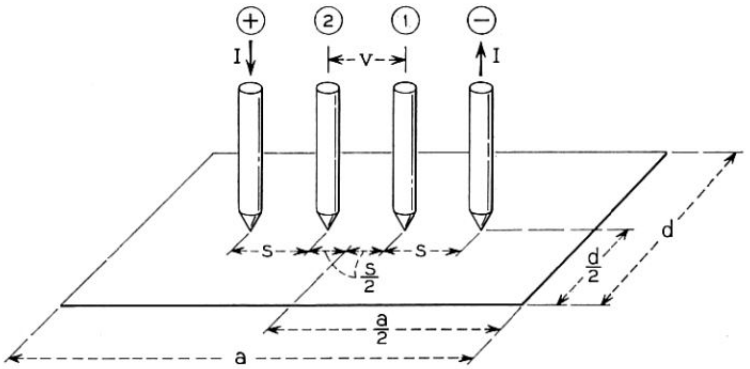


FIGURE 2.1: Schematic drawing of a 4PPM measurement taken from literature [45].

2.1 Specific Resistivity

One of the most important material properties for a metallisation layer is its low specific resistivity, which was the main driver for the still ongoing change from aluminum to copper metalization (3.1 $\mu\Omega$cm vs. 1.7 $\mu\Omega$cm respectively). It is a measure for how easily electrons are transported within the material, and is also connected to the conduction of heat over the Wiedemann-Franz law. Therefore, it is a crucial property for contact pads as well as pure heat sinks. There are two principal methods for the measurement of the specific resistivity: The four-point-probe (4PPM) [45] and the Van-der-Pauw (VdPM) measurement [46]. Detailed explanations as well as a practical comparison of those two methods on porous surfaces can be found in the thesis of C. Travan [47] and will just be summarized briefly here:

In the 4PPM method, four probes are placed in line at defined distance towards each other on a flat surface of the material to be measured, as shown in figure 2.1. The underlying mathematical model needs some assumptions to be made in order to deliver correct results:

- The material has a uniform resistivity in the area of measurement
- There is no considerable surface roughness
- The four probes are oriented in a straight line
- The contact area of the probes is negligible compared to the distance between them
- The surface is infinite and without defects

The VdPM method also uses four probes that are placed on the sample, but here the probes need to be placed on the edge of the sample in an arbitrary position and distance towards each other. Again, some assumptions need to be made for the mathematical model to be valid:

- The contacts are at the edge of the sample
- The sample has a uniform thickness
- The contact diameter is very small
- The surface is not disturbed by any cracks or holes

Considering these very similar assumptions, it is clear that a porous material does not qualify by definition for a 4PPM measurement or a VdPM measurement, which is why resistivity results on such surfaces need to be evaluated carefully. Travan [47] was therefore comparing the results of a 4PPM measurement with the results of a VdPM measurement, as well as comparing them with theoretical models for porous materials from Mori-Tanaka [48] and Ashby [38].

Basically, porosity influences the conductivity in a material in two different ways:

1. The presence of pores reduces the cross-sectional area of conduction, leading to an increase of current density in the connected pathways.
2. The pathway for the electrons from source to destination is prolonged, since the electrons need to travel around the pores.

Considering those two effects, it is intuitive that the resistivity of porous materials will be increased compared to their non-porous counterparts. In general, the electrical conductance G of a material can be described by equation 2.1, with σ_S being the electrical conductivity, S_0 the cross-sectional area and L_0 the length of the specimen.

$$G = \sigma_S \frac{S_0}{L_0} \tag{2.1}$$

For porous materials, either the change in electrical conductivity of the material must be considered within this formula, or the effective cross-sectional area has to be inserted [49]. Depending on whether the porous material has an open or a closed cell structure,

the effect on σ_S can be described by different mathematical models. Travan [47] found the best conformity of experimental data acquired with 4PPM measurement with the Mori-Tanaka model (see equation 2.2).

$$\sigma = \frac{(1-\Theta)}{(1+k\Theta)}\sigma_S \tag{2.2}$$

In this equation, Θ is the porosity and k is a constant related to the geometrical pore characteristic of the porous metal [50]. Spherical pores would be described by a k of 0.8, whereas Travan found that the ethylene glycol based pastes best fit the model with a k of 4.2. Figure 2.2 shows the data of Travan, as well as later experimental data on ethylene glycol based pastes, isoprenoide based pastes and literature values of porous materials taken from [51].

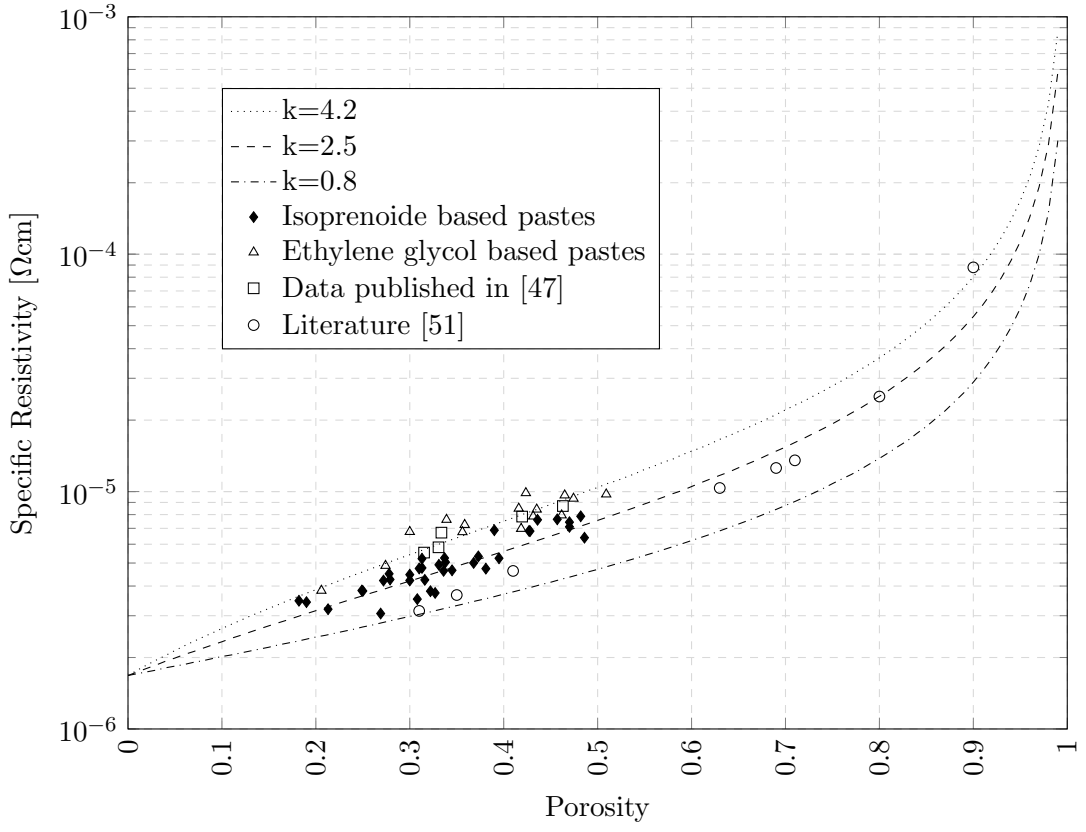


FIGURE 2.2: Specific resistivity vs. porosity of different materials with reference values from [47] and literature values from [51] compared to theoretical prediction of a modified Mori-Tanaka model [50]

The ethylene glycol based pastes are very well in line with the findings of Travan, whereas the isoprenoide based pastes fit the Mori-Tanaka model with a k value of 2.5. Literature

data on the other hand data does not seem to fit the model. Travan also compared the results of 4PPM measurements with values obtained by the Van-der-Pauw method and could find good conformity of the two measurement types. Slightly higher values of the Van-der-Pauw measurements could be explained with insufficient contact of the wedge-bonded gold wires to the copper surface, as was confirmed with SEM analysis [47].

As a conclusion it can be stated that the specific resistivity of printed porous copper layers has a linear correlation with porosity within the porosity range of interest between 20 and 50 % (see figure 2.2). Experimental data fits the Mori-Tanaka model for closed cell porous materials. The plausibility of the measured values could be confirmed by a reference measurement on the same samples with a second method, thus suggesting to continue with the 4PPM measurements as it is easier and faster to apply than the Van-der-Pauw measurement.

2.2 Porosity

The possible methods for the measurement of porosity are manifold. Due to the increasing importance of porous materials in science and engineering, the development of non-destructive means to determine the degree of porosity in a specimen has seen rapid progress. A classical and extremely useful method is the mercury intrusion porosimetry: Liquid mercury is pressed into a specimen, and by measuring the pressure change and the volume of mercury inserted, the volume of open pores can be calculated for a sample of known surface tension and contact angle with mercury [52]. Since mercury does not moisten many surfaces, the liquid is repelled by the material (i.e. forms a large contact angle), demanding for higher pressure to fill the smaller pores. Hence, the change in volume in dependence of the pressure also gives information about the pore size distribution [53]. In a similar approach, the toxic mercury can also be exchanged by a number of suitable gases, in the simplest scenario even air [54]. In case of the use of hydrogen as gas, neutron radiography can be used, which is a sensitive and quantitative method for the detection of hydrogen. This method has been successfully used on rocks [55]. Also other sources of radiation like X-rays (computer tomography, CT) or infra-red radiation can be as an alternative [56]. Indirect methods can be suitable for porosity measurements, but are strongly material dependent. An example for an indirect method

would be the measurement of the porosity dependent electrochemical characteristics of protective coatings [57]. Such methods are usually very sensitive towards impurities in the material and hence together with their stringent limitation towards particular materials do not qualify for a broad use.

2.2.1 Optical Porosimetry

A straight-forward method to determine porosity is the optical determination of the pores in SEM. The acquired SEM images are converted to binary images using defined thresholds. A software tool containing a suitable algorithm can then measure the area of pores in the image [58]. A proprietary software program employing this method is also in use within Infineon Technologies. It was programed on the basis of the Halcon 11 image processing library from MVTec GmbH. For proper functioning, the software needs to be calibrated with reference samples with defined porosity determined by the gravimetric method (see next section 2.2.2). Unfortunately, it could not be successfully adapted for printed copper layers due to the fact that the contrast in SEM pictures is also dependent on grain orientations, which are hard to reproduce and hence would require a huge statistical reference database. Figure 2.3 shows an exemplary FIB cut as it was used for the failed attempts to determine porosity with an optical method.

As mentioned before, the orientation of the copper grains in the specimen have strong influence on the contrast in SEM. Although the magnitude of this effect can be influenced by changing the weighting of the different detectors (back scattered electrons vs. secondary electrons), the effect was still too intense for the algorithm to reliably detect the pores. Also, a cross-section image is not able to give information on the depth of a pore, which means that even a large hole in the layer could be detected as a small pore if the cross-section has been made at an unfortunate position. Again, the severity of this effect to the correctness of the result can only be reduced by statistical information on the particular sample type. Therefore, this method is not suitable for the screening of different material types, but rather finds application as ex-situ quality control measure for a productive process. In the stage of development, the effort of building up a database containing the required statistical information is not compensated by the advantages of this method. To give an example, for the characterization of another porous system,

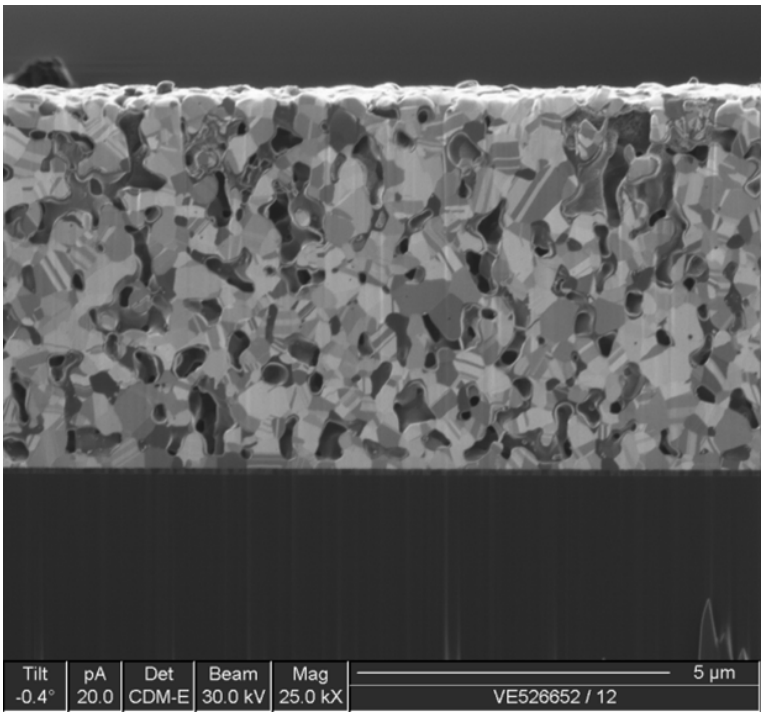


FIGURE 2.3: SEM image of a FIB cut copper paste CP-INF-240415-R1.

which is already used in commercial products, more than 600 cross-section pictures of 31 samples were used [59].

2.2.2 Gravimetric Porosimetry

A robust method to determine the relative density (i.e. the porosity) of a material, which does not require calibration is the gravimetric porosimetry. It is a destructive method that uses etching chemistry to remove a porous layer of known area and thickness and measure the weight difference of the substrate. Typical samples used in this thesis for this method were thick dummy wafers that have been cleaved to $30\times30\,\mathrm{mm}^2$ pieces. The thickness of the porous copper layer on those samples was measured either by SEM or, more commonly, by optical microscopy. Therefore, a piece of around 5 mm thickness was broken off to generate a clean break edge. The rest of the piece was then scanned with a conventional office scanner (in use was a Ricoh MP C3003) with a resolution of 400 dpi together with a scale. The area of the piece was then determined by using the scale and measuring in a digital image analysis software like ImageJ[1]. Repeated measurements on the same samples were repeatable with a typical error of less than

[1]ImageJ is a free software that has been developed by an employee the US National Institute of Health. It is not subject to any copyright.

2 %.The area multiplied with the measured layer thickness then gives the volume of the copper layer.

In a next step, the piece is weighed on an analytical scale (precision ±0.1 mg) and then etched with a proper etching solution. Such a solution can either be a standard copper etching solution like shown in table 3.4, or since no proper etch control is needed, it can be 65% technical grade nitric acid. In any way, one ends up with a blank silicon piece with just the barrier left on. This piece is then weighed again to gain the substrate weight, which is then subtracted from the previously gained over all weight. With the weight and the volume of the copper layer being known, it is then possible to calculate the density of the material, which then gives the relative density of the layer if compared to the literature value for copper.

The advantage of this method is clearly that it can be performed with "in-house" methods, since no equipment else than an analytical scale, a microscope and an office scanner are being required. Also the amount of time that is necessary for the measurement is rather short, within a day dozens of samples can be analyzed in parallel. This is for sure one big advantage over other methods like gas adsorption or mercury porosimetry, where complicated machinery is needed to analyze a single sample. Also, compared to those methods, enclosed pores do not influence the measurement in the negative. One of the biggest disadvantages of gravimetric porosimetry is its susceptibility to errors by measuring wrong layer thicknesses. The layer thickness can vary by several micrometers due to surface roughness and poor uniformity, which can easily be up to 10% of the overall layer thickness. Uniformity describes the layer thickness distribution over a wafer. It is calculated according to equation 2.3, where d_{max} and d_{min} are the maximum and minimum and avg. is the average measured layer thickness. For a homogeneous deposition, the uniformity should be as low as possible, at least below 20%.

$$Unif.[\%] = \frac{d_{max} - d_{min}}{2 \times avg.} \times 100\% \tag{2.3}$$

Additionally, the breaking of the samples creates edges that are not sharp as if they were in case of cutting or grinding the edge, which means that the topography of the edge is problematic for the depth of focus of optical microscopes. With the thickness being a multiplicative factor in the formula for the porosity, this leads to large scattering of

the results, which makes it necessary to reduce this error by statistics. Typically for the characterization of new pastes or new furnace processes, 9 pieces per wafer from different positions (center-edge) were measured, which is one third of the samples gained from the wafer.

2.2.3 Micro-Computed Tomography μCT

When it comes to characterizing the microstructure of closed cell porous materials, any method that relies on intrusion of another material into the porous network like mercury or gas intrusion porosimetry is no longer suitable. To gain insight into the pore structure, the depth-dependent pore size distribution as well as the ratio of open to closed pores, micro computed tomography (μCT) is the method of choice. For this method, x-ray projections of a sample are are taken from many angles around the sample, creating 2D cross-sectional images. Those images are then mathematically converted or "reconstructed" into a three-dimensional representation of the sample. For analysis, the reconstructed data, which is basically a stack of 2D images, needs to be segmented. Segmentation or also called binarisation is a process in which the voxels[2], which in case of 8bit images have 256 grey levels are converted into binary information [60]. In the binary image, in case of porous copper, one color would then represent copper, the other air. Segmentation is done by the setting of thresholds, in the simplest way a global threshold, which means that any level on the grey scale below the threshold will be defined as white, any level above as black. A state of the art μCT tool, the "GE Nanotom m", is located at the Materials Center Leoben (MCL) in Leoben, Styria. Measurements on the tool were carried out by J. Rösc in the group of R. Brunner, both of whom were also involved in the interpretation of the acquired data. The tool has a high resolution with voxel sizes of $0.753 \times 0.753 \times 0.753\,\mu\text{m}^3$. The analysis was performed with the commercial software Avizo Fire v8.1 (first series of samples) and v9.0 (second series). All the work on developing and refining the method of pore detection was carried out by MCL, in collaboration with Infineon Technologies AG. A summary on the results will be described briefly in the next paragraphs.

[2]In the field of computer graphics, a voxel represents a value on a regular grid in a three-dimensional state. The term voxel comprises of the terms volume, element and pixel.

2.2.3.1 Sample Preparation

In a first attempt to analyze a porous copper layer, the paste CP-131113-R1 was printed with a structured stencil on a bare silicon wafer coated with HMDS[3], which is a vapor deposited chemical to decrease the polarity of silicon. The poor adhesion of the copper paste on HMDS enabled an easy removal of the small, structured pads after the curing[4]. The sample was glued onto a holder and analyzed in the computer tomograph. Figure 2.4 shows a rendered 3D model of the sample with the detected pores. It can be seen that a region of interest (ROI) was defined to exclude the unsteady edges of the sample. The color code of the displayed pores is referring to their size, with purple for small, isolated and red for large interconnected pores. The picture shows a concentration of large pores in the area with higher layer thickness on the left side of the picture.

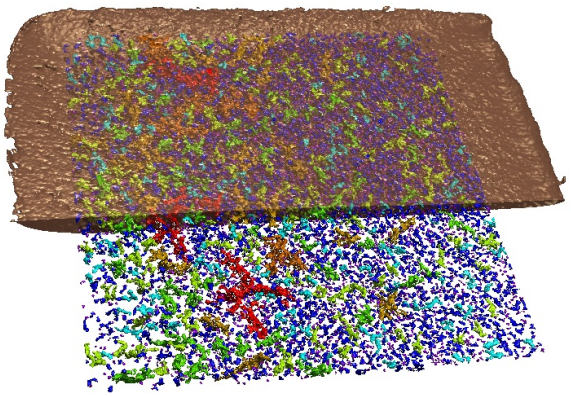


FIGURE 2.4: 3D model of sample MCL001 showing the detected pores.

There are several possible explanations for this effect, which could be related to the layer thickness, the printing direction, the removal process during sample generation or the size of the pad. Since for a first, general insight in the pore characteristics of printed copper the number of external influence factors on porosity should be minimized, this sample type seems not to be suitable. To avoid any influence of the afore mentioned parameters, the second learning cycle was done with full-face printed samples from the center of the wafer.

Therefore, a 200 mm wafer was coated with a sputtered 200 nm titanium and 300 nm copper layer and then ground down to 400 μm thickness. It was then printed full-face

[3]Hexamethyl disilane, CAS No. 1450-14-2.

[4]The curing process was performed according to figure 3.18 given in section 3.3.2 with a prolonged annealing time of 3h at 400 °C.

with CP-003, QNA6344 using a 50 μm Stencil. After drying with the standard procedure at 60 °C for half an hour, the paste was cured under formic acid vapor with a maximum temperature of 400 °C and an annealing time of 180 minutes. The wafer was then diced in a two step process: First, the copper layer was laser-diced using a 355 nm UV laser. Then, after having cleared the sawing streets of copper, the silicon wafer is singulated in a step-cut process with two different mechanical sawing wheels. The dimension of the pieces was about 500×500 μm. This small size is required in order to approach the detector of the μCT tool as close as possible to achieve the maximum possible resolution of 753 nm voxel size. A 3D picture of the acquired data is given in figure 2.5.

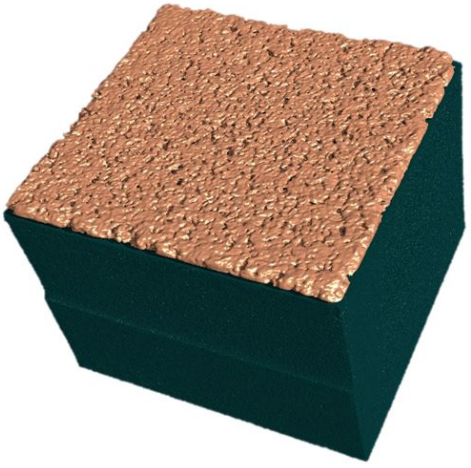


FIGURE 2.5: 3D model of sample MCL003.

As this method proved to be useful, all further samples were generated and analyzed in accordance to this procedure. The next step was to investigate the influence of the furnace treatment on the porosity of the pastes. Therefore, samples were taken at different points of processing. Table 2.1 gives an overview on all the samples and their processing conditions that were generated for the μCT measurements.

The first set of samples (MCL006-MCL011) was printed with a 50 μm stencil using CP-PLS-291014-R1, QNA6449. The wafer was then cleaved into pieces that were processed in the furnace separately. The furnace programs used in this trial were designed according to the optimized curing recipe for CP-PLS described in table 3.7. Based on this recipe, the furnace program was interrupted by a rapid cooling step after reaching 160, 200, 260 and 400 °C, as well as after 60 mins at 400 °C and after the normal recipe end at 180 mins, 400 °C. Those samples were then diced as described before and picked with tweezers by hand from positions close to the former center of the wafer.

Sample	Comment	Max. Temp.	Hold Time
MCL001	Old Paste CP-131113-R1	400 °C	50 min
MCL003	Old Paste CP-003	400 °C	180 min
MCL007 + MCL015	Begin of sintering	160 °C	0 min
MCL011 + MCL017	Max. Temp. for THB[5] resist	200 °C	0 min
MCL006 + MCL012	Max. Temp. for GC Wafers	260 °C	0 min
MCL010 + MCL013	Max. Temp., no anneal	400 °C	0 min
MCL008 + MCL016	Max. Temp., short anneal	400 °C	60 min
MCL009 + MCL014	Max. Temp., long anneal	400 °C	180 min

TABLE 2.1: Overview on the sample types dedicated to μCT investigations.

A scheme of the furnace process used to cure the samples MCL007-MCL014 is shown in figure 2.6. The shown furnace recipe was optimized towards optimal resistivity and bondability, as will be described in detail in section 3.3. The maximum temperature is reached at the end of step 3. The ramp rate in this step was always 5 °C per minute, i.e. in case of a maximum temperature of 400 °C, the step duration was 60 minutes as shown in figure 2.6. In case of a lower maximum temperature, step 3 was canceled e.g. after 20 minutes in case of the samples MCL011 and MCL017, which had a maximum temperature of 200 °C. Step 4 was completely skipped for these samples, whereas it was just shortened down to 60 minutes instead of 180 for samples MCL008 and MCL016. The abbreviations in the top part of figure 2.6 are giving information on which gas was used during this step, with FAV being formic acid vapor, N2 being nitrogen and Vac indicating an evacuation of the chamber down to 2 mbar.

As later results described in section 2.2.3.2 suggested, the copper layer thickness was too small for proper analysis, which is why the second set of samples (MCL012-MCL017) was generated by printing the same pastes on the same type of wafer, but using a 100 μm stencil. All the post-processing steps (cleaving, gravimetric porosimetry, dicing) were identical to the previous set of samples.

2.2.3.2 Sample Analysis

The copper layer thickness was determined by μCT as well as by optical microscopy, which confirmed the μCT measurements. The box plot in figure 2.7 shows the result of those measurements: the whiskers indicate the value of the highest and lowest value, the box shows the first and third quartile and the line in the center of the box gives the average layer thickness. It can be seen that the values scatter over a large range, which

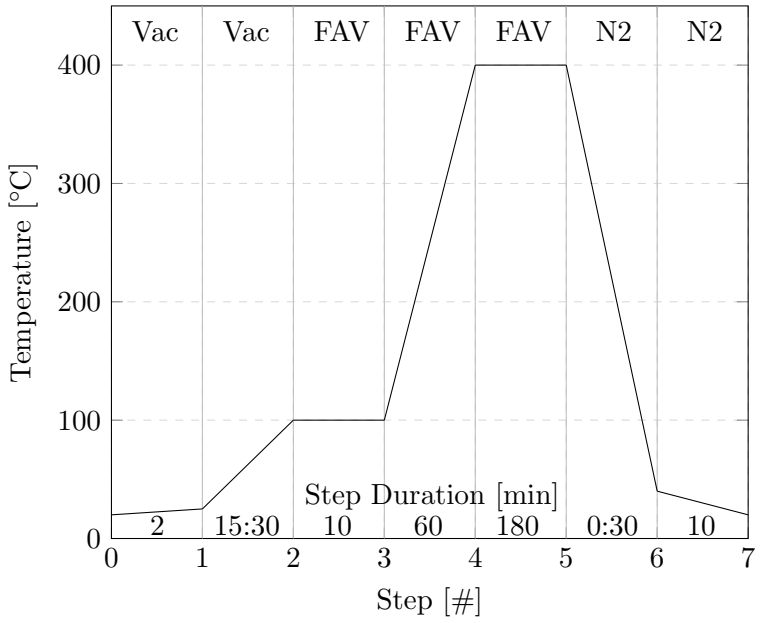


FIGURE 2.6: Optimized furnace recipe for CP-PLS-291014-R1 curing, including a plateau step (2) and an annealing step (4)

is an indication for poor uniformity and the high surface roughness of the samples, being caused by the microparticles as well as by cracks in the surface, as will be shown later.

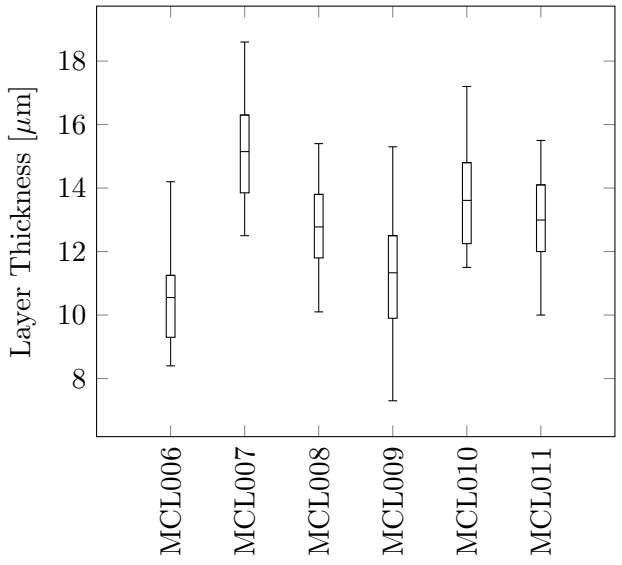
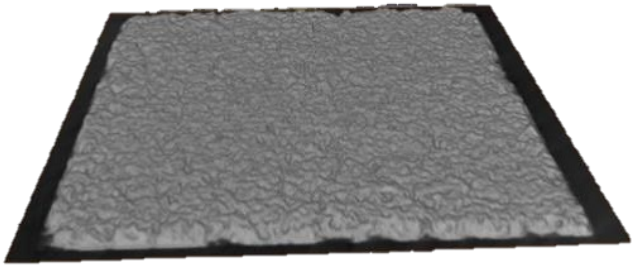


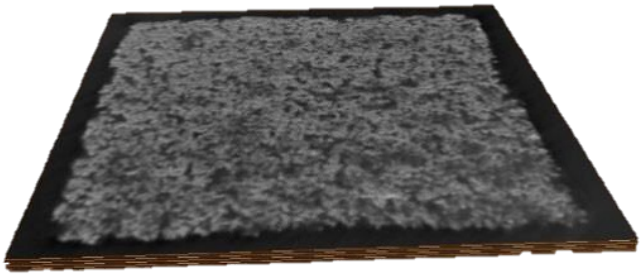
FIGURE 2.7: Box plot of the layer thickness of MCL006-MCL011 measured in μCT.

For the porosity measurement, first an algorithm for the pore detection had to be defined. The segmentation was done with a multi-level algorithm, which was specially adapted for the detection of very small defects. It was not solely relying on gray scale thresholds, but was using a so called "closing" operation to detect the position of the pores. Closing

operations are mathematical procedures for the localization of defects which typically rely on tensorial approaches [61]. After localizing the position of the defects (or pores), the gray-scale profiles of the voxels around the position are analyzed, based on which the voxels are identified as part of a defect or not. After determining the over-all porosity and assigning the pores to size categories, the data set was virtually cut into slices of three voxels, i.e. approximately 2.26 μm in order to analyze the depth dependence of the porosity. Figure 2.8 shows the volumes 1 (0-2.26 μm) and 5 (9.04-11.3 μm) of the sample. It can be seen that the porosity is decreasing with the depth of the layer. The ROI (region of interest) was set to an area of $435\times476\times8.3\,\mu m^3$ to exclude the effect of surface roughness and unsteady edges in the 13 μm thick layer. This ROI gave a porosity of 22.14%. For comparison, a larger ROI of $532\times531\times13\,\mu m^3$ resulted in a detected porosity of 28.55%.



a)



b)

FIGURE 2.8: Slices of sample MCL003 for porosity measurement. a) Slice 1 (0-2.26 μm), b) Slice 5 (9.04-11.3 μm).

Volume 1 has a porosity of 12.46%, while volume 5 already is 62.14% porous, which can be seen in figure 2.8a by the amount of dark areas in the pictures compared to 2.8b. For the overall porosity determination it is therefore critical to carefully define the last volume to consider, as the inclusion of the surface would increase the measured

porosity drastically, thus giving a false impression on the over-all porosity of the bulk material. For the last 3-6 μm of the layers it is more appropriate to speak of surface roughness instead of porosity. In case the limit is set to 13 μm, the total porosity is then as mentioned 28.55%. This is rather far away from the expected value of roughly 40%, which was expected from gravimetric porosity for this paste. Two possible explanations seem likely: first, the layer thickness determination in the gravimetric method is done by optical microscopy, which gives an uncertainty on very rough samples. Second, the μCT can only resolve relatively large pores due to the voxel size of 753 nm, which means that any pores smaller than that will not be detected at all. Hence, a residual deviation between gravimetric results and the μCT measurements will always be present, regardless of the threshold settings and the ROI.

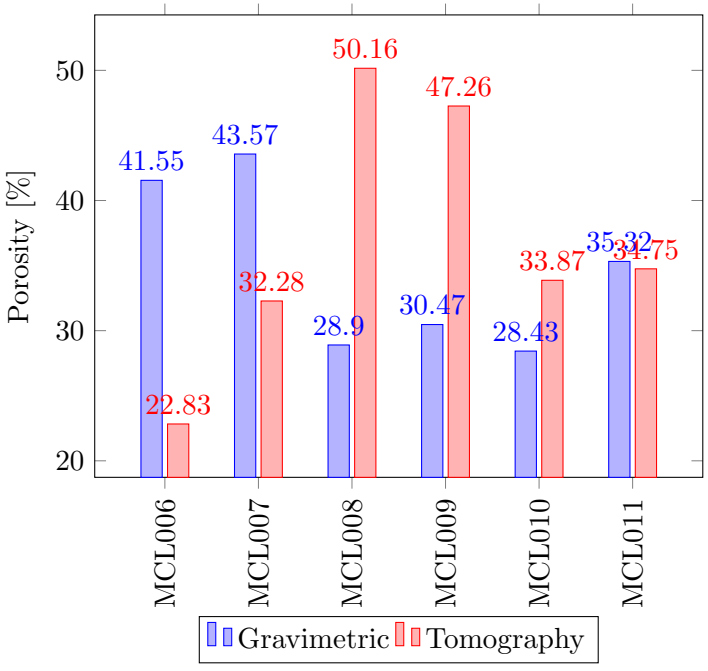


FIGURE 2.9: Comparison of the porosity of MCL006-MCL011 measured in μCT and by gravimetric porosimetry.

For the porosity measurement, the acquired tomography data was analyzed in volumes of 2.26 μm thickness. The total porosity of the layers is shown in figure 2.9, where it is also compared to gravimetric porosity measurements. As can be seen, there is no correlation of the porosity between the samples with vastly varying values between 22.83 and 50.16% in the μCT data, with no correlation to the gravimetric data. The reason for this is clearly the low layer thickness: some samples, e.g. sample 6 is so thin that only two layers can be analyzed by the algorithm. The depth dependency of the porosity is plotted in figure 2.10. As already shown on the example of figure

2.8, the upper most layer cannot be regarded as porous anymore, but consists only of some protruding copper particles contributing to surface roughness. Since the algorithm cannot distinguish between surface roughness and porosity, the border has to be set by the operator. In case of sample MCL006, only the first two layers would be analyzed, in sample MCL007 also the third and the fourth layer would be taken into account.

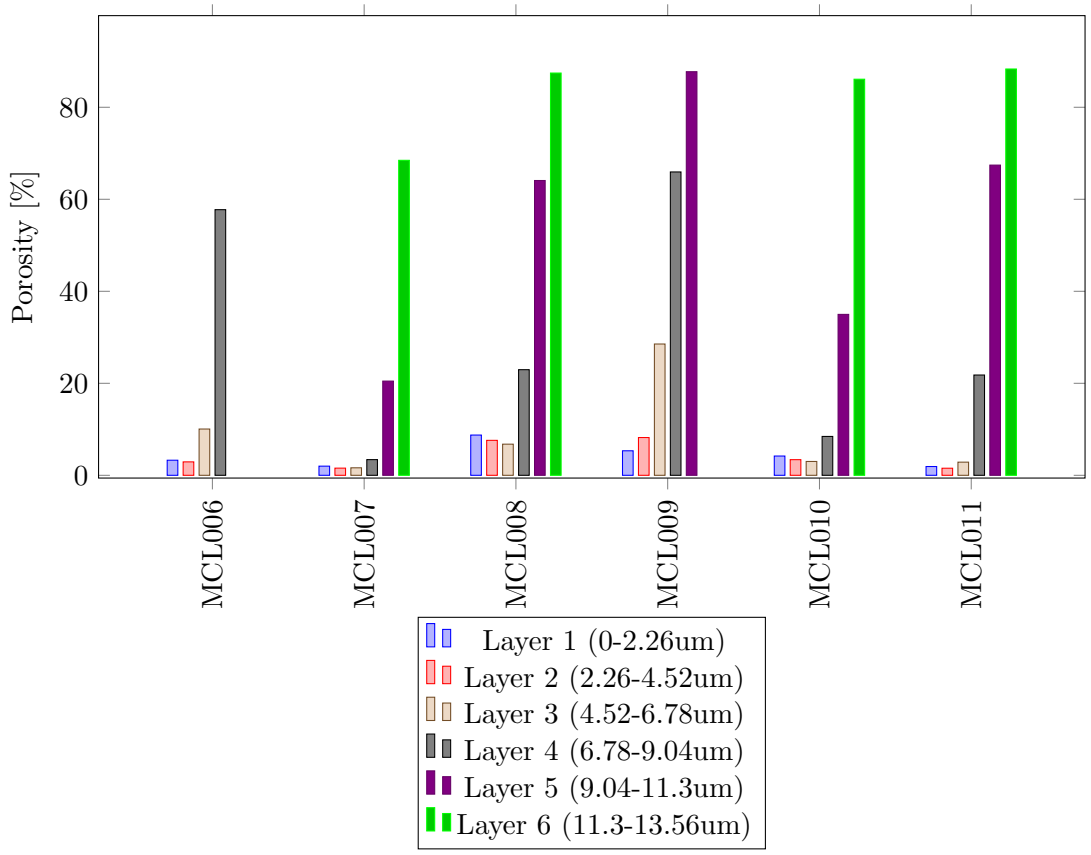


FIGURE 2.10: Depth dependence of the porosity in the samples MCL006-MCL011.

The outcome of those trials was therefore, that much thicker layers are needed for a proper analysis, as has been realized in the samples MCL012-MCL017. For a lack of resources, only the samples processed with the technically most relevant processes were analyzed in μCT: MCL012 (260 °C, process for thin wafers), MCL013 and MCL014 (400 °C without and with annealing time of 3h). The layer thickness of those samples was 20.0, 18.1 and 21.1 μm, respectively. Again, the surface roughness of the samples interfered with the porosity measurements, but in this series, six layers could be used for the analysis. Figure 2.11 shows a rendered 3D model of Sample MCL012 which gives a good impression on the high surface roughness of the printed layers.

The porosity data measured on samples MCL012-MCL014 is listed in table 2.2. Again,

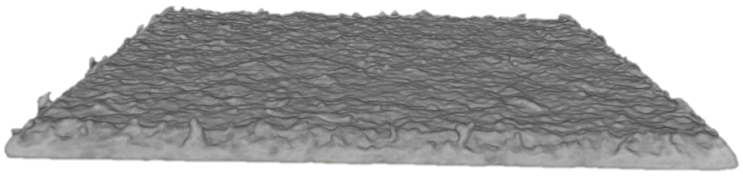


FIGURE 2.11: 3D model of sample MCL012.

the values are much lower than the data from the gravimetric measurements, which as previously discussed might be due to the poor detection of micro pores. Still, the higher sample thickness gives more confidence in the results and allows a first interpretation. The novelty of this method for the 3D porosity determination of porous copper together with the small amount of samples analyzed with it leaves the question on the reproducibility of the results open. It is unclear, whether e.g. the difference of 17.44% and 17.02% (MCL013 and MCL014) is significant or not. This question cannot be answered without a thorough statistical analysis of this method.

Sample	Furnace Treatment	Porosity in μCT
MCL012	260 °C, 0min	12.29%
MCL013	400 °C, 0min	17.44%
MCL014	400 °C, 180min	17.02%

TABLE 2.2: Process parameters and porosity values for the samples MCL012-MCL014.

Assuming that the difference between MCL013 and MCL014 is not statistically relevant, it is interesting to see that the porosity seems to increase between MCL012 and the other two samples. This is contra intuitive, since the sintering and annealing of the particles is accompanied by a shrinking layer thickness, as Eichinger has shown in [62]. A reduced layer thickness would suggest increased density of the material, hence reduced porosity. One possible explanation for this could be interference of hydrocarbons with the threshold setting of the algorithm: the TGA curves of the paste CP-PLS-291014-R1 2.15 shows a mass loss of several percent at around 300 °C, which means that there is still organic material in the layer after processing it at 260 °C like it was done on sample MCL012. This material could be detected as matrix by the algorithm, and the lower density of hydrocarbons compared to copper could explain why a small percentage of mass would disproportionately reduce the pore volume.

2.2.4 Conclusions and Outlook on the Porosimetry of Porous Copper

Summing up the results of the μCT measurements, it is necessary to have a minimum layer thickness for the method to deliver good results. Since it is hard to discriminate between open pores and surface roughness, the detection of open pores is a challenge to this method, also since the definition of where an open pore starts might be uncertain in general. The sample preparation method proved to be reliable, which means that in future a larger quantity of samples could be analyzed by X-ray tomography, which would enable an assessment on the repeatability of the results. Further refinement of the method could be achieved by improving the segmentation algorithm, as well as using non-commercial, tailor-made software tools.

The correlation of gravimetric with μCT data failed. As mentioned above there is a list of possible reasons for this, which should also be assessed in future trials with a larger statistical basis. The poor coherence of the two data sets does not necessarily mean that one of the two methods is wrong, just that they do not analyze the same material property. One weakness of the gravimetric porosimetry is that it cannot distinguish between copper and other materials, i.e. that on samples which contain other metals or organics the results will be compromised. Micro tomography also has difficulties with other materials that might interfere with the threshold setting, but could detect them by their gray scale value if the method would be calibrated for that task.

Another down-side of the gravimetric method is its dependence on the layer thickness measurement, which is typically done with optical microscopy and bears a large uncertainty due to poor layer uniformity and high roughness. In the microscopical layer thickness measurement, typically the top of the copper particles is taken as the upper measurement value, which means that the high porosity of the upper most layer is included in the overall value. This is another important reason for the difference to the μCT data.

In the end, both methods still have their legitimacy: The μCT for sure delivers results with a higher level of confidence and more information on the layers than just a single number, but it is a time and cost extensive method that requires special sample preparation. Gravimetric porosimetry on the other hand only gives a very rough indication on the porosity of the layer, but it is fast, versatile and can be very useful when comparing different layers to each other. In this thesis, any porosity value outside

of this chapter was determined by gravimetric porsosimetry. Deeper investigations on the micro-tomographic analysis of porous copper foams is subject of a subsequent PhD thesis.

2.3 Chemical Component Analysis

Due to the high complexity of semiconductor devices even small amounts of undesired substances can already have a severe impact on their functionality. Ionic substances like sodium or potassium can easily penetrate insulation layers like oxides and alter the dielectric properties [63] of such layers, often in an undesired way. Anions like chlorine or flourine can lead to corrosion of metallic layers [64], [65]. Organic contaminants may lead to electrical problems in the device [66], adhesion problems of subsequent layers [67] or undesired masking effects during wet-chemical etching, as shown within this thesis (section 3.4.2). In order to assess the risk that is imposed by the introduction of a new material, knowledge about its qualitative and quantitative composition is crucial. The material safety data sheet [68] as well as the certificate of analysis [69] (see Appendix for figure A.2) does not give any details on the constituents of the pastes other than copper and "alcohols". Hence, a detailed analysis on the components of the paste as well as on any residues within the cured layers needs to be made.

2.3.1 Anaylses of the Pastes

According to the manufacturer Intrinsiq Materials Ltd., all copper printing pastes consist of organic solvents, binders, glass frit, copper micro-particles and copper nano-particles. The exact composition of the solvents and binders, as well as the particle size distribution of the copper powder is considered company confidential and was not disclosed. The organic components were exchanged in December 2014 upon a request from Infineon for a lower curing temperature. According to the material safety data sheet of the old paste CP003, the organic solvent used up to then was ethylene glycol [70]. The MSDS of the new pastes only mentions "alcohols" without further specification [68], but as it will be shown in the upcoming chapter, the main organic components of the new pastes are terpineol and other isoprenoides. Therefore, when speaking of ethylene glycol based pastes, all the pastes available before December 2014 are meant, while isoprenoide based

pastes denote all the pastes developed after that date. Table 2.3 gives an overview on the most important pastes investigated within this thesis.

Ethylene Glycol based Paste	Isoprenoide based Paste	Comment
CP-003	CP-PLS-291014-R1	Standard Paste
CP-131113-R1	CP-INF-240415-R2	-
CP-181113-R1	CP-INF-240415-R3	-
CP-LT-120614-R2	CP-INF-240415-R1	pure nanoparticle paste

TABLE 2.3: Overview on the different pastes investigated within this thesis

2.3.1.1 Inorganic Components

The first available paste CP-003 was commercially available, but has been improved in terms of purity as part of the ongoing cooperation with Intrinsiq Materials. For example, according to ICP-MS data obtained by Z. Kroener, the lead content within the CP-003, QNA6085 received in September 2013 was 6.36%, which was reduced in the next batch CP-003, QNA6299 down to 0.14% in June 2014. The differences in purity are illustrated in figure 2.12. The overall amount of other metals contained in the paste was reduced from 6.44% to 0.47%, which resulted in a significant drop of specific resistivity from an average of 14.20 $\mu\Omega$cm down to 8.10 $\mu\Omega$cm.

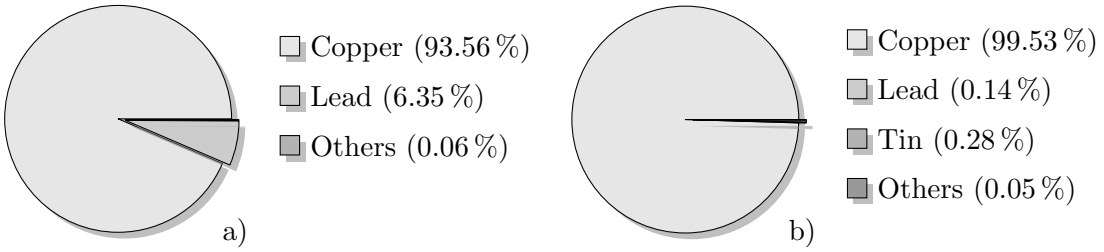


FIGURE 2.12: Composition of CP-003, QNA6085 (a) and QNA6229 (b) according to ICP-MS data.

The reduction of the specific resistivity by reducing the amount of impurities is a well known effect that is also described by Matthiesen's rule, based on the work of Augustus Matthiesen in 1864 [71]. According to him, any impurity will reduce the conductivity of a given metallic material due to scattering of the electrons. The result is that in general, the conductivity of an alloy is lower than the conductivity of any of the pure constituents. Figure A.1 attached in Appendix A shows the resistivity of the Copper-Nickel system at different temperatures to give an impression on the magnitude of this effect.

ICP-MS results of the paste CP-PLS-291214-R1 show that the amount of impurities could be reduced down into the thousandth region. According to internal ICP-MS analyses done on this paste, Batch QNA6449, the amount of non-copper atoms in the sample accounts to only 0.02%, the majority of which being lead (75%), whereas a reference ICP-MS measurement done at SGS Fresenius showed a non-copper atom content of 0.03-0.35%, with lead making up 5-30% of the impurities. SGS Fresenius found large inhomogenities within the sample: The calcium content varied between 0.006 and 0.22 at%, or 1400 and 36 mg/kg. As ion-chromatographic results (figure 2.13) show, the calcium is present in a form that is not water soluble, e.g. calcium carbonate. The determination of the exact nature of the calcium in the paste was not within the scope of this thesis, the most important information is that it is not present in ionic state.

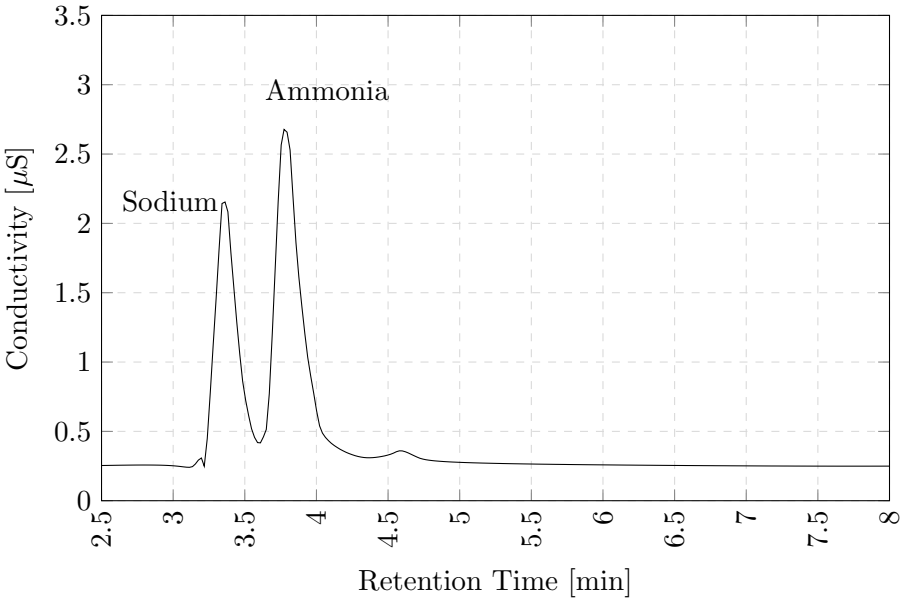


FIGURE 2.13: Ion chormatographic spectrum of the cations in CP-PLS-291014-R1.

Intrinsiq Materials claims to coat its copper nano particles in a way that there is no significant amount of copper oxide present, without revealing the exact coating method. For the micro particles, they do not give any information to what extent they are oxidized. One of the surprising results of a powder diffraction analysis, which was performed to measure the crystallite size of the copper pastes, was that the copper(I)-oxide, Cu_2O, is present in the pastes of up to 62%. This result shows clearly that a reductive atmosphere is necessary to cure the paste layers, when low specific resistivity is required.

The Cu_2O contents of the investigated isoprenoide based pastes can be found in table

Paste	Batch	Cu_2O content
CP-INF-240415-R1	QNA6591	48%
CP-INF-240415-R2	QNA6592	44%
CP-INF-240415-R3	QNA6593	62%
CP-PLS-291214-R1	QNA6483	54%

TABLE 2.4: Oxide content of different copper pastes determined by powder XRD.

2.4. There are significant differences between the pastes, the average Cu_2O content varies between 44 and 62%. Figure 2.14 shows the powder X-ray diffraction pattern of the paste CP-INF-240415-R1, QNA6591. The peaks at 36.5 and 61.5 are correlated to the Cu_2O. The mass ratio was determined by Prof. Roland Resel from TU Graz with the Software tool TOPAS.

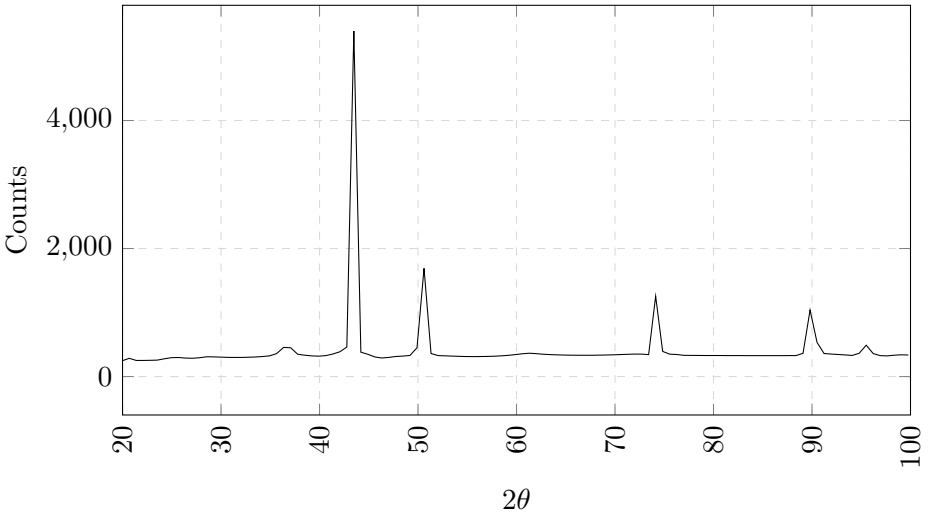


FIGURE 2.14: Powder X-ray diffraction pattern of copper paste CP-INF-240415-R1, QNA6591.

2.3.1.2 Organic Components

The main reason why the organic components are of interest is because they need to be removed from the layers as efficient as possible. Knowledge on the chemical nature of the substances could help creating a suitable furnace recipe for an efficient drying process. A standard method to get an overview on the substances included in a sample, the temperatures at which they evaporate and their amount compared to the non-volatile components is the thermogravimetric analysis (TGA). For comparison, figure 2.15 shows TGA curves of CP-003, QNA6299 (a) and CP-PLS-291214-R1, QNA6393.

The curves were acquired in Regensburg by H. Preu, the ramp rate was $10\,^{\circ}\mathrm{C}\cdot\mathrm{min}^{-1}$ and the atmosphere was nitrogen.

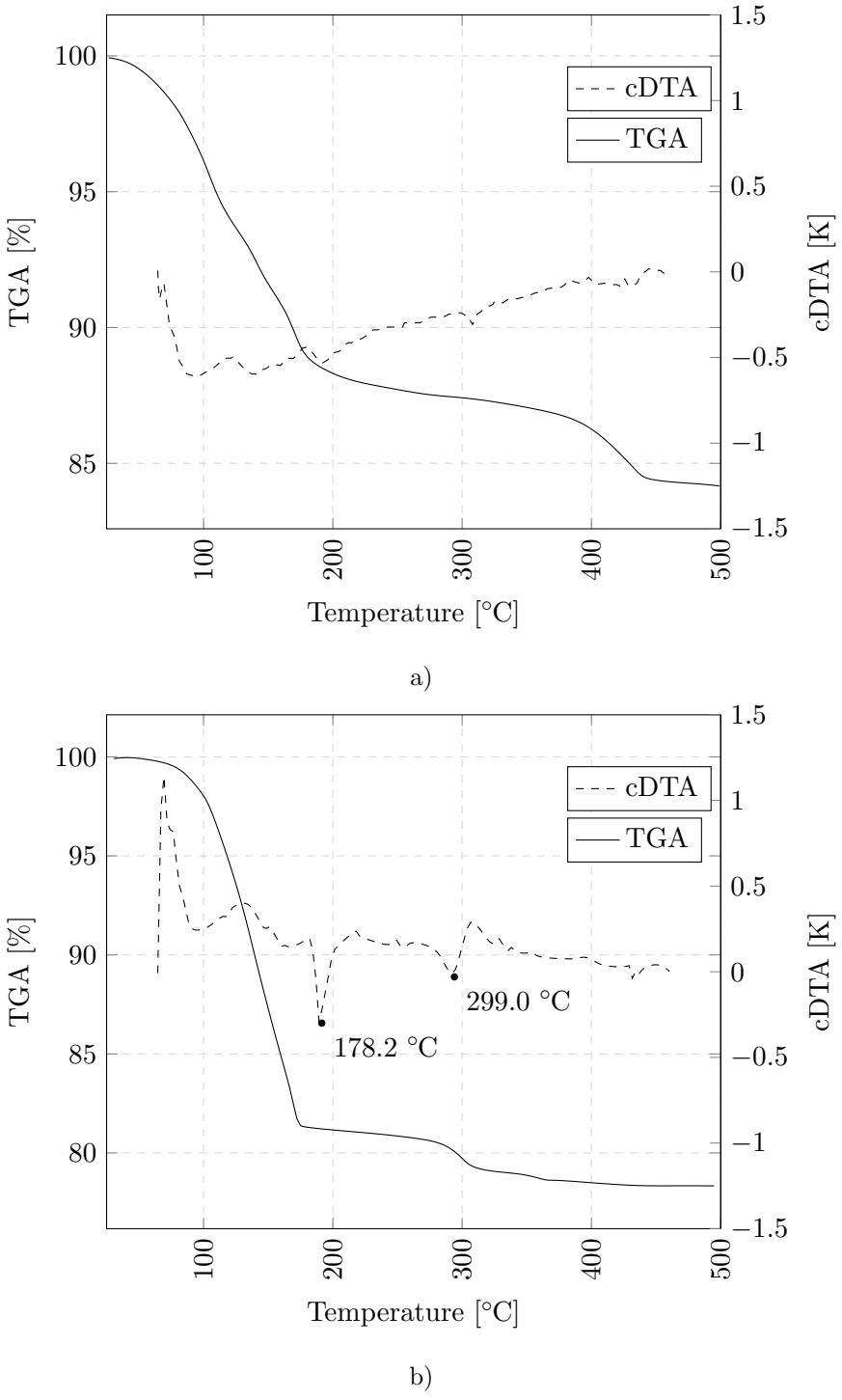


FIGURE 2.15: Thermogravimetric analysis on CP-003 (a) and CP-PLS (b)

The curves from figure 2.15 highlight the difference between the ethylene glycol and the isoprenoide based pastes: While the paste CP-PLS-291015-R1 shows a clear separation

between the solvent evaporation, which is finished at around 175 °C, and the decomposition of the binder between 200 and 400 °C, the paste CP-003 has a blurred transition between those two processes and finishes the decomposition of the binder just at 450 °C. Three things must be kept in mind when analyzing such TGA curves: First, they are done under nitrogen, which means that only the temperature range below 100 °C is representative for the actual furnace process, which is the temperature at which the atmosphere is then changed to formic acid vapor, as was already shown in figure 2.6 and will be discussed in detail in section 3.3. Second, the heating rate is $10\,^{\circ}\mathrm{C}\cdot\mathrm{min}^{-1}$, which is double the rate of the standard furnace process for paste curing. And third, the sample in a TGA is placed in a crucible, not as a defined layer thickness on a wafer, which prolongs the outgassing of the organics in a very undefined way. Hence, the TGA under nitrogen can give an indication about what substance classes are present in the pastes, but cannot give any information on what is happening during the curing process.

To get more insight in to the real curing process, a TGA under formic acid vapor was performed. Since formic acid gases might be corrosive to the equipment, this measurement was only performed once, which is why there is no data on any new isoprenoide based pastes available. The paste which was investigated under formic acid vapor was the ethylene glycol based paste CP-131113-R1.

Figure 2.16b shows the TGA curve under FAV, which was kindly provided by the colleagues from Intrinsiq Materials. For comparison, figure 2.16a shows a TGA of the same paste, batch QNA6198 under nitrogen, acquired by H. Preu from Regensburg. The two TGA curves look very much alike, the different shape of the curve in solvent evaporation area is probably due to differences in the sample amount, tool setting and maybe batch. (IML did not state which batch they were using.) The most important information is acquired by comparing the cDTA/DSC curves (the dashed lines in figure 2.16a and figure 2.16b). While the cDTA curve of the sample heated under nitrogen only shows some distinct endothermal peaks in the lower temperature range, the DSC curve of the sample heated in FAV undergoes a very intense exothermal reaction between 200 and 350 °C, peaking at around 250 °C. This exothermal reaction is clearly the sintering of the nanoparticles, that releases heat due to the energetically favorable reduction of free surface area.

Unfortunately, the equipment used by IML did not include any mass analyzer at the

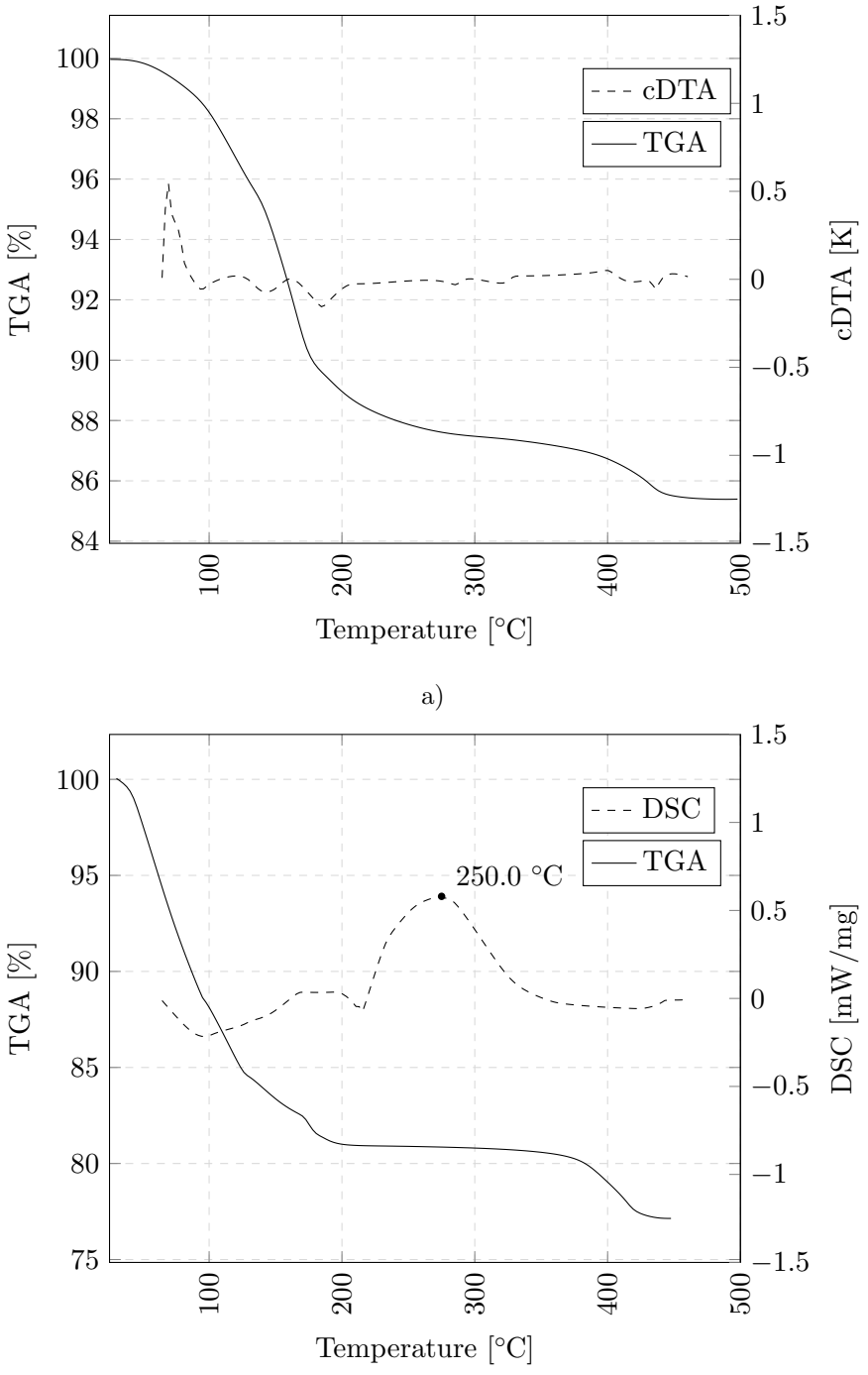


FIGURE 2.16: Thermogravimetric analysis on CP-131113-R1 under nitrogen (a) and formic acid vapor (b)

exhaust which could give information on the chemical nature of the released species. For further investigations on the outgassing substances during the curing process under formic acid, thermodesorption studies at the Institute of Solid State Physics of TU Graz were performed. As can be seen in figure 2.17, most of the solvents are removed at

temperatures below 100 °C, but residues of those substances leave the layer during the whole curing process.

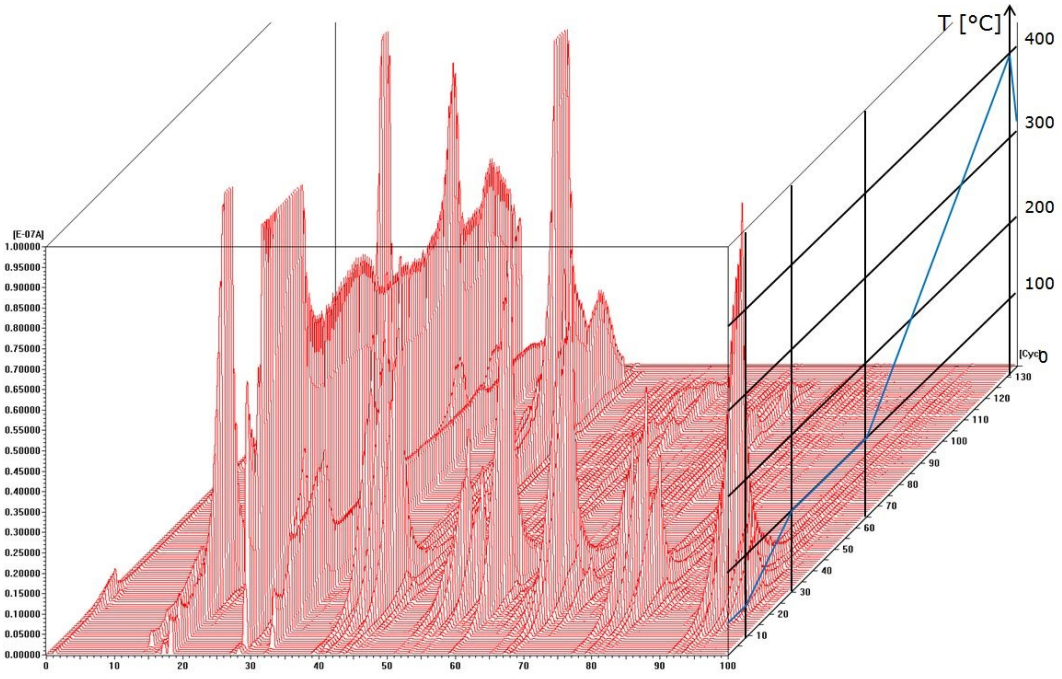


FIGURE 2.17: Mass spectrum of CP-PLS-291014-R1, QNA6449 acquired during a thermodesorption experiment.

Comparing this result to the 3D-FTIR spectrum in figure 2.21 it seems as if the organic solvents are evaporated at lower temperatures, since during the TGA the temperature region of solvent evaporation extended up to 200 °C. There are several differences between the TGA measurement and the TDS measurement. First, the TDS measurement resembles the furnace process shown in figure 2.6 better, using the same temperature steps, hold times and atmospheres. On the other hand, also this measurement does not perfectly simulate a typical curing furnace run: The pressure and gas flow in the TDS chamber was much lower than in the curing furnace since the mass analyzer could not handle such a high signal. The pressure in the TDS chamber is in the 10^{-6} bar range, whereas the vacuum pump of the curing furnace can only evacuate the chamber down to 2 $\times 10^{-3}$ bar. Also, the evaporation behavior of the solvents might very likely be dependent on the layer thickness of the sample.

When analyzing the mass spectrum in figure 2.17, it is difficult to discriminate between the different substance patterns detected. Reference spectra from the NIST database [72] for α-terpineol, limonene and isoborneol confirm the findings of these substances from GC-MS measurements. Additionally, large amounts of water and carbon dioxide

and carbon monoxide in a temperature region around 250 °C indicate the decomposition of the binder system.

The TGA equipment in Regensburg has a FT-IR-spectrometer that can analyze the volatile substances released from the sample. Figure 2.18 shows such spectra in a 3D visualisation that also gives information on the temperature at which the substances were released. Especially in the range between 100 and 300 °C some very intensive signals are detected that are correlated to the evaporation of solvent, whereas at temperatures above 400 °C there is again an increase of signal caused by the decomposition products of the binder system, which would be a typical temperature range for the decomposition of polyethylene glycol [73].

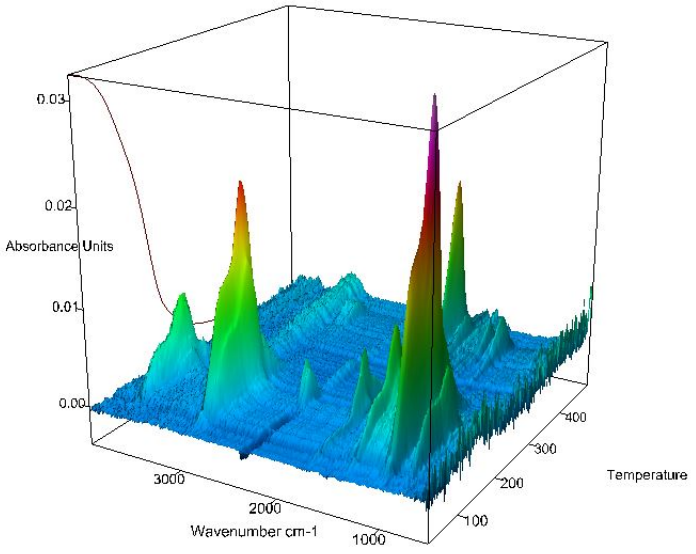


FIGURE 2.18: 3D visualization of the FT-IR spectra gained during TGA of CP-131113-R1 under nitrogen.

The 3D FTIR spectrum shown in figure 2.18 gives an impression on the temperature dependency of the FTIR signals, i.e. which components are evaporated over the temperature range. Figure 2.19 shows two sections of the 3D FTIR spectrum of figure 2.18: The blue line in the spectrum was acquired at 162 °C and shows intense OH (3600 cm^{-1}) and saturated CH (2900 cm^{-1}) bands, as well as a carbonyl band at 1740 cm^{-1}. The spectrum is a good match to the spectrum of (poly-)ethylene glycol [74], [75] with exception to the band at 1740 cm^{-1}, which indicates either the additional presence of another species or a derivatization of the ethylene glycol.

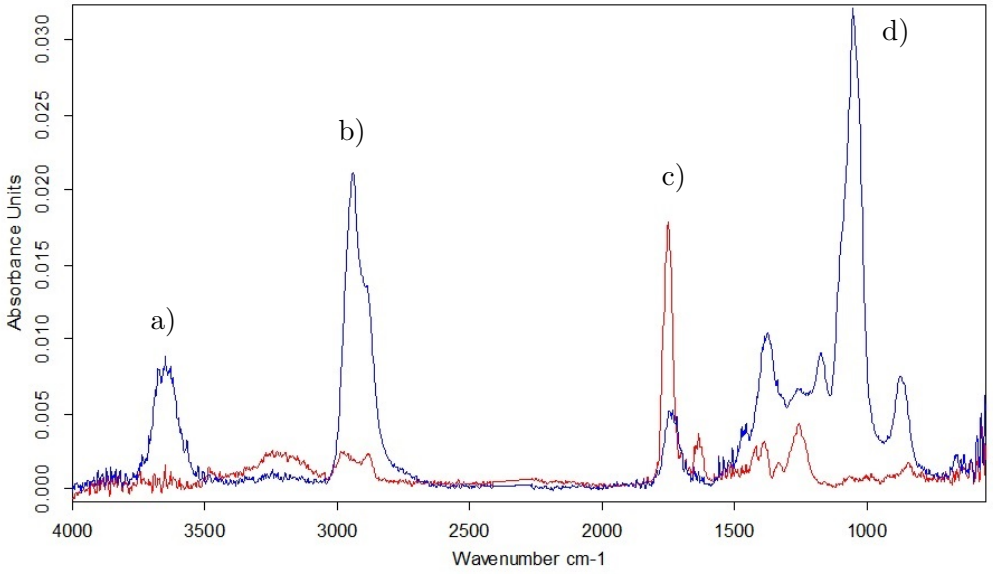


FIGURE 2.19: FT-IR spectra gained during TGA of CP-131113-R1 under nitrogen at 162 °C (blue line) and 424 °C (red line).

In the red spectrum acquired at 424 °C, the distinct bands of the 162 °C spectrum have mostly vanished: The OH band a) is completely gone, while a new intense band c) at 1740 cm^{-1} has emerged, which is clearly a carbonyl band. Hence, it seems likely that the OH groups were chemically transformed into carbonyl groups. This is not in line with literature: Figure 2.20 shows the decomposition of polyethylene glycol during a TGA from 0 to 50% level of degradation found in literature [76]. Comparing those spectra to the spectrum of CP-1311 in figure 2.19, the same phenomena as described before can be seen: The OH band a) is vanishing, the CH band b) is becoming smaller (although it is first becoming larger in the early stage of degradation) and the intense band d) at 1140 cm^{-1}, which is present in figure 2.19 at 162 °C and vanished at 424 °C is loosing its intensity in the literature spectra, again after an increase of intensity in the early stages of degradation. This band is caused by non-cyclic ethers. It seems as if the decomposition of the PEG in the 424 °C spectrum of CP-1311 has already progressed beyond 50%, which is the highest level shown in the cited literature.

The difference to the literature data, especially the presence of the carbonyl band might indicate that there is a chemical reaction other than pure decomposition occurring at higher temperatures. A comparison with FT-IR data acquired from a TGA under formic acid vapor could help to understand the involved mechanism, but could not be done for the afore mentioned reasons.

For the new, isoprenoide based pastes, similar investigations were carried out. Figure 2.21 shows the 3D FT-IR spectrum acquired during the TGA shown in figure 2.15b.

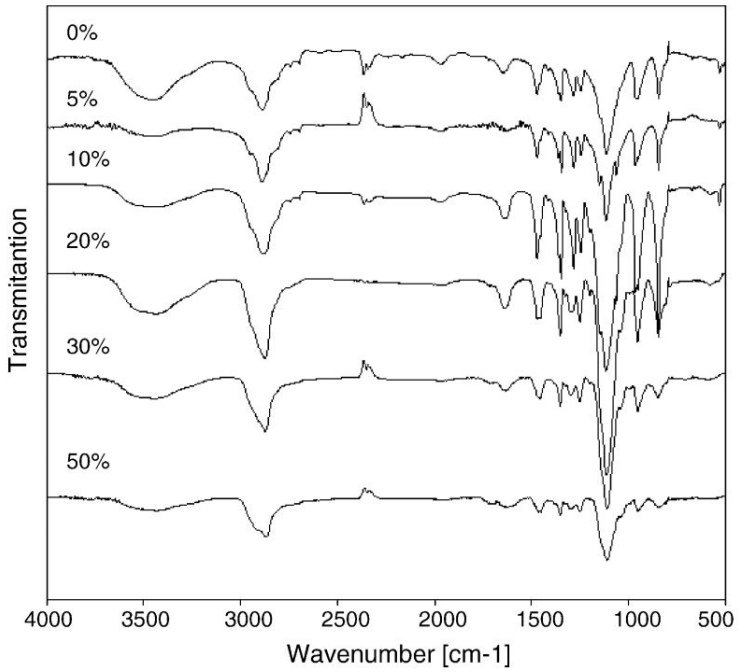


FIGURE 2.20: FT-IR spectra gained during the decomposition of PEG [76].

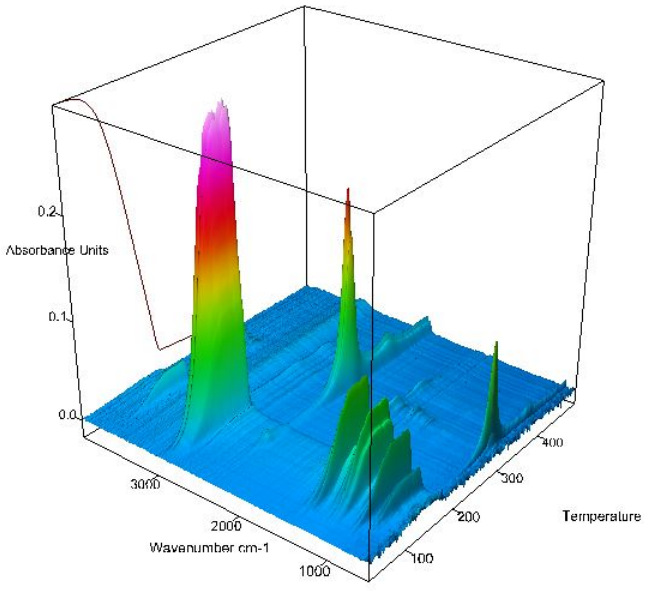


FIGURE 2.21: 3D visualization of the FT-IR spectra gained during TGA of CP-PLS-291014-R1 under nitrogen.

When comparing the 3D-IR spectrum of CP-PLS (figure 2.21) with the corresponding spectrum of CP-1311 (figure 2.18), the difference in the evaporation behavior of the solvent is evident: The solvent of CP-PLS is evaporating in a very defined temperature range of 100-200 °C, much narrower than the range of CP-1311. Same is true for the

decomposition of the binder system, which is happening at 300-350 °C. The spectra in figure 2.22 show clearly that the evaporating solvent is α-terpineol, all the bands can be explained by the reference spectrum and also the fingerprint area, which is the characteristic area in the spectrum between 500 cm^{-1} and 1500 cm^{-1}, is identical. The pink line in figure 2.22 shows the decomposition product of the binder at 306 °C, which according to the reference spectrum (red line) can be identified as carbon dioxide as main component and some smaller amounts of unidentified substances, having bands at 1500 cm^{-1}, 1740 cm^{-1} and 3200 cm^{-1}, most likely water.

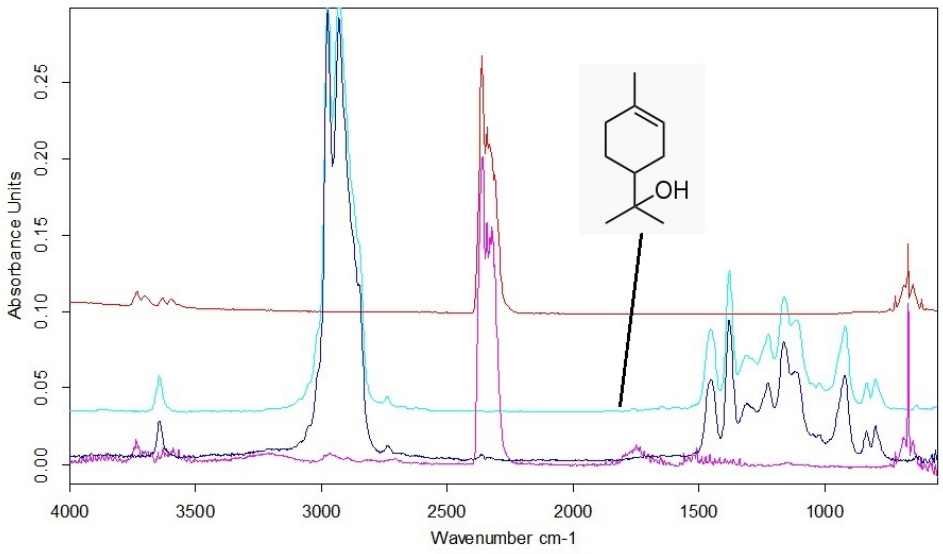


FIGURE 2.22: FT-IR spectra gained during TGA of CP-PLS-291014-R1 under nitrogen at 170 °C (blue line) and 306 °C (pink line), as well as reference spectra of carbon dioxide (red line) and α-terpineol (turquoise line).

As the TGA was carried out under nitrogen, clearly the required oxygen for the decomposition of organic substances to give such distinct carbon dioxide bands had to come out of the material. As the powder x-ray diffraction (XRD) investigations (figure 2.14) could show, there is a significant amount of copper(I)-oxide present in the pastes, which might be the source for the oxygen. If this was the case, this would mean that the binder system has a certain reducing power, i.e. it is able to draw the oxygen out of the copper oxide.

Since the boiling point of α-terpineol is at 217-218 °C [77] and unlike ethylene glycol it cannot polymerize without another substance to co-polymerize with, it is evident that there must be more organic substances contained within the paste CP-PLS that make up the binder system. GC-MS analysis of CP-PLS-291014-R1, QNA6483 leached in

methanol and chloroform shows that there is a total of four substances that could be extracted of the paste. (Figure 2.23) The four substances could be identified as:

1. Limonene (CAS 138-86-3)
2. Isoborneol (CAS 124-76-5)
3. Terpineol (CAS 98-55-5)
4. Isoterpinolene (CAS 586-63-0)

As expected from the TGA data (figure 2.15b), terpineol seems to be the largest fraction in the organic phase. Limonene and isoborneol seem to be involved in the formation of the binder system, as they are not evaporated during the TGA although e.g. the boiling point of limonene (170-180 °C [78]) is lower than terpineol, i.e. it would evaporate earlier. Isoterpinolene might be an impurity in the solvent terpineol, since it can be synthesized from it by eliminating the OH group and is due to its high price an unlikely additive to such a copper paste.

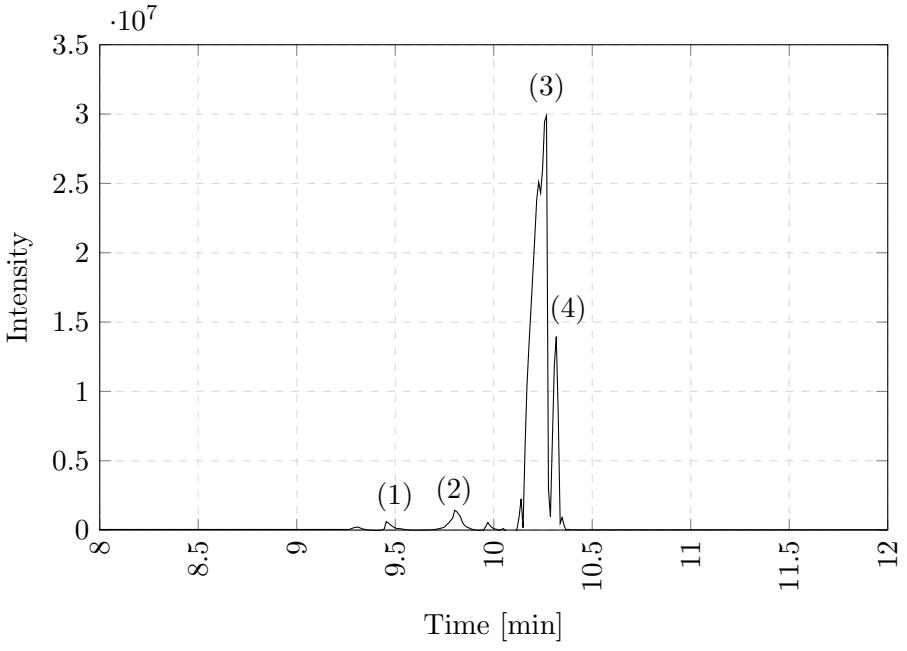


FIGURE 2.23: Gas-chromatographic spectrum of the organic phase of the paste CP-PLS, extracted with methanol.

The TDS-GC-MS (thermodesorption - gas chromatography - mass spectrometry) data presented in figure 2.24 underlines the above stated theory that the binder system is

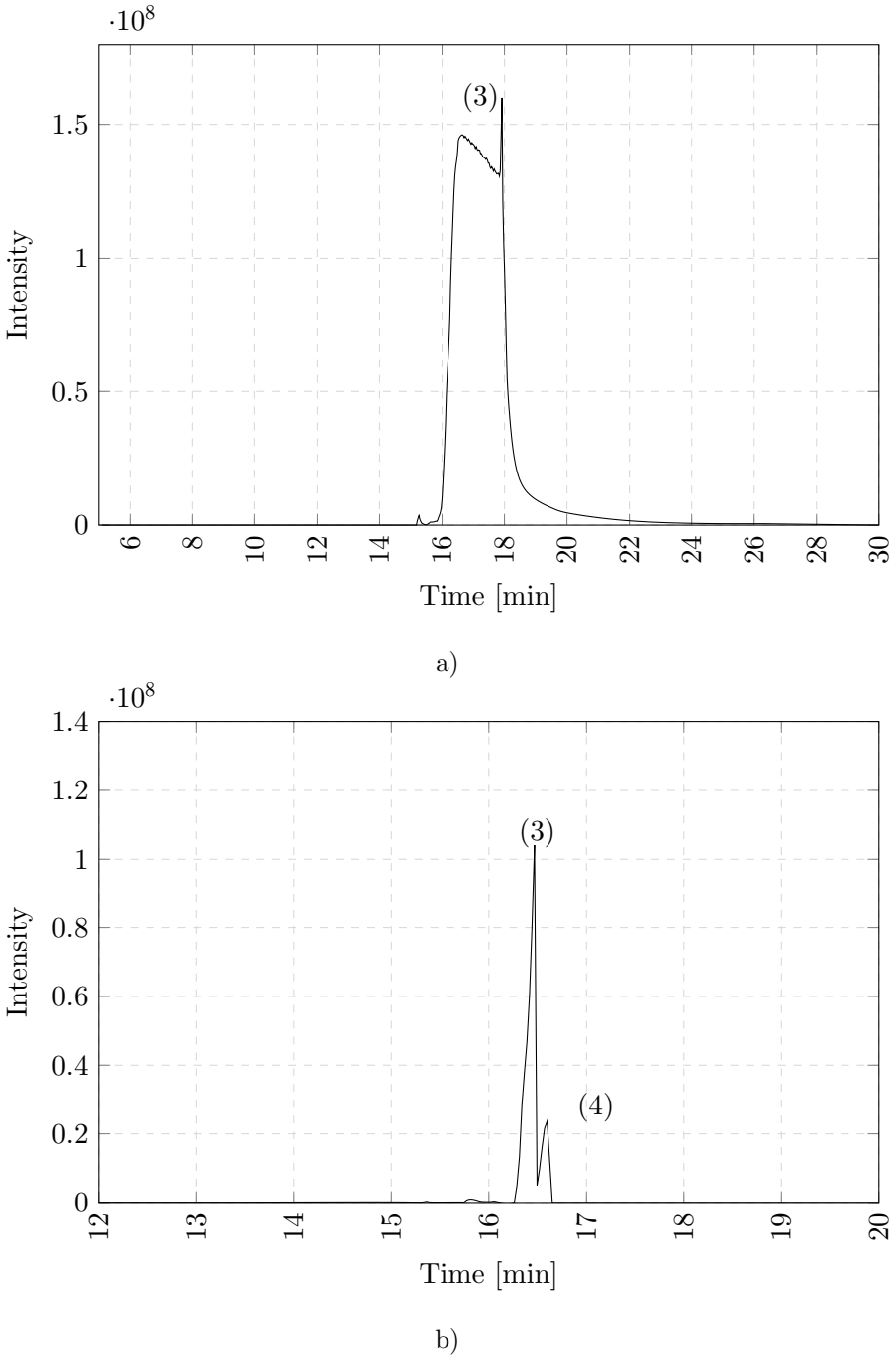


FIGURE 2.24: Gas-chromatographic spectrum of the phase evaporated at 180 °C (a) and 300 °C (b) from CP-PLS

made up by limonene and isoborneol: upon thermal desportion, those two substances are not released from the paste, but seem to react at temperatures below 180 °C either with each other or with a third, not detected constituent. Whatever the underlying mechanism is, after heating the sample up to 180 °C (figure 2.24a), neither of them is detected. Same is true for a TDS measurement at 300 °C (figure 2.24b).

2.3.2 Analysis of the Cured Layers

During the furnace treatment the copper pastes undergo a phase change: First, the solvents are evaporated in the drying step. Then, the particle coating is removed by formic acid vapor [79], so that the isolated copper nano particles can sinter together and form a solid network of copper. Finally, the organic binder system is decomposed, removed from the porous network over the gas phase and the copper grains are growing in a final annealing step. Those changes in the layers, as well as the layers in their final state must be characterized to gain a better understanding on their evolution and properties.

2.3.2.1 TOF-SIMS Analysis

For depth profiles of chemical compositions in organic and inorganic layers, TOF-SIMS is the method of choice [80]. Measurements were carried out at the Institute of Chemical Technologies and Analytics of TU Vienna by S. Schwab (TOF-SIMS). The purpose of the trials was to investigate the effect of the curing procedure on the binder system.

According to TGA data (see figure 2.16) and resistivity measurements [79], [81], the pastes are sensitive towards the used gas atmosphere. This effect was investigated by S. Schwab in his Master's thesis on dummy wafers printed with CP-131113-R1, QNA6198, after different process steps [81]. The data presented in this thesis was acquired on samples of the paste CP-PLS-291014-R1, QNA6449. Negative TOF-SIMS spectra were acquired by sputtering with Caesium, for the positive spectra Oxygen was used as sputtering gas.

The samples were processed according to table 2.1, MCL012 - MCL017. The goal was to correlate the inconclusive μCT results to the removal of organic materials during the curing process to support or falsify the theory of organic matrix interfering with the gray-scale threshold settings during μCT data analysis. In total, eleven samples were investigated by TOF-SIMS analysis (section 2.2.3).

The samples (for details see table 2.5) were selected to represent important points of the curing process: The end-point after three hours of annealing at 400 °C, the point at which the resistance drop in the curing process is over at 260 °C, a midpoint in the resistance drop where the color change has not yet occured (200 °C) and the starting

Sample Name	Max. Temp.	Hold Time	Description
PLS-400-180	400 °C	180 min	fully processed
SEED-400-180	400 °C	180 min	reference
PLS-260-000	260 °C	0 min	min. resistivity reached
SEED-260-000	260 °C	0 min	reference
PLS-200-000	200 °C	0 min	sample color still brown
SEED-200-000	200 °C	0 min	reference
PLS-000-000	-	-	dried paste sample
SEED-000-000	-	-	untreated PVD Cu sample
PLS-400-180-Ox	400 °C	180 min	oxidized in furnace
SEED-400-180-Ox	400 °C	180 min	oxidized in furnace
INF-000-000	-	-	nano-paste

TABLE 2.5: Overview on the sample types dedicated to TOF-SIMS measurements.

point of the process (dried, but uncured sample). Each of those points was referenced with a piece of wafer coated with 5 μm PVD copper (denoted as SEED in table 2.5) to have a comparison with a bulk system, having seen the same furnace processes. The possible removal of organic binder by an oxidation step was investigated by oxidizing a fully processed piece of CP-PLS in the ATV furnace by heating it up under air until a strong discoloration occured (approx. 300 °C). Additionally, one uncured piece of the nano-paste CP-INF, QNA6501 was investigated, since the organic content of this paste is higher compared to CP-PLS, QNA6449.

Some selected TOF-SIMS spectra are shown in figure 2.25 (negative) and figur 2.26 (positive). It is evident that the same fragments are emitted from the samples, with the spectra only differing in the intensity of certain peaks. The masses 23 and 39 in the positive spectrum refer to sodium and potassium, which are typically present on most samples that have not been prepared with the avoidance of such contaminations in mind. The copper isotopes 63 and 65 are present in the spectra as single atoms as well as in form of atom clusters, which weigh a multitude of the atomic mass, e.g. masses 126, 130, 189, 191 and so on. Also copper oxides are present, e.g. the masses 79 or 81. Copper and copper oxides make up the largest part of the mass spectra shown in figure 2.25 and 2.26. Large quantities of carbon and oxygen can be found in the negative spectrum, pointing towards residual organics. For a detailed analysis of the element distribution, a mass signal of interest must be selected, and the depth profile of this mass must be charted.

As the scope of this investigation was to investigate the organic matrix of the binder system, which might be responsible for problems in pore detection in μCT analysis, the

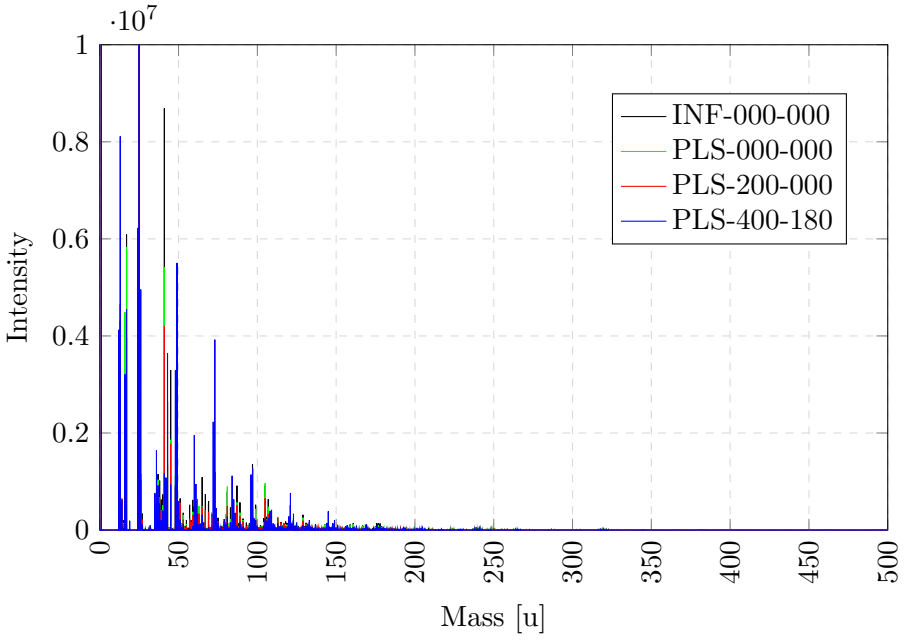


FIGURE 2.25: Combined negative TOF-SIMS spectra of all samples.

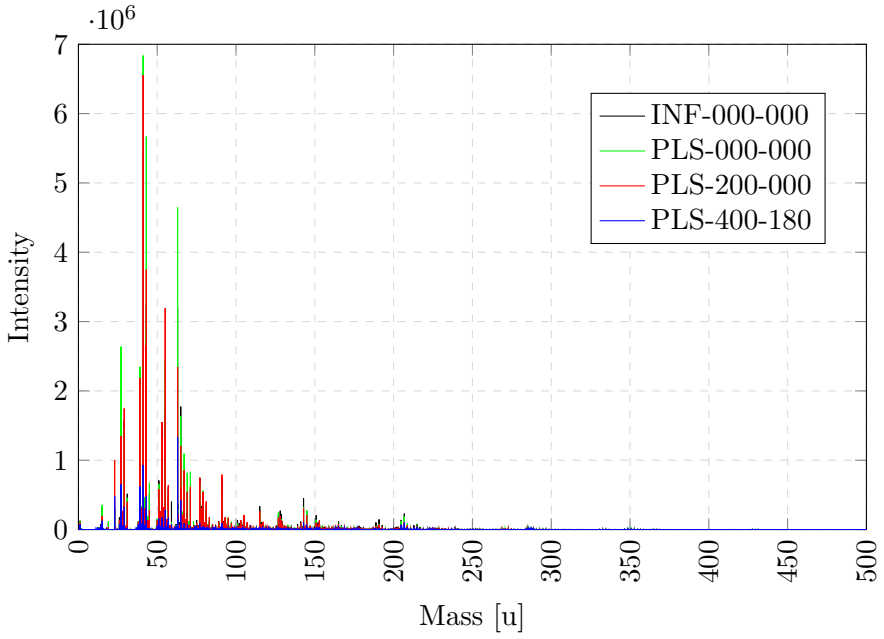


FIGURE 2.26: Combined positive TOF-SIMS spectra of all samples.

signal for Carbon is of primary interest. Figure 2.27 shows the depth distribution of the sum of all carbon and carbon compound signals on the CP-PLS samples, normalized by the total ion current and the copper signal, plotted versus the sputtering time. The sputtering time corresponds to the depth, i.e. the shown graphs are depth profiles. Due to the high roughness of printed Copper, the depth of the sputtering could not

be determined by profilometry on those samples, which is why the sputtering time is shown instead. By measuring the sputtering depth on the PVD copper samples, which have a very low roughness, the sputtering rate could be determined to be 1.15 nm per second. It can be assumed that the sputtering rate is similar on printed copper samples, which means that the sputtering depth for the printed copper samples was between 500 nm (PLS-260-000) and 2.3 μm (INF-000-000). The intense initial drop of the signal in the first seconds is due to surface contaminations and should not be considered relevant. All the samples except the fully cured one show an increase of the carbon signal approximately within the first 100 seconds of sputtering. This effect is due to the surface roughness and is immanent also in other relevant signals like the Cu signal.

The samples of the paste CP-PLS clearly show a decreasing carbon signal with increasing furnace temperature. The result of this measurement is well in line with TGA results (see figure 2.15b), which show a mass loss of several mass percent at temperatures higher than 300 °C. The very small difference between the signals of the dried sample, the sample processed at 200 °C and the one processed at 260 °C shows that more or less all the mass loss in the TGA curve at temperatures below 300 °C is due to the evaporation of solvents, and that the drying procedure of the pastes can be considered effective.

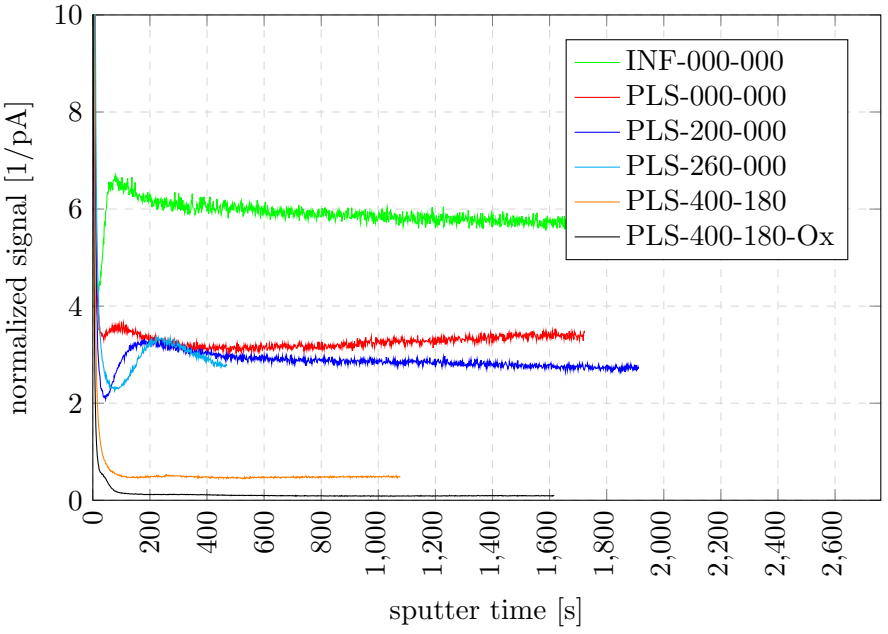


FIGURE 2.27: TOF-SIMS sum of all C signals of paste samples normalized on the Cu signal and the ion current.

The lowest signal in figure 2.27 is the carbon signal of the oxidized paste sample. In absolute values, the signal counts of this sample were reduced to less then half of the non oxidized sample, which means that there was still a significant amount of residual carbon in the fully cured paste, which could still be removed by an oxidation step. It is important to mention here again, that only the first micrometers of the samples were measured in this trial. As it was discussed in the microtomography section 2.2.3, the first few micrometers can be considered surface roughness, which would mean that this is actually the area where carbon would be removed the easiest. In deeper layers, the carbon signal might increase drastically. Such an investigation would be very time consuming for layers greater than 20 μm with sputtering rates of approximately 1.2 nm per second and hence it was not performed.

The high amount of residual carbon in the layer cured at 260 °C supports the theory of a seemingly lower porosity in this sample compared to a fully cured one, although it is no proof. One possible way to prove this would be to oxidize a sample cured at 260 °C to remove residual carbon, repeat the reduction step and then analyze it in μCT against a reference that has been reduced two times without an intermediate oxidation step.

2.3.2.2 IR Spectroscopy on Etched Samples

Another suitable method to characterize the organic components in the printed and cured layers is again infra-red spectroscopy. The tool used for the investigations was a Bruker LUMOS FT-IR microscope located at the Carinthian Tech Research (CTR) institute in Villach, operated by Martin DeBiasio. Consultation for the interpretation of the spectra was done by Martin Kraft. The samples investigated were cured with the same processes as the μCT samples shown in table 2.1.

Previous investigations with IR spectroscopy on cured samples of CP-003 were inconclusive: Measurements on fully and partially cured samples as well as on uncured wafers did show a decreasing signal with increasing state of curing, but the intensity of the signal even on the uncured sample was so low that a qualitative analysis was impossible.

In order to address this issue and to gain more information about the residual organics in the paste, the samples were partially etched with two different etching solutions. The sketch in figure 2.28 tries to explain the mechanism of a concentration of organic

substances due to partial etching of a sample. Since the organic components of the paste are hydrophobic, they are not dissolved and washed away by the etching solution. Therefore, upon removing the copper matrix, the organics are driven forward by the etch front and are concentrated there.

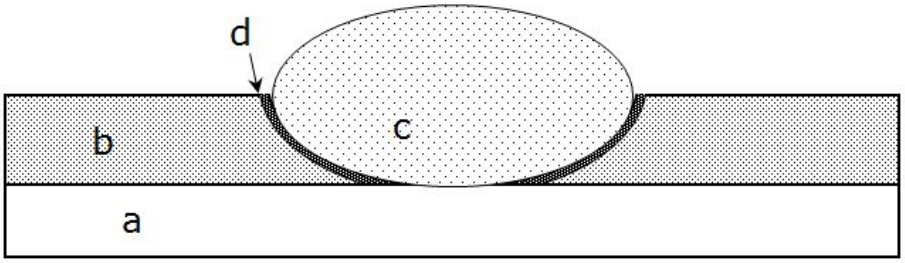


FIGURE 2.28: Schematic explanation of the concentration effect due to etching. a) silicon wafer substrate, b) porous copper with low concentration of organics, c) copper etching solution with very low solubility of organics, d) etch front with high concentration of organics.

As will also be discussed in section 3.2.2 the printed copper pastes leave residues on the barrier after etching, which is e.g. a problem for subsequent barrier etching. For the old ethylene glycol based pastes, the residues were typically bismuth oxides. The new limonene based pastes on the other hand leave seemingly organic residues on the barrier, that form a fragile thin film of black color. This film looks different when the copper layer was etched with different etching chemistries, which might be a chance to gain more insight into the chemical nature of the organic components of the paste.

Each of the samples MCL12-MCL17 (see table 2.1) was etched with two different etching chemistries: The Cu-Seed-Etch as well as the Alu-HAC etch. The exact composition of those two etching mixtures is given in table 2.6 (reprinted in section 3.2.2 as table 3.4).

Purpose of Component	Cu-Seed-Etch	Alu-HAC
Oxidation	0.8 wt% H_2O_2	1.38 wt% HNO_3
Oxide removal	2 wt% H_3PO_4	37.13 wt% H_3PO_4
Diluent	-	45 wt% CH_3COOH
Rest	97.2 wt% H_2O	16,5 wt% H_2O

TABLE 2.6: Composition of the two copper etching solutions used within this thesis.

The etching solutions were prepared fresh for this trial according to table 2.6. The copper seed etching solution, which contains only strongly diluted phosphoric acid and hydrogen peroxide, is much less oxidizing than the Alu-HAC etching solution.

Figure 2.29 shows the spectrum of a sample (MCL014) without modification as blue line. To remove environmental influences, the spectrum must be corrected against a standard, which is done with a gold mirror that has a very high reflectance. This baseline corrected spectrum is shown as red line in Figure 2.29. The spectra of the raw samples (non etched) are shown in figure 2.30. The strong, defined peaks at 2800 - 3000 cm^{-1} indicate the presence of hydro carbons. The many small peaks between 1600 and 2000 cm^{-1} come from water vapor in the air that is due to the presence of machine operators or trespassers in the room. The signal at 850 cm^{-1} might be caused by an inorganic contamination in the paste. The strong increase of the signal line at the end of the spectrum at 500 cm^{-1} is an artifact that comes from the baseline correction.

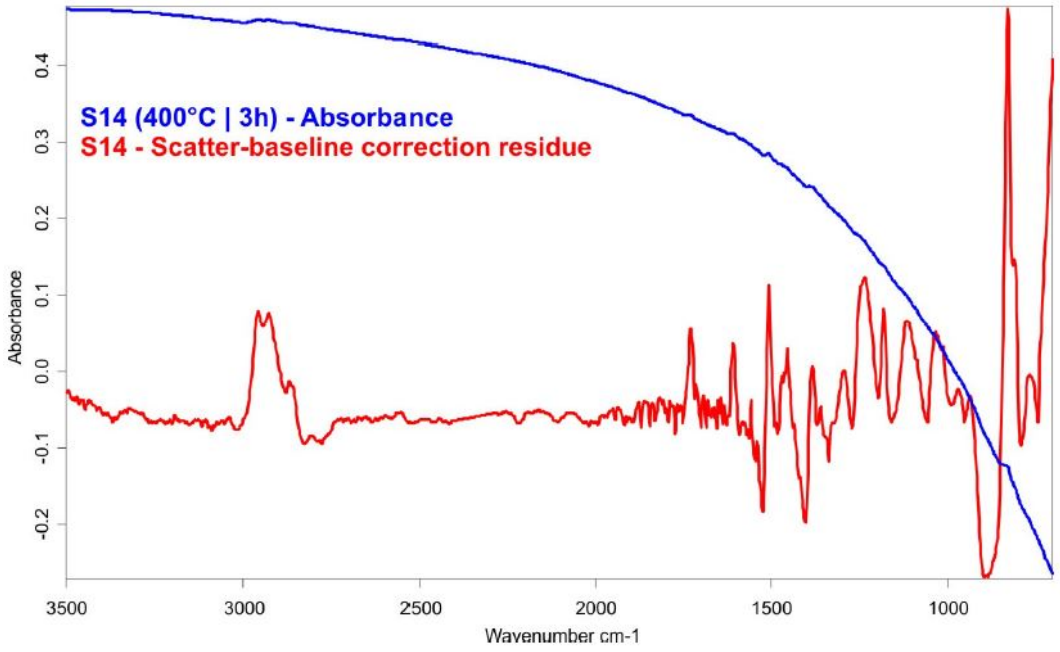


FIGURE 2.29: IR spectrum of MCL14 without baseline correction (blue line) and with baseline correction (red line).

The baseline correction was applied to all recorded spectra, which are displayed in figure 2.30. The first obvious observation that catches the eye when looking at those spectra is that the low-temperature samples generate spectra which are strongly "bent" away from the zero line of absorbance. This is due to the different colors of the samples: The samples that were cured at lower temperatures are more brownish in their color, which means they reflect light less efficiently than the pink samples that were obtained from high temperature processes. The reason for this color change can be related to the loss or organic mass as found in thermo-gravimetric analysis (e.g. figure 3.17). It can be seen that the overall absorbance of the samples is indirectly proportional to the temperature

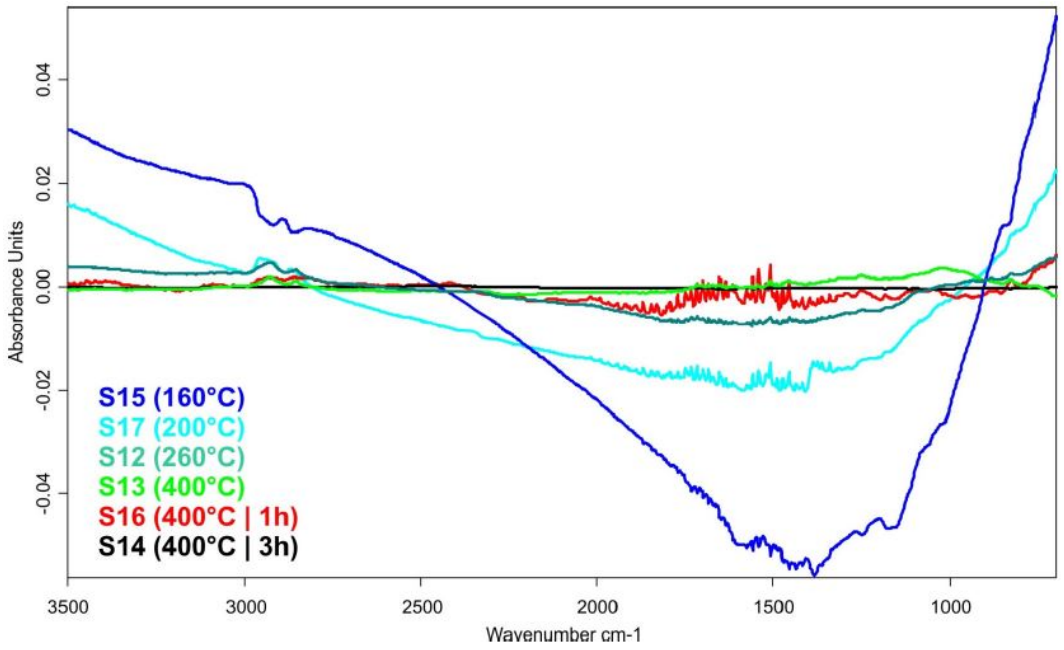


FIGURE 2.30: IR spectra of the samples MCL12-MCL17 (labeled as S12-S17)

of the furnace process. The samples that were cured at temperatures between 260 and 400 °C show very similar overall absorbance. Quantitative comparison of the peaks within this group of samples is difficult, whereas it is clearly visible that the hydrocarbon peak of the samples MCL15 (160 °C) and MCL17 (200 °C) are more distinct than those of the other samples. As discussed above, the small peaks between 1600 and 2000 cm^{-1} are due to the presence of water vapor, which means that the difference of the spectra in this wavelength range does not indicate a difference between the samples.

The identification of substance based on the bands is difficult. The bands in the spectrum of figure 2.30 can be identified as follows:

- 2921 cm^{-1} and 2855 cm^{-1}: CH
- 1729 cm^{-1}: C=O
- 1180 cm^{-1}: C-O
- 1607-1507 cm^{-1}, 1558 cm^{-1} and 1038-1011 cm^{-1}: aromatic ring stretch bands

According to those bands, the substance must be an ester with some aromatic groups. From its presence in the paste it can be concluded that it has to be either a solvent, a polymeric binder or a particle coating. All the main components of the paste were

already identified by GC-MS, and none of them includes aromatic groups. Hence, it is likely that the signal is caused by residues of nano particle coating which was not completely removed during the curing step. A literature screening for probable copper particle coatings pointed towards a specific vinyl ester [82], which shares most of the bands with the spectrum shown in figure 2.29.

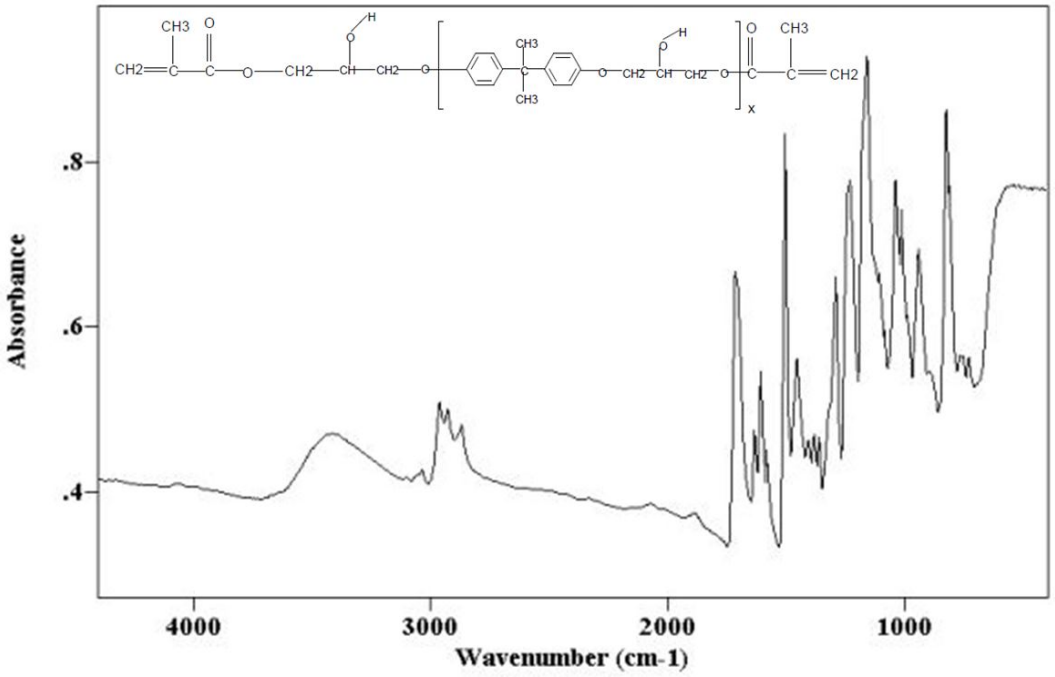


FIGURE 2.31: Reference spectrum of a vinyl ester from literature. [82]

The OH band at around 3500 cm^{-1} from the reference is not very distinct in the spectrum of figure 2.29, but this might be due to the baseline correction. More importantly, the carbonyl and the C-O bands are shifted (1729 cm^{-1} vs. 1712 cm^{-1} and 1180 cm^{-1} vs. 1160 cm^{-1} respectively). The substitution pattern of the aromats in the finger-print range (below 780 cm^{-1}) do not match, and the band at 828 cm^{-1} does not have a counterpart in the reference. Hence, it can be assumed that the substance in the paste has a molecular structure similar to the vinyl ester from the reference [82], but it is not identical.

Having recorded the spectra of the samples as deposited (and cured), the next step is to analyze the impact of the etching solutions on the organic components of the pastes. Figures 2.32 and 2.33 show microscopic pictures of the etched areas as well as the corresponding infra-red spectra. The red squares on the microscopic pictures mark the position of the measurement sites. Out of those measurements, some spectra are

displayed in color on the right hand picture. The colors of the respective spectra are corresponding to the colors of the dots on the left hand pictures.

It can be seen clearly that the etching caused an increase of concentration of the organic components in the partially etched area of the paste. For example in figure 2.32 b) and d), the blue and the pink spectrum are located outside the etched area and therefore show only small peaks, whereas the intensity of the other spectra that were recorded from positions within the etched area have much more distinct peaks in the hydro carbon range of 2800 - 3000 cm^{-1} and in the fingerprint range of 950 - 1750 cm^{-1}.

When comparing the microscopic pictures of the Cu-Seed etched samples, it is very interesting to see that the samples cured at up to 400 °C could be etched completely, i.e. without visible residues on the barrier below the copper seed layer. Upon annealing at 400 °C there seems to be a change either in the nature of the organic material or in the distribution thereof. Sample MCL016, which was annealed for 1h at 400 °C shows residues in the shape of small dots that are deposited on the barrier. On sample MCL014, which was annealed for 3h at 400 °C, the barrier is not visible at all because it seems to be covered by a black film of carbon. It seems as if the prolonged heat treatment caused a pyrolization of the residual organics in the layer and turned them into a kind of graphite. As suggested in chapter 2.3.2.1, these carbon residues might be removed by oxidation with a subsequent reduction step.

The outcome from those investigations was that depending on the intended further processing steps, it might be necessary to interrupt the furnace treatment before the annealing step. Wet-chemical etching can be performed on layers that were treated with temperatures up to 400 °C, whereas prolonged annealing at this temperature leads to insoluble organic residues on the underlying barrier layer. Another possible conclusion from the trials would be that a second plateau step in the furnace recipe shown in figure 2.6 or figure 3.19 and described in table 3.7 could be beneficial. Such a plateau step at 300 °C might give the system more time to decompose and remove the organic binder, which might lead to cleaner layers with modified properties. Since this would be a major change to the furnace process which would affect a vast number of processes, this investigation was not carried outs within this thesis.

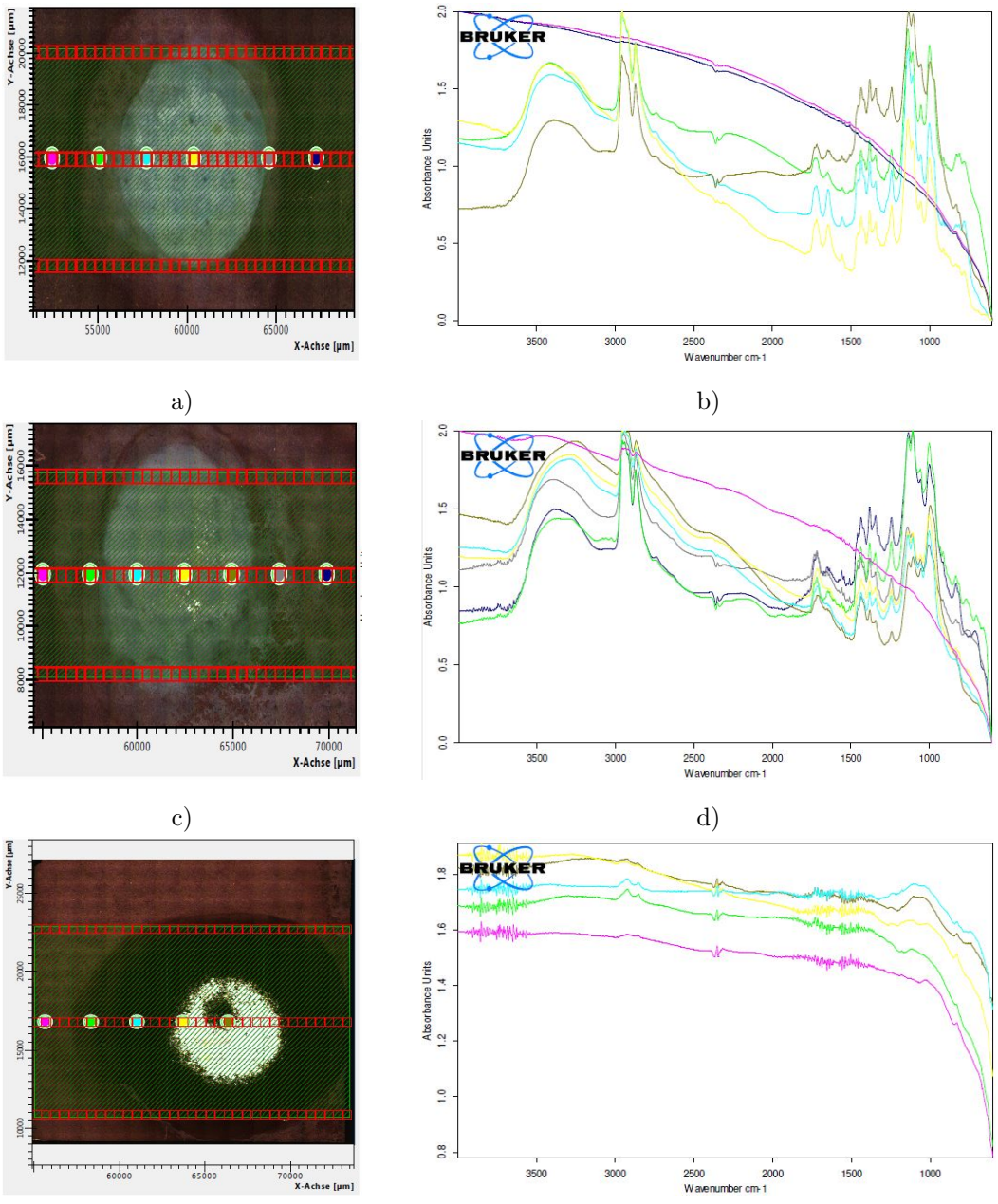


FIGURE 2.32: IR spectra of Alu-HAC etched samples. a) Measurement sites and b) Spectrum of MCL015; c) Measurement sites and d) Spectrum of MCL017 e) Measurement sites and f) Spectrum of MCL012

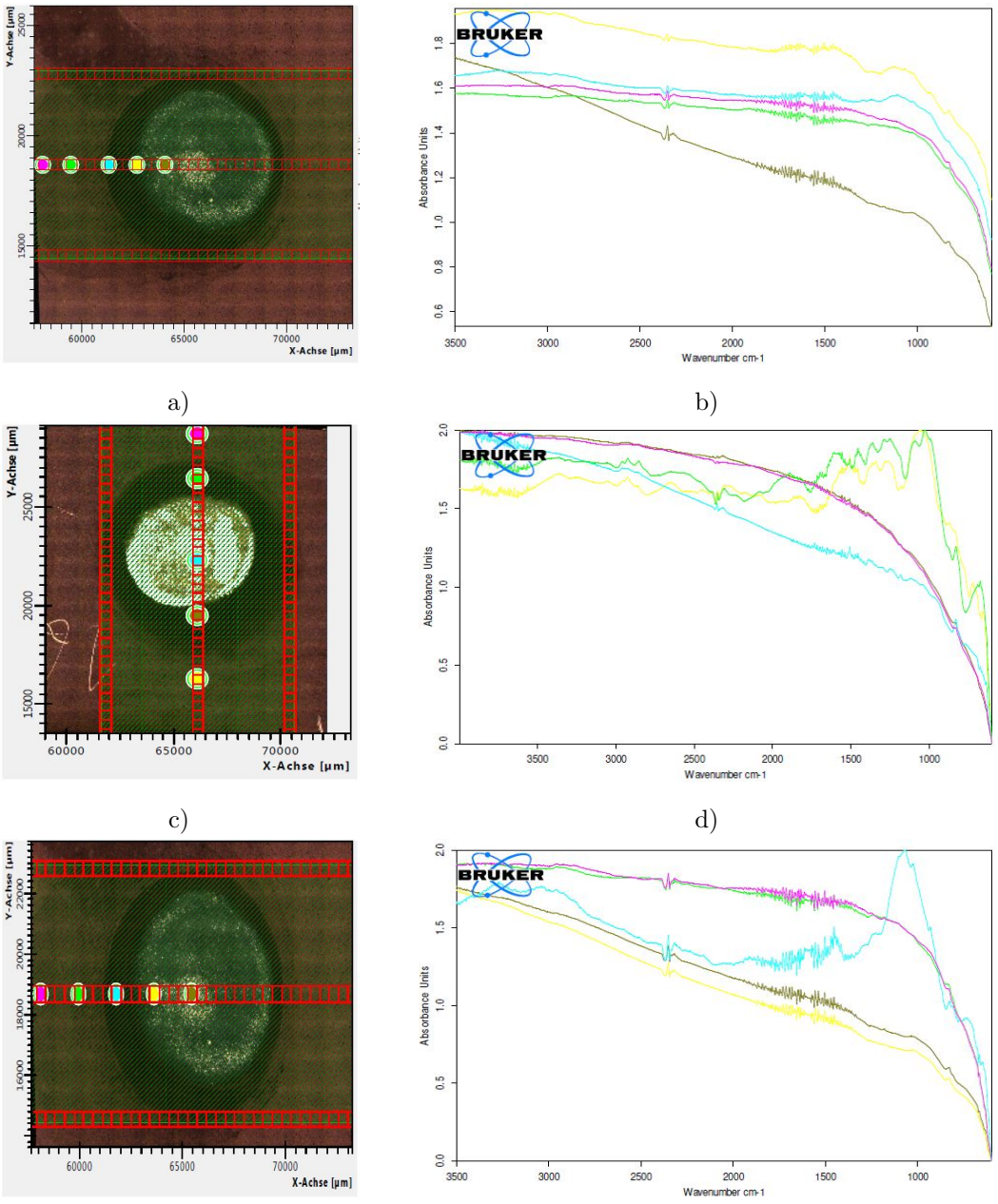


FIGURE 2.33: IR Spectroscopy of Alu-HAC etched samples. a) Measurement sites and b) Spectrum of MCL013; c) Measurement sites and d) Spectrum of MCL016 e) Measurement sites and f) Spectrum of MCL014

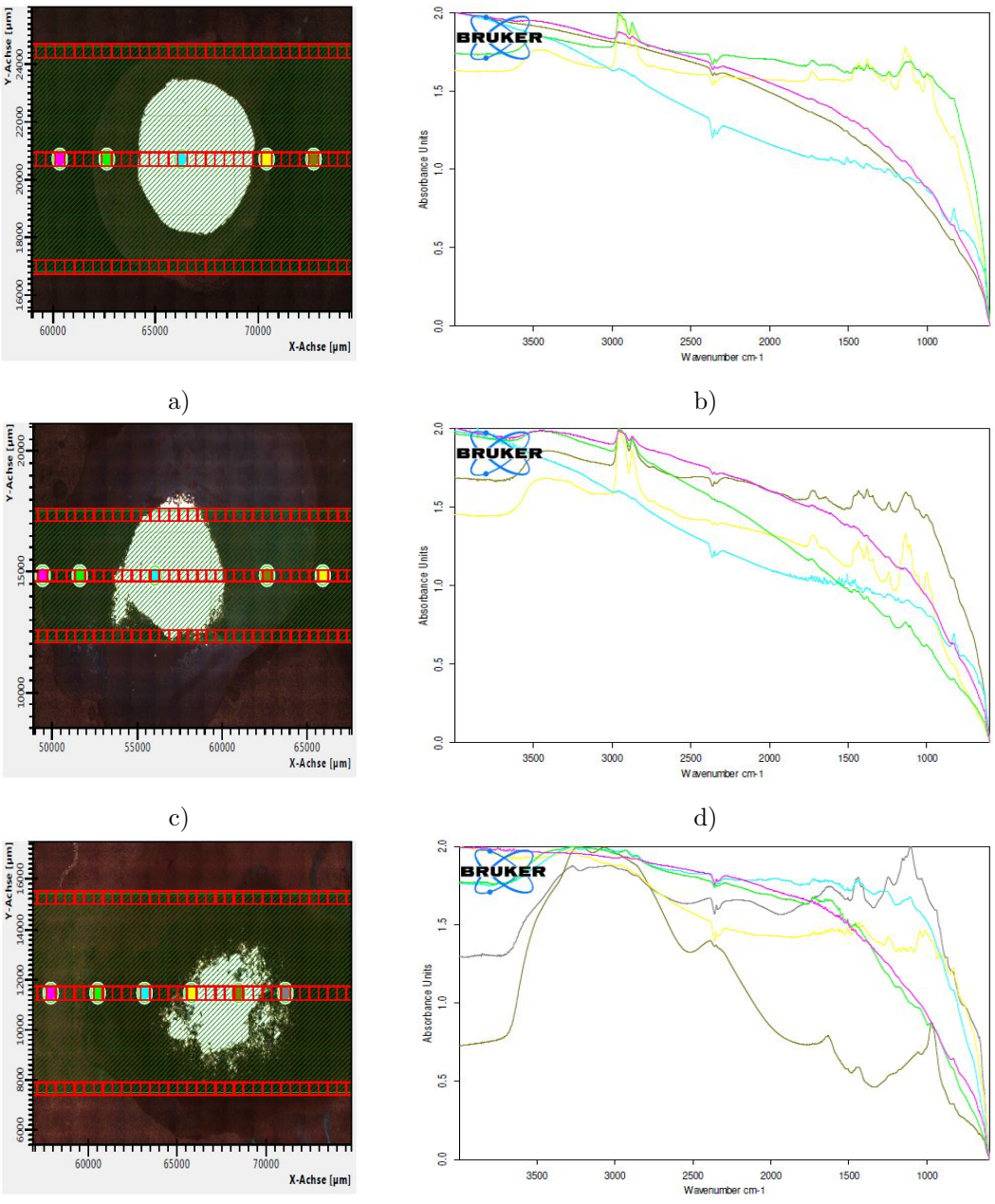


FIGURE 2.34: IR Spectroscopy of Cu-Seed etched samples. a) Measurement sites and b) Spectrum of MCL015; c) Measurement sites and d) Spectrum of MCL017 e) Measurement sites and f) Spectrum of MCL012

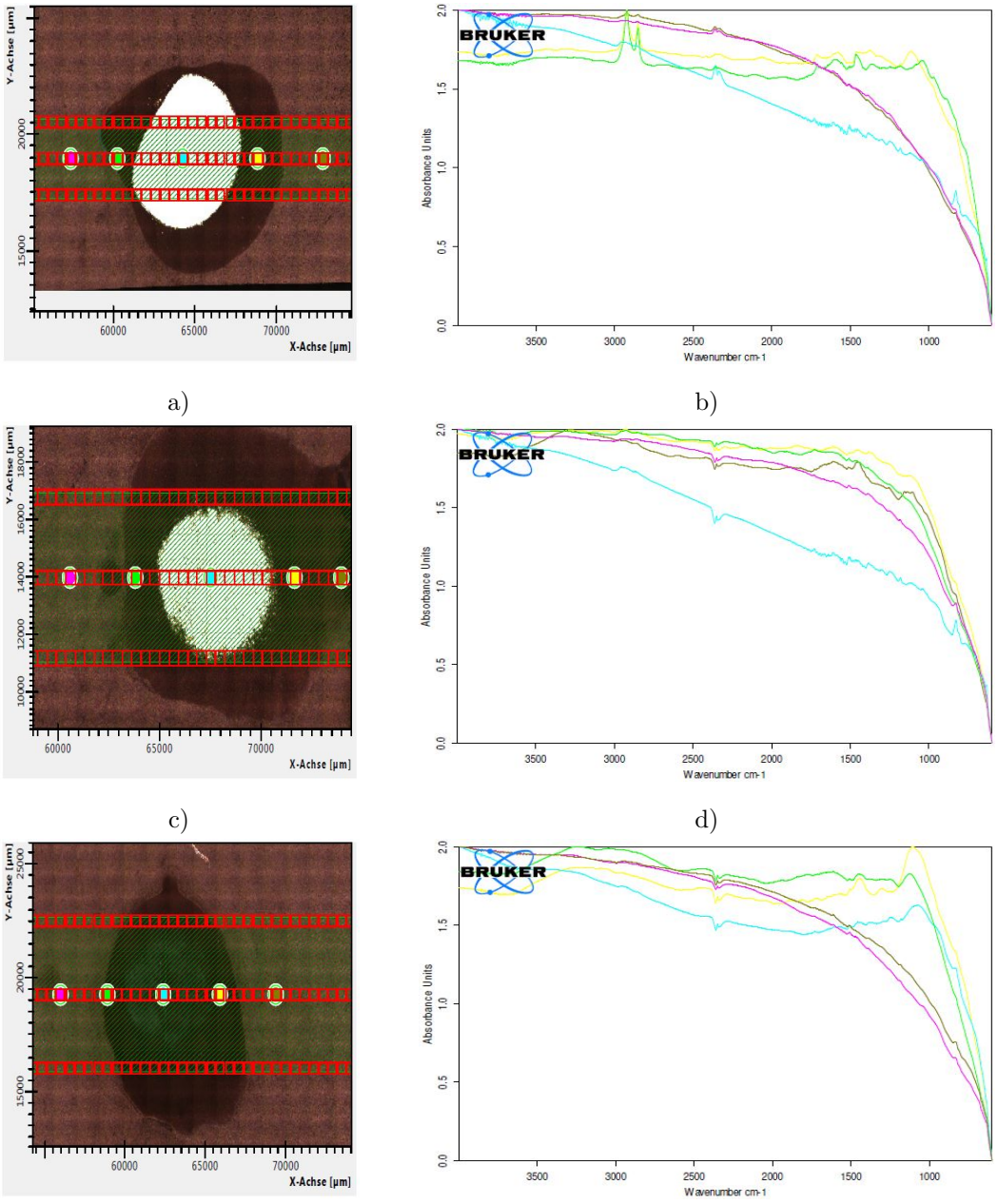


FIGURE 2.35: IR Spectroscopy of Cu-Seed etched samples. a) Measurement sites and b) Spectrum of MCL013; c) Measurement sites and d) Spectrum of MCL016 e) Measurement sites and f) Spectrum of MCL014

2.4 Thermo-Mechanical Properties

When printed copper metalization was first investigated on wafer level in 2013 [79], its favourable thermo-mechanical properties were the main reason for the deeper investigation into the material properties and manufacturing processes, which finally lead to this thesis. In the upcoming sections, material properties like the coefficient of thermal expansion and the Young's modulus as well as their interaction under thermal cycling will be measured and discussed.

2.4.1 Wafer curvature measurements

The CTE (coefficient of thermal expansion) mismatch of silicon and other materials typically leads to wafer bow when the material is heated. Wafer bow means that the wafer is bent from it's flat shape due to the tensile and compressive forces of deposited layers. With wafer curvature measurements, the magnitude of this effect can be studied within a defined temperature range. The acquired charts can also give information about microstructural changes within the system during annealing. It is hence a standard method for material characterization in semiconductor industry. Figure 2.36 shows two stress curves acquired from thermocycling of 1 μm PVD (sputtered) copper on silicon [83]. The two charts differ in the grain size of the copper layers, being 0.1 μm for 2.36a and 1 μm for 2.36b.

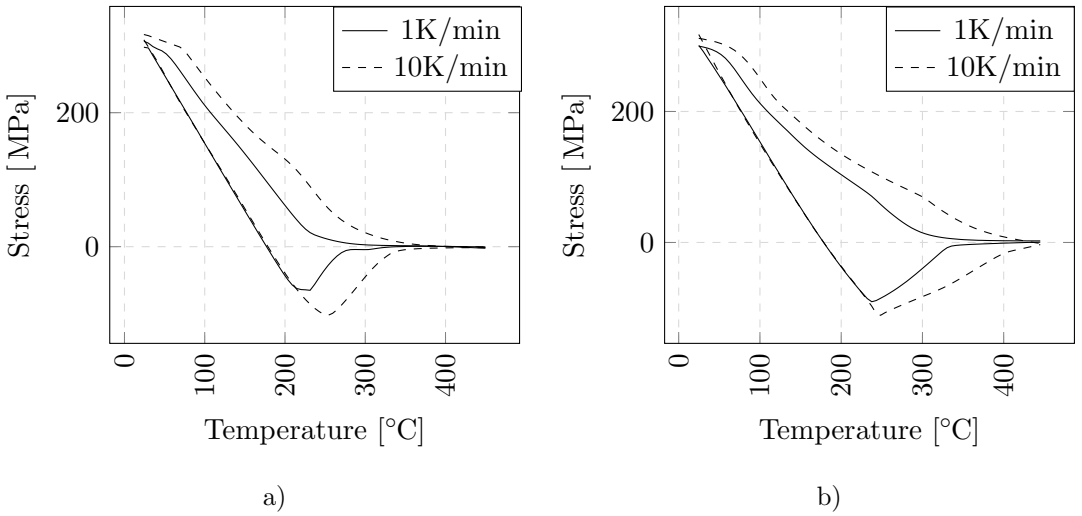


FIGURE 2.36: Stress curves for 1 μm PVD copper with a) 0.1 μm and b) 1 μm grain size on silicon. [83]

Stress relief in copper layers during thermocycling is achieved by grain boundary diffusion at higher temperatures and dislocation motion at all temperatures. According to literature [83], yield only occurs at lower temperatures in the cooling cycle, in the curves presented in figure 2.36 this would be at temperatures below 100 °C and stresses above 250 MPa. For porous materials, literature suggests that yield can occur at lower stress levels [84]. During the heating cycle, the stress curve follows a linear path from the tensile to the compressive regime until a temperature of around 225-250 °C, at which creep deformation starts. At this point, the plastic stress relaxation exeeds the applied loading rate [83].

Wafer curvature measurements of the first copper paste printed on silicon dummy wafers, which was the commercially available paste CP-003 from Intrinsiq Materials Ltd., were done by M. Schneegans. He investigated the wafer curvature during thermo-cycling between 50 and 400 °C and observed an interesting pseudo-elastic behavior. Figure 2.37 shows one result of such a wafer curvature measurement.

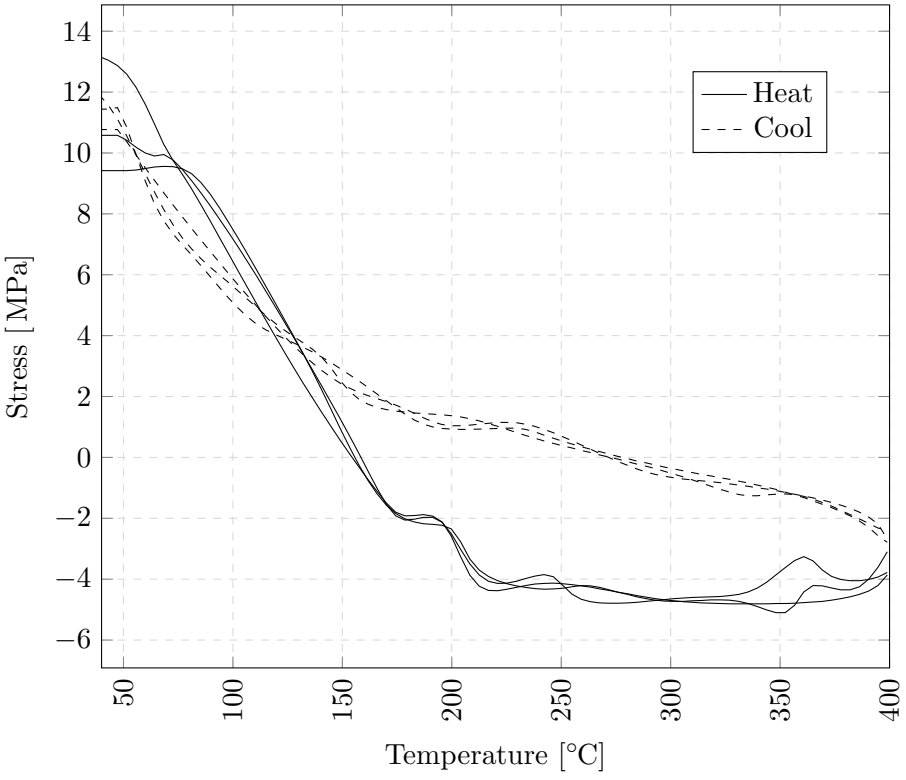


FIGURE 2.37: Layer stress of CP-INF-240415-R2 during thermo-cycling.

The response of this measurement is the wafer curvature, which is used to calculate the stress of the layer by using the Stoney equation. In section B.2.3.1 the method and its

limitations are explained in detail. From the graph, it can be seen that first of all the absolute stress value is only 10 MPa in the tensile (positive stress values)and around 5 MPa in the compressive range (negative stress values). This is extremely low, considering that bulk copper layers can have tensile stresses between 200 and 300 MPa [85]. A standard stress curve for ECD copper which was also acquired by M. Schneegans (figure 2.38) shows the typical behavior of bulk copper on silicon: At 50 °C the copper layer exerts high tensile stress to the wafer, which turns compressive at higher temperatures. Up to a certain temperature, in this case around 200 °C, the stress curve is more or less linear. At 200 °C at a stress of 50 MPa (compressive) creep deformation starts. The temperature is kept at 400 °C for one hour, which enables the material to relax. Upon cooling, the stress does not follow the heating curve but is showing a hysteresis.

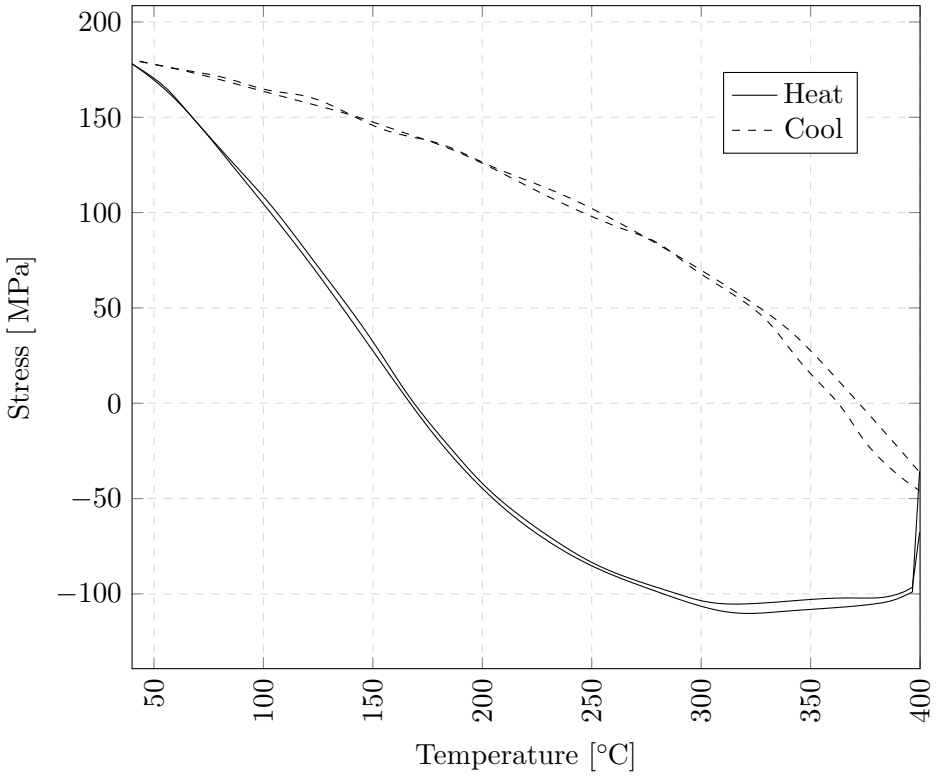


FIGURE 2.38: Layer stress of an electroplated copper film.

Comparing the stress curve of ECD copper to that on printed copper (figure 2.37) it is immediately evident why printed copper is so interesting: Put aside the absolute value of the stress exerted by the layers, the shape of the stress curve shows a pseudo-elastic behavior over the whole temperature range. At around 225 °C the knee in the curve indicates the beginning of creep deformation. The cooling curve is nearly in line with the heating curve.

The curve shown in 2.37 was acquired for the paste CP-INF-240415-R2, which is the paste with the highest porosity (on this wafer 48.9%) and hence also gives a rather high specific resistivity of 7.4$\mu\Omega$cm. Pastes with lower porosity like CP-INF-240415-R3 (36%, 4.8$\mu\Omega$cm) have higher stress values, but still show a similar stress behavior characterized by low hysteresis and pseudo-elastic linearity. The stress curve of CP-INF-R3 is shown in figure 2.39 for comparison.

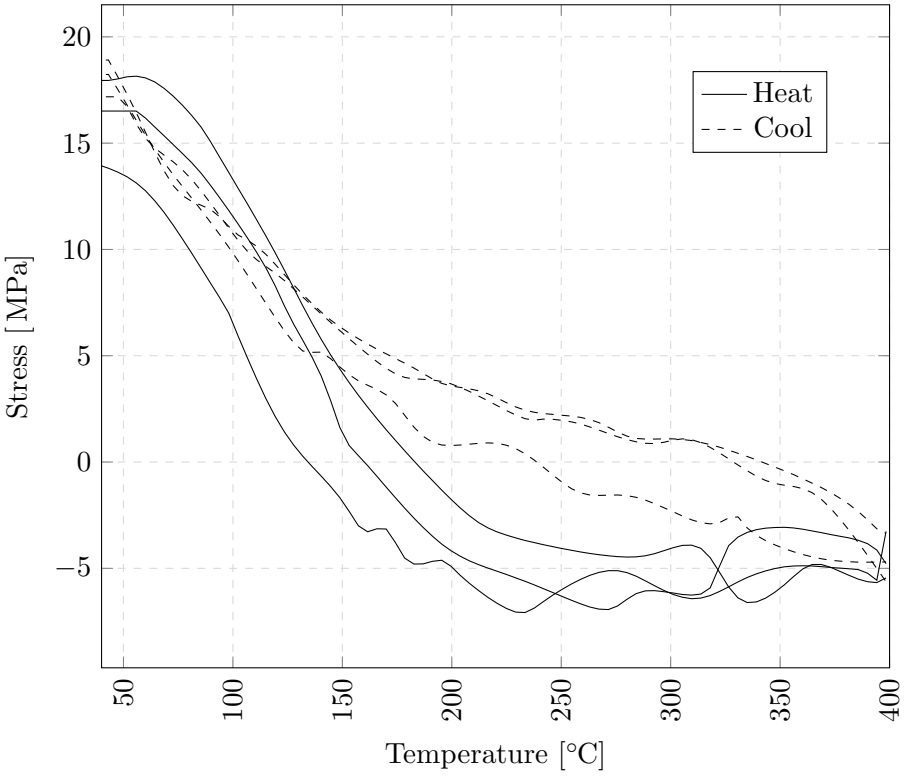


FIGURE 2.39: Layer stress of CP-INF-240415-R3 during thermo-cycling.

Here, the maximum tensile stress rises to around 20 MPa, while the compressive stress is well below 10 MPa. The highest stress is exerted by the paste CP-INF-240415-R1, which is the pure nano paste. It has a porosity of 26.5% (measured by gravimetric porosimetry on this wafer) and a resistivity of 3.7$\mu\Omega$cm, half of the value of CP-INF-R2. Its stress curve shown in figure 2.40 compared to the other pastes shows a destinct hysteresis, with maximum tensile stress of ca. 100 MPa and compressive stress of up to 20 MPa. Hence, the lower the porosity of printed copper, the higher become the maximum tensile and compressive stresses.

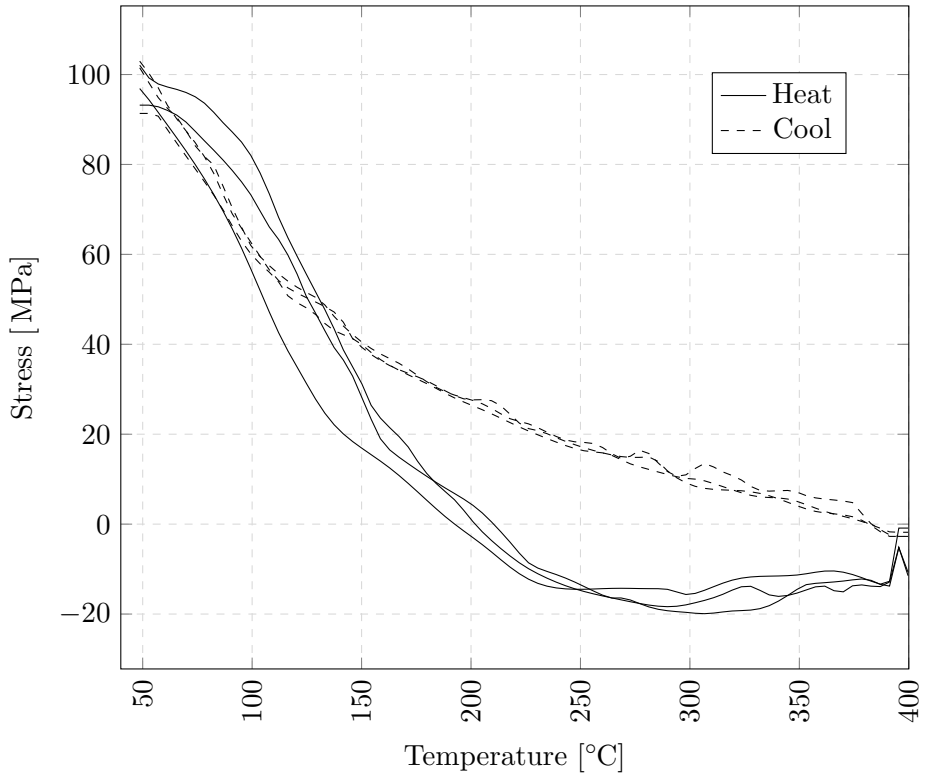


FIGURE 2.40: Layer stress of CP-INF-240415-R1 during thermo-cycling.

2.4.2 Coefficient of Thermal Expansion and Young's Modulus

The different coefficient of thermal expansion (CTE) of copper and silicon is the root cause for the stress that is exerted to the device upon temperature change. This connection can be visualized by a simple formula [83]:

$$\Delta\epsilon = \Delta\alpha\Delta T \tag{2.4}$$

The increment in strain $\Delta\epsilon$ is the product of the difference of the CTE of the two involved materials $\Delta\alpha = \alpha_2 - \alpha_1$ and the change in temperature ΔT. The boundary conditions for this relation are that the substrate is elastic and much thicker than the film. The instantaneous result of such a strain is elastic deformation, although when given time the deformation becomes plastic, which can be seen as stress relaxation e.g. in figure 2.38 during the holding period at 400 °C. For isotropic, equibiaxial stressed films, the stress is dictated by the elastic strain $\epsilon_{elastic}$:

$$\sigma = \bar{E}\epsilon_{elastic} \tag{2.5}$$

Here, $\bar{E}$ is the appropriate modulus given by E/(1-v), where E is the Young's Modulus and v is the Poisson's ratio. As an approximation, the Poisson's ratio can be neglected. Combining equation 2.4 and 2.5 gives:

$$\Delta\sigma_{(T)} = \alpha E \tag{2.6}$$

The slope of the stress curve in the elastic range $\Delta\sigma_{(T)}$ equals the CTE times the Young's modulus of the material. In case of the Paste CP-PLS-291014-R1 (Figure 2.41), the slope of the heating curve between 50 and 150 °C equals 0.289 MPa · K^{-1}, which would give a Young's modulus of 16.4 GPa when using the literature value of the CTE for copper of 17.6 ppm · K^{-1} [86].

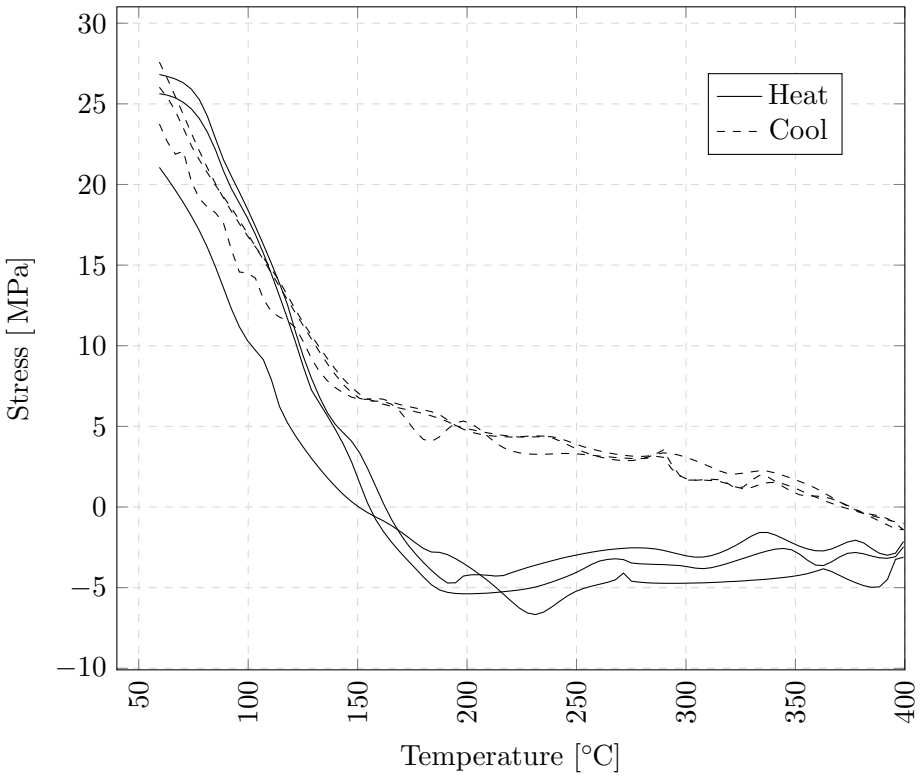


FIGURE 2.41: Layer stress of CP-PLS-291214-R1 during thermo-cycling.

According to literature [38], the CTE is not affected by porosity, hence the assumption that the CTE of printed porous copper is valid in case there are no impurities in the

layer. Since there is at least a small amount of other metals contained in the paste, as could be proven by ICP-MS measurements (section 2.3.1.1), it is unlikely that the CTE is not affected by those at all. Eichinger measured the CTE of CP-PLS [62] and found it to be 18.9 ppm $\cdot$ K^{-1}. Using this CTE in equation 2.6 would give a Young's modulus of 15.3 GPa.

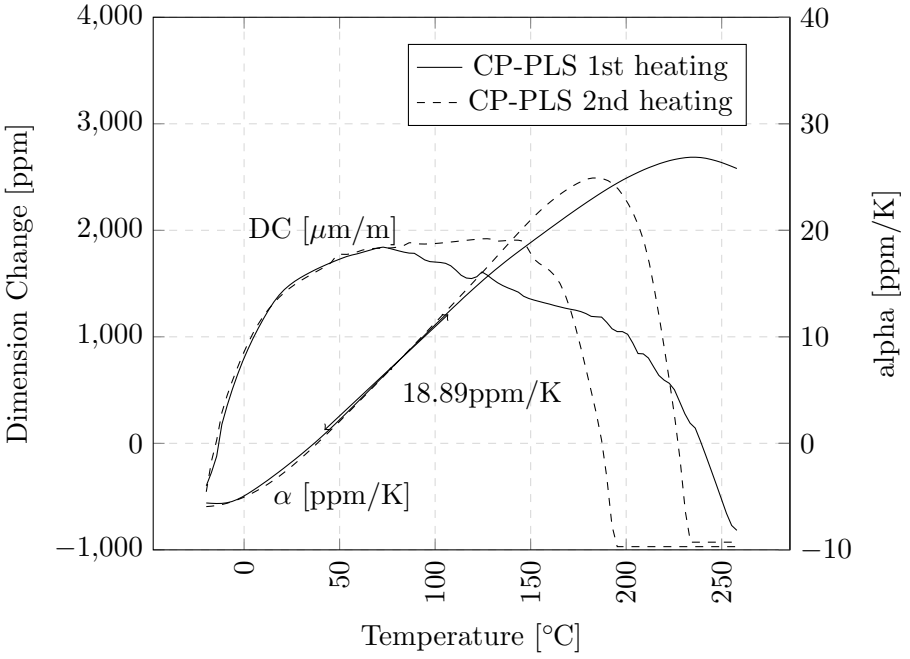


FIGURE 2.42: Coefficient of thermal expansion of cured CP-PLS-291014-R1, measurement by K. Unterhofer, FA Regensburg [62].

For comparison, electroplated copper has a Young's modulus of 23-201 GPa [22], with typical values in the range of 70-180 GPa. The electroplated copper shown in figure 2.38 would have 79.5 GPa, again assuming the CTE of pure copper. A method to directly measure the Young's modulus of polymers is DMA (dynamic mechanical analysis) [87]. In this method, a sinusoidal stress is applied to a layer and the responding strain is measured. For viscoelastic materials, the strain will lag behind the applied stress, following equations 2.7 and 2.8.

$$\sigma = \sigma_0 \, sin(t\omega + \phi) \tag{2.7}$$

$$\epsilon = \epsilon_0 \, sin(t\omega) \tag{2.8}$$

Here, ω is the frequency of the strain, t is the time and ϕ is the phase shift.

$$E' = \frac{\sigma_0}{\epsilon_0} cos\phi \tag{2.9}$$

$$E'' = \frac{\sigma_0}{\epsilon_0} sin\phi \tag{2.10}$$

The storage modulus (equation 2.9) measures the stored energy, representing the elastic portion, whereas the loss modulus (equation 2.10) measures the energy dissipated as heat. The two moduli are connected by the phase angle ϕ (equation 2.11) by which the strain ϵ is lagging behind the sinusoidally applied stress σ.

$$\phi = arctan\frac{E''}{E'} \tag{2.11}$$

Figure 2.44 shows the corresponding loss modulus E" measured on a layer of CP-PLS-291014-R1. As it can be seen by comparison with figure 2.43, it is by more than one order of magnitude lower than the storage modulus E', which indicates clearly elastic behavior. At room temperature (25 °C), the storage modulus is 18.1 GPa, whereas the loss modulus attributes to only 300 MPa.

The plausibility of those results was confirmed by nano-indentation measurements done by K. Unterhofer, who measured on an average of 18 indents at a penetration depth of 1500-2900 nm a Young's modulus of 23.46 ± 10.45 GPa. Despite the high spreading of this result, the range in which the Young's modulus could be expected was confirmed. Table 2.7 gives an overview on the different measurement results:

Method	Young's Modulus
Wafer curvature	15.3-16.4 GPa
DMA	18.1 GPa
Nano-indentation	23.46 ± 10.45 GPa

TABLE 2.7: Young's modulus of CP-PLS-291014-R1 measured with different methods.

Summarizing and putting this data in context, the CTE of printed copper is similar but slightly higher than literature would suggest, which is probably due to impurities in the layers. The elastic modulus is - depending on the reference point - by the factor 5-10 lower than for bulk copper, which is desirable because it results in less stress exhibited to the substrate upon heating. As the stress curves suggest (figures 2.37, 2.39, 2.40, 2.41),

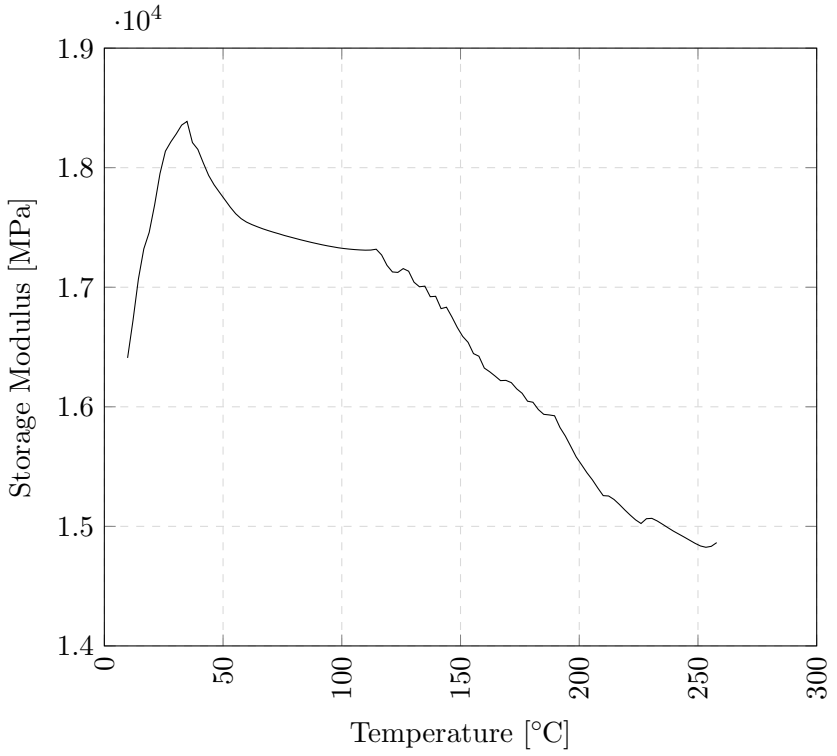


FIGURE 2.43: Storage modulus of cured CP-PLS-291014-R1, measurement by H. Preu, FA Regensburg.

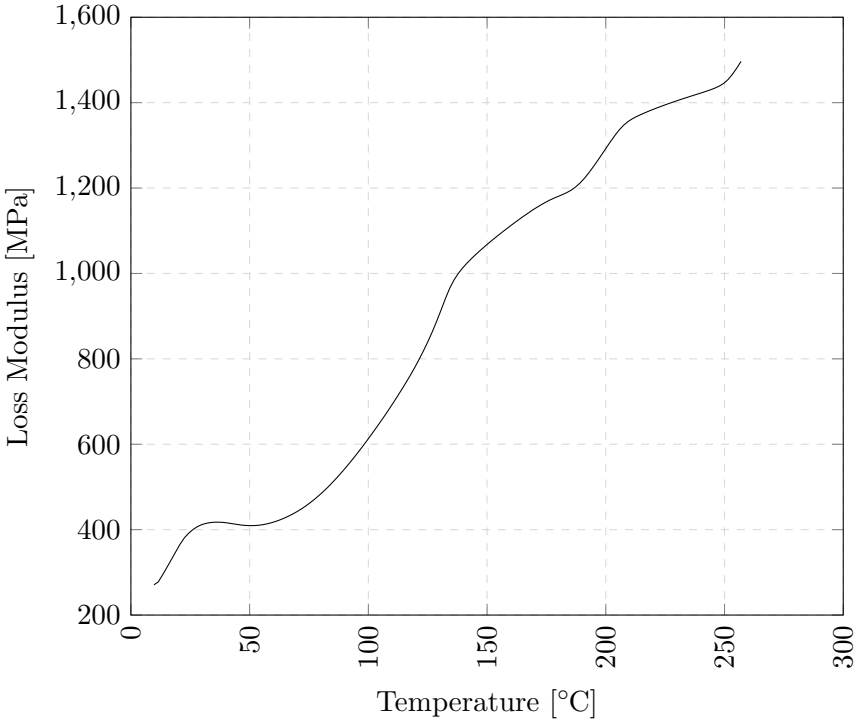


FIGURE 2.44: Loss modulus of cured CP-PLS-291014-R1, measurement by H. Preu, FA Regensburg.

the elastic modulus of porous copper is dependent on the porosity, which is supported by literature [88].

2.5 Reliability

Reliability is defined *as the ability of an item to perform a required function under stated environmental and operational conditions for a specified period of time* [89]. Due to its higher specific heat capacity and thermal conductivity, the introduction of copper metalization and wiring has reportedly increased the reliability of IGBT and free-wheeling diode power semiconductor devices [90]. The introduction of thick porous copper layers might further enhance reliability by providing additional heat capacity to the devices, if on the other hand the material itself does not fail. The upcoming chapter will present data on the oxidation behavior of printed copper layers (section 2.5.1) and report on the attempts to collect reliability data during thermal cycling (section 2.5.2).

2.5.1 Oxidation Stability

In contrast to aluminum, copper does not form a protective passivation layer which inhibits further oxidation [91]. This leads to a continuous oxidation of copper as long as it is exposed to oxidizing ambient. The oxidizing behavior of copper is strongly dependent on the temperature regime it is happening in: While at high temperatures above 1000 °C oxygen travels in copper by lattice diffusion, at lower temperatures below 800 °C it moves predominantly at the grain boundaries [92]. Since impurities are often precipitating at grain boundaries, they influence the oxidation rate of copper at lower temperatures by reducing the activation energy, hence promoting oxidation.

The rate determining step of copper oxidation at temperatures between 600 and 900 °C is the outward diffusion of copper [92]. For semiconductor devices, the temperature range between 150 and ca. 300 °C is the most important. Recent research could confirm that the grain boundary diffusion is the rate determining step also at temperatures below 300 °C [93]. Copper oxidized at low temperatures typically forms a thin CuO layer on the surface, covering a growing Cu_2O layer. Below the Cu_2O there is a decreasing concentration of oxygen dissolved in the copper matrix. Low temperature copper oxides

typically have a very fine grain structure, thus promoting oxygen diffusion, whereas oxides formed at high temperatures form large grains with therefore few grain boundaries. Hence, a short high-temperature oxidation treatment is proposed as oxidation protection of copper surfaces [93].

One of the most severe concerns about the technology integration of porous copper metalizations is the uncertainty on how strong the influence of the porosity on the oxidation rate is. Experiments on that topic were carried out by K. Rott in cooparation with H. Doyen, FA Regensburg. Samples of full-face printed CP-PLS-291014-R1, QNA6449 were oxidized in a furnace under ambient atmosphere at 250 °C together with reference samples of electroplated copper. Figure 2.45 shows the samples before (a) and after up to 150 h (e) of furnace treatment. As expected, the oxide growth is visible by a dark discoloration of the surface.

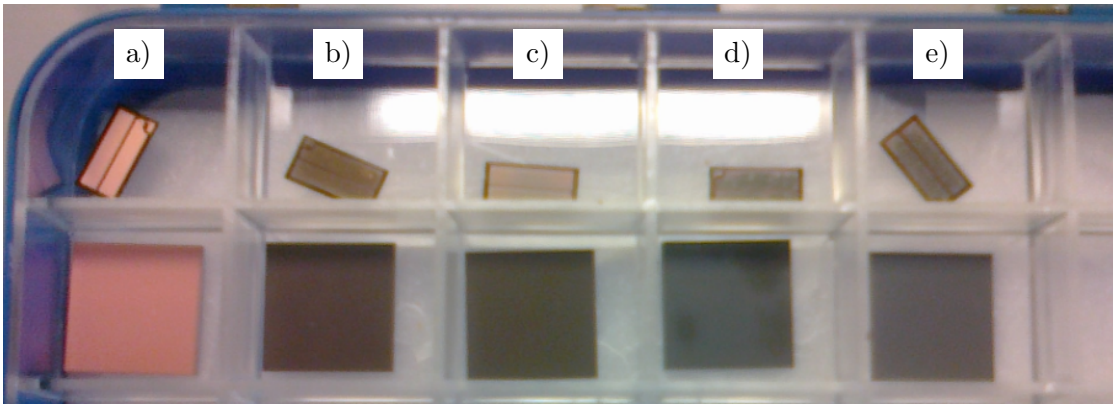


FIGURE 2.45: Samples of CP-PLS (bottom) and ECD copper as a reference (top) after oxidation at 250 °C for a) 0 h, b) 10 h, c) 50 h, d) 100 h and e) 150 h.

The samples were then FIB cut to further investigate the depth of oxidation. Figure 2.46 shows the porous copper sample before (2.46a) and after (2.46b) 150 h of oxidation at 250 °C. It is clearly visible that the pores were partially filled with copper oxide. Copper oxide has a lower density of 6.0 $g \cdot cm^{-3}$ (Cu_2O) or 6.3 $g \cdot cm^{-3}$ (CuO) than pure copper (8.96 $g \cdot cm^{-3}$) [94] and therefore causes a reduced porosity upon growth. The surface of the layer is covered with a dense layer of copper oxide (2.46c), which is a phenomenon similar to the results on ECD copper (2.46d).

The FIB cuts already give a first indication that the oxidation of porous copper layers might be accelerated compared to the ECD deposited samples. The open pores clearly allow for the oxygen to enter the deeper parts of the layer, whereas the oxidation of

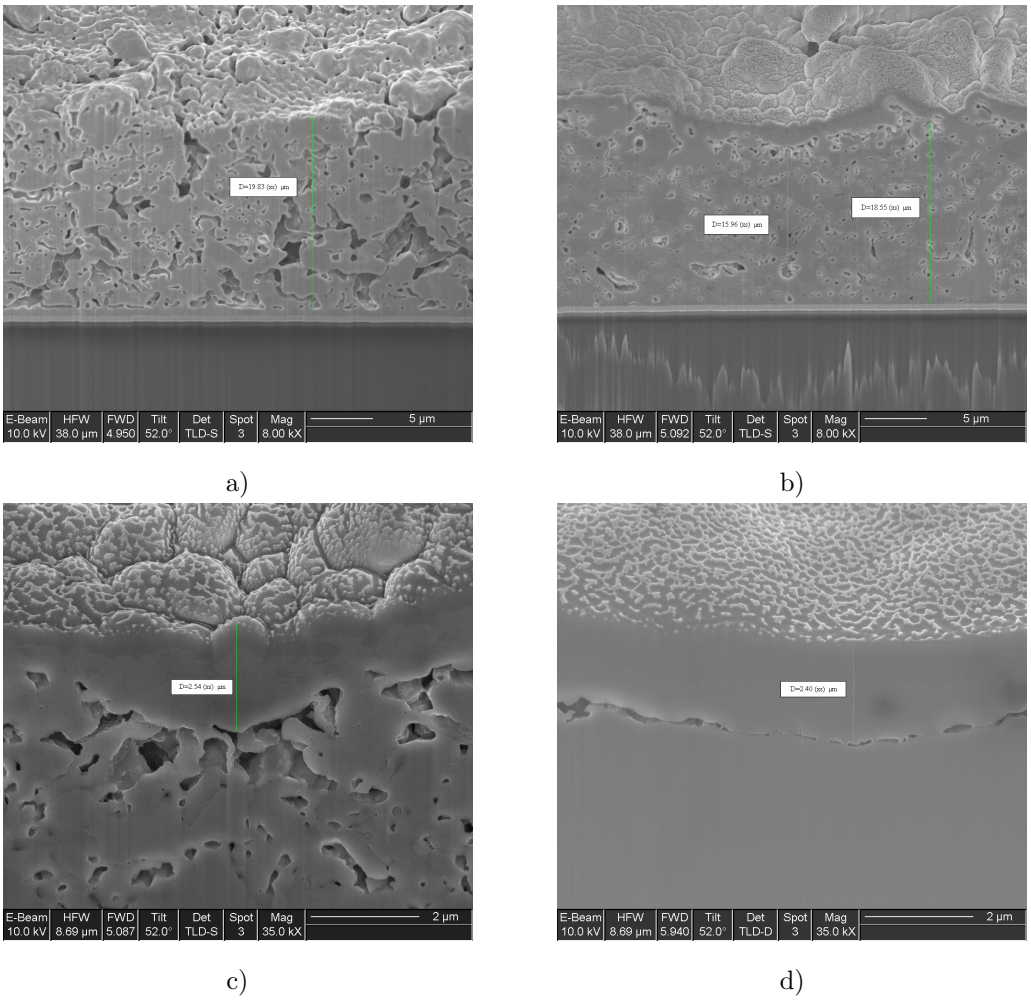
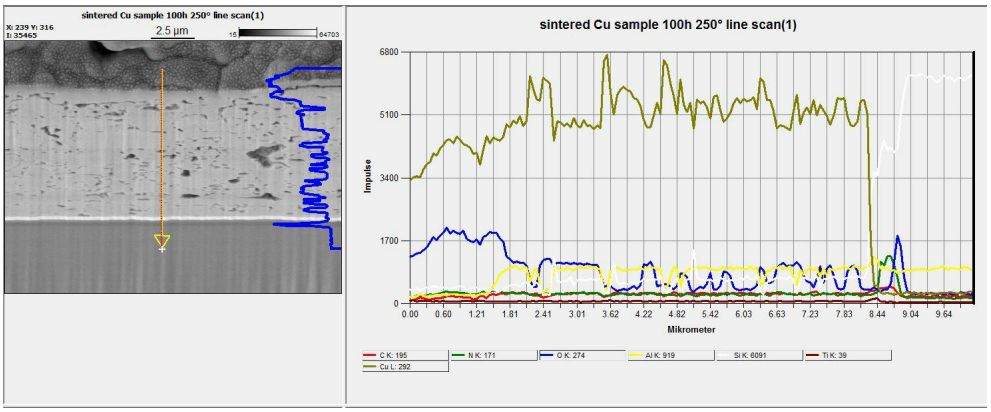


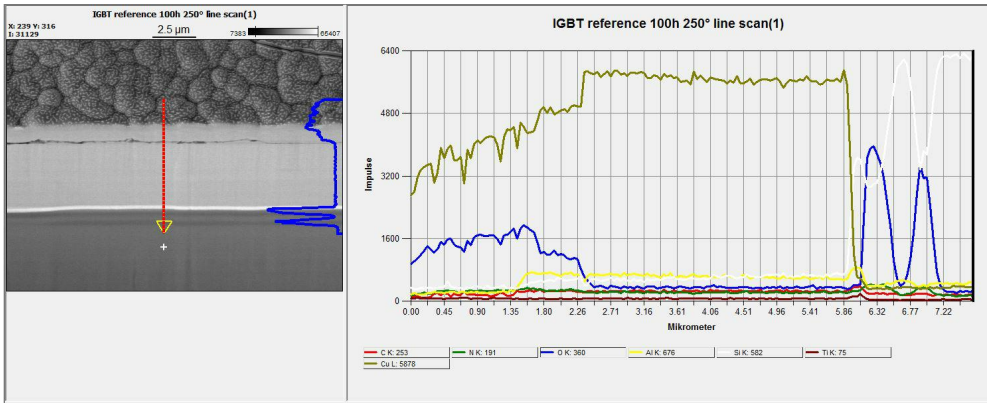
FIGURE 2.46: FIB cut cross-section of CP-PLS sample a) before and b) after 150 h of oxidation, with detailed view on the surface c) and the surface of the reference ECD copper sample d).

the ECD layer is proceeding slowly from the top to the bottom. On the other hand, the pores are closed upon oxidation due to the lower density of the oxide compared to pure copper. This, and the formation of the dense layer of copper oxide on the surface of the samples might slow down the kinetics of the oxidation after an initial phase of rapid oxide growth. Figure 2.47 shows the results of EDX investigations on the oxidized samples. EDX line scans were performed on the cross-section to visualize the oxygen content in dependence on the depth. The ECD sample shows a distinct layer of roughly 2 μm copper oxide on top of a non-oxidized metal layer. The oxygen concentration in the porous copper sample is less uniform, indicating the presence of oxidized and non-oxidized areas in the sample. On top of the layer there is a region with very high oxygen content which can be clearly discriminated from the rest of the sample.

The EDX investigations could show that there is some copper oxide inside the porous



a)



b)

FIGURE 2.47: EDX analysis on the FIB cut cross-section of samples of CP-PLS (a) and ECD copper (b) oxidized for 150 h.

network. To estimate the impact on the reliability of a device metalized with porous copper, resistivity measurements were performed on the oxidized CP-PLS samples as well as on the reference samples. Due to the high thickness of the oxide layer, the standard tool for resistivity measurements, the CDE ResMap, was not suitable for the measurements. Therefore, the test was carried out by E. Griebl in Munich with a wafer testing machine. A photograph of the measurement array is shown together with the results in figure 2.48. To establish contact, the oxide layer was penetrated with the needles by force. The measurement data suggests that there is no significant difference of the change in resistance between the ECD and the printed copper sample, although the data shows a strong scattering of the results. The basic message of this measurement is that there is no dramatic increase of resistivity visible on the porous copper sample, which indicates that despite the oxide growth inside the pores, there seems to be a remaining conductive path of copper particles for the electrons to flow.

A similar behavior was seen during long-time storage of printed copper. A sample of

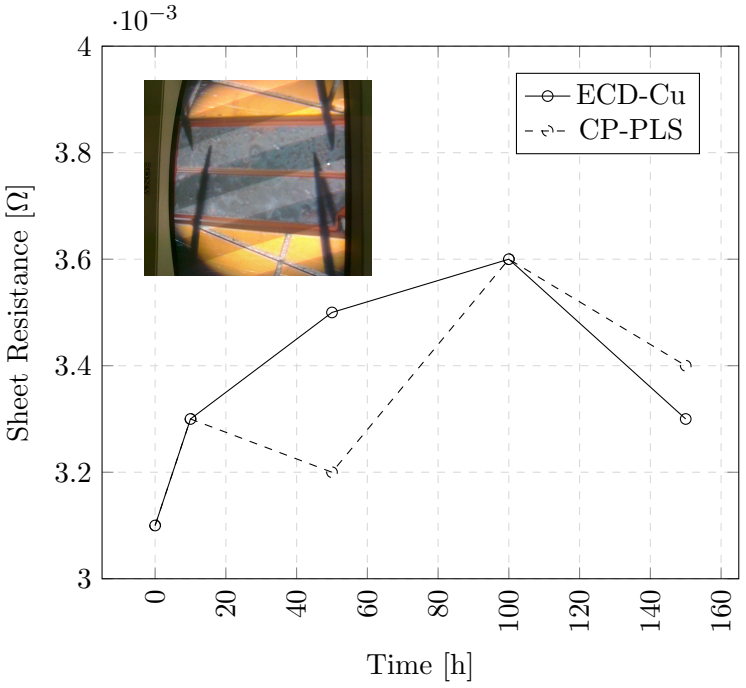


FIGURE 2.48: Resistivity of printed and ECD deposited copper after 0-150 h of oxidation at 250 °C. A picture of the measurement array is shown in the top-left corner of the graph.

CP-PLS-291014-R1, QNA6449 was cured at 400 °C and then stored in the cleanroom for one year. The sheet resistance was measured on the tool CDE ResMap in regular intervals. Figure 2.49 shows the results of this measurement: after an initial rise, the resistivity stays constant. This information is not just important for the application of printed copper, but also for the material characterization and the process development. Based on this knowledge, resistivity measurements were done after a waiting period of 24 h in order to reduce the time factor.

Summarizing, the oxidation behavior of porous copper can be separated into two phases: in the initial phase, a rapid growth of the oxide layer inside the porous network is observed. At high temperatures (250 °C) the oxide growth is fastest on the top of the sample from where the oxygen supply is originated. Therefore, the top oxide layer is expanding, thus closing the pores and initiating the second phase of the oxidation, which is diffusion limited. Instead of entering the porous network via the gas phase, after closing the top layer oxygen and copper need to diffuse through the top copper-oxide, a process which is by far slower and therefore limits further oxidation. This finding is supported by literature, where a parabolic rate constant for the diffusion of copper

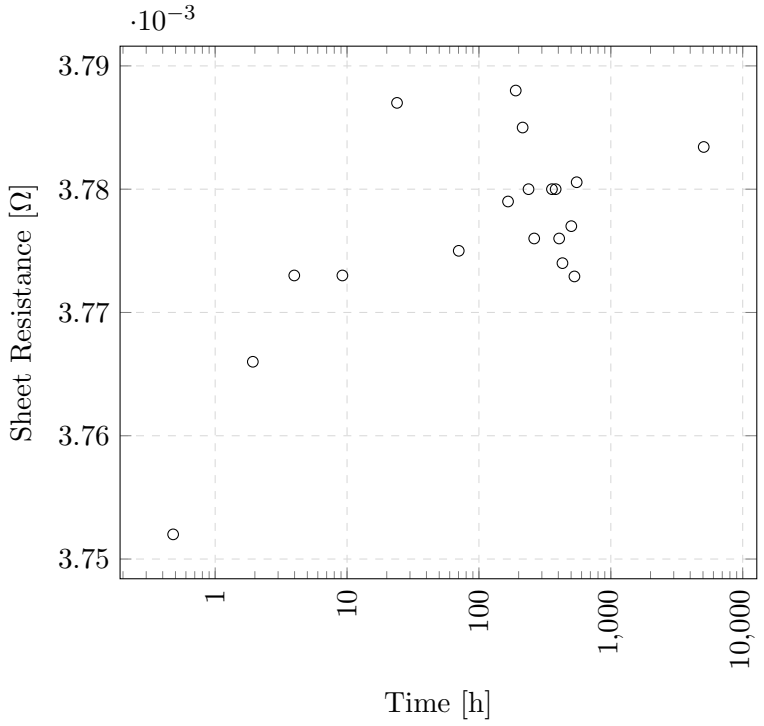


FIGURE 2.49: Development of the resistivity of printed copper during storage in the cleanroom.

atoms via vacancies in Cu_2O was found, i.e. the oxidation rate is reduced by the growing copper oxide layer [92], [95].

Future test series at different temperatures could show whether the formation of the top oxide layer is temperature dependent. This information would be crucial for the technology integration, because it could mean that after wire-bonding a burn-in step would be necessary to close the pores. Also, the microstructure of the layer after oxidation and subsequent reduction could be of interest.

2.5.2 Poly-heater Test

As mentioned in the introduction, modern power semiconductor devices are challenged by increasing power densities and switching rates. Fatigue failures can occur due accumulated permanent damage during thermal cycling, which is happening each time the device undergoes a normal power-up and power-down cycle upon operation. Such temperature cycles induce a cyclical stress, which weakens the materials and can cause several different types of failures, including thin-film cracking, lifted bonds and cracked

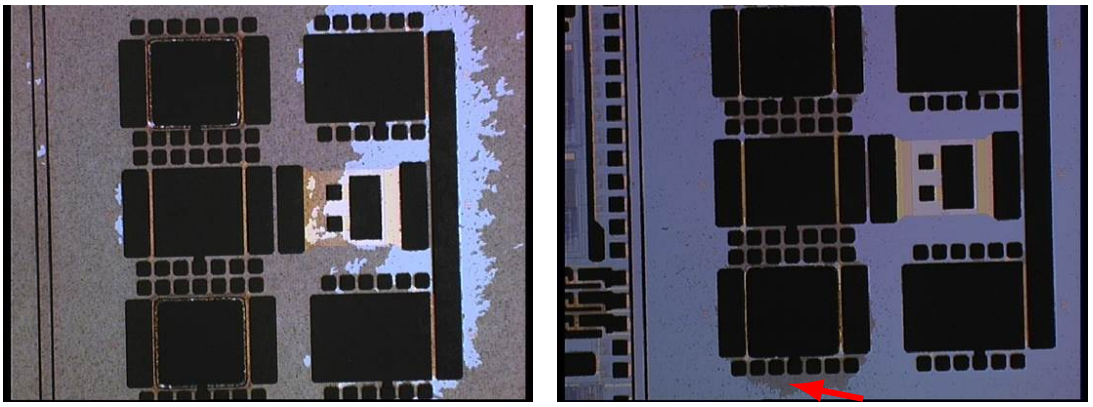
dies, to name a few [96]. For reliability testing it is important to simulate such temperature cycles as close to the application as possible with even harder conditions. The introduction of poly-heater test structures into material reliability testing therefore has extended the capabilities of material scientists to characterize and fine tune power metalizations. In-situ Poly-heaters have the advantage over conventional heat chucks that higher temperatures with very high ramp rates can be realized, which shortens the required testing time and increases the stress to the device [97]. Additionally this type of test setup offers the possibility to generate and conserve defined states of degradation, since also the temperature drop after switching off is very high, leading to negligible additional stress during the cooling time [98].

The favorable thermo-mechanical properties of printed porous copper described in section 2.4 suggest that such materials might also be more reliable than conventional copper metalizations, as they do not cause that much mechanical deformation to the device as non-porous materials. On the other hand, pores - especially when connected to each other - could also pose a predetermined breaking point to the metalization layer, which could cause the device to fail even earlier.

Poly-heater test devices are typically designed on the basis of commercial power semiconductor devices, i.e. they use the same basic material, similar layer stacks and comparable die sizes. The relevant area of the device generally consists of a polycrystalline silicon pad with contact pads and a barrier stack including the metalization layer of interest on top. Also, depending on the poly-heater design, there might be temperature and resistivity sensors integrated within the build-up. The pads under investigation have typical edge lengths of several hundred micrometers up to one millimeter. The contact pads to the integrated sensors and the poly-heater are usually 40-100 μm away from the test pad, which is challenging for printed copper metalizations, as will be further discussed in section 3.2.

In a first approach, poly-heater wafers in the so called "R2015A"-Design were prepared by printing full-face on the test-wafers, leaving open only the alignment marks. After curing, the wafers were covered with a foil resist and exposed with a corresponding mask, aligning on the previously left open marks. After development, the wafers were then wet-chemically etched. Figure 2.50 shows the result after etching: The pads are

interconnected to each other by a material resistant to the etching chemistry. EDX investigations identified the material as bismuth oxide, which according to a response from the manufacturer was used as an additive in the paste at that time (Paste CP-131113-R1, QNA6198).



a) b)

FIGURE 2.50: Wet-chemically etched poly-heater devices with a) strong and b) moderate amount of bismuth-oxide residues. The red arrow indicates the position of the residues around the contact pads.

Since the bismuth oxide layer is interfering with the mandatory barrier etch it would cause short-cuts during the electrical cycling test. This is true for both, the strongly affected areas (figure 2.50a) and the moderately affected areas (figure 2.51b) of the wafer, indicated by a red arrow. As the adhesion of the layer to the underground was poor, removal in an ultrasonic bath with de-ionized water was tried.

The cleaning turned out to be difficult, as figure 2.51 shows: In figure 2.51a, there are still residuals of bismuth oxide present after the ultra-sonic treatment. Additional treatment bears the risk of pads lifting off, as happened to the device shown in figure 2.50b. A small percentage (less than 10%) of the devices looked fine in microscope after the post-treatment (figure 2.50c), but subsequent SEM investigations showed residues even on those devices. Additionally to the losses due to the bismuth oxide residues, the yield on the wafers was low due to poor adhesion of the photoresist foil (see also section 3.2.2.2) which lead to over-etched pads, as displayed in figure 2.50d. These results clearly indicate that an alternative way to wet-chemical etching is required for the sample preparation.

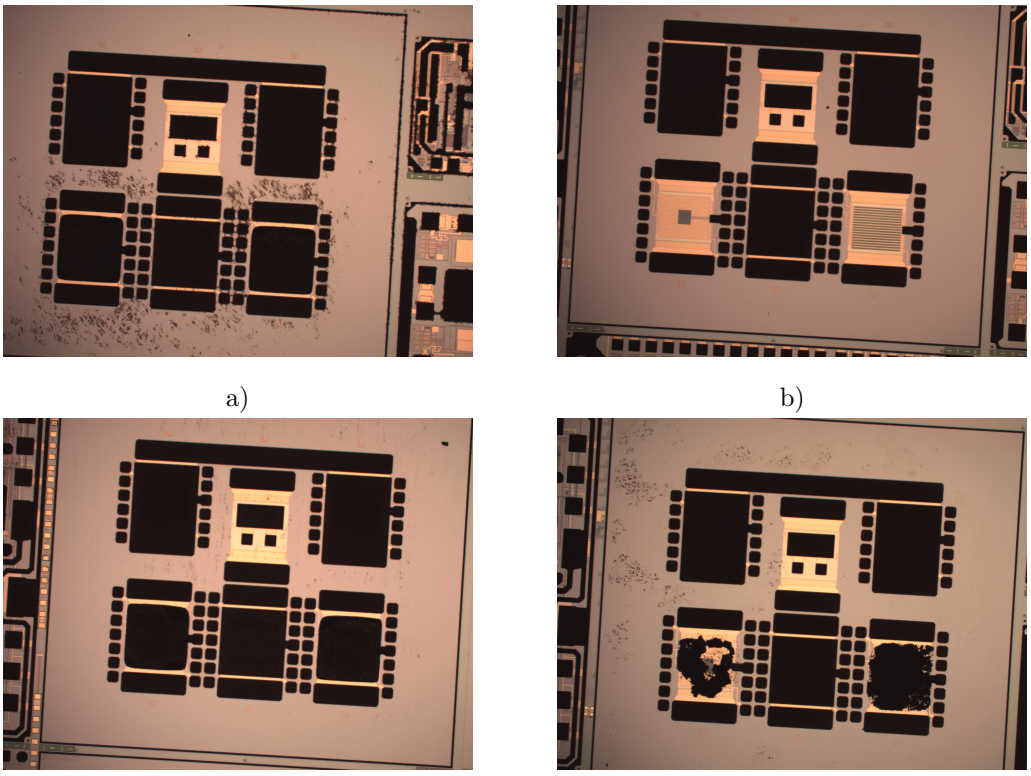
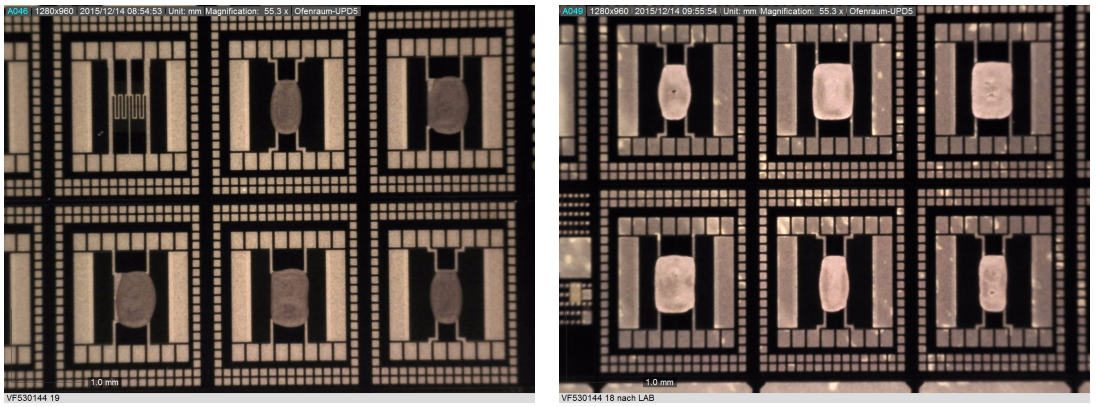


FIGURE 2.51: Wet-chemically etched poly-heater devices after post-treatment in an ultra-sonic bath showing a) insufficient cleaning, b) pad lift-off, c) sufficient cleaning and d) over-etched pads.

A more promising method to prepare poly-heater samples would be pattern pasting, as it will be later described in section 3.2.3. In short, this method includes printing the paste into a photo-resist mask and curing in a two-step process with an intermediate photo-resist removal step. Test wafers of the so called "R3832A" type were coated with a 20 μm thick THB121[6] resist, leaving the test-pad areas open. The paste CP-PLS-291014-R1 was printed with a structured stencil onto those pads. The batches QNA6449 and QNA6483 were used, having viscosities of 33,100 cP and 79,900 cP at 50 s^{-1} respectively. The viscosity of the paste is related to its solid content and is relevant for the layer thickness and the structural preciseness of the print. Best results could be achieved with batch QNA6483. Figure 2.52 shows exemplary test pads printed with this paste.

The shape of the pads is far from perfection, which is mostly due to a too low photo-resist mask height: The THB121 resist mask was 20 μm thick and was printed with a 80 μm stencil, which means that the paste had a total thickness of 100μm in wet state.

[6]For more details see section 3.2.3.



a) b)

FIGURE 2.52: R3832A poly-heater pads before photo-resist removal (a) and after the final curing step (b). Note that not the exact same position on the wafer is seen in the two pictures.

Later trials showed that by using a resist thickness of 50 μm combined with a 50 μm stencil, even smaller pads could be printed precisely (see e.g. figure 3.14). Still, some of the pads would qualify for electrical testing, which is why the wafers were forwarded to mechanical dicing. Here, two unfortunate facts lead to a premature end of the sample preparation: First, the test-wafers were using a rotated substrate. This means, that the dies were oriented with a 45° angle towards the crystal orientation, which was done due to the basic technology the poly-heater test design is based on. Since the wafer diameter was 300 mm, but the sintering furnace was only capable of housing 200 mm wafers, the wafers had to be broken into 200×200 mm squares before. The sharp edge of the wafer in 45° orientation to the sawing direction caused the sawing blades to break upon impact. A workaround that included performing a so-called "round-cut" to gain a wafer-shaped substrate with defined edges again failed due to the wafer thickness of 750 μm. The sawing wheel used for the round-cut was mechanically deformed in the deep sawing streets, causing it to break after reaching a certain depth.

With the blocking point in the dicing step, the wafers could not be further processed and tested. A repetition of the trial should include grinding of the wafers down to a final thickness of ca. 250 μm and avoiding the rotated substrate configuration, which is not required for the test anyway. Additionally, a thicker photo-resist like the THB151 should be used for increased yield during the printing step. Also using another poly-heater test-design like the "R0724D", which is using 200 mm substrate wafers might be an elegant solution to the problem. The R0724D pad design was used for the pattern

pasting trials in section 3.2.3, but on non-functional dummy wafers.

Chapter 3

Process Development and Technology Integration

The integration of a new material into an existing or new semiconductor technology always requires adaption of existing or the development of new processes, which is the reason why those two aspects are dealt with in one common chapter. For the front-side of the wafer, the processes were developed for an IGBT application with large pads and rather large distances between them, whereas the back-side processes were focused on a MOSFET type, which includes the possibility of thick copper pads that are very close to each other. Some major requirements and specifications for these two technologies are listed in table 3.1.

	IGBT	MOSFET
Application Type	front-side	back-side
Spec. Resistivity	$<5\,\mu\Omega$cm	$<3\,\mu\Omega$cm
Pad Size	4-10 mm	0.5-2 mm
Temperature Budget	400 °C	approx. 250 °C
Sawing Street Width	$>80\,\mu$m	approx. $40\,\mu$m
Interconnection	Wedge-wedge bonding	soldering
Low Wafer/Chip bow	not so critical	very important

Table 3.1: Table of requirements and specifications of the IGBT and MOSFET technologies.

Considering these requirements, two very different approaches are necessary to implement printed copper into these technologies. For the IGBT application, the major challenge is to ensure proper interconnection of the metalization layer to the lead-frame

by wire-bonding. In order to cope with the stringent mechanical requirements originating in the wedge-wedge bonding interconnection technique, investigations into an improvement of the barrier stack were done in parallel to this thesis. Therefore in case of the IGBT application, two different types of metal stacks below the copper paste were investigated, here called in short IGBT-A and IGBT-B. The two different stacks are shown in table 3.9 and 3.10. During the optimization of the copper paste itself towards improved bondability, compromises in terms of conductivity and stress reduction would be acceptable. Also, the requirements towards structural preciseness are not so critical.

The main limitation of the MOSFET application on the other hand is its thermal budget. As explained in section 1.8, the glass-carrier stabilization technique used for this technology includes the use of a thermally sensitive glue, thus limiting the maximum temperature that can be applied to the wafer after back-side grinding. Also the structuring is more critical here, since the chips are smaller and the sawing streets are narrower. As design rules require, the sawing streets need to be kept free of metal in order to ensure a smooth sawing process.

The upcoming chapter contains three major blocks of topics: Structuring (section 3.2), Sintering (section 3.3) and Interconnection (section 3.4). The section on structuring will discuss different additive and subtractive structuring methods for (porous) metals, including new innovative methods like etching through an ink-jet printed hot-melt mask (section 3.2.2.3) and structured printing into a removable photoresist mask (section 3.2.3). Within the section on sintering, first different principle ways of metal particle sintering are discussed, before the method used in this thesis is being described and optimized towards low resistivity on the one hand (section 3.3.3) and compatibility with the glass-carrier thin-wafer stabilization technique on the other hand (section 3.3.4). Finally, the topic of interconnection will be addressed, first with focus on different types of wire-bonding (section 3.4.2), then dealing with investigations into the soldering behavior of porous copper (section 3.4.3). Before all of this, a brief section on the risk-handling of cross-contaminations will give an overview on the measures undertaken to prevent spreading of copper particles and ions in the clean room environment.

3.1 Risk-Handling of Cross-Contaminations

Copper is considered a critical material in semiconductor industry as it can cause severe damage to production if contaminations of it are spread within the FEOL. In direct contact with silicon or silicon oxide (e.g. gate oxide!), copper tends to form silicides even at low temperatures (100 °C) [99]. Growth rates are depending on the grain orientation of the silicon substrate, with silicon in the orientation (100) having up to 5 times higher growth rates than on silicon (111) as can be found in literature [100]. Due to the CTE mismatch of copper and silicon, small cracks can then occur in the contaminated oxide passivation, opening channels for accelerated diffusion [101]. Alternatively, also interstitial diffusion rates of copper in silicon are high [102], especially if an electric field is applied [5]. The copper atoms are then forming conductive paths within the silicon oxide, leading to electrical shorts and hence the failure of the dielectric material [101].

In order to avoid cross-contaminations between the BEOL and the FEOL, a number of precautions like dedicated tools, dedicated and optically diverging cassettes and spatial segregation are taken in semiconductor industry. As copper printing pastes are new and not yet in productive use, not much experience exists in terms of contamination paths. Therefore, a thorough risk management is necessary to prevent cross-contaminations.

The printing equipment was dedicated for the use with copper pastes, so it was not in contact with productive wafers. The printer itself is a closed system including an air exhauster, as can be seen in figure 1.11. For applying the paste to the stencil, the printer needed to be opened. The handling area for the paste and the contaminated parts was a white, Teflon^{TM} covered surface which was thoroughly cleaned with isopropyl alcohol after use. The tissues used for cleaning the surface, printer parts and utensils were wrapped into special gloves, which were worn over the standard clean-room gloves during paste handling, and disposed into a dedicated hazardous waste container. The used wafer cassettes were labeled as dedicated for copper pastes and cleaned after each use.

Since the drying furnace was not dedicated solely for the use with copper pastes, it was a possible location for cross-contaminations. The pastes were dried in separate furnace runs, and the sites where the cassettes had contact to the furnace were cleaned

with isopropyl alcohol directly after each run. The equipment was subject to regular contamination checks.

Another critical point was the return of the wafers from the curing furnace into the clean-room, since the curing furnace was located in a maintenance area. Transport outside the clean-room was done with hermetically sealed transport boxes. The hot-plate of the curing furnace was the only part having direct contact to the wafers and was cleaned in regular intervals. Also, only clean silicon wafers were processed on the equipment. Particles lying on the wafer surface were blown of by compressed air before entering the clean-room. Still, this part of the processing block was most critical for contamination risk management, which is why by the end of this thesis a new curing furnace was installed within the clean-room.

Storage of the pastes took place in a locked chemistry cabinet, where the pastes were again stored within a sealed container. Any handling of the pastes or its storage container was performed using an additional pair of gloves worn over the usual clean-room gloves. These measures ensured a relatively safe handling of the material, minimizing the risk of cross-contaminations to the lowest practicable level.

3.2 Structuring

Depending on whether the paste is used as front-side or as back-side metalization, structuring becomes a key aspect of the process flow. On the one hand, the ability to directly structure the paste by stencil printing without the need for lithographic masks is one major advantage of paste printing. On the other hand, the capability of direct printing for the generation of small, defined structures is limited because it is impossible to realize a 90 ° edge angle with direct printing since the solvents will always cause the paste to spread out as soon as the stencil is being removed. Hence, the size of the printed pad and the distance to the next critical structure that must not be overprinted determines whether direct printing is possible, or whether additional structuring methods need to be used. Structuring methods that are used after printing are usually subtractive, for example wet-chemical etching or laser ablation, which makes them usually less favorable because they require additional process steps and also waste material. Also, they are limited in terms of achievable aspect ratio, which is usually an issue on the back-side

of the wafer. Several power semiconductor technologies require gaps as small as 40 μm between two pads, which is impossible to achieve with copper layers of more than 20 μm thickness, as will be explained in the respective section 3.2.2. Since the application of porous copper starts to become interesting at thicknesses of more than 20 μm, alternative ways of structuring need to be developed, as it will be shown in section 3.2.3.

3.2.1 Direct Printing

The correct definition of direct printing would be to structure paste on a blanket wafer, without supporting lithography that keeps the paste in place and prevents rinsing. Usually metal pads are surrounded by a dielectric layer that upon operation prevents arcing[1]. Therefore, direct printing on non-structured wafers is not relevant for production and was not studied in detail. To distinguish between the photoresist assisted pattern pasting discussed in section 3.2.3 and printing into an imide mask, the latter one is referred to as direct printing. This is a valid generalization since the typical thickness of imide passivation layers used on most chip technologies is between 5 and 10 μm [103], meaning that the imide alone will not prevent the wet copper paste from spreading, as it would be the case for a 50 μm THB mask (see section 3.2.3). The main requirement for successful direct printing on power semiconductors like IGBTs is therefore to structure copper paste by a stencil mask in a way that it does not exceed the imide passivation surrounding the pad. This is especially critical in the gate-pad area, since an electrical connection between the source and the gate pad would lead to a devastating short circuit.

An example for a direct printed structure can be seen in figure 3.1. The copper paste is seen as a large dark area in the top-left corner, covering the largest part of the image. The imide mask is the brown frame surrounding the copper paste and separating it from the yellow gate pad. The light brown area between the imide and the dark paste is copper paste that is partially overprinted on the imide. The alignment of the stencil to the imide structures was very good in this trial, but the stencil opening was approximately 20 μm too large in each direction, resulting in the imide being partially overprinted. Still, there is no shortcut between the source and the gate pad. Figure 3.2 shows such shortcuts,

[1] Arcing occurs since the front side of the die (the drain contact) is under a different potential than the DCB.

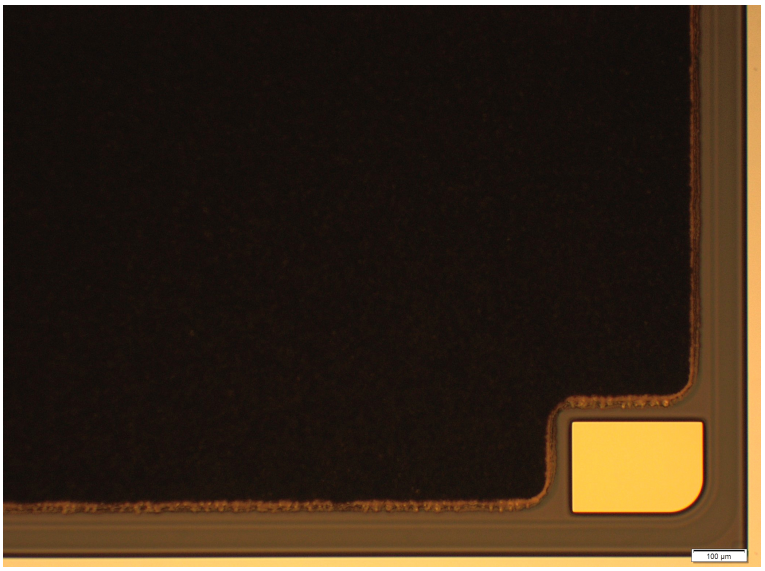
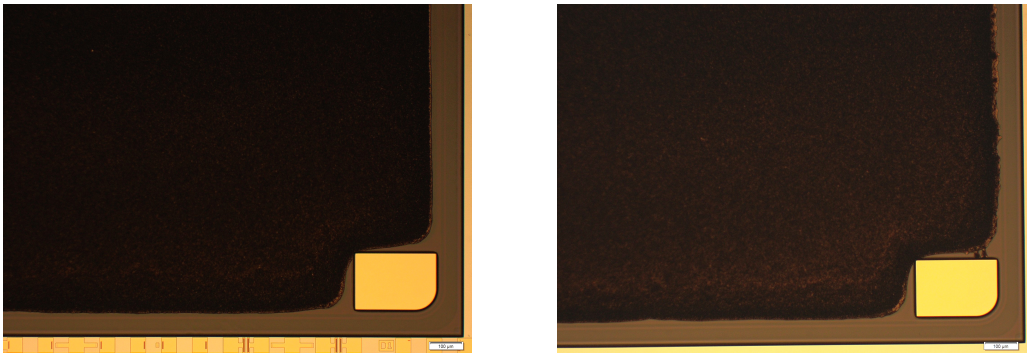


FIGURE 3.1: Direct printed copper pad on an IGBT source pad.

in case of 3.2a due to an issue with the printing direction, in 3.2b due to poor stencil back-side cleaning.



a) b)

FIGURE 3.2: Direct printed copper pads on IGBT source pads with short-cuts due to the printing direction (a) and stencil back-side contamination (b).

The printing direction in figure 3.1 was from the bottom of the picture to the top, meaning that here the paste was pushed away from the imide. The wafer seen in figure 3.2a was printed from top to bottom, which pushed the paste into the corner of the gate pad, leading to a short-cut. The DEK Horizon printer offers the possibility to adjust the alignment of the stencil towards the wafer in x- and y- directions depending on the print direction, so it is possible to increase the distance of the stencil edge to the imide edge when printing downwards by additional e.g. 20 μm, preventing the short. Also, by using another squeegee like the productive pro-flow head, it would be possible to always use the same print direction, thus improving the wafer-to-wafer uniformity. The

pro-flow head has a paste reservoir installed in the print head, which is pushed down to the wafer by pressurized air. This means, that it is possible to print a wafer, then lift the head and lead it over the stencil back to the starting position, whereas with a normal squeegee the copper paste would remain in the end position of the last print and the squeegee would need to push it over the wafer again to reach the starting position.

One way to have the same starting position on every wafer with a standard squeegee would be to use two strokes per wafer, but tests have shown that this leads to an increased spreading of the paste: During the first stroke, some paste is entering the gap between the wafer and the stencil, which is then pressed further if the squeegee is pushed over the stencil a second time. The printing parameter "number of runs" was therefore set to "one" as a standard.

Figure 3.2b additionally shows another issue that is related to stencil printing: The back-side cleaning of the stencil is crucial for the printing results beginning with the second wafer. On the right side of the gate pad there are drops of paste that connect it to the source pad (additionally to the connection due to the printing direction). The wafer shown in that picture was the second wafer of the printing session and the stencil was cleaned three times with a dry paper roll before printing. The fact that it was not possible to print two wafers subsequently without creating short-cuts due to poor back-side cleaning highlights the importance of this issue for direct printing. In pattern pasting as well as in case of subsequent wet-chemical structuring this issue is not so pressing, because in case of pattern pasting, any contaminations will be removed during the photoresist removal step, and in case of wet-chemical etching the wafer would be printed with a full-face stencil, and a precise termination on the wafer edges is not so important.

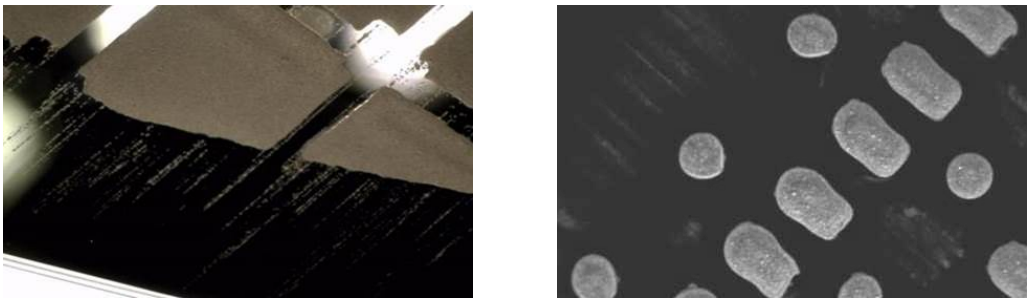
3.2.1.1 Stencil Back-Side Cleaning

The back-side cleaning issue was addressed in two ways: First, a number of different cleaning agents were compared. Second: Two types of stencil back-side coating were tested. The two coatings were the DEK Nano ProTec wipe-on coating and the polymeric DEK Nano Ultra coating. The wipe-on solution DEK Nano ProTec was applied manually to an electroformed nickel stencil using the pre-soaked tissues. The DEK Nano Ultra

coating is a spray-on polymeric coating that is applied by the manufacturer [104]. The evaluated under stencil cleaning agents were:

- ASM Assembly Systems GmbH & Co. KG
  - DEK Pro
  - DEK Pro XF
- Kolb Cleaning Technology GmbH
  - MultiEx GC
  - MultiEx SC
  - Wipe Ex SA 120
  - MultiEx NL-A

The cleaning trials were carried out by spraying the cleaning agent onto the dirty stencil and wiping with a tissue. As reference, isopropyl alcohol (IPA) was used, which is known to dissolve the pastes well, but cannot be used in the printing equipment due to its low flash-point. Additionally to the afore mentioned cleaning agents, a solution of IPA in 85% water was tested, having a flash point of above 30°C [105]. Unfortunately, none of the tested chemicals could dissolve the isoprenoide based pastes, all of them were just smearing the paste, distributing it over the stencil upon wiping with tissue, as two exemplary pictures in figure 3.3 show.



a) b)

FIGURE 3.3: Two exemplary pictures of wafers printed after BS cleaning with DEK Pro XF (a) Kolb MultiEx SC (b).

The wipe-on coating DEK Nano ProTec did not show any effect on the efficiency of back-side cleaning, but the sprayed DEK Nano Ultra coating showed a significant change in

the adhesion of the paste to the stencil, as can be seen on the photo in figure 3.4. The coated area is colored in red and does not show signs of paste residues, whereas the uncoated area shows clear signs of paste that has been removed from the apertures below.

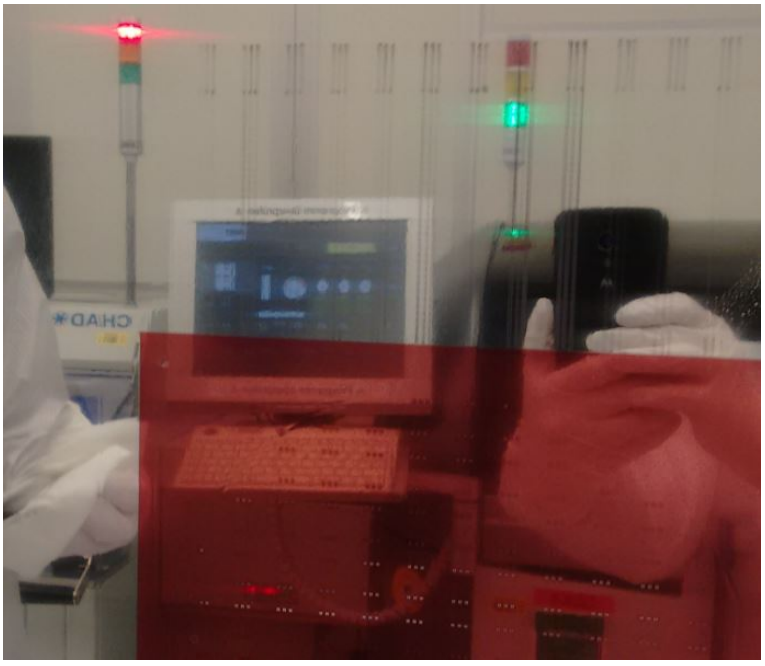


FIGURE 3.4: Photo of a stencil backside with coated (red) and not coated area.

Although the introduction of back-side coated stencils improved the cleaning properties, the search for a compatible cleaning agent is still necessary and could not be completed by the end of this thesis.

3.2.1.2 Printing Parameter Set

Before having a closer look on the influence of the printing parameters on the preciseness of the printed structures, it is important to clarify whether the physical parameters of the printed layers are affected by the deposition parameters. For example, an influence of the squeegee pressure on the porosity could be expected analogous to the densification of porous materials by pressure during sintering [106]. To investigate this question, a Design of Experiment (DoE) with the input parameters listed in table 3.2 was performed. The paste chosen for this trial was the back then latest batch of CP-PLS-291214-R1, QNA6449.

Parameter	Tested Values	No. of Points
Printing Speed	5, 23 and 40 mm/s	3
Printing Pressure	1, 5 and 9 kg	3
Board Thickness	3.0 and 3.4 mm	2
Number of runs	1 and 4	2
Snap-off Speed	0.1, 5 and 10 mm/s	3

TABLE 3.2: Table of printing parameters screened in DoE.

The set-up of the experiment as well as the analysis of the results was done with the software Cornerstone CEDA v3.4.6 using a D-optimal experimental design. This computer generated design gives the maximum information on the investigated system with the least possible amount of trials. A total of 25 wafers were printed according to this design, dried at standard conditions and cured with the standard furnace recipe for CP-PLS, depicted in 3.19. The wafers were analyzed according to the standard procedures explained in chapter 2. The Vickers hardness was measured on a Mitutoya HV testing machine. Uniformity was calculated from the layer thickness data according to formula 2.3. The surface roughness was determined on a Dektak XT mechanical profiler. The solid content was determined by weighing the wafer befoe and after printing as well as after drying. To give an overview on the range of measured physical data, the maximum and minimum results are given in table 3.3.

Parameter	Unit	Range
Paste deposited	g	1.77 - 14.71
Specific Resistivity	$\mu\Omega$cm	4.35 - 5.70
Layer Thickness	μm	12.44 - 90.63
Porosity	%	27.10 - 38.94
Solid Content	%	78.23 - 84.59
Surface roughness	μm	0.740 - 1.100
Uniformity	%	2.91 - 30.76
Vickers Hardness	HV	32.26 - 104.97

TABLE 3.3: Table of physical parameters investigated in DoE.

The analysis of the data by the statistical software showed an interdependence of the layer thickness on the printing speed and the squeegee pressure. The higher the speed and the lower the pressure, the more paste is deposited on the wafer. This happens because at low pressure, the squeegee is not pushed down hard enough to touch the stencil, but is rather floating on a layer of paste. The same thing is true for high printing speeds, whereas the higher the speed, the more pressure is required to strip the stencil clean of paste by the stencil. Typically, a printing pressure of 7kg is sufficient

when using a reasonable printing speed (5-10 mm/s) on the investigated paste, which had a viscosity of 33,100cP [69]. Of course, for pastes of higher viscosity this pressure can be expected to be higher, although this parameter was not included in this DoE.

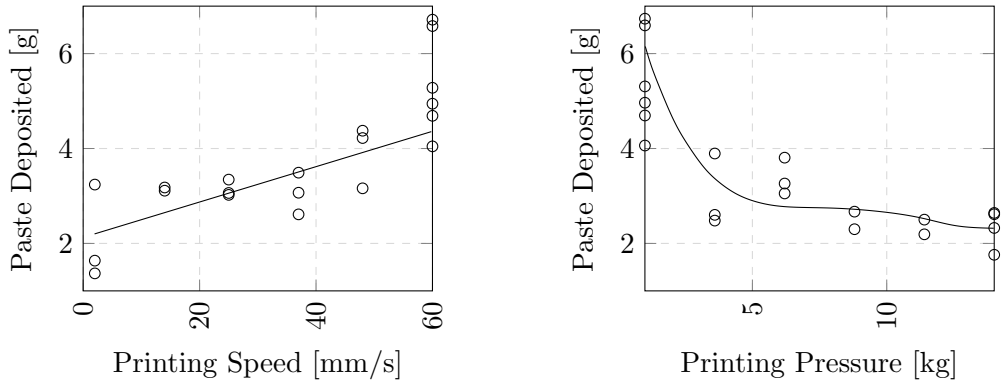


FIGURE 3.5: Influence of printing speed (a) and printing pressure (b) on the amount of paste deposited.

Figure 3.5 shows the influence of the printing pressure and the printing speed on the amount of paste deposited, which is another measure for the layer thickness achieved, since the paste has a uniform density on each wafer, which could be determined by comparing the porosity data of the analyzed pieces.

The layer thickness was the most distinct output parameter that could be influenced by the printer settings. An interdependence of the other output parameters on the input parameters could not be statistically proven. The large variations of those parameters seen in table 3.3 can be related to the varying layer thickness, as figure 3.6 shows. Those graphs show the actual average of the measurements (center line) as well as the upper and lower limit of probability (dashed lines) within the mathematical model.

According to figure 3.6a, the surface roughness measured in μm is indirectly proportional to the layer thickness, with a maximum surface roughness of around 1 μm at layers thinner than 20 μm. The specific resistivity is directly proportional to the layer thickness, which might be due to trapped in organics in the layers or insufficient curing. The Vickers hardness is constant in a range of 35-70 μm layer thickness, having a value of around 45 HV. Thicker layers are softer, probably due to insufficient curing of thick layers, whereas thinner layers seem to be harder, which could be due to the measuring tip pushing through the copper and either touching the interface, or compressing the porous copper until the porosity is vanished and values closer to bulk copper are measured. The

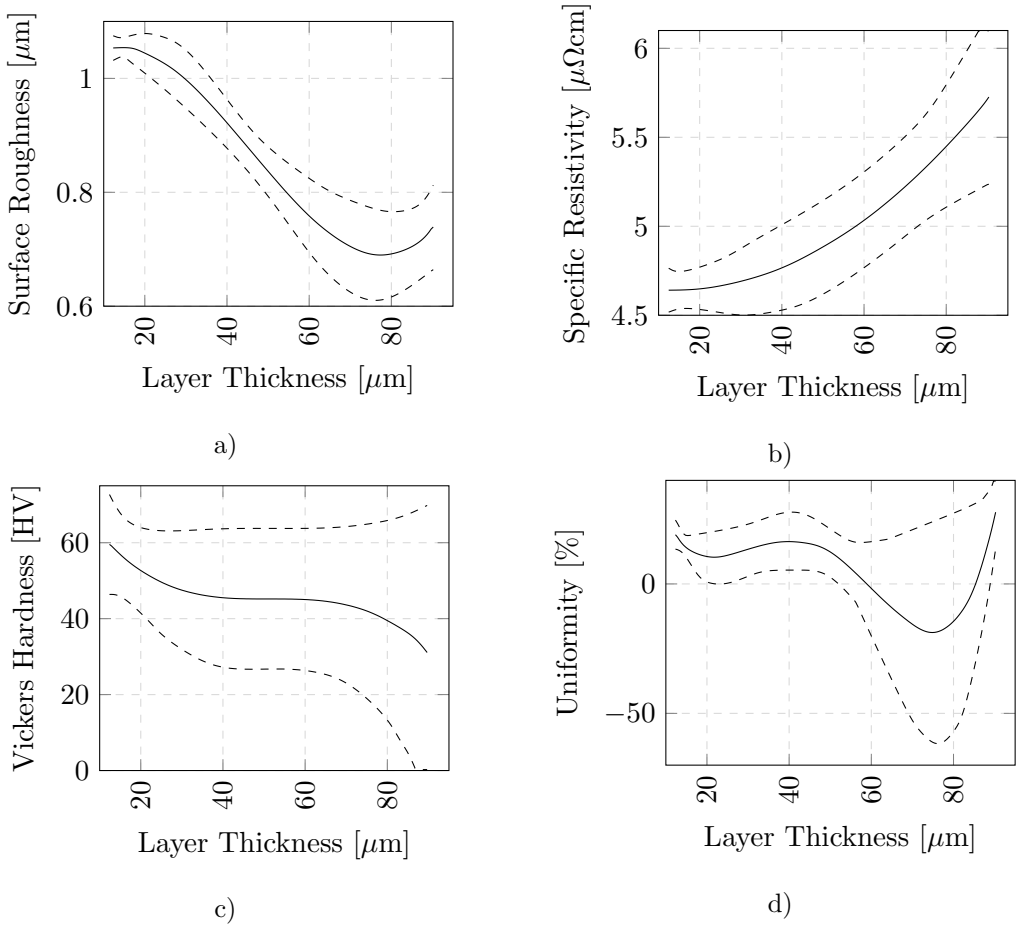


FIGURE 3.6: Variable prediction graphs of a) surface roughness, b) specific resistivity, c) Vickers hardness and d) uniformity in dependence on the layer thickness of the cured layer.

uniformity seems not to be influenced by the layer thickness, as the graph only shows some kind of statistical scattering.

The overall result of the DoE was that none of the printing parameters had any direct influence on a physical parameter of the cured layers other than the layer thickness, i.e. the amount of paste deposited. This is well in line with literature for solder paste printing [107], where also printing speed and pressure have been identified as main influences on the solder bump hight. Additionally, also the print gap (the distance between stencil and wafer) was mentioned as influential for the amount of paste deposited [108], which could not be confirmed for printed copper pastes. To deposit defined layers, a minimum squeegee pressure of 7 kg for printing the 33,100 cP paste CP-PLS, QNA6449 is necessary, as can be seen in figure 3.5b.

The structure preciseness of printed layers strongly depends on the amount of paste

deposited with bridging being the most common failure mode for too high paste pads [108]. Other crucial parameters especially for fine pitch applications are the stencil aperture design, wall quality and dimensional consistency [109]. From the side of printing parameters, for solder paste printing it is beneficial to use high rates of printing speed, separation speed, a large printing gap and separation distance as well as low squeegee pressure. These parameters are tuned towards economical aspects, since for solder paste printing the most important influence on the structural preciseness is the reflow process [109]. In the reflow furnace, the solder bumps are formed due to melting of the solder paste and subsequent surface minimization to form a solder ball. Printed copper pastes do not show this behavior, so the choice of the right printing parameters is more crucial there.

Due to the afore discussed issues of a poor back-side cleaning, no systematic evaluation of the influence of printing parameters on the structural preciseness in form of a DoE was performed. Also, for a DoE, a clear definition of quantifiable results would be required, which is difficult to do for a vague term like structural preciseness. E.g., the amount of paste spreading compared to the aperture size seems like a valuable parameter, but is actually most dependent on the viscosity of the paste. Low viscosity pastes spread more than high viscosity pastes, as has been shown by diluting of a very viscous paste with the proper solvent [79]. For high viscous pastes, the most critical failure mode is bridging, which can effectively be reduced by lowering the separation speed to below $1\,\mathrm{mm\cdot sec^{-1}}$. The printing speed influences the filling of apertures especially at high printing speeds, which can already be seen on full-face wafers in 3.5a. Here, the phenomenon starts with a printing speed greater than $40\,\mathrm{mm\cdot sec^{-1}}$, but the exact value naturally depends on the aperture size, and therefore cannot be generalized. The printing pressure needs to be at least 7 kg for CP-PLS, QNA6449 as mentioned before, and cannot be raised much further as the maximum pressure the equipment can effectively handle is 10 kg. The separation distance, which is typically 2-3 mm was not observed to have any influence on the structural preciseness, and an increase of the printing gap typically reduced the print quality, which is why wafers were typically printed in contact mode.

As said before, those results were obtained by experience and not from a systematic approach. First, a proper and reliable stencil back-side cleaning procedure must be found in order to eliminate the influence of paste residues on the print quality. Then, since the optimal parameter set strongly depends on the aperture design, a target technology

needs to be defined for the optimization. As the technology integration of printed copper did not proceed so far by present day, the optimization was not within the scope of this thesis.

3.2.2 Wet-Chemical Etching

Wet-chemical etching of copper is a standard process in semiconductor industry. The main standard technique of copper deposition is plasma enhanced physical vapor deposition (PEPVD) or also called sputtering. Sputtering is a full face technique, which means that the whole wafer will be covered with a uniform layer of the sputtered material, which then in a subsequent process step needs to be structured by removing the undesired areas. For aluminum, this can be done either wet-chemically or with a plasma process, but for copper the only suitable way is wet-chemical etching. Dry etching processes for copper with argon plasma containing chlorine exist [110], but the end point detection is difficult and the process itself is challenging and not very stable [111]. The chemistry used for wet-chemical etching of copper consists of two main components: one oxidizing agent that oxidizes the copper to copper(I) or copper(II), and an etching agent that removes the copper oxide from the surface. The concentration of those components must provide a constant removal rate of material, that is high enough to be economical, but low enough to be controllable.

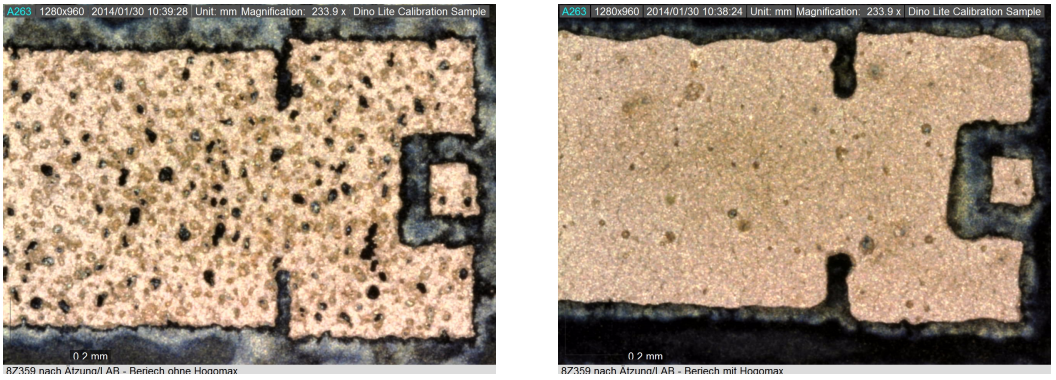
Two types of copper etching solutions were used for the etching trials. Hydrogen peroxide is used as an oxidant in one of them, nitric acid in the other. As etchant of the generated copper oxide, phosphoric acid is used in both cases. The composition of the two standard copper etching solutions used in this work can be found in table 3.4. It is apparent that the Cu-Seed etching solution is a much “softer” etchant than the Alu-HAC, as it contains mostly water. The Alu-HAC is basically an aluminum etching solution that has been diluted with acetic acid in the ratio 55:45. The acetic acid dilutes the aluminum etching solution to reduce its etching rate, thus making the process easier to control while keeping the pH value low. If water would be used to dilute the etching solution, the adhesion of the commonly used etching photoresist IX-335 would be negatively affected, as internal studies performed by P. Fischer have shown.

Purpose of Component	Cu-Seed-Etch	Alu-HAC
Oxidation	0.8 wt% H_2O_2	1.38 wt% HNO_3
Oxide removal	2 wt% H_3PO_4	37.13 wt% H_3PO_4
Diluent	-	45 wt% CH_3COOH
Rest	97.2 wt% H_2O	16,5 wt% H_2O

TABLE 3.4: Composition of the two copper etching solutions used within this thesis.

3.2.2.1 Conventional Spin-on Photoresist

Before etching, the areas that shall remain covered with copper need to be covered with photoresist. A standard commercial spin-on photoresist for this purpose is the IX-335-H-60cP, which is a positive resist with a viscosity of 60 cP. This photoresist can be used to etch both electroplated and sputtered copper layers, but is not suitable for printed porous copper, as with its low viscosity it can easily rinse into the copper network. The problems emerging from this issue can be seen in figure 3.7a, which shows microscopic pictures of wet-chemically etched porous copper layers through a standard copper etching photoresist IX-335. Due to the high surface roughness and the pores, the coverage of the copper layer with photoresist is insufficient, thus exposing parts of the layer to the etching solution and resulting in a "swiss-cheese" like structure. This effect can be reduced but not completely avoided by filling the pores with a water-soluble poly-ethylene glycol polymer (HogoMax^{TM}), as shown in figure 3.7b.

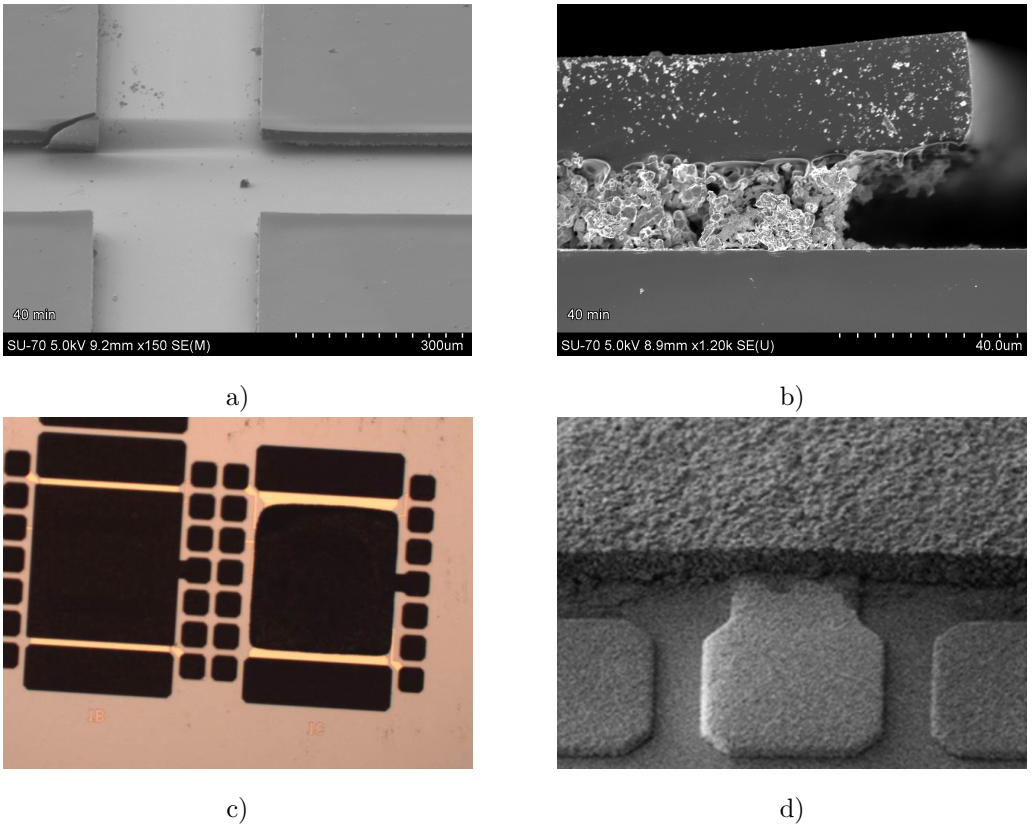


a) b)

FIGURE 3.7: Porous copper wet-chemically etched through a standard resist mask without (a) and with (b) HogoMax filling.

3.2.2.2 Foil-Resist

The problem of photoresist rinsing into the open porous network can be avoided by using a so called "foil resist" instead of a spin-on photoresist, as has been shown on porous copper layers deposited by the plasma-dust method [112]. A foil resist consists of an adhesive layer that connects the substrate to a photosensitive foil that can be structured by lithography. With this method, the issue of insufficient coverage of rough porous layers can be successfully averted.



a) b)

c) d)

FIGURE 3.8: Porous copper wet-chemically etched through a foil resist mask (a) in top view, (b) in cross section view. Poly-heater structure of the same material etched through a foil resist mask after photoresist removal (c) and SEM picture of the same structure (d).

Foil resists are rather exotic materials, which are not used for standard FEOL or BEOL proceses. They were therefore used for trials, but not as a standard technique for copper paste structuring.

3.2.2.3 Hot-Melt Mask

Another alternative way to deposit an etching mask for wet-chemical etching of porous metals would be printing of a hot-melt system by an ink-jet printer. In comparison to traditional methods in semiconductor industry, ink-jet printing offers the possibility to direct print masks without the need for expensive lithography including deposition, exposure and development. Instead, the mask is directly printed only to the areas where it is required, which saves material and additional process steps. A schematic comparison of the two processes is shown in figure 3.9. The conventional method includes the deposition of the photoresist by spin-coating, followed by selective exposure of defined regions to a radiation source (typically UV) through a mask or a reticle[2]. Depending on the chemical composition of the photoresist, the monomers in the exposed areas are either cross-linking (negative photoresist) or the existing polymer chains are being broken apart (positive photoresist). The initiated chemical reaction is then brought to completion during the post-exposure bake in a furnace. After this, the hardened areas of the photoresist are then stable enough (or the destroyed regions are weak enough, respectively) to be developed in a chemical bath, where the undesired areas are washed away. All those process steps can be skipped in case of an ink-jet printed resist mask, since it was already deposited only in the desired areas.

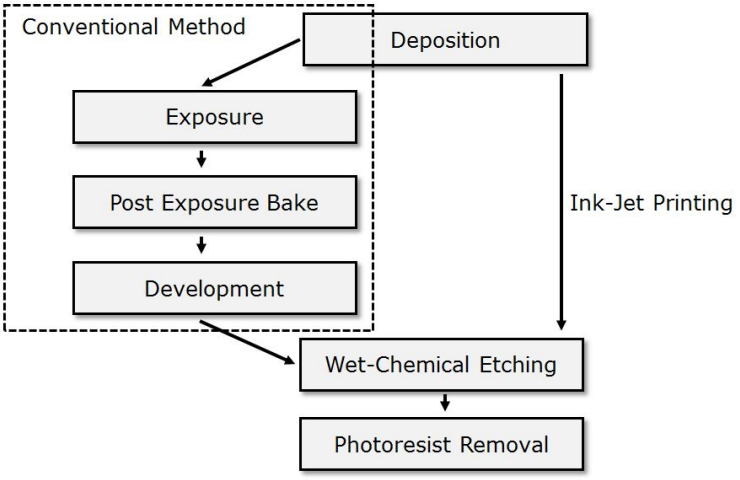


FIGURE 3.9: Schematic process flow of a hot-melt printed resist mask in comparison to a traditional lithographic mask.

[2]A mask is a glass plate with chromium metal deposited on defined areas. It is placed above the wafer during exposure with a radiation source, with the radiation passing through the glass and being reflected by the chromium areas. While the size of a mask is always larger than the wafer diameter, a reticle is a small mask which is moved stepwise over the wafer with alternating movement and exposure steps.

For a better understanding of this section, the working principle of an ink-jet printer will be explained in short: Patterns of ink are created by the deposition of small droplets generated within a print head. The print head consists of one ore more small channels in which the ink is transported to the outside through the so called nozzle. Typically, modern print heads contain up to several hundred nozzles. The distance between two nozzles as well as the angle of the print head towards the printing direction determines the minimum resolution that can be printed. The drop is either generated by inducing a pulse in the nozzle (so called "drop-on-demand" print heads) or it is generated constantly and the generated drops are deflected either onto the substrate or back into the ink reservoir (continuous ink-jet printing). For drop-on-demand ink-jet printing, the most common way to generate the pulse is the piezzo-electric method, which is also used in the print heads used for the trials described within this section [113].

The print-head is moved over the wafer and the ink droplets are selectively deposited as defined within the print file. The ink is stored in a reservoir above the print head and is held back by a negative pressure of around -20 mbar compared to the air pressure. When printing hot-melt inks, special print heads with heatable ink reservoirs need to be used. Here, the ink is generated from the solid state within the ink reservoir and is pumped through the heated print head at a temperature above its melting point. The substrate is held at a lower temperature than the melting point of the ink, which is why the droplet solidifies very fast upon hitting the substrate.

Since the ink is immobilized by the solidification, it cannot enter an open porous network like printed copper layers. The data that will be shown in this section was acquired by Florian Bernsteiner [114] in the course of his master's thesis.

There are several hot-melt waxes on the market, that were designed to be used as masks for wet-chemical etching of metals. The most suitable for the etching of printed copper was the ink EMD9700 from SunChemicals as it could generate the smallest drops of all the tested inks, had good adhesion to the printed copper substrate during the etching process and could be removed completely during the subsequent resist strip. This ink consists of a proprietary wax and a resin, has a melting point of 70-80 °C and a viscosity of 8-12cPs within the jetting temperature range of 85-105 °C. [115]

Figure 3.10 shows the results of Bernsteiner's [114] trials: 3.10a shows the printed hot-melt structures on a approx. 15 μm thick layer of copper paste (CP-PLS-291214R1,

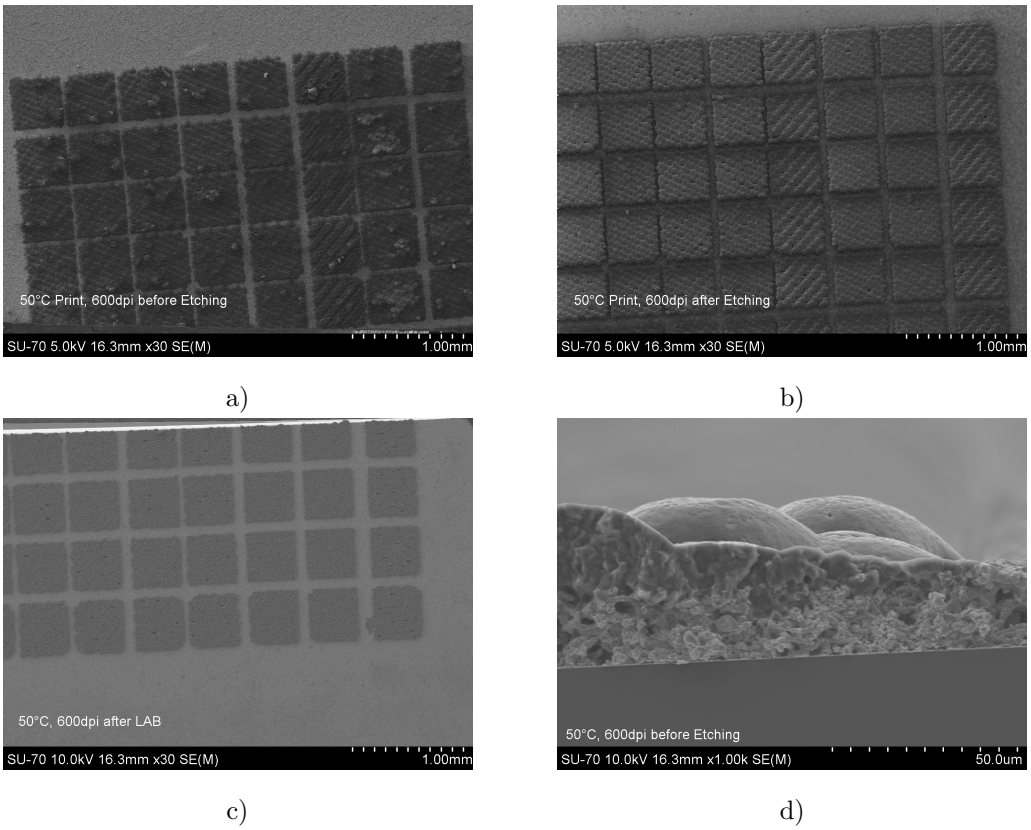


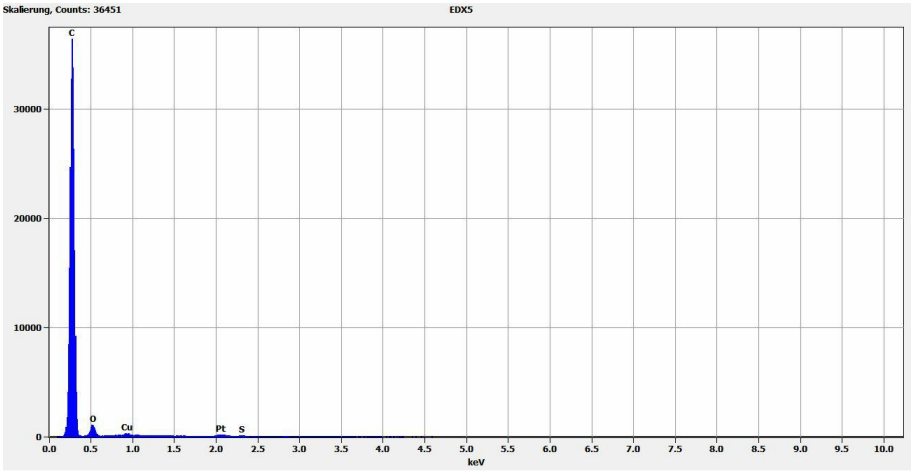
FIGURE 3.10: Porous copper wet-chemically etched through a hot-melt resist mask (a) before etching, (b) after etching, (c) after photoresist removal and (d) before etching in cross-section.

QNA6449). The deposition process is not yet very uniform and suffers from peculiarities that are characteristic for ink-jet printing, in which the achievable resolution strongly depends on the dot size of the printed material on the respective surface. Two important observations show the success of this feasibility study: First, the etched pads after photoresist removal (Fig. 3.10b) do not show the "swiss cheese" like structures as the conventionally etched samples (Fig. 3.7a). Second, the resist does not penetrate into the porous network (Fig. 3.10d) as can also be confirmed by EDX measurements.

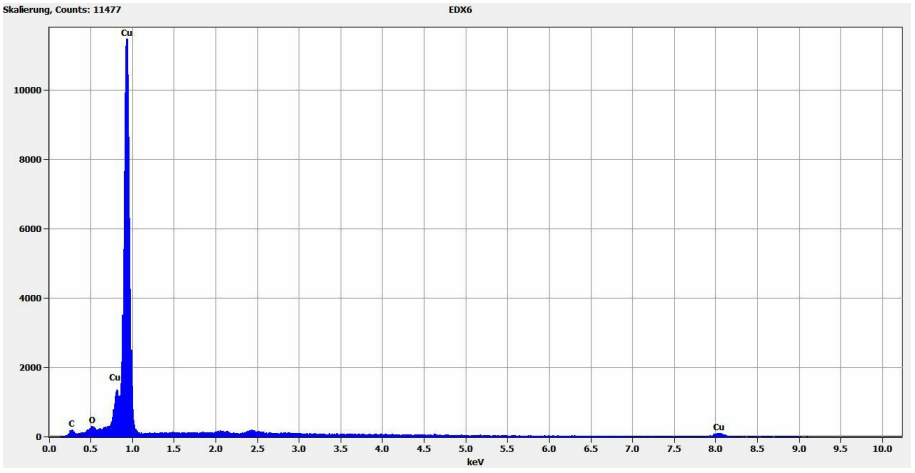
The EDX spectra that are shown in Figure 3.11 clearly indicate that all the organic material was removed during the photoresist strip, as the carbon peak in spectrum *c* is not more intense than in spectrum *b*.

3.2.2.4 Wet-Chemical Etching: Conclusions

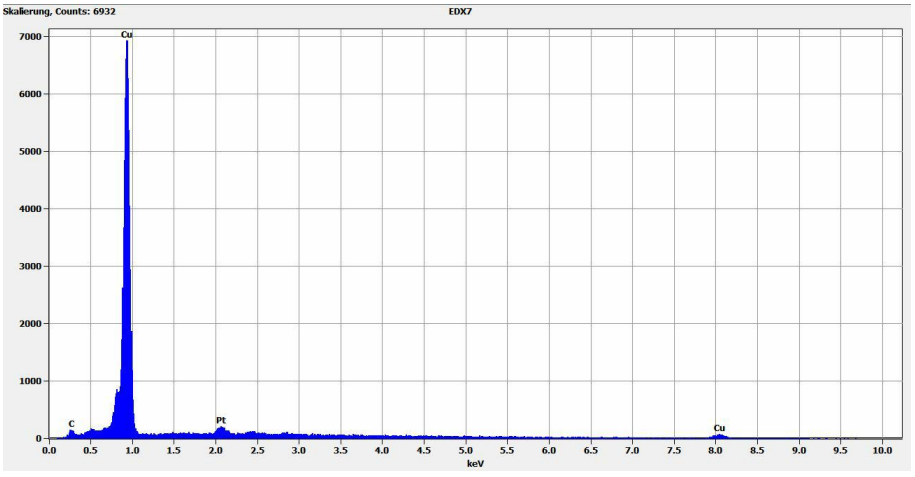
Although it could be shown that wet-chemical etching is a feasible way to structure porous copper, there are several draw-backs that limit its application. First, it is a



a)



b)



c)

FIGURE 3.11: EDX spectra of (a) hot-melt ink on porous copper, (b) porous copper before hot-melt deposition and (c) porous copper after hot-melt deposition, etching and photoresist removal.

subtractive process, which means that depending on the intended coverage of the wafer, a lot of material is wasted, which is a cost driver. Also, in case of the foil-resist, the process steps themselves are expensive since they include lithographic structuring, which consists of deposition, exposure, development and after etching photoresist removal. The deposition of the foil is a non-standard process, since this type of foil is usually not used in the back end of line (BEOL), whereas the deposition of the ink-jet hotmelt ink is still a process under development. The hot-melt process can be regarded as a method with enormous potential, but there are still open questions that need to be answered before it could be used within a productive workflow. The financial issues would still be acceptable if in the end the customer would be willing to pay for it, but the big technological draw back is the isotropic nature of the wet-chemical structuring process:

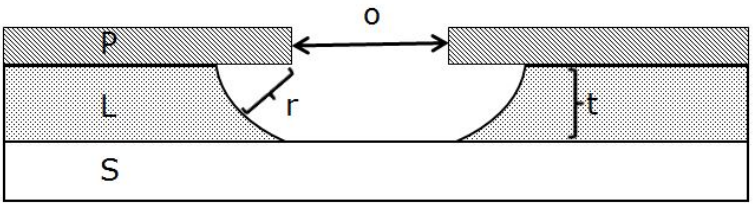


FIGURE 3.12: Illustration of the interdependence of layer thickness and achievable aspect ratio in isotropic etching.

As illustrated in Figure 3.12, the aspect ratio of an isotropic etch process is limited. A layer L with a layer thickness t is structured with a photoresist layer P through an opening o. The etching solution etches isotropically until it reaches the substrate S, which is not etched by the solution. The radius of the etch-front r cannot be smaller than the layer thickness t in order to reach the substrate S. Hence, no gaps that are smaller than two times the layer thickness can be etched isotropically. The overall goal of this thesis is to develop a deposition method for very thick (e.g. larger than 40 μm) copper layers, which in a back-side application would result in a sawing street width of around 80 μm, already too much for most MOSFET technologies, as shown in table 3.1.

Summarizing these findings it can be stated, that it is possible to structure porous materials with wet-chemical etching techniques if specialized deposition methods for the etch mask are used, but the strong economical and technological downsides of this method require the development of complementing techniques.

3.2.3 Pattern Pasting

The term pattern pasting was coined by Infineon Engineer Manfred Schneegans and is an alteration of the term pattern plating. Pattern plating refers to the structured deposition of material (typically copper) by electrochemical deposition. The structuring is done by covering a seed layer of a substrate partially with a lithographically structured photoresist. After an electrochemical copper deposition in the open areas of the wafer, the photoresist is then removed and the seed layer in the previously covered areas is removed by wet-chemical etching. With this technique, thick metal layers (up to 20 μm are common) can be produced with very fine gaps of below 40 μm between the pads. Another typical application for this technique is the plating of interconnections for VLSI[3] devices, where copper pillars of 50 μm diameter and more than 100 μm of height are electroplated [116].

This process flow can be adapted for the use with copper pastes: The seed layer can be structured already before the photoresist deposition, which is beneficial because the surface of the pads will then not be attacked by the etching solution in a later stage. The same photoresist as in the electrochemical deposition can be used, which is typically a THB resist, e.g. THB151 with a layer thickness of 45-50 μm. The printing is done after the photolithographic structuring of the resist by printing through a structured stencil selectively onto the open pads. The openings in the stencil have to be smaller than the openings in the photoresist (overlap) to avoid overprinting onto the resist due to misalignment and rinsing of the paste. The optimal reduction of the stencil opening size to the pad size is dependent on the viscosity of the paste and is typically between 25 and 100 μm. The minimum overlap is defined by the alignment precision of the printing, which in case of the DEK Horizon i02 is 25 μm.

Once the paste is deposited on the wafer, the standard drying procedure is used to remove the solvents from the paste and solidify it. Subsequently, a pre-curing step is necessary to sinter the particles together in order to stabilize them during the following photoresist removal step. Due to its limited thermal budget, possible thermal degradation of the photoresist is limiting the maximum temperature in this process step. If this temperature is exceeded, the subsequent photoresist strip cannot be performed successfully anymore and residues of the photoresist remain on the wafer. On the other hand, if

[3] Very Large Scale Integration, i.e. highly integrated logic devices.

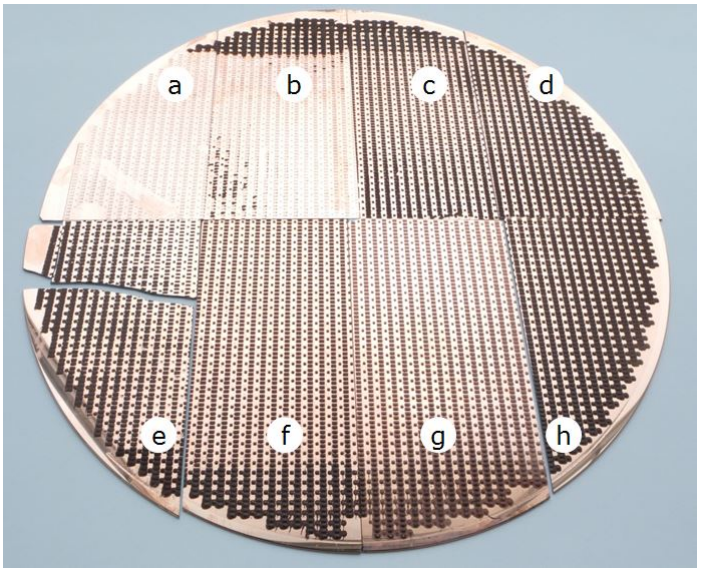


FIGURE 3.13: 200 mm Wafer with paste CP-003 after cleaving, furnace treatment and photoresist strip with EKC162. Furnace treatment: a) 200 °C 15min N2, b) 200 °C 60min N2, c) 250 °C 15min N2, d) 250 °C, 60min N2, e) 200 °C 15min FA, f) 250 °C 15min FA, g) 400 °C 15min FA, h) no furnace and no photoresist strip.

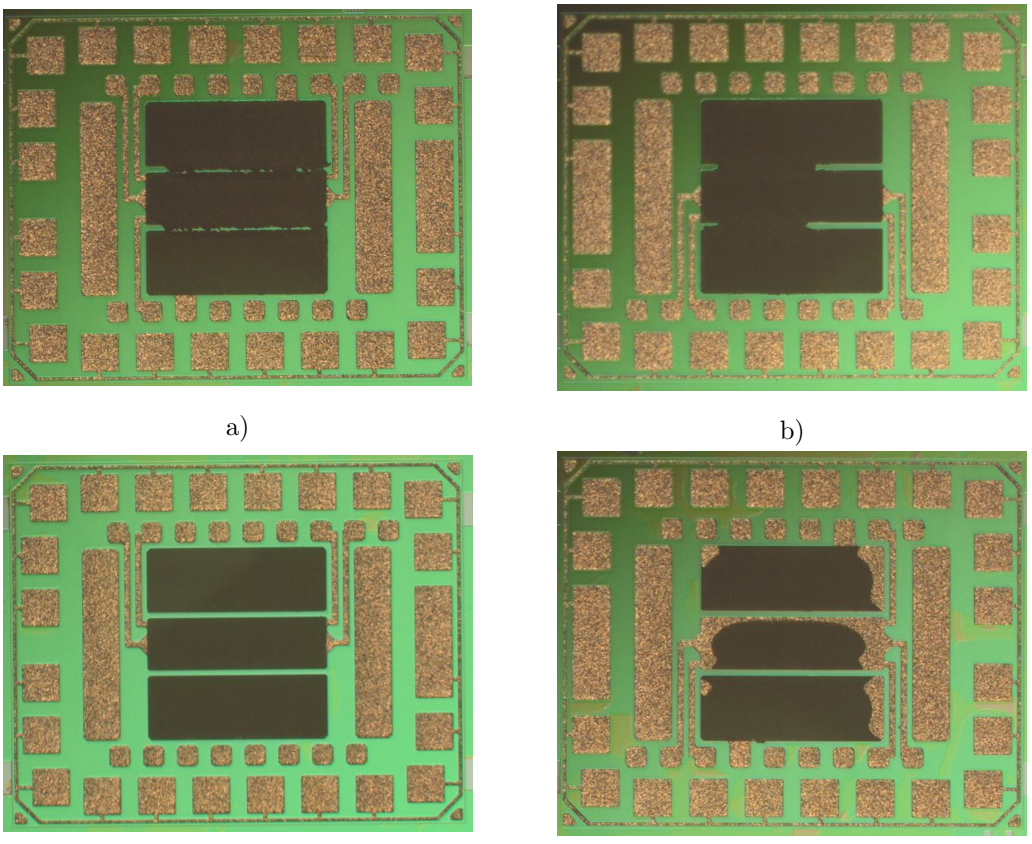
the temperature is too low to sinter the copper particles together, the paste is removed during the wet-chemical stripping procedure as exemplary shown in figure 3.13.

There was no feasible process window for sintering the old ethylene glycol based pastes like CP-003 to a sufficient extend without damaging the photoresist. With the availability of low-temperature sintering isoprenoide based copper pastes, pattern pasting could be established as a reliable method to produce well defined, narrow gaps between printed copper pads. To evaluate the possibilities given by this method, a polyheater pad design with very narrow gap sizes of 40 μm between long, thin pads (290x1020 μm) was chosen. The wafers were coated with a 50 μm thick layer of THB151 and exposed and developed by F. Haering in Regensburg. Printing was done with a multi-shared stencil (i.e. a stencil with different pad sizes to evaluate the optimal overlap) with the paste CP-PLS-291014-R1, QNA6449.

The printing parameters shown in table 3.5 were the best fitting parameters that could be found with a limited amount of wafers. Parameters not listed in the table were found to be insignificant for the output when varied in a rational range. The photoresist was stripped in TechniStrip P1331 at 45 °C for 20mins, followed by washing in deionized water. Exemplary microscopic pictures of structures on the wafer after photoresist strip are shown in figure 3.14. The structures displayed in 3.14a and b were printed through

Parameter	Value	Unit	Comment
Print Pressure	9	kg	influences the amount of paste deposited
Print Speed	20	$mm \cdot s^{-1}$	influences the amount of paste deposited
Separation Speed	0.1	$mm \cdot s^{-1}$	prevents bridging between the pads
Alignment Offset	+0.1 / -0.15	mm	corrects offset of marks to apertures

TABLE 3.5: Best printing parameters found for pattern pasting on polyheater wafers with 40 μm print gap.



a) b) c) d)

FIGURE 3.14: Copper paste printed in polyheater structures with different stencil overlap (a) 50 μm, (b) 100 μm, (c) 150 μm and (d) 200 μm.

apertures with too low overlap, resulting in bridges between the pads. Structure 3.14d is only partially filled, whereas structure 3.14c is filled nicely with no bridges.

With the thermally sensitive photoresist removed, the wafer could then be cured at 400 °C for 3h with the usual furnace program. Figure 3.15 shows the effect of the curing on the lateral dimensions of the pads printed with 150 μm overlap. In Figure 3.15b it is evident that the paste is shrinking laterally by 8 μm upon curing, thus withdrawing from

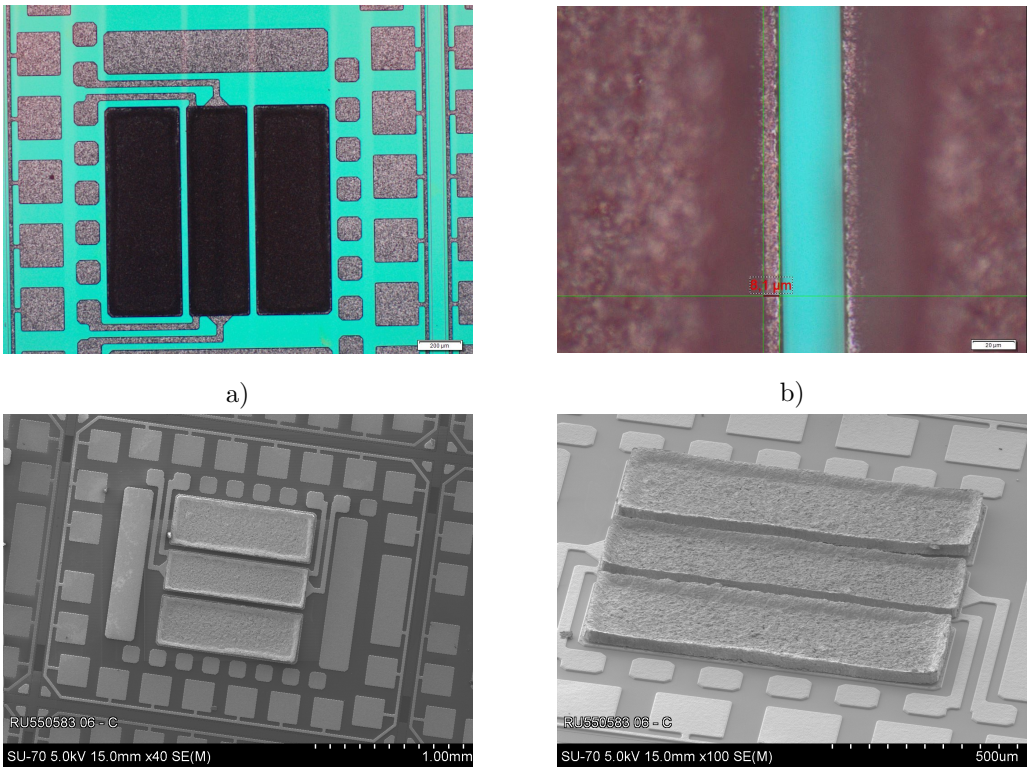


FIGURE 3.15: Copper paste printed with 150 μm overlap in polyheater Structures after final curing (a) microscope, 5x, (b) microscope, 50x, (c) SEM, 40x in top view and (d) SEM, 100x in tilted view.

the ECD copper below. In Figure 3.15d it can be seen that this shrinkage is accompanied by a partial lifting off the edges of the printed copper pads. This is undesired and needs to be addressed in the future. It is yet unclear whether the lifting occurs during the furnace treatment or before, as there were no SEM pictures acquired before the curing. The cause of this effect is likely to be connected to the photoresist strip, since no such behavior of the paste has yet been observed on e.g. IGBT pads that are structured by direct printing.

Despite the observed issues, it could be shown that pattern pasting is an elegant way to structure fine gaps between pads of printed copper, that might enable the use of printed copper as a backside application.

3.3 Sintering

One of the first big commercial applications of printed metal pastes were PV (photovoltaic) solar cells: In spite of the higher material cost, printed silver pastes replaced electrodeposited copper electrodes due to reduced process costs compared to the expensive electroplating and etching steps needed for copper metalization [117]. Silver pastes were fired at temperatures between 600 °C [118] and 850 °C [119] to remove organic content and sinter the particles together. For other applications of printed electronics such high firing temperatures are not feasible, e.g. when printing on polymer or paper substrates. For such substrate materials, metalization was first enabled by the development of silver nano particle inks that could be sintered at 120-250 °C [120]. Also alternative sintering methods like the Novacentrix PulseForge Technique contributed to enabling the use of silver nano particle inks on temperature sensitive substrates. Due to the high material cost of silver efforts were made to replace it with copper, which proved to be difficult because copper is so prone to oxidation. Especially copper nano particles due to their high surface area can be dangerous to handle in ambient air, which means that special coatings are required to protect their surface. One of the first approaches to solve this issue was to coat the copper nano particles with silver [121], [120], but soon also organic coatings were developed [122]. These organic coatings need to be removed during the sintering process in order to enable a solid-state contact between the particles. This is typically done by providing a high energy impulse like a Xenon flash lamp (e.g. in the NovaCentrix PulseForge® system), high power IR lamps [123] or an IR laser [124].

The 808 nm infrared laser LAPS-60 from Intrinsiq Materials Ltd. was evaluated for the application of copper paste on semiconductor wafers, but due to the high thermal conductivity of the silicon substrate, most of the heat was distributed within the substrate and did not lead to a satisfying sintering of the copper particles, affecting just the top layer of the paste [47]. Hence, a furnace process with use of formic acid vapor (FAV) was developed and introduced [79]. The first furnace recipe included a fast ramp phase up to 400 °C in an IR-lamp heated furnace, followed by a short annealing phase of 15-60 min and a fast cooling phase. With the IGBT application in mind, the temperature of 400 °C was set as maximum due to the fact that in front side applicationss. As the furnace process is the production step in which the paste is being turned conductive, it is natural to assume that by changes to this process the material properties of the copper

layers can be altered. In depth understanding of the role of different phases within the furnace program was acquired by B. Eichinger, who was writing a Master's thesis on this topic [62].

3.3.1 Equipment

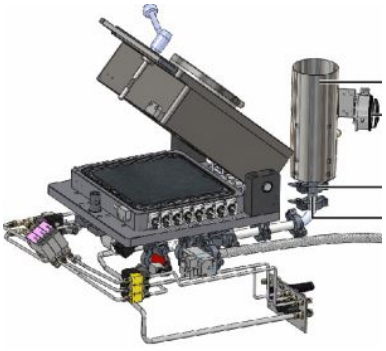
Before going into details on the process, the used equipment and its capabilities shall be briefly discussed. Curing was carried out on a SRO700 vacuum furnace from ATV Technologie GmbH. The furnace shown in figure 3.16 is a small desk tool for development and experiment purposes. Its chamber can hold a single 200 mm wafer on a graphite hotplate, which is heated from below by eight IR lamps organized in two heater zones (figure 3.16c). Each IR lamp delivers a heating output of 750 W, summing up to a total of 6000 W. With this high power, the furnace is able to ramp up from room temperature to 400 °C within around two minutes, achieving a ramp rate of 150 °C$\cdot$ min^{-1}.

The gas inlet, which is located over and in front of the hotplate, can be fed by three different gas lines that are regulated by separate mass flow controllers. Over two of the lines (MVR1 and MVR2), nitrogen with different gas flow settings can be purged into the chamber, whereas the third one (MVR3) delivers nitrogen that has been guided through a formic acid bubbler, thus delivering FAV. The gas streams are set to 20 l$\cdot$min^{-1} (MVR1), 8 l$\cdot$min^{-1} (MVR2) and, depending on the furnace recipe, 1-9 l$\cdot$min^{-1} (MRV3). Before Eichinger evaluated the influence of the FAV flow on the material properties of the layers, the MVR3 flow was set to 3 l$\cdot$min^{-1} as standard setting, delivering 0.2 g$\cdot$min^{-1} formic acid as predefined by the manufacturer.

The chamber can be evacuated by a vacuum pump that is capable of reducing the pressure in the chamber down to around 2 mbar within 2 mins. The evacuation of the chamber with a subsequent nitrogen purge is a standard step in order to remove oxygen that might form an explosive mixture in combination with the formic acid. The use of other chemicals than formic acid is not approved by the manufacturer. For example, it would have been interesting to study the influence of alcohols on the sintering behavior of copper nanoparticles contained within the pastes, as suggested by literature. [125].

Cooling of the furnace chamber walls is established over an external ethylene glycol cooling cycle, whereas the inside of the chamber is cooled by an additional nitrogen inlet

a)



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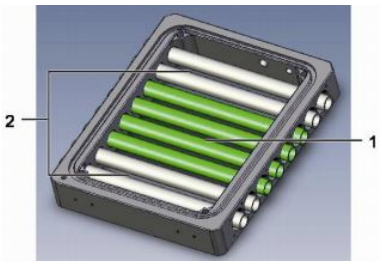


c)

FIGURE 3.16: ATV SRO700 furnace with attached computer (a), schematic of the chamber with hotplate, gas inlets and IR lamps (b) and schematic depicting the two heater zones 1 and 2 (c).

under the hotplate, addressed in the software as "max cooling" functionality. This functionality is typically activated at the end of each recipe, and is automatically activated if the temperature in the chamber is more than 5 °C over the predefined temperature. Such an distinct delta from the set temperature can occur when fast heating is done in vacuum or when a high cooling rate is entered in the software without activating the "max cooling" function in the recipe. Otherwise, the furnace is able to keep the temperature stable at ±0.2 °C. All technical data and schematics have been taken from the manual for the equipment [126].

3.3.2 Removal of Organic Components

After printing, the majority of organic components is removed from the pastes by a simple drying process at 60 °C for 30 mins under nitrogen, as recommended by the supplier. The drying process removes the organic solvents, thus transforming the paste into solid, brown layers that have only weak adhesion to the wafer surface and are not conductive. The copper particles are attached to each other and to the wafer surface by the binder that is still present after drying. Therefore, the wafers can be stored and transported without the immanent danger of mechanical damage to the layer, which is present when the wafers are handled with wet paste. This is important, since as previously mentioned the curing furnace is located outside of the cleanroom. The removal of the binder system is then performed during the curing recipe at temperatures above 200 °C, which can be detected by a mass reduction in the TGA as well as in form of an exothermic peak in the cDTA. Figure 3.17 shows the sintering of CP-PLS-291014-R1 under Nitrogen.

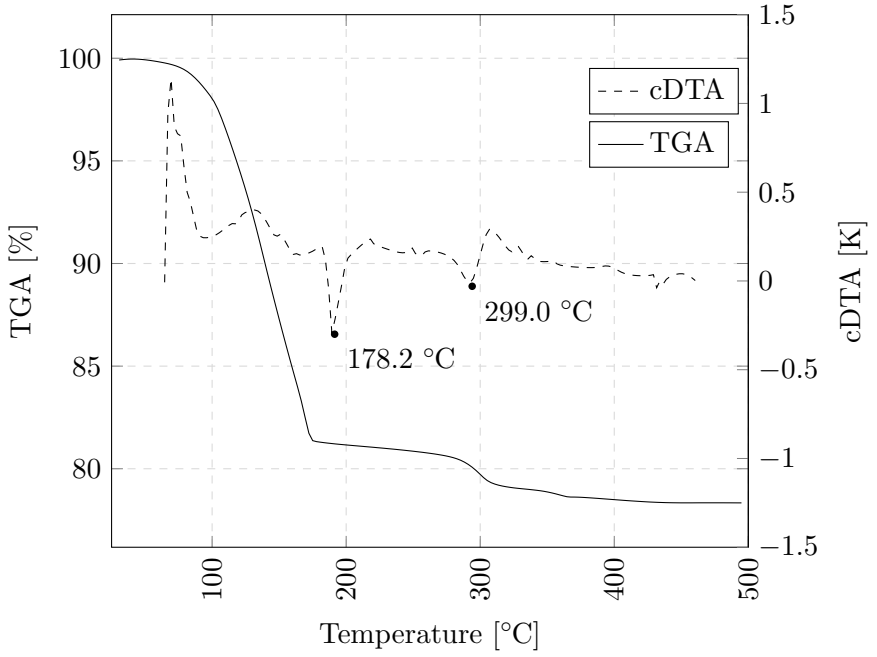


Figure 3.17: TGA/DSC data on the paste CP-PLS-291014-R1, QNA6449 acquired by FA Regensburg

Within this thermal treatment first the solvent is evaporated at temperatures below 180 °C, accounting for a mass loss of 18.5%. At 299 °C the binder is decomposed, which can be detected by a mass reduction in the TGA of further 2.8% as well as in form of an exothermic peak in the cDTA. The exothermic peak in the cDTA at 178.2 °C, which

is not accompanied by a mass reduction, indicates the sintering of the copper nano particles. This process is exothermic, since the particles are reaching an energetically favorable state by reducing their surface area [127]. The presented data was acquired under nitrogen atmosphere and therefore does not resemble the paste curing process as it will be described in the next section.

As it was discovered in previous works [79], [81], for a successful curing process formic acid is not just required, also the temperature at which the formic acid is inserted into the furnace chamber is crucial for the curing result. If the gas is applied to the wafer at 400 °C, the copper layer remains brown and the resistivity does not reach the expected low values [79]. Subsequent reduction with any standard furnace process does not lead to a satisfying result either. The most probable reason for this effect is a polymerization or metathesis reaction within the particle coating or binder system, that leaves back organic residues that hinder the metal-metal contact of the copper particles, as already discussed in more detail in section 2.3.1.2. Schwab investigated this effect by heating up pieces of uncured paste to different temperatures under nitrogen before curing them under formic acid, and found the temperature at which this irreversible transition is happening in the paste CP-131113-R1 to be at around 250 °C [81]. Further investigations on the paste CP-003 (figure 3.21), which uses the same binder and solvent system as CP-131113-R1, showed that this is also the temperature at which the sintering is initiated. This leads to the conclusion that if the organic particle coating is not removed within the critical phase of particle sintering, a chemical reaction is changing its material properties in a way that it can no longer be removed in a later stage. According to Intrinsiq Materials, a suitable particle coating would be a long-chain fatty acid, e.g. oleic acid [128]. Oleic acid could protect copper nano particles by forming a monolayer of copper oleate on their surface [129], [130]. This monolayer could be removed by protonation by another acid, e.g formic acid. If not removed, it could decompose, e.g. in a metathesis reaction.

Oleic acid is just one example for a possible organic coating suitable for copper nanoparticles, its presence could not be proven in the used copper pastes. Analyses that aimed towards identifying the particle coating by TDS-MS, TDS-GC-MS, IR- and Raman spectroscopy as well as TOF-SIMS failed due to the comparably small amount of coating bound to the copper surface embedded in a large amount of other organic substances.

In section 2.3.2.1 of chapter 2 it could be shown that even after 3 h of annealing printed

copper at 400 °C there is still remaining organic material in the layers. Due to their low boiling points the solvents cannot be responsible for the remaining carbon and hydrocarbon signal in TOF-SIMS, which is therefore more likely caused by either binder or coating residues.

3.3.3 Optimization of the Curing Process Parameters

The first furnace process for curing copper pastes on the ATV SRO-700 furnace depicted in figure 3.18 was a simple first approach. Its basic design was chosen to ensure a high throughput of wafers on this single wafer tool. The comparably short process time of around 30 minutes per wafer enabled a large number of quick trials for which the electrical conductivity was not important, e.g. etching, spin-coating, soldering, overprinting[4] and so on.

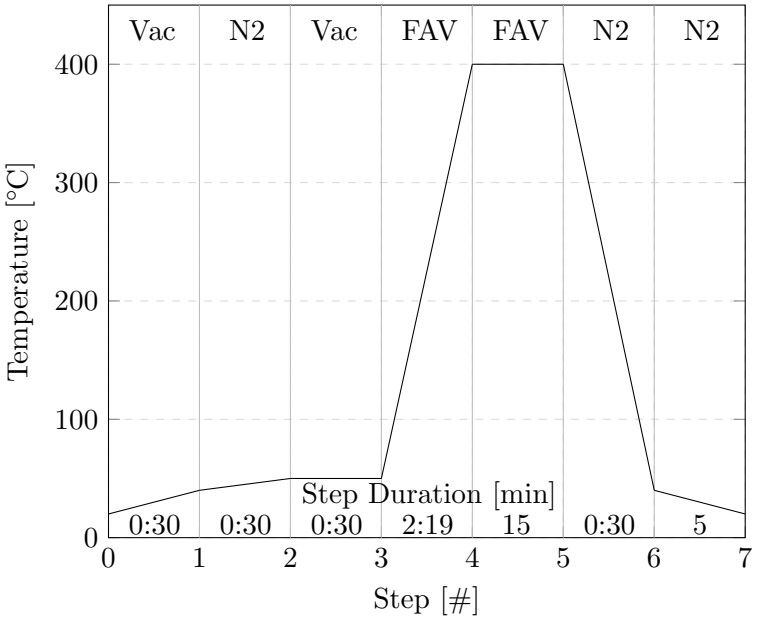


FIGURE 3.18: Early furnace recipe for CP-003 curing including a fast ramp to 400 °C and 15min annealing time.

The first improvement to the curing process was done by Schwab [81], who introduced vacuum steps during a prolonged heating ramp, lowering the specific resistivity of CP-003 layers from previously 13.5 to 8.1 $\mu\Omega$cm. The modified furnace process was very demanding to the equipment, since it required the vacuum pump to clear a hot furnace chamber

[4]The term overprinting denotes the procedure of adding a second layer of porous copper onto an already cured first one. By choosing different paste materials, a porosity gradient can be achieved [131].

Parameter	Range	CP-003	CP-PLS
ramp rate [°C min^{-1}]	5 - 72	n	-
plateau temperature [°C]	100 - 200	+	-
plateau time [min]	10 - 30	-	-
gas atmosphere during plateau	Vac / N_2 / FAV	FAV	FAV
annealing duration [min]	15 - 180	+	○
FAV flow rate [l min^{-1}]	1 - 9	○	○

TABLE 3.6: Screened furnace parameters and their influence on conductivity. Legend:
+ ... positive correlation
- ... negative correlation
○ ... no significant impact
n ... parameter not screened

of formic acid vapor, which lead to corrosion of the pump. Also, the process was not well understood, which lead to the investigations of Eichinger [62], who analyzed the curing process from the scratch.

In order to enhance the removal of organics, a plateau phase within the ramp was introduced. Eichinger investigated the ethlyene glycol based paste CP-003 and the, back then new, isoprenoide based paste CP-PLS-291014-R1. The scanned parameters were correlated with their impact on porosity, specific resistitivy and layer thickness. Simplified results of Eichingers findings are summarized in table 3.6. It is important to mention that this is just a summary, Eichingers actual findings are more complex, since during a DoE also parameter combinations are screened. For example, when varying the plateau time at a constant plateau temperature with the paste CP-003, the effect at the lower parameter value of 100 °C was positive, resulting in layers with higher conductivity, whereas at 200 °C the effect was negative. In this case, the parameter plateau time in table 3.6 is denoted with a negative sign, since the overall best conductivity was achieved with 200 °C plateau temperature and 10 mins of plateau time. Hence, the table shall give an overview on the best combination of the screened parameters, rather than going into details on the correlation between them.

Summarizing the findings of Eichinger, the paste CP-003 is rather insensitive towards changes during the plateau phase, whereas it requires long annealing in order to gain low specific resistivities. The paste CP-PLS on the other hand is strongly dependent on a well-designed plateau step, probably due to its low curing temperature feature, which requires careful removal of organic components at low temperatures prior to the particle sintering. The results shown in table 3.6 only refer to the impact of the furnace parameters on the conductivity, but there are more aspects to consider. For example, the

positive effect of grain growth on the specific resistivity is overlapped by much stronger effects like the removal of organic content and hence is not considered in those results, but might have an important effect on the behavior of the die upon operation, e.g. on its reliability. EBSD analysis has shown that the copper grains of a CP-PLS layer during annealing at 400 °C grow by the factor of three (0.03-0.31 μm vs. 0.09-1.14 μm) [62].

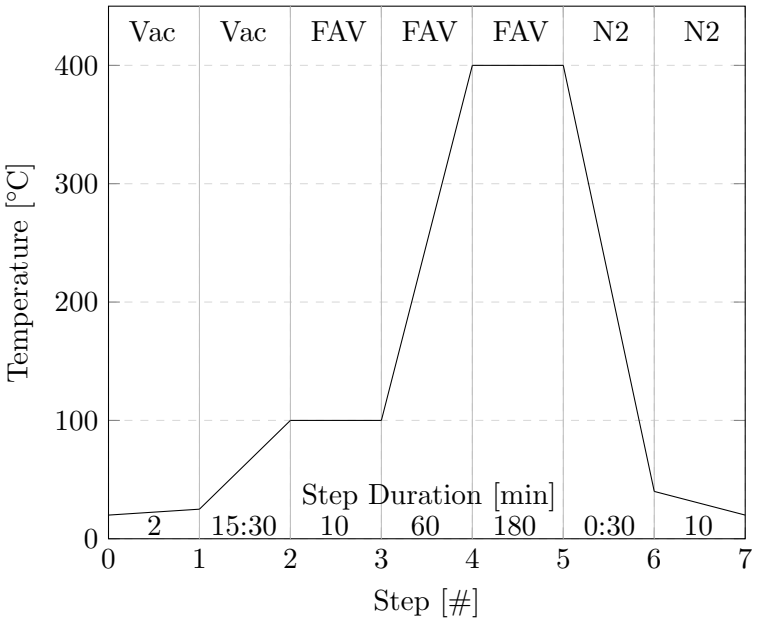


FIGURE 3.19: Optimized furnace recipe for CP-PLS-291014-R1 curing, including a plateau step (2) and an annealing step (4)

Another important finding was that the annealing time has a direct influence on the bondability of the layers. Successful bonding of aluminum and copper wires as discussed in section 3.4.2 was only possible after optimizing the furnace recipe towards higher material hardiness. This vague term, which is hard to quantify, was determined by scratching with a diamond-tip pen in printed copper layers treated with different furnace recipes. Some layers were easy to scratch, indicating only weak connection between the sintered particles. Other layers were so tough that it was even hard to scratch through them to reach the silicon substrate. The samples gained from the DoE of Eichinger were tested with this method and the furnace recipe that was used on the toughest ones was then used for the aluminum and copper wedge bonding trials. The striking feature of this furnace recipe, which is shown in table 3.7 is the long annealing time of 180 mins.

Although the two furnace recipes only differ in the plateau steps, the considerations that lead to those recipes were very different. For CP-003, the most important parameters

Parameter	Unit	CP-003	CP-PLS
ramp rate	°C min^{-1}	5	5
plateau temperature	°C	200	100
plateau time	min	10	10
gas atmosphere during plateau		FAV	FAV
annealing duration	min	180	180
FAV flow rate	l min^{-1}	1	1

TABLE 3.7: Parameters of the optimized furnace recipes for CP-003 and CP-PLS.

are the long annealing time and the high temperature plateau phase under FAV. For CP-PLS, the short plateau time at low temperature under FAV is important to achieve a high conductivity, whereas the long annealing time is needed for bonding. All the other parameters were chosen for economical reasons, i.e. cost saving by reducing the FAV flow and process time reduction by shortening the plateau time. It is important to mention that those parameters were gained from a DoE, meaning that high and low values from each parameter were tested in combination with each other according to a mathematical model. The boundary conditions, i.e. the high and low parameter values, were chosen based on previous experience, but it is possible that the optimal value for those parameters lies outside of that range. For example, the best conductivity values for CP-PLS were achieved with a plateau temperature of 100 °C, but it is not unlikely that the actual optimum is at e.g. 90 °C.

The best furnace process for CP-003 gave a specific resistivity of 6.98 $\mu\Omega$cm, the worst achieved 8.57 $\mu\Omega$cm. For CP-PLS the lowest and highest value were 4.37 and 12.55 $\mu\Omega$cm, respectively. Those values compared to the lowest resistivity achieved with the initial furnace process shown in figure 3.18 point out the enormous potential that lies within an optimization of the furnace process and nourish the hope to even succeed the already very good value of 4.37 $\mu\Omega$cm, which is less than the demanded resistivity of 3 × bulk. Yet, further experiments to narrow down the parameter range to optimal values at this point in time does not seem appropriate, since the ATV SRO-700 furnace is no tool that could be used for a productive process, and the exact values of the optimal parameter set is very dependent on the equipment.

3.3.4 Development of a Curing Process for the Wafer Back-Side

On the wafer back-side the temperature limitation of 400 °C is often reduced further, depending on the thin-wafer carrier technique. All vertical transistors need to be thinned down to a certain thickness that is limited either by the electrical requirements of the technology (high power applications) or by the technological possibilities (low-medium power applications). Thinning a wafer means mechanically grinding its back-side after having finished the front-side, followed by an etching step to remove the distorted part of the silicon crystal. While grinding the back-side, the front-side is protected with either a foil or - if further stabilization is needed - a so called "glass-carrier" (GC), which is a wafer made out of Borofloat® glass that is attached to the wafer front-side with an adhesive glue. The foil can only be used if the final wafer thickness is more than 200 μm, which is the minimum thickness that can be handled without a carrier system, or if the wafer is stabilized with a TAIKO-Ring, which limits the thickness to a minimum of around 80 μm. As explained in section 1.1, for most low-medium voltage MOSFETs the electrically necessary Si-thickness is below 10 μm, which means that the wafer needs to be carried by a rigid glass-carrier wafer. The afore mentioned glue that is used to attach the glass-carrier to the silicon wafer is thermally sensitive. A graph indicating the stability of the glue under thermal load in the ATV SRO-700 furnace is shown in figure 3.20.

The diagram was obtained by heating up glass-carried 35 μm thick dummy[5] wafers in the ATV furnace according to modified versions of the furnace recipe depicted in figure 3.19, in which the maximum temperature and the hold time were changed according to the figures in the diagram. Damage to the glue could be visibly detected through the glass-carrier as bubbles, as it can be seen in the top-right corner of figure 3.20 as white bubbles in the dark area. The maximum temperature without any holding time was determined to be 260 °C, although further investigations by D. Herman [132] showed that depending on the exact wafer type (thickness, technology) the maximum temperature could be as low as 250 °C. Figure 3.21 shows the resistivity of CP-003 and CP-PLS-291014-R1 in dependence of the maximum curing temperature. The curve was acquired ex-situ, i.e. the pieces were cured up to the respective temperature and then

[5] Dummy in this context refers to the absence of any electrically relevant zones like e.g. implantations on the wafer.

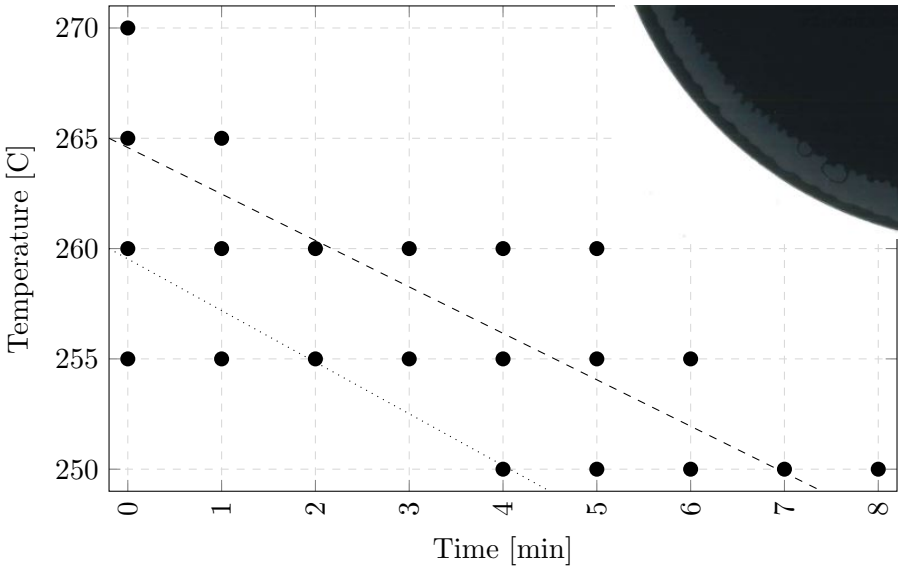


FIGURE 3.20: Thermal stability of the standard glue for GC mounting. Black dots indicate measurements, dots below the dotted line indicate suitable process conditions (no thermal damage), dots between the dashed and the dotted line indicate some yield loss on the wafer edge. The picture in the top-right of the chart shows a thermally damaged glue below the GC.

the furnace was cooled down. The resistivity measurement was done shortly after the curing in order to avoid influence of the growing oxide layer on the surface.

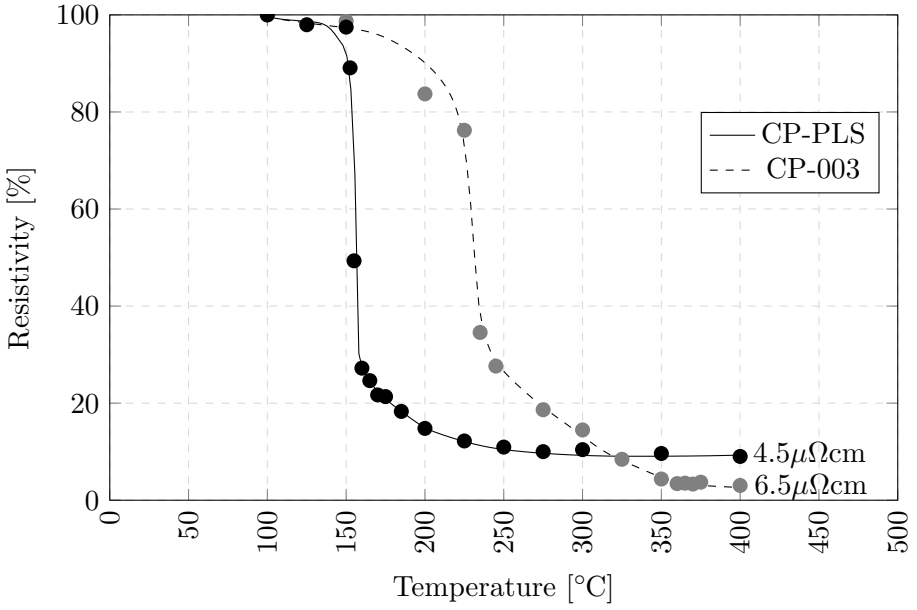
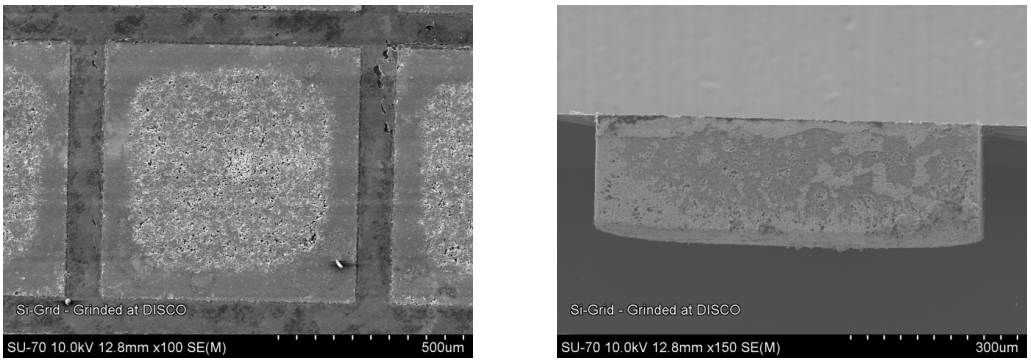


FIGURE 3.21: Development of specific resistivity in dependence of the curing temperature.



a) b)

FIGURE 3.22: Top-view (a) and cross-section view (b) on a chip-TAIKO dummy device filled with copper paste.

As it can be seen in figure 3.21, the paste CP-PLS reaches its final resistivity at approximately 250 °C, while the resistivity of CP-003 continues to fall until a temperature of 350 °C is reached. For ethylene glycol based pastes like the CP-003, sintering on GC is therefore no option. Trials to sinter CP-003 in a two-step process first at 250 °C on glass carrier, then demount the wafer and sinter at 400 °C with a free-floating 40 μm MOSFET wafer resulted in a "tortilla wrap" shaped wafer. Mechanical support by a clamping device lead to wafer breakage due to the high tensile forces of the thick copper paste during the sintering process.

In order to circumvent the temperature limitation of glass-carried wafers, the concept of the chip-TAIKO was applied: Instead of grinding the whole wafer back-side down to the desired end thickness of the active area, a backside mask is applied and only the active areas of the individual chips are thinned by an etching process, e.g. plasma or wet-chemical. The remaining thick silicon in the sawing streets is stabilizing the wafer, hence enabling handling similar to a TAIKO-ring wafer. The cavities must then be filled at least partially with a metalization, e.g. solder paste [133]. In a first attempt to combine this concept with printed copper pastes, Travan manufactured 400 μm thick wafers with 200 μm deep cavities, which then were filled with copper paste (Figure 3.22) [47].

The isoprenoide based paste CP-PLS enables a one-step curing process at temperatures compatible to the glass carrier. Sheet resistivity measurements on the wafers from figure 3.20 that were backside coated with 12 μm CP-PLS-291015-R1, QNA6449 showed that there is no significant difference in the resistivity of the different furnace recipes,

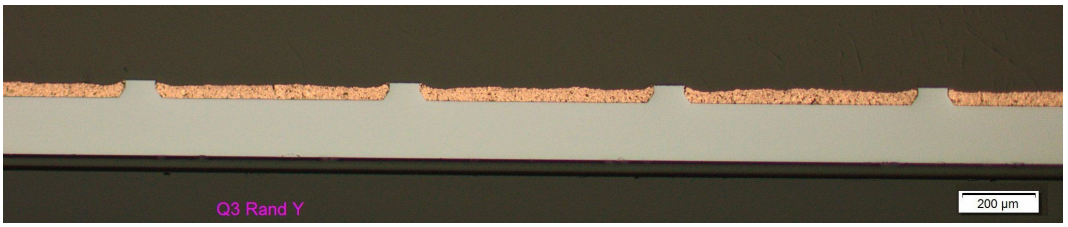


FIGURE 3.23: Microscopic picture of an array of dummy dies with a chip-TAIKO and CP-PLS metalization.

supporting the data acquired for figure 3.21. Combined with a back-side mask, the new isoprenoide based pastes would therefore qualify for a back-side metalization. Herman could prove the feasibility of this process based on a MOSFET technology wafer type [132]. For ultra-thin chips <10 μm also the Chip-TAIKO concept in combination with a glass-carrier was evaluated: Here the thick silicon sawing streets are just 40 μm thick and are not serving as stabilization for the whole wafer in order to avoid the GC, but are serving as chip stabilization during the pick-up process.

An early result of such a Chip-TAIKO wafer can be seen in figure 3.23. The wafer used in this trial still has a thickness of 200 μm, but is still attached to a glass carrier. In a next trial, this back-side metalization will be combined with a new etch-stop technique, enabling the wafer to be thinned down to a final thickness of less than 10 μm while having a thick back-side metal of 40 μm thickness.

3.3.5 Paste Sintering - Conclusions

The sintering process is the single most crucial step for defining the material properties of the final porous copper layers. Depending on its intended application, limitations in maximum temperature and time must be considered.

The old ethylene-glycol based pastes could not be cured at temperatures below 350 °C, thus making them unfit for application on the wafer back-side. As Travan showed [47], alternative concepts of thin wafer stabilization like the Chip-TAIKO technique could be combined with the old pastes, but for a silicon thickness reduction down to the needs of next generation power MOSFETs, also the Chip-TAIKO needs to be combined with a glass-carrier during manufacturing.

After separate optimization of both the paste CP-003 and the paste CP-PLS it became evident that the ethylen-glycole based branch of copper pastes can be discontinued, as

the new isoprenoide based pastes can be cured at lower temperatures and reach better resistivity values without any disadvantage.

3.4 Interconnection

Within this section, different aspects of chip interconnection will be discussed. The interconnection of a pad to the lead-frame is a topic that is treated within the back-end of semiconductor manufacturing and can be considered as a sub-topic of packaging. Packaging is a multi-disciplinary area which touches the fields of material science, mechanical design, electrical layout and modeling and various others, which makes it very complex and its issues are often not very well understood. For example, the viscosity curve of a mold compound or the length of a heat-affected zone of a bond wire during thermosonic bonding can translate into reliability of performance of a given package and hence need to be studied and taken into account [134]. Although in the practical part of this chapter only the interconnection aspect will be treated, it is still important to know and keep in mind where those processes are located within the workflow of semiconductor device packaging. As there are numerous different types of packages in use, the following description will just give an exemplary overview over two types of packages. Before going into detail, some terms must be defined for a common understanding, which are summarized in table 3.8.

When discussing the topic of packaging, one has to distinguish between low-medium power applications like automotive or consumer electronics and high power applications like DC/DC converters for power plants or IGBT modules for electric drive trains in cars trains. In the first case, packages in which the semiconductor device is embedded in a mold compound are used, whereas in the second case the chips are mounted in a module and are protected by a silicone based gel. Figure 3.24 gives an overview on the different process steps that are required for either one of those packaging types. The workflow depicted here would apply for the standard TO220 package in case of low to medium power semiconductors like MOSFETs and for the Econo-DUAL^{TM} power module in case of high power IGBT dies.

Term	Meaning
Package	Metal, ceramic or plastic casing containing one or more semiconductor electronic components
Lead Frame	Metallic structure inside the casing that conducts current to the outside
Wire-bonding	Process of attaching a wire to a semiconductor die and/or a lead-frame
Ultrasonic WB	Type of wire-bonding where the wire is attached by applying ultrasonic force
Thermosonic WB	Special type of ultrasonic WB, where the bonding process is supported by applying heat
Ball-Wedge Bonding	Bonding technique in which the first bond is formed in the shape of a nailhead, whereas the second bond is formed as a wedge. Typically done with thin ($<100\,\mu$m) gold or copper wires.
Wedge-Wedge Bonding	Bonding technique in which all bonds are formed as wedges. Typically done for very thick ($>250\,\mu$m) aluminum or copper wires.
Metal lift-off	Failure mode in wire bonding where the metal pad is separated from the die
Non-stick on pad (NSOP)	Failure mode in wire bonding where the connection of the wire to the metal pad failed
Soldering	Connection of a semiconductor die to the lead-frame by melting a metal (or alloy) with a low melting point to create a solder joint
Diffusion Soldering	Interconnection technique between a die and a lead-frame, in which the joint is not created by melting a metallic phase, but by diffusion of two metallic phases into each other
Mold Compound	Polymer that is used to embed an already interconnected semiconductor die in order to enhance mechanical stability or corrosion resistivity.
VIA	Vertical Interconnect Access, conductive path through a substrate (silicon or mold compound)

Table 3.8: Important terms in packaging technology

3.4.1 Process Flow

The first step that is required in any case is the front-side metalization, which as already discussed brings the silicon transistor in contact with the outside world. After the front-side metal (FSM) is deposited and structured, a passivation layer is applied [135]. This passivation layer can be Silicon Nitride (SNIT), an Imide, an Epoxide or similar dielectric materials and serve the purpose of insulating the die, thus preventing the access of humidity which would lead to corrosion and in case of high-power applications arcing.

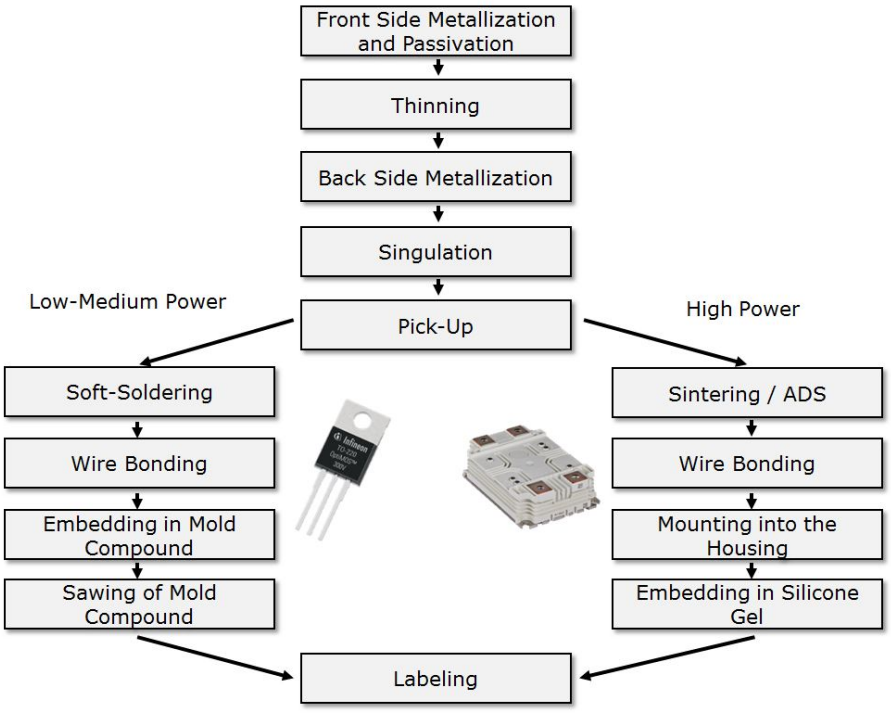


FIGURE 3.24: Scheme of packaging process steps for low-medium and high power devices.

After the front-side is finished, the wafers are thinned to the final thickness and then metallized on the back-side, before being singulated into single dies. This process, also called dicing, can be done either mechanically, by laser, by plasma or by a combination of those. For a detailed explanation of those techniques, the reader is refered to literature [136]. Singulation can be considered the last step within the back-end of line (BEOL), which leaves the singulated dies still adjacent to each other on a dicing foil, mounted on a frame. Those frames are then shipped to back-end sites, where the die-attach is performed.

The chips stick to the sawing-foil due to a photosensitive glue, which reduces its adhesive power upon UV exposure. In back-end, the foils are therefore exposed with a UV lamp and the chips are then picked. The pick-up process is schematically displayed in figure 3.25. A die (a) that is mounted on a sawing foil (b) on a frame (c) is picked from the back-side through the foil with a needle array (d), while it is lifted with a vacuum collet (e) from the top. The chip is then attached to the lead-frame with either a solder-bump, a conductive glue (unusual for power semiconductors), a silver sinter paste or in case the chip has a special backside metalization, it can be attached by diffusion soldering. In any case, the next step is wire bonding.

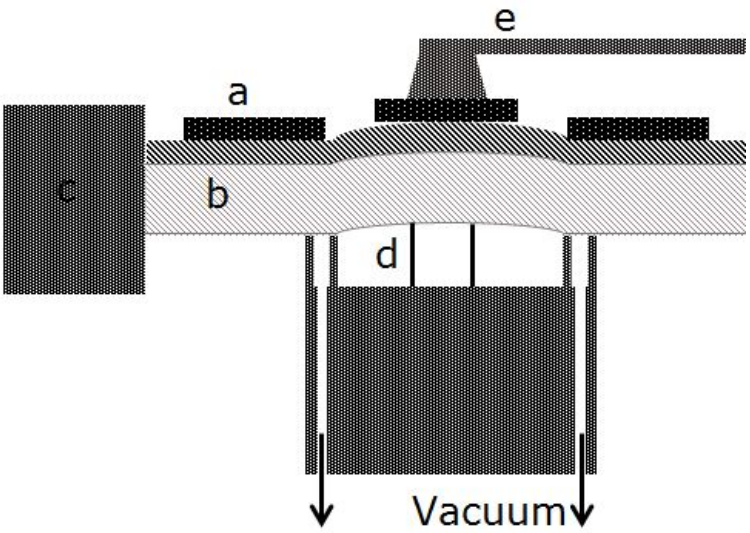


FIGURE 3.25: Sketch of the pick-up process.

The wire bonding process is very critical, since there are a lot of things that could go wrong. The list of possible failure modes in wire bonding includes dielectric cracking, silicon cratering, non-stick on lead-frame or pad, weak bond, poor ball uniformity and metal extrusion [137]. Reasons for such failures can be surface contaminations of the pads or the lead-frame, defects in the silicon due to previous mishandling, improper bonding parameters and many others. Besides those issues, an optimized wire bonding process is crucial for the device since the electrical interconnection between the front-side of the die and the lead-frame is the main resistive contribution to the overall resistance within a package [138]. For printed copper metalizations, this step is particularily critical due to the sponge-like structure of the porous metal and the hence comparably low resistance of the metal towards deformation.

In a next step, the attached and bonded dies are embedded into a housing. In case of low to medium power devices, this is done by molding the whole assembly into a mold-compound, only leaving the pins for the connection to the source, gate and drain protrude from the package. After molding, the mold compound is sawn in order to singulate the now packaged transistors from one another. After labeling, the transistors are ready for distribution.

In case of high power devices, lead-frame containing the attached and bonded dies is mounted into a module case, e.g. by soldering onto a baseplate. Depending on the module size and how many lead-frames are packaged in it, wire bonding of the frames

to each other can also be necessary. Afterwards, the dies are embedded within a silicone gel for further electrical insulation, before the module is closed and labeled.

In case printed copper is used either as front-side or as back-side metalization, it is necessary to develop processes that it can either be bonded with metal wires, or soldered with soft-solder, which will be discussed in the upcoming chapter.

3.4.2 Wire Bonding

As previously mentioned, wire bonding is a critical process due to the complexity of the bond process and the numerous issues that could emerge from surface contaminations or specific material properties. Wire bonding on porous copper is not completely new to literature: In 2013, Strasser et al. [139] reported successful wire bonding on porous copper layers generated by the plasma-dust methode. They found the sponge-like structure of porous copper to be very challenging for the formation of a stable bond and proposed an e-less[6] coating with nickel-phosporus (NiP) or nickel-molybdenum-phosporous (NiMoP) in order to increase the hardness of the layer and improve the bondability [139]. First attempts to perform wire-bonding on printed copper pastes were done by Travan in 2014, who also gives a very good and comprehensive overview on the topic itself [47].

Basically, three types of bonding that are currently in use in industry can be distinguished:

- Ultrasonic Bonding
- Thermosonic Bonding
- Thermocompression Bonding

The first two use ultrasonic force as the main source of energy to establish the bond, whereas the last one is using high heat and bonding force over an extended time period to enhance diffusion of two metals into each other. The use of thermocompression bonding is hence limited to technologies that can withstand such harsh conditions as 450 °C for 45 mins at a pressure greater than 70 kN. Also the method is limited towards usable materials, as e.g. the native oxide on the surface of aluminum is hindering the formation

[6] E-less deposition is done by using the wafer as a catalyst for the reduction of a metal in an oversaturated solution of its precursor compounds and a reducing agent.

of a metal-metal contact. Hence, mostly gold and copper are used for thermocompression bonding in MEMS applications [140]. The other two methods use ultrasonic force, which removes any contaminants and breaks up oxide on the surface of the wire or the pad, thus enabling the bonding of aluminum wires and pads [141], [142]. Therefore, those two methods are the predominant ones used in semiconductor industry and the upcoming section will deal solely with them.

3.4.2.1 Introduction into Wedge-Wedge Bonding

Wedge bonding of large diameter wires is currently the preferred interconnection method for high power electronics due to the high requirements for heat and current conduction [143]. Wedge-wedge bonding is based on ultrasonic bonding, which means that it does

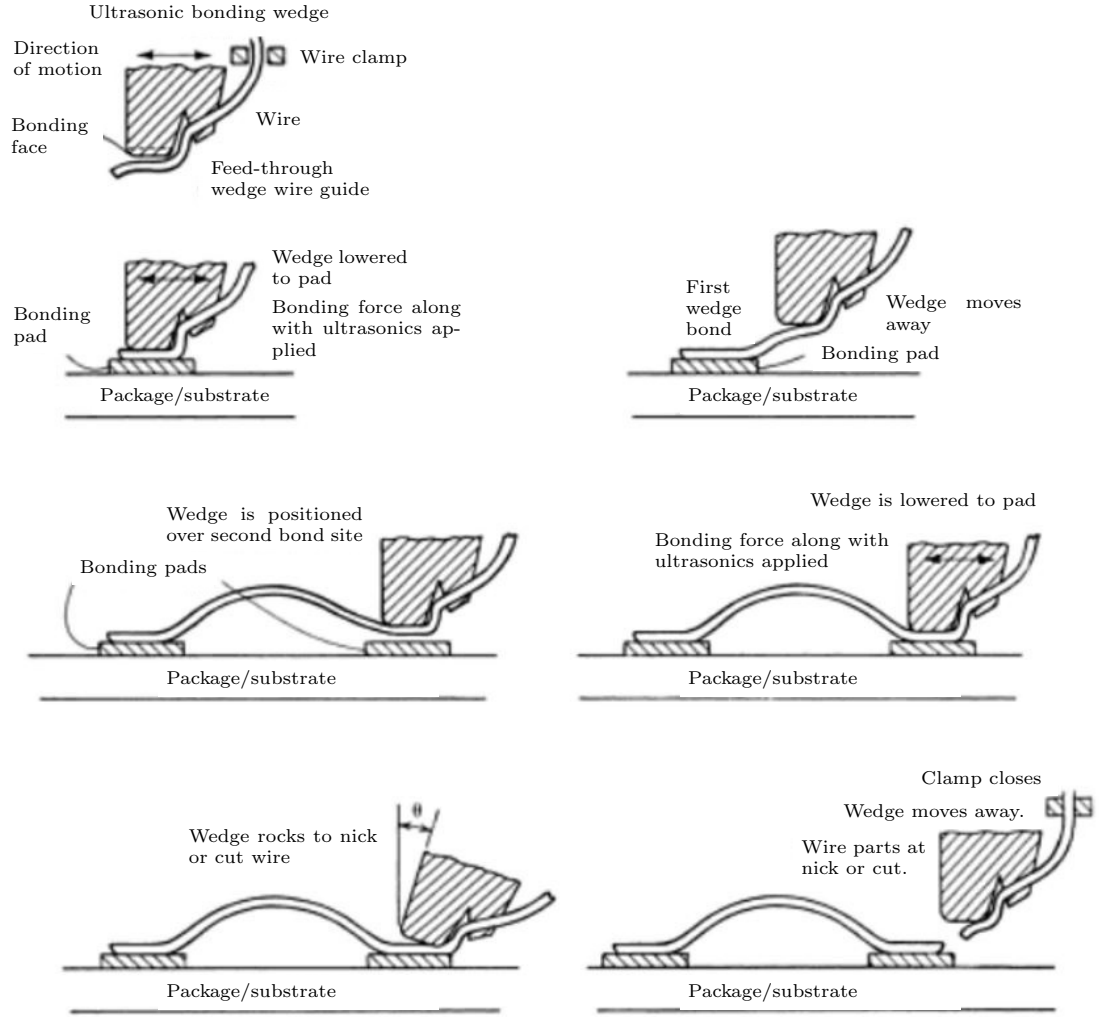


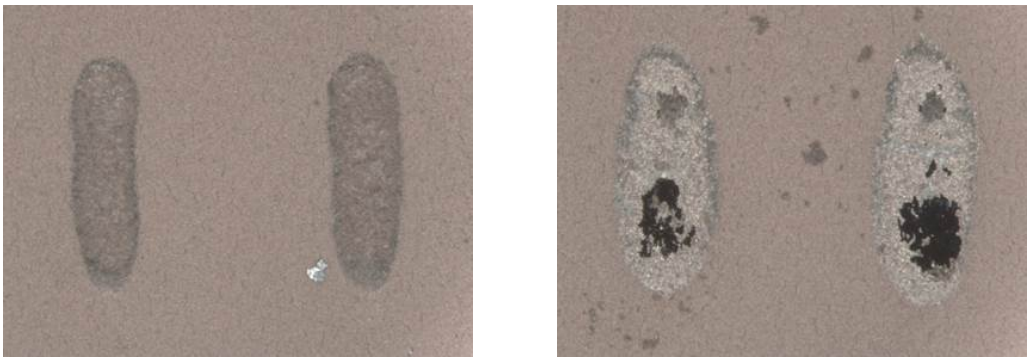
FIGURE 3.26: Sketch of a wedge-wedge bonding process, taken from literature [144].

A metal wire, typically made of aluminum, copper or gold, is fed through a wedge wire guide. The tool is pressed onto the bonding pad and vertical force in combination with ultrasonic vibrations are applied to the tool, which causes the wire to form a solid state contact with the bond pad. In a next step, the tool is lifted and moved in a defined direction with a defined speed to form a loop, before it is set on the second bond site, e.g. a lead-frame or another semiconductor die, where the bond formation is repeated. After the second bond, the wire can be cut or nicked in order to separate the wedge from the rest of the wire. After this step, the next first-bond can be placed at a different site.

While thick aluminum wires are still the industry standard, there is currently a transition to copper wires due to the superior material properties of copper. Infineon Technologies is one of the leading companies in this field, introducing 400 μm wedge bonded copper wires in their IGBT modules within their latest development, the ".XT" technology. Additionally to the copper wires for the chip front-side interconnection, this technology consists of a diffusion soldered back-side connection to the lead-frame and a reworked solder joint for the lead-frame to base-plate connection [145], [146]. With this new technology on the horizon, the trials for the wedge-bonded interconnection of printed copper FSM also focused on the .XT technology. Additionally, for comparison also bonding with 500 μm aluminum wires was evaluated.

3.4.2.2 Aluminum Wedge-Wedge Bonding

As previously mentioned, first attempts to find a suitable process window for wedge bonding on printed copper were carried out by Travan [47]. The focus of her trials was laid on offering a support metalization for low cost, high volume applications. For such applications typically aluminum wires of diameters between 250 μm and 500 μm are in use. Typical die sizes would be e.g. 4×4mm, and for a significant improvement of the heat capacity of the metalization, the printed copper layer was supposed to have a thickness of around 40 μm or more. Travan carried out her trials with the back then available ethylene glycol based pastes CP-003, CP-131113-R1, CP-181113-R1 and CP-LT-120614-R2. Despite huge efforts during several learning cycles, it was not possible to achieve even weak bonds on those porous copper surfaces. The predominant failing modes were non-stick on pads in case of soft bonding parameters and metal lift-off in case of harsh parameters, as can be seen in figure 3.27. In case of multi-layer printed



a) b)

FIGURE 3.27: Copper paste CP-003 after bonding trials with 500 μm aluminum wedges with (a) low and (b) high bonding parameters.

copper, i.e. several layers of the same or different pastes on top of each other the typical failure mode was a delamination between the different porous layers indicating a weak interface.

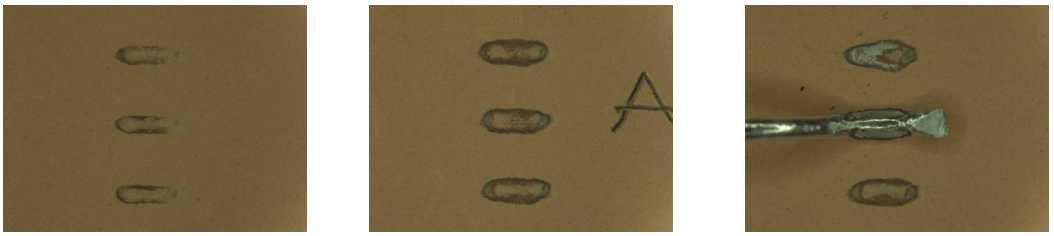
Travan concluded that besides necessary changes to the material itself, precleaning steps like MSA (methanesulfonic acid) clean prior to bonding could improve the results. The first issue was addressed by the paste supplier: The new paste CP-PLS-291014-R1 which was designed to enable back-side processing due to a lower sintering temperature also outperformed the old pastes in terms of bondability. First trials with the new paste were done using an IGBT-A stack substrates. The layer build up of the IGBT-A stack can be found in table 3.9.

Material	Thickness	Purpose
Silicon	725 μm	Substrate
Silicon Oxide	300nm	Passivation layer
Silicon Nitride	800nm	Passivation layer
Tungsten Titanium	150nm	Barrier layer
Tungsten	300nm	Barrier layer
Tungsten Titanium	50nm	Barrier layer
Copper	600nm	Seed layer

TABLE 3.9: Overview on the layers in the IGBT-A stack

The bonding trials were carried out by L. König in Regensburg. After a first parameter screening with low, medium and high bonding parameters (the exact parameters cannot be disclosed), one wedge was sticking (Figure 3.28c).

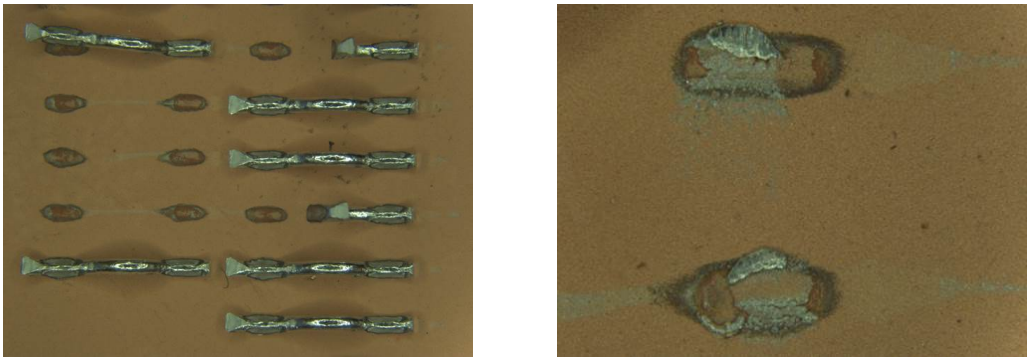
Upon this first positive indication, König investigated variations of the high bond force parameter set and was able to achieve a yield of around one third of sticking wires on



a) b) c)

FIGURE 3.28: Copper paste CP-PLS-291014-R1 after bonding trials with 500 μm aluminum wedges with (a) low (b) medium and (c) high bonding parameters.

this paste, as shown in figure 3.29a. The samples acquired from this test were then used for a shear test, which is a method used to characterize the strength of a wire bond. A steal probe head is pushing off the bond wire at a defined height in horizontal direction. The force necessary to shear off the wire is recorded, and the site is inspected optically to get a qualitative impression of the material failure. A desired result would be more than 2.5 kg of shear force and more than 50% aluminum remnants on the sample, meaning that actually the wire itself was the weakest point of the system and not the interface between wire and the pad. Microscopic pictures of the bonded sites after the shear test can be seen in figure 3.29b.

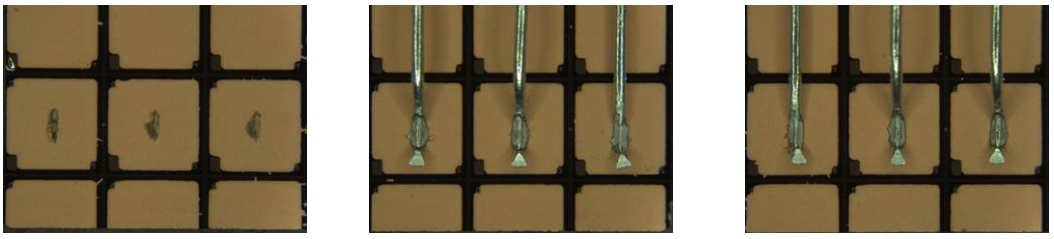


a) b)

FIGURE 3.29: Array of bonded aluminum wires on printed copper paste CP-PLS-291014-R1 on IGBT-A stack (a) and bond feet after shear test on the same bonded wires (b).

The shear test results showed an average shear force of around 3 kg, which would be a pass, but the aluminum remnants after the shear test were covering less than 50% of the area, which would count as a fail. Nevertheless, this is an encouraging result for further trials.

As a next step, the trials were carried out on dummy wafers with structured imide.



a) b) c)

FIGURE 3.30: Copper paste CP-PLS-291014-R1 on IGBT-B stack after bonding trials with 500 μm aluminum wedges with (a) low (b) medium and (c) high bonding parameters.

The wafer preparation of those sampes was carried out by D. Herman, as part of her Master's thesis [132]. The IGBT-B stack used for those trials differs from the IGBT-A stack mainly due to the presence of a Ti/TiN layer and the absence of a CVD tungsten layer. Details can be found in table 3.10. Not listed in this table is a thin layer of silicon nitride, which is deposited on top of the copper seed layer, which is then etched away through the imide mask.

Material	Thickness	Purpose
Silicon	725 μm	Substrate
BPSG	500nm	Passivation layer
Titanium	30nm	Trench filling
Titanium Nitride	40nm	Trench filling
Tungsten Titanium	300nm	Barrier layer
Copper	600nm	Seed layer

TABLE 3.10: Overview on the layers in the IGBT-B stack.

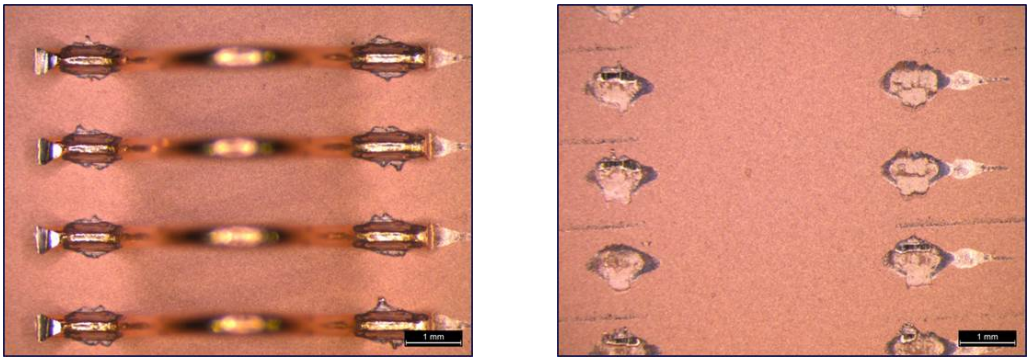
Bonding on structured wafers with IGBT-B stack turned out to be significantly more difficult than on unstructured wafers with IGBT-A stack. There were severe adhesion issues that prevented the paste from forming a solid state contact with the underlying seedlayer. Further investigations on this issue were still ongoing by the time of completition of this thesis. The most probable cause are surface contaminations of carbon or flourine from either the imide structuring or the passivation layer etching. Also remnants of the silicon nitride due to an insufficient plasma etching step could be possible. A detailed SEM analysis was performed but could not detect such remnants, but it could be questioned whether any residues would be visible in SEM at all due to their very thin layer thickness of only a few nanometers. Figure 3.30 shows the best bonding results that could be acquired on this stack, but the bond strength was so weak that no shear test could be performed.

As there is a considerable amount of interest into applying printed copper as low-cost heat sink on volume IGBT technologies, there will be further investigations done on the bonding of thick aluminum wires on this material.

Aluminium wire bonding is the industry standard not just due to cost considerations, but also since copper wire bonding is considered to be much more difficult. Copper as a metal is much harder than aluminum [147],which means that harsher conditions (e.g. higher pressure and ultrasonic force) need to be applied in order to deform the wire thus bringing it into close contact with the surface so it can form a solid state connection.

3.4.2.3 Copper Wedge-Wedge Bonding

For the first trial of bonding 400 μm thick copper wires (as used in the Infineon .XT technology) on printed copper, the intention was to support the porous copper as good as possible in order to increase the likelihood of a successful bond. Therefore, additionally to the IGBT-A stack listed in table 3.9, 5 and 10 μm of ECD copper were plated onto the wafers to mechanically support the porous copper printed on top of that layer. The wafers were sent to Infineon Warstein where they were bonded by C. Kersting. Results of this first bonding trials are shown in figure 3.31.

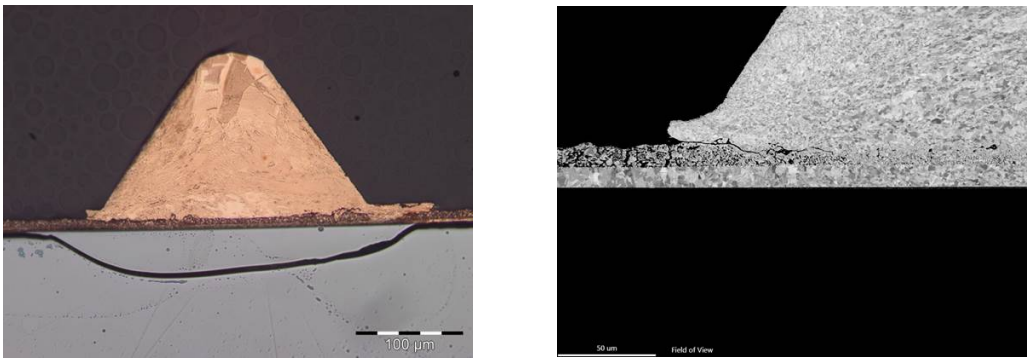


a) b)

FIGURE 3.31: Array of bonded copper wires on printed copper paste CP-PLS-291014-R1 on IGBT-A stack (a) and bond feet after shear test on the same bonded wires (b).

The necessary bond force required to establish adhesion to the printed copper paste was at least 15% higher than for the ECD copper layer used underneath the paste. The wires shown in figure 3.31 were bonded with 25% higher bond force. This amount of force was necessary to have more than 50% copper wire remnants on the wafer after

shear test, a requirement analogous to aluminum wire bonding as discussed before. The shear test gave quantitative results of around 5.8 kg shear force for those samples, which is comparable to results on ECD copper.



a) b)

FIGURE 3.32: Cross-section view on a sample of CP-PLS-291014-R1 bonded with a 400 μm copper wire in optical microscope (a) and in SEM (b).

The cross-section view of polished samples (figure 3.32) shows that the porous copper layer is compressed underneath the wedge and has nearly lost its porosity in this area. At the edge of the copper wedge and printed copper interface the SEM picture (3.32b) seems to show a crack, which is actually just a not-bonded interface. This is a normal effect that occurs due to lower forces acting on the edge of the wire during wedge formation. The crack through the silicon wafer visible in figure 3.32a is an artifact from the sample preparation. It is evident from the cross-section pictures that the printed copper was not pushed aside by the enormous bond forces, but was actually compressed and bonded. Hence, in a next step it is necessary to find out whether the ECD copper layer below the printed copper is necessary at all, and if yes, how much ECD copper is required.

Since the results of the 5 μm and the 10 μm sample were very similar, the thickness of the ECD copper layer used in the second learning cycle was 5 μm to have a reference. Additional samples had a reduced the ECD copper thickness of 1 and 3 μm, 1 μm of additional PVD copper or no metalization support at all. A detailed splitplan of the trials can be found in table 3.11.

Bonding of 400 μm copper wires was successful on all samples but sample number 25 with bond forces typically 10-40% higher than for the standard .XT parameter set, to gain a yield of >98%. The shear force of the bonds was then tested to investigate qualitative differences of the bond interfaces. The results of the shear test are presented in figure

Operation	Sample Number											
IGBT-A stack	24	25	18	19	20	21	22	23	16	17		
150/600nm TiW/Cu											2	3
ECD Cu 1 μm			18	19								
ECD Cu 3 μm					20	21						
ECD Cu 5 μm							22	23				
PVD Cu 1 μm									16	17		
Printed Cu 16 μm	24		18		20		22		16		2	
Printed Cu 33 μm		25		19		21		23		17		3

TABLE 3.11: Overview table on the samples generated for the second learning cycle on copper wedge bonding.

3.33. Several trends can be read out of the presented chart: First, it is striking that on the IGBT-A stack the presence of a supporting metal between the printed copper and the seed layer results in a significant improvement of the shear force. Sample 24, which does not contain any additional metal layer has the lowest shear forces of any 16 μm printed copper samples. Surprisingly, sample NL2 and NL3 (which are denoted as sample 2 and 3 in table 3.11) were sheared with comparable forces to the samples with IGBT-A stack and support metalization, although their metal stack comprises just of a very basic barrier and seed-layer combination.

Secondly, it is evident that thicker copper paste layers required higher bond forces and resulted in lower shear forces. Due to the fact that the high achievable thickness of printed copper metalizations is one of the best arguments for its application in power semiconductors, the inverse relation between layer thickness and bondability poses a challenge to future technology integration. From a mechanistic point of view it is easy to explain the causality of this relation: As can be seen in figure 3.32, the bonding of printed copper leads to a compression of the porous copper network below the wire up to a point where nearly no porosity is left. In case of a thin layer, this can be achieved with relatively low bond pressures, but with increasing layer thickness more force is required to compress the layer to the point where the porosity is eliminated.

On the positive side, the results of this trial clearly indicate that it is not necessary to provide thick ECD copper to achieve good bondability of printed copper, which would be a cost driver. Instead, it would probably already be sufficient to increase the thickness of the PVD seed-layer as mechanical support. The reason why the PVD copper samples 16 and 17 could not outperform the pure IGBT-A stack can be related to the two step PVD process that was used for sample preparation: The wafers were first metallized with the

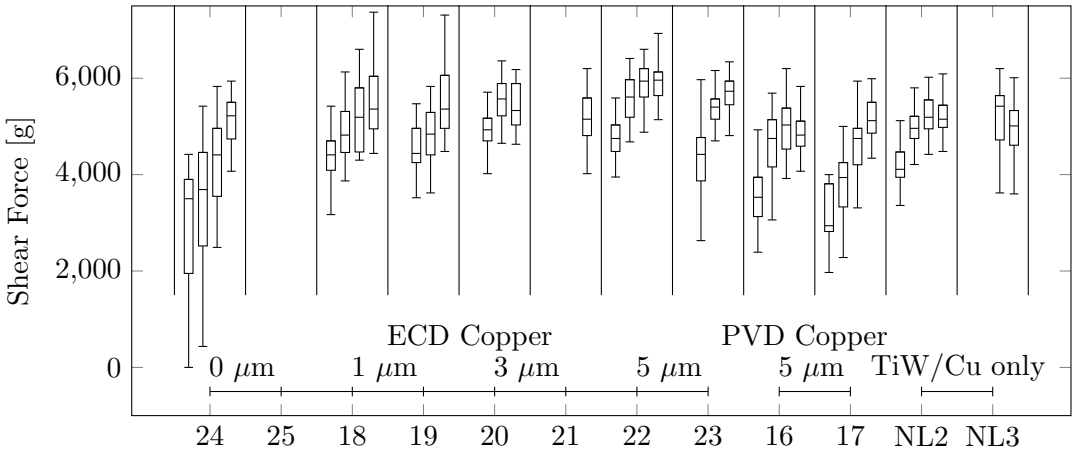
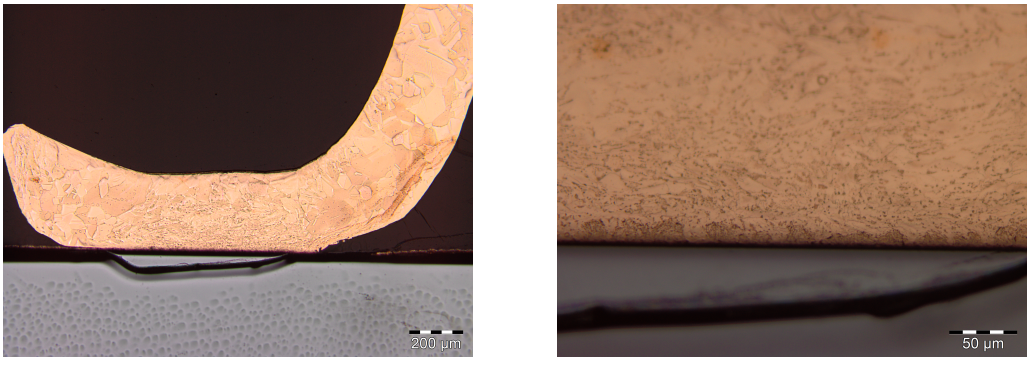


FIGURE 3.33: Box plot on the results of the shear test of copper wedge bonded printed copper on different stacks. Each sample includes four boxes, representing USF110, USF120, USF130 and USF140. Missing boxes indicate NSOP failure mode.

standard IGBT-A stack, and the additional 1 μm was deposited some time later, what enabled the formation of a native oxide on top of the first seedlayer, resulting in a bad interface between the two layers. According to PVD process engineers, an in-situ sputtering process of 1.6 μm PVD copper instead of 0.6 + 1 μm like in this case would eliminate this issue. The ECD samples do not show this weak interface due to a standard MSA preclean step that is performed before the galvanic copper plating.



a) b)

FIGURE 3.34: Cross-section view on a sample of CP-PLS-291014-R1 bonded with a 400 μm copper wire in microscope with (a) 10× magnification and (b) 50× magnification.

The bond interface was investigated on some particularly interesting samples by mechanical grinding and polishing followed by selective wet-chemical etching in order to investigate the grain structure. One typical sample (18) is presented in figure 3.34a with a detailed picture of the interface in higher magnification in 3.34b. The crack through the silicon again can be identified clearly as a preparation artifact, as this is a common

phenomenon and any damage due to the bonding process would have come up during the shear tests. When looking at 3.34a, one can get a good impression of the high forces applied during the bond process by comparing the copper grain sizes in the wire neck with the grain sizes in the area close to the interface.

Figure 3.34b shows the compression of the copper paste below the wedge. In several areas the metal of the wire was able to penetrate through the copper paste and reach the barrier interface, which is a common issue in copper bonding and one of the reasons why thicker copper metalizations are desired.

3.4.2.4 Ball-Wedge Bonding

In contrast to wedge-wedge bonding, ball-wedge bonding is not used for high-power applications due to the limited diameter of the wire. Therefore, this technique is more suitable for logic ICs and low to medium power semiconductors. In fact, thermosonic ball-wedge bonding is the most common first level interconnection technology used in the microelectronics industry [148]. One of the advantages of ball-wedge bonding over wedge-wedge bonding is the flexibility in the direction of the bond wire: The first bond can be put on a specific site, and the bond wire can then be directed in any arbitrary direction, whereas in wedge-wedge bonding the direction of the second bond is limited.

To give a better understanding of a ball-wedge bond process, figure 3.35 displays a typical sequence of process steps. A thin wire is fed through a hollow, heated capillary. A ball is formed at the end of the wire by an electronic flame-off (EFO), which is generated by applying a high current to an electrode in proximity of the wire tip, thus ionizing the air gap between the electrode and the wire. The transferred energy melts the tip of the wire, resulting in the formation of a “free air ball” (FAB). The heat generated in this process is also conducted through the wire, causing a recrystallization in the neck of the wire, the so called “heat-affected zone” (HAZ). This results in an alteration of the material properties within this zone, which underlines the importance of controlling the parameters of the EFO process [149]. The FAB is then pressed onto the bond pad with a vertical force and ultrasonic energy is applied in order to form the first bond. The capillary is then moved away, first vertically, then in any arbitrary direction. The second bond is formed by pressing the capillary onto the second bond pad, and again applying ultrasonic force, which causes the formation of a wedge. By lifting the capillary, the

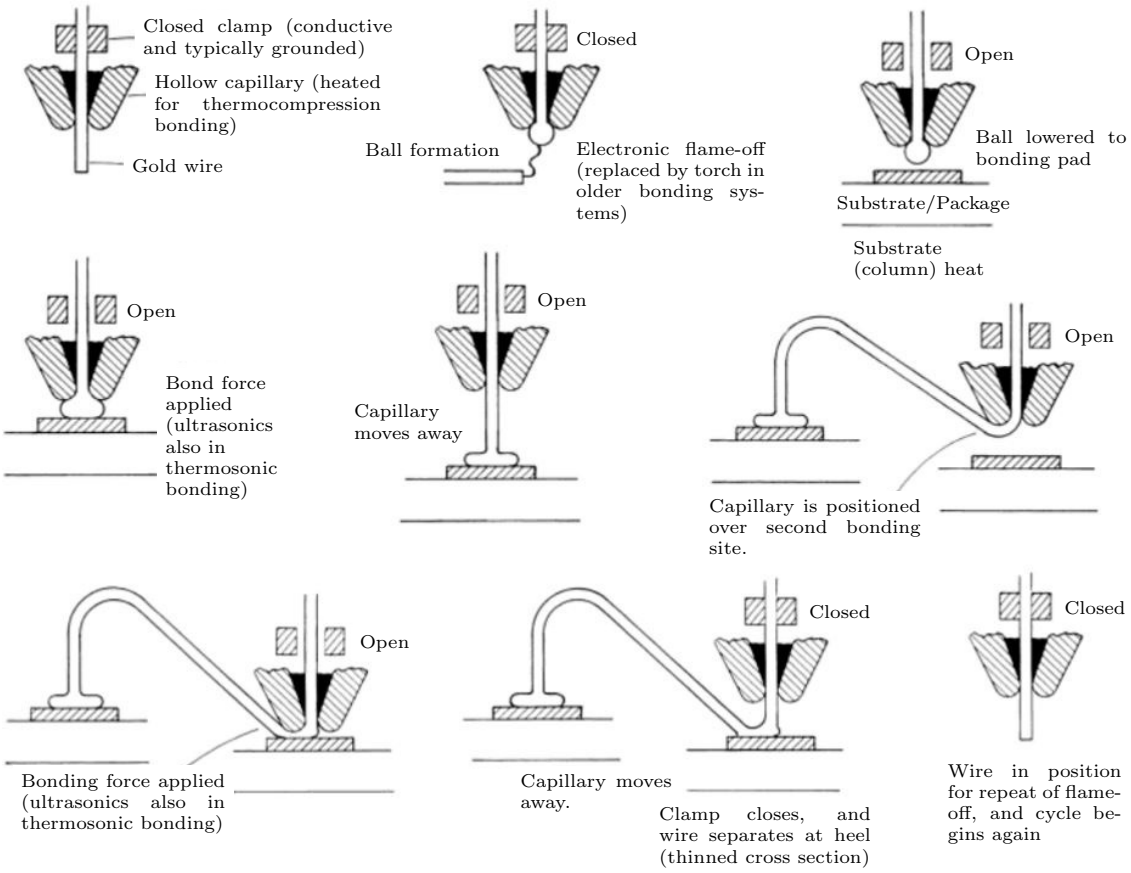


FIGURE 3.35: Sketch of a ball-wedge bonding process, taken from literature [144].

connection of the wire to the wedge is then interrupted and the process can start again by the formation of the next FAB.

Pioneering work in the field of ball bonding on printed copper surfaces has been carried out by C. Travan (Infineon Villach) and M. Hoier (Infineon Regensburg). In contrast to the results with aluminum wedge-bonding, copper ball-bonding was possible already on ethylene glycol based copper pastes. Successful bonding could be demonstrated on the pastes CP-003, CP-131113-R1 and CP-120614-R2 with 25 μm copper wires as well as on combinations of those, whereas the bonding of 50 μm copper wires was successful on all the previously mentioned pastes with the exception of the CP-120614-R2. As underlying barrier layer stack the IGBT-B stack was used. Ball shear tests gave back shear force values in the range of 80-150 g for the 50 μm wires and 60-90 g for the 25 μm wires, with the paste CP-120614-R2 as outlier with only 25 g shear force. To give a reference point, ECD copper should typically achieve shear strengths of more than 150g for 50 μm wires. Most importantly, the qualitative result was unsatisfying, as the predominant failure mode was a ball lift-off or metalization cracking.

The samples were also analyzed in a wire pull test, giving results of 10 to 45 g pull force in case of the 50 μm wires, and 4-13 g in case of the 25 μm wires, with strong variations between the different groups. The predominant failure mode in the wire pull test were ball lift-off and ball lift with pad for the 50 μm wires and wire breaks at different positions for the 25 μm wires. The desired result would be a wire break at the highest position of the loop.

The trials were redone by D. Herman [132] in cooperation with A. Adlhoch and P. Steinbauer on the isoprenoide based paste CP-PLS-291014-R1 on the IGBT-A stack. The most important results of both trial series (Travan and Herman) are shown in figures 3.36-3.38.

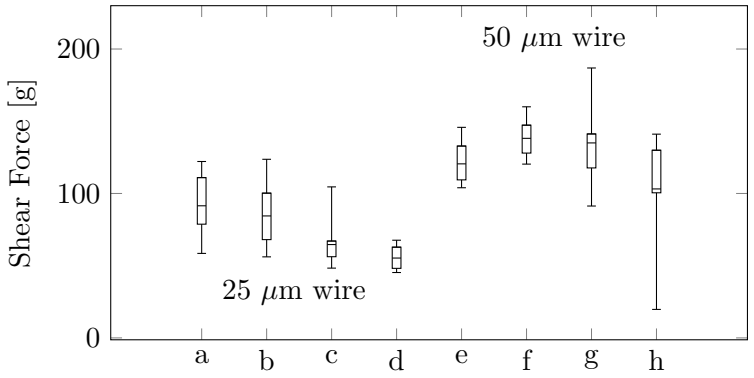


FIGURE 3.36: Box plot of the shear force of copper ball-bonded samples: 25 μm wire on a) 16 μm CP-PLS, b) 33 μm CP-PLS, c) 25 μm CP-003 and d) 25 μm CP-1311; 50 μm wire on e) 16 μm CP-PLS, f) 33 μm CP-PLS, g) 25 μm CP-003 and h) 25 μm CP-1311.

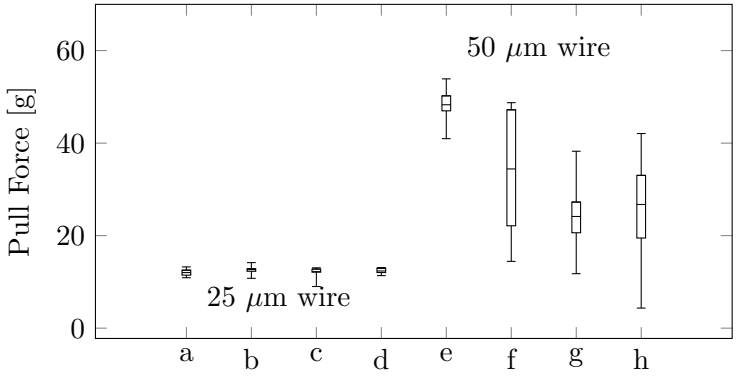


FIGURE 3.37: Box plot of the pull force of copper ball-bonded samples: 25 μm wire on a) 16 μm CP-PLS, b) 33 μm CP-PLS, c) 25 μm CP-003 and d) 25 μm CP-1311; 50 μm wire on e) 16 μm CP-PLS, f) 33 μm CP-PLS, g) 25 μm CP-003 and h) 25 μm CP-1311.

As can be seen in the box plots, there is no significant trend between the old ethylene gylcol based pastes and the new paste CP-PLS. Also, in contrast to the samples used for

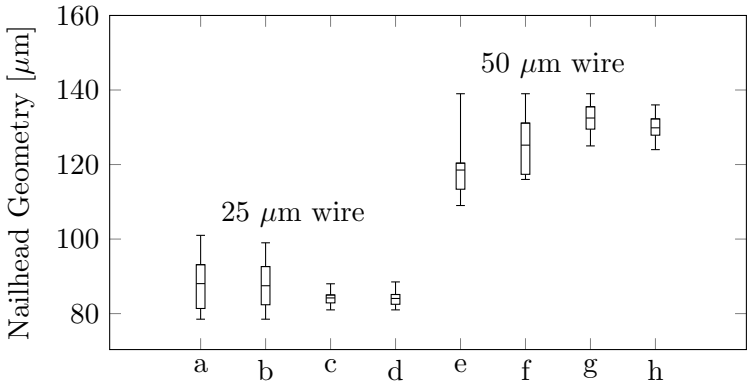


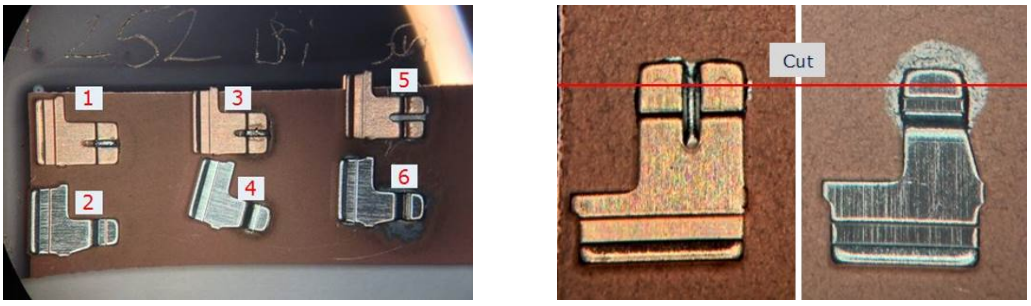
FIGURE 3.38: Box plot of the nailhead geometry of copper ball-bonded samples: 25 μm wire on a) 16 μm CP-PLS, b) 33 μm CP-PLS, c) 25 μm CP-003 and d) 25 μm CP-1311; 50 μm wire on e) 16 μm CP-PLS, f) 33 μm CP-PLS, g) 25 μm CP-003 and h) 25 μm CP-1311.

copper wedge-bonding, there is no significant difference between the two layer thicknesses of CP-PLS. The most important difference between the test series of Travan (ethylene glycol based pastes) [47] and Herman (isoprenoide based paste) [132] was the qualitative result. Travan observed mainly metalization lift off and ball lift-off in destructive testing, whereas Herman observed wire-break at mid-span in pull-test and shearing through the ball in the shear-test. Hence, the interface between the nailhead and the printed copper surface was improved slightly, so that now the wire is the weakest part in the assembly.

3.4.3 Soldering

With wire-bonding being the major front-side interconnection technique, soldering is currently the most important technique to mount the dies onto the lead-frame. Two major solder techniques can be distinguished: soft soldering uses low-melting metal alloys, whereas diffusion soldering is based on the high diffusion rates of particular metals into each other at elevated temperatures. Diffusion soldering is frequently used for the mounting of IGBTs since it is more reliable in high-power applications [150]. High temperatures resulting from large current fluxes can weaken soft solder joints and hence create reliability issues. For MOSFETs, the soft-solder technique is often the prefered method, since it is in use for decades now and hence it is well understood.

Since the main focus of application for copper printing pastes was the front-side of IGBT chips and the back-side of MOSFETs, the use of printed copper for diffusion soldering



a) b)

FIGURE 3.39: (a) Top view on soldered clips on CP-003: PbSnAg solder with (1) Cu and (2) CuAg clip, BiAg solder with (3) Cu and (4) CuAg clip and SnAg solder with (5) Cu and (6) CuAg clip. (b) Top view on two clips with an indicated cut for further analysis.

was not evaluated. Instead, several different solder pastes were combined with porous copper layers gained from different pastes representing a porosity range of 25-50%.

Figure 3.39a shows an overview on different clips soldered with different solder pastes onto CP-003, QNA6085. The samples were prepared and analyzed by M. Schneegans from Infineon Munich. Two different clip materials, copper and a copper-silver alloy were evaluated in combination with PbSnAg, CuAg and SnAg solder materials. The samples were analyzed in SEM after mechanical grinding and ion polishing, with the results being shown in figure 3.40.

The PbSnAg solder that can be seen in figure 3.40a and b as well as the SnAg solder seen in c and d easily enters the porous system and forms intermetallic phases in the whole cross section of the printed copper layer. This result is undesired, because it brings the intermetallic phases very close to the seed layer, which will eventually also be consumed, if not after the reflow process, then in the field during operation. As the newly formed intermetallic phases can have a poor adhesion to the underlying barrier layer, this is an immense risk to reliability and must be avoided. The BiAg solder used in 3.40e and f does not enter the porous copper network, since bismuth and copper cannot form a common metallurgical phase. This on the other hand will lead to poor adhesion in the interface of the solder paste with the copper pad and hence is also no acceptable solution.

The incompatibility of the most common solder materials with the standard ethylene glycol copper paste CP-003 shows that the paste needs to be exchanged in order to qualify printed copper metalizations for a back-side application. The second round of

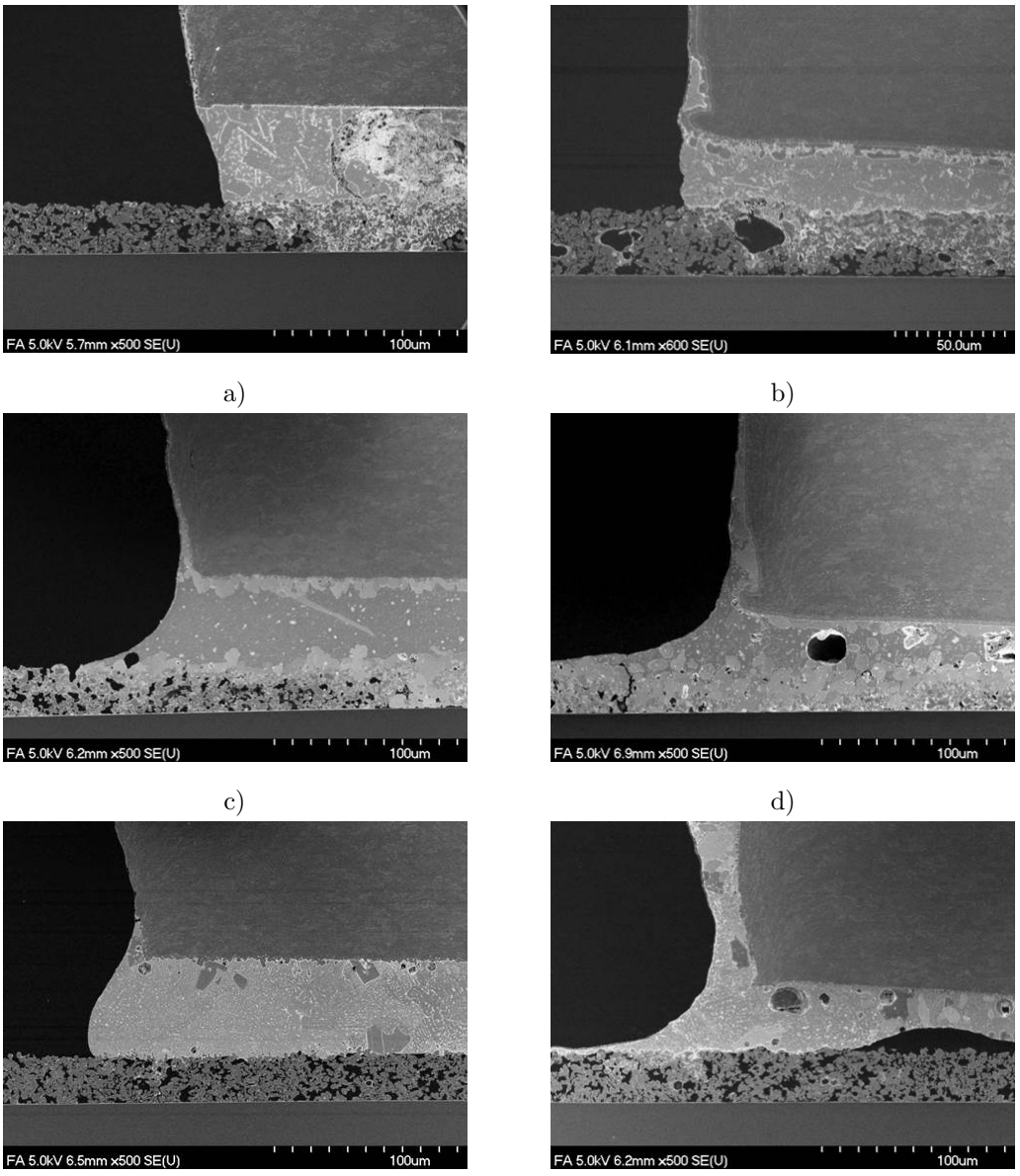


FIGURE 3.40: Cross-section view on soldered CP-003 samples in the positions specified in figure 3.39.

trials was then performed with the new isoprenoide based pastes, but using only the preferred SnAgCu solder material. This solder material is hoped to replace the PbSnAg solder, which is necessary due to the recently implemented RoHS directive requiring the use of lead-free solders in electronics industry. Figure 3.41 shows samples of all four available isoprenoide-based pastes with two solder drops of SAC solder, from left to right: CP-INF-R1, CP-INF-R2, CP-INF-R3, CP-PLS-R1.

The solder paste was applied manually by M. Schneegans. The samples were processed

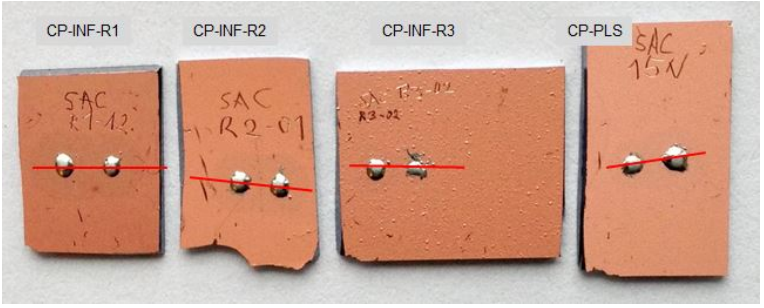


FIGURE 3.41: Top view on isoprenoide-based pastes soldered with SAC (SbAgCu) solder. Samples from left to right: CP-INF-R1, CP-INF-R2, CP-INF-R3, CP-PLS-R1.

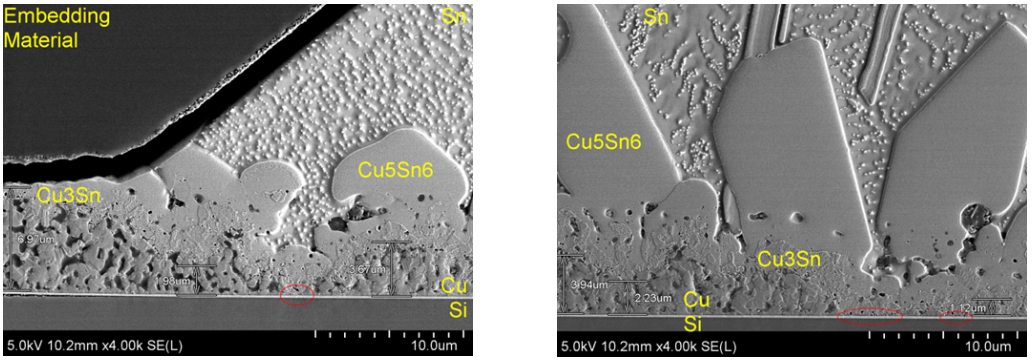
together in the ATV SRO-700 furnace at 20 mbars under FAV for 21 mins at a temperature of 260 °C. The samples were then mechanically ground and ion-polished at the position indicated by the red line in figure 3.41. The results are shown in figure 3.42.

The thickness of the porous copper layer was determined at a position without contact to the solder material (left row of pictures) and at positions below the solder bump (right row of pictures). Figures 3.42a and b show the paste CP-INF-R1, which has the lowest porosity of all the pastes (around 25%), but due to its low solid content also has the lowest layer thickness after deposition and curing. It is clearly visible that the initially 7 μm thick copper layer was completely used up by the solder material at several positions below the bump.

The paste with the highest porosity (around 50%), CP-INF-R2, enabled the liquid solder to rinse through the open pores and flow all the way down to the seed-layer (Figures 3.40c and d). As can already be seen with the bare eye in figure 3.40, the paste CP-INF-R3 has a very high surface roughness, which allows the solder to come into the proximity of the seed-layer.

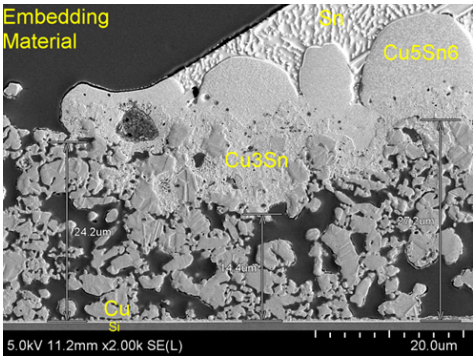
Only the paste CP-PLS-R1 showed a satisfying soldering behavior in this experiment: Although its porosity is higher than that of paste CP-INF-R3 (approx. 38 vs 35%), it was able to keep the solder paste as well as intermetallic phases efficiently away from the seedlayer. The initial layer thickness of 26.5 μm was reduced to 17.5 μm under the solder bump, leaving a comfortable amount of copper between the solder and the seed-layer.

Summing up, there are two different mechanisms by which the tin-rich phases could come into contact with the seed-layer, where they could consume the copper interface on the barrier, leading to adhesion issues: High-porous copper layers allow liquid solder material to rinse through all the way down to the barrier interface, and low-porous copper

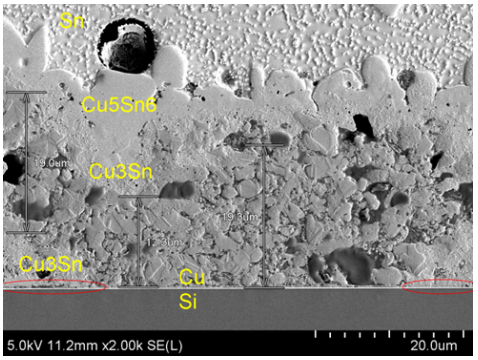


a)

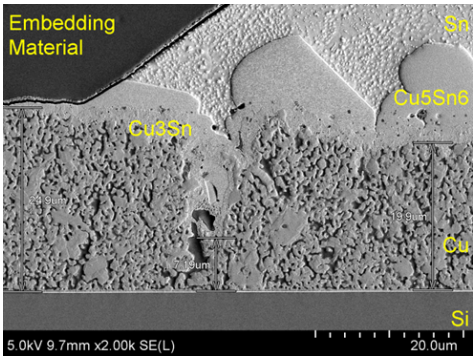
b)



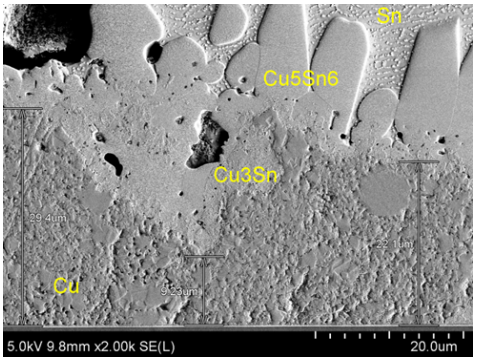
c)



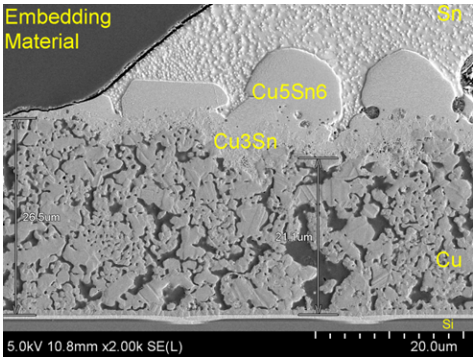
d)



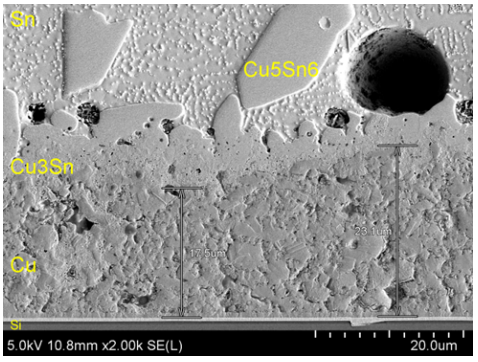
e)



f)



g)



h)

FIGURE 3.42: Cross-section view on soldered isoprenoide-based paste samples. a,b: CP-INF-R1; c,d: CP-INF-R2; e,f: CP-INF-R3; g,h: CP-PLS-R1; Left row: Position on the edge of the solder bump; Right row: Position in the center of the solder bump.

layers that prevent this effect have to be consumed up by an alloying process, with the tin-rich phases slowly dissolving the copper and progressing towards the seed-layer. The latter mechanism is identical to the soldering processes on bulk layers, although it can be assumed that due to the higher contact surface it is at least initially faster than on bulk copper.

Based on the results shown in this section it can be stated that the paste CP-PLS-291014-R1 is best suited for a possible back-side application, whereas the paste CP-INF-R1 could be interesting if it could be deposited in a higher layer thickness. Fabbro found that the paste CP-INF-240415-R1, QNA6591 could be deposited with layer thicknesses up to 70 μm without significant cracks in the surface, but the batch used in his work was corrupted due to an error of the supplier in the mixture, hence making his results not representative for the correct paste composition [151].

3.5 Summary Technology Integration

Based on the results presented in this chapter, the suitability of printed porous copper for front-side and back-side metalization of power semiconductor technologies can be assessed. Besides the specific physical and electrical criteria, the integration of a printed metalization layer into a certain technology has four basic requirements:

- **Structuring is possible:** The desired pad size and shape can be generated either by direct printing or by other structuring techniques like etching or pattern pasting.
- **Temperature budget for paste curing is available:** Printed copper pastes need curing temperatures of at least 260 °C, but depending on the desired material properties even up to 400 °C.
- **Adhesion to the substrate:** For proper sintering of the paste to the underground, a copper seed-layer is required. Any contaminations on this seed-layer might cause adhesion problems of the porous layers.
- **Interconnection is possible:** Any top metalization layer needs to be interconnected to the package by a suitable technique.

It could be shown that the bonding with a variety of wire types is possible on porous copper. Although the processes need to be further refined for reliable and good results, the principle feasibility was shown. This was the most critical question for the front-side integration, since the ability to establish a solid state connection between a wire and a porous layer without any intermediate capping layer was an issue in question. Such a capping layer would have introduced additional cost and would hence have reduced the economical advantage of printed layers over other deposition techniques.

The possible back-side application of porous copper was demonstrated by developing a suitable furnace process which is compatible with the temperature sensitive glue used for the attachment of the standard glass-carrier. Die attach of devices with porous layers on the back-side can then be performed by soft-soldering with e.g. SAC (Sn-Ag-Cu) solder paste. Here, as well as in the front-side application, the paste selection is crucial for success of the interconnection process.

In the field, the devices will have to withstand various harsh conditions like rapid temperature changes, humidity and vibrations. The full reliability qualification of printed copper could not be done within this thesis, but results from a first oxidation test show promising results.

Chapter 4

Summary and Conclusions

4.1 Summary

Printing as a deposition technique for porous copper wafer metalization was studied. Depending on the material, different post-treatment processes need to be applied and the achievable physical properties vary greatly between pastes. Especially the organic components used in the pastes have a large influence on the required processing conditions as well as on the final result.

In the paste, organics serving two different purposes are present: Solvents serve as a matrix to disperse the copper particles and keep them in a printable form. An organic binder system ensures that the particles are kept in place after evaporation of the solvent until they are sintered together. Hence, the binder needs to be removed at a higher temperature than the solvents, resulting in two steps in the TGA curve. A binder system that is based on (poly-)ethylene glycol requires high temperature treatment at 400 °C for the porous layers to gain their final resistivity, whereas an alternative binder system based on a-terpineol and isoborneol has a lower decomposition temperature and enables curing at lower temperatures. This feature is also enabling a purification of the layers, leading to reduced organic residues and hence improving conductivity. For semiconductor applications, especially in case of the presence of thermo-sensitive organic dielectrics or functional polymers, the latter binder system is therefore preferential (Section 3.3).

Besides the chemical and metallurgical purity, the specific resistivity of the porous copper layers is also interdependent on the degree of porosity. It could be shown that the specific resistivity of printed porous copper layers are in line with theoretical predictions of a modified Mori-Tanaka model. Compared to literature values for porous copper layers, printed copper has a slightly increased specific resistivity, which might be due to impurities as discussed before (Section 2.1).

Due to the high surface roughness of printed copper, the determination of the layer thickness turned out to be difficult. This was especially important for the porosity measurements, since the uppermost few micrometers of the porous layer contributes the most to the porosity, which could be shown with x-ray computer tomography (Section 2.2.3). The definition of where the bulk of the open-porous material ends and where surface roughness begins is not trivial and needs to be considered when discussing physical properties that rely on thickness measurements like porosity and specific resistivity. Hence, for the afore mentioned correlation of specific resistivity and porosity, the same layer thickness was used for both calculations.

It could be shown that it is possible to implement printed copper pastes into standard semiconductor manufacturing schemes, including deposition, post-treatment and packaging. The porous copper layer generated from the pastes can be bonded with copper- and aluminum wires with ultrasonic and thermosonic bonding techniques. Because of the lower stiffness of porous copper, the ultrasonic force must be increased compared to electroplated copper, but the bond strength measured by shear tests is comparable to standard bulk copper (Section 3.4.2).

Soldering of porous copper is possible on some selected pastes. On the exemplary system of a tin-silver-copper solder it could be shown that there are two mechanisms of solder paste intrusion into the porous network: rinsing of liquid solder material through the open pores and alloying of copper with tin. While the rinsing through open pores enables the solder paste to quickly reach the copper/barrier interface which is problematic for reliability issues, the alloying is desired for a good adhesion of the solder paste to the copper metalization layer. Here, it is important that the copper paste is thick enough to prevent the copper-tin phases to reach the copper-barrier interface within the lifespan of the device (Section 3.4.3).

One of the main advantages of copper printing over conventional types of deposition is its direct structuring capability which is offering an important cost benefit. For large dies like high power IGBT chips it is possible to structure the pads just with standard printing techniques. For smaller technologies like low to medium voltage MOSFETs additional structuring steps might be necessary, which have been evaluated in section 3.2. Some of them, in particular wet-chemical etching through hot-melt masks (section 3.2.2.3) and pattern pasting (section 3.2.3) are innovative and have therefore been claimed in form of patent applications.

4.2 Outlook

Within this thesis, large and important progress was made on the understanding of printed porous copper layers. The most important physical properties and their interdependence on the processing parameters of the raw material are now known, which creates a strong foundation for the integration of the material into semiconductor technologies. Still, there are some open topics that could not be addressed in this work anymore:

The reliability of the layers under environmental influences and in service could not be shown. Attempts to assess the reliability in thermocycling failed due to blocking points in the manufacturing of the test wafers for a polyheater test. This test uses a layer of poly-silicon as heater plate underneath the metalization layer under investigation. Short current pulses generate heat that is dissipated through the metal and lead to degradation in the course of time. This test requires special pad designs that could only be realized by pattern pasting, which became available at the end of this thesis, but issues during the wafer sawing prohibited the singulation of the dies and hence the execution of the test. With those blocking points now being identified, new test wafers will be produced in the future to generate the required samples.

The mechanical parameters of printed copper are still not known with a statistically significant certainty. Methods to determine the Young's modulus and the CTE of printed copper were evaluated and compared to each other, but the amount of samples was small and more investigations are needed. A new project with Infineon Technologies, MCL and other partners has been started to investigate porous copper layers with novel methods to gain more insights into those critical parameters.

The investigations on the compatibility with standard interconnection techniques is still ongoing. Wedge-bonding of thick aluminum and copper wires on structured dies could not be developed to a reliable process within this work due to adhesion problems. Those problems are probably related to the passivation layer structuring and will be further investigated in the future.

Studies on the integration of porous copper into several types of IGBTs, MOSFETs and other power semiconductor technologies are currently ongoing and should be finished within the next years. Then it will be decided whether porous copper will be part of a product or remains an interesting material without real application.

4.3 Publications

Due to restrictions of Infineon Technologies regarding the publication of intellectual property, no publication of research data in public journals was attempted. In the context of this thesis, a total of eight patent applications were filed in the USA, which are listed below. Applications for the same inventions in other areas are not listed.

4.3.1 Granted Patents

Title: *US9190322B2 - Method for producing a copper layer on a semiconductor body using a printing process*
Priority Date: January 24th, 2014
Abstract: A method for producing a metal layer on a wafer is described. In one embodiment the method comprises providing a semiconductor wafer including a coating, printing a metal particle paste on the semiconductor wafer thereby forming a metal layer and heating the metal layer in a reductive gas for sintering the metal particle paste or for annealing a sintered metal particle paste in an oven.
Authors: Markus Heinrici, Martin Mischitz, Manfred Schneegans

4.3.2 Published Patent Applications

Title: *US20160082718A1 - Methods with Inkjet Processes and Their Application*
Priority Date: September 22nd, 2014

Abstract: A method is described which includes depositing a first component of a multicomponent system by means of an inkjet process, and depositing a second component of the multicomponent system by means of an inkjet process.

Authors: Markus Heinrici, Rafael Janski, Susanne Kraeuter, Martin Mischitz, Stefan Schwab

Title: *US20160141208A1 - Method for processing a semiconductor substrate and a method for processing a semiconductor wafer*

Priority Date: November 14th, 2014

Abstract: According to various embodiments, a method for processing a semiconductor substrate may include: covering a plurality of die regions of the semiconductor substrate with a metal; forming a plurality of dies from the semiconductor substrate, wherein each die of the plurality of dies is covered with the metal; and, subsequently, annealing the metal covering at least one die of the plurality of dies.

Authors: Markus Heinrici, Joachim Hirschler, Michael Roesner, Martin Mischitz, Gudrun Stranzl, Martin Zgaga

Title: *US20160225718A1 - Device including a metallization layer and method of manufacturing a device*

Priority Date: January 29nd, 2015

Abstract: A device comprises a base element and a metallization layer over the base element. The metallization layer comprises pores and has a varying degree of porosity, the degree of porosity being higher in a portion adjacent to the base element than in a portion remote from the base element.

Authors: Markus Heinrici, Martin Mischitz, Stefan Schwab

Title: *US20160204017A1 - Embrittlement device, pick-up system and method of picking up chips*

Priority Date: January 14th, 2015

Abstract: Various embodiments provide a method of picking up a chip from a carrier system, wherein the method comprises providing a carrier system comprising a plurality

of chips comprising edge portions and being attached to a one surface of the carrier system by an adhesive layer; embrittling the adhesive layer selectively at the edge portions of the plurality of chips; and picking up at least one chip of the plurality of chips.

Authors: Markus Heinrici, Joachim Hirschler, Michael Roesner, Chu Hua Goh, Irina Mueller

4.3.3 Unpublished Patent Applications

Official file no.	Title
14/953,456	A device and a method for manufacturing a layerstructure
14/953,492	A method for structuring a substrate
14/997,601	A method for processing a substrate and an electronic device

Appendix A

Graphs

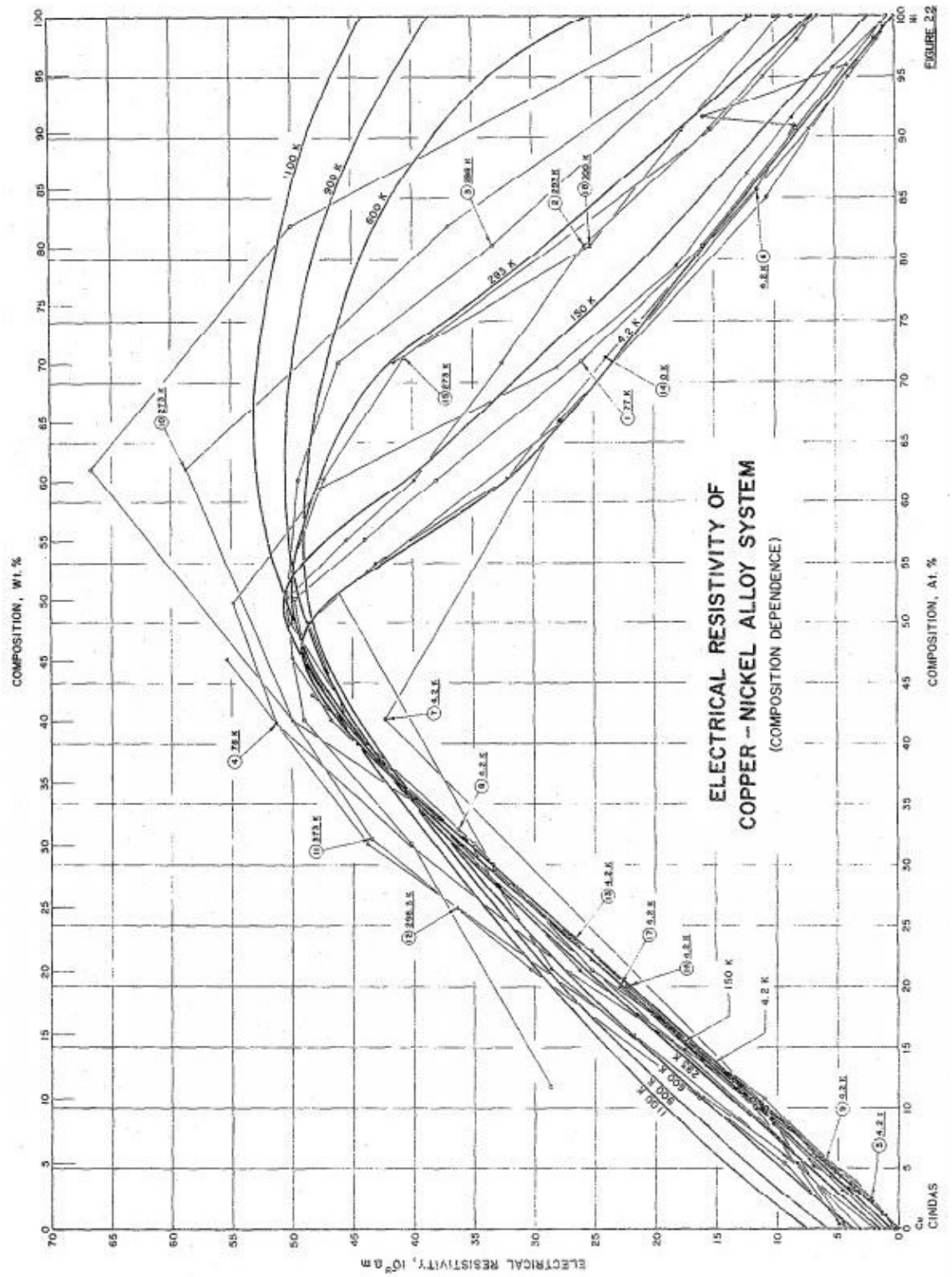


FIGURE A.1: Specific resistivity of the Copper-Nickel System at different Temperatures, found in [152]

CERTIFICATE OF ANALYSIS

Intrinsiq CP-PLS-291014R1 (Screen) Copper Paste

Requestor Name: [redacted]
Purpose: Order
Date: [redacted]

Request #: CP-PLS-291014R1 (Screen)
Amount (g): [redacted]

Paste ID: QNA 6449

Formulation: CP-PLS-291014R1 (Screen)

Solids Content: >78.8%

Viscosity
Bohlin CVO 100
Standard Small. Cone
25°C

Shear Rate	Viscosity (Pa)
50 s^{-1}	33.1
100 s^{-1}	25.8
200 s^{-1}	19.8
230 s^{-1}	18.4
300 s^{-1}	15.4
400 s^{-1}	12.6

Fineness Of Grind Test

	Microns (µm)
1st Streak	15
3rd Streak	5.0
Main Break	2.5

Signed: R Habergham **Date:** [redacted]

Intrinsiq Materials Ltd
Building Y25
Cody Technology Park
Ively Road
Farnborough
Hampshire
GU14 0LX

Tel: 01252 399781
Fax: 01252 397184
Email: sales@intrinsiqmaterials.com
Web: www.intrinsiqmaterials.com

FIGURE A.2: Certificate of Analysis of Intrinsiq Materials Ltd. paste CP-PLS-291014-R1, QNA6449 [69].

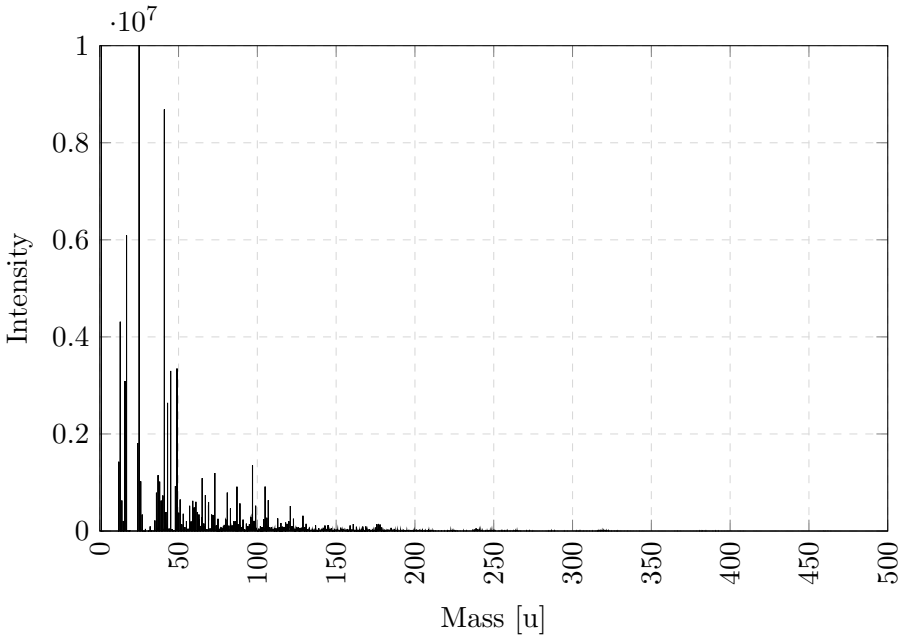


FIGURE A.3: Negative TOF-SIMS spectrum of CP-INF-240415-R1, dried.

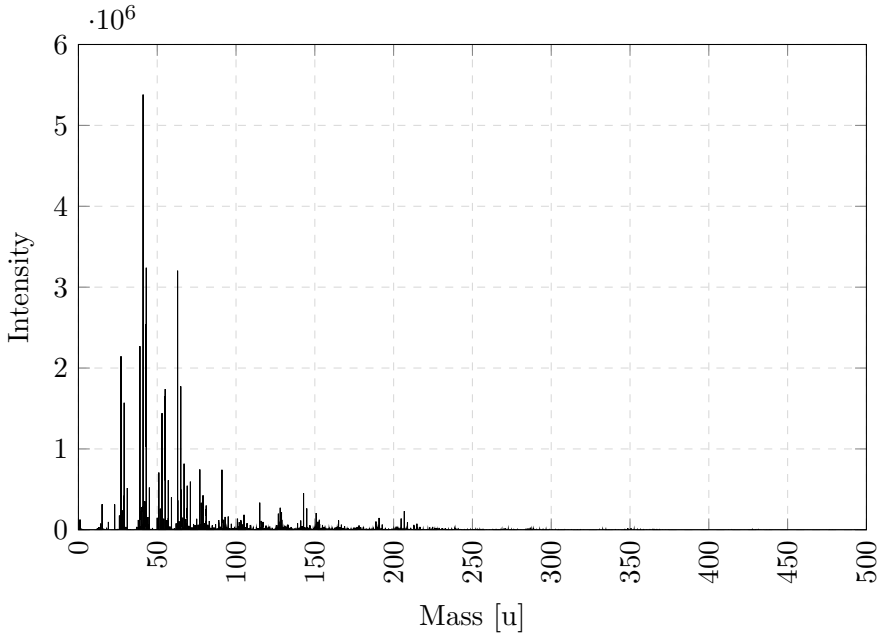


FIGURE A.4: Positive TOF-SIMS spectrum of CP-INF-240415-R1, dried.

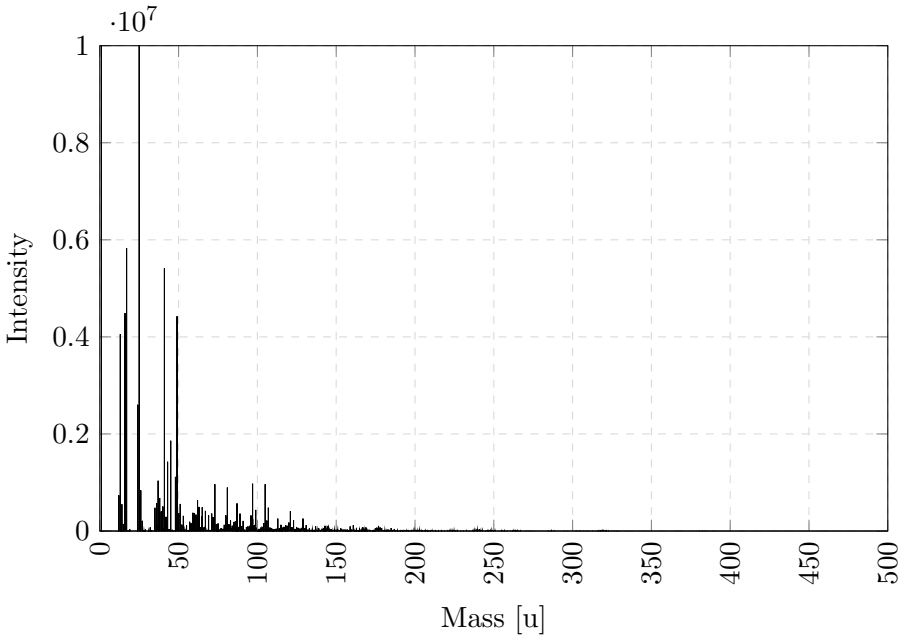


FIGURE A.5: Negative TOF-SIMS spectrum of CP-PLS-291014-R1, dried.

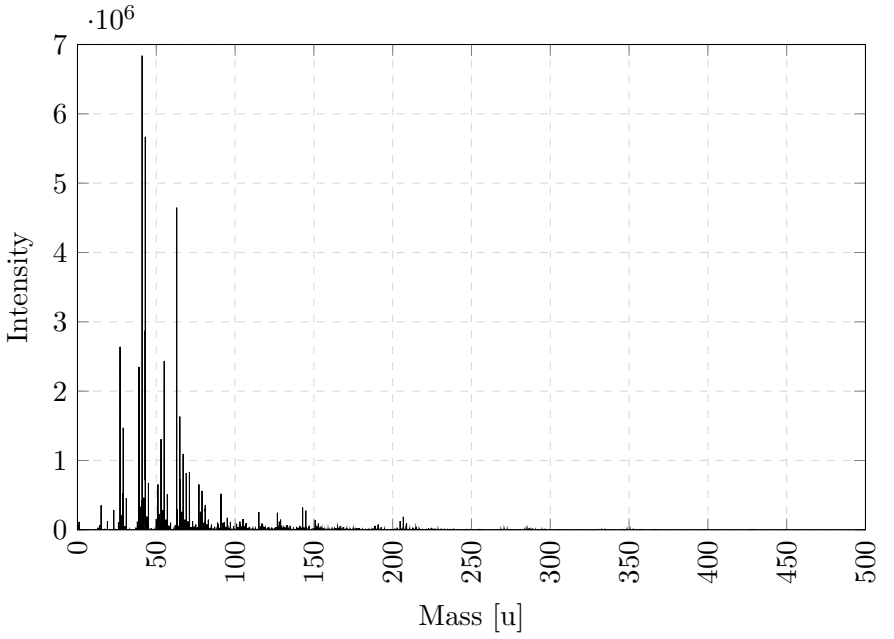


FIGURE A.6: Positive TOF-SIMS spectrum of CP-PLS-291014-R1, dried.

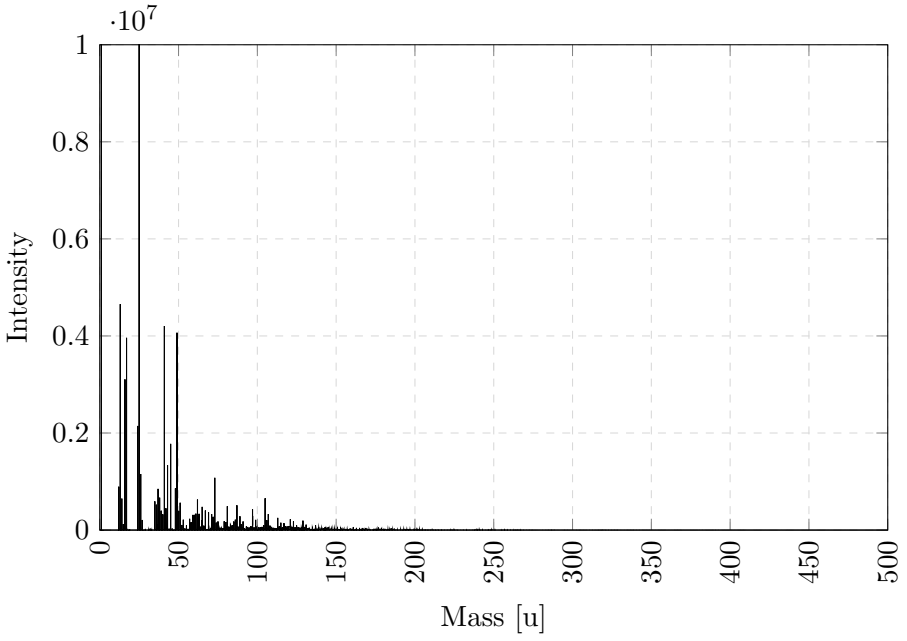


FIGURE A.7: Negative TOF-SIMS spectrum of CP-PLS-291014-R1, heated to 200 °C in formic acid.

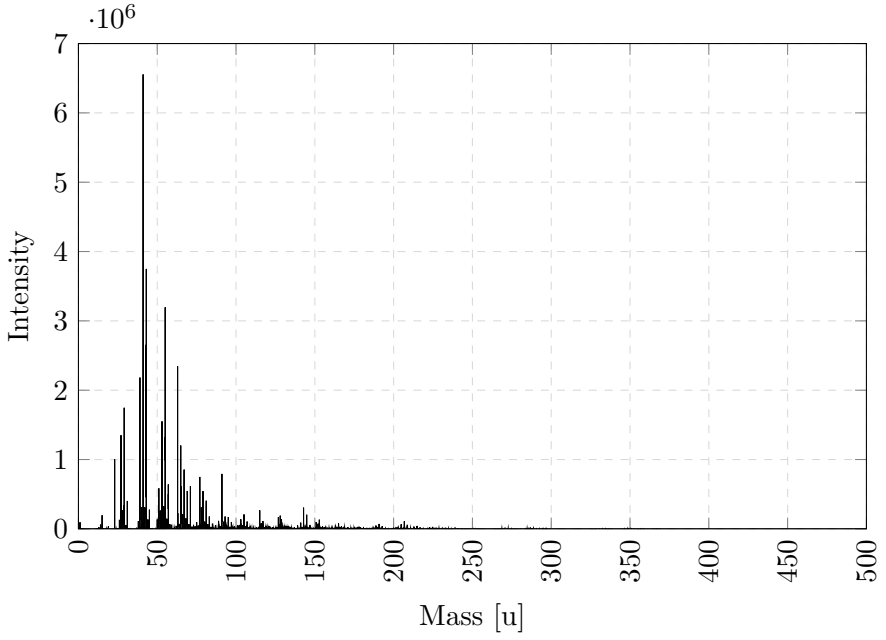


FIGURE A.8: Positive TOF-SIMS spectrum of CP-PLS-291014-R1, heated to 200 °C in formic acid.

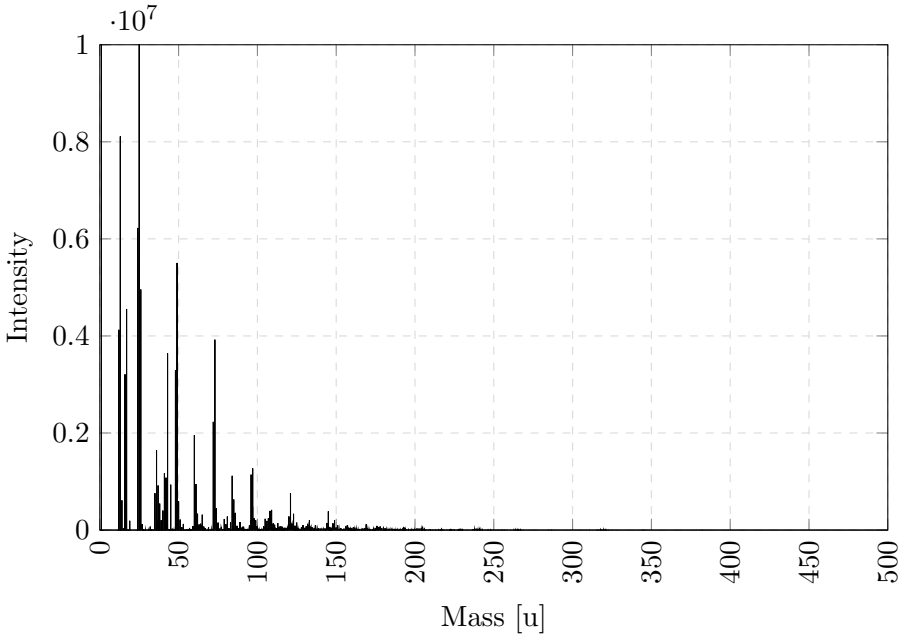


FIGURE A.9: Negative TOF-SIMS spectrum of CP-PLS-291014-R1, heated to 400 °C and held for 180 mins in formic acid.

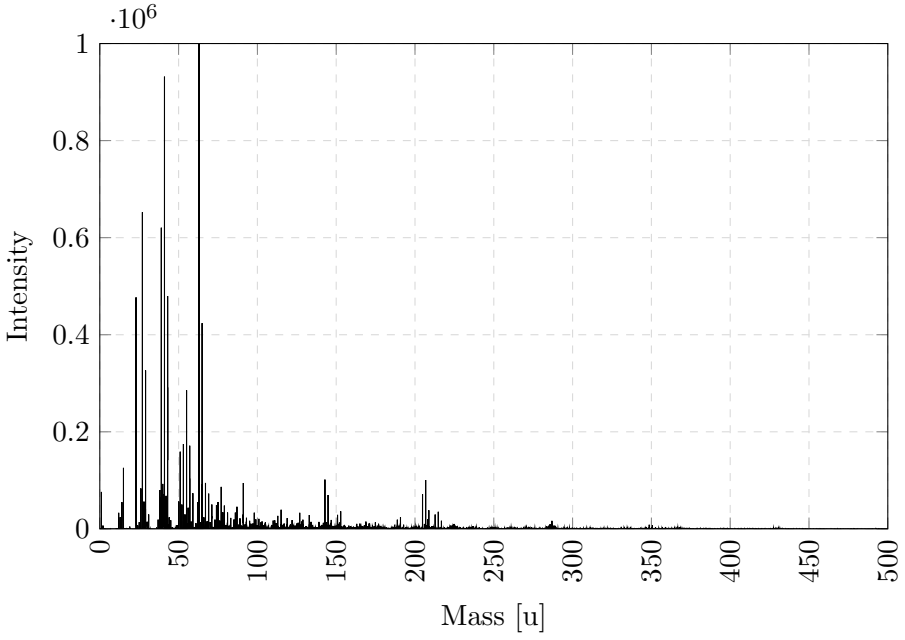


FIGURE A.10: Positive TOF-SIMS spectrum of CP-PLS-291014-R1, heated to 400 °C and held for 180 mins in formic acid.

Appendix B

Measurement Tools and Conditions

B.1 Measurements at SGS Fresenius

The paste CP-PLS-291214-R1, QNA6483 was analyzed at SGS Institut Fresenius GmbH, Königsbrücker Landstraße 161, D-01109 Dresden. The internal IFAct job number was VI15S1-03221, the order number at SGS was 3373513. Two samples (5ml and 10ml) were shipped on April 5, 2015. The samples were analyzed with ion chromatography, TGA, GC-MS, FT-IR and ICP-MS. A final report was submitted on May 7, 2015.

The following details were given on the measurement tools and conditions:

B.1.1 IR-Spectroscopy with Diamond-ATR

- Measurement of pure sample by diamond-ATR on the spectrometer Nicolet 6700

B.1.2 Ion Chromatography

- Sample weighed and extracted with 1ml of de-ionized water
- 30 minutes treatment in ultra-sonic bath
- Measured on the ion-chromatograph Dionex ICS-3000

B.1.3 TGA

- Measurement performed with the tool STA 449 F3 “Jupiter”
- Parameters of each measurement are given within the corresponding graph

B.1.4 TDS-GC-MS

- The sample was put into a thermo-desorption tube and positioned in the tool TDS3 of the company Gerstel
- Heating of the sample up to 90 °C for 30 minutes under helium gas stream
- Concentration and injection of the outgassing substances in a KAS 4 injector at -150 °C
- Measurement with a GC-MS 5975 MSD series of the company Agilent

B.1.5 Analysis of Halogens

B.1.5.1 Chlorine, Bromine

- Ionchromatography according to DIN EN 10304-2
- Wickbold combustion according to DIN 53474

B.1.5.2 Iodine

- Wickbold combustion according to DIN 53474
- Photometric measurement according to the Sandell-Kolthof method

B.1.5.3 Fluorine

- Wickbold combustion according to DIN 53474
- Measurement with ionsensitive electrode according to DIN 38405-D4-1

B.2 Measurements with Infineon Tools

B.2.1 Failure Analysis Facility

The failure analysis (FA) facilities in Villach and Regensburg offers a broad variety of tools and methods for material analysis. The author received training in using the following tools:

- Hitachi SU-70 SEM and EDX
- Nordson DAGE 4000 Multipurpose Bondtester
- Various microscopes
- Dektak XT profilometer
- Mitutoyo Vickers Hardness Testing Machine

Results acquired on other tools like Auger electron spectroscopy, EBSD, TGA-DSC as well as sample preparation techniques like FIB or embedded mechanical cuts were typically generated by FA operators or engineers.

B.2.2 Environmental Protection Laboratory

The environmental protection laboratory is part of the facility management in Villach and checks the sewage and exhaust of the production plant. Some of their tools were also utilized for the measurement of copper pastes:

- Agilent 7500cs ICP-MS
- Agilent 5975C GC-MS with DB624 (30m x 0.25mm x 1.4mm) column

The measurements were done by Zeljka Kröner, who was kindly supporting us. The copper paste samples were weighed and dissolved in aqua regia prior to the ICP-MS analysis. The GC-MS analysis was done on the pure samples.

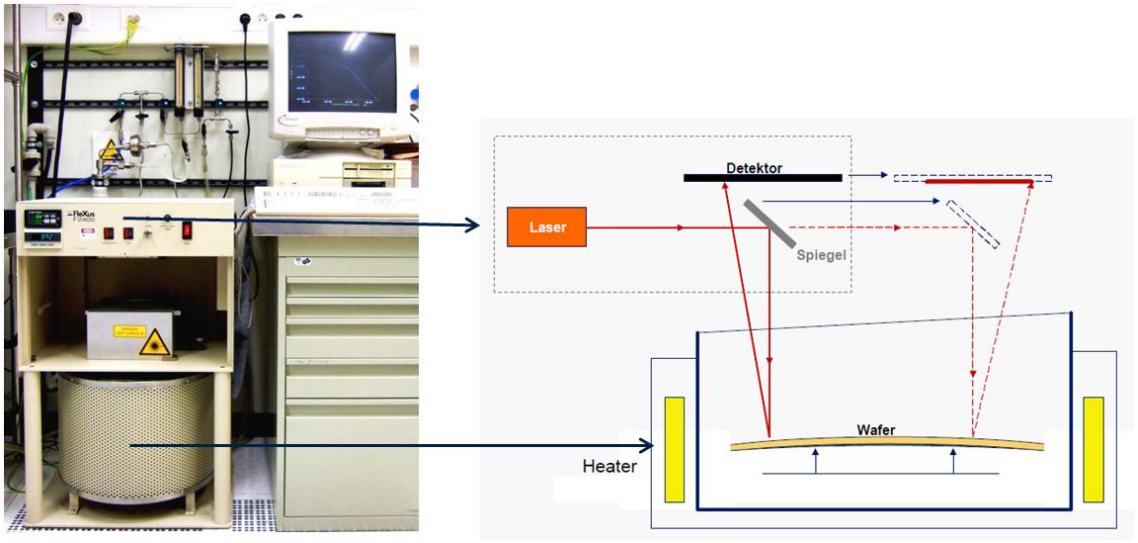


FIGURE B.1: Equipment Flexus F2400 for bow vs. temperature measurements

B.2.3 Infineon Site Munich

B.2.3.1 Wafer Curverture Measurement

Most of the wafer curvature vs. temperature measurements were carried out in Munich by Manfred Schneegans on a Flexus F2400. Since this equipment is not so common, the measurement principle will be explained in short: A wafer is placed in the measurement chamber on a three-point support. The chamber is heated and cooled in a defined way according to the measurement program. A laser beam is split and guided by two mirrors in a way that it is deflected on the wafer surface at two different points. By change of the relative position of the two laser beams towards each other, the wafer curvature can be determined. A schematic explanation of the measurement principle is given in figure B.1.

The chamber which holds the wafer is made of quarz and can be purged with gas, e.g. nitrogen, which can contain formic acid vapor. The machine is capable of heating the wafer up to 600 °C, but for the characterization of metalization layers the peak temperature is typically 400 °C.

The yield stress of a layer can be determined by calculation from the wafer curvature using the Stoney equation B.1 [153].

$$\sigma = \frac{Eh^2}{(1-v)\,6t}\left(\frac{1}{R_2} - \frac{1}{R_1}\right) \tag{B.1}$$

In this equation, σ is the yield stress, E and v correspond to the elastic modulus and the Poisson's ratio of the substrate, h and t are the thickness of the substrate and the film and R_1 and R_2 are the measured radii of curvature before and after film deposition. Typically the curvature measurement was done only after film deposition, leaving some uncertainty on the preciseness of the result, since for R_1 only statistical values of such substrates were used.

The quality of the results is further degraded by the fact that some of the prerequisites of the stoney equation cannot be fulfilled by porous layers, as they are not continuous, without defects and vary significantly in their height due to surface roughness and uniformity issues. Also, their thickness is often more than 10% of the substrate thickness (e.g. 35 μm porous copper on 300μm silicon) and can therefore no longer be considered "thin" compared to the substrate [154]. As Eichinger points out in her thesis, it can still be useful to compare the maximum and minimum stress values of Flexus measurement on a porous material to the respective values of bulk materials in order to get a feeling for the material properties [62]. This should be kept in mind when working with yield stress values of porous materials.

B.2.4 Infineon Site Regensburg

For the copper nailhead bonding trials, the colleagues (A. Adlhoch, M. Hoier, P. Steinbauer and C. Travan) were using the following tools and materials:

The used tool for bonding was an ASM iHawk Xtreme Cu-wirebonder, using a 50 μm SPT capillary for the 50 μm wire, a 25 μm Gaiser capillary for the 25 μm copper wire and an Ablebond 8290 tool for die-attach. The used wires were not coated, manufactured by Tatsuta, and having a purity of 5N (99.999% Cu).

For the adhesion testing, the tool Dage series 4000, BS250R was used with the following parameter settings:

- Power settings: 25.0 g

- Max power setting: 172.7 g
- Shear speed: $5\,\mathrm{mm}\cdot\mathrm{s}^{-1}$
- Shear height: $5\,\mu$m

B.2.5 Cleanroom Villach

Several measurement tools within the cleanroom of the Villach site were used for measurements on deposited layers.

- CDA ResMap 168 wafer mapping tool (resistivity measurement)
- PLu 2300 optical surface profiler
- E+H MX204-8 bow measurement tool
- Various SEMs, microscopes, scales

B.3 Material Center Leoben (MCL)

For the sample analysis at MCL, a General Electrics (GE) Nanotom m with a tungsten X-ray target and a diamond window was used. The voxel size was $0.753\,\mu$m, enabeling a high resolution scan. The measurement is performed by placing the sample on a rotating sample holder which is brought into proximity of the X-ray source. The multitude of 2D pictures acquired from the scans in different rotation angles are then reconstructed by the analysis software to gain a 3D model of the sample. The gray contrast in the pictures is given by the atom mass of the material. Due to its high atomic mass it was necessary to avoid the tungsten barriers typically used within this thesis for the high resolution scans. Instead, a 200nm titanium barrier was used.

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