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ADVANCED MATERIALS SCIENCE

Fields of Expertise TU Graz

Peter Hadley,
Advanced Materials Science
Source: Lunghammer – TU Graz

Our understanding of solids is largely based on studies of ordered materials where the atoms are arranged in straight rows. However, many engineering materials are composites with a high degree of disorder and sometimes a fractal or hierarchical structure. To be able to examine complex materials like this, a consortium of nine institutes from four TU Graz faculties and three institutes from the University of Graz and Med Uni Graz joined together to acquire a µCT instrument with the Austrian Research Promotion Agency (FFG) funding, awarded under its recent infrastructure call. This instrument uses X-rays to determine the microscopic structure and composition of a material. The machine uses a combination of X-ray imaging and X-ray diffraction. X-ray imaging involves measuring the intensity of X-rays that pass through a sample. This produces images like the ones conventionally used in hospitals. By taking X-ray images from a number of different angles, it is possible to make a 3D reconstruction of an object. This method is called computed tomography (CT). A µCT performs computed tomography with a spatial resolution in excess of one micron. X-ray diffraction can be used to determine which atoms are present in a crystal, the arrangement of the atoms, and the distances between the atoms. For instance, the double helix structure of DNA was first determined by crystallising DNA and measuring it by X-ray diffraction. Conventionally, X-ray diffraction has been performed on single crystal samples but the latest µCT devices can focus the X-rays on a small region, and determine how the atoms in that region are arranged. A similar measurement is sometimes performed using an intensely focused X-ray nanobeam in a synchrotron. Once the 3D structure of a material has been determined by µCT, a lot of computational work is still necessary to segment the different components of the material and determine how they are connected together. For instance, a porous material might consist largely of parallel channels or the channels might be twisted with many dead ends. The µCT will be maintained by a senior scientist, who will assist the institutes with programming data analysis routines and travel with them to synchrotrons when additional experiments using a nanobeam are necessary.

Alicja Michalowska-Forsyth,
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Radiation Damage in Microelectronics

Reliability is a wide-ranging subject in microelectronics, covering responses to different kinds of stress as well as measures to increase devices' tolerance against them. This includes ionising radiation stress, which affects device characteristics, leading to circuit degradation. Investigating such problems, as well as irradiation campaigns with custom integrated circuits (ICs) are the day-to-day focus of the team at the Institute of Electronics.

Analog IC design is an integral part of microelectronics. Designers have a host of options when it comes to meeting specifications, they need to make decisions on trade-offs between different parameters, and also need to comply with strict requirements in terms of precision, fast timing and low noise. It becomes even more challenging when reliability issues, such as ionising radiation stress, come into play.

It is this combination that makes research into radiation-hard integrated circuit design so exciting. Ionising radiation changes the electrical characteristics of microelectronic devices. As a consequence, instruments for medical and industrial X-ray imaging, space or high-energy physics have to be qualified and potentially hardened against ionising radiation. >

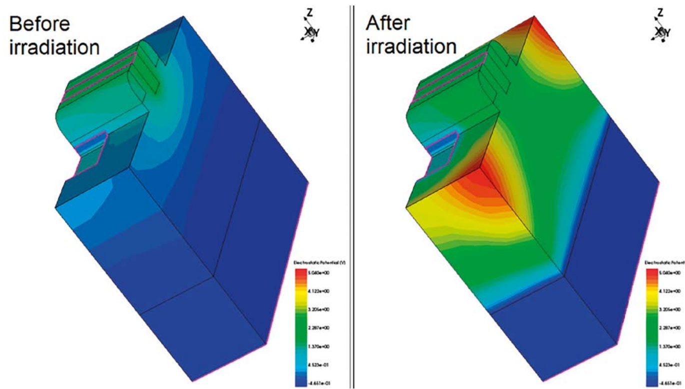

Figure 1: Simulation results: electrostatic potential of an N-type MOS transistor before and after irradiation, simulated with Sentaurus TCAD.
Source: TU Graz/Institute of Electronics

ORIGINS OF IONISATION DAMAGE

Exposing ICs to X-rays or gamma rays causes ionisation, resulting in randomly generated free charge carriers across the structure. Every IC consists of a bulk semiconductor and interleaved layers of metals and insulators. Free charge carriers in the conducting layers can be easily collected. Unless it is generated by energetic particles, the resulting current is negligibly small. In the case of insulator layers, an X-ray photon leaves behind a number of electron-hole pairs. Holes in particular have extremely low mobility, but electrons can escape the interaction region and move towards conductive layers more easily. Meanwhile, holes remain as net positive charge trapped in the insulator, producing a parasitic electric field. This effect is particularly undesirable when the insulator region is adjacent to a device, for example the gate oxide of a metal-oxide-semiconductor (MOS transistor. Even a low radiation flux can accumulate to a significant net charge after receiving a certain dose. Parasitic electric fields in the gate oxide cause the threshold voltage of an MOS transistor to shift (see Figure 1), while leakage current also increases and the intrinsic gain degrades; these are just a few of the possible effects.

In modern complementary metal-oxide-semiconductor (CMOS) ICs, the gate oxide, measured by the number of atomic layers, is so thin that the trapped oxide charge is neutralised by means of the tunnelling effect. In these modern processes, transistors are separated from each other by a much thicker insulator – this is known as shallow trench isolation (STI). After exposure to X-rays the STI is rich in trapped charge that has a strong influence on a device's characteristics. For example, a parasitic transistor is formed along the gate edge (see Figure 2), leading to off-state leakage currents.

With MOS transistors, one way to counteract this problem is to use edgeless or enclosed layouts, where the STI edge only sees the outer terminal, meaning there is no potential path for the leakage current. However, this solution cannot be used with narrow transistors; it also does not comply with the design rules of some semiconductor foundries, in particular in sub-65 nm nodes. Taking these factors into account, as well as requirements for devices other than MOS, new solutions for device geometry and the circuit topology level are urgently required to raise radiation tolerance limits.

COTOMICS AND ROBUSTIC PROJECTS

Our group at the Institute of Electronics is currently involved in several projects dealing with the radiation hardness of ICs. The precursor was the recently completed Cotomics project, which evaluated radiation tolerance and explored hardening strategies for a broad variety of devices in

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Source: Baustädter – TU Graz

Varvara Bezhenova is a university project assistant at the Institute of Electronics. Her research focuses are the overall effects of ionising doses on integrated circuits, radiation hardness of integrated circuits and analogue IC design.

Source: Baustädter – TU Graz

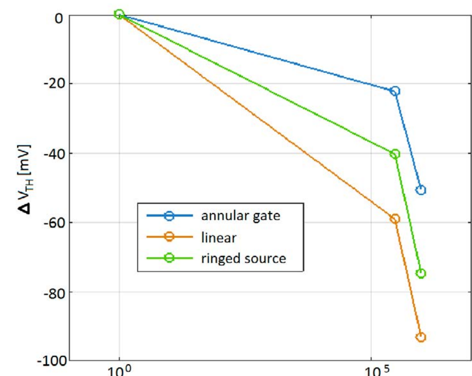

Figure 2: Experimental results: absolute threshold voltage shift of N-type MOS transistors with different layouts and same equivalent channel dimensions as a function of the total ionising dose (TID).
Source: TU Graz/Institute of Electronics

the 180 nm CMOS production process. It targeted reliability improvements in next-generation computed tomography. One of our current projects, RobustIC, is investigating the combined impact of ionising radiation, overvoltage and temperature effects, looking into new custom devices as well as circuit solutions. As a consequence of these two projects, in the last four years we have designed four integrated circuits with a huge number of devices and test circuits for radiation tolerance characterisation. So far, our results have been based on seven irradiation campaigns using a 10-200 keV X-ray tube beam (see Figure 3). For each experiment, the total ionising dose received by the circuit had to be determined at each characterisation step. We were able to calibrate the dose between three different facilities using several dosimetry techniques, in collaboration with experts from MedAustron, Seibersdorf Laboratories, CERN-EP and the Institute of Solid State Physics.

INITIAL FUNDING GRANT

Scaled CMOS processes below 65 nm are attractive for a range of sensing, signal processing and computing applications, but the effects of radiation on individual devices are still not fully understood. In 2018 our group received an initial funding grant from the Advanced Materials Science Field of Expertise to kick off research into radiation tolerance and hardening techniques in 28 nm and 40 nm technology nodes. The new SIRENS project looks beyond medical technologies to the exciting fields of space and high-energy physics instruments, where the amount of energy absorbed over a device's lifetime as a result of radiation can reach previously unexplored levels.

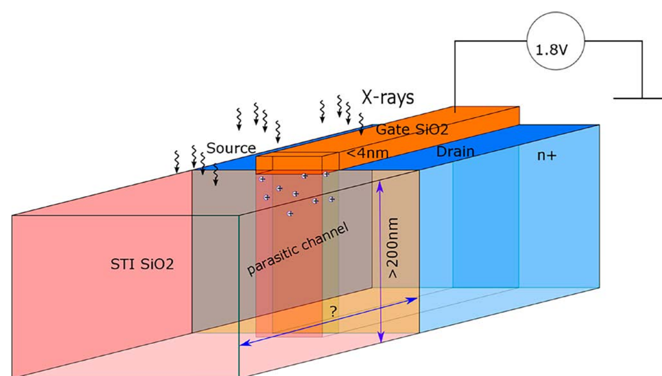

Figure 3: Formation of a radiation-induced parasitic channel by charge trapped in STI along the gate of a standard linear MOS transistor (N-type).
Source: TU Graz/ Institute of Electronics

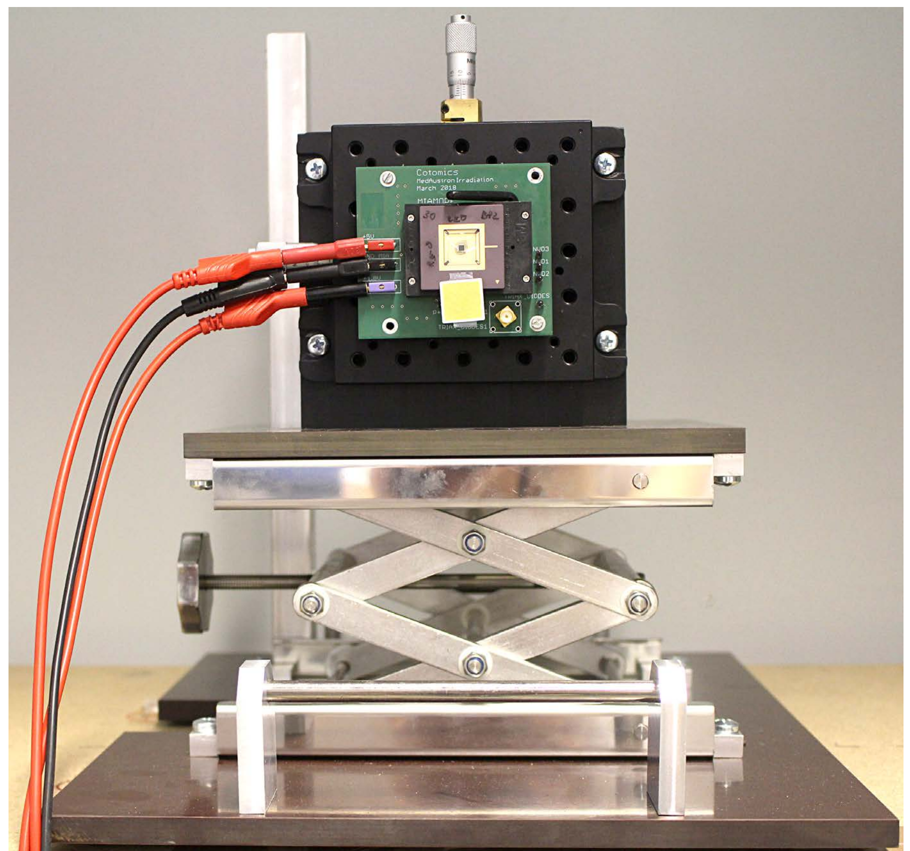

Figure 4: Exposed silicon die of the Mitigation and Modeling of Radiation Effects (MiAMoRE) IC ready for irradiation.
Source: TU Graz/Institute of Electronics