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EMI susceptibility of offset compensated CMOS operational amplifiers

DOCTORAL THESIS

TO ACHIEVE THE UNIVERSITY DEGREE OF DOCTOR IN TECHNICAL SCIENCES SUBMITTED TO

GRAZ UNIVERSITY OF TECHNOLOGY

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Graz, November 2018

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“*Voglio vivere così col sol in fronte.*”

Tonino Carotone

Abstract

CMOS offset compensated operational amplifiers are very often required as part of electronic sensing circuits. In the automotive industry, the demand for accurate sensing of several electric quantities inside the engine compartment is increasing and the importance of accurate sensing functionalities of ICs is then growing. Unfortunately, the engine compartment is a very harsh polluted electromagnetic interference environment and all the circuitry operating in such environment is heavily disturbed by high frequency interferences. The accuracy of offset compensated operational amplifiers used along the sensing mechanisms of intra engine ICs can easily be degraded by the aforementioned disturbances, forcing system engineers to make heavy use of expensive and space consuming external shielding components. Consequently, the need for offset compensated operational amplifiers with enhanced EMI robustness is becoming of crucial importance for several automotive ICs. The framework of the presented Ph.D. work develops along such need to understand how offset compensated CMOS OpAMPs react to high frequency interferences, in order to provide the guidelines for choosing the best offset compensation technique among the existing ones and for enhancing such techniques robustness against EMI. Every hypothesis regarding the susceptibility of the analysed offset compensated OpAMP topology and every solution to enhance the OpAMP robustness against EMI has been verified end proven by means of EMI injection measurements on dedicated test chips. The presented Ph.D. work has been performed in collaboration with Infineon Technologies Villach (AG) as industrial partner. The thesis is structured as follows. After a brief introduction to provide background and motivations in Chapter 1, an overview of how to model the EMI effects on regular offset uncompensated OpAMPs is given in Chapter 2, together with a brief description of the offset compensation techniques whose EMI susceptibility is the focus of this work. Chapter 3 is dedicated to one of the two most important offset compensation techniques, namely the chopping. An extensive overview of the effects of EMI on chopped OpAMPs is provided, highlighting the causes of such effects, comparing the chopped topologies with the offset uncompensated ones and providing then possible countermeasures or guidelines in order to mitigate for the unwanted EMI effects. To validate the theoretical highlights, susceptibility measurement results on several designed and fabricated chopped OpAMPs are shown. Chapter 4 focuses on the other main offset compensation technique, the auto zeroing. Due to the complexity of auto zeroed OpAMPs, usually greater than for chopped OpAMPs, the first part of the chapter is dedicated to a detailed discussion about the design procedure employed for the auto zero topology, highlighting the theory behind the design choices. After that, the analysis of the susceptibility of such topology is presented in the same way it has been done for the chopped amplifier. Chapter 5 provides for an overview of the techniques employed to evaluate the EMI susceptibility of the aforementioned devices, both at simulation level and at measurement level. All the exploited test benches are discussed and analysed in detail and an optimal solution is then illustrated. Finally, the conclusion chapter gives a broad picture of the main results achieved in the presented Ph.D. work and gives some perspective for future research.

Acknowledgements

I would like to thank all the people which patiently supported me along this Ph.D., starting from my mentor and advisor Luca Petruzzi and Prof. Bernd Deutschmann; without their help, advices and suggestions this work would have not been possible. Secondly, I would like to thank Tranca Ioan Alexandru, Herzele Gunter, Hearle Dieter, Paolo Del Croce from Body Power Infineon Villach for their precious help along the technical topics I had to face. Also many thanks to the Winkler Gunter, Soser Peter and Dominik Amschl from Graz Technical University of Technology for their great support in the lab measurements and setup. Thank so much also to my fellows Timucin, Alicia, Varvara, Patrick, Herbert, Rahul, Julia, Susanne, Erika, Beppe, Elvira, Marco, Matias and Markus for the great time spent together. Finally, a special thanks goes to my family and girlfriend Cecilia, which supported me during my staying abroad and pushed me towards the completion of the Ph.D.

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List of Abbreviations

EM	**E**lectro**m**agnetic
EMC	**E**lectro**m**agnetic **C**ompatibility
EMI	**E**lectro**m**agnetic **I**nterference
IC	**I**ntegrated **C**ircuit
OpAMP	**Op**erational **Amp**lifier
OTS	**O**ff **T**he **S**helf
PCB	**P**rinted **C**ircuit **B**oard
VNA	**V**ector **N**etwork **A**nalyser

To my mom and dad.

INTRODUCTION

This Ph.D. work develops along two very broad fields of engineering, namely the electromagnetic compatibility and design of CMOS offset compensated operational amplifiers. In the following, a brief explanation about both fields will be given, highlighting which branches of each field have been of concern for the Ph.D. Furthermore, it will be clarified how and why such big fields have been linked, also providing the motivation for this work.

Since the invention of first discrete electronic components of the early '50s to nowadays billion-transistor integrated circuits, there have been lots of concerns about the effects of electromagnetic interferences polluting the environment these devices operate in and there have also been lots of studies about the possible countermeasures against these disturbances. In particular, along the decades of continuous improvements in semiconductor technologies, it became clear that interferences can deeply affect the correct operation of electronic devices ([1]). Because of this, physicists and engineers started to develop a new field of study to better understand and define the aforementioned issues. According to [2], electromagnetic compatibility can be defined as follows:

"... happy situation in which systems work as intended, both within themselves and within their -environment."

Similarly, electronic devices are said to be electromagnetic compatible when:

"... the electrical noise generated by each does not interfere with the normal performance of any other."

The above sentences highlight that the electromagnetic compatibility of a device or system can be observed from two different perspectives. On one side, the device or system could be electromagnetically not compatible because it generates too much electrical noise. In this sense, such a device or system can be viewed as being electromagnetically too aggressive. On the other side, one device or system could be not electromagnetic compatible because it is too weak against even the minimum electrical disturbance. In such a case, the device or system is said to be electromagnetically too susceptible. In the former case then, the interest will fall on the disturbance emission of the device or system under study, whereas, in the second case, the susceptibility or robustness against electromagnetic disturbances will be the main concern (Fig.

1.1). It is then clear that EMC related problems are always about one or both the aforementioned aspects and the approaches to analyse and solve the issues may deeply differ depending on which of the two cases the engineer is facing. Another very important aspect to clarify about EMC related issues concerns how the interferences propagate from the aggressor to the victim, or, in other words, the definition of the propagation channel. For purpose, three different kinds of interferences and related propagation channels can be distinguished ([3]).

- *Radiated Interferences*

  This type of interferences concerns purely electromagnetic transversal waves and therefore can be seen as a far field radiation originating from long loops (loop antennas) or long conductors (Hertzian antennas). In this case, aggressors are represented by any kind of transmitting station or system which is able to radiate by means of an antenna. Alternatively, a poorly designed printed circuit board (PCB) or cabling apparatus could contain parasitic loops or conductors which could act as unwanted antennas. On the other side, victims can be systems or PCBs which contain wanted or parasitic receiving antennas as well and therefore can collect radiated disturbances from the environment. The expression “far field radiation” refers to a distance much greater than $2\,D^2/\lambda$, where D identifies the size of the transmitting antenna and λ is the wavelength of the disturbance ([4]). Consequently, a 50Hz far field radiation cannot occur on Earth, but since disturbances associated to 50Hz power lines do exists and are in fact very common, they have to be ascribed to another phenomenon or type of interferences, called induced interference.

- *Induced Interferences*

  Induced interferences are often referred to as capacitive or inductive crosstalks and originate from near field coupling, so that the field components, which dominate, are either magnetic (magnetic field coupling) or electric (electric field coupling). This kind of disturbances is then expected in the near field domain. The aggressors are circuits or systems in the proximity of the victims and generate parasitic magnetic or electric fields which can couple to parasitic antenna-like magnetic or electric elements of the victim, inducing then unwanted electric currents or voltages into or across the victim itself.

- *Conducted Interferences*

  Unlike the two previous types of interference, for which the propagation channel is basically represented by free air or dielectric materials, conducted interferences refer to those unintended signals which leave an aggressor IC, PCB or system and propagate through a conductor, like a PCB trace, to another victim IC, PCB or system. It must be pointed out that the aggressor and the victim do not necessarily have to be physically connected for conducted disturbances to take place, because, as it often happens, real disturbances reaching a victim can be generated from heterogeneous mechanisms. For example, radiated interferences can be picked up by a parasitic antenna element on a PCB and then conducted to a victim IC lying on that PCB via the PCB traces.

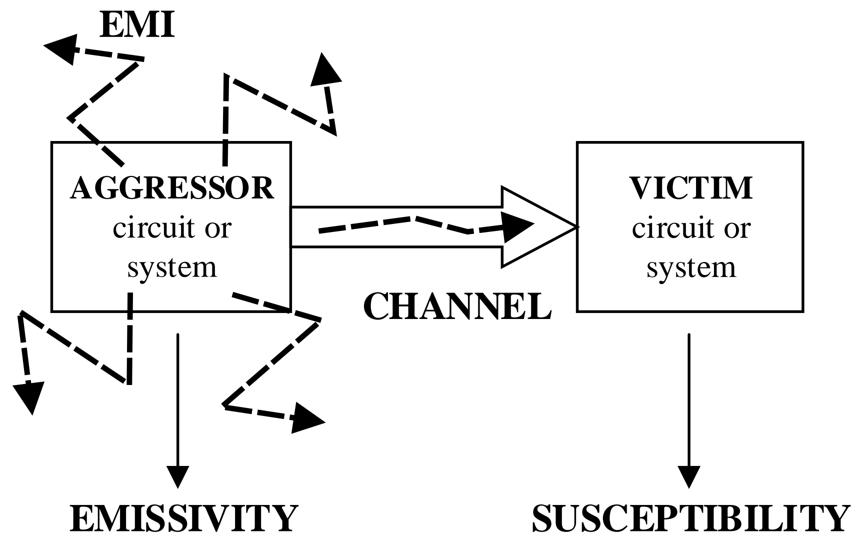

FIGURE 1.1: Electromagnetic compatibility from the aggressor (emissivity) and the victim (susceptibility) perspectives.

From the aforementioned concepts it is clear that, due to its small dimensions (short electrical length), an integrated circuit is intrinsically more robust to radiated and induced interferences as well as less prone to emit far field radiation disturbances. On the other hand, ICs can easily pick up disturbances through their connections to the PCB, so that conducted interferences are one of the most common mechanisms, which do appear dealing with EMC at chip level, either from the robustness or the emission point of view. The general rule is always to quit the aggressor and to harden the victim. However, the great variety of circumstances, under which the EMC related issue can appear, make it difficult to define broad guidelines to solve the problem. These aspects become even more important with the huge spreading of integrated electronic circuits because of the increasing complexity and number of transistors on a single chip.

Since EMC related issues are one of the most common causes of IC redesign and due to the high cost of ICs manufacturing, greater attention and focus have been dedicated to EMC at chip level in order to forecast and avoid emission or susceptibility issues in the early stages of the design. Since 1975, when the first documented paper ([5]) regarding the evaluation of the susceptibility to high frequency interferences of silicon devices has been published, EMC at chip level has become a great concern and several studies and tools have been developed in order to help IC designers to build more reliable circuits.

As a matter of fact, due to the huge amount of circuit topologies which have been developed along more than 50 years of electronics and due to continuous changes of integrated technologies, there is still a big lack of knowledge about how some categories of integrated circuits behave when subjected to electromagnetic interferences. Nevertheless, the increasing use of complex electronics in harsh EMI environments raises EMC problems for circuits which have never been designed to operate under high frequency disturbances. This is the case, for example, for offset compensated operational amplifiers.

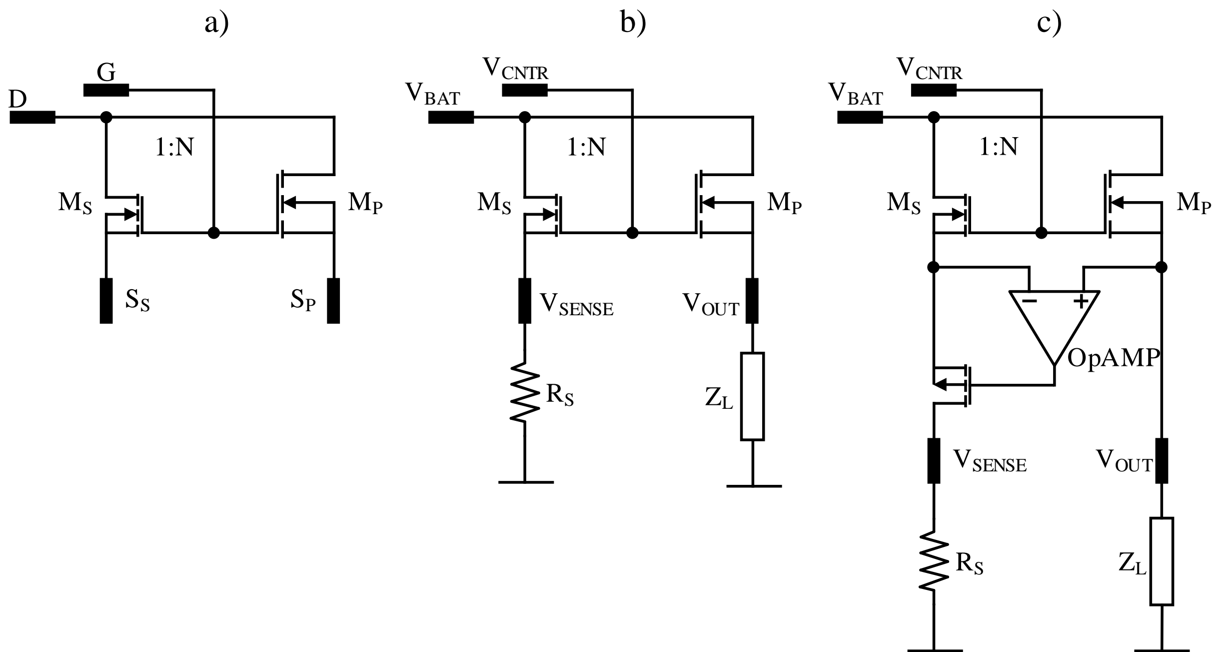

FIGURE 1.2: Current sensing concept based on power MOSFETs dimension scaling.

The operational amplifier is one of the most commonly used electronic devices. Its invention is dated back to the vacuum tubes based circuits in the late '50s. Since then it has found a huge variety of upgrades and applications. In particular, since the first vacuum tubes operational amplifiers, engineers have tried to enhance the accuracy of these devices, making them able to process smaller and smaller DC voltages or currents ([6], [7]). In other words, engineers conceived several mechanisms to compensate for the technological offset (see Chapter 2) of operational amplifiers, inventing the commonly known offset compensation techniques named chopping, auto-zeroing and correlated double sampling. While enhancing the basic principles of these offset reduction techniques, offset compensated OpAMPs started being integrated on silicon, either in their bipolar, CMOS or BiCMOS version and were produced either as off the shelf components or embedded as part of a bigger integrated circuit, reaching nowadays performances of subμV offset voltage levels ([8]). These very accurate devices are designed to be used in EMI clean environments, such as measurement apparatus or lab test benches, but nowadays the trend leads to the need of having high accuracy even while operating under highly disturbed conditions. This is the case, for example, for automotive electronics, which represents a clear connection between the aforementioned engineering topics, namely the conducted electromagnetic interferences and the low offset operational amplifiers.

The engine compartment can be a very harsh EMI environment, because the vehicle contains several km of wires that collect EM pollution from the surrounding environment, from devices used by the vehicle passengers as well as from intra engine subsystems, like spark ignition systems or high current motor drivers ([9]). The collected disturbances are then conducted to the PCBs of the vehicle and can heavily disturb the operation of the electronic devices. This fact, in combination with the heavy use and need of more and more accurate ICs for automotive

electronics, creates the basis for new emissivity and susceptibility issues which have previously not been considered. The case of ICs employed to measure electric quantities, such as load current consumption in the engine compartment, is a very good example to further clarify the aforementioned statements.

The current measurement is required to control, protect, monitor and manage the power in most of nowadays automotive applications. In [10] A. Patel and M. Ferdowsi provided a great overview of current sensing applications for automotive. Most of the current measurement approaches can be categorized as resistive or electromagnetic based. Among the formers, current sensing based on power MOSFET ([11]) is one of the most popular, because it is low cost, accurate and practically lossless. This method is based on the use of a low ohmic power MOSFET transistor (M_P) diffused on the same substrate together with an N times scaled sensing transistor (M_S) (Fig. 1.2a). The devices have the gate (G) and drain (D) terminals in common, the same length and are composed by several unit cells. The source terminals (S_S for the sense transistor and S_P for the power transistor) are separated. The ratio between the number of cells composing M_P and the number of cells composing M_S represents the width scaling N between the two devices.

To perform the current sensing operation, the resulting four terminal device can be connected, for example, as depicted in Fig. 1.2b. The drain terminal is tied to the battery line (V_{BAT} in Fig. 1.2b and Fig. 1.2c), the gate terminal is used to control the on or off state of the switch, the power MOS source is connected to the load line while the sense MOS source is connected to a sensing resistor R_S. Provided that M_P and M_S are matched, the current flowing through the sensing resistor R_S is then N times smaller than the current flowing through the load Z_L. Since the value of N is known by design, the load current can be evaluated by measuring the voltage drop across the resistor R_S, so that the load current consumption can be monitored independently from the load Z_L and the load line can be eventually interrupted in case of over current.

If higher accuracy is needed for the measurement of variable loads currents, as is usually the case for modern vehicles, the basic concept shown so far is no more sufficient, since the gate to source voltage mismatch between M_P and M_S generates an error in the scaling factor, which can become very inaccurate considering also the big difference which can exist between the sense resistor value R_S and the load value Z_L. A regulation loop is then needed in order to keep the sources of M_P and M_S virtually at the same potential and this is usually achieved by means of an operational amplifier, as depicted in Fig. 1.2c ([12]).

As demonstrated in [13], the accuracy in this topology is mostly affected by the technological offset of the operational amplifier (see Chapter 2), so that the current measurement can be further enhanced by using an offset compensated OpAMP (see Chapter 3 and Chapter 4) instead of a regular one. In EMI clean conditions, the proposed modifications can guarantee a lossless, cost effective and accurate measurement of the current flowing into any load, such as a motor coil or a bulb lamp. By looking at the schematic in Fig. 1.2c is otherwise possible to note that, because of the way the mentioned current sensing IC is connected to the automotive environment, there are several ways in which conducted electromagnetic interferences can affect the IC itself. In particular, since both input terminals of the OpAMP are connected either to the battery line (V_{BAT}) and to the load line (V_{OUT}) by means of M_P and M_S when they are in

ON state, the expected scenario is that the high frequency disturbances coming from the battery supply cable harness or collected by the cable harnesses on the load line are conducted to both negative and positive input terminals of the amplifier.

As it will be explained in Chapter 2, one of the known effects of high frequency disturbances reaching the input of an offset uncompensated OpAMP is the generation of a DC offset at the output of the OpAMP itself. This an offset is not ascribed to technological mismatches at the input stage of the amplifier, but it degrades the quality of the current measurement exactly in the same way the technological offset does. Since modern vehicles rely more and more on the on board electronic to perform even safety functions, just like the upcoming autonomous driving, the consequences of the depicted scenario can be harmful. For example, an erroneous EMI induced over current detection could lead to an interruption of the load line by switching off the power transistor M_P and this can in turn cause a shut-down of the device connected to the supply battery by means of M_P itself. It is then clear that this situation can represent a safety hazard if it happens for a device included in safety critical functions. The aforementioned case is a clear example of high accuracy operational amplifiers operating in an EMI harsh environment (see Chapter 3 and Chapter 4) and it represents the perfect scenario to justify the importance of the presented Ph.D. research.

Previous investigations, developed in the past ten years, have in fact extensively shown how the EMI induced offset is generated in standard offset uncompensated operational amplifiers ([14], [15], [16], [17], [18], [19]). Furthermore, several ways have been conceived to enhance the robustness of these standard OpAMPs in order to mitigate the generation of their offset ([19], [20], [21], [22], [23]). The present research work extends the aforementioned investigations, dealing, for the first time, with the EMI robustness of offset compensated amplifiers. The analysis of the susceptibility to conducted input EMI has been carried out for CMOS chopped OpAMPs ([24]) and for auto-zero OpAMPs, validating every achievement by means of simulation and measurements results on dedicated test chips designed for the purpose. Differently from the only previous work on the topic ([25]), the present Ph.D. research has focused, for the first time, on the relationship between the chopping frequency and the frequency of the EMI injected into the amplifier; furthermore, a particular attention has been dedicated to the comparison of the susceptibility of standard OpAMPs with respect to offset compensated ones, in order to help the design community to understand which kind of drawbacks or advantages can be expected, in terms of EMI susceptibility, moving from one category to the other. The most important research results related to the aforementioned topic in this Ph.D. thesis are published in [26], while the investigations on how to enhance the EMI robustness of chopped amplifiers are published in [27].

Furthermore, this Ph.D. research focuses also on an optimized way to evaluate the robustness of CMOS OpAMPs against input EMI by means of a dedicated simulation and measurement setup. In standard international regulations ([28], [29]) as well as in previous investigations ([30], [31] or [32]), the analysis of the test bench and measurement strategies for evaluating the robustness of ICs against conducted EMI is carried out in a broad sense, without focusing on the characteristics of the IC to be measured. The work performed about this topic during this Ph.D. research aimed at shaping the available simulation and measurement techniques to make them suitable to CMOS OpAMPs. This analysis has shown that the original

injection test setup can be greatly simplified while dealing with CMOS operational amplifiers. On the other hand, several guidelines have been provided in order to enhance the way the susceptibility of this category of ICs is evaluate, with the main purpose of finally obtaining a great correlation between simulation and measurement results, which is one of the biggest wish of every IC designer. The most important results about the aforementioned topic are published in [33], [34] and [35] and collected in Chapter 5.

EMI susceptibility of standard CMOS OpAMPs and technological offset compensation

2.1 EMI susceptibility of standard OpAMPs

In order to clarify the main results obtained at present times regarding the susceptibility of standard offset uncompensated OpAMPs, this section discusses the effects of EMI conducted at the input stage of this kind of amplifiers. To do so, previous results ([14] - [19]) are recalled and integrated with a detailed modelling of the input stage parasitics of the CMOS OpAMPs fabricated to perform the presented investigations, taking into account their layout and functional characteristics like power regime and transistors operating region. In particular, the focus is placed on low power amplifiers with the input differential CMOS stage operating in weak inversion.

2.1.1 Modelling of the EMI induced offset for standard OpAMPs

The purpose of the present section is to give an overview on the effects of electromagnetic interferences conducted to the input stage of standard offset uncompensated CMOS operational amplifiers. Although the topic has already been largely discussed in the previous works ([14] - [19]) for strongly inverted devices, it is presented here again but for low power OpAMPs whose input differential stage operates in weak inversion, like the ones designed and fabricated for the presented investigation. Furthermore, a detailed discussion on the input stage parasitics evaluation is provided taking into account the layout characteristics of the devices. Following the same approach employed in [14] and [19], the DC input referred offset voltage, induced by high frequency electromagnetic interferences conducted to the input stage of a CMOS operational amplifier (Fig.2.1), can be expressed as:

$$V_{OS_emi} = \frac{\overline{(i_1 - i_2)}_{emi}}{g_m} = \frac{i_{OS_emi}}{g_m} \tag{2.1}$$

This offset is generated by the concomitant effects of an input common mode and differential mode voltage disturbance. The differential mode disturbance causes a differential non linear current to be created in the two branches of the differential pair. The common mode input

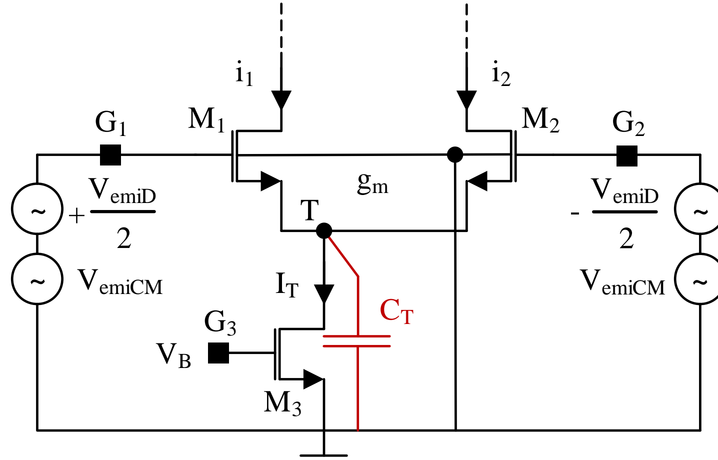

FIGURE 2.1: CMOS OpAMP input differential stage. The input disturbance $V_{emi}(s)$ is represented by its common mode (V_{emiCM}) and differential mode (V_{emiD}) components

voltage disturbance varies, through the impedance at node T (Fig.2.1), the tail bias current of the differential pair itself. Then, the simultaneous variation of the differential non linear component and the common mode component of the differential pair current generates a shift in the DC component of the differential current and, hence, of the output voltage. The parameter g_m represents the transconductance of the input differential pair and can be written, for devices operating in weak inversion, as:

$$g_m = \frac{I_T}{2\, n\, V_t} \tag{2.2}$$

The quantity I_T represents the DC tail biasing current of the input CMOS differential pair, $V_t = \frac{k_B T}{q}$ is the thermal equivalent voltage (26mV @ 300K, k_B being the Boltzmann constant, T the absolute temperature and q the electron charge), while n represents the subthreshold slope factor, a technology dependent parameter. The term i_{OS_emi} is the offset differential current generated at the output of the differential pair because of the input interference and can be written as ([14]):

$$i_{OS_emi} = \frac{g_p}{2} \cdot V_{emiDpk} \cdot V_{emiCMpk} \cdot |Y(s)| \cdot cos\left(\phi_{CM} + \angle Y(s)\right) \tag{2.3}$$

The parameters V_{emiDpk} and $V_{emiCMpk}$ represent, respectively, the differential and common mode peak voltages of the EMI disturbance that reaches the inverting and non-inverting inputs of the differential stage, while ϕ_{CM} is the phase of the common mode input disturbance. The quantity g_P arises from the second order Taylor series expansion of the output differential current i_D generated by the differential pair and it counts for the dependence of such a current from the simultaneous variations of the input differential voltage and the tail current ([15]).

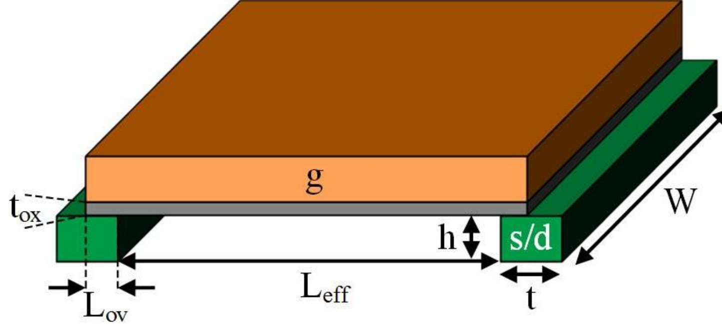

FIGURE 2.2: MOS transistor 3D sketch. The labels stand for gate (g), source (s) and drain (d). Source and drain are interchangeable for the purpose of the analysis.

For a CMOS differential pair operating in weak inversion, it is possible to express the differential current as ([36]):

$$i_D = i_1 - i_2 = I_T \, tanh(\frac{v_D}{n \, V_t}) \tag{2.4}$$

In (2.4) v_D represents the small signal component of the differential input voltage. Considering this model for the differential current and denoting by I_T the tail bias current, it is possible to calculate the parameter g_P for a differential pair in weak inversion:

$$g_P = \frac{\partial^2 \, i_D}{\partial \, v_D \, i_T}\Big|_{v_D = 0 \, , \, i_T = I_T} = \frac{1}{2 \, n \, V_t} \tag{2.5}$$

The lower case letters in (2.5) denote the small signal components of the corresponding quantities. $Y(s)$ is a transfer function which represents how the common mode input disturbances influence the tail current of the differential pair([14]):

$$Y(s) = \frac{i_T(s)}{v_{emiCM}(s)} = \frac{(2 \, g_m \, C_T) \, s}{2 \, g_m + (2 \, C_{gs} + C_T) \, s} \tag{2.6}$$

In (2.6), C_{gs} is the gate to source capacitance of the transistors M_1 and M_2, under the hypothesis that they are perfectly matched. Since these devices operate in saturation region, an estimate for the gate to source capacitance is represented by ([36]):

$$C_{gs} = W \, C_{ox} \, (L_{ov} + 0.67 \, L_{eff}) \tag{2.7}$$

In (2.7), W represents the width of the transistors M_1 and M_2, L_{ov} is the length of their gate-source overlap area (see Fig.2.2) while L_{eff} is their effective channel length, i.e. the channel physical length L minus the two gate-source and gate-drain overlap areas. The parameter C_{ox} is the silicon dioxide capacitance of the MOS structure per unit area and can be calculated as:

$$C_{ox} = \frac{k_{ox} \, \epsilon_0}{t_{ox}} \tag{2.8}$$

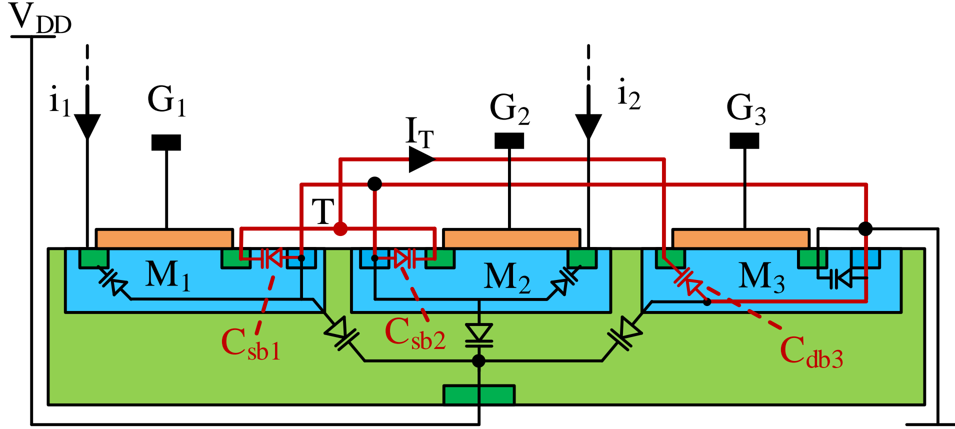

FIGURE 2.3: CMOS differential pair cross section view. Green areas represent n-doped silicon while blue areas represent p-doped silicon.The substrate is n type and it is tied to the supply voltage V_{DD}. Red connections indicate the paths from node T to any AC ground in the circuit.

Where ϵ_0 is the vacuum permittivity, k_{ox} the relative permittivity of silicon dioxide and t_{ox} the silicon dioxide thickness. Furthermore, C_T represents the total parasitic capacitance seen from the tail node T to any AC ground. Up to this point, the treatment mostly resumes what has already been studied by previous researchers, besides for the exception of the weak inversion condition of the input pair devices. Moreover, all the aforementioned parameters regarding the input differential stage can be easily evaluated by the designer, either by hand calculation or by exploiting CAD tools. On the contrary, the evaluation of the parasitic capacitance C_T has rarely been discussed, despite its importance for estimating the EMI induced offset.

A method to evaluate capacitance C_T is now presented. The cross-section in Fig.2.3 represents the view of the circuit depicted in Fig.2.1, i.e. a circuit composed of the differential nMOS pair ($M1 - M2$) and the tail nMOS transistor biased as a DC current source ($M3$), all diffused into an n type well. In the case of a ground connected bulk structure as the one in Fig.2.1, it is possible to recognize three main contributions taking part in the generation of the parasitic capacitance C_T (highlighted in red in Fig.2.3): two source-bulk pn parasitic junctions arising from M_1 and M_2, namely C_{sb1} and C_{sb2} , and the drain-bulk pn parasitic junction of the current source M_3, C_{db3}. Each one of these junctions represents a voltage dependent capacitance which concurs in generating the tail capacitance C_T:

$$C_T = C_{sb1} + C_{sb2} + C_{db3} \tag{2.9}$$

According to [36], the capacitance of a pn junction can be expressed as:

$$C_j = \frac{C_{j0}}{\sqrt{1 + \frac{V_R}{\Phi_0}}} \tag{2.10}$$

TABLE 2.1: Physical parameters

Name	Symbol	Value	Unit
Boltzmann Constant	k_B	$1.3806488\text{x}10^{-23}$	$\frac{\text{m}^2\,\text{Kg}}{\text{s}^2\,\text{K}}$
Electron Charge	q	$1.602\text{x}10^{-19}$	C
Temperature	T	300	K
Vacuum Permittivity	ϵ_0	$8.854\text{x}10^{-12}$	$\frac{\text{F}}{\text{m}}$
Silicon Relative Permittivity	k_s	11.8	
Silicon Dioxide Relative Permittivity	k_{ox}	3.97	

In (2.10), V_R represents the reverse voltage across the junction while Φ_0 is the built in potential of the junction:

$$\Phi_0 = V_t\, ln\left(\frac{N_A\, N_D}{n_i^2}\right) \tag{2.11}$$

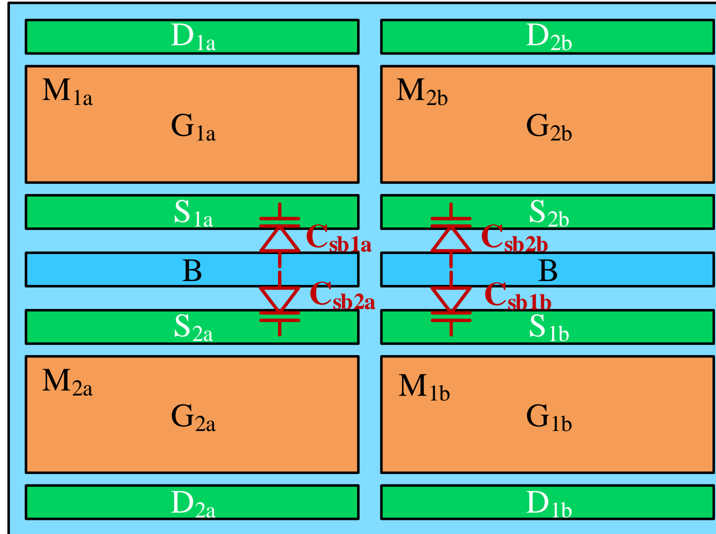

FIGURE 2.4: Input differential pair layout top view. The differential pair transistors M_1 and M_2 are split in two fingers each ($M_{1a} - M_{1b}$ and $M_{2a} - M_{2b}$) to form the square common centroid structure. This gives raise to four source-bulk capacitances: $C_{sb1a} - C_{sb1b}$ for transistor M_1 and $C_{sb2a} - C_{sb2b}$ for transistor M_2.

The quantities N_A and N_D are the technology dependent densities of acceptor and donor dopants respectively, while n_i is the density of free carriers in intrinsic silicon at thermal equilibrium. Finally, k_s is the silicon relative permittivity, C_{j0} represents the junction depletion capacitance per unit area at zero bias voltage and it can be expressed as:

$$C_{j0} = \sqrt{\frac{q\,\epsilon_0\,k_s\,N_A\,N_D}{2\,\Phi_0\,(N_A + N_D)}} \tag{2.12}$$

Table 2.1 summarizes all physical parameters employed so far and their values assigned for the numerical calculation of the parasitic capacitances. The parasitic capacitance C_T can then be calculated as:

$$C_T = A_{sb1}\,C_{j1} + A_{sb2}\,C_{j2} + A_{db3}\,C_{j3} \tag{2.13}$$

The symbols A_{sbi} and A_{dbi} represent the areas of the source-bulk and drain-bulk junctions of the transistor *i*. For a correct evaluation of the aforementioned parasitic junction capacitances

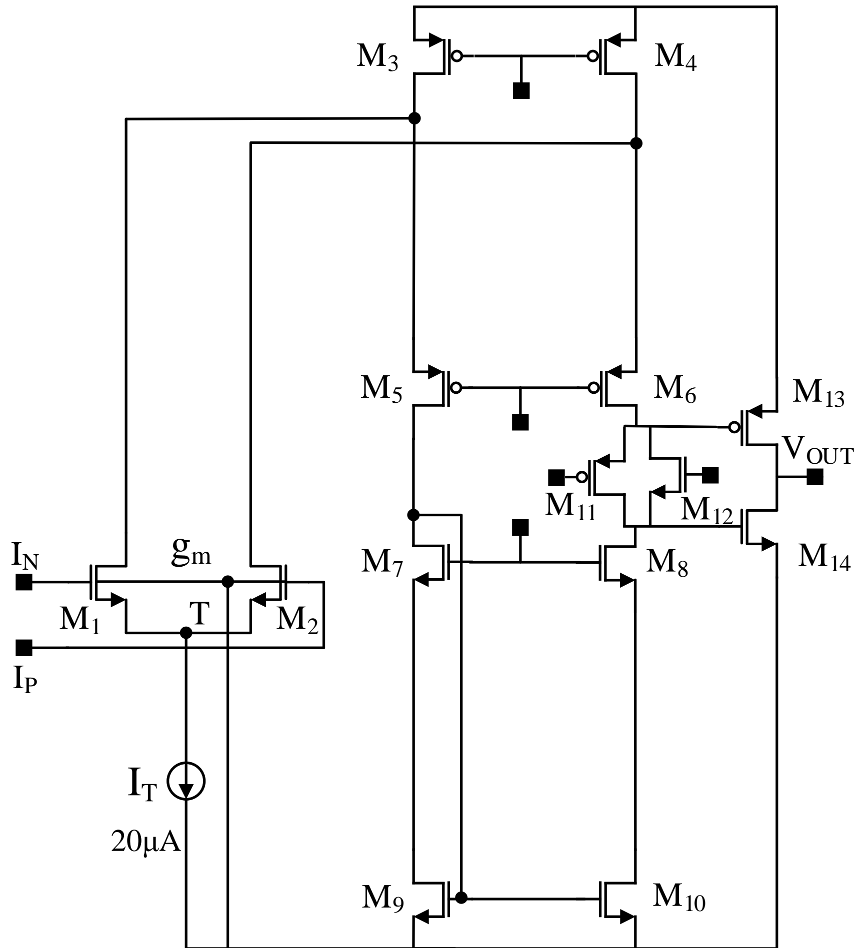

FIGURE 2.5: CMOS folded cascode OpAMP A_{CT} schematic. The biasing networks are not shown. The input differential pair is biased at $20\mu A$.

it is necessary to accurately quantify the area values. This task can only be performed looking over the layout of the differential pair.

Fig.2.4 represents the top view of the differential pair layout employed in all the amplifiers designed for the present analysis. The differential pair is layouted as a common centroid structure ([37]) to enhance the matching, each one of the transistors M_1 and M_2 has been split in two half-width devices (M_{1a}, M_{1b} and M_{2a}, M_{2b}) and distributed in a cross interleaved square structure. The area of a source-bulk junction for a single device must then be multiplied according to the number of devices employed in the centroid. The area of the source-bulk junctions for M_1 and M_2 has therefore been calculated taking into account the two source wells for each transistor. Each junction area can be calculated as the contact area between the parallelepiped shaped source or drain well and the bulk of the transistor. To clarify this aspect, Fig.2.2 represents a single n-type MOS transistor 3D sketch. For this single case, the area of the junction is:

$$A_{xb} = 2\,h_i, t_i + 2\,h_i\,W_i + t_i\,W_i \tag{2.14}$$

The variable x is either the source (*s*) or the drain (*d*) of the transistor *i*, *h* the depth of the well, *t* the length of the well and *W* the width of the transistor. Looking again at the top view of Fig.2.4, it is then possible to state that the source-bulk junction areas for M_1 and M_2 are equal and can be calculated considering four times the area of a single junction:

$$A_{sb12} = 4\,\left(2\,h_{12}\,t_{12} + 2\,h_{12}\,W_{12} + t_{12}\,W_{12}\right) \tag{2.15}$$

Where $h_1 = h_2 = h_{12}$, $t_1 = t_2 = t_{12}$ and $W_1 = W_2 = W_{12}$. For the tail transistor M_3, the area of the junction is represented by the area of a single drain well:

$$A_{db3} = 2\,h_3\,t_3 + 2\,h_3\,W_3 + t_3\,W_3 \tag{2.16}$$

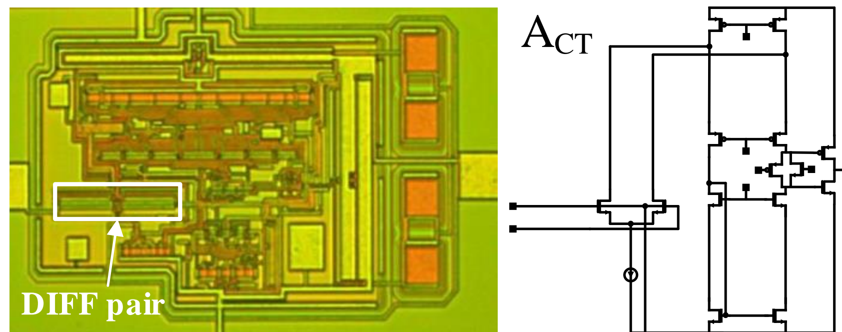

FIGURE 2.6: CMOS folded cascode OpAMP A_{CT} photomicrograph. Highlight of the nMOS input differential pair.

The reverse voltage for all three junctions C_{sb1}, C_{sb2} and C_{db3} is the same and equal to the tail node voltage V_T, hence it is possible to write that:

$$C_{j1} = C_{j2} = C_{j3} = C_j \tag{2.17}$$

Finally, for the case of the presented topologies, the total parasitic capacitance C_T can be rewritten as:

$$C_T = C_j \left(A_{sb12} + A_{db3}\right) \tag{2.18}$$

This capacitance value can be plugged into (2.6) to evaluate the EMI induced offset for whatever CMOS differential input stage connected as in Fig.2.1.

Despite its simplicity, the presented parasitic capacitances model is quite suitable for a first order estimation of the EMI induced offset in a CMOS differential pair. For these reasons, the same model is used in Chapter 3, where the evaluation of the EMI effects is performed and modelled for chopped operational amplifiers. The validation of the discussed model has been performed on a device designed and fabricated for this purpose. The device is depicted in Fig.2.5. It is a continuous time offset uncompensated folded cascode CMOS OpAMP comprising an input nMOS differential stage and a class AB output stage designed to ensure the maximum output swing and avoid distortion of the output voltage.

The device is internally connected as a voltage buffer, hence, the DC shift observed at the output as a consequence of input EMI injection directly corresponds to the EMI induced offset voltage ([38]). The picture in Fig.2.6 shows a photomicrograph of the amplifier in Fig.2.5, called A_{CT}, in order to distinguish it from the other designed amplifiers which are the topic of the following of the thesis. Looking at the sketch in Fig.2.7 it is possible to better understand the behaviour of the circuit under input EMI injection. As soon as only the DC input nominal signal is present, the output of the OpAMP matches this input, being the OpAMP configured as a voltage buffer. Once the EMI is injected at a frequency much greater than the amplifier bandwidth, the output experiences a DC shift which can then be resembled to an input equivalent offset. The graph in Fig.2.8 shows a wafer level (Chapter 5, test bench in Fig. 5.20) measurement results which validate the modelling discussed so far for the EMI induced offset of standard offset uncompensated CMOS operational amplifiers.

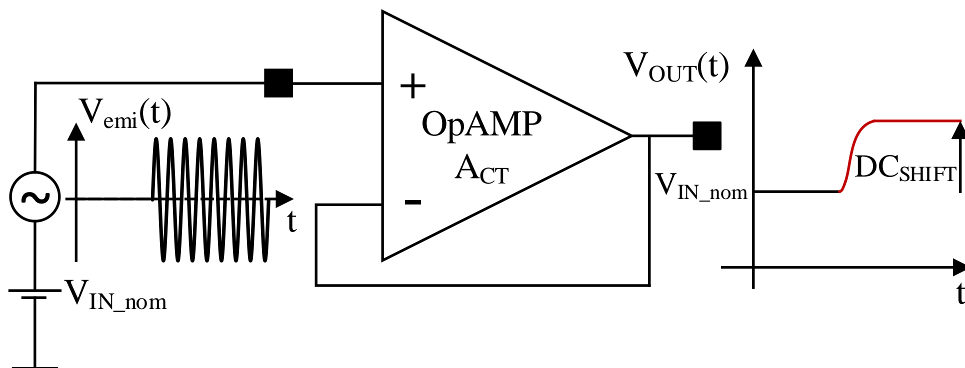

FIGURE 2.7: OpAMP A_{CT}.

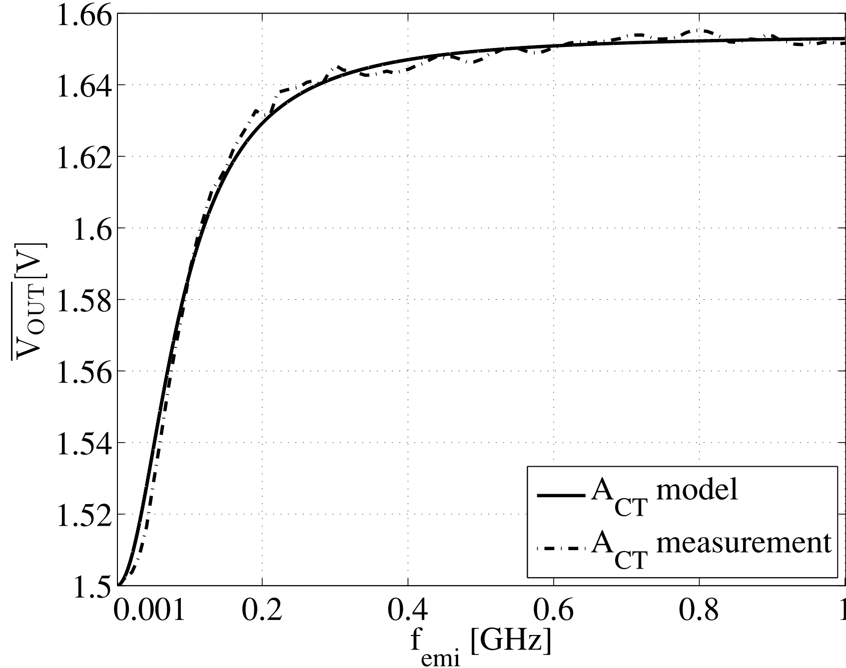

FIGURE 2.8: A_{CT} modelled (continuous line) and measured (dashed line) average output voltage with $P_{emi} = -5\text{dBm}$ ($A_{emi} \simeq 350\text{mV}_{\text{pkpk}}$). The shift of the average output voltage shows the EMI induced offset.

The graph shows the DC shift experienced by the OpAMP as a consequence of high frequency sinusoidal interferences conducted at its non inverting input pin. The nominal output of the amplifier should be $1.5V$, which is the dc voltage applied at the OpAMP input. From the plot it is possible to note that, as soon as the frequency of the input EMI becomes greater than $1MHz$, the DC value of the output ($\overline{V_{OUT}}$) deviates from $1.5V$, eventually reaching $1.65V$ for $f_{emi} = 1GHz$. As it is possible to note, despite the simplicity of the modelling of the tail capacitance C_T, the model results fit quite accurately the measurement results, provided that care is taken for the setting of the measurement test bench (Chapter 5).

2.1.2 EMI hardening of standard OpAMPs

Since the discovery of the offset generation in amplifiers because of input interferences, engineers conceived several methods to enhance the EMI susceptibility of these devices in order to make them more robust against input disturbances in terms of EMI induced offset. The techniques are here briefly described and analysed for sake of completeness, since they represent already established results in the literature.

- *Filtering*

  Filtering at the input stage of the amplifier represents by far the most common and effective EMI hardening technique. The simplest way of achieving a filter effect on the input disturbance is to insert series resistors at the gates of the CMOS differential pair ([19]), so

to build a low pass filter with these resistors and the gate to source parasitic capacitances of the input pair transistors. To enhance this effect, it is also possible to further insert ad-hoc capacitors either towards ground or between the gate and source terminals of the input pair transistors themselves ([39]). As it is possible to note from (2.6), increasing the gate to source capacitance lowers the pole frequency of the transfer function $Y(s)$, anticipating the knee after which the EMI induced offset saturates (denominator of (2.6)) and decreasing, as a consequence, the overall level of EMI induced offset after the pole frequency of $Y(s)$.

Besides these enhancements, more complex input filtering structures can be built in order to greatly improve the EMI susceptibility of the devices. This is the case of commercial EMI hardened OpAMPs designed with advanced EMI filters at the input stage ([40]). Clearly, depending on the application, the technology, the silicon area and the costs, one approach can be employed instead of the other, taking into account that the simple aforementioned input filtering techniques can be effective only to some extent and not on the whole injection frequency span. Nevertheless complex EMI input filter structures may require a very large silicon area and complex stabilization of the amplifier.

- *Linearisation*

  As it emerges from Section 2.1.1, the DC output shift generation takes place because of the non linear distortion operated by the input differential pair on the input high frequency disturbances. As a consequence, one technique which has been conceived to harden the OpAMP in terms of EMI susceptibility is the linearisation of the input differential stage. Linearisation techniques mostly intend to counteract the non linear behaviour of the input differential pair by adding another differential pair which operate in parallel with the main one. The simplest way of obtaining this effect is represented by the design of a rail to rail input stage made of a pMOS and an nMOS pairs both attached to the input ([23]).

  The offset generated by the nMOS pair and the one generated by the pMOS pair is of opposite signs and ideally cancel out at the output of the amplifier. Another technique which has been conceived is to AC couple the EMI compensation pair to the main one, in order to keep the EMI induced offset cancellation independent from the OpAMP expected input swing ([23], Section 3.3). The main limitation of this technique resides in the fact that, being the EMI offset generated from the differential pairs directly dependent on the differential pairs parasitics, the effectiveness of the technique relies on the degree of matching between the parasitics of the two pairs themselves.

  Furthermore, since the compensation pair is AC coupled to the main one, its effect starts to be noticeable only after the AC coupling network pole frequency, therefore the linearisation cannot be profitably obtained for all the EMI frequency span. As well as the linearisation techniques previously mentioned, another way of increasing the linearity of the differential pair consists in source degenerating the pair transistors ([19], [20]). Nevertheless, this approach degrades the transconductance of the OpAMP input stage and increase its input referred noise ([19]).

- *Source Degeneration and Source Buffering*

Another technique which acts on the source node of the input pair in order to decrease the amount of EMI induced offset is called source buffering ([20]). This approach implies the addition of a second differential pair which operates in parallel with the main one and bootstraps the bulk to source voltage of the main pair transistors at a constant value by forcing the common mode transfer function $Y(s)$ to zero. This technique has shown to be quite effective for the elimination of the EMI induced offset ([41]). On the other hand, as the aforementioned linearisation techniques, it forces to double the input stage area and to rely on parasitics or integrated capacitors matching.

The main outcome from the brief list of EMI hardening techniques for OpAMPs is that, as usually happens in analog circuits design, no optimal solution exists in order to enhance the EMI susceptibility of the devices, since every approach previously described has the main drawback of either decreasing the OpAMP nominal performances or increasing the manufacturing costs or die area. More importantly, all the aforementioned techniques have always been discussed for standard offset uncompensated OpAMPs, since, as already stated in Chapter 1, the use of offset compensation techniques along EMI polluted environments represents a new challenge of the upcoming applications and still need to be investigated.

2.2 EMI induced offset, technological offset and compensation techniques

The present section aims at clarifying the important differences between the EMI induced offset discussed so far and the technological offset affecting whatever kind of electronic amplifier based on a differential pair of input devices. The clarification is mandatory due to the seeming likeness of the two unwanted effects, whereas their causes are by far very different, so that the countermeasures which can be taken for one are not necessarily effective for the other.

2.2.1 Technological offset and EMI induced offset diversity

The technological offset V_{OS_tech} affecting operational amplifiers has been observed since the first vacuum tubes amplifying stage of the late '50s ([6]). Its causes mainly reside in the unavoidable mismatch of technological parameters, such as threshold voltage and gain factor ([42]) among devices which are supposed to be perfectly equal on silicon. CMOS amplifiers like the ones discussed in this Ph.D research rely on the matching of several transistor couples or arrays in order to properly operate. The main effect of technological mismatches taking place between transistors of these amplifiers is the generation of an output offset, which appears as an output voltage even if the input differential voltage is nulled. For example, the schematic in Fig.2.9 highlights the main transistor couples which concur in the technological offset generation for a standard folded cascode CMOS amplifier, like the A_{CT} presented in Section 2.1.1.

In such a case, being the OpAMP biased with a single supply voltage, the offset generation is easily observed by connecting the device in a follower configuration (Fig.2.10) and setting a

nominal input voltage. The resulting output voltage, evaluated for several manufactured samples, deviates from the nominal input one according to a Gaussian distribution which represents the technological offset of the amplifier. For this reason, the technological offset information shall be provided in terms of standard deviation (σ value).

The histogram plot of Fig.2.11 depicts, for example, the offset values measured on eleven samples of OpAMP A_{CT} connected as a voltage buffer. As discussed in the known work of M. Pelgrom ([42]), the threshold voltage (V_{th}) and gain factor (β) mismatch sigma values for a

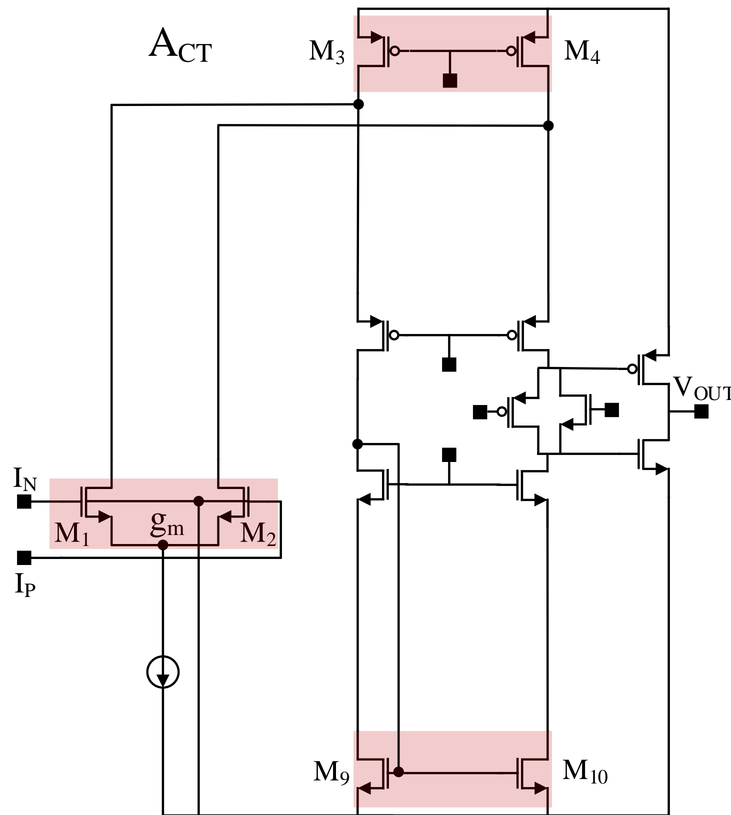

FIGURE 2.9: A_{CT} transistor pairs involved in the generation of the technological offset.

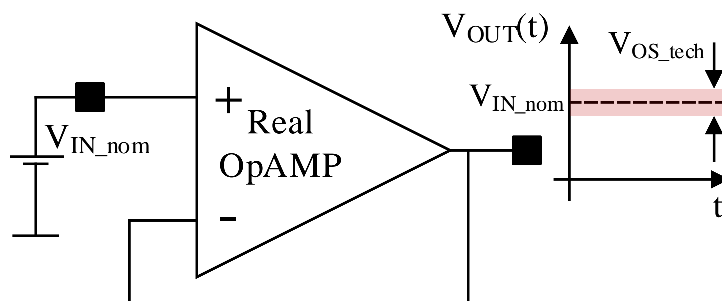

FIGURE 2.10: Technological offset observation for single supply OpAMPs.

couple of MOS transistors is inversely proportional to the square root of the devices area:

$$\sigma(V_{th}) = \frac{A_{V_{th}}}{\sqrt{W\,L}} \ ; \ \sigma(\beta) = \frac{A_{\beta}}{\sqrt{W\,L}} \tag{2.19}$$

Where $A_{V_{th}}$ and A_{β} are the technology dependent parameters and W and L the physical dimensions of the transistors. These sigma values, properly scaled according to the OpAMP transistors and gain stages, are directly linked to the sigma value of the OpAMP technological offset, which can be referred to the input and modelled as a standard DC voltage source (Fig.2.12). The technological offset V_{OS_tech} must then be considered as an intrinsic parameter of the OpAMP, so that each fabricated device is characterized by an offset value which does not depend on the characteristics of the input signal and can be considered fixed in time, although it could depend on other environmental parameters such as temperature ([43]). The EMI induced offset V_{OS_emi} has nevertheless the same effect of V_{OS_tech}, in the sense that it makes the output DC voltage of the amplifier to deviate from its nominal value. For such a reason, also V_{OS_emi} can be referred to the input of the amplifier and modelled as a DC voltage source but, differently from V_{OS_tech}, this DC voltage source value is not fixed since it directly depends on the characteristics of the interferences at the input of the OpAMP itself (Fig.2.12). Furthermore, the EMI is mixed in the input differential pair, producing, at the pair output, a DC offset differential current superimposed to and undistinguishable from the nominal differential current output from the input differential pair itself. As it will be discussed and demonstrated in Chapter 3 and Chapter 4, these considerations have an enormous impact on the way the technological offset compensation techniques handle the EMI induced offset.

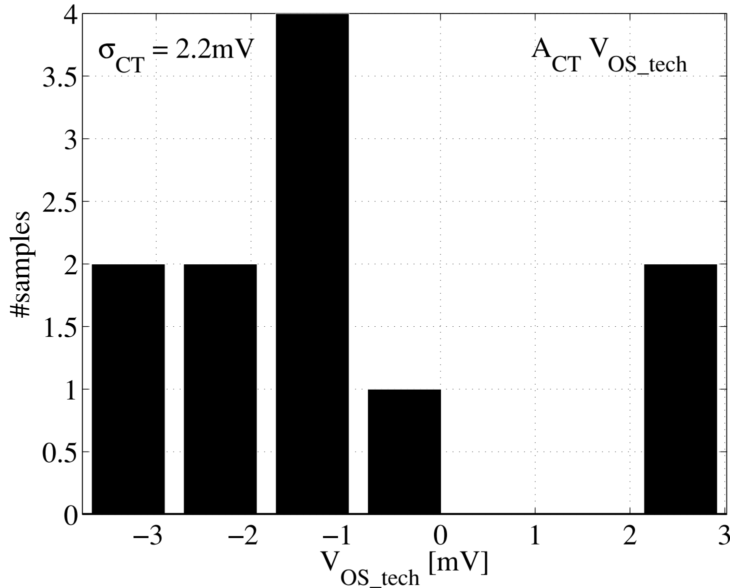

FIGURE 2.11: A_{CT} technological offset measured on 11 samples voltage buffer connected. The resulting σ value of the technological offset is $2.2mV$.

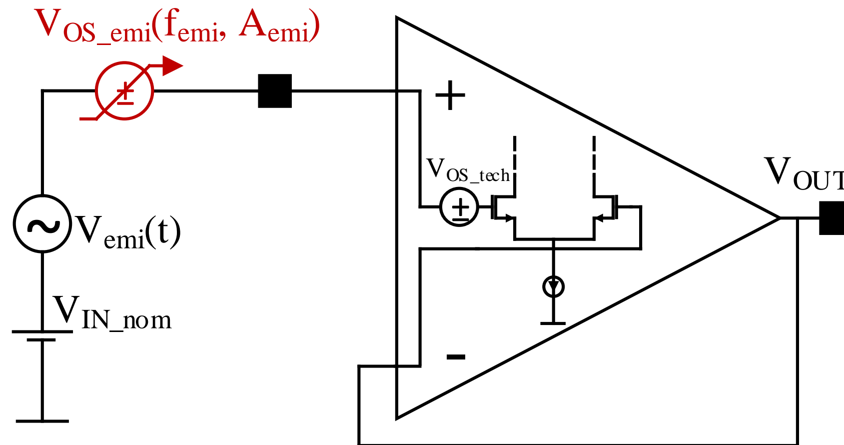

FIGURE 2.12: Technological and EMI induced offset modelling. Both are modelled as DC sources, but the picture highlights that the technological offset is an intrinsic parameter of the OpAMP and is fixed in time, while the EMI induced offset appears only in the presence of input disturbances and depends on the disturbances characteristics, like frequency (f_{emi}) and amplitude (A_{emi}).

2.2.2 Technological offset compensation techniques in EMI harsh environments

The reduction of the dynamic range in linear CMOS low voltage technology, because of the technological DC offset and low frequency noise, has pushed engineers to conceive several ways to compensate for these limitations, inventing offset compensation techniques nowadays known as chopping, autozeroing and correlated double sampling ([44]).

Since the first concept of vacuum tubes chopped amplifiers, these techniques have increased in performance, complexity and number of available topologies, eventually reaching $sub-\mu V$ levels of residual technological offset and low frequency noise ([45]). The most important aspect to point out here concerns how these concepts combine with the topic of EMC. As already spotted in Chapter 1, the need for high accuracy in EMI polluted applications, like the automotive ones, is a relatively new topic, arising from the upcoming new technologies and complex electronic systems employed in EMI harsh environments. As a matter of fact, the reader may wonder why high accuracy amplifiers are used for these applications, if the interferences reaching the devices are anyway generating, for example, a DC offset which is much higher than the target offset for the OpAMP application.

The ongoing trend, in this case, foresees a use of these devices to enhance the accuracy performance of the system they operate into, but the specifications are only expected for nominal operating conditions. The first important target that must be fulfilled is the investigation regarding whether or not such high accuracy amplifiers behave in a better or worse way with respect to their uncompensated counterparts in the presence of EMI. The understanding of this topic provides mainly two benefits. In first place, if the susceptibility of a more advanced offset compensation topology is confirmed to be the same than its standard counterpart, the designer can rely on the fact that the same countermeasures which were taken for the old version would

work also for the new highly performing one. On the other hand, a deep understanding of the mechanisms involved in the EMI susceptibility of offset compensated topologies can provide extremely useful information about how to enhance their robustness or, as a counterpart, whether it is possible to relax the protection strategies previously adopted.

EMI SUSCEPTIBILITY OF CHOPPED OPAMPS

3.1 Chopping offset compensation

The present section aims at giving a brief overview on the chopping offset compensation technique in order to provide a clear basis for the following paragraphs. Chopping is a continuous time technique which does not involve any sampling of the electric quantities. The offset and low frequency noise cancellation is based on a successive modulation and demodulation of the input signal, as sketched in Fig. 3.1.

In order to isolate the technological DC offset and the low frequency noise from the main signal, the chopping uses frequency modulation to upconvert the nominal input signal $IN(t)$ at the odd multiples of the chopping frequency before the DC offset is superimposed to the nominal input signal itself. The modulation is modelled, in Fig. 3.1, as a mixing between

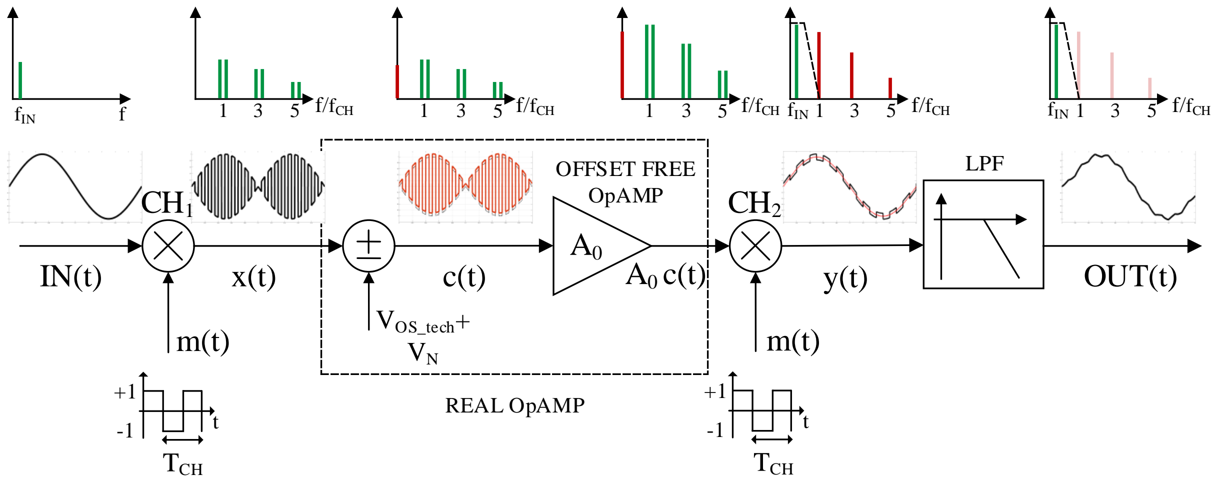

FIGURE 3.1: Concept block diagram of the chopping offset compensation technique. The input signal is considered as a sinusoidal wave at frequency $f_{IN} << f_{CH}$. In the top part of the picture, the spectral content of each signal appearing at the intermediate portions of the chopping chain is represented. The OpAMP DC gain is denoted by A_0.

the input signal and a square wave signal $m(t)$ clocked at the frequency $f_{ch} = \frac{1}{T_{CH}}$. After the first modulation performed by chopper CH_1 in Fig. 3.1 , the DC offset V_{OS_tech} and low frequency noise V_N are superimposed to the modulated signal $x(t)$, generating the corrupted signal $c(t)$. This signal is then amplified, $A_0\,c(t)$, before the output modulator CH_2. The chopper CH_2 demodulates the amplified nominal signal back to its original bandwidth, while upconverts or modulates the amplified DC offset and low frequency noise at the even multiples of the chopping frequency. This operation produces an output signal $y(t)$ whose average value corresponds to the nominal amplified input signal $A_0 \cdot IN(t)$, with a superimposed ideal square wave signal whose peak amplitude is nothing but the amplified DC offset and low frequency noise $A_0(V_{OS_tech} + V_N)$. The uncorrupted amplified signal can then be obtained, for example, by low pass filtering the output of the modulator CH_2 (signal $OUT(t)$).

Ideally, the offset cancellation should be obtained completely, so that no residual offset appears at the OpAMP output beside the one due to systematic effects and finite gain. On the other hand, chopped amplifiers suffer indeed from residual offset mainly due to impedance mismatches at the surrounding ports of the chopper modulators ([46]). As it is shown in section 3.2.3, the modulators are mostly implemented with MOS switches. Each switch delivers a channel charge every time it passes from the ON to the OFF state ([46]), so that voltage spikes are always present at the input or output of the modulator itself. If the impedances loading the modulator branches are not matched, the voltage spikes have different amplitude and time constant between the modulator lines, resulting in a residual DC component different from zero superimposed to the output signal.

3.2 Modelling of the EMI induced offset for chopped OpAMPs

This section presents the CMOS chopped OpAMP topology employed along the present investigation and clarifies the fundamental difference between the ways a chopped OpAMP handles the technological and EMI induced offset. The first main difference between the EMI immunity of chopped OpAMPs with respect to standard OpAMPs is then discussed and a broadband model of the EMI induced offset for chopped OpAMPs is derived and compared to the usual model for standard offset uncompensated amplifiers. As the chopped OpAMP is a clocked device, a mathematical model of the effects of interferences appearing at multiples of the amplifier chopping frequency is also presented.

3.2.1 Chopping against EMI induced offset in OpAMPs

The schematic in Fig. 3.2 represents the block diagram of a chopped operational amplifier while Fig. 3.3 depicts the schematic of the CMOS amplifier topology employed to perform the present investigations. The OpAMP is a folded cascode comprising the input nMOS differential pair with the bulk tied to ground (M_1, M_2), the cascode stage (M_3 to M_{10}) and the class AB output stage (M_{11} to M_{14}), designed to ensure maximum output swing in order to avoid distortion of the output voltage. The transconductance stage g_m, which represents the input differential pair, produces an output differential current proportional to the differential input voltage and is the main cause of the technological offset. The two chopper modulators CH_1 and CH_2 modulate

the technological offset to the chopping frequency f_{CH}, so to make it appear, at the output, as a ripple superimposed to the offset free amplified input signal ([44]).

The technological offset V_{OS_tech}, caused by the mismatch of the input pair MOS devices of the g_m stage, can be modelled as a DC voltage source referred to the input of the g_m stage itself. As clarified in Chapter 2, the technological offset is an intrinsic parameter of the OpAMP which does not depend on the characteristics of the input signal. On the other hand, the EMI induced offset V_{OS_emi} is strictly dependent on the characteristics of the input disturbance superimposed to the nominal signal, such as its frequency f_{emi} (through the transfer function $Y(s)$) and its amplitude A_{emi}. As a consequence, it cannot be added as a DC contribution to the technological offset and must be modelled as a separate DC input referred variable offset source.

Fig. 3.4 and Fig. 3.5 represent the same chopped OpAMP structure of Fig. 3.2 but with the device configured as a voltage follower for simplicity. The two block schematics depict the chopped OpAMP during its two phases of operation, i.e., when the chopper modulators are driven to conduct the signal directly (phase Φ_1) or to invert it (phase Φ_2). The OpAMP nominal input is modelled as a DC signal V_{IN_nom}.

The EMI induced offset V_{OS_emi} is directly related to the characteristics of the input disturbances, hence, it is modelled as an input referred source lying outside the chopping structure for both phases. Under the hypothesis that both offsets V_{OS_tech} and V_{OS_emi} are positive, (3.1) holds for the phase Φ_1 (Fig. 3.4):

$$V_{OUT}(\Phi_1) = V_{IN_nom} + V_{OS_tech} + V_{OS_emi} \tag{3.1}$$

During the phase Φ_2 the chopper modulators are switched, so that the signal path is inverted. In this condition (3.2) holds:

$$V_{OUT}(\Phi_2) = V_{IN_nom} - V_{OS_tech} + V_{OS_emi} \tag{3.2}$$

Since the voltage source that models the EMI induced offset is not located between the

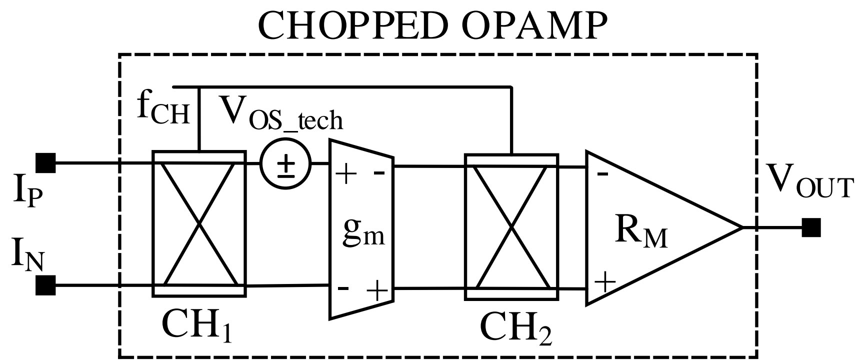

FIGURE 3.2: Chopped OpAMP block diagram. The OpAMP positive and negative inputs are denoted by I_P and I_N respectively. The input (CH_1) and output (CH_2) chopper modulators are clocked at the frequency f_{CH} and embed the transconductance stage g_m. The output transresistance stage R_M converts the differential output current into a single ended output voltage V_{OUT}.

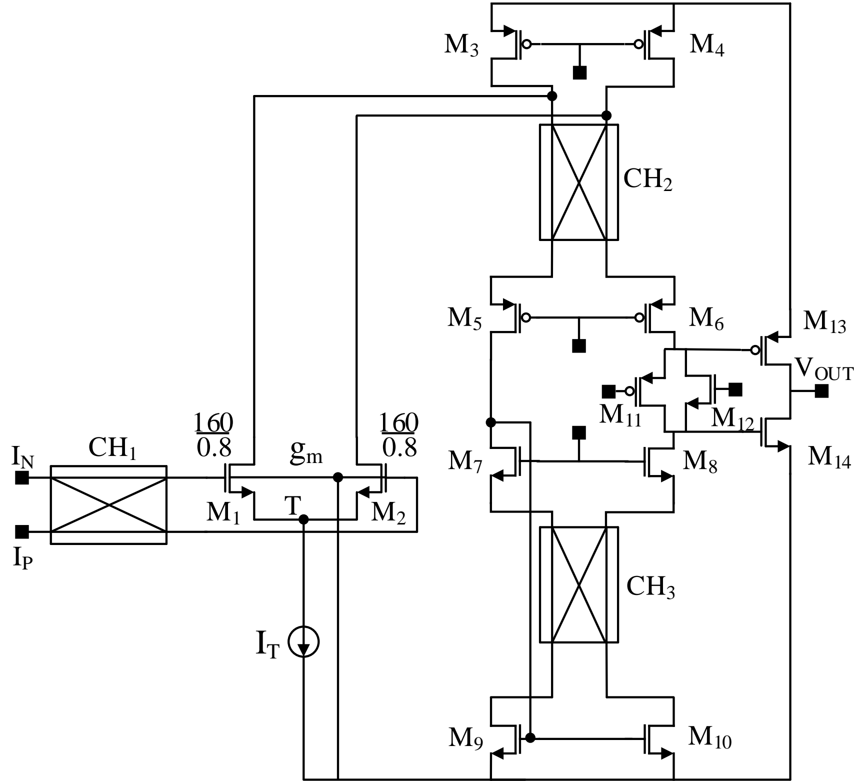

FIGURE 3.3: CMOS folded cascode chopped OpAMP schematic. The biasing networks are not shown. The input differential pair is biased at $20\mu A$ as in OpAMP A_{CT}. The transresistance stage R_M is made by transistors M_3 to M_{14}. Chopper CH_3 has been added to compensate for the technological offset generated by the mismatch of transistors M_9 and M_{10}.

two choppers CH_1 and CH_2, the offset contribution is not modulated and does not change its sign along the two chopping phases. For this reason it is possible to state that chopping cannot compensate the EMI induced offset, which will appear, at the output, as a DC contribution

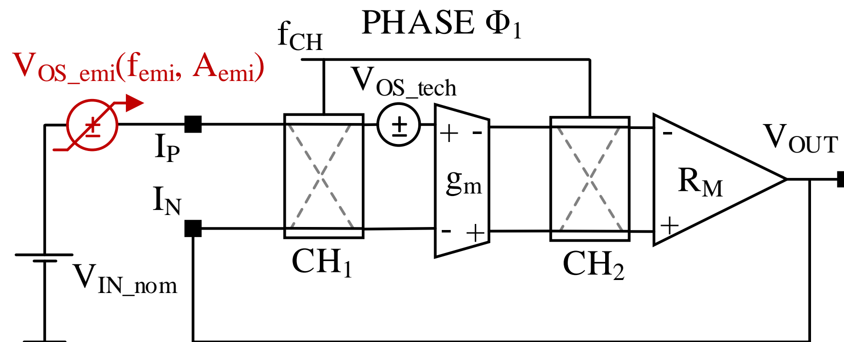

FIGURE 3.4: Chopped OpAMP in phase Φ_1. The chopper modulators are driven to directly transmit the signal.

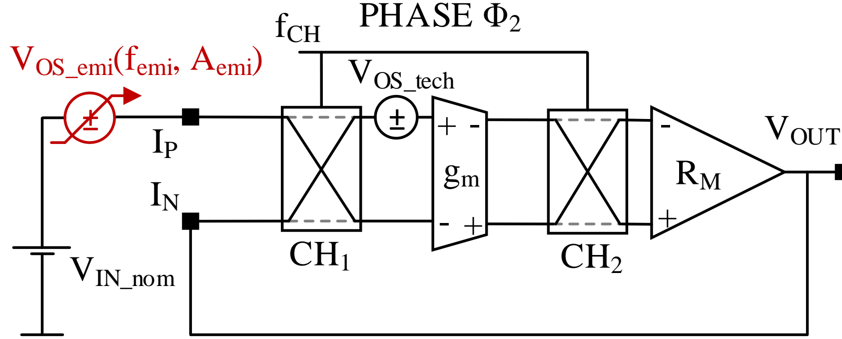

FIGURE 3.5: Chopped OpAMP in phase Φ_2.The chopper modulators are driven to invert the signal.

indistinguishable from the amplified nominal input signal. This fact has important implications. It implies that none of the known techniques, used to isolate the technological offset by subtracting it from the input stage and reducing the output ripple (called ripple reduction techniques, [43]), can be employed to isolate or manipulate the EMI induced offset because it is already superimposed to the nominal amplified input signal.

3.2.2 Broadband immunity of chopped OpAMPs against EMI

This section is dedicated to the analysis of broadband effects observed for CMOS chopped OpAMPs subjected to high frequency input disturbances. From a topological point of view, the most important difference between the input stage of a standard CMOS amplifier and the input stage of a chopped amplifier is the presence of the input modulator, named CH_1 in Fig. 3.2 and Fig. 3.3 and depicted in Fig. 3.6 in three possible topologies, depending on the device used as a switch (namely nMOS, pMOS or transmission gate switches). Neglecting every possible parasitic capacitance of each switch and making the hypothesis that each switch is operating in its linear region, the first order way of modelling the switches is to take into account their on-resistance R_{ON}. This resistance is caused by the channel when the MOS transistor is operating in deep triode region at zero current and can be expressed, in first approximation, as ([36]):

$$R_{ON} = \frac{1}{\mu C_{ox} \dfrac{W}{L} (V_{gs} - V_{th})} \tag{3.3}$$

In (3.3), μ represents the mobility of free charges (μ_n in case of electrons for nMOS transistors or μ_p in case of holes for pMOS transistors); W and L are, respectively, the width and length of the MOS switch, V_{gs} is the gate-source voltage experienced by the switch when it is on and V_{th} is the switch threshold voltage. In the case of a transmission gate based switch, the parasitic on-resistance is then the parallel combination of the nMOS R_{ON} and the pMOS R_{ON}. Independently from the chopping phase, the input differential pair will then always be connected in series to one of the two couples of closed switches, thereby experiencing a series R_{ON} at the gate of the input stage transistors M_1 and M_2 (see Fig. 3.7, example for nMOS based switches). Because of this, the input disturbances are attenuated by the filtering effect of

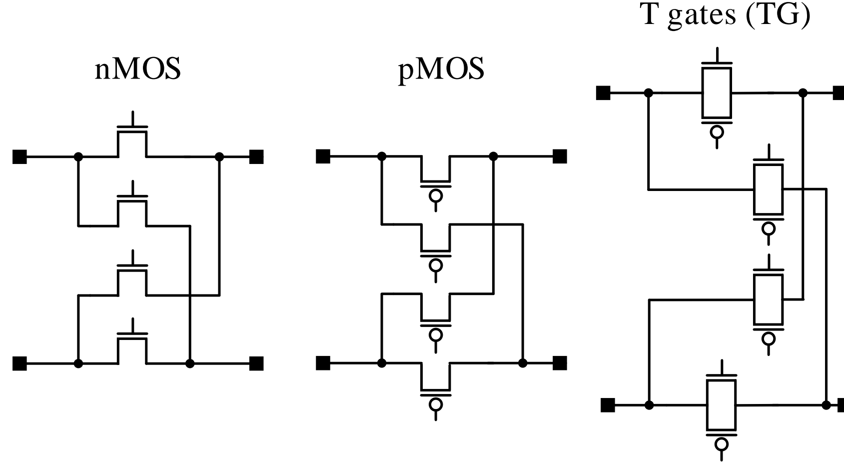

FIGURE 3.6: Chopper modulator topologies. The modulator can be composed either by nMOS only, pMOS only or transmission gates (parallel nMOS-pMOS) switches depending on the voltage level expected at the switch heads.

the resistance R_{ON} together with the input parasitic gate-source capacitances of M_1 and M_2, so that a smaller amount of differential and common mode disturbances reach the gates of the differential pair transistors.

The circuit in Fig. 3.8 depicts a small signal model of the differential pair in one of the two chopping phases, taking into account the on-resistance of the switches that are activated. In order to correctly evaluate the EMI induced offset in this condition, the model discussed in Section 2.1.1 must be modified to take into account the effect of R_{ON} on the differential input disturbances (V_{emiD}) reaching the MOS pair as well as the way the common mode disturbances (V_{emiCM}) influence the tail current. To do so, the transfer function $Y(s)$ from (2.6) can be modified so that it takes into account both effects. The new transfer function Y_{CH}(s) takes the form:

$$Y_{CH}(s) = \frac{1}{1 + s\,R_{ON}\,C_{gs}} \cdot \frac{(2\,g_m\,C_T)s}{(R_{ON}\,C_{gs}\,C_T)\,s^2 + (2\,C_{gs} + C_T)\,s + 2\,g_m} \tag{3.4}$$

As it is possible to note from (3.4), $Y_{CH}(s)$ is composed of two terms. The first one takes into account the attenuation of the differential component of the input disturbance over frequency, while the second one, similar to the original $Y(s)$, takes into account the common mode component of the input disturbance affecting the tail current $i_T(s)$. If R_{ON} is nulled, the expression of Y_{CH}(s) returns to the original $Y(s)$. The plot in Fig. 3.9 shows both transfer functions $Y(s)$ and Y_{CH}(s) in magnitude and phase. As it is noticeable from the plots, the two functions coincide at low frequencies, whereas the modulus of $Y_{CH}(s)$ decreases as the filtering effect of the input modulator starts to show up, indicating an attenuation of the EMI induced offset over frequency.

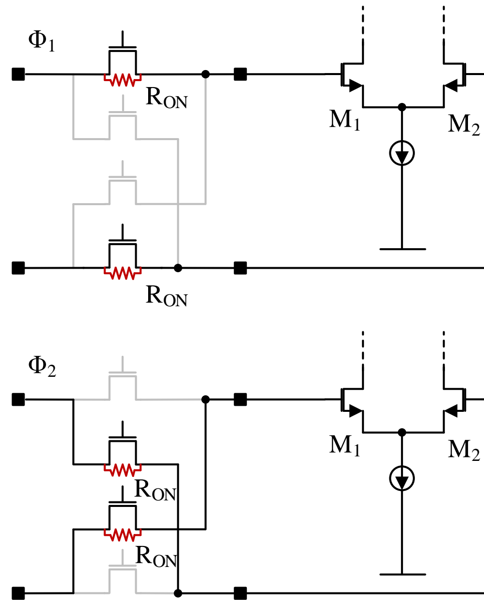

FIGURE 3.7: Input chopper modulator phases in relation with the differential input stage (example for nMOS switches). Highlight of the switches parasitic on-resistance R_{ON} connection in the two chopping phases Φ_1 and Φ_2.

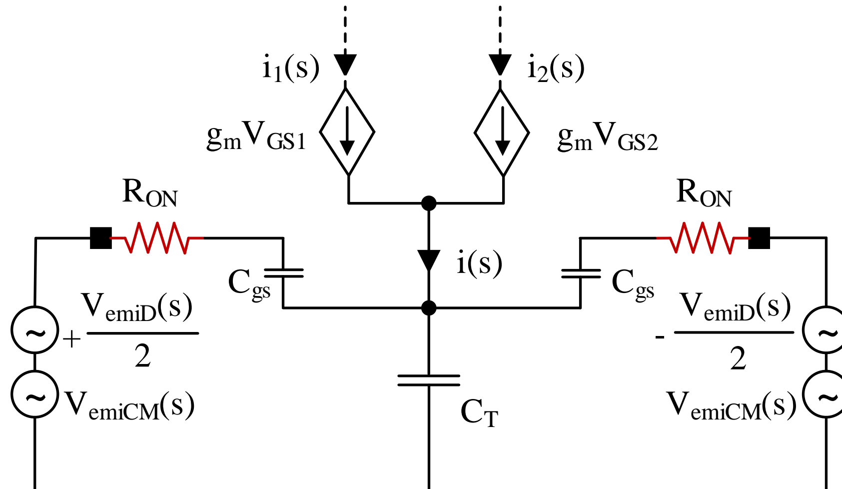

FIGURE 3.8: Differential pair with input chopper small signal model. The input disturbance $v_{emi}(s)$ is represented by its small signal common mode ($v_{emiCM}(s)$) and differential mode ($v_{emiD}(s)$) components.

The expression of Y_{CH}(s) can be plugged into (2.3) to obtain the desired model for the EMI induced offset current (3.5) and, consequently, for the EMI induced offset voltage (3.6)

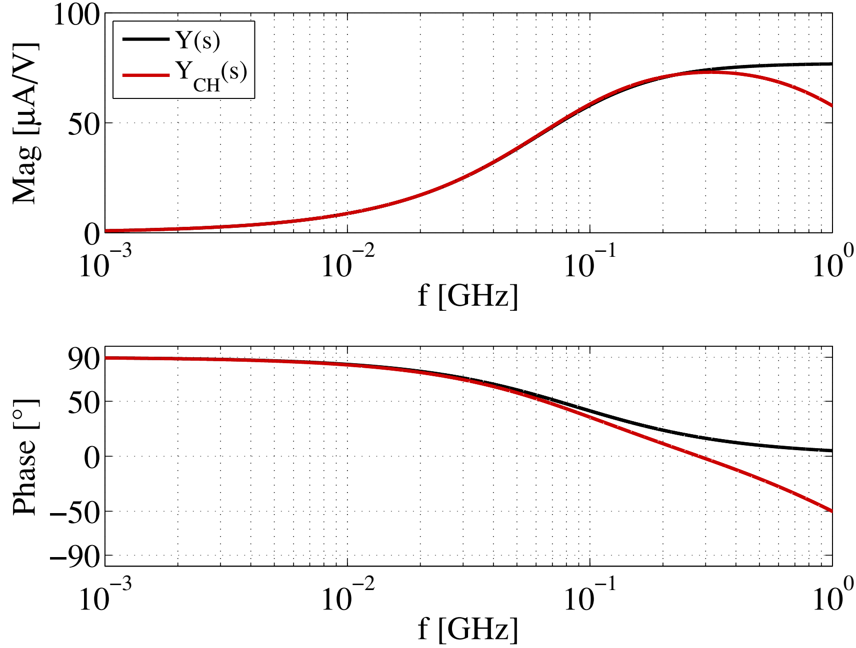

FIGURE 3.9: $Y(s)$ and $Y_{CH}(s)$ transfer functions comparison in magnitude and phase. The magnitude of $Y_{CH}(s)$ starts decreasing after 300MHz in the example.

affecting chopped operational amplifiers:

$$I_{OS_CHemi} = \frac{g_p}{2} V_{emiDpk} V_{emiCMpk} |Y_{CH}(s)| \cdot cos\left(\phi_{CM} + \angle Y_{CH}(s)\right) \tag{3.5}$$

$$V_{OS_CHemi} = g_m I_{OS_CHemi} \tag{3.6}$$

It is important to point out that model (3.4) considers the switch in on-state as a linear resistor and it does not take into account the switch nonlinearity. In real application devices design, if nominal voltages close to the positive (negative) rail are expected at the OpAMP input, pMOS (nMOS) switches are used in the input modulator, while transmission gate switches are usually employed when a rail to rail input range is needed. For this reason the model limitation does not nullify the results, because the input modulator topology is always chosen in order to keep the modulator switches far from their nonlinear region.

3.2.3 Effects of EMI present at multiples of the chopping frequency

In Section 3.2.2 the broadband behaviour of chopped OpAMPs subjected to input conducted interferences has been discussed. Since the chopped OpAMP is a clocked device, this section shows how the input disturbance influences the DC value of the amplifier output when the EMI frequency f_{emi} beats at multiples of the chopping frequency f_{CH}.

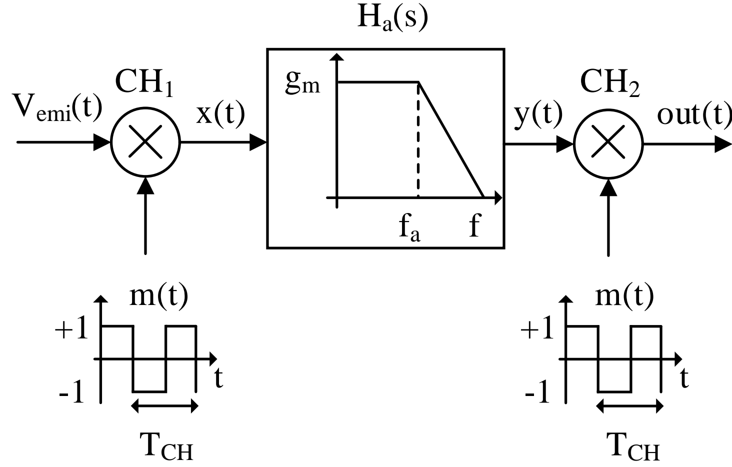

FIGURE 3.10: Voltage-Current transfer function model between input and output choppers. The input is only constituted by the EMI signal for simplicity. This voltage interference ($V_{emi}(t)$) is modulated once by chopper CH_1, becoming the signal $x(t)$, then it is fed to the block $H_a(s)$, that represents the g_m stage connected to the output transresistance stage R_M, becoming a differential current signal $y(t)$ which is then modulated again by chopper CH_2 and converted to a single ended output voltage represented by $out(t)$.

To ease this analysis, a functional block diagram of a chopped OpAMP is depicted in Fig. 3.10. As for Fig. 3.1, the chopper modulators are modelled as mixers which multiply the incoming signal by a square wave whose period is $T_{CH} = \frac{1}{f_{CH}}$. The functional block $H_a(s)$ models the frequency response of the circuit which is surrounded by the modulators in the specific OpAMP topology. With the aid of Fig. 3.11 it is possible to recognize that this block comprises the transconductance stage g_m loaded by the cascode stage (M_3 and M_4) and by the second modulator CH_2 in the actual CMOS OpAMP.

Denoting by v_{I_P} and v_{I_N} the small signal components of the voltages at the positive and negative inputs of the amplifier, the differential current driven by the g_m stage and fed to the cascode stage can be written as:

$$i_D = i_1 - i_2 = g_m\,(v_{I_P} - v_{I_N}) = g_m\,v_D \tag{3.7}$$

The current i_D experiences, at each phase, a load composed of the parallel of the parasitic capacitance at the nodes P_1 and P_2 and the resistance of the MOS switches of the chopper modulator CH_2 in series with the source impedance of the cascode devices M_5 and M_6, resulting then in the output current:

$$i_{oD} = i_{o1} - i_{o2} \tag{3.8}$$

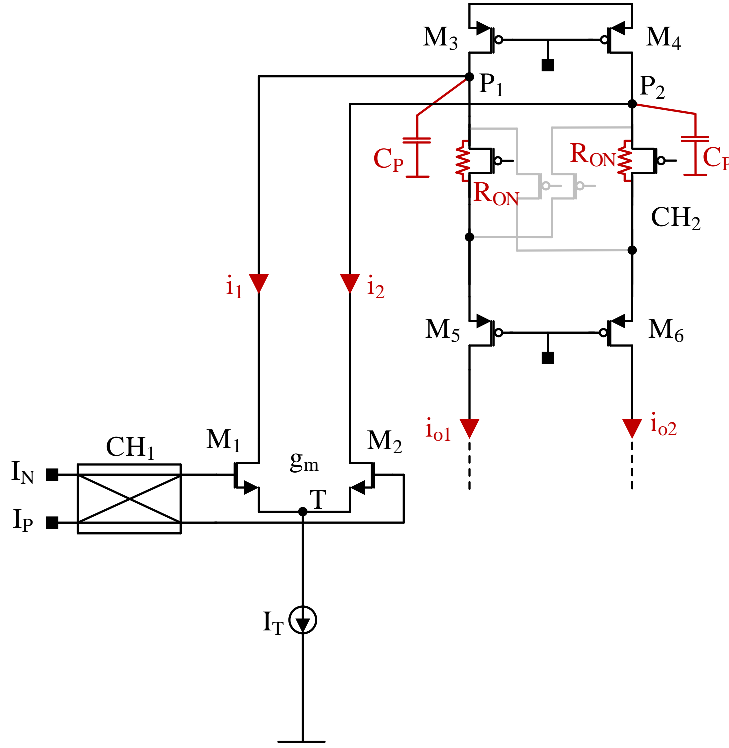

FIGURE 3.11: Components comprising the voltage-current transfer function in the folded cascode chopped OpAMP. The circuit between the choppers CH_1 and CH_2 defines the voltage-current transfer function $H_a(s)$. Since the chopper CH_2 is embedded into the cascode stage, its effect has to be included in the evaluation of the frequency response of the stage during the conversion of the input differential voltage into an output differential current.

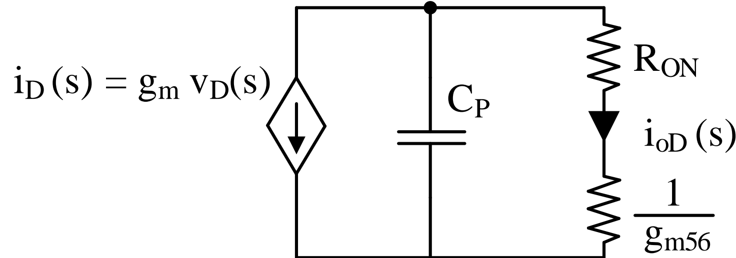

FIGURE 3.12: Model of the voltage-current conversion part of the chopped folded cascode depicted in Fig. 3.11. The bandwidth limitation arises at the generation of the output differential current i_{o_diff} from the input differential current i_{diff} through the impedance composed of R_{ON}, $\frac{1}{g_{m56}}$ and C_P.

The circuit in Fig. 3.12 depicts the model of the aforementioned part of the folded cascode amplifier. The voltage to current transfer function of the block can be expressed as:

$$H_a(s) = \frac{i_{oD}}{v_D} = \frac{g_m}{1 + s\,C_P\left(R_{ON} + \frac{1}{g_{m56}}\right)} \tag{3.9}$$

In (3.9) g_{m56} represents the transconductance of transistors M_5 and M_6 (Fig. 3.3 and Fig. 3.11) and it is assumed that $C_{P1} = C_{P2} = C_P$. The circuit part between the input and output choppers can then be modelled as a single pole low pass system with DC gain g_m and cut-off frequency:

$$f_a = \frac{1}{2\,\pi\,C_P\left(R_{ON} + \dfrac{1}{g_{m56}}\right)} \tag{3.10}$$

This modelling justifies the choice of the transfer function block $H_a(s)$ depicted in Fig. 3.10. In order to intuitively demonstrate what happens to the signals along the path of Fig. 3.10, Fig. 3.13 and Fig. 3.14 depict all these signals in the case of an EMI frequency odd multiple (3 MHz, Fig. 3.13) and even multiple (2 MHz, Fig. 3.14) of the chopping frequency, which is set at 1 MHz. To simplify the analysis, the quantities on the y axis of the plots are dimensionless. The modulated interference $x(t)$ is linearly distorted by the transfer function $H_a(s)$, resulting in the signal $y(t)$, but the main difference lies in the average value of the output signal $out(t)$ in the two cases.

If f_{emi} is an odd multiple of the chopping frequency (Fig. 3.13), the resulting signal after the output modulator CH_2 is distorted symmetrically with respect to its average value, hence it will not cause any DC shift at the output of the amplifier, i.e. it will not cause any additional offset. On the other hand, if f_{emi} is an even multiple of f_{CH} (Fig. 3.14), the demodulation of the disturbance produces an output signal $out(t)$ whose mean value is not null. As a consequence, a DC shift of the output voltage occurs and an equivalent output offset is produced by the input interference superimposed to the nominal signal.

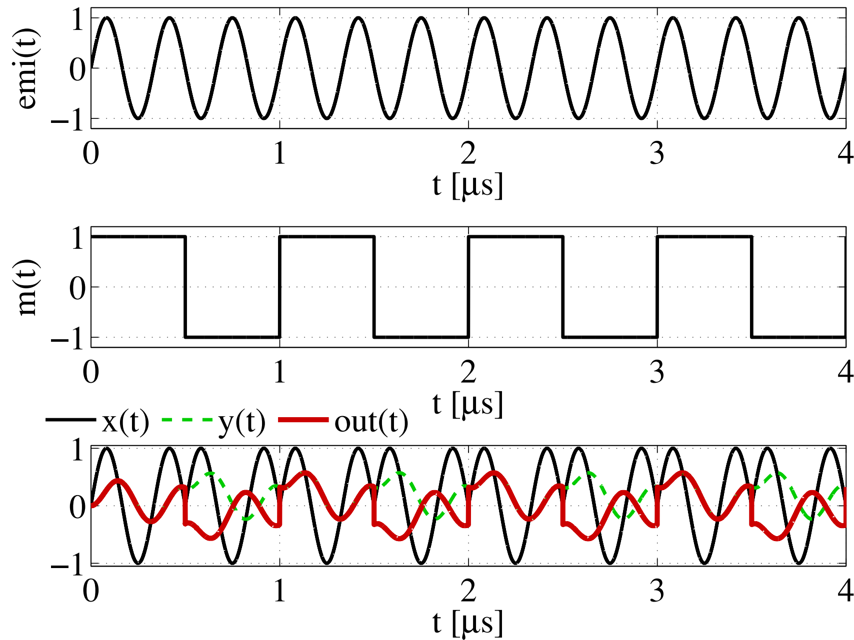

FIGURE 3.13: Simulation of the chopped system with f_{emi} (3 MHz) odd multiple of f_{CH} (1 MHz). The output, highlighted in red, has a null average.

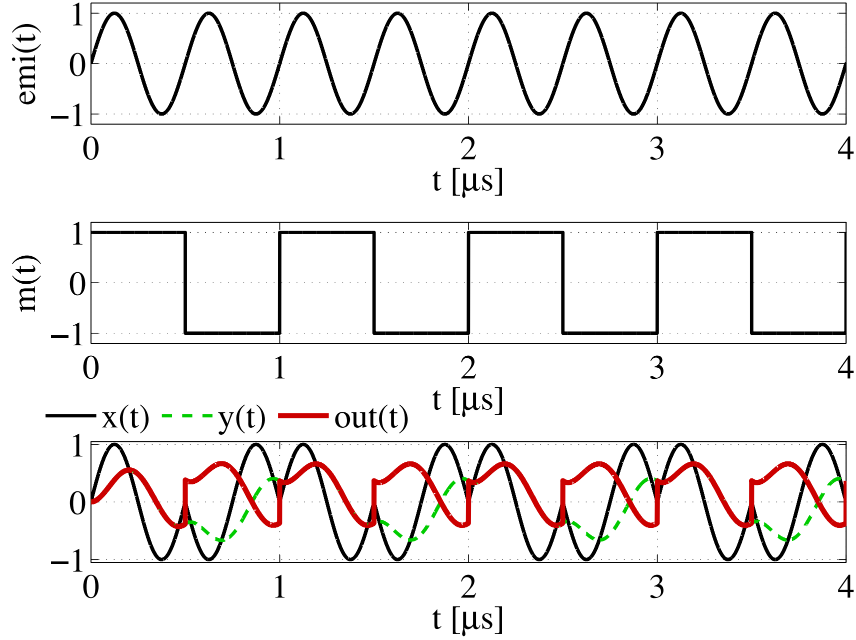

FIGURE 3.14: Simulation of the chopped system with f_{emi} (2 MHz) even multiple of f_{CH} (1 MHz).The output, highlighted in red, has a non-null average.

This DC shift, called V_{OS_L}, is ascribed to the linear distortion experienced by the input disturbances because of the voltage-current transfer function between the input and output chopper modulators. Linear distortion is that kind of distortion produced by a linear system, like a low pass filter, which handles different input frequencies in different ways. It has not to be confused with the nonlinear distortion, which is ascribed to the nonlinear characteristic of a device or circuit (like the quadratic behavior of MOS transistor) and is the responsible of the EMI induced offset in OpAMPs as discussed in Chapter 2. The offset produced in this case must be distinguished from the EMI induced offset mentioned in Section 2.1.1 and ascribed to the nonlinear distortion ([47]) caused by the input differential pair, regardless of the presence of the input and output chopper modulators. The mathematical expression of V_{OS_L} can be formalized using the aid of Fig. 3.10, for which it is possible to define the following signals:

$$V_{emi}(t) = A_{emi}\, sin(2\,\pi\, f_{emi}t + \phi_{emi}) \tag{3.11}$$

$$h_a(t) = \frac{1}{\tau_a} e^{-\frac{1}{\tau_a}} \tag{3.12}$$

$$m(t) = \sum_{n=-\infty}^{+\infty} R_{\frac{T_{CH}}{2}} \left[\left(t - n\,\frac{T_{CH}}{2} \right) (-1)^n \right] \tag{3.13}$$

$$x(t) = V_{emi}(t)\, m(t) \tag{3.14}$$

$$y(t) = x(t) * h_a(t) = (V_{emi}(t)\, m(t)) * h_a(t) \tag{3.15}$$

$$out(t) = y(t)\, m(t) = [(\, V_{emi}(t)\, m(t)\,) * h_a(t)]\, m(t) \tag{3.16}$$

In previous expressions, A_{emi}, f_{emi} and ϕ_{emi} are respectively the peak amplitude, the frequency and the phase of the input disturbance $V_{emi}(t)$. The function h_a(t) is the impulse response of the voltage-current transfer function defined in (3.9) while $\tau_a = 1/(2\pi f_a)$ is the time constant associated to the transfer function cut-off frequency f_a. The signal $m(t)$ is a square wave which represents the chopping clock and is defined by the rectangular function $R(t)$ with the period T_{CH}. Finally, $out(t)$ is the amplifier output caused only by input disturbances. Since the quantity of concern is the mean or DC value of the output, (3.16) must still be averaged to express the actual output offset V_{OS_L} caused by linear distortion:

$$\overline{out(t)} = V_{OS_L} = \frac{1}{T_{out(t)}} \int_0^{T_{out(t)}} out(t)\, dt \tag{3.17}$$

In (3.17), $T_{out(t)}$ denotes the period of signal $out(t)$. The exact expression for $\overline{out(t)}$ can be calculated in the time domain by making some hypotheses in order to simplify the analysis. The first hypothesis is to consider only f_{emi} as a multiple of the chopping frequency f_{CH}. This simplification limits the flexibility of the analysis, but it is necessary in order to get a closed form for the expression of the output DC shift. Since f_{emi} is a multiple of f_{CH}, the output voltage is then periodic with period T_{CH} and its average value can be written as:

$$\begin{aligned} \overline{out(t)} = V_{OS_L} &= \frac{1}{T_{CH}} \int_0^{T_{CH}} out(t)\, dt \\ &= \frac{1}{T_{CH}} \int_0^{T_{CH}} [(V_{emi}(t)\, m(t)) * h_a(t)]\ m(t)\, dt \end{aligned} \tag{3.18}$$

Expression (3.18) is a circular convolution which can be calculated in closed form with the aid of a further approximation, that is considering a fixed phase relation between the input disturbance and the chopping clock. This simplification can be limiting for the analysis but it is necessary to obtain a straightforward calculation in a simple closed form. The solution of (3.18) leads to:

$$\begin{aligned} \overline{out(t)} &= V_{OS_L} \\ &= S\,[cos(\phi_{emi}) + sin(\phi_{emi})]\,[cos(\pi\, M) + 1] \end{aligned} \tag{3.19}$$

In expression (3.19) M represents the ratio between the EMI frequency and the chopping frequency:

$$M = \frac{f_{emi}}{f_{CH}} \tag{3.20}$$

The coefficient S is expressed by the following equation:

$$S = A_{emi} \frac{4\,\pi\, f_{emi}\, f_{CH}}{\frac{1}{\tau_a^2} + (2\,\pi\, f_{emi})^2} \frac{1 - e^{-\frac{T_{CH}}{\tau_a}} - 2\, e^{-\frac{T_{CH}}{2\,\tau_a}}}{1 - e^{-\frac{T_{CH}}{\tau_a}}} \tag{3.21}$$

The most important aspect to note concerns the cosine term containing the parameter M in (3.19). As a matter of fact, the value of V_{OS_L} nulls for odd values of M, while it is different from zero for even values of M, since:

$$cos(\pi M) + 1 \begin{cases} = 0 \; for \; M \; odd \\ \neq 0 \; for \; M \; even \end{cases} \tag{3.22}$$

The plot in Fig. 3.15 shows a simulation result for V_{OS_L} calculated according to the model (3.19) and expressed as a percentage of the EMI peak to peak amplitude $2\,A_{emi}$:

$$V_{OS_L\%} = \frac{V_{OS_L}}{2\,A_{emi}}\,100 \tag{3.23}$$

The simulation has been obtained by sweeping the value of M in the range 1-22 and the EMI phase ϕ_{emi} from $0°$ to $360°$. The plot shows that the offset generated by linear distortion is null for f_{emi} odd multiple of f_{CH}, while it appears for EMI frequencies even multiples of the chopping frequency, with a positive or negative sign depending on the EMI phase and reaching 5% to 7% of the EMI peak to peak voltage. As f_{emi} increases, the DC shift experienced by

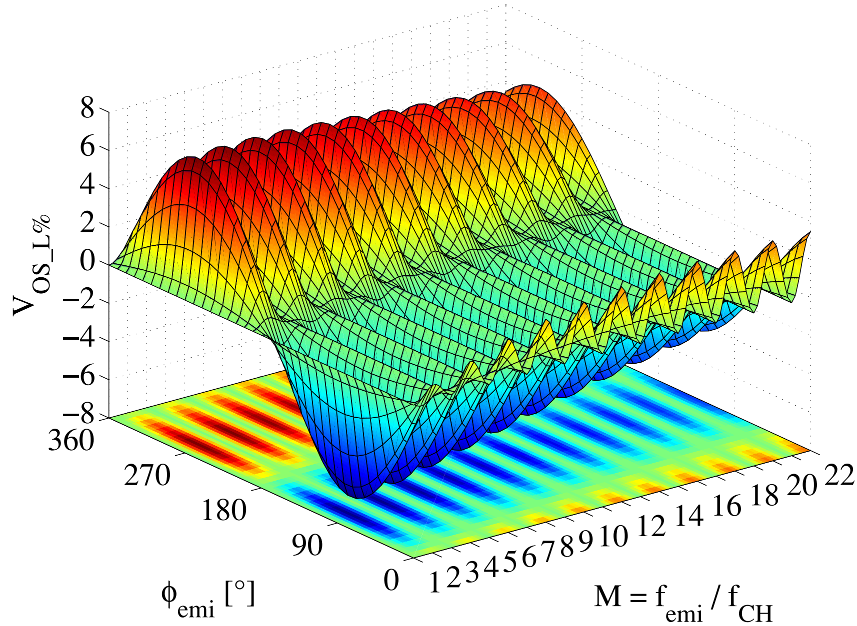

FIGURE 3.15: Model (3.19) result for V_{OS_L}. The value of f_a is set to $18 f_{CH}$.

the output at even multiples of the chopping frequency is gradually attenuated by the low pass filtering effect of the voltage-current transfer function itself.

The obtained results show that EMI injected at the input of chopped amplifiers can produce an output DC shift when the EMI frequency beats at even multiples of the chopping frequency, whereas no DC variations of the output are experienced when f_{emi} appears at odd multiples of f_{CH}. Nevertheless, since the calculation of the linear distortion DC shift V_{OS_L} can be carried out, in closed form, only by considering a fixed phase relation between the interference signal and the chopping signal, no unique expression can be written to quantify the DC shift in all the possible cases. Furthermore, the calculation is provided only for EMI frequencies multiples of the chopping frequency. Although no information is given for each intermediate EMI frequency, simulation results confirm that EMI frequencies which are not multiples of the chopping frequency produce a DC shift which lays in between the peaks produced by the even multiples of the chopping frequency itself. On the other hand, guidelines can be given to IC designers to be aware of this phenomenon and to mitigate it, as described in Section 3.2.4.

3.2.4 Models validation and design insights

This section is dedicated to the analysis of the measurement results and the comparison of these results with the models proposed in Sections 3.2.1, 3.2.2 and 3.2.3. To perform the models validation, three different operational amplifiers have been designed, layouted and fabricated in a $0.35\mu m$ low voltage proprietary CMOS technology. The first amplifier, already presented

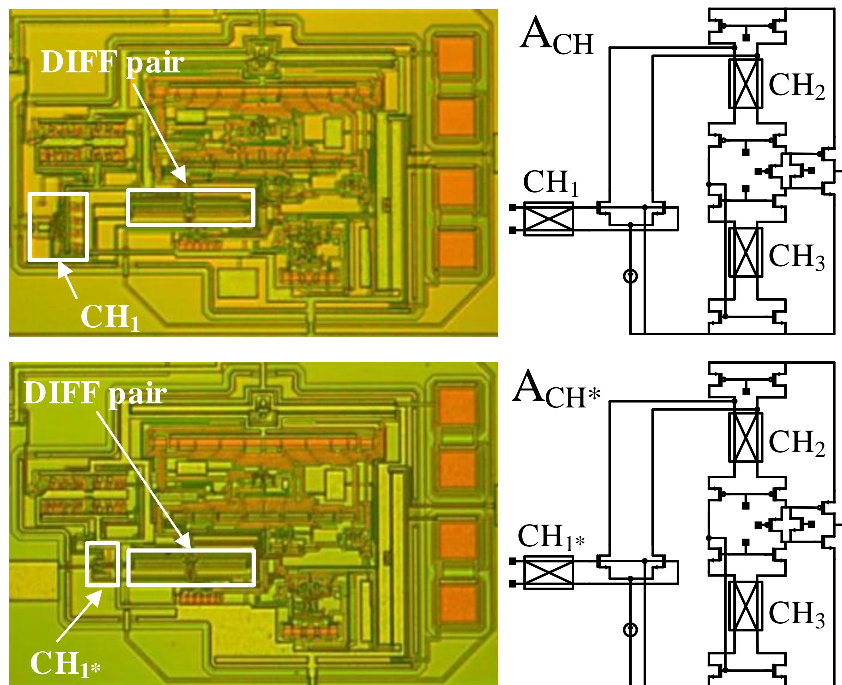

FIGURE 3.16: OpAMPs photomicrographs and schematics. Highlights of the input cross coupled differential pairs and the input chopper modulators CH_1 (TG switches based) and CH_1* (pMOS switches based).

TABLE 3.1: OpAMPs Performance parameters

OpAMP	$I_{DD}[\mu A]$	$GBW[MHz]$	$PM[°]$	DC Gain [dB]
A_{CT}	104	9.8	72	107
A_{CH}	106	9.6	67	107
A_{CH*}	105	9.5	66	107

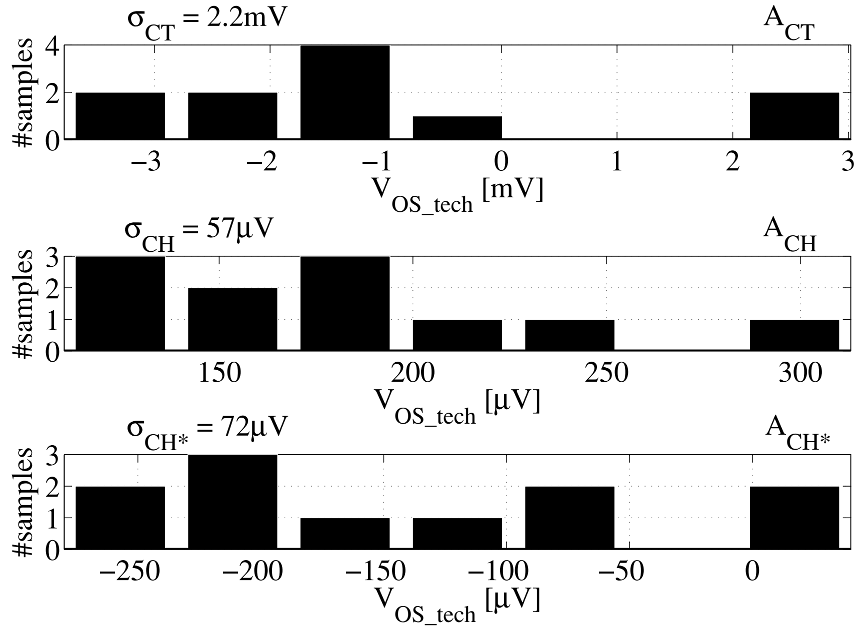

FIGURE 3.17: Measured technological offset V_{OS_tech} for OpAMPs A_{CT}, A_{CH} and A_{CH*}.

in Chapter 2, is a continuous time folded cascode OpAMP (Fig. 2.5 and Fig. 2.6) called A_{CT}. The second amplifier A_{CH} is a chopped folded cascode (Fig. 3.3) characterized by exactly the same design parameters of the amplifier A_{CT}, like device dimensions, bias currents and layout. This amplifier has been equipped with three chopper modulators. The input modulator CH_1 is made of transmission gate switches to ensure maximum input swing and linearity. The output modulator CH_2 is made of pMOS switches since it experiences voltage levels close to the positive power supply. The modulator CH_3 is made of nMOS switches since it experiences voltage levels close to the ground rail. The third amplifier A_{CH*} is again a chopped folded cascode identical to A_{CH} but with the difference of being equipped with an input chopper modulator CH_1* made of pMOS switches instead of transmission gate switches.

Both chopped amplifiers are clocked at the frequency $f_{CH} = 1.12\text{MHz}$. The photomicrographs of the chopped OpAMPs A_{CH} and A_{CH*} together with the relative schematics are shown in Fig. 3.16. All the amplifiers are supplied at $3V$ and have been designed so that the differential pair operates in weak inversion region, with a total DC current consumption for

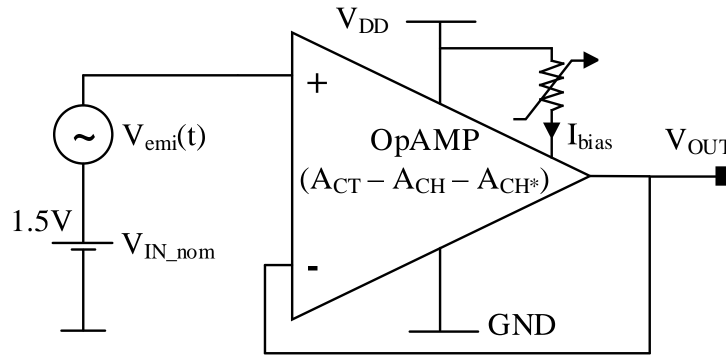

FIGURE 3.18: Conceptual drawing of the EMI injection test on the OpAMPs. Each device is buffer connected and externally biased through a potentiometer. The disturbances are injected and superimposed to a DC nominal input signal of 1.5V.

each OpAMP slightly greater than 100μA. Since the amplifiers are internally connected as voltage buffers, the DC shift observed at the output as a consequence of the input EMI injection directly corresponds to the EMI induced offset voltage ([38]). The OpAMPs have been first tested for their correct operation in nominal conditions. Table 3.1 describes the functional performance and parameters of the amplifiers, while the histogram plots in Fig. 3.17 show the measured offset standard deviation values for 11 samples of A_{CT} (same results from Fig. 2.11), A_{CH} and A_{CH*} respectively. As it can be noted from the plots, A_{CT} experiences a the standard deviation of the offset of 2.2mV, as expected since it has no embedded offset compensation mechanisms. On the contrary, chopped OpAMPs A_{CH} and A_{CH*} show two orders of magnitude offset reduction thanks to the chopping, experiencing a σ of 57μV and 72μV, respectively.

According to the standard regulation for the EMI immunity evaluation against conducted interferences ([29]), the three devices have been subjected to input single tone conducted electromagnetic interferences up to 1 GHz and an EMI power level from -5 dBm to a maximum of -2 dBm, which corresponds to a $1V_{pkpk}$ continuous voltage wave at the input of the amplifiers.

In order to record the DC shift experienced by the devices as a consequence of the EMI injection, the average value of the OpAMPs output voltage has been measured for each injected EMI frequency f_{emi}. In order to avoid spurious effects due to packaging or test board parasitics, the majority of the following immunity tests has been performed at wafer level, injecting the disturbances, biasing and measuring the electric quantities by means of ground-signal-ground (GSG) probes landing directly on the die pads ([24]). To this purpose, a dedicated ground structure has been layouted around the integrated OpAMPs (see Section 5.3).

A conceptual drawing of the injection test is represented in Fig. 3.18 while Fig. 3.19 shows a block diagram of the test bench. For the sake of the EMI susceptibility analysis, only modulators $CH_{1(*)}$ and CH_2 have to be taken into account, since the modulator CH_3 is only used to compensate for the offset due to the mismatch of the bottom cascode nMOS transistors (M_9 and M_{10} in Fig. 3.3) and does not play any noticeable role in affecting the EMI susceptibility of the OpAMPs.

The plot in Fig. 3.20 demonstrates the concept exemplified in Section 3.2.1. The graph shows two curves representing the output average voltage of amplifier A_{CH} affected by the injection of continuous wave disturbances superimposed to the nominal DC input voltage. The difference between the two curves resides in the fact that in one case (dashed line) the chopped amplifier is clocked, so that the chopper modulators are switching and the chopping offset compensation is activated. In the other case (continuous line), the amplifier is not clocked, so that the chopper modulators are stuck in one phase. As it is possible to note from the graph, the two curves are practically the same, confirming that there is no difference for the EMI induced offset if the amplifier modulators are clocked or not. This fact demonstrates that the chopping cannot modulate the EMI induced offset.

For the injection test performed on A_{CH} with the chopping mechanism inactive, the modulators have been toggled on purpose one time during the measurement, between 200 MHz and 250 MHz. The toggling of the modulators demonstrates that the small difference existing between the two curves is, in fact, the technological offset V_{OS_tech}. The curve describing the output of the non-clocked OpAMP shows, at the beginning, a negative technological offset, since it lays below the curve representing the output of the clocked amplifier. After the single toggle of the modulators the offset becomes positive and remains constant.

The plot in Fig. 3.21 compares the model and the measurement results for the output DC shift produced by EMI injection at the input of a continuous time offset uncompensated

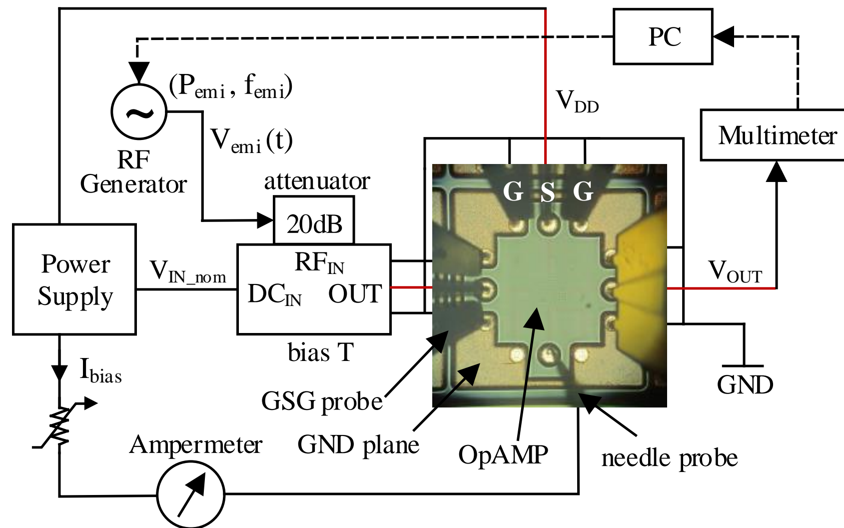

FIGURE 3.19: Wafer level EMI injection test bench (see Section 5.3). The test is automated through a software routine which sets, at the radio frequency (RF) generator side, the power level (P_{emi}) and the frequency (f_{emi}) of the interference at each step (Fig. 5.25a). The bias T decouples the DC path (V_{IN_nom}) from the AC path ($V_{emi}(t)$) while the attenuator counteracts for the reflections appearing along the injection path because of impedance mismatches (Section 5.2.2). The ampermeter monitors the current I_{bias} used to bias the amplifier and the chopping clock generator while the multimeter acquires and averages the output voltage of the OpAMPs.

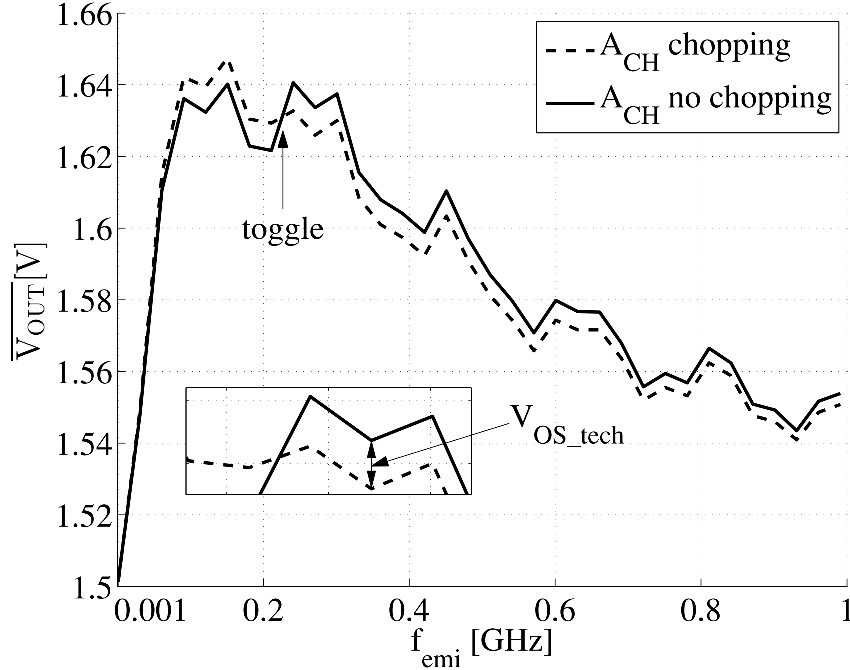

FIGURE 3.20: A_{CH} output average voltage during the immunity test, with chopping active and inactive. The deviation from the input nominal voltage of 1.5V is ascribed to the EMI induced offset as a consequence of the disturbance injection at $P_{emi} = -4\text{dBm}$ ($A_{emi} \simeq 400\text{mV}_{\text{pk}}$). The EMI injection frequency step is 50 MHz. The inset shows the difference between the two curves due to the technological offset V_{OS_tech} ($\simeq 5mV$). The immunity test is performed at PCB level.

OpAMP (A_{CT}) and a chopped OpAMP (A_{CH}). As can be noted from the curves, the models fit the measurements quite accurately, validating the main concepts highlighted in Section 3.2.2.

The standard continuous time CMOS folded cascode amplifier A_{CT} experiences the EMI induced offset, as predicted by the model recalled and refined in Section 2.1.1, showing an output DC shift which increases and then saturates according to the transfer function $Y(s)$. On the other hand, the EMI induced offset experienced by the chopped OpAMP A_{CH} follows a trend similar to the offset experienced by the standard OpAMP A_{CT} up to 100 MHz, then it is attenuated by the filtering effect of the input chopper modulator CH_1 according to the model (3.6) expressed by the transfer function $Y_{CH}(s)$.

To further highlight the filtering effect of the input modulator, a third measurements curve representing the DC shift experienced by the amplifier A_{CH*} has been plotted in Fig. 3.22 and compared to the one experienced by OpAMP A_{CH}. In this case the input DC nominal voltage V_{IN_nom} has been set to 2V instead of 1.5V in order to ensure high linearity and low resistivity of the pMOS based switches of the modulator CH_1*. Differently from the previous plots and in order to enhance the difference between the two results, the curves in Fig. 3.22 directly show the offset values (V_{OS_emi}) at the output of the two amplifiers instead of their average output

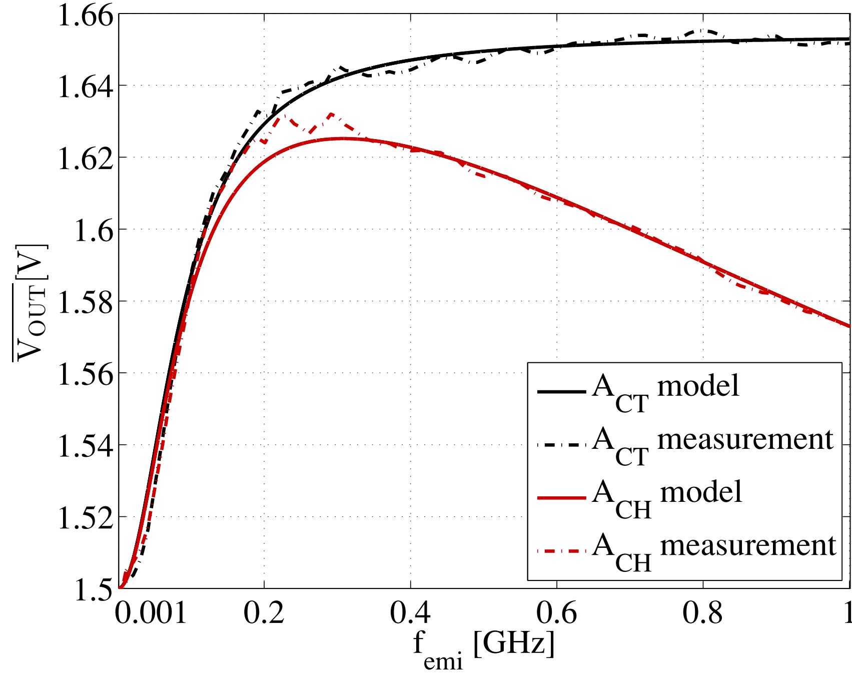

FIGURE 3.21: A_{CT} and A_{CH} modelled (continuous line) and measured (dashed line) average output voltage with $P_{emi} = -5dBm$ ($A_{emi} \simeq 350mV_{pk}$).The EMI injection frequency step is 10MHz. The amplifier A_{CH} is clocked and the chopping offset compensation is active. The immunity test is performed at wafer level.

voltage. These offset quantities have been calculated as:

$$V_{OS_emi} = \overline{V_{out}(t)} - V_{IN_nom} = \overline{V_{out}(t)} - 2V \tag{3.24}$$

The offset induced in A_{CH*} is lower ($\simeq$ 100mV less) with respect to the one induced in amplifier A_{CH}, although both are chopped OpAMPs with the same transistors dimensioning, bias currents and layout. For EMI frequencies greater than 100 MHz, the filtering effect of the input modulator shows up but it is more pronounced for A_{CH*} than for A_{CH}. The reason is the greater on-resistance of the pMOS switches ($R_{ON_P} \simeq 3.2k\Omega$) forming the input modulator CH_{1*} of A_{CH*} with respect to the on-resistance of the transmission gate switches ($R_{ON_TG} \simeq 1.4k\Omega$) of modulator CH_1 in A_{CH}. Although, in this case, the input DC nominal voltage is set to 2V in order to maintain the CH_{1*} switches in their linear region, it is possible to observe that the EMI induced offset of A_{CH*} does not decrease linearly with frequency as the one produced in A_{CH}, but it tends to increase again and saturate after 600 MHz, according to the model described in [48]. Nevertheless, the plot demonstrates that the EMI susceptibility of chopped OpAMPs is deeply affected by the input modulator structure.

The plot in Fig. 3.23 highlights the DC shift (V_{OS_L}) caused by linear distortion in chopped amplifiers when the disturbance frequency hits the multiples of the chopping frequency, as predicted by the model developed in Section 3.2.3. The curve shows how the input EMI frequency f_{emi} hitting the even multiples of f_{CH} (1.12MHz) generates a DC shift at the output of the OpAMP A_{CH} and how the DC shift is superimposed to the baseline EMI induced offset

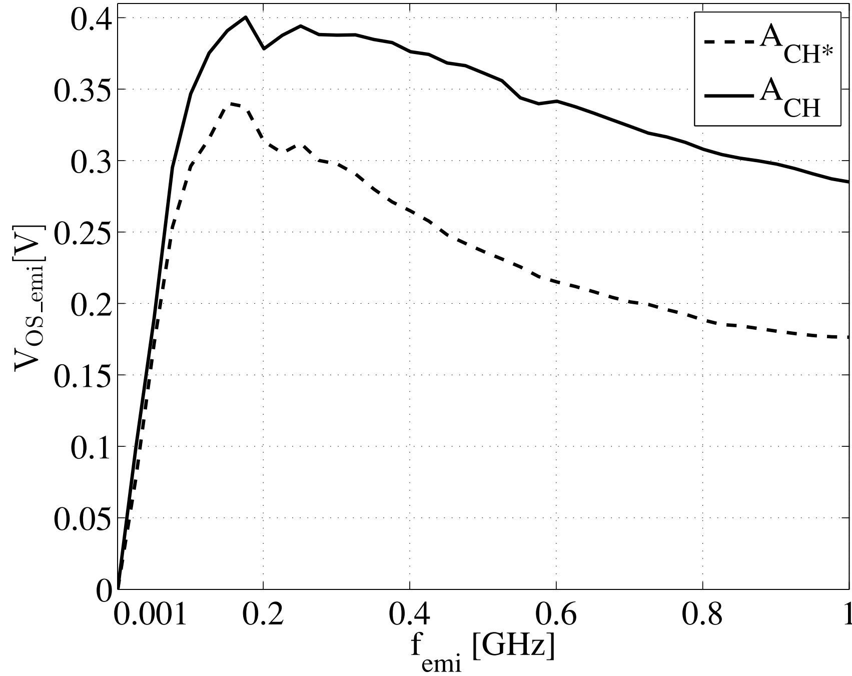

FIGURE 3.22: A_{CH} (continuous line) and A_{CH*} (dashed line) measured EMI induced offset with $P_{emi} = -2dBm$ ($A_{emi} \simeq 500mV_{pk}$) and an EMI injection frequency step of 10 MHz. To mitigate nonlinearity effects of chopper CH_1* the OpAMPs input nominal DC voltage is set to 2V. The immunity test is performed at wafer level.

ascribed to nonlinear distortion.

The output modulator CH_2 of OpAMP A_{CH} is equipped with pMOS transistor switches whose on-resistance is estimated to be approximately $2.5k\Omega$, while the cascode transistors (M_5 and M_6 in in Fig. 3.6 and Fig. 3.11) loading the modulator are characterized by a transconductance of nearly 60μS. According to (3.10), the pole frequency f_a of the voltage-current transfer function $H_a(s)$ for the amplifier A_{CH} is evaluated at $20MHz \simeq 18f_{CH}$, if the parasitics capacitances C_{P1} and C_{P2} are estimated in the range of $400fF$. Furthermore, as stated in Section 3.2.3, the offset caused by linear distortion in chopped OpAMPs mainly affects the lower part of the injection bandwidth, since it is gradually reduced by the low pass filtering of the amplifier itself. For this reasons, the injection measurement depicted in Fig. 3.23 has been performed up to a maximum EMI frequency of 22 MHz.

The condition $f_a \simeq 18f_{CH}$ is the same at which the model simulation in Fig. 3.18 has been performed. The maximum value of $V_{OS_L\%}$, predicted by the model simulation example is 7%. The peaks appearing in the measurement results of Fig. 3.23 (50mV to 70mV positive and negative) exceed 6% of the injected EMI amplitude voltage ($1V_{pkpk}$), showing a good agreement with the model, which provides then a useful tool in order to understand which parameters are involved in the generation of the linear distortion induced offset V_{OS_L}.

In particular, a smaller bandwidth of the transfer function $H_a(s)$ generates a greater linear distortion of the current signal generated by the differential pair and consequently a higher

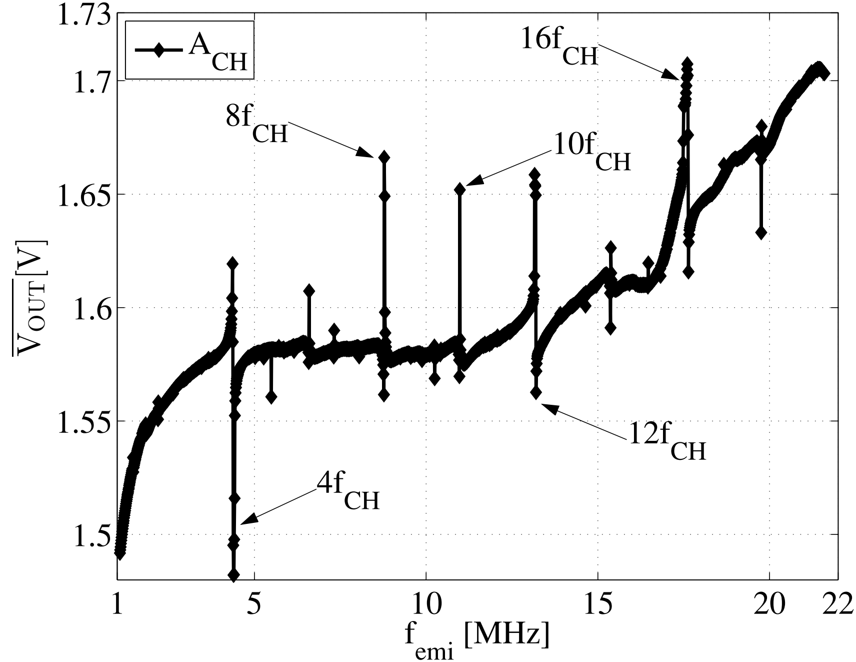

FIGURE 3.23: A_{CH} measured average output voltage with $P_{emi} = -2dBm$ ($A_{emi} \simeq 500mV_{pk}$) and an EMI injection frequency step of 10KHz. The DC shift experienced by the output voltage because of nonlinear distortion (V_{OS_CHemi}) is visible as a baseline shift with superimposed offset peaks due to linear distortion (V_{OS_L}). The immunity test is performed at wafer level.

DC shift of the output of the amplifier for f_{emi} being an even multiple of f_{CH}. As a matter of fact, V_{OS_L} can be mitigated by keeping the bandwidth (f_a) of the voltage-current transfer function between the input and output modulators as large as possible. This task is achieved by mitigating the parasitic capacitance C_{P1} and C_{P2} through transistor dimensioning and careful layout at the cascode nodes, by lowering the on-resistance of the output chopper modulator CH_2 and by increasing the transconductance of the nMOS cascode devices (M_5 and M_6 in Fig. 3.11).

3.3 EMI hardening of chopped OpAMPs

From the considerations discussed in Section 3.2.1 it emerges that, as far as the broadband behaviour is considered, chopped OpAMPs susceptibility is ascribed to the same mechanisms affecting standard continuous time offset uncompensated OpAMPs and involving the nonlinear distortion operated by the input differential pair.

A part from the increased broadband immunity of chopped OpAMPs because of the filtering effect arising from the input chopper modulator, the EMI induced offset generation process can be considered the same for chopped and standard OpAMPs, hence, in principle, all the methodologies described in Section 2.1.2 can be profitably applied to the transconductance stage of chopped OpAMPs to increase their EMI immunity (Fig. 3.24).

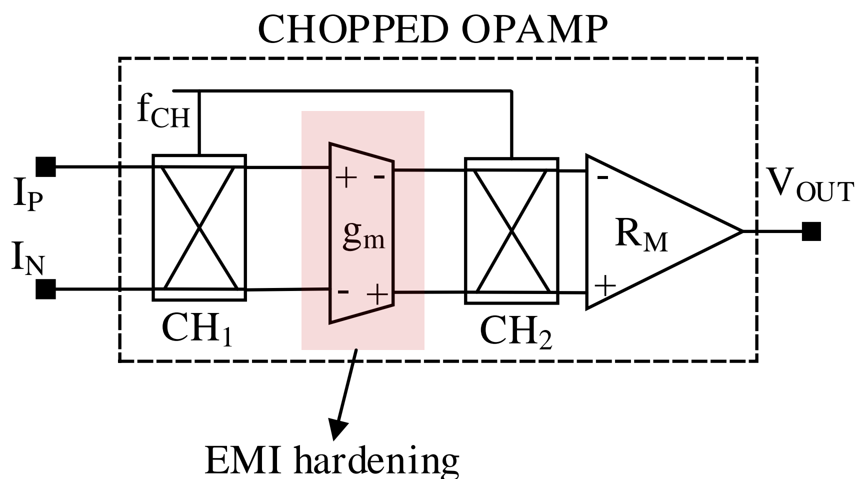

FIGURE 3.24: EMI hardening concept drawing for chopped operational amplifiers.

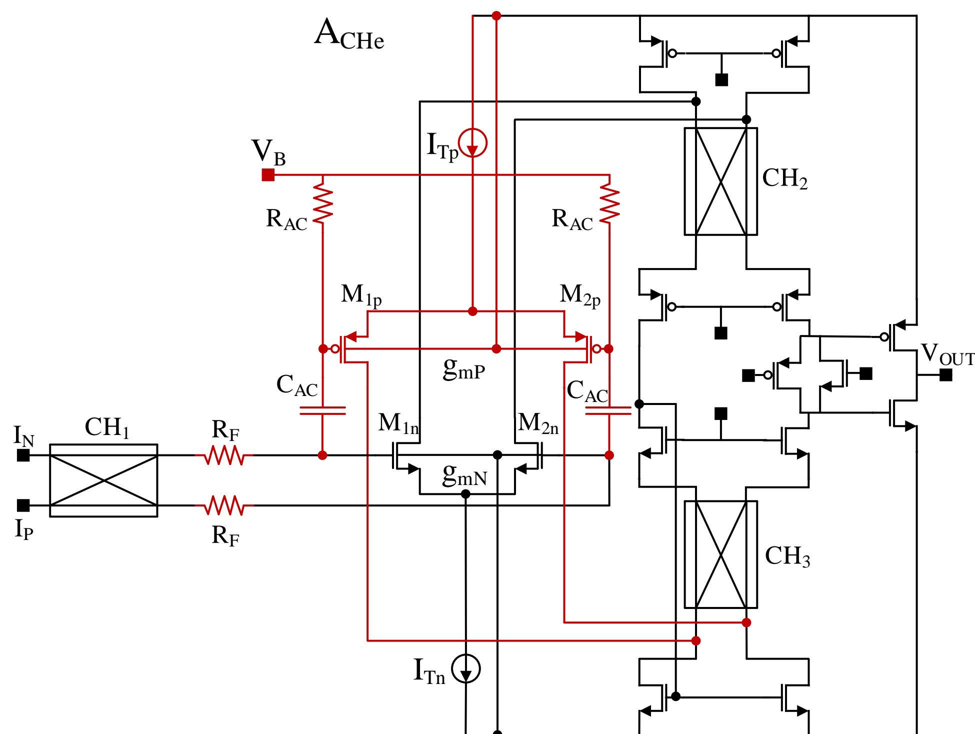

FIGURE 3.25: A_{CHe} EMI enhanced CMOS chopped amplifier. V_B represents the DC voltage used to bias the pMOS input stage.

To show this concept, an EMI hardened CMOS chopped OpAMP has been designed and fabricated. The schematic of the OpAMP, called A_{CHe}, is shown in Fig. 3.25, while its photomicrograph is depicted in Fig. 3.26. The EMI hardening is obtained by means of two combined techniques. At first, input filtering resistors R_F are added as standalone components in order to enhance the input filtering effect operated by the parasitic R_{ON} of chopper CH_1

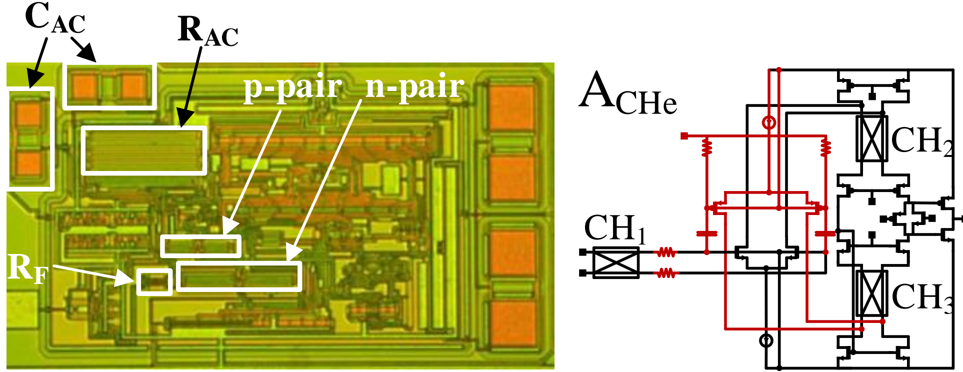

FIGURE 3.26: A_{CHe} photomicrograph. Highlights of the main nMOS differential, the AC coupled compensation pMOS differential pair, the input filtering resistors $R_F \simeq 38k\Omega$ and of the AC coupling network elements R_{AC} and C_{AC}. The overall area increment due to the EMI hardening of the device is less than 50%.

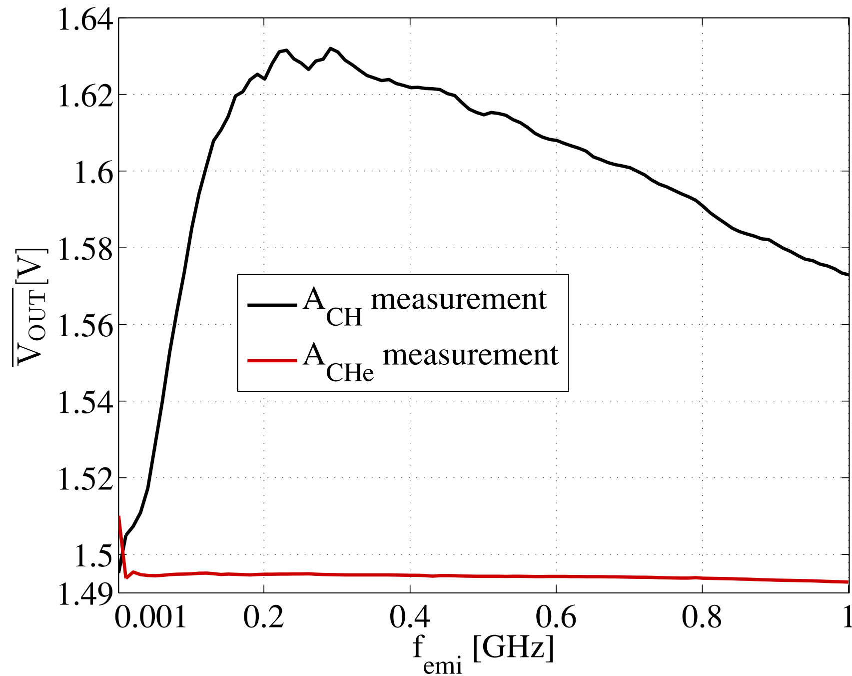

FIGURE 3.27: A_{CH} and A_{CHe} measured average output voltage with $P_{emi} = -5dBm$ ($A_{emi} \simeq 350mV_{pk}$). The EMI injection frequency step is 10MHz. Both amplifiers are clocked. The immunity test is performed at wafer level.

(Section 3.2.2). The value of these resistors is designed to maintain the amplifier phase margin above $60°$. Secondly, an AC coupled pMOS differential pair is inserted in parallel with the main nMOS based differential pair, in order to obtain a linearisation effect only for AC signals, as described in [23]. The graph in Fig. 3.27 shows a susceptibility comparison between the chopped OpAMP A_{CH} and the EMI hardened OpAMP A_{CHe}, according to the test exemplified

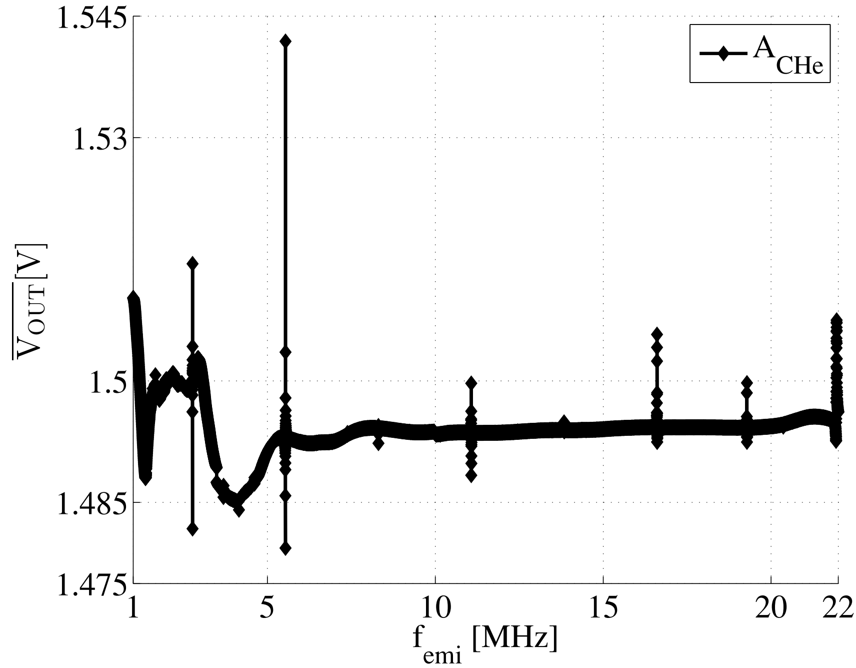

FIGURE 3.28: A_{CHe} measured average output voltage with $P_{emi} = -2\text{dBm}$ ($A_{emi} \simeq 500\text{mV}_{\text{pk}}$) and an EMI injection frequency step of 10KHz. The OpAMP is clocked at $f_{CH} = 1.27$ MHz. The DC shift experienced by the output voltage because of non linear distortion (V_{OS_CHemi}) is attenuated by the EMI hardening circuitry, whereas the superimposed offset peaks due to linear distortion (V_{OS_L}) are evident in the same way as for the chopped OpAMP A_{CH}.

by Fig. 3.18. As it is possible to note, the EMI induced offset V_{OS_emi} caused by nonlinear distortion experiences a maximum attenuation of almost 30dB, with a minimum area and current consumption increase with respect to the original topology. On the other hand, the EMI induced offset cancellation is not performed completely due to the limitations of these EMI hardening techniques, as explained in Section 2.1.2. Furthermore, the aforementioned techniques are effective only concerning the EMI induced offset because of non linear distortion (V_{OS_emi}), since they have been conceived for standard offset uncompensated OpAMPs. The picture in Fig. 3.28 shows that the linear distortion offset (V_{OS_L}, see Section 3.2.3), appearing in chopped OpAMPs at multiples of the chopping frequency, is anyway produced by the EMI hardened chopped OpAMP A_{CHe} and is not profitably attenuated by the circuitry added to counteract for the non linear distortion EMI induced offset V_{OS_emi}.

EMI SUSCEPTIBILITY OF AUTO-ZERO OPAMPS

4.1 Auto-zeroing offset compensation

The chopping technique provides offset compensation by means of a frequency modulation of the DC offset towards higher frequencies. On the contrary, the auto-zero technique modulates the offset and the input signal in the time domain, sampling the amplifier offset during a certain time slot in order to subtract it from the main signal path during a subsequent phase. One of the biggest disadvantages of chopping is the necessity to add either passive (LPF) or active residual ripple suppression mechanisms at the output of the amplifier ([44], [46]), increasing the complexity or the size of the circuit. On the other hand, auto-zero amplifiers are not affected by the output ripple and can therefore achieve high accuracy without bandwidth degradation. The basic principle of the auto-zeroing offset compensation technique implies to store the OpAMP DC offset (V_{OS_tech}) and low frequency noise (V_N) into a capacitor during a predefined time phase (auto-zero phase Φ_Z) and to subtract it from the amplifier signal path during a subsequent time phase (amplification phase Φ_A). Depending on where the DC offset is saved, input offset storage (Fig. 4.1) or output offset storage (Fig. 4.2) concepts are employed.

As described in [44], the DC voltage stored in the capacitor C_Z is subjected to an error whenever the switches connected to such capacitor open to sample the OpAMP offset (Fig.

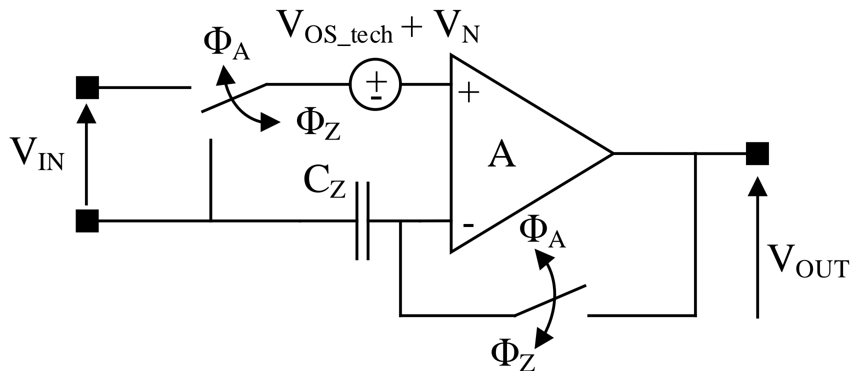

FIGURE 4.1: Auto-zero OpAMP block diagram: input offset storage and cancellation.

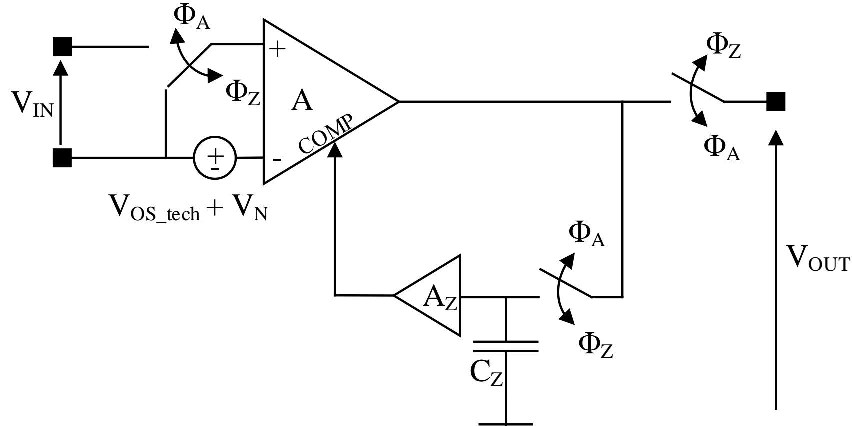

FIGURE 4.2: Auto-zero OpAMP block diagram: output offset storage and cancellation through a compensation port.

4.3). The error voltage step is mainly caused by four factors: the charge injected from the switch (Q_{inj}), the switch leakage current (I_{leak}), the sampled noise (V_N) and the clock signal fed through the capacitor via the switch parasitic capacitance (C_{OV}). All these factors contribute to generate the error in the voltage sampled on the capacitor C_Z and to degrade the accuracy of the offset cancellation, because the voltage across the capacitor during the amplification stage Φ_A is not only the OpAMP technological offset, but is affected by a residual error because of the aforementioned effects. The input offset storage technique cannot counteract this residual error by any means and this fact represents the major limitation of the accuracy performance of such a concept. On the other hand, the output offset storage and cancellation through an auxiliary input port techniques (Fig. 4.2) have been conceived to compensated also for the residual offset due to the switches non idealities, as it will be described in Section 4.2.2.

During the Φ_Z phase, the amplifier is not available to process any input signal, since the OpAMP input is not connected to the actual signal path. Consequently, auto-zero amplifiers cannot provide a continuous time output in their simple form. To counteract this inconvenience, ping-pong ([49], [50]) and offset stabilization ([51], [52]) concepts have been conceived. Ping-pong amplifiers are based on the use of two offset compensated amplifiers which work in parallel, being connected to the input and processing the incoming signals alternatively.

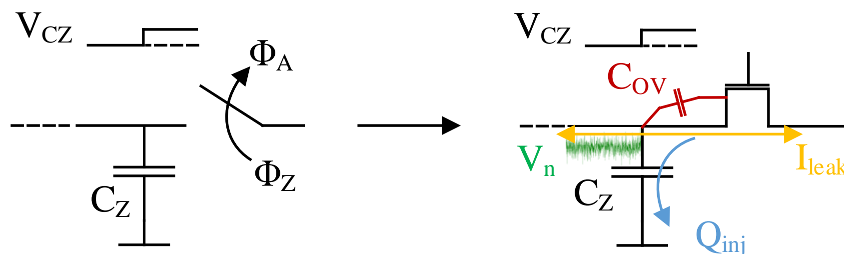

FIGURE 4.3: Hold capacitor voltage step error due to switch charge injection, low frequency noise and clock feed-through.

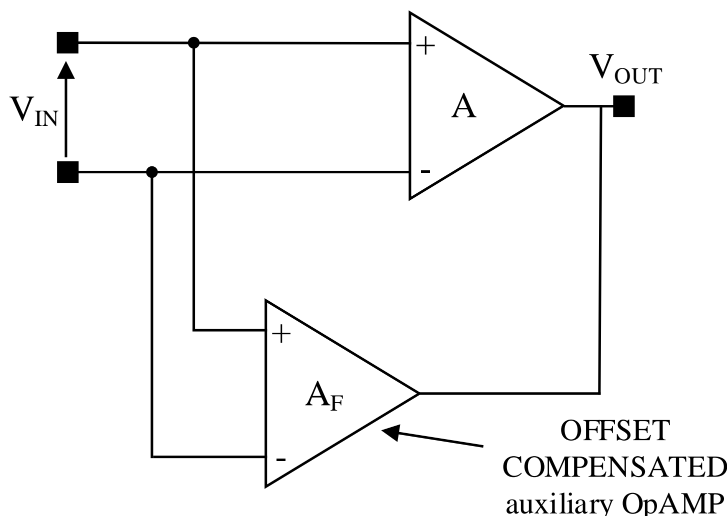

FIGURE 4.4: Offset stabilized amplifier: concept block scheme. The main amplifier (A) offset is reduced by means of the auxiliary amplifier A_F which has to be offset compensated either by auto-zeroing or by chopping.

This technique guarantees continuous time operation but doubles the area of the whole amplifier and increases the power consumption. Offset stabilized amplifiers (Fig. 4.4) are based on the use of an auxiliary amplifier (A_F) to compensate for the offset of the main amplifier A which is never disconnected from the signal path. In this way continuous time operation is guaranteed and the silicon area is increased only by means of the auxiliary amplifier area. The amplifier A_F senses the input offset of the main amplifier A and operates in the loop so to decrease it to a limit imposed by its accuracy. For this reason the auxiliary amplifier must be offset compensated itself, either by means of chopping or auto-zeroing. The design of a topology involving an offset stabilized amplifier in which the auxiliary OpAMP is offset compensated by means of auto-zeroing (auto-zero offset stabilization) is analysed in the following section. The auto-zero offset stabilized OpAMP represents then the reference device employed to investigate the EMI susceptibility of the auto-zero technique along this research work, as described in Section 4.2 and Section 4.3.

4.2 Design case: auto-zero offset stabilized OpAMP

4.2.1 Intuitive Analysis

The block diagram in Fig. 4.5 depicts a concept of the auto-zero offset stabilized OpAMP designed for the Ph.D. investigations on auto-zeroing, while the picture in Fig. 4.6 shows the very same concept highlighting how the amplifiers, the compensation ports and the offset cancellation is performed in terms of circuit functional blocks. The amplifiers are composed of a transconductance stage $G_{M1/F1}$ representing the input differential pair and the cascaded transresistance stages $R_{M/F}$ representing a current to voltage transresistance circuit in charge of converting the differential current of the differential input stage into the output single ended or differential voltage. The compensation ports are formed by the compensation transconductance stages $G_{M2/F2}$ which are in charge of correcting the amplifier output by unbalancing the main differential current in order to correct and null the amplifier offset.

The operation of the whole amplifier is described as follows. During the auto-zero phase Φ_Z (Fig. 4.7), the auxiliary amplifier is disconnected from the input and from the compensation port of the main amplifier and performs a self auto-zero in order to compensate for its own offset V_{OS_F}. To do so, the two inputs of OpAMP A_F are shorted to a common voltage (the voltage at the input node I_P in this case) to make the OpAMP offset A_F appearing at the output. At the same time the output of A_F is monitored via the compensation transconductance stage G_{F2} which measures the output offset and compensate for it adding its differential current contribution to the output of the input differential stage G_{F1}, in a negative feedback loop. This mechanism resembles exactly the schematic in Fig. 4.2 about the output offset storage and cancellation via a compensation port.

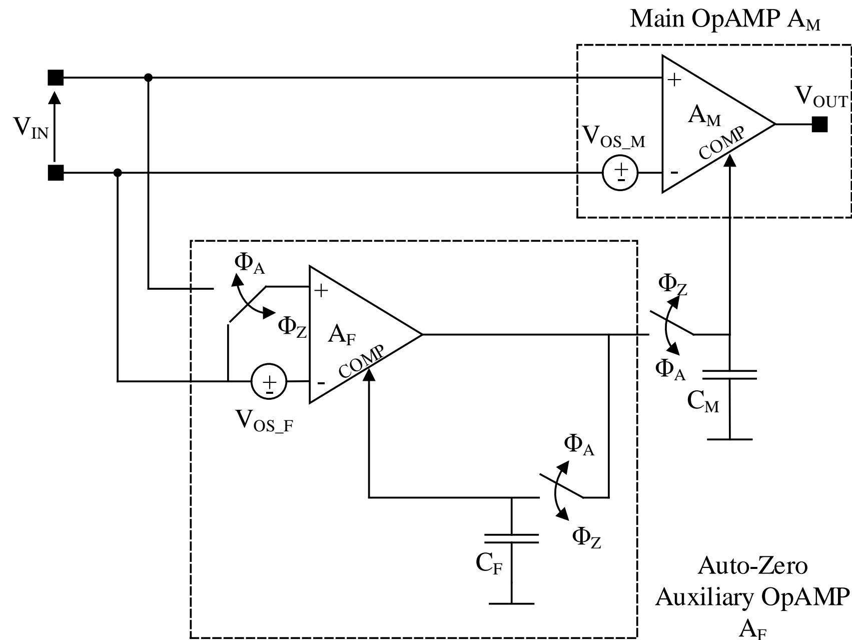

FIGURE 4.5: Auto-zero offset stabilized OpAMP concept block diagram.

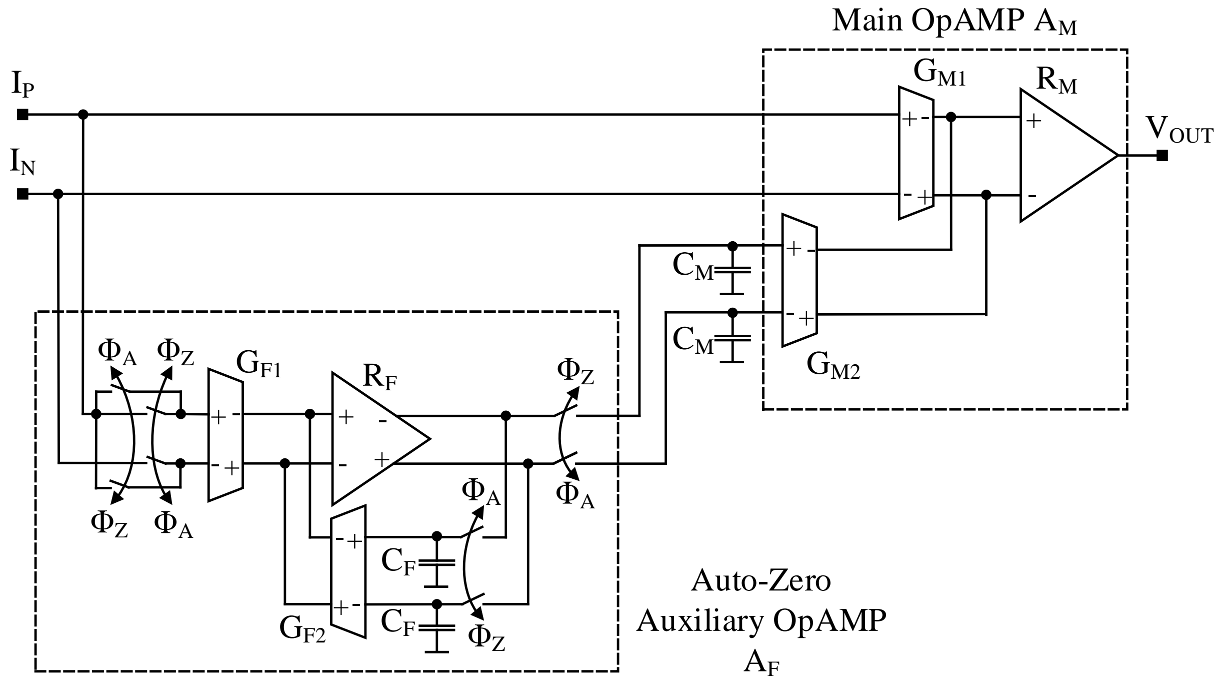

FIGURE 4.6: Auto-zero offset stabilized OpAMP circuit block diagram, highlight of the main circuit function blocks.

The differential voltage needed by the compensation stage G_{F2} to null the input stage G_{F1} offset is stored differentially on the capacitors C_F.

When the OpAMP passes to the amplification phase Φ_A (Fig. 4.8), the auxiliary amplifier A_F and the main amplifier A_M are connected in parallel, while the compensation stage of A_F, G_{F2}, is detached from the output of A_F and the voltage needed to compensate for the auxiliary amplifier offset, V_{OS_F}, is not lost but kept by capacitors C_F. The parallel connection between the two amplifiers is performed in the current domain via the compensation port formed by the transconductance stage G_{F1}. The parallel connection guarantees that the offset V_{OS_M} of the main amplifier A_M is reduced by means of the gain of the auxiliary amplifier A_F, while the offset V_{OS_F} of the auxiliary amplifier A_F propagates to the very output in a very small amount since it has been nulled during the previous auto-zero phase Φ_Z.

Finally, when the auto-zero phase starts again, the differential voltage produced by the auxiliary amplifier during the amplification phase is not lost but kept via capacitors C_M connected to the compensation port of the main amplifier A_M. The plot in Fig. 4.9 shows a time domain simulation of the designed amplifier (see Section 4.2.4) in order to highlight the aforementioned concepts. The simulation is performed with the OpAMP connected as a unity gain voltage buffer with $1.5V$ nominal input (Fig. 4.11). Once the main OpAMP is enabled at $t = 10\mu s$, the output voltage V_{OUT} settles to the same value of the input voltage V_{IN} because of the follower configuration. Furthermore, it is possible to note in Fig. 4.10 that the difference between the input and output voltage can be estimated to be around $50\mu\text{V}$; this difference is caused by the fact that the auxiliary OpAMP A_F is, at the beginning of the simulation, in the auto-zero phase Φ_Z and is therefore detached from the main amplifier.

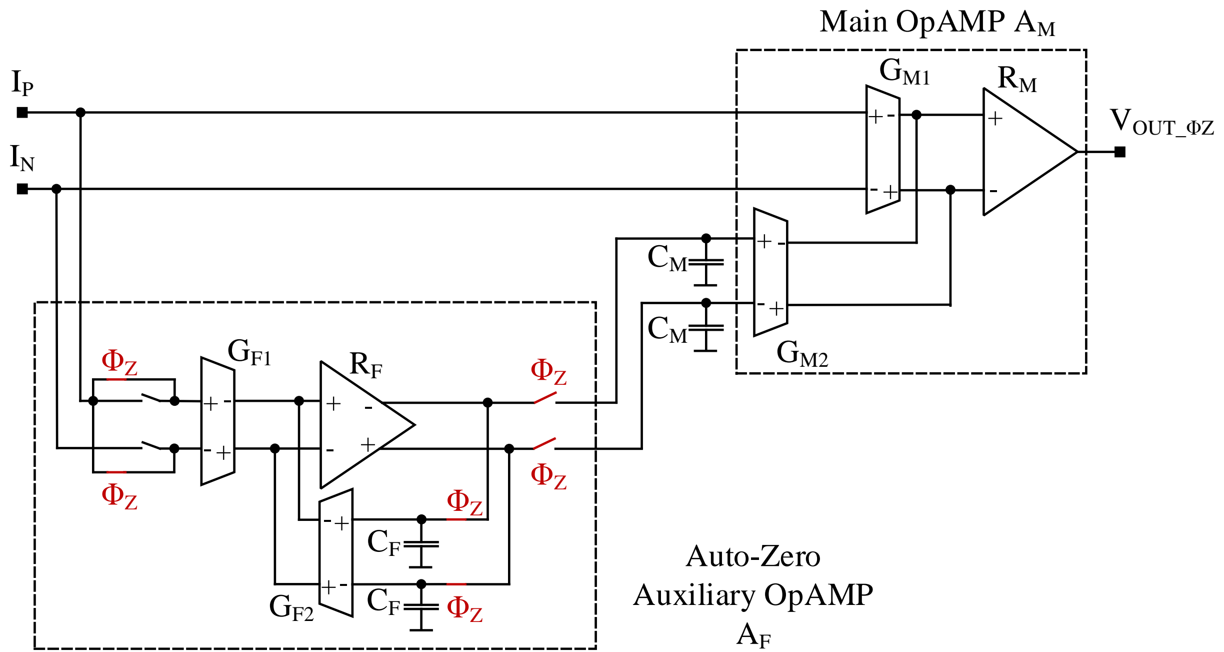

FIGURE 4.7: Auto-zero offset stabilized OpAMP: auto-zero phase Φ_Z configuration.

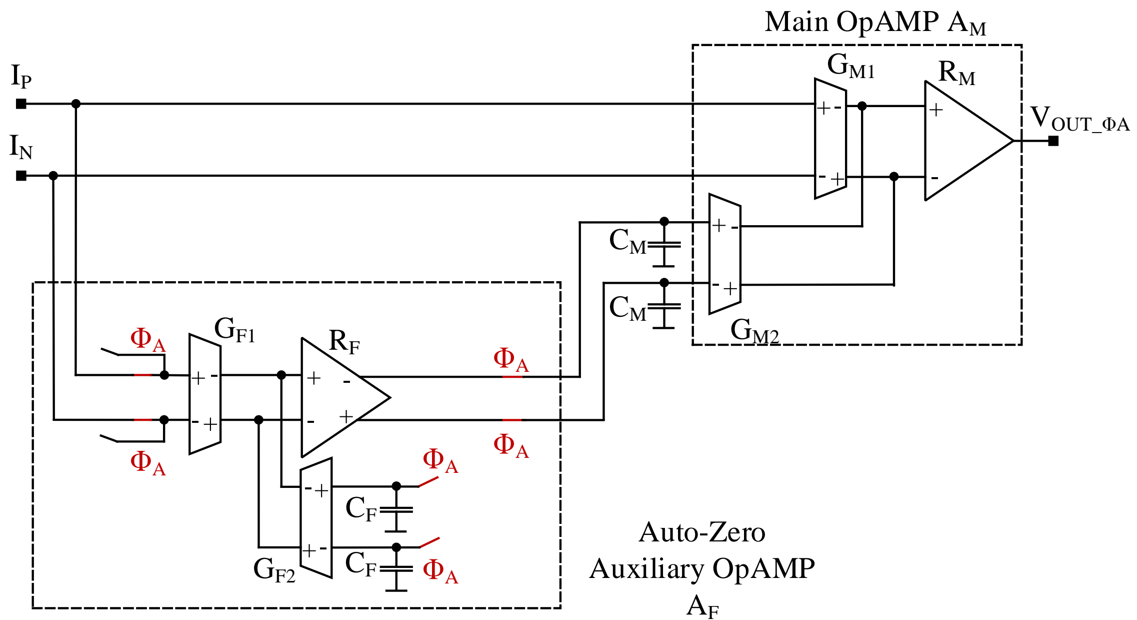

FIGURE 4.8: Auto-zero offset stabilized OpAMP: amplification phase Φ_A configuration.

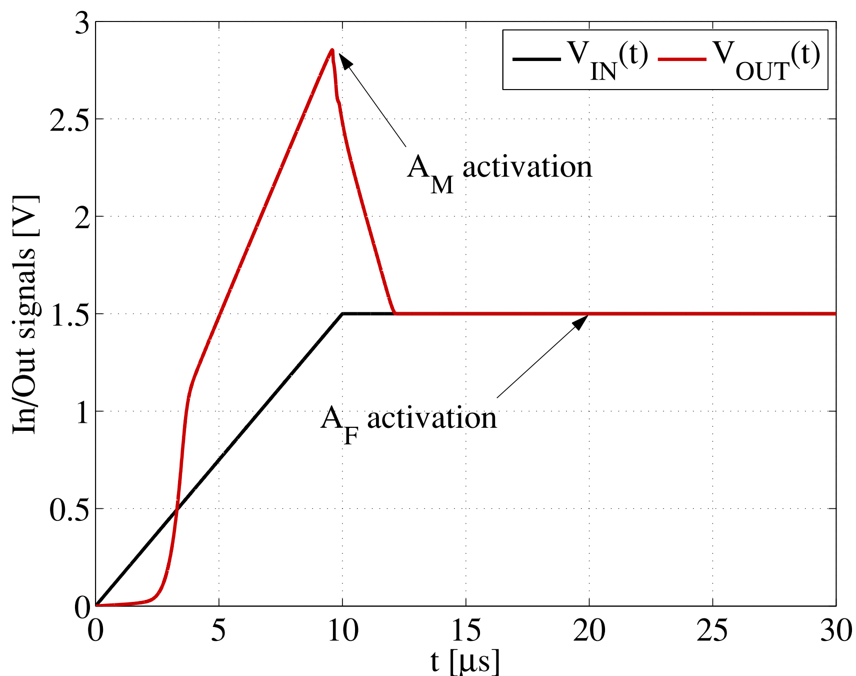

FIGURE 4.9: Auto-zero offset stabilized OpAMP simulation result example. The OpAMP is connected as a unity gain buffer with the input nominal voltage of 1.5 V (Fig. 4.11). The main amplifier A_M is activated at $t = 10\mu s$, while the auxialiary amplifier A_F is activated at $t = 20\mu s$.

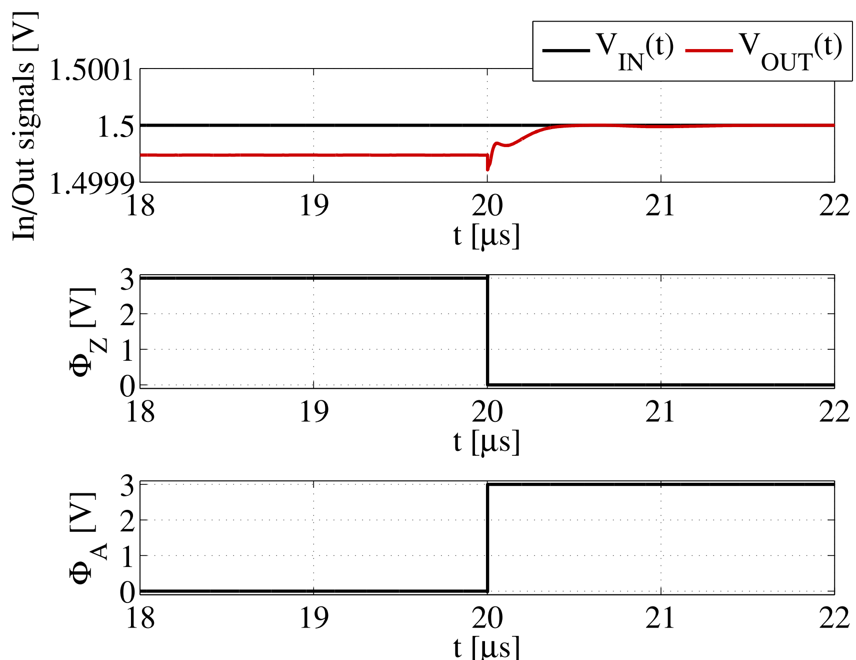

FIGURE 4.10: Inset of the auxiliary amplifier A_F activation effect on the output voltage at $t = 20\mu s$ for the simulation example of Fig. 4.9.

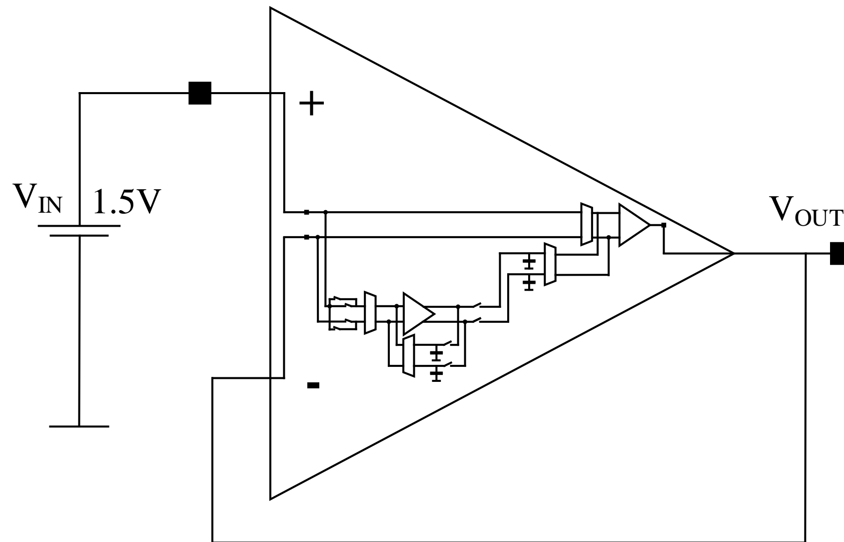

FIGURE 4.11: Auto-zero offset stabilized OpAMP buffer connected for the simulation example of Fig. 4.9 and Fig. 4.10.

When the amplification phase starts at $t = 20\mu s$, the gain of the auxiliary amplifier (already auto-zeroed) adds up to the gain of the main amplifier and the voltage error between input and output is greatly reduced and stays constant, since the differential voltages needed to keep such a small error are stored in the capacitors C_F and C_M. As a final remark, it is worth to highlight that the auxiliary OpAMP topology has been choosen to be fully differential, whereas it could have also been single ended. The reason behind this choice is analytically clarified in Section 4.2.2 but can be explained as follows.

4.2.2 Analytical Design

The residual offset of the presented offset stabilized auto-zero amplifier is mainly caused by the switch non idealities highlighted in Section 4.1. The charge injected by the switches into capacitors C_M and C_F, when the switches go from the on to the off state, generates a residual offset at the output which set the accuracy limit of the amplifier. The differential topology here employed ensures that such residual error is not dependent from the charge injected by a single switch, but it is instead directly related to the mismatch of the charges injected by the couple of switches connected at the differential input and output of the auxiliary amplifier A_F. A careful layout can ensure this charges mismatch to be greatly smaller than the charge injected by a single switch. The drawback of the differential solution resides in the fact that also a good matching between the differential capacitors has to be achieved in order to keep the residual offset at small values. This section is dedicated to the analytical design which has to be performed in order to size the OpAMP components to achieve a target residual offset. The analysis is performed via functional block diagrams showing the building blocks of the auto-zero offset stabilized OpAMP in a single ended version, but the results can be extended to the fully differential case without any modification. A convenient way of analysing the topology is

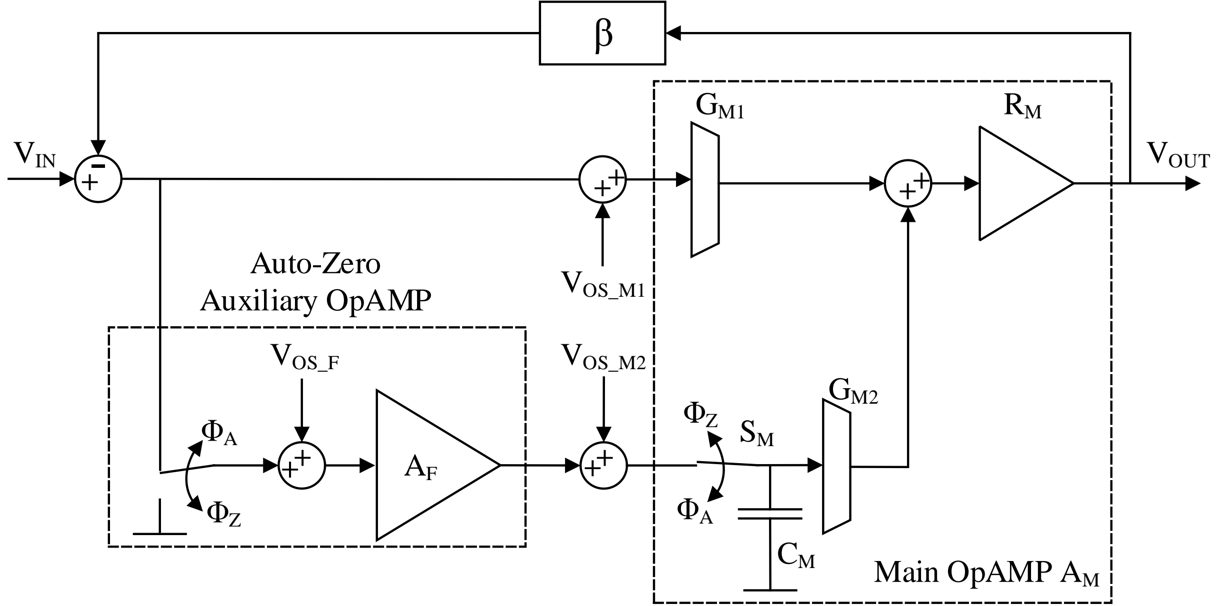

FIGURE 4.12: Offset stabilized OpAMP building blocks and input referred offset contributions during the amplification phase Φ_A. The auxiliary amplifier A_F is depicted as a standalone building block with its own offset contribution V_{OS_F}, regardless of its internal structure.

to start from the parallel connection of the main and auxiliary OpAMPs, deriving the expression of the gain and the various offset contributions.

The picture in Fig. 4.12 shows a functional block diagram of the offset stabilized amplifier, highlighting only the main amplifier A_M components and leaving the auxiliary amplifier A_F as a standalone block. As it is possible to note from Fig. 4.12, all the main offset contributions have been added in their input referred version. The auxiliary amplifier has its own input referred voltage V_{OS_F}, as well as the two transconductance stages of the main amplifier, G_{M1} with its offset V_{OS_M1} and G_{M2} with its offset V_{OS_M2}. The offset contribution of the block R_M, which represents the output transresistance stage of amplifier A_M (see Section 4.2.1), is embedded into the input referred offset G_{M1} as well. For completeness, a negative feedback network β is also inserted in the block diagram.

The quantities A_M and A_F represent the open loop gains of the main and the auxiliary amplifiers respectively and are expressed as (see Fig. 4.6):

$$A_M = G_{M1}\, R_M \tag{4.1}$$

$$A_F = G_{F1}\, R_F \tag{4.2}$$

The open loop gain of the complete offset stabilized OpAMP (phase Φ_A) is equal to:

$$A|_{\Phi_A} = A_M + A_F\, R_M\, G_{M2} \tag{4.3}$$

The input-output characteristic of the OpAMP depicted in Fig. 4.12 during phase Φ_A is then described by ([53]):

$$\begin{aligned} V_{OUT}|_{\Phi_A} &= \frac{A_M + A_F\, G_{M2}\, R_M}{1+\beta(A_M + A_F\, G_{M2}\, R_M)}\, V_{IN} \\ &= \frac{G_{M1}\, R_M + G_{F1}\, R_F\, G_{M2}\, R_M}{1+\beta(G_{M1}\, R_M + G_{F1}\, R_F\, G_{M2}\, R_M)}\, V_{IN} \end{aligned} \tag{4.4}$$

The main and auxiliary amplifier gains sum up, while the auxiliary amplifier gain is also boosted by the presence of the main amplifier compensation port ($R_M\, G_{M2}$).

To evaluate the accuracy performance of the amplifier it is then necessary to estimate how the various offset contributions propagate to the OpAMP output. Looking again at Fig. 4.12 it is possible to express the output voltage ($V_{OUT_OS_i}$) caused by each offset contribution i with the following expressions:

$$V_{OUT_OS_M1}|_{\Phi_A} = A_M\, V_{OS_M1} = (G_{M1}\, R_M)\, V_{OS_M1} \tag{4.5}$$

$$V_{OUT_OS_M2}|_{\Phi_A} = (R_M\, G_{M2})\, V_{OS_M2} \tag{4.6}$$

$$V_{OUT_OS_F}|_{\Phi_A} = (A_F\, R_M\, G_{M2})\, V_{OS_F} \tag{4.7}$$

Unfortunately, considering only these offset contributions would lead to an underestimation of the residual amplifier offset, for the following reason. The switch S_M, depicted in Fig. 4.12 in its single ended version, detaches the auxiliary amplifier from the main amplifier compensation port when the circuit passes from the amplification to the auto-zero phase. When the switch S_M goes from the on to the off state ($\Phi_A \to \Phi_Z$), an error voltage is generated across the hold capacitor C_M because of the charge injection mechanism and the other error sources discussed in Section 4.1. In particular, the capacitor C_M error voltage can be approximated as ([44]):

$$V_{eM}|_{\Phi_A \to \Phi_Z} \simeq \pm \frac{q_{jM}}{C_M} \pm \alpha \frac{C_{OV}}{C_{OV} + C_M} V_{clk} \pm \sqrt{\frac{k_B\, T}{C_M}} \pm \frac{I_{leak}\, T_Z}{C_M} \tag{4.8}$$

Where the four contributions in expression (4.8) are:

1. *Charge injection.* The charge q_{jM} injected from the switch S_M channel to the capacitor C_M generates a voltage step which represents one of the main error contributions to the OpAMP accuracy.

2. *Clock Feed Through.* The parasitic overlap capacitance at the gate edge of the switch, C_{OV}, causes the clock signal controlling the switch to appear at the capacitor site according to the capacitive partition between C_{OV} and C_M itself. The amount of clock feed through also depends on the clock voltage swing V_{clk} and the correction factor α.

3. *Thermal Noise*. Another main contribution is represented by the thermal noise on C_M. In its simple form, this noise can be expressed as the *KTC* noise dependent on the absolute temperature T (k_B being the Boltzmann constant, see Table 2.1).

4. *Current Leakage*. For the off time of the switch (during phase Φ_Z), the switch leakage current make the C_M capacitor voltage to shift depending on the duration of the off state (T_Z).

Expression (4.8) refers to the case of a single S_M switch and a single C_M capacitor. This operational amplifier, designed during the Ph.D. research according to the auto-zero offset stabilization technique, has been made with the fully differential auxiliary amplifier A_F (Fig. 4.6). The main reason for this is to minimize the error contributions presented in (4.8), which can be rewritten considering a fully differential structure (Fig. 4.13):

$$\begin{aligned} \Delta V_{eM}|_{\Phi_A \to \Phi_Z} = &\pm \Delta\left(\frac{q_{jM12}}{C_{M12}}\right) \pm \alpha V_{clk} \Delta\left(\frac{C_{OV12}}{C_{M12}}\right) \\ &\pm \sqrt{k_B \Delta\left(\frac{T_{12}}{C_{M12}}\right)} \pm \mathrm{T}_Z \Delta\left(\frac{I_{leak12}}{C_{M12}}\right) \end{aligned} \tag{4.9}$$

Where the mismatches are denoted by the presence of the Δ and refer to the mismatch of the switches S_{M1} and S_{M2} charge injections (q_{jM12}), overlap capacitances (C_{OV12}) and leakage currents (I_{leak12}), while the capacitors mismatch is taken into account as capacitances difference (C_{M12}) and temperature difference (T_{12}). Provided that the mismatch between the hold capacitors is small, it is possible to state that the error voltage for the fully differential case can be made much smaller than the one of the single ended case:

$$\Delta C_{M12} \simeq 0 \to \Delta V_{eM}|_{\Phi_A \to \Phi_Z} \ll V_{eM}|_{\Phi_A \to \Phi_Z} \tag{4.10}$$

The voltage error on capacitor S_M propagates to the output according to (see Fig. 4.12):

$$V_{OUT_OS_eM}|_{\Phi_A \to \Phi_Z} = (G_{M2}\, R_M)\Delta V_{eM}|_{\Phi_A \to \Phi_Z} \tag{4.11}$$

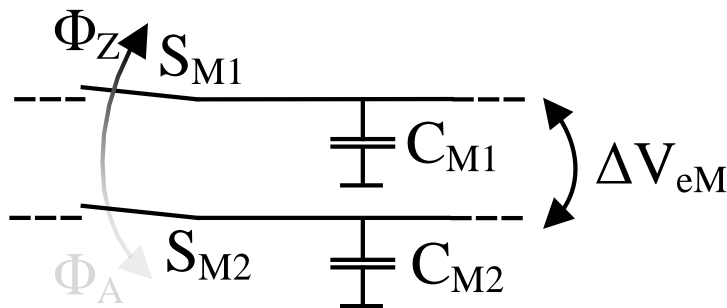

FIGURE 4.13: Switches and hold capacitors in a fully differential structure as for the auxiliary amplifier depicted in Fig. 4.6.

Expressions (4.5), (4.6), (4.7) and (4.11) represent the output residual offset at the end of the amplification phase Φ_A. To obtain the equivalent input referred offset it is sufficient to divide such expression by the open loop gain A of the OpAMP in phase Φ_A (see expression (4.3)). The expression of the total input referred offset at phase Φ_A takes then the form:

$$V_{IN_OS}|_{\Phi_A} = \frac{\pm A_M\, V_{OS_M1} \pm G_{M2}\, R_M\, V_{OS_M2} \pm A_F\, G_{M2}\, R_M\, V_{OS_F} \pm G_{M2}\, R_M\, \Delta V_{eM|_{\Phi_A}}}{A} \tag{4.12}$$

It should be noted that the offset contributions have to be added as root mean squares if the offset value is considered as a statistical standard deviation. Expression (4.12) can be simplified considering (4.1), (4.2) and (4.3) and the following hypothesis:

$$A_F\, G_{M2} \gg G_{M1} \tag{4.13}$$

Then:

$$A \simeq A_F\, G_{M2}\, R_M \tag{4.14}$$

Under this hypothesis and definitions, it is possible to rewrite (4.12) as:

$$V_{IN_OS}|_{\Phi_A} \simeq \pm\frac{G_{M1}/G_{M2}}{A_F}\, V_{OS_M1} \pm \frac{V_{OS_M2}}{A_F} \pm V_{OS_F} \pm \frac{G_{M2}}{G_{M1}}\, \Delta V_{eM|_{\Phi_A}} \tag{4.15}$$

Expression (4.15) is of extreme importance in order to understand which are the main quantities contributing to the residual offset of the auto-zero offset stabilized amplifier. In fact, as long as the auxiliary amplifier gain A_F is high, the offset caused by the differential pairs G_{M1} and G_{M2}, namely V_{OS_M1} and V_{OS_M2}, are reduced by A_F, giving then a negligible contribution to the residual offset. More important, it is possible to note that the auxiliary amplifier offset, V_{OS_F}, is not compensated by any means and fully contribute to the final residual offset $V_{IN_OS}|_{\Phi_A}$. This is the main reason why the auxiliary amplifier must be offset compensated. Finally, the contribution due to the voltage error on capacitors C_M is tapered by the ratio of the transconductance of the compensation and main stages of the A_M amplifier. For this reason, this ratio has to be set carefully in order to control the OpAMP residual offset, as it is shown later in this section.

In order to complete the design analysis, the auxiliary amplifier offset V_{OS_F} has to be evaluated. The quantification of this offset can be made by having a closer look at the auto-zero amplifier structure in Fig. 4.14. The derivation of V_{OS_F} is performed in the same way used for the whole amplifier but considering only phase Φ_Z. Such contribution can then be plugged into (4.15) to obtain a general form of the residual output offset taking also into account the auxiliary amplifier components. The schematic in Fig. 4.14, showing the auxiliary amplifier building blocks, can be used to determine the amount of residual offset of the auxiliary amplifier after the auto-zero phase Φ_Z. It is worth to note how this structure resembles the one of the main amplifier: the difference here is that the compensation port input is the fed back output

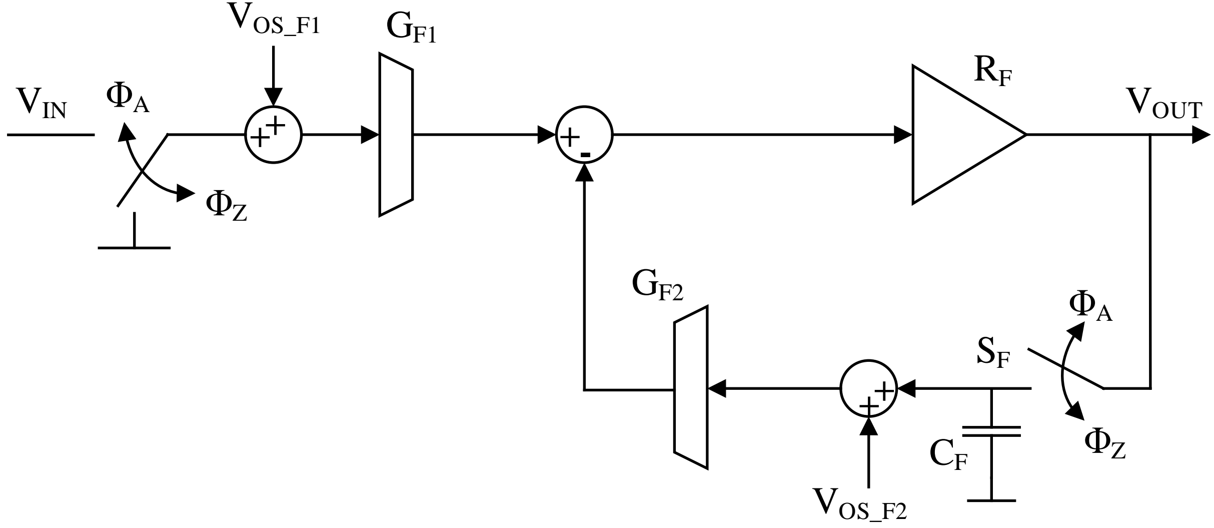

FIGURE 4.14: Auxiliary amplifier A_F building blocks and input referred offset contributions.

itself and does not come from another amplifier. At the phase Φ_Z the auxiliary amplifier input is shorted to have a null input differential voltage, which is equivalent to setting it to ground in Fig. 4.14 or shorting the differential inputs to the common voltage in Fig. 4.6. The auxiliary amplifier output, which should be null but is affected by the main transconductance stage G_{F1} offset (V_{OS_F1}, input referred), is then fed back to the compensation port through the transconductance stage G_{F2} to compensate for V_{OS_F1} itself. At the amplification phase Φ_A, the value needed for the V_{OS_F1} offset compensation stays then stored on the capacitor C_F and the auxiliary amplifier, auto-zeroed, is the connected in parallel to the main amplifier to process the incoming signals. Following the same procedure used for the main amplifier offset calculation, the following equations express the output offset contributions of the auxiliary amplifier:

$$V_{OUT_OS_F1}|_{\Phi_Z} = \pm \frac{R_F\, G_{F1}}{1 + R_F\, G_{F2}}\, V_{OS_F1} \tag{4.16}$$

$$V_{OUT_OS_F2}|_{\Phi_Z} = \mp \frac{R_F\, G_{F2}}{1 + R_F\, G_{F2}}\, V_{OS_F2} \tag{4.17}$$

As for the case of the switch S_M in Fig. 4.12, also in this case the output offset calculation must take into account the error appearing on capacitor C_F at the transition $\Phi_Z \rightarrow \Phi_A$, when the switch S_F opens.

$$V_{OUT_OS_eF}|_{\Phi_Z \rightarrow \Phi_A} = (R_F\, G_{F2}) \Delta V_{eF}|_{\Phi_Z \rightarrow \Phi_A} \tag{4.18}$$

In (4.18), the parameter $\Delta V_{eF}|_{\Phi_Z \rightarrow \Phi_A}$ represents the error voltage appearing on capacitor(s) C_F at the opening of the switch S_F during the transition $\Phi_Z \rightarrow \Phi_A$. This error voltage contribution is determined by exactly the same mechanisms of the error voltage $\Delta V_{eM}|_{\Phi_A \rightarrow \Phi_Z}$ (see (4.9)). Also for this error contribution, the discussion about the single ended versus differential case holds. To obtain the equivalent input referred offset for the auxiliary amplifier (V_{OS_F}) it

is then sufficient to divide the contributions (4.16),(4.17) and (4.18) by the auxiliary amplifier open loop gain $A_F = R_F\, G_{F1}$:

$$V_{OS_F}|_{\Phi_Z} = \pm \frac{V_{OS_F1}}{1 + R_F\, G_{F2}} \mp \frac{G_{F2}/G_{F1}}{1 + R_F\, G_{F2}}\, V_{OS_F2} \pm \frac{G_{F2}}{G_{F1}}\, \Delta V_{eF}|_{\Phi_Z \to \Phi_A} \tag{4.19}$$

Expression (4.19) highlights which are the most important parameters playing a role in the auto-zero offset compensation and in the generation of the residual offset for the auxiliary amplifier. In particular, it is possible to note that both the offset contributions due to the auxiliary amplifier main transconductance G_{F1} and compensation transconductance G_{F2} are greatly reduced by the auto-zero mechanism, being divided by the auto-zero loop gain $1 + R_F\, G_{F2}$. Also in this case, the residual offset is mainly caused by the error voltage on the capacitor C_F. This error voltage is multiplied by the ratio of the compensation and main transconductances of the auxiliary amplifier. Exactly as for the case of the main amplifier (see (4.15)), the ratio G_{F2}/G_{F1} represents a design constraint to control the auto-zero offset stabilized amplifier residual offset. Plugging (4.19) into (4.15) provides then:

$$\begin{aligned} V_{IN_OS} \simeq & \left[\pm \frac{G_{M1}/G_{M2}}{G_{F1}\, R_F}\, V_{OS_M1} \pm \frac{V_{OS_M2}}{G_{F1}\, R_F} \pm \frac{G_{M2}}{G_{M1}}\, \Delta V_{eM|_{\Phi_A}} \right] \\ & + \left[\frac{V_{OS_F1}}{1 + R_F\, G_{F2}} \mp \frac{G_{F2}/G_{F1}}{1 + R_F\, G_{F2}}\, V_{OS_F2} \pm \frac{G_{F2}}{G_{F1}}\, \Delta V_{eF}|_{\Phi_Z \to \Phi_A} \right] \end{aligned} \tag{4.20}$$

Expression (4.20) represents the total residual offset of the discussed auto-zero offset stabilized OpAMP, the first block of the equation representing the contributions caused by the main amplifier and the second block caused by the auxiliary amplifier. As already pointed out, the equation (4.20) represents the maximum offset value, while the standard deviation σ can be obtained combining the terms as a root mean square:

$$V_{IN_OS}|_\sigma \simeq \sqrt{\begin{aligned} & \left[\left| \frac{G_{M1}/G_{M2}}{G_{F1}\, R_F}\, V_{OS_M1}|_\sigma \right|^2 + \left| \frac{V_{OS_M2}|_\sigma}{G_{F1}\, R_F} \right|^2 + \left| \frac{G_{M2}}{G_{M1}}\, \Delta V_{eM}|_\sigma \right|^2 \right] \\ & + \left[\left| \frac{V_{OS_F1}|_\sigma}{1 + R_F\, G_{F2}} \right|^2 + \left| \frac{G_{F2}/G_{F1}}{1 + R_F\, G_{F2}}\, V_{OS_F2}|_\sigma \right|^2 + \left| \frac{G_{F2}}{G_{F1}}\, \Delta V_{eF}|_\sigma \right|^2 \right] \end{aligned}} \tag{4.21}$$

In Expression (4.21) the standard deviations $\sigma(V_{th})$ and $\sigma(\beta)$ referred to the plain offset values can be derived from (2.19) and represent the technological offset voltages of the differential pairs associated to the OpAMP transconductance stages. The maximum and σ values evaluation for the error voltages ΔV_{eM} and ΔV_{eF} is not straightforward, since they depend upon several parameters and can also have a much more complicated model than the one referred by (4.8). The solution adopted for this Ph.D. research has been to simulate the voltage variability

across a couple of capacitors each one connected to a switch (Fig. 4.13). A Montecarlo simulation performed over several runs of successive opening and closing of the switches can provide an estimation of the σ value of the differential error voltage appearing across the capacitors, since it takes into account the mismatch of the switches and the capacitors couples. By doing so and by changing the capacitors value it has been possible to extract, in first approximation, the values of $\Delta V_{eM}|_{\sigma}$ and $\Delta V_{eF}|_{\sigma}$. With the aim of taking a designer approach, looking at expression (4.21) it is possible to make the following considerations:

- The circuit parameter which is crucial to lower the main amplifier offset (V_{OS_M}) is the auxiliary amplifier gain $A_F = G_{F1}\, R_F$.
- The auxiliary amplifier offset (V_{OS_F}) is compensated via the auto-zero technique and it can be reduced as long as the compensation port loop gain ($R_F\, G_{F2}$) is kept high.
- The limitation to the offset reduction is caused by the residual error voltages (ΔV_{eM} and ΔV_{eF}) on the hold capacitors. These error voltages can be reduced by increasing the capacitors values and by keeping low values of the ratios G_{M2}/G_{M1} and G_{F2}/G_{F1}.

While expressions (4.20) and (4.21) can be counterintuitive to investigate, a better insight can be gained if some further approximations are performed. In particular, it is possible to suppose that the offset values for the four transconductance stages are equal and also the capacitors error voltage are of the same value:

$$\begin{aligned} &V_{OS_M1} = V_{OS_M2} = V_{OS_F1} = V_{OS_F2} = V_{OS} \\ &\Delta V_{eM} = \Delta V_{eF} = \Delta V_e \end{aligned} \tag{4.22}$$

This assumption is valid if all the transconductance stages of the amplifier are made of differential pair of the same area and operating in the same biasing condition, whereas the error on the capacitor is the same if all the capacitors are of the same type and dimension and connected to switches of the same type and dimension. If (4.22) holds, expression (4.20) takes the form:

$$V_{IN_OS} \simeq \frac{V_{OS}}{A_F}\left[2 + \frac{1}{N_M} + \frac{1}{N_F}\right] + \Delta V_e\left[N_M + N_F\right] \tag{4.23}$$

Where:

$$\begin{aligned} N_M &= \frac{G_{M2}}{G_{M1}} \\ N_F &= \frac{G_{F2}}{G_{F1}} \end{aligned} \tag{4.24}$$

The advantage of rewriting (4.20) as (4.23) is that expression (4.23) has a locus of minima, as it is shown in the plot of Fig. 4.15. As it is possible to note from Fig. 4.15, under hypotheses

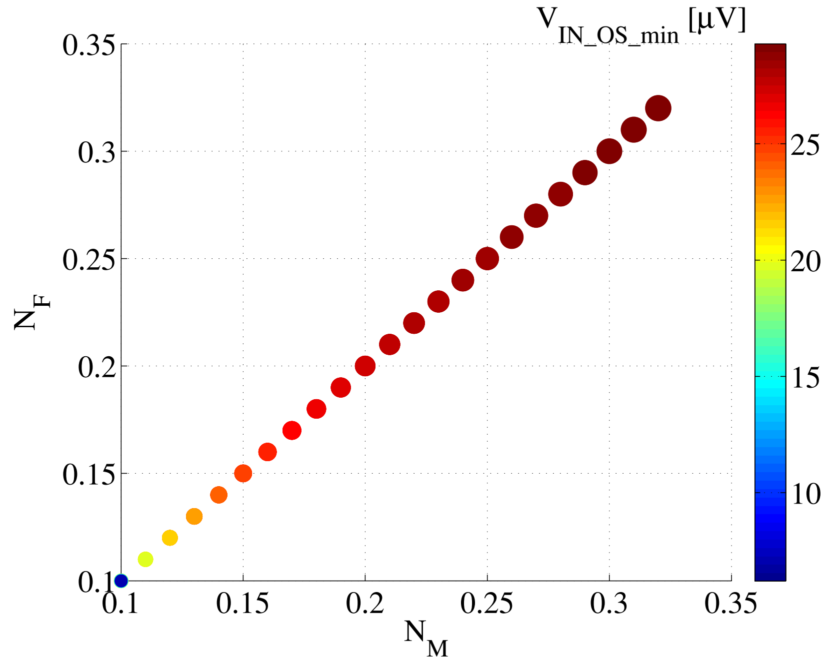

FIGURE 4.15: Minima locus of expression (4.23) with respect to $N_M = G_{M2}/G_{M1}$ and $N_F = G_{F2}/G_{F1}$. The simulation has been obtained with $A_F = 83\text{dB}$, $V_{OS} = 2\text{mV}$ and $\Delta V_e = 20\mu\text{V}$, providing then the minimum offset values displayed on the colour bar.

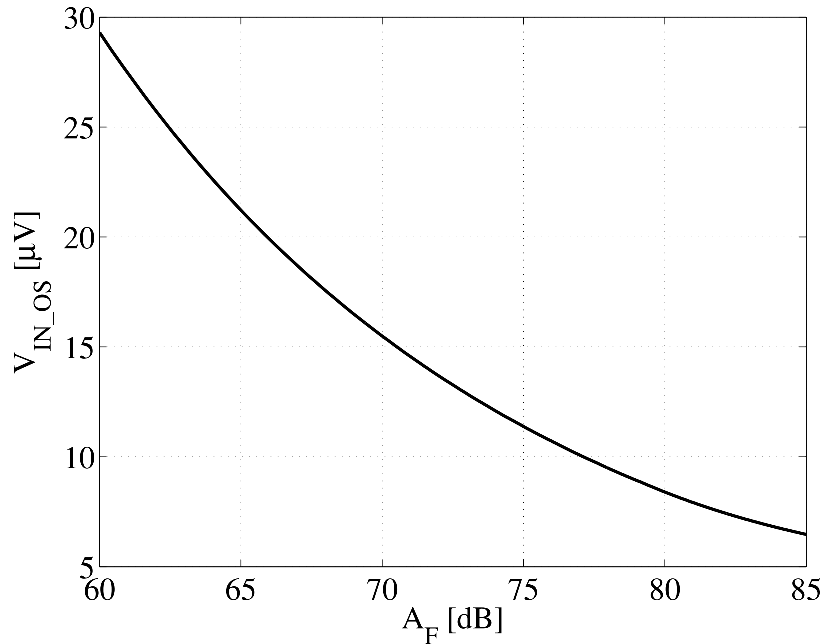

FIGURE 4.16: Expression (4.23) and dependency of the residual input referred offset voltage on the auxiliary amplifier gain A_F. The ratios N_M and N_F are set to the value 0.12.

(4.22), the lowest amount of residual input referred offset V_{IN_OS} is obtained if the ratios N_M and N_F are the same.

This means that, under the assumption of having same technological offset for all the G_M stages of the OpAMP and same amounts of residual error voltages on the differential capacitors, the residual offset voltage out of the auto-zero offset stabilized topology is minimized if the main and auxiliary amplifiers differential pairs (main and compensation ones) are in the same (small) ratio. Another advantage of expression (4.23) is that it let to directly observe the dependency of the residual offset voltage upon the auxiliary amplifier gain A_F, at it is shown in Fig. 4.16.

4.2.3 Clocking and charge injection considerations

This subsection deals with some further considerations and optimizations which can be taken into account along the design of the auto-zero offset stabilized amplifier. The first aspect to consider is about the clocking of the amplification and auto-zero phases. By looking at Fig. 4.6 it is possible to note that there is a switching of signal paths between capacitors C_M and C_F. Since the differential voltage across these capacitors is not the same going from one phase to the other, this results in a spike of the output voltage ([44]). A possible enhancement of such an issue is to use a 4-phase clock to perform the connection and disconnection of the capacitors with a delay, according to the schematic in Fig. 4.17.

The basic principle of the alternative clocking is the following. Going from the amplification phase Φ_A to the auto-zero phase Φ_Z, the auxiliary amplifier is first disconnected from the main amplifier (Φ_{A2} goes low). Only after that, the auxiliary amplifier is also disconnected from the input line (Φ_{A1} goes low). Then, the output of the auxiliary amplifier is fed back to the auxiliary amplifier compensation port (Φ_{Z1} goes high) and finally the auxiliary amplifier input is short circuited to perform the auto-zero of the auxiliary amplifier itself (Φ_{Z2} goes high).

The transition from the auto-zero phase Φ_Z to the amplification phase Φ_A follows a reverse symmetric timing. The delayed connection and disconnection of the auxiliary amplifier to

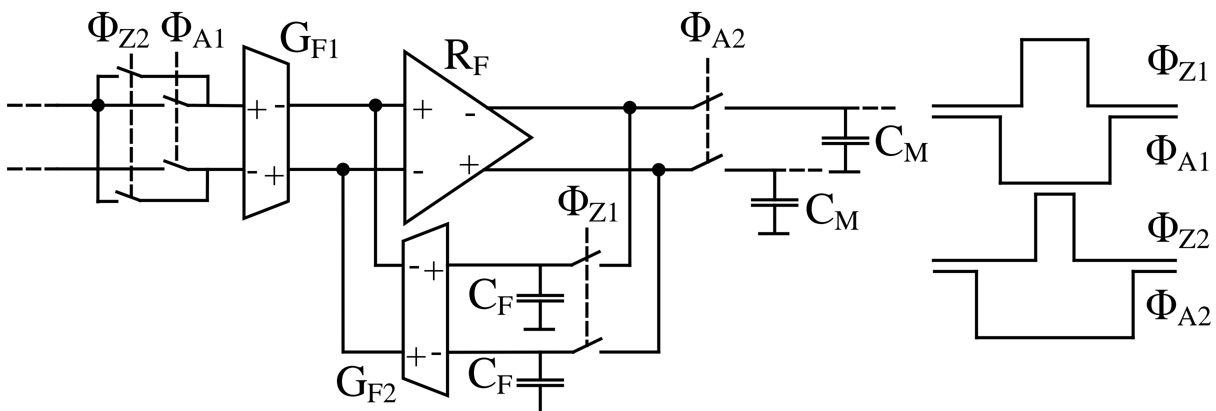

FIGURE 4.17: Alternative 4 clocking phases with delay to reduced voltage spikes. High signals on the switch control lines indicates closing, while low signals indicate opening.

and from the main one ensures a reduced spiking activity at the amplifier output, because the auxiliary amplifier is connected to the main one only after the switching activity performed for the auto-zero operation has taken place and is disconnected before any switching activity starts to operate in it.

As a final consideration about charge injection, several mechanisms and switch topologies have been conceived in order to mitigate this unwanted effect. For example, the use of half-sized dummy switches at the edges of each switch present in the topology ([44]) can be of help in order to lower the residual offset caused by error voltages across the hold capacitors.

4.2.4 Bandwidth and stability considerations

One important aspect to consider while dealing with offset stabilized topologies is the stability and frequency compensation of the amplifier. If either the main and the auxiliary amplifier are designed to be stable, it is important to understand which kind of transfer function is generated by their combination in order to understand the frequency response and stability of the whole offset stabilized amplifier. The circuit in Fig. 4.18 depicts the schematic of the auto-zero offset stabilized OpAMP during the amplification phase Φ_A, highlighting the main transfer function $A(s)$, the sub-blocks transfer functions $A_M(s)$ (main amplifier, amplification path), $A`_M(s)$ (main amplifier, offset stabilization path) and $A_F(s)$ (auxiliary amplifier, amplification path).

Furthermore, the main amplifier output in the schematic is capacitively loaded to stress the presence of an output pole, while the auxiliary amplifier output is by default loaded by the hold capacitors C_M, denoting the presence of another pole. Under the hypothesis that

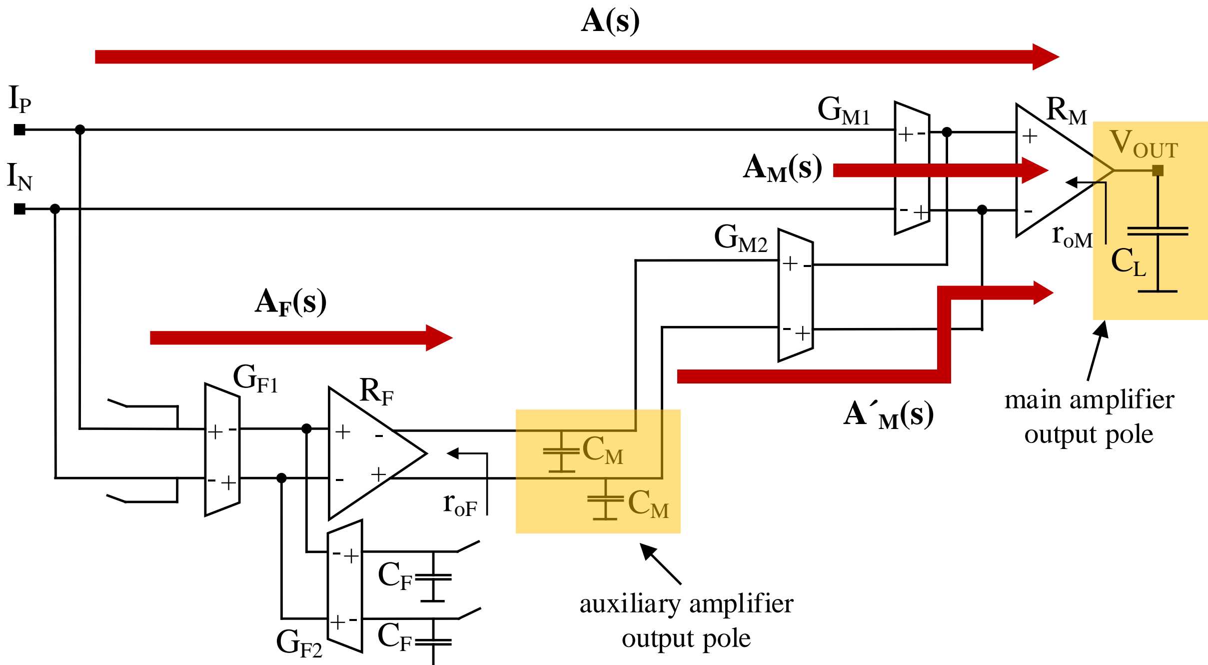

FIGURE 4.18: Auto-zero offset stabilized OpAMP schematic (phase Φ_A). highlights of the sub-blocks transfer functions and poles.

each amplification path in the topology can be modelled as a two pole system, the following equations hold.

$$A_M(s) = \frac{A_{Mo}}{(1 + \frac{s}{\omega_{Md}})(1 + \frac{s}{\omega_{Mh}})} \tag{4.25}$$

$$A`_M(s) = \frac{A`_{Mo}}{(1 + \frac{s}{\omega_{M`d}})(1 + \frac{s}{\omega_{M`h}})} \tag{4.26}$$

$$A_F(s) = \frac{A_{Fo}}{(1 + \frac{s}{\omega_{Fd}})(1 + \frac{s}{\omega_{Fh}})} \tag{4.27}$$

$$A(s) = A_M(s) + A_F(s)\, A`_M(s) \tag{4.28}$$

In (4.25), (4.26) and (4.27), subscripts d and h denotes the dominant and the high frequency pole respectively, subscript o denotes the DC transfer gain of each sub-block while $A`_M(s)$ denotes the transfer function from the compensation port to the output of the main amplifier A_M. First it is noticeable that, for the considered topology, transconductance stages G_{M1} and G_{M2} are loaded by the same stage R_M, therefore it is possible to state that transfer functions

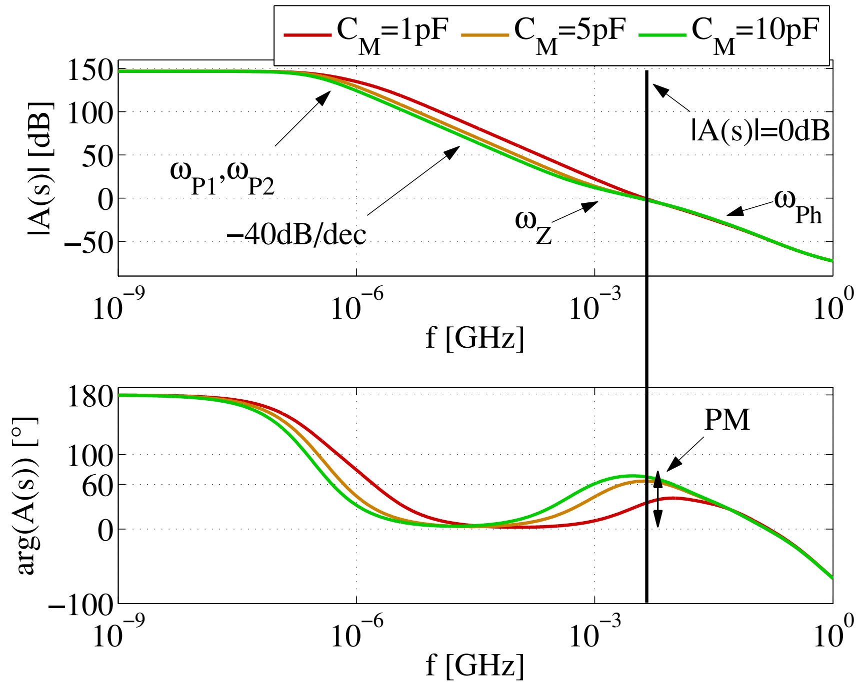

FIGURE 4.19: Auto-zero offset stabilized OpAMP schematic open loop transfer function simulation result during the amplification phase Φ_A. Hold capacitors C_M are parametric, while the output capacitance C_L is set at $10pF$.

$A_M(s)$ and $A`_M(s)$ have the same frequency response:

$$\omega_{M`d} \equiv \omega_{Md}\,;\, \omega_{M`h} \equiv \omega_{Mh} \tag{4.29}$$

It is possible, in general, to write each pole considering the capacitance and output resistance for each stage. Following this approach and calling r_{oM} and r_{oF} the output resistances of the main and auxiliary amplifiers output stages respectively, the dominant poles can be expressed as:

$$\begin{aligned} \omega_{Md} &= \frac{1}{r_{oM}\, C_L} \\ \omega_{Fd} &= \frac{1}{r_{oF}\, C_M} \end{aligned} \tag{4.30}$$

Taking into account (4.29), the whole offset-stabilized amplifier transfer function can be expressed as:

$$A(s) = \frac{A_{Mo}(1+\frac{s}{\omega_{Fd}})(1+\frac{s}{\omega_{Fh}}) + A_{Fo}\, A`_{Mo}}{(1+\frac{s}{\omega_{Md}})(1+\frac{s}{\omega_{Mh}})(1+\frac{s}{\omega_{Fd}})(1+\frac{s}{\omega_{Fh}})} \tag{4.31}$$

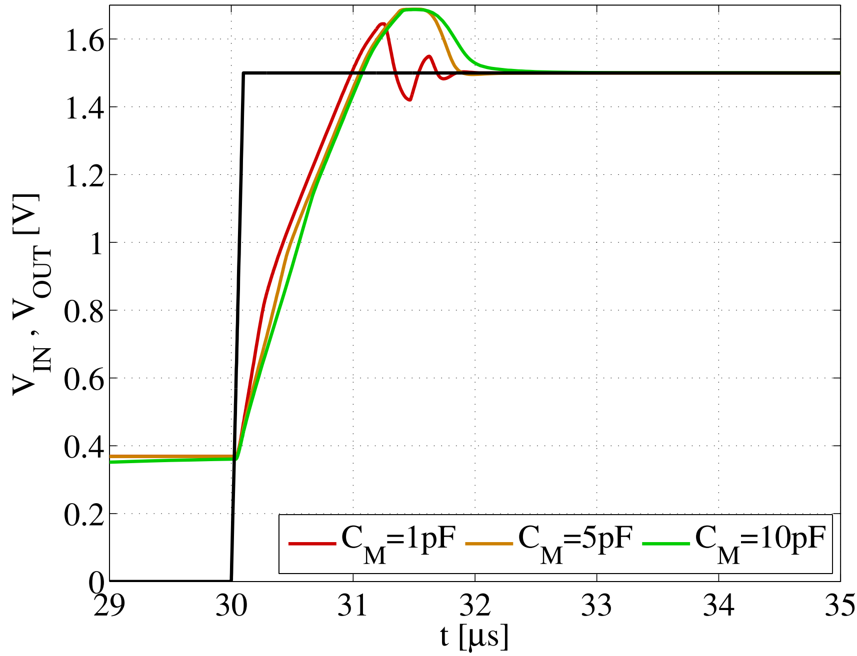

FIGURE 4.20: Auto-zero offset stabilized OpAMP schematic step response parametric simulation result during the amplification phase Φ_A. Hold capacitors C_M are parametric, while the output capacitance C_L is set at 10pF. The amplifier is connected as a voltage buffer and the input step goes from $0V$ to $1.5V$ at $t = 30\mu s$.

Transfer function (4.31) can be simplified with the aid of a further consideration. Independently from the topology employed to design the stages of the offset-stabilized amplifier, it is allowed to assume that, the A_F stage being fully differential, its high frequency pole is located at higher frequency compared to the high frequency pole of the main stage A_M:

$$\omega_{Fh} >> \omega_{Mh} \tag{4.32}$$

This assumption comes from the fact that, the main stage A_M being single ended, it will most probably suffer from the presence of a mirror pole at its output stage ([54]). The mirror pole will generally be located at a lower frequency with respect to the high frequency pole of the fully differential auxiliary amplifier, therefore, in first approximation, such a pole can be neglected for the calculation of the total transfer function. For the sake of the analysis, the following simplifications can also be taken into account:

$$A_{Fo}\, A`_{Mo} >> A_{Mo}\,;\; A_{Fo} \simeq A_{Mo} \tag{4.33}$$

If the assumption (4.33) are valid, (4.30) can be simplified as:

$$A(s) \simeq [A_{Mo} + A_{Fo}\, A`_{Mo}]\, \frac{1 + \dfrac{s}{A`_{Mo}\,\omega_{Fd}}}{(1+\dfrac{s}{\omega_{Md}})(1+\dfrac{s}{\omega_{Mh}})(1+\dfrac{s}{\omega_{Fd}})} \tag{4.34}$$

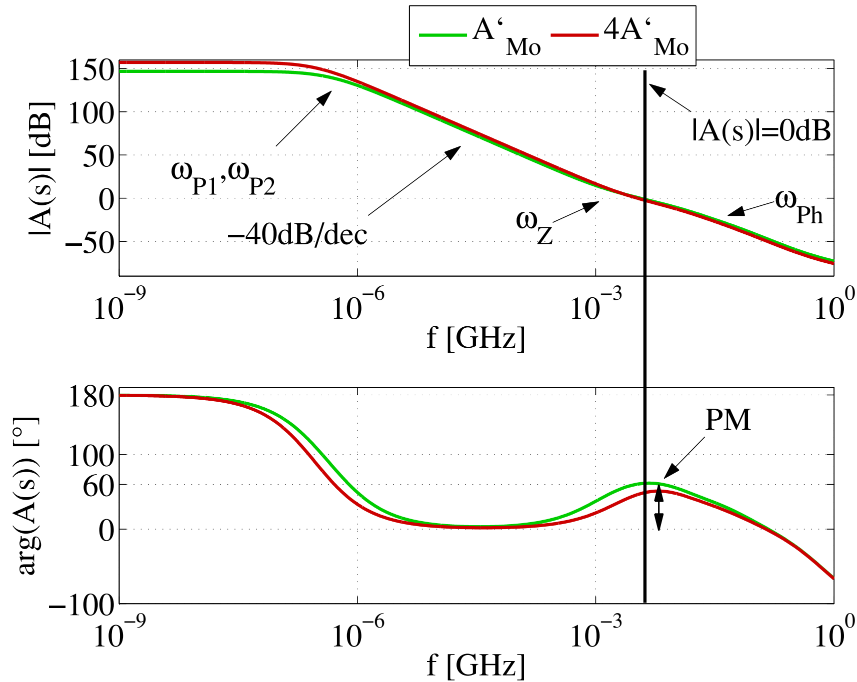

FIGURE 4.21: Auto-zero offset stabilized OpAMP schematic open loop transfer function simulation result during the amplification phase Φ_A. Main amplifier control port gain $A`_{Mo}$ is parametric, while the output capacitance C_L is set at 10pF and the hold capacitors C_M are set to $4pF$.

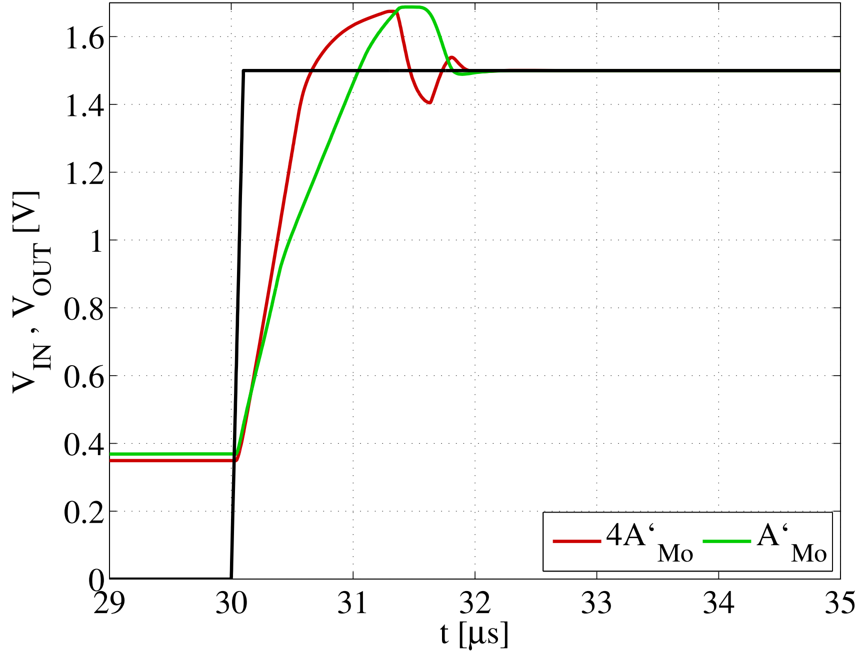

FIGURE 4.22: Auto-zero offset stabilized OpAMP schematic step response parametric simulation result during the amplification phase Φ_A. Hold capacitors C_M is set at $4pF$ while the output capacitance C_0 is set at $10pF$. The main amplifier control port gain $A`_{Mo}$ is parametric The amplifier is connected as a voltage buffer and the input step goes from $0V$ to $1.5V$ at $t = 30\mu s$.

As it is possible to note from (4.34), even if the main and auxiliary amplifier are designed to be stable with one pole dominant stability, their parallel combination can generate a potentially unstable system with two low frequency poles, one low frequency zero and one high frequency pole:

$$\begin{aligned}
\omega_{P1} &= \omega_{Md} \\
\omega_{P2} &= \omega_{Fd} \\
\omega_{Ph} &= \omega_{Mh} \\
\omega_Z &= A`_{Mo}\,\omega_{Fd}
\end{aligned} \tag{4.35}$$

Beside the variety of possible scenarios concerning bandwidth and stability, the present Ph.D. work focuses on the case where a substantial capacitive load C_L is present at the output of the main amplifier. Fig. 4.19 shows a plot of the simulated transfer open loop gain $A(s)$ in magnitude and phase of a real design (see seciotn 4.2.5), with parametric values of the hold capacitors C_M which define the auxiliary amplifier dominant pole ω_{Md}, in order to highlight the main aforementioned characteristics of such transfer function. As it is possible to note, variations of the capacitors C_M cause a frequency shift either of the auxiliary amplifier dominant pole ω_{Md} (through (4.30)), but also of the low frequency zero ω_Z (see (4.35)). The presence of ω_Z raises the phase after the drop due to the two low frequency poles. This phase raise is what

prevents the phase to drop to $0°$ when the magnitude reaches $0\mathrm{dB}$, hence it avoids the amplifier instability according to the Barkhausen's criteria. In particular, the phase margin of the whole amplifier is strictly related to the spacing between the two low frequency poles and the zero: as it is possible to note in Fig. 4.19, increasing the value of C_M lowers either the low frequency pole ω_{Fd} and the zero ω_Z, but the zero becomes more effective as it gets farther from the high frequency poles, thereby increasing the phase margin PM. This effect is also testified by the plot in Fig. 4.20, which depicts a transient step simulation of the auto-zero offset stabilized OpAMP in the same parametric conditions of Fig. 4.19 ($C_M = (1\mathrm{pF}, 5\mathrm{pF}, 10\mathrm{pF})$) while connected as a voltage buffer (Fig. 4.11). Higher values of C_M increase the phase margin but slow down the time response of the amplifier.

To further prove the aforementioned discussion, another set of simulations has been performed varying the DC gain of the main amplifier through its control port, $A`_{Mo}$, so to shift also the zero $\omega_Z$, as shown in Fig. 4.21. The control port gain $A`_{Mo}$ in the simulation has been varied without modifying any of the other parameters involved in the frequency response of the amplifier. In particular, one simulation is performed with the nominal value of $A`_{Mo}$, while another one is performed with four times this value by increasing only the transconductance of the stage G_{M2}, so not to change r_{oM}.

As it is possible to note, increasing the gain $A`_{Mo}$ modifies the DC gain of the whole OpAMP, but also changes the frequency response by shifting the zero to higher frequencies and degrading the phase margin. This effect is also testified by the parametric simulation result in Fig. 4.22, showing a step response of the amplifier connected as a voltage buffer (Fig. 4.11) and in the same parametric conditions of Fig. 4.20.

4.2.5 Implementation

To complete the analysis, this section shows how the CMOS auto-zero offset stabilized OpAMP has been implemented on silicon concerning the topology choices. The circuit in Fig. 4.23 depicts the main amplifier schematic. It is a single ended folded cascode amplifier with nMOS main input pair (G_{M1}). The compensation port G_{M2} is made of another nMOS differential pair connected in parallel to the main one.

The output single ended cascode stage represents the transresistance stage R_M depicted in Fig. 4.6, Fig. 4.12 and Fig. 4.18. The design of the main amplifier, concerning the offset cancellation, mainly involves the ratio N_M between the compensation and the main transconductance differential pairs. Depending on the operating region, this ratio can be controlled either by transistor sizes, tail bias currents or a combination of both.

The picture in Fig. 4.24 depicts the auxiliary amplifier schematic with all the switched capacitors part of the circuit. Concerning the topology, the auxiliary amplifier is a differential

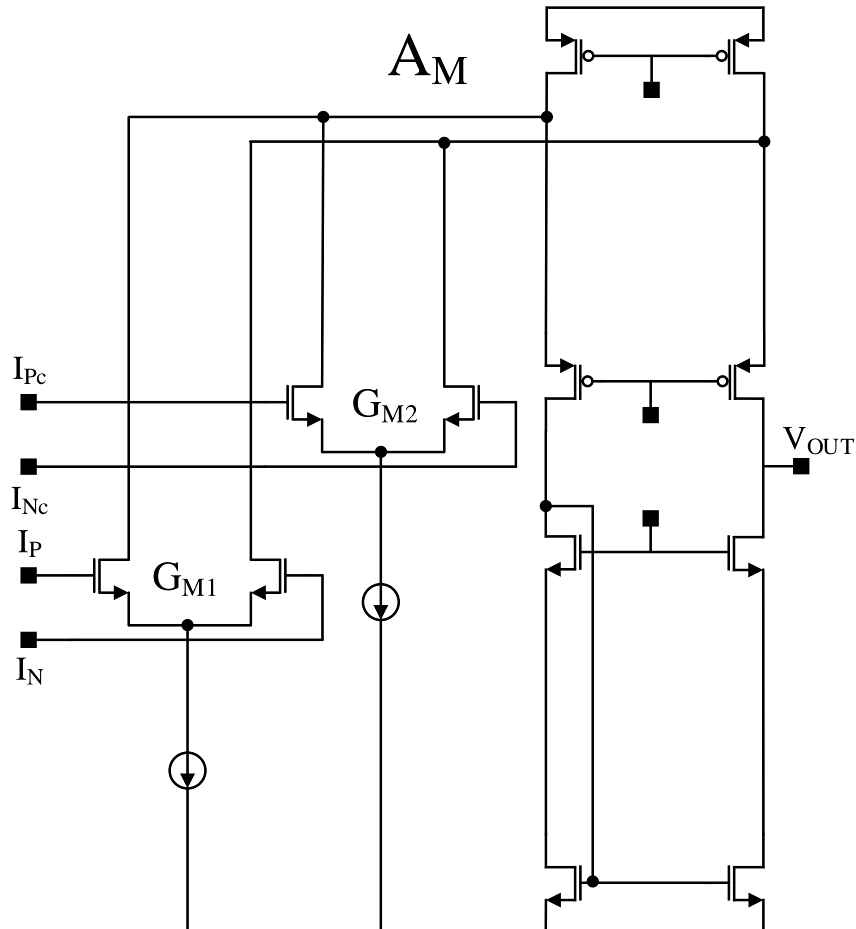

FIGURE 4.23: Main amplifier schematic. The input of the transconductance pair G_{M2} represent the compensation port input of the amplifier (port COMP in Fig. 4.5).

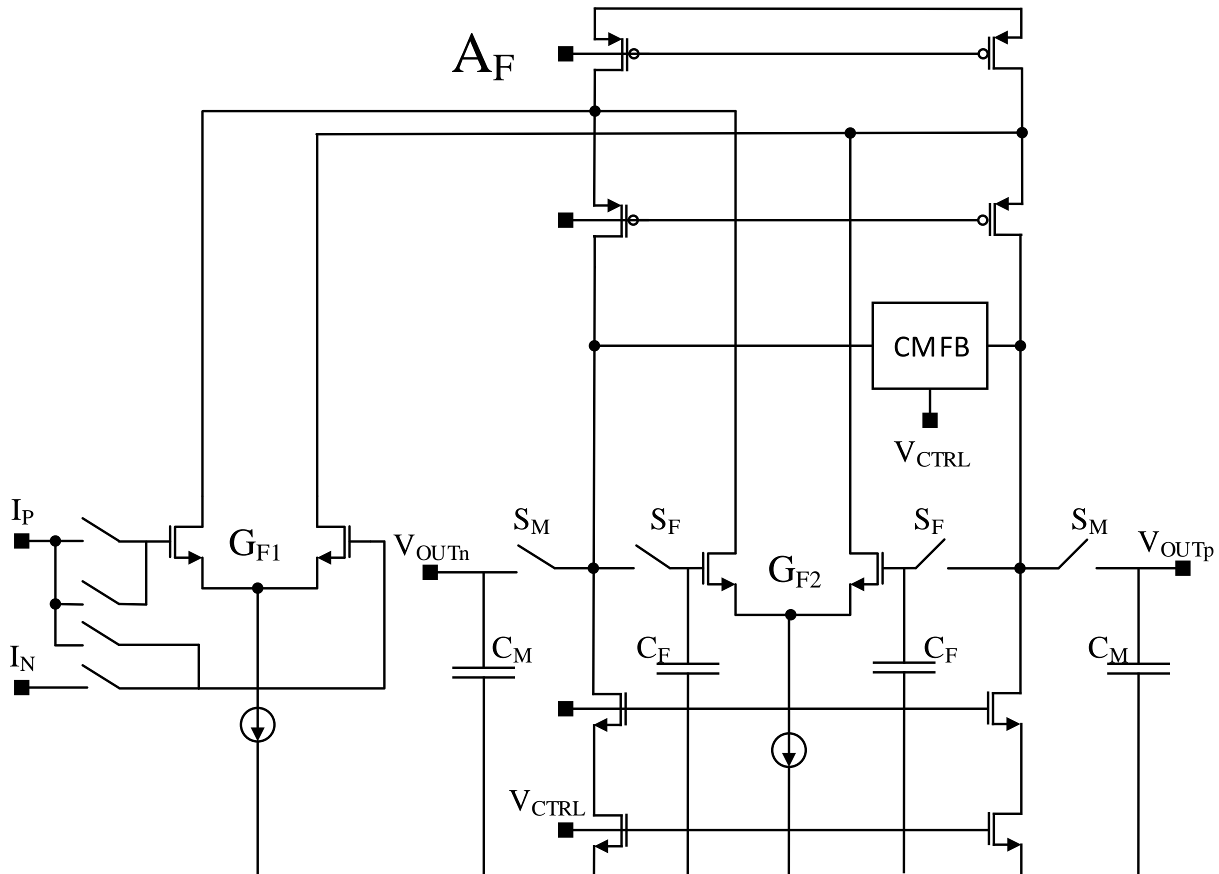

FIGURE 4.24: Auxiliary amplifier schematic. The input of transconductance pair G_{F2} represent the compensation port input of the auxiliary amplifier and it is connected to the amplifier output via switches S_F (Fig. 4.14).

folded cascode OpAMP with nMOS input and compensation pairs. Since both main and auxiliary OTA are based on the folded cascode topology, which can be considered as single pole system with good approximation, equations (4.25), (4.26), (4.27) and (4.28) are valid. Table 4.1 lists the numeric parameters of the amplifier designed for the purpose of the analysis. It is possible to note from the values that hypothesis (4.13) is valid. The offset compensation is achieved through another differential pair connected in parallel to the main one, in the same shape as the main amplifier. The design choice of using the very same topology and compensation port type for the main and the auxiliary amplifier is not casual. As it is shown in Section 4.2.2, under certain assumptions the residual offset can be minimized if the ratios N_M and N_F are equal. Employing the same topology for G_{M1}, G_{M2}, G_{F1} and G_{F2} greatly helps in keeping a certain degree of control and matching among the transconductance ratios, also from a layout perspective.

TABLE 4.1: Auto-Zero offset stabilized OpAMPs performance parameters

Parameter	Description	Value (typ.)
$G_{M1}[\mu S]$	Main OTA main transconductance	218
$G_{F1}[\mu S]$	Auxiliary OTA main transconductance	218
$G_{M2}[\mu S]$	Main OTA compensation transconductance	21
$G_{F2}[\mu S]$	Auxiliary OTA compensation transconductance	21
$A_{M0}[dB]$	Main OTA open loop DC gain	82
$A'_{M0}[dB]$	Main OTA compensation port DC gain	59
$A_{F0}[dB]$	Auxiliary OTA open loop DC gain	81
$A'_{F0}[dB]$	Auxiliary OTA compensation port DC gain	60
$A_0[dB]$	Overall OpAMP DC gain	148
$GBW[MHz]$	Overall OpAMP 0db crossover frequency	5.5
$PM[°]$	Overall OpAMP Phase Margin	76
$C_M[pF]$	Main OTA hold capacitors	5
$C_F[pF]$	Auxiliary hold capacitors	5
$I_{DD}[\mu A]$	Overall OpAMP DC current consumption	116

4.3 Modelling of the EMI induced offset for auto-zero offset stabilized OpAMPs

The EMI induced offset generation mechanism into an auto-zero offset stabilized topology can be analyzed by making the following considerations. Considering the amplifier only during the auto-zero phase Φ_Z, it is possible to recognize that, concerning the EMI path, the amplifier in this condition does not differ from a standard continuous time amplifier, like the one depicted in Fig. 2.5. This aspect is highlighted in Fig. 4.25, which shows the auto-zero offset stabilized topology during the amplification phase and the EMI injection path. During the auto-zero phase Φ_Z, the auxiliary amplifier is detached from the input and performs the auto-zero of its own technological offset. The main amplifier, which is always connected to the input, experience the nominal input voltage and the EMI voltage, generating then a DC EMI induced offset $V_{OS_emi_M}$ following the exact same mechanisms discussed in Chapter 2.

In such conditions it is then possible to state that, ideally, the auxiliary amplifier is completely not affected by EMI and its nominal auto-zeroing operation is performed undisturbed. This is because, even if the EMI is conducted to the input af the auxiliary amplifier, it is conducted in a purely common mode way. Looking again at expression (2.3), it is possible to

observe that the EMI induced offset current in a differential pair can only appear in presence of both common and differential mode EMI voltages. In such a case, the differential mode component of the EMI through the auxiliary amplifier is null, hence no differential offset current should be generated by the differential stage G_{F1}.

In reality, such analysis represents an approximation, since, due to its finite common mode to differential mode rejection, differential stage G_{F1} generates anyway a small amount of differential current thorough a common mode variation of its input voltage due to EMI.

This differential current mixes up with the common mode current generating a DC EMI induced current as stated in Chapter 2. For the sake of the present analysis it is anyway worth it to neglect this effect and to make the hypothesis that no EMI induced offset is generated into the auxiliary amplifier during the auto-zero phase. The schematic in Fig. 4.26 shows what happens to the amplifier subjected to input EMI during the amplification phase Φ_A. The most important aspect to understand is what happens to the EMI induced offset in the main amplifier when the auxiliary amplifier is connected in parallel. In this case, the main amplifier EMI induced offset $V_{OS_emi_M}$ is a DC offset undistinguishable from the main transconductance stage offset V_{OS_M1}. Therefore the offset stabilization mechanism senses such EMI error contribution in the same way it senses the main transconductance stage offset and compensates for it according to (4.15):

$$V_{IN_OS}|_{\Phi_{A_emi_M}} \simeq \pm \frac{G_{M1}/G_{M2}}{A_F}\left(V_{OS_M1} + V_{OS_emi_M}\right) \tag{4.36}$$

On the other hand, the EMI induced offset generated in the auxiliary amplifier main differential stage G_{F1} propagates to the output without any compensation, since the auto-zero mechanism is not active during the amplification phase Φ_A. This offset contribution, $V_{OS_emi_F}$,

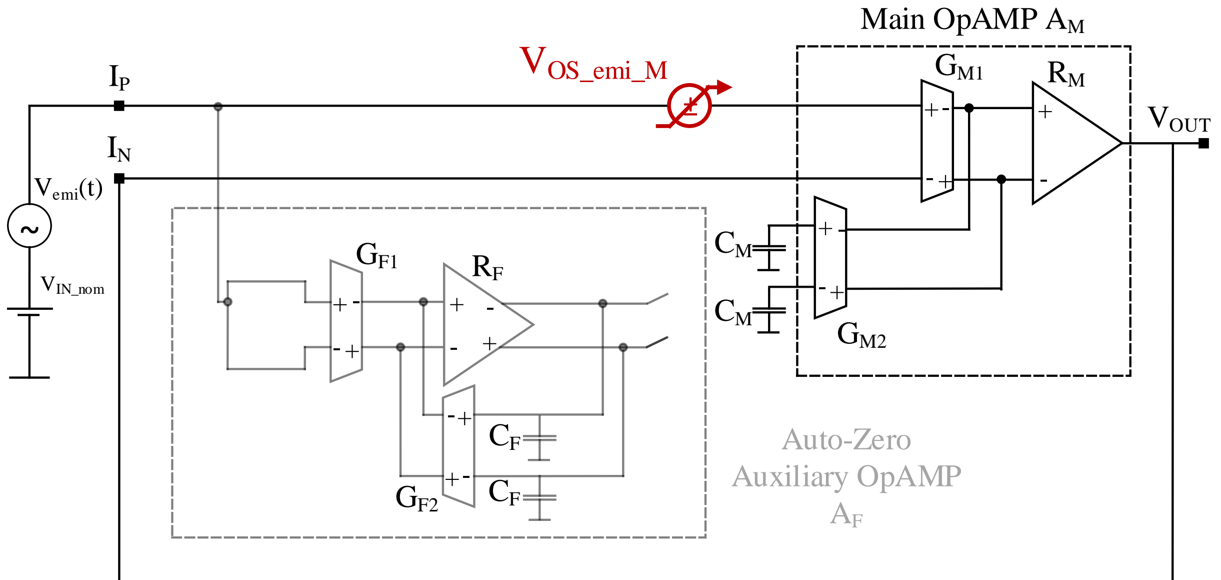

FIGURE 4.25: Auto-zero offset stabilized OpAMP EMI induced offset generation during the auto-zero phase Φ_Z.

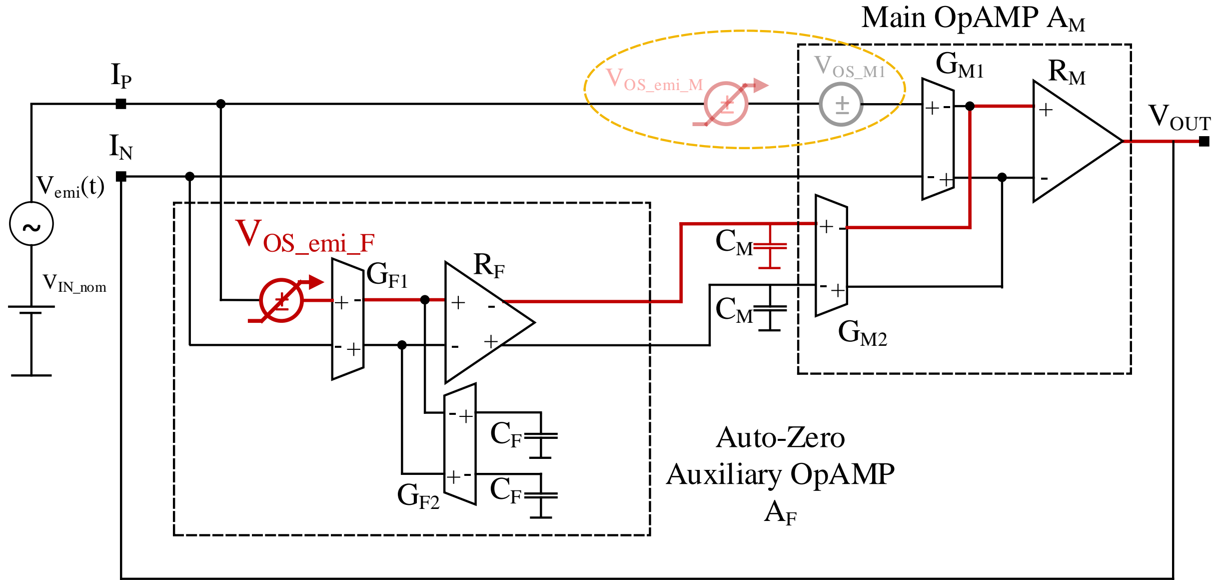

FIGURE 4.26: Auto-zero offset stabilized OpAMP EMI induced offset generation during the amplification phase Φ_A.

appears as a DC error at the amplifier output and is also stored on the capacitors C_M. For this reason, in steady state conditions, this offset remains at the main amplifier output since, even if during the following auto-zero phase the auxiliary amplifier is detached from the input, the EMI contribution generated in G_{F1} stays stored, differentially, on capacitors C_M and remains constant at the whole amplifier output if the input EMI does not change its characteristics (Fig. 4.27). According to the aforementioned considerations it is then possible to state that the EMI induced offset in an auto-zero offset stabilized OpAMP is, in first approximation, equal to the

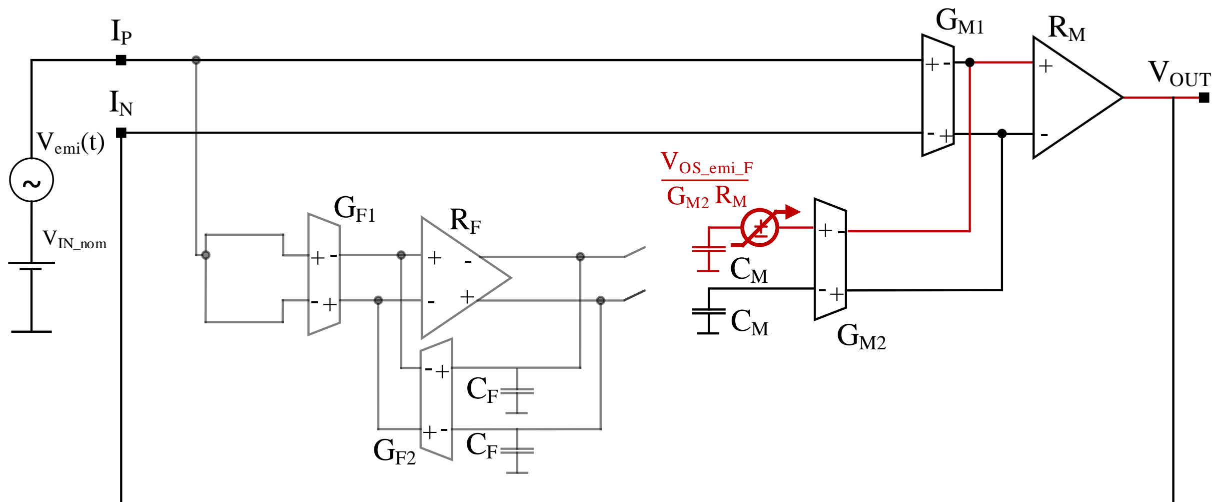

FIGURE 4.27: Auto-zero offset stabilized OpAMP EMI induced offset generation at steady state after the transition from amplification to auto-zero phase.

EMI induced in the auxiliary OpAMP. Such offset contribution can be evaluated employing all the known models discussed in Chapter 2 for standard continuous time OpAMPs:

$$V_{OS_emi}|_{TOT} \simeq V_{OS_emi_F} \tag{4.37}$$

It must be pointed out that, during the amplification phase Φ_A, the auxiliary amplifier is connected to the input via closed switches. For this reason, the modeling of the EMI induced offset in this case should take into account also the on-resistance of these switches in the same way as it has been done for chopped OpAMPs. The EMI induced offset modeling can then be done with more accuracy employing the model (3.4), (3.5) and (3.6) applied for the auxiliary amplifier.

4.3.1 EMI hardening of auto-zero offset stabilized OpAMPs

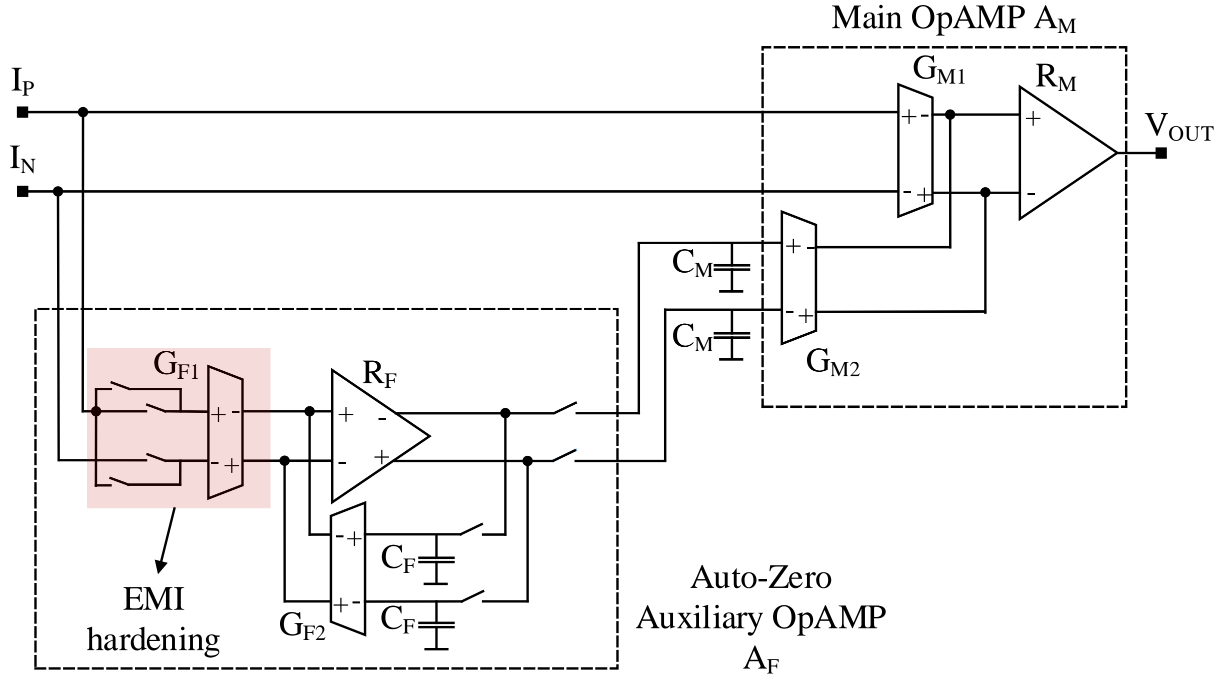

FIGURE 4.28: EMI hardening concept drawing for auto-zero offset stabilized operational amplifiers.

Given the results in Section 4.3 it is possible to state that the EMI hardening of auto-zero offset stabilized OpAMPs mainly concerns the auxiliary amplifier, which is the principal responsible for the DC EMI induced offset appearing at the output of the whole amplifier as a consequence of input EMI injection.

Being, in this case, the auxiliary amplifier a standard continuous time OpAMP, all the techniques known in the literature and listed in Section 2.1.2 are in principle applicable and can be used to harden the auxiliary amplifier input stage G_{F1} (Fig. 4.28). Although the present Ph.D. research cannot provide validation results on a physical EMI hardened auto-zero offset stabilized amplifier, the validation of the root causes of the EMI induced offset for such kind of topologies is proved in the next section and furnishes a solid basis to confirm the aforementioned statement.

It is anyway clear that auto-zero and offset stabilization cannot provide any compensation for the EMI induced offset as they do for the technological one. Although the EMI induced offset in the main amplifier ($V_{OS_emi_M}$) is compensated by the effect of the auxiliary amplifier, the EMI induced offset generated into the auxiliary amplifier itself propagates to the output regardless of the offset compensation technique employed, being it auto-zeroing, as in this case, or chopping.

4.4 Validation

The present Section provides a brief description of the auto-zero offset stabilized operational amplifier designed and fabricated in a $0.35\mu m$ CMOS technology for the purpose of the analysis and furnishes the measurement data comparing them with the model and simulation results in order to validate the concepts highlighted in Section 4.2 and Section 4.3.

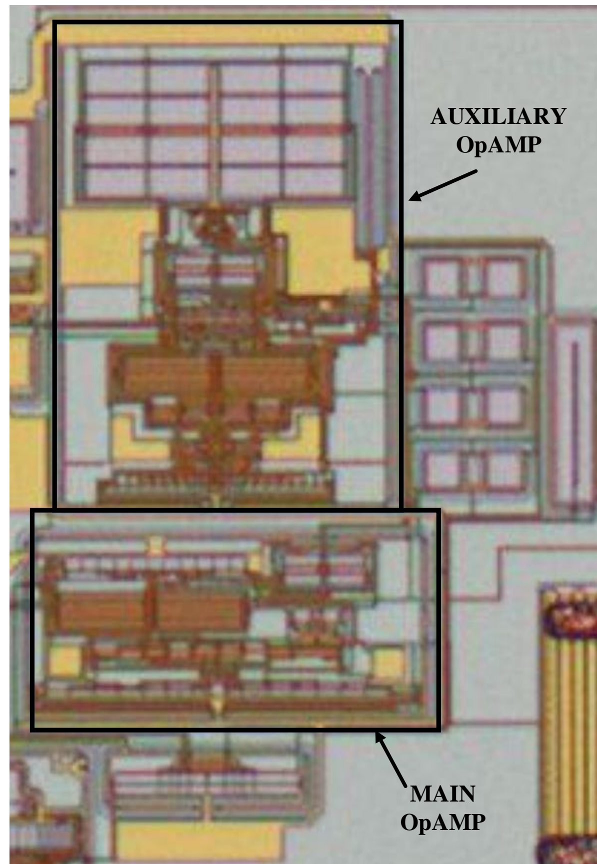

FIGURE 4.29: Photomicrograph of the auto-zero offset stabilized amplifier.

The photomicrograph of the auto-zero offset stabilized amplifier implemented according to Section 4.2.5 is depicted in Fig. 4.29, while Table 4.2 provides the OpAMP nominal performance parameters. The amplifier is internally connected as a voltage buffer, it has been designed so to have equal transconductance ratios ($N_M = N_F \simeq 0.12$) and is provided with $4pF$ capacitor couples for C_M and C_F, while the auto-zero clocking is performed with two phases at $200kHz$. The design of the amplifier has been carried out following the concepts expressed in Sections 4.2.2 and 4.2.4, targeting a sigma residual offset of $10\mu V$, reachable in less than $10\mu s$.

The histogram plot in Fig. 4.30 depicts the measured technological offset of seventeen samples of the fabricated amplifier. As it is possible to note, the sigma for the residual offset voltage can be estimated of around $5\mu V$, while none of the designed and tested devices experienced a residual offset greater than $10\mu V$.

TABLE 4.2: Auto-zero Offset Stabilized OpAMP Performance Parameters

$I_{DD}[\mu A]$	$GBW[MHz]$	$PM[°]$	DC Gain [dB]
206	5.4	58	148

The considerations and modelling of the OpAMP behaviour concerning EMI is instead validated according to the following approach. Since the EMI induced offset for the whole amplifier is supposed to be generated only by the auxiliary amplifier, the evaluation of such offset has been carried out according to the same model used for chopped OpAMPs, considering an nMOS differential pair with MOS based switches series connected at the gate site (Fig. 3.8).

The model parameters have been evaluated for the main transconductance stage G_{F1} of the auxiliary amplifier and plugged into model (3.4), (3.5) and (3.6) to obtain the EMI induced offset generated only by the auxiliary amplifier. Secondly, two set of simulations have been performed. In the first set, the EMI has been injected only at the main amplifier input, leaving the auxiliary amplifier biased but detached from the input path (Fig. 4.31). In the second set, the EMI has been injected only at the auxiliary amplifier input and superimposed to the same input nominal signal of the main amplifier (Fig. 4.32). By doing so it has been possible to highlight, separately, the independent effects of EMI on the main and auxiliary amplifiers at

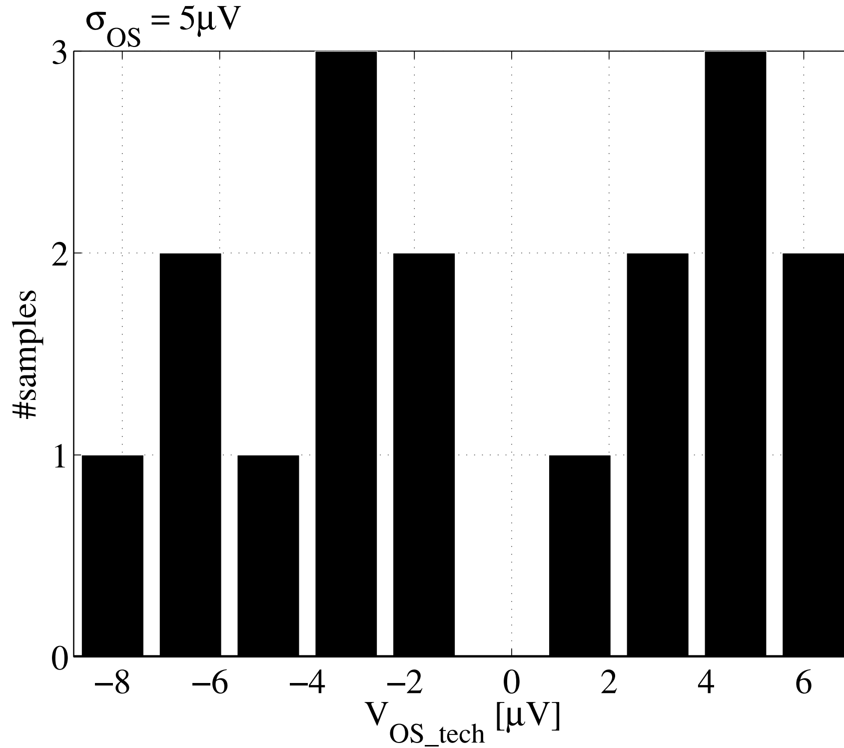

FIGURE 4.30: Measured technological offset V_{OS_tech} for 17 samples of the fabricated auto-zero offset stabilized amplifier.

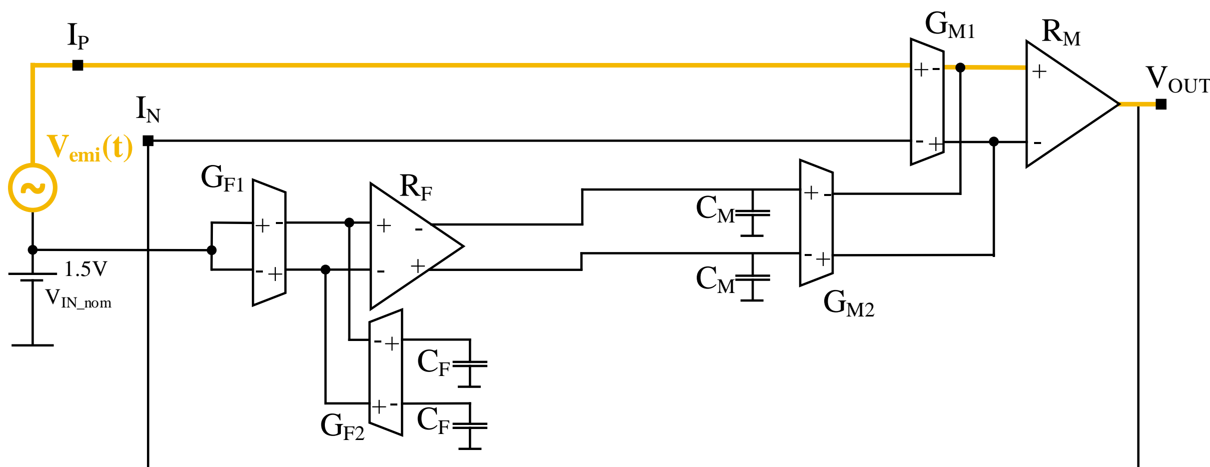

FIGURE 4.31: Simulation setup for the EMI injection at the main amplifier input only. Yellow highlight of the EMI path. The auxiliary amplifier is biased a at the nominal input voltage (1.5V), it is out of the loop and does not experience any EMI.

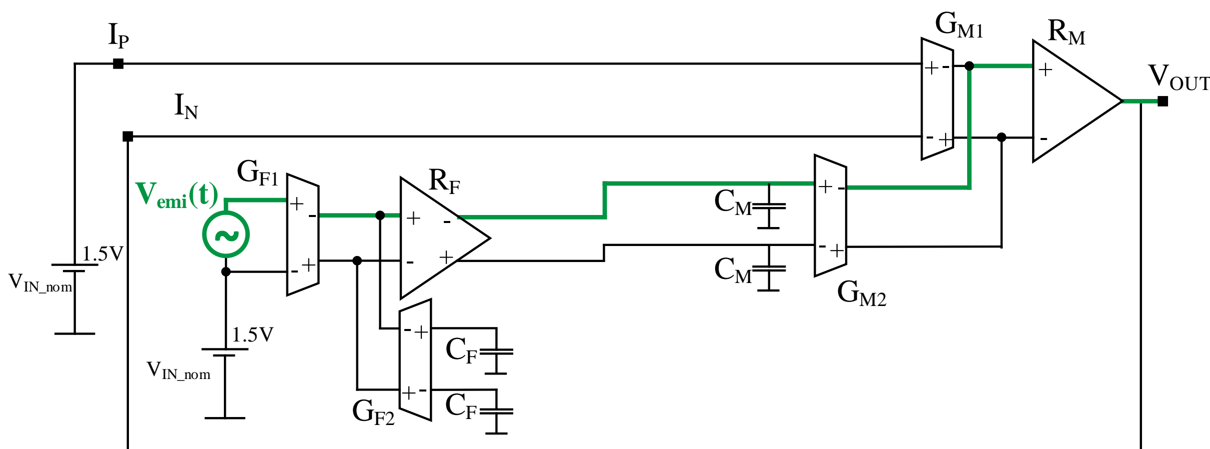

FIGURE 4.32: Simulation setup for the EMI injection at the auxiliary amplifier input only. Green highlight of the EMI path. The auxiliary amplifier is biased a at the nominal input voltage (1.5V) with the superimposed EMI voltage and it is out of the loop, while the main amplifier is buffer connected and fed with the nominal input voltage only.

the output. Lastly, the EMI has been injected at PCB level (see Fig. 5.19 in Chapter 5) and the average output voltage has been measured in order to evaluate the EMI induced offset generated for the whole clocked amplifier.

The picture in Fig. 4.33 shows the four results of the aforementioned tests. As it is possible to note, the model result and the simulation result of the EMI injection in the auxiliary amplifier match quite accurately and, more interestingly, they also match with the EMI induced offset result of the measurement injection performed on the whole clocked OpAMP at PCB level, validating the aforementioned analysis. Furthermore, the yellow line in Fig. 4.33 depicts a

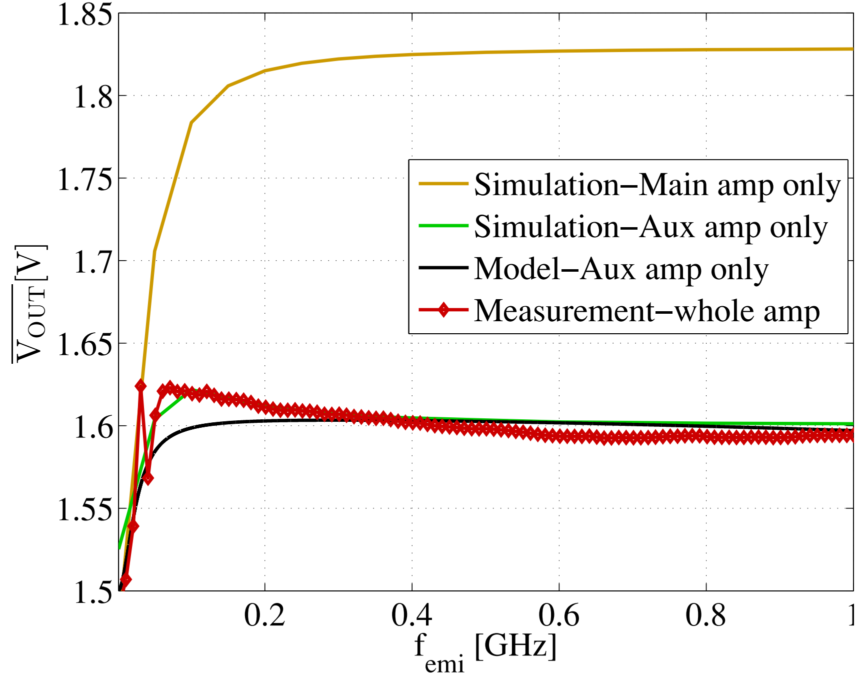

FIGURE 4.33: Modelled (black continuous line), simulated (yellow continuous line for main OpAMP only and green continuous line for auxiliary OpAMP only) and measured (red diamond line for the whole clocked auto-zero offset stabilized OpAMP) average output voltage with $P_{emi} = -2dBm$ ($A_{emi} \simeq 100mV_{pk}$). The EMI injection frequency step in the measurement and simulations is 10MHz. The immunity test is performed at PCB level.

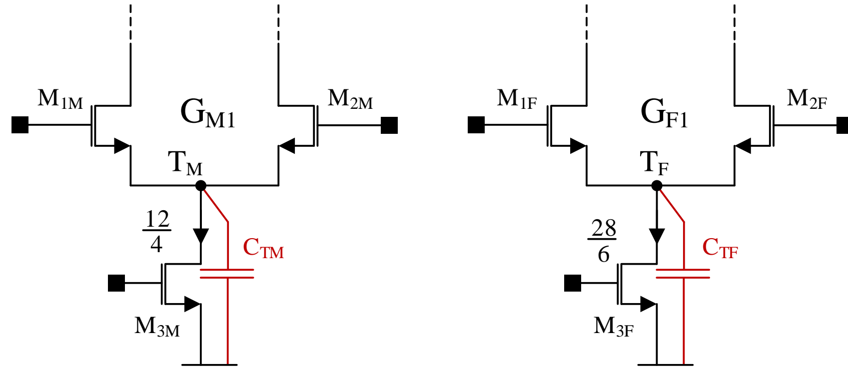

FIGURE 4.34: Main and auxiliary amplifiers input stages. The differential pair transistors are sized equally ($M_{1M} = M_{2M} = M_{1F} = M_{2F}$), while the tail transistor M_{3F} of the auxiliary amplifier main transconductance stage G_{F1} is roughly 3.5 times smaller than the tail transistor M_{3M} of the main amplifier main transconductance stage G_{M1}.

simulation result of the injection in the main amplifier only according to Fig. 4.31.

The DC shift experienced by only the main amplifier is different and greater than the one

experienced by the auxiliary amplifier and by the parallel combination of the two. This is because the main and auxiliary amplifier have been designed on purpose to generate a different amount of EMI induced offset. In particular, in order not to change the designed transconductance ratios, the EMI susceptibility of the amplifiers has been shaped changing the size of the tail node transistors among the differential stages G_{M1} and G_{F1}, as depicted in Fig. 4.34. Even without a complex layout analysis like the one carried out in Section 2.1.1, it is anyway very interesting to compare the simulation result of the EMI injection into the main amplifier only (yellow line in Fig. 4.33) and the measurement result of the injection in the whole amplifier (red diamond line in Fig. 4.33). Under the hypothesis that the tail parasitic capacitance is linearly dependent on the tail node transistor area and recalling from (2.6) that the tail node parasitic capacitance value strictly affects the amount of EMI induce offset, it is interesting to note that the area ratio of the tail node transistor of the main and auxiliary amplifiers is very close to the ratio of the EMI induced offset experienced by the main and the auxiliary amplifier at high frequency:

$$\frac{(WL)|_{3F}}{(WL)|_{3M}} \simeq 3.5 \leftrightarrow \frac{V_{OS_emi_HF}|_{MAIN\,amp}}{V_{OS_emi_HF}|_{AUX\,amp}} \simeq 3.25 \tag{4.38}$$

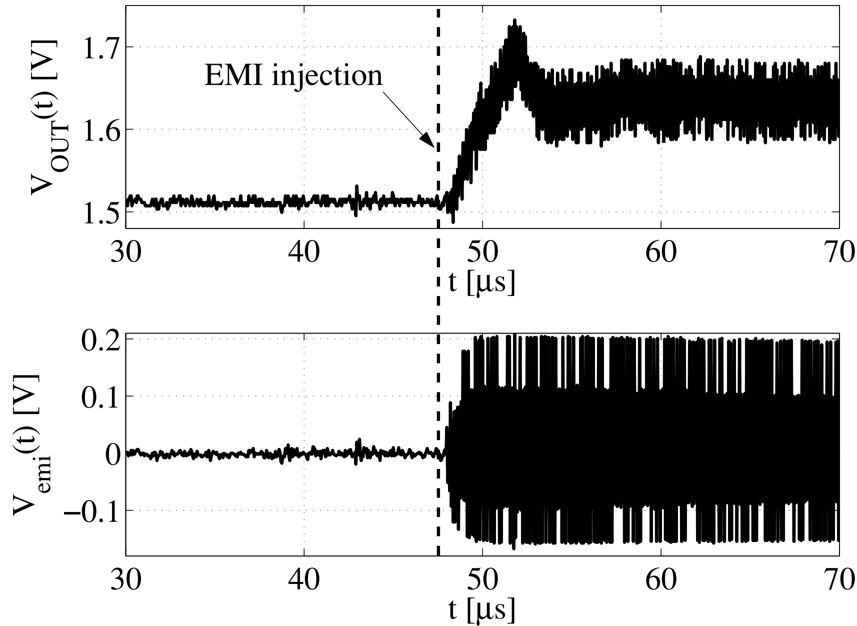

FIGURE 4.35: Measured output voltage with $P_{emi} = -2dBm$ ($A_{emi} \simeq 500mV_{pk}$) and $f_{emi} = 50MHz$, with a nominal input DC voltage of $1.5V$. The measurement has been performed with the oscilloscope by triggering in single mode the output signal just above the input nominal voltage. The DC shift experienced by the output voltage because of non linear distortion increases but then drops after a few microseconds, indicating the effect of the auxiliary amplifier compensating for the EMI induced offset in the main amplifier.

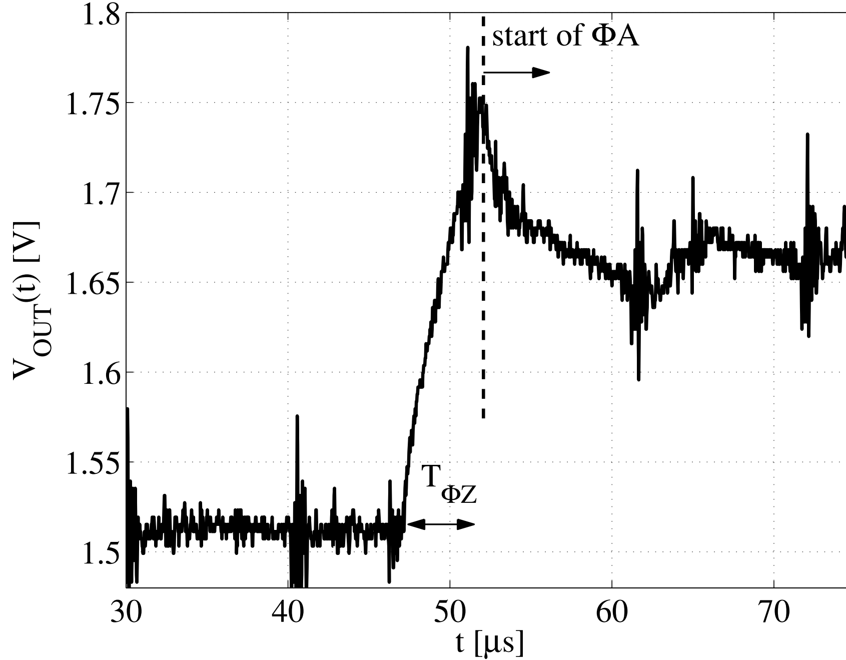

FIGURE 4.36: Measured output voltage with $P_{emi} = -2dBm$ ($A_{emi} \simeq 500mV_{pk}$) and $f_{emi} = 200MHz$, with a nominal input DC voltage of $1.5V$. The measurement has been performed in the same way as the one of Fig. 4.35. The DC shift experienced by the output voltage because of non linear distortion increases but then drops after about $2.5\mu s \simeq T_{\Phi_Z}$, indicating that the DC shift experienced by the main amplifier starts to take place at $t = 48\mu s$ but then, as soon as the OpAMP goes into the amplification phase Φ_A, such DC shift is lowered since it becomes dependent only by the auxiliary amplifier.

As a consequence, it is possible to confirm that if the EMI induced offset of the whole auto-zero offset stabilized amplifier would have been dependent on the characteristics of the main amplifier input stage, such EMI induced offset value, once measured, should have been close to the yellow line of Fig. 4.33, while in reality it is more than three times smaller due to the fact that it depends mostly on the characteristics of the auxiliary amplifier input stage, which, by design, generates a lower amount of EMI induced offset due to its smaller tail node transistor.

In order to highlight the dynamic behaviour of the auto-zero offset stabilized OpAMP subjected to input EMI and to further confirm the previous analysis, time domain measurements have been performed by checking the amplifier output during the disturbances injection. The plot in Fig. 4.35 shows a measurement result performed by checking the amplifier output through an oscilloscope while injecting a $50MHz$ interference at its input. As it is possible to note from the picture, the amplifier output starts rising after $t = 48\mu s$ due to the generation of the EMI induced offset. Strangely, after a few microseconds, the amplifier output experiences a drop and its DC value gets steady and DC shifted at roughly $1.65V$. In order to enhance the clearness of such behaviour, another measurement has been performed in the same way while injecting a $200MHz$ input disturbance, so to get farther from the amplifier bandwidth.

The result of such measurement is shown in Fig. 4.36. The picture highlights two important

characteristics of the amplifier while injected with input EMI. First, it is possible to note how the amplifier output is rising after the injection starts at $t \simeq 48\mu s$. Since the steady value of the DC shifted output decreases after such rise, it is plausible that the amplifier is in the auto-zero phase, so that the EMI induced offset resulting at the output raises as it should do the (greatest) one generated by the main amplifier. After roughly $2.5\mu s$, which correspond to the auto-zero phase duration, the output voltage experiences a DC shift drop towards a smaller value, which settles at around $1.65V$ after some oscillations. The final DC shift value is reached after some clock cycles depending on the durations of the injection transients in the two phases (see Fig. 5.24 in Chapter 5).

This behaviour brings to the conclusion that such drop is caused by the fact that the OpAMP goes to the amplification phase Φ_A, hence, the compensation of the EMI induced offset in the main amplifier by the auxiliary amplifier takes place and the only remaining contribution as a DC shift to the output is the EMI offset generated by the auxiliary amplifier itself.

TEST METHODS AND MEASUREMENTS FOR CMOS OPAMPS EMI SUSCEPTIBILITY EVALUATION

5.1 Introduction to EMI susceptibility test methods

The evaluation of the EMI susceptibility of an integrated circuit is not a trivial process, both at simulation level and even more at measurement level. Furthermore, EMI susceptibility testing can prove to be very time-consuming and costly, therefore it is desirable to achieve high initial pass rate and to forecast the results of the measurements by making realistic and reliable computer aided design (CAD) software simulations.

Since the presented Ph.D. thesis work focuses on the effects of conducted electromagnetic interferences, the present chapter aims at giving a clear picture about all the techniques which have been conceived in order to simulate and measure the susceptibility of ICs subjected to this kind of EMI. At present times there are mainly two different conducted EMI susceptibility tests which have been recognized by the community to be the most reliable and reproducible ones. In the following sections, a simplified description of the techniques which are commonly used to test the susceptibility of ICs to conducted electromagnetic interferences is given. In the rest of the Chapter, a detailed overview of the observed problems and the solutions taken to profitably simulate and test the devices designed during the Ph.D. work are provided, analysing each part of the discussed test bench and highlighting how it has been realized at simulation level and practical level.

5.1.1 The Direct Power Injection Method

The first test is based on a European regulation proposed for the first time in 2002 under the IEC 62132 standards. Among them, the Direct Power Injection (DPI) standard [29] , approved in 2004 and updated in 2006, describes a procedure to inject high frequency conducted disturbances into an IC pin via a DC block capacitor with an optional series resistor. The procedure implies the injection of continuous waves or 1kHz 80% AM modulated disturbance waves over a frequency range spanning from 150kHz to 1GHz and with a maximum power of 37dBm for automotive ICs ([55]), corresponding to 5 Watts or $44.768\mathrm{V_{pkpk}}$ on a matched load.

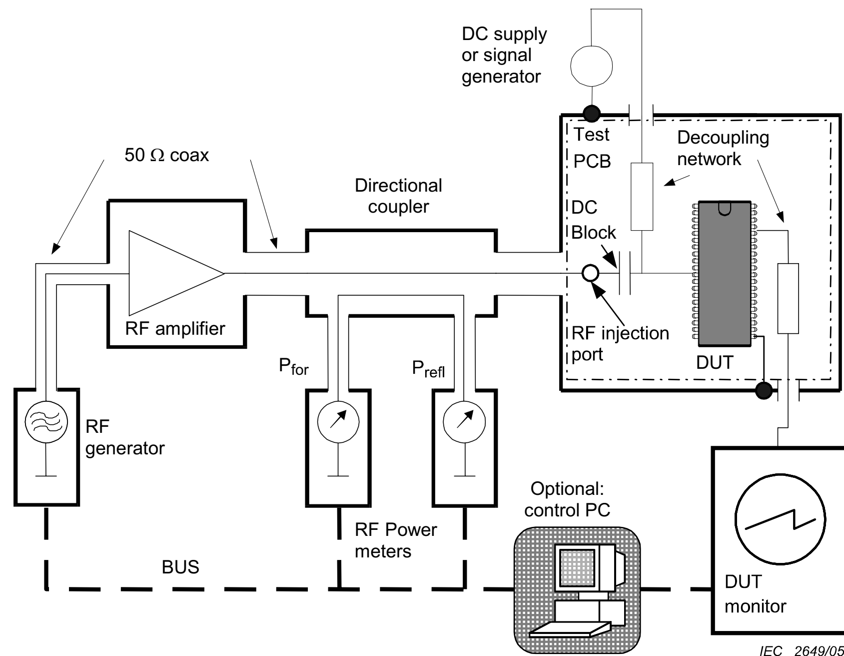

FIGURE 5.1: DPI test bench according to IEC62132-4 [29].

The disturbance is injected starting from 150kHz up to 1MHz with a frequency step lower than 100kHz, then from 1MHz to 100 MHz with a frequency step lower than 1MHz and finally from 100MHz to 1GHz with a frequency step lower than 10MHz [28]. For each disturbance frequency f_{emi}, the power is increased, usually starting from 10dBm, with a power step of 0.5dB. At the same time, the forward and reverse power to and from the device under test (DUT) are monitored and recorded together with the output of the DUT itself. The block diagram in Fig.5.1([29]) represents a sketch of the standard test bench proposed in the regulation to perform the DPI measurement.

The RF generator is capable of producing either continuous wave or modulated waves up to several GHz ([56]), but it usually cannot reach an output power of 37dBm. For this reason an RF amplifier is often cascaded to the generator. In the case such amplifier has not enough bandwidth to cover the whole frequency range several amplifiers have to be used depending on the injected disturbance frequency.

The output impedance of the amplifier must be equal to 50Ω and an attenuator (6dB or 10dB) is often inserted between the amplifier output and the injection line to enhance the matching ([28]). The directional coupler isolates the forward power P_{for} injected into the DUT and measures it by means of an RF power meter. Up to the RF injection port, the impedance of the injection path must be 50Ω in order to avoid losses and to minimize reflections, since ICs pins are usually far away from being 50Ω matched ports and a high percentage of the RF power injected into the IC pin is likely to be reflected back to the injection path itself. For this reason, another power meter could be inserted in order to measure the reflected power P_{refl} from the DUT, so that, by subtracting this power from the forward one, it is possible to measure the actual amount of power absorbed by the DUT.

The directional coupler is connected to the printed circuit board hosting the IC under test. The RF injection port is often coupled to a DC supply or signal generator used to bias or to provide the DUT with a nominal input signal. According to the regulation, the RF injection port on the PCB is composed by a DC block capacitor and optionally a series resistor to AC couple the injection path and the port of the DUT in which the disturbance is injected. The reason of such coupling is mainly to avoid any AC signal to be absorbed by the DUT biasing source through the injection path. Furthermore, the AC coupling avoids any DC signal coming from the DUT biasing source flowing into the RF generator via the injection path. Finally, the output of the IC is monitored and recorded via a PC in order to check how it changes as a result of the interferences injection. The output of the system is usually a graph, plot or table which depicts for which EMI frequency and forward power (f_{emi}, P_{for}) the DUT output has exceeded a certain predefined percentage with respect to its nominal value.

5.1.2 The EMI Rejection Ratio Method

The second method, directly derived from the first one, has been introduced for the first time by Texas Instruments Incorporated (TI) and is based on the EMI rejection ratio (EMIRR) concept [57] in order to specifically evaluate the EMI susceptibility of operational amplifiers. The measurement setup is practically the same as the DPI method. The operational amplifier is set in a buffer configuration and the interferences are injected into the positive input terminal. Since the most common OpAMP response to EMI is a DC shift of the output voltage (Chapter 2), the value of such offset appearing at the output of the device after the EMI injection is used to calculate, for each disturbance frequency, the value of the EMIRR according to Eq.5.1.

$$EMIRR = 20\log\left(\frac{A_{emi}}{\Delta V_{os}}\right) + 20\log\left(\frac{A_{emi}}{100mV_{pk}}\right) \tag{5.1}$$

The quantity A_{emi} is the peak amplitude of the applied EMI voltage. ΔV_{OS} is the input referred change in offset voltage that takes place in response to the applied disturbance. The second logarithmic term in the equation references the EMIRR to an input signal of $100mV_{pk}$. The EMIRR quantity can then be used to characterize whatever operational amplifier in term of EMI robustness with a single number at a specific frequency and it does not require any plot or table to express the measurement result like the DPI method does, although the measurement test bench concepts are practically the same for both kinds of characterization.

5.2 Proposed EMI susceptibility test bench: an IC designer perspective

As it will be clear from the following paragraphs, the injection of disturbances up to 1GHz into an integrated OpAMP forces the engineer to face different issues and to choose one among several strategies in order to obtain meaningful, interpretable and reproducible results. The EMI susceptibility evaluation of the operational amplifiers designed for the purpose of the present Ph.D. work has required several modifications and reworks of the employed test benches before

coming to a suitable solution. As a matter of fact, the standard EMI susceptibility evaluation methods have been reshaped to fit the type of DUTs which have been tested in the case of the presented study.

The first aspect to highlight concerns the characteristics of the amplifiers whose EMI susceptibility had to be evaluated. As mentioned in the Chapter 1, the main focus of the Ph.D. work has been the design and the EMI susceptibility testing of integrated CMOS offset compensated OpAMPs employed inside automotive ICs. Such amplifiers are not supposed to be used as OTS components since they are usually embedded inside a much bigger integrated circuit. For this reason, in a real application, the environment surrounding the amplifier is not directly the package and the PCB, but instead it is composed by further circuitry which eventually is then directly connected to the external word, as exemplified in the picture of Fig.5.2. This aspect leads immediately to a first workflow choice: once an amplifier has been designed, it is possible to evaluate its EMI susceptibility by testing it either in its real application conditions, i.e., embedded into the actual circuitry the whole IC is composed by, or it is possible to fabricate it and to test it as a standalone device directly connected to the outside environment.

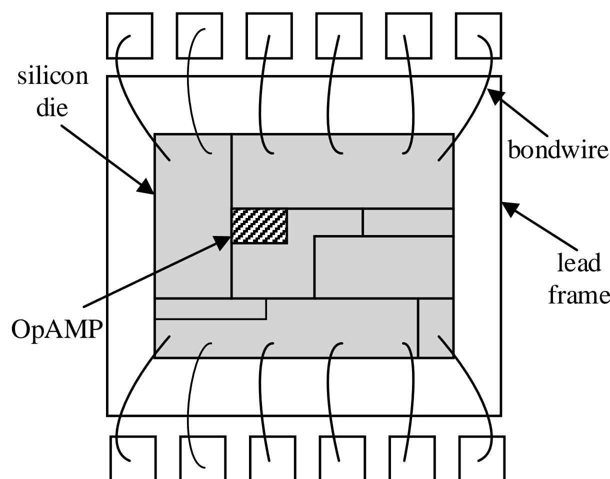

FIGURE 5.2: OpAMP as part of a bigger integrated circuit.

The former strategy has the advantage of being the closest one to the real application, provided that the test bench accurately models the real EMI environment of the application itself. On the other hand, such solution implies several drawbacks. A minor disadvantage is that the fabrication of a whole complete IC, as it should be for a final release, for each amplifier or subblock to be tested it is too expensive and unpractical. More importantly, the results obtained from the EMI susceptibility tests on the whole IC would be also affected by all the circuitry in which the amplifier is embedded, as well as by the OpAMP itself, and would not provide a clear picture about the behaviour of the amplifier subjected to EMI.

For this reason, the strategy adopted for the present Ph.D. work has been to fabricate and test each device as a standalone amplifier, without any further circuity besides the one needed for the OpAMP to be properly biased, clocked and stabilized. The devices have been fabricated and packaged even without ESD protections for the PADs, since ESD structures can be themselves affected by EMI and then hide the behaviour of the tested amplifier ([58]). Although

this approach could seem inconvenient, since the device EMI susceptibility is evaluated in a condition which heavily differs from the real application, it proves to be suitable to the scope of the study, because the EMI susceptibility of each amplifier is expressed only in relation with the EMI susceptibility of a reference amplifier whose behaviour under high frequency input interference is well documented in the state of the art literature. As a consequences, it does not really matter if the amount of disturbances reaching the OpAMP input stage in the real application is attenuated or anyhow modified with respect to the one injected in the standalone device, provided that an upper bound is set for the disturbance power in order to put all the tested amplifiers in the worst possible scenario which could appear when they are operating in the real application.

By comparing the amplifiers EMI performances it is then possible to state that if one amplifier shows a better robustness than another when they are tested as standalone devices, this effect will certainly translate to a better robustness of the entire IC containing the robust amplifier with respect to the IC containing the EMI susceptible one. This approach brings then several simplifications either in the simulation and in the measurement processes and proves to be the best one in order to provide the most general and scientifically valuable results, independently on the application field of the amplifier.

As a matter of fact, the simulation of the EMI effect on the designed devices doesn't require then to simulate the entire IC, hence computational times are greatly shortened. Furthermore, there is no need to fabricate the whole IC in order to test the susceptibility of the OpAMP, so that R&D time and costs are also reduced. For the aforementioned reasons, each CMOS OpAMP designed for the present study has been simulated and tested as a standalone component internally connected as a voltage buffer (Fig.5.3).

The follower configuration is one of the most commonly used in order to test the EMI susceptibility of OpAMPs to interferences conducted in the amplifier input stage, since it guarantees a straightforward way of measuring the OpAMP output DC shift by directly referring it to the amplifier input. Since the follower configuration guarantees for the OpAMP the maximum bandwidth, corresponding to its gain bandwidth product (GBW), all the disturbances with a frequency close or lower than the GBW are processed by the amplifier almost as nominal signals and therefore their effect in producing the output DC shift is reduced. For this reasons

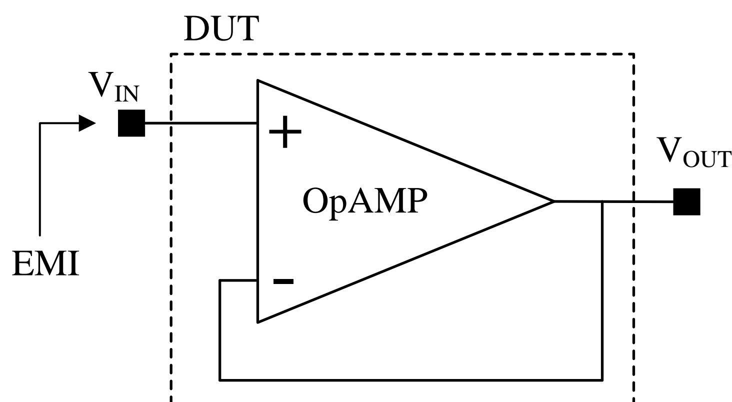

FIGURE 5.3: CMOS OpAMP basic configuration for conducted EMI injection.

there are other solutions to maximize the EMI effect in order to highlight the induced output offset, like the use of two different amplifiers to split the AC and the DC loop ([38]). On the other hand, the OpAMPs tested during the Ph.D. study have been designed in order to sense signals in a bandwidth close to DC, hence their GBW is so close to the lowest EMI injected frequency that the follower configuration has proven to be the easiest and most suitable solution to evaluate their susceptibility.

5.2.1 EMI Power

The first part of the DPI measurement chain is composed by the RF generator and the RF amplifier. According to the regulations ([29],[28] and [55]), the injected forward power into the DUT must have a maximum value of 37dBm and this is the main reason of cascading the RF amplifier to the generator. As already stated previously, the power of 37dBm corresponds to a continuous sinusoidal wave of almost $45V_{pkpk}$ on a matched 50Ω load. The amplifiers which are the object of study of the Ph.D. work are CMOS devices fabricated in a low voltage $0.35\mu m$ proprietary technology with a $7.5nm$ gate oxide thickness. Such technology has a maximum rating for the gate voltage of less than $6V$, hence it cannot withstand such a high input power. The first aspect to consider has then been to establish the maximum power needed to test the CMOS amplifiers in order to evaluate their EMI susceptibility.

Although a simple solution would be represented by arbitrarily deciding the maximum peak to peak voltage value for the input disturbance (for example the positive and negative power rails), the conversion from such voltage value to a dBm power value is not trivial, since it implies the knowledge of the DUT input impedance. For such a reason, the impedance of the positive input differential stage of the designed amplifiers has been evaluated by means of S-parameters measurements at wafer level (Section 5.3, [24]) (Fig. 5.4).

The input differential stage of most of the designed CMOS amplifiers comprises an n type MOS differential pair with devices sized at $(160/0.8)\mathrm{\mu m}$ and biased at $20\mu\mathrm{A}$, hence this is the

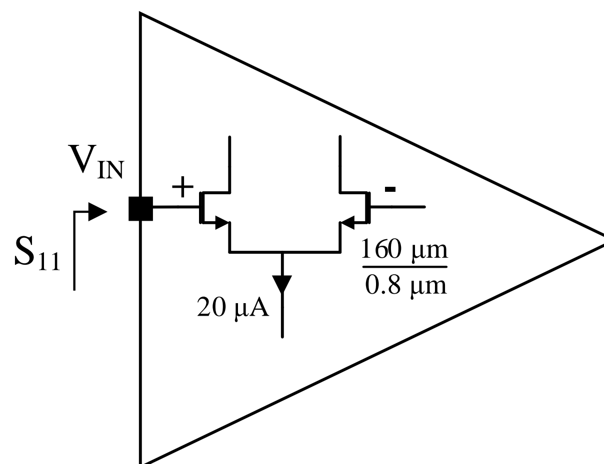

FIGURE 5.4: Structure employed to evaluate the input impedance of the investigated OpAMPs.

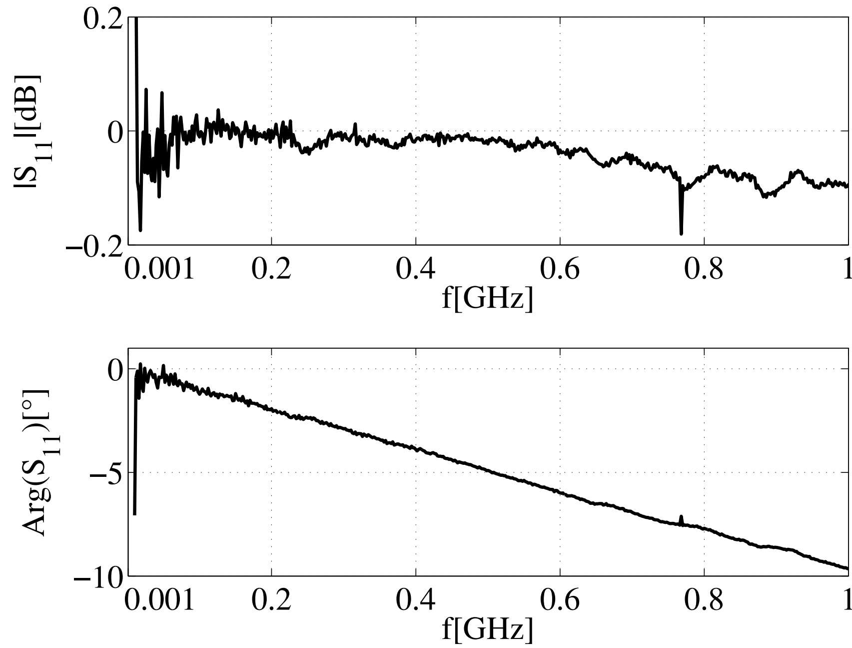

FIGURE 5.5: S11 parameter for the positive input of the biased CMOS differential stage, in magnitude and phase.

structure which has been employed for the input impedance evaluation. The plot in Fig.5.5 shows the S_{11} reflection coefficient, in magnitude and phase up to 1GHz, measured at the gate of the differential pair positive input.

As can be noticed from the S_{11} measurement, the input port of the IC can be considered, with good approximation, an open circuit up to 1GHz. In fact, the modulus of S_{11} never exceeds -0.2dB with a maximum phase shift of $10°$. The reflection coefficient measurement reveals a noisy behaviour at low frequency, where its modulus exceeds 0dB. This trend is not due to an actual amplification of the injected signal, but is an artefact due to the fact that the instrument has to measure a highly reflective not matched device at very low frequency, hence the instrument is actually reaching its sensitivity limit.

Since the OpAMPs input has been confirmed to be very close to an open circuit, several simplifications to the DPI susceptibility measurement framework can be performed. The modification involving the injected EMI power consists in the possibility of completely avoiding the use of an RF amplifier, for the following reason.

If the DUT is characterized by a 50Ω input impedance, the calculation of the EMI peak to peak voltage level reaching its input, given a certain RF power level, is straightforward and can expressed by (5.2), which represents the maximum power delivered by a sinusoidal signal with a peak to peak amplitude equal to $2A_{emi} = A_{emi_pkpk}$ on a load R_L. Rewriting such expression for A_{emi_pkpk} and considering R_L to be a 50Ω load leads to (5.3). In the case of a load impedance almost equal to an open circuit, as it is for the input stage of the studied CMOS OpAMPs, the actual peak to peak voltage level reaching the IC port ($A_{emi_pkpk}|_{OC}$) is doubled

with respect to the value calculated for a 50Ω load, as expressed in (5.4).

$$P_{emi} = \frac{|A_{emi_pkpk}|^2}{8\,R_L\,10^{-3}} \tag{5.2}$$

$$A_{emi_pkpk}|_{50\Omega} = \sqrt{8 \cdot 50\Omega \cdot 10^{-3} \cdot 10^{\frac{P_{emi_dBm}}{10}}} \tag{5.3}$$

$$A_{emi_pkpk}|_{OC} = 2\,A_{emi_pkpk}|_{50\Omega} \tag{5.4}$$

Solving (5.3) and (5.4) for different EMI power values shows that, for example, 2dBm input EMI power already corresponds to an almost $1.6V_{pkpk}$ disturbance reaching the input of the IC. Such a value, for an amplifier powered with a single 3V supply, is already enough to drive the input of the OpAMP in strong non-linear distortion ([59]). For this reason, since no higher power than a few dBm is needed for the injection, the DPI setup can be modified avoiding the use of the RF amplifier, because the RF generator is itself capable of producing a maximum output power of 20dBm ([56]).

The reader may wonder, at this point, how it is possible that commercial automotive ICs are tested with an injected power as high as 37dBm and which is the meaning of testing a device, in this case, with such a low value of EMI power with respect to the one defined in the regulation. The reason for this is represented by the fact that, as already mentioned, the OpAMPs investigated during this research activity represent only a sub-block of the entire IC which, on the contrary, is directly connected to the outside environment by means of a lead frame, bond wires, pins, ESD structures, a package and a PCB with several discrete protection components. All these elements play a remarkable role for the EMI susceptibility of the complete integrated circuit, but they have been avoided on purpose in this research activity in order to purely highlight the EMC performances of the OpAMPs. As a consequence, the injected EMI power levels are scaled accordingly.

5.2.2 Injection Path

Since the input port of the OpAMP can be resembled to an open circuit, most of the injected power is reflected back to the source ([60]) and no forward power is actually absorbed by the DUT. For this reason, the strategy adopted in order to perform the DPI injection on the tested OpAMPs implies to avoid also the use of the directional coupler and the power meters, because there is no real need to know the amount of forward and reflected EMI power in order to characterize the devices. The forward power is then the one accurately produced by the RF generator, while the reverse power will be equal to the forward power minus the eventual losses along the injection path.

The power reflected from the DUT travels then back to the RF generator, which is supposed to have a 50Ω output impedance, hence it is supposed not to reflect back any further power. Unfortunately, because of the high amount of reflected power from the DUT, even a small mismatch along the injection line or at the RF generator output causes further reflections.

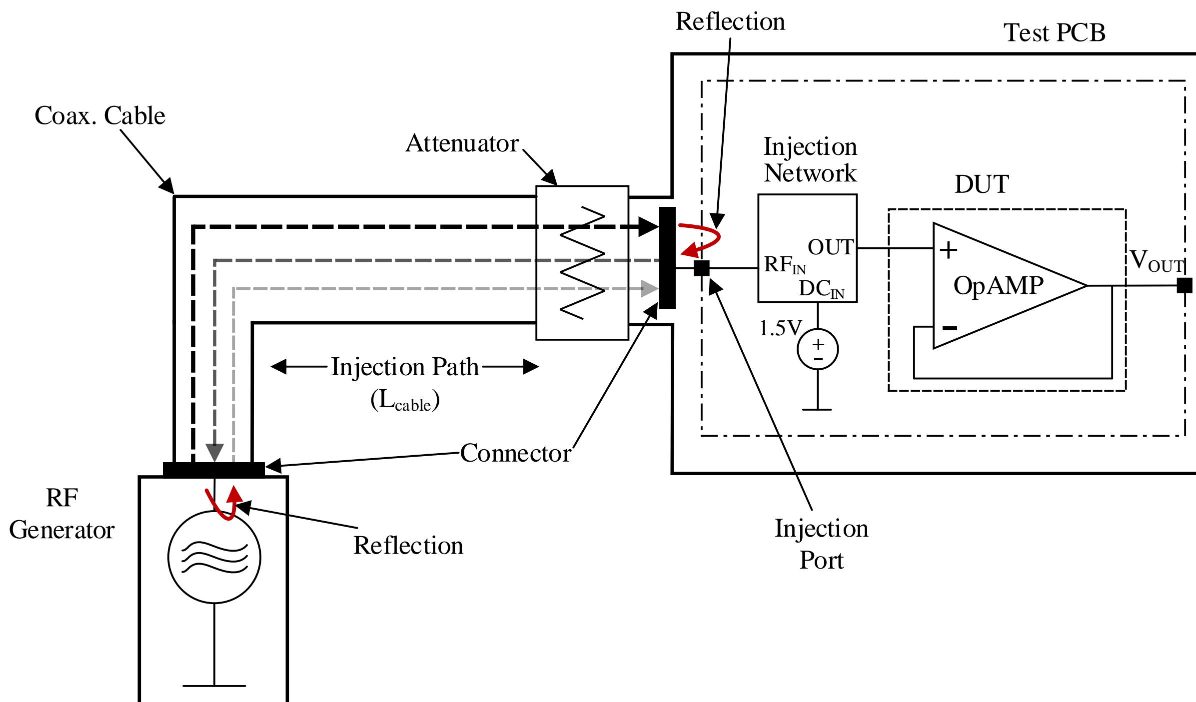

FIGURE 5.6: Multiple reflections along the injection path because of impedance mismatches.

Consequently, a fraction of the power reflected from the DUT is reflected again by the RF generator and the injection line and travels back to the DUT itself (Fig. 5.6). This issue, which can heavily contribute to generate grubby and uninterpretable DPI injection measurements results, is generally true for whatever unmatched DUT but it is more evident in the case of a fully reflective DUT as in the case of the input stage of a CMOS OpAMP. As already mentioned, a 6dB or 10dB attenuator is usually inserted between the RF generator, or the RF amplifier if present, and the injection line: this ensures a better matching and attenuates the power reflected back from the DUT, so that, for a 6dB attenuator, the residual power eventually reflected by the RF generation stage is attenuated by 12dB before reaching the DUT again.

As it is shown in the following, the DPI setup proposed for the Ph.D. DPI investigations does employ a 20dB attenuator, instead of a 6dB one, in order to get rid of the aforementioned measurement ripple. Clearly, such attenuation requires 20dB more power at the generator side but, since no power greater than 2dBm is needed to fully distort the amplifier input stage supplied at 3V, the RF amplifier cascaded to the generator can still be avoided. Another improvement to the setup is represented by keeping the length of the injection path as short as possible, since this produces a bigger ripple period and consequently a lower ripple amount in the measurement results, as it is demonstrated in the following example.

The plot in Fig.5.7 shows the results of a DPI injection performed on a CMOS offset uncompensated OpAMP. The injection has been performed at the non inverting input pin while the amplifier has been connected as a voltage buffer and the output average voltage has been measured with a nominal input DC voltage of 1.5V, as sketched in Fig.5.6. The curves in the

plot represent two injection measurements performed in two different configurations of the injection path. In the first case (continuous line), the injection path is composed by a 1.55m long M17/60-RG142 coaxial cable directly connected at the RF generator output and at the PCB injection port, with no attenuator. The second (dotted line) curve represents instead the case in which the injection path is composed by a 0.4m long M17/84-RG223 coaxial cable, again with no attenuator.

As it is possible to note from the plot, the amplifier average output voltage experiences a DC shift and such induced offset increases over EMI injected frequency, saturating after around 300MHz. Although this behaviour is expected from the theory, the first effect which can be further noticed is that both measurements are affected by a heavy ripple over frequency. Such ripple is one of the main consequences of the aforementioned reflection mechanism, because of which the DUT experiences a peak to peak EMI voltage which is related not only to the EMI power produced by the generator (see (5.2)) but is also the result of the combination of the forward and reflected power waves along the path. The amplitude of the ripple is directly related to the product of the reflection coefficients at the generator and injection port sides, while its periodicity is related to the characteristic frequency of the line, which in first approximation can be expressed as ([61]):

$$f_{line} = \frac{v_p}{2\lambda_{cable}} = \frac{v_{p\%}\, c}{2\lambda_{cable} \cdot 100} \tag{5.5}$$

The parameter v_p represents the velocity of propagation along the line ([62]) and can be calculated looking at the percentage velocity of propagation for a specific cable. Such percentage

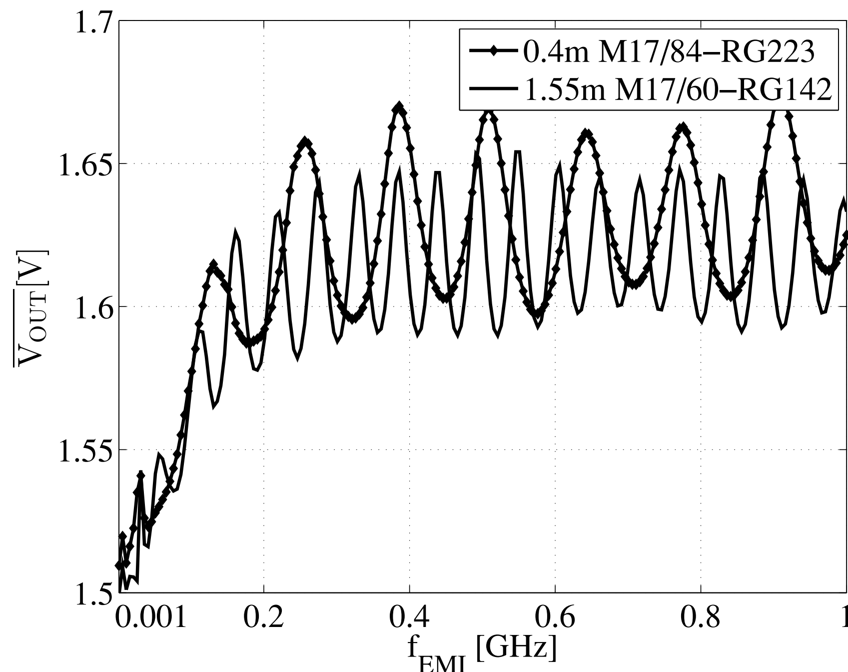

FIGURE 5.7: OpAMP average output voltage over EMI frequency with two injection path cable lengths.

represent the fraction of the light speed with which the signal travels along that cable. From the M17/60-RG142 and the M17/84-RG223 technical datasheets it is possible to determine a percentage velocity of propagation equal to 69% for the former and 66% for the latter, so that multiplying these values by the speed of light (2.398x10^8 m/s) provides the v_p parameter for both coaxial cables.

The quantity λ_{cable} represents the physical length of the cable, being 0.4 meters for the M17/84-RG223 and 1.55 meters for the M17/60-RG142. Calculating the characteristic frequencies for the two setups provides a value of f_{line} equal to 54MHz for the 1.55m M17/60-RG142 cable and 197MHz for the 0.4m M17/84-RG223 cable. Being 5.5 an approximate expression, the calculated values are slightly different from the measurement results, since, as can be appreciated from the plot of Fig.5.7, the longest cable produce a ripple with a characteristic frequency of around 55MHz, while the shortest one generate a ripple whose peaks replicate roughly every 130MHz.

Apart from that, the example shows how the cable length influences the DPI measurement result, such that, even if the cable attenuation is compensated, the measurement is anyway affected by a baseline ripple with a periodicity which increases as the cable length decreases. The plot in Fig.5.8 represents a measurement example which shows the benefit of inserting an attenuation stage along the injection path.

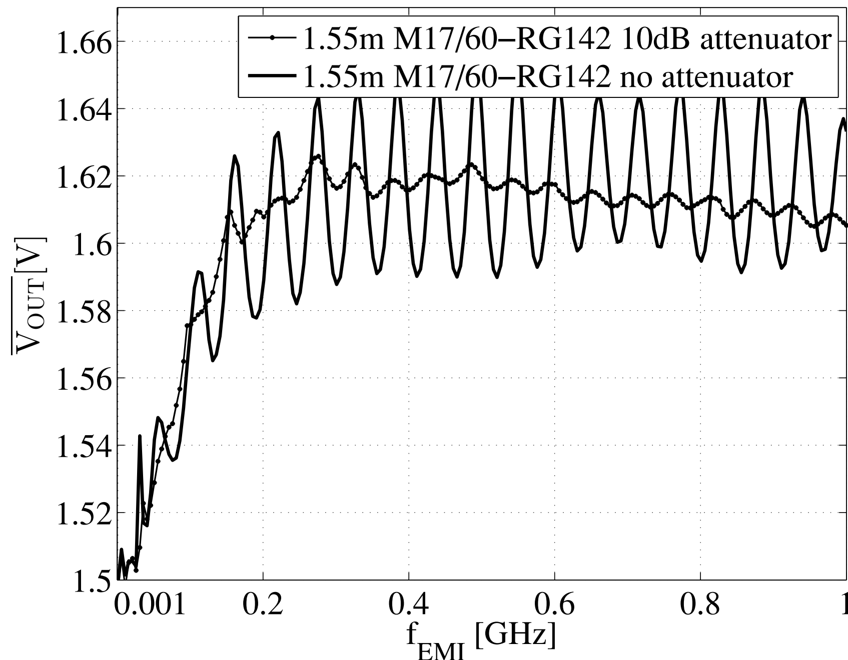

FIGURE 5.8: OpAMP average output voltage over EMI frequency with and without 10dB attenuation along the injection path.

The two curves in the plot are in fact the injection measurement results performed on the same voltage follower amplifier and employing the 1.55 meters long M17/60-RG142 cable but in one case (continuous line) without any attenuator along the line, so to exactly resemble one

of the two results of Fig.5.7, while in the other case (dotted line) with a 10dB attenuator inserted between the coaxial cable and the injection port of the test PCB.

As it is possible to note, the use of an attenuator greatly reduces the output ripple and permit to highlight some of the output features. For example, the output waveform obtained with the 10dB attenuator shows the attenuation of the cable over frequency.

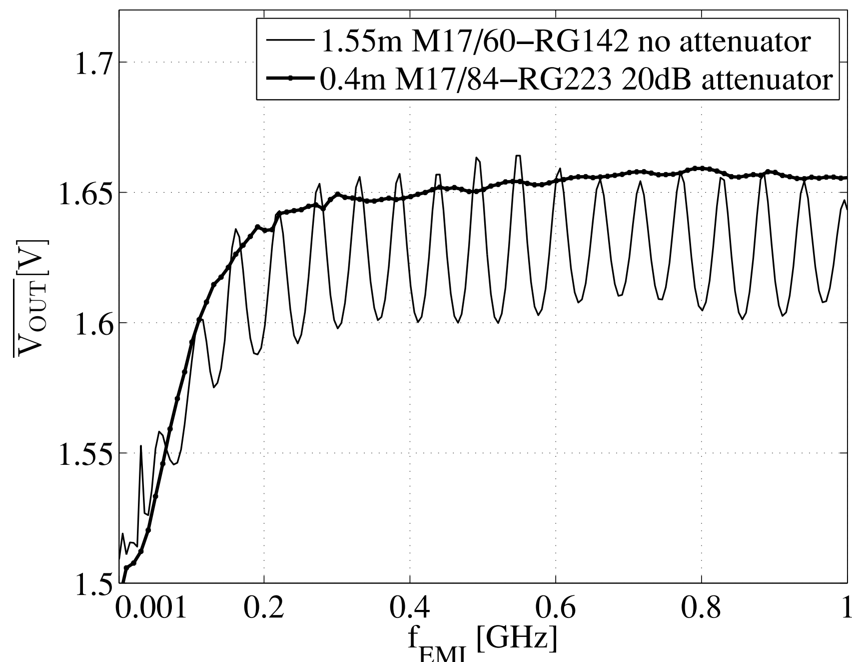

FIGURE 5.9: OpAMP average output voltage over EMI frequency: comparison between standard and optimized injection path setup.

Finally, to fully highlights the final advantages of increasing the attenuation along the line and of keeping the line as short as possible, the plot in Fig.5.9 shows the same measurement results made in one case again with the 1.55 meters long M17/60-RG142 cable with no attenuation (continuous line) and, in the other case (dotted line), with the shorter 0.4 meters long M17/84-RG223 cable and a 20dB attenuator inserted at the injection port.

As the plot demonstrates, for the latter case the ripple is reduced to an unnoticeable level and the attenuation due to the cable is much smaller and cannot even be observed, so that the DC shift produced by the OpAMP, as a consequence of EMI input injection, saturates and stays steady up to 1GHz disturbance frequency, as predicted by the theory. Because of the aforementioned results, the PCB level DPI setup used for testing the devices designed along the Ph.D. work has been optimized employing a 20dB attenuator and the shortest available coaxial cable, so to obtain the cleanest possible measurements.

5.2.3 Injection Network and PCB

The last part which plays an active role for the DPI setup is represented by the injection network and the PCB holding the DUT. IEC standards [29], [28] and [63] provide several guidelines

both for the injection network design and for the PCB layout. The goal of such guidelines is to create a general test setup and PCB which can be reused for all the EMC tests and can generate reproducible and comparable results. Unfortunately, the use of a general solution forces the setup to be suboptimal for a specific EMC test; hence the proposed test bench employed for the DPI investigations along the Ph.D. work has been adapted in order to be optimized for the direct power injection method and for CMOS operational amplifiers as DUTs.

According to [29], the EMI generation stage must be decoupled by a DC block to avoid supplying DC into the RF generator or the RF amplifier. On the other hand, the DUT input bias supply is prevented from getting EMI power by a decoupling block that has a high AC impedance on the side that is connected to the EMI injection path. Such DC and AC decoupling is demanded to a block called injection network or bias T. According to the standard, the DC block on the EMI injection side should be a $6.8nF$ capacitor $C_{DC-block}$ with an optional series resistor up to 100Ω for current limitation ([64]). Furthermore, the DC biasing block should have an AC impedance $Z_{AC-block}$ greater than 400Ω for all the EMI test frequency span. The picture in Fig.5.10 represents a sketch of a possible injection network in the case of employing an inductor $L_{AC-block}$ as DC biasing and AC blocking component.

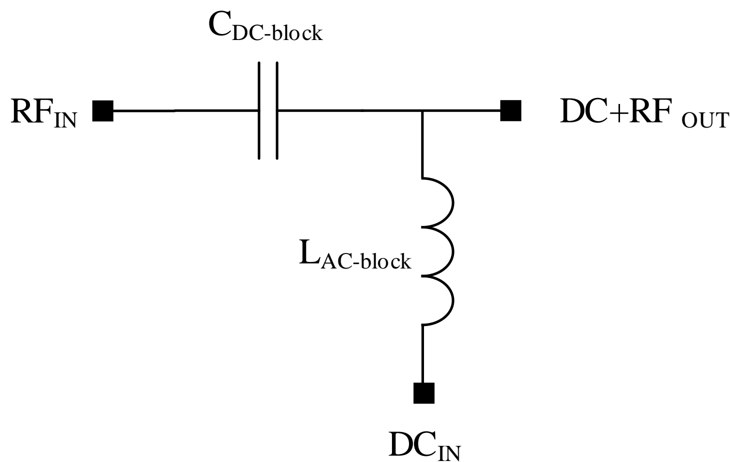

FIGURE 5.10: Injection network basic schematic.

As pointed out in [29], one coil or inductor alone cannot normally cover the whole frequency range maintaing an impedance greater than 400Ω. This fact is ascribed to the self-resonance mechanisms happening for whatever discrete inductor or capacitor ([65]). To show this effect, the picture in Fig.5.11 represents an impedance measurement for three different DC biasing configurations. The first one is made by a single $6.8\mu H$ discrete inductor (dashed line) and, as it is possible to note, such coil maintains its inductive behaviour up to around 70MHz. After that, the component starts decreasing its impedance over frequency with a typical capacitive behaviour. For such reason, several series coils or inductors are usually needed to maintain high AC impedance along the whole frequency test range, putting the lowest inductance component closest to the DUT.

The continuous line in Fig.5.11 shows in fact a second AC block setup composed by a series of three discrete inductors, namely a $680\mu H$ inductor and two coils, one of $6.8\mu H$ inductance

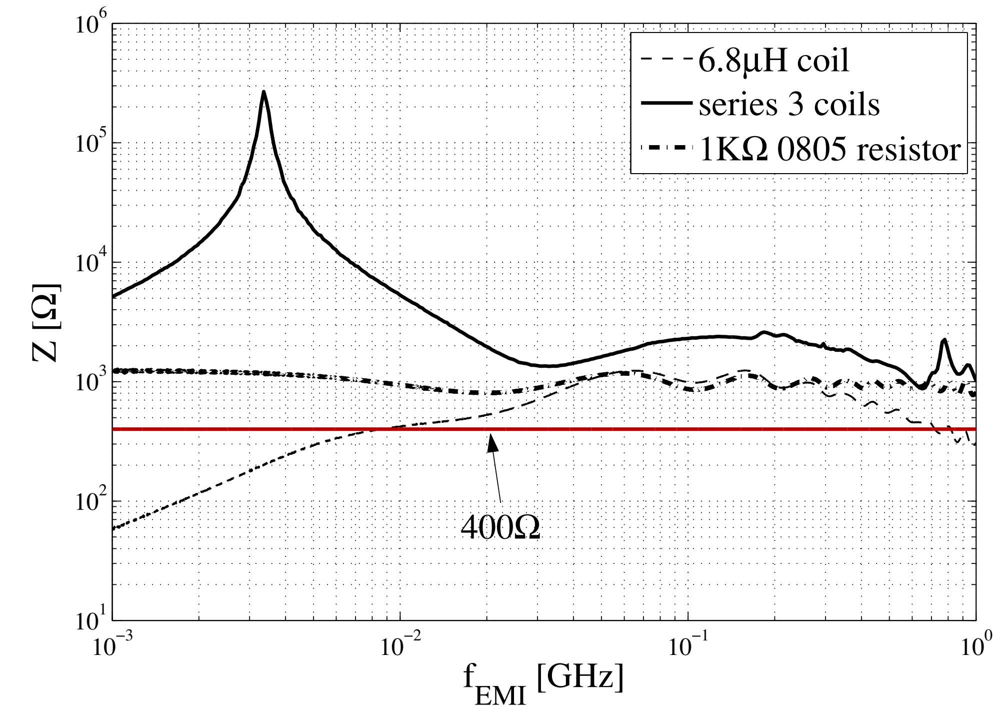

FIGURE 5.11: Single $6.8\mu H$ coil, series of $680\mu H$, $6.8\mu H$ and $4\mu H$ coils and $1\text{k}\Omega$ 0805 resistor impedances over frequency.

while the other of less than $4\mu H$ inductance. Although each single inductor cannot keep its impedance above 400Ω (red line) along the whole frequency range, the series of the aforementioned three inductors reaches the goal. Even if such general configuration could seem to be suitable enough to evaluate the susceptibility of an IC, its practical implementation shows some drawbacks.

Looking again at the plot in Fig.5.11 it is possible to note that, even if the DC biasing path impedance remains above 400Ω on the frequency range 1MHz-1GHz with the series inductors configuration, such impedance is not constant but it has several resonances due to the superposition of the self-resonances of each inductive component. This fact translates into a non-constant amount of EMI absorption by the DC supply and consequently into a non-constant EMI power experienced by the DUT over frequency. This effect loses its importance if the outcome of the DPI test has only to be a pass/fail result, but it becomes of concerns whenever, as in this case, the behaviour of the DUT subjected to EMI injection is of major relevance.

The dotted dashed line of Fig.5.11 shows then a third possible approach which consists in achieving the DC biasing through a single discrete SMD resistor ($1k\Omega$ 0805 in this case). As can be noted from the plot, the impedance of the resistor remains stable up to 1GHz, only showing the typical ripple over frequency already discussed in Section 5.2.2 and affecting also the impedance measurement of the single $6.8\mu H$ inductor. Beside the constant impedance over frequency, the use of a single resistive component in spite of inductive ones provides further advantages. Another problem related to the use of series inductors for the injection network is ascribed to the parasitics which are added to the injection network itself because of the series

inductors physical size. This is even more important considering that, due to their dimensions, the inductors cannot easily be placed very close to the DUT injection pin under test. For this reason, a relatively long trace line could be necessary to connect the inductors to the injection network and such line adds further parasitics to the network itself, generating power losses along the path.

To show such effect it is possible to consider the test measurement depicted in Fig.5.12. It represents the sketch of a test injection network being part of a DPI test bench. As suggested in [29], the DUT IC has been replaced by an SMA connector (PORT 2) and the S_{21} parameter of the injection network has been measured with a vector network analyser (VNA) in three different configurations:

a) Configuration with the DC block capacitor and the 50Ω trace between the VNA port 1 and port 2, without the DC biasing part of the injection network, i.e. without the trace connected to the inductors and without the inductors themselves.

b) Configuration with the DC block capacitor, the 50Ω trace and the line reaching the DC biasing inductors between the VNA port 1 and port 2, without the inductors soldered on the board.

c) Configuration with the DC block capacitor, the 50Ω trace and the line reaching the DC biasing inductors between the VNA port 1 and port 2, with the series inductors soldered on the board and terminated by an open, a short and a 50Ω load.

The first noticeable effect from the S_{21} plot results (Fig.5.13) is the presence of a ripple in the measurement. Such ripple can be ascribed to the reflections along the line due to matching inaccuracies (see Section 5.2.2). The second most important effect to note is the fact that, even without any DC biasing line attached to the injection path (configuration *a*), an evident attenuation is already present, reaching almost $1dB$ after $860MHz$. According to the standard [29],

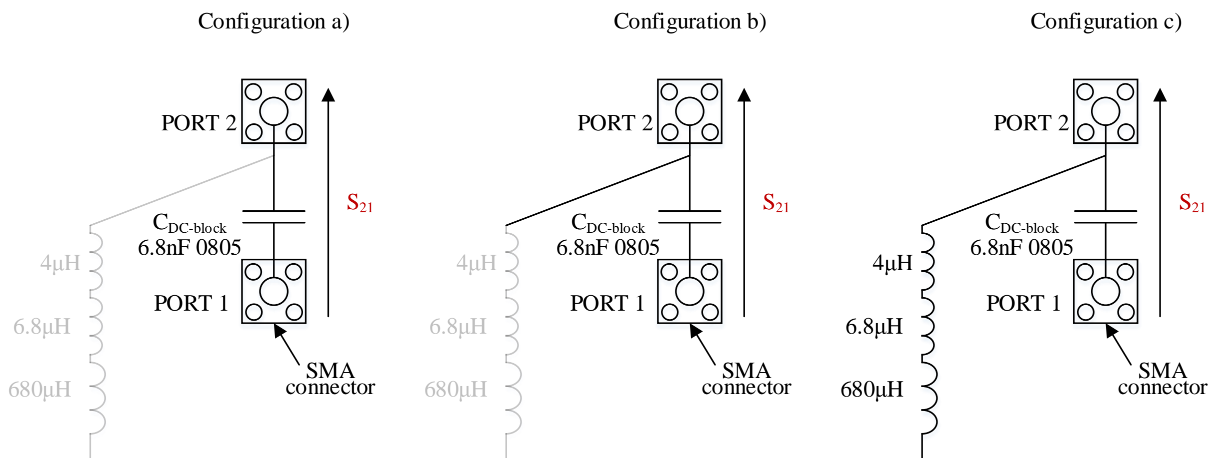

FIGURE 5.12: Injection network configurations for the evaluation of the board and components effects on injection path S_{21} (Transfer Gain). The third configuration shows the termination as short to ground only.

this would already be the maximum allowable attenuation for the injection line. Such attenuation, as well as the attenuation observed for configurations b and c, is ascribed to the power losses which, at frequencies up to 1GHz, are mainly represented by dielectric and conductive losses ([30]).

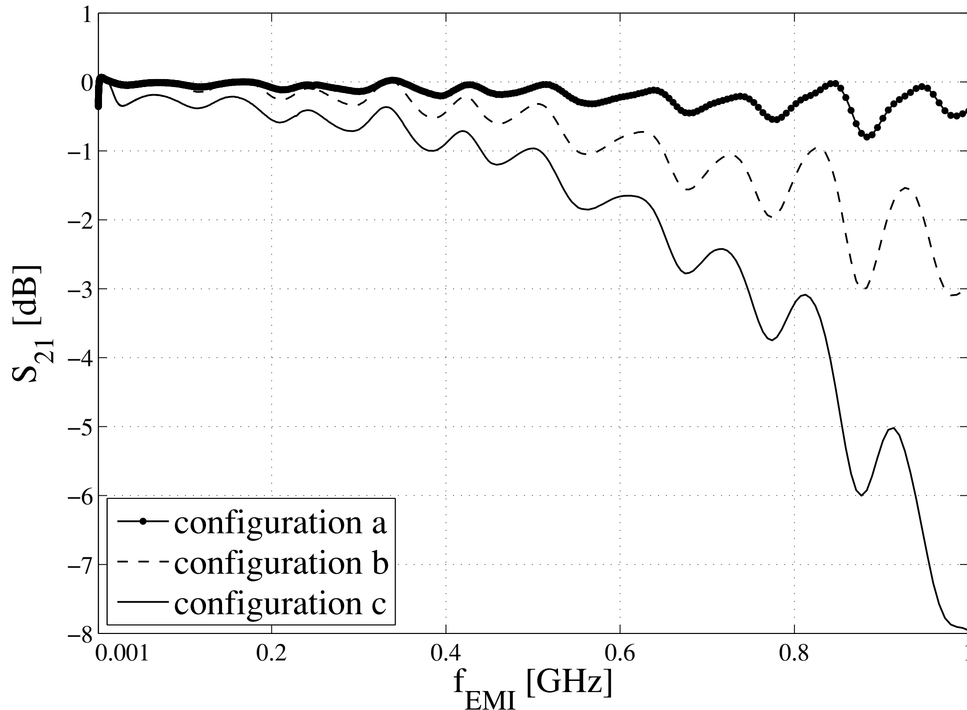

FIGURE 5.13: S_{21} measurement results from three different inductor based injection network configurations.

As can be further appreciated by Fig.5.13, configuration b and even more configuration c show an evident attenuation of the transfer gain S_{21} for the injection path, eventually reaching 8dB at 1GHz, which is an unacceptable value for a DPI test. This example shows that, even if the DC biasing network impedance is compliant with the standard specifications, the transfer characteristics of the whole injection network could prove to be unsuitable to a reliable test. Furthermore, even if the length of the line connecting the DUT IC pin under test to the DC biasing inductor is not much longer than $\lambda/20$ of the highest EMI frequency (15mm at 1GHz against the 20mm of the test board example), the losses caused by the discrete inductors are already enough to bring the setup violating the specifications. The reader may wonder then why the trace connecting the inductors to the DUT IC test pin could not be made shorter. The reason is that a board can usually host an IC with several possible injection pins, so that if a general and single solution has to be employed, one single board must contain the DUT IC with all the needed injection networks for all the possible IC pins which have to be tested under DPI.

This fact contributes to make the board crowded of components, so that bigger distances have to be taken in order to fit all the inductors on the PCB, leading to longer connection traces (Fig.5.14).

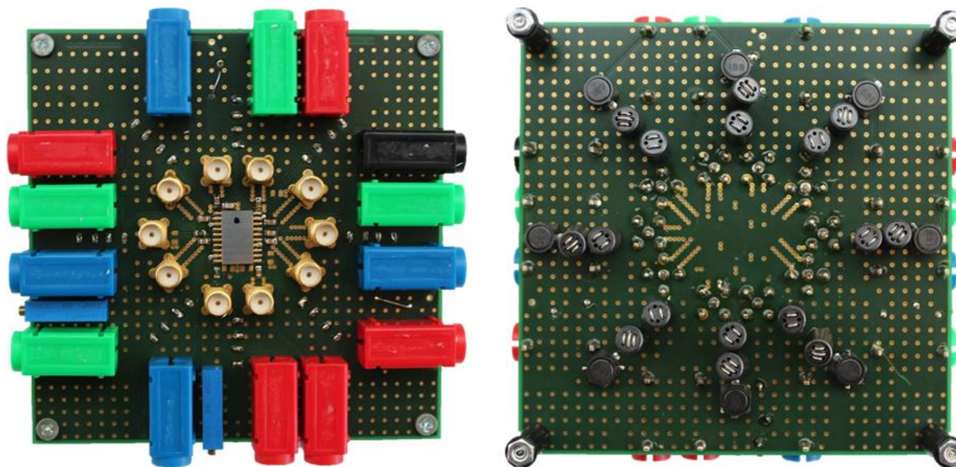

FIGURE 5.14: Example of DPI board with all the necessary injection paths for full IC characterization.

For all the aforementioned reasons, the injection network employed for the present Ph.D. work has been reworked in order to guarantee the cleanest possible susceptibility results. Following the suggestions of the regulation ([29]) and noticing that, as already pointed out previously, the input stage of a CMOS operational amplifier is characterized by a very high impedance and hence does not absorbs noticeable current, the DC biasing network has been modified replacing the inductor by just a single $1k\Omega$ 0805 resistor (Fig.5.15).

The advantages of such setup can be summarized as follows. Being a single passive component, the impedance of the resistor is supposed to be roughly constant over the whole frequency range and large enough to keep the setup much above the required impedance specifications for the DC path. Furthermore, being a much smaller component with respect to a series of inductors, its contributions to the power losses and consequently to the transfer gain S_{21} attenuation are drastically reduced. To show such benefits, the plot in Fig.5.16 depicts the same S_{21} measurement of configuration c together with the S_{21} of a reworked layout which makes the DC

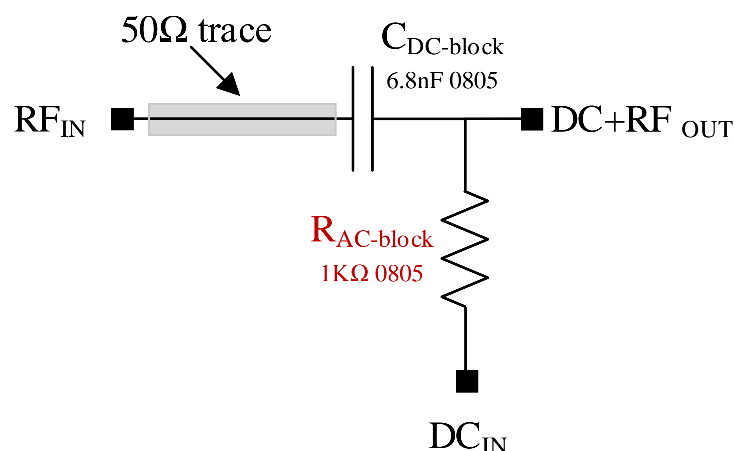

FIGURE 5.15: Proposed injection network.

biasing connection line much shorter than $\lambda_{1GHz}/20$ and with the resistor in spite of the series inductors. As can be seen from the results, the attenuation is drastically reduced, reaching a maximum of roughly 0.2dB at 1GHz.

Concerning the PCB layout, the IEC standards furnish rather detailed guidelines in order to manufacture a reliable board which should guarantee repeatable DPI results. As already discussed for the injection network, such advices aim also at making the board suitable for different EMC tests.

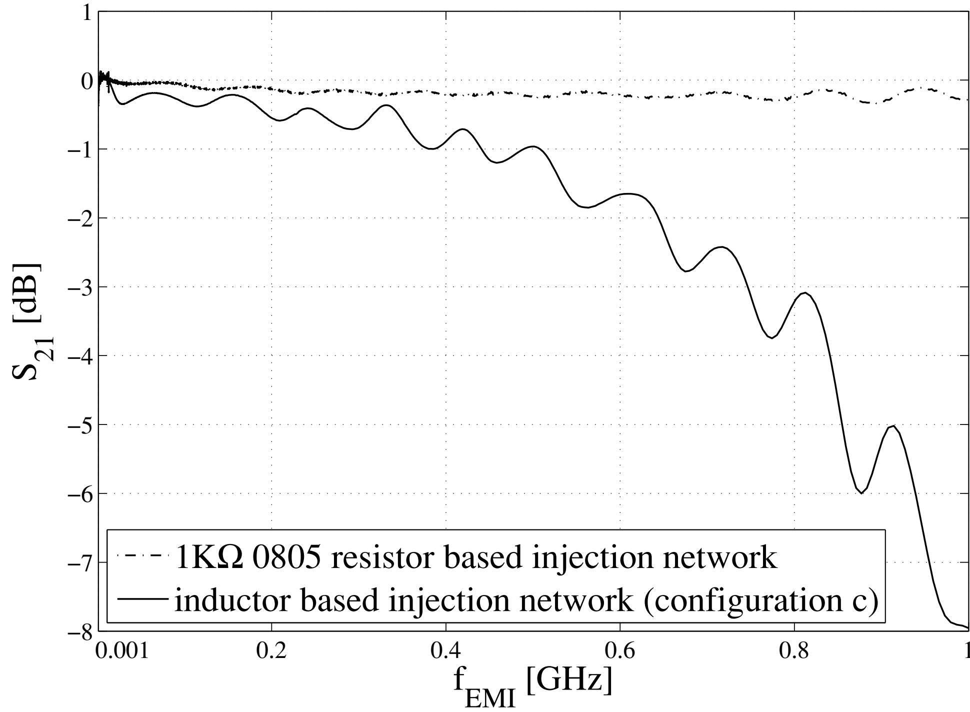

FIGURE 5.16: Comparison between inductor based and redesigned resistor based injection network S_{21}.

For example, the suggested board should be a square of 100mm^2, with only the IC DUT on one side and all the other components on the other side, since this allows it to be employed for susceptibility tests inside a TEM cell ([66], [67]). If the board has to be optimized just for DPI tests, other precautions can be taken. First, the board should be as small as possible, since the power planes resonance frequencies for the mth mode (x direction) and for the nth mode (y direction), can be expressed as ([68]):

$$f_{res} = \frac{c}{\sqrt{\epsilon_r}} \sqrt{\left(\frac{m}{l_x}\right)^2 + \left(\frac{n}{l_y}\right)^2} \tag{5.6}$$

Being c the speed of light, ϵ_r the PCB dielectric permittivity and $l_{x,y}$ the linear dimensions of the PCB power plane. From expression (5.6) it is possible to note that a $7\text{x}7\,\text{cm}^2$ square power plane on a PCB can already have a resonance frequency associated to the 10 or 01 modes close to 1GHz, while a $10\text{x}10\,\text{cm}^2$ power plane has the first resonance frequency at around 700MHz.

As suggested by the regulation, the board should be equipped with two ground planes on both external top and bottom layers and such planes should be connected with vias outdistanced no more than 10mm one from the other and with a diameter of 0.8mm each. Also in this case, if possible, the number of vias should be maximized by decreasing as much as possible the distance between them and their diameter. Another precaution that can be taken is the use of horizontal SMA connectors instead of vertical ones, since this can contribute to reduce the board dimensions.

Finally, special attention should be paid in the layout of the 50Ω traces connecting the EMI injection port of the PCB to the DC blocking capacitor (Fig.5.15). The proposed solution for the test bench setup 50Ω traces is to use traces with the same width of the SMD components they are connected to, like the 6.8nF DC blocking capacitor in this case. From this value it is then possible to calculate the distance between the trace and the surrounding ground plane such to obtain a 50Ω characteristic impedance for the trace itself.

Considering the cross section of a microstrip PCB trace on a two layers PCB with top and bottom ground planes (Fig.5.17), it is possible to resemble such structure to a coplanar waveguide. If the trace width *w* has already been fixed and the PCB parameters, such as the substrate relative dielectric permittivity ϵ_r and the board thickness *h*, are known, it is possible to numerically calculate the trace-ground plane gap *s* needed to obtain a 50Ω characteristic impedance Z_0 of the track, since according to [69]:

$$Z_0 = \frac{60\pi}{\sqrt{\epsilon_{eff}}} \frac{1}{\frac{K(a)}{K(a')} + \frac{K(b)}{K(b')}} \quad (5.7)$$

Where $a = \frac{w}{w+2s}$, $a' = \sqrt{1-a^2}$, $b = \frac{\tanh \frac{w\pi}{4h}}{\tanh \frac{(w+2s)\pi}{4h}}$, $b' = \sqrt{1-b^2}$ and $K(x)$ represents the elliptic integral of first kind.

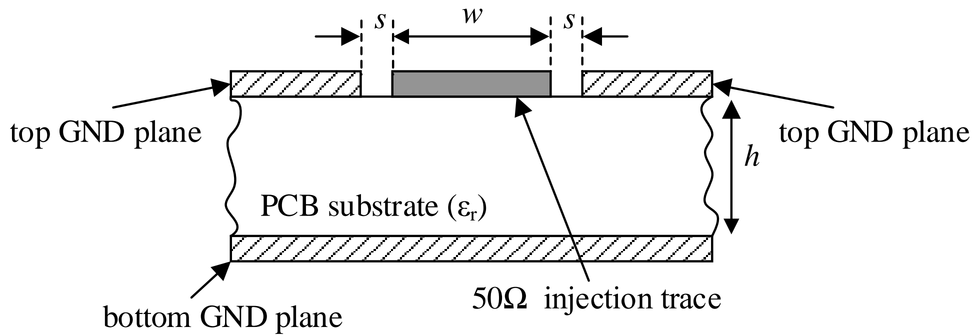

FIGURE 5.17: PCB cross section with injection line, top and bottom ground planes.

For example, a 0805 SMD capacitor has usually a 1.4mm wide PCB footprint for the land pads. Taking this dimension as the track width for the 50Ω line and considering an FR4 ($\epsilon_r = 4.35$) 16mm thick PCB, it is possible to calculate the width of the gap *s* between the ground plane and the trace to be around 0.23mm in order to get a characteristic impedance of 50Ω for that trace. The pictures in Fig.5.14 and Fig.5.18 show an example of DPI test boards

employed for the EMI injection into the devices designed along the Ph.D. work. As can be observed, both PCBs are designed according to the standard guidelines, but the PCB in Fig.5.18 complies with all the aforementioned enhancements made to optimize the results for conducted disturbances up to 1GHz. The proposed DPI test board and injection network design and layout have been conceived in order to optimize the DPI measurement results in terms of clearness, simplicity and compliance with the simulation results. Other more sophisticated injection setups have been proposed in the literature, as alternative solutions to the standard ones described in the regulations, in order to achieve high degree of insulation between the high frequency disturbance path and the DC path. As an example, in [31] the injection path is composed by a solid tubular outer conductor which enables the dielectric and the inner conductor to remain precisely spaced and enables to measure the voltage between the outer and inner conductor at any point. The high performances of such setups make them quite suitable to achieve clean and reliable DPI measurements, although their complexity is higher than the one of a simple PCB. Furthermore, the guidelines proposed in this Chapter do not require any electrical knowledge about the frequency behaviour of the board.

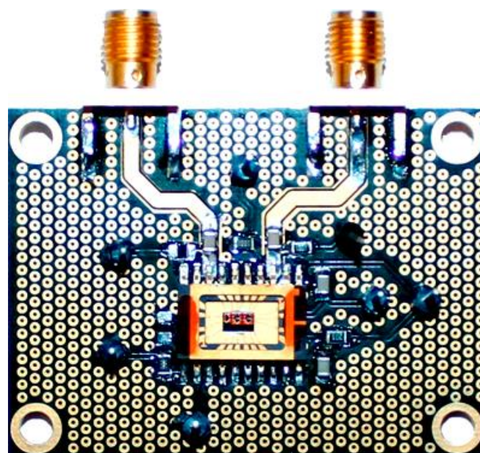

FIGURE 5.18: Enhanced EMI injection PCB example.

As a matter of fact, another popular approach implies to characterize the PCB in the frequency domain by measuring the S parameters between the board injection port and the pad where the DUT pin under test has to be connected ([32]). With this procedure it is possible to precisely measure the attenuation of the injection path due to losses, to evaluate how much power is reflected back by the DUT and to counteract for this during the EMI injection, in such a way to perform a de-embedding of the S-parameters in order to subtract the board effect from the actual measurement and to determine the real power injected into the DUT IC pin.

Such approach has anyway not been adopted for the present Ph.D. work, for which a board layout with almost no effects on the injected signal, up to 1GHz, has been preferred due to its easiness. Nevertheless, the avoidance of the board de-embedding has been possible only because of the simplicity of the tested DUTs, for which not many pins and injection points were needed and very small and simple two layers board layouts could be used to perform the DPI tests. If this would have not been the case, a full test board de-embedding and measurement

system pre-calibration would have been necessary in order to obtain interpretable results for the ICs susceptibility. On the other hand, a simple de-embedding and calibration has been performed for the measurements of the OpAMPs susceptibility at wafer level, as explained in Section 5.3.

5.2.4 Complete enhanced PCB level DPI test bench

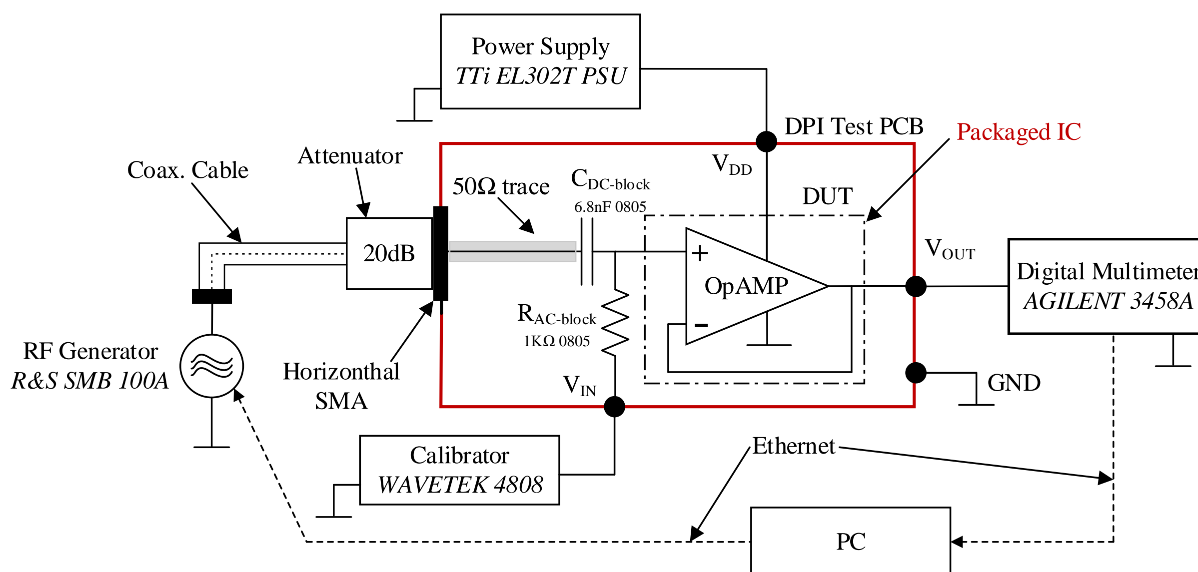

FIGURE 5.19: Complete enhanced PCB level DPI test bench.

5.3 DPI at wafer level

The direct power injection test procedure is usually performed in such a way to evaluate the IC robustness in a condition as close as possible to the one the IC faces in its real word operation. The injection is then performed on a packaged IC laying on a PCB which models, from an EMC point of view, the PCB the IC operates onto in the real application, with all the protection elements included in the test bench. This method proves to be very useful to make a complete system level susceptibility test.

On the other hand, if the aim of the investigation is to understand and evaluate the susceptibility of standalone building blocks composing the whole IC, the system level test can be less suitable, since it hides the susceptibility behaviour of each independent block, making it difficult to evaluate the performance of each part of the design independently from the others.

One solution to this problem could be to fabricate separate ICs containing each one a block of the complete system and to test them separately. Since, in the real application, such blocks will most probably not be connected directly to the external word by means of a lead frame, pads and bond wires, the drawback of this solution is that testing each one of them in a separate package could hide some of their EMI susceptibility characteristics because of the effects the

packaging has on the injected high frequency disturbances ([70]). Furthermore, due to the time and cost overhead such proposal implies, other ways have been conceived in order to independently evaluate the susceptibility of each individual block.

An alternative solution implies to inject the EMI disturbances directly at wafer level, using special high frequency probes which can land directly on the unpackaged silicon die and can be used to bias the IC, to inject the disturbances and to monitor the IC output response without the need for a package and a PCB ([71]). By doing so, it is then possible to perform the cleanest possible EMI susceptibility evaluation of standalone building blocks like operational amplifiers, as it has been the case for the present Ph.D. research. The test bench employed for wafer level DPI is depicted in Fig.5.20.

Up to the end of the injection path, such test bench is identical to the one employed for PCB level DPI (Fig.5.19), hence it comprises an RF generator, an injection path and an attenuator. Being the PCB not present, the wafer level setup needs a separate injection network in order to isolate the DC biasing path from the EMI injection path. This is achieved by a separate standalone PCB dedicated to the bias T structure described in Section 5.2.3 and designed according to all the aforementioned guidelines. The silicon dies are glued to a copper plate used to hold them and to bias their substrate with a defined potential (Fig.5.21). The silicon die pads, connected to the actual integrated circuits, are accessed via such high frequency ground-signal-ground (GSG) probes (Fig.5.21) which are usually employed for microwave metrology. The probes ensure the test bench setup to be a 50Ω system up to the landing pads of the IC, hence they provide the advantage of having no impedance discontinuities from the RF generator up to the DUT pads.

Although the use of such GSG probes brings several advantages, it also forces the IC designer to create the correct pads structure suitable for the probe landing shape. For each signal

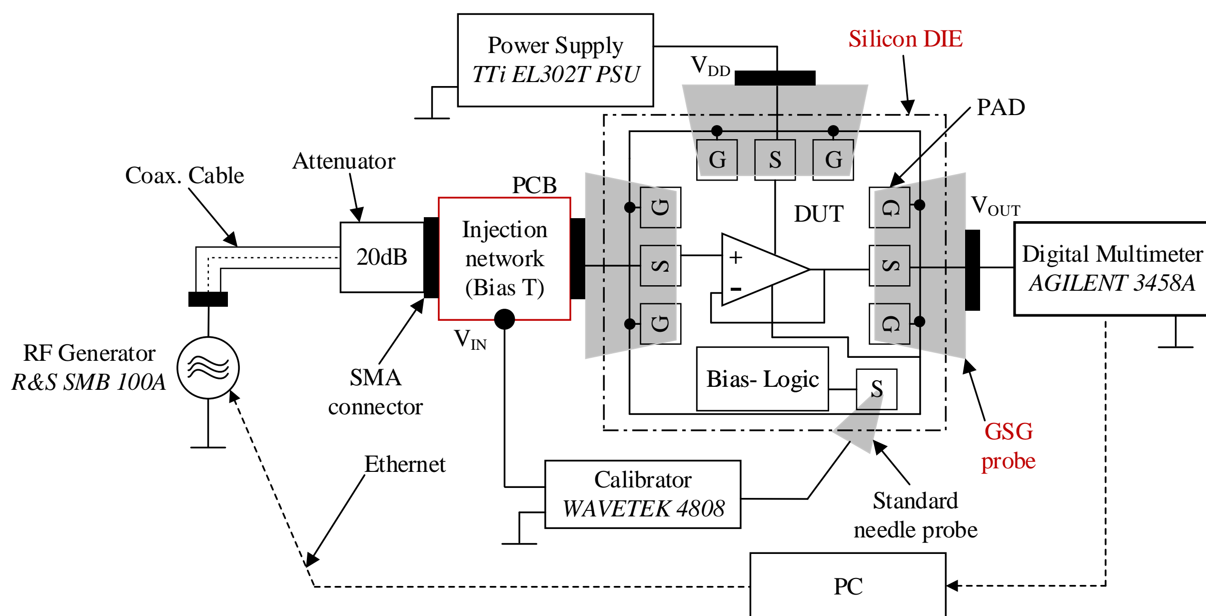

FIGURE 5.20: Complete wafer level DPI test bench.

pad, two surrounding ground pads have to be placed in order to sustain the three needles of the GSG probe. For all the cells investigated along the Ph.D. work, the adopted grounding strategy has been to design and layout a ground plane connecting all the G pads of the RF probes together instead of exploiting single metal traces, so to minimize the parasitics along the ground loop (Fig.5.22).

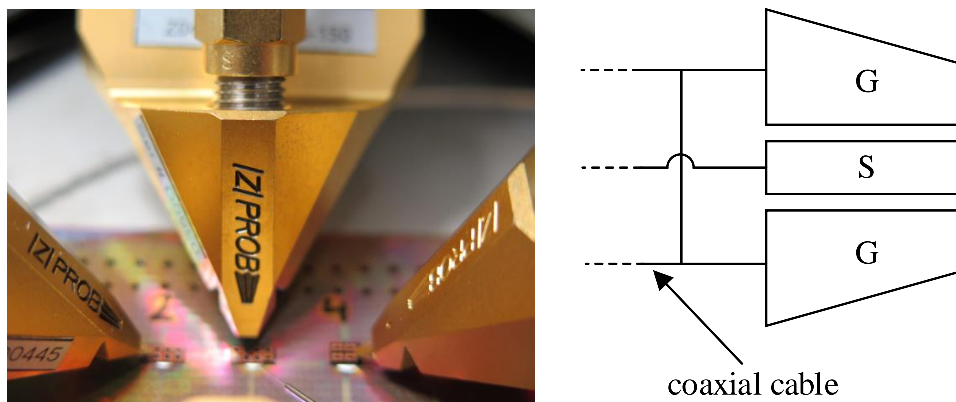

FIGURE 5.21: GSG probes and dies glued on metal substrate.

Not every signal must be handled with the high frequency probes. The paths along with no high frequency disturbance is supposed to propagate can be probed with standard needles, so that no further ground landing pads are needed around the one which is intended to carry the signal itself. This would be the case, for example, of a DC signal exploited to bias the IC and AC decoupled from every possible injection path, as depicted again in Fig.5.20 and in Fig.5.22 (bottom right).

Differently from the case in which the injection is performed through a PCB, the injection at wafer level does not imply a complex characterization ([32]) of the injection setup in order to de-embed it and to counteract for its attenuation. As a consequence, if the RF amplifier, the directional couplers and the RF power meters can be avoided, as it is the case of the presented DPI setup for low injected power levels, and if no PCB holding the packaged IC is used, as

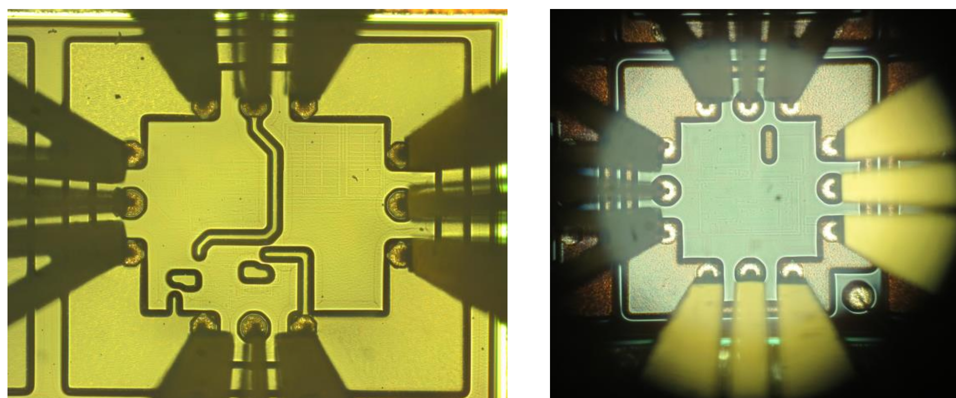

FIGURE 5.22: Ground plane for GSG probes landing.

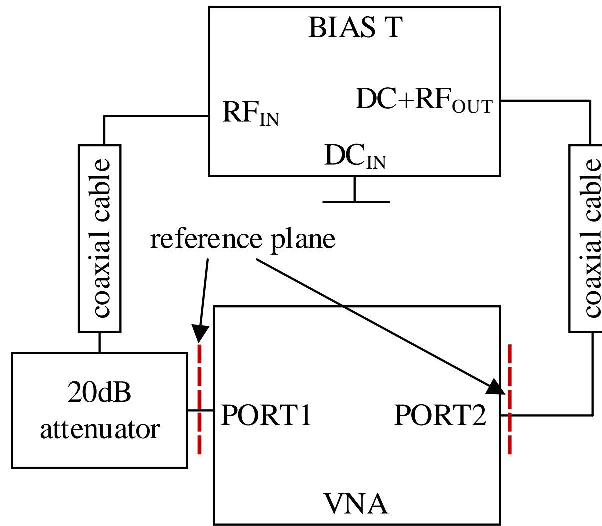

FIGURE 5.23: Injection path and injection network calibration setup.

it is for wafer level measurement, the only remaining part of the test bench which needs to be characterized is the small bias T PCB together with the cables connecting it to the GSG probes and the attenuator. Such calibration procedure is intended to measure the power loss experienced by the EMI signal before it reaches the injection GSG probe and can be carried out exploiting the configuration depicted in Fig.5.23. The bias T, together with the coaxial cables and the attenuator that are used for the injection, can be connected to a VNA and the S parameters of such two port network can be measured. It must be pointed out that, for such kind of characterization and scenario, the $\mathrm{DC_{IN}}$ port of the bias T should be grounded, because the DC source of the injection test bench setup can be considered as an AC ground, so that the bias T can then resemble a two port network. From the S parameters measurement it is then possible to calculate the network insertion loss (IL) defined by (5.8).

$$IL = -20\,log_{10}\left(|S_{21}|\right) \tag{5.8}$$

This parameter IL represents the correction factor that must be added to the RF power of the generator in order to correctly estimate the amount of power reaching the DUT. Since the IL will generally be a function of the frequency, the automation procedure for the injection can be written in order that, at each injection frequency, the power of the RF generator is corrected accordingly to the pre-calibration data. It would be possible to argue that, with such procedure, the attenuation of the RF GSG probes is not taken into account. For most commercial probes, the attenuation is in the range of 0.3dB – 0.4dB ([72]) and since the complete calibration procedure taking into account the probes loss is rather complex, it is possible to simply add such loss as a constant value to the power injected by the RF generator, if the accuracy of the input power can be accepted to be lower than 1dBm.

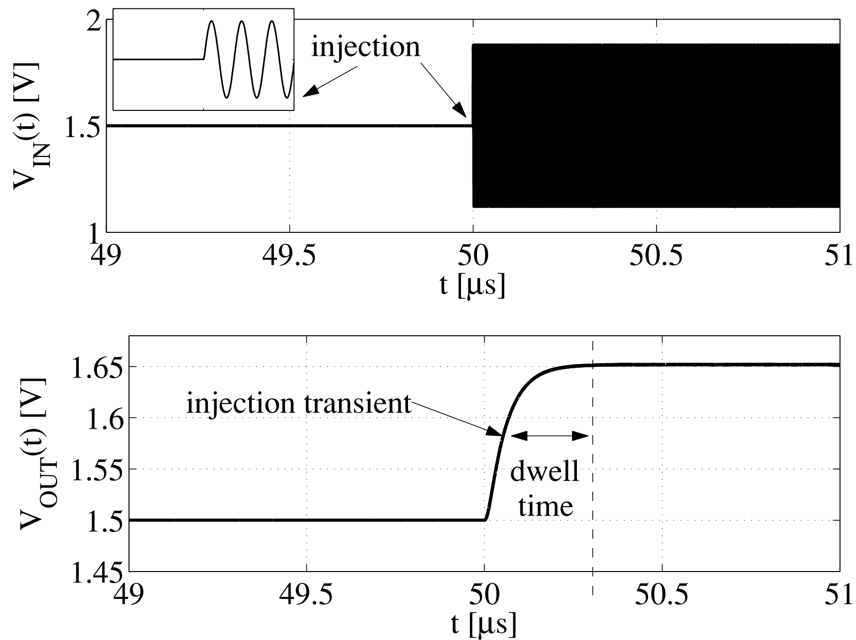

FIGURE 5.24: Injection transient for input and output voltages of a buffer connected OpAMP.

5.4 Measurement automation and data recording

Independently from which DPI scenario is taken into account, either considering PCB level or wafer level injection setups, the susceptibility test implies the injection of disturbances at different frequencies in the range 150kHz – 1GHz, with a frequency step from 100kHz to 1MHz, depending on the injected frequency value and at different power values up to 37dBm, with power steps of 0.5dB ([55], [28]).

As discussed at the beginning of this Chapter, DPI tests on standalone low voltage CMOS OpAMPs designed to operate inside a bigger circuit cannot be performed according to the aforementioned settings. On the other hand, even if the frequency range is shortened or, most importantly, the maximum injection power is lowered, the DPI measurement cannot be performed step by step by the engineer and must be automated. Unfortunately, the way such automation is performed and the way the DPI result data are collected are strictly dependent on the DUT failure criteria.

Since the main focus of the Ph.D. work has been to investigate the DC shift or offset induced by conducted EMI to the input of CMOS OpAMPs, such offset represents then the parameter according to which the susceptibility of the OpAMP is evaluated. In other words, the quantity of interest as a result of the DPI test is represented by the mean value of the amplifier output voltage, regardless of its AC behaviour. Such aspect is of extreme importance since it defines some core characteristics of the measurement, like the type of monitoring device and the timings.

In particular, if the DC shift at the output of the amplifier is of concern, the monitoring

device has to be an instrument with a very low bandwidth compared to the lowest injection frequency, such as a multimeter set as a DC voltmeter. Alternatively, the data can also be acquired by means of an oscilloscope, but the averaging must then be performed in post processing by the operator or by the instrument itself. Another important aspect to be taken into account is represented by the RF generator ON/OFF status and power level control strategy. To explain this concept it is possible to observe the plot in Fig.5.24, which represents a simulation example of injection transient behaviour for a buffer connected CMOS OpAMP injected with a 300MHz continuous wave disturbance at its input (Fig.5.3) superimposed with 1.5V DC nominal signal. As can be noted from Fig.5.24, after the EMI is injected the output of the amplifier gets DC shifted only after a transient, called injection transient. After that, the output voltage takes a steady state value and its average can then be evaluated. The difference between the time the EMI is injected and the time the average output of the OpAMP is recorded is of crucial importance, since recording the output too early leads to a wrong evaluation of the output voltage mean value. The delay between the EMI injection and the output recording is called dwell time ([28]) and must be defined before the automated DPI measurement is performed.

A possible strategy for the automation of the measurement procedure is represented by the flow chart in Fig.5.25a. The control software loops on the disturbance frequency (f_{EMI}) and power (P_{EMI}) ranges so that every couple (f_{EMI}, f_{EMI}) is used for the injection. As can be noticed from the chart, the EMI injection power has to be corrected, at each frequency step, according to the values obtained from the pre-calibration procedure discussed in Section 5.3, so that, at the ith power step of the injection, the actual power selected for the RF generator should be calculated as in (5.9), where $IL(f^j_{EMI})$ represents the insertion loss at the jth frequency step.

$$P^i_{RF_GENERATOR} = P^i_{EMI} + IL(f^j_{EMI}) \tag{5.9}$$

After the interference is injected, the system must wait for the dwell time before recording the output value of the amplifier measured by the monitoring device. Another timing issue is represented by the interruption of the EMI injection: also in this case the OpAMP experiences a transient at its output, so that some time is needed before such output returns to its nominal value and the next injection can be performed. Although shorter dwell times for the automated system mean a faster measurement, if the chosen dwell time is shorter than the actual injection transient, artefacts can appear in the device susceptibility results, as far as the output DC shift is considered. Unfortunately, the prediction of the correct timing is not always possible a priori by means of hand calculations or CAD simulations. Consequently, the best strategy is to perform single DPI measurements at different frequencies and power levels and to monitor the amplifier output with an oscilloscope in order to understand which is the maximum dwell time needed for the device to settle after the injection is turned ON or OFF. The flow chart depicted in Fig.5.25a represents an example of a DPI measurement procedure suitable to highlight the actual behaviour of the device over injected EMI frequency and a common result, out of such a procedure, is represented by an output DC shift curve as the one shown in Fig.5.9 (dotted line). Such way of result data collection is the one mostly employed along the present Ph.D. research, since it explicitly highlight the variation of the amplifier response in dependence of EMI frequency and power.

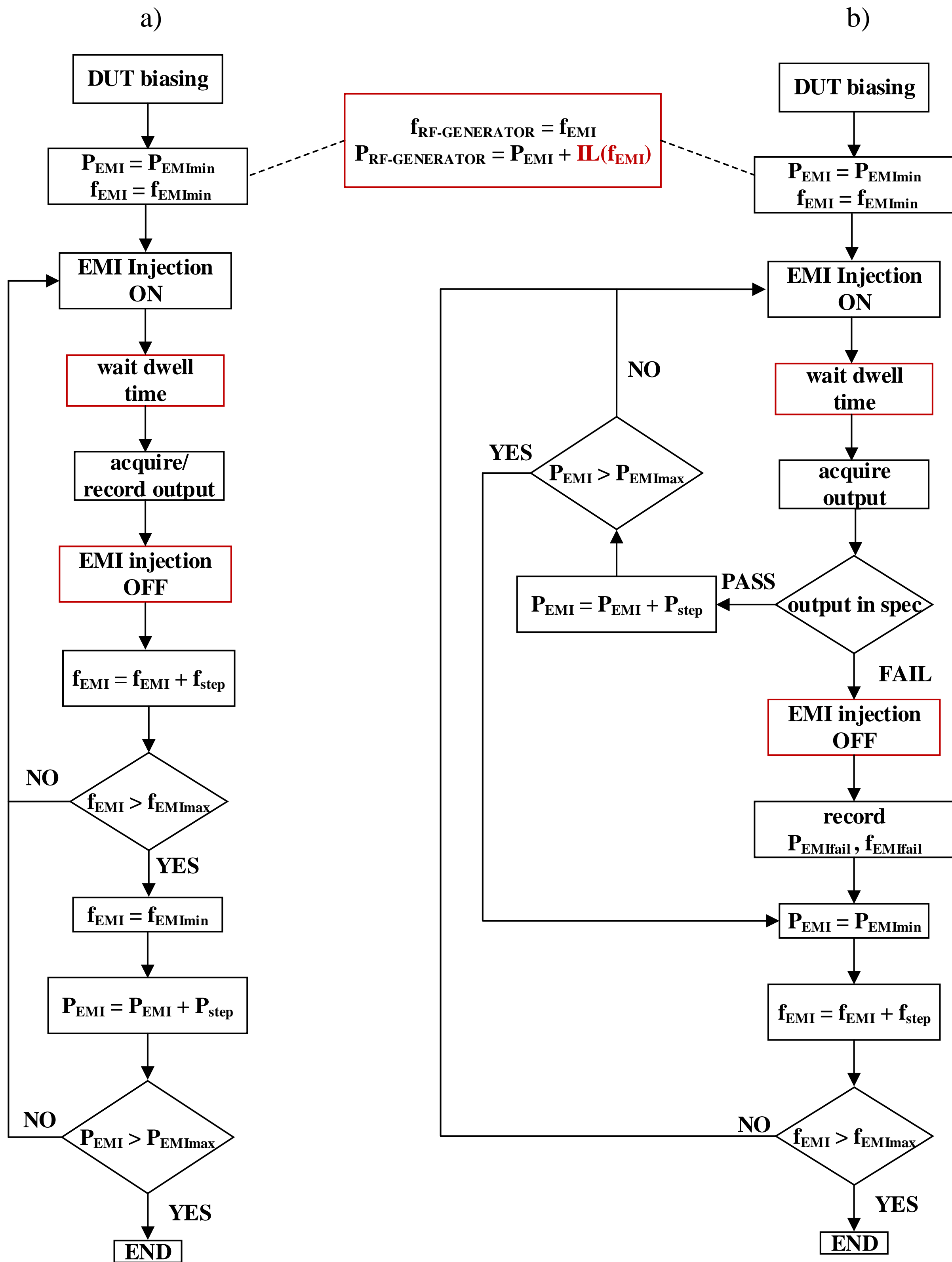

FIGURE 5.25: EMI susceptibility measurement automation flow charts.

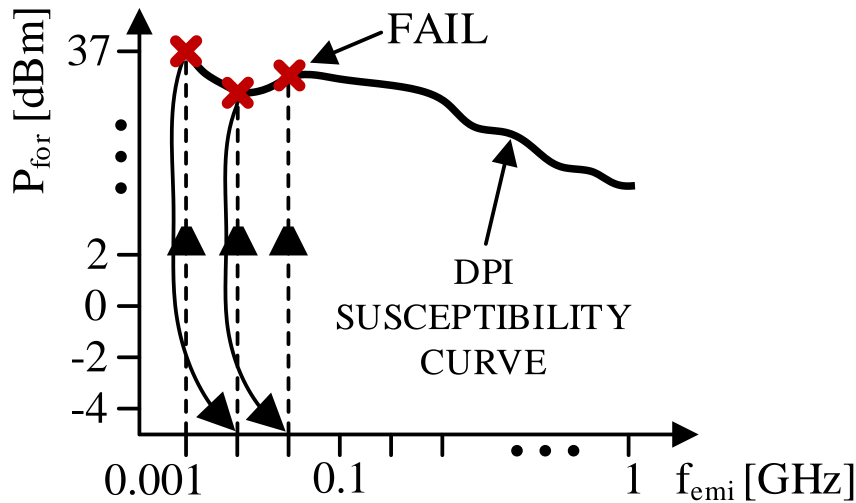

FIGURE 5.26: Example of resulting DPI susceptibility curve out of a PASS/FAIL DPI test.

Another possible and very common way of collecting susceptibility results is represented by a PASS/FAIL DPI test performed according to the strategy shown in Fig.5.25b. In this case, the measurement is performed not accordingly to a predetermined set of EMI frequencies or power levels, but it is instead performed increasing the injection power and the injection frequency up to the point at which the DUT output reaches a failure condition, for example if it exceeds a predefined percentage of its nominal value. When this condition is reached, the injection is then interrupted and the frequency and forward power values at which the failure took place are recorded.

The next injection takes place again starting from the following EMI frequency and raising the EMI power level at each step. The result of such measurement strategy is usually expressed as a curve in the frequency domain, representing the forward power values at which the DUT failed (Fig.5.26).

Although such strategy is very useful, for example, to compare DPI results from different DUTs, it can indeed hide the actual behaviour of the devices under EMI injection, since it does not furnish a complete overview of the devices output trend, but it only highlights at which point the devices reach a certain failure condition. Furthermore, since the test is conceived in such a way to be stopped after the failure condition is reached, no information is then provided about the DUT behavior for EMI power levels and frequencies above the one at which the failure is encountered. Because of the aforementioned issues, this measurement and data collection strategy has not been used in order to investigate the EMI susceptibility of the CMOS OpAMPs designed along the Ph.D. work. Indeed, every susceptibility results presented in this manuscript shows the actual trend of the amplifiers average output voltage during the EMI injection, making it possible to analyse and explain the reasons of such behaviour looking at the OpAMPs structure.

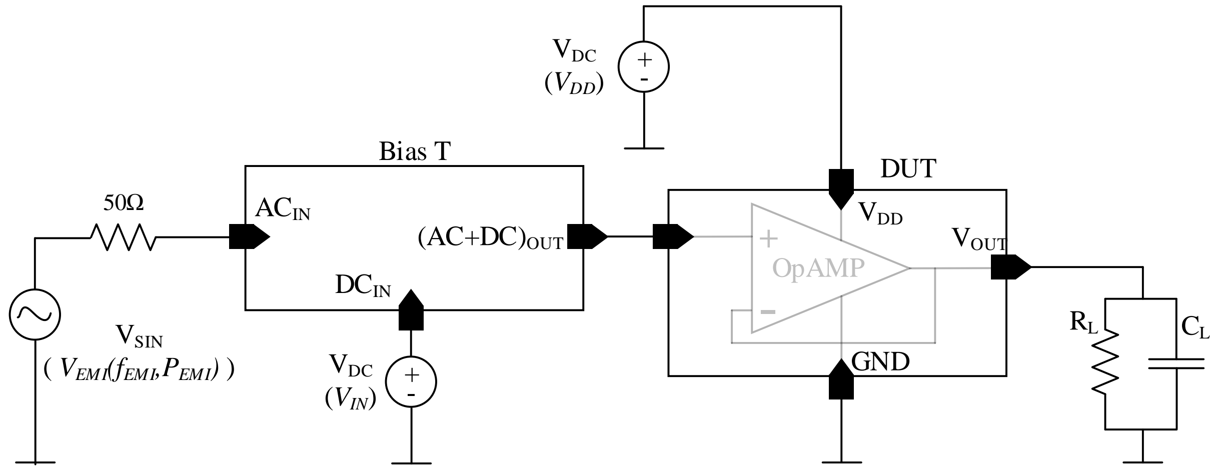

FIGURE 5.27: CAD test bench for EMI injection simulations.

5.5 Simulation strategy and test bench

The present Section provides considerations regarding how DPI immunity tests can be carried out at simulation level by means of CAD tools, like OrCAD Cadence and PSpice. Given the high costs and development time for integrated circuits, companies which design and manufacture ICs which operates in EMI harsh environments tend to avoid redesigns and aim at the lowest possible time to market for their products. This aspect goes somehow against their chance of producing EMI robust ICs according to the standard regulations in one shot, because the EMI susceptibility of ICs cannot usually be easily predicted by rough calculations during the design or concept phase.

From this point of view, CAD simulations can be of great help in order to predict the weak points of the circuit during its operation under EMI. Dealing with automotive ICs makes such simulations almost mandatory since they help companies saving time that would otherwise be lost waiting for the IC to be manufactured together with all the equipment necessary for susceptibility measurements, such as custom EMI test boards.

If such simulations are performed correctly and if the simulation test benches are compliant with the real environment the IC is operating in, the chance to discover and correct EMI susceptibility issues at IC level during the design phase can be dramatically increased, avoiding costly post production redesigns. For all the previous reasons EMC simulations are of crucial importance. Along the present Ph.D. work, special attention has been put in creating a DPI simulation test bench which modelled in the best possible way the actual environment in which the integrated OpAMPs were operating during the DPI injection tests. The test bench CAD schematic employed to evaluate the EMI susceptibility of the devices is sketched in Fig.5.27.

The block called DUT contains the transistor level schematic of the specific operational amplifier, ideal DC voltage generators are used to model the power supply and the input voltage source while an ideal sinusoidal voltage generator is used to model the EMI disturbance as continuous wave (CW) sinusoidal signal. Besides such elements, which are part of the standard analog library of the most common circuit simulators, two other components are added to the

schematic in order to profitably model the DPI measurement environment, namely a bias T and a 50Ω resistor in series to the EMI generator.

The 50Ω resistor serves to model the input impedance of the RF generator ([56]) and has been added as an ideal component. The bias T represents the injection network used to decouple the DC biasing path at the amplifier input stage from the AC disturbance path coming from the RF generator model. The bias T deserves special attention since its frequency behaviour is one of the main contributors affecting the injection path. Although the first way of modelling the bias T would be to use an ideal inductor as an AC block and an ideal capacitor as a DC block, such simple strategy would lead to underestimate too many non ideal effects of actual discrete components, such as inductors and capacitors self-resonances, as already discussed in the Section 5.2.3.

The strategy adopted for the proposed simulation test bench has been the evaluation of the impedance of each element intended to be used in the injection network by means of S parameters measurements (see Section 5.2.3). Considering the improved version of the bias T employing a $1k\Omega$ 0805 resistor as AC block and a $6.8nF$ 0805 DC block capacitor (Fig.5.15), such two discrete components have been subjected to S parameters measurements which have then been fed to the FEM high frequency simulator ADS ([73]) in order to obtain, for each component, a lumped element model which could then be plugged into the Spice simulation environment to resemble the frequency behaviour of the actual discrete components used for the bias T. The picture in Fig.5.28 shows the models obtained for the resistor and capacitor impedance measurements. Concerning the modelling of the OpAMP, the DUT block is made by a Spice netlist representing the amplifier transistor level circuit and containing also all the parasitic capacitances and resistances extracted from the layout view of the OpAMP itself. Such procedure represents what has been done to predict the EMI susceptibility by simulating the ICs designed along the Ph.D. work. The degree of modelling adopted in this case can certainly be enhanced, since, with the presented strategy, no effects of the PCB or cables are either taken into account or modelled ([30]). On the other hand, if the board can be designed

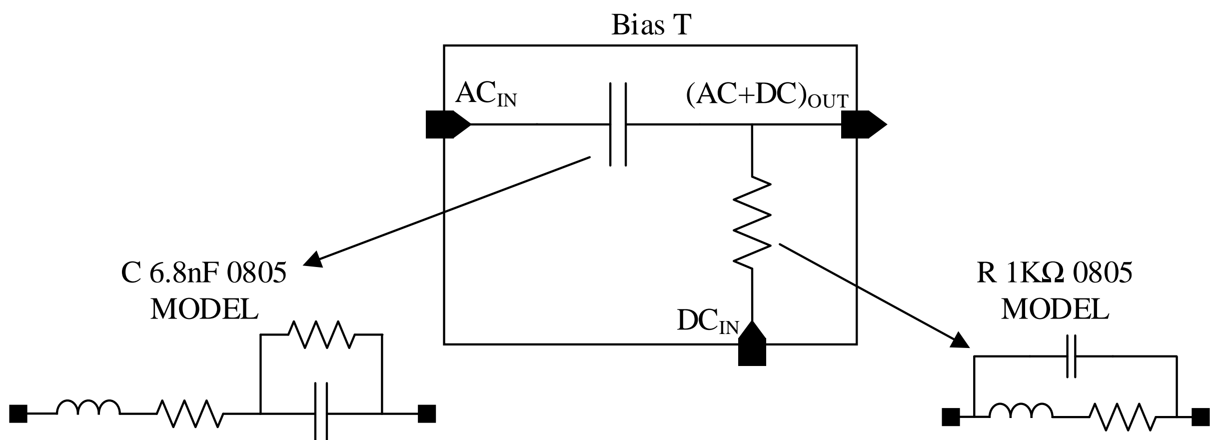

FIGURE 5.28: Bias T lumped elements modelling for the CAD simulation test bench.

such to have negligible effects compared to the one of the bias T elements, as already previously pointed out and explained, the presented strategy can represent a fair trade off between modelling complexity and simulation accuracy.

5.6 Direct Power Injection test bench for automotive ICs

Although the mentioned standards and regulations outline the commonly accepted techniques used to evaluate the EMC performances of integrated circuits, further documents do exist which introduce other concepts and add-ons to the standard test benches in order to perform emission and susceptibility measurements for specific IC operational fields.

The “Generic IC EMC test Specification” ([55]), here mentioned for completeness, is a document which describes the technical basis to define common tests characterizing the EMC behaviour of ICs, with a special attention to the automotive environment. The first remarkable addition to the IEC specifications provided by such document is the introduction of the broadband artificial network (BAN), which has to be added to the injection network described in Section 5.2.3 (Fig.5.29). The BAN is composed by an AC blocking $5\mu H$ coil L_{BAN} and by a series $R_{BAN} - C_{BAN}$ group inserted in parallel to the injection line and consisting of a 150Ω resistor and a $6.8nF$ capacitor.

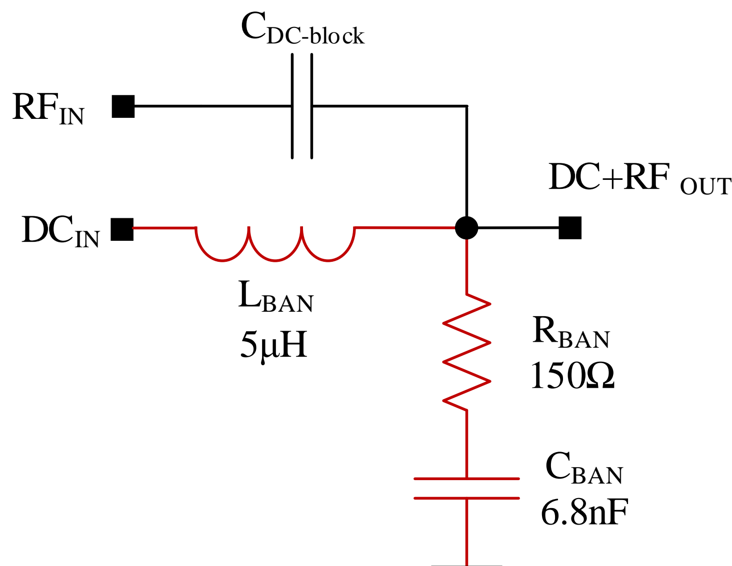

FIGURE 5.29: Broadband Artificial Network (red).

The $5\mu H$ coil L_{BAN} has been conceived in order to model the vehicle cable harnesses inductance. Taking into account that, for an average car length of 5 meters, the IC can be connected to a cable up to five meter long and considering an average inductance of $1\mu H/m$, the value of $5\mu H$ is then suitable to model the worst case parasitic inductive behaviour of automotive wirings. The $R_{BAN} - C_{BAN}$ series network inserted in parallel after the AC blocking coil is used to fix the high frequency impedance of the line to a maximum value of 150Ω. Such series group is in fact employed to model the impedance between the cable harness and the vehicle chassis.

In order to model in the best possible way the effects of the vehicle wirings on the EMC behaviour of the IC itself, the BAN is then connected to every IC pin which is actually attached, in the application, to a vehicle’s cable harness. The described ones are just some of the additions

mentioned in the document, but are actually the most important ones for the evaluation of the ICs EMI immunity against conducted interferences.

Although such modifications and add-ons are extremely useful to model the automotive EMC environment, they have not been used for the proposed test bench employed along the Ph.D. research. The reason is that the setup proposed in [55] aims for the best way of modelling the automotive EMC environment and is meant for automotive ICs as actual commercial products. As already largely discussed, the aim of the present Ph.D. work has been instead to investigate the EMC performances of standalone CMOS amplifiers employed as part of bigger automotive ICs. As a consequence, a clear picture about the devices behaviour under EMI injection was needed in order to perform the investigations and explain the reasons of such behaviour looking at the OpAMPs transistor level structure.

Unfortunately, the BAN network introduces several non-idealities to the injection path, so that a full characterization of the board holding such network would be necessary in order to counteract for these non-idealities and to obtain clean susceptibility measurement results. To further clarify this concept, it is possible to consider the most important non-idealities of the BAN starting from the $5\mu H$ coil L_{BAN}.

The first thing to point out is that the L_{BAN} coil does not have an impedance greater than 400Ω on the frequency range 1MHz-1GHz, as testified by the plot in Fig.5.30, which represents an impedance measurement of a commercial $5\mu H$ EPCOS coil often used for such kind of EMC tests. As it is possible to note, the coil presents an inductive behaviour up to $95MHz$ and its impedance is greater than 400Ω only between $10.5MHz$ and $500MHz$.

Furthermore, the L_{BAN} must be able to withstand high DC currents, since it is used to test the behaviour of ICs connected between the vehicle battery and loads such as a bulb lumps ([55]). Such commercially available $5\mu H$ coils, which are able to withstand up to 10 amperes, are of considerable dimension, hence their presence along the injection path can add several parasitics whose frequency behaviour is hard to model and predict. This aspect can also be highlighted by the impedance plot of Fig.5.30, in which is it possible to note a quite discontinuous behaviour of the coil impedance after the main resonance peak. The second major non-ideal effect of the BAN network is ascribed to the presence of the series $R_{BAN} - C_{BAN}$ group used for impedance fixing.

The presence of these series components inserted in parallel to the injection line creates a low impedance path for the EMI high frequency disturbance, so that such disturbance is partially driven to ground as its frequency increases, resulting in a reduced and non constant EMI power experienced by the DUT over frequency. For all the aforementioned reasons, the EMI injection test bench proposed in this chapter has been preferred also to the one described in [55], being the purpose of the present Ph.D. investigations not the one of evaluating the standalone amplifiers EMI immunity as off the shelf automotive ICs.

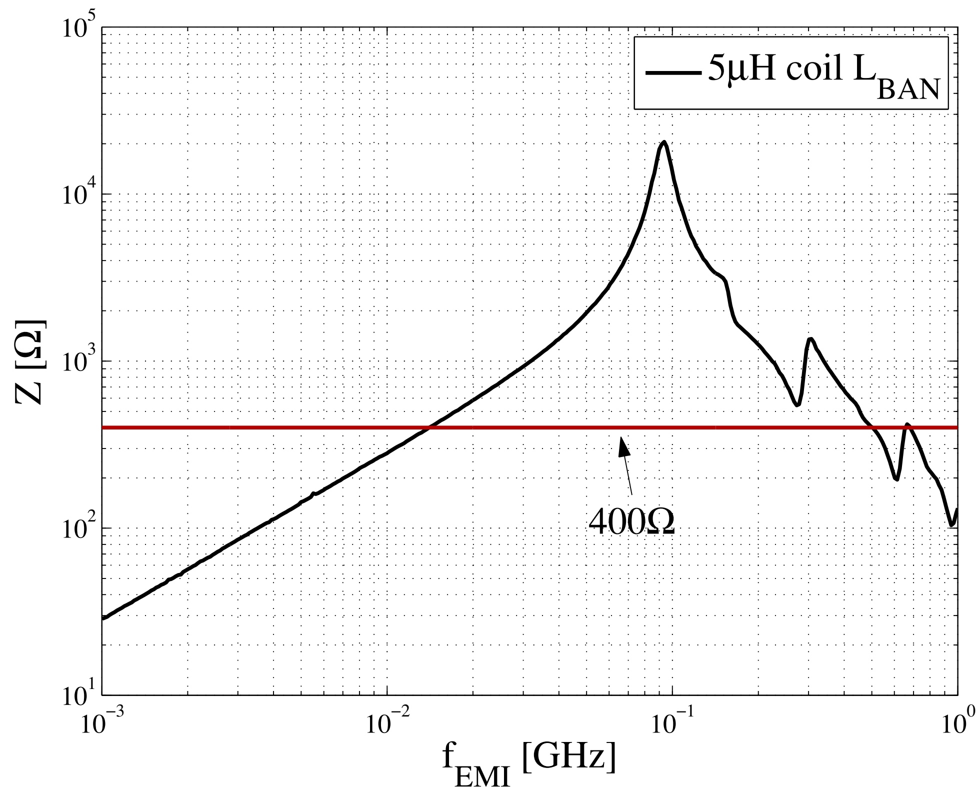

FIGURE 5.30: 5μH EPCOS coil impedance.

CONCLUSIONS

The present Ph.D. dissertation focuses on the susceptibility of integrated precision offset compensated CMOS operational amplifiers to high frequency electromagnetic interferences conducted at the amplifiers input stage. Furthermore, it highlights possible solutions and concepts to enhance the EMI robustness of such integrated circuits depending on the employed topology and technological offset compensation technique. As last, the research work focuses on the optimization of the available test bench simulation and measurement setups in order to enhance the evaluation of the amplifier EMI susceptibility in terms of result clearness. Due to their innovativeness and novelty, all such topics represent a scientific contribution either for the μEMC community and for the industries involved in the development of accurate sensing integrated circuits operating in EMI polluted environments. In particular, research broadens the knowledge about the EMI susceptibility to more sophisticated integrated circuits, moving from the notions about standard operational amplifiers to the offset compensated ones, more complex in terms of topology and operation. Main results are listed in the following.

- The modelling of the EMI induced offset in standard OpAMPs, already largely investigated in the literature ([14], [15] and [19]), is here refined and physically validated focusing on the modelling of the parasitic capacitances of the amplifier input stage while taking into account for OpAMP parameters such as operating region, power consumption and layout. The analysis proves to be useful in providing several tools in order to evaluate the amplifier robustness against EMI directly during the early design phase.

- The modelling of the EMI induced offset in chopped operational amplifier is provided and physically validated, taking into account either the effects of the parasitic on resistance R_{ON} of the input modulator switches (model (4.10)) but also the effect of EMI appearing at the multiples of the chopping frequency f_{CH} (model (4.19)). The results show that, comparing chopped OpAMPs with regular offset uncompensated ones, the formers can be considered less EMI susceptible in a broad sense, because of the filtering effects of the input modulator. On the other hand, the DC shift peaks appearing at the chopped amplifiers output and reaching 7% to 8% of the peak to peak EMI voltage, when the frequency of the disturbance hits the even multiples of the chopping frequency. This

shows that there exist some unlikely-to-happen conditions in which a chopped amplifier can experience an EMI induced offset greater than a regular continuous time offset uncompensated one.

- A detailed design of an auto-zero offset stabilized amplifier is provided and physically validated. Although the partial novelty of such contribution, several aspects concerning pure IC design topics on this topology have been discussed because of their importance for the understanding of the device operation and its EMI susceptibility. Furthermore, although some detailed descriptions are provided in the literature about the design of this kind of offset compensated amplifiers ([44], [43], [46]), the present work touches several details which are barely available in the mentioned literature, such as the stability considerations.

- The modelling of the EMI induced offset in auto-zero offset stabilized operational amplifiers is provided and physically validated. The behaviour of such topology under input EMI injection is largely discussed, showing which parts of the topology are involved in the amplifier's EMI susceptibility and proving that the EMI induced offset generated by an auto-zero offset stabilized amplifier mainly depends on the auxiliary amplifier characteristics.

- The comprehension of the key points involved in the susceptibility of chopped and auto-zero offset stabilized amplifiers provides all the tools needed to perform EMI robustness enhancements of the amplifiers themselves. Some of these robustness enhancements proposals have also been validated, as in the case of the EMI enhanced chopped amplifier of Section 3.3. More importantly, the research work provides a fair and complete comparison between chopping and auto-zero offset stabilization techniques in terms of EMI susceptibility. The main outcomes of such comparison can be listed as follow:

  - Neither chopping nor auto-zeroing can be employed to compensate for the EMI induced offset as they do for the technological one.
  - The EMI susceptibility of chopped OpAMPs can be considered, to some extent, close to the one of regular OpAMPs, with the exceptions highlighted in Chapter 3. The EMI susceptibility of auto-zero offset compensated OpAMPs mainly depends on the EMI susceptibility of the auxiliary OpAMP, hence, the fair comparison between the two techniques is deeply affected by the characteristics of the auxiliary OpAMP itself. If such amplifier uses auto-zeroing for technological offset compensation, its susceptibility no longer differs from the susceptibility of a regular OpAMP with the same characteristics (input stage, biasing, etc.) of the auxiliary OpAMP. If the auxiliary amplifier uses chopping, the whole amplifier susceptibility is the same of a chopped OpAMP with the same characteristics of the auxiliary chopped OpAMP.
  - The choice for a chopped or an auto-zero offset compensated OpAMP can then be hardly driven by EMC considerations, since none of the two has particular benefits in terms of EMI susceptibility with respect to the other. Rather, the performance and

operating specification driven design should be preferred, but taking into account that the higher complexity of an auto-zero offset stabilized amplifier can be more difficult to harden against EMI with respect to a chopped one.

- Optimization of the standard measurement and simulation techniques employed for the EMI susceptibility evaluation of CMOS OpAMPs is provided and validated. The discussed enhancements affect every part of the test bench, from the RF generator side to the DUT side, touching the injection path implementation, the injection network implementation and the simulation procedure. The enhancements aim at shaping the test procedures to make them particularly suitable for CMOS operational amplifiers, since the measurement procedures in the regulations are standardized and can hide some effect of the disturbances on the IC or degrade the measurement clearness. The results are validated, showing the importance of obtaining clear and understandable simulation and measurement results in order to profitably compare the hypotheses, the developed mathematical models and the technology models with the actual behaviour of the physical devices subjected to high frequency input disturbances.

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