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Verification and Optimization of Galvanically Decoupled High Data Rate Battery Management System in a Standard CMOS Logic Process

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Abstract

Most state-of-the-art automotive battery management systems (BMSs) are using isolating Controller Area Network (CAN) buses for the communication between cell monitoring system and management system. This communication system is fast, secure and robust, but for a distributed system a way to expensive because CAN transceiver and CAN controller are necessary for every battery monitoring unit (BMU). To bypass the cost factor of the isolating CAN technology a new galvanically separated communication interface between the BMUs was invented by Infineon Technologies and allows data transfer between the monitoring units supplied by different local supply in case of stacked battery packs. The purpose of this master thesis is to verify and proof the functionality and optimize the communication testchip made in standard CMOS logic process.

Keywords: BMS, automotive, isolated communication system, EMC

Kurzfassung

Die meisten modernen Batteriemanagementsysteme verwenden für die Kommunikation zwischen Batterieüberwachungs- und Managementsystem isolierende CAN-Busse. Dieses Kommunikationssystem ist schnell, sicher und robust aber für ein verteiltes System viel zu teuer, weil zusätzlich zum Batteriemanagementsystem auch Sender- und Empfangskomponenten und die Kontrolleinheit für das Überwachungssystem erforderlich sind. Um die Kosten für zusätzliche teure Komponenten der CAN Struktur zu umgehen wurde ein neues galvanisch entkoppeltes Kommunikationskonzept zwischen den Überwachungssystemen von Infineon Technologies erfunden. Es erlaubt Datenübertragungen zwischen diesen Überwachungssystemen welche auf gestaffelten lokalen Versorgungen hängen. Der Zweck dieser Masterarbeit ist es, die Funktionalität des Kommunikationstestchips im Standard CMOS Logik Prozess zu verifizieren und zu optimieren.

Schlüsselwörter: BMS, Automobil, Isoliertes Kommunikationssystem, EMV

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Contents

Chapter 1

Motivation

Today's development of the electronics industry is progressing very fast. Thus, since the last century not only mobile phones and computers have changed and progressed significantly, but also the larger counterparts in the automotive industry. Mechanical work become steadily replaced by electronics. And much electronics also requires more monitoring systems to cover all the safety aspects. Especially when it comes to the electric car, the steady monitoring of the traction battery is mandatory so as not to be exposed to unnecessary danger of improper handling. The traction battery is available in a variety of shapes, styles and arrangements, but to reach its 200V - 400V, it has to be stacked, which means that every module and not just the entire battery has to be monitored. And to monitor these monitoring units on each module or cell, it is logical that this existing voltage is used to supply the BMS. Since these BMS modules now have to communicate with each other, a galvanically separated communication path must be created, as is already possible with the isolated CAN. For cost reasons, an Infineon own concept is presented. The goal of this thesis is to analyze a communication testchip in standard CMOS logic which handles this galvanically separated communication way.

Furthermore this environment belongs to electro mobility whose requirements should fulfill the "Radio disturbance characteristics for the protection of receivers used on board vehicles, boats, and on devices - Limits and methods of measurement (CISPR 25)" [1] and the International Electrotechnical Commission (IEC) [2] respectively. These standards are describing the limits of Electromagnetic Interferences (EMIs) and Electromagnetic Emissions (EMEs) and its methods to reduce or make the Device Under Test (DUT) less susceptible against EMI. Especially the CISPR 25 is important for electromagnetic investigations and will be taken into account for this environment.

Chapter 2

Fundamentals

2.1 Battery Management System

Mobility is one the the biggest challenges in the future. To overcome issues due to finite fossil fuels a lot of research for alternatives is necessary. The use of electrical motors is already common for Electrical Vehicles (EVs) these days, but the focus of research lies still on the greatest weakness, the traction battery. Lithium Ionen (Li-Ion) cells are used as they are today's state of the art energy storage with appropriate security, capacity and energy density for EVs.

To drive the electrical motor many of these cells are used and as they are not exactly identical the use of a battery management system (BMS) is required to control the behavior of the cells. Parameters like voltage, current and temperature of each cell are permanently monitored, so the BMS uses following sensors for the required information for secure fuel gauging:

- Cell Voltage Sensing
- Current Sensing
- Temperature Sensing
- Humidity Detection
- Strain Gauge

Especially for Li-Ion with its big advantage of energy density there is the disadvantage of hazardous damage and injury if the temperatures or voltages of the cells of the battery pack are out of range of the specified values. BMSs are used to control the external battery parameters because they have enormous influence on the performance the usage and the life time of the battery cell [3]. Indicator of the operating conditions of a battery system are the State of Charge (SOC) and State of Health (SOH). Decisions made by the BMS are regulated by these indicators to

improve the safety and longevity. Accurate measurements are therefore necessary to get good estimations of the SOC and SOH [4].

The challenge in electro mobility is to provide a power supply that uses battery cells in parallel to enable sufficient capacity and battery cells in series to reach the necessary operating voltage to drive the motor. Many cells are used for driving the EVs which makes the whole system more probable to fail. The more cells used, the greater the opportunities to fail and the worse the reliability. That is why cell balancing is used. For the parallel stack cells are self balancing since the parallel connection holds all the cells at the same voltage. Problems may occur if there is a short circuit in one single cell which will exacerbating the problem by discharging all other cells and it may become dangerous.

2.1.1 Battery Management System Architectures

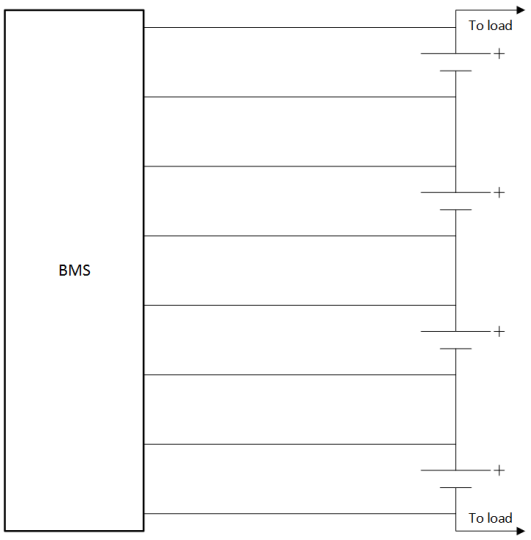

Figure 2.1: Monolithic battery management system

It is task of the BMS to verify each single cell and determine all parameters that makes the whole system work reliable. The degree of modularity which is made for BMS development varies. So there are several different architectures how to implement this system.

The simplest solution are the ”Monolithic” systems (Figure 2.1). It just consists of one BMS which is doing all the work with sensing and measuring the single

cells on battery systems. So the whole management functionality is placed into one BMS-module. This architecture offers for large format battery strings just the required features for providing the lowest cost and complexity at the expense of flexibility and scalability.

The semi-distributed architecture (Figure 2.2) uses already the advantage of a smaller number of sensing circuits which are not integrated into the actual BMS. It is better scalable and expandable, also for larger battery strings. While the BMS-Master does the management and evaluation, the single sensing modules are responsible for a higher amount of cells and for the transfer of the information back to the master. These slave modules operate together with a high-voltage measurement. They have an isolated communication interface to the master module to handle the huge voltage difference between the modules.

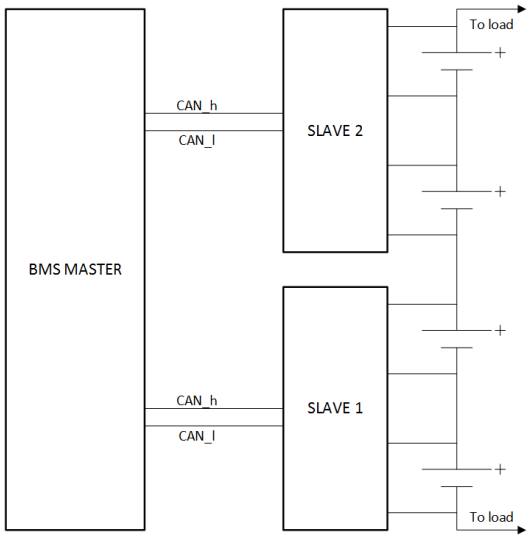

Figure 2.2: Semi-distributed battery management system

Distributed systems work with cell satellites as a separated measurement system with the functionality to communicate with the master device. In this master and slave architecture the master is mostly called the battery control unit (BCU). The cell satellites - the slave modules - are connected to battery cells or modules and are just responsible for the measurement of cell voltages and temperatures and reporting this information to the master device. If it is about accuracy, the distributed architecture is the best choice. But the protocol for communication is not as simple as for the previous architectures and there are also a lot more communication circuits and electromagnetic compatibility (EMC) and electrostatic

discharge (ESD) structures and hence more silicon area is necessary. It is mostly designed as ring topology to have the shortest way for communication from cell to cell and hence a better redundancy. Figure 2.3 shows such a distributed BMS in ring topology. The distributed architecture is the architecture which is leading to the highest costs and also increase of weight, size and parasitic power consumption at the expense of a high degree of modularity and integration [5].

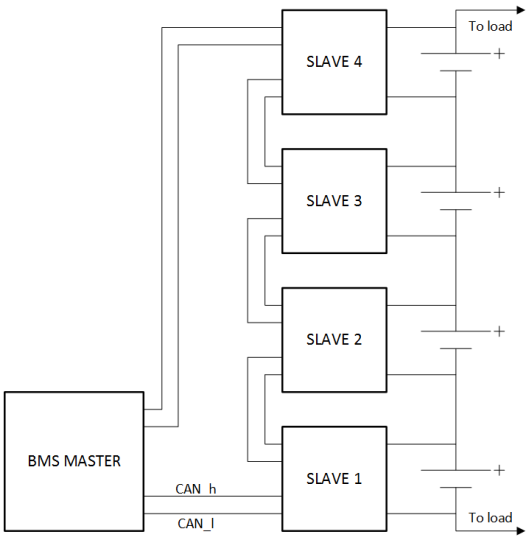

Figure 2.3: Distributed battery management system

2.1.2 Communication Protocols

To design a BMS means also to decide a suitable communication link between these systems. Mostly a serial link is used to communicate between master and slave devices within the battery pack. Serial communication interfaces have the advantage in smaller number of required wires, higher data rates and robustness against message loss. There is a short overview of commonly used serial communication protocols [5]:

I2C/SPI

I^2C and SPI protocols have been developed for communication between Integrated Circuits (ICs) which are located on the same Printed Circuit Board (PCB) and

it is not recommended to use them for communication between different PCBs. Especially for communication between battery monitoring ICs it may be possible to use a "level-shifted" version of these SPI or I^2C communication buses. But with respect to robust communication design this might be the wrong solution as long as there are no isolation components between the monitoring ICs.

RS-232/RS-485

BMS in automotive sector have to be robust, especially the communication line. RS-232 is the worst choice for this demand as it is serial, but single-ended. So it is very susceptible for incoming interferences. Generally these protocol was developed for point-to-point communication and is not recommended for use in a star- or ring topology. That's why even the advantage of differential signaling of the RS-485 and hence the robustness against emissions is no good choice for the usage as communication type for BMS.

Local Interconnect Network (LIN)

The LIN protocol was developed for the usage in automotive applications with all the advantages what other serial protocols can't offer. It is cheap and has high robustness which make it really attractive for BMS applications. At least it is potentially possible to use it but it just offers a limited data rate of up to $19.2kBit/s$, what makes it unattractive for high quality and functional safety BMS applications.

Controller Area Network (CAN)

The CAN protocol offers nearly all advantages for the automotive industry. It provides high data rates and hence near-real time performance for many types of signals and also offers high robustness against EMI. It is mainly used for the automotive sector as it fulfills these requirements, but even for BMSs it becomes difficult with this kind of protocol as it not supports communication between two communication units which are working in different level-shifted supply domains. More informations about the CAN bus are described in chapter 3.1.

Flexray

Even more reliable and faster than the CAN bus is the Flexray communication bus. This bus was just developed recently and is responsible for current high-end challenges for in-vehicle-networks if it comes to really high reliability and safety, like Drive-by-Wire or Steer-by-Wire applications where also high data rates are necessary. In contrary to LIN and CAN this bus is even more cost intensive.

2.1.3 Communication Types

Based on the general requirements of the BMS interface several methods for physical communication between BMSs was investigated and are briefly shown.

- Conducted communication method
- Capacitive coupled communication method
- Power Line Communication (PLC)
- Wireless
- Optical Communication

Conducted communication method / Twisted Pair

The simplest form of communication type would be the conducted physical one (Figure 3.2). Therefore a communication interface was developed by Infineon Technologies which fulfills automobile as well as stationary requirements with communication concepts up to 100 BMS modules. It is based on a ring topology which makes it possible to transfer data clockwise or counter clockwise and brings also the advantage of redundancy of the data sent by one BMS slave module which allows the module to transfer the data in opposite direction in case of line break. For functional safety reasons such line breaks can be immediately detected due to the ring structure. Point-to-point topologies would not be able to work properly anymore in such a case. The concept of this communication method brings several advantages. As communication medium just a twisted pair cable is necessary and the special feature is the galvanic isolation between the interfaces by means of capacitor or transformer. External components like capacitors and resistors are directly located at the pins of the IC and are not worth mentioning for cost reasons. As already mentioned this bus is working with capacitive and inductive coupling depending on the length of the wire. For longer connections it is more suitable to use inductances instead of capacitors. The data rate is with 2 Mbit/s

high enough to fulfill the general requirements. Wakeup- and sleep functionality is also included so the interface uses just power in case of transmitting and receiving data. This method is described in more detail in chapter 3.

Capacitive coupled communication method

In contrast to the previously mentioned method this capacitive coupled structure is not using any kind of conductor like twisted pair cable between the interfaces. The only medium between the conductive area on the cell as electrode and the other conductive rails is air and a dielectric layer for the required isolation. This possible arrangement is shown in Figure 2.4 and was in this kind of form invented by Fraunhofer [6]. The electrodes on the cell build up a capacitor with the area of the rails which is part of the bus and connects the master BMS with the single cell ICs in parallel. To improve the robustness of signal transmission a differential realization is used. The BMS architecture is a distributed one, what was already mentioned in the introduction in chapter 2.1.1. Every cell uses a battery monitoring unit (BMU), so that unit which is responsible for a single cell has to consist of an own interface for receiving and transmitting. But measurements are hence very accurate because sensing wires haven't got a long way to the supply pins of the cells.

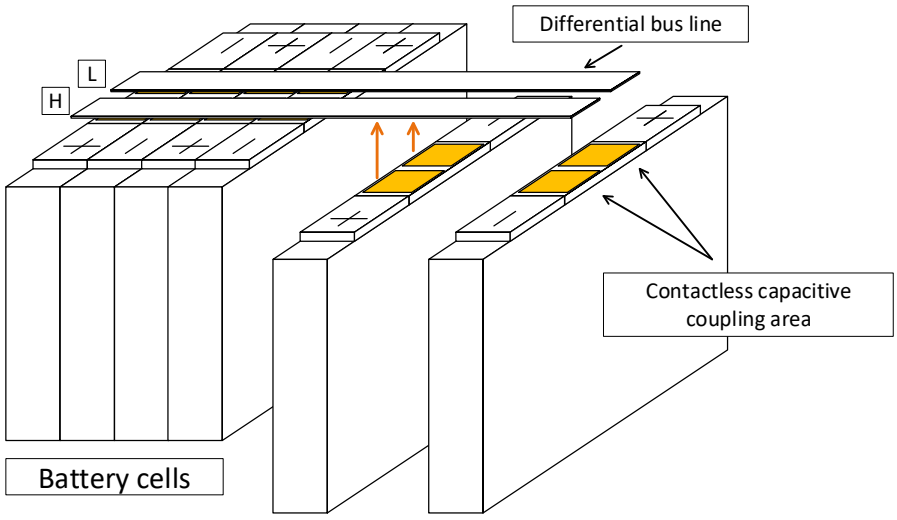

Figure 2.4: Communication concept based on capacitive coupled differential bus rail

The advantage of this kind of communication method is the barely used number

of wires and hence cost reduction due to non-existent connectors. Only a flat conducted bus is necessary which comes with challenges as this bus has to build up a sufficiently high capacity to every cell electrode and diagnostic functions are very important to get information about a lost connection. Another important advantage is the omission of susceptible plug contacts which are the main reason for incoming interferences through that path. Additionally if there is a failure of one ore more monitoring ICs the communication with the other ICs does not stop working as the bus is connected with every unit.

A similar capacitive coupled communication method was also introduced in the context of Infineon Technologies and works in series (Figure 2.5). A flexprint PCB was made (Figure2.6) which fulfills the specifications of flexible conductive wings on both sides with predefined area to build up a capacitance with the neighboring flexprint board. The flexprint boards are located on the top of a prismatic battery cell with both wings folded down between these battery cells. With this method the electrode comes with the PCB, so flexible boards are preferred to use which pushes up the costs and brings restrictions with the PCB design in comparison with commonly used PCBs. Functionality is illustrated in Figure 2.7. As can be seen in this schematic this is just a single wire interface and hence more susceptible to noise and parasitic effects. Higher data rates might be possible but in case of high parasitics from the circuit board to the battery cell the communication behavior of this capacitive coupled method was limited. A more detailed explanation can be found in another report [7].

Power Line Communication

This concept uses directly the noisy High Voltage (HV) DC powerline to reach every member stacked over a wide range of battery cells. To accomplish that the data have to become overlaid by a high frequency modulated carrier by Frequency Shift Keying (FSK) or Amplitude Shift Keying (ASK). FSK means that there are 2 frequencies slightly bigger and smaller than the carrier frequency which are used for logical ”1” and logical ”0” and ASK has the difference between the logic levels in its amplitude. It’s a very challenging way to get a BMS working with this kind of communication because the HV path of the battery stack is within a very noisy environment due to the high frequency switching noises of the power switches between source and motor and all the inductive loads as well as the whole noise generation by the engine [8]. The carrier frequency has to be chosen carefully to not get communication troubles by interlocking couplings by the switching noise. Band-stop filters are eventually used to filter out that noise frequencies, so to avoid

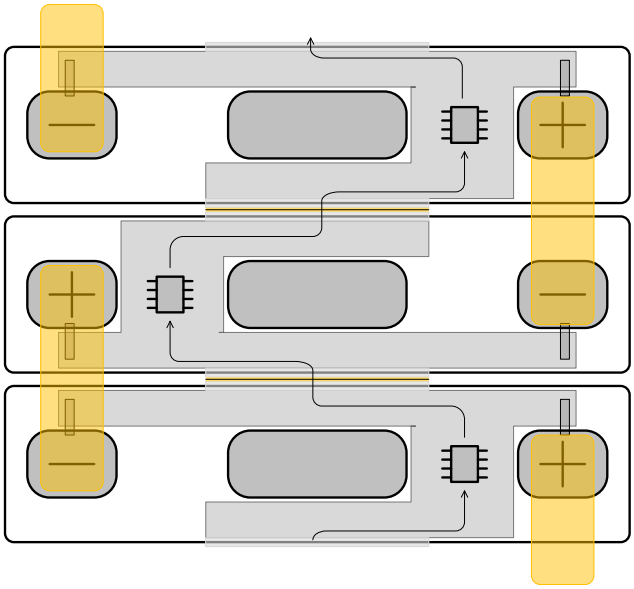

Figure 2.5: Communication concept based on capacitive coupled flexible PCB area

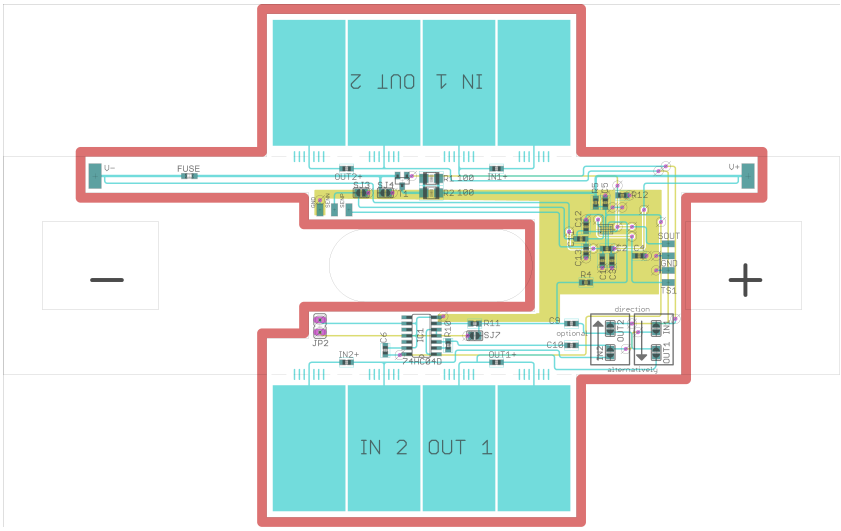

Figure 2.6: Flexible PCB monitoring unit

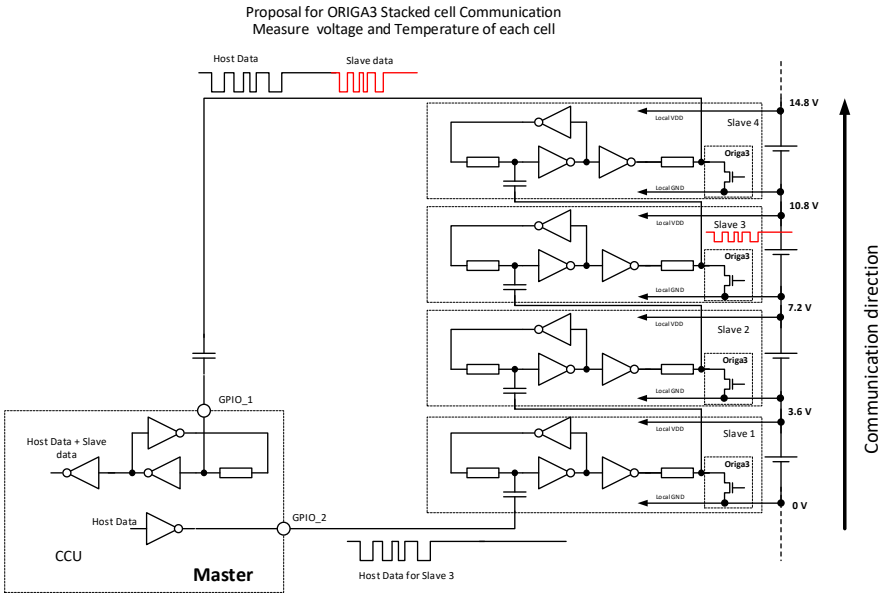

Figure 2.7: Capacitive bus holder circuit concept

a powerline path with high signal attenuation these frequencies should not be chosen as modulation carrier. The advantages for the PLC method are clear, there is less wire harness in comparison with the conducted communication methods. The data rate is directly coupled to the carrier frequency of the modulation which plays an important role in case of the high amount of inductances in the powerline and which leads to higher signal attenuation with higher frequency. PLC in BMS is a great opportunity to get rid of communication cables but is in contrary to the wireless solution associated with much more effort.

Wireless

The approach of radio based communication methods comes from Fraunhofer Institut ISB. Each cell is equipped with at least a transmitter. Dependent of the communication scheme the cell can also be equipped with a transceiver which allows bidirectional communication between the monitoring IC and the BMS. There are 3 approaches how wireless communication methods can be set up for different kinds of applications:

Unidirectional communication is for low cost applications e.g. BMS for starter batteries in non-electric vehicles. Only a transmitter is used for the battery cell,

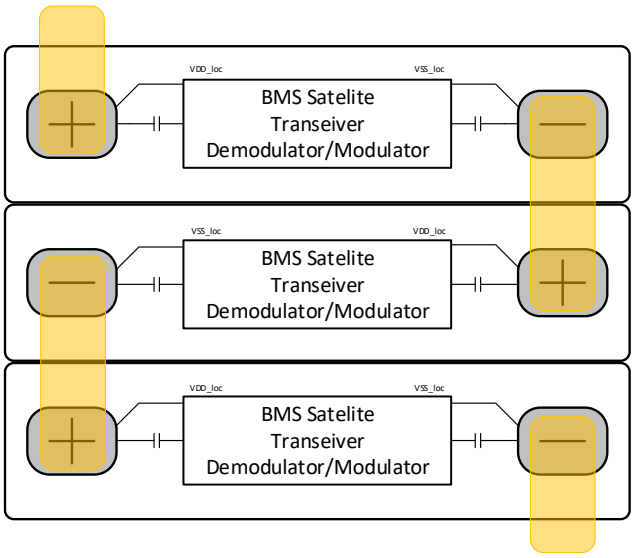

Figure 2.8: Communication concept by Powerline

so only communication in one direction from the BMS to the cell is possible. Power consumption is higher because the monitoring unit on the cell can't receive power down commands, so it is powered up all the time. To save energy due to the missing channel from the BMS to the cells, the sampling rate of the voltage measurement adapts to the voltage change.

Bidirectional communication with active transponder uses on every cell only active transponder which allows synchronous voltage measurement but is very power consumption and cost extensive.

Bidirectional communication with active and passive transponder using the passive transponder (e.g. RFID) to wake up the monitoring unit from an energy-saving sleep mode, as the passive transponder takes his energy from the incoming wake command. For communication between BMS and the cells and vice versa the active transponder will be used.

The advantages of a wireless method is a totally galvanically separation between BMS and cells which is the main factor of challenges with the other approaches. On the other hand the usage of radio based communication within the battery system is very challenging due to metallic components located around the system and their cause of reflections. Orientation and correct placing as well as design of the antennas need an increased amount of effort.

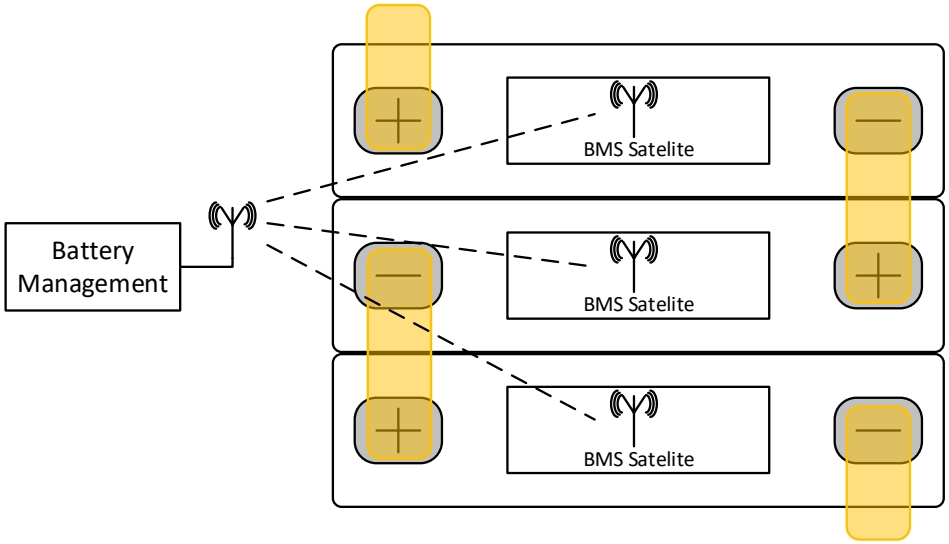

Figure 2.9: Communication concept with wireless transceiver

Optical communication method

There is another wired method for communication which is actually completely galvanically separated between BMS and cell. For this approach an optical fiber is necessary as medium for unidirectional communication between receiver and transmitter. Additionally external components like the transmitting and receiving diodes have to be used to transmit the data by infrared light. Infrared light is used, because the attenuation of fiber is much less at the wavelength of infrared light than for visual light, which has a shorter wavelength. Such a diode only can be used for transmission or receiving, not both at the same time. For bidirectional communication there has to be a second implementation of optical fiber with all its external components.

Using an optical way to transfer data is very EMC robust. The fiber wires are not able to act like antennas and TX and RX side using an optical source and optical detector so there is no entry path for interferences or field couplings. Even though this method is EMC robust this is not the case for the mechanical robustness of the optical fiber and aging of the infrared emitters.

2.2 Introduction to Electromagnetic Compatibility (EMC)

There is a brief introduction to get elementary knowledge about electromagnetism and its interferences and how to prevent it. It is generally known that since the time of radio and telegraph communications electromagnetic waves are used for the information transport over a wide distance. Such transceivers uses carrier frequencies which carries the information by an overlapped signal. In an ideal way this carrier frequency has a peak at exactly one point. As it comes to a real world system these operation frequencies are shaped with harmonics and other distortions. So in the frequency spectrum a wider range of frequencies are present. Electromagnetic compatibility (EMC) is a design technique which handles electrical and electronic systems to be compatible with disturbing incoming interferences and to accomplish a state of immunity. Electrical and electronic systems should be able to be susceptible to incoming interferences, as also should have less outgoing interferences which could cause incorrect function to another electrical and electronic system.

Paul [9] writes in his book, that a system is electromagnetically compatible with its environment if it satisfies three criteria:

1. It does not cause interference with other systems.
2. It is not susceptible to emissions from other systems.
3. It does not cause interference with itself.

Important keywords for this topic are also the **aggressor**, which is generally seen as the generator of the EMI and therefore also the source of EME. The **receptor** on the other hand, or also called the victim, is the counterpart of the aggressor. Actually all electrical or electronic systems can be receptors of EMI if they are not well enough protected or not robust enough against it.

Even if there is no possibility to turn off interferences, EMC designers have to find a way to suppress them as much as possible.

The source of interferences comes primarily from switching between two stages. That is why digital circuits are mostly affected as well as oscillator circuits, which are causing permanently interferences due ot their clocking. Fast rise- and fall times of the clock are the primary contributor to the high-frequency spectral content of these signals. To keep emissions low means in this case to make switching times slowlier.

Common Reference Ground and Crosstalk

To mention here at this point is the importance of a well designed ground. Noise reduction for electronic systems starts here. The larger and the faster the system with higher frequency or shorter rising times is, the more important it is to have a stable signal ground. Even low frequency and DC systems normally are requiring a well designed ground for an optimal performance. In 1979 Ott [10] already wrote with the sentence "The equipotential concept, defines what a ground "ideally" should be, while the current concept, defines what a ground actually is" about its importance. Especially if it comes to topics around EMC it is a big mistake thinking of ground as being a simple conductor with an equipotential surface with all points on it with same voltage level. It is all about the impedance in which the current flow is present.

The influence of an interfering current is shown in Figure 2.10. If more than one circuit is using the same ground plane as returning path, then there is an influence of circuit 1 from circuit 2. Following equations are shown to understand this ground problem.

$$R_L = \frac{V_S - V_G}{I_1} \tag{2.1}$$

Thinking of the ground as a small impedance, then the voltage over the load is mentioned in equation 2.1. Is the same returning path is also used by another circuit - in this case this is a noise current I_N coming from somewhere - then this noise current is inducing a noise voltage on the ground's finite impedance, which also affects the load with following equation:

$$V_N = I_N Z_G \tag{2.2}$$

$$V_G = (I_N + I_1) Z_G \tag{2.3}$$

$$R_L = \frac{V_S - (I_N + I_1) Z_G}{I_1} \tag{2.4}$$

This problem is generally described as the **galvanic coupling**. Therefore circuits have to be well designed and ground paths have to be designed in star topology, so the ground impedances of susceptible circuits are separated with circuits which acts as aggressor.

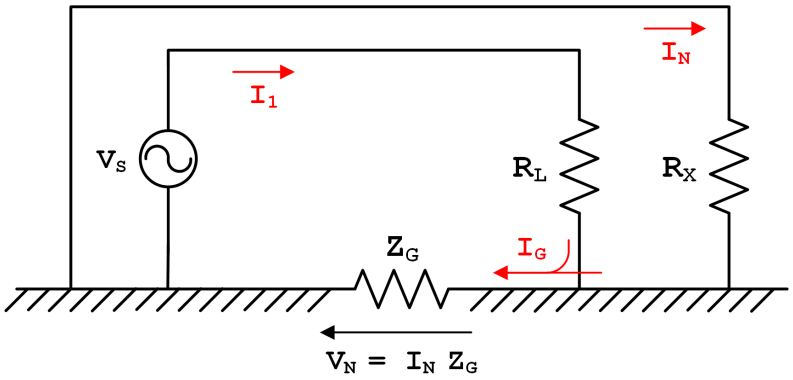

Figure 2.10: Single Conductor above ground plane [10]

Another kind of crosstalk is the **capacitive**, the **inductive** and the **far field coupling**. Capacitive and inductive coupling and how noise can affect a circuit is shown together in Figure 2.11. First of all there is a circuit with a source and a load. If the length of the wire in that circuit is really long, then capacitive parasitics C_{1x} will result between this wire of that circuit and another aggressor circuit with an voltage noise source u_{CN}. Such an electric field coupling can be modeled as a current generator connected between the susceptible receptor circuit and ground. It's magnitude in frequency domain is then

$$I_{CN} = \mathrm{j}\omega C_{1x} V_{CN} \tag{2.5}$$

which is in time domain

$$i_{CN} = C_{1x} \frac{dv_{CN}}{dt} \tag{2.6}$$

The capacity can easily be modeled (2.7) by the area A in parallel, the distance d from these parallel plates and its medium ϵ between. The area is calculated with length L and width W of the conductor from the main circuit and the conductor of the aggressor circuit.

$$C = \epsilon_0 \epsilon_r \frac{A}{d} \tag{2.7}$$

If the area of this circuit is assumed really big and there is another aggressor loop nearby, then both loops are connected by the magnetic flux Φ which is

proportional to the current. The voltage V_{LN} is induced in the susceptible circuit due to a magnetic field with a magnitude of

$$V_{LN} = \mathrm{j}\omega M I_{LN} \tag{2.8}$$

which is in the time domain

$$v_{LN} = M \frac{di_{LN}}{dt} \tag{2.9}$$

with the mutual inductance

$$M = \frac{\Phi}{I} \tag{2.10}$$

The mutual inductance in this case is the magnetic flux in the susceptible circuit with the current from the aggressor circuit.

Back to the circuit in Figure 2.11 the load of the receptor circuit has a different voltage U_{RL} due to the influences of the aggressor (2.11). The frequency domain is shown in equation 2.12.

$$U_{RL} = (I_1 + i_{CN})R_L - v_{LN} \tag{2.11}$$

$$U_{RL} = I_1 R_L + \mathrm{j}\omega(C_{1x} R_L V_{CN} - M I_{LN}) \tag{2.12}$$

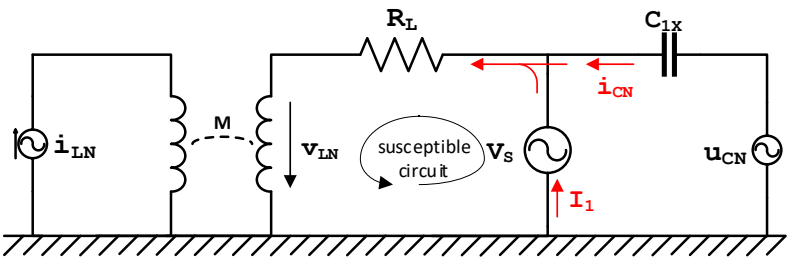

Figure 2.11: Capacitive and inductive coupling in 1 circuit

Differential vs. Single ended

Single-ended signals which are affected by electromagnetic interferences have to expect huge consequences. There is not only no damping effect of the interferences but also an amplification of these interferences. So there is no chance anymore for successful amplification and rebuilding of the input signal. The left side of figure 2.12 shows an input and output signal which is affected by the switching of a digital clock signal. Ground bounce noise from the switching gets induced to the common source stage amplifier and influences the analog signals if they share the same reference ground. The peaks which are shown on the input signal VIN are therefore amplified through this amplifier too and resulting to a way higher peak as shown on the output signal $VOUT$.

The right side of this figure shows in comparison to the left figure a differential pair which is affected by the same clocking as well. This differential pair consists of two common source stages which senses in this case only differential signals at its input while rejecting changes in its common-mode input. So the result of amplification (A) is zero for common mode signals if there is no differential change between the two input signals $VIN1$ and $VIN2$ in respect to time (2.13).

$$\frac{d(Vx - Vy)}{dt} = \frac{\Delta V_{INdiff}}{\Delta t} = 0 \qquad \rightarrow \qquad A = 0 \tag{2.13}$$

The ground bounce interference coming from the clock and influence the reference ground of this circuit happens simultaneously and affect the whole circuit same. The voltage levels on Vx and Vy are overlaid by these interferences now, but it comes from the same reference and does not have any differential changes in time, which means it is not amplified. The result is a clean output signal $VOUT$ which is not affected by any common mode interferences coming through crosstalk and is ready now for further processes.

Some additionally points may be important. Noises like thermal noise, shot noise or the so-called 1/f noise which are not coming from crosstalk are getting still amplified to the output signal because this is a random noise which have no special tendency together.

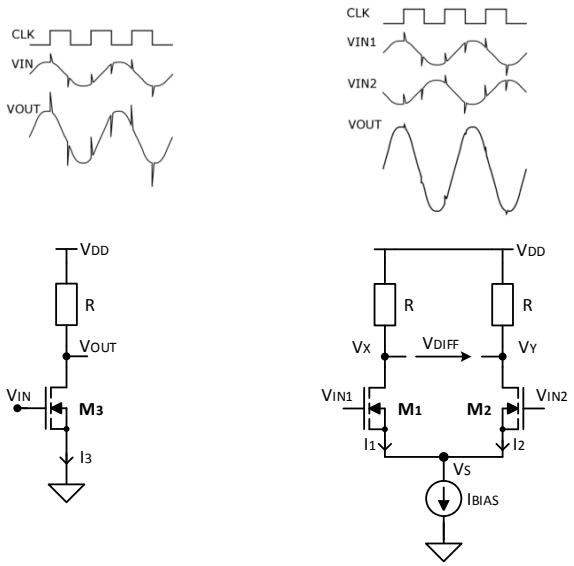

Figure 2.12: Differential Signals with common mode disturbance rejection [11]

Chapter 3

Intercell Communication Interface

3.1 Overview

State of the art communication bus for automotive usage is the CAN bus, which connects all periphery together inside vehicles. Voltage supplies like the traction battery to drive the electrical motor consist of stacked battery cells to reach a higher operating voltage. But every single of these cells should get monitored to get its informations like voltage, current and temperatures for functional safety reasons and general informations about its SOC. All these informations have to take a communication way in direction to the central unit. The state of the art CAN bus can't be used in that case, because the monitoring units on each cell are supplied by that cells, so they are not in the same voltage domain and can't communicate anymore due to its galvanic connection between the transceivers. A galvanically isolated communication bus and interface has to be used in this case, so the isolated CAN was introduced. It uses additional to the CAN controller an isolated CAN module on each side of the interface which galvanically separates two units and makes it possible to communicate again over a wide range of stacked battery modules. The disadvantage of this ISO-CAN is the cost and area intensive method of construction. Every side of the communication interface has to use an additional IC to separate the supplies.

The connectivity between the introduced BMS is build up with the Intercell Communication (ICC) Interface, which acts as connection between all the BMS modules. This interface and its bus is generally designed by Infineon Technologies. The main advantage of it is the galvanic separation between the modules and hence the independence of any expensive connector modules or transformers to separate the supply of the stacked BMS modules and hence a cost and area reduction for the customer.

The BMS modules consist of one Master (MA) device and a row of Slave (SL) devices, which are connected together in a Daisy Chain topology. Informations are transmittable over a differential signal between the interfaces of the modules. A differential bus is used to reduce effects of external noise, so the need of expensive shielding is not necessary. For the communication path a twisted pair cable is used. Necessary external component additionally to the BMS IC is a capacitive coupling path directly after the differential interface pins. The communication system is half duplex. That means communication is possible in both directions, but not simultaneously. Only one direction is allowed at the same time. Speaking and listening of those BMS modules are possible with predefined commands. With the start command for measurements all SLs have the task to start their measurements in the BMU. This includes accurate voltage and current measurement to get the SOC and an exact temperature of the batteries to get aging information and the SOH to fulfill all diagnostic information of the whole system. All this informations are necessary for safe operations of the BMS and its batteries. After all measurements are finished the transmission from a SL addressed by the MA will occur. So the MA receives the whole information about the SL modules successively and the evaluation process occurs.

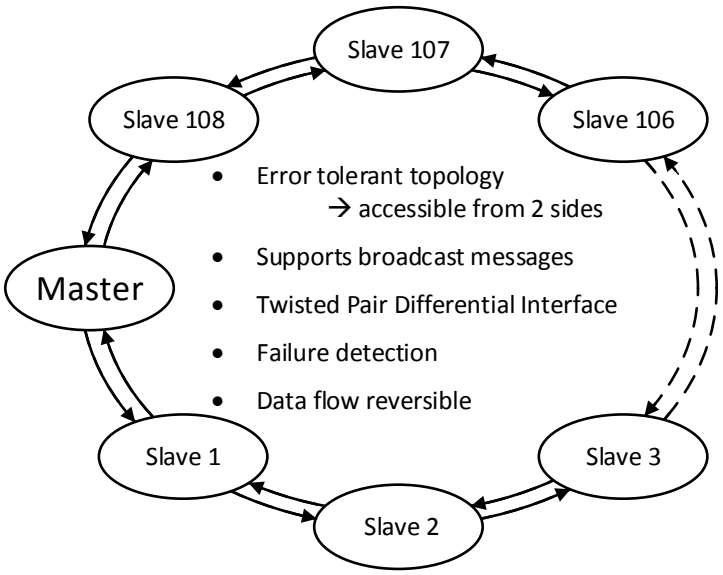

Figure 3.1: Master-Slave principle with both-way communication

A basic Master-Slave chain is shown in figure 3.1. It shows the MA module connected with its SLs as a distributed BMS looks like. The interface is designed

to keep errors over a raising number of SLs small. This is possible with a buffering and transmitting of the received data after every SL. Thus it would be able to include countless SLs into the chain without loss of data. A traction vehicle battery should reach a voltage of around 380V to finally drive the electric motor. That requires a total of at least 108 BMS modules per cell supply voltage of nominal 3.6V in series. Another advantage is the use of this Master-Slave principle as chain, so every SL is accessible from both sides, which improves the redundancy and make communication to every SL still possible, even if there is a failure of one SL. Important is only to separate the master device with the slaves by transformers. So a total of 2 transformers are necessary, otherwise the master device will see the whole stacked traction supply voltage. Redundancy is essential to inform the driver in case of a failure in the communication lines or the interfaces. In such a case, if there is a failure of communication line or the interfaces, the Microcontroller (μC) should still be able to communicate with the rest of the BMSs and should be able to reach all BMUs. Higher redundancy makes it possible to achieve a safer system.

Broadcast messages are supported, which means there is only one command from the MA to reach and go through all the SLs and thus save time and keeps the power consumption lower because there is just one command instead of commands of the number of SLs.

Figure 3.2 shows such a BMS how it looks like in a daisy chain ring topology. A μC handles all commands and the MA transceiver transfers all informations around the circle so that every SL BMU module receives these commands. The battery HV stack is including in series single cells which are connected to its BMS module and supply them. Between the master device and the HV stack is a transformer which is separating the direct current (DC) voltage levels as this battery module consists of 8 cells of around totally 32V.

Generally the most important task for the interface next to the data transmission is reliability and robustness if it comes to data transmissions between the modules and over the whole chain of modules.

If data go every time the same way around there is a kind of imbalance which may affect the interface over a long term and it may not be as reliable anymore. That happens if the master communicates from bottom or respectively from top only, then one BMU plus interface has the most working load and therefore the most power consumption because it handles more data through the ring and therefore are some interfaces consuming more power than the other ones. This is a result of imbalance due to different discharging time of the module cells which is leading

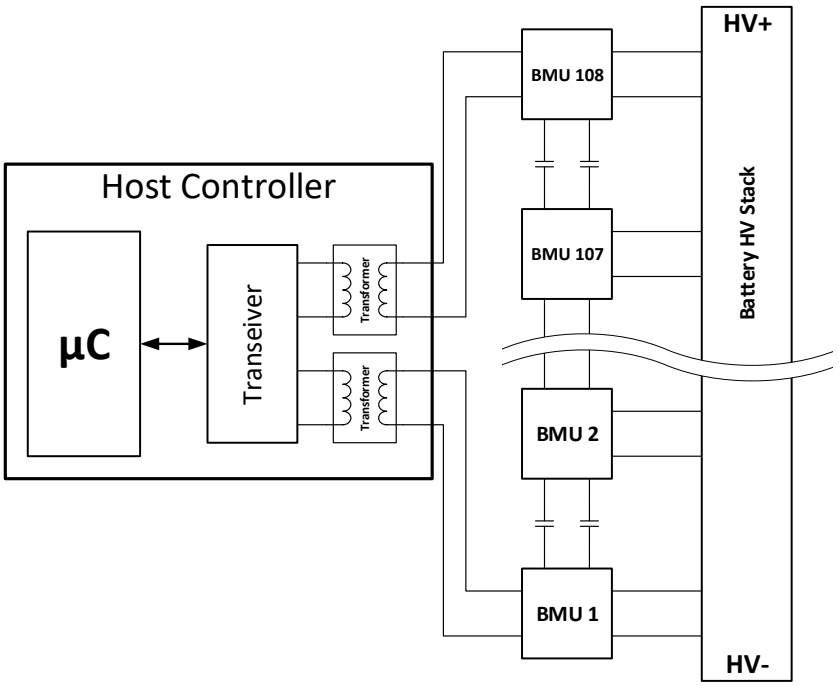

Figure 3.2: BMS ring topology

in a longer passive balancing time and overall charging time for the HV stack. The big advantage of using the BMS system in a ring topology and additional the changeable direction of the interfaces is the use of a protocol that handles the communication in both ways alternating. Every BMS transfers the collected informations about the battery cell to both directions. So every other BMS has to work the same time and is consuming the same power. The overall average power consumption is rising with this kind of protocol, but all modules become claimed equally with same power consumption and thus the passive balancing and charging is leading to a huge improvement [12]. The reliability has also be proven in case of a transmission from module to module over a certain length of communication wire including EMC interferences.

Data exchange starts with a command from the MA to start speaking with the SLs. All SL modules get this command as broadcast message to start the measurements and pause their activity after finishing the task of getting all the results out of the state of the battery cell. After that each SL is waiting for an addressed command from the MA to return the requested informations.

The duration of a whole cycle and all informations about every battery cell

depends on few factors:

- Number of BMS modules N
- Time depending on the total length of communication wires t_{wires}
- Processing of the interfaces t_{IF}
- Runtime of the BMU t_{BMU}
- WakeUp duration t_{wake}

$$Cycle = (t_{BMU} + t_{IF} + t_{wake}) \cdot N + t_{wires} \tag{3.1}$$

If the cells are still in sleep mode then the duration increases by the wakeup time of the IC. Every SL needs an own wakeup pattern, because the first wakeup for the first SL will not get transmitted so it needs time until the IC is ready for operation and after that the first SL allows to send the next pattern to the second SL. The procedure how the wakeup pattern works before communication is possible is shown in figure .2 in the Appendix chapter.

If there is a sudden short somewhere between the cells it has to be noticed soon to warn the MA about some dysfunctions or in worst case about hazardous consequences. That is why speed is really important for the communication in battery management systems.

One requirement of the BMU is to get the temperature determined by a small resolution impedance measurement what requires an exact frequency. The differential ICC bus makes it possible to send a serial sequence of synchronization stream that handles the accuracy of an oscillator in the BMU. The complete information about the measurements are therefore not just depending on the reliability as also on the accuracy of the interfaces.

In summary the interface should have following characteristics:

- *Reliability* of the whole system in case of failure
- *Robustness* against EMI independent of the number of SLs
- *Accuracy* in case of Local Oscillator (LO) trimming
- Communication over supply shift (*Isolation*)
- *Cost reduced* architecture (CAN-bus already established)

Data communication systems in BMS for automotive purpose are already established like the CAN network which is state of the art in nowadays communication systems in mobility. The CAN-bus is an universal architecture which main purpose is the connectivity of periphery. Cost reduction plays a minor role for the CAN architecture. Connectivity and cables are cost intensive and for reliability

purpose in case of redundancy they need additional connectivities what makes this binary unit system (BUS) a way more expensive. On the other hand this bus fulfills the EMC requirements in extremely harsh automotive environment.

3.2 Concept

The BMS communication IC which is used for this thesis is build up in a standard CMOS logic process c11fl. The challenge for this interface is to establish a successful connection between the modules. Unlike for other applications than BMS where the communication is really straight forward it is for this type of communication in case of a high voltage system difficult. From interface to interface there is always a voltage shift of the cell voltage which raises the common mode power potential level after each module because the modules are supplied directly by the in series connected battery cells. Since every module is actively supplied by these local cell supplies there is no common reference ground potential.

For a functional system there has to be a separation of the DC voltage levels between the interfaces. This is possible with a galvanic separation by capacitor or inductor between two adjacent cell modules. They are acting as DC blocker and allow only signals over a certain frequency to pass. As already mentioned before there is no reference ground potential, that is why a differential communication way has to be chosen for the interface primarily to close the current flow and on the other hand also to get rid of the issue of common mode disturbances.

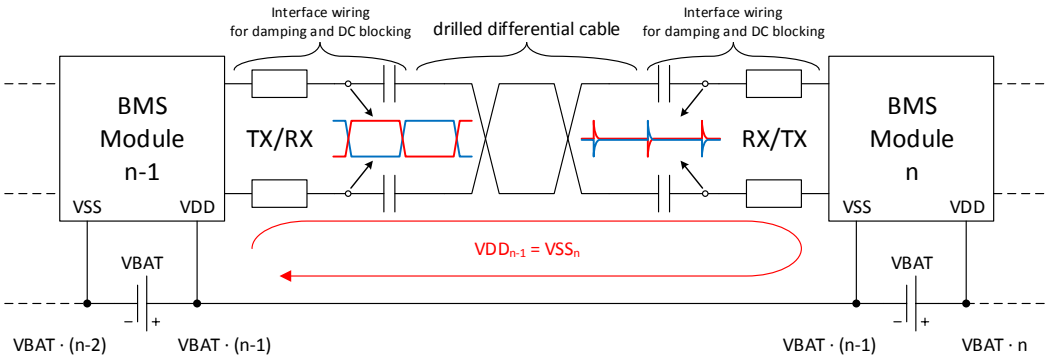

Figure 3.3: General connectivity concept

Figure 3.3 shows basically the concept of the connection between the cell modules. The Modules are supplied with the battery cell supply V_{BAT}. So the potential of

every node between the cells raises with the number of the modules. Communication without a galvanic separation of both interfaces is not possible, because the VDD supply of the receiving interface is with the difference V_{BAT} higher than the VDD of the transmitting interface. The total supply range between 2 modules is hence $2 \cdot V_{BAT}$. The first module on the left is in Transmitter Exchange (TX) mode. It is forwarding the data coming from the previous module after getting buffered. The other module on the right should be in Receiver Exchange (RX) mode for successfully processing the arriving data. Both inputs are tied to the internal supply voltage of the interface coming from a linear regulator and are low impedance. Tied to this voltage in RX mode it is possible to observe small voltage peaks depending on the arriving edges. These voltage peaks become amplified by the receiver and after that are ready for further processions.

Figure 3.4 shows the simple concept of the BMS module. The MA and the SL have the same construction. Both modules have 2 interfaces (IFs) with differential pair BUS pins and General Purpose Input/Output (GPIO) pins. The MA communicates with the μC over Universal Asynchronous Receiver Transmitter (UART) by the GPIO pins. Commands to the SL are coming generally from the μC, which handles all the communications, gives further instructions and receives the protocols with all the measuring informations. The interface of the SL is connected with the Measuring Unit (MU) by the GPIO pins, which is also a digital part. The MU is waiting until commands arriving to start the measurements. The GPIO pins are important for feeding the interface with data, which are changed there from single ended to differential. And the direction pins DIR_N and DIR_S changes the direction of data transfer between RX and TX.

The interface block of every module consists of 2 interfaces as already mentioned before. The IF on the top is called "IF North" with its differential pairs of IFN_L and IFN_H. The one at the bottom is the complementary one and is called "IF South".

A more detailed view of the half part of the whole IF block we can see at figure 3.5. The "X" in "IFX" stands for either North or South. What is striking out is the Interface Control Unit (ICU) as also the Wake Up block directly after the differential pair input. The ICU controls the direction of the Transeiver (TRX) and the data flow and prepares the output levels for communicating with digital levels. The direction input DIR_X is just an enable/disable for the TX block and vice versa with the RX block. The BMS module is also able to go to sleep-mode and reduces its power consumption, and on the other hand to wake up again, if there is a detection of new data. Is this the case, the wake up block gives an enable for

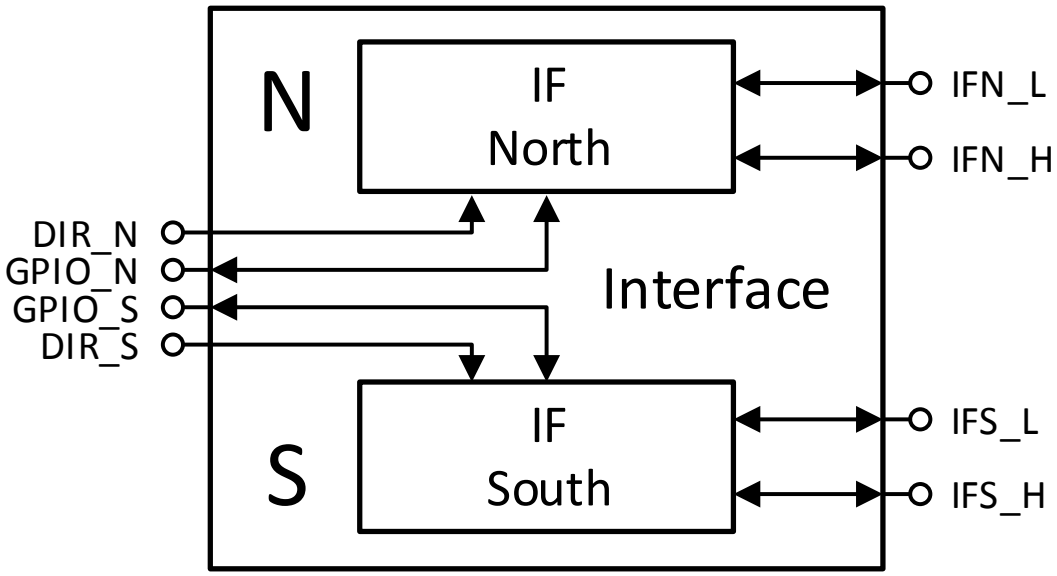

Figure 3.4: Interface Block Diagram

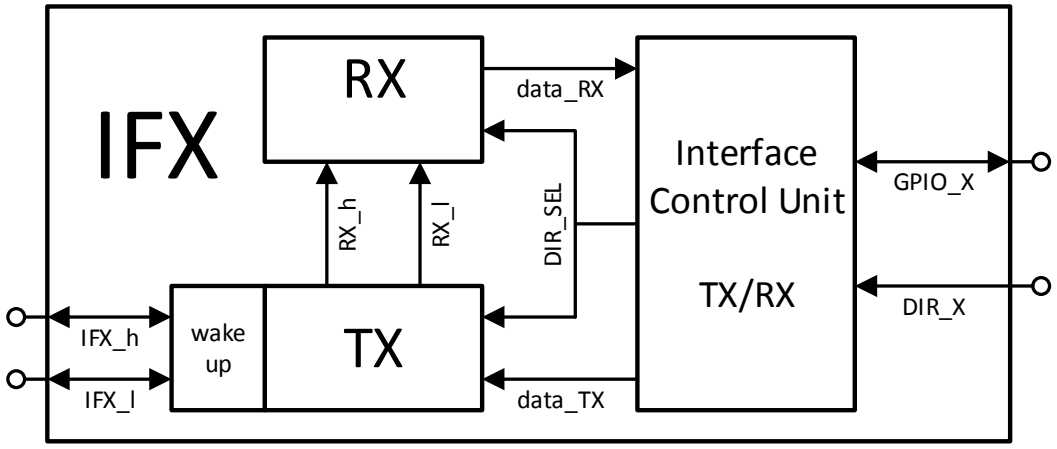

Figure 3.5: Detailed Interface Block Diagram

the internal power regulator that supplies the interfaces and after the start-up time and some clock cycles the IF is ready to process the data.

The TRX consists of 2 blocks, the transmitting part is the TX block and the receiving part is the RX block. The direction given from the ICU is by default in RX mode. Receiving commands are going through the "wake up" and TX stage to the receiver. Differential to single ended conversion happens there and the ICU receives this command and transfers it further to the BMU. In contrast for transmitting commands the ICU will change the directions for the transceiver which disables the RX and enables the driver of the TX.

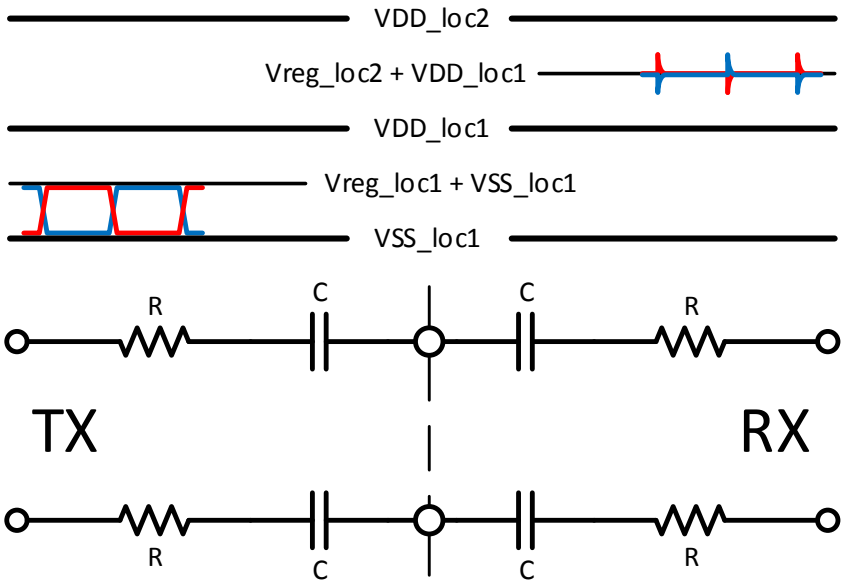

Figure 3.6: Communication Bus

The external wiring between two BMS modules for communication is predefined with a serial RC network (Figure 3.6). This capacitive coupled structure separates the two different DC voltage levels on each end. The voltage at the RX side is low impedance clamped to the $Vreg_{loc2}$ voltage above $VSS_{loc2} = VDD_{loc1}$. Due to different voltage levels the capacitors are already charged. It comes to charge redistribution if there is a change of the input signal what is leading to the upwards and downwards spikes seen on the RX side of Figure 3.6 in the voltage diagram. The discharge duration of these voltage spikes are depending on the RC time constant. Even if the voltage on receivers side is clamped to its local regulated voltage, the differential current behavior at the input can become amplified and the signal over the bus reconstructed. Common mode disturbances coming from

the transmitter or through capacitive or inductive coupling have no chance to make an imbalance. Each of the RC networks is on an own BMS on each side of the interface and after the RC network the modules are connected with a differential cable which is twisted pair to reduce capacitive coupling effects and inductive loop antennas for smaller impact of external interferences.

3.2.1 Power Management Unit PMU

To make a short summary about the Power Management Unit (PMU) used for the communication IC there is a block diagram with the most important components in figure 3.7. For limitation of the whole-over power consumption this IC is operating in sleep mode if there is no wake-up command coming from the interface. The IC is permanently connected with the cell voltage **Vbat** and generates with a low power supply voltage called **vSleep** in the ″generate Vsleep″ block.

The ″PMU Control″ block is already presupplied with the battery voltage and consists only with couple of combinatoric circuits and an RS-flipflop waiting for the incoming ″wake_Vsleep″ to enable the ″Start-Up″ and the ″Low Dropout (LDO) Regulator″. As the name of the incoming enable signal already shows this signal is originally coming from the ″Vsleep″ supply. The ″PMU Control″ unit only resets the whole IC again with incoming ″Auto_PD″ signal from the ″Goto PowerDown″ block. The enable from the control unit is a ″PD″ logical ″0″ that turns on the ″Start-Up″ circuit to generate a temporarily inaccurate **v2v0** which can offer just one fifth of the current in comparison to the LDO-regulator. But this start-up voltage is necessary for the ″PMU Reference″ to generate the bandgap voltage ″Vreg_1V2″ that is necessary to accurately generate the real accurate **v2v0** from the ″LDO Regulator″ block. As soon as the bandgap voltage is available will the **Nreset** from the ″PMU Reference″ will set to logical ″1″ after a short delay what will show that the IC could start up correctly.

Nreset activates the ″Goto PowerDown″ block which can turn off the PMU from now on if there is no data anymore coming from the **Data_IO** pin. The ″Goto PowerDown″ block did originally have an own pin for only adding an external capacitance and hence adding a time constant for external changing the time by this capacitance after which a PowerDown should occur. Incoming data from **Data_IO** and the **wake_Vsleep** keep the external capacitance charged. Is the voltage of the capacitance falling under a threshold of an n-channel metal-oxide-semiconductor (NMOS) then the ″Auto_PD″ will occur and will turn off the PMU

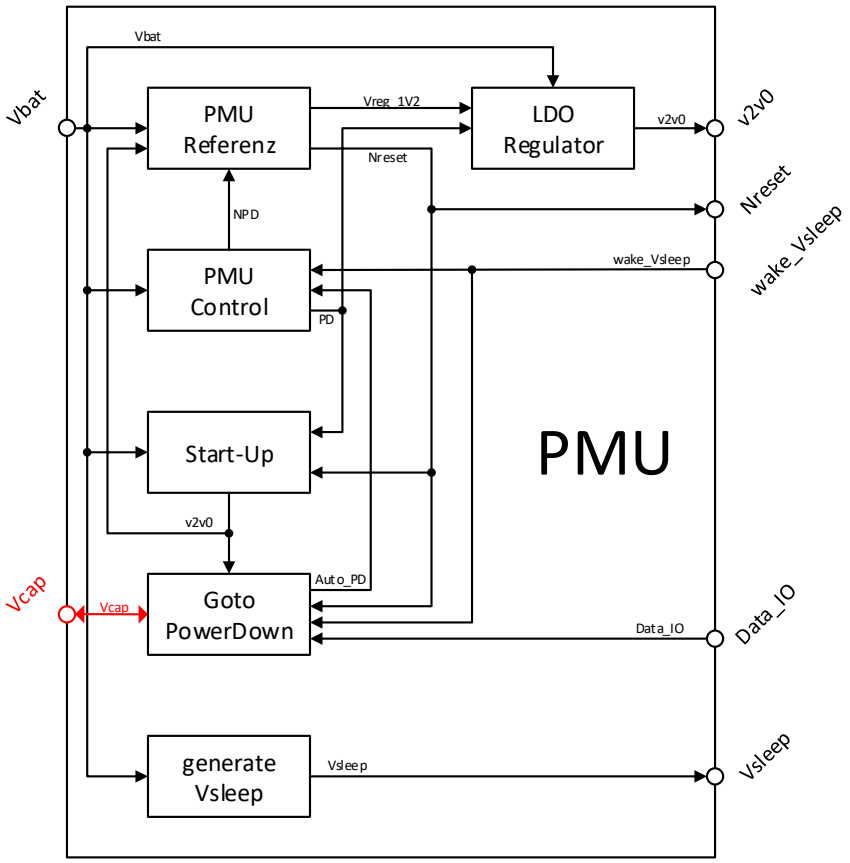

Figure 3.7: Power Management Unit

and hence the supply for the interface by signaling the **Nreset** with logical "0". The PMU is waiting from now again for an incoming data wake signal.

The notation of the supply voltage **v2v0** is used because the supply has a voltage of 2V. In the following chapter it will be named just by Vreg_loc. The pin **Vcap** was on the old version of the IC and was crossed out for the new IC with another package. A revised version of the "Goto PowerDown" block will be described in chapter 5.2.

3.2.2 Transmitter TX

This chapter provides a short overview about the transmitter and what has been taken into account if it is about EMC interferences coming from the transmitter part. Basically the TX just consists of a single to differential conversion and two strong output drivers which create the differential output and delivers enough current over the communication bus. Figure 3.8 shows the principal circuit for the TX stage. The block diagram in Figure 3.5 shows the TX as the first stage with *data_TX* as input and *IFX_l* and *IFX_h* as input/output. To reduce second order EMC effects a break-before-make (BBM) circuit is designed. The so-called Crowbar current will be reduced for the output driver with this circuit. This is a short circuit current that flows directly from the VDD node to the VSS node of an inverter structure and generates a huge current surge if both the p-channel metal-oxide-semiconductor (PMOS) and the NMOS are on for a minimal time period [13]. To have a BBM structure before the output driver reduces not only the overall power consumption. It is also necessary not to generate a certain amount of ground bounce, which may effect the rest of the circuit with its high current amplitudes and generates additional ringing to the whole circuit. The concept of the communication bus by charge shifting may also be affected by this sudden current surge.

Compared to the preamplifier which are the small inverter structures at the gate of MP and MN respectively the size of the output driver is in the order of around 100 bigger. To design a well symmetric output driver also the gate capacitances C_G of the output driver transistors have to be taken into account. There is a difference between the mobility of holes and electrons, so the PMOS transistor with its p-channel delivers his mobility carriers around half so fast as the NMOS transistor with its electrons in the n-channel if they have same W/L. Half speed of mobility carriers leads to half current. The gate capacitance C_G is directly dependent of the area of the transistor with the factor $W \cdot L$. With a bigger size there comes also a

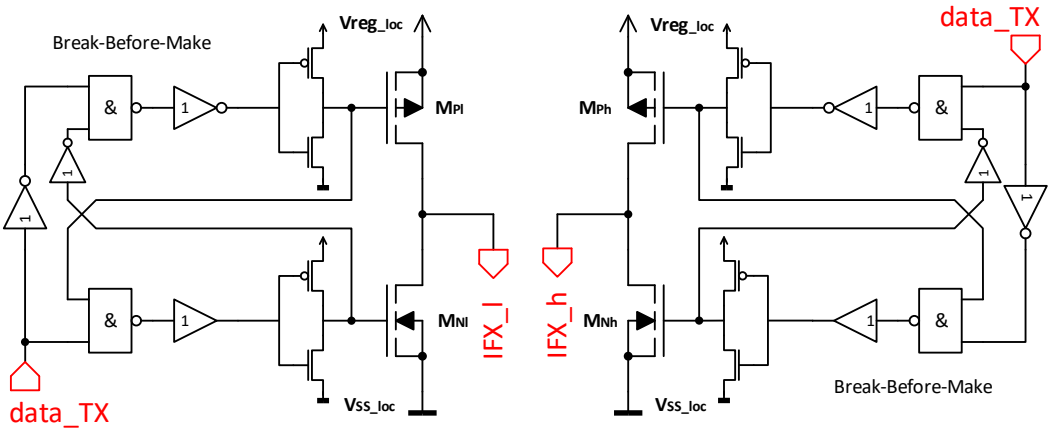

Figure 3.8: TX stage

bigger C_G and the duration of changing the charge on the gate by the preamplifier becomes longer. It is important to take this capacitance into account for the design of this output structure. Such a big transistor with big gate capacitance can not charge or discharge this capacitance fast with just a small inverter structure in front of that transistor.

3.2.3 Receiver RX

The receiver part is designed to have the charge redistribution over the communication wires as input thanks to the capacitive coupling path and converts this redistribution into a data output signal referred to the local reference ground to this BMS. The purpose of this input stage is to find a way to exchange a data flow between two systems of different supply levels. To mention is that there is still a galvanically connection between the supply of two BMSs as already is shown in figure 3.3 and therefore a closed alternating current (AC) path over the capacitive communication wire. So communication over a single path is possible by this charge transfer but not recommended as further operations at the input stage of the receiver (e.g. amplifications) are affected by common mode disturbances. This is not the case for a differential current input as will be shown at the EMC tests.

Figure 3.9 shows the input stage of the receiver with a differential current input. The task of this circuit is to convert the current peaks into a voltage and amplify that over some stages to a newly buffered *DATAOUT* data stream to be ready to communicate with the digital part of the BMS. The data stream coming from the

communication wires influenced by interferences become refreshed and buffered and actually so to speak recycled. This is a big advantage if the whole system is considered to keep communication wires between the single BMSs short. Otherwise there will be more influence by EMC or parasitics due to a longer length of the cables.

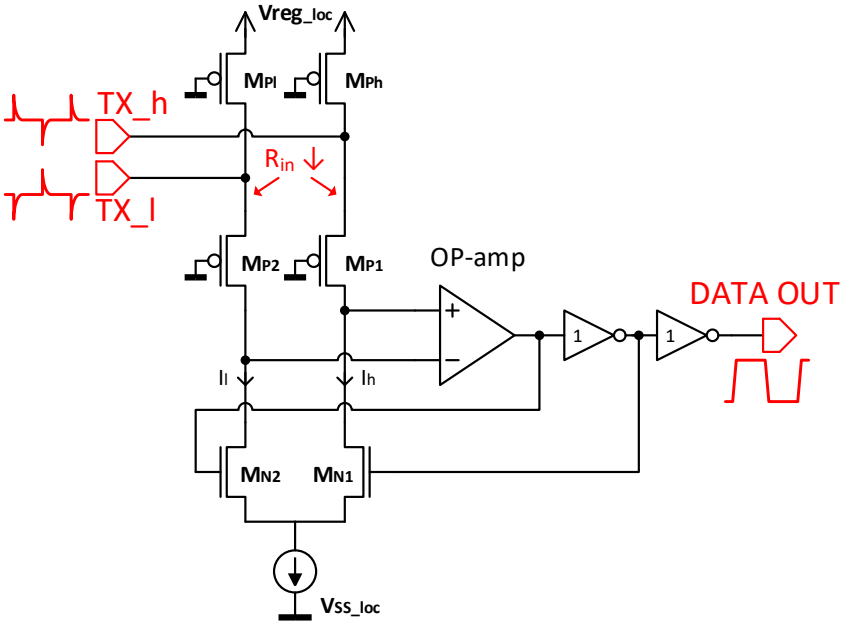

Figure 3.9: RX stage

The supply and ground of the receiver is named with VDD_loc and VSS_loc as they refer to the new interface supply which lies a cell voltage over or under the supply of the previous transmitter from which the signal is coming. The switched-on PMOS transistors M_Pl and M_Ph are used as pull-up resistances to refer these nodes to the local supply voltage VDD_loc of the current module. This terminates the end of the communication bus and hence makes the input of the receiver low impedance.

TX_h and TX_l are considered to be a current input. The nodes at both inputs TX_h and TX_l are low impedance as already mentioned before which is the reason for the capacitive peaks in the data input signal what is caused by the charge of the capacitive coupling what is shown in the Figure 3.9. The discharge of the capacitor depends on the input impedance, that is why the communication bus is already specified in terms of capacitive and resistive values. A common gate stage converts the input current peaks into voltage peaks. This stage is necessary

to reduce feedback effects to the input. The differential voltage signal becomes amplified and results as a data output signal referred to the new reference ground which is equal to the input data stream. Noise or interferences coming from the ground or the supply will not influence this differential signal. Positive feedback will be used to increase the efficiency of the differential to single-ended conversion and to make the voltage node at the inputs of the operational amplifier (OPA) more stable.

In summary this RX block converts a raising edge on the TX_h input due to the capacitive charge transfer to a ”logical High” and a raising edge on the TX_l input to a ”logical Low”. The OPA consists of more than three stages to successfully amplify the small voltage peaks of few tens mV to a very clean output stream.

3.2.4 Wake-up

For power consumption limitation reasons there is a wake-up and power-down function included. Sleep supply which is directly generated by the cell voltage supplies the most required functions to wake up the IC in case of incoming data from one of the interfaces. The wake command consists of a few consecutive clock cycles which have to arrive within a certain RC time constant to finally give the enable for the wake up of the PMU and hence leave the sleep mode.

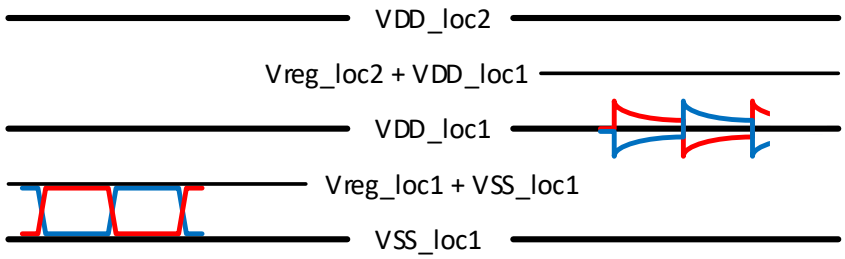

Figure 3.10: Receiver RX in sleep mode - PMU off

The transistors $MP1$ & $MP2$ at the receiver in figure 3.9 are usually switched on and makes the node of the arriving interface signals low impedance for fast reaction. Is the receiving IC in sleep mode, so this receiver circuit is not working due to the missing $Vreg_{loc}$. The before mentioned transistors are switched off and make the input nodes more high impedance (in comparison figure 3.10 and figure 3.6). For reconstruction of the input signal the ”Wake-up” block is responsible which is supplied by the ”Vsleep” voltage.

Chapter 4

Laboratory Verification

4.1 Communication Interface Testchip

Leading to a functional BMS IC there has to be first a complete check of all the sectors, which are included in such a battery system. In this case it will be the communication interface, so there is an own testchip designed, which just proves the functionality of the communication system. Every part of the battery management has to work properly, so the concept of the galvanically separated differential bus is no exception.

For this thesis a test-IC is already available to prove the communication quality. It consists of 2 interfaces which were already shown in figure 3.5. Both interfaces are changeable between TX and RX by an own setting pin but for the demonstration of communication one of those interfaces is for receiving data from the previous satellite and one is for transmitting this data to the next satellite. This testchip has 3 functions:

- Received differential data becomes translated into single ended and buffered
- Data exchange between the MU and the interfaces by UART over the GPIO pins
- Data from MU or the receiving interface becomes translated into differential pair and buffered by a strong driver

For the testchip the Infineon package PG-TSDSO (Plastic Green Thin Shrink Dual Small Outline) with 14 Pins was used (Figure 4.1). The testchip is equipped with ESD diodes on every pin to reduce the harm on the chip through voltage breakdown and therefore through a transient current peak. The following points give a short introduction to the single pins.

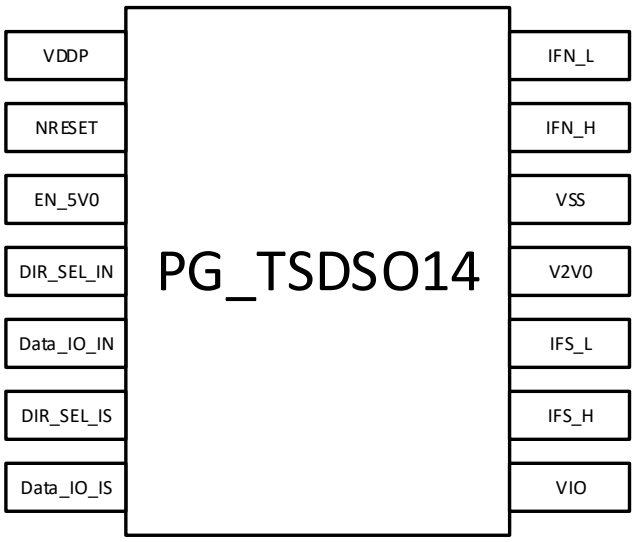

Figure 4.1: Testchip

- **VDDP**: The IC is supplied by the battery voltage with this power pin. In terms of this thesis also called as local supply or local VDD.
- **NRESET**: This is an output pin which is "High" if the IC become enabled. *NRESET* will be used to enable the *Interface* structure and the *Power Down* structure. It will also be used to enable external components like an external $3V3$ voltage regulator what supplies the *GPIO*.
- **EN_5Vo**: This input enables the PMU of the IC that generates the V_reg voltage.
- **DIR_SEL_IX**: The communication direction will be chosen for the north-interface X=N and the south-interface X=S.
  RX: $DIR\_SEL\_IX = 0$
  TX: $DIR\_SEL\_IX = 1$
- **Data_IO_IX**: The GPIO pins are the connection to other periphery like the BMU or the μC.
- **VIO**: This power input sets the supply voltage level for the GPIO pins and is usually connected with the $V2Vo$ pin in case of a slave. The MA have to communicate with a μC by $3V3$ levels, so the *VIO* is in this case connected with an external $3V3$ voltage regulator.
- **IFX_Diff**: They are the differential interface pins IFX_H and IFX_L (High and Low) for the *north* side and the *south* side to connect with the $Slave_{n-1}$ and the $Slave_{n+1}$ over the external wiring.

- **V2V0**: The voltage regulator output V_{reg} is used as power supply for the differential interface and is around half of the cell voltage. This voltage is available if the IC become enabled by the *EN_5V0* pin or in case of receiving data from one of the differential interfaces. There is always generated a *help*-voltage permanently by the cell voltage which give enough supply for the *Standby* mode to generate a wake up signal to enable the PMU as well. The following version of this IC have replaced the supply of 2V with a supply of 1.8V.
- **VSS**: The local ground of the chip which is directly connected with the minus of the battery cell.

4.2 Communication BMS Demonstrator

With the communication testchip mentioned in the previous chapter a demonstrator was designed to show the functionality and success of data transmission and the communication inaccuracies as well as the proof of EMC. To show up that functionality several PCBs are designed which have the same function of communication.

The red PCB in figure 4.2 is used as the master device of the demonstrator (Figure 4.3). The design of this board is the footprint of a single battery cell module with its positive and negative pole on the sides. So it easily can connect them together. This board was usually prepared for EMC measurements to proof Direct Power Injection (DPI) and bulk current injection (BCI). Therefore the board was given an EMC conform design with micro stripline length $< \lambda/20$ and same wire lengths at the differential transceiver side and a wire thickness of 70μm of the PCB copper plane to support a higher current flow. Additionally there are SubMiniatur version A (SMA) connectors and footprints for a network between that connector and the differential interfaces prepared. That makes it possible to build up a capacitive network test setup for the DPI measurement as well as a network for the 150Ω method for common mode emission measurements [2]. Vias in the communication path were endured and the bottom area consists of a ground plane.

The green PCBs on the right side of figure 4.3 are designed as multicell testboards. They consists of 3 slaves and each of those slaves can have its own cell supply with 18650 lithium battery cells which can be connected in a row to simulate a realistic behavior of BMS in ring topology with independent supply.

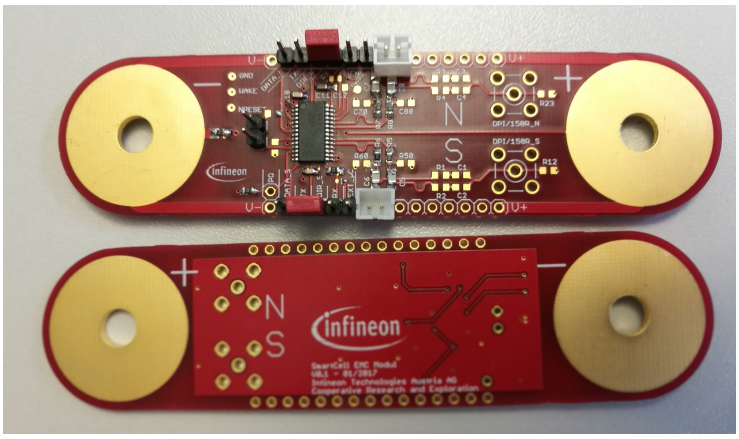

Figure 4.2: EMC-Modul Demonstrator

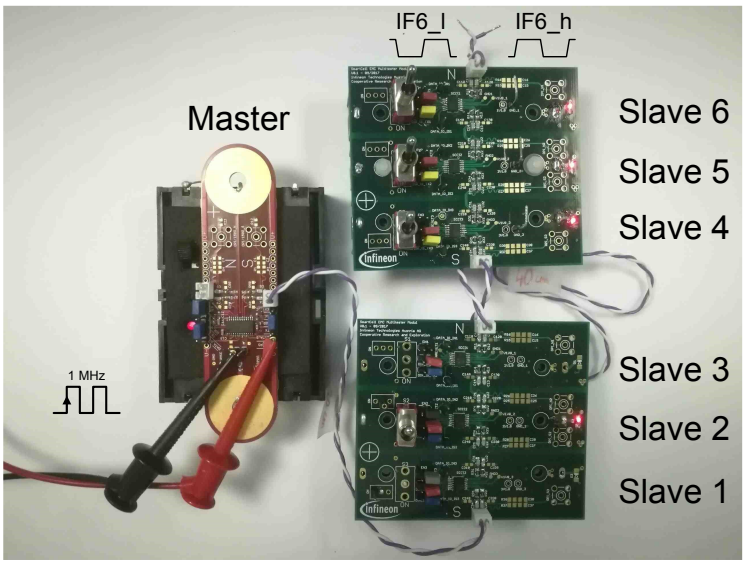

Figure 4.3: Demonstrator setup with runtime measurement

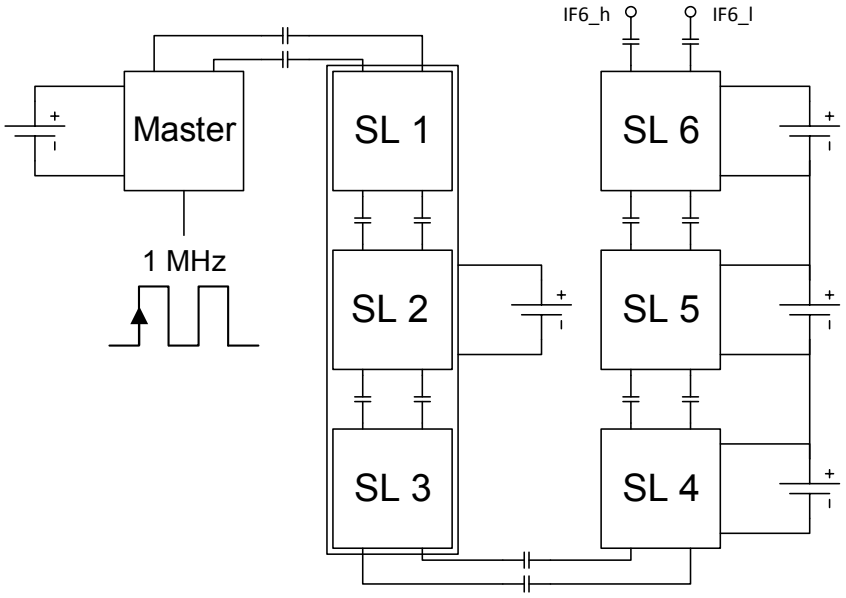

Figure 4.4: Schematic of the demonstrator board

A 1 MHz square input signal is coming from a signal generator and enters the GPIO input of the master device. For measurements over all PCBs an isolation transformer is used for signal generator or oscilloscope to separate its grounds. Otherwise there will be a short between the ground of the master device and the ground of the multicell boards. As overview of this demonstrator a schematic is shown in figure 4.4.

Figure 4.5 and 4.6 shows both sides of the multicell testboard. These constellations are possible:

1. The cells can be connected in series with the jumpers ”RBAT12” and ”RBAT23” ((1) in figure 4.6) to simulate a battery module with stacked cell supplies. Each slave should then have a switch for power-on.
2. All slaves are supplied by one cell for test cases as stripped down variant. Only one cell and one switch will be needed. 4 jumpers from (2) in figure 4.6 are necessary to connect slave 1 and slave 3 to the cell supply

Standard communication of those multicell boards is from ”South” to ”North”, marked with ”S” and ”N”. To change the direction of communication the red and the blue jumper seen in Figure 4.5 must be set. The black jumper is for activating the ICs regulator to supply the interface. It is the Enable pin **EN_5V0**. In case of

the master device those jumpered digital inputs can be regulated by the μC.

An RF SMA-connector with a combined DPI and 150Ω input/output impedance matching network is prepared for EMC measurements on each side of the differential interfaces.

On the back of this PCB in figure 4.6 a battery holder for 18650 battery cells is mounted to demonstrate a well behaved BMS board separated to any other ground, only connected with the differential bus.

The schematic of the demonstrator is shown in figure 4.4. It uses the 2 different constellations for each multicell board. The first board with 3 slaves in parallel supply and the second board with each slave its own supply in a row.

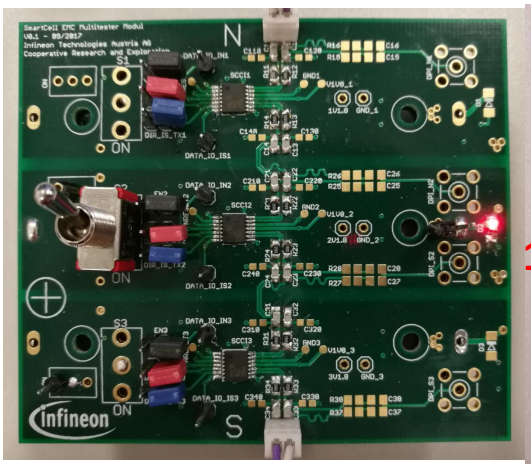

Figure 4.5: Latest Demonstrator PCB - front

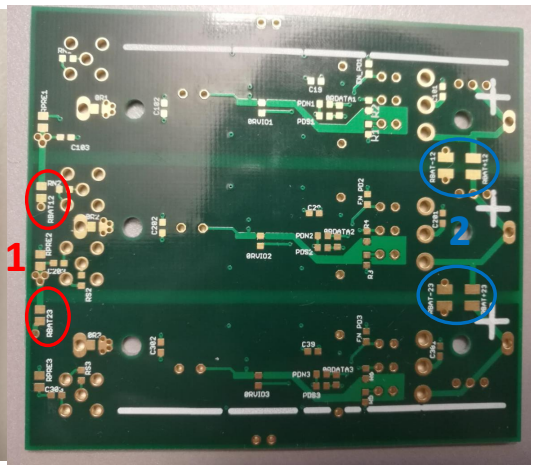

Figure 4.6: Latest Demonstrator PCB - back

4.3 Function Simulation

To verify the start up of the IC a command of successive data pulses is sent from a master device over the ICC bus to a sleeping slave device. In figure 3.10 there are shown 6 clock cycles. They are the trigger for finally starting up the device with the rising edge of the wake-up pulse (blue color). The voltage **v2v0** in purple color is rising immediately by the start-up supply regulator and with it rises the bandgap voltage **Vreg1v2** shown in cyan. With an RC time constant of around 26*ns* shown in Figure 3.10 after generating the bandgap voltage the **Nreset** will

occur which finally turns off the wake signal and turns on the LDO regulator supply for the interface.

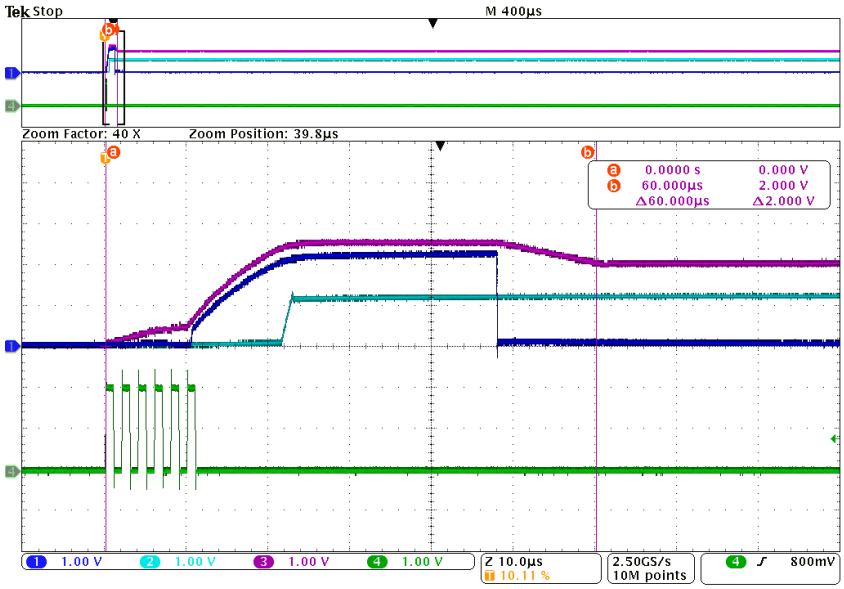

Figure 4.7: Wake-up from incoming data stream

For proofing the communication and data rate limits the master device was connected with 4 slave devices (Figure 4.2) with same supply in ring topology (Figure 4.8). So a function generator with pulse source was connected with one of the GPIO pins from the master device and transfered this pulse signal over the ICC bus to the other slaves and detects this signal again at the other GPIO pin. Data rate measurements were made with frequencies of 100kHz, 1MHz, 4MHz, 5MHz, 10MHz and 16MHz and are shown in figure 4.9 with the order from left to right and top to bottom. The purple signal on the oscillator pictures is the detected signal arriving again at the master device. The other one is the input signal from the signal generator and the blue and green ones are the differential signals leaving the master device. A general requirement for this BMS solution is a data rate of $2Mbit/s$ and therefore a frequency of $1MHz$ is just necessary. In contrary to the $100kHz$ that is a really clean signal the $1MHz$ signal is possessed by ground bounce which can be seen very well in the second picture. The reason is the dynamic switching current due to the strong differential output stage. The input pulse signal affects the output signal in time of the switching because both signals pass simultaneously through the same master board with the same ground. The ringing shown in the input signal is caused by the function generator due to

capacitive or inductive loads and therefore a mismatched impedance.

The measurements 3 to 6 shown in that figure shows the data signals in case of higher data rate. So theoretically this IC is capable to transfer data up to $16MHz$ over 4 slaves. Above this level it comes to dropouts. A data rate with more than $2MHz$ suffers much from ringing because the output nodes are too less stabilized.

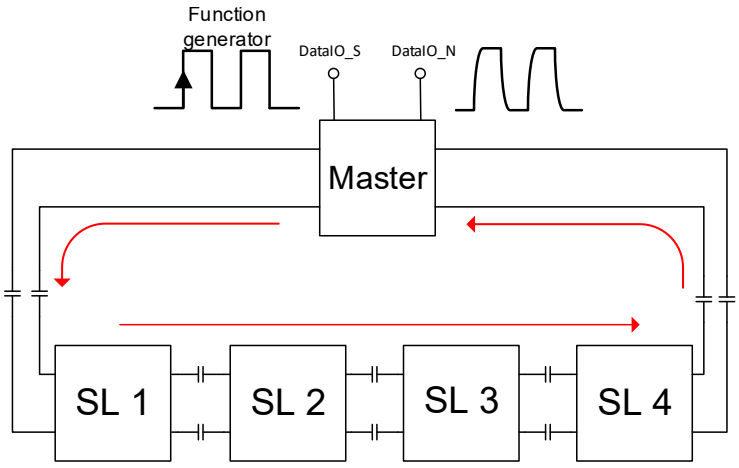

Figure 4.8: Data Rate Measurement: 100kHz - 16MHz

With the demonstrator construct from figure 4.10 jitter measurements have been performed with an Agilent Oscilloscope. For the first measurement just the jitter over one board - the master board - was measured. So the input signal was triggered on the rising and falling edge and it was resulting the differential signals IFX_h & IFX_l on figure 4.11. The interface of the master device was only in TX mode, because the master was not receiving any differential signals. So the IC got the data from the GPIO port based on the IC ground and translated the signal into differential. As it is shown in this figure the differential output of the master device is still ok. The data rate is just $2Mbit/s$ so jitter will not have any impact, but in case of several boards in a row this might be different.

For the farther planned communication measurements of the slaves a big issue appeared. It seems that the differential RX stage is asymmetric, which leads to a difference in time between the differential output in comparison of rising and falling GPIO input signal. This might lead to troubles in communication after a higher number of slaves in a row as the duty cycle is rising after each slave. This

Figure 4.9: Data Rate Measurement: 100kHz - 16MHz

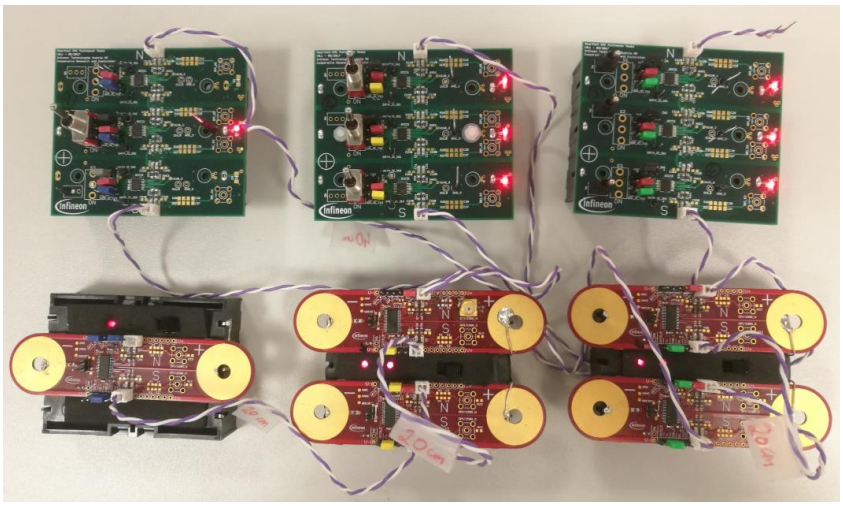

Figure 4.10: Measurement of jitter properties

behavior is linear, so after each slave there is a systematic offset in time which will add up step by step.

Another issue is also showed in the same figure but appeared already at the master output stage. The differential output stage of the interface hasn't the same rising and falling time. The Push-Pull output driver stage was actually designed with the right geometry of the transistors, but it seemed that the preliminary driver had wrong proportions which had been updated with an upcoming tapeout. The W/L of the p-channel transistors of the preliminary driver stage becomes bigger, so they can raise the gate level of the huge low-side n-channel transistors of the differential output stage faster. As the output stage is really huge, so are the parasitic capacitances between the transistor terminals. The capacitance C_{GS} is able to charge faster with higher current and that opens the channel of the NMOS faster.

In total these inaccuracies are leading to a general duty cycle distortion as seen in figure 4.11. Duty cycle distortion is a kind of jitter, which is caused when certain bit states have different durations. So the ”high” level is longer than the ”low” level and vice versa.

There is prepared another demonstrator (figure 4.10) with a total of 13 slaves to analyze this systematic offset to show up a trend how far this offset is leading. Measurements are made again with those 13 slaves in a row, then an interpolation is used until a maximum number of 108 slaves.

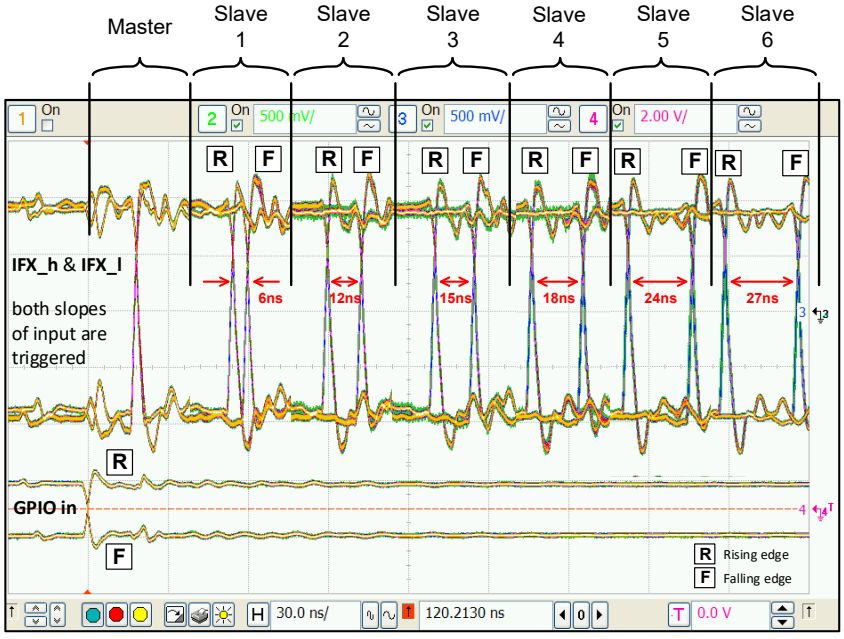

Figure 4.11: Results of runtime measurement

The results of this propagation delay between rising and falling GPIO input signal is listed in the table 4.1. As already mentioned before does the first measurement from master GPIO input to differential output causing no additional propagation delay. So the duty cycle is still exactly 50%. That shows what is already proven that the receiver stage is causing this delay between rising and falling input.

The average jitter value from master board over the slaves is around $4ns$. It is calculated by the average factor of the accumulated jitter values from previous slave to slave.

$$Jitter_{average} = \frac{1}{N} \sum_{n=0}^{N} \left(Jitter_n - Jitter_{n-1} \right) =\sim 4ns \tag{4.1}$$

To reach a duty cycle of 90% it would need a row of 100 slaves for a communication signal with the period of $1MHz$. Still then the transceiver is theoretically able to receive the data because that would mean a communication data rate of $5MHz$. For a $10MHz$ frequency the system is only able to transmit over 9 slaves to reach a duty cycle of 90%.

	peak-to-peak jitter	Δ between DataIO_M & IFX_h/IFX_l
	[ns]	[ns]
M - M	1,8	0
M - S1	5,5	3,5
M - S2	9,5	7,5
M - S3	12	10
M - S4	18	15,5
M - S5	25	23
M - S6	27	25
M - S7	32	29,5
M - S8	36	34,5
M - S9	40	38
M - S10	45	43
M - S11	49	46
M - S12	52	49
M - S13	54	51

Table 4.1: Jitter measurements

4.4 Immunity Measurement Methods Bulk Current Injection & Direct Power Injection

The direct RF power injection method is a measuring method to determine the immunity of an IC as function of the effective power transmitted to the circuit. It is a test method with an integrated circuit under test coupled with radio frequency (RF) disturbances. The schematic in figure 4.12 shows the construct with the exact current flow. It is a component test, so only the IC is coupled with the DPI source at its interface input pins. In receiver RX mode the end is terminated by switching on the PMOS in the push-pull stage. The DPI disturbances won't enter the receiver part because this is a differential pair shown in previous chapter in figure 3.9 and is damping common mode disturbances. So finally the power injected into the differential pins is heading to the regulated supply voltage and over its external 100nF capacitor back to the same ground of the DPI source.

The frequency range for the measurement of the DPI injection is between 150kHz and 1 GHz for 30dBm and 37dBm. The fault rate is shown in table 4.2. Both the 30dBm and 37dBm are leading to dropouts of the functionality.

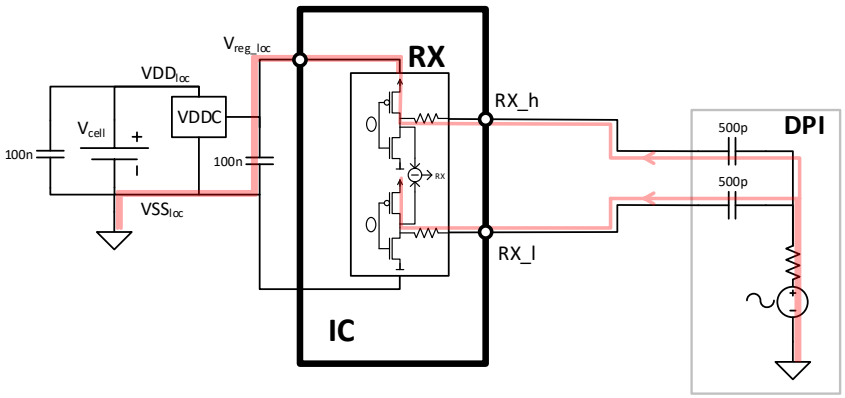

Figure 4.12: Current flow in case of DPI

The BCI test is a similar immunity test method and is also used to characterize the immunity of an IC to conducted electromagnetic disturbances. The difference to the DPI method is to test a whole system with this method and not only an IC. So external components are also available. The test schematic is shown in figure 4.15 which is also showing the current flow in case of current injection. An RF generator and amplifier is used to create a strong magnetic field in an injection probe. Through this injection probe finally the twisted pair cable is connected on both ends with the external components of the interface.

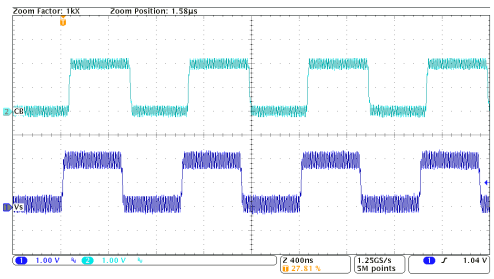

Figure 4.13: DPI level: 37dBm 69MHz

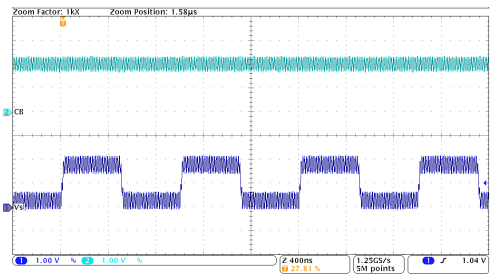

Figure 4.14: DPI level: 37dBm 70MHz

To prove the functionality currents of 200mA and 300mA are injected. This current is also not able to enter the receiver circuit because the PMOS push stage is switched on and opens a low impedance channel in direction to the regulated supply voltage. From there an RF channel over the 100nF capacitor is leading over the battery cell connected current bar to the battery cell voltage capacitor. From there it goes the way back over the transmitter stage and searches the most low

Direct Power Injection (DPI)	
30dBm	37dBm
Frequency in MHz	
77 - 87	71 - 145
97 -123	
	179 -186
208 - 349	207 - 351
374 - 400	371 - 400

Table 4.2: DPI Fails

impedance way in direction to the pins. The W/L of the output stage transistors have to be designed as big to withstand a current flow of 300mA. Otherwise only external components are affected from this RF current. The IC is still working in most cases. But there are similar frequencies like from the DPI test method that causes dropouts of the functionality.

4.5 Emission Measurement Methods 150Ω Direct Coupling Method

To get an insight of the electromagnetic emissions coming from the interface an emission measurement was made with the test method proposed from IEC for conducted emissions which includes the direct RF current measurement with 1Ω resistive probe and RF voltage measurement using a 150Ω coupling network. For the measurements of the communication IC interface a test setup with the EMC demonstrator board of figure 4.3 was build up as illustrated in figure 4.16. Measurements were made for 3 conditions:

- IC in sleep mode
- IC awake with data transfer
- IC awake without data transfer before Power Down (PD)

There are regulations from the CISPR 25 which show up the limitation of emissions coming from automotive components [1]. Several values from certain radio bands should not be exceeded to not disturb these radio bands. These limitation values are divided into 5 classes. The limits for Class 1 are shown in figure 4.20. This is the lowest class and the interface fulfills the requirements for this class.

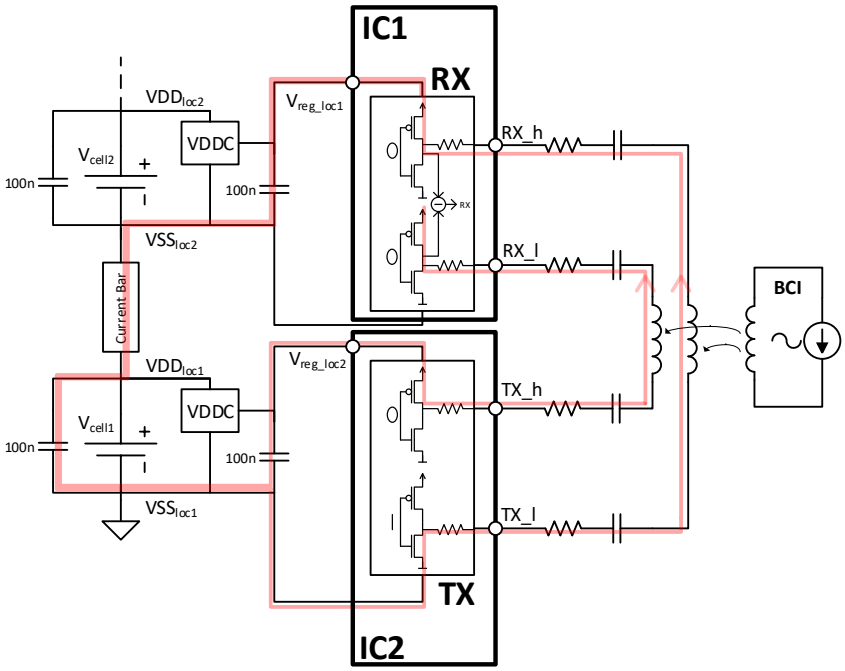

Figure 4.15: Current flow in case of BCI

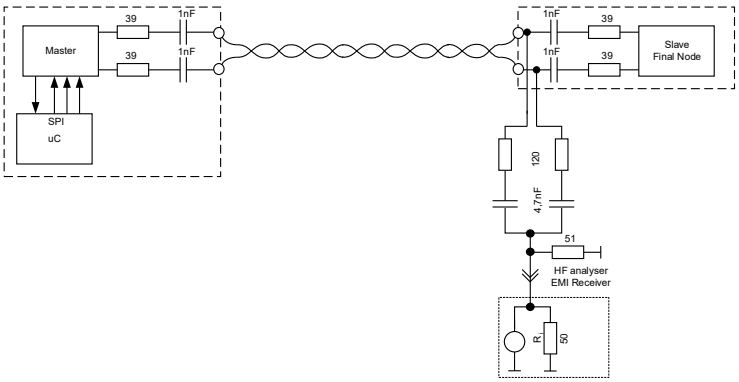

Figure 4.16: Test setup for 150Ω conducted emission measurement

While the IC is turned on and is in communication mode as shown in figure 4.18 the emissions are between $10MHz$ and $100MHz$ at its limit of around $60dB\mu V$. These emissions come from noises like the dynamic switching current in the output stage structure. To neglect the crowbar current by using a break-before-make in front of the output stage is definitely a huge improvement with respect to emissions, but to reduce the dynamic switching current at the output stage means to reduce its $\frac{di}{dt}$. A low-pass filter can be used to handle this.

Another consideration of this high noise level is the additional noise floor because the measurements were not made in a shielded measurement room. However, it can be assumed that the reason for this emission is a less well-designed output stage.

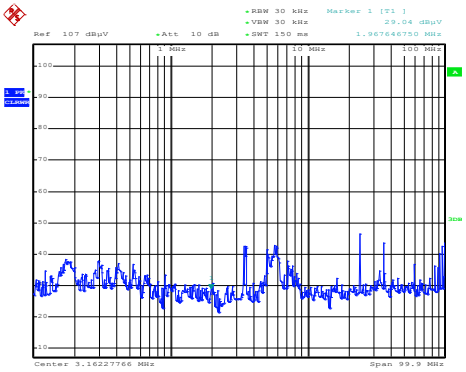

Figure 4.17: 1^{st} condition / sleep mode

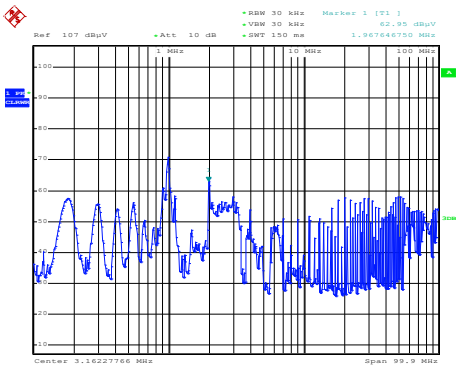

Figure 4.18: 2^{nd} condition / data transfer

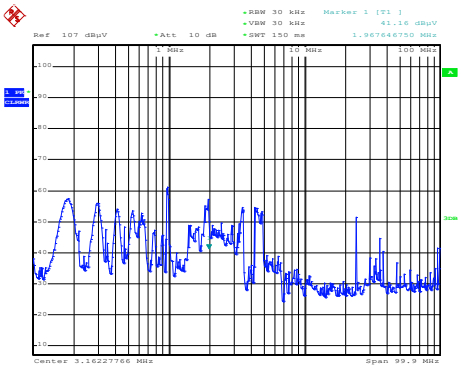

Figure 4.19: 3^{rd} condition / data stop

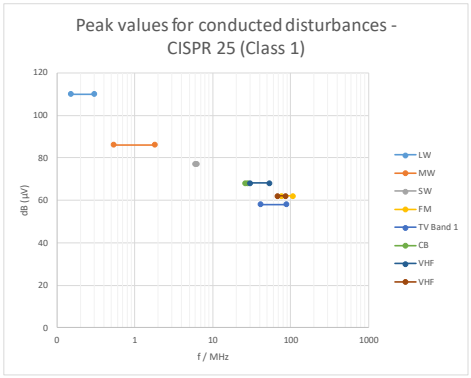

Figure 4.20: Peak values for conducted disturbances

Chapter 5

Resimulation & Optimization

5.1 Correction of the Duty Cycle Distortion

In figure 5.1 are shown equivalent results like the laboratory verification results in figure 4.11. This behavior was resimulated with following testbench in figure 5.3 to find out the reason of this duty cycle distortion. The speculation about the asynchronous differential receiver turned out to be wrong. And as already guessed it is not the wrong proportion of the differential transmitter output stage. The problem is the GPIO output pad driver after the differential to single ended conversion of the receiver. This pad driver seems to suffer from imbalance in one of the preliminary drivers. This causes a delay of around $4ns$.

The simulation was made again without these pad output drivers and the result is shown in figure 5.2. Duty cycle distortion is still present, but the impact of it was reduced. To use the right proportions between the W/L of the transistors of this pad the output driver will prevent adding up such a delay.

Another optimization that was made is the symmetrization of preliminary driver before the differential output stage. The PMOS of this push-pull stage was given a bigger W/L for faster discharging of the gate-source capacitance of the low-side driver. The old version in the IC is shown in figure 5.4. Such an asynchronous switching of the differential output causes ground bounce within the time when both output stages are logic ”high”. The voltage bounce caused by the asynchronous output stage has a peak value of $+0.8V$.

In contrary to the first figure is in figure 5.5 the PMOS transistor of the preliminary stage much stronger designed than before. This push stage is too strong so the NMOS of the push-pull output stage is now a bit faster than the PMOS. Ground bounce is shown now in opposite direction but less strong because the output stage is almost balanced.

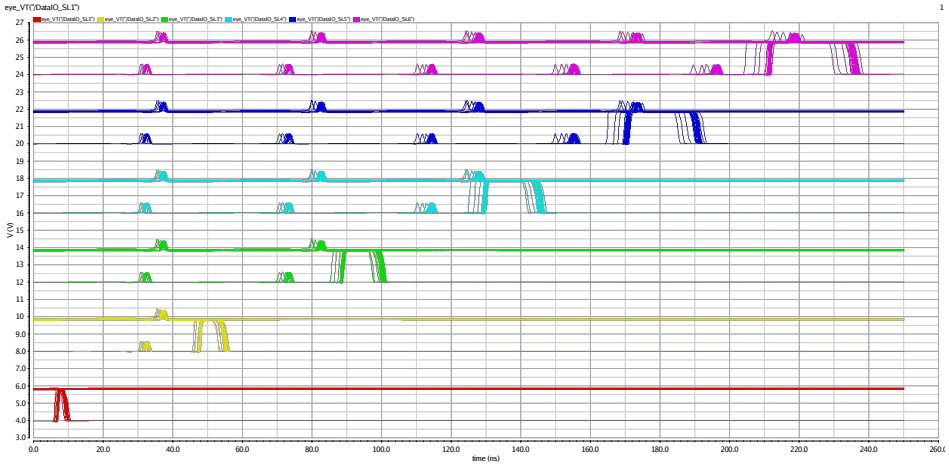

Figure 5.1: Resimulation of duty cycle distortion cause of pad driver

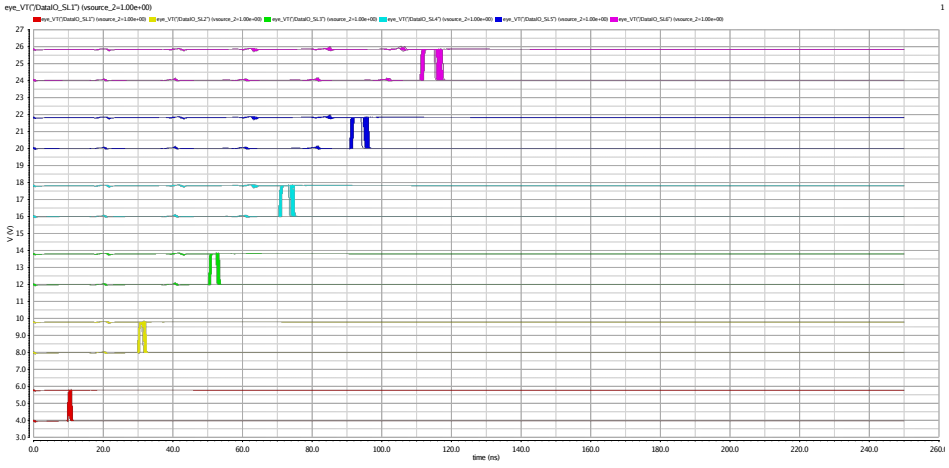

Figure 5.2: Reduced impact of duty cycle distortion

The optimized version is shown in figure 5.6. The preliminary driver is perfectly balanced to finally makes the output stage cross at exactly $V_{reg}/2$. This symmetrization has no impact on the duty cycle regeneration but ground bounce is completely neglected due to the right proportions of the preliminary driver and thus no additional current surge affecting the supply of the whole stack anymore.

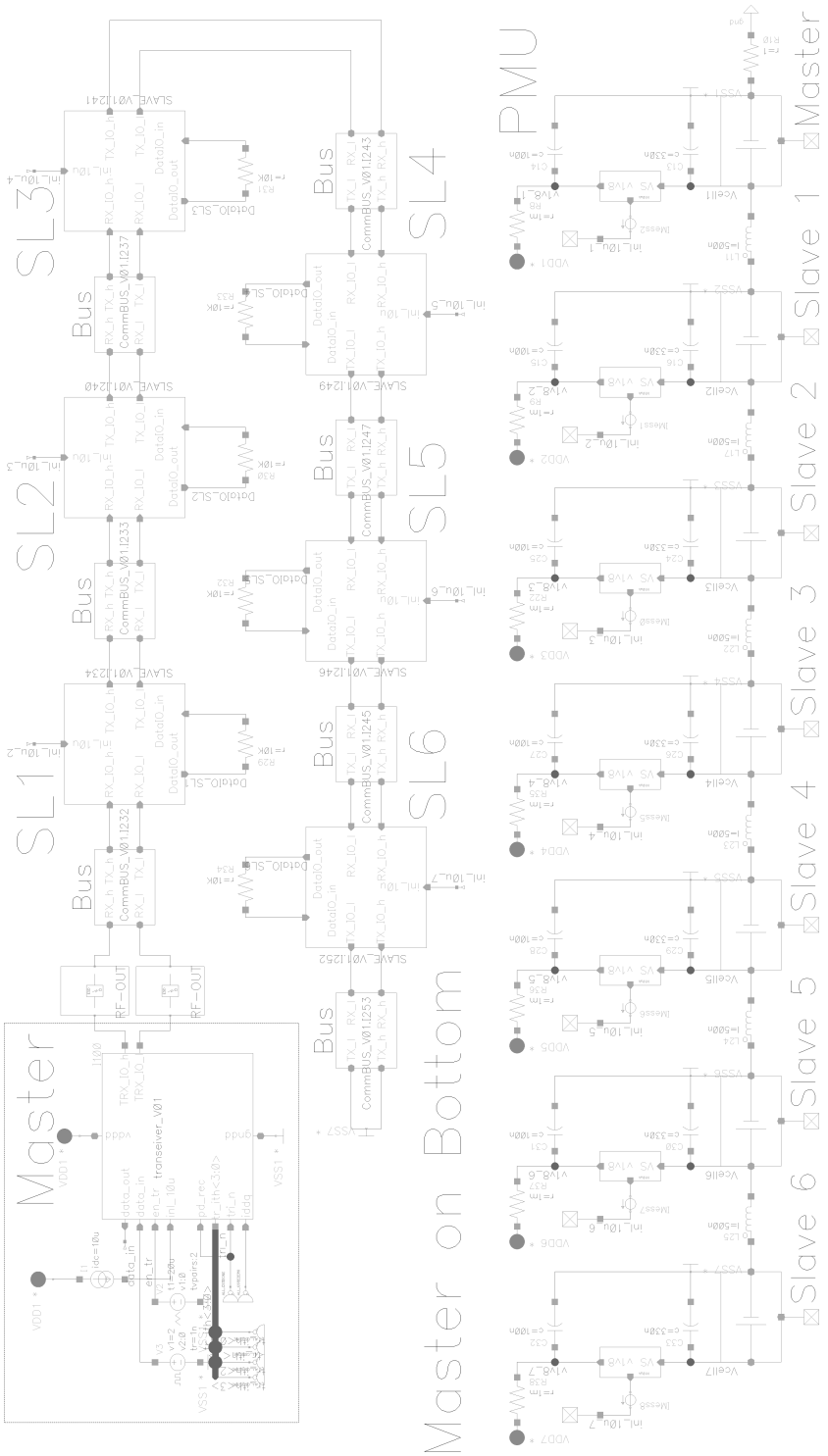

Figure 5.3: Testbench of the resimulation of the duty cycle distortion noise

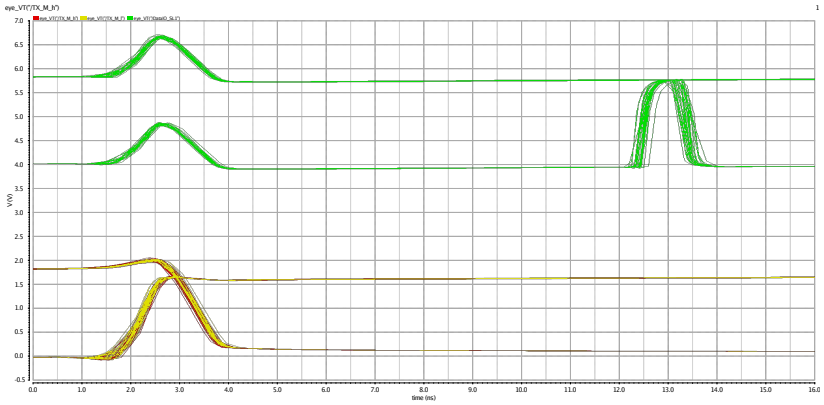

Figure 5.4: Resimulation of differential output stage

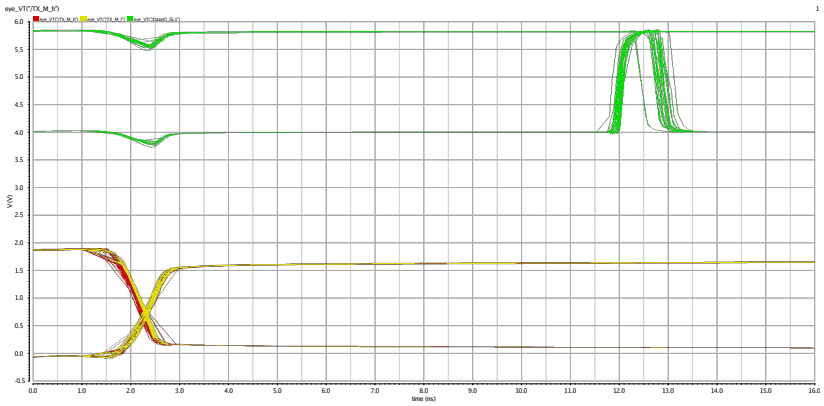

Figure 5.5: First edit of the output stage

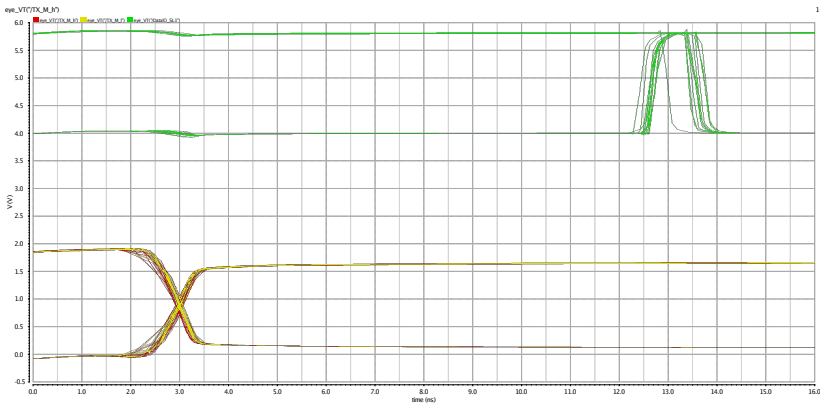

Figure 5.6: Second edit without ground bounce impact

5.2 Improved Auto Power Down Circuit

The power down circuit was originally just dependent on a capacitor and a current source which is discharging this capacitor. This was already mentioned before in chapter 3.2.1. The outcome of the verification of the first version of this IC showed much yield loss. Some ICs were not able to go back in sleep mode even if there was no communication. A part of the ICs could finally go in sleep mode if the external cap on **Vcap** pin was shorted, but this worked not for all of them and was no solution. It turned out that the current source which was there for discharging the capacitor was not working properly and was much dependent on temperature and process. So a simple oscillator was designed to act as timer for the Power down block to solve the issue with the Power down mode.

The time from the last edge of data until the final PD occurs are few hundred milliseconds to seconds. So there is no need for a special oscillator in accuracy or frequency. A simple non-sinusoidal relaxation oscillator was designed (Figure 5.7). The main component of this oscillator is the capacitor that makes a time constant which is directly related to the final frequency. Another important component is the transistor *N7* that creates the hysteresis to define a upper and lower threshold for the switchover by successively shortening the *N4* which is used as a diode.

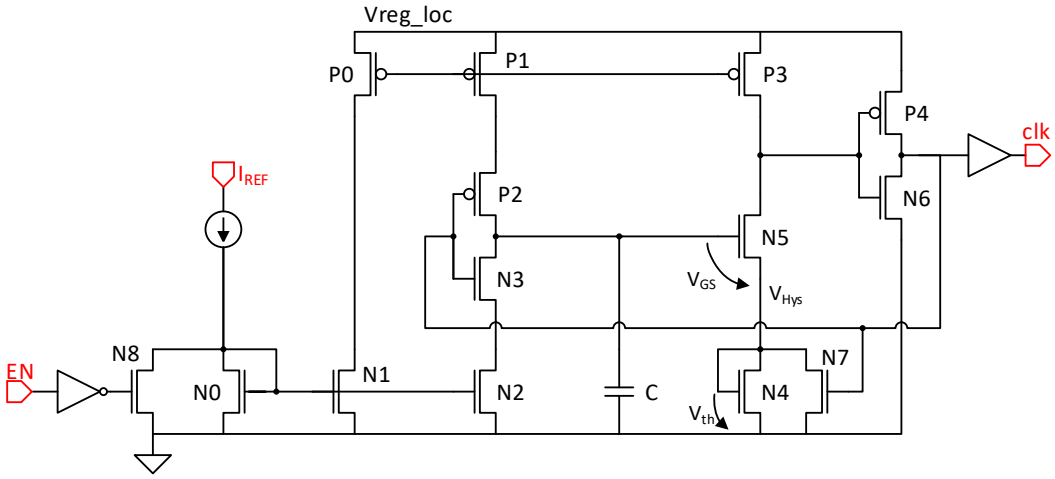

Figure 5.7: Relaxation oscillator for power down functionality

The hysteresis voltage is the threshold of the diode-connected transistor *N4* (5.1). The capacitor is charging if the voltage level of the capacitor is below the threshold of transistor *N5* (5.2). As soon as the capacitor voltage reaches the

gate-source voltage of $N5$ plus the hysteresis voltage (5.3) the output will toggle that deactivates the hysteresis by shortening the transistor $N4$. The feedback of the output to the input will finally toggle the input inverter structure that discharges the capacitor again.

$$Hysteresis: \qquad V_{Hys} = V_{th(N4)} \tag{5.1}$$

$$C \uparrow: \qquad V_C < V_{GS(N5)} \tag{5.2}$$

$$C \downarrow: \qquad V_C > V_{GS(N5)} + V_{Hys} \tag{5.3}$$

The reference current is coming from an proportional to absolute temperature (PTAT) current source and is temperature independent. But the output frequency is proportional to the capacitor who is strongly dependent on process and temperature. The output frequency therefore varies between fast process with $150°C$ and a slow process with $-40°C$ with almost $\pm 30\%$. On the other hand this oscillator has low power consumption and is really small in area.

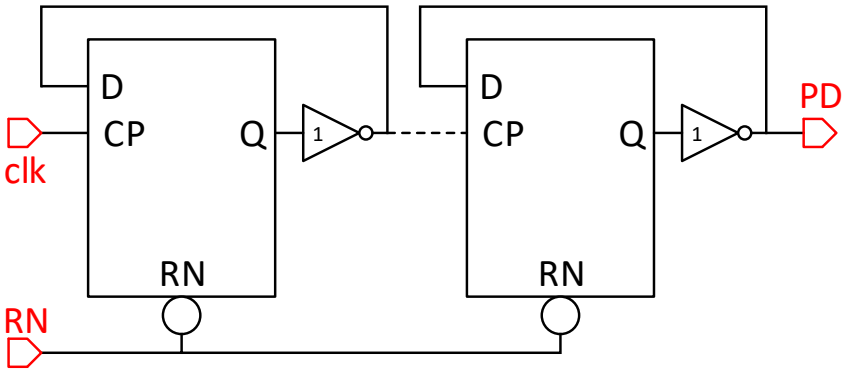

Figure 5.8: Simple frequency divider with latch

A simple cascaded D-Latch series (Figure 5.8) is used as frequency divider or as ″divide-by-2″ counter by feeding back the inverted output to the input terminal ″D″. That should finally generate the PD after a specified time. The frequency at output ″Q″ of one D-Latch is exactly one half of the input clock frequency of this D-Latch. A row of D-Latches can therefore be used to divide the clock signal of the oscillator with an factor of $N = 2^n$ with n is the number of D-Latches. The time after PD occurs is therefore calculated with following equation:

$$t_{PD} = \frac{2^{n-1}}{f_{clk}} \tag{5.4}$$

The data detection circuit 5.9 resets the cascaded D-Latch permanently while there is communication ongoing. If the communication at both inputs "Data_out_N" and "Data_out_S" from the interface stops the series of D-Latches will get an enable signal that activates the frequency divider circuit.

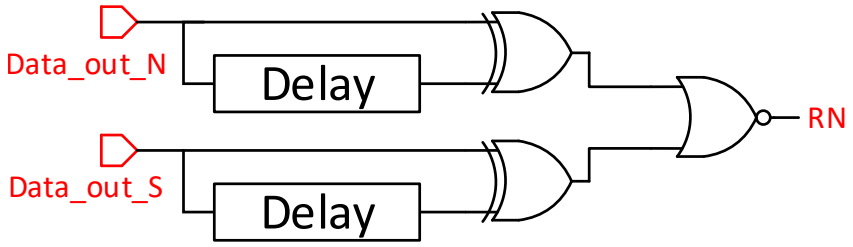

Figure 5.9: Data detection by combinational logic

Chapter 6

Conclusion

Special attention was paid to duty cycle distortion jitter and symmetrization of the differential output stage, as it is necessary to minimize these factors in case of long communications chains, otherwise failures at a communications device might occur at certain process corners and temperatures, and since this is not a centralized but a ring communication system, which results in failure of all modules behind it. For the immunity test with BCI and DPI failures occur in both cases at 37dBm and 300mA respectively, whereby the results of the BCI measurements were no longer available. Overall there should be a clear improvement in the electromagnetic emission values, as the output drivers have been adjusted as well as possible. Another tapeout of this test chip with these changes was not planned within the time period of this master thesis, so that the optimized version of the emission values could not be compared with the old ones.

List of Abbreviations

AC alternating current
ASK Amplitude Shift Keying
BBM break-before-make
BCI bulk current injection
BCU battery control unit
BMU battery monitoring unit
BMS battery management system
BUS binary unit system
CAN Controller Area Network
CISPR 25 Radio disturbance characteristics for the protection of receivers used on board vehicles, boats, and on devices - Limits and methods of measurement
DPI Direct Power Injection
DUT Device Under Test
DC direct current
EV Electrical Vehicle
EMC electromagnetic compatibility
EMI Electromagnetic Interference
EME Electromagnetic Emission
ESD electrostatic discharge
FSK Frequency Shift Keying
GPIO General Purpose Input/Output
HV High Voltage
IC Integrated Circuit
ICC Intercell Communication
ICU Interface Control Unit
IEC International Electrotechnical Commission
IF interface
LDO Low Dropout
Li-Ion Lithium Ionen
LIN Local Interconnect Network
LO Local Oscillator
MA Master

MU Measuring Unit
μC Microcontroller
NMOS n-channel metal-oxide-semiconductor
OPA operational amplifier
PCB Printed Circuit Board
PD Power Down
PLC Power Line Communication
PMOS p-channel metal-oxide-semiconductor
PMU Power Management Unit
PTAT proportional to absolute temperature
RF radio frequency
RFI Radio Frequency Interference
RFID Radio-Frequency Identification
RX Receiver Exchange
SL Slave
SOC State of Charge
SOH State of Health
SMA SubMiniatur version A
TRX Transeiver
TX Transmitter Exchange
UART Universal Asynchronous Receiver Transmitter

List of Figures

Appendix

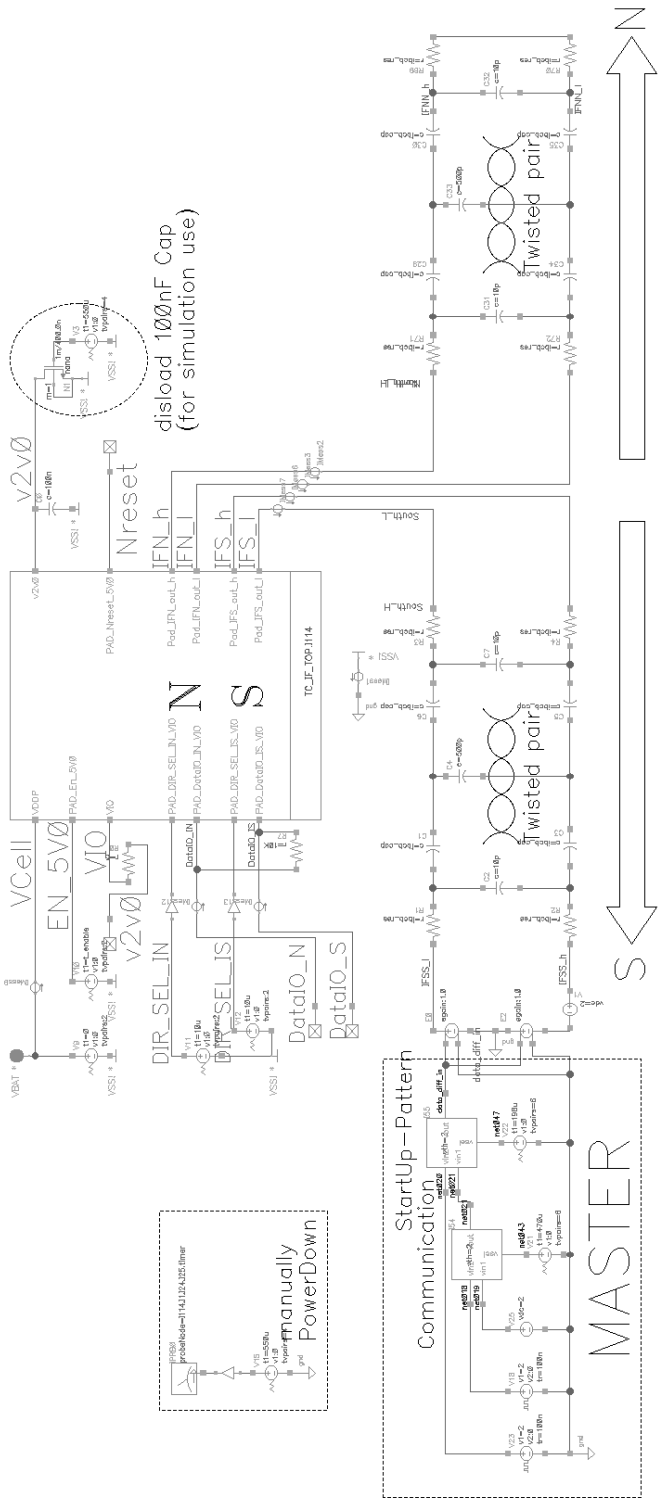

Figure .1: Testbench with whole Communication IC - base functionality

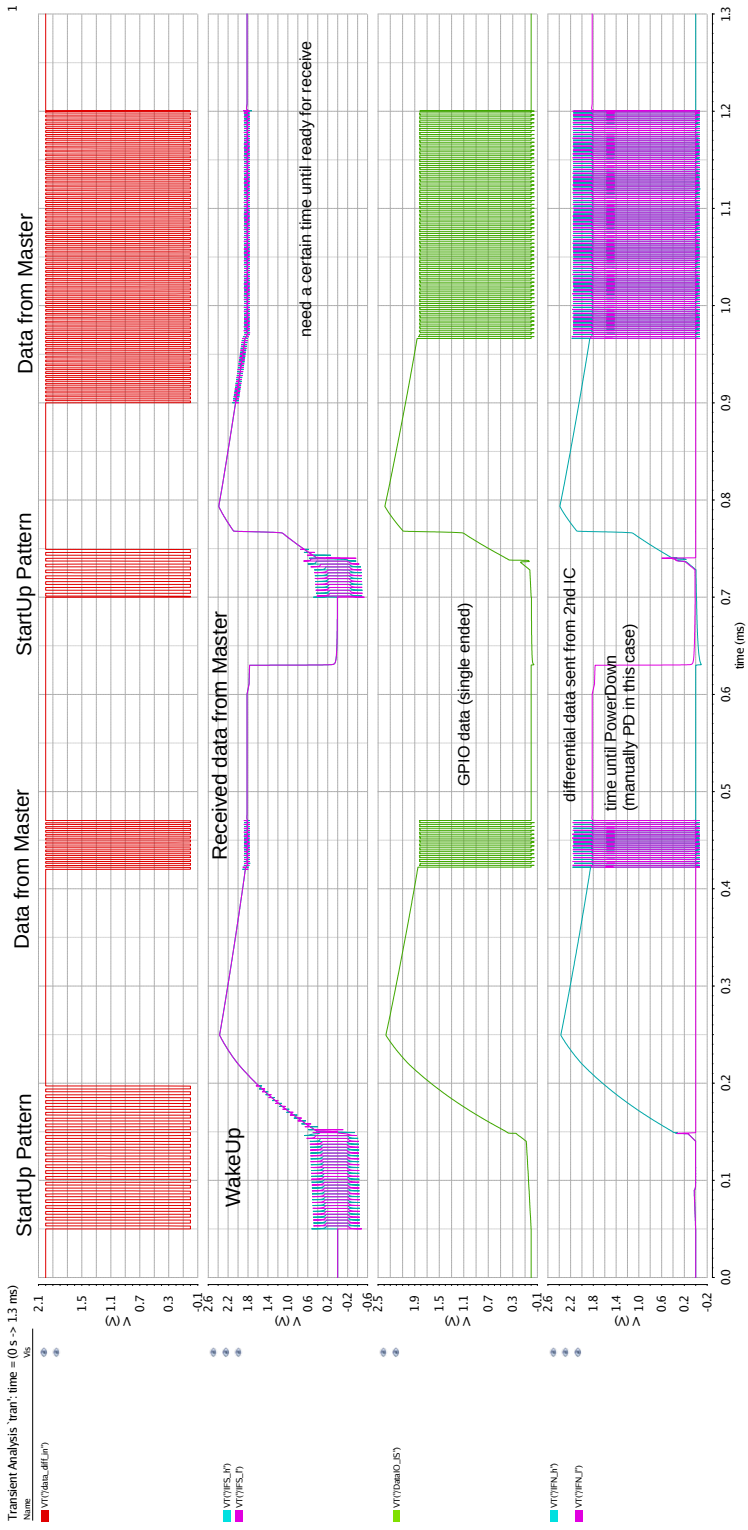

Figure .2: Communication with wake up procedure

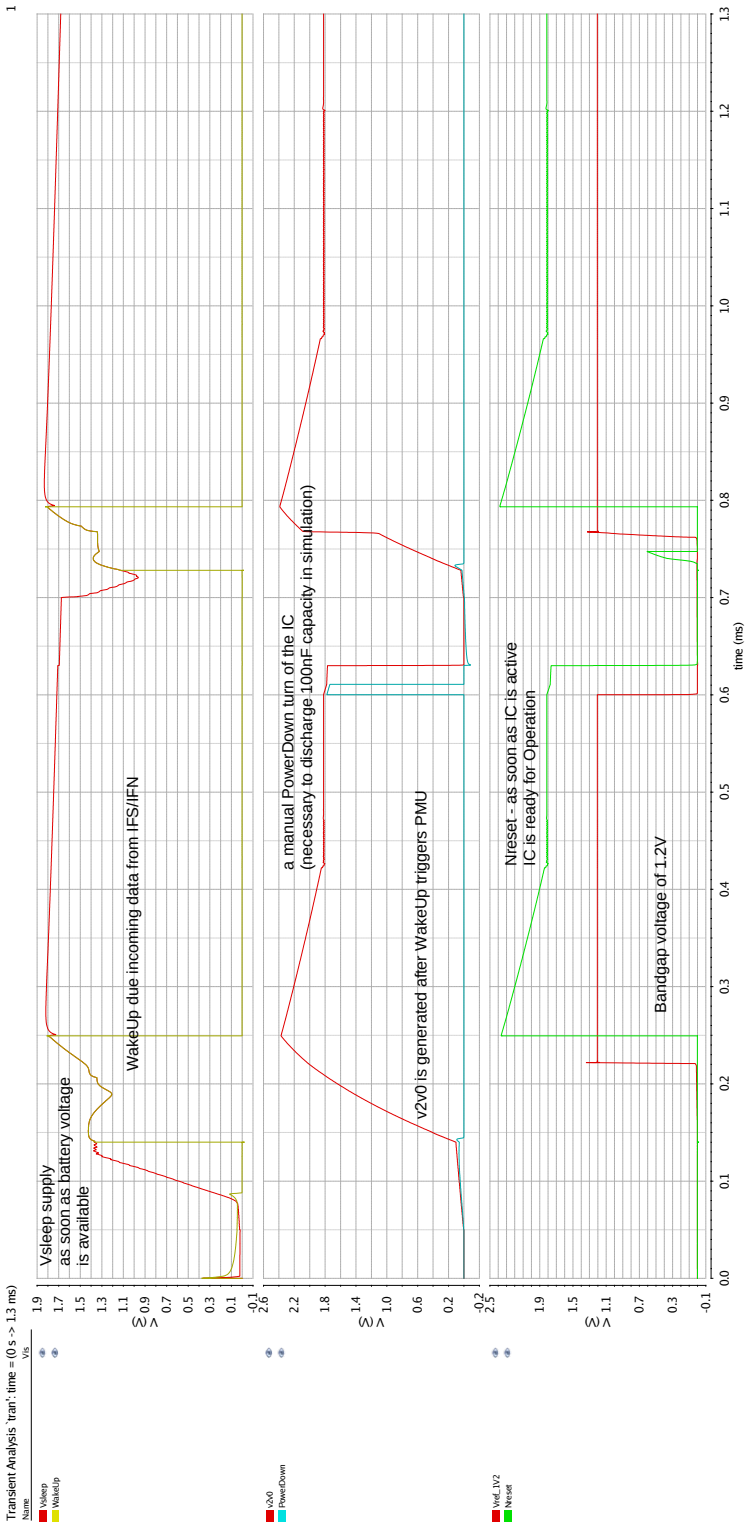

Figure .3: Power down functionality - optimized

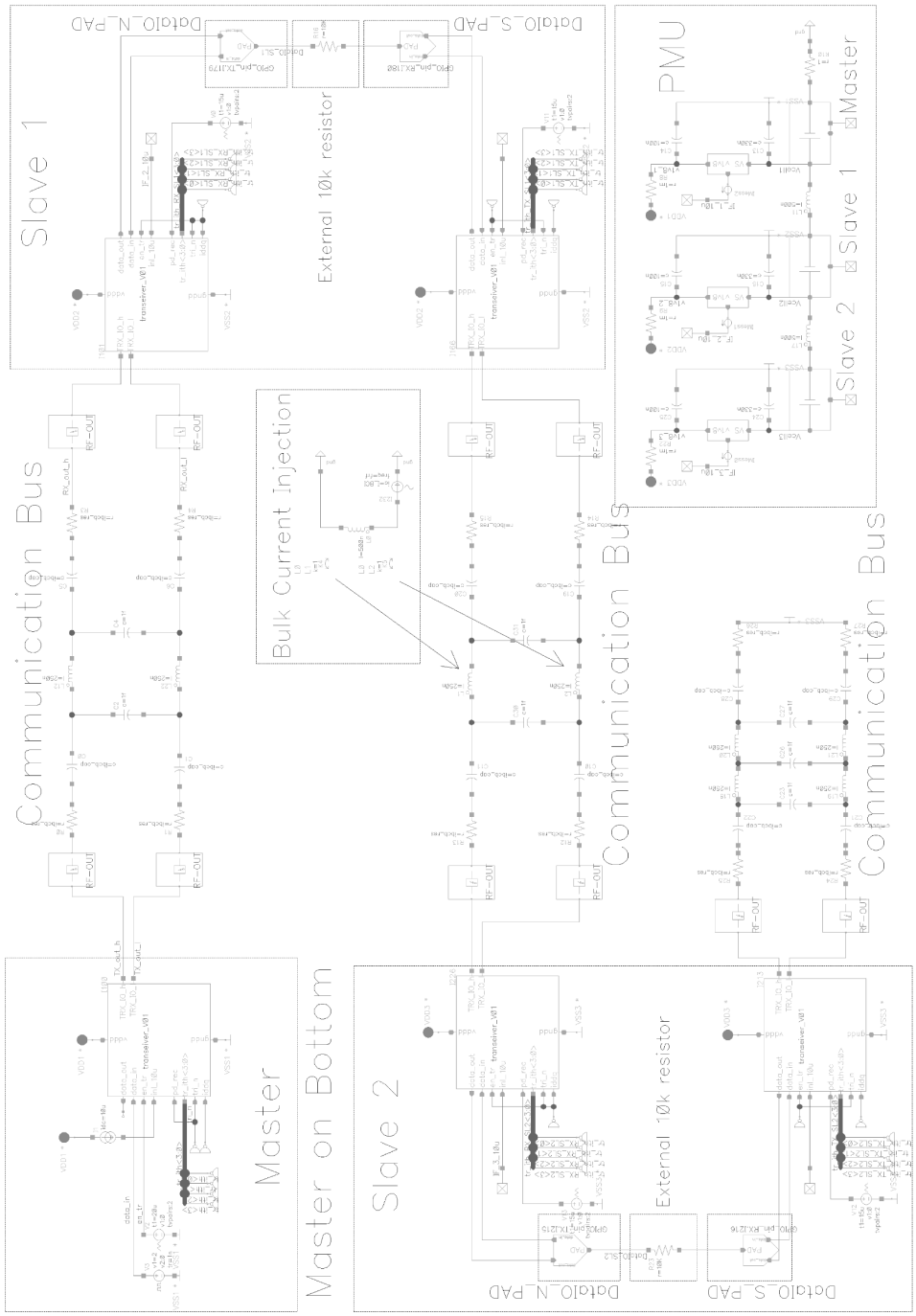

Figure .4: Testbench for BCI test method

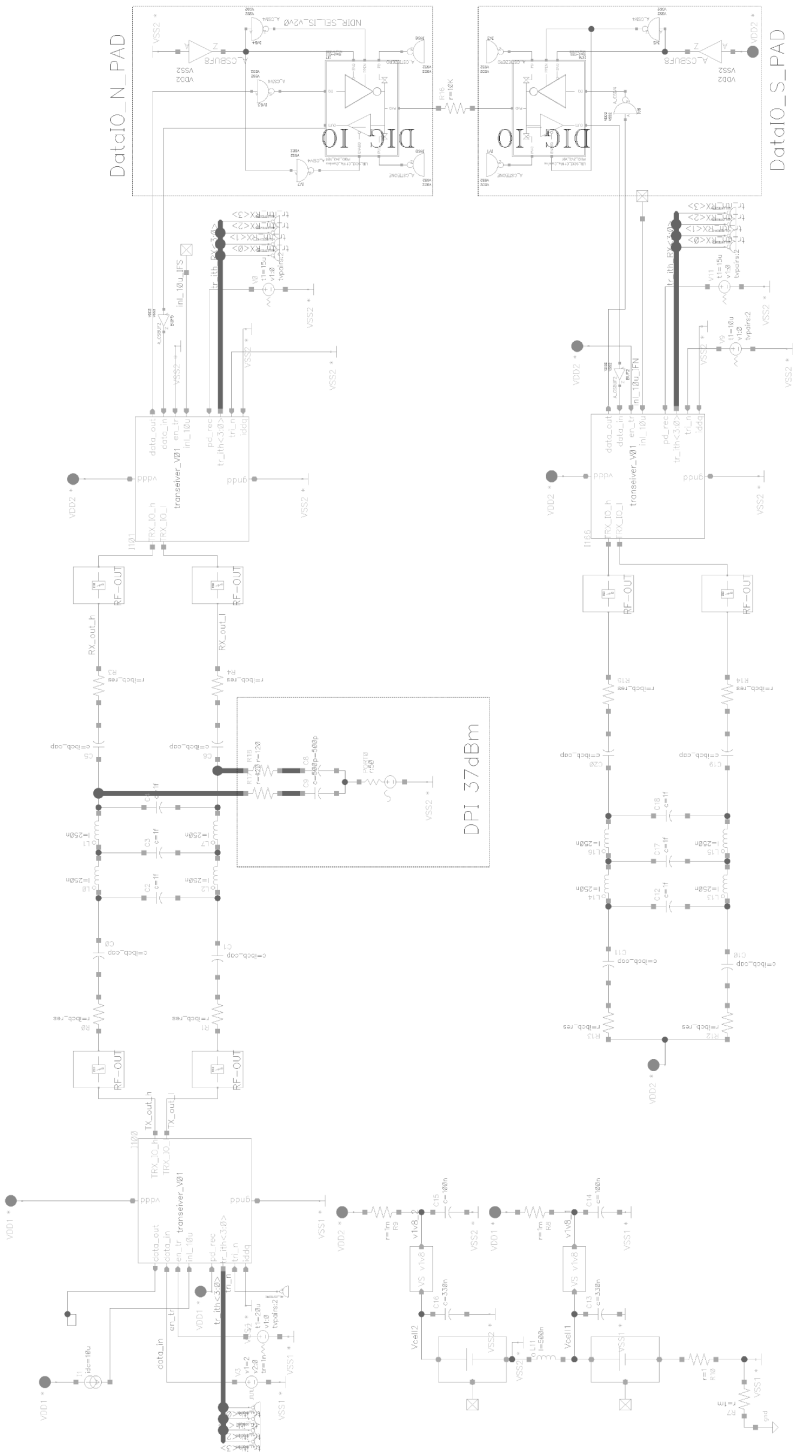

Figure .5: Testbench for DPI test method

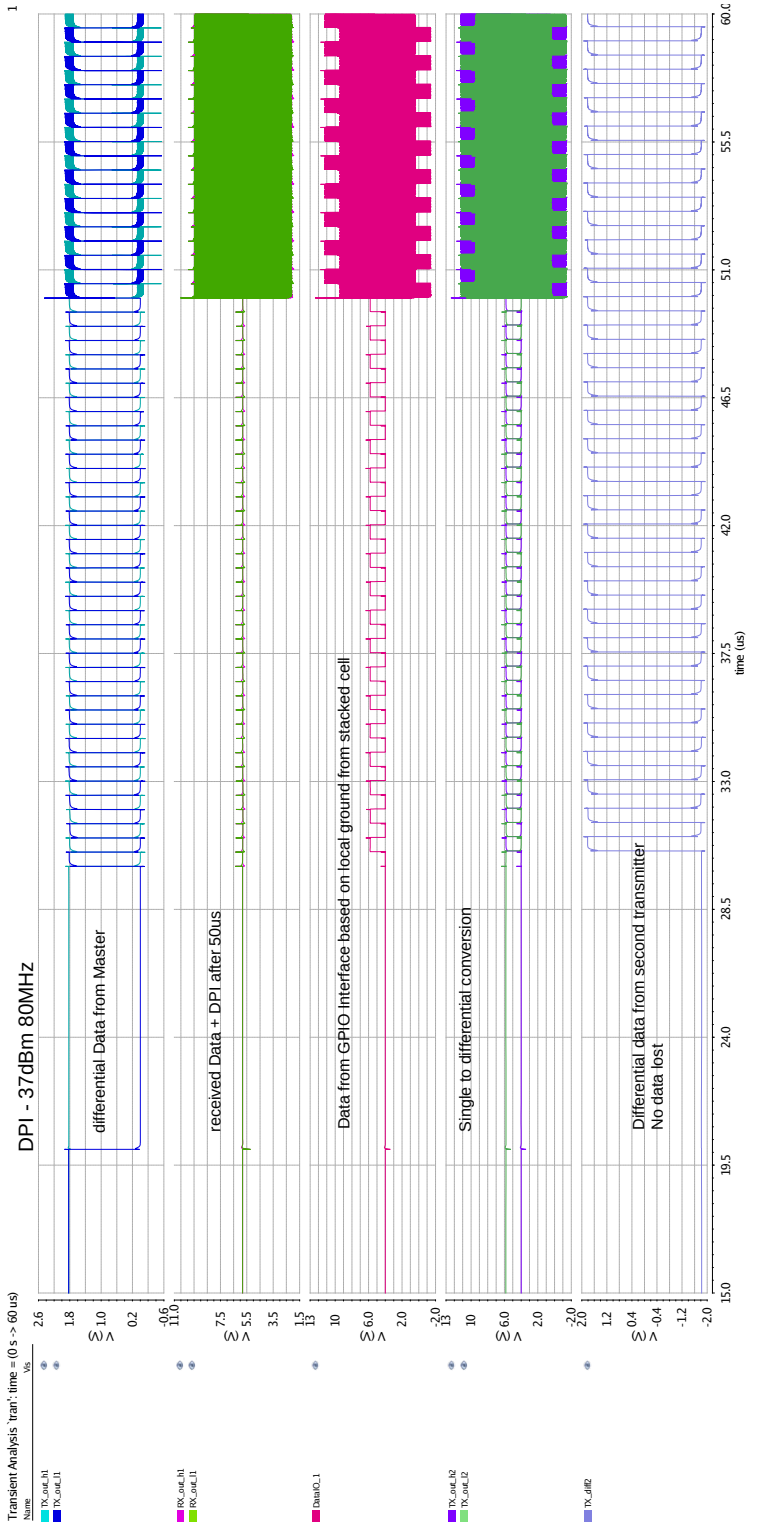

Figure .6: Resimulation of DPI at 80MHz with 37dBm - no failure

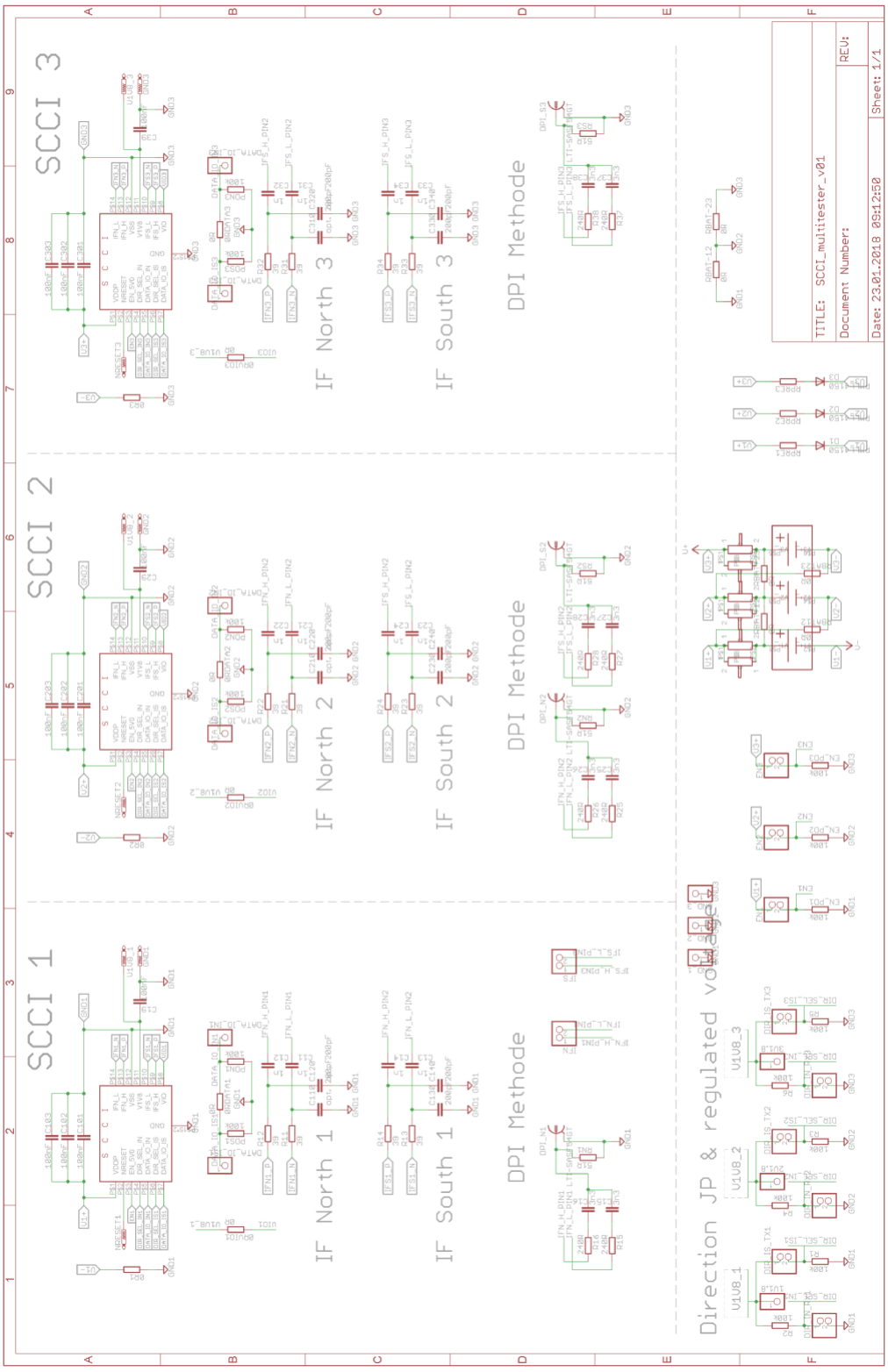

Figure .7: Eagle schematic of the Multicell board

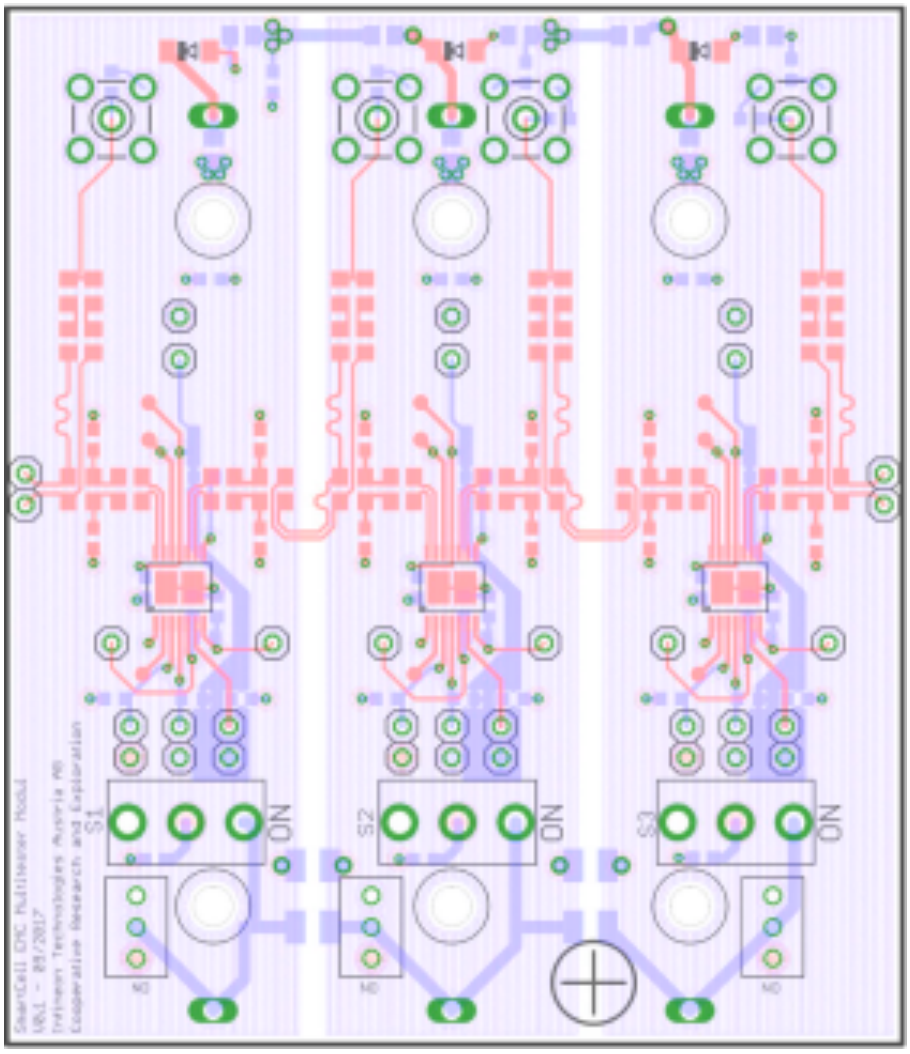

Figure .8: PCB design of the Multicell board

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