Khaled A. Mahafzah, M.Sc.

Design Considerations to Improve the Efficiency of an AC-AC Converter at Low Partial Load

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Supervisor

Univ.-Prof. Dr.-Ing. Annette Mütze

Electric Drives and Machines Institute, Graz University of Technology

External Examiner

Prof. Dr.-Ing. Mario Pacas

Institute for Power Electronics and Electrical Drives, University of Siegen, Germany

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Khaled A. Mahafzah, M.Sc.

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Contents

Zusammenfassung

DC-AC Wechselrichter haben eine breite Palette von Anwendungen in der Industrie gefunden, mit sehr breiten Leistungsbereichen der Lasten. Der Wirkungsgrad dieser Wechselrichter ist für viele Anwendungen ein wichtiger Punkt geworden. Typischerweise werden drei Arten von Verlusten unterschieden: Leitungs-, Schalt- und Ansteuerungsverluste.

Diese Arbeit vergleicht die Leistung der konventionellen dreiphasigen Wechselrichter mit Pulsweitenmodulation (PWM) für Hart schaltend und weich schaltend unter sehr schwacher Last (7 W, 150 mA-Peak, 50 V-Peak). Ein Auxiliary Resonant Commutated Pole Inverter (ARCPI) wurde als Soft switching Topologie f´r diese Arbeit ausgewählt.

Um die Gesamtverluste in jedem Wechselrichter zu berechnen, werden analytische Methoden verwendet. Verschiedene Arten von MOSFETs und IGBTs werden untersucht, um das Optimum für diese Anwendung zu finden. Weiters werden Optionen zur Verbesserung des Wirkungsgrades dieser Wechselrichter gezeigt. Nach Auswahl der passenden Wechselrichtertopologie mit den jeweiligen Halbleiterschaltern wird für diese Anordnung die optimale Zwi-schenkreisspannung gewählt. Dann wird eine Schaltung zur Leistungsfaktorkorrektur (PFC) entworfen, um die Oberschwingungen und die Welligkeit des Eingangswechselstroms zu reduzieren.

Dann werden Möglichkeiten zur Verbesserung des Wirkungsgrades der gesamten Schaltung eingeführt. Mit den entwickelten Algorithmen fr die Berechnung der Verluste des dreiphasigen Wechselrichters und der PFC-Eingangsstufe wird eine Gesamtoptimierung durchgefhrt.

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To my father and mother who taught me to always do my best; your reputation is worth more than a quick profit . . .

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To my beloved wife Saja for being in my life. . .
I love you all

Chapter 1

Thesis Structure and Outline

1.1 Introduction

DC-AC converters have found a wide range of applications within the industry, with wide power ranges of the loads. The energy conversion efficiency of these converters has become aa important point for many applications. Typically, three types of losses are distinguished between: conduction, switching and gate drive or control losses.

This study compares the performance of conventionally controlled Pulse Width Modulation (PWM) three phase Hard and Soft Switching Inverters under very light load (7 W, 150 mA-peak, 50 V-peak). An Auxiliary Resonant Pole Inverter (ARCPI) was selected as soft switching topology for this study.

Analytic methods are used to calculate the total loss in each inverter. Both types of MOSFETs and IGBTs were investigated to select the best fit for this application. Then, options to enhance and improve the efficiency of these inverters are introduced. After selecting the best fit inverter's switching topology with main components of the circuit and the optimized DC link voltage, Power Factor Correction Circuit (PFC) was designed in order to reduce the harmonics and the ripple of the line currents.

Next, the options to improve the efficiency of the overall circuit are introduced. Using the developed algorithms for computing losses of the three phase inverter

and the PFC input stage, an overall optimization was carried out.

1.2 Thesis Structure

This thesis contains seven chapters. The structure of this thesis is summarized as follows:

Chapter 1 Thesis Structure and Outline introduces the thesis structure and briefly gives a general overview of each chapter.

Chapter 2 Hard Switching Inverter Loss Analysis studies the performance of a three phase Hard Switching Inverter (HSI) for low power applications. The total losses of the inverter are computed using analytic methods for different power transistors. While the switching losses of the MOSFETs are computed in the literature in detail, further improvements in the calculation are discussed, resulting in an optimized single phase inverter prototype. The standard hard switching approach is used.

Chapter 3 Soft Switching Inverter Loss Analysis studies the performance of a three phase Soft Switching Inverter under extremely light load conditions. An Auxiliary Resonant Commutated Pole Inverter (ARCPI) has been selected as soft switching topology for this study. An analytic approach is used to compute the losses in this inverter. Finally, the main circuit component (main switches, auxiliary switches and resonant inductor) selection guideline is discussed and presented.

Chapter 4 Power Factor Correction Circuit Loss Analysis: this thesis proposes a new single-phase hybrid bridge-less step down PFC converter. Targeting high energy conversion efficiency, the individual loss components are computed. The proposed PFC is operated under Critical Conduction Mode (CRM) with Constant On Time (COT). This control method reduces the losses caused by the body diode reverse recovery charge of the synchronous switch.

Chapter 5 Efficiency Enhancement introduces the investigated options to enhance the efficiency of all presented topologies which are discussed in detail as follows:

- Hard Switching Inverter. Two suggestions to improve the inverter efficiency are discussed: First, the effect of optimizing the turn on dead time of both switches, the operating and synchronous switches, on the total losses is studied. Second, the potential of gate drive loss reduction using a Resonant Gate Drive (RGD) is investigated.

- Soft Switching Inverter. Several options for enhancing the efficiency of this inverter are discussed. First, this study suggests reducing the losses in the commutation circuit by optimizing the time instants of turning on/off of the auxiliary switches. Second, the loss reduction in the commutation circuit due to skipping one of the auxiliary pulses per switching cycle is presented. Third, this study discusses the losses reduction due to adjusting the boost current according to the load current value. Finally, the potential of using a Resonant Gate Drive (RGD) is investigated to reduce the gate drive losses of the switches.

- Power Factor Correction Circuit. A detail analysis for operating sequences, loss analysis and control requirements are presented. The comparison between the proposed converter and the conventional buck PFC has been carried out. Both converters operate under Boundary Conduction Mode (BCM) or Critical Conduction Mode (CRM). An improved Critical Conduction Mode with Constant On Time has been proposed in order to reduce the switching losses of the PFC.

Chapter 6 Test Setup and Results Validation discusses the test setup and the methods for loss measurements in the following structure:

- Hard switching prototype: The single leg of the three phase inverter is built for results validations. Two prototypes are tested to validate the computations: The first is a single leg prototype using low blocking voltage MOSFETs. The second is a single leg prototype using high blocking voltage MOSFETs. The method for distinguishing between the conduction losses and the switching losses is presented. The effect of the RGD on the total losses is discussed by connecting this circuit to the gate source of the lower switch and checking the results.

- Soft switching prototype: The single leg of the three phase inverter is built for test purposes. High voltage blocking voltage MOSFETs are used as main and auxiliary switches (homogeneous ARCP). Some discussions and waveforms analysis are presented. The losses of this prototype are measured and compared with the computed ones.

- Gate drive losses: Finally, two arrangements are prepared to measure the power saved by the use of RGD. In the case of a standard hard gate drive (including the external gate drive), the losses are compared to the losses in the case of resonant gate drive (including the resonant inductor) at a specific switching frequency. Additionally, the RGD prototype is connected to the hard and soft switching prototypes (connected to the gate source of the lower switch). Then, the conduction plus switching losses of the two inverter topologies are measured for both directions of the load current in order to check the influence of this circuit on conduction plus switching losses.

- Power Factor Correction Circuit prototype: A conventional Buck PFC is built to test the improved Critical Conduction Mode (CRM) with Constant On Time (COT) and to validate the results. The discussion of both DC

and AC measurements and waveforms analysis are presented. The loss measurements are discussed. The proposed step down PFC is left for future work.

Chapter 7 Component Selection of The AC-AC converter presents some tips and recommendations for component selection based based on both technical and economical criteria.

Chapter 8 Discussion, Conclusions and Future Works the conclusions of the work and possible future works are drawn in this chapter.

1.3 The Intention of Testing an Inverter's Single-Leg Prototype

The input power and the output power are both in the same range and the difference between them (the losses) is small in relation to the high-efficiency driving system. To minimize the error in the measurements in both input and output power, the output power is reduced as much as possible. Thus, the input power is in the same range as the output power and equal to the sum of the output power and the losses in the circuit. To realize this, the full bridge inverter is tested and operated under an extremely low difference in the duty cycles between the two legs, resulting in low output power; this setup is presented [C1]. The only drawback of the full bridge is the difficulty to set the difference in the duty cycles of the legs in order to keep the output power low. Thus, the full bridge is replaced by the inverter's single-leg as discussed herein. The single leg of the inverter is operated under the same load current.

1.4 Loss Measurement: Power Analyzer Versus Calorimeter

For loss measurements, the power analyzer (N5000) was used instead of a Calorimeter. The second method requires a long time to reach the thermal equilibrium of the total system; thus, instead of taking the measurement over the voltage range within a few minutes by using N5000, the same measurements will take a few hours using the calorimeter.

1.5 Load Characteristics

In this study, the load is designed for a home appliance application. The rated power of this load is 70 W with 260 V-peak and 310 mA-peak; but this rated power is required only a few times during the life of the application and is, thus, not relevant to the energy consumption. Most of the time, the load operates at partial load, i.e., 7 W, which is 10 % of the thermally maximum permissible power. Operating the inverter under partial load conditions, as an alternative to designing an inverter for low load only and providing overload capabilities, both increases its lifetime and allows the component count to be kept at a minimum, hence, reducing its cost and size.

It should be noticed that, there is an extremely wide range efficiency of the driving systems these days. A wide range of load conditions is also available, depending on the application. However, the load in this Ph.D. thesis is lower than that found in the literature. Hence, dealing with this light load itself is one of the novelties of this thesis in addition to the discussed options to enhance the efficiency in the thesis.

1.6 New Contributions in this Thesis

The following contributions are made:

- The driving system is designed for an extremely light load application. See Section 1.5.

- The loss computations of the hard switching inverter are reviewed in detail both for MOSFETs and IGBTs. The computations of the switching losses of MOSFETs have been improved. The potential of applying two suggestions to improve the efficiency of such an inverter is investigated. First, the effect of optimizing the turn on dead time of both switches, the operating and synchronous switches, on the total losses is studied. Second, the potential of gate drive losses reduction by using a Resonant Gate Drive (RGD) is investigated.

- Several options for improving the efficiency of the Auxiliary Resonant Commutated Pole Inverter (ARCPI) are proposed. First, this study suggests the reduction of losses in the commutation circuit by optimizing the time instants of the turning on/off of the auxiliary switches. Second, the loss reduction in the commutation circuit due to skipping one of the auxiliary pulses per switching cycle is presented. Third, this study discusses the losses reduction due to adjusting the boost current according to the load current value. Finally, the potential of using a Resonant Gate Drive (RGD) is investigated to reduce the gate drive losses of the switches.

- A new single-phase hybrid step-down PFC converter is proposed. The proposed PFC is forced to operate under Critical Conduction Mode (CRM) with Constant On Time (COT) in order to reduce the switching loss. Moreover, this operating method has been improved by keeping the synchronous switch conduct a bit longer than it should be. In standard CRM, the synchronous

switch is gated off when the inductor current hits zero. In an improved CRM with COT, the synchronous switch keeps conducting for longer than it does in the standard CRM. Allowing the inductor current decreases to boost value and stores some energy in the inductor. At this instant the aynchronous switch is gated off and the resonance between the inductor and the non-linear capacitance starts. At the end of the resonance period, the operating switch is gated on under ZVS. Furthermore, an additional signal has been added to the constant conduction time (T_{on}), further improving the Power Factor (PF) and reducing the total harmonics distortion (THD) of the line power.

- The performances of the three circuits have been experimentally validated.

1.7 List of Publications

The work presented in this thesis has resulted in the following conference publications:

[**C1**] K. A. Mahafzah, K. Krischan and A. Muetze, "Efficiency Enhancement of a Three Phase Hard Switching Inverter Under Light Load Conditions", *IECON 2016*, pp. 3372 - 3377, October 2016.

[**C2**] K. A. Mahafzah, K. Krischan and A. Muetze, "Efficiency Enhancement of a Three Phase Soft Switching Inverter Under Light Load Conditions", *IECON 2016*, pp. 3378 - 3383, October 2016.

Chapter 2

Hard Switching Inverter Loss Analysis

2.1 Introduction

DC - AC converters have found many different applications in the industry with a wide range of loads. Often, the energy conversion efficiency of these converters has become a key point. Typically, three types of losses are distinguished between: conduction, switching and gate drive or control losses [1]. A well-known and established topology, conventional Pulse Width Modulation controlled three phase Hard Switching Inverter (HSI), used for extremely light load conditions is discussed in this study.

Many researchers have already studied HSIs intensively under different loads, showing the importance of the topology in their papers: In [2], the authors evaluated the circuit under small load by employing high voltage IGBTs which are used in mid power applications under a small load conditions of 10 % to 20 % of the inverter's nominal load. In [3], a three phase voltage source inverter, a PV grid-tie micro-inverter (with three different topologies of inverters) was studied and tested under low load. MOSFETs were used and the losses were calculated to compare the performances of the different topologies. In [4], a relatively high load of 4 kW was fed by hard and soft switching topologies to compare the efficiencies

between these two inverters. High voltage IGBTs were used for evaluation. Another comparison between hard and soft switching inverters for a load of 100 kVA was introduced in [5] in which 1200 V, 300 A IGBTs were selected.

In [6], the losses in the hard and soft switching inverters were estimated by developing a practical simulator. IGBTs were used in the topologies to feed a load of 5 kW. In [7], the authors evaluated and compared the switching losses and on state voltages of different high voltage (2.5 - 6.5 kV) IGBTs and 3.3 kV IEGTs at different conditions (voltages, currents and temperatures) for different topologies, e.g., hard switching and soft switching topologies. A 95 % efficiency has been achieved at 5 kHz switching frequency.

While these studies discussed the HSIs for different load ranges using different switches, further research is needed to fill the gaps–e.g, extremely light load range with high overload capability, more detail in the losses computation and suggestions to improve the HSI efficiency–between this research and the previous works.

In this chapter, this type of inverter designed for extremely light load at 10 % of its thermally rated power is investigated and optimized with a special focus on the very light load application. The efficiency of such an inverter needs to be carefully computed and discussed; hence, the different loss types are discussed in detail, and approaches for circuit optimization are investigated, thereby expanding the previous works.

First, the mathematical model of the losses is discussed in detail. Previous switching loss computations are improved for MOSFETs. Then, this mathematical model is used to compare the losses in case of using a conventional half bridge gate driver which introduces fixed delay time with the case of adjusting the delay times in both switching transitions (turn on the operating and synchronous switches). Taking advantage of this mathematical model, the best fit switch for this application is selected.

This inverter is designed for driving the load which has been described in Section 1.5. It should be noticed that, the inverter, optimized in such a way, needs to be able to drive the rated load continuously. The best fit switches of the inverter can drive the load at rated power. As the inverter is located in close proximity to the motor, no output filter is considered.

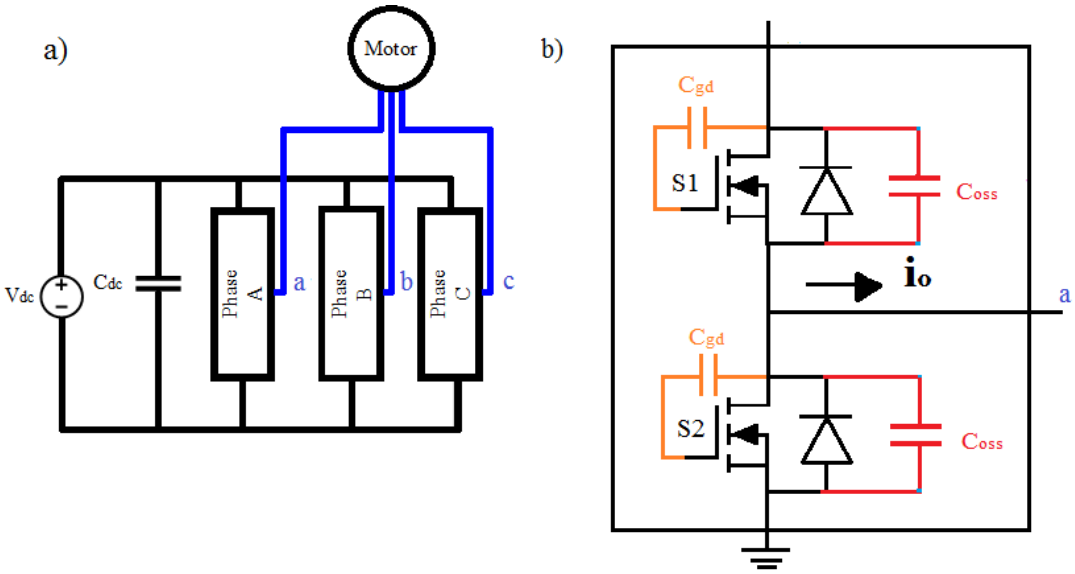


Figure 2.1: a) A three phase hard switching inverter, each phase contains the arrangement shown in part (b) of this figure. b) Single phase of a three phase hard switching inverter with some parasitic capacitances of the MOSFET. For each phase, a from (a) is connected to a (b).

2.2 HSI Loss Analysis

In this section, the computation of the loss components is explained. The losses are computed for a single leg of a three phase HSI, as shown in Figure 2.1a, because the three phase HSI is composed of three identical legs and operated with symmetrical load as shown in Figure 2.1b. As mentioned above, the losses in the HSI are divided into conduction losses, switching losses and gate drive losses.

The most relevant components of a single leg of a three phase HSI that are used in the next analysis are illustrated in Figure 2.1b. They comprise the DC link capacitor (C_{dc}) and the two power switches (S_1 and S_2) (here, MOSFETs,

but these can also be replaced by IGBTs with internal or external anti-parallel diodes). Also, it shows the two most relevant parasitic capacitances (C_{gd}, C_{oss}).

In the analysis, the following nomenclature is used for both types of switches (MOSFET and IGBT):

- R_{on} denotes the on-state resistance for the MOSFETs (R_{dson}) and the differential resistance for the IGBTs (R_{ce}). R_{f}, R_{L} symbolize the differential resistance of the body diode and the internal DC resistance of the inductor, respectively.

- The voltage across the semiconductor device (diode or the channel of the switch) is symbolized by V_{x}. It is a combination of the on voltage at zero current plus the multiplication of the differential resistance and the current (I_{x}) passing through the device. ($V_{\mathrm{f}} + R_{\mathrm{f}} I_{\mathrm{x}}$ for diodes, $V_{\mathrm{ce}} + R_{\mathrm{ce}} I_{\mathrm{x}}$ for IGBTs and $0 + R_{\mathrm{dson}} I_{\mathrm{x}}$ for MOSFETs.)

- The current drawn by the load within n^{th} switching cycle is denoted by $i_{\mathrm{o\text{-}n}}$ and it is assumed to be constant during this switching cycle.

- The switching losses are not affected by the ripple in the load current, because the components of the switching losses that are influenced by the load current is much lower than the component that is influenced by the capacitances.

Due to the symmetry of i_{o} (sinusoidal load current), the energy losses are calculated for the positive half of the fundamental period, then, averaged over half of the fundamental period.

2.2.1 Conduction Losses

The conduction losses (on-state losses) are the losses caused by R_{on}, V_{on} , V_{f}, R_{f} and i_{o}. The energy dissipated in the operating switch for one load current direction,

e.g., positive load current, within one switching cycle (T_s) with duty cycle (D_n) in switching period number n are given respectively by [8, 9]:

$$E_{\mathrm{condS1\text{-}n}} = (V_{\mathrm{on1}} + R_{\mathrm{on1}} i_{\mathrm{o\text{-}n}}) i_{\mathrm{o\text{-}n}} D_\mathrm{n} T_\mathrm{s} \tag{2.1}$$

For low load current, the body diode will not conduct as long as ($R_{\mathrm{on}} i_{\mathrm{o\text{-}n}} < V_\mathrm{f}$) and the channel of the MOSFET is gated on. The conduction loss in the synchronous switch is given by:

$$E_{\mathrm{condS2\text{-}n}} = (V_{\mathrm{f2}} I_{\mathrm{D2}} + R_{\mathrm{f2}} I_\mathrm{D}^2 + V_{\mathrm{on2}} I_{\mathrm{CH2}} + R_{\mathrm{on2}} I_{\mathrm{CH2}}^2)(1 - D_\mathrm{n}) T_\mathrm{s} \tag{2.2}$$

where I_{D2} is the current passes through the body diode, I_{CH2} is the current passes through the channel of the synchronous switch. Assuming parallel conduction between the body diode and channel of the MOSFET, those currents are given by, respectively:

$$I_{\mathrm{D2}} = \frac{R_{\mathrm{on2}}(i_{\mathrm{o\text{-}n}} + \Delta i_{\mathrm{o\text{-}n}}) - V_{\mathrm{f2}}}{R_{\mathrm{on2}} + R_{\mathrm{f2}}} \tag{2.3}$$

$$I_{\mathrm{CH2}} = \frac{V_{\mathrm{f2}} + R_{\mathrm{f2}}(i_{\mathrm{o\text{-}n}} + \Delta i_{\mathrm{o\text{-}n}})}{R_{\mathrm{on2}} + R_{\mathrm{f2}}} \tag{2.4}$$

where $\Delta i_{\mathrm{o\text{-}n}}$ is the ripple in the load current. The conduction losses are influenced by Δi_o where the RMS ripple current is approximated by:

$$\Delta i_{\mathrm{o\text{-}n\text{-}rms}} = \frac{V_\mathrm{dc} D_\mathrm{n} (1 - D_\mathrm{n}) T_\mathrm{s}}{\sqrt{12} L} \tag{2.5}$$

where L is the load inductance. (2.1) and (2.2) can be rewritten as:

$$E_{\mathrm{condS1\text{-}n}} = (V_{\mathrm{on1}} i_{\mathrm{o\text{-}n}} + R_{\mathrm{on1}} (i_{\mathrm{o\text{-}n}}^2 + \Delta i_{\mathrm{o\text{-}n\text{-}rms}}^2)) D_\mathrm{n} T_\mathrm{s} \tag{2.6}$$

$$E_{\text{condS2-n}} = \begin{cases} (V_{\text{on2}} i_{\text{o-n}} + R_{\text{on2}}(i^2_{\text{o-n}} + \Delta i^2_{\text{o-n-rms}}))(1 - D_{\text{n}})T_{\text{s}} & \text{CH. only} \\ (V_{\text{f2}} i_{\text{o-n}} + R_{\text{f2}}(i^2_{\text{o-n}} + \Delta i^2_{\text{o-n-rms}})(1 - D_{\text{n}})T_{\text{s}} & \text{BD. only} \\ (V_{\text{f2}} I_{\text{D2}} + R_{\text{f2}} I^2_{\text{D}} + V_{\text{on2}} I_{\text{CH2}} + R_{\text{on2}} I^2_{\text{CH2}})(1 - D_{\text{n}})T_{\text{s}} & \text{Paral. Cond} \end{cases} \quad (2.7)$$

The conduction losses are given by (N switching cycles per $0.5/f_{\text{mod}}$) [10]:

$$P_{\text{cond}} = \; 2 f_{\text{mod}} \sum_{n=1}^{N} (E_{\text{condS-n}} + E_{\text{condD-n}}) \,. \quad (2.8)$$

2.2.2 Switching Losses

Switching Losses of the MOSFETs

The switching losses in a power MOSFET depend on its transient behavior, i.e., its turn on (T_{on}) and turn off (T_{off}) times. The times are stated in the data sheet of power MOSFETs for specific nominal conditions (e.g., drain current, drain to source voltage, etc.), see Table 17 in [11] for an example. If the load changes, these times need to be scaled. So that:

$$T_{\text{on-new}} \;\; = \;\; t_{\text{ri-new}} + t_{\text{fv-new}} \quad (2.9)$$

where $t_{\text{ri-new}}$ denotes the scaled current rise time and $t_{\text{fv-new}}$ denotes the scaled voltage fall time at turn on. The general equation for calculating the nominal rise time t_{rn} (at nominal load current) is given by [8, 12–14]:

$$t_{\text{rn}} \;\; = \;\; R_{\text{g}} C_{\text{iss}} \ln\left(\frac{V_{\text{dr}} - V_{\text{th}}}{V_{\text{dr}} - V_{\text{gp}}}\right) \quad (2.10)$$

$$t_{\text{ri-new}} \;\; = \;\; \frac{t_{\text{rn}}}{I_{\text{n}}} i_{\text{o-n}} \quad (2.11)$$

where (2.11) scales for the actual switch current, R_{g} is the total (internal plus external, if included) gate resistance, C_{iss} is the input capacitance of one MOSFET, V_{dr} is the actual driving voltage applied to the gate, V_{th} is the threshold voltage, V_{gp} is the gate plateau voltage (dependence on i_{o} is neglected) and I_{n} is the nominal drain to source current.

For MOSFET [15], the computed $t_{\text{ri-new}}$ is 0.5 ns when the drain current is 150 mA, whereas, the computed nominal rise time is 12.2 ns when the drain current is 3.6 A. The new rise time is about 4.3 % of the nominal rise time when the load current is 4.2 % of the MOSFET's nominal current.

To calculate $t_{\text{fv-new}}$, the gate current during this time must be calculated [14]:

$$I_{\mathrm{gon}} = \frac{V_{\mathrm{dr}} - V_{\mathrm{gp}}}{R_{\mathrm{g}}} \tag{2.12}$$

Then, the new voltage fall time at turn on is given by (based on [8]):

$$t_{\text{fv-new}} = \frac{Q_{\mathrm{gd}}(V_{\mathrm{dc}}) - Q_{\mathrm{gd}}(V_{\mathrm{dc}})(R_{\mathrm{on}} i_{\text{o-n}})}{I_{\mathrm{gon}}} \tag{2.13}$$

where (2.13) scales for the actual driving voltage, $Q_{\mathrm{gd}}(V_{\mathrm{dc}})$ denotes the accumulative gate-drain charge, which can be calculated by integrating the gate drain capacitance C_{gd} over V_{dc} [16–18], where:

$$Q_{\mathrm{gd}}(V_{\mathrm{dc}}) = \int_0^{V_{\mathrm{dc}}} C_{\mathrm{gd}}(v)dv \tag{2.14}$$

The energy drawn from the dc-link due to the reverse recovery of the bottom MOSFET body diode is given by [8, 10]:

$$E_{\text{onrr-n}} = Q_{\mathrm{rr}} \frac{i_{\text{o-n}}}{I_{\mathrm{n}}} V_{\mathrm{dc}} \tag{2.15}$$

where Q_{rr} is the reverse recovery charge at nominal load current. This amount of energy is dissipated within the bottom MOSFET body diode and partly dissipated

in the upper MOSFET channel.

The energy drawn from the DC link voltage due to charging the output capacitance is estimated:

$$E_{\text{oss-n}} = Q_{\text{oss}}(V_{\text{dc}})V_{\text{dc}} \tag{2.16}$$

where Q_{oss} is the charge of the MOSFET's output capacitance (C_{oss}). This charge can be estimated by integration of the output capacitance over the DC link voltage [14, 17, 18]:

$$Q_{\text{oss}}(V_{\text{dc}}) = \int_0^{V_{\text{dc}}} C_{\text{oss}}(v)dv \tag{2.17}$$

This amount of energy is partly dissipated in the upper MOSFET channel and partly stored in the bottom MOSFET output capacitance (which is later dissipated during turn on of the bottom MOSFET). The same amount, as the latter part, is dissipated within the upper MOSFET as it discharges its output capacitance during the voltage fall time.

The switching on energy during the voltage fall time of the upper MOSFET caused by the output current can be calculated by integrating the power over $t_{\text{fv-new}}$, this is given by:

$$E_{\text{onMv-n}} = \int_0^{t_{\text{fv-new-n}}} v_{\text{ds}}(t)i_{\text{o-n}}dt \tag{2.18}$$

where $v_{\text{ds}}(t)$ is the drain source voltage of the switch and it is assumed that, this voltage is linearly increases over time.

Also, the switching on energy during the current rise time $t_{\text{ri-new}}$ of the upper MOSFET is given by (assuming constant voltage and linear current change):

$$E_{\text{onMi-n}} = \frac{1}{2}V_{dc}i_{\text{o-n}}t_{\text{ri-new-n}} \tag{2.19}$$

Then, the energy losses dissipated within the half bridge at turn on of the upper MOSFET is given by:

$$E_{\text{onM-n}} = E_{\text{onMi-n}} + E_{\text{onMv-n}} + E_{\text{onrr-n}} + E_{\text{oss-n}} + E_{\text{add}} \tag{2.20}$$

where E_{add} is the energy losses caused by the parasitic capacitance of the load, which is discussed in Sections 6.1.1 and 6.1.4 in more detail. To estimate this charge the two pulse test has been applied to the circuit shown in Figure 2.1b and measure the drain currents of both switches. The difference between S_1 drain current and S_2 drain current gives the parasitic charge of the load.

The same procedure is followed to calculate the switching losses at turn off of the upper MOSFET:

$$T_{\text{off-new}} = t_{\text{fi-new}} + t_{\text{rv-new}} \tag{2.21}$$

where $t_{\text{fi-new}}$ denotes the scaled current fall time and $t_{\text{rv-new}}$ denotes the scaled voltage rise time at turn off [8, 12–14]. Then:

$$t_{\text{fn}} = R_{\text{g}} C_{\text{iss}} \ln \frac{V_{\text{gp}}}{V_{\text{th}}} \tag{2.22}$$

$$t_{\text{fi-new}} = \frac{t_{\text{fn}}}{I_{\text{n}}} i_{\text{o-n}} \tag{2.23}$$

where (2.23) scales for the actual switch current. The gate current during $t_{\text{rv-new}}$ is given by [14]:

$$I_{\text{goff}} = \frac{V_{\text{gp}}}{R_{\text{g}}} \tag{2.24}$$

The new voltage rise time at turn off (based on [8]) is:

$$t_{\text{rv-new}} = \frac{Q_{\text{gd}}(V_{\text{dc}}) - Q_{\text{gd}}(V_{\text{dc}})(R_{\text{on}} i_{\text{o-n}})}{I_{\text{goff}}} \tag{2.25}$$

where $Q_{\text{gd}}(V_{\text{ds}})$ is found using (2.14).

The switching off energy during the voltage rise time of the upper MOSFET is calculated by integrating the power over $t_{\text{rv-new}}$:

$$E_{\text{offMv-n}} = \int_0^{t_{\text{rv-new-n}}} v_{\text{ds}}(t) i_{\text{o-n}} dt \tag{2.26}$$

where $v_{\text{ds}}(t)$ is the drain source voltage of the switch and it is assumed that, this voltage is linearly increases over time.

The switching off energy during the current fall time $t_{\text{fi-new}}$ of the upper MOSFET is given by (assuming constant voltage and linear current change):

$$E_{\text{offMi-n}} = \frac{1}{2} V_{\text{dc}} i_{\text{o-n}} t_{\text{fi-new-n}} \tag{2.27}$$

Then, the energy losses dissipated within the single leg of the HSI at turn off the upper MOSFET is given by:

$$E_{\text{offM-n}} = E_{\text{offMi-n}} + E_{\text{offMv-n}} + E_{\text{oss-n}} \tag{2.28}$$

Then, the total switching energy for the single leg for switching cycle n is given by:

$$E_{\text{sw-n}} = E_{\text{onM-n}} + E_{\text{offM-n}} \tag{2.29}$$

The switching power losses are given by (with N switching cycles per $0.5/f_{\text{mod}}$) [10]:

$$P_{\text{sw}} = 2 f_{\text{mod}} \sum_{n=1}^{N} E_{\text{sw-n}} \tag{2.30}$$

Switching Losses of the IGBTs

In this study, the switching losses in the IGBTs are calculated based on Figures 13, 14 and 16 from the data sheet [19], where the figures represent the relationships between the switching losses and collector current, gate resistor and collector emitter voltage, respectively. All these relations show approximately linear dependencies between the IGBT's switching energy and $i_{\text{o-n}}$, R_{g} and V_{dc}. The switching energy for the single leg of the inverter per one switching cycle is given by [9]:

$$E_{\text{sw-n}} = \frac{E_{\text{n}}(K_{\text{i}} i_{\text{o-n}} + C_{\text{i}})(K_{\text{R}} R_{\text{g}} + C_{\text{R}})(K_{\text{V}} V_{\text{dc}} + C_{\text{V}})}{E_{\text{oi}} E_{\text{or}} E_{\text{ov}}} \tag{2.31}$$

where:

- K_{i}, K_{R} and K_{V} describe the slope of the E_{ts} line from the aforementioned Figures 13, 14, and 16 of [19], respectively.
- C_{i}, C_{R} and C_{V} describe the constant values of the E_{ts} line from the aforementioned Figures 13, 14, and 16 of [19], respectively.
- E_{oi}, E_{or} and E_{ov} describe energies at nominal conditions taken from the aforementioned Figures 13, 14, and 16 of [19], respectively.
- E_{n} is the total switching losses at nominal conditions.

Then, the switching losses for the single leg are calculated using (2.30).

2.2.3 Gate Drive Losses

The gate drive losses are the losses dissipated in the gate resistance (internal plus external, if included) due to the charging/discharging of the input capacitance of the power switch. The gate drive loss energy for single switch is given by:

$$E_{\text{g-S}} = Q_{\text{gt}} \frac{V_{\text{dr}}^2}{V_{\text{qg}}} f_{\text{s}} \tag{2.32}$$

where, Q_{gt} is the total gate charge at voltage V_{qg} as given in the data sheet, V_{dr} is the actual driving voltage. The dependence of total gate charge on the drain source voltage of the switch is neglected.

Thus, the power losses for the two power switches in the single leg of the inverter are approximated by [8, 9]:

$$P_{\mathrm{gt}} = 2E_{\mathrm{g\text{-}S}}f_{\mathrm{s}} \tag{2.33}$$

Chapter 3

Soft Switching Inverter Loss Analysis

3.1 Introduction

In industrial applications, the energy conversion efficiency of power electronics systems has commonly been a matter of utmost importance. Targeting efficiency requires taking all losses in a power circuit into consideration. The losses are commonly divided into three components: conduction, switching and gate drive losses [1].

The Auxiliary Resonant Commutated Pole Inverter (ARCPI), proposed in [20] and shown in Figure 3.1, is one of the soft switching topologies. Many studies have discussed an ARCPI in detail and various enhancements have been introduced to improve this inverter's performance (e.g., [21, 22]).

Most studies conducted on ARCPIs focus on applications with relatively high loads. For example, in [23], the operation of an ARCPI was reviewed and the losses were estimated analytically. This inverter was simulated under the assumption that the load current was 26 A-peak and the DC link voltage was 300 V. In [24], the design of an ARCPI was reviewed for an AC drive as the target application, in which the design data were as follows: The load current was 20 A-peak and DC link voltage was 200 V. In [25], an ARCPI had been designed for a 3.3 hp

brushless DC motor drive system. In [7], the authors evaluated and compared the switching losses and the on state voltages of different high voltage (2.5 - 6.5 kV) IGBTs and 3.3 kV IEGTs at different conditions (voltages, currents and temperatures) for different topologies, e.g., hard switching and soft switching topologies, ultimately achieving 95 % efficiency at 5 kHz switching frequency. Finally, in [26], a new modulation strategy was introduced to reduce the losses in the auxiliary circuit during commutation process. A 10 kW/16 kHz ARCP prototype was built to validate the results. Furthermore, showing the importance of operating the inverters under different partial loads, [27, 28] study the efficiency of different inverter topologies with various control schemes. In these works, the efficiencies are computed and measured for both rated and partial load conditions.

Considering the results presented this far, more research is needed to address the specific requirements of extremely light load ranges, at which the system operates for a majority of the time, but with high long-term capable overload capability. See Section 1.5.

This thesis proposes three different options for reducing the losses of the ARCPI's commutation circuit. These options all prove to effectively reduce the commutation circuit losses, increasing the inverter efficiency by up to 2 %, which is considered significant, given the application's sensitivity towards the overall system's efficiency.

1. A new switching sequence is presented in which both auxiliary switches are gated on simultaneously and turned off sequentially. Figure 3.2b shows the proposed switching sequence in contrast to Figure 3.2a which depicts the conventional switching sequence. This new proposal can essentially offset the effect of the reverse recovery charge of the body diodes of the auxiliary switches (in case of MOSFETs). Moreover, since the conducting channel is parallel to the body diode, the conduction losses in the auxiliary switches are reduced, hence, reducing the commutation losses.

2. These commutation losses are further reduced by initiating a resonant commutation cycle only every second output voltage transition. Voltage transitions initiated by turning off the previously forward conducting main switch are soft, as the main switch's non-linear output capacitances act as snubber capacitors.

3. The ARCPI total losses are reduced by adjusting the boost current according to the sinusoidal load current.

4. The Resonant Gate Drive circuit's (RGD) potential has been tested to reduce the gate drive losses of the switches. Moreover, the effect of the RGD on the inverter's total loss is studied.

In contrast to [22, 25, 26, 29, 30], the commutation losses in this paper are reduced without introducing any extra circuitry. Thus, they keep the commutation circuit simple. Moreover, in contrast to [22], in which MOSFETs are also used as auxiliary switches. The evaluation conditions are $V_{\mathrm{dc}} = 60\,\mathrm{V}$ and $i_{\mathrm{o}} = 5\,\mathrm{A}$, but only for testing purposes, and a second prototype has been built with rated power of $P_{\mathrm{o}} = 8.9\,\mathrm{kW}$ and $i_{\mathrm{o}} = 30\,\mathrm{A}$, the work presented here studies their use for extremely light load conditions.

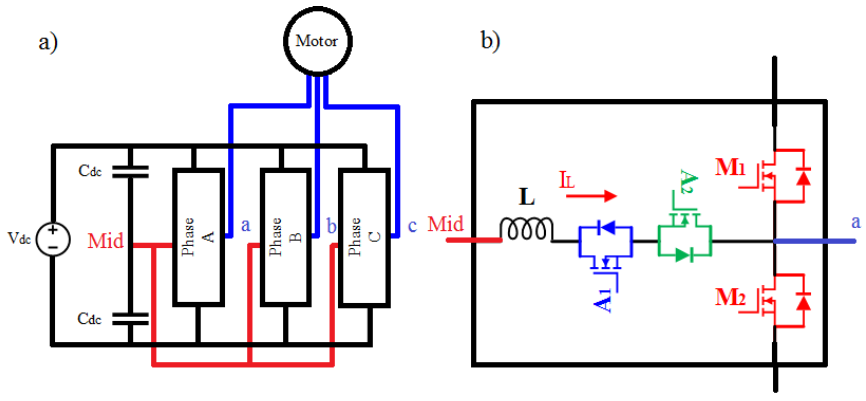


Figure 3.1: a) An Auxiliray Resonant Commutated Pole Inverter [20], each phase contains the arrangement shown in part (b) of this figure. b) Single phase of an Auxiliray Resonant Commutated Pole Inverter (Auxiliary Resonant Commutated Pole, ARCP). For each phase, a and Mid from (a) are connected to a and Mid from (b), respectively.

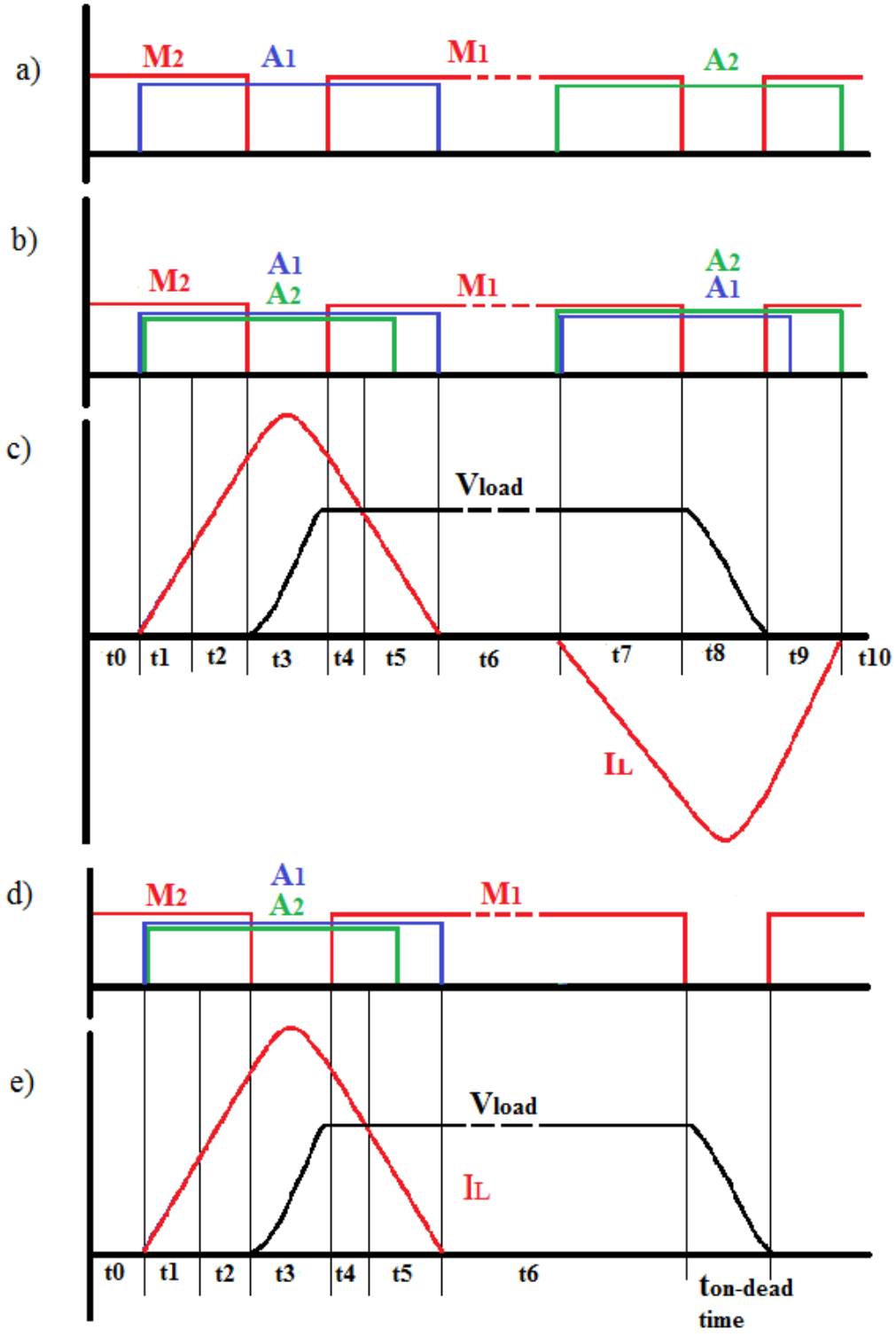


Figure 3.2: Switching sequence per switching cycle: a) Conventional switching of ARCP, b) Proposed switching of ARCP. c) The load voltage (V_{load}) and the inductor current I_{L}. The switching sequence per switching cycle applying option 2, positive load current direction: d) The proposed switching of ARCP under option 2. e) The load voltage (V_{load}) and the inductor current I_{L}.

3.2 ARCPI Operating Sequences

This section discusses the ARCPI operating sequences based on the suggested switching sequences. The three phase ARCPI is composed of three identical legs and operated with a symmetrical load as shown in Figure 3.1a. The structure of the legs is illustrated in Figure 3.1b. Unless otherwise specified, all reference is made to the full three-leg inverter or a quantity related to it (such as the power), all discussions, such as the operating sequences and the loss computations, are presented for a single leg of an ARCPI (an Auxiliary Resonant Commutated Pole, ARCP) as illustrated in Figure 3.1b.

In the analysis, the previously mentioned nomenclatures in Section 2.2 are used in the here presented analysis. It should be noticed that, the equations in the following subsection are based on the homogeneous ARCP using MOSFETs only, but they can easily be extended for IGBTs.

The current drawn by the load is symmetrical in the positive and the negative half cycles of the fundamental period, so the energy losses are calculated for the positive half wave only. Then, they are averaged over half of the fundamental period.

The ARCP has ten operating sequences within one switching period [20, 29, 31]. Figure 3.2a shows the conventional switching sequence for all the switches per one switching cycle whereas Figure 3.2b illustrates the proposed switching sequence for all the switches per one switching cycle of this inverter. Figure 3.2c shows the load voltage V_{load} and the inductor current I_{L}. For each sequence, Table 3.1 summarizes the state of all the semiconductors and the equation numbers for the inductor current and the time period. Table 3.1 also shows the resistance and the driving voltages for the resonant inductor current differential equations.

It should be noticed that, the semiconductor devices change their switching states per sequences within one switching cycle, thus, each sequence has been analyzed and justified in detail.

- Sequence 1, period t_1: The lower main switch M_2 and both auxiliary switches A_1, A_2 are gated on. M_2 and A_2 are conducting in reverse direction and A_1 is conducting in forward direction. Applying Kirchhoff's voltage law (KVL) through the loop results in:

$$\frac{-V_{\mathrm{dc}}}{2} + V_{\mathrm{xa1}} - V_{\mathrm{xa2}} + I_{\mathrm{L1}}R_{\mathrm{L}} + L\frac{dI_{\mathrm{L1}}}{dt} + V_{\mathrm{xm2}} = 0 \tag{3.1}$$

where $V_{\mathrm{xm2}} = (I_{\mathrm{L1}} - i_{\mathrm{o\text{-}n}})R_{\mathrm{onm2}}$ (in case of MOSFET). Rearranging this equation yields:

$$L\frac{dI_{\mathrm{L1}}}{dt} + R_{\mathrm{t1}}I_{\mathrm{L1}} = V_{\mathrm{t1}} \tag{3.2}$$

As discussed in Section 2.2, the body diodes of A_2 and M_2 might not conduct ($R_{\mathrm{on}}i_{\mathrm{o\text{-}n}} < V_{\mathrm{f}}$, which is not the case when $i_{\mathrm{o\text{-}n}}$ is replaced by the boost current $I_{\mathrm{b\text{-}n}} = 3.5i_{\mathrm{o}}$), so that R_{t1} and V_{t1} are found in switching cycle number n, as summarized in Table 3.1:

$$R_{\mathrm{t1}} = \quad R_{\mathrm{L}} + 2R_{\mathrm{ona}} + R_{\mathrm{onm2}} \tag{3.3}$$

$$V_{\mathrm{t1\text{-}n}} = \qquad \frac{V_{\mathrm{dc}}}{2} - V_{\mathrm{xm2\text{-}n}} \tag{3.4}$$

(3.2) is a first order differential equation with the initial condition $I_{\mathrm{L}}(t_{\mathrm{1i}}) = 0$ and the final condition $I_{\mathrm{L}}(t_{\mathrm{1f\text{-}n}}) = i_{\mathrm{o\text{-}n}}$. Solving for the inductor current yields:

$$I_{\mathrm{L1\text{-}n}} = \frac{V_{\mathrm{t1\text{-}n}}}{R_{\mathrm{t1}}}\left(1 - e^{\frac{-R_{\mathrm{t1}}}{L}t}\right) \tag{3.5}$$

Then, sequence 1 has the duration of:

$$t_{\mathrm{1\text{-}n}} = \frac{-L}{R_{\mathrm{t1}}}\ln\left(1 - R_{\mathrm{t1}}\frac{i_{\mathrm{o\text{-}n}}}{V_{\mathrm{t1\text{-}n}}}\right) \tag{3.6}$$

- Sequence 2, period t_2: The initial and final conditions are $I_{\text{L}}(t_{\text{2i-n}}) = i_{\text{o-n}}$ and $I_{\text{L}}(t_{\text{2f-n}}) = I_{\text{b-n}}$. Sequence 2 does have the same components conducting and the same differential equation as in sequence 1. Then, solving for the inductor current yields:

$$I_{\text{L2-n}} = \frac{V_{\text{t2-n}}}{R_{\text{t2}}} + \left(i_{\text{o-n}} - \frac{V_{\text{t2-n}}}{R_{\text{t2}}} \right) e^{\frac{-R_{\text{t2}}}{L} t} \tag{3.7}$$

Sequence 2 has the duration of:

$$t_{\text{2-n}} = \frac{-L}{R_{\text{t2}}} \ln \left(\frac{I_{\text{b-n}} - \frac{V_{\text{t2-n}}}{R_{\text{t2}}}}{i_{\text{o-n}} - \frac{V_{\text{t2-n}}}{R_{\text{t2}}}} \right) \tag{3.8}$$

- Sequence 3, period t_3: This is the first resonant mode per switching cycle with the inductor is connected in series to the combination of non-linear output capacitances of the main switches and the constant load capacitance (all capacitances are acting in parallel). The total capacitance during the resonant mode is given by:

$$C_{3\text{t}} = C_{\text{oss-M1}}(v_{\text{ds1}}) + C_{\text{oss-M2}}(v_{\text{ds2}}) + C_{\text{load}} \tag{3.9}$$

where C_{load} is the parasitic capacitance of the load.

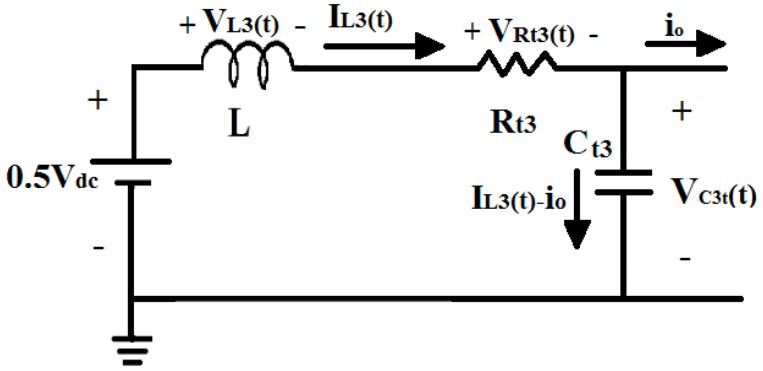


Figure 3.3: The equivalent circuit of the resonant mode 3.

Applying KVL yields (based on Figure 3.3):

$$\frac{-V_{\mathrm{dc}}}{2} + V_{\mathrm{xa1}} - V_{\mathrm{xa2}} + R_{\mathrm{L}} I_{\mathrm{L3}} + L\frac{dI_{\mathrm{L3}}}{dt} + V_{\mathrm{C3t}} = 0 \tag{3.10}$$

V_{C3t} is obtained by:

$$V_{\mathrm{C3t}} = \frac{1}{C_{3\mathrm{t}}} \int (I_{\mathrm{L3}} - i_{\mathrm{o\text{-}n}}) dt \tag{3.11}$$

where $C_{3\mathrm{t}}$ is defined in Table 3.2.

In order to increase the accuracy of the computations for the resonance modes (sequences 3 and 8), the non-linearity of the output capacitances of the main switches has been considered by interpolating these values from the device data sheet over the drain source voltage range of M_2 (the ARCP output voltage) within equally spaced intervals. The time duration of each voltage step has been estimated using ($A_{3\text{-n}}$, $B_{3\text{-n}}$ and $t_{3\text{-n}}$ in [32]) and by inserting the initial and final conditions based on output voltage step and the computed inductor current for each voltage step. Then, each time duration is added up to the next time step until the final conditions are reached.

Finding the first derivative of (3.10) and rearranging the terms yield:

$$L\frac{dI^2_{\mathrm{L3\text{-}n}}}{dt^2} + R_{\mathrm{t3}}\frac{dI_{\mathrm{L3\text{-}n}}}{dt} + \frac{I_{\mathrm{L3\text{-}n}} - i_{\mathrm{o\text{-}n}}}{C_{3\mathrm{t}}} = 0 \tag{3.12}$$

where R_{t3} is shown in Table 3.1.

This is a second order differential equation with the initial condition $I_{\mathrm{L3\text{-}n}}(t_{3i-n}) = I_{\mathrm{b\text{-}n}}$ ($I_{\mathrm{b\text{-}n}}$ is the boost current in n^{th} switching cycle), the non-linear output capacitance of the switch initial voltage $V_{\mathrm{Ci3\text{-}n}} = V_{\mathrm{xm2\text{-}n}}$ and the final voltage of this capacitor $V_{\mathrm{Cf3\text{-}n}} = V_{\mathrm{dc}} + V_{\mathrm{xm1\text{-}n}}$. Solving the characteristic equation of

(3.12) results in:

$$\delta_3 = \frac{R_{\text{t3}}}{2L} \tag{3.13}$$

$$\omega_3 = \sqrt{-\delta_3^2 + \frac{1}{LC_{3\text{t}}}} \tag{3.14}$$

$$\lambda_{13,23} = -\delta_3 + j\omega_3, -\delta_3 - j\omega_3 \tag{3.15}$$

Solving for the inductor current during the resonance mode yields (this is valid for constant capacitance but dealing with the non-linearity of the output capacitance is discussed in Section 6.2.2):

$$I_{\text{L3-n}} = C_{3\text{t}} e^{-\delta_3 t}(\lambda_{13} A_{3\text{-n}} e^{j\omega_3 t} + \lambda_{23} B_{3\text{-n}} e^{-j\omega_3 t}) + i_{\text{o-n}} \tag{3.16}$$

where:

$$A_{3\text{-n}} = \frac{I_{\text{t3i-n}} - i_{\text{o-n}} - C_{3\text{t}}\lambda_{23}(V_{\text{Ci3-n}} - 0.5V_{\text{dc}} + R_{\text{t3}} i_{\text{o-n}})}{2j\omega_3 C_{3\text{t}}} \tag{3.17}$$

$$B_{3\text{-n}} = \frac{-I_{\text{t3i-n}} + i_{\text{o-n}} + C_{3\text{t}}\lambda_{13}(V_{\text{Ci3-n}} - 0.5V_{\text{dc}} + R_{\text{t3}} i_{\text{o-n}})}{2j\omega_3 C_{3\text{t}}} \tag{3.18}$$

The duration of this sequence (assuming $C_{3\text{t}}$ here is constant and neglecting the damping factor) is given by:

$$t_{3\text{-n}} = \frac{\ln\left(\frac{(V_{\text{Cf3-n}} + V_{\text{x3-n}})}{2B_{3\text{-n}}} + \sqrt{\frac{(V_{\text{Cf3-n}} + V_{\text{x3-n}})^2}{4B_{3\text{-n}}^2} - \frac{A_{3\text{-n}}}{B_{3\text{-n}}}}\right)}{-j\omega_3} \tag{3.19}$$

where $V_{\text{x3-n}} = i_{\text{o-n}} R_{\text{t3}} - 0.5V_{\text{dc}}$.

- Sequence 4, period t_4: Solving for the inductor current with the initial and final conditions of $I_{\text{L4}}(t_{4\text{i-n}}) = I_{\text{b-n}}$ (the losses during the resonant period, lowering the current below I_{b} are neglected) and $I_{\text{L4}}(t_{4\text{f-n}}) = i_{\text{o-n}}$ yields:

$$I_{\text{L4-n}} = \frac{V_{\text{t4-n}}}{R_{\text{t4}}} + \left(I_{\text{b-n}} - \frac{V_{\text{t4-n}}}{R_{\text{t4}}}\right) e^{-\frac{R_{\text{t4}}}{L} t} \tag{3.20}$$

where R_{t4} and V_{t4} are shown in Table 3.1. The duration of this sequence is given by:

$$t_{4\text{-n}} = \frac{-L}{R_{t4}} \ln \left(\frac{i_{\text{o-n}} - \frac{V_{t4\text{-n}}}{R_{t4}}}{I_{\text{b-n}} - \frac{V_{t4\text{-n}}}{R_{t4}}} \right) \tag{3.21}$$

- Sequence 5, period t_5: The initial and final conditions are $I_{\text{L5}}(t_{5\text{i-n}}) = i_{\text{o-n}}$ and $I_{\text{L5}}(t_{5\text{f-n}}) = 0$. The inductor current is given by:

$$I_{\text{L5-n}} = \frac{V_{t5\text{-n}}}{R_{t5}} + \left(i_{\text{o-n}} - \frac{V_{t5\text{-n}}}{R_{t5}} \right) e^{-\frac{R_{t5}}{L} t} \tag{3.22}$$

  Then, the duration of this sequence is given by:

$$t_{5\text{-n}} = \frac{-L}{R_{t5}} \ln \left(\frac{\frac{-V_{t5\text{-n}}}{R_{t5}}}{\frac{-V_{t5\text{-n}}}{R_{t5}} + i_{\text{o-n}}} \right) \tag{3.23}$$

- Sequence 6, period t_6: In this sequence, no current flows in the resonant inductor. The duration of this sequence can be calculated by:

$$t_{6\text{-n}} = D_{\text{n}} T_{\text{s}} - (t_{4\text{-n}} + t_{5\text{-n}} + t_{7\text{-n}}) \tag{3.24}$$

  where, T_{s} is the switching period and D_{n} is the duty cycle during switching period n.

- Sequence 7, period t_7: The initial and final conditions are $I_{\text{L7}}(t_{7\text{i-n}}) = 0$ and $I_{\text{L7-n}}(t_{7f-n}) = -I_{\text{b-n}}$. Then:

$$I_{\text{L7-n}} = \frac{V_{t7\text{-n}}}{R_{t7}} \left(1 - e^{\frac{-R_{t7}}{L} t} \right) \tag{3.25}$$

  The duration of this sequence is given by:

$$t_{7\text{-n}} = \frac{-L}{R_{t7}} \ln \left(1 + \frac{I_{\text{b-n}} R_{t7}}{V_{t7\text{-n}}} \right) \tag{3.26}$$

- Sequence 8, period t_8: This is the second resonance period of the switching cycle in which the inductor resonates with the non-linear output capacitances of the main switches plus load capacitance (as stated in (3.9), where $C_{8\text{t}} = C_{3\text{t}}$). The initial and final conditions for this sequence are: $I_{\text{L8}}(t_{8\text{i-n}}) = -I_{\text{b-n}}$, the initial voltage of the non-linear output capacitance $V_{\text{Ci8-n}} = V_{\text{dc}} - V_{\text{xm1-n}}$ and its final voltage is $V_{\text{Cf8-n}} = V_{\text{xm2-n}}$. The same procedure used in sequence 3, but using the associated total resistance and capacitance of mode 8, is followed to obtain the inductor current. The inductor current during the resonance mode is given by:

$$I_{\text{L8-n}} = C_{8\text{t}} e^{-\delta_8 t}(\lambda_{18} A_{8\text{-n}} e^{j\omega_8 t} + \lambda_{28} B_{8\text{-n}} e^{-j\omega_8 t}) + i_{\text{o-n}} \tag{3.27}$$

where:

$$A_{8\text{-n}} = \frac{I_{\text{t8i-n}} - i_{\text{o-n}} - C_{8\text{t}}\lambda_{28}(V_{\text{Ci8-n}} - 0.5V_{\text{dc}} + R_{\text{t8}} i_{\text{o-n}})}{2j\omega_8 C_{8\text{t}}} \tag{3.28}$$

$$B_{8\text{-n}} = \frac{-I_{\text{t8i-n}} + i_{\text{o-n}} + C_{8\text{t}}\lambda_{18}(V_{\text{Ci8-n}} - 0.5V_{\text{dc}} + R_{\text{t8}} i_{\text{o-n}})}{2j\omega_8 C_{8\text{t}}} \tag{3.29}$$

The duration of this sequence is given by:

$$t_{8\text{-n}} = \frac{\ln\left(\frac{(V_{\text{Cf8-n}} + V_{\text{x8-n}})}{2A_{8\text{-n}}} + \sqrt{\frac{(V_{\text{Cf8-n}} + V_{\text{x8-n}})^2}{4A_{8\text{-n}}^2} - \frac{B_{8\text{-n}}}{A_{8\text{-n}}}}\right)}{j\omega_8} \tag{3.30}$$

where $V_{\text{x8-n}} = i_{\text{o-n}} R_{\text{t8}} - 0.5V_{\text{dc}}$.

- Sequence 9, period t_9: The initial and final conditions are $I_{\text{L9}}(t_{9\text{i-n}}) = -I_{\text{b-n}}$ and $I_{\text{L9}}(t_{9\text{f-n}}) = 0$. The inductor current is given by:

$$I_{\text{L9-n}} = \frac{V_{\text{t9-n}}}{R_{\text{t9}}} + \left(-I_{\text{b-n}} - \frac{V_{\text{t9-n}}}{R_{\text{t9}}}\right) e^{\frac{-R_{\text{t9}}}{L} t} \tag{3.31}$$

and the duration of this sequence is:

$$t_{9\text{-n}} = \frac{-L}{R_{\text{t9}}} \ln\left(\frac{\frac{-V_{\text{t9-n}}}{R_{\text{t9}}}}{-I_{\text{b-n}}} - \frac{V_{\text{t9-n}}}{R_{\text{t9}}}\right) \tag{3.32}$$

- Sequence 10, period t_{10}: In this sequence, no current flows in the resonant inductor. The duration of this mode is given by:

$$t_{10\text{-n}} = (1 - D_{\text{n}})T_{\text{s}} - (t_{1\text{-n}} + t_{2\text{-n}} + t_{3\text{-n}} + t_{8\text{-n}} + t_{9\text{-n}}) \tag{3.33}$$

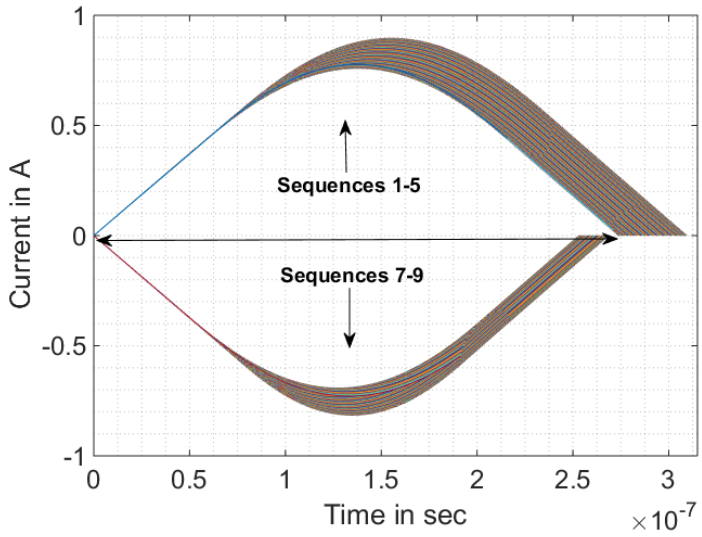


Figure 3.4: Simulated inductor current per switching cycle within the positive half of the output waveform, at 300 V DC link voltage and AC load current of 150 mA peak.

Figure 3.4 shows the simulated inductor current for each switching cycle within the positive half of the output current of the fundamental period. The simulation conditions are 300 V DC link voltage and AC load current with peak value of 150 mA. The positive resonant inductor current represents the sequences from $1-5$. Whereas, the negative indcutor current represents the sequences $7-9$.

As a summary of the derived mathematical model, the inductor current for each sequence of operation is given by:

$$I_{\text{Lk-n}}(t) = \begin{cases} C_{\text{kt}} e^{-\delta_{\text{k}} t}(\lambda_{1\text{k}} A_{\text{k-n}} e^{j\omega_{\text{k}} t} + \\ \qquad +\lambda_{2\text{k}} B_{\text{k-n}} e^{-j\omega_{\text{k}} t}) + i_{\text{o-n}} & k \in \{3, 8\} \\ \frac{V_{\text{tk-n}}}{R_{\text{tk}}} + \left(I_{\text{L}}(t_{\text{ki-n}}) - \frac{V_{\text{tk-n}}}{R_{\text{tk}}}\right) e^{\frac{-R_{\text{tk}}}{L} t} & \text{otherwise} \end{cases} \tag{3.34}$$

and the time period for each sequence is given by:

$$t_{\text{k-n}} = \begin{cases} \frac{\ln\left(\frac{(V_{\text{Cfk-n}}+V_{\text{xk-n}})}{2B_{\text{k-n}}} + \sqrt{\frac{(V_{\text{Cfk-n}}+V_{\text{xk-n}})^2}{4B_{\text{k-n}}^2} - \frac{A_{\text{k-n}}}{B_{\text{k-n}}}}\right)}{-j\omega_{\text{k}}} & k \in \{3\} \\ \frac{\ln\left(\frac{(V_{\text{Cfk-n}}+V_{\text{xk-n}})}{2A_{\text{k-n}}} + \sqrt{\frac{(V_{\text{Cfk-n}}+V_{\text{xk-n}})^2}{4A_{\text{k-n}}^2} - \frac{B_{\text{k-n}}}{A_{\text{k-n}}}}\right)}{j\omega_{\text{k}}} & k \in \{8\} \\ \frac{-L}{R_{\text{tk}}} \ln\left(\frac{I_{\text{L}}(t_{\text{kf-n}}) - \frac{V_{\text{tk-n}}}{R_{\text{tk}}}}{I_{\text{L}}(t_{\text{ki-n}}) - \frac{V_{\text{tk-n}}}{R_{\text{tk}}}}\right) & \text{otherwise} \end{cases} \tag{3.35}$$

where k is the sequence number, $V_{\text{xm-n}}$ denotes the voltage drop across the conducting main semiconductor based on Table 3.1. Table 3.1 summarizes the state of all the semiconductors, the resistance, the driving voltages, the initial and final conditions for the resonant inductor current differential equations. Table 3.2 lists the symbols used.

Table 3.1: Initial and final conditions, equivalent resistances and voltages and the statuses of the switches for each sequence, for the computation of the inductor currents and time durations as per (3.34) and (3.35).

k	Initial cond.	final cond.	R_{t}	V_{t}	M_1	M_2	A_1	A_2
1	$I_{\text{L}}(t_{1\text{i}}) = 0$	$I_{\text{L}}(t_{1\text{f-n}}) = i_{\text{o-n}}$	$R_{\text{L}} + 2R_{\text{ona}} + R_{\text{onm2}}$	$0.5V_{\text{dc}} - V_{\text{xm2-n}}$	Off	-CH	CH	-CH
2	$I_{\text{L}}(t_{2\text{i-n}}) = i_{\text{o-n}}$	$I_{\text{L}}(t_{2\text{f-n}}) = I_{\text{b-n}}$	$R_{\text{L}} + 2R_{\text{ona}} + R_{\text{onm2}}$	$0.5V_{\text{dc}} - V_{\text{xm2-n}}$	Off	CH	CH	-CH
3	$I_{\text{L}}(t_{3i-n}) = I_{\text{b-n}}$ $V_{\text{Ci3-n}} = V_{\text{xm2-n}}$	$V_{\text{Cf3-n}} = V_{\text{dc}}+$ $+V_{\text{xm1-n}}$	$R_{\text{L}} + 2R_{\text{ona}}$		Off	Off	CH	-CH
4	$I_{\text{L4}}(t_{4\text{i-n}}) = I_{\text{b-n}}$	$I_{\text{L4}}(t_{4\text{f-n}}) = i_{\text{o-n}}$	$R_{\text{L}} + 2R_{\text{ona1}} + R_{\text{onm1}}$	$-0.5V_{\text{dc}} + V_{\text{xm1-n}}$	-CH	Off	CH	-CH
5	$I_{\text{L5}}(t_{5\text{i-n}}) = i_{\text{o-n}}$	$I_{\text{L5}}(t_{5\text{f-n}}) = 0$	$R_{\text{L}} + 2R_{\text{ona1}} + R_{\text{onm1}}$	$-0.5V_{\text{dc}} + V_{\text{xm1-n}}$	CH	Off	CH	-CH
6	$I_{\text{L6-n}} = 0$		R_{onm1}		CH	Off	Off	Off
7	$I_{\text{L7}}(t_{7\text{i-n}}) = 0$	$I_{\text{L7-n}}(t_{7f-n}) = -I_{\text{b-n}}$	$R_{\text{L}} + 2R_{\text{ona}} + R_{\text{onm1}}$	$-0.5V_{\text{dc}} + V_{\text{xm1-n}}$	CH	Off	-CH	CH
8	$I_{\text{L8}}(t_{8\text{i-n}}) = -I_{\text{b-n}}$ $V_{\text{Ci8-n}} = V_{\text{dc}} - V_{\text{xm1-n}}$	$V_{\text{Cf8-n}} = V_{\text{xm2-n}}$	$R_{\text{L}} + 2R_{\text{ona2}}$		Off	Off	-CH	CH
9	$I_{\text{L9}}(t_{9\text{i-n}}) = -I_{\text{b-n}}$	$I_{\text{L9}}(t_{9\text{f-n}}) = 0$	$R_{\text{L}} + 2R_{\text{ona2}} + R_{\text{onm2}}$	$0.5V_{\text{dc}} - V_{\text{xm2-n}}$	Off	-CH	-CH	CH
10	$I_{\text{L10-n}} = 0$		R_{onm2}		Off	-CH	Off	Off

Table 3.2: Definition of symbols.

Symbol	Definition
R_{on}	On-state resistances. For MOSFETs R_{dson}, for IGBTs R_{ce}.
R_{L}	Internal DC resistance of the inductor.
V_{x}	Voltage across the semiconductor device (diode or the channel).
V_{tk}	Equivalent voltage of sequence k.
R_{tk}	Equivalent resistance of sequence k.
$i_{\text{o-n}}$	Current drawn by the load in the n^{th} switching cycle.
$I_{\text{b-n}}$	Boost current in the n^{th} switching cycle.
$C_{3\text{t}}$	$C_{\text{oss-M1}}(v_{\text{ds1}}) + C_{\text{oss-M2}}(v_{\text{ds2}}) + C_{\text{load}}$ and $C_{3\text{t}} = C_{8\text{t}}$.
$C_{\text{oss-M1}}$	Non-linear output capacitance of switch M_1.
$C_{\text{oss-M2}}$	Non-linear output capacitance of switch M_2.
C_{load}	Parasitic capacitance of the load.
R_{f}	Differential resistance of the body diode.
V_{f}	Forward voltage of the body diode at zero current.
V_{dc}	DC link voltage.
Q_{oss}	Output charge of the main switch M_1 or M_2.
$t_{\text{r-v-max}}$	Voltage rise time at turning off of M_1 which is assumed $0.1T_{\text{s}}$.

3.3 ARCPI Loss Analysis

The current drawn by the load is symmetrical in the positive and the negative half cycles of the fundamental period, so the energy losses are calculated for the positive half wave only. Then, two of these energy losses are averaged over one fundamental period.

From the duration and the inductor current of each mode, the loss components in an ARCP are calculated as follows [23, 24, 33, 34]:

- The conduction losses related to the commutation:

$$E_{\text{k-n}} = \begin{cases} \int_0^{t_{\text{k-n}}} (R_{\text{tk}} I_{\text{Lk-n}}^2) dt & k \in \{3, 8\} \\ \int_0^{t_{\text{k-n}}} [(R_{\text{tk}} - R_{\text{onm}}) I_{\text{Lk-n}}^2 + & \\ \quad + R_{\text{onm}} (I_{\text{Lk-n}} - i_{\text{o-n}})^2] dt & \text{otherwise} \end{cases} \tag{3.36}$$

  where R_{tk} (for MOSFETs only) based on Table 3.1.

  The energy losses in the commutation circuit due to conduction only are given by (derived from (3.36)):

$$E_{\text{commut-n}} = \sum_{k=1}^{K} E_{\text{k-n}} \tag{3.37}$$

  where K is the number of sequences and $E_{\text{k-n}}$ is the energy computed by (3.36) depending on the number of k.

- The energy losses in the main switches (conduction losses which are not related to commutation) are given by (This is valid for MOSFETs, IGBTs and diodes):

$$E_{\text{Main-n}} = \int_0^{t_{\text{6-n}}} V_{\text{xm1-n}} i_{\text{o-n}} dt + \int_0^{t_{\text{10-n}}} V_{\text{xm2-n}} i_{\text{o-n}} dt \tag{3.38}$$

- Switching losses of the two auxiliary switches (A_1 and A_2): Prior to sequence one, M_2 conducts and A_2 is reverse biased, thus, the body diode conducts any leakage current which might pass through A_1 which is blocking $0.5\,V_{\mathrm{dc}}$. As sequence 1 starts with turning on A_1 and A_2, the output capacitance of A_1 is discharged from $0.5V_{\mathrm{dc}}$ to 0 and the energy stored in this capacitance is dissipated. This energy dissipation is given by:

$$E_{\text{swon-n1}} = \int_0^{\frac{V_{\mathrm{dc}}}{2}} v\; C_{\text{aux-A1-on}}(v)\; dv \tag{3.39}$$

where $C_{\mathrm{aux}}(v)$ is the non-linear output capacitance of the auxiliary switch A_1.

However, as seen from Figure 6.14, the peak of drain source voltage of the auxiliary switch A_2 reaches the DC link voltage. Therefore, the peak energy being stored in the output capacitance of A_2 is given by (3.40). The first part of this energy is dissipated during the oscillation following the voltage peak. The remaining energy is given by (3.39) and it is dissipated at the beginning of the next commutation cycle as described above. Thus, the switching losses related to one commutation cycle equals (3.40).

$$E_{\text{swon-n}} = \int_0^{V_{\mathrm{dc}}} v\; C_{\text{aux-A2-off}}(v)\; dv \tag{3.40}$$

During sequence 5, A_2 is turned off just before the zero crossing of the inductor current. This reduces the reverse recovery charge build up of the body diode. After the inductor current crossing zero, switch A_1 is turned off. The reverse recovery period is divided into two intervals of equal length. During the first half, the reverse current reaches its maximum causing energy to be stored in the inductor, which yields:

$$E_{\text{L-n}} = \frac{L I_{\mathrm{RM}}^2}{2} \tag{3.41}$$

The peak of this reverse current I_{RM} is estimated by:

$$V_{\mathrm{L}} = L\frac{di}{dt} = L\frac{2I_{\mathrm{RM}}}{t_{\mathrm{rr}}} \tag{3.42}$$

$$t_{\mathrm{rr}} = \frac{2LI_{\mathrm{RM}}}{V_{\mathrm{L}}} \tag{3.43}$$

where V_{L}= $0.5\,V_{\mathrm{dc}}$. Then, I_{RM} is given by (based on [32]):

$$I_{\mathrm{RM}} = \sqrt{\frac{I_{\text{b-n}}Q_{\mathrm{rr}}V_{\mathrm{L}}}{LI_{\text{aux-N}}}} \tag{3.44}$$

where Q_{rr} is the reverse recovery charge mentioned in the data sheet and $I_{\text{aux-N}}$ is the nominal current of the auxiliary switches mentioned in the data sheet.

During the second part of the reverse recovery time, there are two parts of energy dissipation:

- First, the reverse current decreases linearly to zero with non-zero drain source voltage of A_2. Assuming that the drain source voltage of A_2 increases linearly (during positive edge of the output voltage-see Figure 6.14), the energy dissipated in the switch is approximated by:

$$E_{\text{off-sw-n}} = \int_0^{0.5t_{\mathrm{rr}}} I_{\mathrm{R}}(t).V_{\mathrm{ds}}(t)dt = I_{\mathrm{RM}}V_{\text{ds-peak}}\frac{t_{\mathrm{rr}}}{12} \tag{3.45}$$

  where $V_{\text{ds-peak}}$ is the peak value of the drain source voltage of A_2.

- Second, the energy drawn from the supply due to the reverse recovery which is given by:

$$E_{\text{off-Qrr-n}} = \frac{I_{\mathrm{RM}}\frac{t_{\mathrm{rr}}}{2}}{2}\frac{V_{\mathrm{dc}}}{2} \tag{3.46}$$

The last part of the switching losses is the energy dissipated at turn off of M_2 ($C_{3\mathrm{t}}$, see Table 3.2, the equivalent capacitance for mode 3 is acting as

snubber capacitance). This energy is estimated by:

$$E_{\text{offM-n}} = \frac{((I_{\text{b-n}} - i_{\text{o-n}})t_{\text{fi-new-n}})^2}{24C_{3\text{t}}} \tag{3.47}$$

where $t_{\text{fi-new-n}}$ is the current fall time (the computation of this time was presented in (2.23)) and $C_{3\text{t}}$ is defined in Table 3.2. The total switching losses of both auxiliary switches for both the positive and the negative period of the resonant current are given by (twice the sum of (3.40), (3.41), (3.45), (3.46) and (3.47)):

$$E_{\text{sw-n}} = 2(E_{\text{swon-n}} + E_{\text{L-n}} + E_{\text{off-sw-n}} + E_{\text{off-Qrr-n}} + E_{\text{offM-n}}) \tag{3.48}$$

- The energy lost in the gate resistance (internal plus external, if included) of the two main switches and the two auxiliary switches is given by:

$$E_{\text{gt-n}} = 2Q_{\text{gt-main}}\frac{V_{\text{drm}}^2}{V_{\text{qgm}}} + 2Q_{\text{gt-aux}}\frac{V_{\text{draux}}^2}{V_{\text{qgaux}}} \tag{3.49}$$

Q_{gt} is the total gate charge at a gate voltage of V_{qg} as given in the data sheet and V_{dr} is the actual driving voltage as shwon in Section 2.2.3.

- Finally, to determine the total power losses in the ARCP, the energy lost in all components of the circuit is summed over N switching cycles within the positive half of the output current waveform ($0.5/f_{\text{mod}}$). This energy is, then, averaged over half of the fundamental period, where:

$$P_{\text{ARCP}} = 2f_{\text{mod}}\sum_{n=1}^{N}(E_{\text{Main-n}} + E_{\text{commut-n}} + E_{\text{sw-n}} + E_{\text{gt-n}}) \tag{3.50}$$

Chapter 4

Power Factor Correction Circuit Loss Analysis

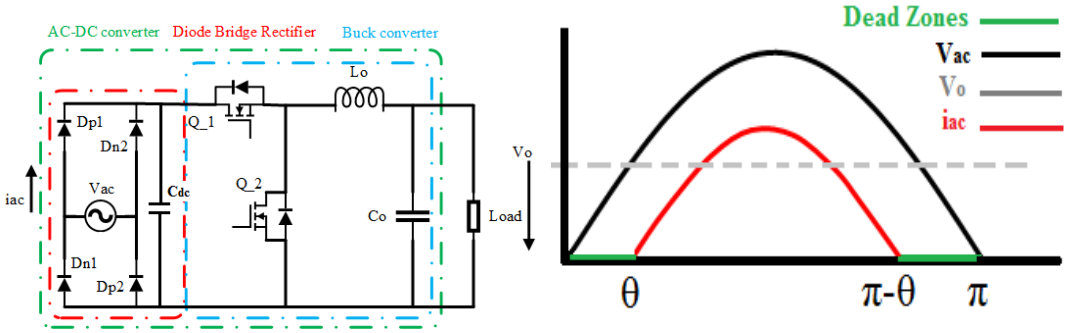
4.1 Introduction

More attention has been payed to AC – DC converters over the last few decades because of their ability to improve the power factor of input power and keep the Total Harmonics Distortion (THD) in the line current within the standard limits [35]. Recently, improving the efficiency of these converters has become a significant milestone under economical and some standard constraints for different industrial applications.

Many topologies of Power Facor Correction (PFCs) converters are proposed and presented in literature. Conventionally, in order to build a buck PFC (green dashed box in Figure 4.1a), a Diode Bridge Rectifier (DBR red dashed box in Figure 4.1a) is connected with a DC – DC converter (blue dashed box in Figure 4.1a). This converter in Figure 4.1a is a buck converter and could be replaced by a boost converter [36, 37], a buck-boost converter [38–40], buck-flyback converter [41].

However, for low power applications, the buck PFCs are more efficient than other PFCs topologies, e.g., boost PFC, because of reducing the voltage stress across the switch due to the fact that the buck PFC output voltage is always

lower than the input voltage [35, 42, 43].



(a) Conventional Buck PFC.

(b) Operating Conditions-positive half cycle of the AC line voltage.

Figure 4.1: The conventional buck PFC and its operating conditions within positive half cycle of the AC line voltage.

The buck PFC with a DBR in front has some drawbacks [44–48]: First, the voltage drop across the DBR's diodes prevents high efficiency from being achieved. Second, the AC input current flows in the circuit when the input AC voltage exceeds the output voltage (boundary voltage) as shown in Figure 4.1b. This causes poor power factor, and thus, high harmonic distortion.

In order to improve the efficiency of the conventional PFCs, bridge-less PFCs are proposed to reduce the on state voltage drop, thereby reducing the conduction losses in the circuit (e.g., [42, 45]).

Showing the importance of the buck PFC in different applications, Table 4.1 summarizes different toplogies that have been presented so far.

In [49], a conventional buck PFC is designed using the predictive line voltage reconstruction technique. The designed converter is operated in Continuous Conduction Mode (CCM) with Average Current Mode (ACM) control. The designed converter has an improved EMI performance compared to the conventional buck converter controlled by the Constant On Time (COT) method. Hence, the power factor and the efficiency of 100 W prototype are 95 % and 98 %, respectively, at AC line voltage of 110 V. More discussions showing the importance of control strategies of the buck converter are introduced in [50–54].

Table 4.1: Comparison of different buck PFC topologies.

	Figure 4.1a	[35]	[42]	[45]	[55]	[41]	Figure 4.2
Number of diodes	4	7	4	5	5	6	2
Number of switches	2	2	2	1	1	2	6
Number of capacitors	1	1	2	3	2	1	1
Number of indcutors	1	1	2	3	1	1	2
Input voltage range V	$90-270$	$80-265$	$115-230$	100	$90-265$	$90-265$	$90-265$
Output voltage V	20	–	160	48	90	80	50
Power rating W	70	100	700	100	100	150	70
Efficiency P_{max}	-	$95.4-95.6$	96.4	96.3	$95.5-96.7$	$94.6-96.3$	
Efficiency P_{min}	-	-	96.4(50% load)	-	90, 83(10% load)	-	
Rating V/I-diodes-DBR	$600V$,$0.5A$	-	$600V/15A$	-	-	$600V/8A$	-
Rating V/I-diodes-others	-	-	-	-	$600V/8A$	D_2,$150V/30A$	-
Rating V/I-capacitors	$220uF/200V$	-	$1000uF/100VDC$	-	$660uF/100V$	$100V/490uF$,C_o	-
Rating V/I-indcutors	$2mH/3A$	-	$60uH/24turnes/litzwires$	-	$150uH$	$135uH$	-

While more refinements are proposed to improve the conventional buck PFC converters (Figure 4.1a) as in [35] and [41], a new bridge-less buck PFC converter is proposed in order to eliminate the diode bride rectifier which reduces the conduction losses. Both PFCs (Figure 4.1a and Figure 4.2) are operated under extremely light load conditions (even lower than the proposed load in [44]). These load conditions are specified in (see Section 1.5).

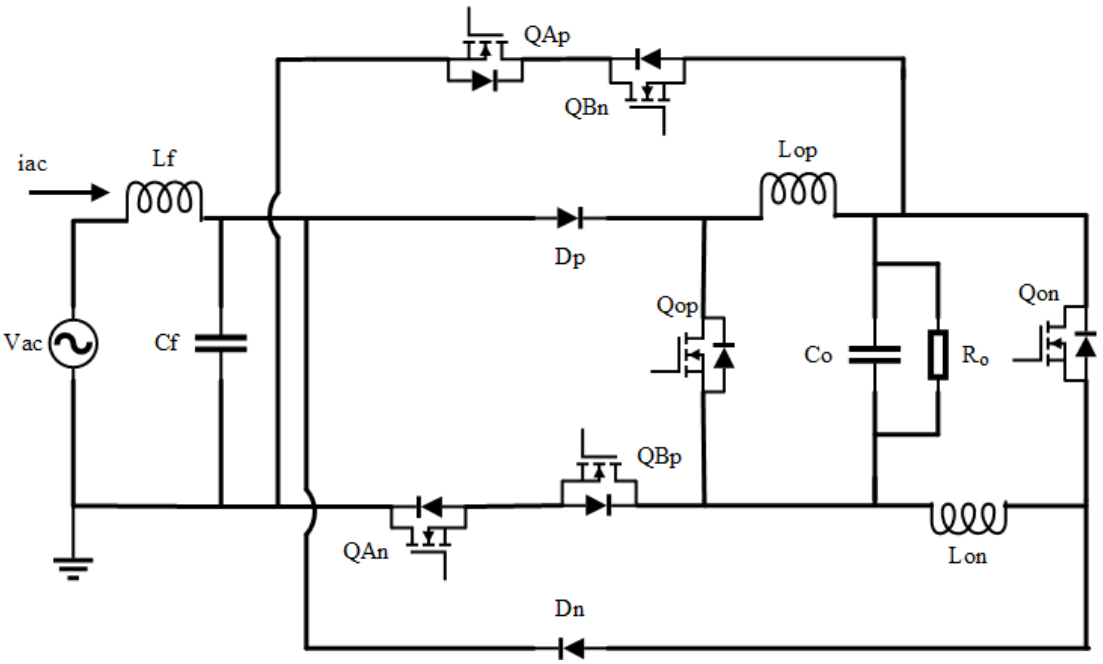


Figure 4.2: Proposed single-phase hybrid bridge-less step PFC down converter, in which V_{ac} is the single phase rms grid voltage, C_o is the output capacitance (filter capacitance) and R_o is the load resistance.

4.2 "The Proposed Converter"

The term hybrid is used because of the proposed circuit based on two different topologies (buck - boost and boost topologies). Figure 4.2 shows a schematic of the proposed converter. It should be noted that the diode bridge rectifier is eliminated. The operation modes and the key waveforms are shown in Figure 4.3.

The discussion of the operating principles of the proposed converter is based on the following assumptions:

- The input AC line voltage is assumed to be pure sine wave.
- The switching frequency (f_{s}) is high enough the inductor's current is assumed to be constant during n^{th} switching cycle.
- The ratio between the on time of the auxiliary switch Q_{Ap} and the turn on time of the buck switch Q_{Bp} is assumed to be constant: $T_{\text{on-QAp}} = kT_{\text{on-QBp}} = kT_{\mathrm{on}}$, where k is the design constant.

4.2.1 Operation Modes: Positive Half Cycle of the Line Voltage

As the proposed converter is symmetrical in both half cycles of the AC line voltage (positive and negative), the following discussion is presented for the positive half cycle of the AC line voltage. The proposed converter is controlled using Critical Conduction Mode with Constant On Time (CRM with COT). This method removes the effect of the reverse recovery charge of the diode or the synchronous switch body diode, thus, reducing the switching losses.

When $V_{\mathbf{ac}} < V_{\mathbf{b}}$

When the AC line voltage is lower than the boundary voltage ($V_{\mathrm{ac}} < V_{\mathrm{b}}$), the converter is operated as buck-boost topology. There are two modes, as follow:

- Mode 1: the auxiliary switch Q_{AP} is gated on and the output inductor L_{op} is connected to the supply voltage and energized through the path $D_{\mathrm{p}} - L_{\mathrm{op}} - Q_{\mathrm{Bn}} - Q_{\mathrm{Ap}}$, see Figure 4.3a. The inductor L_{op} is energized. The peak value of the inducor current is given by:

$$i_{\mathrm{p1}}(\theta) = \frac{\sqrt{2}V_{\mathrm{ac}}\sin(\theta)}{L_{\mathrm{op}}}kT_{\mathrm{on}} \tag{4.1}$$

  where V_{ac} is the single phase rms grid voltage and T_{on} is the on time.

- Mode 2: the auxiliary switch Q_{AP} is gated off and the output capacitor C_{o} is charged to reach V_{o} (load voltage). The capacitor is charged from the energy stored in the inductor from mode 1 through the path $Q_{\mathrm{op}} - L_{\mathrm{op}} - C_{\mathrm{o}}$, Figure 4.3b.

When $V_{\mathbf{ac}} > V_{\mathbf{b}}$

When the AC line voltage is greater than the boundary voltage ($V_{\mathrm{ac}} > V_{\mathrm{b}}$), the converter is operated as buck topology. There are two modes, as follow:

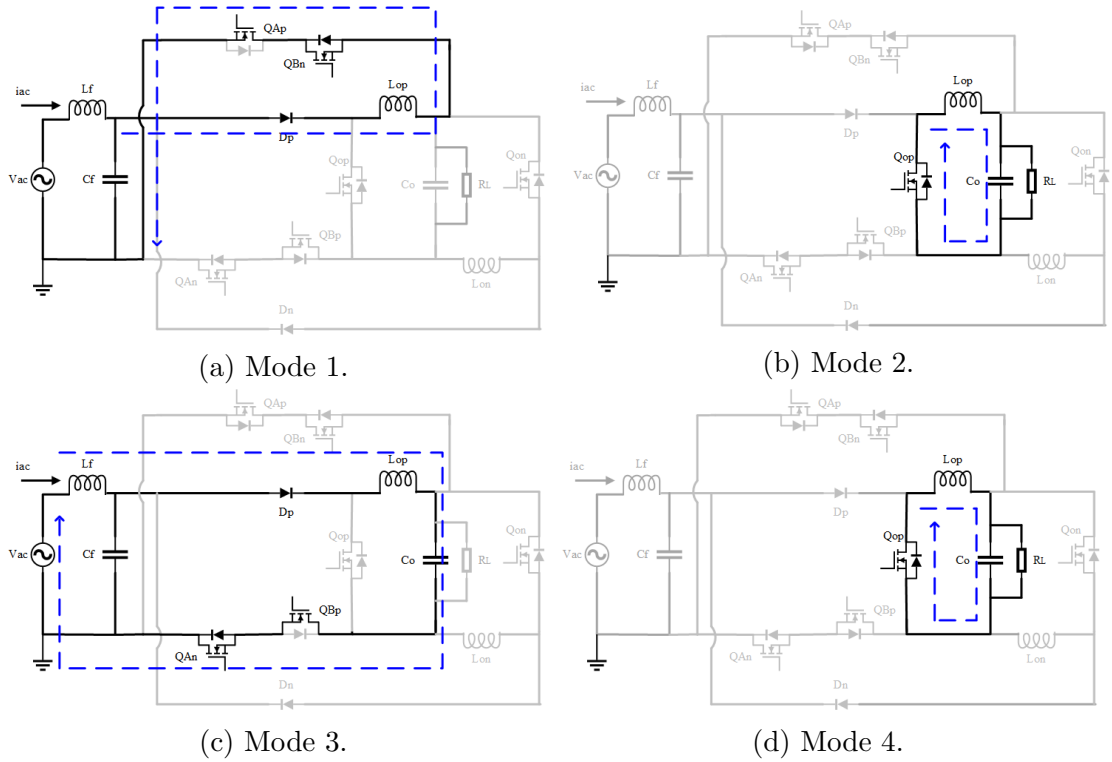
- Mode 3: the auxiliary switch Q_{BP} is gated on and the output inductor L_{op} is connected to the supply voltage and energized through the path $D_{\mathrm{p}} - L_{\mathrm{op}} - C_{\mathrm{o}} - Q_{\mathrm{Bp}} - Q_{\mathrm{An}}$, see Figure 4.3c. The inductor L_{op} is energized. The peak value of the inductor current is given by:

$$i_{\mathrm{p2}}(\theta) = \frac{(\sqrt{2}V_{\mathrm{ac}}\sin(\theta) - V_{\mathrm{o}})}{L_{\mathrm{op}}}T_{\mathrm{on}} \tag{4.2}$$

- Mode 4: the auxiliary switch Q_{BP} is gated off and the output capacitor C_{o} is charged through the path $Q_{\mathrm{op}} - L_{\mathrm{op}} - C_{\mathrm{o}}$, see Figure 4.3d. The output capacitor C_{o} is charged to reach V_{o}.

When $V_{ac} < V_b$

When the AC line voltage is lower than the boundary voltage ($V_{ac} < V_b$), there are two Modes as depicted in Figures 4.3a and 4.3b.



(a) Mode 1.

(b) Mode 2.

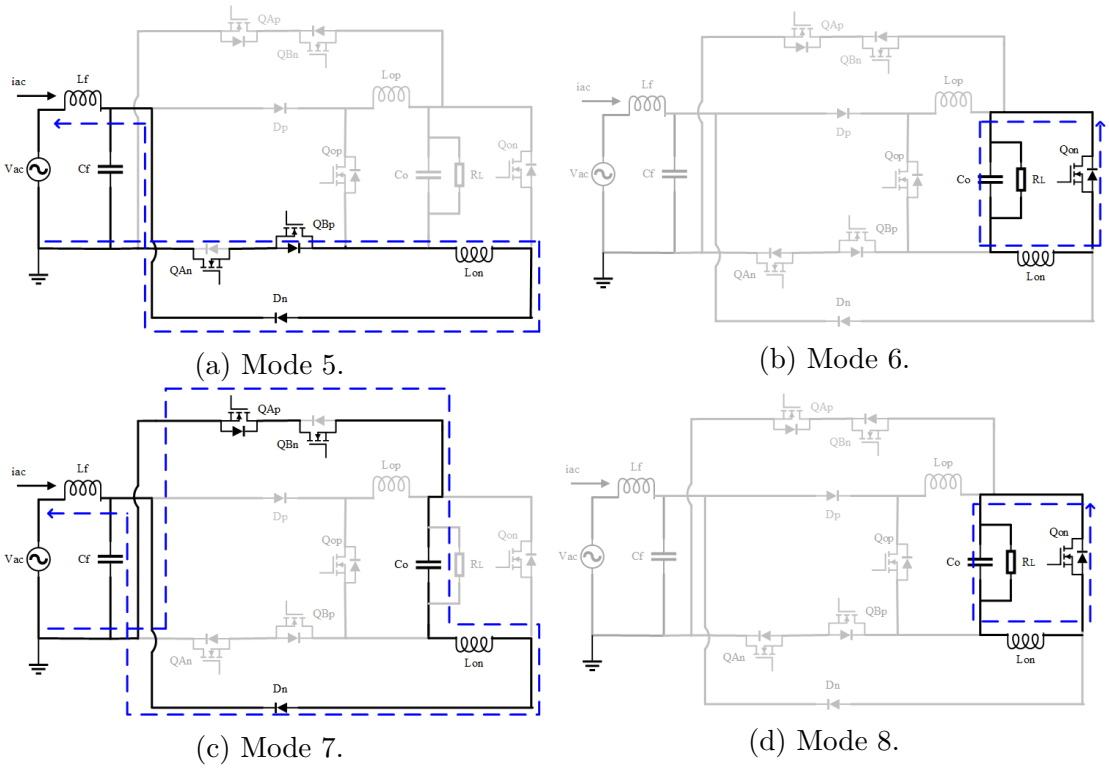
(c) Mode 3.

(d) Mode 4.

Figure 4.3: Operation modes of the proposed bridge-less step down converter-positive half cycle of the line voltage.

4.2.2 Operation Modes: Negative Half Cycle of the Line Voltage

During this half cycle, the operating modes of the proposed converter are the same for the positive half cycle of the AC line voltage. The corresponding components for this cycle are labeled by the following: Q_{Bn}, Q_{An}, D_n, Q_{on} and L_{on} as illustrated in Figure 4.2. Figures 4.4a-4.4d show the conducting devices and paths of the current during the negative half cycle of the line voltage (during the modes 5-8).



(a) Mode 5.

(b) Mode 6.

(c) Mode 7.

(d) Mode 8.

Figure 4.4: Operation modes of the proposed bridge-less step down converter-negative half cycle of the line voltage.

4.3 Design Procedures and Analysis

This section discusses the mathematical model which is used to design the proposed converter. The analysis is discussed for the positive half cycle of the AC line voltage because of the symmetry between the positive and negative half cycles. The proposed converter eliminates the dead zones which are illustrated in Figure 4.1b.

4.3.1 Analysis of AC Line Voltage and Current

As mentioned above, the AC line current starts flowing into the circuit when the auxiliary switch Q_{Ap} is turned on (operating as buck boost topology). The average

AC input current is given by:

$$\overline{i_{\mathrm{ac}}}(\theta) = \begin{cases} \frac{i_{\mathrm{p2}}(\theta)}{2} \frac{V_{\mathrm{o}}}{\sqrt{2}V_{\mathrm{ac}}\sin(\theta)} & \theta_0 < \theta < \pi - \theta_0 \\ \frac{i_{\mathrm{p1}}(\theta)}{2} \frac{V_{\mathrm{o}}}{(\sqrt{2}V_{\mathrm{ac}}\sin(\theta)+V_{\mathrm{o}})} & \text{otherwise} \end{cases} \tag{4.3}$$

where i_{p1} and i_{p2} are given by (4.1) and (4.2), respectively. V_{ac} is the customary RMS phase voltage (for universal operation $90 < V_{\mathrm{ac}} < 270$), $\theta = \omega\, t$, $\omega = 2\pi f_{\mathrm{l}}$, f_{l} is the line frequency (50 Hz), k is the design constant and θ_0 is the boundary angle which can be seen in Figure 4.1b and is given by:

$$\theta_0 = \sin^{-1}(\frac{V_{\mathrm{b}}}{\sqrt{2}V_{\mathrm{ac}}}) \tag{4.4}$$

In the proposed hybrid PFC, the boundary voltage V_{b} determines the boundary angle at which the hybrid PFC changes its mode of operation. The turn on time T_{on} which is assumed to be constant (Constant On Time control) within the switching cycle can be computed based on balancing the average input and output power (e.g., $P_{\mathrm{in}} = P_{\mathrm{o}}/\eta$) where the circuit efficiency is assumed to be equal to the desired value (η) and P_{in} is estimated by:

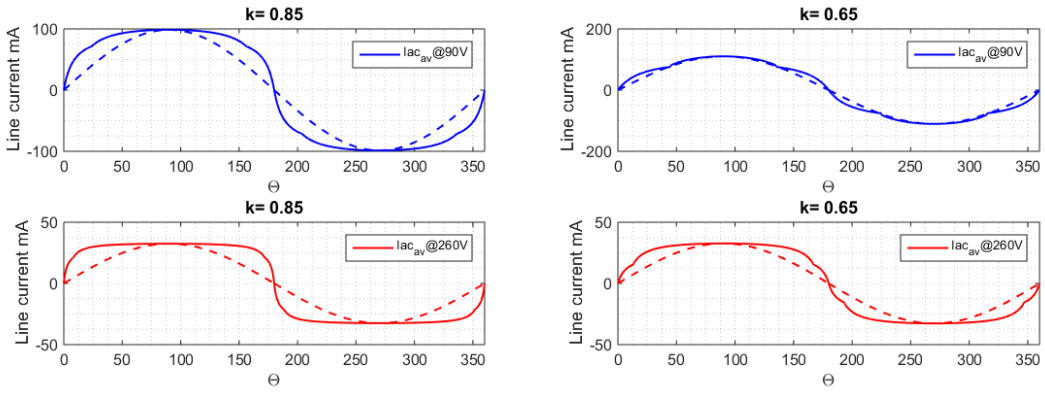
$$P_{\mathrm{in}} = \frac{1}{\pi}\int_0^{\pi} V_{\mathrm{ac}}(\theta) i_{\mathrm{ac}}(\theta) d\theta \tag{4.5}$$

solving for T_{on} using (4.5) and (4.3), this gives:

$$T_{\mathrm{on}} = \frac{2\pi P_{\mathrm{o}} L_{\mathrm{op}}/(\eta V_{\mathrm{o}})}{2k\int_0^{\theta_0} \frac{(\sqrt{2}V_{\mathrm{ac}}\sin(\theta))^2}{\sqrt{2}V_{\mathrm{ac}}\sin(\theta)+V_{\mathrm{o}}} d\theta + \int_{\theta_0}^{\pi-\theta_0} (\sqrt{2}V_{\mathrm{ac}}\sin(\theta) - V_{\mathrm{o}}) d\theta} \tag{4.6}$$

The off time of both modes of operations is given by:

$$T_{\mathrm{off}}(\theta) = \begin{cases} \frac{\sqrt{2}V_{\mathrm{ac}}\sin(\theta)-V_{\mathrm{o}}}{V_{\mathrm{o}}} T_{\mathrm{on}} & \theta_0 < \theta < \pi - \theta_0 \\ \frac{\sqrt{2}V_{\mathrm{ac}}\sin(\theta)}{V_{\mathrm{o}}} k T_{\mathrm{on}} & \text{otherwise} \end{cases} \tag{4.7}$$



(a) When $k = 0.85$ and $V_o = 20\,\text{V}$. (b) When $k = 0.65$ and $V_o = 50\,\text{V}$.

Figure 4.5: Average AC current:, V_{ac} are 90 V, 260 V for two different load voltages and constant load $P_o = 7\,\text{W}$. The dashed curves are pure sinusoidal wave. The amplitude of this wave is equal to the peak of the AC line current.

Figure 4.5a shows averaged AC line current when the design constant k is 0.85. The proposed PFC shows closely resembles a sinusoidal shape of the averaged AC line current when changing the load voltage to $V_o = 50\,\text{V}$ and $k = 0.65$, as shown in Figure 4.5b. The average line currents (solid curves) are compared with sinusoidal waves (dashed curves) for the line voltages of 90 V and 260 V, respectively. It should be noted that the minimum switching frequency occurs when the AC line voltage is at its peak (i.e., $\sin\theta = 1$); thus, the minimum switching frequency for each mode of operation (buck-boost and boost) is expressed by:

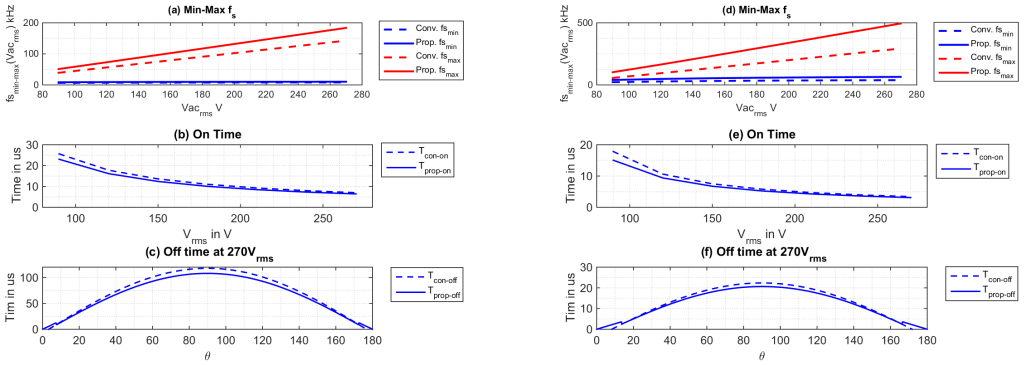
$$f_{\text{s-min}} = \begin{cases} \dfrac{V_o}{\sqrt{2}V_{ac}T_{on}} & \theta_0 < \theta < \pi - \theta_0 \\ \dfrac{V_o}{(1+\sqrt{2}V_{ac})kT_{on}} & \text{otherwise} \end{cases} \tag{4.8}$$

Besides, the maximum switching frequency is estimated when $T_{off}(\theta) = 0$, thus, it is given by:

$$f_{\text{s-max}} = \begin{cases} \dfrac{1}{T_{on}} & \theta_0 < \theta < \pi - \theta_0 \\ \dfrac{1}{kT_{on}} & \text{otherwise} \end{cases} \tag{4.9}$$

Figure 4.6 compares the minimum and maximum switching frequencies, on

time and off time of both PFCs at a constant output power of 7 W but with two different voltage and current conditions. Figure 4.6a(top) shows the range of the minimum and maximum switching frequency over the universal AC line voltage when the output voltage and current are 20 V and 350 mA, respectively. The proposed PFC does have a slightly higher switching frequency (minimum and maximum) than the conventional PFC. The reason for this deviation is that the computed on and off times of the proposed PFC are lower than the on and off times of the conventional PFC.

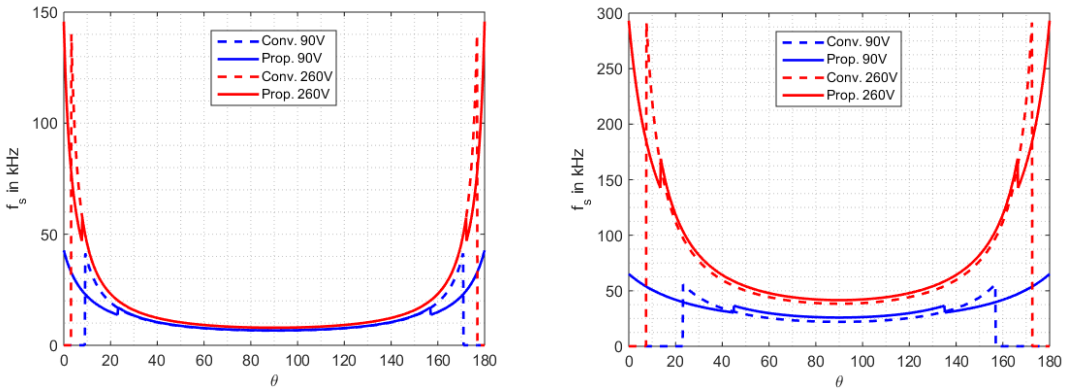


(a) When $k = 0.85$ and $V_o = 20$ V. (b) When $k = 0.65$ and $V_o = 50$ V.

Figure 4.6: Comparison of minimum and maximum switching frequencies, on time over AC line voltage range and off time of both PFCs for two different load voltages and constant load $P_o = 7$ W. The dashed curves represent the conventional buck and solid curves represent the proposed converter.

Figure 4.6a(mid) shows the computed on time of both PFCs over rms line voltage range and Figure 4.6a(bottom) shows the computed off time of both PFCs at 270 V-rms. The same discussion can be applied to Figure 4.6b which shows the curves when the load conditions are 7 W, 50 V and 150 mA.

Figure 4.7 shows the changing of the switching frequency over the positive half cycle of the AC line voltage for PFCs. The solid curves illustrate the switching frequencies of the proposed PFC and the dashed curves illustrate the switching frequencies of the conventional PFC with a 7 W output power but with two different voltage/current conditions. Figure 4.7a shows the switching frequencies when



(a) When $k = 0.85$ and $V_o = 20\,\text{V}$.

(b) When $k = 0.65$ and $V_o = 50\,\text{V}$.

Figure 4.7: Switching frequency over the positive half cycle of the line voltage, for low and high line voltage and for two different load voltages and constant load $P_o = 7\,\text{W}$. The dashed curves represent the conventional buck and the solid curves represent the proposed converter.

$V_o = 20\,\text{V}$ and $i_o = 350\,\text{mA}$ and Figure 4.7b shows the switching frequencies when $V_o = 50\,\text{V}$ and $i_o = 150\,\text{mA}$.

4.3.2 Power Factor and Harmonics Analysis

The power factor is given by:

$$\lambda = \frac{P_{\text{in}}}{V_{\text{ac-rms}} I_{\text{ac-rms}}} \tag{4.10}$$

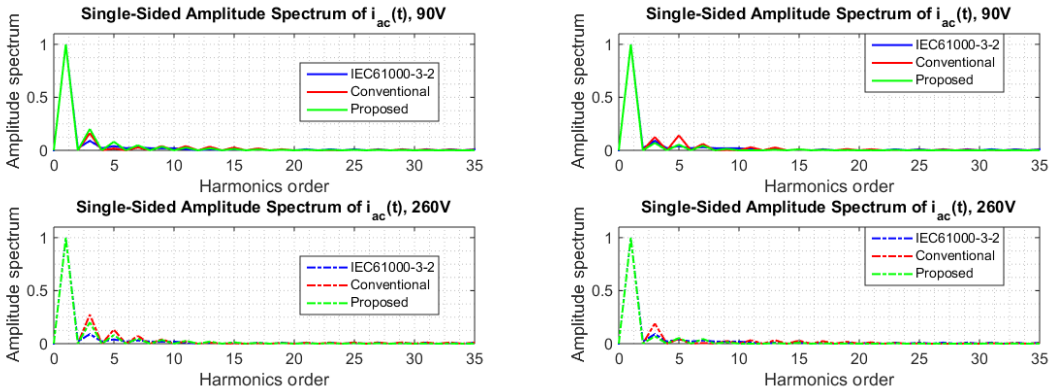
and $I_{\text{ac-rms}}$ is the RMS value of the AC line current which is obtained as follows:

$$I_{\text{ac-rms}} = \sqrt{\frac{1}{\pi}\int_0^{\pi} (\overline{i_{\text{ac}}}(\theta))^2 d\theta} \tag{4.11}$$

Then, the Total Harmonics Distortion (THD) is estimated by:

$$THD = \sqrt{(\frac{cos(\phi)}{\lambda})^2 - 1} \tag{4.12}$$

where ϕ is the phase shift caused by the input filter and which is assumed to be zero, so that increasing the phase shift between the AC line voltage and current decreases the PF. The zero phase shift can be achieved by the proper selection of the input filter's parameters; λ is the power factor computed by (4.10).



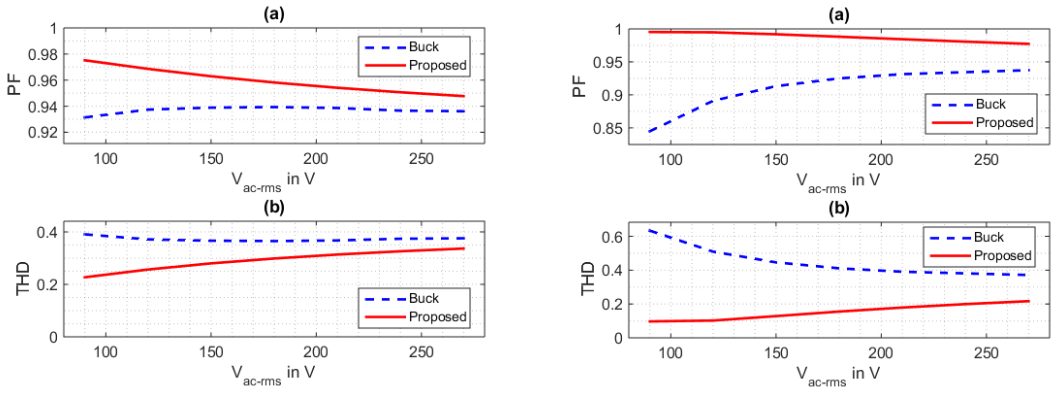
(a) When $k = 0.85$, $V_o = 20\,\text{V}$.

(b) When $k = 0.65$, $V_o = 50\,\text{V}$.

Figure 4.8: Single-sided amplitude spectrum for two different load voltages and constant load $P_o = 7\,\text{W}$ relative to fundamental FFT value.

The Fast Fourier Transform (FFT) analysis has been applied to the AC line current of conventional PFC (red curves), proposed PFC (green curves) together with standard $IEC61000-3-2$ limits (blue curves), as shown in Figure 4.8, for low and high AC line voltages. The normalized harmonics (relative to fundamental) of the line current changes with changing the load conditions. Adjusting the load voltage changes the on time value, thus affecting the average AC line current, as shown in Figure 4.5. The line current of the proposed PFC shows lower harmonics contents than that of a conventional one when the load voltage is 50 V, as shown in Figure 4.8b.

The computed power factor and total harmonic distortion for both the conventional buck PFC (Figure 4.1a) and proposed hybrid PFC (Figure 4.2) are shown in Figure 4.9a and Figure 4.9b. The power factor of the hybrid PFC is higher than the conventional buck PFC over the AC line voltage. Moreover, the power factor of the hybrid PFC is higher than that of the conventional buck PFC at low AC



(a) $k = 0.85$, $V_o = 20\,\text{V}$, $P_o = 7\,\text{W}$. (b) $k = 0.65$, $V_o = 50\,\text{V}$, $P_o = 7\,\text{W}$.

Figure 4.9: Comparison between the topologies: a. PF, b. THD.

line voltage and for two load voltages. As a result of improving the power factor, the THD of the hybrid PFC is lower than the THD of the conventional buck PFC, and it is reduced compared to the conventional buck PFC at low AC line voltage.

4.4 PFC Loss Analysis

The loss components of the conventional and proposed PFC converters are broken down. The losses are identified as follows: Conduction losses, switching losses, gate losses, copper losses of the output inductor and core losses of the output inductor. The loss computations are based on the constant load of 7 W, 20 V and 350 mA. Because of the symmetry between the positive and negative half cycles of the AC line voltage, the following analysis has been done for one half of the line frequency and the results are doubled for losses throughout the fundamental period.

4.4.1 Conduction Losses

The conduction losses per switching cycle in the proposed converter are divided as follows:

1. The conduction losses in the diode D_{p} is given by:

$$E_{\text{cond-Dp}} = \begin{cases} (V_{\mathrm{fd}} I_{\text{L2-av}} + R_{\mathrm{fd}} I^2_{\text{L2-rms}}) T_{\mathrm{on}} & \theta_0 < \theta < \pi - \theta_0 \\ (V_{\mathrm{fd}} I_{\text{L1-av}} + R_{\mathrm{fd}} I^2_{\text{1-rms}}) k T_{\mathrm{on}} & \text{otherwise} \end{cases} \tag{4.13}$$

where V_{fd} is the forward voltage of the diode at zero current, R_{fd} is the differential resistance of the diode, $I_{\text{L1-av}}$ and $I_{\text{L2-av}}$ are the average inductor current and $I_{\text{L1-rms}}$ and $I_{\text{L2-rms}}$ are the RMS values of the inductor currents, depending on the mode of operation. It should be noted that the conduction energy of the conventional buck PFC is twice the amount of the first case of the energy computed by (4.13), because it has two diodes, both of which conduct (D_{p1} and D_{p2}, see Figure 4.1a) during the on time of the operating switch.

2. The conduction losses in the controlled switches: The conduction energy loss can be estimated as presented in Section 2.2.1. But it should be noticed that the proposed inverter has different modes of operations. Thus, the operating switch and synchronous switch must be defined. For the positive half cycle of the AC line voltage:

   - The switches Q_{Ap} and Q_{Bp} are acting as operating switches, depending on the mode of operation; Thus, the conduction loss energy of those switches is estimated by (2.1), where T_{on} is computed by (4.6) and $i_{\text{o-n}}$ is replaced by the inductor current $I_{\text{L1-av}}$ and $I_{\text{L2-av}}$.
   - The switch Q_{op} acts as a synchronous switch in all modes of operation within the positive half of line voltage. Thus, the conduction loss energy is estimated by (2.7), where T_{off} is computed by (4.7) and $i_{\text{o-n}}$ is replaced by the inductor current $I_{\text{L1-av}}$ and $I_{\text{L2-av}}$.
   - The switches Q_{An} and Q_{Bn} are operated at the line frequency. The conduction loss energy is estimated by (2.1) with $T_{\mathrm{on}} = T_{\mathrm{mod}}$.

The conduction loss power is computed by:

$$P_{\text{cond-t}} = 2f_{\text{mod}} \int_0^{0.5T_{\text{mod}}} (E_{\text{cond-Dp}} + E_{\text{Q-Ap}} + E_{\text{Q-Bp}} + E_{\text{Q-op}} + \\ + E_{\text{Q-An}} + E_{\text{Q-Bn}})dt \tag{4.14}$$

4.4.2 Switching Losses

The proposed converter operates Critical Conduction Mode (CRM) with Constant On Time (COT). The procedure to compute the switching losses of the proposed converter is the same one used to compute the switching losses in hard switching cases. (More detail is presented and discussed in Section 2.2.2.) It should be noted that operating the proposed converter under CRM with COT eliminates the reverse recovery losses of the body diode of switch Q_{op} zero current turn off. Thus, (2.15) is zero in this case. The switching power losses are given by:

$$P_{\text{sw-t}} = 2f_{\text{mod}} \int_0^{0.5T_{\text{mod}}} E_{\text{sw-n}}dt \tag{4.15}$$

where $E_{\text{sw-n}}$ is the total switching energy per switching cycle, and the components of this energy are shown in Table 4.2.

Table 4.2: Switching energy components.

Component	equation	more detail see
Switching on energy during $t_{\text{fv-new-n}}$	$E_{\text{onMv-n}} = \int_0^{t_{\text{fv-new-n}}} v_{\text{ds}}(t) i_{\text{p-n}} dt$	2.18
Switching on energy during $t_{\text{ri-new-n}}$	$E_{\text{onMi-n}} = \frac{1}{2} v_{ds} i_{\text{p-n}} t_{\text{ri-new-n}}$	2.19
The energy drawn from the supply to charging the output capacitance	$E_{\text{oss-n}} = Q_{\text{oss}}(v_{\text{ds}}) v_{\text{ds}}$	2.17
The energy off due to snubber capacitance	$E_{\text{offM-n}} = \frac{(i_{\text{p-n}} t_f)^2}{24 C_{\text{t}}}$	

$i_{\text{p-n}}$ is the inductor current and it is computed based on the mode of operation as presented in (4.2) and (4.1). C_{t} is the sum of the non-linear output capacitance of the switches in each mode and the parasitic capacitance of L_{o} and the measuring device if presented.

4.4.3 Gate Drive Losses

The gate drive loss component is shown in Table 4.3.

Table 4.3: Gate drive power loss components - positive half cycle of AC line voltage.

Switch	Power loss	
Q_{Ap}	$P_{\mathrm{Ap}} = 2f_{\mathrm{mod}} \int_0^{t_1} E_{\text{g-S}} dt$	t_1 is the duration of 1^{st}buck-boost mode
Q_{op}	$P_{\mathrm{op}} = f_{\mathrm{mod}} \int_0^{0.5T_{\mathrm{mod}}} E_{\text{g-S}} dt$	
Q_{Bp}	$P_{\mathrm{Bp}} = f_{\mathrm{mod}} \int_0^{t_2} E_{\text{g-S}} dt$	t_2 is the duration of buck mode
Q_{Bn}	$P_{\mathrm{Bn}} = E_{\text{g-S}} f_{\mathrm{mod}}$	

where $E_{\text{g-S}}$ is the gate drive energy loss which is computed by (2.32). Then, the total gate drive loss is given by:

$$P_{\text{g-t}} = 2(P_{\mathrm{Ap}} + P_{\mathrm{op}} + P_{\mathrm{Bp}} + P_{\mathrm{Bn}}) \tag{4.16}$$

4.4.4 Total Losses

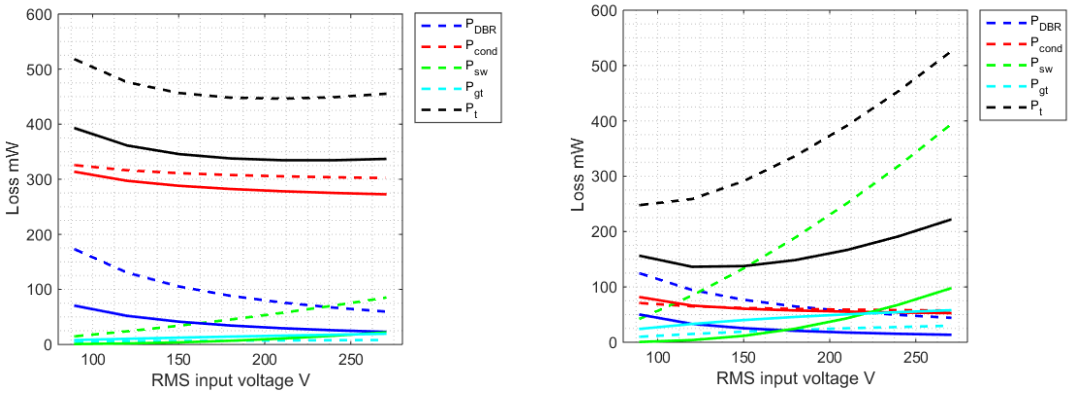
The total loss in the proposed converter is given by:

$$P_{\mathrm{t}} = P_{\text{cond-t}} + P_{\text{sw-t}} + P_{\text{g-t}} \tag{4.17}$$

Figure 4.10 compares the computed loss components of both topologies: the first one is the conventional PFC Figures 4.1a (all dashed curves). The second,one is the proposed PFC Figures 4.2 (all solid curves). Two different load voltage/current conditions have been applied for this comparison.

Both Figures 4.10a and 4.10b show that the proposed PFC has lower total losses than the conventional PFC. The on time of the proposed PFC is lower than the conventional PFC, hence, the conduction loss of the switches in the proposed PFC is lower than the same losses in the conventional PFC (red curves). Additionally, the conduction loss in the DBR of the conventional PFC is higher

than the same losses in the proposed PFC (the number of diodes are reduced in the proposed PFC), as depicted in the blue curves.



(a) When $k = 0.85$, $V_o = 20\,\text{V}$, $P_o = 7\,\text{W}$. (b) When $k = 0.65$, $V_o = 50\,\text{V}$, $P_o = 7\,\text{W}$.

Figure 4.10: Comparison between loss components. Dashed curves represent the loss components of conventional buck PFC and the solid curves represent the loss components of proposed PFC. All computations based on constant output power of 7 W for two different load voltages.

The switching losses of the conventional PFC are higher than the proposed PFC. As the on time of the proposed PFC is lower, this reduces the peak inductor current of the proposed PFC, thus, reducing the switching losses (green curves). Finally, the gate losses of the proposed PFC are slightly higher than the conventional PFC (cyan curves).

4.5 Control Requirements

4.5.1 Control of the Conventional Buck PFC

The converter shown in Figure 4.1a is controlled as illustrated in Figure 4.11. The voltage divider, containing R_3 and R_4, detects the output voltage. The feedback is connected to an inverting error amplifier with reference voltage V_{ref}. The feedback of the error amplifier contains R_{fb} and C_{fb}. The output of the error amplifier is

compared with the saw-tooth voltage (V_{ramp}) which defines the conduction time (T_{on}) of the operating switch Q_1.

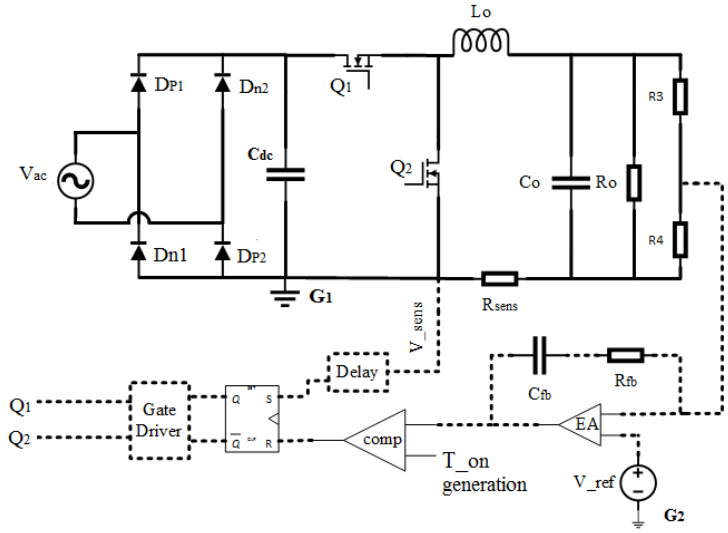


Figure 4.11: Control schematic for conventional buck PFC.

The inductor current is detected two times per switching cycle forcing the controller IC to generate the proper timing signals as follows:

- The on time T_{on} is generated by an IC controller. A resistance is connected between IC's pin (which is named set pin) to ground to set the charging current of the capacitance. This capacitance is connected from the ramp pin to the ground. The inductor current reaches its peak value at the end of the conduction time of Q_1.

- During the conduction of the synchronous switch Q_2, the inductor current ramps down to zero. At the zero crossing instant Q_2 is gated off.

As illustrated in Figure 4.11, the inductor current is sensed by detecting the voltage to the ground across the sensing resistance R_{sens} which is connected through the returning path of the inductor current. Then, the output signals of the previously mentioned process are connected to the gate driver to generate proper synchronized gating signals.

4.5.2 Control of the Proposed PFC

In addition to the previously mentioned control procedure in Section 4.5.1, one more aspect is needed to control the proposed converter. The switches Q_{An} and Q_{Bn} are operated at the line voltage frequency (in the positive half cycle of the line voltage). Conversely, the switches Q_{Ap} and Q_{Bp} in the negative half cycle of the line voltage and at line voltage frequency. Thus, the boundary voltage V_{b} determines the instant of turning on/off of the anti-series switches within the path of the inductor current. Hence, a voltage divider is connected in parallel across the supply to sense the input voltage.

When the input voltage is lower than the boundary voltage, the switch Q_{Bn} is gated on. After the sensing input voltage exceeds the boundary voltage, the switch Q_{An} is gated on until the input voltage decreases below the boundary voltage again forcing Q_{Bn} to turn on once more in this half cycle of the line voltage.

Chapter 5

Efficiency Enhancement

In this chapter, the options to enhance the efficiency of the previously presented topologies (HSI, ARCPI and PFC) are discussed and presented.

5.1 Efficiency Enhancement of HSI Topology

The suggestions to enhance the efficiency of HSI are discussed in this Section. Therefore, the different loss causes are studied in detail. Conduction losses are not avoidable because they are caused by the on state voltage of the power switch. To reduce the switching losses, the optimization of dead times (turn on dead time of the operating and synchronous switches in the single leg of the inverter) is discussed. Finally, the potential of a resonant gate drive to reduce the gate drive losses is investigated.

5.1.1 Conduction and Switching Losses

Table 5.1 shows the computed single leg conduction losses for the selected high blocking voltage and low blocking voltage MOSFETs [15, 56] and IGBT [19] (with an external diode as stated in the data sheet) at 10 % of the maximum load power. The IGBT has higher conduction losses compared to the MOSFETs. Moreover, the low blocking voltage MOSFET has higher conduction loss compared with the high blocking voltage MOSFET, because the conduction losses have been

computed at two different load currents as shown in Table 5.1. The conduction losses are independent of DC link voltage as discussed in Section 2.2.

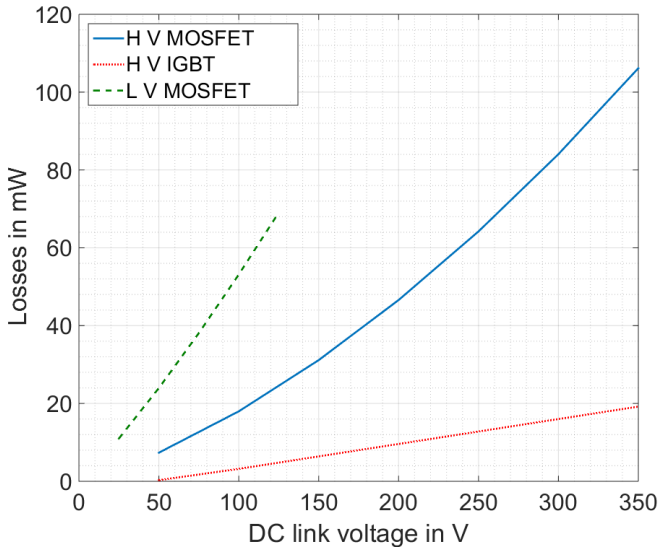


Figure 5.1: Single leg computed switching losses of some selected switches. Where HV MOSFET is [15], LV MOSFET is [56] and HV IGBT is [19] with external diode at 10 % of maximum power.

Table 5.1: Computed conduction losses for different switches, single leg of the inverter.

Switch	Conduction losses in mW	Load current in mA-peak
HV MOSFET [15]	22.31	150
LV MOSFET [56]	43.42	300
HV IGBT [19]	89.6	150

Figure 5.1 shows the computed single phase switching losses, mainly depending on the switch's input and output capacitances and the load current. The switching losses of the MOSFET are higher than those of the IGBT over the full DC link voltage range. This is because the output capacitances of the selected MOSFETs ([15][56]) are higher than those of the selected IGBT [19] which can be seen in the data sheets. Also, the HV MOSFET [15] has lower switching losses than the LV MOSFET [56], because HV MOSFET has lower output capacitance. Moreover,

the load current in the HV MOSFET prototype is half of the load current of the LV MOSFET prototype.

The inverter in this study is used to drive an extremely light load. The load current is very low; hence, the MOSFETs have lower conduction losses than the IGBTs. The switching frequency is set to (20 kHz). However, the switching losses of the IGBTs are lower than the MOSFETs.

5.1.2 Dead Time Optimization

With HSIs, dead time optimization is of the utmost importance. Dead time (or interlock time) denotes the duration of the time interval in which both switches in the single leg of the inverter are off. Non-optimized dead times affect the switching behavior of the semiconductor device; and thus the efficiency of the inverter. Increasing dead times also causes disturbances in the waveforms, hence increasing the Total Harmonic Distortion (THD) [57, 58].

This subsection discusses the effect of dead dime adjustments and optimizations for efficiency improvement. The following discussion is based on the assumption of positive load current (i.e., current flows out of the inverter phase leg into the load). Thus, the upper switch S_1 is referred to also as the operating switch and the lower switch S_2 is termed the synchronous switch. Conversely for negative load current the switches S_2 and S_1 are termed the operating and synchronous switches, respectively.

Turn on Dead Time of the Operating Switch

The operating switch S_1 is in the off state (its body diode and channel block the DC link voltage) while the synchronous switch S_2 conducts the load current in the reverse direction with its channel gated on. Once the gate source voltage of S_2 has fallen below the threshold voltage V_{th2}, the current starts flowing in the lower body diode and the reverse recovery charge (Q_{rr}) starts to accumulate. The

reverse recovery charge keeps accumulating until the gate source voltage of S_1 is equal to a value above the threshold. At this point, the current in its channel equals the load current and the lower body diode current reverses the polarity, extracting the previously built up reverse recovery charge. After extracting a sufficient amount of reverse recovery charge, the lower MOSFET's body diode regains its blocking capability and the drain to source the voltage of the upper switch starts decreasing.

The effect of changing turn on dead time on the switching transition of the inverter can be summarized as follows, [57–59]:

- Normally, the turn on dead time of both switches is set by half bridge drivers. This delay prevents any cross conduction in the single phase leg, ensuring the two switches conducting alternatively.

- Too long of a delay increases the body diode conduction losses and causes more accumulated reverse charge.

- To avoid both the cross conduction and accumulation of the reverse recovery charge, the operating switch S_1 should be turned on as soon as the synchronous switch S_2 is turned off. In other words, the ideal delay time is found when both gate to source voltages reach their threshold voltages at the same time.

Figure 5.2 shows the measured gate source voltages of both switches of the LV MOSFET prototype. Further discussion is given in Section 6.1.2. Figure 5.2 also shows the drain currents of both switches at the turning on of the operating switch. The arrow in the figure indicates the optimum switching point, i.e., the optimum instant to turn on the operating switch (upper switch).

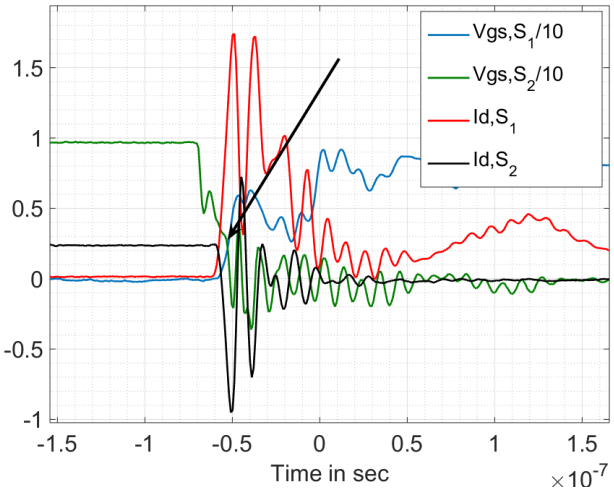


Figure 5.2: Measured optimum instant for turning on of the operating switch S_1, $V_{\text{gs,S1}}$ is the S_1 gate source voltage scaled by 1/10 and $V_{\text{gs,S2}}$ is the S_2 gate source voltage scaled by 1/10, and the drain currents of the two switches, as illustrated in Figure 2.1, LV MOSFET prototype.

The switching on and off energies of both MOSFETs after adjusting the turn on dead time can be computed by:

$$E_{\text{onM-n}} = E_{\text{onMi-n}} + E_{\text{onMv-n}} + E_{\text{oss-n}} + E_{\text{add}} \tag{5.1}$$

$$E_{\text{offM-n}} = E_{\text{offMi-n}} + E_{\text{offMv-n}} + E_{\text{oss-n}} \tag{5.2}$$

where E_{add} is the energy lost due to the parasitic capacitance of the load (i.e., winding capacitance of the machine and instrument input capacitance, if present).

Turn on Dead Time of the Synchronous Switch

While turning on the synchronous switch transition, it is important to set a longer turn on dead time of the synchronous switch to allow for the load current to charge the output capacitance of S_1 and to discharge the output capacitance of S_2, i.e., avoiding charging/discharging these capacitances through the channels.

Before turning on the synchronous switch, the positive load current is conducted by the operating switch channel while the synchronous switch is off. The

upper MOSFET output capacitance is discharged, whereas the lower MOSFET output capacitance is charged to V_{dc}. After turning off the operating switch, the output current starts charging and discharging the upper and lower MOSFET output capacitances, respectively. The voltage rise time at the point of turning off the operating switch can be approximated by:

$$t_{\text{r-v}} = \frac{V_{\mathrm{dc}} C_{\mathrm{load}} + 2Q_{\mathrm{oss}}(V_{\mathrm{dc}})}{i_{\mathrm{o}}} \tag{5.3}$$

where Q_{oss} is the non-constant output charge of the switch. C_{load} is the constant parasitic capacitance of the load. This capacitance has been measured by applying two pulse tests to the single inverter leg. i_{o} is the load current.

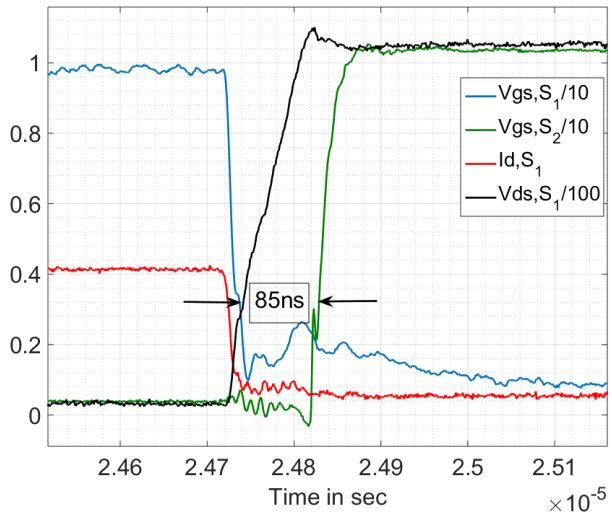


Figure 5.3: Measured optimum instant for turning on the synchronous switch S_2, $V_{\mathrm{gs,S2}}$ is the S_2 gate source voltage, scaled by 1/10. $V_{\mathrm{gs,S1}}$ and ,$V_{\mathrm{ds,S1}}$ are the S_1 gate source voltage and drain source voltage, scaled by 1/10 and 1/100, respectively, $I_{\mathrm{d,S1}}$ denotes the drain current of S_1, as illustrated in Figure 2.1, LV MOSFET prototype.

Figure 5.3 shows the gate source voltages of both switches of the LV MOSFET prototype as well as the drain source voltage and the drain current of the operating switch S_1 at turn on of the synchronous switch S_2. Further discussion is given in Section 6.1.4. As can be seen from the waveforms depicted, the turn on dead time for the given operating point needs to be set to 85 ns.

According to the aforementioned discussion, adjusting the operating switch turn on dead time can reduce the amount of reverse recovery charge seen in the switch current; thus, improving the phase leg efficiency. Adjusting the turn on delay time of the synchronous switch results in avoiding the dissipation of energy stored in the output capacitance, within the channel as well as conduction of the body diode, thus, improving the efficiency of the single leg of the inverter.

The switching energy of the single leg of the inverter after adjusting the turn on dead time of the synchronous switch, the energy components of (2.20) and (2.28), respectively, can be computed by:

$$E_{\text{onM-n}} = E_{\text{onMi-n}} + E_{\text{onMv-n}} + E_{\text{onrr-n}} + E_{\text{oss-n}} + E_{\text{add}} \tag{5.4}$$

$$E_{\text{offM-n}} = \frac{(i_{\text{o-n}} t_{\text{fi-new-n}})^2}{24(C_{\text{oss}}(v_{\text{ds1}}) + C_{\text{oss}}(v_{\text{ds2}}) + C_{\text{load}})} \tag{5.5}$$

Optimizing Turn on Dead Times of both Switches

As discussed above, optimizing the turn on dead time of the operating switch can avoid part of the reverse recovery charge. Optimizing turn on dead time of the synchronous switch avoids dissipating the energy stored in the output capacitance within the switch's channels.

Optimizing both turn on dead times of the operating and synchronous switches simultaneously does the aforementioned loss reductions. Hence, the energy lost in the single leg of the inverter, when turn on dead times for both switches in the single leg of the inverter which are optimized, can be estimated by:

$$E_{\text{onM-n}} = E_{\text{onMi-n}} + E_{\text{onMv-n}} + E_{\text{oss-n}} + E_{\text{add}} \tag{5.6}$$

$$E_{\text{offM-n}} = \frac{(i_{\text{o-n}} t_{\text{fi-new-n}})^2}{24(C_{\text{oss}}(v_{\text{ds1}}) + C_{\text{oss}}(v_{\text{ds2}}) + C_{\text{load}})} \tag{5.7}$$

5.1.3 Gate Drive Losses

The computed gate drive losses for the single leg of the inverter are summarized in Table 5.2 (the computed gate drive losses for two switches). This loss component has a considerable high influence on the overall efficiency in the case of applications with high switching frequencies and extremely light load ranges, especially at low DC link voltages. Therefore, a Resonant Gate Drive (RGD) circuit is introduced.

Table 5.2: Computed gate drive losses, single leg of the inverter at 20 kHz.

Switch	Gate drive losses in mW
HV MOSFET [15]	11.6
LV MOSFET [56]	2.6
HV IGBT [19]	54.3

As shown in Table 5.2, the gate drive loss of the LV MOSFET is the lowest because the lowest total gate charge.

5.1.4 The Resonant Gate Drive (RGD)

Many RGD typologies have been introduced and discussed. Most of these works focused on applications with switching frequencies between 500 kHz and 1.5 MHz (e.g., [60–66]). In this study, the RGD circuit which was proposed in [66] has been

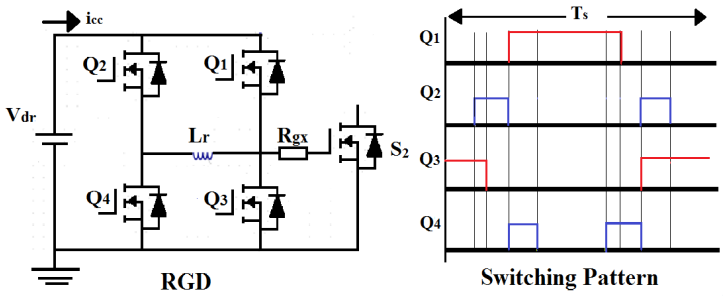


Figure 5.4: RGD circuit as proposed in [66] (left), switching pattern (right).

employed to reduce the gate drive losses (Figure 5.4 (left)). It is important to select the most suitable switches for the RGD circuit. To select the best fitting

switch for the driving circuit, the same procedure as specified in [66] has been followed. In the RGD, the losses are mainly conduction and gate drive losses, where the switching losses are not considered because the RGD is a soft switching topology operating at nearly zero switching losses.

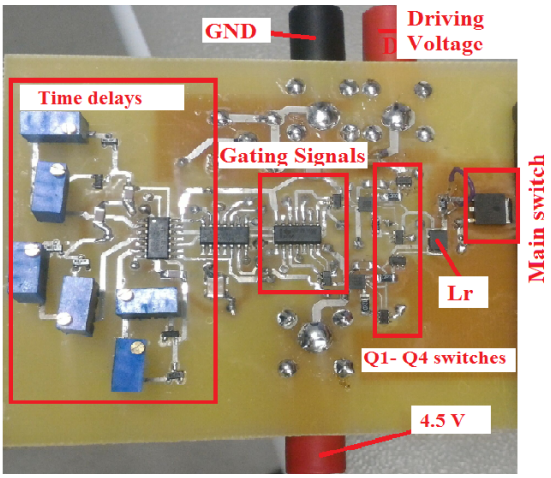


Figure 5.5: The RGD prototype.

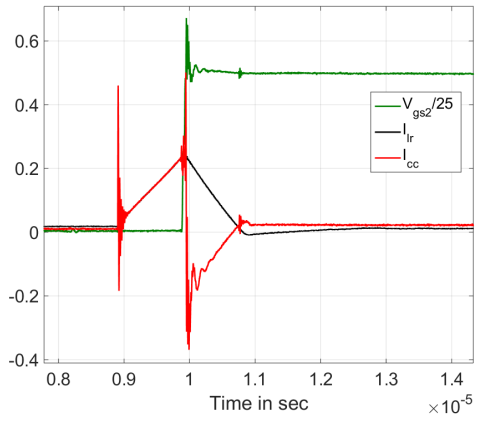


Figure 5.6: Measured turn on waveforms of main MOSFET, S_2 using the RGD.

To select the inductor (L_r), the following should be considered: Firstly, it should have low DC internal resistance to reduce the resistive losses in the circuit. Secondly, the current rate in the inductor ($\frac{di}{dt}$) should be lower than that of the selected RGD's MOSFETs, ensuring low switching losses. Thirdly, the peak current capability of the inductor must be higher than the charging/discharging current of the main gate MOSFET ((2.12) and (2.24), respectively).

As proposed from the topology, the inductor current ramps down to zero as soon as Q_2 and Q_4 are turned off (Q_2 is turned off first then Q_4 is turned on). But, as shown in Figure 5.6, the inductor current (black curve) decreases below zero. This is due to the output capacitance of the selected driving MOSFET of the RGD (the driving MOSFET is Si3588DV [67]). Then, the inductor current approaches zero while circulating through Q1 and the body diode of Q2. Figure 5.6 shows the measured gate source voltage of the main switch (green curve, scaled by 1/25), and the supply current (I_{cc}, red curve). The negative supply current results in recovery of energy stored in the inductor.

5.2 Efficiency Enhancement of ARCPI Topology

To improve the overall efficiency of the ARCPI, the contributions of each loss component is investigated separately as follows:

5.2.1 Option 1: New Control Sequence

The switching losses of the auxiliary switches are a combination of the following:

- Discharging of the non-linear output capacitance of these switches at turn on of the auxiliary switches.
- The energy stored in the inductor at turn off of the auxiliary switch (due to the reverse recovery current (3.44) and the energy computed by (3.41)).
- The energy stored in the non-linear output capacitance of the auxiliary switches (at turn off) (See (3.48); this energy is dissipated in the channel of A_2 at the beginning of mode 7).

Actually, in a conventional control sequence of an ARCPI, the auxiliary switches are turned on and off at different times per switching cycle (i.e., A_1 during the positive inductor current and A_2 during the negative indcutor current). However, in this research, the auxiliary switches are turned on simultaneously. The turn off sequence of the auxiliary switches is optimized as follows:

The reverse conducting auxiliary switch (A_2 in sequence 4) is turned off just before the zero crossing of the resonant inductor current, thus reducing the reverse recovery current and the associated losses (this discussion is valid for MOSFETs. Further reduction of the reverse recovery charge can be achieved by reducing the boost current). The second auxiliary switch is turned off after the zero crossing, allowing for the oscillation to decay smoothly. Furthermore, the body diode of the auxiliary MOSFET will conduct together with the channel (As long as $i_{\text{o-n}} R_{\text{on}} < V_{\text{f}}$, both the body diode and the channel of the MOSFET will be conducted at

the same time if the channel is gated on). Thus, this parallel connection reduces the conduction losses in the commutation circuit.

5.2.2 Option 2: Skipping one of the Auxiliary Pulses

Throughout this approach, a positive load current direction is assumed, as shown in Figure 3.1. During sequences 1 and 2, the inductor L is energized. This energy is subsequently transferred to the total capacitance $C_{3\mathrm{t}}$ during the resonance mode 3. Thus, the upper main switch M_1 is softly turned on.

Conversely, M_1 can be turned off softly by optimizing the turn on dead time of the lower main switch M_2. This dead time allows the load current to charge the non-linear output capacitance of M_1 and discharge the non-linear capacitance of M_2. This enables an avoidance of charging/discharging these capacitances through the channels (see 5.1.2). The use of this option is limited by the load current value. To ensure ZVS in case of this extremely light load, the current limit should be greater than 2 % of $i_{\text{o-peak}}$ which is estimated by (5.8). (For the variables' definitions, refer to Table 3.2.)

$$i_{\text{o-min}} = \frac{V_{\text{dc}} C_{\text{load}} + 2Q_{\text{oss}}(V_{\text{dc}})}{t_{\text{r-v-max}}} \tag{5.8}$$

As a result of this optimization, it is possible to omit the sequences from $(7-9)$ (while A_1 and A_2 remain switched off), and conversely for negative load current (flowing into the ARCP). Figure 3.2d illustrates the previous description and Figure 3.2e shows the load voltage and inductor current when applying this option.

Operating the ARCP (single leg of ARCPI) based upon this assumption causes an imbalance in the charge which is drawn from the DC capacitances C_{dc}, node Mid in Figure 3.1 (more charge is drawn from the bottom DC capacitor and is returned to the top one for a positive inductor current). This charge is canceled

out during the negative output current cycle. In three phase systems, balancing the charge partly takes place between the single legs as well.

5.2.3 Option 3: Adjusting the Boost Current

The boost current is modified by adjusting the instant of turning off the main switch M_2, i.e., the duration of $t_1 + t_2$ as shown in Figure 3.2c. Thus far, this duration has been assumed to be constant during the fundamental period, as presented in, e.g., [20, 21, 23]. The third option proposes changing the boost current sinusoidally according to the load current so as to reduce the commutation circuit losses by properly adjusting the duration of $t_1 + t_2$. However, the boost current to load current ratio is not constant: Around the zero crossing of the load current, the boost current must be set to some minimum so as to provide enough energy to energize the resonant inductor, and thereby enable full soft turn on of M_1.

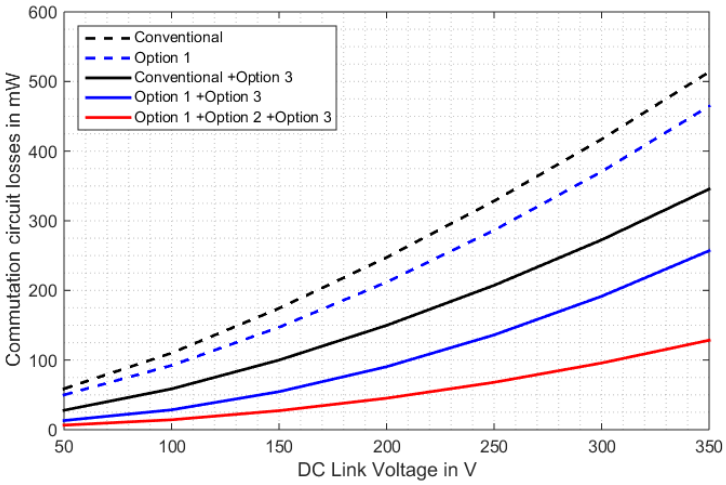


Figure 5.7: The commutation circuit losses when adjusting the boost current (ARCPI-3). The legend (top-bottom): conventional switching with $I_{\text{b-n}} = 3.5i_{\text{o-peak}}$, proposed switching with $I_{\text{b-n}} = 3.5i_{\text{o-peak}}$, conventional switching with $I_{\text{b-n}} = 3.5i_{\text{o-n}}$, proposed switching with $I_{\text{b-n}} = 3.5i_{\text{o-n}}$ for proposed switching with $I_{\text{b-n}} = 3.5i_{\text{o-n}}$ plus skipping one of the auxiliary pulses per switching cycle.

Figure 5.7 compares the commutation circuit losses for two cases: First, the boost current is assumed to be constant within one fundamental period ($I_{\text{b-n}} =$

$3.5i_{\text{o-peak}}$, dashed curves). Second, the boost current is adjusted according to the sinusoidal load current ($I_{\text{b-n}} = 3.5i_{\text{o-n}}$, and $i_{\text{o-n}} = i_{\text{o-peak}} \sin(2\pi f_{\text{line}} tn)$, solid curves). Additionally, Figure 5.7 shows the commutation circuit losses in both cases: conventional switching sequence (black curves), proposed switching sequence (blue curves) and the red curve shows the commutation loss when applying options $1-3$ together. It should be noted that the commutation circuit losses are reduced when operating them under the proposed switching sequence.

5.2.4 Option 4: The RGD

As gate drive losses have a significant impact on the total losses in case of light loads, the resonant gate drive circuits have been introduced to reduce the gate drive losses. More details are presented in Section 5.1.4. Table 5.3 summarizes the gate drive losses for the cases of a homogeneous and a hybrid ARCP.

Table 5.3: Computed gate drive losses for ARCP, at 20 kHz.

Main Switches	Auxiliary Switches	Gate drive losses in mW
MOSFET A [15]	MOSFET A [15]	27.18
MOSFET A [15]	IGBT C[19]	67.86

5.3 Efficiency Enhancement of PFC Topology

In addition to the proposed converter, this thesis presents a method to improve both the efficiency and the performance of the conventional buck PFC or even the proposed converter.

5.3.1 An Improved Critical Conduction Mode with Constant On Time

According to [55], the operating switch Q_1 is only turned on under ZVS as soon as the input voltage is less than double the output voltage. In order to achieve ZVS turn on of Q_1 within the line frequency, this thesis suggests the following:

The synchronous switch Q_2 keeps conducting after the inductor current crosses zero. This allows the inductor current to decrease to a boost value and store some energy in the inductor. Thus, when Q_2 is gated off, resonance between the output inductor L_o and the non-linear output capacitances of both switches takes place and transfers the energy between these passive components. As a result, Q_1 can be turned on at Zero Voltage Switching (ZVS).

The boost current can be estimated analytically by estimating the sufficient energy to be stored in the inductor for resonance. Thus, it is given by:

$$E_{\text{Lo-stored}} = \int_0^{V_{\text{over}}} vC_{\text{oss}}(v)dv - \int_0^{2V_\mathrm{o}} vC_{\text{oss-t}}(v)dv \tag{5.9}$$

where $V_{\text{over}} = \sqrt{2}V_{\text{ac}}\sin(2\pi f_{\text{mod}}t) > 2V_\mathrm{o}$, $C_{\text{oss-t}}$ is the total non-linear output capacitance ($C_{\text{oss-t}} = C_{\text{oss1}}(V_{\text{ds1}}) + C_{\text{oss2}}(V_{\text{ds2}})$). The energy stored in the inductor is given by:

$$E_{\text{Lo-stored}} = \frac{1}{2}L_\mathrm{o}I_{\text{boost}}^2 \tag{5.10}$$

solving for I_{boost} yields:

$$I_{\text{boost}} = \sqrt{\frac{2E_{\text{Lo-stored}}}{L_\mathrm{o}}} \tag{5.11}$$

The synchronous rectification switch (Q_2) conducts for a longer time after the zero crossing instant. This time is estimated by:

$$t_{\text{delay-on}} = L_{\text{o}} \frac{I_{\text{boost}}}{V_{\text{o}}} \tag{5.12}$$

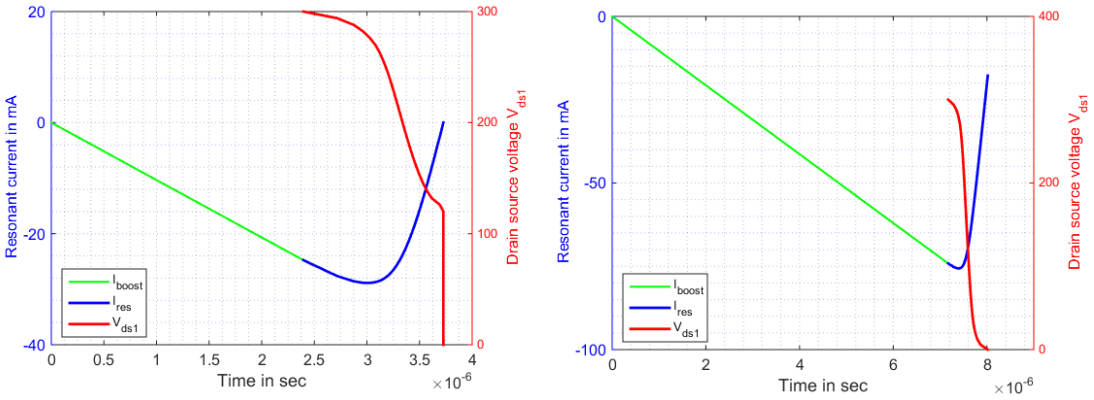
As shown in Figure 5.8, the inductor current decreases to the boost value as long as Q_2 conducts (the green curve). At the boost value, Q_2 is gated off and the resonance starts. The drain source voltage of Q_1 decreases during this period. Figure 5.8b shows the inductor current within the resonant period. The boost current is not high enough to turn on Q_1 under ZVS, but increasing the boost current (absolute value) leads to turning on Q_1 under ZVS, as shown in Figure 5.8a.

The switching energy $E_{\text{sw-n}}$ in (4.15) should be recomputed according to these resonant circumstances. Thus, the energies are computed by (2.18), (2.19), (2.15) and (2.16) are zeros. The non-linear capacitance C_{oss} plus the parasitic capacitance of L_{o} act as a snubber at turn off of the switch Q_2. The switching energy is given by:

$$E_{\text{sw-n}} = \frac{(I_{\text{Lo}} t_{\text{f}})^2}{24(C_{\text{oss}}(v_{\text{ds1}}) + C_{\text{oss}}(v_{\text{ds2}}) + C_{\text{load}})} \tag{5.13}$$

where t_{f} is the scaled current fall time and it is estimated by (2.23) and I_{Lo} is the inductor current. Then, the switching power loss is computed using (4.15).

As shown in Figure 5.9, the switching losses are significantly reduced when forcing both PFCs (conventional and proposed) to operate under resonance mode. The green curves represent the switching losses under resonance mode, whereas, the blue curves represent the switching losses in normal operation. All dashed curves are for the conventional buck PFC and the solid curves are for the proposed converter.



(a) Low boost current. (b) High boost current.

Figure 5.8: Resonant current and operating switch's drain source voltage during the resonant period.

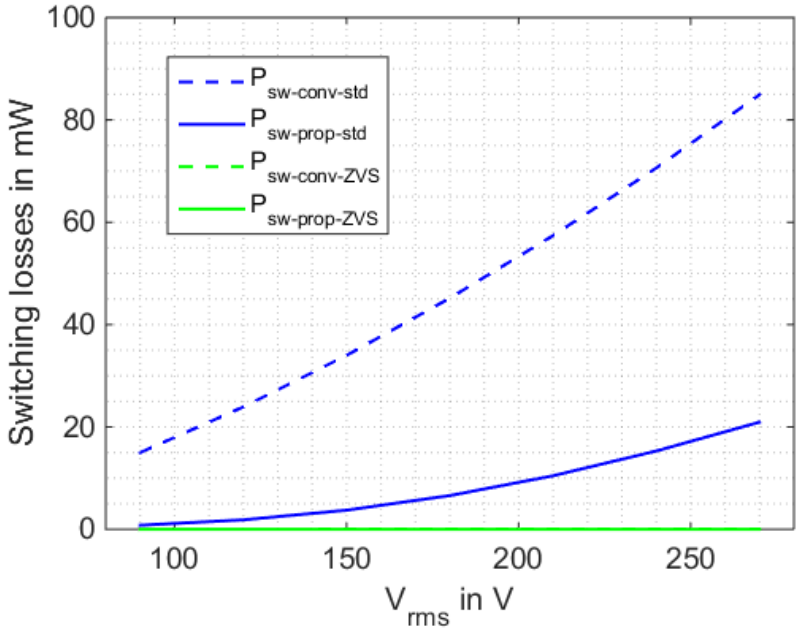
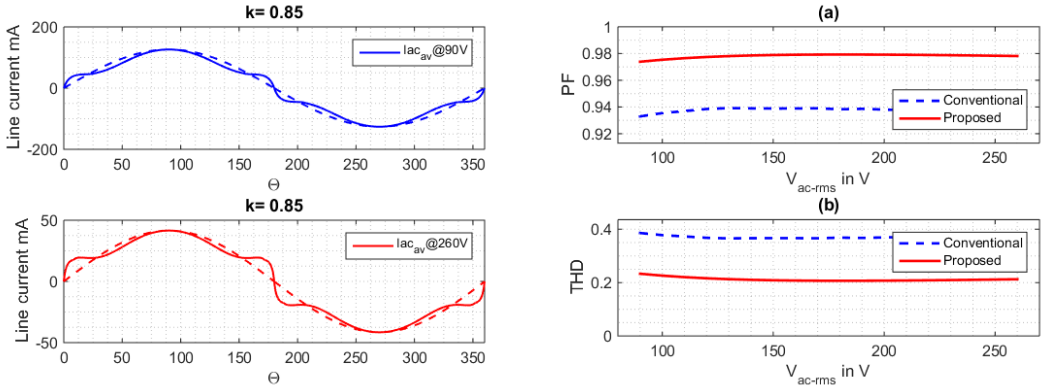


Figure 5.9: Computed switching losses.

5.3.2 Adding Additional Signal to the Constant On Time

As shown in Figure 4.5, the AC average line current deviates from the standard sinusoidal shape. This deviation is related to the on time (T_{on}, see (4.6)) is a constant within the fundamental cycle. In order to slightly change this constant



(a) An improved average AC current. (b) An improved: a. PF, b. THD.

Figure 5.10: An improved average AC line current, an improved PFC and THD due to add additional signal to the constant on time.

on time, an additional signal has been added as follows:

$$T_{\text{on-new}} = T_{\text{on}}(1 - K_3 \sin(3\omega_{\text{line}}t) - K_5 \sin(5\omega_{\text{line}}t)) \tag{5.14}$$

where K_3 and K_5 are constants and equal 0.33 and 0.05 respectively. ω_{line} is the angular line frequency. K_3 and K_5 are selected in order to achieve sinusoidal AC average line current.

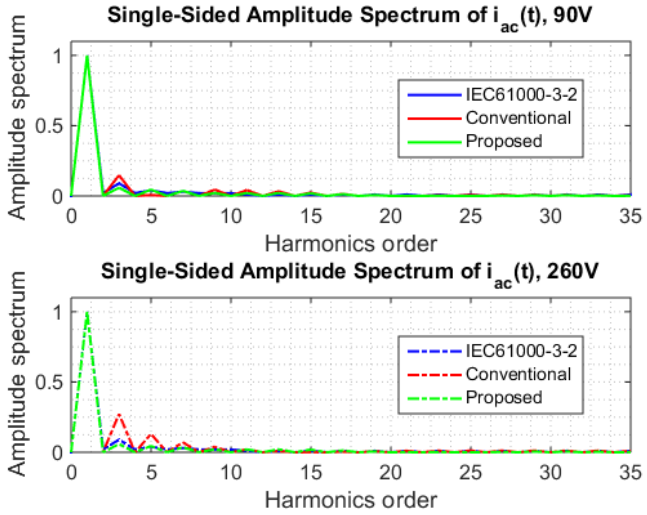


Figure 5.11: Single-sided amplitude spectrum of the AC line current relative to fundamental spectrum when adding additional signal to the constant on time, $V_{\text{o}} = 20\,\text{V}$.

The effect of this additional harmonics components can be clearly seen in the AC line current waveform as shown in Figure 5.10a. However, adding those harmonics components to the constant T_{on} causes the AC line current to be more sinusoidal compared to Figure 4.5a. Also adding those harmonics components improves the power factor of the proposed converter and thus the total harmonics distortion, as shown in Figure 5.10b. The improved power factor approaches 98 % keeping the THD around 20 % above the AC line voltage range compared with the curves shown in Figure 4.9a.

As shown in Figure 5.11, the third harmonic amplitudes of the proposed PFC are lower than the standard limits compared with the conventional buck PFC for both cases of line voltage. But the seventh and ninth harmonics of both PFCs are higher than the standard limits.

Chapter 6

Test Setup and Results Validation

6.1 Hard Switching Inverter

6.1.1 Test Circuit, Setup and Methods

Figure 6.1 shows the test circuit to measure the losses. The prototype circuit was built from a single leg of the inverter. To reduce the ripple current and achieve nearly DC load currrent, a resistance connected in series to a large inductor (10 mH) was used. A variable DC-power supply provided the DC link voltage.

The voltage and current input channels of the power analyzer (N5000) [68] were connected to the input and the load of the single phase leg as indicated in Figure 2.1. As the DC input resistance of the power analyzer voltage channel is in the range of MegOhms, its influence on the power measurement may be neglected. However, the input capacitance must be considered when comparing the measured losses with the computed losses. A constant duty cycle Pulse Width Modulation was applied to the circuit to adjust the load current.

The losses were determined as follows:

- The total losses, e.g., the sum of switching and conduction losses, of the single phase leg equal the difference of the measured input and output power.
- The switching and conduction losses were separated by taking measurements at two different switching frequencies (f_{s1} and f_{s2}) and at constant load

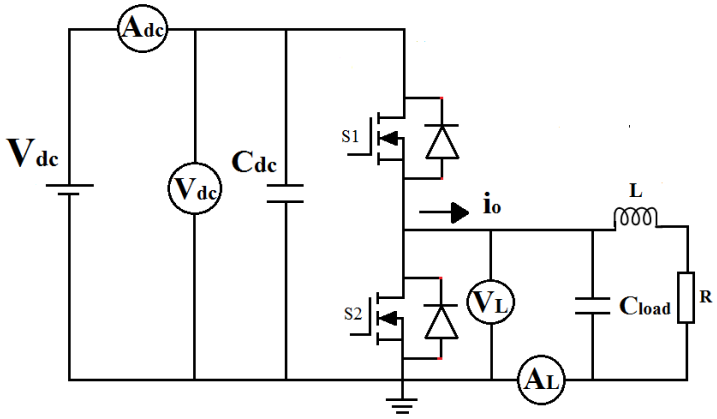


Figure 6.1: Test setup showing the power analyzer channels connected to the input and output sides of the single leg of HSI.

current. As:

$$P_{\mathrm{tm}}(f_{\mathrm{s}}) = P_{\mathrm{condm}} + f_{\mathrm{s}} E_{\mathrm{swm}} \tag{6.1}$$

where P_{tm} are the measured total losses (conduction plus switching losses), P_{condm} are the measured conduction losses, E_{swm} is the measured switching energy, which includes the energy lost due to the parasitic capacitance of both the load and the power analyzer channels [68] and the non-constant output capacitance of the two switches.

The measured switching and additional losses are calculated so that:

$$E_{\mathrm{swm}} = \frac{P_{\mathrm{tm2}} - P_{\mathrm{tm1}}}{f_{\mathrm{s2}} - f_{\mathrm{s1}}} \tag{6.2}$$

(6.2) assumes the constant switching energy and constant conduction loss (both do not change with the switching frequency).

- The measured conduction losses can be calculated by:

$$P_{\mathrm{condm}} = P_{\mathrm{tm1}} - f_{\mathrm{s1}} \frac{P_{\mathrm{tm2}} - P_{\mathrm{tm1}}}{f_{\mathrm{s2}} - f_{\mathrm{s1}}} \tag{6.3}$$

- The energy dissipated due to charging/discharging the gate capacitance is proportional to the switching frequency. This energy can be calculated similarly to the switching energy of the single leg of the inverter as given in (6.2). To estimate the power saved by the use of the RGD, the power consumption of the RGD circuit (Figure 5.4, R_{gx} shorted) is compared to the power consumption of the standard gate drive (L_{r} removed) at one switching frequency, as summarized in Table 6.3. Thus, the difference between the power consumption of the two configurations represents the power saved by the use of the RGD.

6.1.2 Experimental Results: Hard Switching Inverter

Single Leg Prototype - Low Voltage MOSFET

MOSFET type FDD6N25 [56] was selected for a load current of 300 mA, corresponding to the load current peak value at 7 W, 25 V-peak.

Figure 6.2 shows the measured (dashed curve, using a standard half bridge driver) and computed (solid curve) losses over the range of DC link voltages up to 125 V. The losses were measured using a standard hard switching drive with external gate resistance R_{gx} (L_{r} removed in Figure 5.4, dashed-dotted curve). Also, the RGD was connected to S_2 in Figure 2.1 and the losses were measured, again, in the case of the positive load current (dotted curve) and a negative load current (solid and dotted curve). For the RGD, the peak of the gate current has been adjusted to the value during the plateau interval at turn on according to (2.12) for positive and negative directions of the load current. Figure 6.2 shows how congruent the computed and measured losses are.

The turn on dead time optimization of both switches has been applied to the single leg of the inverter. The losses of the single leg of the inverter were computed in case of optimizing the turn on dead time of the synchronous switch only (Figure 6.3, solid curve) and compared to the measured losses (Figure 6.3, dashed curve).

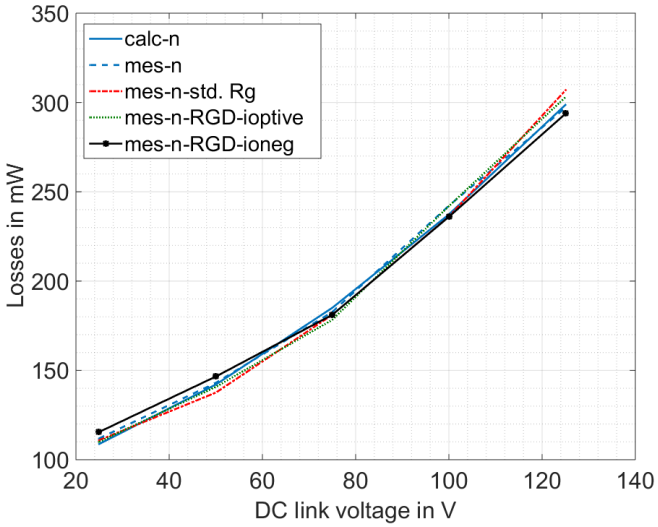


Figure 6.2: Measured and calculated conduction and switching losses LV MOSFET [56], 300 mA DC load current. The peak of the gate current has been adjusted to the value during the plateau interval at turn on according to (2.12). The explanation of the legend is summarized in Table 6.1.

Table 6.1: Legend of Figure 6.2, I_{gon} is computed by (2.12).

Legend	Meaning
calc-n	Computed losses without optimizing dead times
mes-n	Measured losses using standard half bridge driver
mes-n-std. R_{g}	Measured losses using standard hard switching drive (L_{r} removed in Figure 5.4)
mes-n-RGD-ioptive	Measured losses using RGD and positive load current
mes-n-RGD-ioneg	Measured using RGD and negative load current.

These curves are compared to the computed one without adjusting any dead time (blue curve in Figure 6.3). An excellent congruency has been achieved as seen in Figure 6.3.

Figure 6.4 shows the computed losses (solid curve) and the measured losses (dashed curve) in case of adjusting the turn on dead time of the operating switch only compared to the computed losses without adjusting any dead time (blue curve). Again a good congruency with the measured and the computed losses has been achieved in Figure 6.4.

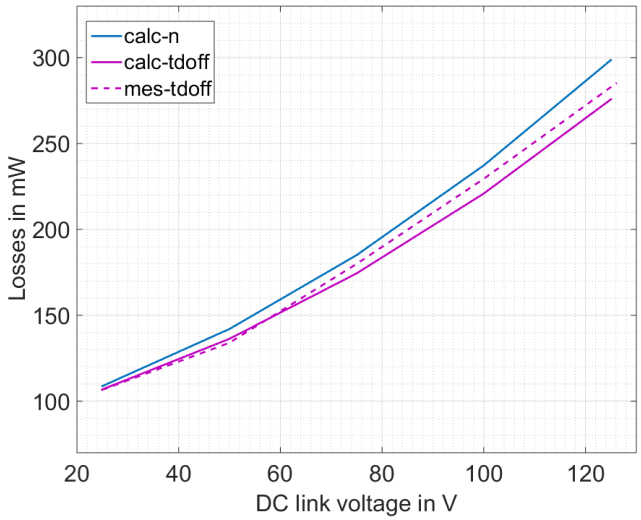


Figure 6.3: Measured and calculated conduction and switching losses LV MOSFET [56], 300 mA DC load current. Adjusting only turn on dead time of the synchronous switch.

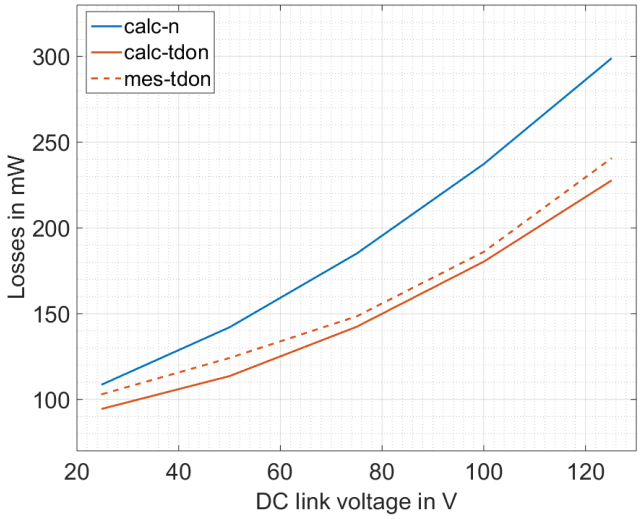


Figure 6.4: Measured and calculated conduction and switching losses LV MOSFET [56], 300 mA DC load current. Adjusting only turn on dead time of the operating switch.

Finally, Figure 6.5 compares the computed losses (solid curve) with the measured (dashed curve) when optimizing both turn on dead times for both switches. Also, it shows the measured losses when using the RGD for driving S_2 (positive load current) (dotted curve). The blue curve in this Figure shows the computed losses without optimizing any dead time. As shown in Figure 6.5, the measured

and the computed losses are congruent. Some deviation in the measured losses is due to the use of the RGD.

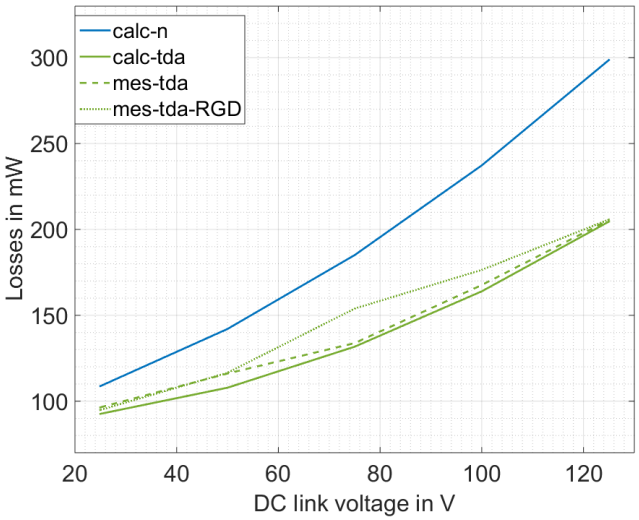


Figure 6.5: Measured and calculated conduction and switching losses LV MOSFET [56], 300 mA DC load current. Adjusting turn on dead times of both switches in the single leg of the inverter.

Single Leg Prototype - High Voltage MOSFET

MOSFET type IRFR812PbF [15] was selected for the HV prototype. The results are discussed for a DC load current of 150 mA, (corresponding to the load current peak value at 7 W and 50 V-peak) over the range of DC link voltages up to 350 V.

Figure 6.6 shows the measured (mes-n) and the computed losses (calc-n). The measurements have been conducted for the single leg of the inverter using standard half bridge gate driver (mes-n) and using RGD labelled by (mes-n-RGD). For the RGD, the peak of the gate current has been adjusted to the value during the plateau interval at turn on according to (2.12) for positive and negative directions of the load current labelled by mes-n-RGD-Igcom and mes-n-RGD-Igcom-ioneg, respectively.

To investigate the effect of changing the switching speed of the MOSFET on the losses, the peak of the gate current was increased to twice the previous

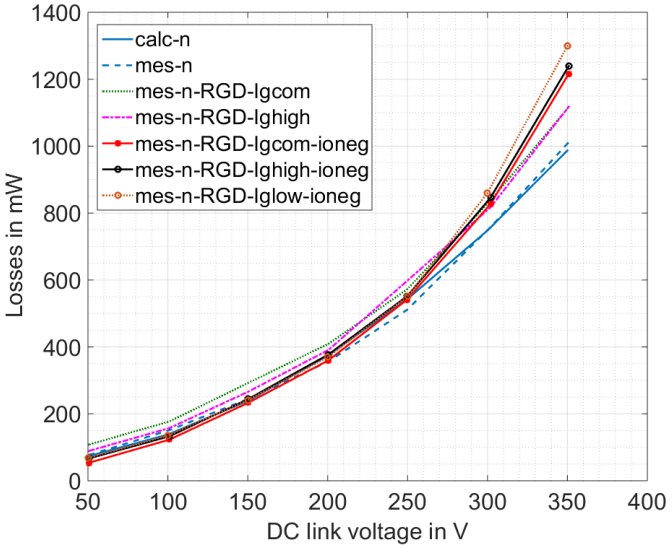


Figure 6.6: Measured and calculated conduction and switching losses HV MOSFET [15], 150 mA DC load current. The explanation of the legend is summarized in Table 6.2.

Table 6.2: Legend of Figure 6.6, I_{gon} is computed by (2.12).

Legend	Meaning
calc-n	Computed losses without optimizing the dead times
mes-n	Measured losses standard half bridge driver
mes-n-RGD-Igcom	Measured losses with RGD $I_{\text{Lr}} = I_{\text{gon}}$, i_o positive
mes-n-RGD-Ighigh	Measured losses with RGD $I_{\text{Lr}} = 2I_{\text{gon}}$, i_o positive
mes-n-RGD-Igcom-ioneg	Measured losses with RGD $I_{\text{Lr}} = I_{\text{gon}}$, i_o negative
mes-n-RGD-Ighigh-ioneg	Measured losses with RGD $I_{\text{Lr}} = 2I_{\text{gon}}$, i_o negative
mes-n-RGD-Iglow-ioneg	Measured losses with RGD $I_{\text{Lr}} = 0.5I_{\text{gon}}$, i_o negative

value according to (2.12) (by changing the delay times of of the control circuit and changing the resonant inductor value of Figure 5.4) labelled by mes-n-RGD-Ighigh and mes-n-RGD-Ighigh-ioneg, for positive and negative direction of the load current, respectively. Then, the peak of the gate current was decreased to half of its computed value labelled by mes-n-RGD-Iglow. The losses have been measured and compared to the computed losses as shown in Figure 6.6. A good congruency of the computations with the measurements has been achieved when using standard gate drive. For other measurements, a good congruency has been

achieved up to 250 V, but for higher DC link voltage than 250 V the measurements deviate from the computed losses. This is due to some oscillations introduced by connecting the RGD.

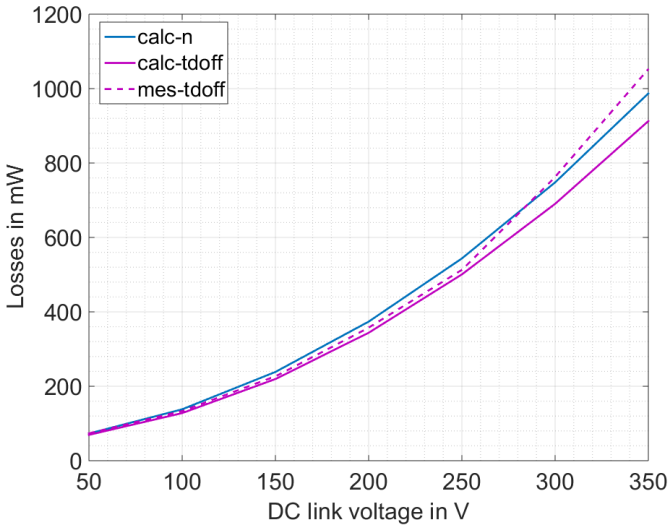


Figure 6.7: Measured and calculated conduction and switching losses HV MOSFET [15], 150 mA DC load current, adjusting only turn on dead time of the synchronous switch.

Again, the turn on dead times optimization for both switches have been applied to the single leg of the inverter. The losses of the phase leg were computed in case of optimizing the turn on dead time of the synchronous switch only (Figure 6.7, solid curve) and compared to the measured losses (Figure 6.7, dashed curve). A good congruency of the measured losses with the measured and the computed losses has been achieved.

Figure 6.8 shows the computed losses (solid curve) and the measured losses (dashed curve) in case of adjusting turn on dead time of the operating switch only.

Finally, Figure 6.9 compares the measured losses (dashed green curve) with the computed (solid green curve) when optimizing turn on dead times for both switches in the single leg of the inverter. The figure also shows also the computed losses of the single leg of the inverter without adjusting any dead time (solid blue

curve). Again, a good congruence of the measured with the computed losses is shown in Figure 6.9.

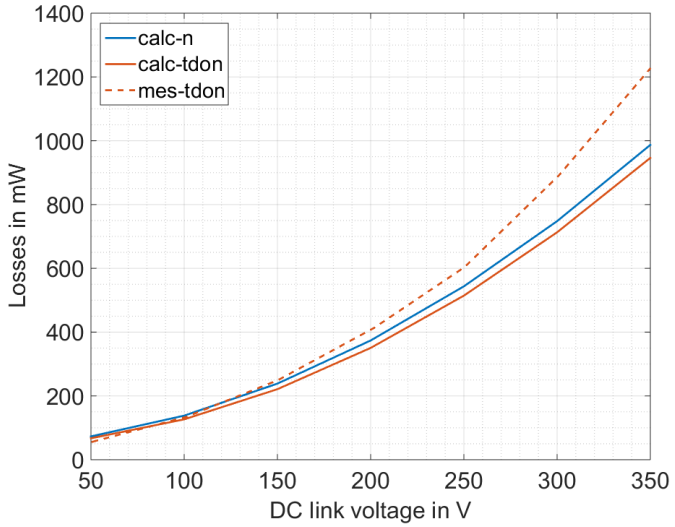


Figure 6.8: Measured and calculated conduction and switching losses HV MOSFET [15], 150 mA DC load current, adjusting only turn on dead time of the operating switch.

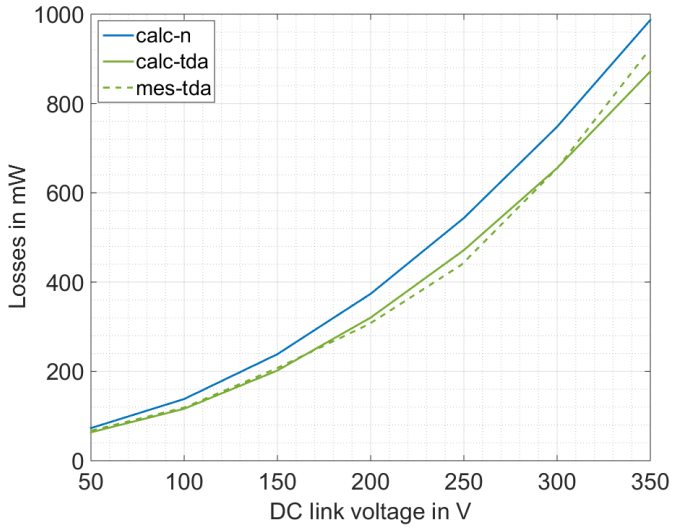


Figure 6.9: Measured and calculated conduction and switching losses HV MOSFET [15], 150 mA DC load current, adjusting turn on dead times for both switches.

6.1.3 Gate Drive Loss Measurements: Hard Switching Inverter

Finally, the gate drive losses of the operating switch were measured in case of using the RGD and compared to the gate drive losses in case of a standard hard drive. Two arrangements are used to measure the power reduction due to the use of the RGD. The power consumption is measured in case of standard hard driving (remove the inductor L_{r} in Figure 5.4) at specific switching frequency. Then, another reading was taken in case of shorting out the external gate resistance R_{gx} in Figure 5.4 at the same switching frequency. The difference between the power consumption in each configuration represents the amount of the power saved using the RGD. The results are summarized in Table 6.6.

If the internal gate resistance increases, the energy recovery by using the RGD will be decreased. Thus, above a certain value of the internal gate resistance, more energy is drawn from the supply due to the use of the RGD than using a standard hard drive [66]. For this application, experimental results show increasing gate drive losses due to the high internal gate resistance of the selected MOSFET. The results are summarized in Table 6.3 (these measurements have been conducted for a single switch of the inverter's single leg and different peak values of current needed to charge the gate (I_{gon} in (2.12))).

Table 6.3: Gate drive losses measured for HV MOSFET [15] - Single Switch at 20 kHz.

	Standard hard switching drive ($I_{\mathrm{gon}} = 185\mathrm{mA}$)	RGD-L_{r}-peak 50 mA	RGD-L_{r}-peak 200 mA
Losses in mW	5.66	6.78	8.93

Due to the switch's internal gate resistance and the peak of the resonant current of the RGD to achieve comparable switching speed, the RGD does not reduce the gate drive losses, for this MOSFET, in this application.

The gate drive losses of the LV MOSFET [56] would not be reduced because according to its datasheet it has an even higher internal gate resistance than the HV MOSFET[15].

6.1.4 Discussion: Hard Switching Inverter

Effect of the Load Capacitance "Parasitic Capacitance"

The efficiency of the designed three phase inverter was estimated at different DC link voltages by:

$$\eta = \frac{7}{7 + 3(P_{\text{cond}} + P_{\text{sw}} + P_{\text{gt}})} 100\% \tag{6.4}$$

where 7 W is the output power of the invertert (10% of the rated power), P_{cond} is referred to the single leg of the inverter conduction losses, P_{sw} is referred to the single leg of the inverter switching losses and P_{gt} is referred to the single leg of the inverter gate drive losses as discussed in Section 2.2. The sum of these losses is multiplied by 3 to estimate the total losses of the three legs of three phase inverter. These computations are based on the sinusoidal load current and PWM.

The high blocking voltage MOSFET showed better efficiency than the low blocking voltage MOSFET over the range of DC link voltages. This is because the HV prototype has lower conduction losses. It has been tested with a load current of 150 mA, whereas, the LV prototype has been tested with a load current of 300 mA. Moreover, the non-linear output capacitance of the HV MOSFET is lower than those capacitances of LV MOSFET which reduces the switching losses.

The inverter efficiency without regarding the parasitic capacitance of the load, i.e., $C_{\text{load}} = 0$, (solid curves in Figure 6.10) was higher than the inverter efficiency when taking this parasitic capacitance into consideration because of unavoidable energy lost in the parasitic capacitance of the load, C_{load} in Figure 2.1.

The parasitic capacitance of the designed load is reflected in the switching losses of the MOSFETs. The dotted curves in Figure 6.10 show the efficiency when the parasitic capacitance of the load was respected without dead time optimization, and the dashed curves show the efficiency of the inverter when turn on dead times of both switches (operating and synchronous switches) were optimized.

In both prototypes, the measurements and computations using standard gate driver are highly congruous. For the high blocking voltage MOSFET prototype, however, the measurements with RGD, especially at high DC link voltages, show some deviations which are related to the change in the circuit layout together with changing the current of the parasitic capacitance. This change might cause some additional oscillations which lead to a slight deviation in the measurements.

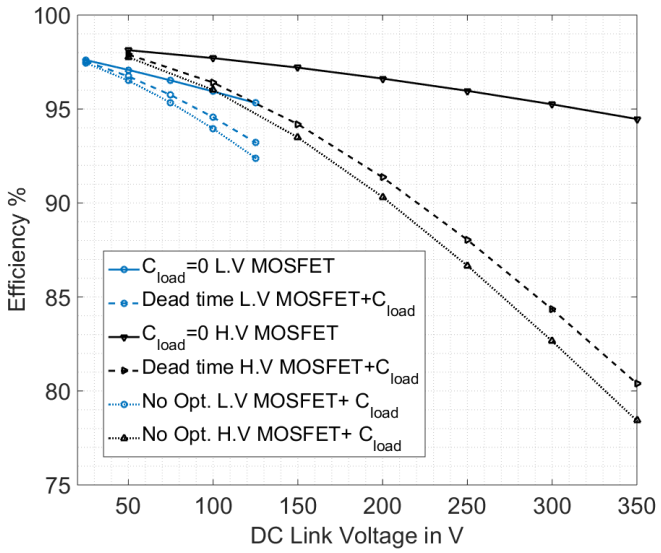


Figure 6.10: Efficiency of the designed Hard Switching Inverter using: HV MOSFET [15] (black curves) and LV MOSFET [56] (blue curves). At 150 mA and 300 mA DC load current, respectively.

Effect of the Dead Time Optimization

As seen from Figure 6.10, the efficiency of the inverter using high blocking voltage MOSFET was improved by 0.14 % at 50 V DC link voltage and by 1.97 % at 350 V DC link voltage.

The inverter efficiency using low blocking voltage MOSFET was improved by 0.08 % at 25 V DC link voltage and by 0.82 % at 125 V DC link voltage. In other words, the dead time optimization improves the efficiency with increasing effect at higher DC link voltages (as seen from Figure 6.10).

Effect of the RGD

As summarized in Table 6.3, the RGD did not improve the efficiency of the inverter because of the internal gate resistance of the used MOSFETs.

Changing the peak value of the resonant current in the RGD circuit slightly affects the conduction and switching losses of the inverter over the full range of the DC link voltage. However, the gate drive losses were increased when the RGD was used with higher resonant currents (inductor current).

6.2 ARCPI

6.2.1 Test Circuit, Setup and Methods

Figure 6.11 shows the test circuit to measure the losses. The circuit comprises one ARCP. The other details are introduced in Section 6.1.1. A high blocking voltage MOSFET type *IRFR812PbF* [15] ($ARCP-3$ as indicated in Table 6.2) has been selected for testing purposes. The resonant inductor $L = 20\,\text{uH}$. The measurement setup is discussed in detail in [32].

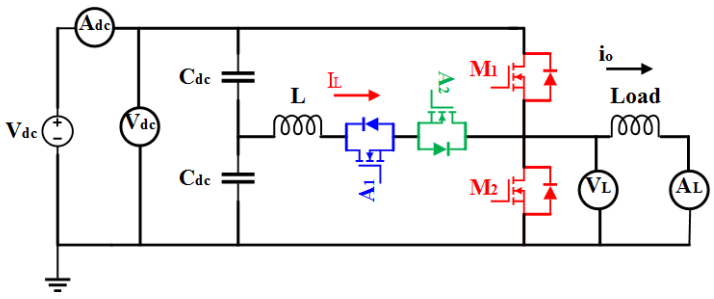


Figure 6.11: Test setup showing the power analyzer channels connected to the input and output sides of the ARCP.

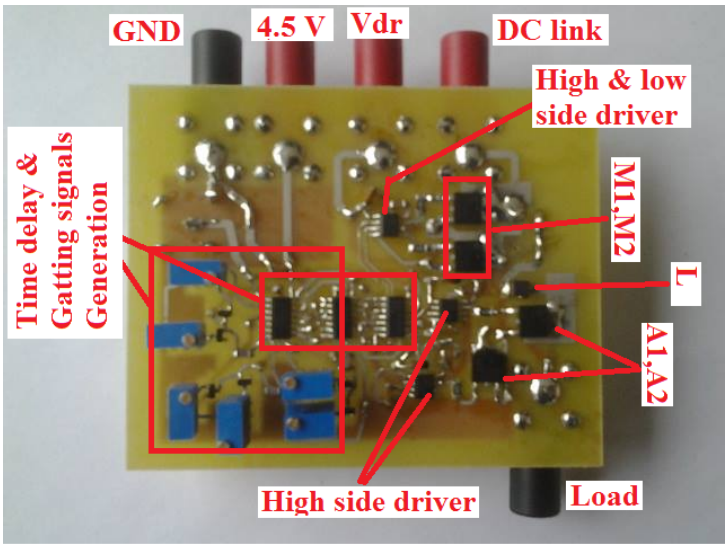


Figure 6.12: Single leg of ARCPI prototype.

The gate drive losses measurements setup are discussed in Section 6.1.3 and [32]. Figure 6.12 shows the ARCP prototype.

6.2.2 Experimental Results: Soft Switching Inverter

Waveform Analysis

Figure 6.13 shows the computed inductor current for sequences (1-5) and compares the computations with the measured positive inductor current (red dashed curve). After the inductor current crosses zero (end of sequence 5), some oscillations are started between the inductor L and the non-linear output capacitance of the auxiliary switches.

Figure 6.13 compares the computed (solid blue curve) output voltage during sequence 3 with the measured output voltage (dashed red curve). It should be noted that the proposed value of the boost current is not sufficient to reach the DC link voltage. This could correspond to the slight deviation between computed and measured waveforms at the beginning of the resonant mode. This may cause some additional losses. However, a high congruency is achieved between the computed and measured current and voltage, as shown in Figure 6.13.

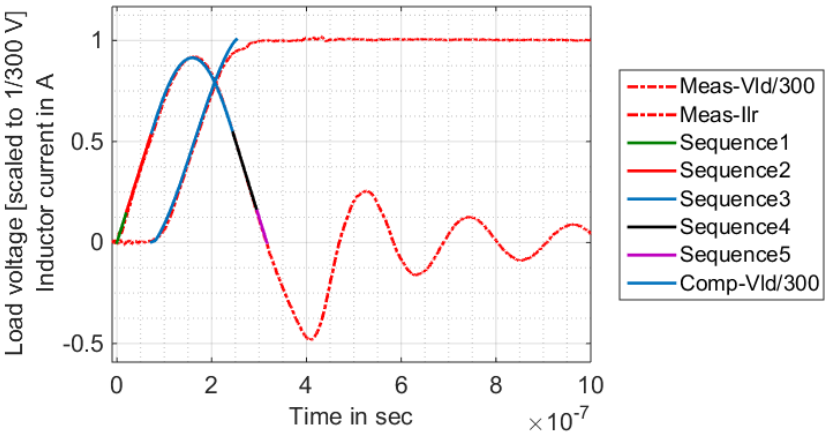


Figure 6.13: The computed (solid) and measured (dashed) inductor current, 300 V DC link voltage, 150 mA DC load current and the computed (solid) and measured (dashed) load voltage scaled to, 1/300 V DC link voltage, 150 mA DC load current.

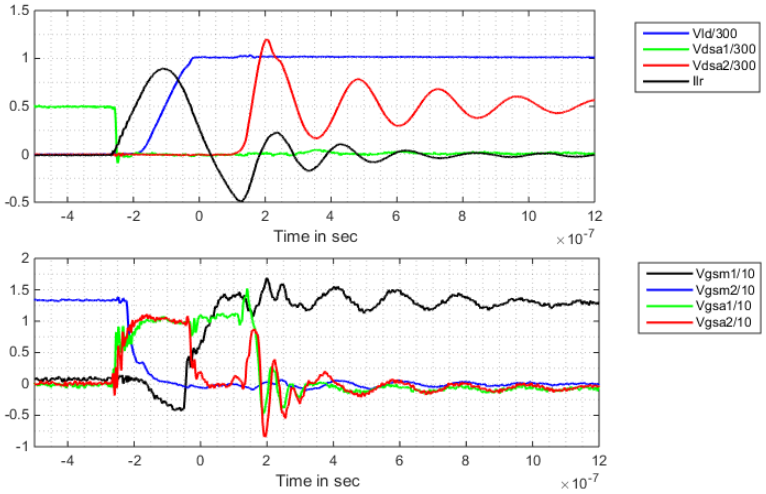


Figure 6.14: Measured waveforms at 300 V DC link voltage and 150 mA load current, based on Figure 3.1. Positive inductor current. The legend (top-bottom): V_{dsm2} is the drain source voltage of main MOSFET M_2 (load voltage) and is scaled to 1/300, V_{dsa1}, V_{dsa2} are the drain source voltages of the auxiliary switches, both are scaled to 1/300, I_{L} is the inductor L current. V_{gsm1}, V_{gsm2} are the gate source voltage of the main switches, V_{gsa1}, V_{gsa2} are the gate source voltage of the auxiliary switches. All gate source voltages are scaled to 1/10.

The top of Figure 6.14 shows the recorded waveforms of drain source voltages of the auxiliary switches (V_{dsa1}, V_{dsa2}) are depicted in the green and red curves, respectively. The load voltage (V_{ld}) is depicted in the blue curve, scaled to 1/300. The resonant current, shown in the black curve, represents the positive resonant current. The bottom Figure 6.14 shows the gate source voltages of all switches:

V_{gsm1} in black, V_{gsm2} in blue, V_{gsa1} in green, V_{gsa2} in red, respectively, all scaled to 1/10. Additionally, the figure shows the optimum instants for turning on and off of both auxiliary switches as suggested in this study (sequences 1-5). When A_2 is turned off, the inductor current decreases below zero, and increases again to zero. Then, the current shows some oscillations due to the resonance between L and the non-linear output capacitances of the auxiliary switches before returning to zero. The converse occurs during modes 7 to 9, if those pulses are not skipped, (the negative slope of the ARCP output voltage).

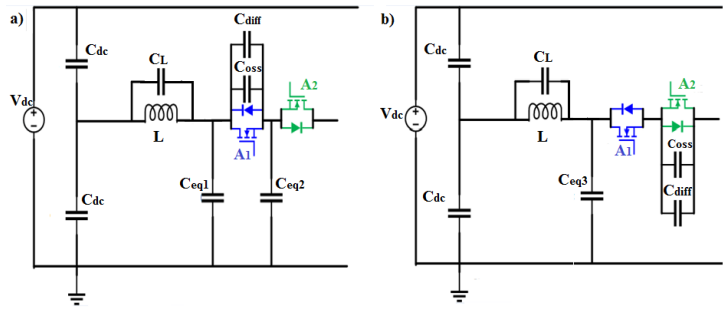


Figure 6.15: The parasitic capacitances in the commutation circuit. a) A_1 is off. b) A_2 is off. The symbols' definitions are listed in Table6.4.

Table 6.4: Symbol definitions of Figure 6.15.

Symbol	Definition
C_{eq1}	The equivelant parasitic cap between Drain A_2 to GND, which contains: $C_{\text{ly}} + C_{\text{v-g}}$.
C_{ly}	Layout capacitance (drain to ground capacitance) of A_1.
$C_{\text{v-g}}$	Capacitance to ground of the active probe.
C_{eq2}	The equivalent parasitic capacitances between common source to GND, it contains: $3C_{\text{v-g}} + C_{\text{route}} + 2C_{\text{coup}}$.
C_{route}	Route capacitance (common source to ground).
C_{coup}	Coupling capacitance from gate driver (Measured at low voltage (18 V) from source to ground).
C_{eq3}	This capacitance equals $C_{\text{ly}} + C_{\text{v-g}}$.
C_{L}	Parasitic capacitance of the resonant inductor L.
C_{oss}	Non-linear output capacitance of the switch.
C_{diff}	Differential capacitance of the active probe.

Losses Measurements

The switching plus conduction losses are computed and compared with the measured ones as shown in Figure 6.16. The measured losses are shown by the green

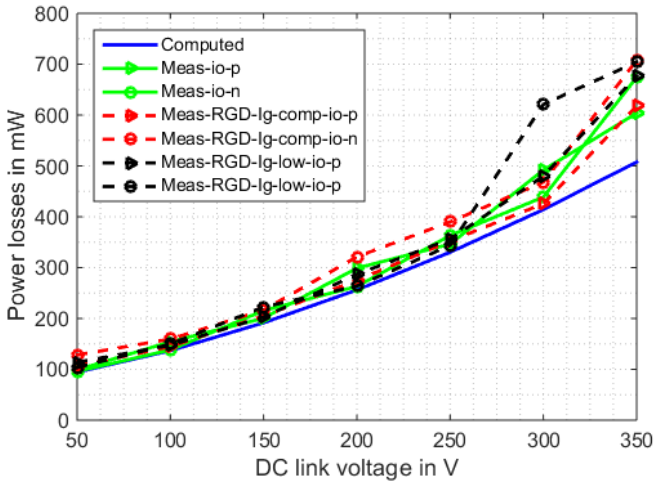


Figure 6.16: Measured and computed losses, without the driving losses, over DC link voltage and 150 mA load current (main and auxiliary switches are *IRFR812PbF* [15]). The legend is illustrated in Table 6.5.

Table 6.5: The legend of Figure 6.16. $I_{\text{gate-peak}}$ is estimated by (2.12).

Top-bottom	Description
1	Computed losses.
2	Measured losses, positive load current.
3	Measured losses, negative load current.
4	Measured losses, the RGD is connected to M_2 at $I_{\text{Lr-peak}} = I_{\text{gate-peak}}$, positive load current.
5	Measured losses, the RGD is connected to M_2 at $I_{\text{Lr-peak}} = I_{\text{gate-peak}}$, negative load current.
6	Measured losses, the RGD is connected to M_2 at $I_{\text{Lr-peak}} = 0.25 I_{\text{gate-peak}}$, positive load current.
7	Measured losses, the RGD is connected to M_2 at $I_{\text{Lr-peak}} = 0.25 I_{\text{gate-peak}}$, negative load current.

curves for both directions of the load current. The parasitic capacitances are introduced by the voltage probes, the resonant inductor and the auxiliary switches gate drivers act in parallel to the non-linear output capacitances of the auxiliary switches. Thus, their influences on the power losses are put into consideration by adding the corresponding capacitance values as shown in Figure 6.15 in (3.40).

Effect of the RGD

The RGD is connected to the gate and source of M_2. The losses are measured in both directions of the load current. The peak of the resonant inductor current of the RGD (L_r in Figure 5.4) is adjusted to reach a comparable peak of the current needed to charge the gate of M_2 (this current is estimated by (2.12)).

At this value of the peak gate current, the measured conduction plus switching losses of the ARCP are shown in Figure 6.16 in red curves for both directions of the load current. Then, the peak of the gate current of M_2 is reduced to 25 % of the value mentioned above. The losses are measured again for both directions of the load current (black curves).

As shown in Figure 6.16, the RGD only slightly affects the measurements in spite of reducing the peak of the gate current. A very good agreement between the computed losses and the measured ones has been achieved up to 250 V, but for higher DC link voltages there is slight deviations in the measurements.

Table 6.6: Gate drive losses measured for MOSFET A [15] - single switch, at 20 kHz.

	Computed	Standard hard switching drive ($I_\mathrm{gon} = 185\mathrm{mA}$)	RGD-L_r-peak 50 mA	RGD-L_r-peak 200 mA
Losses in mW	6.8	6.61	10.92	14.61

6.2.3 Gate Drive Loss Measurements: Soft Switching Inverter

Section 6.1.3 discusses the method for measuring the gate drive losses. The same procedure has been followed to measure the gate drive losses in the ARCP prototype. Table 6.6 summarizes the results. The slight deviation between the measurement in ARCP prototype case and the HS prototype case is caused by the

capacitance to ground of thew active probe. Because it was connected between the gate and the source when measuring those losses.

6.2.4 Discussion: Soft Switching Inverter

Figure 6.17 shows that the proposed switching sequence with constant boost current ($I_{\text{b-n}} = 3.5 i_{\text{o-peak}}$) improves the efficiency over the DC link voltage range if compared with the conventional switching sequence of ARCPI. Over the full range of the DC link voltage, the homogeneous ARCPI has higher efficiency than the hybrid ARCPI. Furthermore, the efficiency of the ARCPI is improved when adjusting the boost current according to the sinusoidal load current, and skipping one of the auxiliary pulses (dashed line with circles). A 95.4 % efficiency can be expected with new switching sequence, it exceeds 97 % when skipping one of the auxiliary pulses and adjusting the boost current according to the load conditions. The efficiency of the inverter is computed by:

$$\eta = \frac{7W}{7W + 3P_{\text{ARCP}}} 100\% \tag{6.5}$$

where the load power is 7 W and P_{ARCP} are the losses of the ARCP computed by (3.50).

According to Figures 5.7 and 6.17, the losses of the inverter are already very low when driving its load, because the latter is a very light load. At the operating load conditions (150 mA-peak and 50 V-peak), the losses are 320 mW, when applying the conventional switching, providing an efficiency of 95.64 %. When applying the proposed modified switching sequence (option 1), the losses are reduced by 26.8 mW, resulting in a 96 % efficiency. Furthermore, when applying options 1 to 3, the losses are further reduced to 175 mW. This reduction of 145 mW results in a 1.92 % improvement in efficiency. Table 6.7 shows the loss reductions in the inverter and the related efficiencies when applying the various options proposed

that are notably effective at the partial load conditions.

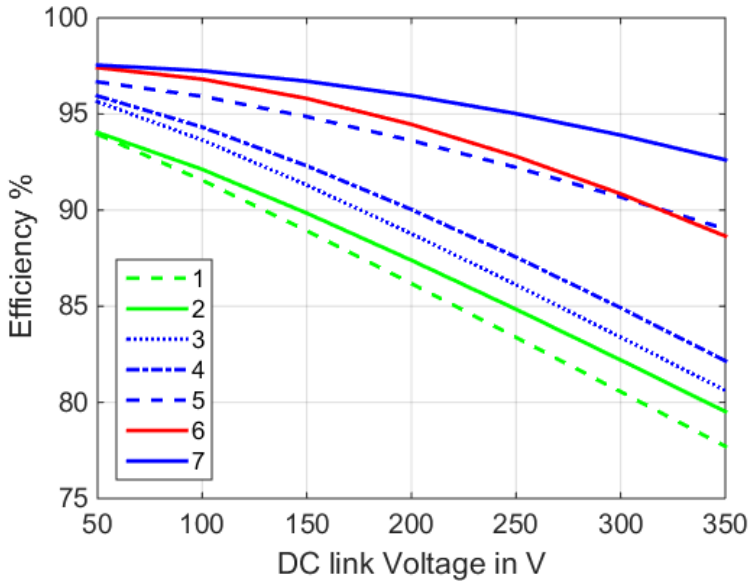


Figure 6.17: Computed efficiencies of ARCPI: ARCPI-4 (Hybrid) in green curves and ARCPI-3 (Homogeneous) all other curves as specified in Table 6.8. The legend is: (1) ARCPI-4 with conventional switching sequence, (2) ARCPI-4 with proposed switching sequence (option 1), (3) ARCPI-3 with conventional switching sequence, (4) ARCPI-3 with proposed switching sequence, (5) ARCPI-3 with options 1 and 2, (6) ARCPI-3 with options 1 and 3, (7) ARCPI-3 with options 1 to 3.

Table 6.7: Summary of overall efficiency at 7 W, 150 mA-peak and 50 V DC link voltage of both HSI and ARCPI.

Option/ Options	Loss (mW)	Loss reduction (mW)	η (%)	Improvement %
		HSI		
Conven. switching	166.2	-	97.7	-
Adjust $T_{\text{on-S1}}$	155.1	11.1	97.8	0.1
Adjust $T_{\text{on-S2}}$	155.7	10.5	97.8	0.1
Both dead times	144.6	21.6	98	0.3
		ARCPI		
Conven. switching	320	-	95.64	-
1	293.2	26.8	96	0.36
1 and 2	273.6	46.4	96.24	0.6
2 and 3	189.5	130.5	97.36	1.72
1 and 3	183	137	97.45	1.81
1 to 3	175	145	97.56	1.92

Table 6.8: ARCPI of Figure 6.17.

ARCPI	Main switches	Auxiliary switches
1	MOSFET B [56]	MOSFET A [15]
2	MOSFET B [56]	IGBT C [19]
3	MOSFET A [15]	MOSFET A [15]
4	MOSFET A [15]	IGBT C [19]

6.3 Power Factor Correction Circuit

6.3.1 Test Circuit, Setup and Methods

Figure 6.18 shows 3D model PCB of the conventional buck PFC (see Figure 4.1a). The main components are illustrated on the PCB- Figure 6.18. Table 6.9 lists the main circuit components.

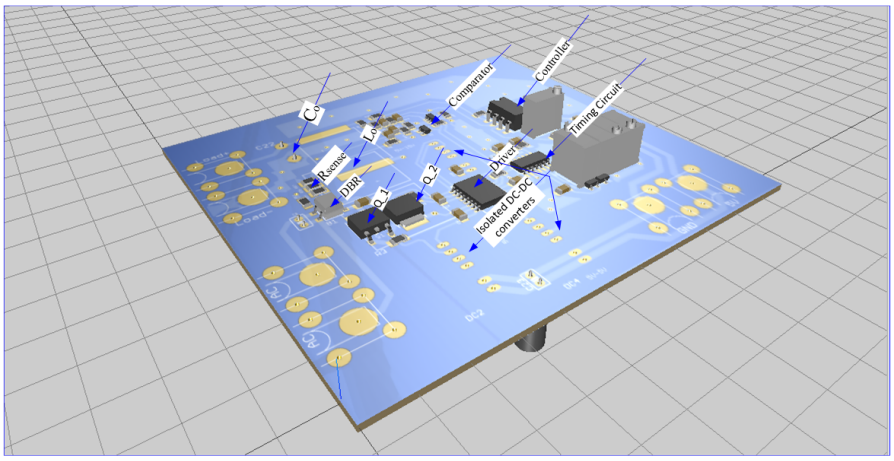


Figure 6.18: 3D model of the conventional buck PFC.

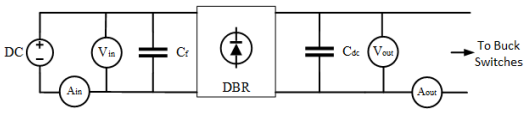
6.3.2 Experimental Results

DC Test

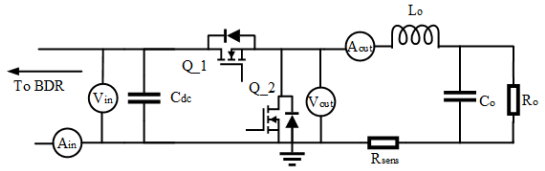
A variable DC supply up to 300 V has been connected to the board. Applying the DC test, the results can be easily validated for few switching cycles, e.g., showing

Table 6.9: Main circuit components of Figure 4.1a and Figure 6.18.

Component	Definition
Diode Bridge Rectifier	MB6S, 600 V, 500 mA
Power switches	COOLMOS $IPD65R1K4CFD$
Gate Driver	UCC21521, Isolated Dual-Channel Gate Driver with Enable
Controller IC	UC3852NG4, PFC Controller IC
Timing Circuit	74HC14, Schmitt Trigger
Comparator	TLV1391CDBVR, Analogue Comparator, Single, Differential
Output inductor L_o	60B684C-Murata power solution 3×680uH
Output capacitor C_o	200PK220MEFC16X31.5, 220 uF, 200 V
Load R_o	Constant Resistance, 59 Ω
Voltage divider to sense the rectified voltage	148.2 kΩ
Sensing resistance	0.3 Ω
Others	Four isolated DC-DC converters:
	2×R05P215s/p + R05P205s/p+IL2424s



(a) Test setup to measure the DBR losses.



(b) Test setup to measure the buck switches losses.

Figure 6.19: Test setup to measure the losses in the DBR and Buck switches by using the power analyzer.

few cycles of DC test is sufficient to proof the circuit functionality. Figure 6.19 shows the test setup to measure the losses in the diode bridge rectifier (Figure 6.19a) and the losses in the buck switches (Figure 6.19b). The voltage and current channels of the power analyzer [68] have been connected as shown in Figure 6.19.

The on time of the operating switch is computed by:

$$T_{\text{on-dc}} = 2\frac{P_{\text{o}}L_{\text{o}}}{\eta V_{\text{o}}(V_{\text{dc}} - V_{\text{o}})} \tag{6.6}$$

The peak of the inductor current is given by:

$$I_{\text{L-peak-dc}} = \frac{(V_{\text{dc}} - V_{\text{o}})T_{\text{on-dc}}}{L_{\text{o}}} \tag{6.7}$$

Then, the off time of the operating switch and the switching time are given by, respectively:

$$T_{\text{off-dc}} = \frac{(V_{\text{dc}} - V_{\text{o}})T_{\text{on-dc}}}{V_{\text{o}}} \tag{6.8}$$

$$T_{\text{s-dc}} = T_{\text{on-dc}} + T_{\text{off-dc}} \tag{6.9}$$

where P_{o} is the output power, L_{o} is the output inductor, η is the circuit efficiency V_{o} is the output voltage, $T_{\text{s-dc}}$ is the switching time. The driver does have a minimum dead time which is 150 ns.

Figure 6.20 shows few switching cycles of some measured waveforms. As soon as the operating switch Q_1 is gated on the inductor current ramps up to its peak. During T_{on}, the inductor is being energized. At the end of this transition, the inductor current is high enough to discharges the output capacitance of Q_2, hence, the synchronous switch Q_2 is turned on under ZVS (as seen in Figure 6.22). During the conduction time of Q_2 (T_{off}), the inductor current ramps down to zero. The controller IC detects the zero crossing instant of the inductor current Figure 6.21a and sends a signal to the driver to turn off Q_2 and after some delay which is set by the driver, switch Q_1 is gated on, as shown in Figure 6.21b. This is hard turn on of Q_1. Table 6.10 compares the measured turn on, turn off times and the inductor peak current with the computed ones.

Table 6.10: Comparison of T_{on}, T_{off} and $I_{\text{L-peak}}$ at 90 and 150 V.

	T_{on}	T_{off}	$I_{\text{L-peak}}$
Computed-90V	23.4usec	74.8usec	770 mA
Measured-90V	24.4usec	72.5usec	768 mA
Computed-150V	12.5usec	74.6usec	775 mA
Measured-150V	13.2usec	74.8usec	770 mA

In order to reduce the switching losses in the conventional buck PFC, as proposed in Section 5.3.1, Q_2 conducts for longer time, this increases the negative

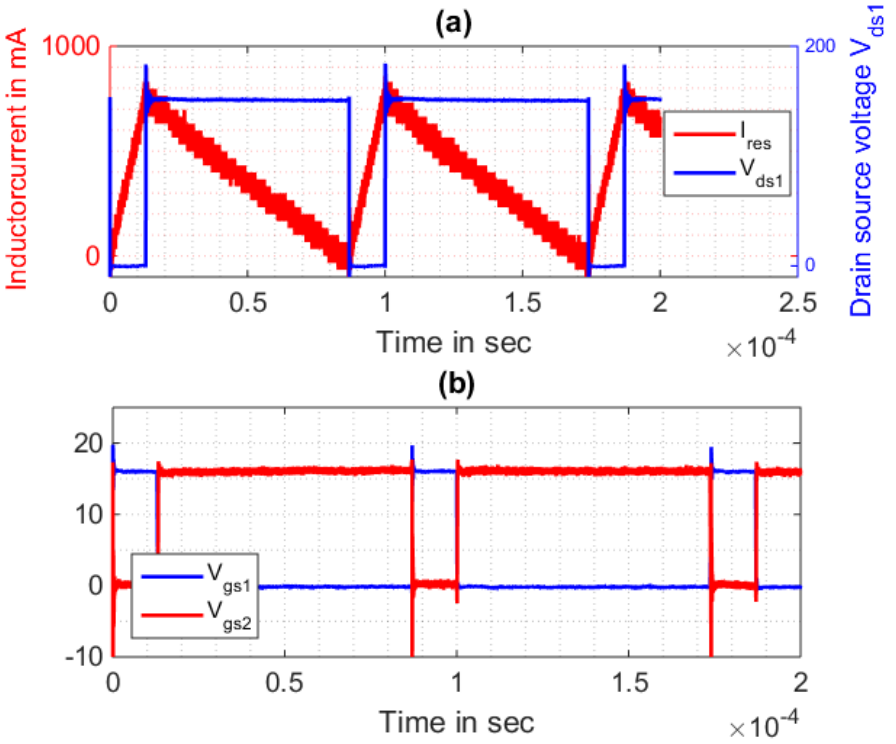


Figure 6.20: (a) Drain source voltage of Q_1 and inductor current. (b) Gate source voltages at 150 V DC.

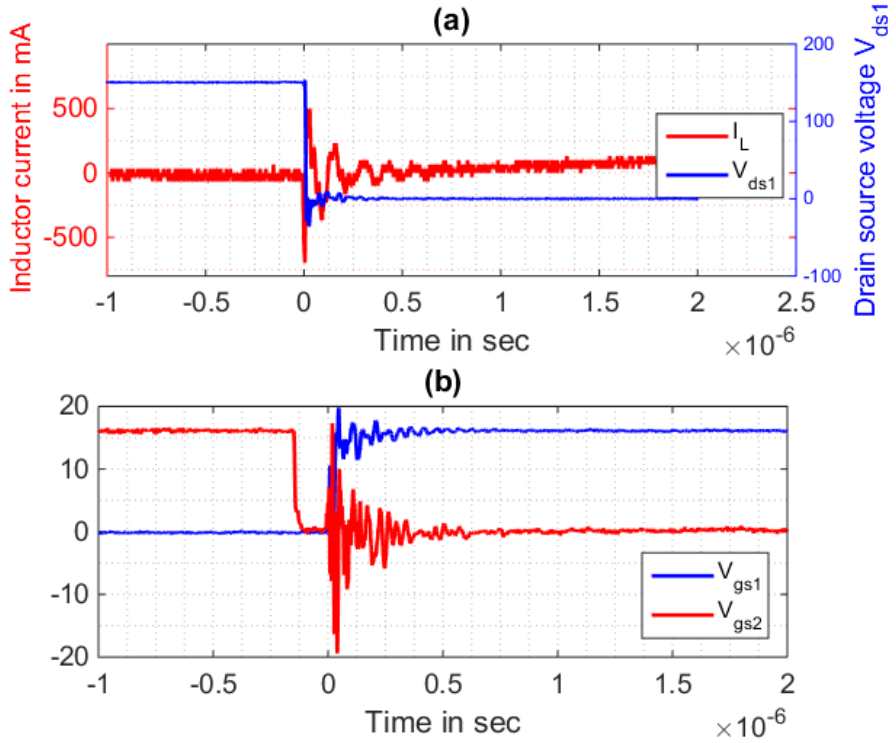


Figure 6.21: Zoomed in Figure 6.20 (a) Drain source voltage of Q_1 and inductor current. (b) Gate source voltages at 150 V DC.

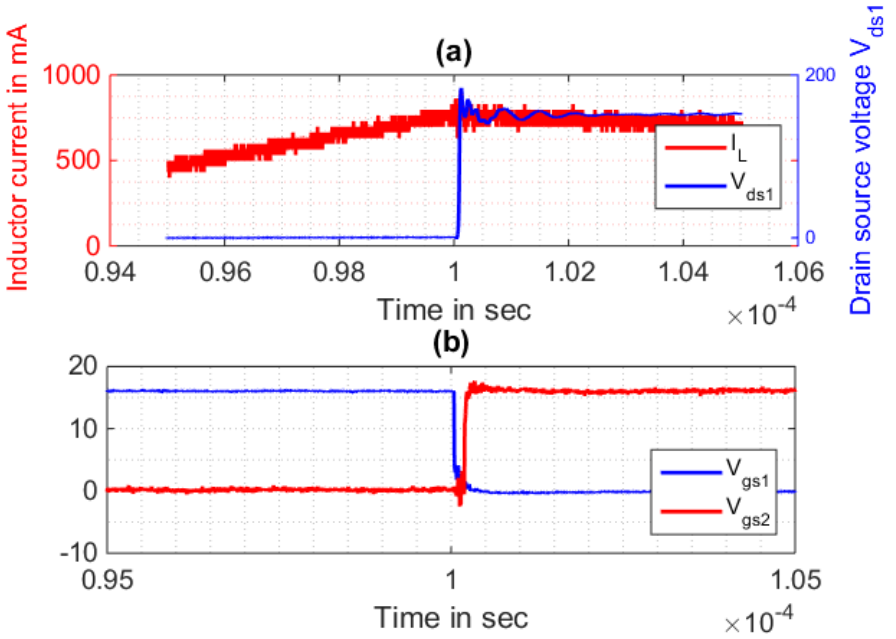


Figure 6.22: Zoomed in Figure 6.20 (a) Drain source voltage of Q_1 and inductor current. (b) Gate source voltages at 150 V DC.

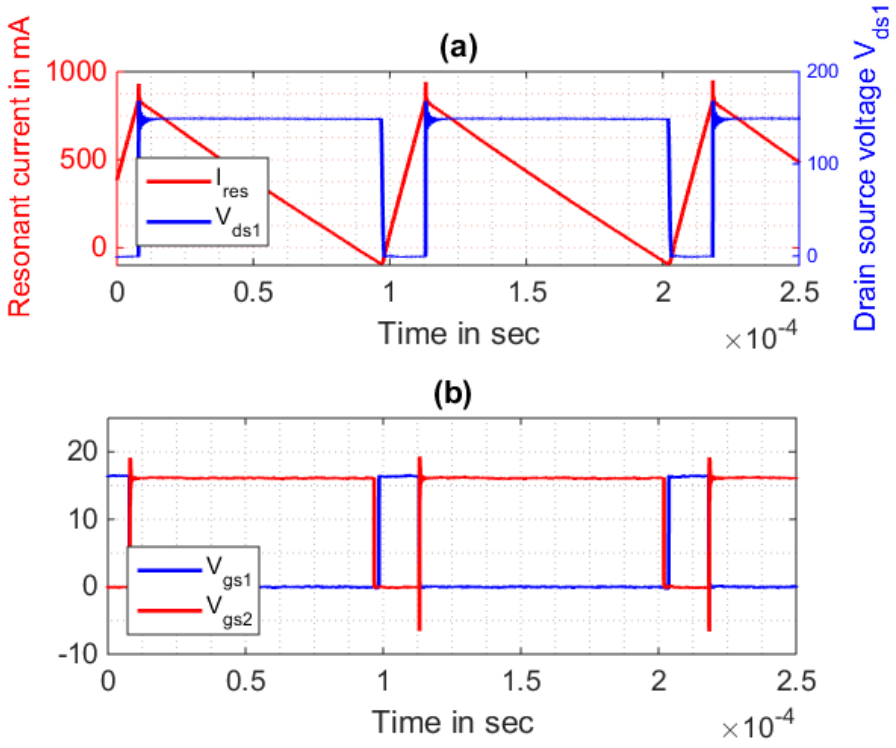


Figure 6.23: (a) Drain source voltage of Q_1 and inductor current. (b) Gate source voltages at 150 V DC.

inductor current and puts more energy in the inductor. When reaching the boost current, Q_2 is gated off and the resonance takes place and the non-linear output

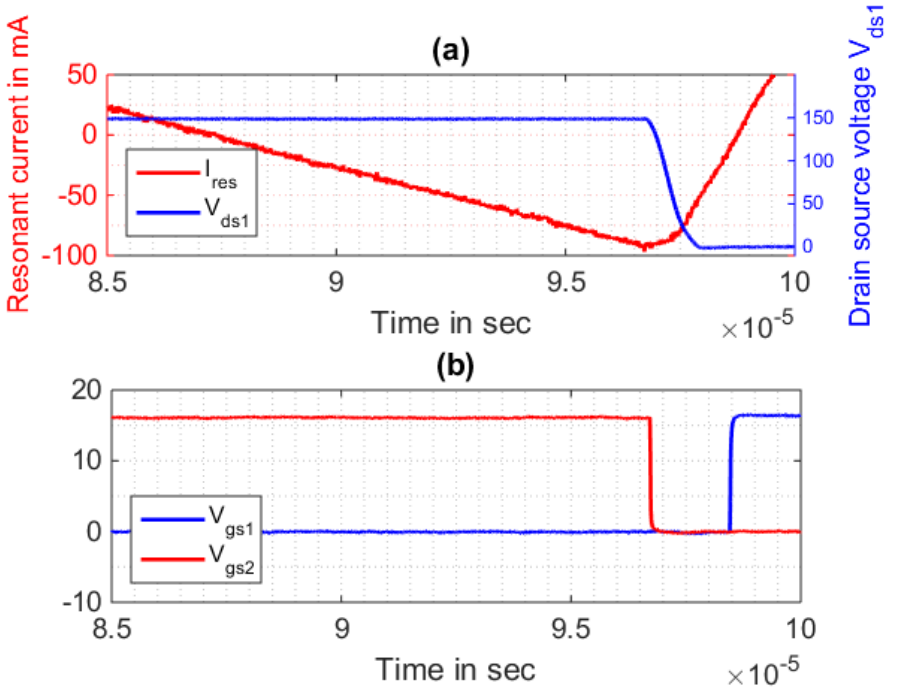
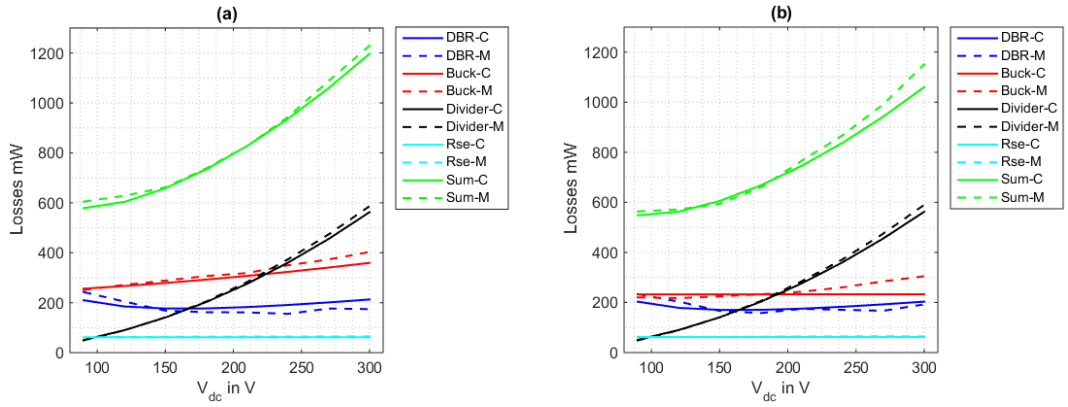


Figure 6.24: Zoomed in Figure 6.23: (a) Drain source voltage of Q_1 and inductor current. (b) Gate source voltages at 150 V DC.



(a) Loss measurement, DC voltage supply and standard CRM with COT.

(b) Loss measurement, DC voltage supply and an improved CRM with COT.

Figure 6.25: Measured loss over DC voltage supply and constant load of 7 W. The legend from top to bottom is: DBR losses, Buck switches losses (excluding the losses of L_o), Input voltage divider losses, Losses in the current sensing resistance and Total loss.

capacitance of Q_1 is being discharged by the inductor current (and Q_2 output capacitance is being charged) before turning on Q_1, Figure 6.24 shows the instant of turn on of Q_1. As shown in Figure 6.24b, fully ZVS turn on of Q_1 has been achieved.

As shown in Figure 6.25b, the losses in the buck switches (red curves) are reduced compared when applying the improved CRM with COT, whereas, the losses of the buck switches are higher in case of standard CRM with COT as seen in Figure 6.25a. The power consumption of the input voltage divider does have a high impact of the total loss of the PFC. In order to reduce these losses, the resistances of this divider have to be re-dimensioned based on the bias current of the selected comparator. A very good agreement between the computed losses and the measured ones has been achieved. But the slight deviation in the measured loss of the buck switches at higher voltages is due to not totally soft turn on of Q_1.

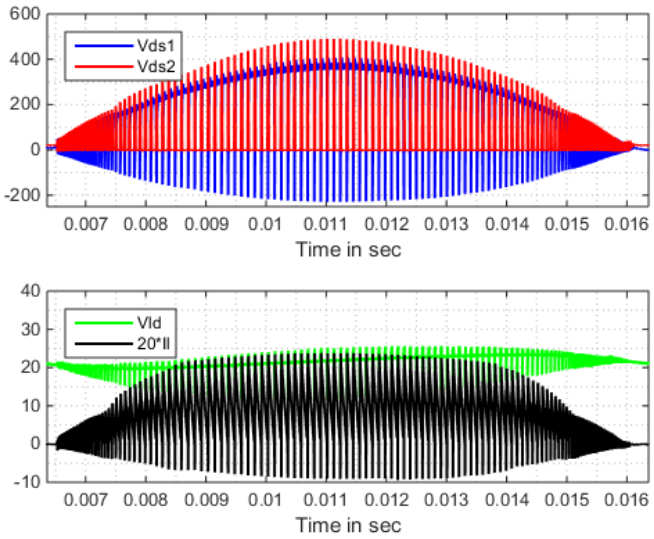
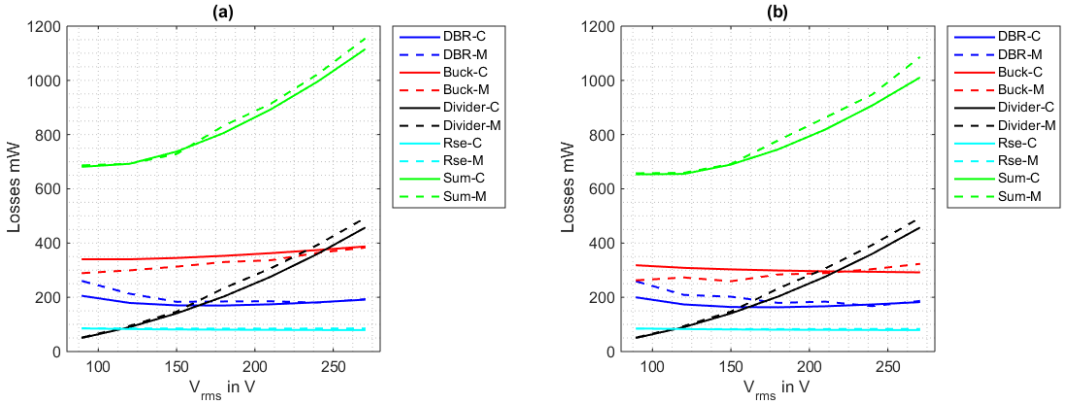


Figure 6.26: Drain source voltages of both switches, load voltage and inductor current scaled by 20 over half of the line frequency, 270 V.

AC Test

The DC supply shown in Figure 6.19a has been replaced by a variable AC supply voltage. The connection of the power analyzer's channels are in the same arrangement as shown in Figure 6.19. The measured drain source voltages of the switches Q_1 and Q_2 are shown together with the load voltage and the inductor current in Figure 6.26 at 270 V RMS line voltage over half cycle of the line frequency.

The losses of the AC test in case of standard CRM with COT and in the case of the improved CRM with COT are shown in Figures 6.27a and 6.27b, respectively. The losses of the buck switches (red curves as shown in Figure 6.27a) are reduced compared to the same losses which are seen in Figure 6.27b. As seen from Figure 6.27b, the measured and computed losses are quite congruent.



(a) Loss measurement, AC voltage supply and standard CRM with COT.

(b) Loss measurement, AC voltage supply and an improved CRM with COT.

Figure 6.27: Measured loss over AC voltage supply and constant load of 7 W. The legend from top to bottom is: DBR losses, Buck switches losses (excluding the losses of L_o), Input voltage divider losses, Losses in the current sensing resistance and Total loss.

6.3.3 Discussion: PFC

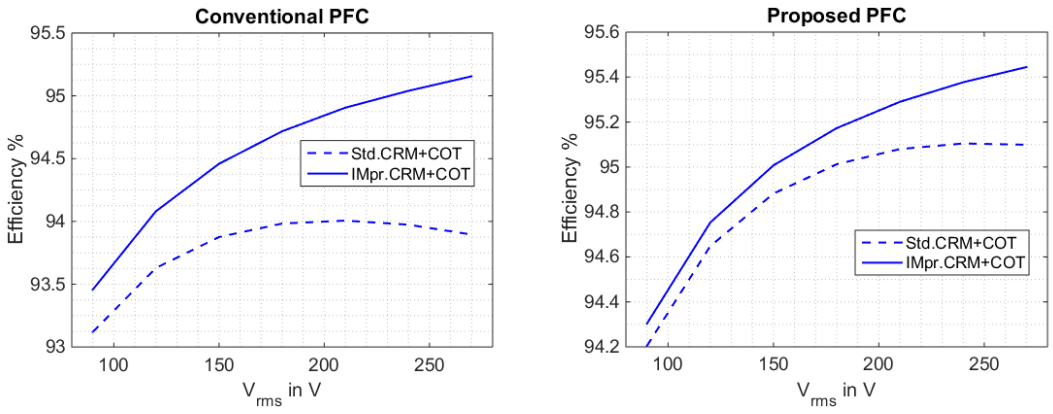
The efficiency of the designed PFCs was estimated at different RMS line voltages by:

$$\eta = \frac{7}{7 + P_t} 100\% \tag{6.10}$$

where 7 W is the load power, P_t is the total losses in the PFC which estimated by (4.17).

As shown in Figure 6.28, the improved CRM with COT enhances the efficiency of both PFCs. The efficiency of the conventional PFC (Figure 4.1a) is shown in Figure 6.28a when applying the improved CRM with COT (solid curve) has higher

efficiency than applying standard CRM with COT (dashed curve). Moreover, the efficiency of the proposed PFC (Figure 4.2) is shown in Figure 6.28b when applying the improved CRM with COT (solid curve) has higher efficiency than applying standard CRM with COT (dashed curve). Additionally, Figure 6.28 shows that the proposed PFC has slightly higher efficiency than the conventional PFC over RMS line voltage and in both cases of CRM with COT.



(a) Conventional PFC (b) Proposed PFC

Figure 6.28: Efficiency comparison of the conventional buck PFC and the proposed one, the switches efficiency (excluding the losses in L_o) in both cases. For both, the standard CRM with COT- dashed curve. The improved CRM with COT-solid curve.

Chapter 7

Component Selection of the AC-AC Converter

7.1 Selection of Load Voltage and Current

A three phase pulse width modulation Voltage Source Inverter (VSI) is designed with the rated power of the load. In this project, the decision was made to design an inverter able to drive a rated load of 70 W while most of the time it drives a partial load of 10 % of its maximum thermal capability, see Section 1.5. Typically, an inverter is designed for its rated conditions with some overload capability. Designing an inverter which operates at partial load conditions increases its lifetime. Moreover, there is no need to add an additional circuitry for overload conditions, thus keeping the inverter component count as small as possible.

These VSIs are loaded by connecting an electrical motor to the VSI's output terminals. For low power applications, a Permanent magnet motor (PM motor), e.g., Brushless AC Motors. The Brushless AC motors are often used because of their high reliability and efficiency; they are small in size and light, have a long life with low maintenance cos and low and EMI issues becuase the PM motor has no rotating brushes to commutate its winding [69–72]. Motors generate a back Electromotive Force (back EMF), which is caused, according to Faraday's law,

when the current carrying the conductor cuts the magnetic field.

At the rated power, the torque and the speed of the machine are both maximum ($\tau_{\max}$ and $n_{\max}$, respectively). But at the optimum power point, they are selected to be (50 % $\tau_{\max}$ and 20 % $n_{\max}$, respectively).

Thus, the voltage and current at optimum power point have to be set to 20 % $V_{\text{o-max}}$ and 50 % $i_{\text{o-max}}$. The voltage is directly proportional to the number of turns of the stator coil and the current is inversely proportional to the number of turns of the stator coil. The designer has the freedom to select the rated voltage of the load or the optimum voltage at optimum power point. The change in the rated/optimum voltage can be achieved easily by selecting the proper number of turns of the coil of the machine.

7.2 Component Selection of Individual Circuits

7.2.1 HSI-leg

The losses occurring in the single leg of the inverter were estimated using the previously discussed analysis in Chapter 2. To select the best fit power switch, the losses were estimated for different power transistors from different technologies (e.g., IGBTs, Si MOSFETs, SiC MOSFETs) and different blocking voltages as follows:

- High blocking voltage power switches (500 - 1200 V MOSFETs/ IGBTs): the losses were estimated for the respective load current (150 mA-Peak) with a variable DC link voltage up to 350 V.
- Low blocking voltage power switches (250 V MOSFETs): the losses were estimated for the respective load current (300 mA-Peak) with a variable DC link voltage up to 125 V.

These two pairs of load voltage are justified according to the fact that the selected switch must be able to block twice of the rated load voltage.

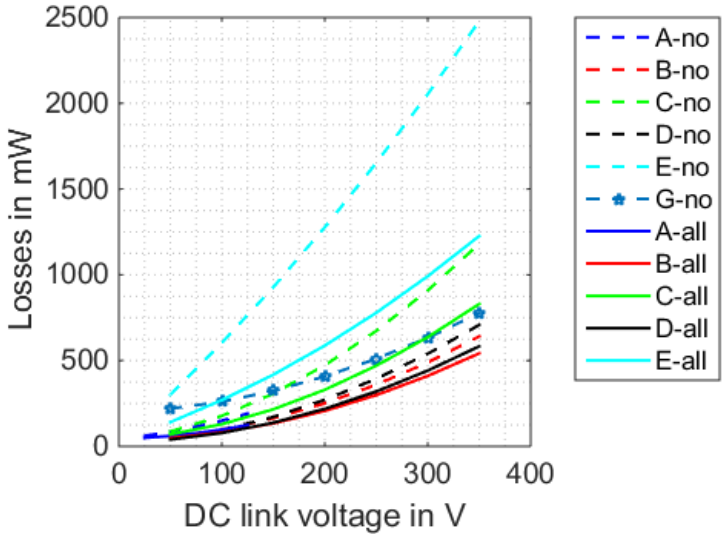


Figure 7.1: Single leg computed total losses for some selected power switches at 10 % of maximum power, which is the desired point of maximum efficiency (7 W), with two different load current/voltage. Table 7.1 defines the MOSFETs. All dashed curves represent the losses without dead time optimization and all solid curves show the losses with dead time optimization.

Table 7.1: Data sheet parameters of different switches.

Switch	Number	V_{on} V R_{on} Ω	I_N A	V_{ds} or V_{ce} V	Q_{gt} nC	Q_{rr} nC	Switch Technology
MOSFET	*A* [56]	0/0.9	2.2	250	4.5	550	Si-based
MOSFET	*B* [15]	0/1.85	3.6	500	20	135	Si-based
MOSFET	*C* [11]	0/1.26	1.5	650	10	100	Si-based
MOSFET	*D* [73]	0/0.45	10	1200	27	13	SiC-based
MOSFET	*E* [74]	0/0.12	29	650	61	53	SiC-based
MOSFET	*F* [75]	0/0.17	9.5	600	63	6900	Si-based
IGBT	*G* [19]	0.9/0.06	15	600	90	1000	Si-based

As can be seen from these results, the IGBTs have an additional P region in their physical structure which causes an initial voltage at zero current (V_{ce0}). This initial voltage prevents achieving high efficiency when using the IGBTs for an extremely light load.

Figure 7.1 shows the computed total losses of a single leg of the inverter. The figure compares the total losses of the selected power switches for each of the investigated families by averaging the losses over one fundamental period. MOSFETs B and D have the lowest losses over the DC link voltage range. MOSFET B has slightly lower losses than MOSFET D for DC link voltage higher than 120 V. Moreover, The dead time optimization reduces the total loss in the HSI as shown in Figure 7.1.

The next comparison is carried out based on the loss break down as shown in Figure 7.2:

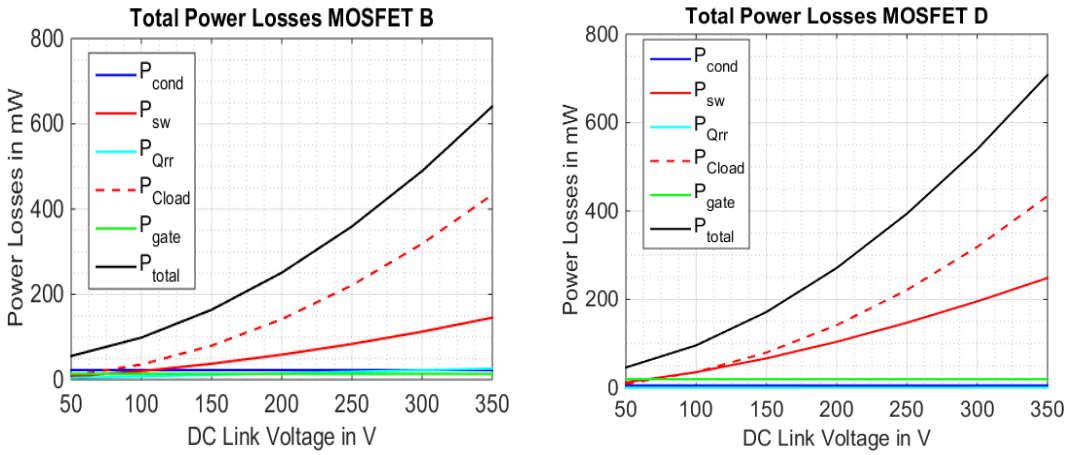
1. Figure 7.2a shows higher conduction losses than Figure 7.2b (blue curves). This is because MOSFET B has higher on-state resistance than MOSFET D.

2. Figure 7.2a shows lower switching losses than Figure 7.2b (solid red curves). MOSFET B has a lower chip size than MOSFET D and thus a lower non-linear capacitance.

3. The gate drive losses (green curves) of Figure 7.2a are lower than the gate losses of Figure 7.2b. The total gate charge of MOSFET D is slightly higher than the total gate charge of MOSFET B. Furthermore, the driving voltage applied to drive MOSFET D is higher than the driving voltage of MOSFET B.

4. The dashed red curves show the effect of parasitic capacitance of the stator. These losses constitute a large contribution in the switching losses in both cases.

Each family of power switches has a constant called figure of merit [18], which is well-known in MOSFETs and IGBTs design, which can be estimated from the data sheet parameters. This constant gives an indication of the total losses in this



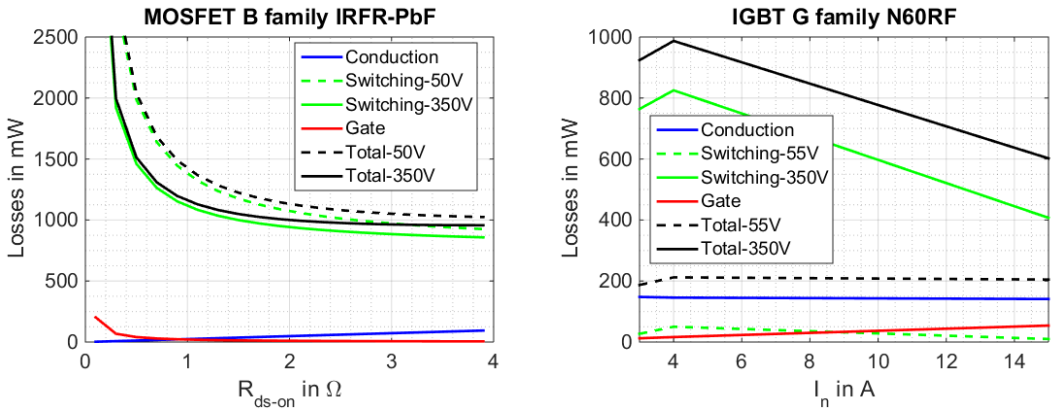
(a) Loss break down, MOSFET B. (b) Loss break down, MOSFET D.

Figure 7.2: Loss break down of MOSFETs B and D at 7 W load.

family at given specifications, e.g., switching frequency. Also, it gives a guideline to select one switch from this family. This can be summarized as follows:

- For each MOSFET family, the multiplication of the on-state resistance and input/output capacitances gives a constant value. As shown in Figure 7.3a for one MOSFET, the conduction losses increase with increasing the on-state resistance (blue curve) and the switching losses decrease when increasing the on-state resistance (solid and dashed green curves, for 350 V and 50 V, respectively). The switching losses are influenced by the parasitic capacitance of the load as seen in Section 6.1.4. But dead time optimization does reduces the total losses in the HSI, as seen in Section 6.1.4. The gate drive losses (red curves) decrease with increasing on-state resistance. The dashed and solid black curves in Figure 7.3a show the single leg total losses for DC link voltages of 50 V and 350 V, respectively.

- For each IGBT family, the division of the input/output capacitances over nominal current gives a constant value. As shown in Figure 7.3b, increasing the nominal current keeps the conduction losses constant (solid and dashed blue curves), but it increases the gate drive losses (red curves). The switching losses decrease when increasing the chip area (solid and dashed green curves,



(a) MOSFET B, family ($IRFR--PbF$). (b) IGBT G, family ($N60RF$).

Figure 7.3: Single leg computed total losses for MOSFET family ($IRFR--PbF$) and IGBT family, DC link voltage at 50 V and 350 V at 10 % of maximum power 7 W.

for 350 V and 55 V, respectively). As seen in (2.31), the switching losses in the IGBTs are computed based on some figures in the their data sheet. As shown in Figure 7.3b, these losses decrease when increasing the nominal current. This can be justified by the fact that the recommended external gate resistance, as stated in the IGBT data sheet, of this IGBT family decreases when increasing the chip area. Furthermore, the energies E_{oi} and E_{or} in (2.31) increase when increasing the chip area, hence reducing the switching losses. The dashed and solid black curves in Figure 7.3b show the single leg total losses of the N60RF- family for DC link voltages of 55 V and 350 V, respectively.

7.2.2 ARCP

The best fit main and auxiliary switches, and the resonant inductor for the ARCP are selected based on the computational results as discussed above in Chapter 3. A deeper understanding of these results can be gained by the following statements:

- *The main switches*: the conduction losses of the main switches are dominant because in soft switching topology, the effect of the non-linear output capacitance of the main switches and the load parasitic capacitance are ideally

eliminated. Thus, MOSFETs with big chip areas are recommended.

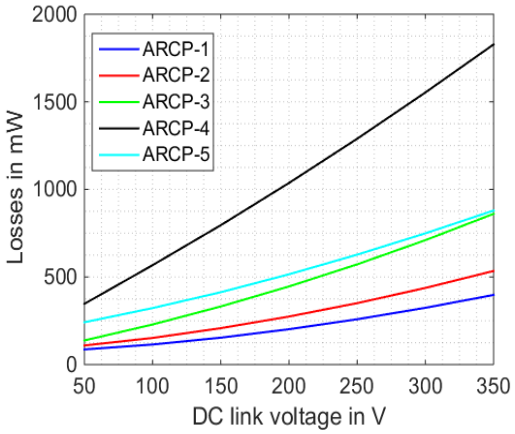
- *The auxiliary switches*: as the auxiliary switches conduct for a very short time, the conduction losses of these switches are low. The capacitive losses of the auxiliary switches are dominant. The (non-linear) output capacitance of these switches should be low. In other words, these switches should have small chip areas (low output capacitance; but may show higher on state resistance).

- *The resonant inductor*: first, this should have a low DC internal resistance for low resistive losses. Second, the self resonant frequency of this inductor (caused by resonating with its parasitic capacitance) should be much higher than the resonant frequency which is computed in sequences 3 and 8. Finally, the current carrying capability of this inductor should be higher than the peak value of the resonant current of the inductor (peak current of sequences 3 and 8) to avoid core saturation of the inductor.

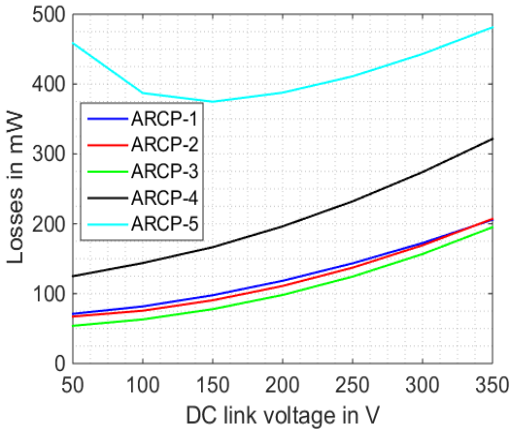
Figure 7.4 shows the total loss for five different ARCPs (for ARCPs definition see Table 7.1 and Table 7.2). The main switches are MOSFET [75] which has low on state resistance, see Table 7.1. Figure 7.4a shows the total loss when applying the new switching sequence only (Option 1, see Section 5.2). ARCP-1 and ARCP-2 show lower losses than other ARCPs. Furthermore, Figure 7.4b shows the loss computation for the five ARCPs when applying the options 1-3, as mentioned in Section 5.2. ARCP-3 shows lower losses compared to other ARCPs. The next discussion has been carried out based on loss break down, as shown in Figure 7.5 and Table 7.1. Figure 7.5 shows the loss break down of different ARCPs:

1. The conduction loss of the main switches P_{condM} is quite low.

2. The conduction loss of the auxiliary switches P_{condA} increases when decreasing the chip area. Using an IGBTs as auxiliary switches increases the conduction loss as shown in Figure 7.5d. As seen in Figure 7.5d, the conduction

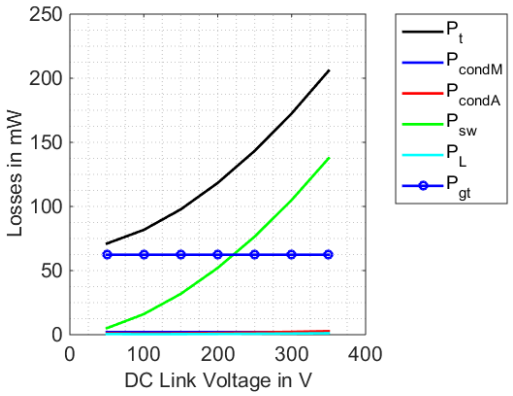


(a) Option 1 is applied.

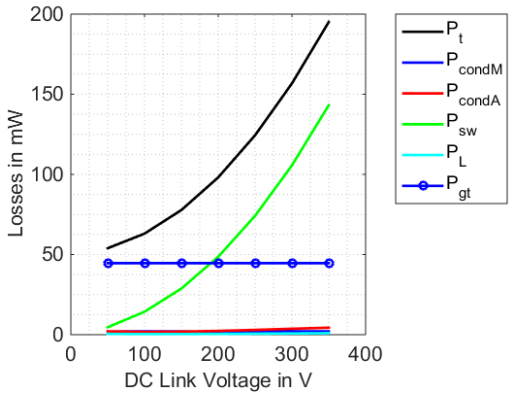


(b) All options 1-3 are applied.

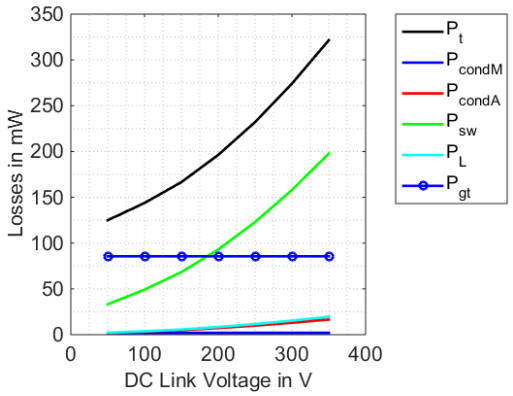
Figure 7.4: Single leg computed total losses for some ARCP as listed in Table 7.2 at 7 W and 150 mA.



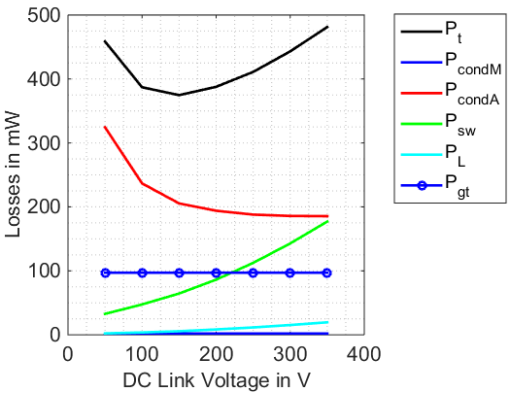
(a) Loss break down ARCP-1.



(b) Loss break down ARCP-3.



(c) Loss break down ARCP-4.



(d) Loss break down ARCP-5.

Figure 7.5: Figure 7.4b (options 1-3) loss break down of ARCP-1,ARCP-3, ARCP-4 and ARCP-5 as listed in Table 7.2 at 7 W and 150 mA.

Table 7.2: Legend of Figure 7.4, for switches definition see Table 7.1.

ARCP	Main switch	Auxiliary switch
$ARCP-1$	F	D
$ARCP-2$	F	B
$ARCP-3$	F	A
$ARCP-4$	F	F
$ARCP-5$	F	G

loss of the auxiliary switches has the largest contribution. These losses decrease with increasing the DC link voltage. This can be explained by the fact that the conduction period of the auxiliary switches decreases when increasing the DC link voltage.

3. The switching losses P_{sw} in the commutation circuit do have high contribution in the total loss of the ARCPs. Increasing the chip are increases the switching losses in the commutation circuit.

4. The resistive losses in the resonant inductor P_{L} are directly affected by the inductor current and the duration of resonance period. Increasing the inductance value increases the resonance time (decreases the resonance frequency).

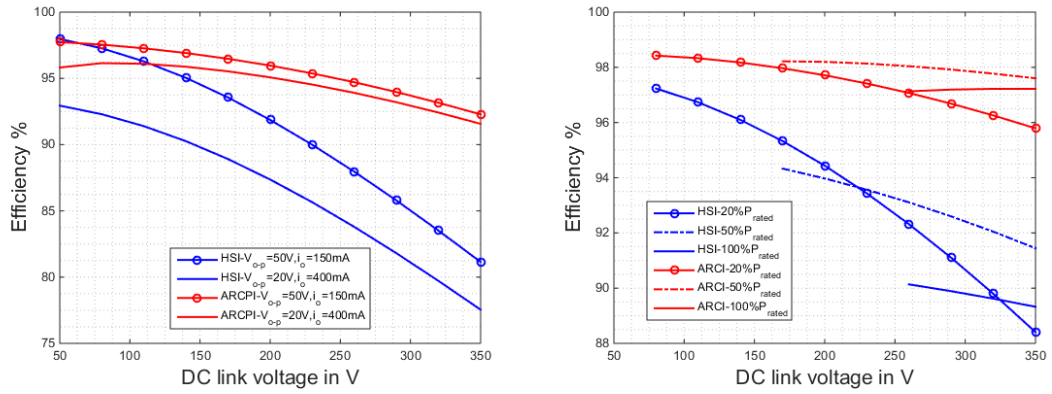
5. The gate drive losses of both main and auxiliary switches P_{gt} have a large contribution for lower DC link voltage than 200 V. The drawback of using large chip areas as main switches is increasing the gate drive losses.

7.2.3 Comparison between HSI and ARCPI

The efficiencies of HSI and ARCPI are compared over the range of DC link voltage as shown in Figure 7.6a. The load conditions are changed but the load power is constant. As shown in Figure 7.6a, the HSI is more efficient than ARCPI only when the load current is low and when the DC link voltage is lower than 55 V;

otherwise, the ARCPI is more efficient. It should be noticed that for higher currents (and lower voltage), MOSFET *B* is not the best choice. There might be a better MOSFET fit at these conditions.

The comparison between the two inverters when changing the load is shown in Figure 7.6b. The efficiencies are computed when the dead time has been optimized for HSI and all options (1-3) have been applied to the ARCPI. The efficiency decreases when the load is increased in both inverters. Again, the ARCPI is more efficient than the HSI over the DC link voltage range.



(a) HSI Vs ARCPI efficiency for two different load voltage and current.

(b) Computed efficiencies of HSI and ARCPI for different load power.

Figure 7.6: Computed efficiencies of HSI and ARCPI topologies for different test conditions, all optimization methods are applied. MOSFET *B* is used in HSI and ARCPI-3, see Tables 7.1 and 7.2.

7.2.4 Selection of MOSFET Technology

Recently, the interest in the wide-gap materials, e.g., Silicon Carbide (SiC) and Gallium Nitride (GaN) has been increased because of their interesting features over the Super Junction MOSFETs, e.g., Sillicon MOSFETs (Si), such as: They do have lower output capacitance which allows to increase the switching frequency with low switching losses in power converters applications [76–79]. Moreover, these material offer a higher thermal capability [80].

In this work, Si-MOSFETs have been selected for both hard switching and soft switching prototypes despite the existence of wide-gap material semiconductors such as SiC and GaN MOSFETs. As a matter of fact, these wide-bandgap materials might be used as auxiliary switches in ARCPI because they do have very low output capacitances, reducing the commutation circuit switching losses. Additionally, the use of the wide-bandgap semiconductors over the use of Si based power semiconductors in a hard switching inverter counterpart driving the partial load presented here is not considered promising. This is due to the fact that the switching losses in the hard switching inverter are dominated by the parasitic capacitance of the load (as presented in Section 5.1.2 and in Section 6.1.4) and not the output capacitance of the semiconductor devices used.

In the work presented herein, both inverters (hard switching and ARCPI) are operated under partial load conditions for most of the lifetime of the application, the application does not exploit the higher range of thermal capability that the wide-bandgap materials offer. Moreover, the use of wide-gap materials is excluded in the components selection because these components are also significantly more costly, which is critical in the mass production of the product under consideration here.

7.2.5 The Conventional PFC

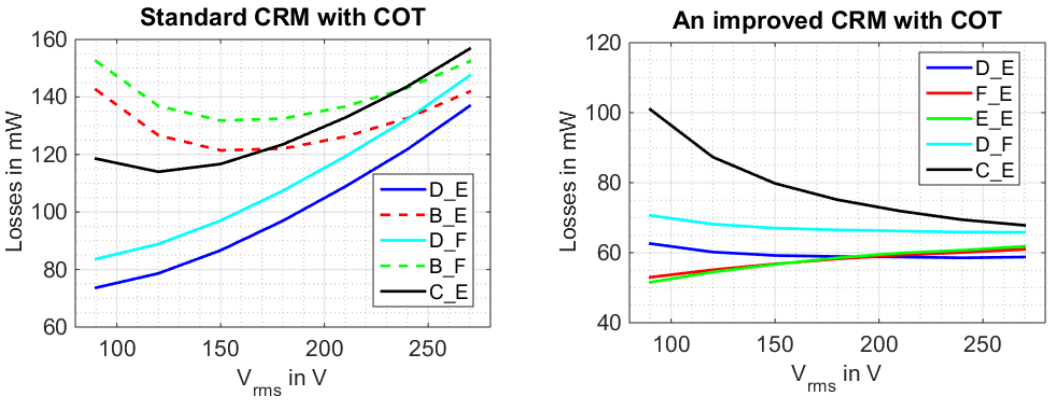
The conventional buck PFC suffers from the dead zones in the AC line current when the AC line voltage is lower than the load voltage. Dead zones are bigger with a lower ratio (AC line voltage)/(DC output voltage). Thus, THD increases with lower AC line voltage and higher DC output voltage. The conventional Buck PFC components are, as shown in Figure 4.1a:

1. The losses in the Diode Bridge Rectifier are influenced by the forward voltage of the diode at zero current, differential resistance. The loss components in the DBR are the conduction losses. In order to reduce the conduction loss

in the DBR, this rectifier should have low forward voltage at zero current alongside with low differential resistance.

2. The Buck converter switches: this converter contains two switches, the operating and the synchronous switch. In the work presented herein, the conduction losses are dominated by the on state resistance of the synchronous switch because it conducts for a long time. Hence, the synchronous switch should have low on state resistance. On the other hand, the synchronous switch is turned on under ZVS and it is turned off under Zero Current Switching (ZCS). Thus, the synchronous switch provides nearly zero switching losses.

   The switching losses in the buck converter are dominated by the operating switch non-linear capacitance and some parasitic capacitances, e.g., the parasitic capacitance of the output inductor, because the synchronous switch turns on at zero voltage. Thus, for standard operation of CRM, the operating switch should have a small chip (low non-linear output capacitance) in order to reduce the switching losses.



(a) With standard CRM with COT. (b) With an improved CRM with COT.

Figure 7.7: Losses in conventional Buck switches (exluding the losses in L_o) for different switch combinations at 7 W, $V_o = 20$ V and $i_o = 350$ mA, for legends definition see Table 7.1.

As the improved CRM with COT provides ZVS turn on of the operating switch, it is recommended to select a switch with low on state resistance

(big chip area). Moreover, both switches must be able to block the input voltage (universal voltage range). Figure 7.7 shows computed losses in the conventional buck switches (excluding the losses in the output inductor L_o, but including the effect of its parasitic capacitance). The figure compares different combinations of operating and synchronous switches. Also, it compares the buck switches losses in the case of standard CRM with COT and the losses in the case of the improved CRM with COT. The combination D and E (blue curves, for switches definitions see Table 7.1) shows the lowest losses over the universal line voltage in the cases of standard CRM with COT, as shown in Figure 7.7a. Furthermore, the total losses, in Figure 7.7a, increase with increasing the line voltage because of increasing the switching losses due to non-linear output capacitance of the operating switch plus the parasitic capacitance of the inductor L_o.

On the other hand, Figure 7.7b compares the total losses of the buck switches for different combinations over universal line voltage range in the case of the improved CRM with COT. The switches with the big chip area (low on state resistance and high output capacitance) are the best fit to play the role of the operating and a synchronous switch.

It should be noticed that, the SiC-based MOSFET D, see Table 7.1, does not show the superior performance in the losses in Figure 7.7b. The Si-based MOSFET E shows lower losses when the line voltage is lower than 200 V and nearly the same losses with SiC-based MOSFET D when the line voltage is higher than 200 V. Thus, as mentioned in Section 7.2.4, and due to the high cost of the wide-gap material semiconductor, they could be replaced by Si-based MOSFETs for this specific application. Furthermore, IGBTs are excluded from the selection process because they showed high conduction losses which prevent high efficiency from being achieved, as mentioned in Section 7.2.1.

The computed loss break down of conventional buck PFC, using MOSFET F for both switches and for the improved CRM with COT, is shown in Figure 7.8 (the other components of the circuit are listed in Table 6.9). The losses in the buck switches (conduction plus switching plus gate drive) are lower than the power dissipated in the DBR, voltage divider and the sensing resistance.

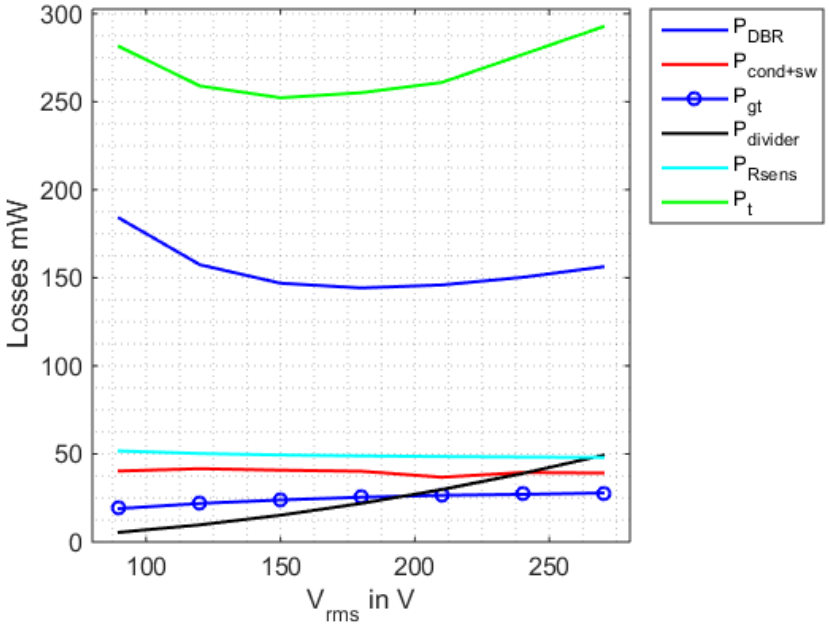


Figure 7.8: Computed loss break down of conventional buck PFC with an improved CRM with COT, using MOSFET F. The other components are listed in Table 6.9.

3. The output inductor: this inductor should have low DC resistance in order to reduce the conduction losses. Also, when selecting this inductor, it should be noted that the parasitic capacitance must be low in order to reduce the switching losses of the PFC. Additionally, the rated current of the inductor must be high enough to avoid any core saturation which might be caused.

7.2.6 The Proposed PFC

In contrast to the conventional PFC, the proposed PFC eliminates the dead zones from appearing in the AC line current. Thus, it is possible to use the proposed PFC over the whole AC line voltage range. In order to select the switches of the proposed PFC, as shown in Figure 4.2. The following should be considered:

1. The operating switches Q_{Ap}, Q_{Bp} are turned on at zero voltage, because of applying the improved CRM with COT. Thus, the conduction losses are the dominant.

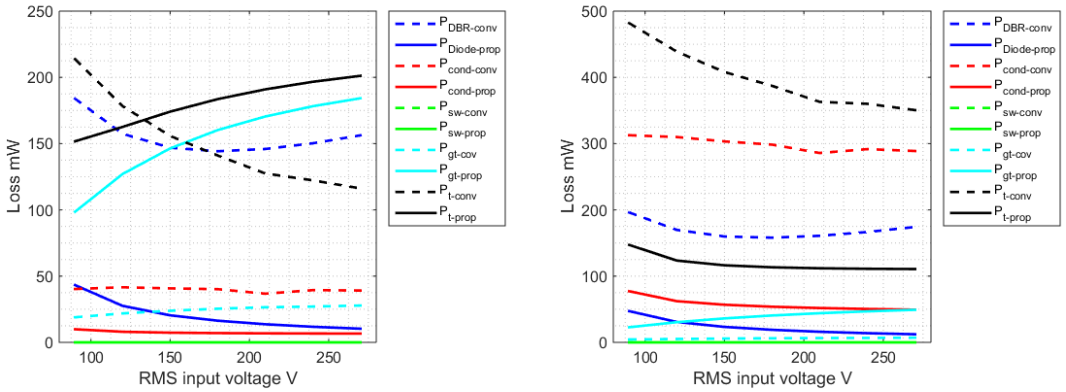
2. The synchronous switch Q_{op} is turned on at zero voltage. Thus, the conduction losses have the highest contribution.

3. The gate drive losses will be relatively high in the proposed PFC because of the switching frequency range of the proposed PFC is higher than the conventional PFC, as shown in Figure 4.6.

4. Switches Q_{An} and Q_{Bn} are operated at line frequency, thus, the switching and gate drive losses are negligible. Again, the conduction losses do have the highest contribution in the total loss.

5. The output inductor of the proposed PFC is selected based on the criteria used in Section 7.2.5.

Figures 7.9a and 7.9b show the computed losses break down of both conventional PFC (all dashed curves) and the proposed PFC (all solid curves) using MOSFETs C and F, respectively, see Table 7.1. The diode conduction losses are significantly decreased in the proposed PFC. This loss reduction for both MOSFETs is justified by the fact that the proposed PFC has lower number of diodes and lower inductor peak current due to lower on time T_{on} compared to the conventional PFC on time.



(a) Using MOSFET F. (b) Using MOSFET C.

Figure 7.9: Computed loss break down of conventional PFC and proposed PFC with an improved CRM with COT, using MOSFETs F and C.

The gate drive losses of the proposed PFC (solid cyan curve) are higher than the same losses of the conventional PFC (dashed cyan curve), as mentioned previously. As shown in Figure 7.9a, the gate drive losses of the proposed PFC have the highest contribution in the total loss in case of using MOSFET F because it has a high total gate charge. When using MOSFET C, Figure 7.9b, in the proposed PFC, the conduction losses are the dominant in the total loss. Also, the gate drive losses have a high contribution in the total losses.

It can be concluded that the proposed PFC has lower total losses in case of using small chip area (MOSFET C) than the conventional PFC. Additionally, the small chip ares switch does have lower total losses than the big chip area in case of the proposed PFC (solid black curves). As the total losses still decrease with increasing RMS voltage, a bigger chip area might result in even lower total losses.

Chapter 8

Discussion, Conclusions and Future Work

8.1 Introduction

This thesis discussed the loss performance of three different topologies, e.g., AC-DC converters (PFC) and DC-AC converters (three phase pulse width modulation voltage source inverters: hard and soft switching inverters). The designed AC-AC converter is used to feed an extremely light load for home appliance applications. The rated power of the load is 70 W, but for most of the lifetime of this load is working at 10 % of its rated power. This rated power is not relevant to energy consumption. Thus, the losses in these stages of the converter were computed at the optimum power point 7 W.

The main core of this thesis is to design a highly efficient AC-AC converter. Therefore, the guideline to select the best fit switches was discussed. Furthermore, some options have been studied/introduced to reduce the total losses in this converter. One of those options was employing the resonant gate drive to reduce the gate drive losses.

As seen in Section 7.2.3, the DC-AC has high efficiency at low DC link voltage. Thus, the DC link voltage has been tested at two load voltages as follows:

1. *Point one*: when load voltage/current are $V_{\text{o}} = 25\,\text{V}$ and $i_{\text{o-peak}} = 300\,\text{mA}$

at optimal power point. Then, the load voltage and current at rated conditions are set to 125 V and $i_{\text{o-peak-rated}} = 160\,\text{mA}$, i.e., $V_{\text{o-rated}} = 5V_{\text{o}}$ and $i_{\text{o-peak-rated}} = 2i_{\text{o-peak}}$.

2. *Point two*: when load voltage is $V_{\text{o}} = 50\,\text{V}$ and $i_{\text{o-peak-rated}} = 150\,\text{mA}$ at optimal power point, the rated voltage/current of the load are 250 V and $i_{\text{o-peak-rated}} = 300\,\text{mA}$.

Thus, the buck PFC has been selected as the AC-DC converter stage. The drawback to the conventional buck PFC is the THD increases with increasing the dead zones in the AC line current. The output voltage of the PFC (DC link voltage) together with the input voltage determine the borders of these dead zones. Thus, using the conventional PFC when the DC link voltage at optimal power point is around *point one* is recommended.

Conversely, if the output voltage of the conventional buck PFC increased, the THD in the AC line current is increased. In order to eliminate the dead zones and decrease the THD in the AC line current, a bridge-less step down PFC has been proposed. Thus, the proposed PFC is recommended when the DC link voltage is around *point two*.

The hard switching inverter is more efficient than the auxiliary resonant pole inverter for the low DC link voltage range. Thus, the conventional PFC with HSI is a good combination for *point one* operating conditions. Also, the proposed PFC with ARCPI is a good combination for *Point two* operating conditions.

8.2 AC-DC Converter Stage

This thesis proposes a new single-phase hybrid bridge-less step down PFC converter. The design procedure, the mathematical model of the AC line current, the PF and the THD have been discussed. Furthermore, the loss component had been

studied individually and compared with the loss components of the conventional buck PFC.

Both PFCs were operated under standard Critical Conduction Mode with Constant On Time (CRM with COT) in order to remove the reverse recovery losses of the synchronous switch body diode. Then, the standard CRM with COT was improved to achieve Zero Voltage turn on of the operating switch. Also, an additional signal was added to the constant on time in order to sinusoidally shape the average line current, thus improving the PF.

A 7 W conventional buck PFC was built using MOSFET B to measure the losses and to validate the improved CRM with COT. Different measurements, e.g., T_{on}, T_{off}, peak of the inductor current and the losses excluding the losses in the buck inductor L_{o}, had been compared with the computations.

8.3 DC-AC Inverter Stage

The loss components were computed and discussed in detail for two conventional pulse width modulation inverters. The first inverter type was Hard Switching Inverters (HSI). The second was soft switching inverter. An Auxiliary Commutated Pole Inverter (ARCPI) was selected as a soft switching topology.

The losses were computed and compared for different switches such as MOSFETs and IGBTs with different blocking voltages and different technologies. The following can be concluded from the outcomes of this converter stage:

8.3.1 HSI

A single phase prototype was built and the losses were measured. Both low blocking voltage MOSFET A and high blocking voltage MOSFET B were experimentally analyzed. The measurements were compared with computed total losses

based on formulas and parameters from data sheets of the switches. The algorithm is well suited for the optimization procedure and for the selection of the best fit switch for this application under given operating conditions (DC link voltage (V_{dc}) and load current (i_{o})). The high blocking voltage MOSFET had higher efficiency than the low blocking voltage MOSFET at comparable points of load voltage (i.e., when the applied DC link voltage in case of HV MOSFET is twice the applied DC link voltage in case of using LV MOSFET).

Due to the internal gate resistance of the selected MOSFETs, the use of a RGD did not reduce the gate drive losses at comparable switching speeds.

8.3.2 ARCPI

The thesis discussed several options to improve the inverter efficiency. The first option was introducing a new switching sequence by turning on both auxiliary switches simultaneously. The second option was skipping one of the auxiliary pulses per switching cycle. The third option explores the effect of adjusting the boost current according to the sinusoidal load current was discussed.

A single pole prototype was built to measure the losses using MOSFET *B* as main and auxiliary switches. The computed losses were compared with the measured ones.

Due to the internal gate resistance of the selected MOSFETs, the use of an RGD did not reduce the gate drive losses at comparable switching speeds.

8.4 Component Selection

This thesis presented several aspects to select the best fit components of the individual stages of the AC-AC converter.

8.5 Component Count and Cost for the Individual Stage

Table 8.1 shows the main component count of HS-leg prototype and ARCP. The component count of the conventional PFC is listed in Table 6.9 and the comparison between component counts (switches, inductors, diodes and capacitors) is shown in Table 4.1.

The HS-leg has one half bridge driver, whereas the ARCP has one half bridge driver and two isolated drivers in order to drive the auxiliary switches.

The timing circuit used in the ARCP prototype contains a schmitt trigger connected with some passive components such as resistance and capacitances to set the time constant of the RC circuit. Additionally, some OR and AND gate chips are used in order to generate the proper timing sequence of the main and auxiliary switches.

The DC link voltage capacitors in case of ARCPI should have rated voltage slightly higher than half of the DC link voltage, because the DC link voltage is divided between those capacitance.

Table 8.1: Main components count HS-leg Vs ARCP, used in this thesis.

	HS-leg	ARCP	Part number
Number of switches	2	4	MOSFET *B*
Drivers	1	3	2EDL05N06PF
Timing circuit	-	1	see Table 6.9
DC link capcitances	1	2	EEUEE2V150, 15uF/350V
Gate resistances	2	4	18 Ω, SMD 1206

8.6 Future Work and Suggestions

The following suggestions and thoughts are left for future work:

1. The buck PFC output inductor: in addition to the discussion in Section 7.2.5, another factor should be taken into account which is the switching frequency. The inductance value is inversely proportional with the switching frequency. Increasing the switching frequency increases the switching losses and decreases the switching frequency results in increasing the size of the inductor.

2. Input filter components: the input filter's capacitor is dimensioned to limit the reactive power of the converter and to attenuate the switching harmonics. When connecting the capacitor with the converter, a current passes through this capacitor. Thus, the line current leads the line voltage by an angle (ϕ). To limit this angle, the capacitor should not exceed the maximum limit. This limit can be estimated as follows [81]:

$$\frac{V_{\text{ac-peak}}}{\mid X_{\text{c}} \mid} = I_{\text{ac-peak}} \tan \phi \tag{8.1}$$

Assuming the voltage drop across the filter inductor is small. Thus, the capacitor voltage is equal to the input line voltage. Rearranging (8.1), the capacitor limit is estimated by [46, 81]:

$$C_{\text{max}} \leq \frac{I_{\text{ac-peak}}}{\omega_{\text{l}} V_{\text{ac-peak}}} \tan \phi \tag{8.2}$$

where $V_{\text{ac-peak}}$ is the peak of the AC line voltage, $I_{\text{ac-peak}}$ is the peak value of the real component of the AC line current, ω_{l} is the line angular frequency and ϕ is the displacement angle caused by the input filter. To ensure high power factor ϕ has to be small. Then, the filter inductor is estimated by

(the cut-off frequency should be known):

$$L_{\text{filter}} = \frac{1}{C_{\text{selected}}\omega_{\text{cut-off}}^2} \tag{8.3}$$

It should be noticed that, the input filter causes some oscillation at the resonance frequency of the filter components due to its very low resistance. This oscillation appears when changing the load conditions, resulting in extra harmonics and distortion in the line current [82]. To overcome this issue, an output voltage control loop is designed in order to prevent any change in the load voltage.

3. The DC link capacitor is designed to prevent any harmonics order higher than the second harmonics. This capacitor is designed as follows: Assuming the line current and voltage are both sinusoidal waves and both are in phase to ensure high PF, the peak to peak ripple in the load voltage (the output voltage of the PFC stage) is given by:

$$\Delta V_{\text{o-p-p}} \leq \frac{I_{\text{o}}}{2f_{\text{mod}}C_{\text{dc}}} \tag{8.4}$$

where $\Delta V_{\text{o-p-p}}$ is the peak to peak ripple voltage, I_{o} is DC current (the output current of the PFC) and f_{mod} is the line frequency. Rearranging (8.4) gives:

$$C_{\text{dc}} \geq \frac{I_{\text{o}}}{2f_{\text{mod}}\Delta V_{\text{o-p-p}}} \tag{8.5}$$

It should be noticed that, when doing the loss measurements of the inverter, this means a part of the losses caused by charging/discharging the DC link capacitor (employed to remove high-frequency components in the supply current) has been included because the channels (current and voltage) of

the power analyzer are connected before this capacitor. Furthermore, if the inverter has been well controlled (currents are controlled to sinusoidal shape).

4. Re-dimension of the resistances of the voltage divider and select a new resistance values according the bias current of the comparator in order to reduce the associated loss.

5. Design the control loops (current and voltage) of the proposed PFC. The control loop of the proposed PFC should be able to distinguish between the positive and negative half cycle of the line voltage. Also, the control loop should be able to detect the limit where the AC line voltage exceeds the boundary voltage.

6. Design the PCB for the proposed PFC.

7. Measure the losses in the proposed PFC and compare the results with the computations.

8. Estimate the total cost of different topologies based on mass production process.

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List of Abbreviations

AC	**A**lternating **C**urrent
ACM	**A**verage **C**urrent **M**ode
ARCPI	**A**uxiliary **R**esonant **C**ommutated **P**ole **I**nverter
BCM	**B**oundary **C**onduction **M**ode
CCM	**C**ontinuous **C**onduction **M**ode
COT	**C**onstant **O**n **T**ime
CRM	**CR**itical conduction **M**ode
DBR	**D**iode **B**ridge **R**ectifier
DC	**D**irect **C**urrent
FFT	**F**ast **F**ourier **T**ransformation
HSI	**H**ard **S**witching **I**nverter
HV MOSFET	**H**igh **V**oltage MOSFET
IGBT	**I**sulated **G**ate **B**ipolar**T**ransistor
LV MOSFET	**L**ow **V**oltage MOSFET
MOSFET	**M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor
PF	**P**ower **F**actor
PFC	**P**ower **F**actor **C**orrection
PWM	**P**ulse **W**idth **M**odulation
RGD	**R**esonant **G**ate **D**rive
RMS	**R**oot **M**ean **S**quare
THD	**T**otal **H**armonics **D**istortion

Appendix A

MATLAB Code for Loss Computation - Proposed PFC

```
%% General Informations
fmod = 50;     % Fundamental (electrical) freq. in Hz
Pmax = 70;     % Maximum output power in W
Popt  = 7;       % Optimal output power in W (3-phase)
% RMS universal voltage (customer Voltage)
Vcus_vec= 90:30:270;
% LL Max output voltage in V
Vomax = 0.8*(sqrt(2)*Vcus_vec);
% LL Optimum output voltage in V
Voopt = 0.2*Vomax;
% Max Peak of the load current in A
Iomax = 2*Pmax./(sqrt(3)*Vomax);
% Optimum Peak of the load current in A
Ioopt = 2*Popt./(sqrt(3)*Voopt);
Vo  = 20;%50;   % output voltage
Vb = 50;%90;   % boundary voltage
% Half of fundamental period
t   =(0:0.5/fmod/1000:0.5/fmod);
Lo  = 69   0e-6*3;
effi  = 0.95;       % Desired efficiency
Rgx   = 12;
Vfdd  = 0.6;
Rfdd  = 0.7;
stp   = 20;
Rl    = 0.139*3;
delay11= 150e-9;
delay22= 150e-9;
```

```
28 OperationBB = {'CRMBB-Res','CRMBB+Res'};
29 OperationBB = OperationBB{2};
30 % with noise means with additional signal
31 OnTime = {'without_noise','with_noise'};
32 OnTime = OnTime{1};
33 %% Initialization
34 Dbuck    = zeros(length(Vcus_vec),length(t));
35  t_buck = Dbuck; t_buck_boost = Dbuck; Ts = Dbuck;
36  fs = Dbuck; iLo_p = Dbuck; mat1 = Dbuck;
37 mat2 = Dbuck; Ton = zeros(length(Vcus_vec),1);
38 ILo_av = Dbuck; IACI_rms = Ton; theta0 = Ton; Toff = Dbuck;
39 PF_BB = Ton; THD_BB = Ton; t_3bb = Dbuck; Ton_cons = Ton;
40  I_cond1 = Dbuck; I_cond2 = I_cond1;
41  fs_min = Dbuck;  fs_max = Dbuck;
42 %% MOSFET Data sheet
43 MOSFETBB   = {'M65R1400CFD2'};
44 ind       = 1:length(MOSFETBB);
45 filename = [MOSFETBB{ind}];
46 load (['DeviceDefinitionFolder\xy' filename '.mat']);
47 P_cond_DBRB = zeros(1,length(Vcus_vec));
48 P_cond_BuckB = P_cond_DBRB; P_sw_BuckB  = P_cond_DBRB; Pgt_BuckB = P_cond_DBRB;
49 Pt_BuckB = P_cond_DBRB; P_gt_QA = P_cond_DBRB; P_gt_QB = P_cond_DBRB; P_gt_Qop =
       P_cond_DBRB;
50
51 for indvcus = 1:length(Vcus_vec)
52     Vcus = Vcus_vec(indvcus);
53     Vac_vec = sqrt(2)*Vcus*sin(2*pi*fmod*t);
54     %boundary angle rad
55     theta0(indvcus)  = asin(Vb/(sqrt(2)*Vcus));
56     I1 = find(Vac_vec >= Vb); % Buck Mode
57     for indi1= 1:length(I1);
58         ii1 = I1(indi1);
59         % duty cycle B
60         Dbuck(indvcus,ii1) = Vo./(sqrt(2)*Vcus*sin(2*pi*fmod*t(ii1)));
61         t_buck(indvcus,ii1)= t(ii1);
62         mat1(indvcus,ii1) = 1;
63     end
64     I2 = find(Vac_vec < Vb);  % Buck-Boost Mode
65     for indi2= 1:length(I2);
66         ii2 = I2(indi2);
67         % duty cycle BB
68         Dbuck(indvcus,ii2) = Vo./(sqrt(2)*Vcus*sin(2*pi*fmod*t(ii2))+Vo);
69         t_buck_boost(indvcus,ii2) = t(ii2);
```

```
70          mat2(indvcus,ii2) = 1;
71      end
72      k = 0.85; % Design factor
73      Ton_cons(indvcus) = 2*(pi*Popt/effi)./(k*trapz(2*pi*fmod*t,mat2(indvcus,:)
            .*(((sqrt(2)*Vcus*sin(2*pi*fmod*t)).^2*Vo)./(Lo*(sqrt(2)*Vcus*sin(2*pi*
            fmod*t)+Vo))))+trapz(2*pi*fmod*t,Vo*mat1(indvcus,:).*((sqrt(2)*Vcus*sin
            (2*pi*fmod*t)-Vo)/Lo)));
74      switch OnTime
75          case 'without_noise'
76              Ton =  Ton_cons(indvcus)*ones(1,length(t));
77          case 'with_noise'
78              Ton = Ton_cons(indvcus)*(1-0.33*sin(3*2*pi*fmod*t)-0.05*sin(5*2*pi*
                    fmod*t));
79      end
80      switch OperationBB
81          case 'CRMBB-Res'
82              t_3bb(indvcus,:)  = 0;
83
84          case 'CRMBB+Res'
85              % Resonance MOSDE
86              t_rvBB  = zeros(1,length(t));
87               t_res_omegaBB = t_rvBB;
88              I_rBB   = zeros(stp+1,length(t));
89              t_cBB   = I_rBB; i_bb   = zeros(1,length(t)); V_os_LfBB = i_bb;
90
91              indbb    = find(Vac_vec>2*Vo);
92              V_os_iBB = 0:2*Vo/stp:2*Vo;
93              V_os_LBB = Vac_vec(indbb);
94
95              for indlbb = 1:length(indbb)
96                  V_os_fBB = 0:V_os_LBB(indlbb)/stp:V_os_LBB(indlbb);
97                  %estimate the boost current:
98                  %Energy in Coss at 2*Vo:
99                  Coss_vobb= interp1(xos_data,yos_data*1e-12,V_os_iBB,'spline');
100                 E_os_ibb = trapz(V_os_iBB,V_os_iBB.*Coss_vobb);
101                 % Energy in Coss at (Vac(indb)>2*Vo):
102                 Coss_vfbb= interp1(xos_data,yos_data*1e-12,V_os_fBB,'spline');
103                 E_os_fbb = trapz(V_os_fBB,V_os_fBB.*Coss_vfbb);
104                 % Net energy stored in Lo
105                 E_L_tbb    = E_os_fbb-E_os_ibb;
106                 % Estimated boost current:
107                 i_bb(indbb(indlbb)) = sqrt(2*E_L_tbb/Lo);
108                 V_os_LfBB(indbb(indlbb))= V_os_LBB(indlbb);
```

```
109                 end
110             for indt_rbb=1:length(t)
111                 I_bBB  = -i_bb(indt_rbb);
112                 VrecBB  = Vac_vec(indt_rbb);
113                 mode3_BuckB;
114                 tr_tBB              = [0 cumsum(t_rBB)];
115                 t_rvBB(:,indt_rbb) = max(tr_tBB);
116                 t_cBB(:,indt_rbb)  = [0 cumsum(t_rBB)]';
117                 I_rBB(:,indt_rbb)  = i_rbb';
118                 t_res_omegaBB(:,indt_rbb) = mean(2*pi./omegabb);
119             end
120             t_3bb(indvcus,:)  = t_rvBB;
121     end
122     for indi1= 1:length(I1);
123       ii1         = I1(indi1);
124       Toff(indvcus,ii1) = ((Vac_vec(ii1)-Vo)/Vo).*Ton(ii1);
125       Ts(indvcus,ii1)= Ton(ii1)+Toff(indvcus,ii1)+t_3bb(indvcus,ii1)+delay11+
              delay22;
126       fs(indvcus,ii1)= 1/Ts(indvcus,ii1);
127       fs_min(indvcus,ii1)= Vo/(Ton(ii1)*sqrt(2)*Vcus);
128       fs_max(indvcus,ii1)= 1/(Ton(ii1));
129       iLo_p(indvcus,ii1) = mat1(indvcus,ii1).*(sqrt(2)*Vcus*sin(2*pi*fmod*t(ii1))
             -Vo)*Ton(ii1)/Lo;
130       ILo_av(indvcus,ii1)= iLo_p(indvcus,ii1)*Vo./(2*sqrt(2)*Vcus*sin(2*pi*fmod*t
              (ii1)));
131       I_cond1(indvcus,ii1) = iLo_p(indvcus,ii1);
132     end
133     for indi2= 1:length(I2);
134         ii2         = I2(indi2);
135         Toff(indvcus,ii2)=(Vac_vec(ii2)/Vo)*k*Ton(ii2);
136         Ts(indvcus,ii2)=Ton(ii2)+Toff(indvcus,ii2)+t_3bb(indvcus,ii2)+delay11+
              delay22;
137         fs(indvcus,ii2)=1/Ts(indvcus,ii2);
138         fs_min(indvcus,ii2)=Vo/(k*Ton(ii2)*(1+sqrt(2)*Vcus));
139         fs_max(indvcus,ii2)=1/(k*Ton(ii2));
140         iLo_p(indvcus,ii2)=mat2(indvcus,ii2).*(sqrt(2)*Vcus*sin(2*pi*fmod*t(ii2))
              )*k*Ton(ii2)/Lo;
141         ILo_av(indvcus,ii2)= iLo_p(indvcus,ii2)*Vo./(2*(sqrt(2)*Vcus*sin(2*pi*
              fmod*t(ii2))+Vo*mat2(indvcus,ii2)));
142         I_cond2(indvcus,ii2) = iLo_p(indvcus,ii2);
143     end
144
145     IACI_rms(indvcus)    = rms(ILo_av(indvcus,:));
```

```
146     PF_BB(indvcus) = (Popt/effi)./(Vcus*IACI_rms(indvcus));
147     THD_BB(indvcus)= sqrt((1/PF_BB(indvcus))^2-1);
148 %% Loss analysis:
149 % Mode 1
150     t1BB = (0:1/stp:1)'*Ton;
151     Il1BB = (t1BB/Ton)*iLo_p(indvcus,:);
152 % Mode 2
153     t2BB  = (0:1/stp:1)'*Toff(indvcus,:);
154     Il2BB = -(t2BB-repmat(Toff(indvcus,:),stp+1,1))/Toff(indvcus,:)*iLo_p(indvcus
            ,:);
155 % To compute the diode and the channel currents - MOSFETs:
156 %Body Diode current of MOSFETs (Q\_Bn, Q\_an)-Mode 1:
157     Id1 = (Rds*Il1BB-Vdf)/(Rds+Rf);
158     % Channel current
159     Ich1 = (Vdf+Rf*Il1BB)/(Rds+Rf);
160     % Body Diode current of MOSFETs (synch-rec)-Mode 2:
161     Id2 = (Rds*Il2BB-Vdf)/(Rds+Rf);
162     % Channel current
163     Ich2 = (Vdf+Rf*Il2BB)/(Rds+Rf);
164 %Check the channel and the diode current-Main switches:
165 % Mode 1:
166     indsI1 = find(Id1<0);
167     Ich1(indsI1)=Il1BB(indsI1);
168     Id1(indsI1)=0;
169     % Mode 1:
170     indsI2 = find(Id2<0);
171     Ich2(indsI2)=Il2BB(indsI2);
172     Id2(indsI2)=0;
173 % Loss analysis Conventional Buck:
174 % Conduction losses-Mode 1:
175     indvac = indvcus;
176     E_cond_Mod1BB_DBR = (Vfdd*(k*I_cond1(indvcus,:)/2+I_cond2(indvcus,:)/2)+(Rfdd
            )*(k*(I_cond1(indvcus,:).^2/3)+(I_cond2(indvcus,:).^2/3))).*Ton+(Vdf*
            trapz(Id1)+Rf*trapz(Id1.^2))*(1/stp).*Ton;
177     E_cond_Mod1BB_SWI = ((Rds)*(k*(I_cond1(indvcus,:).^2/3)+(I_cond2(indvcus,:)
            .^2/3))).*Ton+(Rds*trapz(Ich1.^2))*(1/stp).*Ton;
178     % Conduction losses-Mode 2:
179     E_cond_Mod2BB_SWI = (Rds)*(I_cond1(indvcus,:).^2/3+I_cond2(indvcus,:).^2/3).*
            Toff(indvac,:);
180 switch OperationBB
181         case 'CRMBB-Res'
182             E_cond_Mod3BB = 0;
183     % The switching losses:
```

```
184     % Interpolate Coss, Crss:
185             interpolCaps_kconv;
186     % Turn on losses:
187     % Reise time calculation/current: nominal rise time
188             trn = (Rg+Rgx)*Ciss*log((Vdr-Vth)/(Vdr-Vgp));
189    % new rise time
190             tr = (trn/In)*iLo_p(indvac,:);
191     % gate current Igon
192             Ig_onB = (Vdr-Vgp)/(Rg+Rgx);
193             v_ds_buckB = 0:0.1*(Vac_vec+1e-5):Vac_vec+1e-5;
194             Efv_mat_buckB = zeros(1,length(t)); Erv_matB = Efv_mat_buckB;
195             tf_vmat_buckB = Qgd_on_BuckB(:,indvac)*((1-Rds*...
196                 iLo_p(indvac,:)./(Vac_vec+1e-5))/Ig_onB);
197             p_on_BuckB  = v_ds_buckB'*iLo_p(indvac,:);
198             for n = 1:length(iLo_p(indvac,:));
199                 Efv_mat_buckB(n) = trapz(tf_vmat_buckB(:,n),p_on_BuckB(:,n));
200             end
201      % This includes the integration of load current and ds voltage over voltage
            fall time plus the losses during the current rise time
202             EonMv_BuckB = Efv_mat_buckB; %sum(Efv_mat);
203             EonMi_BuckB = 0.5*(Vac_vec.*iLo_p(indvac,:)).*tr;
204             % The losses due to the reverse recovery charge
205             EonrrB= 0;
206             % The losses due to the output capacitance
207             Eoss_BuckB = Qoss_BuckB(indvac)*(Vac_vec);
208             % Turn off losses:}
209             % Fall time calculation: nominal fall time
210             tfn = (Rg+Rgx)*Ciss*log(Vgp/Vth);
211             % new fall time
212             tf = (tfn/In)*iLo_p(indvac,:);
213             % gate currentIgoff
214             Ig_offB = Vgp/(Rg+Rgx);
215             tr_vmat= Qgd_off_BuckB(:,indvac)*((1-Rds*iLo_p(indvac,:)./(Vac_vec+1e
                    -5))/Ig_offB);
216             p_off_BuckB  = v_ds_buckB'*iLo_p(indvac,:);
217             for n = 1:length(iLo_p(indvac,:))
218                 Erv_matB(n) = trapz(tr_vmat(:,n),p_off_BuckB(:,n));
219             end
220             % Energy losses in turn off state of MOSFET
221             EoffMv_BuckB = Erv_matB; %sum(Erv_mat);
222             EoffMi_BuckB = 0.5*(Vac_vec.*iLo_p(indvac,:)).*tf;
223             % Energy losses in turn off state of DIODE
224             EoffDB= 0;
```

```
225                 EoffM_BuckB=(EoffMi_BuckB+EoffMv_BuckB);
226                 % Energy losses in turn on state in MOSFET
227                 EonM_BuckB=(EonMi_BuckB+EonMv_BuckB+EonrrB+Eoss_BuckB);
228             case 'CRMBB+Res'
229             E_cond_Mod3BB = Rl*trapz(I_rBB.^2).*t_3bb(indvcus,:)*(1/stp);
230               % The switching losses:
231                % Interpolate Coss, Crss:
232                 interpolCaps_kconv;
233                 % This includes the integration of load current and ds voltage over
                        voltage fall time plus the losses during the current rise time
234                 EonMv_BuckB = 0; %ZVS
235                 EonMi_BuckB = 0;  %ZCS
236                 % The losses due to the reverse recovery charge
237                 EonrrB= 0;
238                 % The losses due to the output capacitance
239                 Eoss_BuckB = 0; % soft switching
240                % Turn off losses:
241                %Fall time calculation: nominal fall time
242                 tfn = (Rg+Rgx)*Ciss*log(Vgp/Vth);
243                 % new fall time
244                 tf = (tfn/In)*iLo_p(indvac,:);
245                 EoffM_BuckB=(iLo_p(indvac,:).*tf).^2/(4*6*Coss_BuckB);
246                 % Energy losses in turn on state in MOSFET
247                 EonM_BuckB=(EonMi_BuckB+EonMv_BuckB+EonrrB+Eoss_BuckB);
248         end
249 %% Sum up switching losses
250  % Conduction losses
251         Econd_BuckB = E_cond_Mod1BB_SWI+E_cond_Mod2BB_SWI+E_cond_Mod3BB;
252         % Total Switching losses in MOSFET
253         Esw_BuckB = (EonM_BuckB+EoffM_BuckB);
254         % Gate Drive Energy
255         Egt_BuckB = Qgt*(Vdr/Vqg)*Vdr; % eq(4.20)
256 %Power losses:
257         P_cond_DBRB(indvac) =(2*fmod)*trapz(t,E_cond_Mod1BB_DBR.*fs(indvac,:));
258         P_cond_BuckB(indvac)=(2*fmod)*trapz(t,Econd_BuckB.*fs(indvcus,:));
259         P_sw_BuckB(indvac)=(2*fmod)*trapz(t,Esw_BuckB.*fs(indvcus,:));
260         P_gt_QA(indvac)= (2*fmod)*trapz(t(I2),(Egt_BuckB*ones(1,length(I2)).*fs(
                indvcus,I2)))+(2*50*Qgt*(Vdr/Vqg)*Vdr);
261         P_gt_QB(indvac)      = (2*fmod)*trapz(t(I1),(Egt_BuckB*ones(1,length(I1)).*fs(
                indvcus,I1)));
262         P_gt_Qop(indvac)     = (2*fmod)*trapz(t,(Egt_BuckB*ones(1,length(t)).*fs(
                indvcus,:)));
263         Pgt_BuckB(indvac)    = P_gt_QA(indvac)+P_gt_QB(indvac)+P_gt_Qop(indvac);
```

```
264     Pt_BuckB(indvac)     = P_cond_DBRB(indvac)+P_cond_BuckB(indvcus)+P_sw_BuckB(
            indvcus)+Pgt_BuckB(indvcus);
265 end
266
267 % Conventional Buck Mode Synch. Rec.
268 CRM_COT_BUCK; % This m. file  simulates the conventional PFC, See Appendix B
269 close all
270
271 %% FFT:
272 % Half of fundamental period
273 t_n = (0.5/fmod:0.5/fmod/1000:1/fmod);
274 figure(7);subplot(2,1,1);
275 plot(t*2*180*fmod,sqrt(2)*Vcus_vec(1)*sin(2*pi*fmod*t),'b--',t_n*2*180*fmod,sqrt
        (2)*Vcus_vec(1)*sin(2*pi*fmod*t_n),'b--',...
276 'LineWidth',1.5);legend('Vac_{rms}=90V');xlabel('\Theta');set(gca,'FontSize',12);
277 grid minor;hold off; ylabel('Line voltage');set(gca,'XLim',[0 360]); set(gca,'
        FontSize',12);
278 subplot(2,1,2);
279 plot(t*2*180*fmod,1000*ILo_av(1,:),'b',t_n*2*180*fmod,-1000*ILo_av(1,:),'b','
        LineWidth',1.5);
280 xlabel('\Theta');set(gca,'FontSize',12); grid minor;hold off;ylabel('Line current
        -mA')
281 set(gca,'XLim',[0 360]); set(gca,'FontSize',12);legend('Iac_{av}@90V');
282
283 i_l_t_1 = [ILo_av(1,:) -ILo_av(1,:)];
284 i_fft_1 = fft(i_l_t_1);
285 % Ploting the FFT of line current:
286 i_fft_1_mag2 = abs(i_fft_1)/(2*length(t));
287 i_fft_1_mag1 = i_fft_1_mag2(1:(2*length(t))/2+1);
288 i_fft_1_mag1(2:end-1) = 2*i_fft_1_mag1(2:end-1);
289 % Sampling freq.
290 f_fs1  = 1/(t(2)-t(1))*(0:length(t))/(2*length(t));
291 figure(9);subplot(2,1,1);
292 plot(t*2*180*fmod,sqrt(2)*Vcus_vec(end)*sin(2*pi*fmod*t),'b--',t_n*2*180*fmod,
        sqrt(2)*Vcus_vec(end)*sin(2*pi*fmod*t_n),'b--','LineWidth',1.5);legend('Vac_{
        rms}=260V');xlabel('\Theta');set(gca,'FontSize',12);
293 grid minor;ylabel('Line voltage');set(gca,'XLim',[0 360]); set(gca,'FontSize',12)
        ;
294 subplot(2,1,2);
295 plot(t*2*180*fmod,1000*ILo_av(end,:),'b',t_n*2*180*fmod,-1e3*ILo_av(end,:),'b','
        LineWidth',1.5);
296 xlabel('\Theta');set(gca,'FontSize',12);grid minor;hold off;ylabel('Line current-
        mA')
```

```
297 set(gca,'XLim',[0 360]); set(gca,'FontSize',12);legend('Iac_{av}@260V');
298
299 i_l_t_end = [ILo_av(end,:) -ILo_av(end,:)];
300 i_fft_end = fft(i_l_t_end);
301 % Ploting the FFT of line current:
302 i_fft_end_mag2 = abs(i_fft_end)/(2*length(t));
303 i_fft_end_mag1 = i_fft_1_mag2(1:(2*length(t))/2+1);
304 i_fft_end_mag1(2:end-1) = 2*i_fft_end_mag1(2:end-1);
305 % Sampling freq.
306 f_fs2  = 1/(t(2)-t(1))*(0:length(t))/(2*length(t));
307 % IEC61000-3-2 standard: (NO LIMITS for EQUIPMANTS HAS LOWER POWER THAN
308 % 75W(RATED));
309 Hr_or=[0 1 0.02 0.09 0.02 0.04 0.02 0.03 0.02 0.02 0.02 0.01 0 0.01 0 0.01 0 0.01
        0 0.01 0 0.01 0 0.01 0 0.01 0 0.01 0 0.01 0 0.01 0 0.01 0 0.01];
310 f_f_f = 0:35;
311 figure(11);subplot(2,1,1);
312 plot(f_f_f,Hr_or,'b',f_c_fs1/fmod,i_c_fft_1_mag1/i_c_fft_1_mag1(2),'r',f_fs1/fmod
        ,i_fft_1_mag1i_fft_1_mag1(2),'g','LineWidth',1.5);
313 set(gca,'FontSize',12);xlim([0 35]);ylim([0 1.1]);
314 grid minor;title('Single-Sided Amplitude Spectrum of i_{ac}(t), 90V');
315 xlabel('Harmonics order');ylabel('Amplitude spectrum');
316 legend('IEC61000-3-2','Conventional','Proposed','Location','best');set(gca,'
        FontSize',12);set(gca,'FontSize',12);
317
318 subplot(2,1,2);
319 plot(f_f_f,Hr_or,'b-.',f_c_fs2/fmod,i_c_fft_end_mag1/i_c_fft_end_mag1(2),'r-.',
        f_fs2/fmod,i_fft_end_mag1/i_fft_end_mag1(2),'g-.','LineWidth',1.5);set(gca,'
        FontSize',12);xlim([0 35]);ylim([0 1.1]);
320 grid minor;title('Single-Sided Amplitude Spectrum of i_{ac}(t), 260V');
321 xlabel('Harmonics order');ylabel('Amplitude spectrum');
322 legend('IEC61000-3-2','Conventional','Proposed','Location','best');
323 set(gca,'FontSize',12);
324 figure(12);plot(2*fmod*t*180,[(Ton_cons(end)*1e6.*ones(1,length(t)))'(Ton_cons(
        end)*1e6.*(1-0.33*sin(3*2*pi*fmod*t)-0.05*sin(5*2*pi*fmod*t)))'],'LineWidth'
        ,1.5);
325 set(gca,'FontSize',12);grid minor;xlim([0 180]);
326 xlabel('\theta');ylabel('Time in\mu s');legend('Ton','Ton+nois');
327
328 switch OperationBB
329     case 'CRMBB+Res'
330         figure(13);plot(2*fmod*t*180,[i_b' i_bb' Vac_vec'/10000 2*Vo/10000*ones(
                length(t),1)],'LineWidth',1.5);
331         set(gca,'FontSize',12);xlim([0 180]);ylim([0 50e-3]);grid minor;
```

```
332         xlabel('\Theta');ylabel('Boost current');legend('I_{b}-conventional','I_{
                b}-proposed');
333 end
334
335 figure(15);subplot(3,1,1);
336 plot(Vac_rms,fs_rms_min*1e-3,'b--',Vcus_vec,fs_min(:,1)*1e-3,'b',Vac_rms,
        fs_rms_max*1e-3,'r--',Vcus_vec,fs_max(:,end)*1e-3,'r','LineWidth',2);grid
        minor;
337 xlabel('Vac_{rms} V'),ylabel('fs_{min-max}(Vac_{rms}) kHz');xlim([80 280]);
338 legend('Conv. fs_{min}','Prop. fs_{min}','Conv. fs_{max}','Prop. fs_{max}','
        Location','BestOutside');
339 title('(d) Min-Max f_{s}');
340 subplot(3,1,2);
341 plot(Vac_rms,Ton_rms*1e6,'b--',Vcus_vec,Ton_cons*1e6,'b','LineWidth',1.5);
342 grid minor;legend('T_{con-on}','T_{prop-on}','Location','BestOutside');
343 xlabel('V_{rms} in V');ylabel('Time in us');set(gca,'FontSize',12);
344 xlim([80 280]);ylim([0 20]);title('(e) On Time');
345 subplot(3,1,3);
346 plot(2*t(I)*180*fmod,Tof_rms(end,I)*1e6,'b--',2*t*180*fmod,Toff(end,:)*1e6,'b','
        LineWidth',1.5);
347 xlabel('\theta'),ylabel('Tim in us');grid minor;set(gca,'FontSize',12);
348 legend('T_{con-off}','T_{prop-off}','Location','BestOutside');
349 title('(f) Off time at 270V_{rms}');ylim([0 30]);xlim([0 180]);
350
351 figure(16);plot(2*fmod*t*180,fs_rms(1,:)*1e-3,'b--',2*fmod*t*180, fs(1,:)*1e-3,'b
        ',2*fmod*t*180,fs_rms(end,:)*1e-3,'r--',2*fmod*t*180,fs(end,:)*1e-3,'r','
        LineWidth',2);grid minor;
352 legend('Conv. 90V','Prop. 90V','Conv. 260V','Prop. 260V','Location','Best');
353 xlabel('\theta');xlim([0 180]);set(gca,'FontSize',12);
354 ylabel('f_{s} in kHz');
355
356 str = 'k';
357 num = k;
358 figure(14);subplot(2,1,1);
359 plot(t*2*180*fmod,1000*ILo_av(1,:),'b',t_n*2*180*fmod,-1e3*ILo_av(1,:),'b','
        LineWidth',1.5);
360 hold on;plot(t*2*180*fmod,1e3*max(ILo_av(1,:))*sin(2*pi*fmod*t),'b--',t_n*2*180*
        fmod,1e3*max(ILo_av(1,:))*sin(2*pi*fmod*t_n),'b--','LineWidth',1.5);
361 legend('Iac_{av}@90V');xlabel('\Theta');set(gca,'FontSize',12);hold on;
362 grid minor;hold off;ylabel('Line current mA');
363 set(gca,'XLim',[0 360]); set(gca,'FontSize',12);
364 title([str '= ' num2str(k)]);
365
```

```
366 subplot(2,1,2);
367 plot(t*2*180*fmod,1000*ILo_av(end,:),'r',t_n*2*180*fmod,-1e3*ILo_av(end,:),'r','
        LineWidth',1.5);
368 hold on;plot(t*2*180*fmod,1e3*max(ILo_av(end,:))*sin(2*pi*fmod*t),'r--',t_n
        *2*180*fmod,1e3*max(ILo_av(end,:))*sin(2*pi*fmod*t_n),'r--','LineWidth',1.5);
369 legend('Iac_{av}@260V');xlabel('\Theta');set(gca,'FontSize',12);hold on;
370 grid minor;hold off;ylabel('Line current mA');
371 set(gca,'XLim',[0 360]); set(gca,'FontSize',12);
372 title([str '= ' num2str(k)]);
373
374 %% mode3_BuckB
375 Vds_2bb  = 0:(VrecBB+0.2)/stp:VrecBB+0.2;        % Drain source of M2
376 Vds_1bb  = VrecBB+0.2:-(VrecBB+0.2)/stp:0;       % Drain source of M1
377
378 t_rBB = zeros(1,length(Vds_2bb)-1);
379 i_rbb =zeros(1,length(Vds_2bb));
380 A_rbb = t_rBB; B_rbb = t_rBB; V_cbb = t_rBB;
381
382 Cds2bb     = interp1(xos_data,yos_data*1e-12,Vds_2bb,'spline');
383 Cds1bb     = interp1(xos_data,yos_data*1e-12,Vds_1bb,'spline');
384 Cresbb     = Cds1bb+Cds2bb;
385 deltabb    = Rl/(2*Lo);              % Damping factor
386 omegabb    = sqrt(-deltabb.^2+1./(Lo*Cresbb));
387 lambda_1bb = -deltabb +1i*omegabb;
388 lambda_2bb = -deltabb -1i*omegabb;
389
390 A_rbb(1) = (I_bBB-Cresbb(1)*lambda_2bb(1)*(Vo-VrecBB+Vds_1bb(1)))/(Cresbb(1)*(
        lambda_1bb(1)-lambda_2bb(1)));
391 B_rbb(1) = (-I_bBB+Cresbb(1)*lambda_1bb(1)*(Vo-VrecBB+Vds_1bb(1)))/(Cresbb(1)*(
        lambda_1bb(1)-lambda_2bb(1)));
392 i_rbb(1) = I_bBB;
393 V_cbb(1) = Vds_1bb(1);
394
395 t_rBB(1) = real( (1/(1i*omegabb(1))*log( (-(VrecBB-Vo-Vds_1bb(2)) + sqrt((VrecBB-
        Vo-Vds_1bb(2))^2-4*A_rbb(1)*B_rbb(1)))/(2*A_rbb(1)))));
396
397 for inddbb = 2:length(Vds_2bb)-1
398 V_cbb(inddbb) = A_rbb(inddbb-1)*exp(lambda_1bb(inddbb-1)*t_rBB(inddbb-1))+B_rbb(
        inddbb-1)*exp(lambda_2bb(inddbb-1)*t_rBB(inddbb-1))+VrecBB-Vo;
399 i_rbb(inddbb) = Cresbb(inddbb-1)*(A_rbb(inddbb-1)*lambda_1bb(inddbb-1)*exp(
        lambda_1bb(inddbb-1)*t_rBB(inddbb-1))+B_rbb(inddbb-1)*lambda_2bb(inddbb-1)*
        exp(lambda_2bb(inddbb-1)*t_rBB(inddbb-1)));
```

```
400 A_rbb(inddbb) = (i_rbb(inddbb)-Cresbb(inddbb)*lambda_2bb(inddbb)*(Vo-VrecBB+
        Vds_1bb(inddbb)))/(Cresbb(inddbb)*(lambda_1bb(inddbb)-lambda_2bb(inddbb)));
401 B_rbb(inddbb) = (-i_rbb(inddbb)+Cresbb(inddbb)*lambda_1bb(inddbb)*(Vo-VrecBB+
        Vds_1bb(inddbb)))/(Cresbb(inddbb)*(lambda_1bb(inddbb)-lambda_2bb(inddbb)));
402 t_rBB(inddbb) = real( (1/(1i*omegabb(inddbb))*log( (-(VrecBB-Vo-Vds_1bb(inddbb+1)
        ) + sqrt((VrecBB-Vo-Vds_1bb(inddbb+1))^2-4*A_rbb(inddbb)*B_rbb(inddbb)))/(2*
        A_rbb(inddbb)))));
403 end
404 inddbb = length(Vds_2bb);
405 V_cbb(inddbb) = A_rbb(inddbb-1)*exp(lambda_1bb(inddbb-1)*t_rBB(inddbb-1))+B_rbb(
        inddbb-1)*exp(lambda_2bb(inddbb-1)*t_rBB(inddbb-1))+VrecBB-Vo;
406 i_rbb(inddbb) = Cresbb(inddbb-1)*(A_rbb(inddbb-1)*lambda_1bb(inddbb-1)*exp(
        lambda_1bb(inddbb-1)*t_rBB(inddbb-1))+B_rbb(inddbb-1)*lambda_2bb(inddbb-1)*
        exp(lambda_2bb(inddbb-1)*t_rBB(inddbb-1)));
407
408 figure(1); plot([0 cumsum(t_rBB)],i_rbb,'LineWidth',1.5) ;xlabel('Time [S]');
        ylabel('Resonant current [A]') ;grid minor;set(gca,'FontSize',12);
409  figure(2); plot([0 cumsum(t_rBB)],[V_cbb' Vds_1bb'],'LineWidth',1.5);xlabel('
         Time [S]');ylabel({'Capacitor Voltage [V]','Vds1'});grid minor;set(gca,'
         FontSize',12);
```

Appendix B

MATLAB Code for Loss Computation - Conventional PFC

```
%% General Informations
%See appendix A - General Information
Test  = {'DC_test','AC_test'};
Test  = Test{2};
Operation = {'CRM-Hard-Switching','CRM-ZVS'};
Operation = Operation{2};
 %Select Test: DC or AC
switch Test
    case 'DC_test'
        Vac_rms = 90:30:300;
    case 'AC_test'
        Vac_rms = 90:30:270;
end
  %Initializations:
Iac_av=zeros(length(Vac_rms),length(t));
theta0_rms=zeros(1,length(Vac_rms));
Vac = zeros (1,length(t)); Ts_rms = Iac_av;
 fs_rms = Iac_av;Ton_rms = theta0_rms; IL_p = Iac_av;
 fs_rms_min = theta0_rms;intg_rms = theta0_rms; IAC_av = Iac_av;
  IAC_rms = theta0_rms;Tof_rms = Iac_av;
  D_buck = Iac_av; fs_rms_max = fs_rms_min;
  i_res  = zeros(stp+1,length(t)); t_3  = Iac_av;
  I_Res = zeros(1,stp+1); Il1 = i_res; Il2 = i_res;
   Is = Iac_av; Isrms = Iac_av;
%%%%%%%%%%%%%%%%%%%
P_cond_DBR = zeros(1,length(Vac_rms));
P_cond_Buck = P_cond_DBR; P_sw_Buck  = P_cond_DBR;
```

```
28 Pgt_Buck = P_cond_DBR; Pt_Buck = P_cond_DBR;
29 P_DBR_only = P_cond_DBR; P_Buck_only = P_cond_DBR; P_Lo_only = P_cond_DBR;
30 P_Rse_only = P_cond_DBR; P_Div_only = P_cond_DBR;
31  P_tot_only = P_cond_DBR;P_Buck_cond = P_cond_DBR;
32  P_Buck_swit = P_cond_DBR;
33 %MOSFET Data sheet
34 MOSFET   = {'M65R1400CFD2'};
35 ind      = 1:length(MOSFET);
36 filename = [MOSFET{ind}];
37 load (['DeviceDefinitionFolder\xy' filename '.mat']);
38 for indvac  = 1:length(Vac_rms)
39     switch Test
40         case 'DC_test'
41             Vac_vec  = Vac_rms(indvac).*ones(1,length(t));
42             I = find(Vac_vec > Vo);
43             Vac(I)    = Vac_vec(I);
44             Ton_rms(indvac)  = Po*2*Lo/(eta*Vo*(Vac_rms(indvac)-Vo));
45         case 'AC_test'
46             Vac_vec  = sqrt(2)*Vac_rms(indvac)*sin(2*pi*fmod*t);
47             theta0_rms(indvac) = asin(Vo/(sqrt(2)*Vac_rms(indvac)));
48             I = find(Vac_vec > Vo);
49             Vac(I)    = Vac_vec(I);
50             intg_rms(indvac) = Vo*(2*sqrt(2)*Vac_rms(indvac)*cos(theta0_rms(
                   indvac))-Vo*(pi-2*theta0_rms(indvac)))/Lo;
51             Ton_rms(indvac) = 2*(pi*Po/eta)./intg_rms(indvac); % Ton
52     end
53    switch Operation
54         case 'CRM-ZVS'
55             switch Test
56                 case 'AC_test'
57                     %Resonance MOSDE}
58                     t_rv  = zeros(1,length(t(I))); t_res_omega = t_rv;
59                     I_r   = zeros(stp+1,length(t(I)));
60                     t_c   = I_r; i_b   = zeros(1,length(t)); V_os_Lf = i_b;
61
62                     indb  = find(Vac>2*Vo);
63                     V_os_i = 0:2*Vo/stp:2*Vo;
64                     V_os_L = Vac(indb);
65
66                     for indl = 1:length(indb)
67                         V_os_f = 0:V_os_L(indl)/stp:V_os_L(indl);
68                         % Estimate the boost current:
69                         % Energy in Coss at 2*Vo:
```

```
70                          Coss_vo  = interp1(xos_data,yos_data*1e-12,V_os_i,'spline
                                ');
71                          E_os_i   = trapz(V_os_i,V_os_i.*Coss_vo);
72                        % Energy in Coss at (Vac(indb)>2*Vo):
73                          Coss_vf  = interp1(xos_data,yos_data*1e-12,V_os_f,'spline
                                ');
74                         E_os_f   = trapz(V_os_f,V_os_f.*Coss_vf);
75                          % Net energy stored in Lo
76                          E_L_t    = 8*E_os_f-E_os_i;
77                          % Estimated boost current:
78                          i_b(indb(indl))    = sqrt(2*E_L_t/Lo);
79                          V_os_Lf(indb(indl))= V_os_L(indl);
80                      end
81
82                  case 'DC_test'
83                     %Resonance MOSDE
84                      t_rv  = zeros(1,length(t(I))); t_res_omega = t_rv;
85                      I_r   = zeros(stp+1,length(t(I)));
86                      t_c   = I_r; i_b   = zeros(1,length(t)); V_os_Lf = i_b;
87                      indb  = find(Vac>Vo);
88                      V_os_i = 0:Vo/stp:Vo;
89                      V_os_L = Vac(indb);
90                      for indl = 1:length(indb)
91                          V_os_f = 0:V_os_L(indl)/stp:V_os_L(indl);
92                          % Estimate the boost current:
93                          % Energy in Coss at 2*Vo:
94                          Coss_vo  = interp1(xos_data,yos_data*1e-12,V_os_i,'spline
                                ');
95                          E_os_i   = trapz(V_os_i,V_os_i.*Coss_vo);
96                        % Energy in Coss at (Vac(indb)>2*Vo):
97                          Coss_vf  = interp1(xos_data,yos_data*1e-12,V_os_f,'spline
                                ');
98                          E_os_f   = trapz(V_os_f,V_os_f.*Coss_vf);
99                          % Net energy stored in Lo
100                         E_L_t    = 8*E_os_f-E_os_i;
101                         % Estimated boost current:
102                         i_b(indb(indl))    = sqrt(2*E_L_t/Lo);
103                         V_os_Lf(indb(indl))= V_os_L(indl);
104                     end
105             end
106             for indt_r=1:length(t(I))
107                 I_b  = -i_b(indt_r);
108                 t_don= Lo*abs(I_b)/Vo;
```

```
109                 Vrec   = Vac(I(indt_r));
110                 mode3_Buck;
111                 tr_t             = t_don+[0 cumsum(t_r)];
112                 t_rv(:,indt_r) = max(tr_t);
113                 t_c(:,indt_r)  = t_don+[0 cumsum(t_r)]';
114                 I_r(:,indt_r)  = i_r';
115                 t_res_omega(:,indt_r) = mean(2*pi./omega);
116             end
117             t_3(indvac,I)  = t_rv;
118     end
119           %Inductor current and Toff
120            IL_p(indvac,I)    = (Vac(I)-Vo)*Ton_rms(indvac)/Lo;
121           Tof_rms(indvac,I)= (Vac(I)-Vo)*Ton_rms(indvac)/Vo-delay1-delay2;
122           Iac_av(indvac,I)  = IL_p(indvac,I)*Vo./(2*Vac_vec(I));
123           fs_rms_min(indvac)= Vo/(sqrt(2)*Vac_rms(indvac)*Ton_rms(indvac));
124           fs_rms_max(indvac)= 1./Ton_rms(indvac);
125          %mean(Iac_av(indvac,I));
126          IAC_av (indvac,I) = Iac_av(indvac,I);
127          IAC_rms(indvac)   = rms(Iac_av(indvac,I));
128
129     switch Operation
130         case 'CRM-Hard-Switching'
131             t_3(indvac,I)  = 0;
132             t_don = 0;
133             % fs per switching cycle
134             fs_rms(indvac,I) = 1./(Ton_rms(indvac)+Tof_rms(indvac,I)+t_3(indvac,I
                    )+delay1+delay2);
135             Ts_rms(indvac,I) = (Ton_rms(indvac)+Tof_rms(indvac,I)+t_3(indvac,I));
                     % Ts per switching cycle
136              % D per switching cycle
137             D_buck(indvac,I) = Ton_rms(indvac)./(Ts_rms(indvac,I));
138
139         case 'CRM-ZVS'
140             % fs per switching cycle
141             fs_rms(indvac,I) = 1./(Ton_rms(indvac)+Tof_rms(indvac,I)+t_3(indvac,I
                    )+delay1+delay2);
142             % Ts per switching cycle
143             Ts_rms(indvac,I) = (Ton_rms(indvac)+Tof_rms(indvac,I)+t_3(indvac,I));
144             % D per switching cycle
145             D_buck(indvac,I) = Ton_rms(indvac)./(Ts_rms(indvac,I));
146
147     end
148      %Loss analysis Conventional Buck}
```

```
149     switch Operation
150         case 'CRM-Hard-Switching'
151             % Conduction losses:
152             E_DBR_only  = (2*Vfdd*IL_p(indvac,I)/2+2*Rfdd*(IL_p(indvac,I).^2/3))
                    .*Ton_rms(indvac);
153             E_Buck_only= (Rds+R_pcb)*(IL_p(indvac,I).^2/3).*(Ton_rms(indvac)+
                    Tof_rms(indvac,I)+t_don);
154             E_RLo_only = Rl*(IL_p(indvac,I).^2/3).*Ts_rms(indvac,I);
155             E_Rse_only = Rsens*(IL_p(indvac,I).^2/3).*Ts_rms(indvac,I);
156             E_cond_Mod3 = 0;
157             %The switching losses:
158             %Interpolate Coss,Crss:
159             interpolCaps_buck;
160             % Turn on losses: Reise time calculation/current: nominal rise time
161            trn = (Rg+Rgx_on)*Ciss*log((Vdr-Vth)/(Vdr-Vgp));
162             % new current rise time
163             tr = (trn/In)*IL_p(indvac,I);
164             % gate current Igon
165             Ig_on = (Vdr-Vgp)/(Rg+Rgx_on);
166             v_ds_buck = 0:0.1*Vac(I):Vac(I);
167             Efv_mat_buck = zeros(1,length(t(I)));
168             Erv_mat = Efv_mat_buck;
169             tf_vmat_buck = Qgd_on_Buck(:,indvac)*((1-Rds*IL_p(indvac,I)./(Vac(I))
                    )/Ig_on);
170             p_on_Buck  = v_ds_buck'*IL_p(indvac,I);
171             for n = 1:length(IL_p(I));
172                 Efv_mat_buck(n) = trapz(tf_vmat_buck(:,n),p_on_Buck(:,n));
173             end
174             %  This includes the integration of load current and ds voltage  over
                     voltage fall time plus the losses during the current rise time
                    During the voltage fall time the resonant current  must be used
                    instead of the peak inductor current to compute EonMv_Buck
175             EonMv_Buck =  Efv_mat_buck;
176             EonMi_Buck = 0.5*(Vac(I).*IL_p(indvac,I)).*tr;
177             %  The losses due to the reverse recovery charge
178             Eonrr= 0*(Qrr/In)*IL_p(indvac,I).*Vac(I);
179
180             % The losses due to the output capacitance and parasitic caps of Lo
181             Eoss_Buck = Qoss_Buck.*Vac(I);
182             Einst     = ((C_Lo+C_N5)*Vac(I)).*Vac(I);
183            %Turn off losses:
184            %Fall time calculation: nominal fall time
185             tfn = (Rg+Rgx)*Ciss*log(Vgp/Vth);
```

```
186             % new curren fall time
187             tf_c = (tfn/In)*IL_p(indvac,I);
188                 % Energy losses in turn off state of MOSFET
189                 EoffMv_Buck = Erv_mat; %sum(Erv_mat);
190                 EoffMi_Buck = 0.5*(Vac(I).*IL_p(indvac,I)).*tf_c;
191                 % Energy losses in turn off state of DIODE
192                 EoffD= 0;
193                 EoffM_Buck= EoffMv_Buck+EoffMi_Buck;
194             end
195             EoffM_Buck=(IL_p(indvac,I).*tf_c).^2/(4*6*(Coss_Buck+C_N5+C_Lo));
196             EonM_Buck=(EonMi_Buck+EonMv_Buck+Eonrr+Eoss_Buck+Einst);
197
198         case 'CRM-ZVS'
199             % Conduction losses:
200             E_DBR_only  = (2*Vfdd*IL_p(indvac,I)/2+2*Rfdd*(IL_p(indvac,I).^2/3))
                    .*Ton_rms(indvac);
201             E_Buck_only= (Rds+R_pcb)*(IL_p(indvac,I).^2/3).*(Ton_rms(indvac)+
                    Tof_rms(indvac,I)+t_don);
202             E_RLo_only = Rl*(IL_p(indvac,I).^2/3).*Ts_rms(indvac,I);
203             E_Rse_only = Rsens*(IL_p(indvac,I).^2/3).*Ts_rms(indvac,I);
204             E_cond_Mod3 = Rl*trapz(I_r.^2).*t_3(indvac,I)*(1/stp);
205            %The switching losses:
206            %Interpolate Coss,Crss:
207             interpolCaps_buck;
208             EonMv_Buck = 0; % ZVS,
209             EonMi_Buck = 0; % ZCS
210             % The losses due to the reverse recovery charge
211             Eonrr= 0;
212             Eoss_Buck  = 0;
213             %Turn off losses:
214             %Fall time calculation: nominal fall time
215             tfn = (Rg+Rgx)*Ciss*log(Vgp/Vth);
216             % new curren fall time
217             tf_c = (tfn/In)*IL_p(indvac,I);
218             EoffM_Buck=2*(IL_p(indvac,I).*tf_c).^2/(4*6*(Coss_Buck+C_Lo+C_N5+
                    C_prob));
219             % Energy losses in turn on state in MOSFET
220             EonM_Buck=(EonMi_Buck+EonMv_Buck+Eonrr+Eoss_Buck);
221     end
222 %Conduction Losses
223     Econd_Buck = E_DBR_only+E_Buck_only+E_cond_Mod3;
224 %Sum up switching losses
225 %Total Switching losses in MOSFET
```

```
226     Esw_Buck = (EonM_Buck+EoffM_Buck);
227
228 %Gate Drive Energy
229     Egt_Buck = 2*Qgt*(Vdr/Vqg)*Vdr*ones(1,length(t(I)));
230
231 %Power losses:
232     P_cond_Buck(indvac)= (2*fmod)*trapz(t(I),Econd_Buck.*fs_rms(indvac,I));
233     P_sw_Buck(indvac)  = (2*fmod)*trapz(t(I),Esw_Buck.*fs_rms(indvac,I));
234     Pgt_Buck(indvac)   = (2*fmod)*trapz(t(I),Egt_Buck.*fs_rms(indvac,I));
235     Pt_Buck(indvac)    = P_cond_Buck(indvac)+P_sw_Buck(indvac)+Pgt_Buck(indvac);
236     P_DBR_only(indvac) = (2*fmod)*trapz(t(I),E_DBR_only.*fs_rms(indvac,I));
237     P_Buck_cond(indvac)= (2*fmod)*trapz(t(I),(E_Buck_only+E_cond_Mod3).*fs_rms(
            indvac,I));
238     P_Buck_swit(indvac)= (2*fmod)*trapz(t(I),Esw_Buck.*fs_rms(indvac,I));
239     P_Buck_only(indvac)= P_Buck_cond(indvac)+P_Buck_swit(indvac);
240     P_Div_only(indvac) = (Vac_rms(indvac))^2/Rdivd;
241     P_Lo_only(indvac)  = 0*(2*fmod)*trapz(t(I),E_RLo_only.*fs_rms(indvac,I));
242     P_Rse_only(indvac) = (2*fmod)*trapz(t(I),E_Rse_only.*fs_rms(indvac,I));
243     P_tot_only(indvac) = P_DBR_only(indvac)+P_Buck_only(indvac)+P_Div_only(indvac
            )+P_Lo_only(indvac)+P_Rse_only(indvac);
244 end
245 figure(26);plot(Vac_rms,P_DBR_only*1e3,'b',Vac_rms,P_Buck_only*1e3,'r',Vac_rms,
        Pgt_Buck*1e3,'b-o'  ,Vac_rms,P_Div_only*1e3,'k',Vac_rms,P_Rse_only*1e3,'c',
        Vac_rms,1e3*P_tot_only,'g','LineWidth',1.5);
246 xlabel('V_{rms} in V');grid minor;ylabel('Losses mW');
247 legend('P_{DBR}','P_{cond+sw}','P_{gt}','P_{divider}','P_{Rsens}','P_{t}','
        Location','bestoutside');
248 set(gca,'FontSize',12);xlim([80 280]);ylim([0 P_tot_only(end)*1e3+10]);
249
250 PF = zeros(1,length(Vac_rms)); THD = PF;
251 for indvo = 1:length(Vac_rms)
252     PF(indvo) = (Po/eta)./(Vac_rms(indvo)*IAC_rms(indvo));
253     THD(indvo) = sqrt((1/PF(indvo))^2-1);
254 end
255 %FFT
256 i_c_t_1 = [Iac_av(1,:) -Iac_av(1,:)];
257 i_c_fft_1 = fft(i_c_t_1);
258
259 % Ploting the FFT of line current:
260 i_c_fft_1_mag2 = abs(i_c_fft_1)/(2*length(t));
261 i_c_fft_1_mag1 = i_c_fft_1_mag2(1:(2*length(t))/2+1);
262 i_c_fft_1_mag1(2:end-1) = 2*i_c_fft_1_mag1(2:end-1);
263 % Sampling freq.
```

```
264 f_c_fs1  = 1/(t(2)-t(1))*(0:length(t))/(2*length(t));
265
266 i_c_t_end = [Iac_av(end,:) -Iac_av(end,:)];
267 i_c_fft_end = fft(i_c_t_end);
268
269 % Ploting the FFT of line current:
270 i_c_fft_end_mag2 = abs(i_c_fft_end)/(2*length(t));
271 i_c_fft_end_mag1 = i_c_fft_end_mag2(1:(2*length(t))/2+1);
272 i_c_fft_end_mag1(2:end-1) = 2*i_c_fft_end_mag1(2:end-1);
273 % Sampling freq.
274 f_c_fs2  = 1/(t(2)-t(1))*(0:length(t))/(2*length(t));
275
276 %% mode3_Buck
277 % Initializations
278 %Vrec   = max(Vac);
279 Vds_2  = 0:Vrec/stp:Vrec;        % Drain source of M2
280 Vds_1  = Vrec:-Vrec/stp:0;       % Drain source of M1
281 t_r = zeros(1,length(Vds_2)-1);
282 i_r =zeros(1,length(Vds_2));
283 A_r = t_r; B_r = t_r; V_c = t_r;
284
285 Cds2     = interp1(xos_data,yos_data*1e-12,Vds_2,'spline');
286 Cds1     = interp1(xos_data,yos_data*1e-12,Vds_1,'spline');
287 Cres     = Cds1+Cds2+C_Lo+C_prob+C_N5;
288 delta    = Rl/(2*Lo);            % Damping factor
289 omega    = sqrt(-delta.^2+1./(Lo*Cres));
290 lambda_1 = -delta +1i*omega;
291 lambda_2 = -delta -1i*omega;
292
293 A_r(1) = (I_b-Cres(1)*lambda_2(1)*(Vo-Vrec+Vds_1(1)))/(Cres(1)*(lambda_1(1)-
        lambda_2(1)));
294 B_r(1) = (-I_b+Cres(1)*lambda_1(1)*(Vo-Vrec+Vds_1(1)))/(Cres(1)*(lambda_1(1)-
        lambda_2(1)));
295 i_r(1) = I_b;
296 V_c(1) = Vds_1(1);
297
298 t_r(1) = real( (1/(1i*omega(1))*log( (-(Vrec-Vo-Vds_1(2)) + sqrt((Vrec-Vo-Vds_1
        (2))^2-4*A_r(1)*B_r(1)))/(2*A_r(1)))));
299
300 for indd = 2:length(Vds_2)-1
301 V_c(indd) = A_r(indd-1)*exp(lambda_1(indd-1)*t_r(indd-1))+B_r(indd-1)*exp(
        lambda_2(indd-1)*t_r(indd-1))+Vrec-Vo;
```

```
302     i_r(indd) = Cres(indd-1)*(A_r(indd-1)*lambda_1(indd-1)*exp(lambda_1(indd-1)*
            t_r(indd-1))+B_r(indd-1)*lambda_2(indd-1)*exp(lambda_2(indd-1)*t_r(indd
            -1)));
303 A_r(indd) = (i_r(indd)-Cres(indd)*lambda_2(indd)*(Vo-Vrec+Vds_1(indd)))/(Cres(
        indd)*(lambda_1(indd)-lambda_2(indd)));
304 B_r(indd) = (-i_r(indd)+Cres(indd)*lambda_1(indd)*(Vo-Vrec+Vds_1(indd)))/(Cres(
        indd)*(lambda_1(indd)-lambda_2(indd)));
305 t_r(indd) = real( (1/(1i*omega(indd))*log( (-(Vrec-Vo-Vds_1(indd+1)) + sqrt((Vrec
        -Vo-Vds_1(indd+1))^2-4*A_r(indd)*B_r(indd)))/(2*A_r(indd)))));
306 end
307 indd = length(Vds_2);
308 V_c(indd) = A_r(indd-1)*exp(lambda_1(indd-1)*t_r(indd-1))+B_r(indd-1)*exp(
        lambda_2(indd-1)*t_r(indd-1))+Vrec-Vo;
309 i_r(indd) = Cres(indd-1)*(A_r(indd-1)*lambda_1(indd-1)*exp(lambda_1(indd-1)*t_r(
        indd-1))+B_r(indd-1)*lambda_2(indd-1)*exp(lambda_2(indd-1)*t_r(indd-1)));
310
311 figure(1); plot([0 cumsum(t_r)],i_r) ;xlabel('Time [S]');ylabel('Resonant current
        [A]') ;grid minor;
312 figure(2); plot([0 cumsum(t_r)],[V_c' Vds_1']);xlabel('Time [S]');ylabel({'
        Capacitor Voltage [V]','Vds1'});grid minor;
```

Appendix C

MATLAB Code for Loss Computation - HSI

```
% This code is to calculate the HARD SWITCHING losses in single leg inverter
    MOSFET Blocking Voltage
Blocking = {'High','Low'};
Blocking = Blocking{1};
% Test type
TESTHS = {'ACTEST','DCTEST'};
TESTHS = TESTHS{1};
for adj=1:4;
% Select type of dead time optimizazion
    Adjust={'nothing_adjusted','adjust_positive_edge','adjust_negative_edge','
        adjust_both_edges'};
    Adjust=Adjust{adj};
% General information:
    fmod  = 50;   % Fundamental (electrical) freq. in Hz
    fs    = 20e3;   % Switching frequency in Hz
    Ts    = 1/fs;    % Switching time in sec
    Pmax  = 70;  % Maximum output power in W
    Popt  = 7;     % Optimal output power in W (3-phase)
    Vcus  = 230;  % RMS phase voltage (customer Voltage)
     % LL Max output voltage in V
    Vomax =0.8*(sqrt(2)*Vcus);
    switch Blocking
        case 'High'
        % LL Optimum output voltage in V
            Voopt = 0.2*Vomax;
            Vdc_vec=20:30:350;   % DC link voltage loop
        case 'Low'
```

```
26          % LL Optimum output voltage in V
27              Voopt = 0.1*Vomax;
28              Vdc_vec=25:25:125;   % DC link voltage loop
29      end
30      Vdcmax= sqrt(2)*Vcus;  % Max DC supply voltage in v
31      Vdcmin= 1/0.9*Voopt;     % Min DC supply voltage
32      % Max Peak of the load current in A
33      Iomax = 2*Pmax/(sqrt(3)*Vomax);
34      % Optimum Peak of the load current in A
35      Ioopt = 2*Popt/(sqrt(3)*Voopt);
36      Rgx    =18;           % External gate resistance
37      % Half of fundamental period
38      t      =(0:Ts:0.5/fmod);
39      % Number of switching cycles over fmod
40      intint=(fs/(2*fmod))+1;
41      % N5000 capacitance of V.ch=20e-12 F
42      Cn5    = 20e-12;
43      % Load cap = 310e-12F, Xavier's(157e-12)
44      Cly    = 157e-12;
45      Ld     = 10e-3;     % Load inductance;
46  % Switches Type:
47      switch Blocking
48          case 'High' % High blocking voltage MOSFET
49              MOSFET = {'IRFR812PbF'};
50          case 'Low' % Low blocking voltage MOSFET
51              MOSFET = {'FDD6N25'};
52      end
53  % Type of TEST
54      switch TESTHS
55          case 'ACTEST'
56              io= Ioopt*sin(2*pi*fmod*t);
57          case 'DCTEST'
58              io= Ioopt;
59      end
60      MOSFETloop
61  % Selection of The best five switches:
62  % best N switches
63      B=1:1;
64      selectbest
65  % MOSFET loop
66  % Power losses initialization:
67  PconM_mat=zeros(length(Vdc_vec),length(MOSFET));
68  PconD_mat= PconM_mat; PcondM_mat = PconM_mat;
```

```
69  PswM_mat = PconM_mat; PswD_mat    = PconM_mat;
70  Psw_mat  = PconM_mat; Pgt_mat     = PconM_mat;
71  Pt_mat   = PconM_mat; Pcap_mat    = PconM_mat;
72  % legend
73  legendStrings=cell(1,length(MOSFET));
74  % Starting Switch loop/ MOSFET loop:
75  for indM=1:length(MOSFET)
76      filename=[MOSFET{indM}];
77      load (['DeviceDefinitionFolder\xy' filename '.mat']);
78   % Interpolate Coss, Crss:
79      interpolCaps;
80      Name=[MOSFET{indM}];
81      Num = indM;
82      Qn5=zeros(length(Vdc_vec),1); Qly=zeros(length(Vdc_vec),1);
83      tfv1 = zeros(length(Vdc_vec),length(io)); tfv2 = tfv1;
84      trv1 = tfv1; trv2 = tfv1; Ton = tfv1; Toff = tfv1;
85      pin  = zeros(length(Vdc_vec),length(io)); pif = pin;
86  % Starting the voltage loop:
87      voltageloopHS
88  % Power Calculations for all MOSFET types:
89      PconM_mat(:,Num) = PconM;
90      PconD_mat(:,Num) = PconD;
91      PcondM_mat(:,Num)= PcondM;
92      Psw_mat(:,Num)   = Psw;
93      Pgt_mat(:,Num)   = Pgt;
94      Pt_mat(:,Num)    = Pt;
95      legendStrings{Num}=Name;
96  end
97  PconM =zeros(length(Vdc_vec),1); PconD=PconM;
98  PcondM=PconM;          Psw  =PconM;
99  Pgt   =PconM;          Pt   =PconM;
100 EoffMi_mat=PconM;          EoffMv_mat=PconM; EonMi_mat=PconM;
101 EonMv_mat=PconM;           Eonrr_mat=PconM;  Eoss_mat=PconM;
102 for indVdc=1:length(Vdc_vec)
103     Vdc=Vdc_vec(indVdc);
104    % Modulation index (peak to peak phase voltage divided by Vdc):
105    ma= (2/sqrt(3))*(Voopt/Vdc);
106    % Duty cycle:
107    D = 0.5*(1+ma*sin(2*pi*fmod*t)+ma/6*sin(3*2*pi*fmod*t));
108     losses;
109     switch TESTHS
110         case 'ACTEST'
111 % Power Calculations for one bridge leg for one MOSFET type
```

```
112             PconM(indVdc) = 2*fmod*trapz(t,EconM*fs);
113             PconD(indVdc) = 2*fmod*trapz(t,EconD*fs);
114             PcondM(indVdc)= PconM(indVdc)+PconD(indVdc);
115             Pqrr(indVdc)  = 2*fmod*trapz(t,Eonrr*fs)*0;
116             Pparas(indVdc)= 2*fmod*trapz(t,Einst*fs)*0;
117             Psw(indVdc)   = 2*fmod*trapz(t,Esw*fs)-Pqrr(indVdc)-Pparas(indVdc);
118             Pgt(indVdc)   = 2*fmod*trapz(t,Egt*fs);
119             Pt(indVdc)    = PcondM(indVdc)+Psw(indVdc)+Pgt(indVdc)+0*Pqrr(indVdc)
                    +0*Pparas(indVdc);
120
121         case 'DCTEST'
122 % Power Calculations for one bridge leg for one MOSFET type:
123             PcondM(indVdc)      = EcondM*fs;
124             EoffMi_mat(indVdc) = EoffMi;
125             EoffMv_mat(indVdc) = EoffMv;
126             EonMi_mat(indVdc)  = EonMi;
127             EonMv_mat(indVdc)  = EonMv;
128             Eonrr_mat(indVdc)  = Eonrr;
129             Eoss_mat(indVdc)   = Eoss;
130             Psw(indVdc)        = Esw*fs;
131             Pgt(indVdc)        = Egt*fs;
132             Pt(indVdc)         = PcondM(indVdc)+Psw(indVdc)+Pgt(indVdc);
133     end
134 end
135
136 is = Vdc*D.*(1-D)*Ts/Ld; % peak-peak rippile current
137 isrms= is/sqrt(12);              % RMS rippile current
138
139 % CONDUCTION LOSSES in MOSFET and DIODE:
140 % Energy Conduction losses in MOSFET
141 EconM = (Rds*io.^2+isrms.^2).*D*Ts;
142 % Energy Conduction losses in DIODE
143 EconD = (Rds*io.^2+isrms.^2).*(1-D)*Ts;
144 % Total MOSFET Conduction Energy Losses
145 EcondM= Rds*(io.^2+isrms.^2)*Ts;
146 % SWITCHING LOSSES in MOSFET and DIODE
147 % Turn on//Switching on MOSFET:
148 % Reise time calculation/current: nominal rise time
149 trn = (Rg+Rgx)*Ciss*log((Vdr-Vth)/(Vdr-Vgp));
150 % new current rise time
151 tr = (trn/In)*io;
152 % gate current Igon
153 Igo = (Vdr-Vgp)/(Rg+Rgx);
```

```
154 v_ds = 0:0.1*Vdc:Vdc;
155 Efv_mat = zeros(1,length(io)); Erv_mat = Efv_mat;
156 tf_vmat = Qgd_on(:,indVdc)*((1-Rds*io/Vdc)/Igo);
157 p_on  = v_ds'*io;
158 for n = 1:length(io);
159     Efv_mat(n) = trapz(tf_vmat(:,n),p_on(:,n));
160 end
161 % This includes the integration of load current and ds voltage over voltage fall
        time plus the losses during the current rise time
162 EonMv= Efv_mat; %sum(Efv_mat);
163 EonMi= 0.5*Vdc*io.*tr;
164 % The losses due to the reverse recovery charge
165 Eonrr= (Qrr/In)*io*Vdc;
166 % The losses due to the output capacitance
167 Eoss = Qoss(indVdc)*Vdc*ones(1,length(io));
168 % Losses of instruments and load:
169 % N5000 charge (just voltage channel of the load)
170 Qn5(indVdc)=Cn5*Vdc;
171 % load charge (Data measured on 21.01.2016)
172 Qly(indVdc)=Cly*Vdc;
173 % Turn off//Switching off MOSFET:
174 % Fall time calculation: nominal fall time
175 tfn = (Rg+Rgx)*Ciss*log(Vgp/Vth);
176 % new current fall time
177 tf = (tfn/In)*io;
178 % gate currentIgoff
179 Igof= Vgp/(Rg+Rgx);
180 tr_vmat= Qgd_off(:,indVdc)*(1-Rds*io/Vdc)/Igof;
181 p_off  = v_ds'*io;
182 for n = 1:length(io)
183     Erv_mat(n) = trapz(tr_vmat(:,n),p_off(:,n));
184 end
185 % Energy losses in turn off state of MOSFET
186 EoffMv= Erv_mat;
187 EoffMi= 0.5*Vdc*io.*tf;
188 % Energy losses in turn off state of DIODE
189 EoffD= zeros(1,length(io));
190
191 switch Adjust
192 % Nothing adjusted
193     case 'nothing_adjusted'
194         % losses due to the channels of N5000 and load capacitance
195         Einst=(Qn5(indVdc)+Qly(indVdc)+Qoss(indVdc))*Vdc*ones(1,length(io));
```

```
196         EoffM=(EoffMi+EoffMv+EoffD)+Einst;
197         % Energy losses in turn on state in MOSFET
198         EonM=(EonMi+EonMv+Eonrr+Eoss);
199 % Positive edge djusted (Reduce the reverse charge losses)
200     case 'adjust_positive_edge'
201         % losses due to the channels of N5000 and load capacitance
202         Einst=(Qn5(indVdc)+Qly(indVdc)+Qoss(indVdc))*Vdc*ones(1,length(io));
203         EoffM=(EoffMi+EoffMv+EoffD)+Einst;
204         % Reverse recovery losses is zero
205         EonM=(EonMi+EonMv+Eoss)+0*Eonrr;
206 % Negative edge djusted (Reduce the output capacitance losses)
207     case 'adjust_negative_edge'
208         % losses due to the channels of N5000 and load capacitance
209         Einst=((Qn5(indVdc)+Qly(indVdc))+Qoss(indVdc))*Vdc*ones(1,length(io));
210         EoffM= (io.*tf).^2/(4*6*(Cly+Cn5+Coss(indVdc)));
211         % Energy losses in turn on state in MOSFET, part of Capacitive losses is
                zero
212         EonM=(EonMi+EonMv+Eonrr)+Einst+0*Eoss;
213 % Adusting both negative and positive edge
214     case 'adjust_both_edges'
215         % with snubber capacitor:
216         % losses due to the channels of N5000 and load capacitance
217         Einst=(Qn5(indVdc)+Qly(indVdc)+Qoss(indVdc))*Vdc*ones(1,length(io));
218         % turn off losses with snubber
219         EoffM= (io.*tf).^2/(4*6*(Cly+Cn5+Coss(indVdc)));
220         % Energy losses in turn on state in MOSFET (ZVS)
221         EonM=EonMi+EonMv+Einst+0*(Eonrr+Eoss);
222 end
223 % Sum up switching losses}
224 Total Switching losses in MOSFET
225 Esw= (EonM+EoffM);
226
227 %Energy losses in gate drive circuit:
228 Egt= 2*Qgt*(Vdr/Vqg)*Vdr*ones(1,length(io));
229
230 % Total Energy losses in MOSFET
231 EtM = EconM+Esw;
232 % Total Energy losses in DIODE
233 EtD = EconD;
234 % Total Energy losses in MOSFET and DIODE with driving energy
235 Et = EcondM+Esw+Egt;
236 %% Selection of The best five switches:}
237 A=Pt_mat(length(Vdc_vec),:);
```

```
238 Value_vec=zeros(1,length(B));
239 Index_vec=zeros(1,length(B));
240 MOSFETNum_vec=zeros(1,length(B));
241 Nameb_vec=cell(1,length(B));
242 best_t      =zeros(length(Vdc_vec),length(B));
243 best_gt     =zeros(length(Vdc_vec),length(B));
244 best_sw     =zeros(length(Vdc_vec),length(B));
245 best_conM   =zeros(length(Vdc_vec),length(B));
246 best_conD   =zeros(length(Vdc_vec),length(B));
247 best_condM  =zeros(length(Vdc_vec),length(B));
248 for indmin=1:length(B)
249     [M,I] = min(A);
250     Value_vec(indmin)=M;
251     Index_vec(indmin)=I;
252     best_t(:,indmin)     = Pt_mat(:,Index_vec(indmin));
253     A(I)=[NaN];
254     MOSFETNum_vec(indmin)=Index_vec(indmin);
255     Nameb_vec{indmin}=[MOSFET{MOSFETNum_vec(indmin)}];
256 end
257 for indbt=1:length(Index_vec)
258     best_t(:,indbt)     = Pt_mat(:,Index_vec(indbt));
259     best_gt(:,indbt)    = Pgt_mat(:,Index_vec(indbt));
260     best_sw(:,indbt)    = Psw_mat(:,Index_vec(indbt));
261     best_conM(:,indbt)  = PconM_mat(:,Index_vec(indbt));
262     best_conD(:,indbt)  = PconD_mat(:,Index_vec(indbt));
263     best_condM(:,indbt)= PcondM_mat(:,Index_vec(indbt));
264 end
```

Appendix D

MATLAB Code for Loss Computation - ARCPI

```
% Select type of load current
TESTSS  = {'ACTEST','DCTEST'};
TESTSS  = TESTSS{1};
% Blocking voltage
Voltage = {'Low','High'};
Voltage = Voltage{2};
% Auxiliary switches
AuxSWITCHA = {'MOSFET','IGBT'};
AuxSWITCHA = AuxSWITCHA{1};
% Number of Aux. Pulses
PulseNumber= {'1pulses','2pulses'};
PulseNumber= PulseNumber{1};
% Bosst current
BoostCurrent= {'Constant','function_of(io)'};
BoostCurrent= BoostCurrent{2};
%% General information - See appendix C - General information
% number of division per one swit. cycle;
x       = 25;
Cdiff = 6e-12;  % diffirantial cap of diff.Probs
Cv_g  = 1e-12;  % capacitance to ground of Diff. Probs
Cl_r  = 6.3e-12; % parasitic caps of Lr
% lyout capacitance (drain to ground capacitance) of A1;
Cly   = 3.5e-12;
Croot = 2e-12;  % root capcitance (common source to ground)
% Coupling capacitance from gate driver(Measured at low
%voltage (18V) from source to ground)
C_coup= 10e-12;
```

```
% Main and Auxiliary Switches Data:
switch Voltage
    case 'Low'
        MainSWITCH = {'FDD6N25'};
    case 'High'
        MainSWITCH = {'M60R19C6'};
end
switch AuxSWITCHA
    case 'MOSFET'
        AuxSWITCH = {'FDD6N25'};
    case 'IGBT'
        AuxSWITCH = {'D15N60RF'};
end
% For loop for choosing SWITCHES combination
% Vdcmin is the min DC voltage where D=1;
switch TESTSS
    % CASE ACTEST
    case 'ACTEST'
        io_vec=Ioopt*sin(2*pi*fmod*t);     % AC current
        intint = length(t);                % 0.5*(fs/fmod)
        stp    = 1/x;%1/(length(t)-1);
        % Modulation index (peak to peak phase voltage divided by Vdc):
        ma= (2/sqrt(3))*(Voopt/Vdc);
        % Duty cycle:
        D = 0.5*(1+ma*sin(2*pi*fmod*t)+ma/6*sin(3*2*pi*fmod*t));
        switch BoostCurrent
            % Boost Current is constant
            case 'Constant'
                Ib_vec =3.5*ones(1,length(t))*Ioopt;

            case 'function_of(io)'
                % Boost Current is function of load current
                Ib_vec =3.5*io_vec;
        end
        % CASE DCTEST
    case 'DCTEST'
        io_vec = Ioopt*ones(1,length(t));  % DC current
        intint = length(t);                % 0.5*(fs/fmod)
        stp    = 1/x;
        % Modulation index (peak to peak phase voltage divided by Vdc):
        ma= (2/sqrt(3))*(Voopt/Vdc);
        % Duty cycle (constant duty cycle):
        D = 0.2;
```

```
71          Ib_vec =3.5*io_vec;
72          % END of this cas
73  end
74
75  % Starting Switch loop/ MOSFET loop:
76  mainloop;
77
78  % Selection of The best five switches:
79  Bb=1:5;       % best N switches
80  selectbestsoft;
81
82   % Main switches loop
83  for indM=1:length(MainSWITCH);
84       filenameM=[MainSWITCH{indM}];
85       filename = filenameM;
86      load (['DeviceDefinitionFolderSoft\xy' filename '.mat']);
87
88  %Interpolate Coss, Crss:
89       interpolcaps;
90       Sm=load (['DeviceDefinitionFolderSoft\xy' filename '.mat']);
91       Sm.Coss=Coss;
92       Sm.Chos=Chos;
93       Sm.Crss=Crss;
94       Sm.Qoss=Qoss;
95       Sm.Qhos=Qhos;
96       Sm.Qrss=Qrss;
97
98       Vfm    = Sm.Vf;
99       Rfm    = Sm.Rf;
100      Rdsm   = Sm.Rds;
101      Cm     = Sm.Coss;
102      Ch     = Sm.Chos;
103      Qom    = Sm.Qoss;
104      Qgtm   = Sm.Qgt;
105      Vqgm   = Sm.Vqg;
106      Vdrmm  = Sm.Vdrm;
107      Vdrmi  = Sm.Vdri;
108      Vceom  = Sm.Vce;
109      Rcem   = Sm.Rce;
110      Rfi    = Sm.Rfi;
111      Vfi    = Sm.Vfi;
112      Qrm    = Sm.Qr;
113      Inm    = Sm.If;
```

```
114
115 %Auxiliary switch loop
116     auxloop;
117 end
118 %% auxloop
119 % Initialization of power losses
120 Pt_cmp=zeros(length(Vdc_vec),length(MainSWITCH)*length(AuxSWITCH));
121 PcondM_cmp=Pt_cmp; PcondA_cmp=Pt_cmp; PL_cmp=Pt_cmp;
122 Pgt_cmp=Pt_cmp; Pswn_cmp=Pt_cmp; Prra_cmp=Pt_cmp;
123 % Name of the combinations
124 legendStrings=cell(1,length(MainSWITCH)*length(AuxSWITCH));
125 for indA=1:length(AuxSWITCH);
126     filenameA=[AuxSWITCH{indA}];
127     filename = filenameA;
128     Name  = [MainSWITCH{indM} '\_' AuxSWITCH{indA}];
129     Num   = length(MainSWITCH)*(indM-1)+indA;
130     switch AuxSWITCHA
131         case 'MOSFET'
132             load (['DeviceDefinitionFolderSoft\xy' filename '.mat']);
133   % Interpolate Coss, Crss:}
134             interpolcaps;
135             Sa = load (['DeviceDefinitionFolderSoft\xy' filename '.mat']);
136             Sa.Coss=Coss;
137             Sa.Chos=Chos;
138             Sa.Crss=Crss;
139             Sa.Qoss=Qoss;
140             Sa.Qhos=Qhoss;
141             Sa.Qrss=Qrss;
142
143             Vfa   = Sa.Vf;
144             Rfa   = Sa.Rf;
145             Rdsa  = Sa.Rds;
146             Ca    = Sa.Coss;
147             Qoa   = Sa.Qhos; % at half of DC link voltage
148             Qoaf  = Sa.Qoss; % at full of DC link voltage
149             Qgta  = Sa.Qgt;
150             Vqga  = Sa.Vqg;
151             Vdram = Sa.Vdrm;
152             Vdrai = Sa.Vdri;
153             Vceoa = Sa.Vce;
154             Rcea  = Sa.Rce;
155             Qra   = Sa.Qr;
156             Ina   = Sa.If;
```

```
157
158 % Loss computations for each Vdc
159             switch PulseNumber
160                 case '1pulses'
161                     voltageloopsoft_n;
162                 case '2pulses'
163                     voltageloopsoft;
164             end
165         case 'IGBT'
166             load (['DeviceDefinitionFolderSoft\xy' filename '.mat']);
167             Sa = load (['DeviceDefinitionFolderSoft\xy' filename '.mat']);
168             Sa.Coss=Coss;
169             Sa.Chos=Chos;
170             Sa.Crss=Crss;
171             Sa.Qoss=Qoss;
172             Sa.Qhos=Qhoss;
173             Sa.Qrss=Qrss;
174
175             Vfa   = Sa.Vf;
176             Rfa   = Sa.Rf;
177             Rdsa  = Sa.Rds;
178             Ca    = Sa.Coss;
179             Qoa   = Sa.Qhos; % at half of DC link voltage
180             Qoaf  = Sa.Qoss; % at full of DC link voltage
181             Qgta  = Sa.Qgt;
182             Vqga  = Sa.Vqg;
183             Vdram = Sa.Vdrm;
184             Vdrai = Sa.Vdri;
185             Vceoa = Sa.Vce;
186             Rcea  = Sa.Rce;
187             Qra   = Sa.Qr;
188             Ina   = Sa.If;
189
190 % Loss computations for each Vdc
191             switch PulseNumber
192                 case '1pulses'
193                     voltageloopsoft_n;
194                 case '2pulses'
195                     voltageloopsoft;
196             end
197     end
198 % For loop for changing DC voltage
199     PcondM_cmp(:,Num) = PcondM;
```

```
200     PcondA_cmp(:,Num) = PcondA;
201     Pswn_cmp(:,Num)   = Psw;
202     % Prra_cmp(:,Num)    = Prra;
203     PL_cmp(:,Num)       = PL;
204     Pgt_cmp(:,Num)      = Pgt;
205     Pt_cmp(:,Num)       = Pt;
206     legendStrings{Num}=Name;
207 end
208
209 %% voltageloopsoft
210 % Initializations
211 PcondM = zeros(size(Vdc_vec))';
212 PAc = PcondM; Psw = PcondM;
213 Pgt = PcondM; PL = PcondM;
214 PcondA = PcondM; Pt = PcondM;
215 Il1 = zeros(x+1,length(t)); Il2 = Il1; Il3 = Il1; Il4 = Il1; Il5 = Il1;
216 Il6 = Il1; Il7 = Il1; Il8 = Il1; Il9 = Il1; Il10 = Il1;
217 for indVdc=1:length(Vdc_vec)
218     Vdc=Vdc_vec(indVdc);
219     %Ib=Ib_vec(indVdc);
220     Ib = Ib_vec;
221
222 % Current Modes:}
223     % Mode 1 [t0-t1], lower Main diode conducts: KVL -> Rl,Rdsa1,Rf2a,Ronm;
224     % Io*Rdsa<Vfa -> Rt1=Rl+2*Rdsa+Rfm; Rt1=Rl+2*(Rdsa+Rcea)+Rfm;
225     Rt1=Rl+2*(Rdsa+Rcea)+(Rdsm+Rcem); % According to the assumbtion
226     % VL+VR=Vdc*0.5-Vfa+Vfm+io*Rfm; -> Vt1=Vdc*0.5+Vfm+io*Rfm;
227     % Vt1=Vdc*0.5+Vfm+io*Rfm;
228     Vt1=0.5*Vdc+Vceom+io_vec*(Rdsm+Rcem);
229     t1 = -L/Rt1*log(1-Rt1*(io_vec./Vt1));
230     ta  = (0:stp:1)'*t1;
231     for indsw =1:length(io_vec);
232         Il1(:,indsw) = (Vt1(indsw)/Rt1)*(1-exp(-ta(:,indsw)*Rt1/L));
233         %Il1 = ones(1,intint)'*(Vt1/Rt1).*(1-exp(-ta*Rt1/L));
234     end
235     % Mode 2 [t1,t2], lower MOSFET conducts: KVL; -> Rl,Rdsa,Rdsa,Rdsm;
236     % ->Rt1=Rl+2*Rdsa+Rdsm;
237     Rt2=Rl+2*(Rdsa+Rcea)+Rdsm+Rcem; % According to assumbtion
238     % VL+VR=Vdc*0.5-Vfa+io*Rdsm; -> Vt2=Vdc*0.5+io*Rdsm;
239     Vt2=Vdc*0.5-Vceoa+io_vec*(Rdsm+Rcem);
240     t2 = -L/Rt2*log((Ib-Vt2/Rt2)./(io_vec-Vt2/Rt2));
241     tb  = (0:stp:1)'*t2;
242     for indsw =1:length(io_vec);
```

```
243         Il2(:,indsw) = (Vt2(indsw)/Rt2)+(io_vec(indsw)-Vt2(indsw)/Rt2).*...
244             exp(-tb(:,indsw)*Rt2/L);
245     end
246     % Mode 3 [t2-t3], Resonance mode:
247     t3  = zeros(1,length(io_vec));
248     Il3 = zeros(1/stp+1,length(io_vec));
249     tc  = Il3;
250     for indio=1:length(io_vec)
251         io = io_vec(indio);
252         Ib = Ib_vec(indio);
253         mode3new;
254         t3tt         = [0 cumsum(t3t)];
255         t3(:,indio) = max(t3tt);
256         tc(:,indio) = [0 cumsum(t3t)]';
257         Il3(:,indio)= i3t';
258     end
259     % Mode 4 [t3-t4], upper diode conducts: Rt4 = Rl+2*(Rdsa+Rcea)-Rfm;
260     Rt4 = Rl+2*(Rdsa+Rcea)+(Rdsm+Rcem); % According to the assumbtion
261     % Vt4 = (-Vdc*0.5--Vfm-io*Rfm);
262     Vt4 = (-Vdc*0.5-Vceom-io_vec*Rdsm);
263     Ib4 = Il3(end,:);
264     t4 = -L/Rt4*log((io_vec-Vt4/Rt4)./(Ib4-Vt4/Rt4));
265     td  = (0:stp:1)'*t4;
266     for indsw =1:length(io_vec);
267         Il4(:,indsw) = (Vt4(indsw)/Rt4)+(Ib4(indsw)-Vt4(indsw)/Rt4).*...
268             exp(-td(:,indsw)*Rt4/L);
269     end
270     % Mode 5 [t4-t5], upper MOSFET conducts:
271     Rt5 = Rl+2*(Rdsa+Rcea)+(Rdsm+Rcem);
272     Vt5 = -Vdc*0.5+Vceom-io_vec*(Rdsm+Rcem);
273     Ib5 = Il4(end,:);
274     t5 = -L/Rt5*log((-Vt5/Rt5)./(-Vt5/Rt5+Ib5));
275     te  = (0:stp:1)'*t5;
276     for indsw =1:length(io_vec);
277         Il5(:,indsw) = (Vt5(indsw)/Rt5)+(Ib5(indsw)-Vt5(indsw)/Rt5).*...
278             exp(-te(:,indsw)*Rt5/L);
279     end
280     % Mode 7 [t6-t7], current decrease:
281     Rt7 = Rl+2*(Rdsa+Rcea)+(Rdsm+Rcem);
282     Vt7 = -Vdc*0.5+Vceom-(Rdsm+Rcem)*io_vec;
283     t7 = -L/Rt7*log(1+Ib_vec*Rt7./Vt7);
284     tg  = (0:stp:1)'*t7;
285     for indsw =1:length(io_vec);
```

```
286         Il7(:,indsw) = (Vt7(indsw)/Rt7).*(1-exp(-tg(:,indsw)*Rt7/L));
287     end
288     % Mode 8 [t7-t8], Resonance mode:
289     t8  = zeros(1,length(io_vec));
290     Il8 = zeros(1/stp+1,length(io_vec));
291     th  = Il8;
292     for indio=1:length(io_vec)
293         io = io_vec(indio);
294         Ib = Ib_vec(indio);
295         if 1
296             mode8new;
297             t8tt          = [0 cumsum(t8t)];
298             t8(:,indio)   = max(t8tt);
299             th(:,indio) = [0 cumsum(t8t)]';
300             Il8(:,indio) = i8t';
301         end
302     end
303     % Mode 9 [t8-t9], current decrease to zero: Rt9 =
304     % Rl+2*(Rdsa+Rcea)+Rdsm;
305     Rt9 = Rl+2*(Rdsa+Rcea)+Rfm;
306     % Vt9 = Vdc*0.5+Vfm+Rfm*io;
307     Vt9 = Vdc*0.5+Vceom+io_vec*Rdsm;
308     Ib9 = Il8(end,:);
309     t9 = real(-L/Rt9*log((-Vt9/Rt9)./(Ib9-Vt9/Rt9)));
310     ti  = (0:stp:1)'*t9;
311     for indsw =1:length(io_vec);
312         Il9(:,indsw) = (Vt9(indsw)/Rt9)+(Ib9(indsw)-Vt9(indsw)/Rt9).*...
313             exp(-ti(:,indsw)*Rt9/L);
314     end
315     % Mode 6 [t5-t6], Upper MOSFET conducts:
316     t6 = Ts*D-(t4+t5);
317     tf=(0:stp:1)'*t6;
318     Il6 = 0*tf;
319     % Mode 10 [t9-t0], Lower diode conducts: Conduction time for all
320     % switches:
321     Tm1 = D.*Ts;
322     Tm2 = (1-D).*Ts-(t1+t2+t3);
323     Ta1 = t1+t2+t3+t4+t5;
324     Ta2 = t7+t8+t9;
325     tx = (0:stp:1)'*Tm2;
326     Il0= 0*tx;
327
328 % the next computations are only for Auxiliary Switches:
```

```
% Body Diode current in each mode: Body diode A2
    Id1 = (Vceoa+(Rcea+Rdsa)*Il1-Vfa)/(Rdsa+Rfa+Rcea);
    Id2 = (Vceoa+(Rcea+Rdsa)*Il2-Vfa)/(Rdsa+Rfa+Rcea);
    Id3 = (Vceoa+(Rcea+Rdsa)*Il3-Vfa)/(Rdsa+Rfa+Rcea);
    Id4 = (Vceoa+(Rcea+Rdsa)*Il4-Vfa)/(Rdsa+Rfa+Rcea);
    Id5 = (Vceoa+(Rcea+Rdsa)*Il5-Vfa)/(Rdsa+Rfa+Rcea);
    % Body diode A1
    Id7 = (Vceoa+(Rcea+Rdsa)*Il7+Vfa)/(Rdsa+Rfa+Rcea);
    Id8 = (Vceoa+(Rcea+Rdsa)*Il8+Vfa)/(Rdsa+Rfa+Rcea);
    Id9 = (Vceoa+(Rcea+Rdsa)*Il9+Vfa)/(Rdsa+Rfa+Rcea);
    % Channel current in each mode: switch A2
    Ich1 = (Vfa+Il1*Rfa)/(Rdsa+Rfa+Rcea);
    Ich2 = (Vfa+Il2*Rfa)/(Rdsa+Rfa+Rcea);
    Ich3 = (Vfa+Il3*Rfa)/(Rdsa+Rfa+Rcea);
    Ich4 = (Vfa+Il4*Rfa)/(Rdsa+Rfa+Rcea);
    Ich5 = (Vfa+Il5*Rfa)/(Rdsa+Rfa+Rcea);
    % switch A1
    Ich7 = (-Vfa+Il7*Rfa)/(Rdsa+Rfa+Rcea);
    Ich8 = (-Vfa+Il8*Rfa)/(Rdsa+Rfa+Rcea);
    Ich9 = (-Vfa+Il9*Rfa)/(Rdsa+Rfa+Rcea);
% Check the channel and the diode current-Auxiliary switches:
    inds = find(Id1<0);
    Ich1(inds)=Il1(inds);
    Id1(inds)=0;
    inds = find(Id2<0);
    Ich2(inds)=Il2(inds);
    Id2(inds)=0;
    inds = find(Id3<0);
    Ich3(inds)=Il3(inds);
    Id3(inds)=0;
    inds = find(Id4<0);
    Ich4(inds)=Il4(inds);
    Id4(inds)=0;
    inds = find(Id5<0);
    Ich5(inds)=Il5(inds);
    Id5(inds)=0;
    inds = find(Id7>0);
    Ich7(inds)=Il7(inds);
    Id7(inds)=0;
    inds = find(Id8>0);
    Ich8(inds)=Il8(inds);
    Id8(inds)=0;
    inds = find(Id9>0);
```

```
372      Ich9(inds)=Il9(inds);
373      Id9(inds)=0;
374 % The next computations are only for Main Switches:}
375 % Body Diode current in each mode: Body diode A1
376  IdM1 = (Rdsm*(Il1-repmat(io_vec,x+1,1))-Vfm)/(Rdsm+Rfm);
377  IdM2 = (Rdsm*(Il2-repmat(io_vec,x+1,1))-Vfm)/(Rdsm+Rfm);
378  IdM3 = 0*(Rdsm*(Il3-repmat(io_vec,x+1,1))-Vfm)/(Rdsm+Rfm);
379  IdM4 = (Rdsm*(Il4-repmat(io_vec,x+1,1))-Vfm)/(Rdsm+Rfm);
380  IdM5 = (Rdsm*(Il5-repmat(io_vec,x+1,1))-Vfm)/(Rdsm+Rfm);
381 % Body diode A1
382  IdM7 = (Rdsm*(Il7+repmat(io_vec,x+1,1))+Vfm)/(Rdsm+Rfm);
383  IdM8 = 0*(Rdsm*(Il8+repmat(io_vec,x+1,1))+Vfm)/(Rdsm+Rfm);
384  IdM9 = (Rdsm*(Il9+repmat(io_vec,x+1,1))+Vfm)/(Rdsm+Rfm);
385  % Channel current in each mode: switch M2
386  IchM1 = (Vfm+(Il1-repmat(io_vec,x+1,1))*Rfm)/(Rdsm+Rfm);
387  IchM2 = (Vfm+(Il2-repmat(io_vec,x+1,1))*Rfm)/(Rdsm+Rfm);
388  IchM3 = 0*(Vfm+(Il3-repmat(io_vec,x+1,1))*Rfm)/(Rdsm+Rfm);
389  IchM4 = (Vfm+(Il4-repmat(io_vec,x+1,1))*Rfm)/(Rdsm+Rfm);
390  IchM5 = (Vfm+(Il5-repmat(io_vec,x+1,1))*Rfm)/(Rdsm+Rfm);
391 % switch A1
392  IchM7 = (-Vfm+(Il7+repmat(io_vec,x+1,1))*Rfm)/(Rdsm+Rfm);
393  IchM8 = 0*(-Vfm+(Il8+repmat(io_vec,x+1,1))*Rfm)/(Rdsm+Rfm);
394  IchM9 = (-Vfm+(Il9+repmat(io_vec,x+1,1))*Rfm)/(Rdsm+Rfm);
395      Iout   = repmat(io_vec,x+1,1);
396      IBoost = repmat(Ib_vec,x+1,1);
397 % Check the channel and the diode current-Main switches:
398      inds = find(IdM1<0);
399      IchM1(inds)=Il1(inds)-Iout(inds);
400      IdM1(inds)=0;
401      inds = find(IdM2<Iout);
402      IchM2(inds)=Il2(inds)-Iout(inds);
403      IdM2(inds)=0;
404      inds = find(IdM3<0);
405      IchM3(inds)=0*(Il3(inds)-Iout(inds));
406      IdM3(inds)=0;
407      inds = find(IdM4<0);
408      IchM4(inds)=Il4(inds)-Iout(inds);
409      IdM4(inds)=0;
410      inds = find(IdM5<0);
411      IchM5(inds)=Il5(inds)-Iout(inds);
412      IdM5(inds)=0;
413      inds = find(IdM7>-Iout);
414      IchM7(inds)=Il7(inds)+Iout(inds);
```

```
415     IdM7(inds)=0;
416     inds = find(IdM8>0);
417     IchM8(inds)=0*(I18(inds)+Iout(inds));
418     IdM8(inds)=0;
419     inds = find(IdM9>0);
420     IchM9(inds)=I19(inds)+Iout(inds);
421     IdM9(inds)=0;
422 %% LOSS CALCULATION:
423 %Positive inductor current io*Rdsa\ensuremath{<}Vfa -\ensuremath{>} Diode will
        not conducts ... no Vfa*Il1 loosses The conduction energy is averaged over
        one switching cycle
424 %(stp) then it is averaged over fund. periode (t1,t3.....)
425 E1 = ((Rl+(Rdsa+Rcea))*trapz(Il1.^2)+Vceoa*trapz(Il1)+(Rdsa+Rcea)*trapz(Ich1.^2)
        +(Vfa*trapz(Id1)+Rfa*trapz(Id1.^2))+Vceoa*trapz(Ich1)+(Rdsm+Rcem)*trapz((
        IchM1).^2)+(Vceom)*trapz(IchM1)+(Rfm)*trapz((IdM1).^2)+(Vfm)*trapz(IdM1))*stp
        .*t1;
426 E2 = ((Rl+(Rdsa+Rcea))*trapz(Il2.^2)+Vceoa*trapz(Il2)+(Rdsa+Rcea)*trapz(Ich2.^2)
        +(Vfa*trapz(Id2)+Rfa*trapz(Id2.^2))+Vceoa*trapz(Ich2)+(Rdsm+Rcem)*trapz((
        IchM2).^2)+(Vceom)*trapz(IchM2)+(Rfm)*trapz((IdM2).^2)+(Vfm)*trapz(IdM2))*stp
        .*t2;
427 E3 = ((Rl+(Rdsa+Rcea))*trapz(Il3.^2)+Vceoa*trapz(Il3)+(Rdsa+Rcea)*trapz(Ich3.^2)
        +(Vfa*trapz(Id3)+Rfa*trapz(Id3.^2))+Vceoa*trapz(Ich3))*stp.*t3;
428 E4 = ((Rl+(Rdsa+Rcea))*trapz(Il4.^2)+Vceoa*trapz(Il4)+(Rdsa+Rcea)*trapz(Ich4.^2)
        +(Vfa*trapz(Id4)+Rfa*trapz(Id4.^2))+Vceoa*trapz(Ich4)+(Rdsm+Rcem)*trapz((
        IchM4).^2)+(Vceom)*trapz(IchM4)+(Vceom)*trapz(IchM4)+(Rfm)*trapz((IdM4).^2)+(
        Vfm)*trapz(IdM4))*stp.*t4;
429 E5 = ((Rl+(Rdsa+Rcea))*trapz(Il5.^2)+Vceoa*trapz(Il5)+(Rdsa+Rcea)*trapz(Ich5.^2)
        +(Vfa*trapz(Id5)+Rfa*trapz(Id5.^2))+Vceoa*trapz(Ich5)+(Rdsm+Rcem)*trapz((
        IchM5).^2)+(Vceom)*trapz(IchM5)+(Vceom)*trapz(IchM5)+(Rfm)*trapz((IdM5).^2)+(
        Vfm)*trapz(IdM5))*stp.*t5;
430 % Negative inductor current
431 E7 = ((Rl+(Rdsa+Rcea))*trapz(Il7.^2)-Vceoa*trapz(Il7)+(Rdsa+Rcea)*trapz(Ich7.^2)
        +(-Vfa*trapz(Id7)+Rfa*trapz(Id7.^2))-Vceoa*trapz(Ich7)+(Rdsm+Rcem)*trapz((
        IchM7).^2)+(Vceom)*trapz(IchM7)+(Vceom)*trapz(IchM7)+(Rfm)*trapz((IdM7).^2)+(
        Vfm)*trapz(IdM7))*stp.*t7;
432 E8 = ((Rl+(Rdsa+Rcea))*trapz(Il8.^2)-Vceoa*trapz(Il8)+(Rdsa+Rcea)*trapz(Ich8.^2)
        +(-Vfa*trapz(Id8)+Rfa*trapz(Id8.^2))-Vceoa*trapz(Ich8))*stp.*t8;
433 E9 = ((Rl+(Rdsa+Rcea))*trapz(Il9.^2)-Vceoa*trapz(Il9)+(Rdsa+Rcea)*trapz(Ich2.^2)
        +(-Vfa*trapz(Id9)+Rfa*trapz(Id9.^2))-Vceoa*trapz(Ich9)+(Rdsm+Rcem)*trapz((
        IchM9).^2)+(Vceom)*trapz(IchM9)+(Vceom)*trapz(IchM9)+(Rfm)*trapz((IdM9).^2)+(
        Vfm)*trapz(IdM9))*stp.*t9;
434 % Inductor losses
```

```
435 EL =Rl*(trapz(Il1.^2).*t1+trapz(Il2.^2).*t2+trapz(Il3.^2).*t3+trapz(Il4.^2).*t4+
        trapz(Il5.^2).*t5+trapz(Il7.^2).*t7+trapz(Il8.^2).*t8+trapz(Il9.^2).*t9)*stp;
    % Looses in Auxiliary Cirtcuit (Aux. switches and inductor):
436 EAc = E1+E2+E3+E4+E5+E7+E8+E9;
437 % Conduction losses in Auxiliary switches:
438 EcondA = (((Rdsa+Rcea)*trapz(Il1.^2)+Vceoa*trapz(Il1)+Vfa*trapz(Id1)+Rfa*trapz(
        Id1.^2)+(Rdsa+Rcea)*trapz(Ich1.^2)+Vceoa*trapz(Ich1)).*t1+((Rdsa+Rcea)*trapz(
        Il2.^2)+Vceoa*trapz(Il2)+Vfa*trapz(Id2)+Rfa*trapz(Id2.^2)+(Rdsa+Rcea)*trapz(
        Ich2.^2)+Vceoa*trapz(Ich2)).*t2+((Rdsa+Rcea)*trapz(Il3.^2)+Vceoa*trapz(Il3)+
        Vfa*trapz(Id3)+Rfa*trapz(Id3.^2)+(Rdsa+Rcea)*trapz(Ich3.^2)+Vceoa*trapz(Ich3)
        ).*t3+((Rdsa+Rcea)*trapz(Il4.^2)+Vceoa*trapz(Il4)+Vfa*trapz(Id4)+Rfa*trapz(
        Id4.^2)+(Rdsa+Rcea)*trapz(Ich4.^2)+Vceoa*trapz(Ich4)).*t4+((Rdsa+Rcea)*trapz(
        Il5.^2)+Vceoa*trapz(Il5)+Vfa*trapz(Id5)+Rfa*trapz(Id5.^2)+(Rdsa+Rcea)*trapz(
        Ich5.^2)+Vceoa*trapz(Ich5)).*t5+((Rdsa+Rcea)*trapz(Il7.^2)-Vceoa*trapz(Il7)-
        Vfa*trapz(Id7)+Rfa*trapz(Id7.^2)+(Rdsa+Rcea)*trapz(Ich7.^2)-Vceoa*trapz(Ich7)
        ).*t7+((Rdsa+Rcea)*trapz(Il8.^2)+Vceoa*trapz(Il8)-Vfa*trapz(Id8)+Rfa*trapz(
        Id8.^2)+(Rdsa+Rcea)*trapz(Ich8.^2)-Vceoa*trapz(Ich8)).*t8+((Rdsa+Rcea)*trapz(
        Il1.^2)-Vceoa*trapz(Il9)-Vfa*trapz(Id9)+Rfa*trapz(Id9.^2)+(Rdsa+Rcea)*trapz(
        Ich9.^2)-Vceoa*trapz(Ich9)).*t9)*stp;
439 % Conduction Losses for Main switches:
440 E6 = (Vceom*io_vec+(Rdsm+Rcem)*io_vec.^2).*Tm1;
441 % E10= (Vfi*io+(Rdsm+Rfi)*io.^2).*Tm2;
442 E10= (Vceom*io_vec+(Rdsm+Rcem)*io_vec.^2).*Tm2;
443 EcondM = E6+E10;
444 % Switching losses in Auxiliary switches:
445 % at turn on both A1 and A2 are turned on at the same time "the output
        capacitance of A1 is discharged while the output capacitance of A2 is shorted
         by the body diode, the opposite for negative current slope". energy lost is
        given by (2 aux sw),
446     VovA2  = 1.2*Vdc;
447     VovA1 = 1.7*Vdc;
448
449     switch AuxSWITCHA
450         case 'MOSFET'
451             % Aux 1 Energy
452             Ecap_ext  = ((Cdiff+5*Cv_g+Cl_r/2+Cly+Croot+2*C_coup)*VovA2^2/2)+((
                    Cdiff+  Cv_g+Cl_r/2+Cly)*VovA1^2/2);
453             compuener = cumtrapz(xos_data,xos_data.*yos_data*1e-12);
454             E_interp = interp1(xos_data,compuener,VovA2,'spline')+interp1(
                    xos_data,compuener,VovA1,'spline');
455             Ecap = (E_interp+Ecap_ext)*ones(1,length(t));
456         case 'IGBT'
```

```
457                 Ecap_ext  = ((Cv_g+Cl_r/2+Cdiff+Cly+C_coup)*VovA2^2/2)+((Cdiff+2*Cv_g
                        +Croot)*VovA1^2/2);
458                 compuener = cumtrapz(xos_data,xos_data.*yos_data*1e-12);
459                 E_interp = interp1(xos_data,compuener,VovA2,'spline')+interp1(
                        xos_data,compuener,VovA1,'spline');
460                 Ecap = (E_interp+Ecap_ext)*ones(1,length(t));
461         end
462         % A1 is turned off after the reverse current reached his max, this current
                can be estimate by (Iboost=Ib):
463         Irm = sqrt(Ib*(Qra/Ina)*0.5*Vdc/L);
464         % then the reverse recovery time can be estimated by:
465         trra= 2*Irm*L/(0.5*Vdc);
466         % turn off losses:
467         Eswa = ones(1,length(io_vec))*(Irm*VovA2*trra/12+Irm*VovA1*trra/12);
468         % the Irm^2*L energy losses:
469         ELr = 2*ones(1,length(io_vec))*(L*Irm^2/2+Irm*trra*Vdc/8);
470         % turn off losses due to the snubber Caps, Fall time calculation:
471         % nominal fall time
472         tfnx = (Rg+Rgx)*Ciss*log(Vgp/Vth);
473         % new fall time
474         tfx = (tfnx/Inm)*(Ib_vec-io_vec);
475         % snubber losses
476         EoffM_M= 2*((Ib_vec-io_vec).*tfx).^2/(4*6*(Cld+Cm(indVdc)));
477         % Sum up the switching losses:
478         Esw = Ecap+Eswa+ELr+EoffM_M;
479 % Gate Drive Energy 2 main switches
480         Egm = 2*Qgtm/Vqgm*(Vdrmm+Vdrmi)^2;
481         % Gate Drive Energy 2 auxiliary switches
482         Ega = 2*Qgta/Vqga*(Vdram+Vdrai)^2;
483         % Total gate losses
484         Egt = ones(1,length(io_vec))*(Egm+Ega);
485 % Total Energy loss:
486        %Et = EcondM+EAc+Esw+Egt;
487         Et = EcondM+EcondA+EL+Esw+Egt;
488 % Power Losses Calculations:
489         PcondM(indVdc)= 2*sum(EcondM)*fmod; % Conduction Main
490         PcondA(indVdc)= 2*sum(EcondA)*fmod; % Conduction Auxiliary
491         Psw(indVdc)= 2*sum(Esw)*fmod;     % Switching Losses Ca loss
492         PL(indVdc)= 2*sum(EL)*fmod;       % Inductor resistive loss
493         Pgt(indVdc)= 2*sum(Egt)*fmod;     % Gate Driving Losses
494         Pt(indVdc)= 2*sum(Et)*fmod;       % Total losses
495 end
496 %% Proposed switching sequence with 1 resonance pulse
```

```
%% voltageloopsoftn
% Initializations
PcondM = zeros(size(Vdc_vec))';
PAc = PcondM; Psw = PcondM;
Pgt = PcondM; PL = PcondM;
PcondA = PcondM; Pt = PcondM;
Il1 = zeros(x+1,length(t)); Il2 = Il1; Il3 = Il1; Il4 = Il1; Il5 = Il1;
Il6 = Il1; Il7 = Il1; Il8 = Il1; Il9 = Il1; Il10 = Il1;
for indVdc=1:length(Vdc_vec)
    Vdc=Vdc_vec(indVdc);
    %Ib=Ib_vec(indVdc);
    Ib = Ib_vec;
% Current Modes:
    % Mode 1 [t0-t1], lower Main diode conducts: KVL -> Rl,Rdsa1,Rf2a,Ronm;
    % Io*Rdsa<Vfa -> Rt1=Rl+2*Rdsa+Rfm; Rt1=Rl+2*(Rdsa+Rcea)+Rfm;
    Rt1=Rl+2*(Rdsa+Rcea)+(Rdsm+Rcem); % According to the assumbtion
    % VL+VR=Vdc*0.5-Vfa+Vfm+io*Rfm; -> Vt1=Vdc*0.5+Vfm+io*Rfm;
    % Vt1=Vdc*0.5+Vfm+io*Rfm;
    Vt1=0.5*Vdc+Vceom+io_vec*(Rdsm+Rcem);
    t1 = -L/Rt1*log(1-Rt1*(io_vec./Vt1));
    ta  = (0:stp:1)'*t1;
    for indsw =1:length(io_vec);
        Il1(:,indsw) = (Vt1(indsw)/Rt1)*(1-exp(-ta(:,indsw)*Rt1/L));
        %Il1 = ones(1,intint)'*(Vt1/Rt1).*(1-exp(-ta*Rt1/L));
    end
    % Mode 2 [t1,t2], lower MOSFET conducts: KVL; -> Rl,Rdsa,Rdsa,Rdsm;
    % ->Rt1=Rl+2*Rdsa+Rdsm;
    Rt2=Rl+2*(Rdsa+Rcea)+Rdsm+Rcem; % According to assumbtion
    % VL+VR=Vdc*0.5-Vfa+io*Rdsm; -> Vt2=Vdc*0.5+io*Rdsm;
    Vt2=Vdc*0.5-Vceoa+io_vec*(Rdsm+Rcem);
    t2 = -L/Rt2*log((Ib-Vt2/Rt2)./(io_vec-Vt2/Rt2));
    tb  = (0:stp:1)'*t2;
    for indsw =1:length(io_vec);
        Il2(:,indsw) = (Vt2(indsw)/Rt2)+(io_vec(indsw)-...
            Vt2(indsw)/Rt2).*exp(-tb(:,indsw)*Rt2/L);
    end
    % Mode 3 [t2-t3], Resonance mode:
    t3  = zeros(1,length(io_vec));
    Il3 = zeros(1/stp+1,length(io_vec));
    tc  = Il3;
    for indio=1:length(io_vec)
        io = io_vec(indio);
        Ib = Ib_vec(indio);
```

```
540         mode3new;
541         t3tt          = [0 cumsum(t3t)];
542         t3(:,indio) = max(t3tt);
543         tc(:,indio) = [0 cumsum(t3t)]';
544         Il3(:,indio)= i3t';
545     end
546     % Mode 4 [t3-t4], upper diode conducts: Rt4 = Rl+2*(Rdsa+Rcea)-Rfm;
547     % According to the assumption
548     Rt4 = Rl+2*(Rdsa+Rcea)+(Rdsm+Rcem);
549     % Vt4 = (-Vdc*0.5--Vfm-io*Rfm);
550     Vt4 = (-Vdc*0.5-Vceom-io_vec*Rdsm);
551     Ib4 = Il3(end,:);
552     t4 = -L/Rt4*log((io_vec-Vt4/Rt4)./(Ib4-Vt4/Rt4));
553     td  = (0:stp:1)'*t4;
554     for indsw =1:length(io_vec);
555         Il4(:,indsw) = (Vt4(indsw)/Rt4)+(Ib4(indsw)-...
556             Vt4(indsw)/Rt4).*exp(-td(:,indsw)*Rt4/L);
557     end
558     % Mode 5 [t4-t5], upper MOSFET conducts:
559     Rt5 = Rl+2*(Rdsa+Rcea)+(Rdsm+Rcem);
560     Vt5 = -Vdc*0.5+Vceom-io_vec*(Rdsm+Rcem);
561     Ib5 = Il4(end,:);
562     t5 = -L/Rt5*log((-Vt5/Rt5)./(-Vt5/Rt5+Ib5));
563     te  = (0:stp:1)'*t5;
564     for indsw =1:length(io_vec);
565         Il5(:,indsw) = (Vt5(indsw)/Rt5)+(Ib5(indsw)-...
566             Vt5(indsw)/Rt5).*exp(-te(:,indsw)*Rt5/L);
567     end
568     % Mode 7 [t6-t7], current decrease:
569     Rt7 = Rl+2*(Rdsa+Rcea)+(Rdsm+Rcem);
570     Vt7 = -Vdc*0.5+Vceom-(Rdsm+Rcem)*io_vec;
571     t7 = -L/Rt7*log(1+Ib_vec*Rt7./Vt7);
572     tg  = (0:stp:1)'*t7;
573     for indsw =1:length(io_vec);
574         Il7(:,indsw) = (Vt7(indsw)/Rt7).*(1-exp(-tg(:,indsw)*Rt7/L));
575     end
576     % Mode 8 [t7-t8], Resonance mode:
577     t8  = zeros(1,length(io_vec));
578     Il8 = zeros(1/stp+1,length(io_vec));
579     th  = Il8;
580     for indio=1:length(io_vec)
581         io = io_vec(indio);
582         Ib = Ib_vec(indio);
```

```
583         if 1
584             mode8new;
585             t8tt          = [0 cumsum(t8t)];
586             t8(:,indio)   = max(t8tt);
587             th(:,indio) = [0 cumsum(t8t)]';
588             I18(:,indio) = i8t';
589         end
590     end
591     % Mode 9 [t8-t9], current decrease to zero: Rt9 =
592     % Rl+2*(Rdsa+Rcea)+Rdsm;
593     Rt9 = Rl+2*(Rdsa+Rcea)+Rfm;
594     % Vt9 = Vdc*0.5+Vfm+Rfm*io;
595     Vt9 = Vdc*0.5+Vceom+io_vec*Rdsm;
596     Ib9 = I18(end,:);
597     t9 = real(-L/Rt9*log((-Vt9/Rt9)./(Ib9-Vt9/Rt9)));
598     ti  = (0:stp:1)'*t9;
599     for indsw =1:length(io_vec);
600         I19(:,indsw) = (Vt9(indsw)/Rt9)+(Ib9(indsw)-...
601             Vt9(indsw)/Rt9).*exp(-ti(:,indsw)*Rt9/L);
602     end
603     % Mode 6 [t5-t6], Upper MOSFET conducts:
604     t6 = Ts*D-(t4+t5);
605     tf=(0:stp:1)'*t6;
606     I16 = 0*tf;
607     % Mode 10 [t9-t0], Lower diode conducts: Conduction time for all
608     % switches:
609     Tm1 = D.*Ts;
610     Tm2 = (1-D).*Ts-(t1+t2+t3);
611     Ta1 = t1+t2+t3+t4+t5;
612     Ta2 = t7+t8+t9;
613     tx = (0:stp:1)'*Tm2;
614     I10= 0*tx;
615
616 % The next computations are only for Auxiliary Switches:}
617 % Body Diode current in each mode: Body diode A2
618     Id1 = (Vceoa+(Rcea+Rdsa)*I11-Vfa)/(Rdsa+Rfa+Rcea);
619     Id2 = (Vceoa+(Rcea+Rdsa)*I12-Vfa)/(Rdsa+Rfa+Rcea);
620     Id3 = (Vceoa+(Rcea+Rdsa)*I13-Vfa)/(Rdsa+Rfa+Rcea);
621     Id4 = (Vceoa+(Rcea+Rdsa)*I14-Vfa)/(Rdsa+Rfa+Rcea);
622     Id5 = (Vceoa+(Rcea+Rdsa)*I15-Vfa)/(Rdsa+Rfa+Rcea);
623     % Body diode A1
624     Id7 = 0*(Rdsa*I17+Vfa)/(Rdsa+Rfa);
625     Id8 = 0*(Rdsa*I18+Vfa)/(Rdsa+Rfa);
```

```
626      Id9 = 0*(Rdsa*Il9+Vfa)/(Rdsa+Rfa);
627       % Channel current in each mode: switch A2
628      Ich1 = (Vfa+Il1*Rfa)/(Rdsa+Rfa+Rcea);
629      Ich2 = (Vfa+Il2*Rfa)/(Rdsa+Rfa+Rcea);
630      Ich3 = (Vfa+Il3*Rfa)/(Rdsa+Rfa+Rcea);
631      Ich4 = (Vfa+Il4*Rfa)/(Rdsa+Rfa+Rcea);
632      Ich5 = (Vfa+Il5*Rfa)/(Rdsa+Rfa+Rcea);
633     % switch A1
634      Ich7 = 0*(-Vfa+Il7*Rfa)/(Rdsa+Rfa);
635      Ich8 = 0*(-Vfa+Il8*Rfa)/(Rdsa+Rfa);
636      Ich9 = 0*(-Vfa+Il9*Rfa)/(Rdsa+Rfa);
637 % Check the channel and the diode current-Auxiliary switches:}
638      inds = find(Id1<0);
639      Ich1(inds)=Il1(inds);
640      Id1(inds)=0;
641      inds = find(Id2<0);
642      Ich2(inds)=Il2(inds);
643      Id2(inds)=0;
644      inds = find(Id3<0);
645      Ich3(inds)=Il3(inds);
646      Id3(inds)=0;
647      inds = find(Id4<0);
648      Ich4(inds)=Il4(inds);
649      Id4(inds)=0;
650      inds = find(Id5<0);
651      Ich5(inds)=Il5(inds);
652      Id5(inds)=0;
653      inds = find(Id7>0);
654      Ich7(inds)=Il7(inds);
655      Id7(inds)=0;
656      inds = find(Id8>0);
657      Ich8(inds)=Il8(inds);
658      Id8(inds)=0;
659      inds = find(Id9>0);
660      Ich9(inds)=Il9(inds);
661      Id9(inds)=0;
662 % The next computations are only for Main Switches:}
663 % Body Diode current in each mode: Body diode A1
664 IdM1 = (Rdsm*(Il1-repmat(io_vec,x+1,1))-Vfm)/(Rdsm+Rfm);
665 IdM2 = (Rdsm*(Il2-repmat(io_vec,x+1,1))-Vfm)/(Rdsm+Rfm);
666 IdM3 = 0*(Rdsm*(Il3-repmat(io_vec,x+1,1))-Vfm)/(Rdsm+Rfm);
667 IdM4 = (Rdsm*(Il4-repmat(io_vec,x+1,1))-Vfm)/(Rdsm+Rfm);
668 IdM5 = (Rdsm*(Il5-repmat(io_vec,x+1,1))-Vfm)/(Rdsm+Rfm);
```

```
669 % Body diode A1
670 IdM7 = (Rdsm*(Il7+repmat(io_vec,x+1,1))+Vfm)/(Rdsm+Rfm);
671 IdM8 = 0*(Rdsm*(Il8+repmat(io_vec,x+1,1))+Vfm)/(Rdsm+Rfm);
672 IdM9 = (Rdsm*(Il9+repmat(io_vec,x+1,1))+Vfm)/(Rdsm+Rfm);
673 % Channel current in each mode: switch M2
674 IchM1 = (Vfm+(Il1-repmat(io_vec,x+1,1))*Rfm)/(Rdsm+Rfm);
675 IchM2 = (Vfm+(Il2-repmat(io_vec,x+1,1))*Rfm)/(Rdsm+Rfm);
676 IchM3 = 0*(Vfm+(Il3-repmat(io_vec,x+1,1))*Rfm)/(Rdsm+Rfm);
677 IchM4 = (Vfm+(Il4-repmat(io_vec,x+1,1))*Rfm)/(Rdsm+Rfm);
678 IchM5 = (Vfm+(Il5-repmat(io_vec,x+1,1))*Rfm)/(Rdsm+Rfm);
679 % switch A1
680 IchM7 = (-Vfm+(Il7+repmat(io_vec,x+1,1))*Rfm)/(Rdsm+Rfm);
681 IchM8 = 0*(-Vfm+(Il8+repmat(io_vec,x+1,1))*Rfm)/(Rdsm+Rfm);
682 IchM9 = (-Vfm+(Il9+repmat(io_vec,x+1,1))*Rfm)/(Rdsm+Rfm);
683     Iout  = repmat(io_vec,x+1,1);
684     IBoost = repmat(Ib_vec,x+1,1);
685
686 % Check the channel and the diode current-Main switches:
687     inds = find(IdM1<0);
688     IchM1(inds)=Il1(inds)-Iout(inds);
689     IdM1(inds)=0;
690     inds = find(IdM2<Iout);
691     IchM2(inds)=Il2(inds)-Iout(inds);
692     IdM2(inds)=0;
693     inds = find(IdM3<0);
694     IchM3(inds)=0*(Il3(inds)-Iout(inds));
695     IdM3(inds)=0;
696     inds = find(IdM4<0);
697     IchM4(inds)=Il4(inds)-Iout(inds);
698     IdM4(inds)=0;
699     inds = find(IdM5<0);
700     IchM5(inds)=Il5(inds)-Iout(inds);
701     IdM5(inds)=0;
702     inds = find(IdM7>-Iout);
703     IchM7(inds)=Il7(inds)+Iout(inds);
704     IdM7(inds)=0;
705     inds = find(IdM8>0);
706     IchM8(inds)=0*(Il8(inds)+Iout(inds));
707     IdM8(inds)=0;
708     inds = find(IdM9>0);
709     IchM9(inds)=Il9(inds)+Iout(inds);
710     IdM9(inds)=0;
711 % LOSS CALCULATION:
```

```
712 % Positive inductor current io*Rdsa\ensuremath{<}Vfa -\ensuremath{>} Diode will
        not conducts ... no Vfa*Il1 loosses The conduction energy is averaged over
        one switching cycle (stp) then
713     %it is averaged over fund. periode (t1,t3.....)
714 E1 = ((Rl+(Rdsa+Rcea))*trapz(Il1.^2)+Vceoa*trapz(Il1)+(Rdsa+Rcea)*trapz(Ich1.^2)
        +(Vfa*trapz(Id1)+      Rfa*trapz(Id1.^2))+Vceoa*trapz(Ich1)+(Rdsm+Rcem)*trapz
        ((IchM1).^2)+(Vceom)*trapz(IchM1)+    (Rfm)*trapz((IdM1).^2)+(Vfm)*trapz(IdM1)
        )*stp.*t1;
715 E2 = ((Rl+(Rdsa+Rcea))*trapz(Il2.^2)+Vceoa*trapz(Il2)+(Rdsa+Rcea)*trapz(Ich2.^2)
        +(Vfa*trapz(Id2)+Rfa*trapz(Id2.^2))+Vceoa*trapz(Ich2)+(Rdsm+Rcem)*trapz((
        IchM2).^2)+(Vceom)*trapz(IchM2)+(Rfm)*trapz((IdM2).^2)+(Vfm)*trapz(IdM2))*stp
        .*t2;
716 E3 = ((Rl+(Rdsa+Rcea))*trapz(Il3.^2)+Vceoa*trapz(Il3)+(Rdsa+Rcea)*trapz(Ich3.^2)
        +(Vfa*trapz(Id3)+          Rfa*trapz(Id3.^2))+Vceoa*trapz(Ich3))*stp.*t3;
717 E4 = ((Rl+(Rdsa+Rcea))*trapz(Il4.^2)+Vceoa*trapz(Il4)+(Rdsa+Rcea)*trapz(Ich4.^2)
        +(Vfa*trapz(Id4)+Rfa*trapz(Id4.^2))+Vceoa*trapz(Ich4)+(Rdsm+Rcem)*trapz((
        IchM4).^2)+(Vceom)*trapz(IchM4)+(Vceom)*trapz(IchM4)+(Rfm)*trapz((IdM4).^2)+(
        Vfm)*trapz(IdM4))*stp.*t4;
718 E5 = ((Rl+(Rdsa+Rcea))*trapz(Il5.^2)+Vceoa*trapz(Il5)+(Rdsa+Rcea)*trapz(Ich5.^2)
        +(Vfa*trapz(Id5)+Rfa*trapz(Id5.^2))+Vceoa*trapz(Ich5)+(Rdsm+Rcem)*trapz((
        IchM5).^2)+(Vceom)*trapz(IchM5)+(Vceom)*trapz(IchM5)+(Rfm)*trapz((IdM5).^2)+(
        Vfm)*trapz(IdM5))*stp.*t5;
719 % Negative inductor current
720 E7 = ((Rl+(Rdsa+Rcea))*trapz(Il7.^2)-Vceoa*trapz(Il7)+(Rdsa+Rcea)*trapz(Ich7.^2)
        +(-Vfa*trapz(Id7)+          Rfa*trapz(Id7.^2))-Vceoa*trapz(Ich7)+(Rdsm+Rcem)*
        trapz((IchM7).^2)+(Vceom)*trapz(IchM7)+ (Vceom)*trapz(IchM7)+(Rfm)*trapz((
        IdM7).^2)+(Vfm)*trapz(IdM7))*stp.*t7;
721 E8 = ((Rl+(Rdsa+Rcea))*trapz(Il8.^2)-Vceoa*trapz(Il8)+(Rdsa+Rcea)*trapz(Ich8.^2)
        +(-Vfa*trapz(Id8)+Rfa*trapz(Id8.^2))-Vceoa*trapz(Ich8))*stp.*t8;
722 E9 = ((Rl+(Rdsa+Rcea))*trapz(Il9.^2)-Vceoa*trapz(Il9)+(Rdsa+Rcea)*trapz(Ich2.^2)
        +(-Vfa*trapz(Id9)+Rfa*trapz(Id9.^2))-Vceoa*trapz(Ich9)+(Rdsm+Rcem)*trapz((
        IchM9).^2)+(Vceom)*trapz(IchM9)+(Vceom)*trapz(IchM9)+(Rfm)*trapz((IdM9).^2)+(
        Vfm)*trapz(IdM9))*stp.*t9;
723 % Inductor losses
724 EL = Rl*(trapz(Il1.^2).*t1+trapz(Il2.^2).*t2+trapz(Il3.^2).*t3+trapz(Il4.^2).*t4
          +trapz(Il5.^2).*t5+trapz(Il7.^2).*t7+trapz(Il8.^2).*t8+trapz(Il9.^2).*t9
        )*stp;
725 % Looses in Auxiliary Cirtcuit (Aux. switches and inductor):
726 EAc = E1+E2+E3+E4+E5+E7+E8+E9;
727 % Conduction losses in Auxiliary switches:
```

```
728 EcondA = (((Rdsa+Rcea)*trapz(Il1.^2)+Vceoa*trapz(Il1)+Vfa*trapz(Id1)+Rfa*trapz(
        Id1.^2)+(Rdsa+Rcea)*trapz(Ich1.^2)+Vceoa*trapz(Ich1)).*t1+((Rdsa+Rcea)*trapz(
        Il2.^2)+Vceoa*trapz(Il2)+Vfa*trapz(Id2)+Rfa*trapz(Id2.^2)+(Rdsa+Rcea)*trapz(
        Ich2.^2)+Vceoa*trapz(Ich2)).*t2+((Rdsa+Rcea)*trapz(Il3.^2)+Vceoa*trapz(Il3)+
        Vfa*trapz(Id3)+Rfa*trapz(Id3.^2)+(Rdsa+Rcea)*trapz(Ich3.^2)+Vceoa*trapz(Ich3)
        ).*t3+((Rdsa+Rcea)*trapz(Il4.^2)+Vceoa*trapz(Il4)+Vfa*trapz(Id4)+Rfa*trapz(
        Id4.^2)+(Rdsa+Rcea)*trapz(Ich4.^2)+Vceoa*trapz(Ich4)).*t4+((Rdsa+Rcea)*trapz(
        Il5.^2)+Vceoa*trapz(Il5)+Vfa*trapz(Id5)+Rfa*trapz(Id5.^2)+(Rdsa+Rcea)*trapz(
        Ich5.^2)+Vceoa*trapz(Ich5)).*t5+((Rdsa+Rcea)*trapz(Il7.^2)-Vceoa*trapz(Il7)-
        Vfa*trapz(Id7)+Rfa*trapz(Id7.^2)+(Rdsa+Rcea)*trapz(Ich7.^2)-Vceoa*trapz(Ich7)
        ).*t7+((Rdsa+Rcea)*trapz(Il8.^2)+Vceoa*trapz(Il8)-Vfa*trapz(Id8)+Rfa*trapz(
        Id8.^2)+(Rdsa+Rcea)*trapz(Ich8.^2)-Vceoa*trapz(Ich8)).*t8+((Rdsa+Rcea)*trapz(
        Il1.^2)-Vceoa*trapz(Il9)-Vfa*trapz(Id9)+Rfa*trapz(Id9.^2)+(Rdsa+Rcea)*trapz(
        Ich9.^2)-Vceoa*trapz(Ich9)).*t9)*stp;
729 % Conduction Losses for Main switches:
730 E6 = (Vceom*io_vec+(Rdsm+Rcem)*io_vec.^2).*Tm1;
731 E10= (Vceom*io_vec+(Rdsm+Rcem)*io_vec.^2).*Tm2;
732 EcondM = E6+E10;
733 % Switching losses in Auxiliary switches:
734 %at turn on both A1 and A2 are turned on at the same time "the output capacitance
        of A1 is discharged while the output capacitance of A2 is shorted by the
       body diode, the opposite for negative current slope". energy lost is given by
        (2 aux sw)
735       VovA2  = 1.2*Vdc;
736       VovA1 = 1.7*Vdc;
737       switch AuxSWITCHA
738           case 'MOSFET'
739               Ecap_ext  = ((Cdiff+5*Cv_g+Cl_r/2+Cly+Croot+2*C_coup)*VovA2^2/2)+((
                      Cdiff+  Cv_g+Cl_r/2+Cly)*VovA1^2/2);
740               compuener = cumtrapz(xos_data,xos_data.*yos_data*1e-12);
741               E_interp = interp1(xos_data,compuener,VovA2,'spline')+interp1(
                      xos_data,compuener,VovA1,'spline');
742               Ecap = (E_interp+Ecap_ext)*ones(1,length(t));
743           case 'IGBT'
744               Ecap_ext  = ((Cv_g+Cl_r/2+Cdiff+Cly+C_coup)*VovA2^2/2)+((Cdiff+2*Cv_g
                      +Croot)*VovA1^2/2);
745               compuener = cumtrapz(xos_data,xos_data.*yos_data*1e-12);
746               E_interp = interp1(xos_data,compuener,VovA2,'spline')+interp1(
                      xos_data,compuener,VovA1,'spline');
747               Ecap = (E_interp+Ecap_ext)*ones(1,length(t));
748       end
749 % A1 is turned off after the reverse current reached his max, this
750 % current can be estimate by (Iboost=Ib):
```

```
751 Irm = sqrt(Ib*(Qra/Ina)*0.5*Vdc/L);
752 % then the reverse recovery time can be estimated by:
753 trra= 2*Irm*L/(0.5*Vdc);
754 % turn off losses:
755 Eswa = ones(1,length(io_vec))*(Irm*VovA2*trra/12+Irm*VovA1*trra/12);
756 % the Irm^2*L energy losses:
757 ELr = 2*ones(1,length(io_vec))*(L*Irm^2/2+Irm*trra*Vdc/8);
758 % turn off losses due to the snubber Caps, Fall time calculation:
759 % nominal fall time
760 tfnx = (Rg+Rgx)*Ciss*log(Vgp/Vth);
761 % new fall time
762 tfx = (tfnx/Inm)*(Ib_vec-io_vec);
763 EoffM_M= ((Ib_vec-io_vec).*tfx).^2/(4*6*(Cld+Cm(indVdc)));
764 % Sum up the switching losses:
765 Esw = (Ecap+Eswa+ELr+EoffM_M)/2;
766 % Gate Drive Energy 2 main switches
767 Egm = 2*Qgtm/Vqgm*(Vdrmm+Vdrmi)^2;
768 % Gate Drive Energy 2 auxiliary switches
769 Ega = 2*Qgta/Vqga*(Vdram+Vdrai)^2;
770 % Total gate losses
771 Egt = ones(1,length(io_vec))*(Egm+Ega);
772 % Total Energy loss:
773 Et = EcondM+EcondA+EL+Esw+Egt;
774 % Power Losses Calculations:
775   PcondM(indVdc)= 2*sum(EcondM)*fmod; % Conduction Main
776   PcondA(indVdc)= 2*sum(EcondA)*fmod; % Conduction Auxiliary
777   Psw(indVdc)   = 2*sum(Esw)*fmod;    % Switching Losses Ca loss
778   PL(indVdc)    = 2*sum(EL)*fmod;     % Inductor resistive loss
779   Pgt(indVdc)   = 2*sum(Egt)*fmod;    % Gate Driving Losses
780   Pt(indVdc)    = 2*sum(Et)*fmod;     % Total losses
781  end
782 %% mode3new
783 % Initializations
784 % Mode 3 [t2-t3], Resonance mode: Aux is MOSFET; -\ensuremath{>} Rl,Rdsa,Rdsa; -\
        ensuremath{>} Rt3=Rl+2*Rdsa; Acoording to assumbtion
785 Rt3 = Rl+(Rdsa+Rcea)+(Rfa*(Rdsa+Rcea)/(Rfa+Rdsa+Rcea));
786 % VL+VR+VC=Vdc*0.5-Vfa; -> Vt3=Vdc*0.5;
787 Uq  = Vdc/2;
788 Vt3 = Uq;
789 uC0 = Vceom+(Rdsm+Rcem)*(Ib-io); % Initial Voltage Coss
790 iL0 = Ib;                  % Initial current
791 Ue  = Vdc+Vfm;   % final voltage Coss
792 xt = stp;                  % Number of points in this mode
```

```
% Start
delta3x = Rt3/(2*L);  % Damping factor
Vds2    = uC0:Ue*xt:Ue+uC0;  % Drain source of M2
Vds1    = Ue+uC0:-Ue*stp:uC0;% Drain source of M1
% set to zero
t3t  = zeros(1,length(Vds2)-1);
i3t  = zeros(1,length(Vds2));
A3t  = t3t; B3t = t3t; C3x = t3t;
Vc3t = i3t;
% Total Capacitance (C3x) of this mode and lambda1,2
for indVds2=1:length(Vds2)
    Cds2(indVds2)     = interp1(xos_data,yos_data*1e-12,Vds2(indVds2),'spline');
    Cds1(indVds2)     = interp1(xos_data,yos_data*1e-12,Vds1(indVds2),'spline');
    C3x(indVds2)      = (Cds1(indVds2)+Cds2(indVds2)+Cld);
    omega3x(indVds2) = sqrt(-delta3x.^2+1/(L*C3x(indVds2)));
    lambda1t(indVds2)= -delta3x +1i*omega3x(indVds2);
    lambda2t(indVds2)= -delta3x -1i*omega3x(indVds2);
end
% Finding the constants of the second order equation at each step:
% The initial solution
A3t(1) = (iL0-io-C3x(1).*lambda2t(1).*(uC0+Rt3*io-Uq))./(C3x(1).*(lambda1t(1)-
    lambda2t(1)));
B3t(1) = (io-iL0+C3x(1).*lambda1t(1).*(uC0+Rt3*io-Uq))./(C3x(1).*(lambda1t(1)-
    lambda2t(1)));
% Time step #1:
t3t(1) = real( (1./(-1i*omega3x(1))).*(log( (-(-Vds2(2)-io*Rt3+Uq)+sqrt((-Vds2(2)
    -io*Rt3+Uq).^2-4.*A3t(1).*B3t(1)))./(2*B3t(1)))));
Vc3t(1)= uC0;
i3t(1) = iL0;
for indv = 2:length(Vds2)-1
% Next capacitore voltage value:
Vc3t(indv) = A3t(indv-1).*exp(lambda1t(indv-1).*t3t(indv-1))+B3t(indv-1).*exp(
    lambda2t(indv-1).*t3t(indv-1))+Uq-io*Rt3;
% Next inductor current value:
i3t(indv)  = C3x(indv-1).*(lambda1t(indv-1).*A3t(indv-1).*exp(lambda1t(indv-1).*
    t3t(indv-1))+lambda2t(indv-1).*   B3t(indv-1).*exp(lambda2t(indv-1).*t3t(indv
    -1)))+io;
% Next constats
A3t(indv)  = (i3t(indv)-io-C3x(indv).*lambda2t(indv).*(Vc3t(indv)+Rt3*io-Uq))./(
    C3x(indv).*(lambda1t(indv)-lambda2t(indv)));
B3t(indv)  = (io-i3t(indv)+C3x(indv).*lambda1t(indv).*(Vc3t(indv)+Rt3*io-Uq))./(
    C3x(indv).*(lambda1t(indv)-lambda2t(indv)));
% Next time step
```

```
828 t3t(indv) = real( (1./(-1i*omega3x(indv))).*(log( (-(-Vds2(indv+1)-io*Rt3+Uq)+
        sqrt((-Vds2(indv+1)-io*Rt3+Uq).^2-4.*A3t(indv).*B3t(indv))./(2*B3t(indv)))))
        ;
829 end
830 indv = length(Vds2);
831 Vc3t(indv) = A3t(indv-1).*exp(lambda1t(indv-1).*t3t(indv-1))+B3t(indv-1).*exp(
        lambda2t(indv-1).*t3t(indv-1))+Uq-io*Rt3;
832 % Next inductor current value:
833 i3t(indv) = C3x(indv-1).*(lambda1t(indv-1).*A3t(indv-1).*exp(lambda1t(indv-1).*
        t3t(indv-1))+lambda2t(indv-1).* B3t(indv-1).*exp(lambda2t(indv-1).*t3t(indv
        -1)))+io;
834 figure(1); plot([0 cumsum(t3t)],i3t) ;xlabel('Time [S]');
835 ylabel('Resonant current [A]') ;grid minor;
836 figure(2); plot([0 cumsum(t3t)],[Vc3t' Vds2']);xlabel('Time [S]');
837 ylabel({'Capacitor Voltage [V]','Vds2'});grid minor;
838
839 %% mode8new
840 % Mode 8 [t7-t8], Resonance mode: Aux is MOSFET; -\ensuremath{>} Rl,Rdsa,Rdsa; -\
        ensuremath{>} Rt3=Rl+2*Rdsa;
841 % Acoording to assumbtion
842 Rt8 = Rl+(Rdsa+Rcea)+(Rfa*(Rdsa+Rcea)/(Rfa+Rdsa+Rcea));
843 % VL+VR+VC=Vdc*0.5-Vfa; -> Vt3=Vdc*0.5;
844 Uq      = Vdc/2;
845 uC80 = Vdc-Vfm;            % Initial Voltage Coss
846 iL80    = -Ib;               % Initial current
847 Ue8     = Vceom+Rdsm*io;     % final voltage Coss
848 xt = stp;                % Number of points in this mode
849 delta8x  = 0*Rt8/(2*L);             % Damping factor
850 Vds18    = Ue8:uC80*xt:Ue8+uC80;      % Drain source of M2
851 Vds28    = uC80+Ue8:-uC80*xt:Ue8;    % Drain source of M1
852 % set to zero
853 t8t  = zeros(1,length(Vds28)-1);
854 i8t  = zeros(1,length(Vds28));
855 A8t  = t8t; B8t = t8t; C8x = t8t;
856 Vc8t = i8t;
857 for indVds28=1:length(Vds28)
858     Cds28(indVds28)     = interp1(xos_data,yos_data*1e-12,Vds28(indVds28),'spline'
            );
859     Cds18(indVds28)     = interp1(xos_data,yos_data*1e-12,Vds18(indVds28),'spline'
            );
860     C8x(indVds28)       = (Cds18(indVds28)+Cds28(indVds28)+Cld);
861     omega8x(indVds28)   = sqrt(-delta8x.^2+1/(L*C8x(indVds28)));
862     lambda18t(indVds28)= -delta8x +1i*omega8x(indVds28);
```

```
863     lambda28t(indVds28)= -delta8x -1i*omega8x(indVds28);
864 end
865 % The initial solution
866 A8t(1) = (iL80-io-C8x(1).*lambda28t(1).*(uC80+Rt8*io-Uq))./(C8x(1).*(lambda18t(1)
        -lambda28t(1)));
867 B8t(1) = (io-iL80+C8x(1).*lambda18t(1).*(uC80+Rt8*io-Uq))./(C8x(1).*(lambda18t(1)
        -lambda28t(1)));
868 % Time step #1:
869 t8t(1) = real( (1./(1i*omega8x(1))).*(log( (-(-Vds28(2)-io*Rt8+Uq)+sqrt((-Vds28
        (2)-io*Rt8+Uq).^2-4.*A8t(1).*B8t(1)))./(2*A8t(1)))));
870 Vc8t(1)= uC80;
871 i8t(1) = iL80;
872 for indv8 = 2:length(Vds28)-1
873 % Next capacitore voltage value:
874 Vc8t(indv8) = A8t(indv8-1).*exp(lambda18t(indv8-1).*t8t(indv8-1))+B8t(indv8-1).*
        exp(lambda28t(indv8-1).*t8t(indv8-1))+Uq-io*Rt8;
875 % Next inductor current value:
876 i8t(indv8)  = C8x(indv8-1).*(lambda18t(indv8-1).*A8t(indv8-1).*exp(lambda18t(
        indv8-1).*t8t(indv8-1))+lambda28t(indv8-1).*B8t(indv8-1).*exp(lambda28t(indv8
        -1).*t8t(indv8-1)))+io;
877 % Next constats
878 A8t(indv8)  = (i8t(indv8)-io-C8x(indv8).*lambda28t(indv8).*(Vc8t(indv8)+Rt8*io-Uq
        ))./(C8x(indv8).*(lambda18t(indv8)-lambda28t(indv8)));
879 B8t(indv8)  = (io-i8t(indv8)+C8x(indv8).*lambda18t(indv8).*(Vc8t(indv8)+Rt8*io-Uq
        ))./(C8x(indv8).*(lambda18t(indv8)-lambda28t(indv8)));
880 % Next time step
881 t8t(indv8)  = real( (1./(1i*omega8x(indv8))).*(log( (-(-Vds28(indv8+1)-io*Rt8+Uq)
        +sqrt((-Vds28(indv8+1)-io*Rt8+Uq).^2-4.*A8t(indv8).*B8t(indv8)))./(2*A8t(
        indv8)))));
882 end
883 indv8 = length(Vds28);
884 Vc8t(indv8) = A8t(indv8-1).*exp(lambda18t(indv8-1).*t8t(indv8-1))+B8t(indv8-1).*
        exp(lambda28t(indv8-1).*t8t(indv8-1))+Uq-io*Rt8;
885 % Next inductor current value:
886 i8t(indv8)  = C8x(indv8-1).*(lambda18t(indv8-1).*A8t(indv8-1).*exp(lambda18t(
        indv8-1).*t8t(indv8-1))+lambda28t(indv8-1).*B8t(indv8-1).*exp(lambda28t(indv8
        -1).*t8t(indv8-1)))+io;
887 figure(1); plot([0 cumsum(t8t)],i8t) ;xlabel('Time [S]');ylabel('Resonant current
        [A]') ;grid minor;
888 figure(2); plot([0 cumsum(t8t)],[Vc8t' Vds28']);xlabel('Time [S]');ylabel({'
        Capacitor Voltage [V]','Vds2'});grid minor;
889 %% mode3voltage
```

```
890 % Mode 3 [t2-t3], Resonance mode: Aux is MOSFET; -> Rl,Rdsa,Rdsa; -> Rt3=Rl+2*
        Rdsa;
891 Rt3=Rl+2*(Rdsa+Rcea); % Acoording to assumbtion
892 % VL+VR+VC=Vdc*0.5-Vfa; -> Vt3=Vdc*0.5;
893 Uq=Vdc/2;
894 Vt3=Uq;
895 uC0=Vceom+(Rdsm+Rcem)*(Ib-io); % Initial Voltage Coss
896 iL0=Ib;                        % Initial current
897 Ue=Vdc+Vfm;                    % final voltage Coss
898 N=1;
899 delta3x=Rt3/(2*L);
900 Vds2=uC0;
901 t3x=0;
902 i3x=Ib;
903 %i3x(end)=Ib;
904 tstep=0.1e-9;
905 Cds1=[];
906 Cds2=[];
907 while (Vds2<Ue+uC0);        % voltage loop
908     Cds2(N)= interp1(xos_data,yos_data*1e-12,Vds2(N),'spline');
909     Cds1(N)= interp1(xos_data,yos_data*1e-12,(Ue-Vds2(N)),'spline');
910     omega3x(N)=sqrt(-delta3x.^2+1/(L*(Cds1(N)+Cds2(N)+Cld)));
911     lambda1x(N)=-delta3x +1i*omega3x(N); %(Root 1)
912     lambda2x(N)=-delta3x -1i*omega3x(N); %(Root 2)
913     % A and B are coming from nonhomo. second order diff.equ.solution
914     A3x(N)=( i3x(N)-io-(Cds1(N)+Cds2(N)+Cld)*lambda2x(N).*(Vds2(N)-Uq+Rt3*io))
            ./(2i*omega3x(N)*(Cds1(N)+Cds2(N)+Cld));
915     B3x(N)=(-i3x(N)+io+(Cds1(N)+Cds2(N)+Cld)*lambda1x(N).*(Vds2(N)-Uq+Rt3*io))
            ./(2i*omega3x(N)*(Cds1(N)+Cds2(N)+Cld));
916     t3x(N+1)=(N)*tstep;
917     Vds2(N+1)=Uq-Rt3*io+exp(-delta3x.*tstep).*( A3x(N).*exp(1i*omega3x(N).*tstep)
            + B3x(N).*exp(-1i*omega3x(N).*tstep));
918     i3x(N+1)=(Cds1(N)+Cds2(N)+Cld).*exp(-delta3x.*tstep).*(lambda1x(N).*A3x(N).*
            exp(1i*omega3x(N).*tstep)+lambda2x(N).*B3x(N).*exp(-1i*omega3x(N).*tstep)
            )+io;
919     N=N+1;
920 end
921 figure(1); plot(t3x,i3x);
922 xlabel('Time in Sec'); ylabel('Current in resonance mode - mode 3')
923 grid minor;
924 figure(2);plot(t3x,Vds2);grid minor;
925 figure(3); plot(t3x(1:end-1),Cds1+Cds2);grid minor;
```