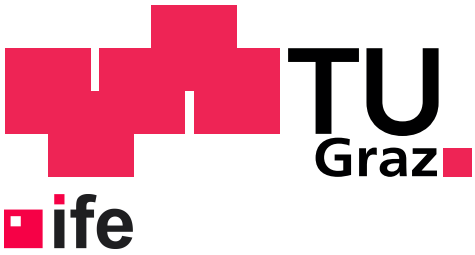
Master's Thesis



Graz University of Technology
Faculty of Electrical and Information Engineering

Institute of Electronics

Fully-Integrated Time References

A Very Low-Power Design for System Wake-Up

Lukas Niederwieser

Head: Univ.-Prof. Dipl.-Ing. Dr.techn. Bernd Deutschmann
Supervisor: Ass.-Prof. Dipl.-Ing. Dr.techn. Mario Auer
Field of study: Electrical Engineering
Subfield: Analog Chip Design
March 2018

Acknowledgements

I would like to thank my supervisor Ass.-Prof. Dipl.-Ing. Dr.techn. Mario Auer for supporting me throughout this thesis.

Furthermore, special thanks goes to Jakob Jongsma and the complete team of Panthronics AG for giving me the opportunity of being surrounded by many smart and pleasant people during the last months. Thank you for providing a very professional atmosphere and the innovative way of thinking within this start-up.

I would also like to acknowledge Petr Olšák who created the LaTeX-template the design of this thesis is based on and of course I would like to thank everybody that spend time on proofreading.

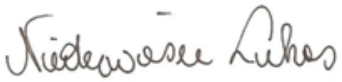
Words can't express my gratitude to my dear friends and family. This boundless support and the lovely conversations always helped me to go one step further. I am truly lucky to have such great people around me.

Once again, I would love to thank my parents for supporting me and my studies throughout all these years. Regardless how far away they are physically, they are never far from my heart and mind. *This thesis is dedicated to them.*

Declaration

I declare that I have authored this thesis independently, that I have not used other than the declared sources / resources, and that I have explicitly marked all material which has been quoted either literally or by content from the used sources.

Graz, 02. March 2018



Abstract

In this thesis the design of a low-power on-chip dual-phase CMOS relaxation oscillator is presented, which produces a $100kHz$ 50% duty-cycle clock signal for wake-up timers in battery powered systems. It consumes only $500nA$ from a $1.8V$ supply, while having a very good temperature stability of $65\frac{ppm}{°C}$ from $-50°C$ to $120°C$. The supply voltage coefficient is $9\frac{\%}{V}$.

Part of the design is a novel CMOS-only reference generator, that provides both a temperature compensated current and voltage to the oscillator. The temperature coefficients of the current and voltage are as low as $52\frac{ppm}{°C}$ and $68\frac{ppm}{°C}$, with a maximum process spread of $\pm 7.1\%$ and $\pm 3.5\%$. A self-biased continuous-time comparator with adaptive biasing speeds up operation and ensures rail-to-rail output signals with low rise and fall times.

The oscillator is designed for one of TSMC's 180nm technologies and occupies an area of $0.073mm^2$.

Abstrakt

In dieser Arbeit wird der Schaltungsentwurf eines vollintegierten, stromsparenden CMOS Oszillators, welcher ein $100kHz$ Ausgangssignal mit 50% Pulsweite erzeugt, beschrieben. Dieses Taktsignal wird für Wake-up Timer in batteriebetriebenen Systemen eingesetzt und hat dabei einen geringen Stromverbrauch von nur $500nA$ bei $1.8V$ Versorgung. Der Oszillator erreicht eine sehr gute Temperaturstabilität von $65\frac{ppm}{°C}$ über einen Temperaturbereich von $-50°C$ bis $120°C$. Der Spannungskoeffizient liegt bei $9\frac{\%}{V}$.

Teil der Schaltungsentwicklung war der Entwurf eines neuen, widerstandslosen Referenzgenerators. Dieser erzeugt einen kompensierten Strom und eine Spannung mit niedrigen Temperaturkoeffizienten von $52\frac{ppm}{°C}$ und $68\frac{ppm}{°C}$. Dabei ist die maximale Prozessschwankung für Strom und Spannung mit $\pm 7.1\%$ und $\pm 3.5\%$ gering. Ein zeitkontinuierlicher Komparator, welcher sein Strombudget im Umschaltzeitpunkt erhöht, sorgt für niedrige Anstiegs- und Abfallzeiten sowie rail-to-rail Ausgangssignale.

Der Oszillator ist für eine TSMC 180nm Technologie entworfen und nimmt eine Fläche von $0.073mm^2$ ein.

Contents

Figures

Tables

Chapter 1

Introduction

1.1 Motivation

The Internet of Things, short IoT, is a term that is around for years now and refers to a ever-growing network of all kinds of physical objects - from health monitors over wearables, household and entertainment systems down to industrial equipment. This attractive prospect leads to more productivity and efficiency, easier control, safety, less data re-entry and many benefits concerning data analysis. Therefore it is emerging as the third wave in development of the Internet and will rearrange the technical landscape, again.

Figure 1.1: IoT illustrated - labs.sogeti.com

Decisive that the IoT developed, step-by-step, is the greatly decrease of size and simultaneous intensively increase in complexity of integrated circuits during the last few decades. Featured by habitually shrink of technology nodes[1], VLSI[2] has enjoyed the rapid exponential growth characterized by

[1] 10nm ramp-up announced at the end of 2016
[2] Very Large Scale Integration

Moore's Law. As a result, we have semiconductor ICs that successfully integrate complex signal processing chains, CPU[3] cores, digital functions as well as analog circuitry within modern sub-micron technologies.

Nowadays, most of us routinely use portable electronic devices that include hundreds of integrated circuits, predominant SoCs[4], as keystone for increased functionality, performance and connectivity. All of these devices include energy storage technology that enhances much slower than semiconductor technologies do. Reducing energy consumption of integrated circuits is therefore vital to preserve the available battery capacity and guarantee long-term operation.

Hence, it is essential for modern integrated circuits that target portable devices, connecting to the IoT, to include low-power circuitry.

1.2 Problem statement

In a battery-powered, portable device, SoCs are most of the time in stand-by mode and woken up at a regular interval. Then the system starts to perform and after it is out of action for a certain time, the energy consumption is minimized by setting it into a low-power mode to preserve battery capacity. The time spend in this mode is usually much longer than time spend in active mode. Energy is defined as:

$$E = \int P(t) \cdot dt.$$

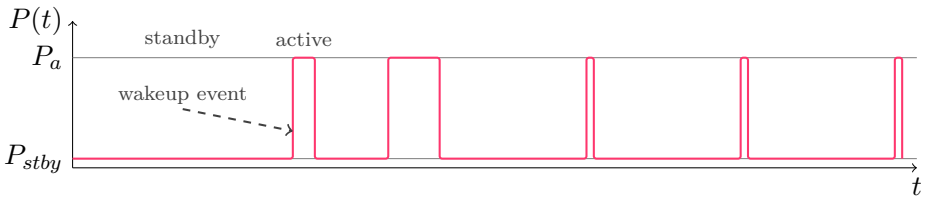


Figure 1.2: Power profile illustrated

Energy is the integral of power $P(t)$ over time t. Thus, it is important that the internal wake-up function does not consume excessive power from the battery as it works continuously and should never become the dominant energy consumer against primary system functions, accessible during active mode. On the other hand, by reduction of the overall energy consumption costs of portable devices are lower due to smaller battery capacities for a guaranteed lifetime. In such applications very low-power operation is a major challenge, especially for clock generators, which are the heart of any digital circuit. In additon a certain accuracy has to be achieved to prevent that the battery capacity needs an extra margin. The power consumption of digital

[3] Central Processing Unit
[4] System on Chip

circuitry $P_{digital}$ that is driven by the clock source can be defined as follows, [NJ97, GM16].

$$P_{digital} = P_{dyn} + P_{stat}$$

with

$$P_{dyn} = \alpha \cdot C_L \cdot V_{DD}^2 \cdot f_{CLK}$$

and

$$P_{stat} \propto T^2 \cdot e^{-\beta/T}$$

The dynamic power P_{dyn}, major part of power consumption, is direct proportional to the frequency of the clock generator f_{CLK}, the load capacitance C_L and a technology based constant α. An excessive frequency variation is therefore undesirable. The relation between dynamic power consumption and the supply voltage V_{DD} is quadratic and most of the time fixed within a certain technology. Static power consumption P_{stat}, namely leakage, is dependent on temperature T and another technology parameter β.

Thus, main requirements for such circuits are, that they can be fully integrated and have low sensitivity to temperature, supply voltage and process.

What is it about? This thesis is about fully-integrated time-references and a very low-power relaxation oscillator for system wake-up, that is designed for TSMCs 180nm technology node. The design is used in a SoC, targeting devices that want to provide NFC[5] within the IoT.

1.3 Outline

This thesis is organized in three parts:

Part I

The first part gives basics concerning oscillators and contains information how oscillators in general are characterized. This is followed by a chapter of fully-integrated time reference concepts and covers a wide range of different oscillator structures. Including basic considerations, behavioural models as well as circuitry examples and benchmarks. This part can be considered to be a theoretical summary of oscillators that don't use any off-chip components and their design constraints.

[5] Near Field Communication

Part II

This part is dedicated to the design of a very-low power oscillator. After knowledge of various structures was gained throughout the previous part of the thesis, a appropriate structure can be chosen. Of course the specifications are given and the concept of the dual-phase system is introduced. All system blocks and their theoretical backgrounds are discussed. Further, new approaches that led to a very low-power design are shown and implemented in this part. The last chapter deals with leakage and a dedicated calibration scheme suitable for low-power designs and how the overall specifications are met.

Part III

The last part includes a chapter that shows results in a very compact way. Additional, the calibration flowchart that can be easily implemented within the digital regime is shown. Schematics and layout can also be seen in this part. The summary gives all achieved performance parameters and compares the specification against this low-power design. Finally, the conclusion and future work is given.

Part I

Background

Chapter 2

Oscillator Basics

For most of today's modern integrated circuits oscillators are an integral part. They provide a stable time reference and are essential for every digital circuitry, like microprocessors. Other crucial applications range from carrier synthesis in cellular phones down to wake-up time references within PMUs[1], requiring different topologies and performance characteristics.

Oscillators are designed to provide a periodic output signal without necessity of an input signal. They act as a kind of feedback amplifier that is only connected to the supply voltage. Over years many different types of oscillators have been developed that are able to provide different waveforms, sinusoidal or non-sinusoidal.

This chapter deals with some basic considerations concerning oscillators and how they can be characterized. Section 2.1 gives information about criteria that can be applied to a subset of linear systems, to analyse if they are capable of oscillation.

2.1 Barkhausen criterion

First of all, it has to be noted that Barkhausen's criterion is simple and intuitive. Hence it is used throughout this thesis to explain basic behaviour, but gives not full information if a system is stable or gives oscillation at a certain frequency, [Teo13], [AK13]. Usually oscillators give a periodic output in form of voltage V_{out}. As there is no input signal the circuit must entail a self-sustaining mechanism, that provides a periodic fluctuation of energy. In case of linear oscillators[2] this is achieved by a feedback system depicted in figure 2.1 and the overall transfer function $T(s)$, where $F(s)$ is the transfer function of the feedback itself and $A(s)$ of an amplifier.

$$T(s) = \frac{V_{out}}{V_{in}} = \frac{A(s)}{1 - A(s)\,F(s)}$$

As the system's steady state behaviour is analysed, the complex frequency s is set to be purely imaginary. This special case of the generalized Laplace

[1] Power Management Unit

[2] sinusoidal output

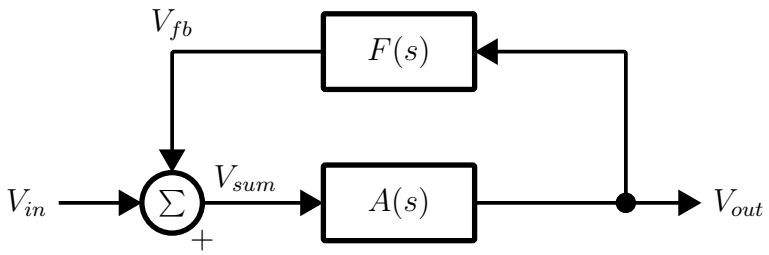


Figure 2.1: Feedback system

Transform implies that the transient behaviour is not of interest at this point.

$$s \to j\omega_0$$

Self-sustaining implies that oscillation occurs without input signal $V_{in} = 0$. Therefore, Barkhausen's criterion for oscillation at ω_0 is written as follows.

$$A\left(j\omega_0\right) F\left(j\omega_0\right) = 1.$$

This can be split into gain and phase criterion.

Gain criterion

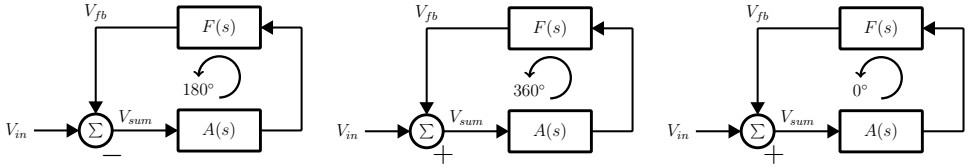
$$\left|A\left(j\omega_0\right) \cdot F\left(j\omega_0\right)\right| \geq 1$$

Phase criterion

$$\angle A\left(j\omega_0\right) + \angle F\left(j\omega_0\right) = 0° or\ n \cdot 360°$$

Which n as a positive integer value, the gain and phase criterion must be simultaneously be met at ω_0. The phase criterion implies that a positive feedback is needed to make a system oscillate. Once again it is stated that general systems with a feedback path are able to, but not necessarily oscillates if the gain and the phase shift of the loop is chosen properly.

Usually the feedback path, formed out of passive elements, is an attenuator and this means that $A\left(j\omega_0\right)$ must be an amplifier to get the loop gain equal to or greater than one. If the amplification factor is much higher than needed, systems turn into non-linear oscillators and the output is a non-sinusoidal waveform. Additional, amplifiers in integrated circuits have low-pass characteristics (capacitive behaviour) so the feedback path needs to shift back the phase by an inductive behaviour or shift it further to get n-times 360° phase shift. There are different feedback configurations that are



(a) phase shift: 180° **(b)** phase shift: 360° **(c)** phase shift: 0°

Figure 2.2: Various views of oscillator feedback

able to make a system oscillate. Seen in figure 2.2, where figure 2.2a includes a negative summing point.

In a common amplifier design exactly this oscillation criteria should never be met. For this structures the phase margin[3] at unity gain is therefore an important design parameter.

2.2 Classification

It is not easy to classify oscillators as there is enormous variation in target applications, behaviour and structure. There are many methods to categorize these circuits. In this thesis three approaches has been chosen. The first one is based on the oscillation mode and the second one on the amplitude stabilization method. The third one takes frequency range and power level into account.

Furthermore, one might also classify oscillators based on the structure, order of the resonator, noise characteristics or simply on the basis of it's application.

Oscillation mode

Truly sinusoidal waveforms can only be found in ideal undamped systems. Anyway, all real circuits cause distortion and therefore the term 'harmonic mode' refers to low distorted, weakly non-linear oscillators, e.g. in LC resonators, and is used for classification. The amount of distortion caused by the oscillator depends on various aspects, such as it's limiting mechanism and structure.

The term 'relaxation mode' is commonly used for circuits where the gain factor is much higher than required for an oscillation build-up, [ES53].

$$|A(j\omega_0)|\,|F(j\omega_0)| \gg 1$$

This results in a rapid state transition, followed by a long period of an almost constant state. Nowadays ring oscillators and multi-vibrators are commonly called relaxation oscillators, but the term itself dates back to the era of vacuum tubes. They build up tension slowly, but can quickly release

[3] how many degrees are left to hit a systems oscillation point

(i.e. relax) their voltage. Figure 2.3 shows how waveforms for an integrated relaxation oscillator could look like.

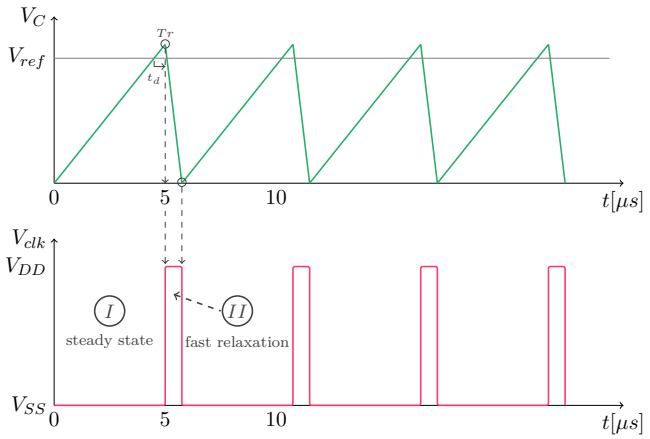


Figure 2.3: Waveform example of an integrated relaxation oscillator

Although there is a strict separation between these two modes, ring oscillators and multi-vibrators can be designed to produce almost sinusoidal waveforms. If the frequency is increased these circuits do not necessarily oscillate in relaxation mode. Also LC oscillators enter relaxation mode under certain conditions. This means that the oscillation mode, determined by design, does not depend on an oscillators structure.

Amplitude stabilization

All oscillators include an amplitude stabilization or limiting mechanism. There are different approaches like clipping, an amplitude control loop, self-limiting or introducing a power-sensitive attenuator.

One option for amplitude stabilization, that is often used in modern IC implementations, is 'self-limiting'. They are simply to design and alternatives rarely show better performance. Non-linear characteristics of an active element, most of the time the amplifier, are used for limitation. No additional circuitry is needed and this method is often applied in high-frequency oscillators.

Another method is to introduce an 'amplitude control loop', also called AGC[4]. For low distortion and a constant amplitude over various parameters such as temperature, process or supply voltage an amplitude control loop is established. The system seen in figure 2.4 consists out of an amplitude detector, providing a voltage that is proportional to the amplitude, an error amplifier and a gain control block that is fed by the amplifiers output. This block changes the bias current to adjust the transconductance and therefore the gain of the oscillator. This leads to more complexity, increased power consumption and might include stability issues.

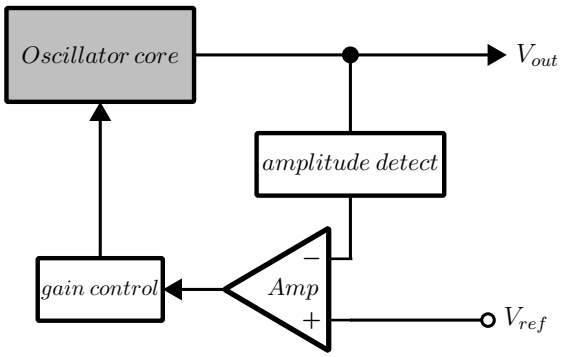


Figure 2.4: Amplitude control loop

'Power-sensitive attenuators' might be used in low distortion designs but are not very suitable within integrated circuits. Usually this are some kinds of temperature-sensitive resistors and the systems suffer from long time constants that make them inappropriate for high frequency oscillators.

The last method to limit the amplitude is 'clipping' and causes an noisy oscillator. Anyway it can be used in systems that oscillate in relaxation mode as it might be an desired behaviour, e.g. rail to rail square-wave output.

Power level and frequency range

Oscillators can also be classified on basis of the application, targeting a certain feature. Based on the frequency range, oscillators can be classified as listed in table 2.1.

[4] Automatic Gain Control

Classification	Frequency Range
Very Low Frequency	<30Hz - 30kHz
Low Frequency	30kHz - 300kHz
High Frequency	300kHz - 3MHz
Medium Frequency	3MHz - 30MHz
Very High Frequency	30MHz - 300MHz
Ultra High Frequency	300MHz - 3GHz

Table 2.1: Frequency classification

Taking the power level as characterization method there is a major dependency on the operating frequency and therefore on the application. Common terms are 'Low Power' and 'Very-Low Power'. Sometimes also the term 'sub μ-Watt' is used for low frequency oscillators.

Chapter 3

Fully-Integrated Time References

In this chapter information about oscillator structures that can be fully integrated are given. Distinguished by their output waveform, either a linear or non-linear oscillator is described.

3.0.1 Linear to nonlinear

As already described in section 2.1 a linear system can turn into a non-linear one if high gain is applied to the closed loop, and active elements get piled out of their linear region as the signal amplitude continuously rises. Therefore, to obtain linear oscillators, an amplitude limitation is significant. Figure 3.1 shows the large signal characteristics of a differential pair. It's commonly used as input stage for amplifiers and biased with the current I_{BIAS}. If the differential input signal $V_{inp} - V_{inn}$ exceeds $\sqrt{\frac{I_{BIAS}}{K}}$, with the process transconductance $K \propto \frac{W}{L}$, the circuit gets strongly non-linear and sinusoidal signals are distorted. By introduction of non-linearity the harmonic content increases and the waveform changes, i.e. figure 3.2.

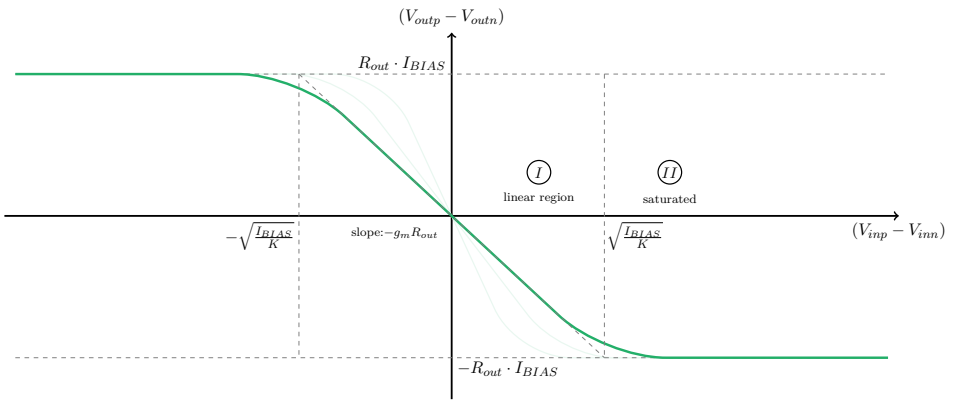


Figure 3.1: Large signal - differential pair

Generally, most oscillators, linear and non-linear, are designed to satisfy the Barkhausen criterion. However, this only indicates a constant periodic output signal and not the shape of the waveform. In integrated circuits this signals get buffered, resulting in a square-wave signal that can be used as a

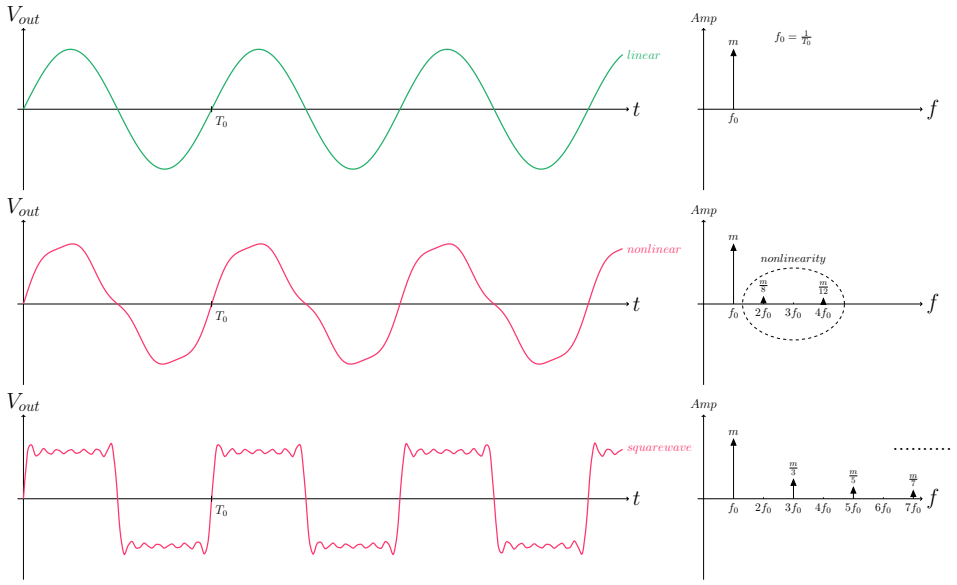


Figure 3.2: Output waveforms - linear and non-linear system

clock reference for digital circuitry. Many on-chip oscillators, especially for low-power applications, are comparator based designs that are capable of giving square-wave output without internal sinusoidal signals. Additional to low power consumption this leads to a good noise performance, as internal nodes are low ohmic most of the time. This designs are commonly named relaxation oscillators and in this thesis listed under non-linear (RC) oscillators, as they have non-sinusoidal square-wave outputs. Figure 3.2 shows a linear harmonic signal, a distorted, and a square-wave signal including 6 harmonics.

3.1 LC based oscillators

This oscillator structure is preferred if higher frequencies of oscillation, usually greater than 20 MHz, are required. They are known for their quasi linear behaviour and the low phase noise. This makes them common circuits within RF designs. They can be fully-integrated in modern RF technologies, having monolithic inductors available, but consume more chip area compared to RC oscillators.

3.1.1 Behavioral model

This type of oscillators consist out of a frequency selective tank (C, L, g_t) that is connected to an active transconductance element g_m. The basic idea is shown in figure 3.3, where g_t models the losses within the LC tank.

Analysing the basic structural model of the LC oscillator gives the transfer function of the feedback network $F(j\omega)$, formed by the impedance of the tank and the amplifier transfer function $A(j\omega)$, given by g_m.

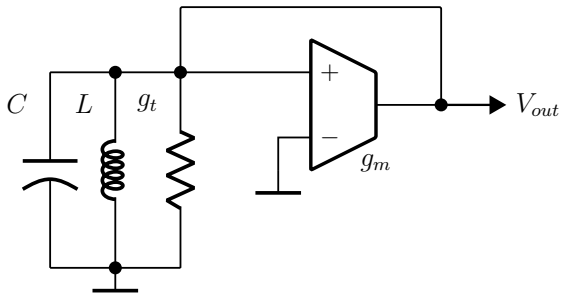


Figure 3.3: Structure of a LC based oscillator

$$F(j\omega) = \frac{1}{g_t \cdot \left(1 + j\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right) \cdot Q\right)}$$

$$A(j\omega) = g_m$$

Where Q, the quality factor, is given as follows.

$$Q = \frac{1}{g_t} \cdot \sqrt{\frac{C}{L}}$$

To fulfil Barkhausen's criterion for $\omega = \omega_0$, the amplifier has to compensate the losses of the tank circuit. To obtain a loop gain $|A(j\omega_0) \cdot F(j\omega_0)|$ of unity, $g_m = g_t$ has to be met. The overall phase shift is 0° due to a −90° shift caused by the capacitance and 90° shift by the inductance. As g_m cancels g_t, the frequency f_0 can be calculated considering only a simple LC resonator.

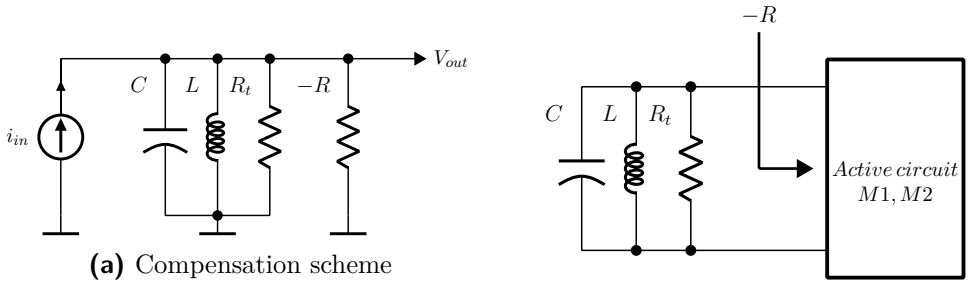
$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

To build-up an oscillation the active g_m has to be larger than g_t, and therefore a continuous amplitude increase is provided. After having reached the steady state amplitude, g_m has to be limited to g_t.

3.1.2 Basic integrated LC circuit

In integrated circuits it is a common approach to use cross-coupled transistor pairs to introduce negative resistance to a system. This is also capable for LC tank circuits, seen in figure 3.4a. The g_m of the behavioural model can be replaced by the negative resistance that compensates the tank losses. g_t is renamed to R_t to make this approach obvious.

The active circuit of figure 3.4b that is used to generate negative resistance is shown in figure 3.5a. Analysing the small signal differential behaviour gives the input resistance r_{in}.



(a) Compensation scheme

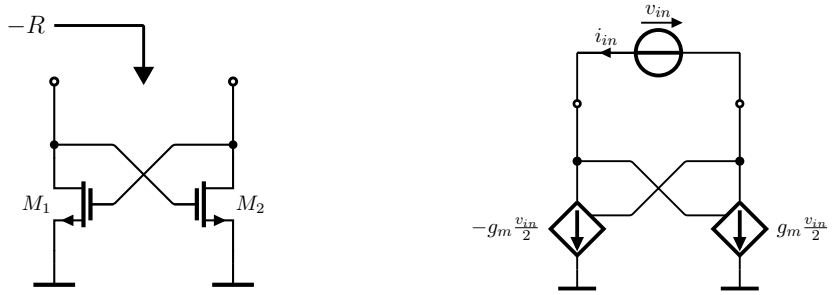
(b) With active circuitry

Figure 3.4: Negative resistance approach

$$r_{in} = \frac{v_{in}}{i_{in}} = \frac{v_{in}}{-g_m \frac{v_{in}}{2} - g_m \frac{v_{in}}{2}} = -\frac{2}{g_m}$$

with the same transconductance g_m for both devices

$$g_{m1} = g_{m2} = g_m$$



(a) Cross-coupled pair

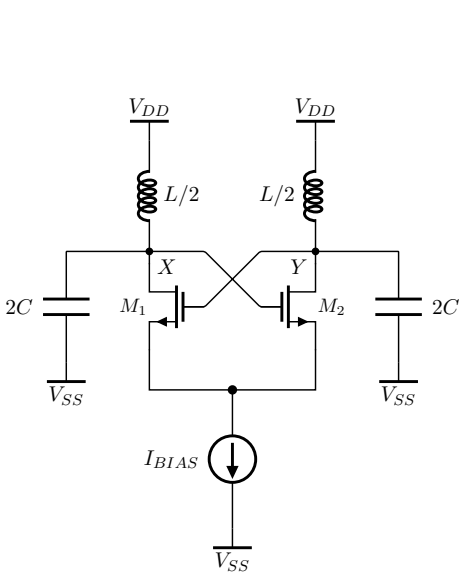
(b) Small signal analysis

Figure 3.5: Active cross coupled pair

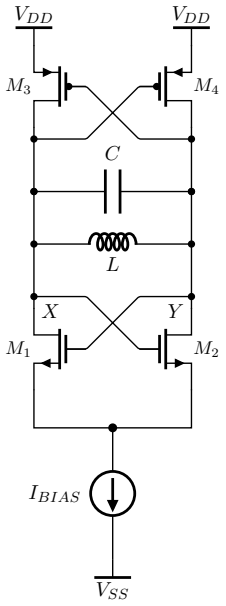
A common circuit known as differential nMOS LC circuit, that forms the core of many integrated LC oscillators is shown in figure 3.6a. This differential structure features two active MOS devices that form a negative resistance between node X and Y, and four passive elements (L and C). It is easy to implement and the output frequency is primarily the resonant frequency of the tank circuit. The complementary version that includes nMOS and pMOS devices can be seen in figure 3.6b. It features two cross-coupled pairs and provides a larger tank amplitude for a given bias current I_{BIAS}, in reference to [Dar15]. The benchmark of different LC structures is shown in table 3.1.

3.1.3 Coupled LC oscillator

By coupling of two differential LC oscillators, shown in figure 3.7, quadrature outputs that are indispensable for RF front-ends are obtained. Two differential



(a) Differential nMOS LC oscillator



(b) Differential complementary LC oscillator

Figure 3.6: Differential LC circuits

pairs are introduced, [OFF+08], acting as soft-limiter. They sense the output voltages at node $N1$, $N2$, $N3$ and $N4$, convert it to a current and trigger the opposite oscillator. After synchronization there is a 90° phase shift between the differential output signals, V_{out1} and V_{out2}. This can be seen in figure 3.8. The phase shift is only obtained if there is a strong coupling between the LC structures and this leads to increased gate sizes ($M5$, $M6$, $M7$, $M8$) and therefore also increased parasitics. Hence, accurate matching of circuit elements is required and the noise performance is degraded compared to a single differential LC oscillator.

The transfer function of the loop $L(s)$ can be calculated by using the linear model, depicted in figure 3.9 and taken from [OFF+08]. The corresponding impedance $Z(s)$ of a single LC oscillator and the transconductance g_{mc} of the coupling circuit gives the overall transfer function. The negative sign is due to the 180° phase shift caused by the cross coupled connection.

$$L(s) = A(s)\,F(s) = -\left(g_{mc} \cdot Z(s)\right)^2$$

with

$$Z(s) = \frac{1}{\frac{1}{sL} + sC + g_t - g_m} = \frac{sL}{1 + sL\left(g_t - g_m\right) + s^2LC}$$

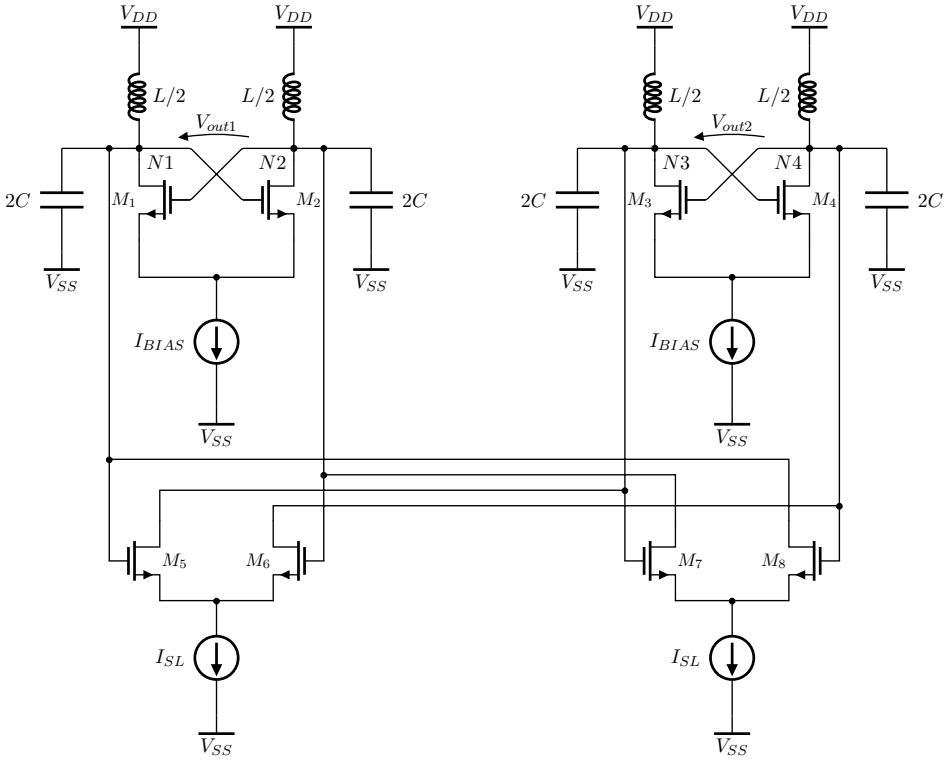


Figure 3.7: LC based coupled oscillator

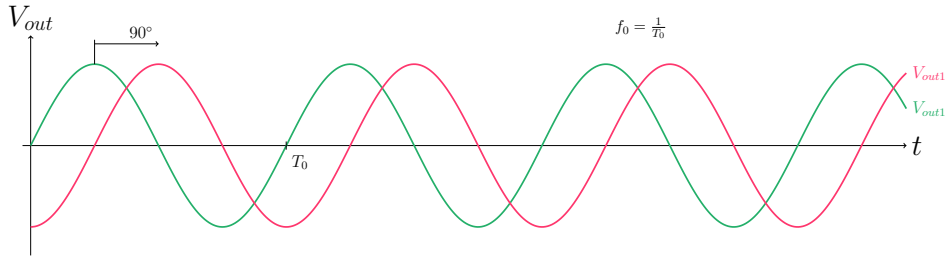


Figure 3.8: Output waveforms coupled LC oscillator

Applying Barkhausen's criterion gives:

$$A(s)\,F(s) = 1$$

$$g_t = g_m$$

with

$$s \to j\omega$$

gives

$$\pm 1 = \frac{g_{mc}\omega L}{1 - \omega^2 LC}$$

To compare the frequency of the coupled LC circuit ω with that of a single differential LC oscillator ω_0, the basic formula $\omega_0 = \frac{1}{\sqrt{LC}}$ is appended. This gives two possible solutions.

$$\omega_{1/2} = \pm\frac{g_{mc}}{2C} + \omega_0\sqrt{1 + L\frac{g_{mc}^2}{4C}}$$

with the following term much smaller than one

$$L\frac{g_{mc}^2}{4C} \ll 1$$

gives the frequency ω

$$\omega_{1/2} \approx \omega_0 \pm \frac{g_{mc}}{2C}$$

It can be seen that the frequency, by coupling of two integrated LC oscillators, is shifted and it can lock either to a higher or lower frequency. Please note that higher coupling leads to higher frequency shift.

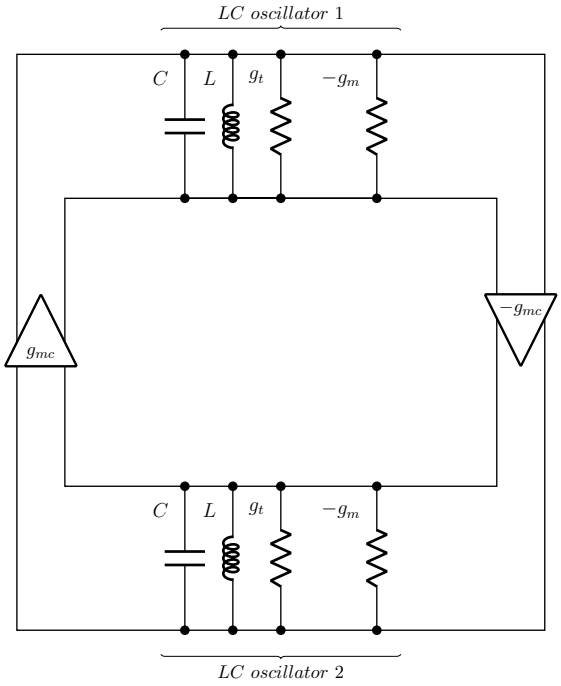


Figure 3.9: Linear model coupled LC oscillator

3.1.4 Colpitts oscillator

Single-ended Colpitts oscillators are seen in figure 3.10a. In comparison to cross-coupled LC oscillators they have good cyclostationary noise properties, [HL99, AH02], and achieve higher voltage swing for a given bias current

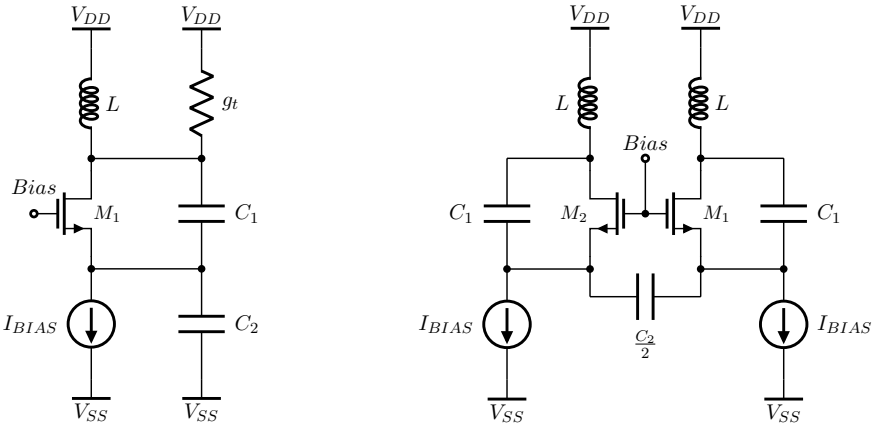
Topology	Diff. amplitude	Efficiency	Noise factor **
n/pMOS LC	$\frac{2}{\pi}\frac{I_{BIAS}}{g_t}$	$\frac{1}{\pi}\frac{A}{V_{DD}}$	$1+\gamma+\gamma\frac{1}{4}\frac{\pi A}{V_{eff}}$
CMOS LC	$\frac{4}{\pi}\frac{I_{BIAS}}{g_t}$	$\frac{2}{\pi}\frac{A}{V_{DD}}$	$1+\gamma+\gamma\frac{\pi A}{V_{eff}}$
Colpitts LC *	$2\frac{C_2}{C_1+C_2}\frac{I_{BIAS}}{g_t}$	$\frac{C_2}{C_1+C_2}\frac{A}{V_{DD}}$	$1+\gamma\frac{C_2}{C_1}+\gamma\left(\frac{C_1}{C_1+C_2}\right)^2\frac{\pi A}{V_{eff}}$

* Please note that a single-ended Colpitts structure is considered.
** V_{eff} - effective voltage of current source, γ - noise coefficient

Table 3.1: Benchmark LC structures

I_{BIAS} and resonator (L, C, g_t). The voltage amplitudes A within the tank, efficiency and noise factor taken from [Dar15] are shown in table 3.1.

If the capacitance C_1 is designed to be greater than C_2, a noise factor less than that of the standard differential LC topologies can be achieved. This on the other hand decreases the efficiency and as shown in [AWVF05], the FoM of Colpitts oscillators is always less compared to standard LC structures. Please consider that the tank losses modeled by g_t are only shown for the single-ended structure in figure 3.10a.

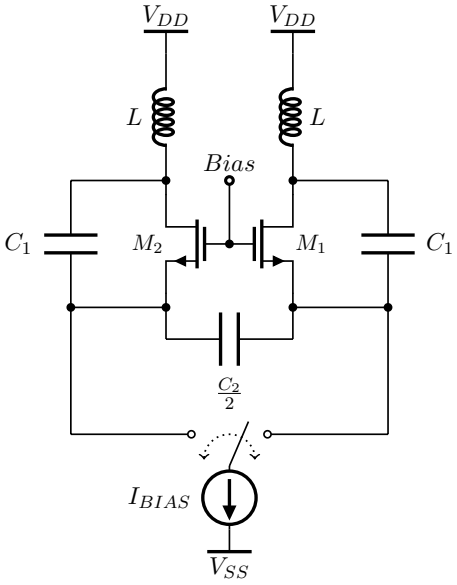


(a) Single ended Colpitts structure **(b)** Differential Colpitts structure

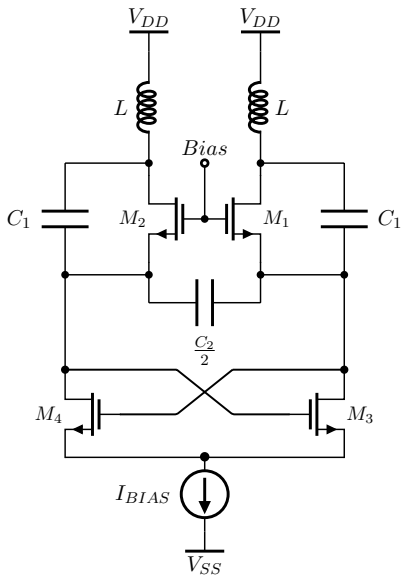
Figure 3.10: Basic Colpitts structures

As single-ended Colpitts circuits require higher gains to start-up and have the typical disadvantages of single-ended structures, implying noise sensitivity, they are rarely used within integrated RF circuits. A differential Colpitts structure as seen in figure 3.10b is able to overcome this issues, but also increases the power consumption as two currents I_{BIAS} are used for biasing. However, current flows less than half of the period through one branch and therefore it is possible to reuse it, leading to another improved Colpitts structure that is depicted in figure 3.11a. To ensure synchronized current switching [AH02] has introduced a tail cross-coupled pair that is shown in figure 3.11b. Another advantage of this circuits is the improved start-up

condition as the small-signal loop gain increases.



(a) Differential switched Colpitts structure



(b) Differential switched Colpitts circuitry

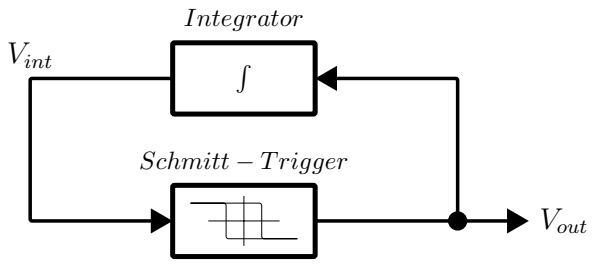
Figure 3.11: Advanced Colpitts structures

3.2 RC based oscillators

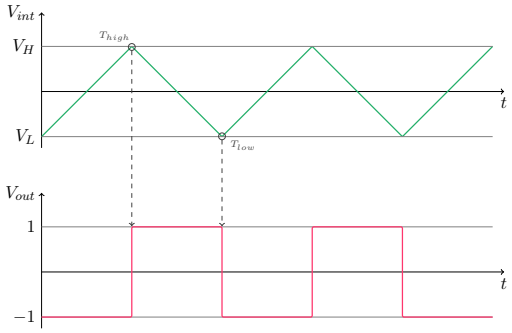
RC oscillators are most of the time designed to act as non-linear systems and are therefore often called Relaxation Oscillators. They are generally used for output frequencies up to several tenths of MHz, or higher if phase-noise requirements are relaxed. Typically as part of a phase-locked loop. As already mentioned for high frequency, low noise applications linear LC circuits, discussed in section 3.1, are superior and should be used if monolithic inductors are available within the process. Anyway, also RC oscillators can be designed to be linear. [OFF+08] gives detailed information about relaxation oscillators and advanced structures discussed in section 3.2.4 and 3.2.5.

3.2.1 Behavioral model

The non-linear behaviour of RC oscillators can be modeled as shown in figure 3.12a. It consists out of a Schmitt-trigger that is used as memory element and an integrator. The output of the Schmitt-trigger V_{out} is fed to the input of the integrator and therefore switches the sign of the integration constant by reaching it's thresholds. The output V_{int} of the integrator is again the input of the Schmitt-trigger which leads to a closed loop system. Hence, the output signal V_{out} is a squarewave and the output signal of the integrator V_{int} is triangular shaped, shown in figure 3.12b. The frequency and duty cycle of the output signal depends on the threshold voltages of the Schmitt-trigger and the integration constant.



(a) Behavioural model non-linear RC oscillator

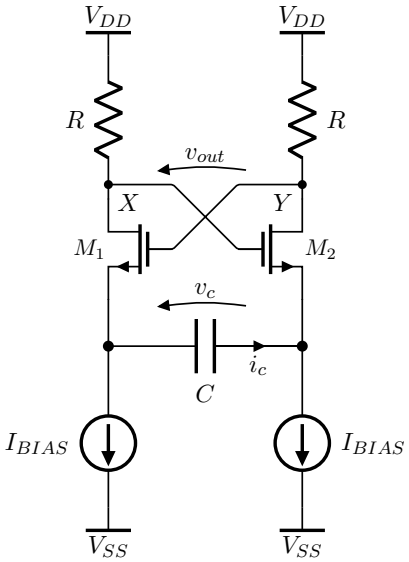


(b) Waveforms behavioural model

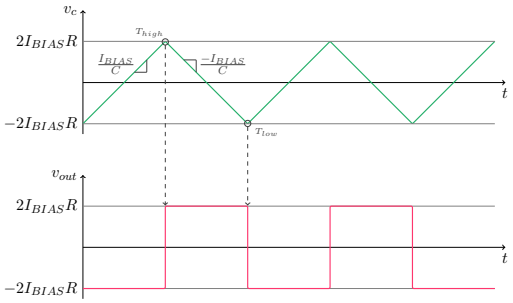
Figure 3.12: Non-linear RC oscillator model

3.2.2 Basic integrated RC circuit

Figure 3.13a shows a common implementation of differential RC oscillators. Due to it's simplicity that circuit is capable of high frequency operation as it implies few parasitics and noise sources.



(a) Differential RC oscillator circuit



(b) Waveforms differential RC oscillator

Figure 3.13: Differential RC oscillator

Corresponding to the behavioural model, discussed in section 3.2.1, the integrator is formed, as simple as it is, by a capacitance C. The Schmitt-trigger is shown in figure 3.14a. The output of the Schmitt-trigger is the current i_c and the input is the voltage v_c, with figure 3.14b showing it's transfer characteristics. To understand the relaxation behaviour of the circuitry in figure 3.13a, it is assumed that the switching between the two states occurs when the sign of the voltage difference $V_{GS1} - V_{GS2}$ changes. Considering that M_1 is in the cut-off region as initial state, given that $V_{GS1} < 0$, the current i_1 is equal to zero and i_2 is equal to $2I_{BIAS}$. Therefore, X is equal to the supply voltage V_{DD} and Y is $V_{DD} - 2RI_{BIAS}$. Implying that i_c is equal to $-I_{BIAS}$ and therefore the capacitor voltage v_c between the sources of M_1 and M_2 decreases constant with the rate of $\frac{I_{BIAS}}{C}$. Hence, the switching condition can be defined as follows.

$$V_{GS1} - V_{GS2} = 0$$

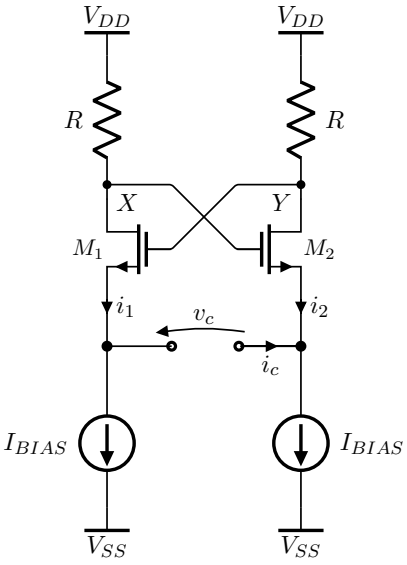
Therefore, the capacitor voltage v_c is given by:

$$v_c = Y - X$$

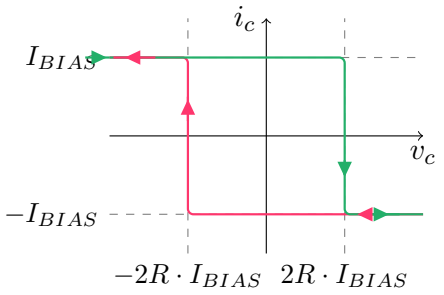
And this gives depending on the initial state:

$$v_c = \pm 2RI_{BIAS}$$

Whenever v_c reaches $-2RI_{BIAS}$ the state switches and M_2 gets into the cut-off region. i_c is equal to I_{BIAS}, X is equal to $V_{DD} - 2RI_{BIAS}$, Y is equal to V_{DD} and the capacitor voltage v_c increases constant with the rate of $\frac{I_{BIAS}}{C}$ till it reaches $2RI_{BIAS}$, and the circuit switches back to the first state.



(a) Schmitt-trigger circuit



(b) Schmitt-trigger characteristic

Figure 3.14: Schmitt-trigger differential RC oscillator

The differential output current of the Schmitt-trigger ic is transferred into a differential output voltage v_{out}.

$$v_{out} = -2R \cdot i_c$$

And therefore, the amplitude of the output signal v_{out} is $\pm 2RI_{BIAS}$. The waveforms of this very basic differential RC oscillator are shown in figure 3.13b. Thus, the output frequency f_0 can be defined as:

$$f_0 = \frac{I_{BIAS}}{2C(4RI_{BIAS})} = \frac{1}{8RC}$$

However, this circuit only behaves non-linear for low output frequencies. If the design implies a higher output frequency, the output signal gets sinusoidal (with decreased amplitude) which leads to linear behaviour. It has been assumed that there is a rapid transition between the cut-off and saturation region when $V_{GS1} - V_{GS2}$ changes the sign. But it has to be said that noise is introduced, as there is a certain period of time where these transistors operate within the triode region.

3.2.3 Linear and non-linear behaviour

If high frequency operation is desired, the influence of parasitics increases. As C decreases, the input of the Schmitt-trigger is loaded by the parasitic capacitances C_{gs1} and C_{gs2}. This causes an inductor equivalent behaviour, [Lop10, Dia09]. Similar to LC oscillators the imaginary part of the inductor and the capacitor impedance cancel each other to form a resonator. This leads to a linear system, with sinusoidal output waveforms, where Barkhausen's criterion can be applied. Figure 3.15a shows the linear model of the Schmitt-trigger with it's input impedance z_{in}. As the transistors form a cross-coupled pair their gate-to-source capacitances are equal and therefore $C_{gs} = C_{gs1} = C_{gs2}$. With $G = \frac{1}{R}$, this gives an input impedance of:

$$z_{in} = \frac{g_{m1} + g_{m2}}{g_{m1} g_{m2}} \cdot \frac{G + sC_{gs}}{G} - \frac{2}{G}.$$

If the integration capacitance C is included, the characteristic equation can be obtained as:

$$z_{in} + \frac{1}{sC} = 0.$$

And this gives the equation:

$$s^2 + s\left[\frac{1}{RC_{gs}}\left(1 - 2R\frac{g_{m1}g_{m2}}{g_{m1} + g_{m2}}\right)\right] + \frac{g_{m1}g_{m2}}{C_{gs}RC(g_{m1} + g_{m2})} = 0.$$

To simplify the term, it is assumed that $g_m = g_{m1} = g_{m2}$ as it can be considered that an equal current flows in both branches whenever the oscillation starts. Therefore, the equation can be rewritten.

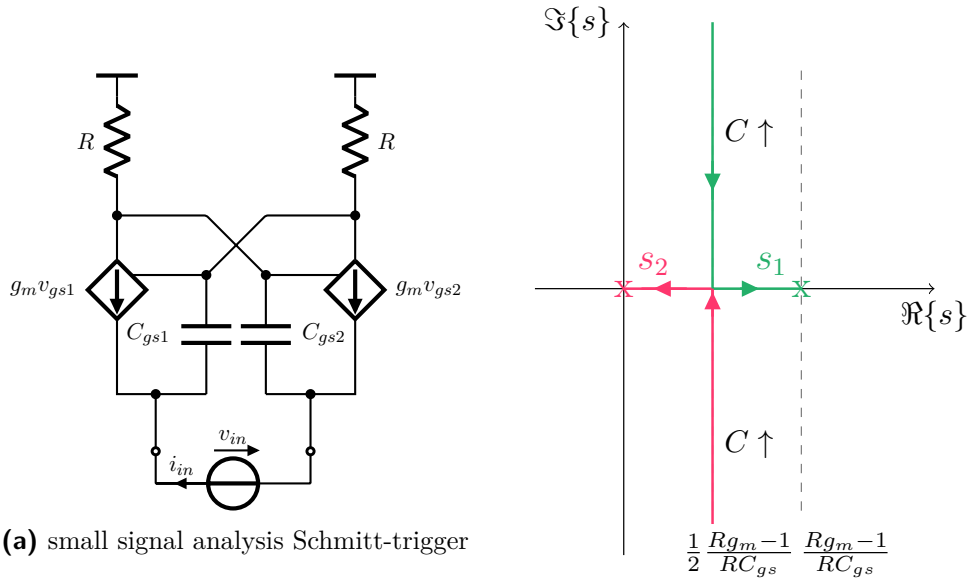
$$s^2 + s\left(\frac{1 - Rg_m}{RC_{gs}}\right) + \frac{g_m}{2C_{gs}RC} = 0$$

To analyze the damping factor ζ and the oscillation frequency ω_0 of this system, the roots are analysed.

$$s_{1/2} = \frac{Rg_m - 1}{2RC_{gs}} \pm \frac{\sqrt{(Rg_m - 1)^2 - \frac{2RC_{gs}g_m}{C}}}{2RC_{gs}}$$

With the roots $\lambda_1 = 1 - Rg_m$, $\lambda_2 = \frac{g_m}{2C}$ and $\lambda_3 = RC_{gs}$ the equation for the damping factor ζ and the oscillation frequency ω_0 can be written as follows.

$$\omega_0 = \sqrt{\frac{\lambda_2}{\lambda_3}} = \sqrt{\frac{g_m}{2CRC_{gs}}}$$



(a) small signal analysis Schmitt-trigger

(b) s-plane movement

Figure 3.15: Schmitt trigger - analysis

$$\zeta = \frac{\lambda_1}{2\sqrt{\lambda_2\lambda_3}} = \frac{1 - Rg_m}{2\sqrt{\frac{g_m RC_{gs}}{2C}}}$$

The oscillation starts with the frequency ω_0 when the damping factor ζ has a negative sign. Therefore $1 - Rg_m$ must be smaller than zero, or $g_m > \frac{1}{R}$. By variation of the capacitance C the system starts to change it's behaviour. For small values of C there are conjugate complex roots that implies linear action. By increase of C, the poles move towards to the real axis as the imaginary part decreases. They arrive at the real axis when $(1 - Rg_m)^2 - \frac{2RC_{gs}g_m}{C} = 0$, or $C = \frac{2RC_{gs}g_m}{(1-Rg_m)^2}$ applies. At this point the system starts to get non-linear. If C further increases the roots are moving along the real axis, one in the left and one in the right direction. The final positions are $s_1 = 0$ and $s_2 = \frac{Rg_m-1}{RC_g s}$. Figure 3.15b shows the corresponding s-plane and the pole movement. The transition between the linear and non-linear behaviour is smooth. The harmonic content increases gradually and the sinusoidal wave gets distorted more and more. At the end the system oscillates in relaxation mode with squarewave output signals.

To get the amplitude of the output signal, the differential equation of the linear system has to be defined. As the term $\frac{g_{m1}g_{m2}}{g_{m1}+g_{m2}}$ varies with respect to the capacitor current i_c, following approximation can be made:

$$\frac{g_{m1}g_{m2}}{g_{m1} + g_{m2}} \approx \frac{g_m}{2}\left[1 - \left(\frac{i_c}{I_{BIAS}\sqrt{2}}\right)^2\right].$$

Therefore, the differential equation can be written as follows.

$$\frac{d^2}{dt^2} + \frac{d}{dt}\left[\frac{1}{RC_{gs}}\left(1 - Rg_m\left(1 - \left(\frac{i_c}{I_{BIAS}\sqrt{2}}\right)^2\right)\right)\right] + \omega_0^2 i_c = 0$$

By introduction of the normalized variable $n = \frac{i_c}{I_{BIAS}\sqrt{2}}$ and notations $\lambda_4 = \frac{Rg_m - 1}{2RC_{gs}}$, $\lambda_5 = \frac{g_m}{2C_{gs}}$ the simplified version of the differential equation is given by the equation below.

$$\frac{d^2 n}{dt^2} - \frac{dn}{dt} 2\left(\lambda_4 - \lambda_5 n^2\right) + \omega_0^2 n = 0$$

The corresponding solution can be written.

$$n = 2\sqrt{\frac{\lambda_4}{\lambda_5}}\sin(\omega_0 t)$$

With the current to voltage relation, the output voltage v_{out} can be shown to be:

$$v_{out} = 4\sqrt{2} I_{BIAS} R\sqrt{\frac{\lambda_4}{\lambda_5}}\sin(\omega_0 t) = 4 I_{BIAS} R\sqrt{2}\sqrt{1 - \frac{1}{Rg_m}}\sin(\omega_0 t).$$

Table 3.2 gives a short summary concerning linear and non-linear behaviour of differential RC oscillators.

Mode	Diff. amplitude	Frequency	Waveform
harmonic	$4RI_{BIAS}\sqrt{2}\sqrt{1 - \frac{1}{Rg_m}}$	$\frac{1}{2\pi}\sqrt{\frac{g_m}{2CRC_{gs}}}$	sinusoidal
relaxation	$4RI_{BIAS}$	$\frac{1}{8RC}$	square

Table 3.2: Summary linear vs non-linear behaviour of RC oscillators

3.2.4 Coupled RC oscillator

As already discussed in section 3.1.3, oscillators can be coupled to get quadrature output signals. This also applies to differential RC oscillators, [OFF+08]. They are coupled via limiters and provide 90° phase shifted squarewave signals at their outputs. A squarewave output signal can only appear if the limiters have sufficient gain. Unlike Schmitt-triggers, limiters start to saturate if the triangular shaped input, provided by the integrator, crosses zero. With this technique an open loop structure itself could provide a 90° shifted square wave signal. However, there is an error introduced as the output signals have different paths. In coupled RC oscillators the outputs of the limiters are used to synchronize two oscillators, shown in figure 3.16. The signal of the opposite limiter is added to the integrators output and therefore the output

signals V_{out1} and V_{out2} have always 90° phase shift and the same output frequency. This structure leads to a cross-coupled relaxation oscillator in a feedback structure. The waveforms of this system are shown in figure 3.17. This structure is less noise sensitive as the state transition is defined by steep slopes of V_1 and V_2, rather than the gradually variation of the integrator's output. The outputs of the limiters with their corresponding inputs can be seen as V_{int1}, V_{lim1} and V_{int2}, V_{lim2}. Their gain defines the steepness of the slope.

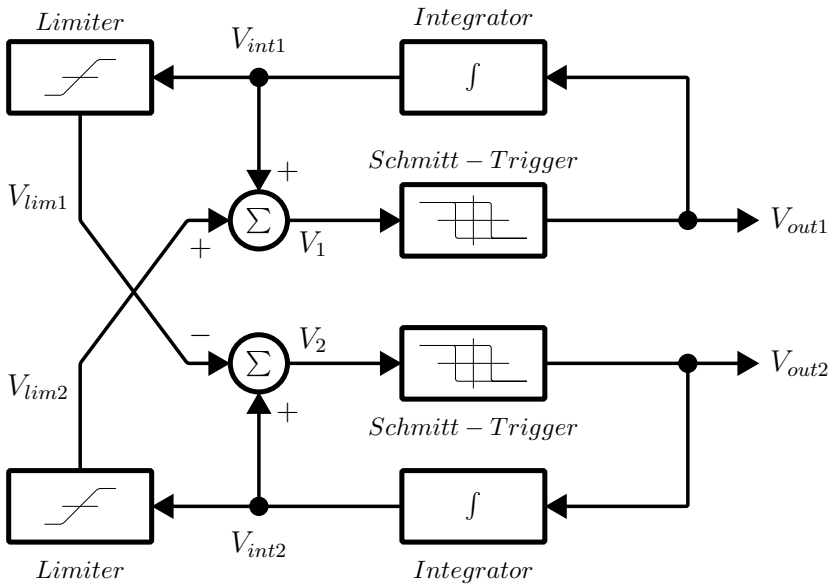


Figure 3.16: Behavioural model of coupled RC oscillator

Different to coupled LC oscillators the output frequency is not changed by coupling of two differential RC oscillators in relaxation mode. If they are designed to operate within the harmonic mode the output frequency is affected, similar to LC structures. The limiters can be implemented as differential pair, depicted in figure 3.18. The circuit is studied as two relaxation oscillators that are coupled via two additional current sources I_L. The currents i_{L1}, i_{L2}, i_{L3} and i_{L4}, controlled by v_{c1} and v_{c2}, are provided by the limiters and trigger the opposite RC oscillator synchronously. Thus, one of the differential pairs has to be cross coupled, leading to the negative sign at the summing point in figure 3.16. Assuming that switching between the states occurs instantly the circuit can be analysed in a simple way. As the system is symmetric, the analysis is only done for one output voltage v_{out1} with an initial state, that considers M_1 as turned off and M_2 as fully conductive. In this state the potential at X_1 is $V_{DD} - i_{L1}R$ and at Y_1 it is $V_{DD} - 2I_{BIAS}R - i_{L1}R$. As $i_{L1} + i_{L2} = I_L$, this gives a state dependent output voltage of:

$$v_{out1}, v_{out2} = \pm 2 \left(I_{BIAS} + \frac{I_L}{2} \right) R$$

The switching point is determined the same way as for the basic RC circuit.

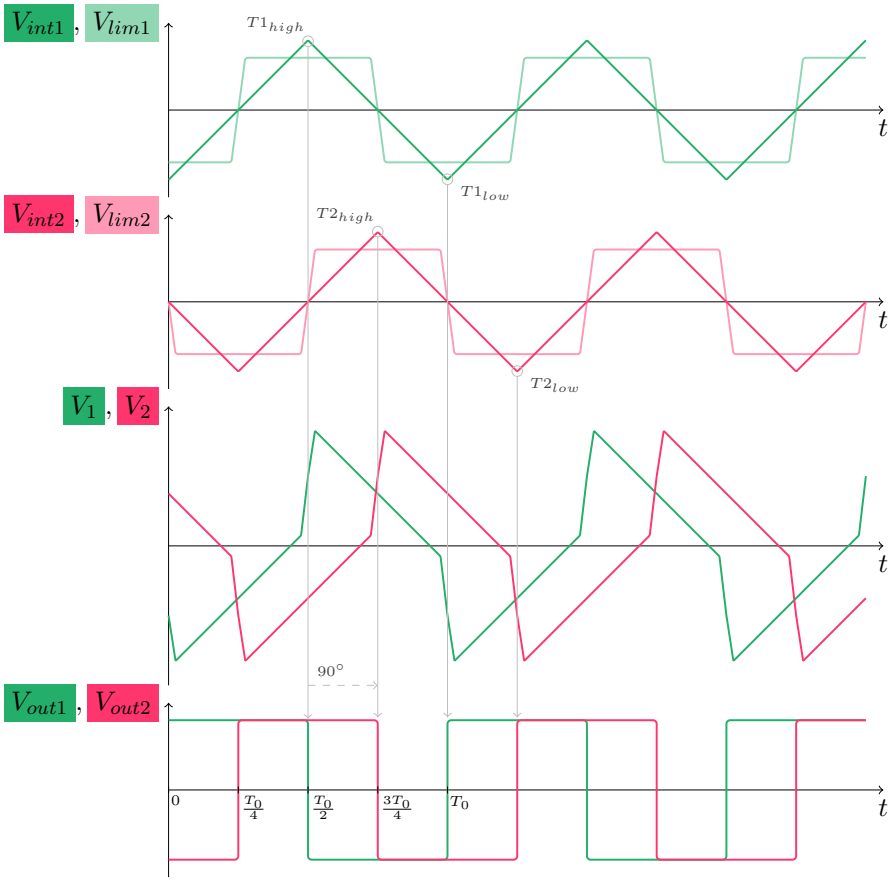


Figure 3.17: Waveforms of coupled RC oscillator model

$$v_{c1}, v_{c2} = \pm 2 I_{BIAS} R - (i_{L2} - i_{L1})\, R$$

Since switching occurs with small values of $(i_{L2} - i_{L1})\, R$ the maximum values of the capacitor voltages v_{c1} and v_{c2} are:

$$v_{c1}, v_{c2} = \pm 2 I_{BIAS} R.$$

The waveforms of the coupled RC oscillator are shown in figure 3.19. The four operating phases are:

1. M_1 on, M_3 on, v_{c1} increases, v_{c2} increases
2. M_1 off, M_3 on, v_{c1} decreases, v_{c2} increases
3. M_1 off, M_3 off, v_{c1} decreases, v_{c2} decreases
4. M_1 on, M_3 off, v_{c1} increases, v_{c2} decreases

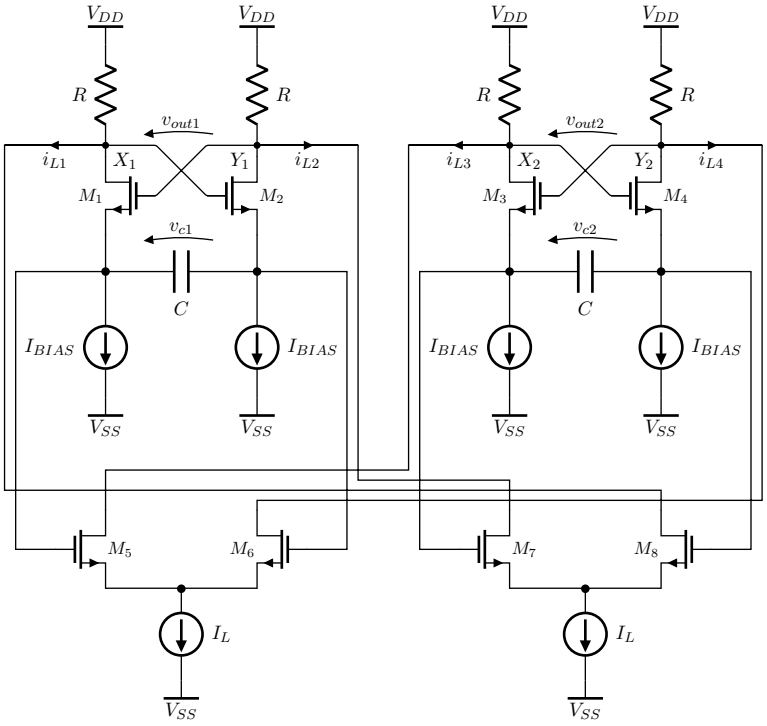


Figure 3.18: Coupled RC oscillator circuit

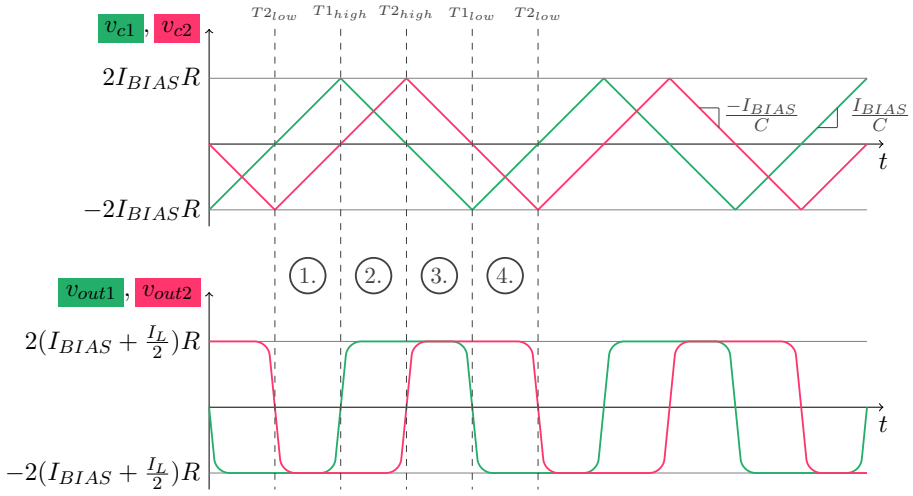


Figure 3.19: Waveforms of coupled RC oscillator circuit

Whenever the capacitor voltage v_{c1} or v_{c2} changes the polarity, one of the output voltages is forced to change it's state, seen in figure 3.19.

The coupled RC structure is not capable of having low power consumption as a certain supply voltage is needed to ensure correct operation. To overcome this issue new coupling techniques have been developed. One approach is capacitive coupling that leads to lower power consumption as well as better noise performance.

However, this structures have been widely accepted and became the subject of many studies, due to the fact that it consumes low area, has good performance and provides quadrature squarewave output signals.

Comparison coupled oscillator structures

For low noise applications coupled LC oscillators may be still preferred but on the cost of area and the need of monolithic inductors. In [OFF+08] one coupled linear RC and one LC oscillator were designed, having the same output frequency ($5GHz$), supply voltage and process. Table 3.3 summarizes the measured results.

Structure/Coupling*	Phase-noise**	Quadrat. Error	Area factor
LC/strong	$-96\ dBc/Hz$	1.5°	x7.7
LC/weak	$-101\ dBc/Hz$	3.5°	x7.7
RC/strong	$-97\ dBc/Hz$	1°	x1
RC/weak	$-87\ dBc/Hz$	2.7°	x1

* Strong coupling: $I_L = 6mA$, Weak coupling: $I_L = 1mA$
** @$1MHz$

Table 3.3: Benchmark coupled oscillators

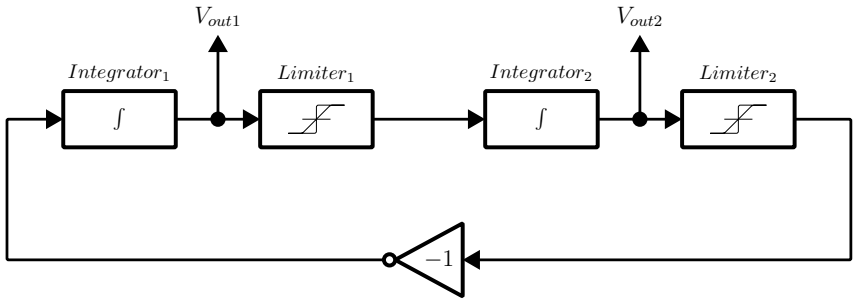
Generally, RC oscillators, designed for high frequency applications, are known for their poor phase-noise performance if compared to LC oscillators. This is true for single oscillator structures, but not for coupled oscillator structures.

3.2.5 Two integrator oscillator

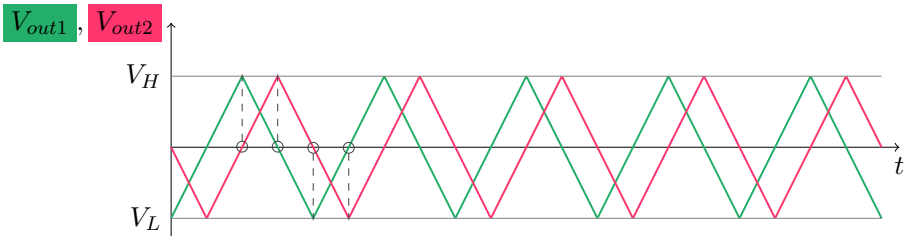
An uncoupled oscillator that generates inherent quadrature outputs, seen in figure 3.20b and 3.20c, is known as the two integrator oscillator. It has two integrators in a feedback structure and is capable of high oscillation frequencies and a wider tuning range compared to other RC oscillators. Depending on the behaviour of the limiters, the oscillator is designed to act as a non-linear (triangular shaped outputs) or linear system, [OFF+08]. The behavioural model is shown in figure 3.20a.

Non-linear behaviour

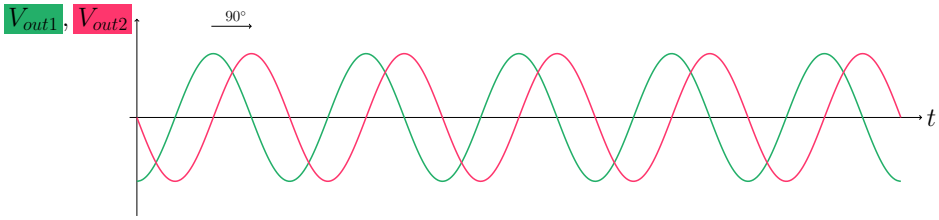
If a two integration oscillator is designed to be in relaxation mode, the limiters act like saturated amplifiers and are called hard limiters. Thus, the output of the limiters give square waveforms and change their sign when their input crosses zero. Looking at the closed loop behaviour, this implies that each integrator output determines the input polarity of the other integrator. This can be seen in figure 3.20b. The frequency of the output is dependent on the initial states of the integrator outputs $V_{out1}(0)$, $V_{out2}(0)$ and the integration constants K_{i1}, K_{i2}. For $K_{i1} = K_{i2} = K_i$ the output frequency f_0 can be written as follows.



(a) Behavioural model of two integrator oscillator



(b) Waveforms: non-linear behaviour - same integration constants



(c) Waveforms: linear behavior - same integration constants

Figure 3.20: Two integrator oscillator model

$$f_0 = \frac{K_i}{2\left(V_{out1}(0) + V_{out2}(0)\right)}$$

And for $K_{i1} \neq K_{i2}$:

$$f_0 = \frac{1}{4\left(\frac{V_{out1}(0)}{K_{i1}} + \frac{V_{out2}(0)}{K_{i2}}\right)}.$$

Linear behaviour

For linear behaviour the amplifiers act as soft limiters and operate in their linear region. The sinusoidal outputs, depicted in figure 3.20c, are not saturating these limiters and therefore better noise performance is achieved. Hence, this approach is superior for high frequency designs. Also to be said, hard limiters for high frequencies are difficult to design. The loop function can be written as:

$$L(s) = \frac{K_1 K_2}{s^2}.$$

The gain factor K_1 belongs to System 1 while K_2 belongs to System 2, seen in figure 3.20a. By applying Barkhausen's criterion, setting the loop transfer $L(s) = 1$, the output frequency ω_0 can be defined as

$$\omega_0 = \sqrt{K_1 K_2}.$$

Circuit implementation

For this structure the integrators are implemented as differential pairs. The devices M_D interact with the capacitors C as seen in figure 3.21. The cross coupled pairs, provided by the devices M_L, are included to compensate the resistance related losses of R as well as to provide an amplitude limitation mechanism. The amplitudes of the output signals are controlled by the current I_{Lim}. This circuitry acts corresponding to the behavioural model where an ideal integrator is connected to the limiter. The inverter is realized by a cross coupled connection.

The behaviour of the circuit depends on the operating region of the upper cross coupled differential pair. By increase of the transconductance of the limiters g_{mL} the slope gets steeper, losses are over-compensated, and the circuit gets strongly non-linear. Thus, the oscillator operates in relaxation mode. As $g_{mL} \propto \sqrt{I_{Lim}}$, this current can be used to control the oscillator's behaviour. The differential output current I_{out} as function of the differential input voltage V_{in} is given below.

$$I_{out}(V_{in}) \begin{cases} I_{Lim}, & V_{in} < -\sqrt{\frac{I_{Lim}}{K}} \\ -g_{mL} \cdot V_{in}, & \sqrt{\frac{I_{Lim}}{K}} \geq V_{in} \geq -\sqrt{\frac{I_{Lim}}{K}} \\ -I_{Lim}, & V_{in} > \sqrt{\frac{I_{Lim}}{K}} \end{cases}$$

It can be seen that the maximum output voltage is proportional to I_{Lim} and the linear region increases with the factor of $\sqrt{I_{Lim}}$. This leads to a voltage gain factor ($g_{mL} R_{out}$) that is proportional to $\sqrt{I_{Lim}}$. Hence, by increasing the current, saturation happens earlier.

Non-linear circuit behaviour

With increased current I_{Lim} the system is strongly non-linear and the transistors can be considered to operate as switches. The lower differential pair determines the sign of the differential current i_{c1} or i_{c2} depending on the sign of it's input voltage. As the capacitors C form the integration constants, the output frequency f_0 can be written as follows.

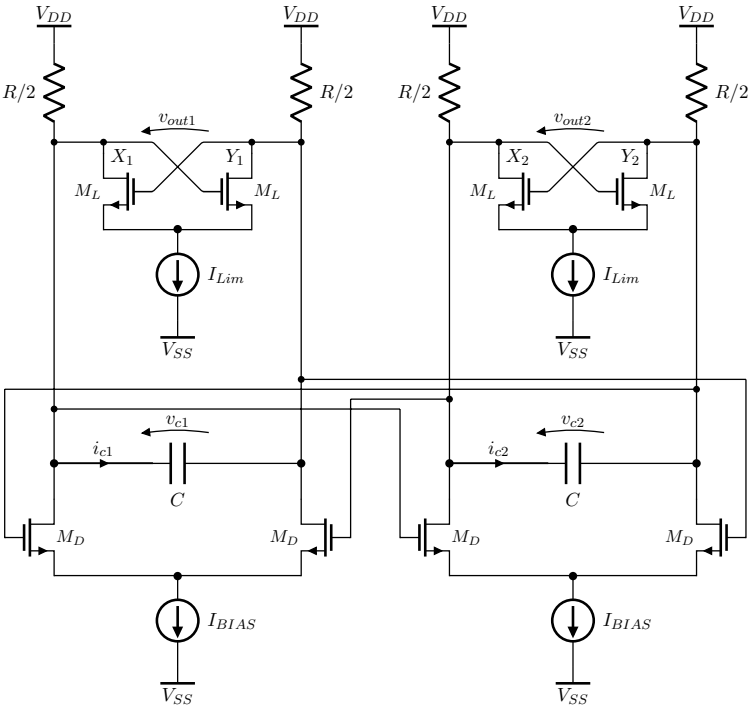


Figure 3.21: Two integrator circuit

$$f_0 = \frac{I_{BIAS}}{2C\left(V_{out1}(0) + V_{out2}(0)\right)}$$

The output voltage V_{out} has approximately a triangular waveform with an amplitude v_{amp}. This amplitude is determined by the current I_{Lim} and R.

$$v_{amp} \approx I_{Lim} R$$

Linear circuit behaviour

If the upper differential pair operates in it's linear region and the losses are not (or only for start-up) overcompensated, sinusoidal output signals can be obtained.

$$\frac{1}{g_{mL}} = R$$

To ensure a stable oscillation, this equation has to be met. 3.22 shows the linear model of the circuit. The loop function $L(s)$ can be defined as follows.

$$L(s) = A(s) F(s) = \frac{-g_{mD}^2}{s^2 C^2}$$

Where g_{mD} is the transconductance of the devices M_D. Applying Barkhausen's criterion, $A(s)\,F(s) = 1$, with $s \to j\omega_0$ gives the output frequency f_0.

$$f_0 = \frac{g_{mD}}{2\pi C}$$

The phase shift of the complete loop is 360° as there is one signal inversion and two 90° phase shifts due to the capacitance C. The output frequency can be either changed by adjusting the transconductance g_{mD}, most likely by changing I_{BIAS}, or the capacitance C. Hence, an advantage of this kind of RC oscillator is the wide tuning range.

The output amplitude of the sinusoidal signal is considered to be less than in relaxation mode, to ensure that the cross coupled differential pair doesn't enter the saturated region.

$$v_{amp} < I_{Lim} R$$

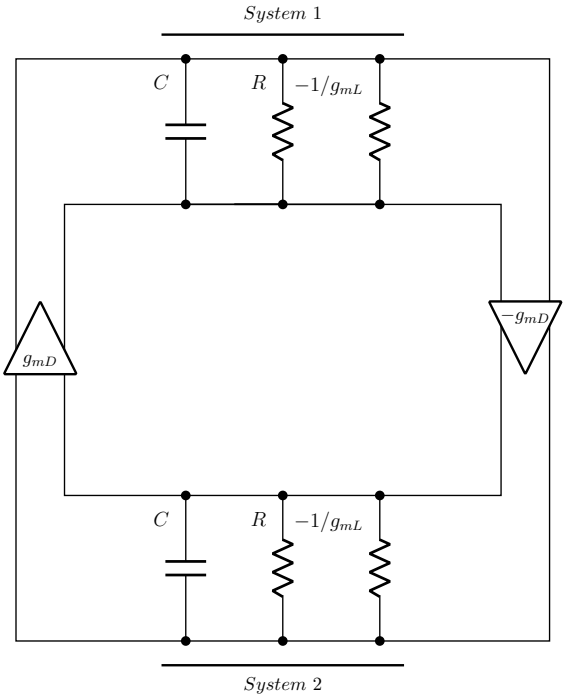


Figure 3.22: Linear model two integrator oscillator

3.2.6 Comparator based RC oscillator

This kind of RC oscillators are widely used for low-power, compact-size and low-frequency applications. They are called RC oscillators as their output frequency mainly depends on an integration constant formed by reference currents and capacitances. Usually a current is defined by a resistance and

therefore the term RC applies. In this section the conventional single- and double comparator structures are discussed.

Double comparator structure

A double comparator circuit, depicted in figure 3.23, is realized by monitoring the voltage of the capacitor V_c that is charged or discharged by a constant current, either I_C or I_D. The voltages V_L and V_H are threshold voltages that cause the two comparators to set or reset the memory element, that is realized by a RS-flip-flop. The output signal V_{out} controls if the capacitor is charged or discharged, by switching between the sourcing and sinking current.

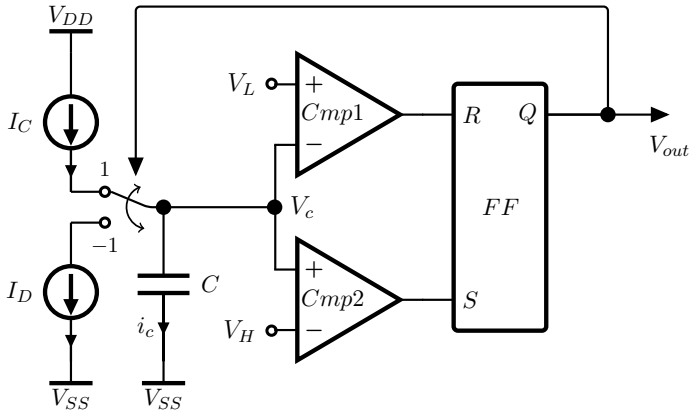


Figure 3.23: Double comparator circuit

Comparing with figure 3.2.1, the Schmitt trigger is realized by the comparators in combination with the flip-flop and the integrator by the current source or sink in combination with the capacitor C. If I_C is equal to I_D, the integrator has equal integration constants for rising and falling slopes, seen in figure 3.24. The oscillation period is therefore:

$$T_0 = \frac{C\,(V_H - V_L)}{I_C} + \frac{C\,(V_H - V_L)}{I_D} + t_{dH} + t_{dL}.$$

t_{dH} and t_{dL} are the delays of the feedback loop formed by the comparators and the flip-flop. If the current source and sink are well matched, $I_C = I_D = I_{ref}$, and the delays are equal, $t_{dH} = t_{dL} = t_d$, the equation can be simplified to:

$$T_0 = \frac{2C\,(V_H - V_L)}{I_{ref}} + 2t_d.$$

If the delay time t_d is designed to be as short as the hold-time of the flip-flop it can be neglected. High quality on-chip capacitors, i.e. MIM[1] capacitors,

[1] Metal Insulator Metal

have low temperature and voltage coefficients. Hence, the overall temperature coefficient is affected by the temperature behaviour of the reference currents and voltages leading to a main design challenge. The duty cycle of the output signal is affected by the current matching ratio $\frac{I_C}{I_D}$.

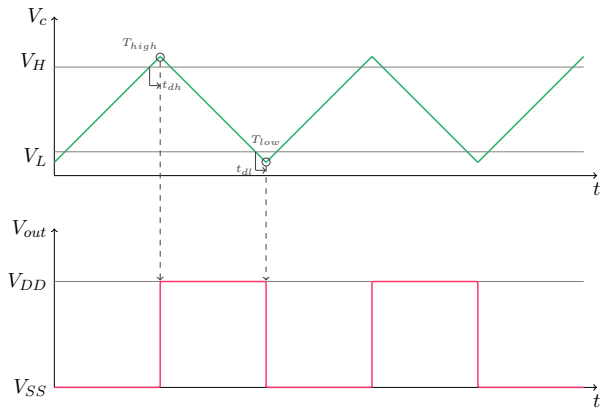


Figure 3.24: Double comparator RO - waveforms

Single comparator structure

The main purpose of this structure, depicted in figure 3.25, is to minimize the power consumption as less circuitry is needed. Instead of changing the sign of the integration constant, the integrator is reset within each clock cycle. There is only one reference current and one reference voltage in use, making this structure, on the face of it, easier to compensate over temperature.

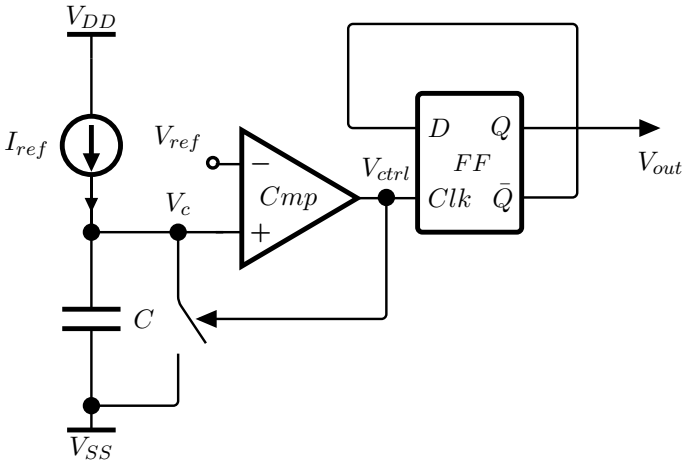


Figure 3.25: Single comparator circuit

The waveforms are shown in figure 3.26 and the oscillation period can be written as follows.

$$T_0 = \frac{2CV_{ref}}{I_{ref}} + 2t_d$$

In this equation t_d is defined as the delay of the comparator summed with the discharging delay of the reset switch, illustrated in figure 3.26. V_{ref} and I_{ref} are the corresponding reference voltage and current. A main drawback of this structure is that it usually creates spikes at the output of the comparator, V_{ctrl}. The spike's pulse width and voltage level V_{spike} is dependent on the delay t_d. As V_{spike} must reach the input referred high-level of the D-flip-flop as well as the threshold voltage of the switch. This structure is not capable to be designed for a low delay t_d. As t_d is sensitive to temperature and process variation, temperature compensation is difficult to achieve. Additional, as V_{ctrl} generally not reaches V_{DD}, this structure is also sensitive to noise and jitter. The D-flip-flop, that also increases the dynamic power consumption, is toggled by V_{ctrl} to create a 50% duty cycle at the output of the oscillator V_{out}.

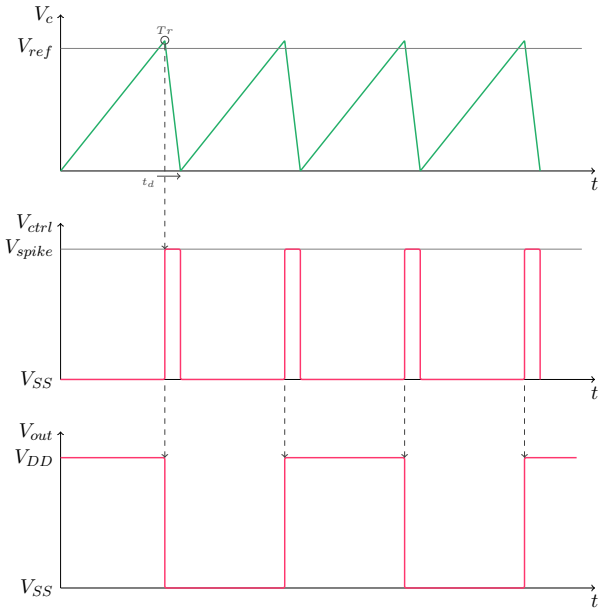


Figure 3.26: Single comparator RO - waveforms

The equation for the oscillator's period reveals the design strategy for temperature compensation. It is about matching the temperature characteristics of I_{ref}, V_{ref} and t_d while considering a capacitor with a low temperature coefficient. [Den10] uses the capacitor characteristics of a MOS transistor to further compensate the overall temperature coefficient and improve the intrinsic gain sensitivity. A ultra low power concept for this structure is obtained by introduction of a current mode comparator. The benefit is that it can share one current branch with the capacitor charging path, [DR15, Den10, Chi14].

3.3 Ring oscillators

This type of oscillators are made from gain or delay stages in a feedback structure. There are many different implementations with very different stage topologies found in the literature. In this thesis inverter based and differential-pair based ring oscillators, as they are commonly used, are discussed.

3.3.1 Behavioural Model

Figure 3.27 shows the behavioural model of ring oscillators with n stages connected to form a ring. Each stage consists of a gain and limiter block. As long as the stages operate in their linear region the limiters can be described as soft-limiters and sinusoidal output signals can be considered. On the other hand, if the stages get pulled out of their linear regions and start to saturate or the signal swing is to high and clipping occurs, the limiters are modeled as hard-limiters that give a squarewave output.

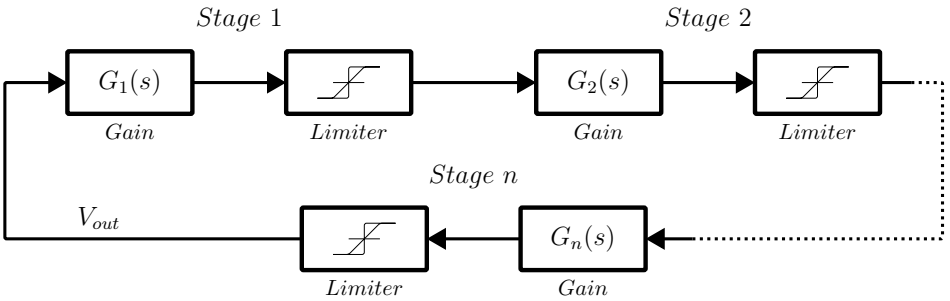


Figure 3.27: Behavioral model ring oscillator

Considering that every stage is identical, which implies same behaviour and therefore the same transfer function $G(s)$, we can analyse the loop function $L(s)$. The transfer function $G(s)$ of a 1 pole gain or amplifier stage loaded with C_L can be described as seen below.

$$G(s) = -\frac{G_0}{1 + \frac{s}{\omega_G}}$$

with

$$G_0 = g_m R_{out}$$

and

$$\omega_G = \frac{1}{R_{out} C_L}$$

Where, G_0 is the low frequency gain, ω_G is the $-3dB$ bandwidth, g_m is the transconductance and R_{out} is the output impedance of the gain stage. Hence,

the overall loop function $L(s)$ for a n-stage ring oscillator can be described as:

$$L(s) = A(s)F(s) = \frac{(-G_0)^n}{\left(1 + \frac{s}{\omega_G}\right)^n}.$$

By considering a negative phase shift per amplifier stage and applying Barkhausen's phase criterion, the frequency ω_0 where the overall loop phase shift is 0° respectively 360° is given by:

$$\omega_0(n) \begin{cases} \omega_G \cdot \tan\left(\frac{180°}{n}\right), & odd\, n \\ \omega_G \cdot \tan\left(\frac{360°}{n}\right), & even\, n \end{cases}$$

Barkhausen's gain criterion with $s \to j\omega_0$ gives:

$$G_0 = \sqrt{1 + \left(\frac{\omega_0}{\omega_G}\right)^2}.$$

By fulfil of both criterion, the required ω_G and G_0 for a specified ω_0 can be calculated. This leads to a fixed R_{out} and g_m of each stage. Please consider that the input impedance of each stage is in parallel with R_{out}. This gives a new impedance $R'_{out} = R_{out}||z_{in}(\omega_0)$ for calculation. As the amplifier stage is a one pole system, they are capable of shifting the phase by −90° but only on a very high frequency where the gain criterion can not be met. Hence, from the phase criterion it can be clearly seen, that for odd n's at least 3 and for even n's at least 6 stages are required. This is true for single ended structures, but not for differential ones because an ideal −180° phase shift can be implemented by a simple cross-coupled connection. One of this differential structures is shown in figure 3.32. If the overall system gain is more than unity there is an steady signal increase leading to a non-linear behaviour. This had been discussed for a 3 stage oscillator in [Raz01]. The transfer function $T(s)$ of the closed loop system is given by:

$$T(s) = \frac{V_{out}}{V_{in}} = \frac{(-G_0)^3}{G_0^3 + \left(1 + \frac{s}{\omega_G}\right)^3}.$$

Splitting the poles of the system gives:

$$G_0^3 + \left(1 + \frac{s}{\omega_G}\right)^3 = \left(1 + \frac{s}{\omega_G} + G_0\right) \cdot \left[\left(1 + \frac{s}{\omega_G}\right)^2 - \left(1 + \frac{s}{\omega_G}\right) G_0 + G_0^2\right].$$

Therefor the 3 poles can be written.

$$s_1 = -\left(1 + G_0\right) \omega_G$$

$$s_{2/3} = \frac{G_0 - 2}{2}\omega_G \pm j\frac{G_0\sqrt{3}}{2}\omega_G$$

Looking at the pole s_1 it can be seen that the imaginary part is zero and this pole leads to an exponential term, $e^{-t(1+G_0)\omega_G}$, if inverse Laplace transferred. As G_0 is positive this term is zero for the steady state oscillation and therefore it gets neglected. The inverse Laplace transformation gives:

$$V_{out}(t) = \mathcal{L}^{-1}\left[\frac{(-G_0)^3}{\left(1+\frac{s}{\omega_G}\right)^2 - \left(1+\frac{s}{\omega_G}\right)G_0 + G_0^2}\right] = \lambda_1 \cdot e^{\lambda_2 t} \cdot \sin(\lambda_3 t)$$

with

$$\lambda_1 = \frac{-2G_0^2}{\sqrt{3}\omega_G}$$

$$\lambda_2 = \Re(s_{2/3}) = \frac{G_0 - 2}{2}\omega_G$$

$$\lambda_3 = \Im(s_{2/3}) = \frac{G_0\sqrt{3}}{2}\omega_G.$$

The phase and gain criterion gives for $n = 3$: $\frac{\omega_0}{\omega_G} = \sqrt{3}$ and $G_0 = 2$. Clearly, it can be seen that the oscillation frequency λ_3 is ω_0 and the exponential term is equal to unity because $\lambda_2 = 0$. Figure 3.28 shows how the output signal V_{out} is affected if the gain factor G_0 is not equal to 2. If it is less than the oscillation stops after a certain time due to the decrease in signal swing. On the other hand, if it is greater than 2 the oscillation sustains and the amplitude increases till it is limited by saturation or clipping. Within this condition the small-signal gain of the closed-loop is greater than unity. However, if the system is saturated the loop gain decreases and the averaged loop gain is still equal to unity. For saturated conditions the gain stages are considered as delay cells and the output frequency is defined as in subsection 3.3.2.

This behaviour can be directly obtained if the equations of the poles are considered. The real part of the conjugated complex poles $s_{2/3}$ is corresponding to the systems damping factor and the imaginary part to it's output frequency. This means if the G_0 doesn't exactly meet the gain criterion, not only the amplitude starts to de- or increase, but also the output frequency starts to deviate. The pole movement can be seen in figure 3.29.

3.3.2 Inverter based ring oscillator

Single ended ring oscillator are commonly implemented by connecting odd numbers of CMOS inverters in a closed loop, illustrated in figure 3.30. These inverters are usually used for digital circuitry and are not considered as typical

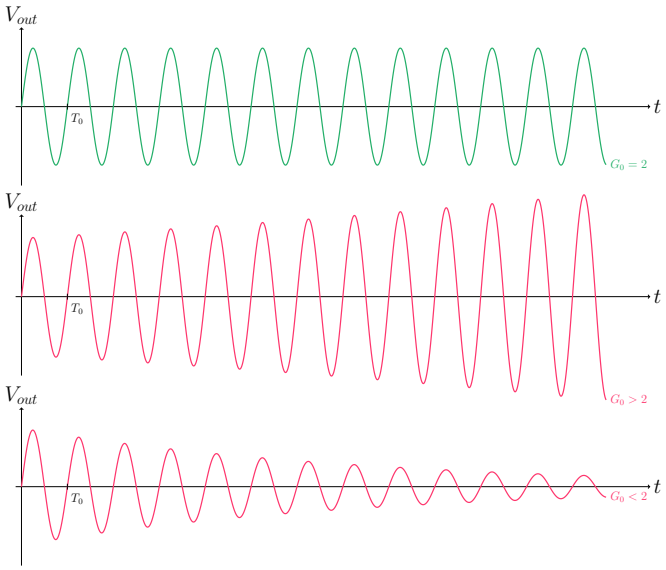


Figure 3.28: Signals behaviour - 3 stage ring oscillator

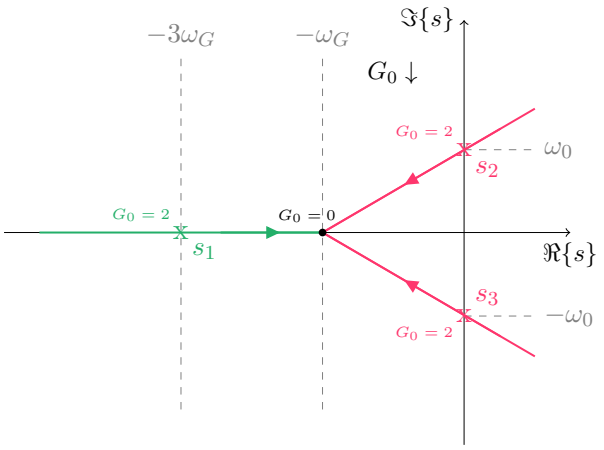


Figure 3.29: Pole movement - 3 stage ring oscillator

one pole gain stages. They are not biased within there linear region, consist out of a nMOS and pMOS device and are capable of rail-to-rail outputs. Typically inverters are described as delay cells in the large-signal regime. After a signal change on an inverter's input the corresponding output state appears one propagation delay t_p delayed. Hence, the output frequency f_0 for n stages in the large-signal regime can be defined as seen below.

$$f_0 = \frac{1}{2nt_p}$$

It has to be said that the inverse Laplace transformation can't be applied to calculate the steady state output frequency, as this system is non-linear

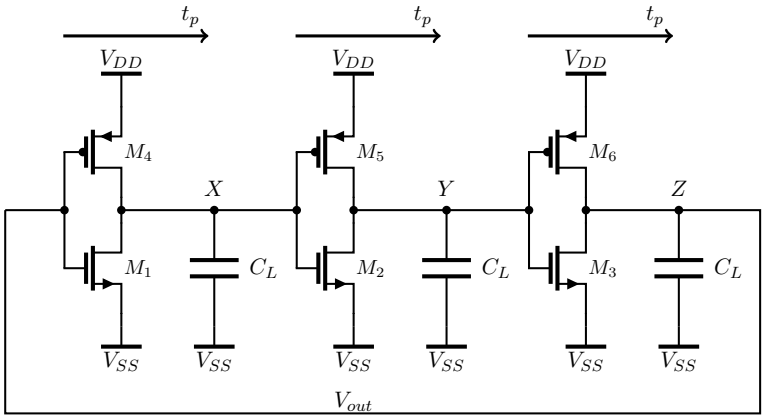


Figure 3.30: Inverter based ring oscillator

and the inverter's gain is a function of the input voltage. They only provide gain during state transition. The gain G_0 and V_{out} vs the input voltage V_{in} can be seen in figure 3.31. For low input voltages the nMOS device is in the cutoff region and the pMOS in triode region. As the input voltage increases the nMOS gets into the saturation region if the threshold voltage V_{Tn} is reached. Further increase leads to a steep slope and the inverter is forced into it's linear region as both MOS devices are saturated. The gain increases with a peak at mid voltage V_M, with $V_{out} = V_{in}$. Near to the voltage $V_{DD} + V_{Tp}$ the nMOS is forced to the triode region and beyond the pMOS cuts off.

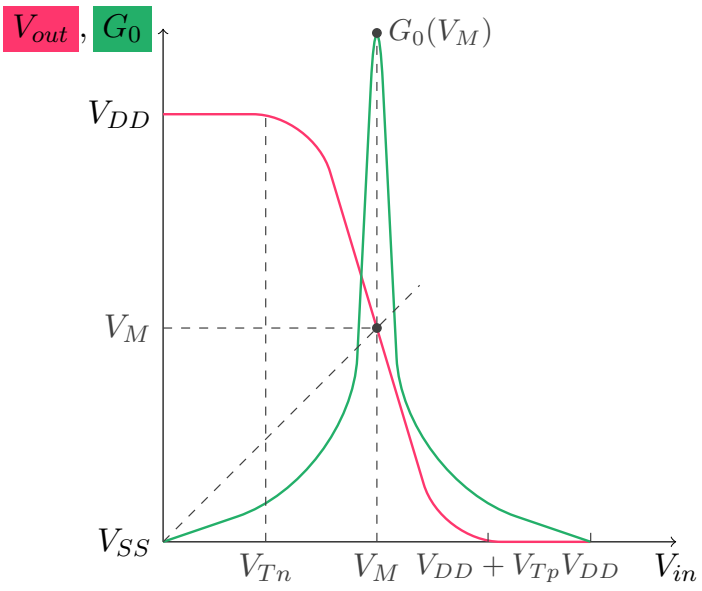


Figure 3.31: Inverter characteristics

The gain peak at V_M can be calculated within the small-signal regime as both devices are saturated.

$$G_0(V_M) = -\left(g_{mn} + g_{mp}\right)\left(r_{dsn} || r_{dsp}\right)$$

with

$$V_M = \frac{V_{Tn} + \sqrt{\frac{K_n}{K_p}}\left(V_{DD} + V_{Tp}\right)}{1 + \sqrt{\frac{K_n}{K_p}}}$$

As the threshold voltages, V_{Tn} and V_{Tp}, are fixed within the process it can be seen that the mid voltage V_M can be laid down through the ratio of the process transconductances $\frac{K_n}{K_p}$. VDD refers to the supply voltage, while g_m and r_{ds} are the transconductance and the drain-to-source resistance of the MOS devices. By applying the gain and phase criterion the start-up frequency of the oscillator can be indicated. After the signal amplitude raises and one of the transistors gets out of saturation, this frequency shifts to the value of the delay based equation.

3.3.3 Differential pair based ring oscillator

Differential ring oscillators are widely used and are based on differential gain or delay stages. As they are biased with a tail current I_{BIAS}, they don't provide rail-to-rail output swing. The signal swing as well as the propagation delay t_d are determined by this current. The load of the differential pairs can either be active or passive and a replica bias block (CMFB) is used to maintain a constant DC level. Their strength is that they have a proper power supply rejection, as noise on the supply appears as common-mode and is rejected by the next stage in the chain, and the propagation delay is only dependent on the differential resistance. A very basic differential delay cell, without a replica circuit is shown in figure 3.32. The propagation delay t_p, defined as delay between an input step and the zero crossing of the differential outputs, can be calculated as follows, [Abi06].

$$t_p = \frac{C_L V_{sw} \ln(2)}{I_{BIAS}} = RC_L \ln(2)$$

With the differential output swing V_{sw}:

$$V_{sw} = I_{BIAS} R$$

Gives for a n-stage ring oscillator, biased with a current I_{BIAS}, the load capacitance C_L and loaded with the resistance R:

$$f_0 = \frac{1}{2nRC_L \ln(2)}.$$

A very popular differential delay cell, often used in phase locked loops, is the Maneatis cell [MH93]. It replaces the passive by an active symmetric load

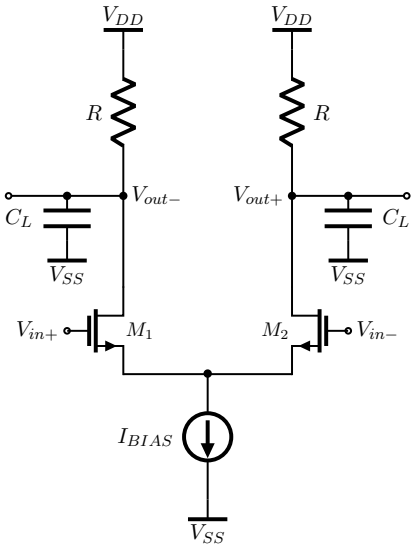
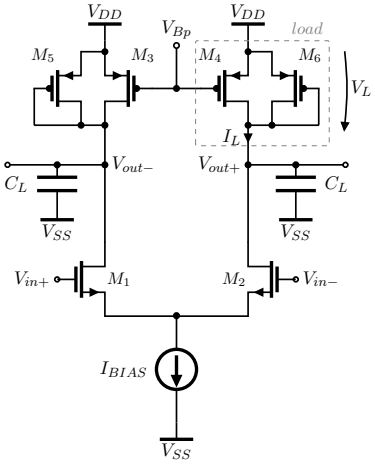
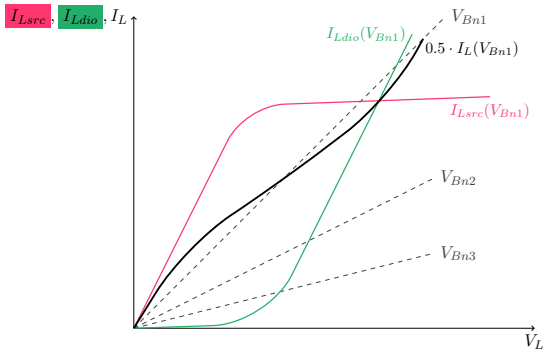


Figure 3.32: Basic differential delay cell



(a) Basic circuitry - without replica circuit



(b) Load characteristics

Figure 3.33: Maneatis delay cell

which is formed by a current source and a diode connected MOS device. The main idea is to form linear I-V characteristics for the symmetric loads. That approach is leading to a superior power supply rejection and wide tuning ranges if they are used within a VCO design.

The circuitry and the corresponding load characteristics of the Maneatis cell are shown in figure 3.33. The load can be seen as a circuit that averages or adds a pMOS source current I_{Lsrc} and a diode connected pMOS current I_{Ldio}. As they are equal sized the overall current I_L with respect to the load voltage V_L has a linear characteristics over a certain output swing range,

depicted in figure 3.33b. The impedances of the loads might vary over swing but they are equal to each other. To limit the output swing to the symmetric range of the load, a dynamic bias scheme has to be added, [CVPHM07]. The corresponding dynamic bias and the basic ring oscillator circuitry can be seen in figure 3.34. The differential resistance and the output frequency is controlled via V_{BIAS}. Additionally an amplifier stage can be included to the biasing circuit to reduce the supply voltage sensitivity, shown in figure 3.35. The feedback loop detects changes due to supply variation and adjusts the gate source voltage of the nMOS current sources. Therefore, the output impedance of the delay cells are increased.

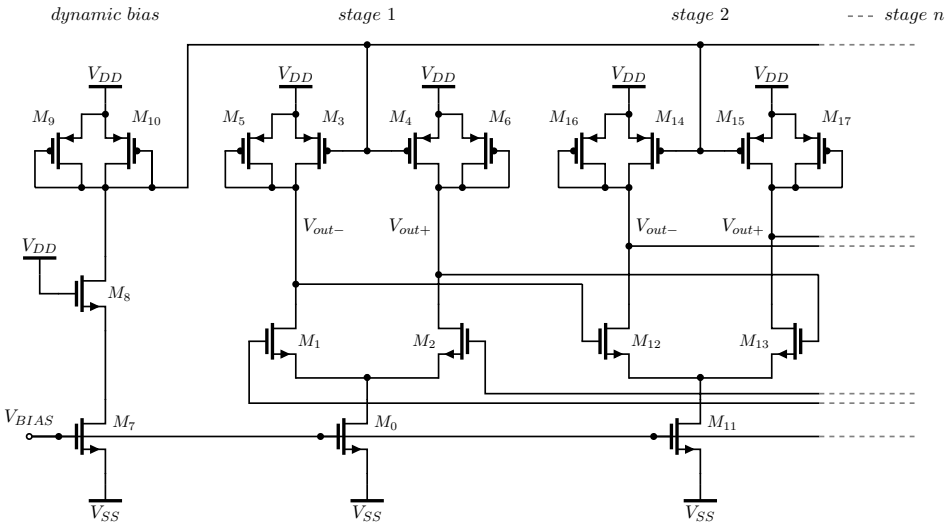


Figure 3.34: Differential ring oscillator based on Maneatis delay cells

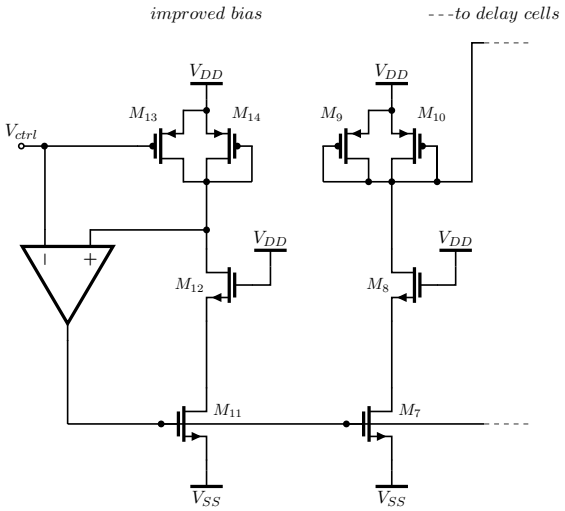


Figure 3.35: Improved bias circuit

3.3.4 Pseudo differential ring oscillator

Many of the recently published delay cells are pseudo differential structures without a tail-current bias and are capable of providing rail-to-rail outputs, [PK99] [CL11]. A widely spread pseudo differential delay cell is the Kim Lee cell [LK00], shown in figure 3.36. The delay element that consists out of six MOS devices uses two cross-coupled pMOS transistors, M_3 and M_4, to generate pseudo differential output signals with low rise- and fall times as they form a positive feedback latch. The output frequency is controlled by M_5 and M_6 via V_{ctrl}. This structure gives rail-to-rail outputs and therefore, in contrast to the biased differential structure, no additional level shifters are required to get digital CMOS levels.

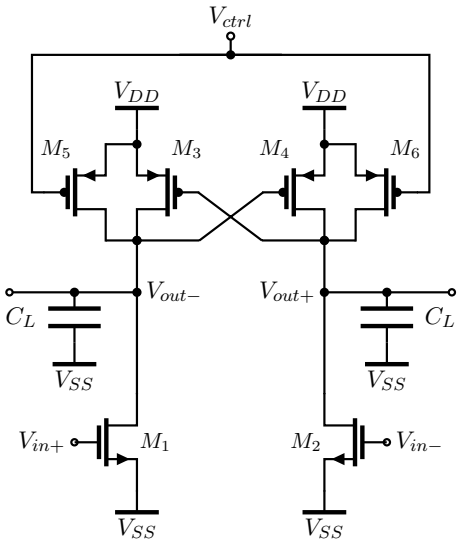


Figure 3.36: Kim Lee delay cell

Recent ring oscillator designs

As ring oscillators in CMOS technology have been used for a long time there have been many different pseudo and fully-differential ring oscillators published. Table 3.4 gives a comparison of recent designs in respective to power consumption, output frequency and their FoM, [JJA13].

Archit.*	Topol.	FOM[$\frac{dBc}{Hz}$]	Power[mW]	Freq.[GHz]	Ref.
3-stage, sl	Pseudo	-157.6	2	2.4	[DT11]
2-stage, sl	Pseudo	-194.3	9.5	9	[SL11]
4-stage, dl	Pseudo	-161.35	100	5.22	[YST10]
4-stage, ml	Pseudo	-163.3	60	7.64	[HL09]
3-stage, dl	Pseudo	-172.3	9	5	[MP08]
4-stage, sl	Fully	-149.1	12.6	3.13	[CSA11]
3-stage, ml	Fully	-145.1	72	7	[HL08]
2-stage, sl	Fully	-165.96	11.38	0.85	[LdP07]
2-stage, sl	Fully	-148.92	17	3.6	[WHT04]

* sl: single delay loop, dl: dual delay loop, ml: multiloop

Table 3.4: Comparison of ring oscillator designs

3.4 Digital oscillators

Realizing circuits that have been mainly implemented as analog designs in the past becomes more and more popular recently. Many digital PLLs and DLLs have been published as well as approaches for digital oscillators, [Yan12]. The idea is to get sinusoidal, harmonic outputs out of digital, harmonic distorted signals. By applying digital harmonic cancellation techniques and filtering this can be achieved. The harmonic cancellation block sums up phase-shifted squarewave inputs with respect to digital algorithms to cancel certain harmonics. The rest of the harmonic content is suppressed by a filter module.

3.4.1 Principle

A simple example of harmonic cancellation is the suppression of even harmonics through differential signal paths, seen in figure 3.37. m is the fundamental amplitude and m_{dc} the dc level of the single-ended signals. It can be seen that the even harmonics including the dc voltage are cancelled, the amplitudes of the odd's double and as a result the THD decreases. By applying a low pass filter the THD would further decrease and the signal shape would more and more transform into a sinusoidal one.

An already mentioned digital harmonic cancellation, short DHC, is a technique that sums phase shifted signals of same frequency, depicted in figure 3.38a. As a result the 3^{rd} and 5^{th} harmonic can be cancelled and by applying different summing coefficients via a mathematical algorithm it is possible to remove more harmonic content at the output. The Fourier series expansion of a squarewave is:

$$x(t) = \frac{4}{\pi} \sum_{k=1,3,5...}^{\infty} \frac{1}{k} \cos(k\omega_0 t).$$

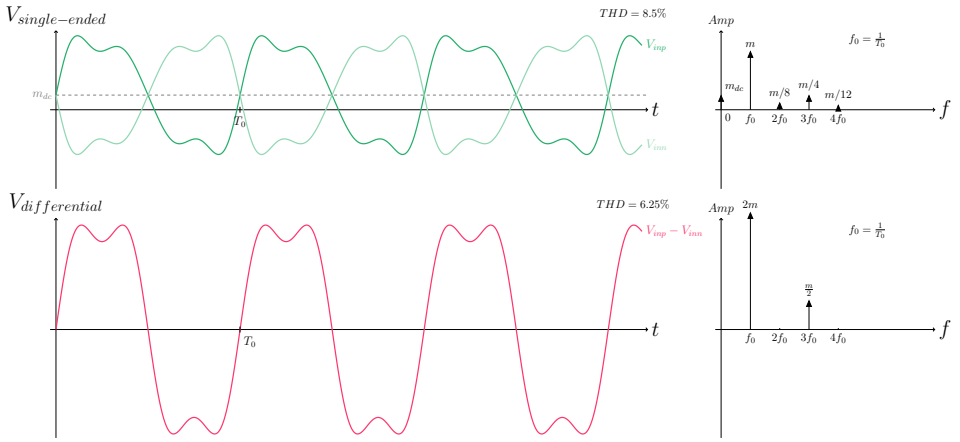


Figure 3.37: Differential harmonic cancellation

Where ω_0 is the fundamental frequency and the harmonic index k is restricted to odd values. If a time-shift δt is applied the Fourier series can be written as:

$$x(t+\delta t) = \frac{4}{\pi}\sum_{k=1}^{\infty}\left[\frac{1}{k}\cos(k\omega_0 t)\cos(k\omega_0\delta t)\right] - \left[\frac{1}{k}\sin(k\omega_0 t)\sin(k\omega_0\delta t)\right].$$

If the former signal would be added with the shifted version, the summed signal would get unsymmetrical around the origin. Therefore, a signal with negative time-shift $-\delta t$ is introduced. The sum of signals with opposite time-shift gives:

$$x(t+\delta t) + x(t-\delta t) = \frac{4}{\pi}\sum_{k=1}^{\infty}\left[\frac{1}{k}\cos(k\omega_0 t)2\cos(k\omega_0\delta t)\right].$$

From this series it can be seen that each harmonic is multiplied by a factor of $2\cos(k\omega_0\delta t)$. If n time-shifted signal pairs with $\delta t_1 ... \delta t_n$ and summing coefficients are added, the harmonic multiplication factor M_k for each harmonic is given by:

$$M_k = \frac{4}{\pi k} 2 \sum_{i=1}^{n} \cos(k\omega_0\delta t_i).$$

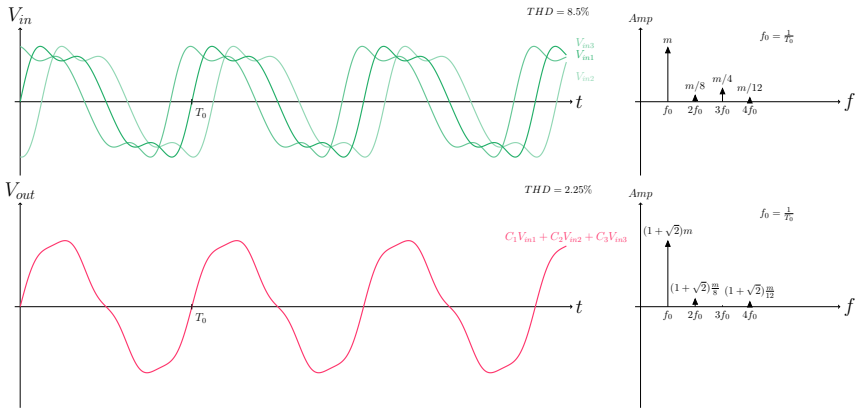
Introducing summing coefficients C_s with $s = 0$ for the initial unshifted signal and $s = 1$ to n for the time-shifted pairs gives the Fourier series of the overall sum $s(t)$:

$$s(t) = \frac{4}{\pi}\sum_{k=1}^{\infty}\frac{1}{k}\cos(k\omega_0 t)\left[C_0 + 2\sum_{i=1}^{n} C_i\cos(k\omega_0\delta t_i)\right].$$

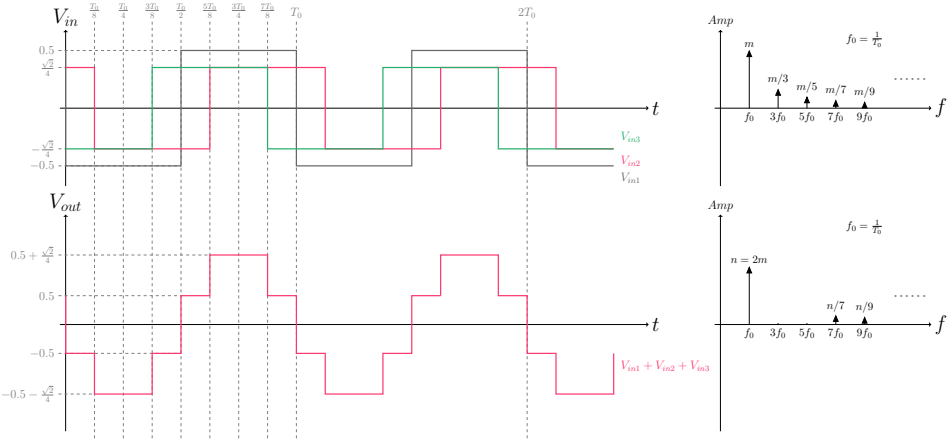
Applying this to signals with one time-shifted pair $n = 1$ with summing coefficients, $C_0 = 1$ and $C_1 = \frac{\sqrt{2}}{2}$, and time shifts of $\delta t_1 = (\pm)\frac{T_0}{8}$ gives the signals shown in figure 3.38b, [Yan12]. It can be seen that at the output the 3^{rd} and 5^{th} harmonic as well as higher harmonics are fully cancelled. The multiplication factors of the harmonics can therefore be written as:

$$M_k = \frac{4}{\pi k}\left[1 + \sqrt{2}\cos\left(k\frac{\pi}{4}\right)\right].$$

From this equation it is seen that harmonics with indexes $k = 3 + 8i$ and $k = 5 + 8i$ for $i = 1$ to ∞ are cancelled. Please note that at the beginning of this section it was defined that only odd k's are included.



(a) Summing waveforms with phase-shift



(b) Summing shifted squarewave signals

Figure 3.38: Harmonic cancellation by summing

Hence, by choosing proper summing coefficients and phase shifts of digital signals followed by a passive linear filter the harmonic content of the corresponding output signal can be shaped. The two main approaches in the digital oscillator design are open-loop and feedback systems.

3.4.2 Digital open-loop oscillator

By using this structures it is possible to design low power, small area and large output swing oscillators with THD$<-70dB$, hardly achieved with standard structures in modern technologies, [ESS10]. Rather than acting in voltage or current-mode in this oscillators, the information is represented by the time difference between two digital state transitions. For advanced technologies this gives main advantages as the supply voltage is decreasing, giving less dynamic voltage range, and on the other hand the speed of digital circuitry is increased. This leads to very precise timings and therefore a very good dynamic time range. To obtain sinusoidal output signals V_{out}, this oscillators are fed by a square-wave input signal V_{in} provided by a frequency synthesizer. This signal is processed by a digital harmonic cancellation module, followed by a passive low-pass filter, depicted in figure 3.39. Compared to digital feedback oscillators the requirements for the DHC block as well as for the filter are relaxed. The input of this oscillator is a high frequency Nf_0 signal that is converted to the desired output frequency f_0 via the DHC block. This block suppresses low harmonic content making a simple passive LPF capable of removing the high harmonic content. This leads to a low THD at the output and gives another advantage as the frequency and amplitude of the input only affects the noise floor but not the harmonic cancellation. Instead of introducing summing coefficients it is preferable to add more phase-shifted pairs for digital circuitry. This gives easy DHC block designs as well as the possibility to extend to pseudo differential topologies. This designs are called time-mode oscillators, [ESS10]. If digital oscillator designs include summing coefficients and time-shift pairs, they are called time-voltage-mode oscillator and are capable of suppressing even more harmonic content within their DHC block. Another approach is high-order-harmonic-boosting where also the fundamental frequency is suppressed to use one of the harmonic tones as main frequency for the output signal.

3.4.3 Digital feedback oscillator

A basic digital feedback oscillator is shown in figure 3.40a. It consists out of a two-level voltage comparator and a BPF. In this approach no harmonic content is cancelled, it is just suppressed by the BPF and implies the need of a high quality factor. The sinusoidal signal is provided by filtering the squarewave output signal of the comparator. After the oscillation build up, the averaged loop gain is equal to unity and Barkhausen's criterion is fulfilled. As it is difficult to design high Q integrated BPF's the linearity is a major design challenge. The distortion HD_k caused by the k^{th} harmonic at the output of a BPF can be approximately expressed as follows, [Yan12].

$$HD_k \approx \frac{1}{k^2 Q}$$

Hence, the total harmonic distortion THD can be expressed as:

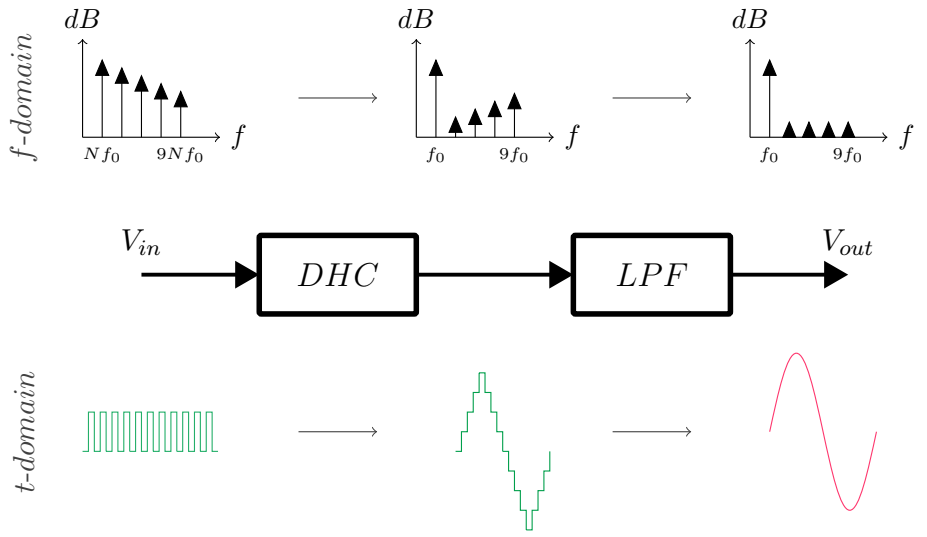


Figure 3.39: Digital open loop oscillator

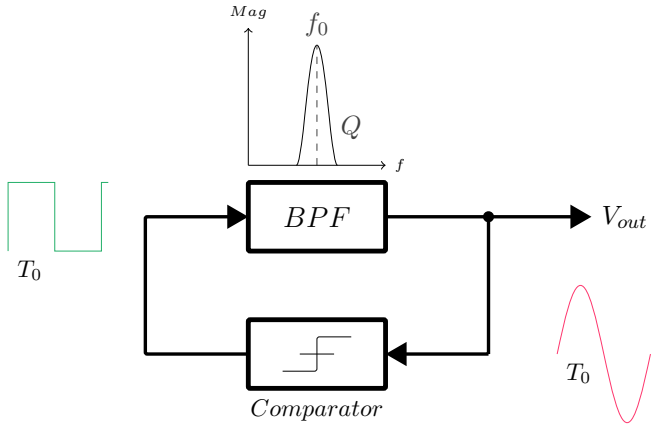
$$THD \approx \frac{1}{Q} \sum_{k=3,5,7..}^{\infty} \frac{1}{k^2}.$$

Taking into account harmonics from $k = 1, 3, 5$ to 11 and targeting a THD of $-50dB$ the quality factor of the filter Q must be greater than 60. This is not practicable within integrated circuits where the Q factor of BPF's hardly exceeds 15. Hence, this structure suffers from linearity limitations. To overcome this limitation the lower harmonic content, that is main contributer of distortion, can be cancelled by a DHC module and therefore relaxes the filter requirements. In figure 3.40b this block is realized by a multilevel comparator, [SPSS07]. This mulitlevel comparator modifies the squarewave in the same way as shown in figure 3.38b and gives a $20dB$ THD improvement.

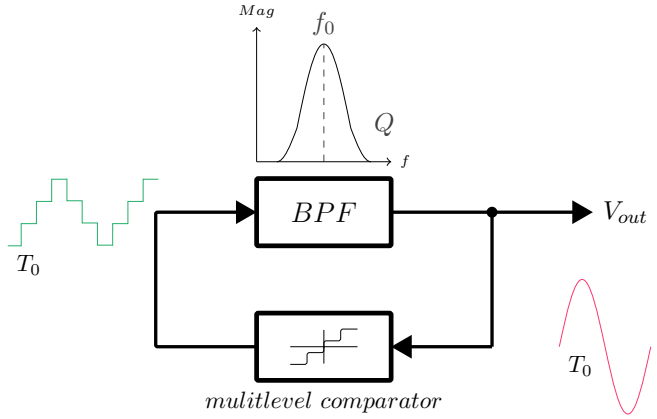
Further decrease of harmonic content can be achieved by adding more clamping levels to the comparator. On the other hand, this also increases the complexity and power consumption of the oscillator and designing high Q BPF's, mainly done by using the switch capacitor approach, leads to even more design challenges. Thus, in recent very low distortion oscillators the open loop structure is dominant.

3.5 Characterization

According to the need of an application different oscillator structures are preferable. From an economical perspective the area, power consumption or the need of special components might be a reason to rule out certain structures for a given application. For low-power applications it is important that the oscillator keeps it's oscillation frequency over temperature and supply voltage as usually no continuous regulation loop is implemented. Most likely



(a) Comparator based



(b) Mulitlevel comparator based

Figure 3.40: Digital feedback oscillators

they operate at much lower frequencies than RF oscillators. On the other hand high-performance oscillators are most likely part of a regulation loop (PLL) and the main challenge is to minimize phase noise. Hence, different figures of merit have been defined.

3.5.1 Phase noise requirement

As already discussed, the amplitude of an oscillator is well defined and in most cases limited by circuit non-linearity. If the signal amplitude raises and the system gets non-linear the loop gain decreases and is dampened. As the amplitude drops, the oscillator gets in it's linear operating region, the loop gain increases and the amplitude raises again. The averaged loop gain of this self regulation mechanism is unity and fulfils Barkhausen's criterion at it's operating frequency. The phase of the oscillator on the other hand has no regulation mechanism and therefore phase errors persist. Noise due to amplitude modulation is rejected and oscillators mainly generate phase noise. Therefore, the output spectrum of an oscillator flattens around $\pm f_0$ rather

than having a single peak. As in any non-ideal system the energy can't be concentrated in a single point. It's spread but focused around this desired point of interest, seen in figure 3.41.

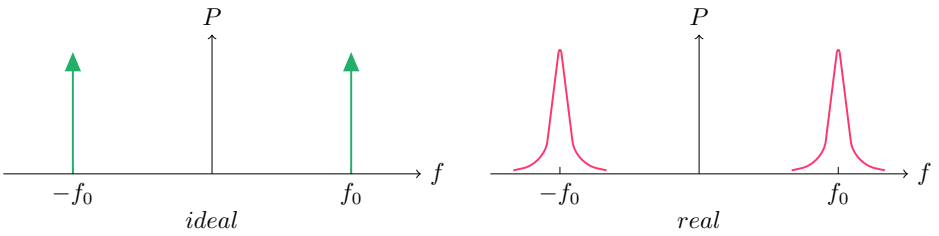


Figure 3.41: Ideal vs. real spectrum

Taking a basic RLC tank model, illustrated in figure 3.3, the losses are compensated by the transconductance gm and it is acting as a ideal LC parallel circuit. It is assumed that the only noise source is the tank circuit. During the voltage peak v_{pk} the complete energy E_{tank} is stored within the electrical field of the capacitance. This peak voltage can be expressed as corresponding mean-square voltage $\bar{v_s^2}$.

$$E_{tank} = \frac{1}{2} C v_{pk}^2 = C\bar{v_s^2}$$

To get the total mean-square noise voltage, the thermal noise density of the resistance has to be integrated over the bandwidth of the RLC resonator in reference to [Ody02]. The impedance of the tank Z_{RLC} circuit is well known, [VW48].

$$Z_{RLC}(f) = R\frac{d}{d + j\left(\frac{f}{f_0} - \frac{f_0}{f}\right)}$$

With the resonance frequency f_0:

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

and the damping factor d:

$$d = \frac{1}{Q} = \frac{1}{R}\sqrt{\frac{L}{C}} = \frac{2\pi f_0 L}{R} = \frac{1}{2\pi f_0 RC}$$

By definition the quality factor Q of the tank is fixed as:

$$Q = \frac{\omega_0 E_{tank}}{P_{diss}}$$

Where P_{diss} is the power dissipation and $\omega_0 = 2\pi f_0$. The total mean-square noise $\bar{v_n^2}$ can be found below.

$$\bar{v_n^2} = 4k_BTR\int_0^\infty \left|\frac{Z_{RLC}(f)}{R}\right|^2 df = 4k_BTR\frac{1}{4RC} = \frac{k_BT}{C}$$

The signal to noise ratio SNR can be determined from the initial equation in combination with this relation. k_B is Bolzmann's constant and T the absolute temperature. The expression $\frac{k_BT}{C}$, well known for RC circuits, is also found in RLC circuits.

$$SNR = \frac{\bar{v_s^2}}{\bar{v_n^2}} = \frac{E_{tank}}{k_BT} = \frac{QP_{diss}}{\omega_0 k_BT}$$

From the equation above it can be seen that increasing the Q factor of an ideal oscillator model, where losses are compensated and the resistance in the tank is the only noise source, directly benefits the SNR. Therefore to minimize noise within a LC oscillator, maximizing Q is essential. To invest on the noise distribution around the resonance frequency ω_0 the impedance of LC tank at a small offset frequency $\Delta\omega$ is approximately to be:

$$Z_{LC}(\omega_0 + \Delta\omega) \approx j\frac{\omega_0 L}{2\frac{\Delta\omega}{\omega_0}}.$$

By incorporating the unloaded tank quality factor Q, solving for L, and substitution of the absolute value of the impedance, the impedance Z_{LC} can be rewritten as follows.

$$|Z_{LC}(\omega_0 + \Delta\omega)| \approx R\frac{\omega_0}{2Q|\Delta\omega|}$$

To obtain the spectral density of the mean-square noise voltage $\bar{v_n^2}$, the spectral density of the noise current $\bar{i_n^2}$ has to be multiplied by the squared magnitude of the impedance.

$$\frac{\bar{v_n^2}}{\Delta f} = \frac{\bar{i_n^2}}{\Delta f}|Z_{LC}|^2 = 4k_BTR\left(\frac{f_0}{2Q\Delta f}\right)^2$$

It can be seen that the spectral density of the mean-square voltage has a $\frac{1}{f^2}$ behaviour. As the voltage frequency response of a LC circuit rolls of with $\frac{1}{f}$ at each side of the center and the power is proportional to the squared voltage, this relationship is not surprising. The noise density again benefits from large quality factors Q. Please note that this equation represents the total noise that impacts both amplitude and phase of the oscillators output. The equipartition theorem states that noise impact splits evenly between amplitude and phase for sinusoidal signals, [Lee98]. Hence, only half of the spectral noise density is considered, as amplitude noise is rejected. To get the

well known term for the power noise spectral density $L\{\Delta f\}$ a normalization to carrier signal power is done:

$$L\{\Delta f\} = 10\log\left[\frac{k_B T}{2P_{sig}Q^2}\left(\frac{f_0}{\Delta f}\right)^2\right]$$

Therefore, it can be seen that phase noise at given offset Δf improves either by increasing the signal power P_{sig} of the carrier, or quadratically by having a higher quality factor Q. This equation only includes the tank resistance as noise source. If also the negative resistance of the active circuitry is taken into account, the spectral noise density is given as follows. This can be seen in figure 3.42.

$$\frac{\bar{v_n^2}}{\Delta f} = \left(\frac{\bar{i_{nR}^2}}{\Delta f} + \frac{\bar{i_{ngm}^2}}{\Delta f}\right)|Z_{LC}|^2 = \frac{\bar{i_{nR}^2}}{\Delta f}\overbrace{\left(1 + \frac{\frac{\bar{i_{nR}^2}}{\Delta f}}{\frac{\bar{i_{ngm}^2}}{\Delta f}}\right)}^{F(\Delta f)}|Z_{LC}|^2$$

$$L\{\Delta f\} = 10\log\left[F(\Delta f)\frac{k_B T}{2P_{sig}Q^2}\left(\frac{f_0}{\Delta f}\right)^2\right]$$

The factor $F(\Delta f)$ gives the ratio of total noise in the tank to noise caused by the tank resistance at a frequency offset Δf. However, in real circuits the actual situation is much more complicated because noise is not only caused by resistors. MOS devices have $\frac{1}{f}$ flicker noise and can degrade the quality factor of the tank as well as their noise might be modulated by other transistors. Anyway, in practical oscillators the overall spectral noise density follows the $\frac{1}{f^2}$ rule over a wide frequency range, but there is also a $\frac{1}{f^3}$ region for low offset frequencies illustrated in figure 3.43.

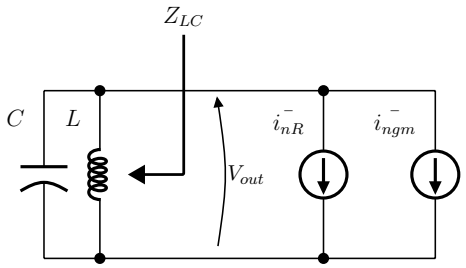


Figure 3.42: More noise sources

Leeson did a modification of the phase noise expression with a consideration of $F(\Delta f) = const = F$ to capture the noise profile of figure 3.43, [Lee96].

$$L\{\Delta f\} = 10\log\left[\frac{2Fk_B T}{P_{sig}}\left(1 + \left(\frac{f_0}{2Q\Delta f}\right)^2\right)\left(1 + \frac{\Delta f_{\frac{1}{f^3}}}{|\Delta f|}\right)\right]$$

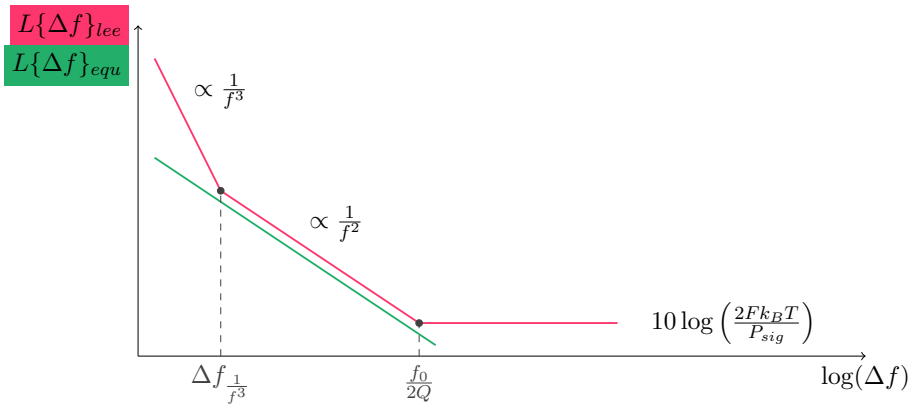


Figure 3.43: Equation vs. practical power noise density

3.5.2 Additional performance parameters

Phase noise is the main requirement for RF oscillators, but on the other hand low-power time-references focus on a different set of performance parameters. Not being re-adjusted by continuous regulation loops, a robust design that is as insensitive to process, supply voltage and temperature is essential.

1. Temperature coefficient, TC in $\frac{ppm}{C^\circ}$
2. Voltage coefficient, VC in $\frac{\%}{V}$
3. Process sensitivity, statistical 3σ-value
4. Power consumption and area

Beside the main requirement to consume low power, this designs are challenging because temperature compensation within this low power operation is not easy to achieve. To get low cost implementations the area should be minimized.

3.5.3 Figure of merit

For designs where the focus lies on low power consumption, e.g. energy harvesting or wake-up circuits, FoM_1 and FoM_2 are preferred. High performance oscillators focusing on low phase noise and low conversion losses from DC to AC energy are mainly benchmarked by FoM_3 for a single frequency and by FoM_{3T} if tunable, [CRA+07].

$$FoM = 10\log\left[\left(\frac{f_0}{\Delta f}\right)^2 \frac{1}{P_{diss}\cdot L\{\Delta f\}}\right]$$

$$FoM_T = 10\log\left[\left(\frac{f_{range}}{\Delta f}\right)^2 \frac{k_B\cdot T}{P_{diss}\cdot L\{\Delta f\}}\right]$$

$$FoM_1 = \frac{P_{diss}}{f_0}$$

$$FoM_2 = 10 \log \left(\frac{f_0 \cdot Lmin}{P_{diss} \cdot TC \cdot A} \right)$$

Where P_{diss} is the power dissipation, f_0 the operation frequency, L_{min} the process length, TC the temperature coefficient, A the area of the circuit, $L\{\Delta f\}$ the phase noise at the offset frequency Δf, f_{range} the tuning range $(f_{max} - f_{min})$, k_B is Bolzmann's constant and T the absolute temperature. Please note that within FoM_{3T} the temperature dependency of the phase noise is cancelled by $k_B T$ and could also be applied to FoM_3. The phase noise dependency on the offset frequency is cancelled in FoM. This figure of merits are used to compare and benchmark fully-integrated oscillators.

Part II

Design and Simulation

Chapter 4

System Overview

4.1 Specifications

As the desired oscillator is the digital heart of a SoC's standby mode, it's power consumption is essential to meet the overall system specification. All wake-up functions are dependent on this oscillator. Hence, a robust PVT-insensitive design is required. The oscillator's output waveforms must be squarewave rail-to-rail signals with a 50% duty-cycle. The rise- and falltimes should be minimized while keeping the power consumption low. Main requirements of the low power oscillator are:

Specification	Value
Operation frequency	100 - 200kHz
Accuracy over PVT	$\pm 5\%$
Supply voltage	$1.8V \pm 10\%$
Current consumption	1 - 2μA
Trimming	Yes
Temperature range	-50 to 120°C
CMOS-Process	TSMC 180nm
Area	less than 0.1mm^2

Table 4.1: Design specification

During the standby mode the oscillator is supplied by a low power LDO regulator and it's clock feeds the wake-up timer, the power on reset circuit as well as the control logic and other digital circuitry that is active during low power operation. This is illustrated in figure 4.1. The low power oscillator should provide a dedicated reference generator if there are reference voltages or currents needed. No bandgap voltage is provided by the system during standby. The oscillator's process sensitivity should be low and trimming capabilities have to be included to calibrate the absolute output frequency. Once the oscillator is trimmed, it should stay within $\pm 5\%$ of the operation frequency over temperature and supply voltage. No monolithic inductors or special MOS devices should be used.

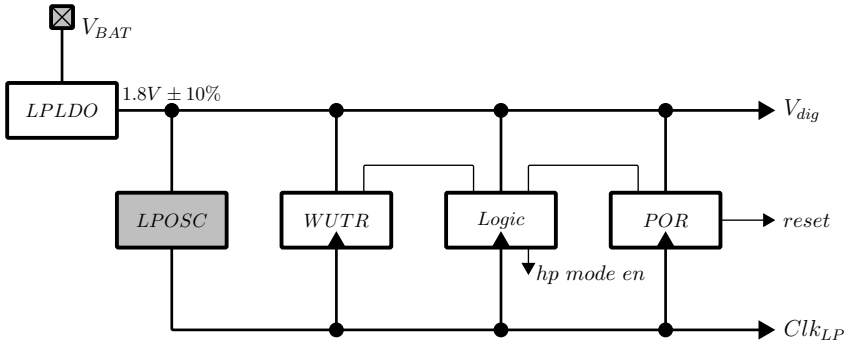


Figure 4.1: LPO within standby mode

Selection of oscillator topology

The given specification rules out some of the oscillator topologies discussed in chapter 3. An LC oscillator design is out of question because of several factors. First of all, there are no monolithic inductors available. If they would be available the operation frequency is far too low to reach the desired area in reference to the frequency equation in subsection 3.1.1. These structures don't provide squarewave rail-to-rail outputs and would have a high current consumption to get high signal swing. A ring oscillator design would be an option but not with differential or pseudo-differential delay cells. Even if they have improved performance they don't provide rail-to-rail outputs. Inverter-based ring oscillators are able to provide rail-to-rail outputs but are very process dependent and the current consumption is not well defined. If current-starved inverters are used the current consumption is defined but again no rail-to-rail outputs are provided. Anyway, a combination of different delay cells would be possible but ring oscillators are most likely designed for high operating frequencies. To get output frequencies in the range of $200kHz$ a lot of delay cells would be needed and this implies that the current consumption requirement can't be met, in reference to table 3.4. Digital oscillators can be ruled out simple by the fact that no digital circuitry is running without the low power oscillator. Last but not least RC oscillators are a good option for a low power design. A differential to single-ended transformation is necessary to use differential RC oscillators in relaxation mode as clock source for this application. This increases the complexity and current consumption. Looking at table 3.2 shows that the requirements can't be met with this structures. The best choice for very low power operation is a comparator based relaxation oscillator design as it's possible to get very low reference currents while a comparator provides rail-to-rail output signals. As stated several times, temperature compensation is a major challenge for this oscillator structures.

4.2 Dual-phase system

This section explains the main idea of the oscillator structure used throughout this thesis. It is a dual-phase system with two adaptive biased comparators and a shared latch. The proposed reference generator is able to provide a temperature compensated reference current and voltage to the oscillator core. This oscillator structure gives two pseudo-differential squarewave output signals, each with rail-to-rail signal swing. Figure 4.2 shows the concept of the dual-phase oscillator. The nominal operation frequency has been chosen to be $100kHz$ and is not influenced by the capacitor discharge time as seen in figure 4.2b.

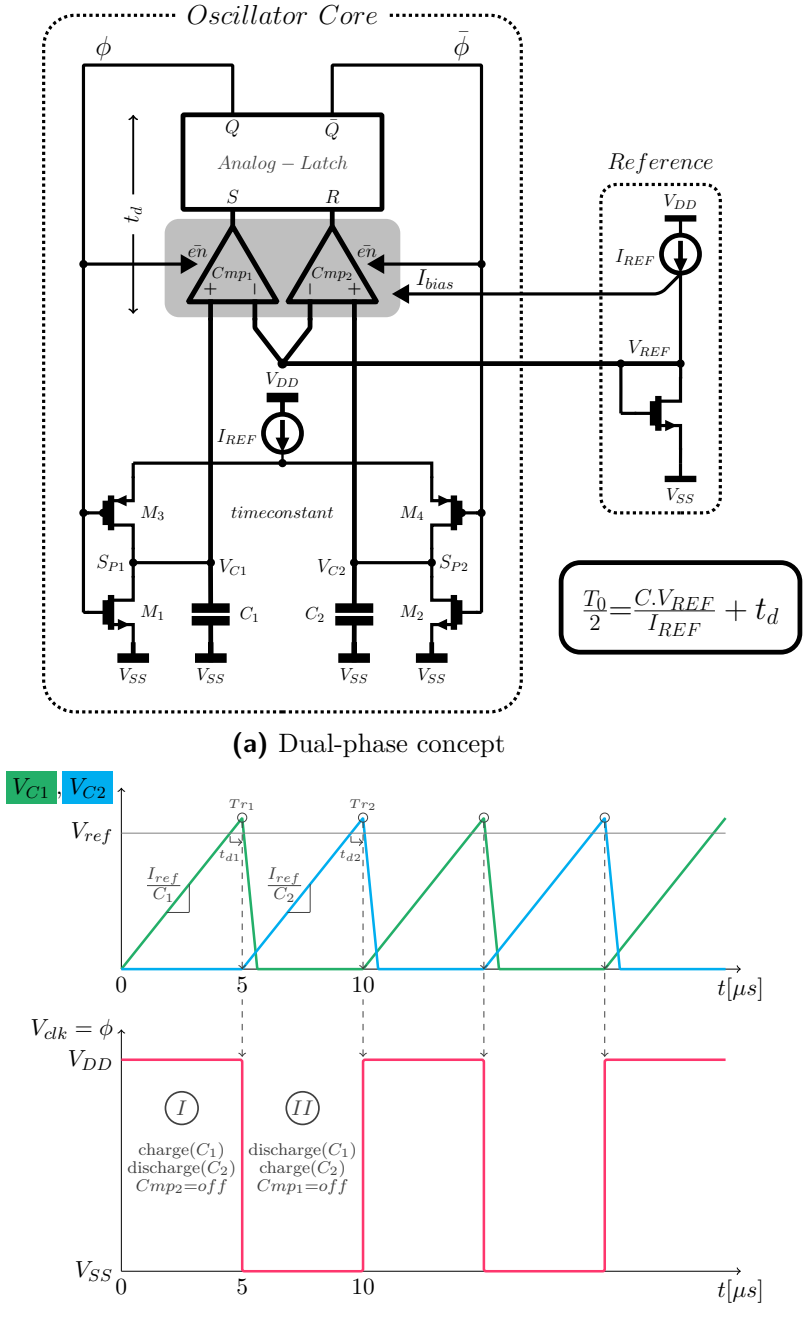
The oscillator period T_0 can be defined as:

$$T_0 = (C_1 + C_2)\frac{V_{ref}}{I_{ref}} + t_{d1} + t_{d2}.$$

If the delays and the capacitors are well matched, $C = C_1 = C_2$ and $t_d = t_{d1} = t_{d2}$, the term can be simplified to:

$$T_0 = 2C\frac{V_{ref}}{I_{ref}} + 2t_d.$$

Where t_d is the delay of one of the comparators in combination with the latch. The capacitors C_1 and C_2 get alternately charged by the reference current I_{ref}. The transistor M_1 or M_2 discharges one of the capacitors, while M_3 and M_4 determine in which branch I_{ref} flows. As the charging current is constant, the capacitor acts as an integrator and the voltage V_{C1} or V_{C2} ramps up with a slope of $\frac{I_{ref}}{C_{1,2}}$. A certain time delayed the capacitor voltage exceeds V_{ref} and the trigger point T_{r1} or T_{r2} is reached. The system changes it's state, the corresponding capacitor gets discharged and the reference current is redirected to charge the other capacitor. The discharging time is not of interest as long as the capacitor voltage reaches zero in less than $\frac{T_0}{2}$. This structure gives some advantages compared to those in section 3.2.6. For the double comparator RC oscillator a well matched current source and sink is important and two different reference voltages are needed. Therefore, low power consumption and temperature compensation is very difficult to achieve. The single comparator circuit's discharge delay influences the oscillator period and is process and temperature dependent. The main task within this design is to keep the overall temperature coefficient as low as possible while minimizing the current consumption. The proposed design also eliminates the need of a resistance to define the reference current, by introducing a MOS-only self-biased structure that is able to generate a compensated reference current and voltage. The temperature dependency of the $\frac{V_{ref}}{I_{ref}}$-ratio is minimized and the delay of the comparator is kept low by using a low static bias current and adding a dynamic bias current only during state transition. The temperature coefficient of the delay is matched with the capacitor one's. Rather than



(a) Dual-phase concept

(b) Waveforms

Figure 4.2: Dual-phase relaxation oscillator

narrow pulses with not well defined voltage levels it's output is a 50% duty-cycle rail-to-rail squarewave signal, that eliminates the need of additional digital circuitry to shape the signal. To tune the absolute output frequency, a trim scheme is proposed that benefits the overall temperature coefficient of the oscillator. This scheme was extended by a current trimming approach that gives a linear monotonic frequency variation over trim-word.

Chapter 5

Literature review

The dual-phase oscillator's main building blocks are the reference generator and the comparator. This chapter reveals basic principles and circuits, frequently used and found in literature and other articles.

5.1 Reference generator

As a circuit that generates a compensated reference voltage is an essential building block within a modern IC, many different design approaches have been made. In combination with an accurate resistor (-ratio) also a stable DC current could be provided.

5.1.1 Bandgap reference

A widely used approach to provide temperature compensated references is to combine a CTAT[1] and a PTAT[2] circuit. As the name implies, the outputs, voltage or current, of these circuits vary linearly with temperature but in opposite directions. By adding them with proper weighting, a temperature compensated output can be achieved. There have been many variations of this concept but the main idea, shown in figure 5.1, stays the same.

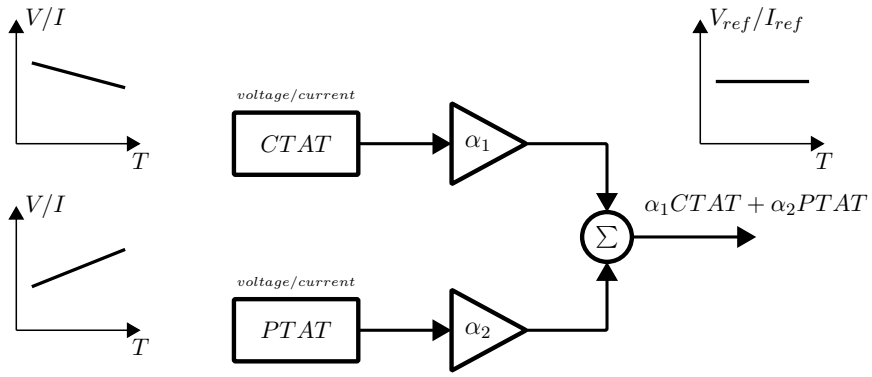


Figure 5.1: Combination of PTAT and CTAT

[1]CTAT: complementary to absolute temperature
[2]PTAT: proportional to absolute temperature

A well-known circuit that combines the CTAT behaviour of the forward-bias-voltage of a PN junction[3] with the PTAT behaviour of the extracted difference voltage ΔV_{BE} of two bipolar transistors on different current densities, is called band-gab reference, [Bro74]. The principle is shown in figure 5.2.

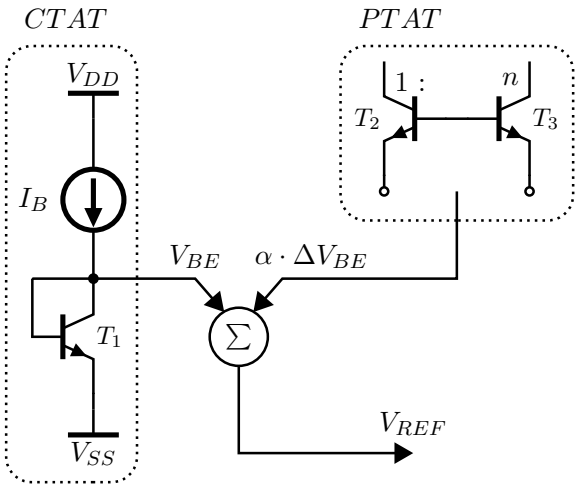


Figure 5.2: Principle of a bandgap reference

The base-emitter voltage V_{BE} of a bipolar transistor as a function of temperature can be expressed as follows.

$$V_{BE}(T) = V_{G0}\left(1 - \frac{T}{T_0}\right) + V_{BE0}\frac{T}{T_0} + mV_t \ln\left(\frac{T_0}{T}\right) + V_t \ln\left(\frac{J_C}{J_{C0}}\right)$$

with the thermal voltage V_t:

$$V_t = \frac{k_B T}{q}$$

Where V_{G0} is the bandgap voltage of silicon[4], T_0 is the reference temperature, V_{BE0} is the junction voltage at reference temperature and J_C, J_{C0} are the collector current densities for the actual and the reference temperature. k_B is Boltzmann's constant, q is the charge of an electron and m[5] is a temperature constant. Under the assumption that current densities stay constant and $T = T_0 = 300°K$ (room temperature), the calculation of the temperature coefficient for V_{BE} is shown:

$$\left.\frac{\delta V_{BE}}{\delta T}\right|_{T=T_0=300°K} = \frac{k_B}{q}\left[-m + \left(\frac{V_{BE0} - V_{G0}}{V_t}\right)\right] \approx -2\frac{mV}{°K}$$

Thus, the difference voltage ΔV_{BE} and it's temperature coefficient can be easily expressed as:

[3] or the base-emitter voltage V_{BE} of a bipolar transistor
[4] $V_{G0} \approx 1.206V$
[5] $m \approx 2.3$

$$\Delta V_{BE}(T) = V_{BE1} - V_{BE2} = \frac{k_B T}{q} \ln\left(\frac{J_{C1}}{J_{C2}}\right).$$

And the temperature coefficient is given by:

$$\left.\frac{\delta \Delta V_{BE}}{\delta T}\right|_{\frac{J_{C1}}{J_{C2}}=10} = \frac{k_B}{q} \ln\left(\frac{J_{C1}}{J_{C2}}\right) = 0.198 \frac{mV}{^\circ K}.$$

This means that for a current density ratio $n = \frac{J_{C1}}{J_{C2}} = 10$ the corresponding difference voltage ΔV_{BE} should be amplified by a factor of $\alpha \approx 10$ to compensate over temperature. To get the optimal amplification factor α and to achieve zero first-order temperature dependency of the output voltage V_{REF}, the following expression in reference to figure 5.2 is fundamental. Please note that the current junction density is usually proportional to absolute temperature and therefore, $\frac{J_{Ci}}{J_{Ci0}} = \frac{T}{T0}$ can be concluded.

$$V_{REF}(T) = V_{BE}(T)_1 + \alpha \Delta V_{BE}(T)_{2/3}$$

$$= V_{G0} + \frac{T}{T_0}\left(V_{BE0_1} - V_{G0}\right) + V_t \ln\left(\frac{T}{T_0}\right)(1-m) + \alpha V_t \ln\left(\frac{J_{C2}}{J_{C3}}\right)$$

By differentiating this equation with respect to temperature, the temperature coefficient of the output voltage V_{REF} can be written as:

$$\frac{\delta V_{REF}}{\delta T} = \frac{1}{T_0}\left(V_{BE0_1} - V_{G0}\right) + \frac{k_B}{q}\left[\ln\left(\frac{T}{T_0}\right) + 1\right](1-m) + \alpha \frac{k_B}{q} \ln\left(\frac{J_{C2}}{J_{C3}}\right).$$

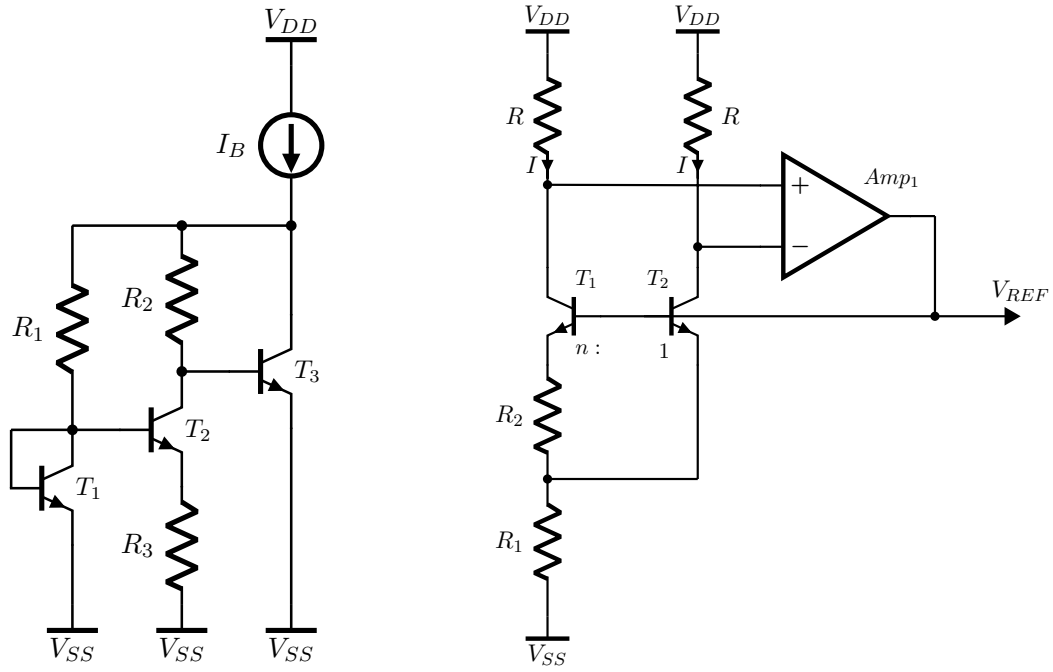
To obtain a zero temperature coefficient at reference temperature, $T = T_0 = 300^\circ K$, this equation is set equal to zero and terms are rearranged to find the optimal amplification factor α as well as the reference voltage V_{REF}.

$$V_{BE0_1} + \alpha \frac{k_B T_0}{q} \ln\left(\frac{J_{C2}}{J_{C3}}\right) = V_{G0} + (m-1)\frac{k_B T_0}{q}$$

$$\left.\alpha\right|_{T=T_0=300^\circ K} = \frac{\frac{V_{G0} - V_{BE0_1}}{V_t} + m - 1}{\ln\left(\frac{J_{C2}}{J_{C3}}\right)}$$

$$\left.V_{REF}\right|_{T=T_0=300^\circ K} = V_{G0} + (m-1)\frac{k_B T_0}{q}$$

Thus, the output voltage V_{REF} for zero TC is equal to $1.24V$ and for $\frac{J_{C2}}{J_{C3}} = n = 10$ this would lead to an amplification factor of $\alpha = 9.92$. A bandgap reference that only uses two bipolar devices to generate both the



(a) Three device bandgap reference -Widlar bandgap

(b) Two device bandgap reference - Brokaw bandgap

Figure 5.3: Bandgap reference design approaches

CTAT and PTAT behaviour has been the basis for many voltage reference designs, [Bro74]. Till this design came up a three devices design was the common way to go. Figure 5.3 shows both design approaches.

The emitter area and therefore current density ratio $\frac{J_{C1}}{J_{C2}} = \frac{1}{n}$, in reference to figure 5.3b. The current and voltage expressions are given by:

$$V_{REF} = V_{BE2} + V_{R1}.$$

As the amplifier forces the collector voltages of T_1 and T_2 to be equal, also equal collector currents flow through each branch. The current is fixed by R_2.

$$I_{R2} = \frac{\Delta V_{BE12}}{R_2}$$

$$V_{R1} = 2I_{R2}R1$$

$$V_{REF} = V_{BE2} + \underbrace{\frac{2R_1}{R_2}}_{\alpha} \Delta V_{BE12}$$

Therefore, assuming a current density ratio of $n = 10$ the resistor ratio $\frac{R_1}{R_2} = \frac{\alpha}{2}$ should be equal to 4.96. Anyway, it has to be said that the base currents

of the bipolar devices differ due to different collector current densities and therefore introduce an offset into the loop that decreases ΔV_{BE}. This offset can be compensated by adding a resistance between the bases of transistor T_1 and T_2, but in return leads to decreased noise performance. Generally spoken, bandgap circuits achieve a first order temperature compensation of their outputs, either current or voltage. The typical curvature of the output is caused by the third term seen in the V_{BE} equation, $mV_t \ln\left(\frac{T_0}{T}\right)$. Hence, $\frac{\delta V_{BE}}{\delta T}$ is still a function of temperature and therefore V_{BE} has not perfect CTAT characteristics. The logarithmic term has a strong quadratic component[6], that gives a temperature dependency similar to figure 5.4. Further compensation can be achieved by combining this curvature with one that has the same form but different sign. Figure 5.5 shows a waveform of V_{REF}, resulting from the combination of a curvature voltage V_{curv} and a opposite signed curvature V_{curv-}.

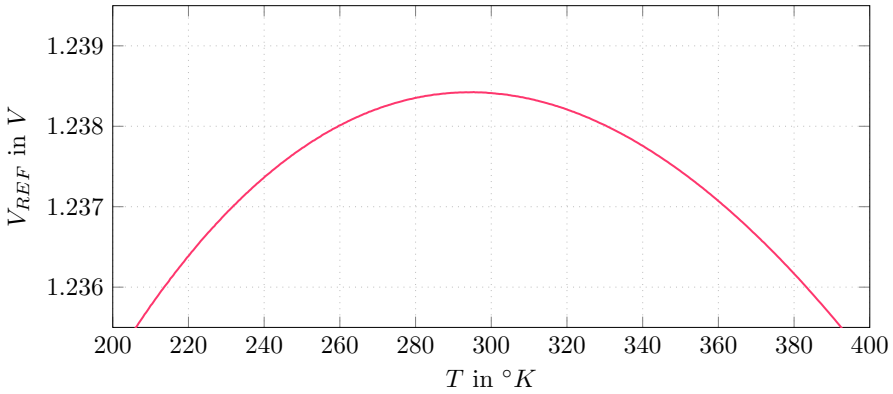


Figure 5.4: Curvature of reference voltage

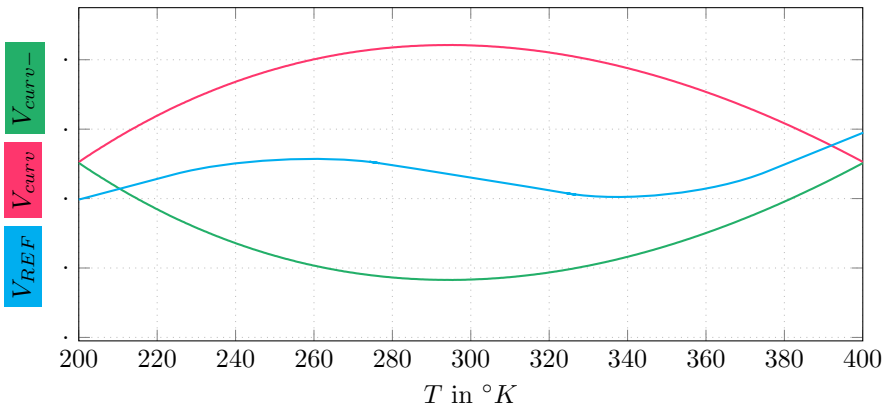


Figure 5.5: Compensation of bandgap curvature

Nowadays, the majority of integrated circuits are fabricated within CMOS processes that lack dedicated vertical bipolar devices. Therefore, a bandgap reference that uses junctions, which can be easily fabricated by any CMOS

[6] when doing a series expansion

process, was developed, [BSU+99]. Within this circuit the reference voltage is not fixed and can be used for low voltage operation as this is a requirement in modern technology nodes. This design uses parasitic PNP transistors[7] and is based on current summing to obtain a temperature compensated reference, depicted in figure 5.6.

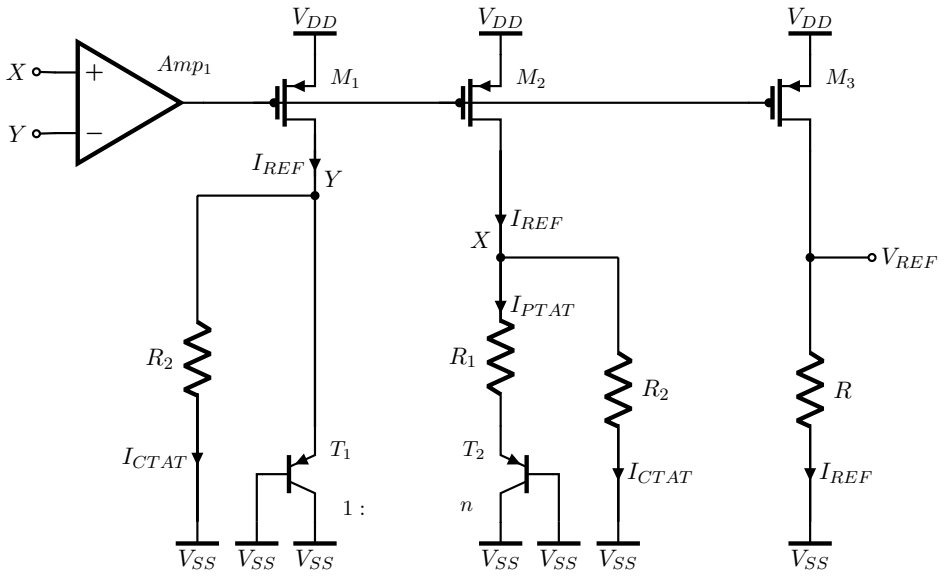


Figure 5.6: Principle of a sub-bandgap circuit

The amplifier forces nodes X and Y to the same potential as it's output controls the equal sized devices M_1 and M_2. Hence, $Y = X = V_{BE1}$ and R_1 defines a PTAT current as $V_{R1} = V_{BE1} - V_{BE2} = \Delta V_{BE12}$ applies.

$$I_{PTAT} = \frac{\Delta V_{BE12}}{R_1} = \frac{V_t}{R_1} \ln(n)$$

The CTAT current I_{CTAT} is defined via the equal sized resistors R_2. As already mentioned $Y = X = V_{BE1}$.

$$I_{CTAT} = \frac{V_{BE1}}{R_2}$$

Hence, I_{REF}, delivered by M_1 and M_2, is the sum of I_{PTAT} and I_{CTAT}.

$$I_{REF} = I_{PTAT} + I_{CTAT} = \frac{1}{R_1} V_t \ln(n) + \frac{1}{R_2} V_{BE1}$$

$$V_{REF} = \frac{R}{R_1} V_t \ln(n) + \frac{R}{R_2} V_{BE1}$$

[7] even in a simple n-well process available

Different to the previous discussed bandgap reference circuits, the CTAT is also scalable. Introducing α_1 and α_2 in reference to figure 5.1 gives:

$$V_{REF}(T) = \alpha_1 V_{BE}(T)_1 + \alpha_2 \Delta V_{BE}(T)_{1/2} =$$

$$= \alpha_1 \left[V_{G0} + \frac{T}{T_0} \left(V_{BE0_1} - V_{G0} \right) + V_t \ln \left(\frac{T}{T_0} \right) (1 - m) \right] + \alpha_2 V_t \ln \left(\frac{J_{C1}}{J_{C2}} \right).$$

Thus, the deviation over temperature can be written as:

$$\frac{\delta V_{REF}}{\delta T} = \alpha_1 \left[\frac{1}{T_0} \left(V_{BE0_1} - V_{G0} \right) + \frac{k_B}{q} \left[\ln \left(\frac{T}{T_0} \right) + 1 \right] (1 - m) \right] + \alpha_2 \frac{k_B}{q} \ln \left(\frac{J_{C1}}{J_{C2}} \right).$$

By setting this equation to zero the optimal ratio of $\frac{\alpha_2}{\alpha_1}$ and the corresponding reference voltage V_{REF} can be calculated for $T = T_0 = 300°K$.

$$\alpha_1 V_{BE0_1} + \alpha_2 \frac{k_B T_0}{q} \ln \left(\frac{J_{C1}}{J_{C2}} \right) = \alpha_1 \left[V_{G0} + (m - 1) \frac{k_B T_0}{q} \right]$$

$$\frac{\alpha_2}{\alpha_1}\Big|_{T=T_0=300°K} = \frac{\frac{V_{G0} - V_{BE0_1}}{V_t} + m - 1}{\ln \left(\frac{J_{C1}}{J_{C2}} \right)}$$

$$V_{REF}\Big|_{T=T_0=300°K} = \alpha_1 \left[V_{G0} + (m - 1) \frac{k_B T_0}{q} \right]$$

As a consequence, the absolute value of V_{REF} is not fixed anymore. Therefore, such bandgap circuits give freedom to design for low reference voltages, while keeping the $\frac{\alpha_2}{\alpha_1}$ ratio at it's optimum. This design approach is used in many modern semiconductor processes that get more and more limited by lower supply voltages[8]. Going back to the voltage expression of the circuitry and it's equations, the following design expressions are given.

$$\frac{R_2}{R_1} = \frac{\frac{V_{G0} - V_{BE0_1}}{V_t} + m - 1}{\ln (n)}$$

has to be met to achieve first order temperature compensation with

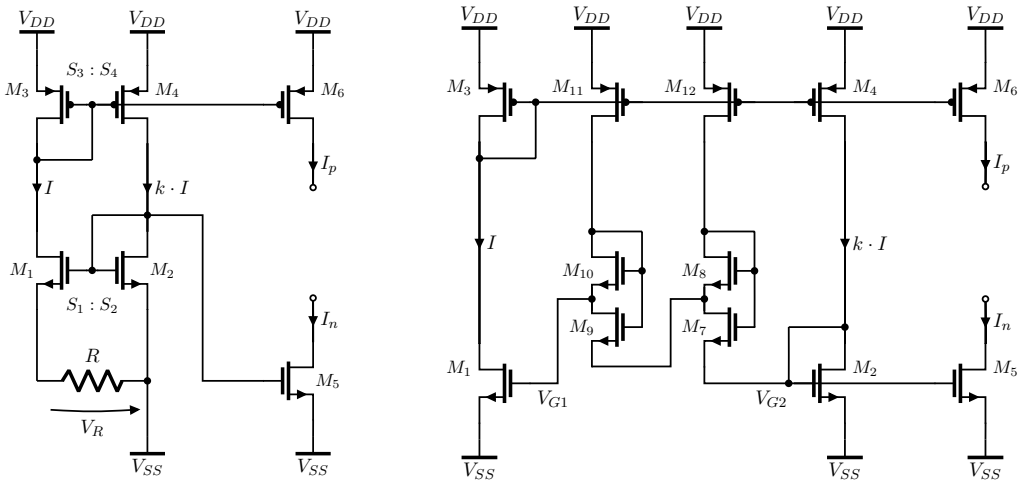
$$V_{REF}\Big|_{T=T_0=300°K} = \frac{R}{R_2} \left[V_{G0} + (m - 1) \frac{k_B T_0}{q} \right]$$

as the absolute value of the reference voltage V_{REF}.

[8] in 2017 TSMC announced a 7nm CMOS platform that operates down to $0.5V$

5.1.2 CMOS current reference

Nowadays, for economic reasons, analog circuits has often to be designed without bipolar transistors as more process steps are required. Especially, if only MOS transistors are used, the creation of CTAT and PTAT behaviour is difficult. Therefore, devices are often biased within the weak inversion regime. Main relationships and reasons can be found in subsection 6.3. In general, current references are derived from voltage references by means of an additional voltage to current converter. The easiest way to convert voltage into current is by the use of a resistor, shown in figure 5.7a and in reference to [VF77]. The transistors M_1 and M_2 are operating in weak inversion and therefore the PTAT voltage V_R and current I is given by:



(a) PTAT current generation

(b) MOS-only circuit

Figure 5.7: Known current reference principles

$$V_R = V_t \ln\left(\frac{S_1}{S_2}\frac{S_4}{S_3}\right)$$

$$I = \frac{V_R}{R}.$$

Where V_t is the thermal voltage, equal to $\frac{k_B T}{q}$, and S_i are aspect ratios $\frac{W_i}{L_i}$ of corresponding MOS devices. The current I can be reproduced by further current mirrors, M_3 and M_6 for current sourcing or M_2 and M_5 for current sinking.

Anyway, the use of a resistor as current defining element has some drawbacks as the absolute value has a high tolerance and in most cases it's temperature coefficient is not well defined, or is wrong signed. This makes it difficult to apply compensation schemes. For very low currents within the nA range a

high resistance is needed that occupies a lot chip area. Another approach that can be implemented just with MOS transistors is shown in figure 5.7b, [SES88]. The gate voltage difference between M_1 and M_2, $V_{G1} - V_{G2}$ has PTAT characteristics. Various transistor pairs like M_9 and M_{10}, that are biased in weak inversion, are used to form a floating PTAT voltage source out of stacked drain-source voltages, [VN79]. The PTAT voltage V_{PTAT} of one pair, in reference to figure 5.7b, can be written as follows.

$$V_{DS9} = \frac{k_B T}{q} \ln\left(1 + \frac{S_{10}}{S_9}\frac{I_9}{I_{10}}\right)$$

$$V_{PTAT} = V_{G1} - V_{G2} = V_{DS9} + V_{DS7} + \ldots$$

Transistors M_1 and M_2 are biased in strong inversion and their threshold mismatch can be minimized as the floating voltage source is inserted between the gates, [VN79]. The mobility and therefore the process transconductance parameter K has a temperature dependency of:

$$K = K_0 \left(\frac{T}{T_0}\right)^{-m}.$$

With m as a process parameter and K_0 the process transconductance at $T = T_0$. As the current in strong inversion follows the squared PTAT voltage, an overall temperature dependency of T^{2-m} can be obtained, [SES88].

$$I = \frac{K_1}{2}\frac{(V_{PTAT} - V_{TH1} + V_{TH2})^2}{\left(1 - \sqrt{M}\right)^2}$$

with V_{TH1} and V_{TH2} as threshold voltages and

$$M = \frac{S_1}{S_2}\frac{S_4}{S_3}.$$

Within this design approach the accuracy of the reference current I is mainly limited due to the tolerance of process transconductance, rather than the resistor tolerances. This is beneficial if no process trimming can be applied and therefore smaller tolerance is required.

5.2 Comparator

This chapter deals with well-known comparator structures. Most comparators use a transconductance stage at the input that converts a differential input voltage into a differential current. This current feeds a latch that switches to a low or high state within the digital domain. Hence, comparators act as a interface between the analog and digital world.

5.2.1 Clocked comparator

In clocked comparators as their name implies a clock source is used to define the point in time when the decision is made. The clock period T_{clk} is divided into a evaluation-phase and reset-phase, giving the comparator time to recover. During the evaluation-phase the comparator reacts to it's input signals, makes a decision and gives after a certain delay t_d a digital output signal. By increasing the clock frequency the comparator circuit has to get faster as the evaluation and reset-phase are reduced, seen in figure 5.8.

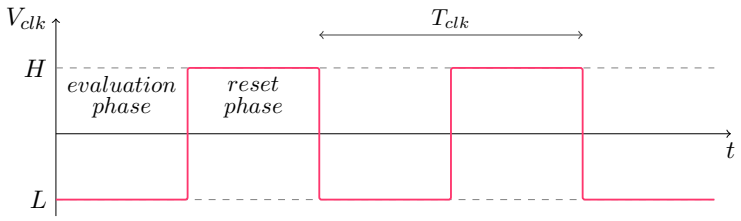


Figure 5.8: Clock signal comparator

Figure 5.9a shows a simple clocked comparator circuit with a differential pair M_8 and M_9, in combination with the current source I_{BIAS}, that acts as input stage. This input stage is loaded by diode-connected pMOS devices M_7 and M_6, that form together with M_3 and M_4 current mirrors to connect to the cross-coupled devices M_1 and M_2. Through this constellation a positive feedback and consequently a latch is formed. Please consider that high performance comparators usually in addition use pre-amplifiers to decrease the offset voltage of the latch and enhance together with a buffer stage the gain and delay time of a comparator. When the clock signal goes high, the output nodes V_{out+} and V_{out-} are shorted by the switch M_5 to reset the circuit and give the latch time to recover. By applying a negative edge to the clock signal, the comparator enters the evaluation phase and the latch is set free to initialize the next decision.

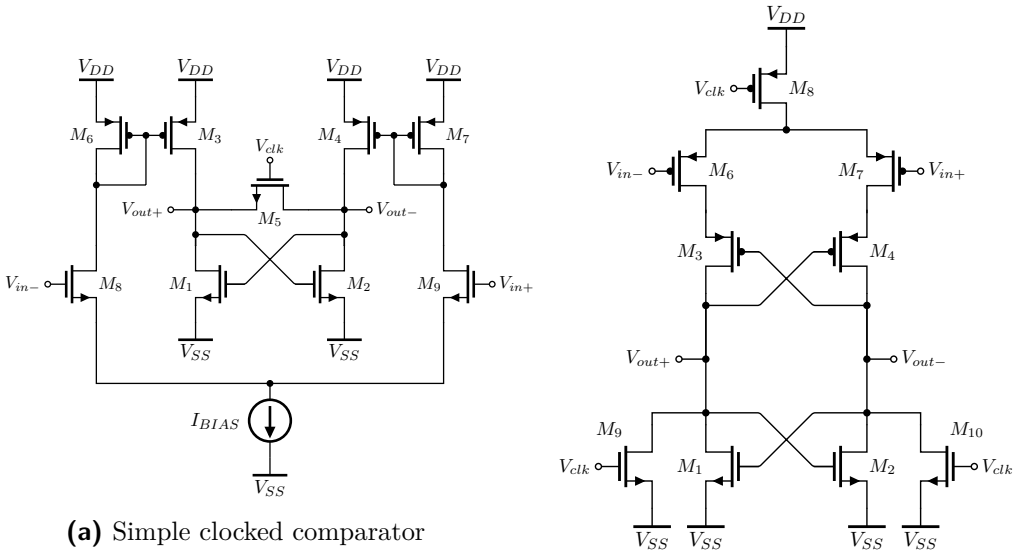
The comparator's output voltage V_{out} grows roughly exponential till it reaches the desired voltage level, [Man90].

$$V_{out} = V_{in}A \cdot e^{\frac{t}{\tau}}$$

Where, A is the initial circuit gain during the evaluation phase and τ is a circuit constant, composed out of the load capacitance C_{out} and the effective transconductance of the latch $g_{m_{eff}}$.

$$\tau = \frac{C_{out}}{g_{m_{eff}}}$$

It can be seen that the input voltage V_{in} affects the time that is needed by the comparator to reach a certain digital output voltage level V_{out}. As the clock period and therefore the evaluation phase is fixed in most designs, there is a minimum input voltage that can be detected by the comparator. The



(a) Simple clocked comparator

(b) Popular clocked comparator

Figure 5.9: Common clocked comparator circuits

effective gain A_{eff} of the circuit during the evaluation phase can be written as:

$$A_{eff} = \frac{V_{out}}{V_{in}} = A \cdot e^{\frac{t}{\tau}}.$$

A_{eff} increases exponential with time t, due to the positive feedback of the latch. Hence, lowering the time-constant τ for a given evaluation phase decreases the voltage resolution Q of clocked comparators. By integration of the effective gain over the time-slot of the evaluation phase T_{ep}, the expression for Q can be obtained for an output swing ΔV_{out} that is required to reach a desired logic level.

$$Q = \frac{\Delta V_{out}}{A} \frac{\frac{T_{ep}}{\tau}}{e^{\frac{T_{ep}}{\tau}} - 1}$$

Therefore, by increasing the $\frac{T_{ep}}{\tau}$-ratio the voltage resolution Q can be minimized. To minimize τ, that is inversely proportional to the circuits gain-bandwidth-product, the designer can follow similar design approaches as for continuous-time amplifiers. To extract the time-constant τ out of simulations, the transient behaviour of the output nodes is observed while varying the input voltage step size.

$$\Delta t = t_2 - t_1 = \ln\left(\frac{V_{in_1}}{V_{in_2}}\right)\tau$$

Here, V_{in1} and t_1 are the input voltage step size and the time when the output crosses the midpoint for the first transient simulation, and V_{in2} respectively

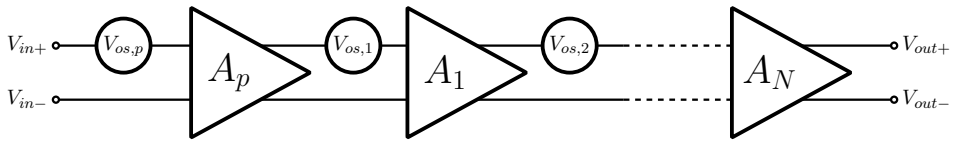


Figure 5.10: Multi stage comparator

t_2 for the second one. This analysis should be done for different step sizes to ensure that the accuracy of the simulator is not limiting.

Till now, only a single latch stage has been considered. As already mentioned, for high performance comparators usually a pre amplifier and N latch stages are used. This concept is illustrated in figure 5.10. The enhanced effective gain A_{eff} can be written as follows.

$$A_{eff} = \frac{V_{out}}{V_{in}} = A_p \sum_{i=1}^{N} A_i \cdot e^{\frac{t_i}{\tau_i}}$$

with

$$\tau_i = \frac{C_i}{g_{mi_{eff}}}$$

Where, A_p is the gain of the pre-amplifier, A_i the gains of single latches and τ_i the corresponding time-constants. t_i is the duration of the evaluation phase for each latch and usually equal as they are clocked synchronously. The use of a pre-amplifier is also benefiting the total offset voltage V_{os}. Offset voltages of the individual stages are named $V_{os,n}$, seen in figure 5.10.

$$V_{os}^2 = V_{os,p}^2 + \left(\frac{V_{os,1}}{A_p}\right)^2 + \sum_{n=2}^{N} \left(\frac{V_{os,n}}{A_p \prod_{i=1}^{n-1} A_i}\right)^2$$

The offset of CMOS latches, especially with small devices, can be large as cross-coupled MOS transistors have large V_{GS} voltages. One can see that the first stage, which might be the main contributor of the total offset voltage, benefits a lot from the use of a pre-amplifier. The pre-amplifier should be designed in such a way that the overall offset voltage is minimized, while keeping high speed operation.

Single-tail comparator

Clocked comparators usually aim low power consumption and high gain to maximize the input voltage resolution. Thus, the circuit of figure 5.9a is not the preferred solution because the bias current I_{BIAS} adds to the static power consumption. A popular structure that consumes no static power

and is used within several comparator circuits is seen in figure 5.9b and in reference to [KNSF93], [WY04]. In the literature this clocked regenerative circuits are called single-tail latched comparators and can be designed for low power consumption and fast speed, [GZ09]. During the reset phase, the clock signal V_{clk} is high and the tail transistor M_8 is opened preventing any current flow. Transistors M_9 and M_{10} define the voltage level of the output signals during reset and give the initial condition, after the circuit enters the evaluation phase by applying a negative edge to the clock signal. Assuming that $V_{in+} > V_{in-}$, the current in the left branch is more than that in the right one. Therefore, node V_{out+} is charged quicker than node V_{out-}. At some point in time, V_{out+} reaches the threshold voltage V_{Tn} of transistor M_2 and V_{out-} starts to decrease. The difference voltage $V_{out+} - V_{out-}$ is amplified through the positive feedback of the cross-coupled devices M_1, M_2 and M_3, M_4 to full logic level and the latch has made it's decision. If $V_{in+} < V_{in-}$, the same actions take place just in the opposite branch. Hence, the overall delay t_d can be described as the sum of the delay t_0, till the load capacitor C_{out} is charged to the threshold voltage V_{Tn}, and the latching delay t_{latch} of the cross-coupled inverters to reach a certain output voltage swing ΔV_{out}, [WNSL04].

$$t_0 = \frac{2C_{out}V_{Tn}}{I_{tail}}$$

$$t_{latch} = \frac{\overbrace{C_{out}}^{\tau}}{g_{m_{eff}}} \ln\left(2\frac{\Delta V_{out}}{\Delta V_0}\right)$$

After t_0 the voltage difference at the output nodes is equal to ΔV_0, the cross-coupled inverters imply positive feedback and take t_{latch} to amplify the output voltage to ΔV_{out}. The output voltage transfer characteristics for ΔV_0 can be written as follows, [WNSL04].

$$\Delta V_0 = V_{Tn}\sqrt{\frac{8K_p}{I_{tail}}}\Delta V_{in}$$

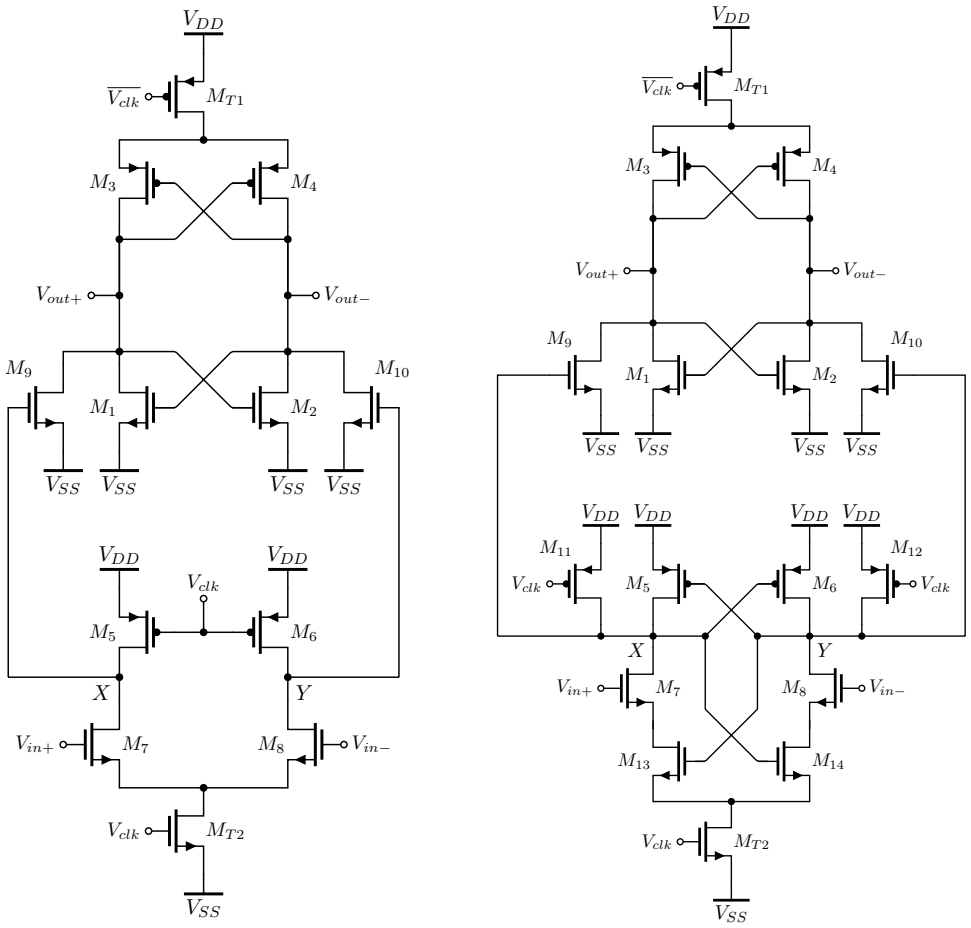
ΔV_{in} is the differential input voltage of the comparator and K_p the transconductance factor of the pMOS input devices. Thus, the expression of the overall delay can be written as:

$$t_d = \frac{2C_{out}V_{Tn}}{I_{tail}} + \frac{C_{out}}{g_{m_{eff}}} \ln\left(\frac{1}{V_{Tn}}\sqrt{\frac{I_{tail}}{2K_p}}\frac{\Delta V_{out}}{\Delta V_{in}}\right).$$

Double-tail comparator

The single-tail circuit requires large voltage headroom, due to the stack of transistors and the limiting effect of the current I_{tail} within the input and

latch stage. An alternative is to use two tail transistors and split the input and latch stage to enhance performance, [SMK+07]. This enables a large current in the latching stage for fast switching and a small current in the input stage to minimize offset.



(a) Double tail comparator

(b) Enhanced version

Figure 5.11: Double-tail comparator circuits

Figure 5.11a shows the main idea of the double-tailed comparator. The input and latching stage don't share any current path, but are coupled via transistor M_9 and M_{10}. During the reset phase the clock signal V_{clk} is low and the nodes X and Y are pulled to V_{DD}, while the tail transistors M_{T1} and M_{T2} turned off. Therefore, the nodes V_{out+} and V_{out-} are getting close to V_{SS} and give the initial condition, before the evaluation phase is entered by applying a positive edge to the clock signal. When the clock signal V_{clk} goes high the evaluation phase is entered and the tail transistors turn on. The common mode voltage at the nodes X and Y starts to drop with a rate of $\frac{I_{M_{T2}}}{C_{X,Y}}$ and a differential voltage ΔV_{XY} that is dependent on the differential input voltage ΔV_{in} will build up between them. As the common mode voltages of X and Y

start to decrease, the transistors M_9 and M_{10} get less conductive and start to release the output nodes from V_{SS} and pass ΔV_{XY} to the latch. The positive feedback of the latch starts to regenerate the voltage difference. This circuit implies less kickback noise as M_9 and M_{10} provide additional shielding between the latching stage and the input nodes.

The delay t_0 till one nMOS transistor reaches it's threshold voltage V_{Tn} and the general definition of the latch delay t_{latch} have been discussed before. In addition, the transfer characteristics of the input voltage ΔV_{in} to the latch circuit after $t = t_0$ can be written as:

$$\Delta V_0 = \frac{4V_{Tn}^2}{I_{M_{T1}}^2} \frac{C_{out}}{C_{X,Y}} g_{m_{7,8}} g_{m_{9,10}} \Delta V_{in}.$$

Where, $g_{m_{7,8}}$ is the transconductance of input and $g_{m_{9,10}}$ of the coupling devices. $C_{X,Y}$ is the capacitive load at node X and Y, C_{out} the load capacitance of the latch and $I_{M_{T1}}$ the current delivered by the tail transistor M_{T1}. The overall delay of this comparator therefore can be expressed as:

$$t_d = \frac{2C_{out}V_{Tn}}{I_{M_{T1}}} + \frac{C_{out}}{g_{m_{eff}}} \ln\left(\frac{I_{M_{T1}}^2}{2V_{Tn}^2} \frac{C_{X,Y}}{C_{out} g_{m_{7,8}} g_{m_{9,10}}} \frac{\Delta V_{out}}{\Delta V_{in}}\right).$$

Of course the delay time t_d is also dependent on the tail current $I_{M_{T2}}$ of the input stage, as it's transconductance $g_{m_{7,8}}$ is equal to $\sqrt{2K_n I_{M_{T2}}}$. And as already mentioned for this structures it is preferable to use a small current in the input stage, to benefit the overall offset voltage and shifting most of the required gain into the fast latching stage. By transistor sizing, the optimal timing of the individual phases and an optimal operation point can be achieved.

A enhanced version of the double-tail comparator can be seen in figure 5.11b. Positive feedback was added to the input stage to speed up the circuit and decrease the delay with reduction of static current consumption, but on the other hand kick-back noise is increased. During the reset phase the X and Y node as well as the output nodes are defined in the same way as for the conventional dual-tail comparator. The idea is to increase the regenerative effect of the upper latch by increasing the differential voltage ΔV_0, available after $t = t_0$, by an additional latch within the input stage.

$$\Delta V_0 = \frac{4V_{Tn}|V_{Tp}|}{I_{M_{T1}} I_{M_{T2}}} g_{m_{7,8}} g_{m_{9,10}} \Delta V_{in} e^{\frac{t_0}{\tau_2}}$$

with

$$\tau_2 = \frac{C_{X,Y}}{g_{m_{eff,2}}}$$

and

$$t_0 = \frac{2C_{out}V_{Tn}}{I_{M_{T1}}}$$

Where, $g_{m_{7,8}}$ is the transconductance of input and $g_{m_{9,10}}$ of the coupling devices. $C_{X,Y}$ is the capacitive load at node X and Y and C_{out} the load capacitance of the output latch. $I_{M_{T1}}$, $I_{M_{T2}}$ are the tail currents and $g_{m_{eff,2}}$ is the effective transconductance of the latch within the input stage. V_{Tn} respectively V_{Tp} are threshold voltages of the MOS devices. The overall delay of this comparator therefore can be expressed as follows.

$$t_d = \frac{2C_{out}V_{Tn}}{I_{M_{T1}}} + \overbrace{\frac{C_{out}}{g_{m_{eff,1}} + g_{m_{9,10}}}}^{\tau} \ln\left(\frac{I_{M_{T1}}I_{M_{T2}}}{2V_{Tn}|V_{Tp}|}\frac{1}{g_{m_{7,8}}g_{m_{9,10}}e^{\frac{t_0}{\tau_2}}}\frac{\Delta V_{out}}{\Delta V_{in}}\right)$$

Here, the effective transconductance of the output latch is named $g_{m_{eff,1}}$ and it can be seen that it's overall time constant τ is decreased, compared to the conventional double-tail comparator.

The input latch devices M_5 and M_6 add an additional current path to the input stage. As soon as this circuit detects a voltage difference between the nodes X and Y, the regeneration process starts and one node is pulled back to V_{DD}. Hence, this transistor turns on and a current path to V_{SS} is enabled. This would result in static current consumption, destroying the power-efficiency of the circuit. To overcome this issue, devices M_{13} and M_{14} are added to cut down this conductive path. Table 5.1 gives some values concerning power consumption and delay of the individual clocked comparator structures, [GY14].

Structure	Delay	Power consumption
Single-tail	$7ns$	$66\mu W$
Conventional double-tail	$7.5ns$	$15\mu W$
Advanced double-tail	$7.3ns$	$12\mu W$

Table 5.1: Clocked comparator benchmark

It has to be said that clocked latch-type comparators are very fast and power-efficient, but mismatch and noise can lead to wrong decision making, if the input voltage difference is small. Further, in absence of clock signals they are not operational and therefore they are unsuitable for the concept of the dual-phase low-power oscillator.

5.2.2 Continuous-time comparator

In contrast to clocked comparators, the output of an continuous-time comparator is updated any-time the input voltage changes. Usually clocked comparator structures achieve lower power consumption, as they don't need to track the input continuously through their clock triggered nature. Continuous-time comparators are designed in the same way as common amplifier circuits but without applying any negative feedback. They are proposed to work in open-loop and are designed to have high gain to get good input voltage sensitivity as well as to have high bandwidth to decrease the settling time. Thus, delay time necessary to reach valid logic levels is also decreased.

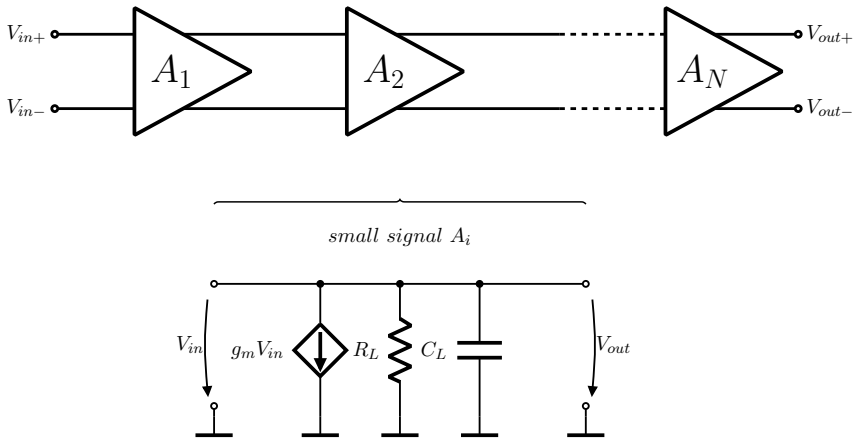


Figure 5.12: Small signal behaviour of comparator

Considering a single pole open loop amplifier, depicted in figure 5.12, the step response of the output voltage V_{out} is given by the following well-known equation:

$$V_{out} = V_{in} A_0 \left(1 - e^{-\frac{t}{\tau}}\right).$$

The DC gain A_0 is equal to $g_m R_L$ and τ is equal to $C_L R_L$. Therefore the expression can be simplified for small signals with $t << \tau$ to:

$$V_{out} \approx V_{in} A_0 \left(\frac{t}{\tau}\right) = V_{in} \frac{g_m}{C_L} t.$$

By integration over time t, the transfer function for N cascoded single-pole stages, seen in figure 5.12, can be found.

$$V_{out} = V_{in} \left(\frac{g_m}{C_L}\right)^N \frac{t^N}{N!}$$

Rearranging the terms gives the time t needed to amplify the input signal V_{in} to V_{out}.

$$t = \frac{C_L}{g_m} \left(N! \frac{V_{out}}{V_{in}}\right)^{\frac{1}{N}}$$

Thus, for a certain $\frac{V_{out}}{V_{in}}$-ratio, or gain, a optimal number of stages N can be chosen.

Figure 5.13 shows how the normalized delay $t\frac{g_m}{C_L}$ varies with number of stages. It can be seen that two to three stages usually get low delay, while keeping circuit complexity and therefore area consumption low. The higher the desired gain factor, the more preferable it is to add more stages. From figure 5.14 it can be seen that the normalized delay increases over desired

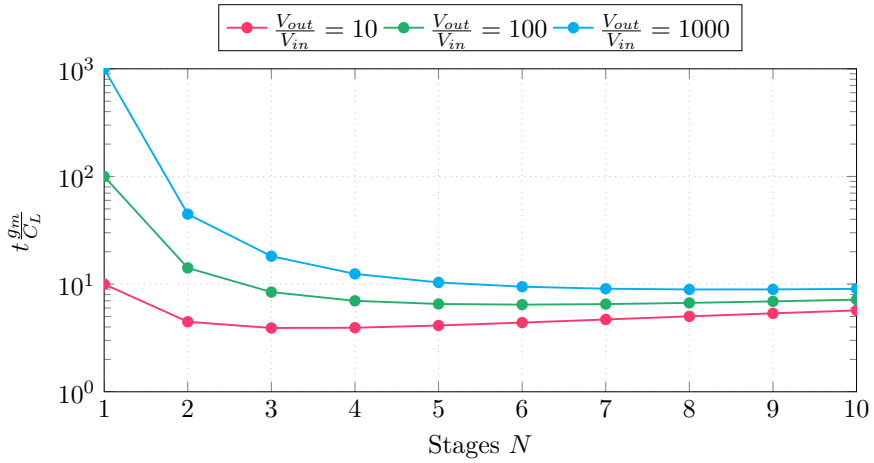


Figure 5.13: Number of stages vs. normalized delay

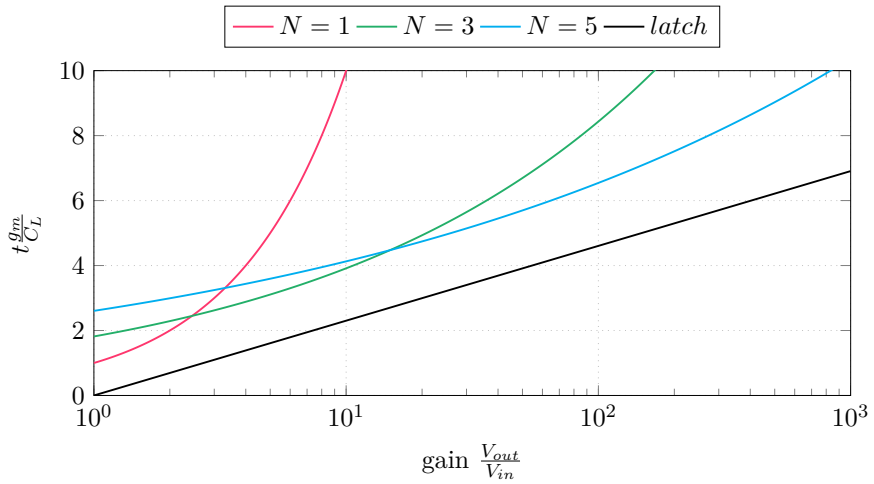


Figure 5.14: Gain vs. normalized delay

gain factor. Therefore, a large N is needed for high gain factors to keep the delay low. It can also be seen that a latching stage that includes positive feedback always outperforms a basic continuous-time circuit as it regenerates faster, with $t_{latch} = \frac{C_L}{g_m} \ln\left(\frac{V_{out}}{V_{in}}\right)$.

Hence, also in continuous time comparators positive feedback can be used to speed up operation. Practically, uncompensated two-stage amplifiers are suitable for high-gain, open-loop comparators. The poles of this circuits are designed to be much larger than the dominant pole of a typical compensated operational amplifier and therefore they have a much faster linear response, due to higher circuit bandwidth. Depending on the load capacitor, a fast transient response can only be achieved, if the circuit has no slew rate limitation. A very simple continuous-time comparator can be seen in figure 5.15. A differential pair loaded by diode-connected transistors M_3 and M_4 forms the input stage. This circuit is well-known and compared to a traditional

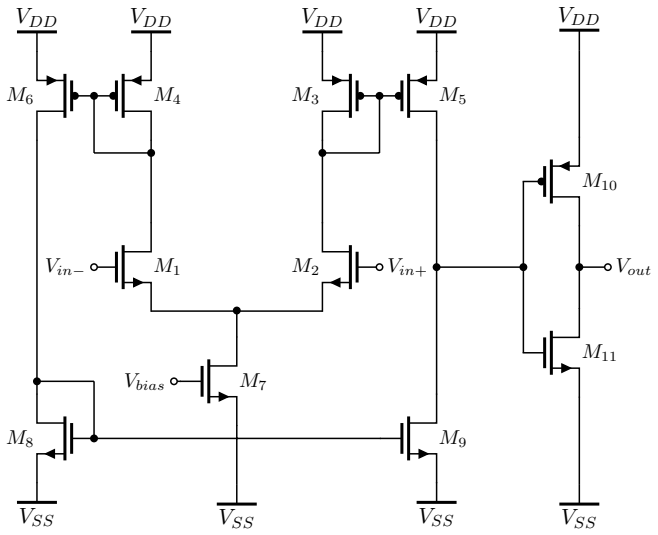


Figure 5.15: Simple continuous-time comparator

structure, with a current mirror load, this avoids slew rate limitation within the first stage, as the signal swing is decreased. The push-pull output of the second stage, M_5 and M_9, in combination with the buffer circuit makes this circuit able to provide a very high slew rate at the output node V_{out}. A modified version of this comparator is seen in figure 5.16, [WDJF15]. It uses additional circuitry to increase the tail current of the differential pair when the voltage levels are close to the flip point. And therefore it is possible to reduce the overall power consumption, while keeping the delay time low. The dc gain A, the bandwidth BW and the gain-bandwidth product GBW of the two stage[9] circuit can be written as follows.

$$A = g_m k_1 \left(r_{ds5} || r_{ds9}\right)$$

$$BW = \frac{1}{2\pi \left(r_{ds5} || r_{ds9}\right) C_X}$$

$$GBW = k_1 \frac{g_m}{2\pi C_X}$$

With $k_1 = \frac{S_6}{S_4} = \frac{S_5}{S_3}$ as the current gain factor, g_m the transconductance of the input stage, r_{ds} the corresponding drain-to-source resistance and C_X the capacitive load at node X. Please note that k_1 can not be increased to very high value, as the capacitive load at the drains of the input transistors M_1 and M_2 increases. The corresponding non-dominant pole would decrease and start to make the circuit slow. The transconductance g_m is proportional to the square root of the tail current I_{tail}.

[9] inverter not included

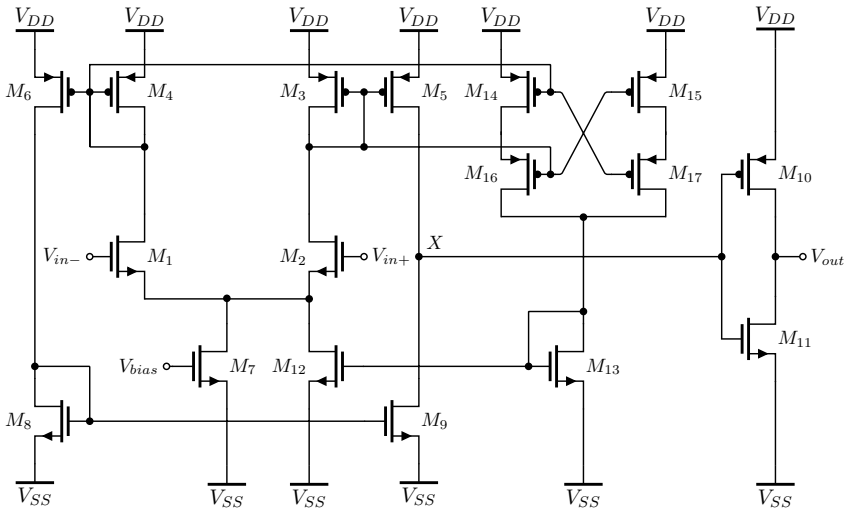


Figure 5.16: Modified continuous-time comparator

The tail current can be written as the sum of currents provided by M_7 and M_{12}.

$$I_{tail} = I_7 + I_{12}$$

The current provided by M_{12} can be expressed as:

$$I_{12} = I_7 \frac{k_2}{2 - k_2}.$$

Where k_2 is the radio of $\frac{S_{14}}{S_4} = \frac{S_{16}}{S_3}$. It can be seen that it is important to choose k_2 in such a way that I_{12} convergences. Otherwise the overall tail current will get very large and a oscillation may occur.

For the comparator circuit of the proposed oscillator a similar adaptive biasing scheme has been implemented, seen in the following section.

Chapter 6

Design Methodology

This chapter gives information about the design methodology used throughout this thesis. Beside simulations with embedded BSIM[1] models, provided by the foundry's design kit, an easy approach was found by the use of a compact model with reduced parameters. This model is called ACM and it is an effective tool to do initial hand design. The main parameters for the hand calculations can be extracted from the BSIM model. Here, the term of inversion coefficient has been found to be very useful to achieve a low power design including devices in different inversion regions, especially for the designed reference generator. As weak inversion gives some special properties, this is discussed in short within this chapter. The final circuit design has been simulated with the BSIM model that has been developed over many years and gives very accurate results. It is optimized via many parameters to give best matching between simulation and silicon.

6.1 The ACM model

This section gives general information about ACM[2], a compact current-mode MOS transistor model that uses the concept of inversion levels. In reference to [CSGM98]. It is shown that the normalized output characteristic of a long-channel MOS device within this model is independent of technology and transistor dimensions. This makes it usable in modern technologies and valid in the whole inversion regime. The expressions provided by the model are accurate in weak, moderate, and strong inversion and fit well for low voltage and low current applications. As MOS devices have an intrinsic source-to-drain symmetry, [EKV95], the overall drain current can be split into forward and reverse current components. The forward component is a function of the terminal voltages V_G and V_S, while the reverse current is a function of V_G and V_D. Please note that all voltages are referred to the bulk terminal. The normalized forward and reverse components are defined as follows.

[1] Berkeley Short-channel IGFET Model by the BSIM Group
[2] Advanced Compact MOSFET

$$i_f = \frac{I_F}{I_S} = \frac{I(V_G, V_S)}{I_S}$$

$$i_r = \frac{I_R}{I_S} = \frac{I(V_G, V_D)}{I_S}$$

with

$$I_S = \overbrace{\mu n C'_{ox} \frac{V_t^2}{2}}^{I_{S\square}} \frac{W}{L}$$

Where I_S is the specific current determined by multiplying the technology parameter $I_{S\square}$ with $\frac{W}{L}$. μ is the mobility, n the slope factor[3], $V_t = \frac{k_B T}{q}$ the thermal voltage and C'_{ox} is the oxide capacitance per unit area. Depending on which value is larger, i_f or i_r is usually referred as the inversion coefficient and indicates in which inversion regime the device operates. The overall drain current I_D is the superposition of independent and symmetrical effects of the drain and source voltage V_D and V_S, seen in figure 6.1.

$$I_D = I_F - I_R = I_S \left(i_f - i_r\right)$$

Or the integral form in reference to [Tsi87]:

$$I_D = \overbrace{\mu C'_{ox} \frac{W}{L}}^{\beta} \int_{V_S}^{V_D} -\frac{Q_i}{C'_{ox}} dV.$$

Where V is the channel voltage and Q_i is the local mobile inversion charge in the channel. This relationship comes from physical features of the MOS transistor structure. It is based on the charge-sheet model and the relationship between the surface potential and the inversion charge density.

Within the ACM model all static and dynamic transistor characteristics can be expressed as functions of the two inversion coefficients and this gives an easy approach to do hand calculations. As it is a continuous model, it is easy to define the inversion regime the devices are working in, and to obtain if a device is in it's saturation region. An forward inversion coefficient greater than 100 usually indicates strong inversion. Up to $i_f = 1$ the device is in weak inversion and between 1 and 100 moderate inversion is indicated, [CSGM98].

Table 6.1 gives the ACM model's most relevant relationships and figure 6.2 illustrates very important design parameters in respect to the inversion coefficient. V_P is the pinch-off voltage and V_{T0} is the gate threshold voltage for $V = 0$. Only three parameters (I_S, C_{ox} and n) are required to characterize the small-signal behaviour. The majority of analog circuits are current biased and

[3] typical values: 1.2 to 1.6

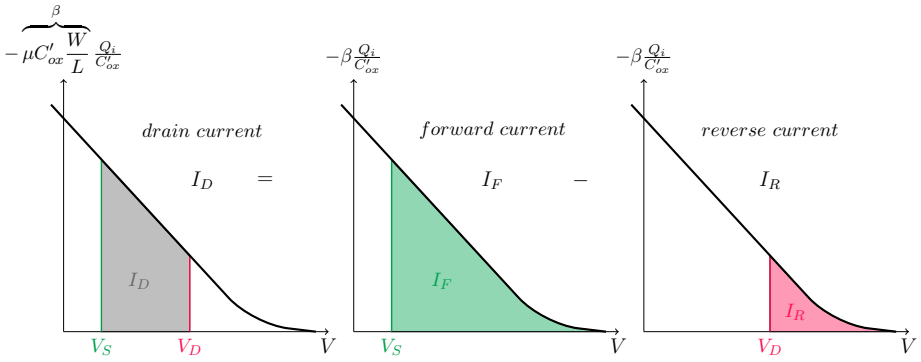
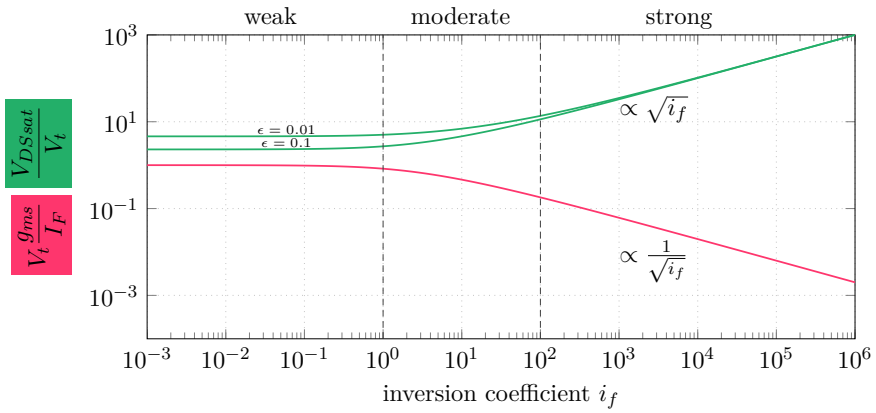


Figure 6.1: drain current components, $V_G = const$

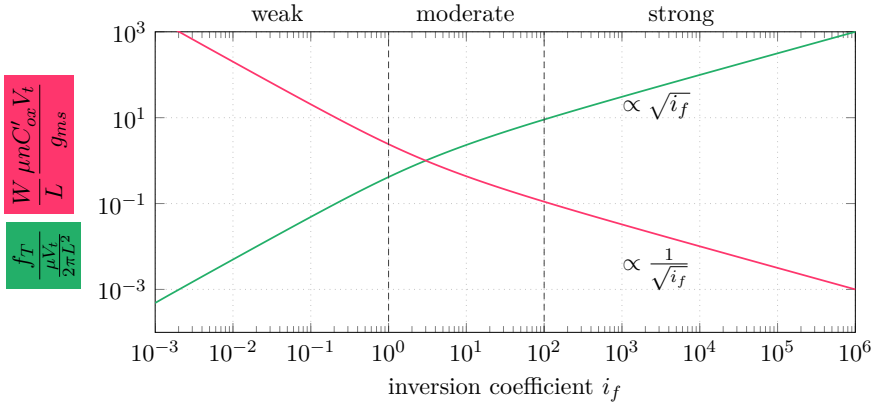
№	Variable	Expression
(1)	$I_D =$	$I_S\,(i_f - i_r)$
(2)	$g_{ms(d)} =$	$\frac{2I_S}{V_t}\left(\sqrt{1+i_{f(r)}}-1\right)$
(3)	$g_{mg} =$	$\frac{g_{ms}-g_{md}}{n}$
(4)	$C_{gs(d)} =$	$\frac{2}{3}C_{ox}\left(1-\frac{1}{\sqrt{1+i_{f(r)}}}\right)\left[1-\frac{1+i_{r(f)}}{\left(\sqrt{1+i_f}+\sqrt{1+i_r}\right)^2}\right]$
(5)	$\frac{V_P-V_{S(D)}}{V_t} =$	$\sqrt{1+i_{f(r)}}-2+\ln\left(\sqrt{1+i_{f(r)}}-1\right)$
(6)	$\frac{V_{DS}}{V_t} =$	$\sqrt{1+i_f}-\sqrt{1+i_r}+\ln\left(\frac{\sqrt{1+i_f}-1}{\sqrt{1+i_r}-1}\right)$
(7)	$\frac{I_{F(R)}}{V_t g_{ms(d)}} =$	$\frac{\sqrt{1+i_{f(r)}}+1}{2}$
(8)	$\frac{V_{DSsat}}{V_t} =$	$\ln\left(\frac{1}{\epsilon}+\sqrt{1+i_f}-1\right)$
(9)	$f_T\frac{2\pi L^2}{\mu V_t} \cong$	$2\left(\sqrt{1+i_f}-1\right)$
(10)	$\frac{W}{L}\frac{\mu n C'_{ox} V_t}{g_{ms}} =$	$\frac{1}{\sqrt{1+i_f}-1}$

Table 6.1: ACM model - important relationships, $C_{ox} = C'_{ox}WL$, $V_P \cong \frac{V_G - V_{T0}}{n}$

this makes all expressions very useful as they are current based. Hence, using the inversion coefficient as the main design variable is a very powerful tool and it is easy to sketch the area consumption as well as the power consumption of a specific design, by the use of equation (7) in combination with (10). Equation (5) gives the main current to voltage relationship and (6) shows that the normalized output characteristics of a MOS device are independent of technology and transistor dimensions. As the current-to-transconductance relationship is essential in most analog designs, (7) is an important expression and is used to extract the specific current I_S out of the measured or simulated current-to-transconductance ratios. Key is that it's independent of gate voltage, transistor dimensions, technology and temperature. The expression (8) gives the boundary V_{DSsat} between the saturation and triode region in terms of inversion coefficient. ϵ is an arbitrary number that is much smaller than one. Figure 6.2a shows that the saturation boundary and the transconductance-to-current ratio are independent of the inversion coefficient



(a) normalized V_{DSsat} and $\frac{g_{ms}}{I_F}$



(b) normalized f_T and $\frac{W}{L}$

Figure 6.2: inversion coefficient as design variable

in weak inversion, while they are direct respectively indirect proportional to it's square root in strong inversion.

The intrinsic cut-off frequency f_T, expressed through equation (9), reflects the frequency capability and therefore the speed of a MOS device. This as well as the geometric ratio expression (10) are represented in figure 6.2b. Often the intrinsic cut-off frequency is chosen to be higher than required due to the lack of appropriate models. This leads to an increase of power consumption not needed to fulfil the specified requirements.

6.2 Model parameters

It is seen in table 6.1 that three parameters I_S, C'_{ox} and n are required to make use of the ACM model's equations. Further, the definition of the threshold voltage V_{T0} is different for this model. As C'_{ox} is a parameter that is given by most technology datasheets, the focus lies on the extraction of $I_{S\square}$, V_{T0} and n. In this subsection the procedure and results of this extraction is shown.

6.2.1 Extraction of V_{T0} and $I_{S\square}$

Starting point is equation (5) of table 6.1 that gives for the forward component

$$\frac{V_P - V_S}{V_t} = \sqrt{1 + i_f} - 2 + \ln\left(\sqrt{1 + i_f} - 1\right).$$

To get a direct relation between the gate voltage V_G and the threshold voltage V_{T0}, the equation is simplified by forcing a forward coefficient of $i_f = 3$ while keeping the source voltage on the same level as the bulk, $V_S = 0$. Hence, the right side term is equal to zero. With $V_P \cong \frac{V_G - V_{T0}}{n}$ is equal to zero it is seen that for $i_f = 3$ and $V_S = 0$ indeed

$$V_G = V_{T0}.$$

To cancel out the thermal voltage V_t, the drain voltage is fixed to $V_D = \frac{V_t}{2}$. Therefore, the reverse component can be written as

$$\frac{1}{2} = \sqrt{1 + i_r} - 2 + \ln\left(\sqrt{1 + i_r} - 1\right).$$

This value set gives an reverse coefficient of $i_r = 2.115$. By applying the reverse and forward coefficient to equation (1), the specific sheet current can be obtained:

$$I_{S\square} = \frac{I_D}{0.885\frac{W}{L}}.$$

In the next step a relation between the threshold voltage and the transconductance-to-drain-current ratio $\frac{g_{mg}}{I_D}$ is found. By substitution of equation (2) into (3) and dividing through (1) the ratio can be written as follows.

$$\frac{g_{mg}}{I_D} = \frac{1}{V_t n} \frac{2}{\sqrt{1 + i_f} + \sqrt{1 + i_r}}$$

Hence, the maximum of $\frac{g_{mg}}{I_D}$ is equal to $\frac{1}{V_t n}$ and reached whenever the inversion coefficients are zero. For the given value set this gives

$$\frac{g_{mg}}{I_D} = \underbrace{\frac{1}{V_t n}}_{\frac{g_{mg}}{I_D},\max} \frac{2}{\sqrt{1+3} + \sqrt{1+2.115}} \cong 0.53 \frac{g_{mg}}{I_D},\max$$

for $V_G = V_{T0}$ and $V_D = \frac{V_t}{2}$. Figure 6.3 shows the principle of extraction. The gate voltage V_G is varied while the drain current and the transconductance-to-drain-current ratio are analysed. As explained above, this results in the finding of V_{T0} and $I_{S\square}$.

Figure 6.5 shows plots for a nMOS and pMOS device. At 0.53-times the maximum of the $\frac{g_m}{I_D}$ curve the threshold voltage V_{T0} is found, with a drain current equal to $I_D = 0.885\frac{W}{L} I_{S\square}$.

The complete value set for the extracted values of $I_{S\square}$ and V_{T0} over different transistor lengths and widths is shown in figure 6.6 and 6.7.

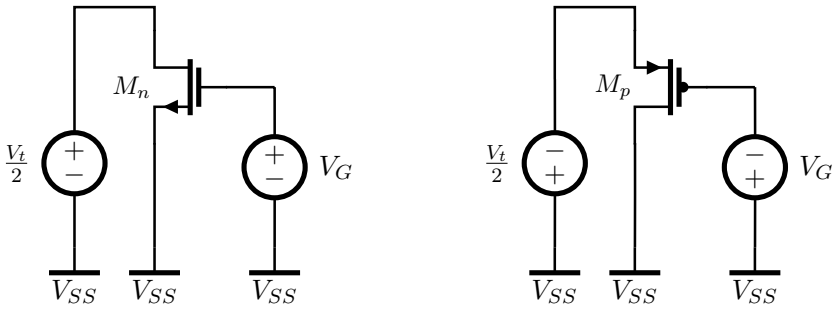


Figure 6.3: Principle of extracting $I_{S\square}$ and V_{T0}. $V_B = V_{SS}$.

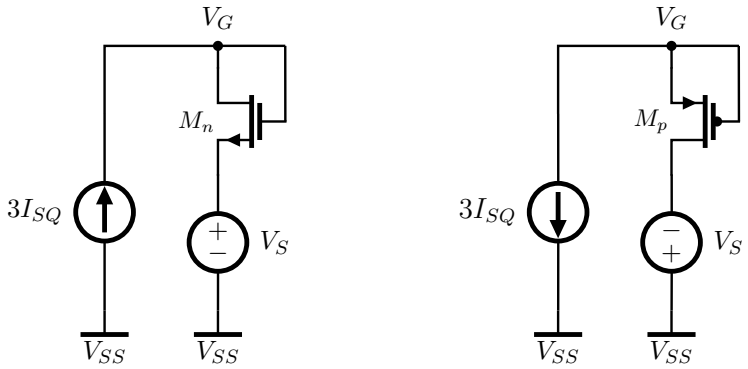


Figure 6.4: Principle of extracting n. $V_B = V_{SS}$.

6.2.2 Extraction of the slope factor n

For the extraction of the slope factor again a forward coefficient of $i_f = 3$ is forced. But different to the previous extraction circuit the MOS devices are connected in diode configuration, by means of $i_f >> i_r$. This is seen in figure 6.4 and therefore the voltage equation (5) can be written as

$$\frac{V_P - V_S}{V_t} = 0.$$

Further, with the voltage $V_P \cong \frac{V_G - V_{T0}}{n}$ it is seen that

$$nV_S = V_G - V_{T0}.$$

By taking the derivative of V_S, the slope factor n can be isolated and as the threshold voltage doesn't vary with respect to V_S, the slope factor can be expressed as

$$n = \frac{dV_G}{dV_S}.$$

The result of this analysis is shown in figure 6.8.

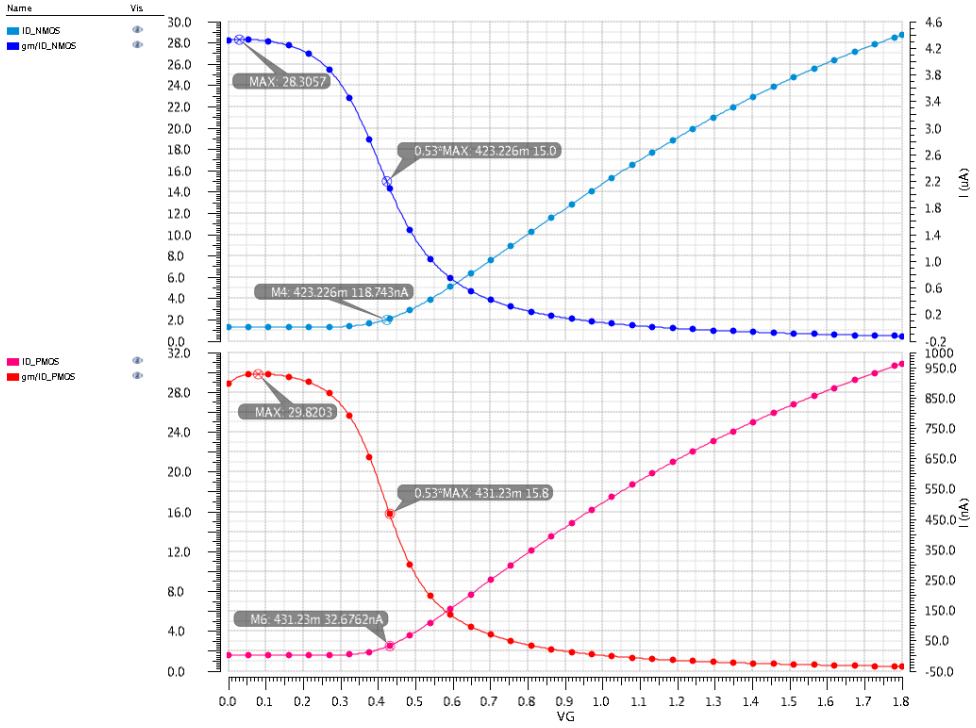


Figure 6.5: Extraction of $I_{S\square}$ and V_{T0} for L=W=10μm

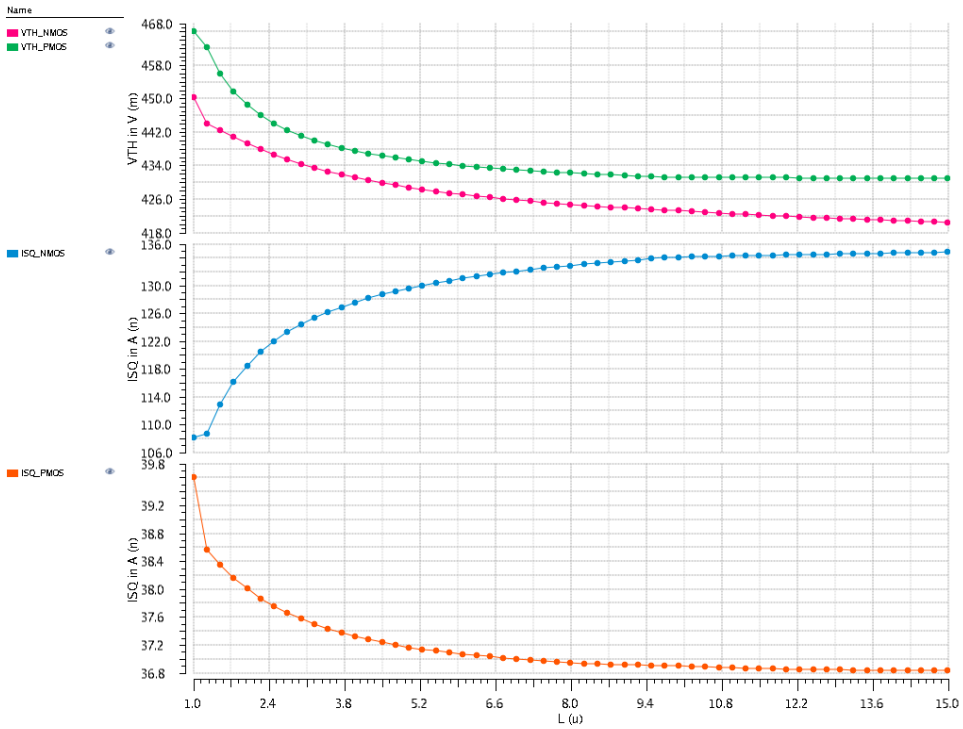


Figure 6.6: Extraction of $I_{S\square}$ and V_{T0} over L. W=10μm.

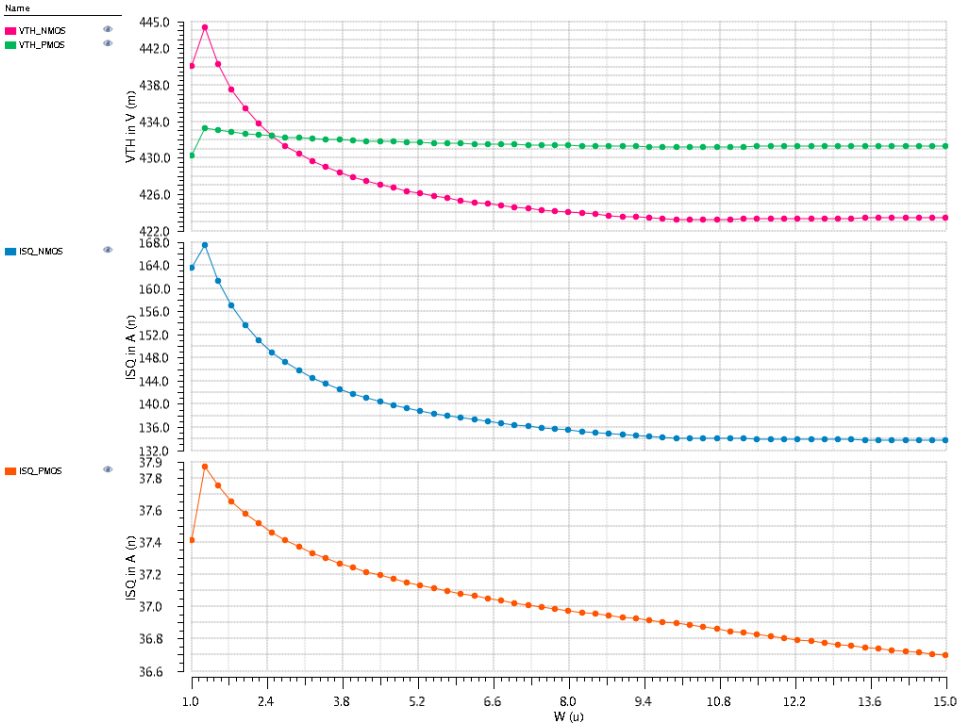


Figure 6.7: Extraction of $I_{S\square}$ and V_{T0} over W. L=10μm.

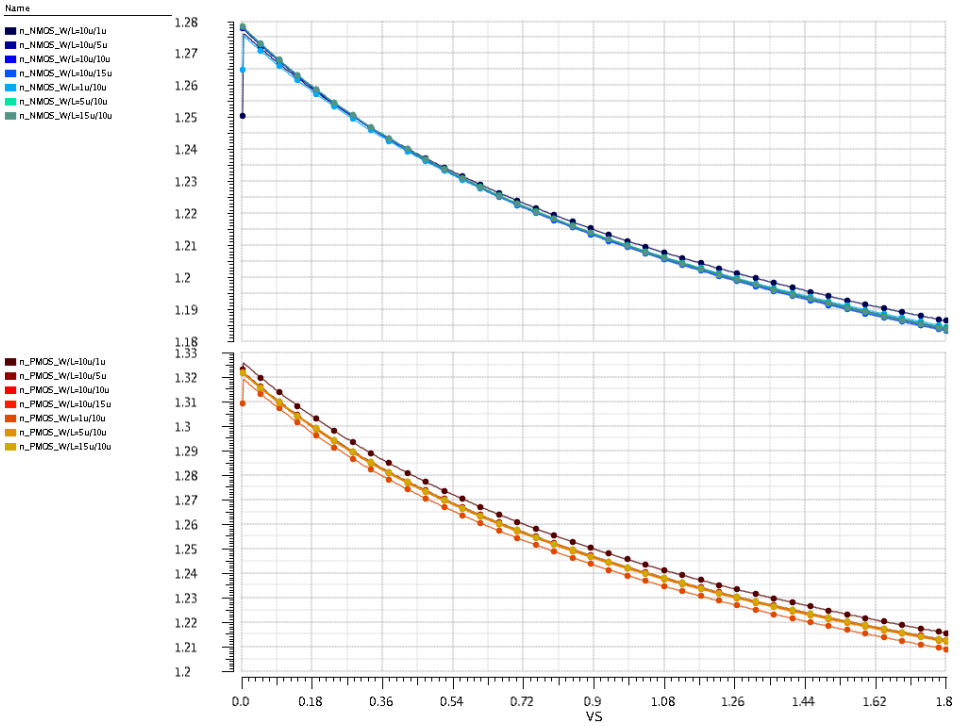


Figure 6.8: Extraction of n over V_S for different sizes

6.3 Features of weak inversion

As discussed in section 6.1, the characteristics of a transistor can be modeled over the whole inversion regime and is different for weak and strong inversion. Designing within the weak inversion regime gives the ability to decrease the overall power consumption, [WCC06]. Some advantages are the exponential characteristics (voltage to current), maximum output swing as the saturation boundaries are a minimum, and maximum $\frac{g_m}{I_D}$-ratio. However, weak inversion designs have drawbacks like low speed and weak current matching (dominated by V_{T0} mismatch), as well as maximum noise content of the drain current. Depending on the function of a MOS device it has to be decided in which inversion regime it has to be biased. A combination of devices working within the weak, moderate and strong inversion region might give the best performance.

The deviation that gives the drain current expression in weak inversion with I_{D0} as a process-dependent constant follows:

$$-\frac{Q_i}{C'_{ox}} = 2nV_t e^{\frac{V_P - V}{V_t}}$$

and with the voltage $V_P \cong \frac{V_G - V_{T0}}{n}$ the drain current expression I_D is given by:

$$I_D = 4I_S e^{\frac{V_G - V_{T0}}{nV_t}} (e^{\frac{-V_S}{V_t}} - e^{\frac{-V_D}{V_t}}) = \underbrace{4I_S e^{\frac{-V_{T0}}{nV_t}}}_{I_{D0}} e^{\frac{V_G}{nV_t}} (e^{\frac{-V_S}{V_t}} - e^{\frac{-V_D}{V_t}}).$$

Rearranging the terms gives the well known expression:

$$I_D = I_{D0} e^{\frac{\frac{1}{n}V_G - V_S}{V_t}} \left(1 - e^{\frac{-V_{DS}}{V_t}}\right).$$

Where, V_G, V_D and V_S are the terminal voltages of a MOS device and V_{DS} the corresponding voltage between drain and source. n is the subthreshold slope factor and V_t the thermal voltage. From the forward characteristics that are related to the current expression, depicted in figure 6.9, it can be seen that V_{DSsat} is in the range of $4 - 6V_t$. The slopes of the logarithmic gate and source transfer characteristics are $\frac{1}{n}$ respectively -1 and this leads to some special properties within weak inversion: Similar to bipolar devices it is possible to extract a voltage that is proportional to the thermal voltage, to be used within voltage and current references. The exponential relationship is also used for amplitude regulators and log-domain filters. As the saturation voltages are at their minimum, very low voltage designs can be achieved if the threshold voltage is sufficient low.

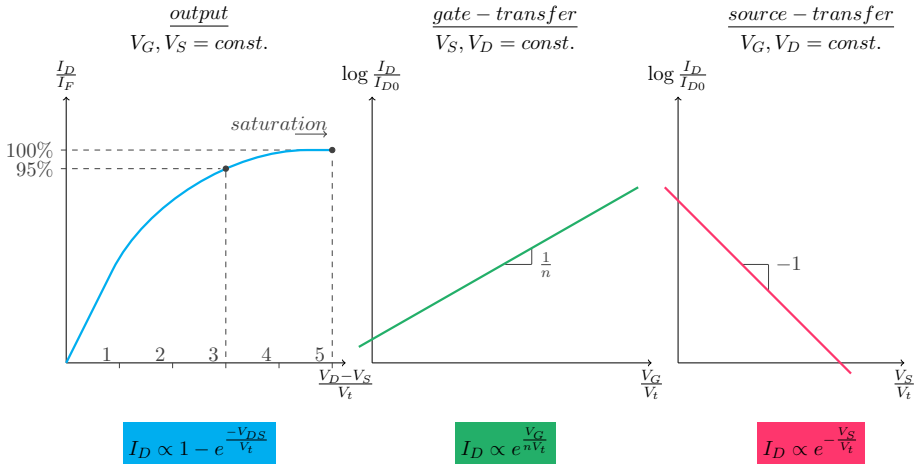


Figure 6.9: Forward characteristics

Chapter 7

Reference Generator

A major challenge of the proposed low power oscillator is the design of a voltage and low current reference circuit. The main objective is to establish a dc voltage and current, while compensating the oscillator's period over temperature. Beside the delay introduced by the comparator and temperature coefficient of the capacitor, this circuit influences the frequency change over temperature the most.

This chapter deals with a novel reference generator design that was implemented throughout this thesis. It is a circuit that provides a compensated reference voltage V_{REF} for the comparators, as well as a compensated reference current I_{REF} to charge the capacitors of the integrator block. To prevent high power consumption it was essential to keep this block as simple as possible, while getting low temperature coefficients to satisfy the oscillator's requirements.

7.1 Principle and schematics

The core of the proposed reference circuit is a self-biased CMOS structure with M_5 and M_6 working in weak inversion, seen in figure 7.1. All other devices are biased in strong or moderate inversion while the drain-to-source voltage of M_2 and M_3 is limited to keep them in their linear region. By the elimination of resistance as voltage to current converter, the total process spread is reduced. The schematics of the reference generator is depicted below. The start-up circuit that is connected to nodes X, Y and Z is discussed in subsection 7.4.

7.2 Derivation of design equations

The drain current equations for saturation-, linear- and subthreshold- region are shown below. Please note that channel length modulation was not considered.

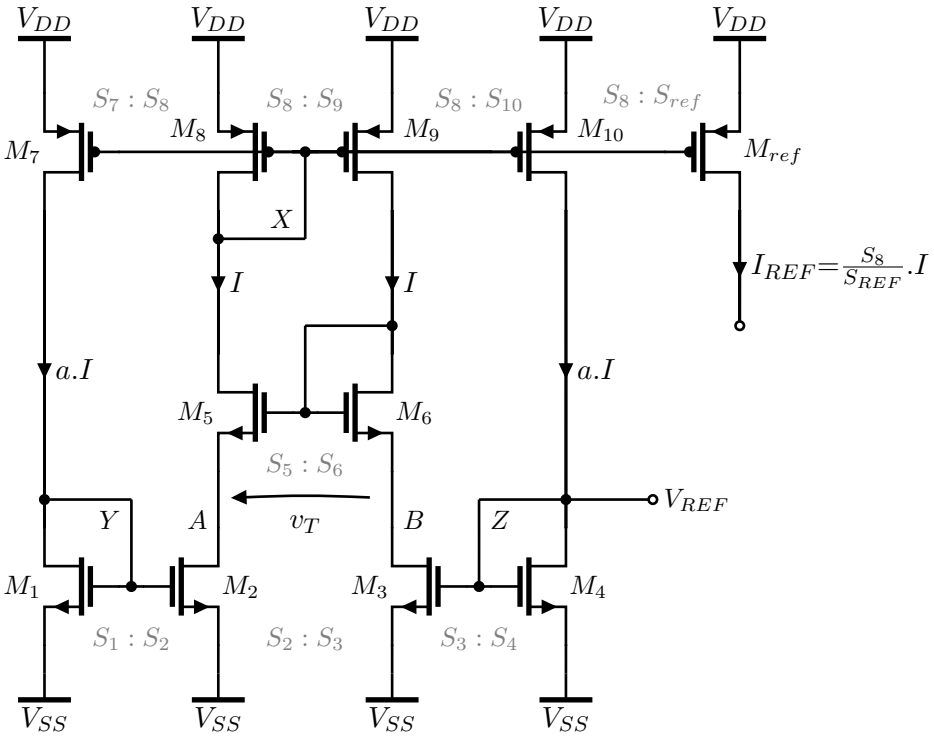


Figure 7.1: Principle of the proposed reference circuit

Saturation:

$$I_D = \frac{\mu C_{ox}}{2}\frac{W}{L}\left(V_{GS} - V_{TH}\right)^2 = \frac{K}{2}\left(V_{GS} - V_{TH}\right)^2$$

Linear region:

$$I_D = \mu C_{ox}\frac{W}{L}\left[\left(V_{GS} - V_{TH}\right)V_{DS} - \frac{V_{DS}^2}{2}\right] = K\left[\left(V_{GS} - V_{TH}\right)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

Weak inversion:

$$I_D = \mu V_t^2 \frac{W}{L} e^{\frac{\frac{1}{n}V_{GS} - V_{TH}}{V_t}}\left(1 - e^{\frac{-V_{DS}}{V_t}}\right)$$

Where μ is the carrier mobility, V_t is the thermal voltage, V_{TH} is the threshold voltage and n the subthreshold slope factor. K is the device transconductance and given by $\mu C_{ox}\frac{W}{L}$.

7.2.1 Reference current

If MOS devices are biased within weak inversion they have similar properties than bipolar transistors. Hence, a PTAT voltage v_T can be obtained by operating them on different current densities. If both bulks are connected to V_{SS}, the difference voltage between their sources in reference to figure 7.1 can be written as:

$$v_T = V_{DS3} - V_{DS2} = nV_t \ln\left(\frac{K_6}{K_5}\right).$$

By using the equation for the linear region, the drain-to-source voltages can be written as follows.

$$V_{DS3_{1/2}} = \sqrt{\frac{2I}{K_4}}\sqrt{\frac{K_{10}}{K_8}}\left(1 \pm \sqrt{1 - \frac{K_4}{K_3}\frac{K_8}{K_{10}}}\right)$$

$$V_{DS2_{1/2}} = \sqrt{\frac{2I}{K_1}}\sqrt{\frac{K_7}{K_8}}\left(1 \pm \sqrt{1 - \frac{K_1}{K_2}\frac{K_8}{K_7}}\right)$$

As a consequence of the quadratic equation the linear region is modeled by, the solution with the negative sign is chosen. By substitution and introducing $\frac{K_{10}}{K_8} = \frac{K_7}{K_8} = a$, $\frac{K_4}{K_3} = \frac{K_1}{K_2} = b$, $\frac{K_1}{K_4} = c$ and $\frac{K_6}{K_5} = d$ the current expression I can be obtained.

$$I = \frac{K_1}{2}\frac{n^2V_t^2\ln(d)^2}{(\sqrt{c}-1)^2\left[\sqrt{a}\left(1-\sqrt{1-\frac{b}{a}}\right)\right]^2}$$

If devices M_5 and M_6 are not designed to sit in a dedicated well, or the process is not capable of, the body effect gives some additional temperature behaviour. This happens because the bulk terminals are connected to V_{SS}. The body effect is modeled by:

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{V_{SB} + 2\phi_F} - \sqrt{2\phi_F}\right).$$

With the surface potential ϕ_F assumed to be proportional to V_t[1] and the body effect parameter γ. By considering a difference in threshold voltage due to different bulk-to-source voltages, it can be written:

$$v_T = nV_t\ln(d) - \Delta V_{TH56}.$$

Therefore, as $V_{TH0_5} = V_{TH0_6}$ the expression for the threshold voltage difference ΔV_{TH} is given by:

$$\Delta V_{TH56} = \sqrt{2\phi_F}\gamma\left(\sqrt{1+\frac{V_{DS3}}{2\phi_F}} - \sqrt{1+\frac{V_{DS2}}{2\phi_F}}\right).$$

[1] only first order effects considered

The ratio of $\frac{V_{DS3}}{V_{DS2}}$ is equal to $\sqrt{c}$, seen in the equations of the drain-source-voltages. The temperature dependency of this term can be written as proportional to $T^{0.5}$, as the ratios $\frac{V_{DS3}}{2\phi_F}$ and $\frac{V_{DS2}}{2\phi_F}$ stay constant over temperature[2].

$$\Delta V_{TH56} = \Delta V_{TH0_{56}} \left(\frac{T}{T_0}\right)^{0.5}$$

Hence, the overall temperature behaviour of the reference current can be expressed as follows.

$$I = \frac{K_{0_1}}{A} \left(\frac{T}{T_0}\right)^{-m} \left[V_{PTAT0} \left(\frac{T}{T_0}\right) - \Delta V_{TH0_{56}} \left(\frac{T}{T_0}\right)^{0.5}\right]^2$$

Where, $A = 2\left(\sqrt{c}-1\right)^2 \left[\sqrt{a}\left(1-\sqrt{1-\frac{b}{a}}\right)\right]^2$, $V_{PTAT0} = n\frac{k_B T_0}{q}\ln(d)$ and $\Delta V_{TH0_{56}}$ is the threshold difference voltage for $T = T_0$. K_{0_1} is the process transconductance for $T = T_0$. However, if by design the effect of the threshold voltage term is minimized, the resulting current can be considered to be proportinal to T^{2-m}. From [Sze81], and also mentioned in [FA01], it has to be said that the mobility exponent m of a nMOS device within modern technologies most likely gets close to 2[3] and results in a good first order temperature compensation.

7.2.2 Reference voltage

By substituting the current equation into the equation for saturation, the reference voltage V_{REF} that is equal to V_{GS4} can be expressed as follows.

$$V_{REF} = \sqrt{\frac{c \cdot a}{\left|\sqrt{c}-1\right|\sqrt{a}\left(1-\sqrt{1-\frac{b}{a}}\right)}} n \ln(d)\, V_t + V_{TH4}$$

The temperature dependency of the threshold voltage $V_{TH}(T)$ is given by:

$$V_{TH}(T) = V_{TH}(T_0) + \alpha_{V_{TH}}\left(T - T_0\right).$$

Hence, the reference voltage is composed out of a PTAT voltage that follows the thermal voltage V_t and a CTAT voltage, as the threshold coefficient $\alpha_{V_{TH}}$ has a negative sign. This gives by choosing proper geometric factors the possibility to form a first-order compensated curvature voltage, similar to bandgap circuits.

[2] both V_{DS} and ϕ_F are proportional to T

[3] for $0.35\mu m$ CMOS: between 1.9 and 2.1, [FA01]

7.3 Circuit design based on ACM

By the use of the ACM model's easy approach of inversion coefficients, some design considerations concerning device sizing can be made. First of all it has to be said that devices M_1 to M_4 are designed to not get into weak inversion. The reason for that is that there is enough voltage headroom and the bad current matching properties within the weak inversion regime, [KAGM06]. To keep the overall power consumption low, the current I is designed to be in the nA-range. This implies that the devices aspect ratios are very low, to get the current density within the channel up. As already mentioned M_1 and M_4 are saturated, while M_2 and M_3 are sized to be in their linear region. Therefore, $i_{f1} \gg i_{r1}$ and $i_{f4} \gg i_{r4}$. This gives for the forward inversion coefficient i_{f1}:

$$i_{f1} = \frac{aI}{S_1 I_{1S\square}}.$$

With the geometric factor a, the device aspect ratio S_1 and the sheet specific current $I_{S\square 1}$. Clearly it can be seen that a determines the inversion coefficient of M_1 for a given current target I. Please note, that the aspect ratio cancels within the current's design equation. In the next steps the remaining inversion coefficients are refered to i_{f1}. As M_1 and M_2 share the same gate voltage $V_G = V_{G1} = V_{G2}$, $V_{S1} = V_{S2} = 0$, and the threshold voltage V_{T0} is close for long channel devices, equation (5) gives:

$$\sqrt{1+i_{f1}} - 2 + \ln\left(\sqrt{1+i_{f1}} - 1\right) = \sqrt{1+i_{f2}} - 2 + \ln\left(\sqrt{1+i_{f2}} - 1\right).$$

$$i_{f2} = i_{f1}$$

The reverse coefficient i_{r2} for M_2, operating below saturation, follows:

$$I = S_2 I_{2S\square}\left(i_{f2} - i_{r2}\right).$$

By substitution of the equation of i_{f1} and implying that $I_{2S\square}$ is close to $I_{1S\square}$ it can be written:

$$i_{r2} = i_{f1}\left(1 - \frac{b}{a}\right).$$

The same approach for device M_4 and M_3 gives the following equations:

$$i_{f4} = i_{f1} c$$

$$i_{f3} = i_{f1} c$$

$$i_{r3} = i_{f1} c \left(1 - \frac{b}{a}\right).$$

Hence, the ratio $\frac{b}{a}$ has to be designed to be lower than one, to get M_2 and M_3 out of saturation. Another important design consideration is to not choose too low values for c, as M_3 and M_4 would enter the weak inversion regime.

7.3.1 Device sizing

For this design the minimal reference current target should be greater than $10nA$ to minimize the dependency on leakage. Hence, the target was set to $I = 20nA$ to get a good trade-off between current consumption and a robust design that is not dependent on second order effects.

In the next step, in accordance to the design considerations out of the ACM model, the ratio $\frac{b}{a}$ is set to 0.5, c is set 0.25 and a to 3. Care has to be taken by setting the value of d. For a given set of values, d has to be scaled to get the reference voltage V_{REF} first order temperature compensated. This means that:

$$\ln(d) \sqrt{\frac{c \cdot a}{|\sqrt{c} - 1| \sqrt{a} \left(1 - \sqrt{1 - \frac{b}{a}}\right)}} \frac{k_B}{q} = -\alpha_{V_{TH}}$$

With k_B as Boltzmann's constant, q as the charge of an electron and the geometric factors. For this design a value of $d = 6$ was found to be appropriate. Now, S_1 can be sized to get the target current I, by applying the design equation of the current. Once S_1 is fixed, S_2 to S_4 follow. Afterwards S_8 is given by designing M_8 to be in strong inversion, $i_{f_8} > 100$. Together with a, S_7 to S_{10} are given. M_5 and M_6 are designed to enter the weak inversion regime. Hence, in combination with d and the current target I, S_6 and S_5 are sized for an inversion coefficient less than 1. All device dimensions for the reference generator and their corresponding inversion coefficient are listed in table 7.1.

Clearly it can be seen that devices that operate in strong and moderate inversion have low $\frac{W}{L}$-ratios. These devices were composed out of a series stack of transistors. For the device length this is indicated by the dot, while for the width the dot means a parallel composition of transistors.

If one of the devices is found to work in a wrong inversion regime, the geometric factors can be reset and the transistor ratios adapted.

To show how easy hand calculations by the use of the ACM and the inversion coefficient approach are, two voltages are calculated. By applying the voltage equation (5), the gate voltage V_G of M_1 and M_2 can be calculated to be around $889mV$ while for M_3 and M_4 the voltage is around $639mV$. Figure 7.2 illustrates the DC-simulation results with embedded BSIM models.

Device	$\frac{W}{L}$	i_f	Inversion regime
M_1	$1u/42 \cdot 10u$	185	strong
M_2	$1u/63 \cdot 10u$	185	strong
M_3	$4u/63 \cdot 10u$	23	moderate
M_4	$4u/42 \cdot 10u$	46	moderate
M_5	$10u/5.5u$	0.081	weak
M_6	$6 \cdot 10u/5.5u$	0.0135	weak
M_7,M_{10}	$3 \cdot 1u/20 \cdot 10u$	108	strong
M_8,M_9	$1u/20 \cdot 10u$	108	strong

Table 7.1: Device sizes and inversion coefficients

To sum up, by choosing proper geometric factors a, b, c, d, the reference generator can be designed for a target current I and a corresponding V_{REF}, with devices working in the right inversion regime and proper first order temperature compensation. After having fixed those values, it is easy to size the transistors and estimate the total area. All the formulas of table 6.1 can be applied once the inversion coefficients have been calculated.

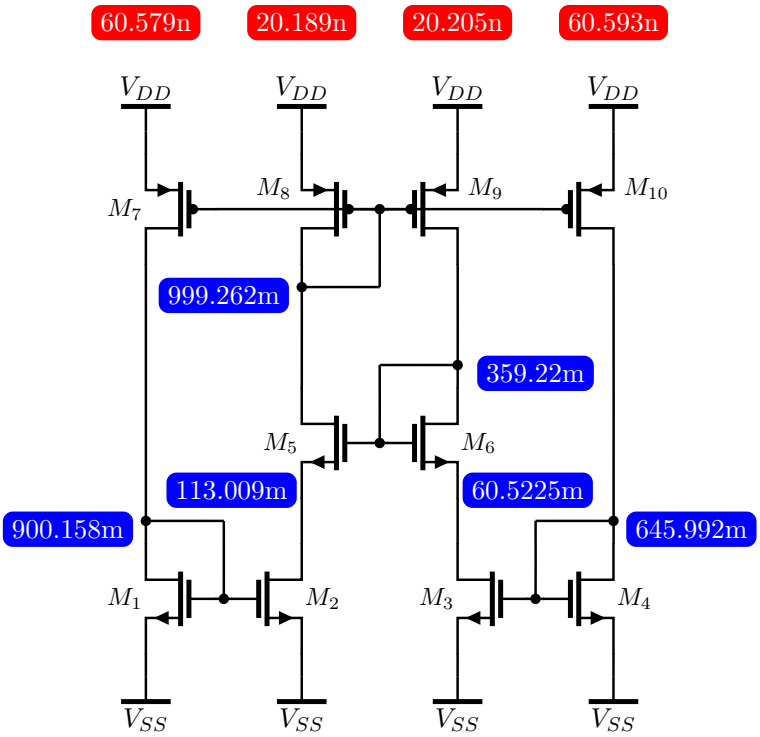


Figure 7.2: BSIM: DC operating point of reference generator

In table 7.2 a comparison between the simulated values and the calculated ones, out of the design equations can be seen. For the calculation the process transconductance was found with $K_n = 341.4\frac{\mu A}{V^2}$, the subthreshold slope factor $n = 1.28$, the threshold voltage for nominal temperature $V_{TH}(T_0) = 458mV$

and it's temperature coefficient $\alpha_{V_{TH}} = -0.37\frac{mV}{°K}$.

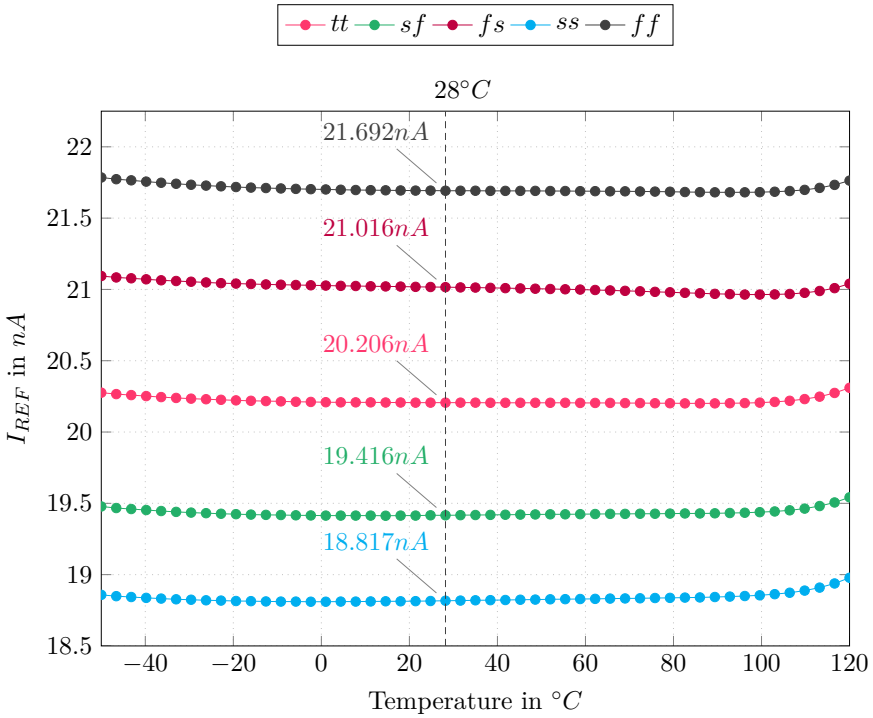
Design variable	Design equation	Simulation
Current I	$19.38nA$	$20.2nA$
Voltage V_{REF}	$640.7mV$	$646mV$
PTAT voltage v_T	-59.3mV	-52.5mV

Table 7.2: Accuracy of design equations

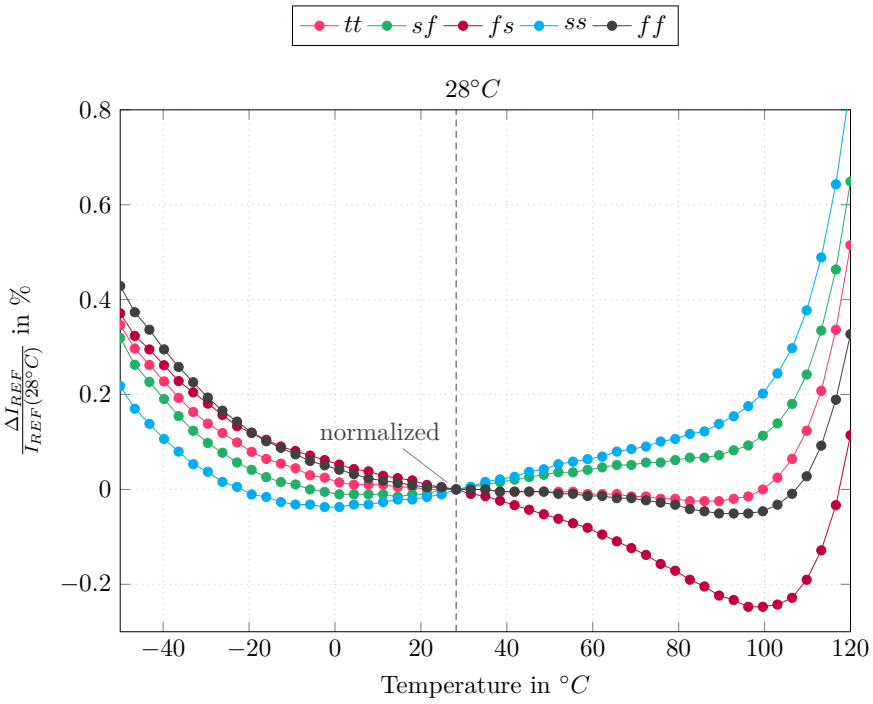
7.3.2 Achievements

Figure 7.3 shows the simulated temperature behaviour of the reference current for different corner cases. It is seen that this design enables a unique approach to achieve temperature-compensated reference currents, while keeping the process spread low. Monte-Carlo sampling over process and mismatch confirmed a very robust design with standard deviations of less than 2.5% and 1.5%, seen in figure 7.4. As intended, the implemented design gives a reference current close to $20nA$ that is first-order temperature-compensated with low spread across process and mismatch variation.

And in figure 7.5 the simulated temperature behaviour of the reference voltage for different corner cases is shown. The sub-1V reference voltage is also first-order compensated. Monte-Carlo sampling over process and mismatch showed that the variation for voltage is even lower than for the current, with standard deviations of 1.3% and 0.3%. This can be seen in figure 7.6. Of course a bandgap reference circuit could achieve better compensation, but this novel circuit is able to generate a compensated reference voltage and current with low power consumption, while keeping overall process and mismatch spread low. Therefore, this circuit is a perfect match for the proposed dual-phase low-power oscillator.

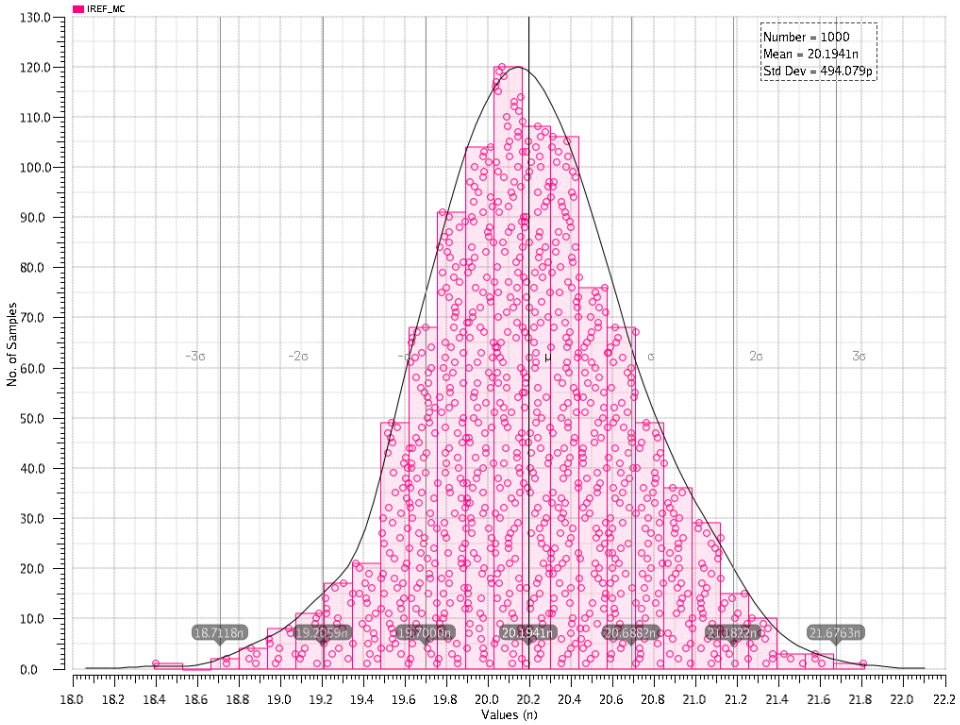


(a) Variation of absolute reference current

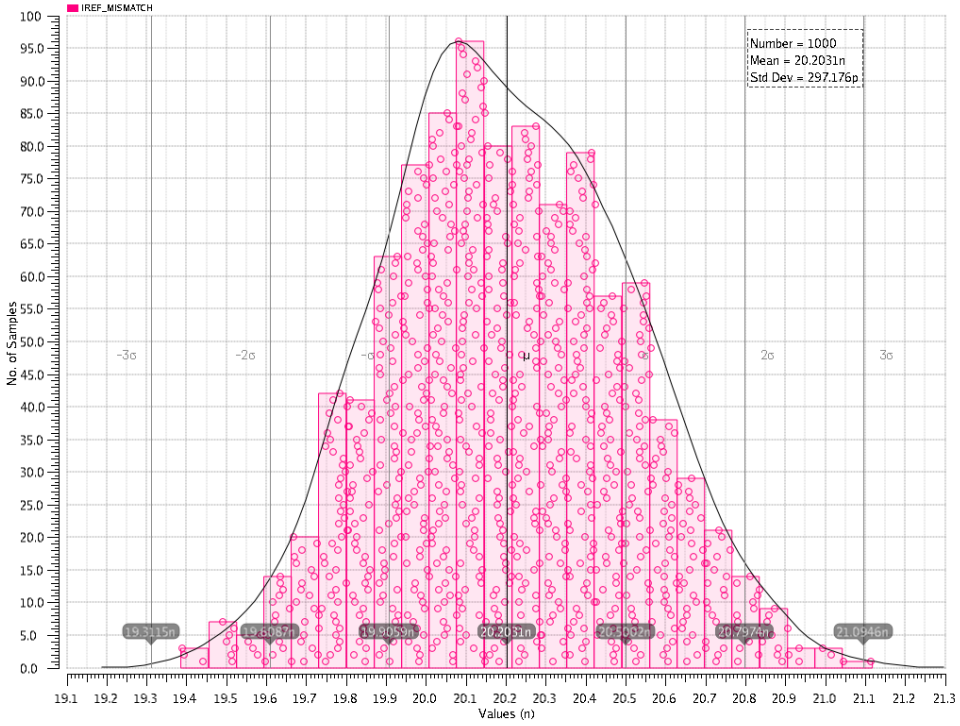


(b) Normalized variation over temperature

Figure 7.3: Temperature characteristics of reference current

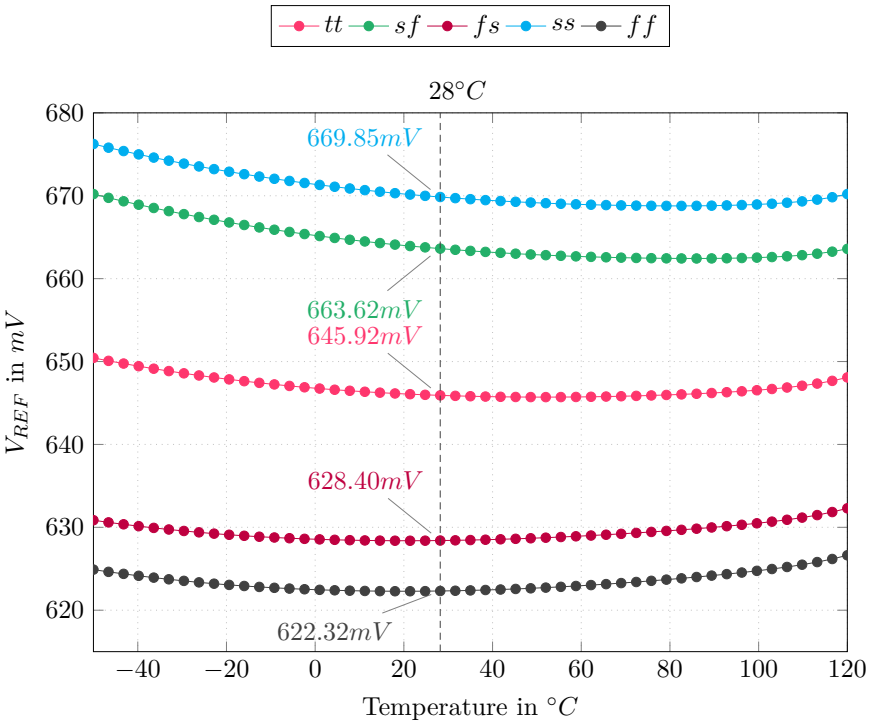


(a) Process variation - Histogram 1000 samples

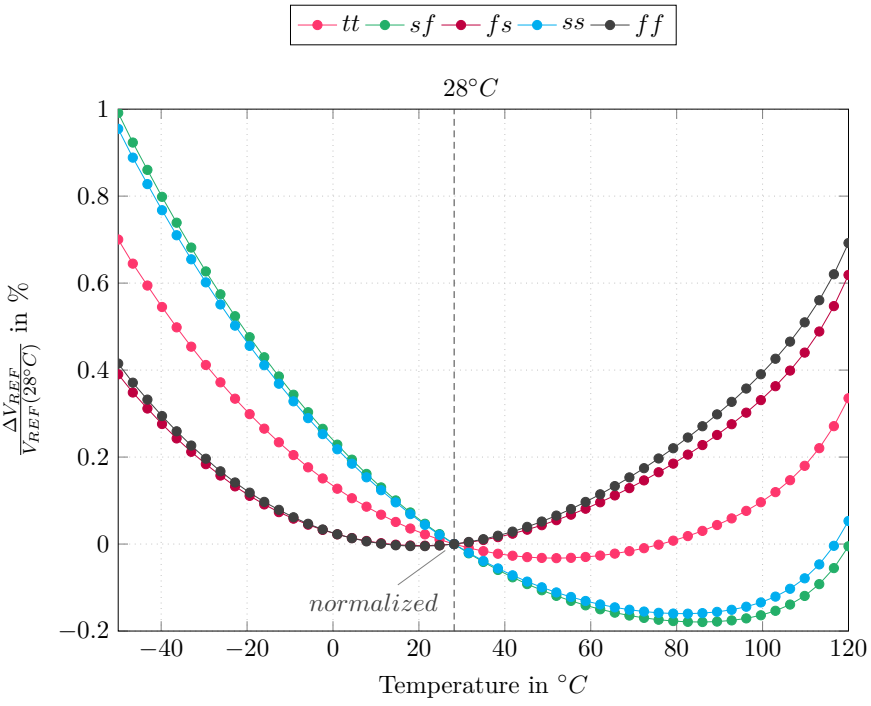


(b) Mismatch analysis - Histogram 1000 samples

Figure 7.4: Process and mismatch analysis - reference current

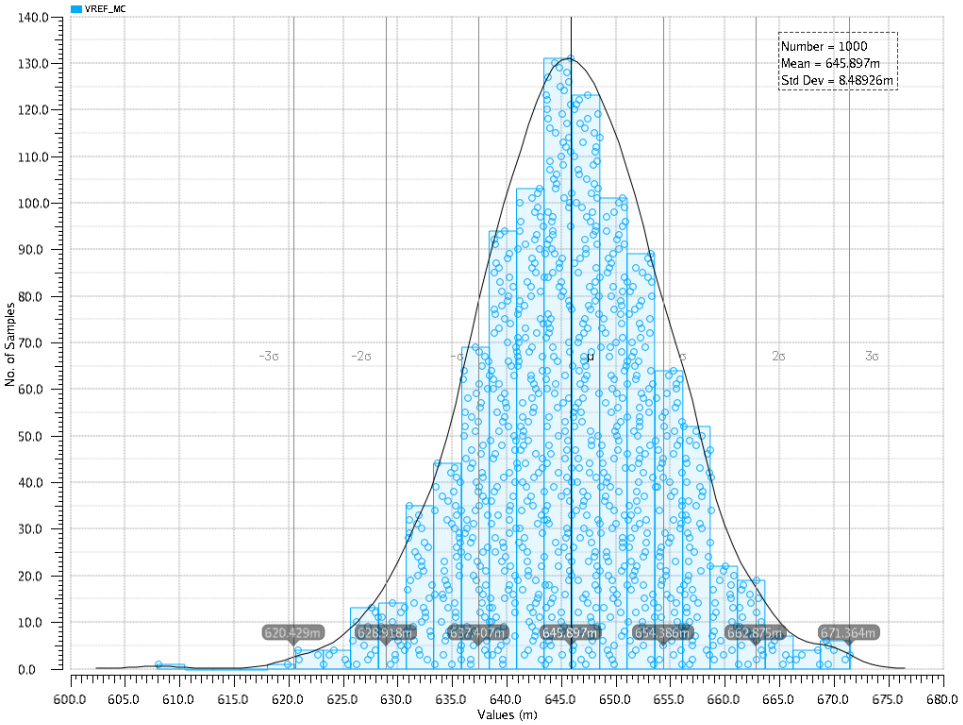


(a) Variation of absolute reference voltage

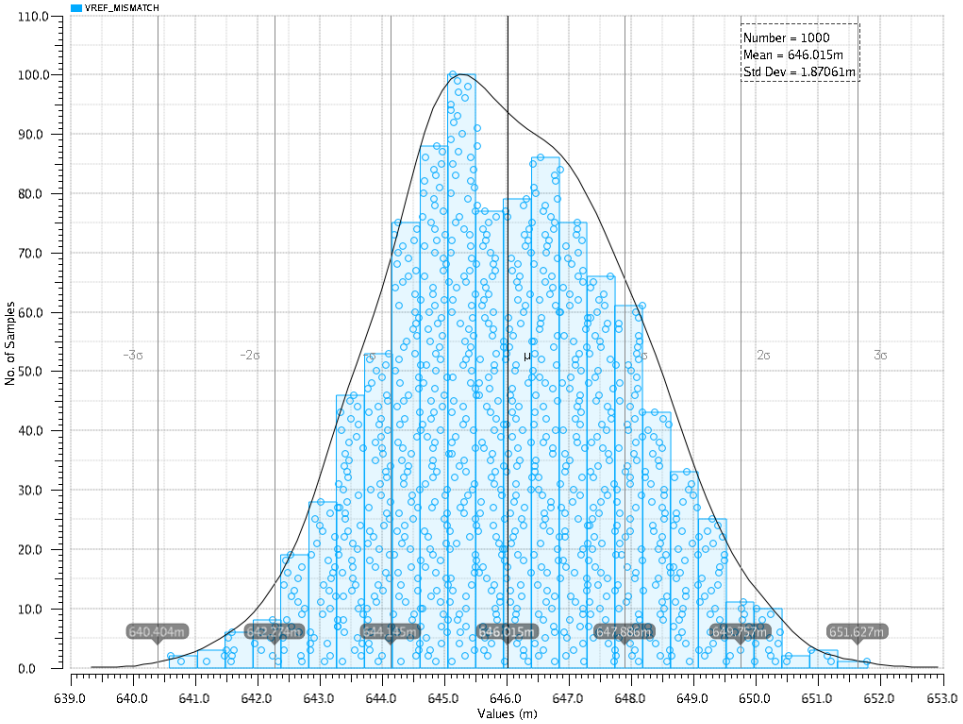


(b) Normalized variation over temperature

Figure 7.5: Temperature characteristics of reference voltage



(a) Process variation - Histogram 1000 samples



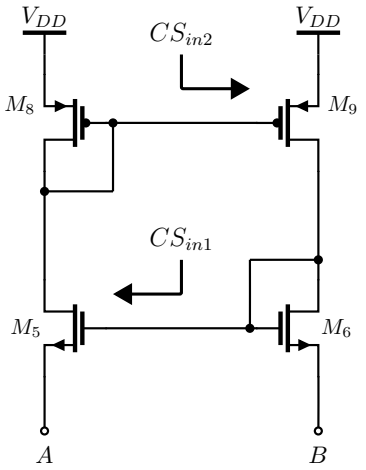
(b) Mismatch analysis - Histogram 1000 samples

Figure 7.6: Process and mismatch analysis - reference voltage

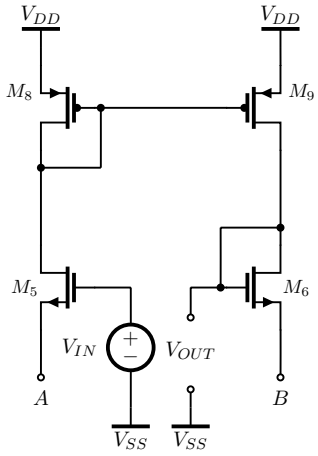
7.4 Operation point

As the proposed low power oscillator acts as a time-reference for the power-on-reset block, it is essential to make sure that it comes up and is not stuck in an unwanted operation point. If the self-biased reference generator is trapped in it's zero-current condition, it not only makes the low power oscillator inoperative, but also the complete SoC. The conventional way to verify circuit start-up is to run repeated transient simulations. However, even if a start-up circuit gets rid of the zero-current condition, the simulator will only provide one solution to a circuit and therefore it's not guaranteed that this is the only stable equilibrium point. Other stable points can be captured by the circuit under special conditions. This makes it very important to do further analysis [WZG+12] to observe hidden operation points and if needed remove them by additional circuitry.

The self biased structure M_5, M_6, M_8 and M_9 of the reference generator is a positive feedback system with two common-source stages connected together. This can be seen in figure 7.7a. To investigate possible operation points, this loop is broken and an ideal voltage source V_{IN} added to one of the inputs, while keeping track of the output voltage V_{OUT}, depicted in figure 7.7b.



(a) Self-biased MOS structure

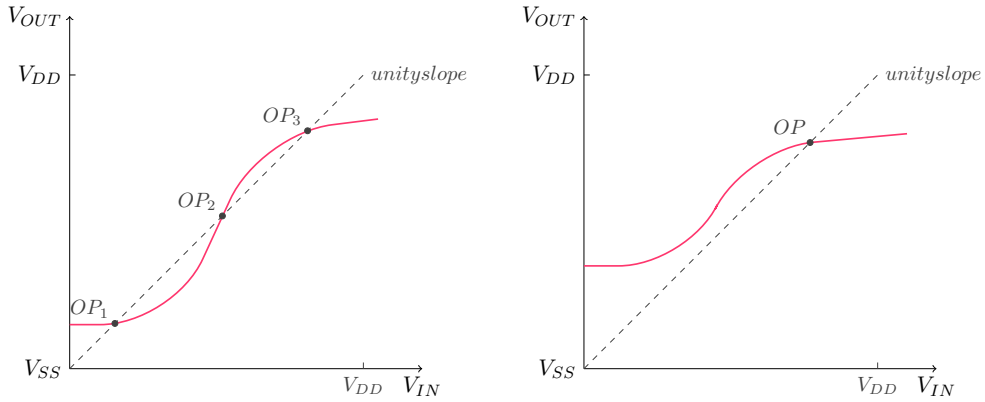


(b) Broken loop for OP analysis

Figure 7.7: Reference generator operation point analysis

This procedure gives the transfer characteristics and it is observed that for this circuitry two possible cases exist. Whenever the transfer curve crosses the unity-slope, one stable point of equilibrium can be concluded. The two cases can be seen in figure 7.8. If this analysis results in only one single crossing point, no start-up is needed, this case is shown in figure 7.8b. However, as this curve moves with process a detailed analysis over corners has to be done to make sure that the system stays inherently stable.

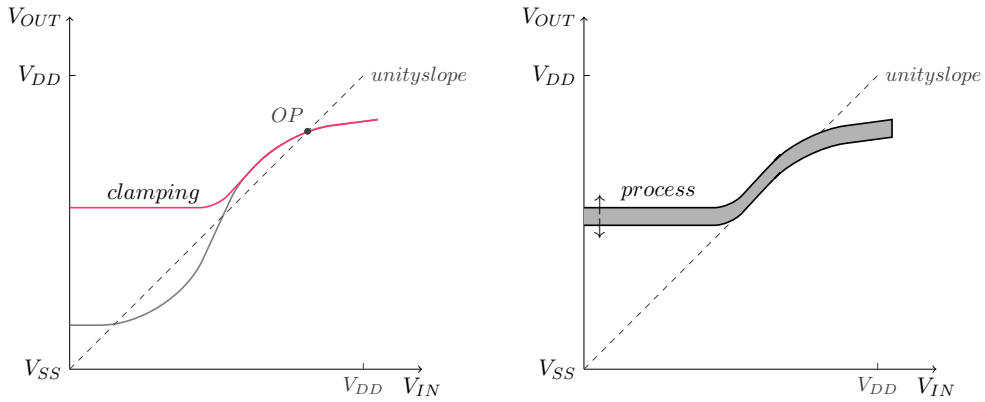
On the other hand, if the transfer curve crosses the unity-slope three times



(a) three possible operation points **(b)** one possible operation point

Figure 7.8: Broken loop transfer characteristics

it is inevitable to add a proper start-up circuit. Figure 7.8a shows the initial characteristics and 7.9a how the start-up circuitry clamps the transfer to eliminate operation point OP_1 and OP_2. Again, care should be taken to verify the singularity of operation point over multiple corners. In figure 7.9b the grey area shows how process variation shifts the circuit's transfer curve and, as the reference generator is supposed to work over a wide temperature range, the possible deviation is even higher.



(a) Clamping of transfer curve **(b)** Variation over process

Figure 7.9: Transfer characteristics after adding start-up

In figure 7.10 the outcome of this advanced operation point analysis can be seen. Under all conditions the unity-slope is crossed in one point and therefore a singular operating point is concluded.

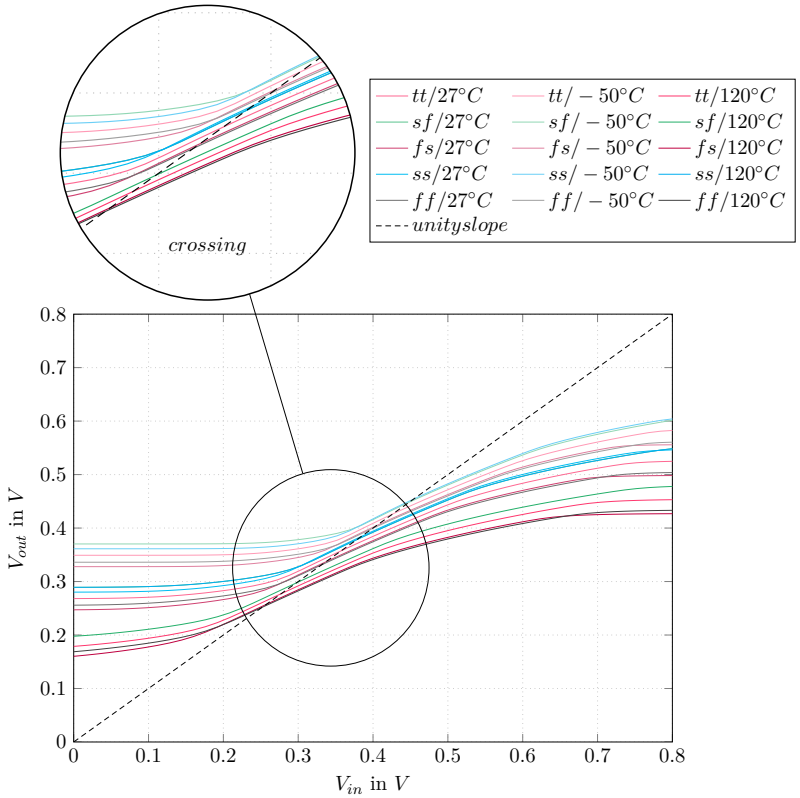


Figure 7.10: Reference - OP analysis

7.5 Start-up circuit and settling

It has to be said, that even if analysis leads to the conclusion that the system has only one operation point, it might be preferable to add start-up circuit to help the reference generator get up faster after initial power cycling. Also from a system perspective start-up time could be an issue and therefore it is common practise to add such circuitry. Figure 7.11 shows the start-up circuit of the proposed reference generator. Nodes X, Y and Z are connected to the reference generator as seen in figure 7.1. The idea is to form a circuit that is active during power-up but disables itself as the reference gets closer to the desired operation point. Rather than charge injection, used by many circuits to start-up faster, this concept is based on charge exchange. This means that node X shares it's charge to node Y and Z. Hence, the potential at node X gets down and node Y and Z are pushed up to decrease start-up time. After a certain threshold, the circuit disables itself and by the use of stacked long channel transistors the leakage and therefore the influence on the rest of the circuit is minimized. It has to be said that the reference generator is self-starting even without start-up circuit, if the leakage of M_6 is more than that of M_5 and therefore $S_6 > S_5$.

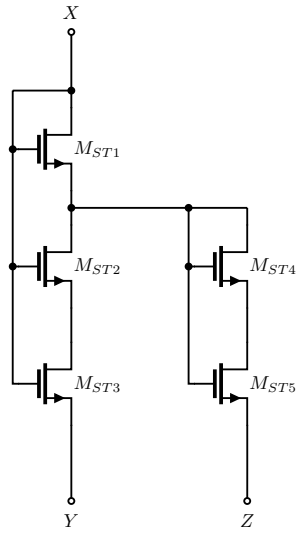


Figure 7.11: Start-up circuit of reference generator

7.5.1 Device sizing

All devices of the start-up are designed for low leakage currents between the upper node X and the lower nodes Y and Z whenever the operation point is reached. Therefore, both current branches are designed out of series stacked long transistors in diode configuration. As depicted in figure 7.2 the settled voltage levels of X and Y are close, while there is an about $350mV$ difference between X and Z. Therefore, the right hand-side branch is connected to the source of M_{ST1} to get two diode-connected devices in series and an overall higher threshold voltage. This means that there is a more high-ohmic connection between X and Z.

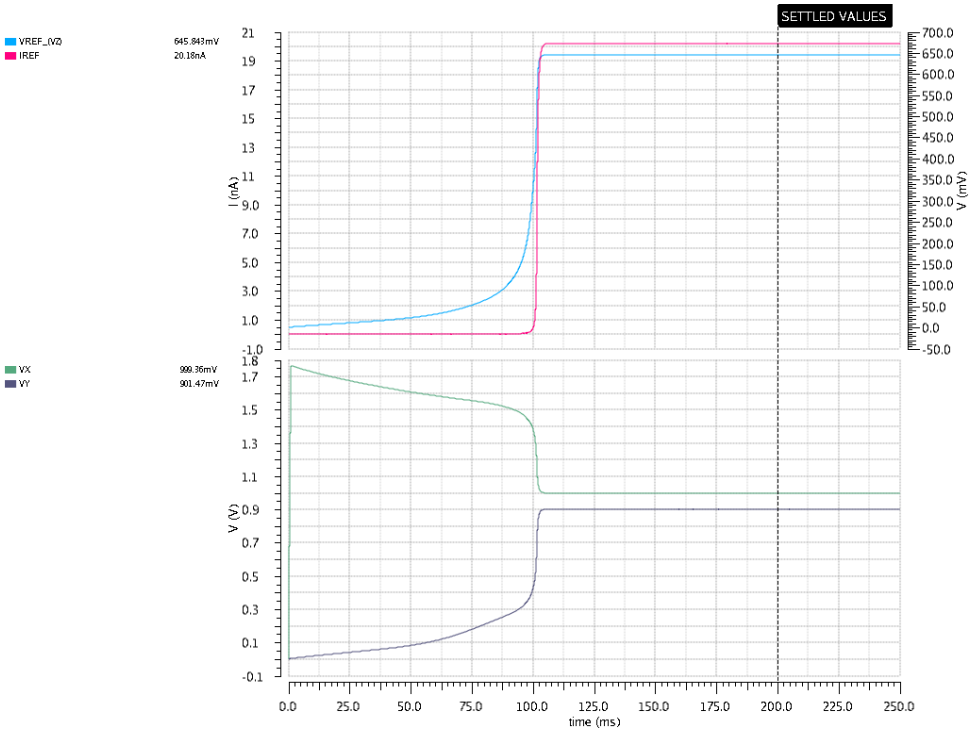
There is a trade-off between leakage current and reduction in settling time. The time constant of the charge distribution process is dependent on the resistance between the terminals. This resistance is indirect proportional to the $\frac{W}{L}$-ratio of the diodes, while the leakage current is direct proportional to it. Hence, for lower settling times one have to decrease the resistance, but on the other side increases leakage currents. A good compromise has been found with the sizes of transistors M_{ST1} to M_{ST5} that are shown in table 7.3. These dimensions showed little impact on the settled values, while giving a significant speed up in settling.

Device	$\frac{W}{L}$
M_{ST1}	$220n/15u$
M_{ST2}	$220n/15u$
M_{ST3}	$220n/15u$
M_{ST4}	$220n/10.5u$
M_{ST5}	$220n/10.5u$

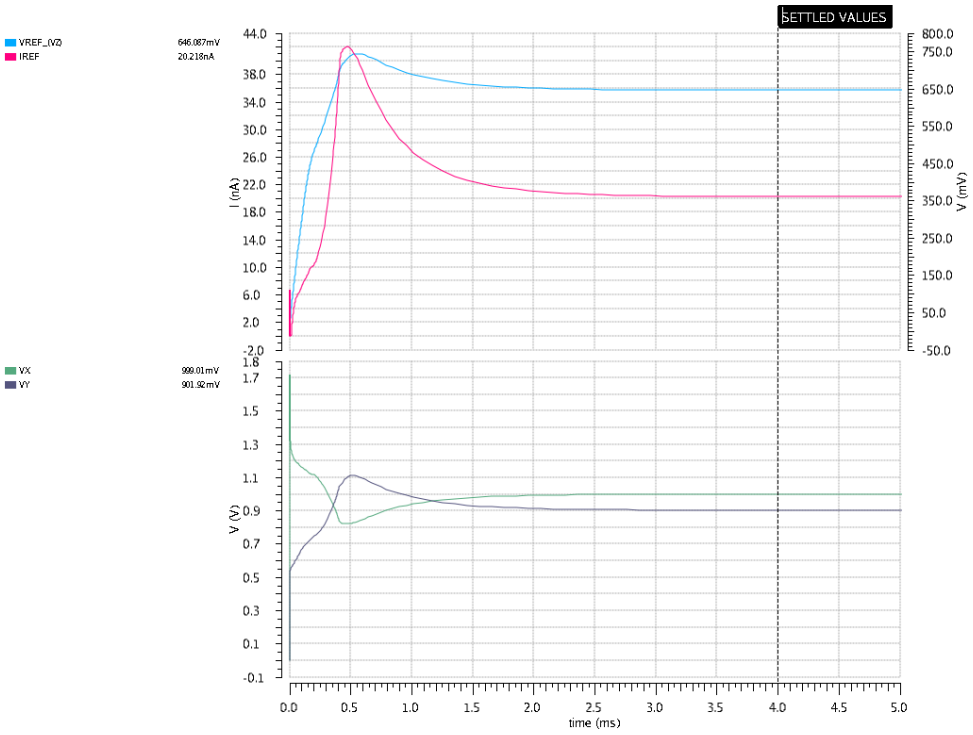
Table 7.3: Device sizes of start-up circuit

7.5.2 Achievements

As already mentioned the start-up circuitry enhances the start-up time and as seen in figure 7.12a without this feature the leakage based start-up would have a significant influence on the start-up time of the complete SoC. The settling time is decreased by a factor of more than 30 and it is proven that the start-up circuit has minimal influence on the settled values of the reference generator. In addition this circuit consumes no static power. Figure 7.12b shows how charge is exchanged between nodes X and Y. Please note that the reference current is pushed to a higher value first and settles back to the target. This benefits the start-up of the designed oscillator. Figure 7.13 shows the transient settling for different temperatures and process corners. In this plot again the low variation over process and temperature can be seen. The temperature range was set to be $170°C$. A plot of the settling time over temperature is given by figure 7.14. In this case the settling time is defined as the time the current takes to get 95% within it's final value.



(a) without start-up circuit



(b) with start-up circuit

Figure 7.12: Settling behaviour of reference generator - TT corner

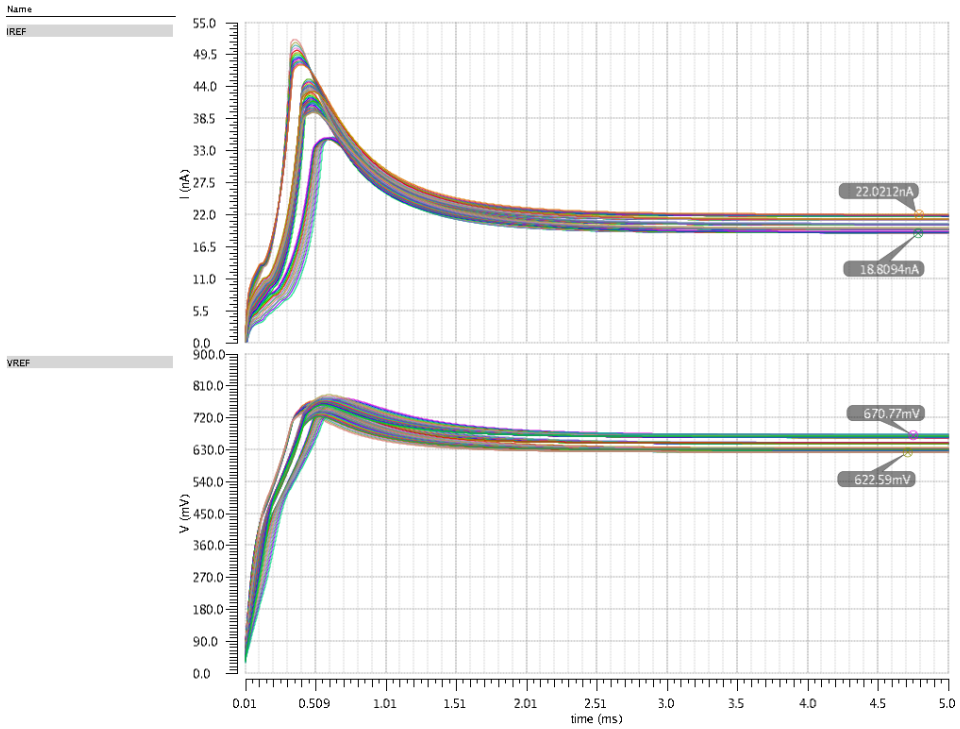


Figure 7.13: Transient waveform of settling over corners and temperature

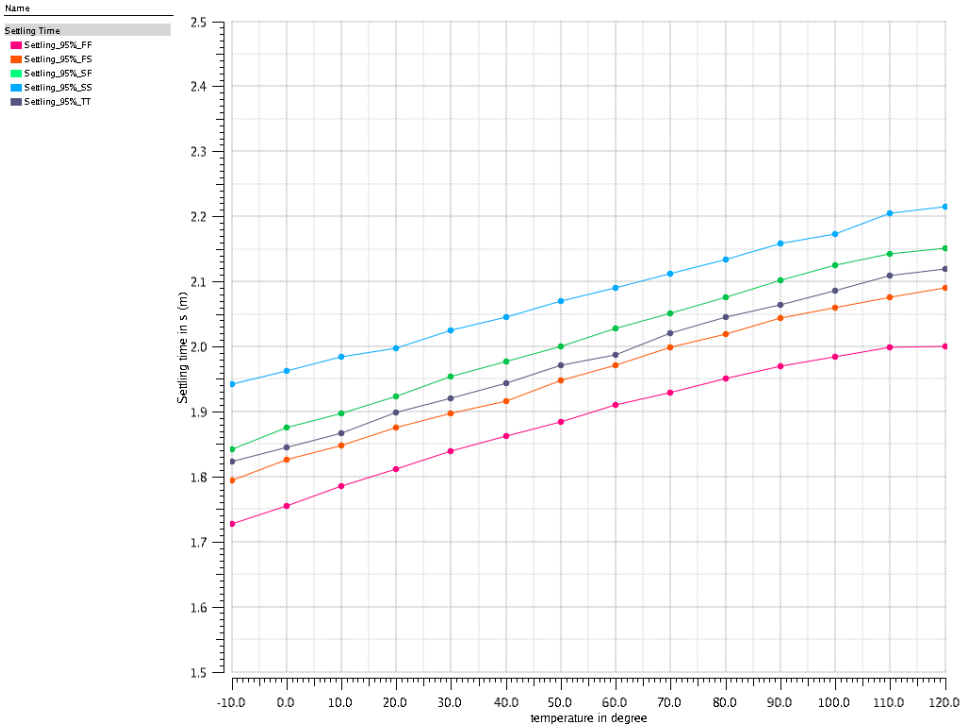


Figure 7.14: Settling time for different corners over temperature

Chapter 8

Comparator

This chapter deals with the proposed adaptive-biased low-power comparator that was implemented throughout this thesis. Within the dual-phase oscillator it converts analog signals into a digital clock with 50% duty cycle if circuitry is well-matched. In respect to system behaviour, the comparator's delay time t_d impacts the period of the output signal directly. Even if the reference generator is well-designed and provides a temperature compensated voltage V_{REF} and current I_{REF}, the delay time moves with temperature. As the oscillator is optimized for low-power the delay time can't be made negligible. Kick-back is suppressed by the dual-phase concept and therefore the size of the comparator's input devices is not limited. Therefore, the focus lies on designing the delay time to get good temperature behaviour while keeping the power consumption as low as possible.

8.1 Principle

As seen in figure 8.1, the two comparators of the oscillator share a latching and buffer stage to keep power consumption low. The pre-amplifiers A_1 and A_2 are separated and whenever the capacitor voltage V_{C1} or V_{C2} exceeds the reference voltage, the latch switches it's state and needless to say the output voltages V_{clk} and $\overline{V_{clk}}$ do so.

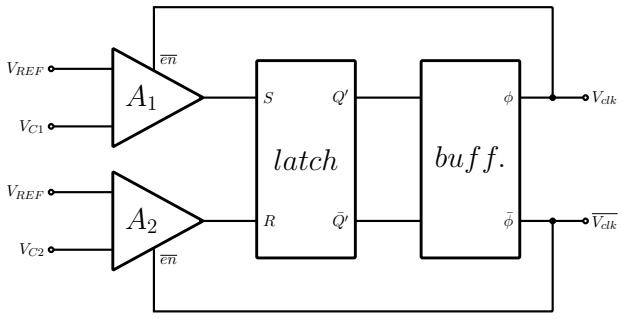


Figure 8.1: Principle of comparator

If the state gets flipped, parts of the pre-amplifier that did the corresponding decision get shut down, while the opposite amplifier is enabled. This approach

gives possibility not only to further decrease the power consumption but also to introduce positive feedback to the first stage of the comparator, as enough regeneration time is given. Hence, the pre-amps are only active for half of a clock period T_{clk}. The design considerations for each block of the comparator are discussed in the following subsections.

8.2 Pre-amplifier

The pre-amplifier circuits consist out of a differential pair loaded by diode-connected and cross-coupled nMOS devices, [BB97]. In differential-mode this offers a high output impedance, as the negative resistance of the cross-coupled devices cancels the positive one. Another advantage is that this fully-differential structure implies local common-mode feedback without the need of additional devices. The common-mode impedance is low and therefore the common mode level stabilizes itself at one V_{GS} above V_{SS}. Thus, this structure has a low common-mode and a high differential-mode gain as well as a good common-mode rejection and the lack of common-mode feedback makes it suitable for very low-power designs. Figure 8.2 shows the complete pre-amplifier that also includes a adaptive biasing scheme to speed up the circuit.

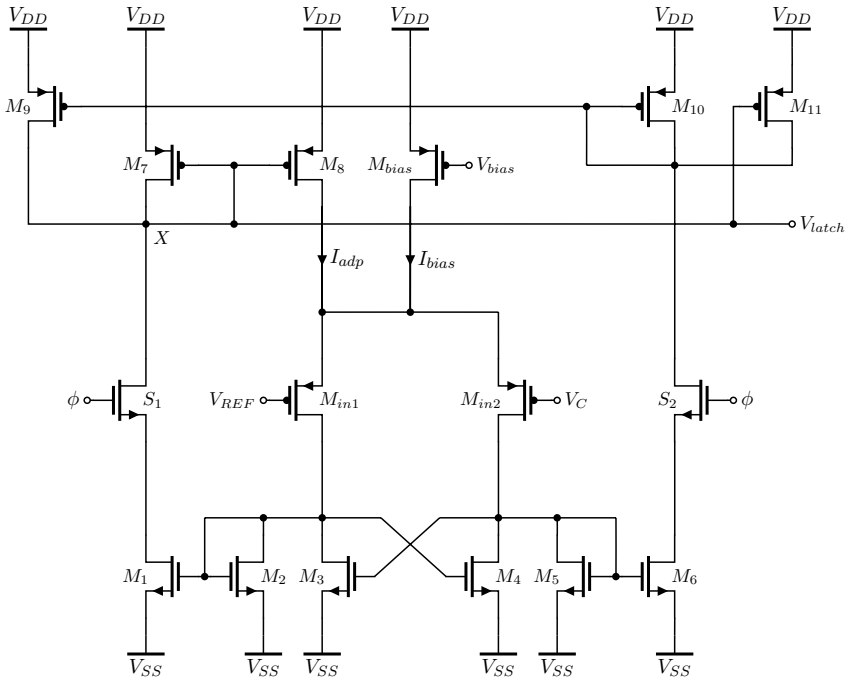


Figure 8.2: Input stage of comparator

8.2.1 Small signal analysis

In reference to figure 8.3, the differential voltage gain A_d of the circuit can be written as:

$$A_d = -g_{m_{in}} \left(\frac{1}{g_{m_2}} || - \frac{1}{g_{m_3}} || r_{ds_{in}} || r_{ds_2} || r_{ds_3} \right) \approx \frac{-g_{m_{in}} r_{ds_{in}}}{3}.$$

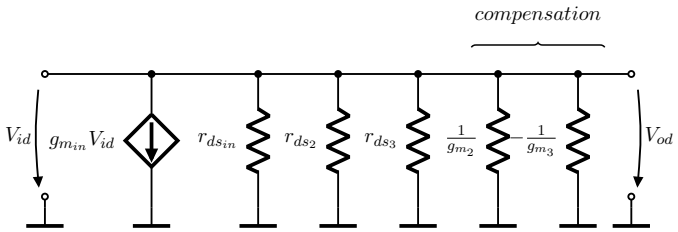


Figure 8.3: Differential-mode small signal analysis

Figure 8.4 shows the common-mode small signal analysis. Therefore, the common-mode voltage gain A_c is found as:

$$A_c = -\frac{g_{m_{in}}}{1 + 2 g_{m_{in}} r_{ds_{bias}}} \left(\frac{1}{g_{m_2}} || \frac{1}{g_{m_3}} \right) \approx \frac{1}{2 r_{ds_{bias}} \left(g_{m_3} + g_{m_2} \right)}.$$

Where, the transconductances are fixed to $g_{m_3} = g_{m_4}$, $g_{m_2} = g_{m_5}$ and $g_{m_{in}}$. The small signal drain-source-resistance $r_{ds_{in}}$ refers to the input devices of the differential pair.

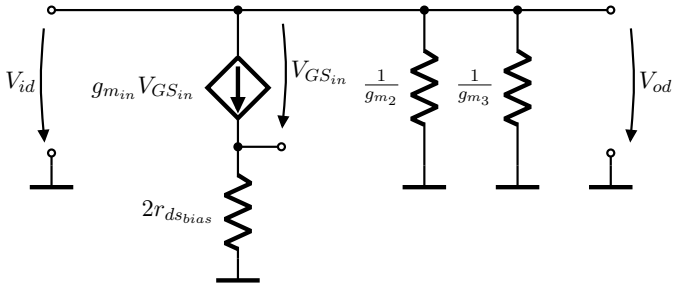


Figure 8.4: Common-mode small signal analysis

Transfer characteristics of the differential pair for different load configurations are shown in figure 8.5. The upper graph shows flat transfer and low gain, if only diode-connected transistors are used. The graph in the middle corresponds to a current-mirror load and the lower one to the loading seen in figure 8.2. The last graph shows that the implemented structure has enhanced symmetry and similar gain compared to a current mirror load.

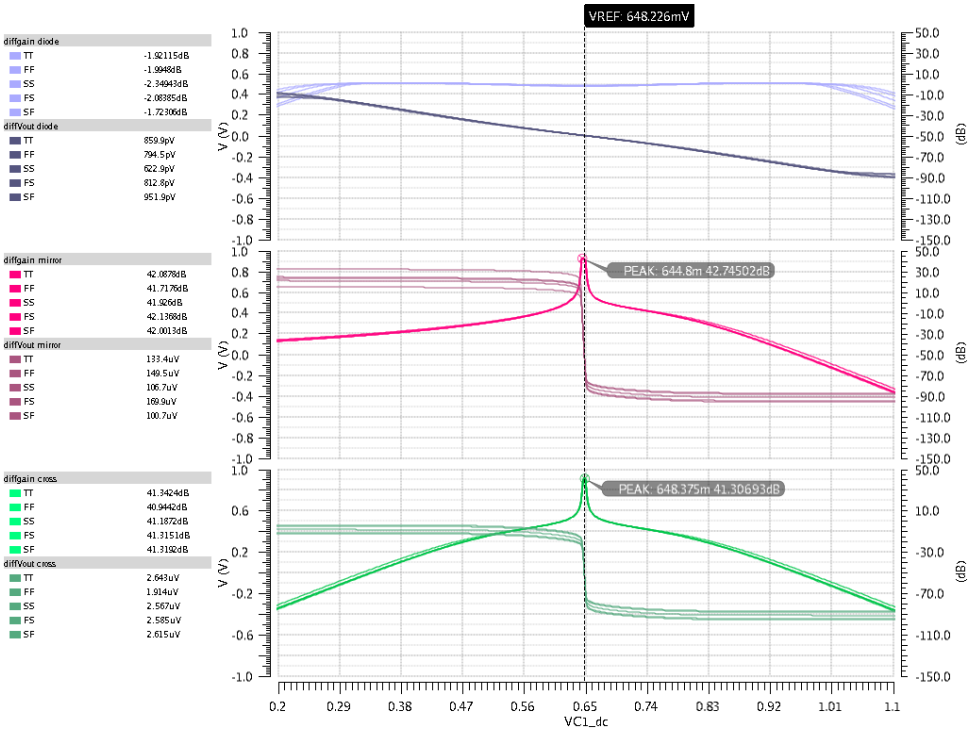


Figure 8.5: Transfer characteristics for different loads

8.2.2 Adaptive biasing

Whenever V_C increases and gets close to V_{REF}, an additional current I_{adp} is injected into the tail of the differential pair to speed up the transmission. This current is provided by an positive feedback loop that consists out of the devices M_2, M_1, M_7 and M_8. In difference to [IHT+11], within the dual phase system only the pre-amplifier's positive edge is adaptive biased because the latch is flipped back by action of the second pre-amplifier, depicted in figure 4.2b. After a decision has been made and the latch has flipped, the additional current paths of the corresponding pre-amplifier get shut-down by switches S_1 and S_2, while at the same time this paths within the second pre-amp gets activated.

Whenever the gate of M_{in1} is on a lower potential than the gate of M_{in2}, respectively V_C went higer than V_{REF}, the positive feedback loop gets active. If these two voltages are close in both branches an equal current of $\frac{I_{bias}}{2}$ is present. Hence, in M_{in1} depending on the input voltages a current equal to αI_{bias}, with α between 0.5 and 1, flows. This current is amplified by the positive feedback loop with the current gain of K and increases with time.

$$I_{adp} = \alpha I_{bias} \left(1 + K + K^2 + K^3 + \dots\right)$$

with

$$0.5 < \alpha < 1$$

and

$$K = \frac{S_1}{S_2}\frac{S_8}{S_7}$$

It can be seen that by designing K to be larger than one, I_{adp} can increase very fast and forces the latch to flip it's state. As it is important for low power circuits to have a defined current consumption the adaptive current I_{adp} was limited. Whenever the input voltages are close, both current paths get active and the adaptive current is limited by M_9 and M_{11}. Applying Kirchhoff's law to node X, seen in figure 8.2, the current I_7 flowing through M_7 can be written as follows.

$$I_7 = K\frac{I_{bias}}{2} - K'I_7 = \frac{K}{1+K'}\frac{I_{bias}}{2}$$

with

$$K' = \frac{S_9}{S_7} = \frac{S_{11}}{S_{10}}$$

Thus, the adaptive current can be expressed as:

$$I_{adp} = \frac{I_{bias}}{2}\left[1 + \frac{K}{1+K'} + \left(\frac{K}{1+K'}\right)^2 + \left(\frac{K}{1+K'}\right)^3 + \dots\right].$$

This approach can be seen as a combination of positive and negative feedback to make the current convergent and to prevent high current consumption. By designing $\frac{K}{1+K'}$ to be smaller than one, the expression can be simplified to:

$$I_{adp} = \frac{I_{bias}}{2}\frac{1+K'}{1+K'-K}.$$

with

$$\frac{K}{1+K'} < 1$$

Hence, the current consumption is even defined when the input voltages are close or when the switching delay would lead to an increased current consumption. The single-ended output node V_{latch} of each pre amplifier is connected to the latching stage, described in the following subsection.

Figure 8.6 shows the action of this adaptive biasing scheme during operation. The upper waveforms show the input voltages, V_{REF} and V_{C1}, of one pre-amplifier, while the most bottom one shows one of the corresponding output signals after the buffer circuit. In-between the introduced adaptive current as well as the current consumption of the complete pre-amplifier are plotted. It can be seen how the state transition is speed up while the current consumption is kept low.

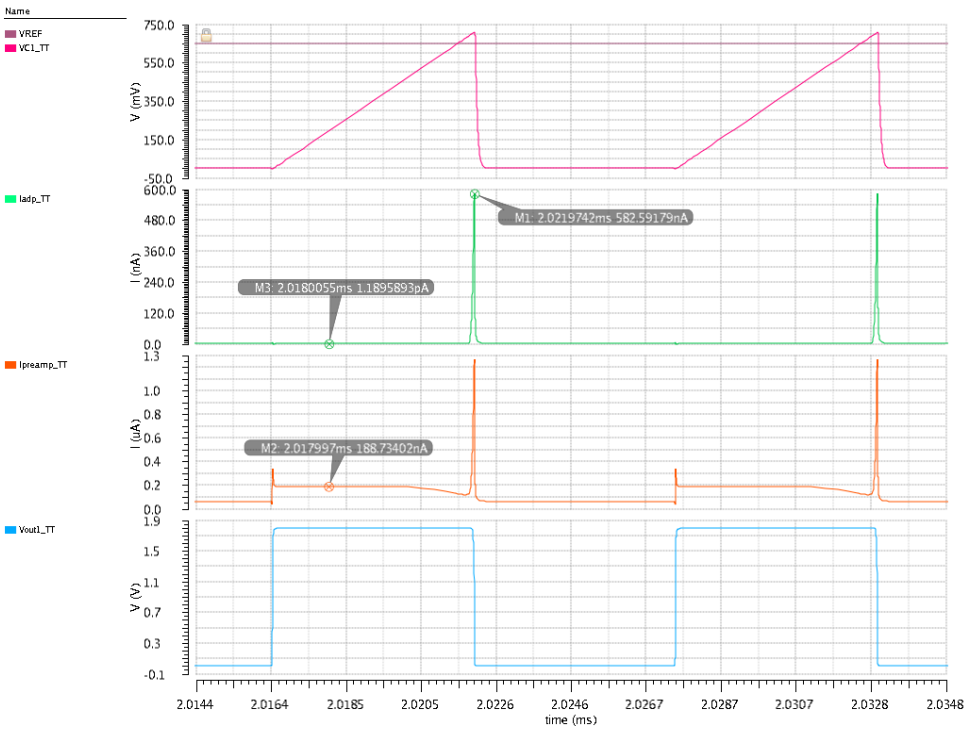


Figure 8.6: Adoptive current seen during operation

8.3 Latch and buffer

The two pre-amplifier circuits are connected to the latching stage, followed by the output buffer. Both the latch itself as well as the buffer stage include cross-coupled devices and ensure that the full output logic levels are reached. Figure 8.7 shows the circuitry of these stages. The latching stage was implemented as low energy level converter, in reference to [ST07] and [ST09]. The buffer stage makes sure that there is no slew rate limitation at the oscillators output nodes ϕ and $\overline{\phi}$.

Within the latching stage two transistors M_5 and M_6 ensure that the positive feedback is triggered even with low input voltages V_{pre1} and V_{pre2}. They weaken the pull-down capability of M_3 and M_4 to make sure that even a small current out of M_1 or M_2 can pull-up node X or Y above the threshold voltage, to activate the feedback. Whenever this happens, also the input devices of the buffer stage get active and after a certain delay the positive feedback of the last stage kicks in.

It should be needed, that the current provided by M_1 or M_2 during the state transition is derived from the adaptive biasing current I_{adp} of the pre-amplifier. Thus, the crowbar currents within the latching and buffer stage are well defined.

Figure 8.8 shows waveforms within the latch and buffer stage during operation. On the top the current consumption of this stages is plotted. The

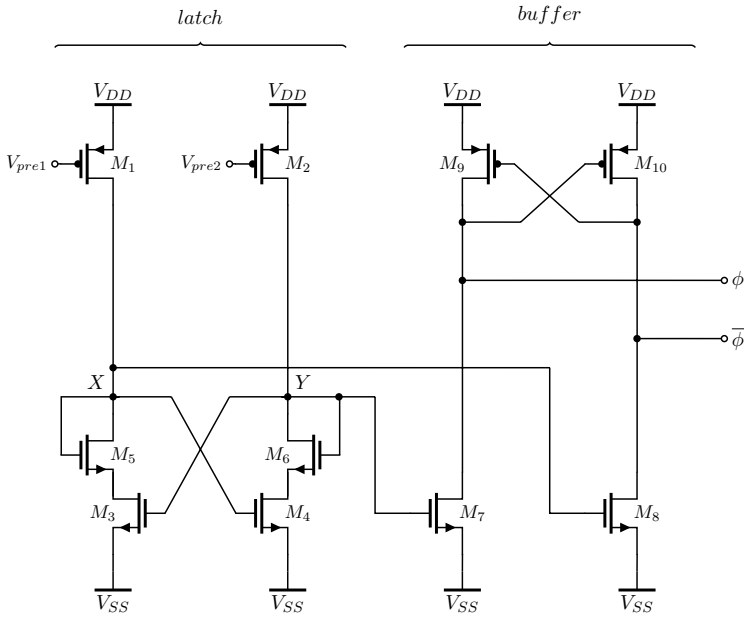


Figure 8.7: Latch and buffer stage of comparator

adaptive biasing also acts on this part of the circuit and it is seen that the static current consumption is very low, while large dynamic currents flip the circuit's state fast. The waveforms in the middle represent the output voltages of the latch, corresponding to node X and Y. In the last plot it is seen that this concept gives clean digital output signals with low fall and rise times.

8.4 Circuit design based on ACM

One of the important steps is to design the pre-amplifier's differential gain. For this step the advanced biasing scheme is neglected and the pure differential input stage considered. It has already been shown that the differential gain A_d is determined by the intrinsic gain of the input devices M_{in}. Now, it is shown that by the use of the ACM model it is easy to design for a certain gain value. As the input devices are saturated, the reverse inversion coefficient can be set to $i_{rin} = 0$. Hence, the equation for the $\frac{g_{mg}}{I_D}$-ratio, derived in subsection 6.2.1, can be simplified to be:

$$\frac{g_{m_{in}}}{I_D} = \frac{1}{V_t n} \frac{2}{\sqrt{1 + i_{fin}} + 1}.$$

With the thermal voltage V_t, the subthrehold slope factor n and the forward inversion coefficient i_{fin}. This coefficient can be calculated out of the bias current I_{BIAS} and the device aspect ratio S_{in}. During the gain peak, it has to be considered that the devices are balanced and $I_D = \frac{I_{BIAS}}{2}$ flows in each branch.

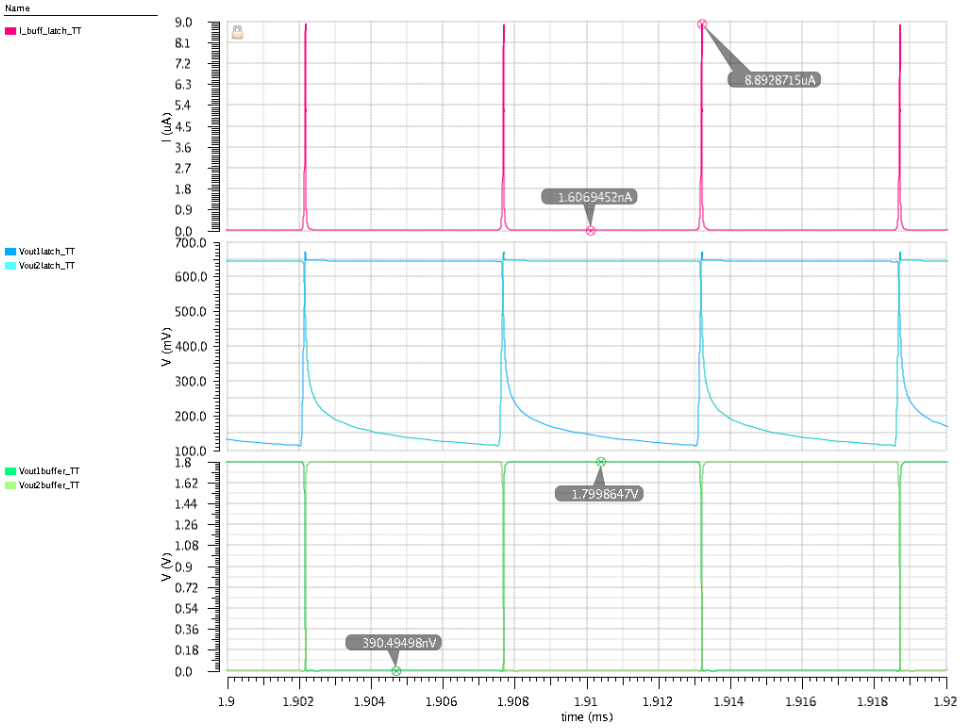


Figure 8.8: Current and voltage waveforms of the latch and buffer stage

$$i_{fin} = \frac{I_D}{S_{in} I_{inS\square}}$$

The intrinsic gain A_{in} of the input pair can be written as follows:

$$A_{in} = g_{m_{in}} r_{ds_{in}}$$

With $r_{ds_{in}}$ as the small-signal output resistance of the input transistor. This value is dependent on the normalized channel modulation factor λ_0, the device length L_{in} and the drain current I_D.

$$r_{ds_{in}} = \frac{L_{in}}{\lambda_0 I_D}$$

Therefore, the intrinsic gain can be rewritten as:

$$A_{in} = \frac{g_{m_{in}}}{I_D} \frac{L_{in}}{\lambda_0}$$

This results in some design considerations. To get a large intrinsic gain the inversion coefficient has to be small, while the $\frac{g_{mg}}{I_D}$-ratio gets large. This implies that increasing the bias current I_{BIAS} would speed up the circuit, but decrease the gain and therefore the resolution of the pre-amplifier.

I_{BIAS}	$20nA$	$40nA$	$80nA$
A_{in}	391	373	342
$r_{ds_{in}}$	1.88G	1.07G	0.614G
$g_{m_{in}}$	208n	349n	557n
λ_0	0.114	0.1	0.087
$\frac{g_{m_{in}}}{I_D}$	20.83	17.44	13.93
ACM: calculated with $\lambda_0 = 0.1$			
A_{in}	465	385	307
$\frac{g_{m_{in}}}{I_D}$	21.17	17.53	13.95
i_{fin}	2.7	5.4	10.81

Table 8.1: Input characteristics vs. bias current. $L_{in} = 2.2\mu$. λ_0 in $\frac{\mu m}{V}$

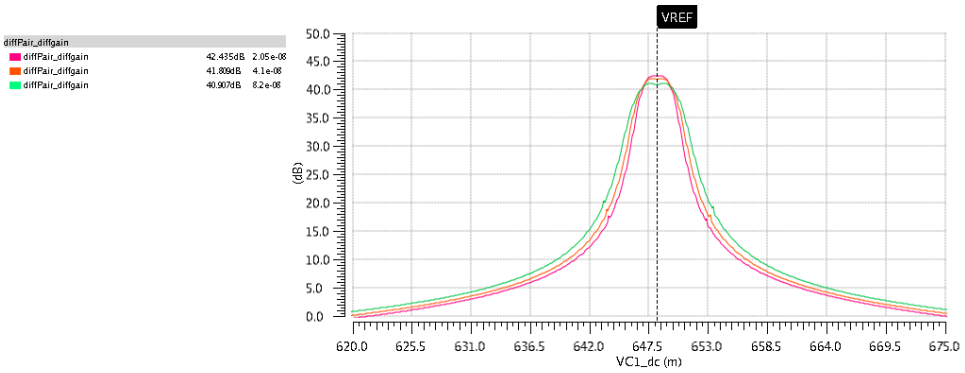


Figure 8.9: Simulated transfer for different bias currents

Table 8.1 shows simulation results of this behaviour. It is seen that the normalized channel length factor λ_0 has current related dependencies in the BSIM model. Hence, the effect of an increased $\frac{g_{m_{in}}}{I_D}$ is less dominant due to an decrease of λ_0, seen in figure 8.9.

Another important consideration is the scaling of L_{in}. It can be seen that long input transistors increase the inversion coefficient i_{fin} as the current density in the channel goes up. The $\frac{g_{m_{in}}}{I_D}$-ratio is proportional to $L_{in}^{-0.5}$ and as the gain is proportional to L_{in}, overall the gain increases. But in a opposite manor, the circuit gets slower. For this design it was preferred to design for a higher gain, as the circuit is speed up via the adaptive biasing approach.

Table 8.2 shows simulation results of this behaviour. It is seen that the normalized channel length factor λ_0 stays constant over a change of length L_{in}. Thus, the effect is more dominant, depicted in figure 8.10.

Therefore, the gain of the pre-amplifier should be scaled via adaptation of transistor lengths. Once a faster circuit is needed or matching analysis show bad results, the bias current can be increased but with a negative impact on power consumption. This can be seen in figure 8.13.

As the comparator delay effects the overall temperature behaviour of the oscillator, it has to be designed carefully. Of course it could be made as fast

L_{in}	1.1μ	2.2μ	4.4μ
A_{in}	208	356	540
$r_{ds_{in}}$	0.36G	0.77G	1.51G
$g_{m_{in}}$	575n	461n	358n
λ_0	0.099	0.093	0.095
$\frac{g_{m_{in}}}{I_D}$	20.83	17.44	13.93
ACM: calculated with $\lambda_0 = 0.1$			
A_{in}	210	339	529
$\frac{g_{m_{in}}}{I_D}$	19.06	15.41	12.02
i_{fin}	4.05	8.1	16.2

Table 8.2: Input characteristics vs. length. $I_{BIAS} = 60nA$. λ_0 in $\frac{\mu m}{V}$

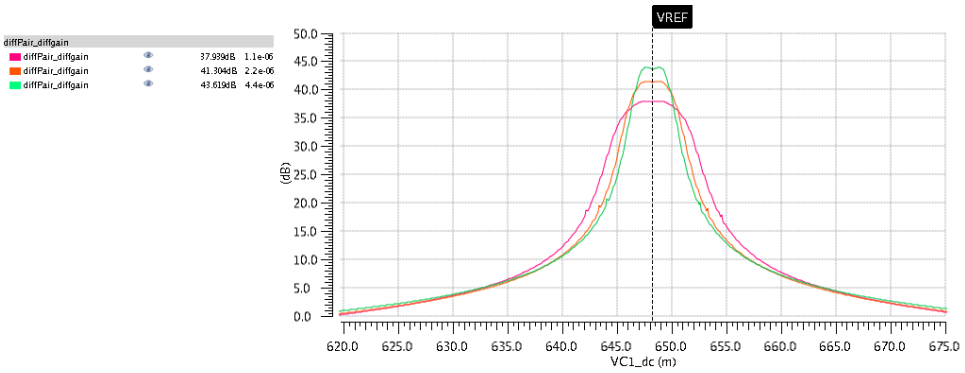


Figure 8.10: Simulated transfer for different lengths

as possible to have low impact on the output frequency, but a better approach was found. The temperature coefficient of the comparator's delay was matched with the temperature behaviour of the charging capacitor. Hence, the current budget was conserved while getting a lower temperature dependency of the output frequency.

8.4.1 Device sizing

Please note that the current I_{BIAS} was fixed to be three times the core current of the reference generator, with a value of $60.6nA$ in reference to subsection 8.4.2. The pre-amplifier was designed to have a differential gain of more than $40dB$, seen in the bottom plot of figure 8.5.

The adaptive biasing was implemented with the geometric factors of $K = 2$ and $K' = 1.5$. Hence, the design restriction of

$$\frac{K}{1 + K'} < 1$$

is fulfilled. As this circuit is biased with a low current, care has also to be taken about matching. Again, by looking at the ACM's inversion coefficient

the devices can be designed to work in moderate or strong inversion by means of reduced current mismatch, [KAGM06]. Thus, to get the devices out of weak inversion, long unity transistors have to be considered. As the circuit's delay is sensitive to mismatch, seen in figure 8.16b, it is preferable to compose all devices out of unity transistors that can be matched in a single well.

Even with the lowest current condition of $\frac{I_{BIAS}}{4}$ the nMOS devices should not enter weak inversion. The aspect ratios S_n of this devices can be calculated to be:

$$\frac{I_{BIAS}}{4I_{nS\square}} > S_n.$$

For the pMOS devices the minimum current is K-times higher:

$$\frac{KI_{BIAS}}{4I_{pS\square}} > S_p.$$

Where the sheet specific currents $I_{nS\square}$ and $I_{pS\square}$ were extracted form the BSIM models. To keep the area low, $S_n = S_p = 0.1$ and a narrow width for all unity devices was chosen. From the small-signal analysis it is clear that $S_2 = S_3 = S_4 = S_5 = S_n$ applies. The biasing scheme gives $S_1 = S_6 = KS_n$, $S_7 = S_8 = S_{10} = S_p$ and $S_9 = S_{11} = K'S_p$. Table 8.3 shows the corresponding transistor dimensions for the pre-amplifier. Voltages and currents of the input stage, for the input voltages $V_{in1} = V_{in2} = V_{REF}$, are shown in figure 8.11.

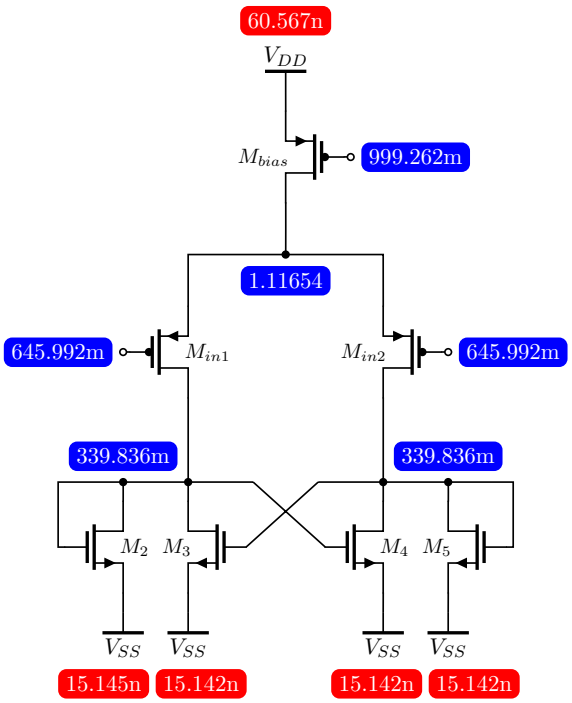


Figure 8.11: Voltages and currents balanced pre-amplifier

Device	$\frac{W}{L}$
M_{bias}	$3 \cdot 1u/20 \cdot 10u$
M_{in1}, M_{in2}	$220n/2.2u$
M_2 to M_5	$220n/2.2u$
M_1, M_6	$2 \cdot 220n/2.2u$
M_7, M_8, M_{10}	$220n/2.2u$
M_9, M_{11}	$330n/2.2u$
S_1, S_2	$1u/720n$

Table 8.3: Device sizes of pre-amplifier circuit

For a given bias current, in this case multiples of the reference generators core current, the absolute value of the delay can be tweaked by the size of the two diode-connected nMOS transistor of the latch. This method doesn't influence the temperature behaviour of the delay. Please note, that the devices of the buffer and latch stage are also composed out of unity transistors. Figure 8.12 shows how changing the multiplier does affect the delay for different corners. The transistors in the buffer stage are designed to have a big multiplier to improve the slew-rate at the oscillator's output. Out of design the buffer drives area-intense switches, that are designed to overcome leakage dependencies. Table 8.4 shows the transistor sizes for the latch and buffer stage.

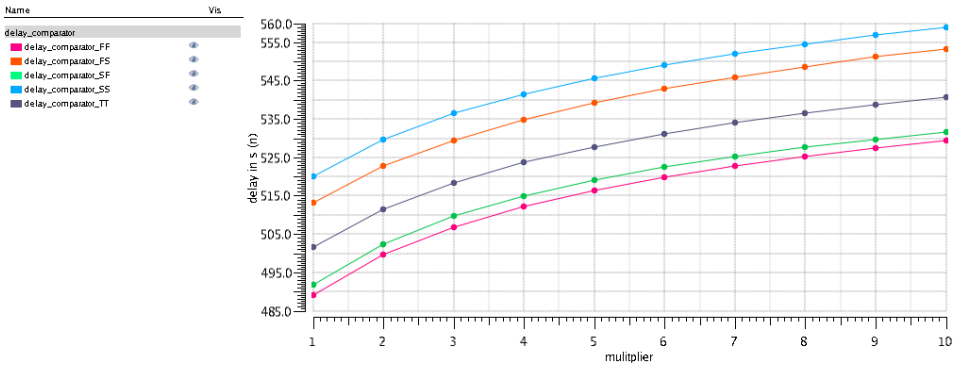


Figure 8.12: Optimization of comparator delay

Device	$\frac{W}{L}$
M_1 to M_4, M_9, M_{10}	$220n/2.2u$
M_5, M_6	$2 \cdot 220n/2.2u$
M_7, M_8	$10 \cdot 220n/2.2u$

Table 8.4: Device sizes of latch and buffer circuit

8.4.2 Achievements

The delay and current consumption are the main design parameters for the comparator, therefore in this subsection simulation results and statistical analysis are represented. For simulations of the delay, the current source of the reference generator and it's voltage reference as well as the MIM capacitors were replaced by ideal components. The time-constant was fixed for an ideal $100kHz$ clock. The deviation of the output signal from the ideal clock was calculated as delay.

It is clear that the bias current influences the speed of the comparator circuit. In figure 8.13 this effect is shown for different corner cases. It is seen that the decrease in delay flattens out with increased bias currents. As the current consumption increases linearly, it doesn't make sense to bias the circuit with a very large current. A good trade-off between delay and current budget was found at three times I_{REF}, that corresponds to around $60nA$ and gives a delay of around 5% of the oscillator's period.

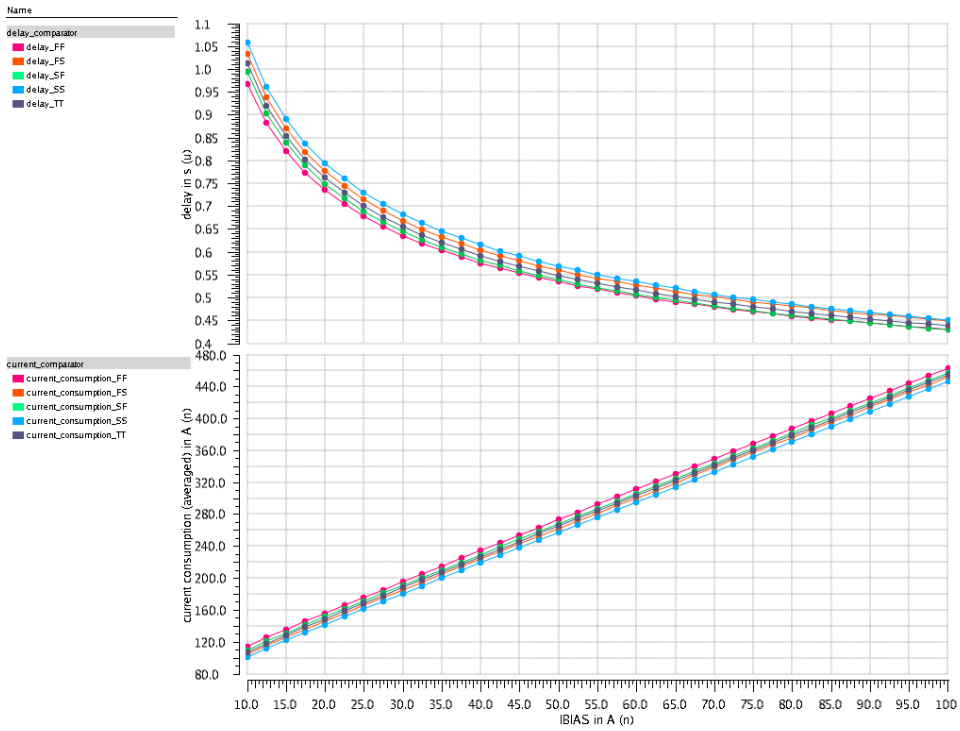


Figure 8.13: Delay and current consumption vs bias current

Figure 8.14 shows the temperature characteristics of the comparator delay and current consumption. The temperature coefficient of the delay can be calculated to be around $650\frac{ppm}{°C}$. But as already mentioned, only 5% of the clock period are caused by the comparator delay. Thus, the delay dependent temperature coefficent of the oscillator period is in the range of $33\frac{ppm}{°C}$. And that value is well matched with the temperature coefficient of the MIM capacitors used throughout this design. As all the currents in the comparator circuit are fixed by the adaptive biasing scheme, it is not surprising that the

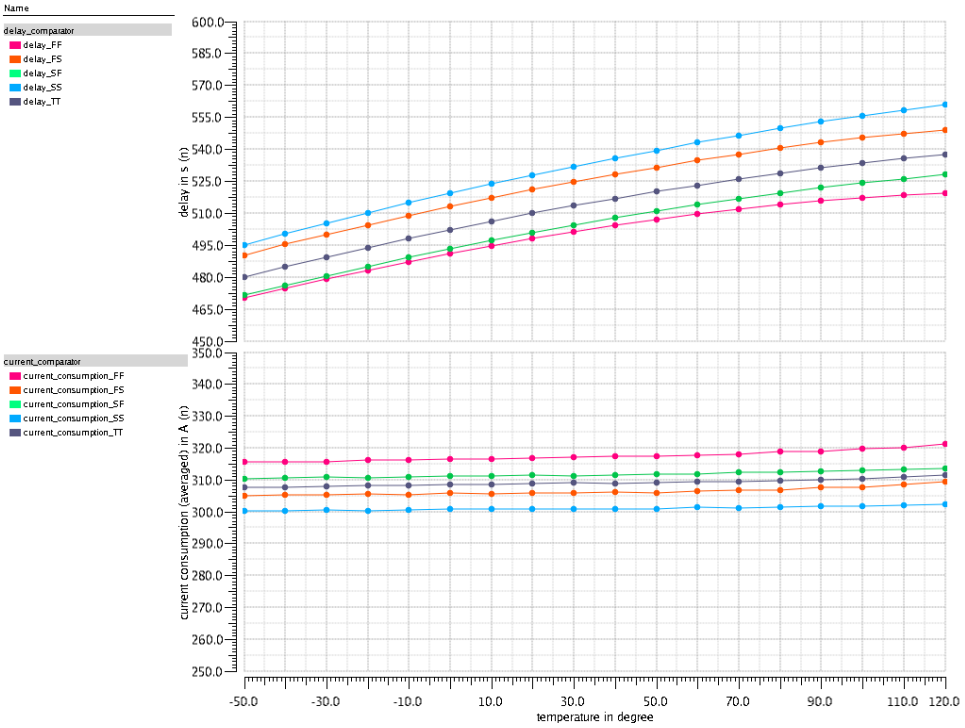
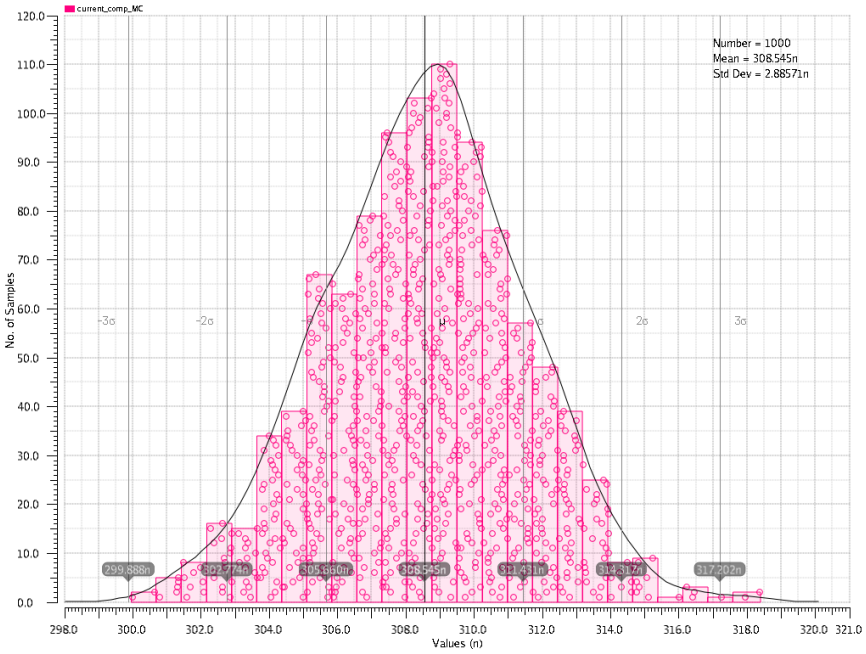


Figure 8.14: Delay and current consumption vs temperature

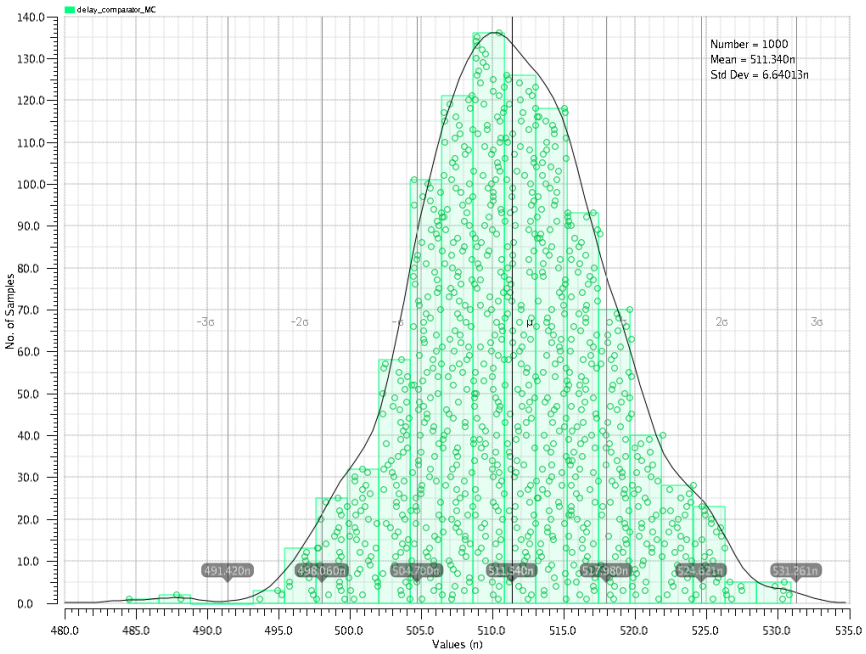
current consumption is little varying with temperature, seen in the bottom plot.

Both the comparator delay and the current consumption have been statistical analysed. The histograms for process variation can be seen in figure 8.15. The standard deviation for the delay and current consumption are at 1.3% and 1%. The Gaussian distributions and the low values for the standard deviation indicate a robust design with fixed current consumption.

Figure 8.16 gives information about mismatch sensitivity of the circuit. A standard deviation of 2% and 9.5% are reached for the current consumption and the comparator delay. Even if spread for the delay seems to be high, it has to be said that the oscillator period would only vary by 0.5% for one sigma. Overall the impact of mismatch is not having an significant effect on the system performance and the current consumption stays very centred.

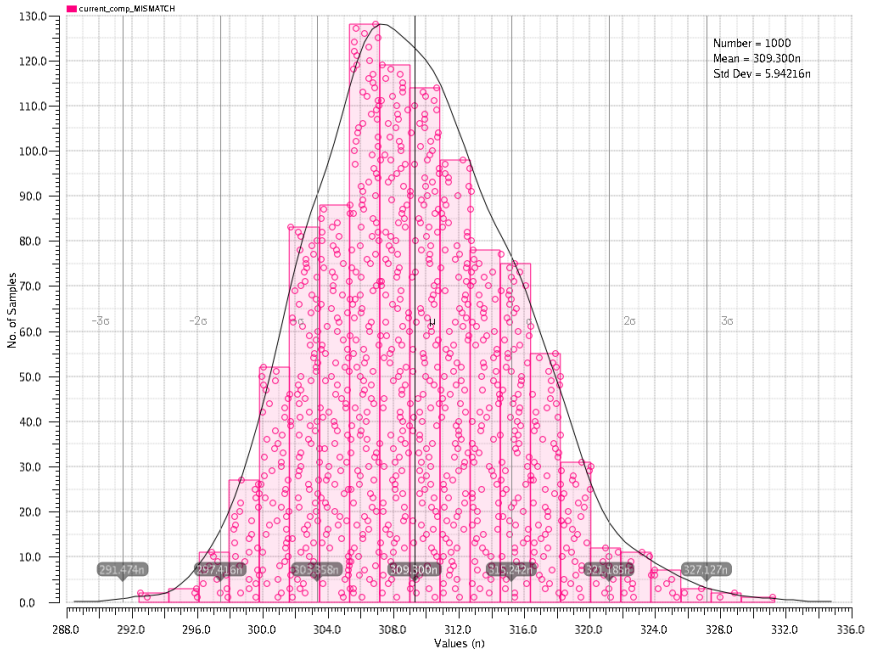


(a) Current consumption - Histogram 1000 samples

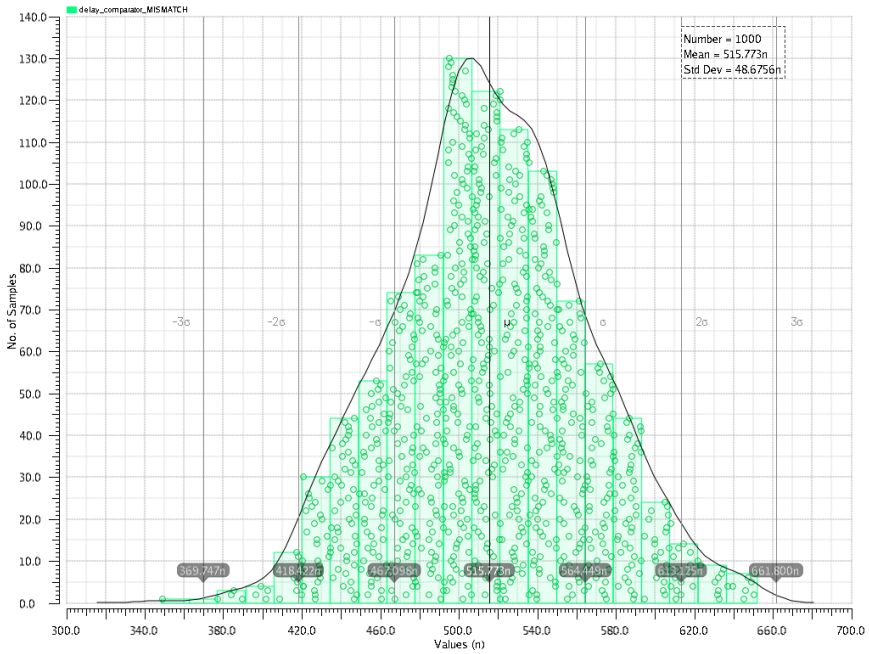


(b) Delay - Histogram 1000 samples

Figure 8.15: Process variation of comparator delay and current consumption



(a) Current consumption - Histogram 1000 samples



(b) Delay - Histogram 1000 samples

Figure 8.16: Mismatch analysis of comparator delay and current consumption

Chapter 9

Time-Constant

The time-constant refers to the main principle of the dual-phase system. It consists out of two capacitors, that get charged by the reference current alternately. The capacitors act as current integrators and whenever the reference voltage is reached, after a certain delay, one of the comparators flips the latch. This immediately starts to discharge the corresponding capacitor and re-routes the current to the opposite one. Figure 9.1 shows the principle during a state transmission. The capacitor voltage V_{C1} reached V_{REF}, and t_d delayed the switches S_2 and S_3 close while S_1 and S_4 open. C_1 gets discharged and the voltage V_{C2} starts to increase with a rate of $\frac{I_{REF}}{C_2}$. After V_{C2} reached V_{REF} the sequence repeats in the opposite way.

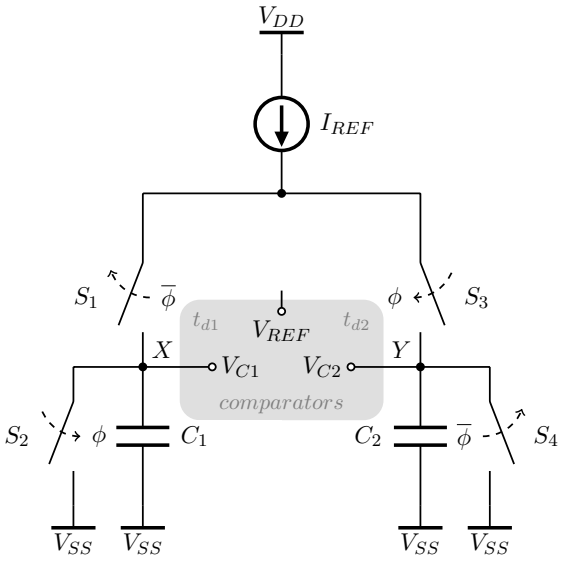


Figure 9.1: Time-constant of dual-phase oscillator

As already mentioned, if the circuitry is well matched, $C = C_1 = C_2$ and $t_d = t_{d1} = t_{d2}$, the period T_0 of the output signal can be written as:

$$T_0 = 2C\frac{V_{REF}}{I_{REF}} + 2t_d.$$

The oscillator's period is supposed to stay within $\pm 5\%$ over temperature,

process and voltage change, while digital programming is applied to trimm it's absolute value. Not only the temperature dependency of the reference voltage V_{REF}, reference current I_{REF}, capacitor C and the delay t_d give the overall temperature coefficient, but also the leakage current of the switches has to be taken into account. This subthreshold and junction leakage is heavily dependent on temperature and process. Especially for low-power circuits, where the reference current is low, the impact should not be underestimated. By applying digital programming to the circuit, even more switches have to be considered. Therefore, leakage reduction techniques have been implemented in the design.

The transient waveforms of the oscillator can be seen in figure 9.2. The upper waveforms represent the voltages across the capacitors, V_{C1} and V_{C2}, and the reference voltage V_{REF}. Clearly, it can be seen that the comparator delay gives rise to a increased period and therefore a reduction of output frequency. As already stated, the temperature coefficient of this delay was matched to the temperature behaviour of the MIM capacitors. As the reference current and voltage itself have by design a low temperature dependency, the oscillator period is stabilised over temperature. By using current trimming, explained in subsection 9.2.2, as preferred trim option, another advantage is given. The temperature behaviour stays stable while trimming the absolute value of the output frequency. This would not be the case, if the reference current would have been designed as PTAT. The lower waveforms show the output signals of the oscillator and the transient current consumption of the complete oscillator design.

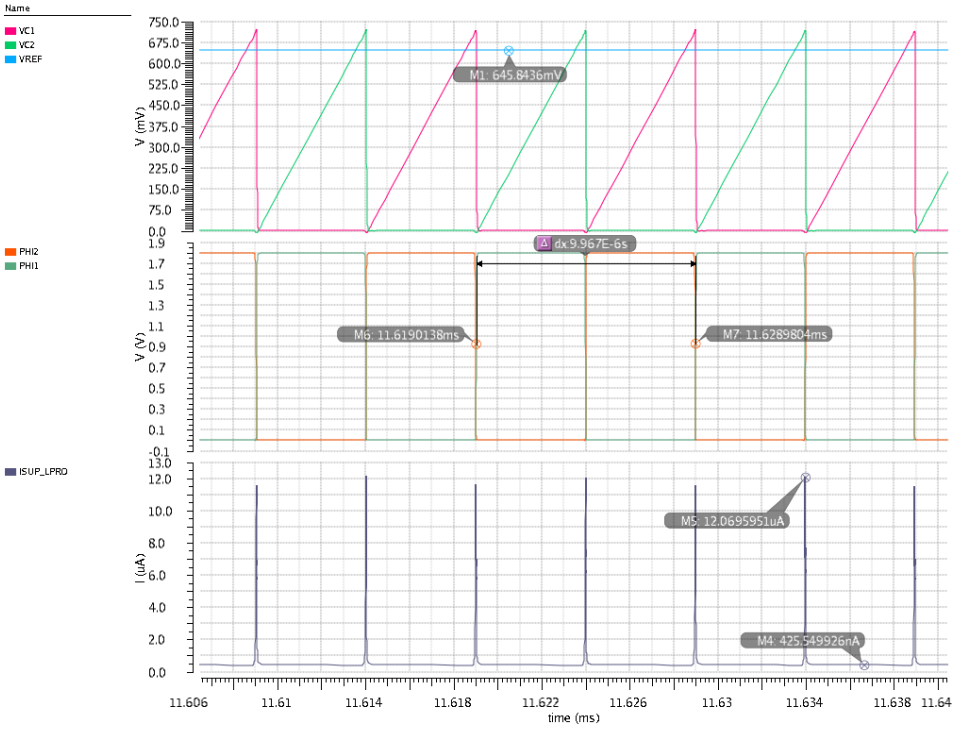


Figure 9.2: Transient simulation of the low-power oscillator

Figure 9.3 shows a zoomed view into one of the oscillator's phases. This approach is superior to single capacitor designs, as the discharging delay, seen in the green curve, is not contributing to the clock period. Another advantage is that the design gets by on only one reference current and voltage. Hence, this low-power design enables the ability to give a 50% duty-cycle output clock that is proper temperature-compensated.

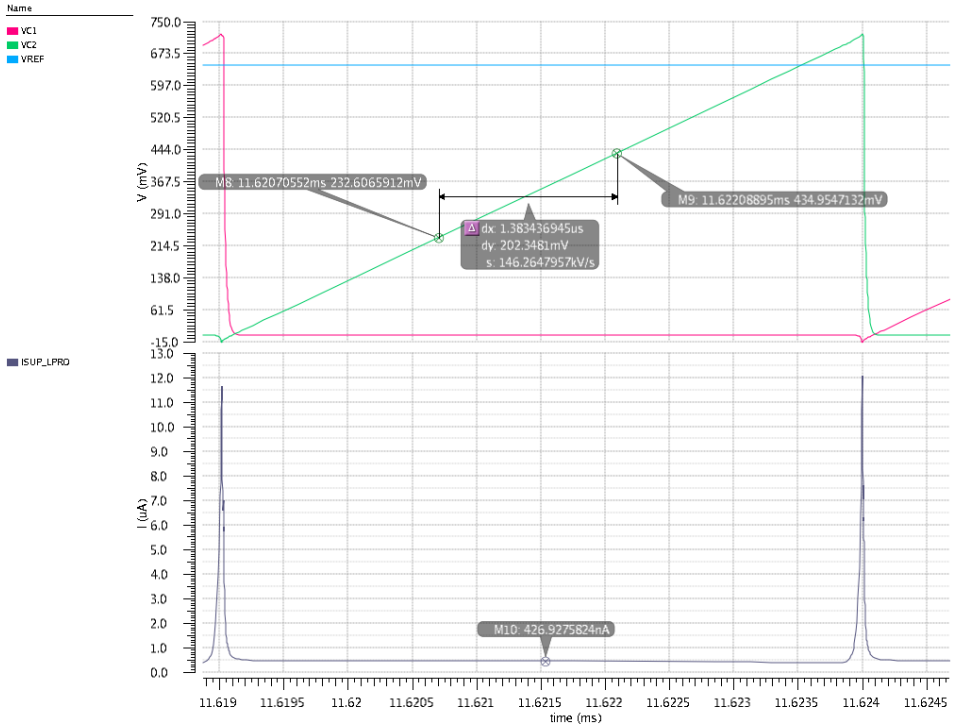


Figure 9.3: Detailed look into one charging phase

It is seen in table 9.1 that the capacitance C gets into a reasonable range for the $100kHz$ output clock. The reference current I_{REF} was fixed to be five times the reference generator's core current.

Parameter	Value
V_{REF}	$646mV$
I_{REF}	$101nA$
C	$700fF$

Table 9.1: Design for $100kHz$ output clock

9.1 Leakage reduction

A very detailed look into leakage mechanisms and reduction techniques is given by [RMMM03]. As in modern technologies the oxide thickness and therefore threshold voltages get lower and lower, it is more difficult to turn a transistor completely off. Even if the gate-to-source voltage is zero, if the device acts as switch, a leakage current persists. Please note that the threshold voltage further decreases and additional the subthreshold slope gets linearly higher with temperature. Hence, more voltage reduction is needed for a certain current shrinkage and it is obvious that the leakage current increases.

A very effective way to reduce the leakage current within a current path, is the use of transistor stacks, [YBD98] and [CJWR98]. This area and power efficient technique can also be applied to the switching devices of the dual-phase oscillator, [IKT+06]. The principle is seen in figure 9.4. Whenever the switch is turned off, the middle voltage V_M is clamped to a fixed voltage. In this case V_{DD} or V_{SS}. This means that device M_1 has a negative gate-to-source voltage V_{GS} and is therefore fully cut-off. Hence, node A is isolated in a much stronger way from node B. As MOS transistors are symmetric devices, depending on the voltage level of node B, leakage could occur via M_3 and M_2. Whenever the switches are closed, the reference current I_{REF} is only affected by leakage into node A. Therefore, this would not lead to an influence of the system's temperature coefficient.

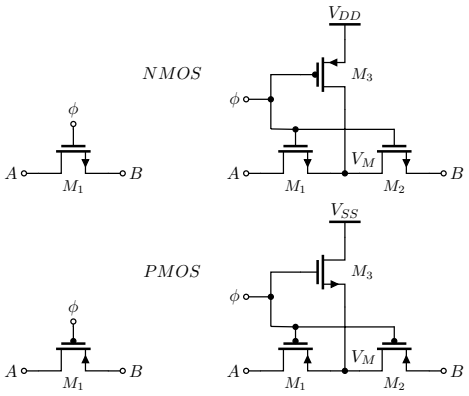


Figure 9.4: Simple and reduced leakage switch

The effect of this technique is made visible in the figures below. Both graphs show the leakage current from the capacitor node over the discharge switch to ground. This was simulated for two high temperature points while both devices had equally $\frac{W}{L}$-ratios. Figure 9.5 gives the graph for a simple nMOS switch and figure 9.6 for the modified low-leakage switch.

The upper part of the graphs give the charging current and the lower one the unwanted leakage towards ground. Clearly it can be seen, that the leakage is reduced by a factor of 3. Please not that not only the ground switch is connected to the capacitor node, but also switches that are used for

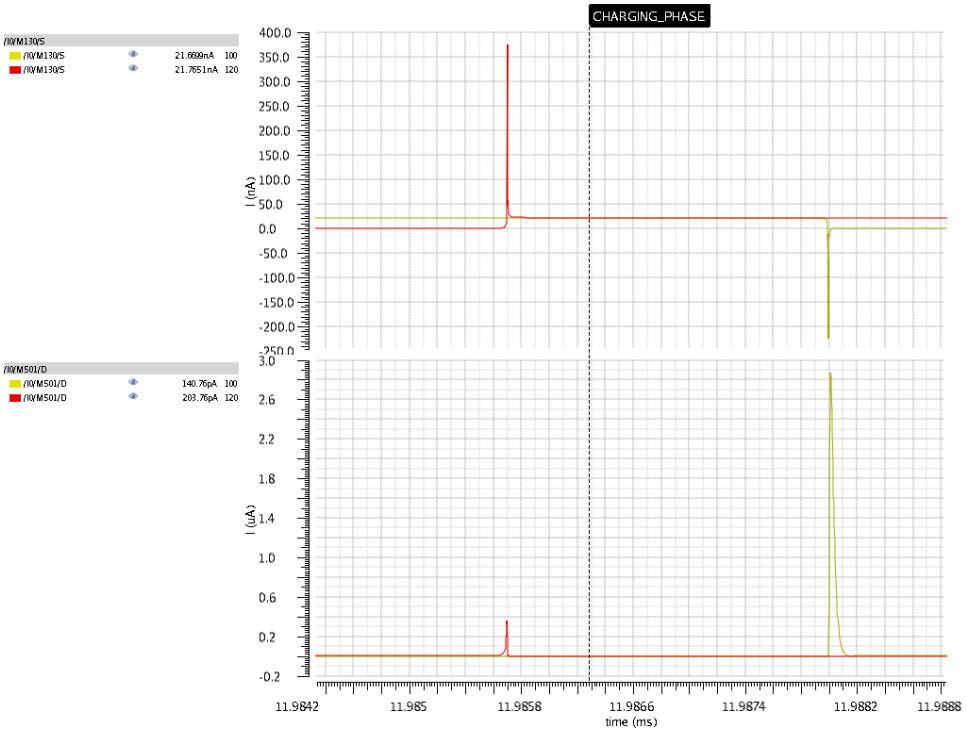


Figure 9.5: Leakage - simple switch

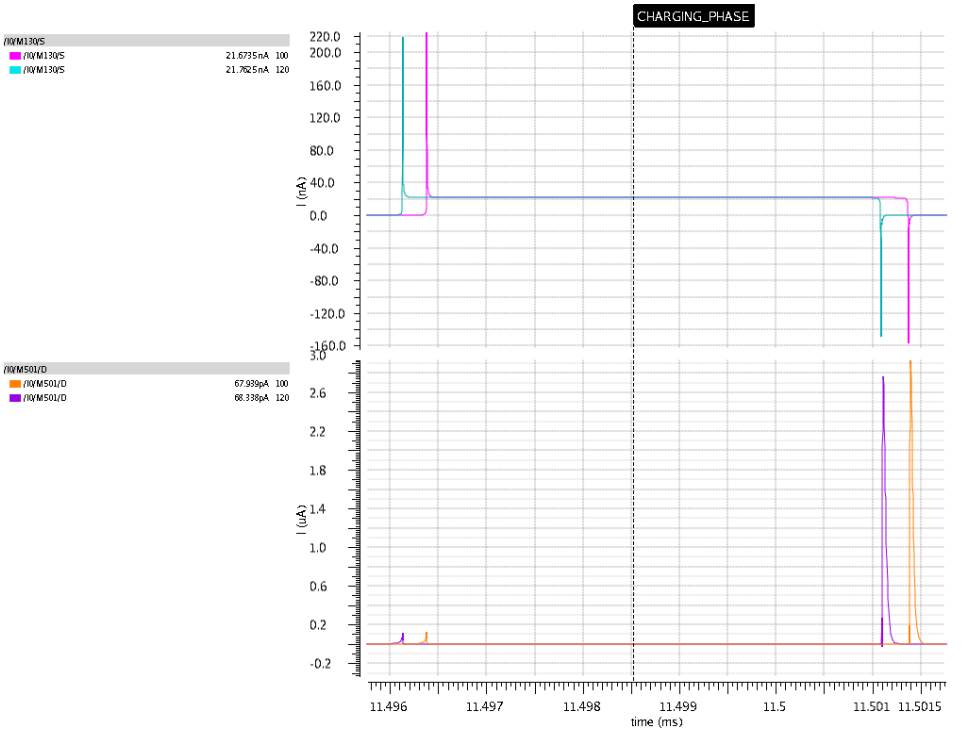


Figure 9.6: Reduced leakage - modified switch

capacitive trimming. Therefore, even if the process is not optimized for low leakage, this technique may enable the design of low-power circuits.

Figure 9.7 shows how leakage reduced switches are applied in the design. The switches have low aspect ratios as they are designed for high off-resistance rather than low on-resistance. The pMOS devices route the reference current I_{REF} between both branches while the nMOS devices make sure that leakage against ground is minimized. The corresponding device sizing is seen in table 9.2.

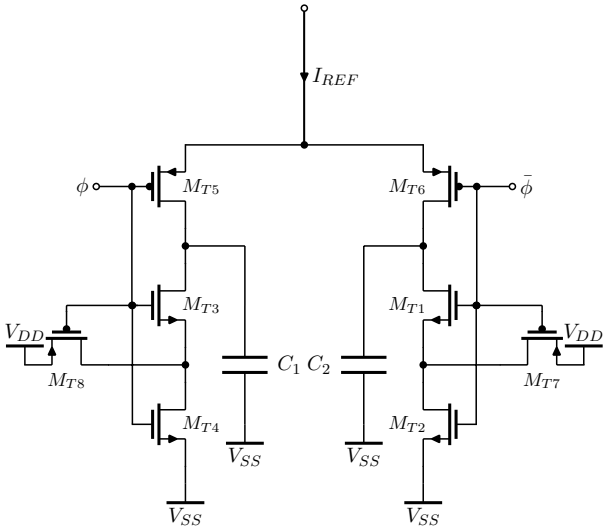


Figure 9.7: Leakage reduction applied

Device	$\frac{W}{L}$
M_{T1} to M_{T4}	$220n/2.2u$
M_{T5}, M_{T6}	$220n/4.4u$
M_{T7}, M_{T8}	$220n/8.8u$

Table 9.2: Device sizes of switches

9.2 Digital programming

Before the system goes into power-down mode, the absolute value of the output frequency is trimmed once during active mode. The system clock that is provided by an accurate phase-locked-loop circuit, gives the reference for the trimming procedure. A synchronisation signal, that stays over a defined number of B periods high, is generated out of the low-power oscillators output and acts as an enable signal for a synchronous counter. This circuit counts the number of system clocks, synchronized via it's enable. And therefore the accuracy Q_{DP} of the digital programming can be written as:

$$Q_{DP} = \frac{2}{B}\frac{f_{LPO}}{f_{SYS}}.$$

Where, f_{LPO} is the frequency of the low-power oscillator, f_{SYS} the high frequency system clock and B the number of clock cycles the synchronisation signal stays high. One iteration of the trimming loop has a duration of t_i seconds and gives a counter output C.

$$t_i = \frac{B}{f_{LPO}}$$

The relation between the counter output and the actual frequency of the low-power oscillator is therefore given by:

$$f_{LPO} = \frac{B}{C} f_{SYS} \pm \left(\frac{Q_{DP}}{2}\right)\%.$$

The maximum duration t_{max} of the complete trimming procedure is dependent on the number of trim bits n. t_s refers to a possible settling time after each iteration.

$$t_{max} = 2^n \left(t_i + t_s\right)$$

For the n-bit digital programming it is essential to implement a monotonic analog trimming scheme into the oscillator. For this design this can be done either by trimming the reference current I_{REF} or the capacitors C. Additional a coarse and fine trimming procedure was applied. The flowchart of the trimming procedure can be seen in section 10.3. Table 9.3 shows the parameter values for the design including the accuracy Q_{DP} reached with 5-bit programming.

9.2.1 Capacitor trimming

Throughout this thesis MIM[1] capacitors were used, as they have superior density, linearity and matching properties. But most important is their low temperature coefficient that makes them very suitable for this design. To

[1] Metal Insulator Metal

Parameter	Value
f_{SYS}	$13.56MHz$
f_{LPO}	$100kHz$
B	5
n	5
t_s	1 LPO cycle
t_{max}	$1.92ms$
Q_{DP}	0.295%

Table 9.3: Parameters for digital programming

vary the capacitance on node X and Y, seen in figure 9.1, they are connected in parallel via leakage reduced nMOS switches. As this approach introduces many parasitics and post-layout simulations showed that for low reference currents I_{REF} no monotonic trimming characteristic can be achieved, it was found that current trimming is superior for this low-power design. Only one bit capacitive trimming is applied.

9.2.2 Current trimming

The device that provides the reference current I_{REF} is by design a $M+1$-times parallel composition of a $N+1$-times stacked unity transistor. The current trimming is done by shorting these pMOS devices. Therefore, the $\frac{W}{L}$-ratio and the current provided by the transistor stack changes. Figure 9.8 shows the trimming matrix of the current sourcing device.

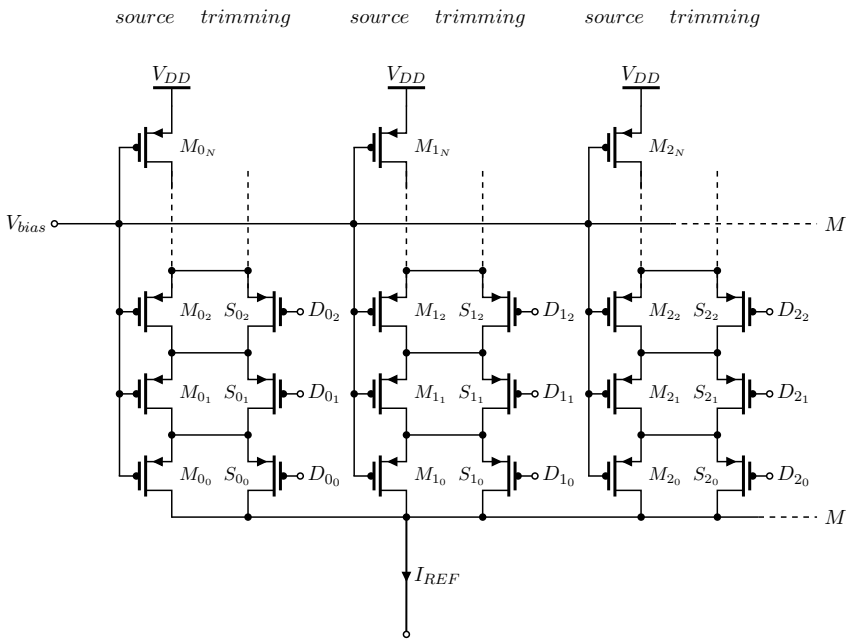


Figure 9.8: Current trim matrix

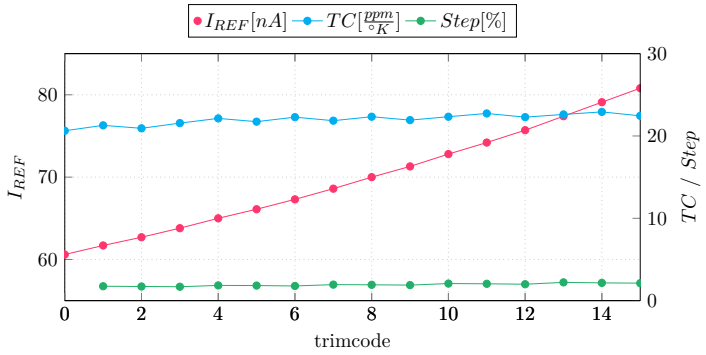


Figure 9.9: Simulated trim characteristics

Just the lower $X + 1$ unity transistors get shorted to keep the trimming characteristics as linear as possible. A decoder has to ensure that the switches S_{0_0} to S_{M_X} are closed from the bottom left to the top right part of the matrix. This approach gives a linear, monotonic trimming procedure that has minimal impact on the temperature coefficient of the reference current. This is depicted in figure 9.9. This graph corresponds to the following design variable values $N = 9$, $M = 2$ and $X = 4$. Increasing M would lead to a further reduction of the step size and therefore the trimming resolution would increase. The design would get more insensitive against parasitics but on the other hand area and power consumption is increased. N as well as the current step I_{step}, after shorting one unity transistor, is fixed by the design of the current reference. Hence, the accuracy of the trimming Q_T can be written as:

$$Q_T = \frac{I_{step}}{(M+1)\, I_{REF_0}}.$$

Where, I_{REF_0} is the current delivered by one transistor stack. It can be seen that there is a trade-off between trimming accuracy and current consumption. The number of desired digital bits n is given by

$$n = \lceil \log_2 \left[(M+1)\,(X+1) \right] \rceil.$$

The corresponding parameters for the design are shown in table 9.4a. Hence, the trim-matrix consists out of ten series devices, M_{x_0} to M_{x_9} and five parallel branches, M_{0_x} to M_{4_x}. Six devices in each branch can be shorted via switches S_{x_0} to S_{x_5}. Once again, the switches are designed for low leakage with low aspect ratios. Moreover to benefit layout, they are kept at the same length than the sourcing devices, seen in table 9.4b.

Parameter	Value
I_{step}	$1.18nA$
I_{REF_0}	$20.2nA$
M	4
X	5
Q_T	1.17%

(a) Parameters

Device	$\frac{W}{L}$
M_{x_x}	$1u/10u$
S_{x_x}	$220n/10u$

(b) Device sizes

Table 9.4: Current trimming of design

9.3 Meeting the specification

To meet the specifications, first X has to be chosen to meet the following condition:

$$D_{PM} < (X+1)\frac{I_{step}}{I_{REF_0}}.$$

Where, D_{PM} is the maximum deviation over process and mismatch. Please note that a linear trimming function, illustrated in figure 9.9, is only achieved if X is close to or less than $\frac{N}{2}$. The maximum deviation should also include the process dependency of the capacitor. To fulfil the accuracy specification given in 4.1, the sum of the deviation over voltage D_{VC} and the deviation over temperature D_{TC}, in combination with the trim accuracy Q_T and the accuracy of the digital programming Q_{DP} has to be lower than the specification $SPEC$.

$$SPEC > D_{VC} + D_{TC} + Q_{DP} + Q_T$$

Variable	in combination with	gives
M	current reference	Q_T
X	current reference	$> \mathbf{D_{PM}}$
B	PLL accuracy	Q_{DP}
TC	temperature range	D_{TC}
VC	voltage range	D_{VC}
Q_T,Q_{DP},D_{TC},D_{VC}		$<$ **SPEC**

Table 9.5: Summary of design variables

Part III

Results and Summary

Chapter 10

Results

Simulation results of the reference generator, comparator and trimming scheme have been shown before. This chapter deals with the system performance of the implemented oscillator design. Many graphs give a compact view on the performance. The layout as well as complete schematics are shown and a summary is included in section 10.6.

10.1 Performance analysis

Important performance characteristics of the low-power oscillator can be seen in this section. The variation of the output frequency with respect to supply voltage and temperature are shown for different process corners. Another graph gives the settling behaviour for the typical, slowest and fastest corner case.

In figure 10.1 the output frequency in respect to time is seen. After initial start-up, the oscillator gives an output clock after several microseconds and starts to increase the frequency fast. Looking at the typical case, after about $0.5\mu s$ the start-up circuit of the reference generator deactivates itself and the frequency starts to converge slowly till the final value is reached. This behaviour can be seen in figure 7.12b. After both the reference current and voltage reached the peak, the slow settling behaviour occurs.

The variation of the output frequency in respect to supply voltage is plotted in figure 10.2. For the fast-fast corner it is seen that a high voltage coefficient is obtained and therefore this gives one drawback of the design. However, as this design is well compensated over temperature, the variation over PVT is well within the specification.

Figure 10.3 shows the normalized variation of the output frequency in respect to temperature. At temperatures above $80°C$ the output frequency starts to rise for all corner cases. This is due to low leakage of the switches. As the reference current itself gets higher and the leakage-reduced switches lower the charging current far less, the current to the capacitors is increased for higher temperatures. This increases the frequency and the beneficial effect of the reduced leakage is made visible within this graph.

The design's current consumption over temperature for different corners is shown in figure 10.4. It is seen that variation of the absolute current over

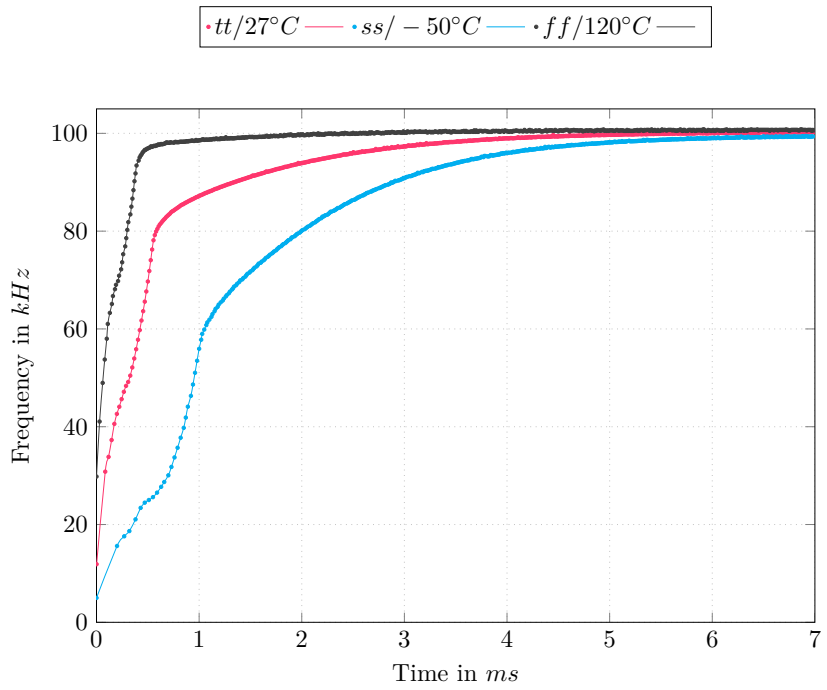


Figure 10.1: Settling time over corners

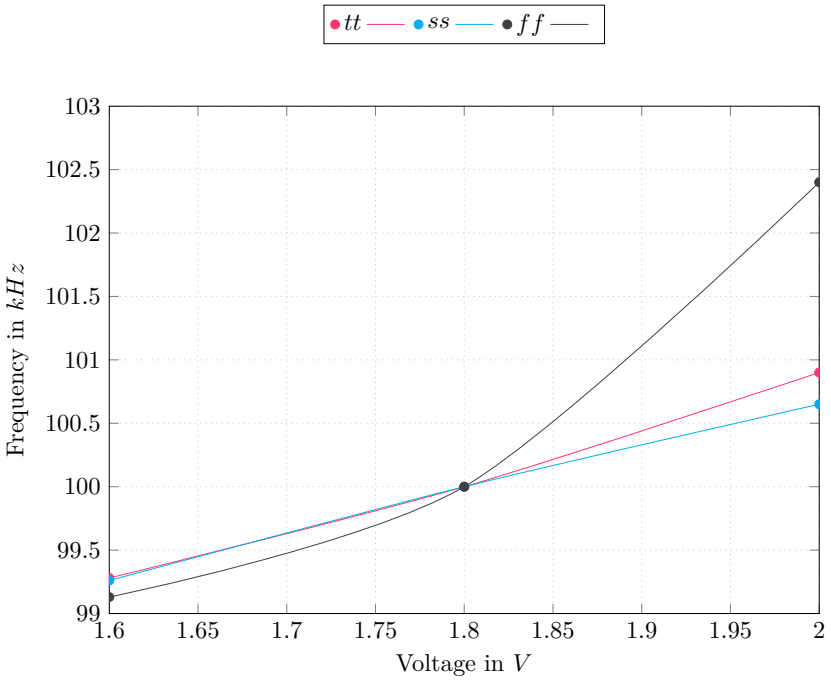


Figure 10.2: Frequency over voltage

process is less than ±10%. As TSMC's 180nm process isn't designed for low leakage, the current consumption increases for high temperatures. At the worst condition the current peaks at around 725nA. It has to be said, that

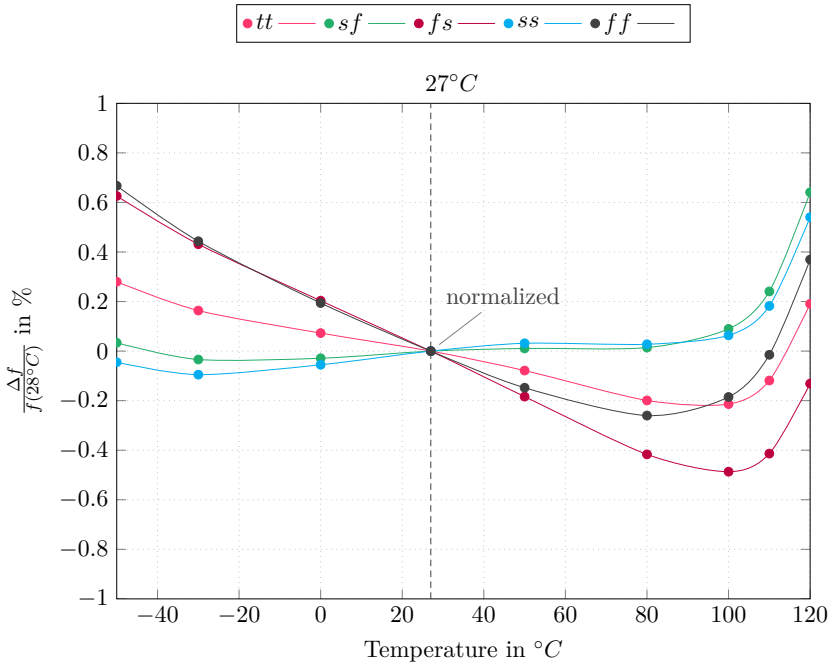


Figure 10.3: Normalized variation of frequency over temperature

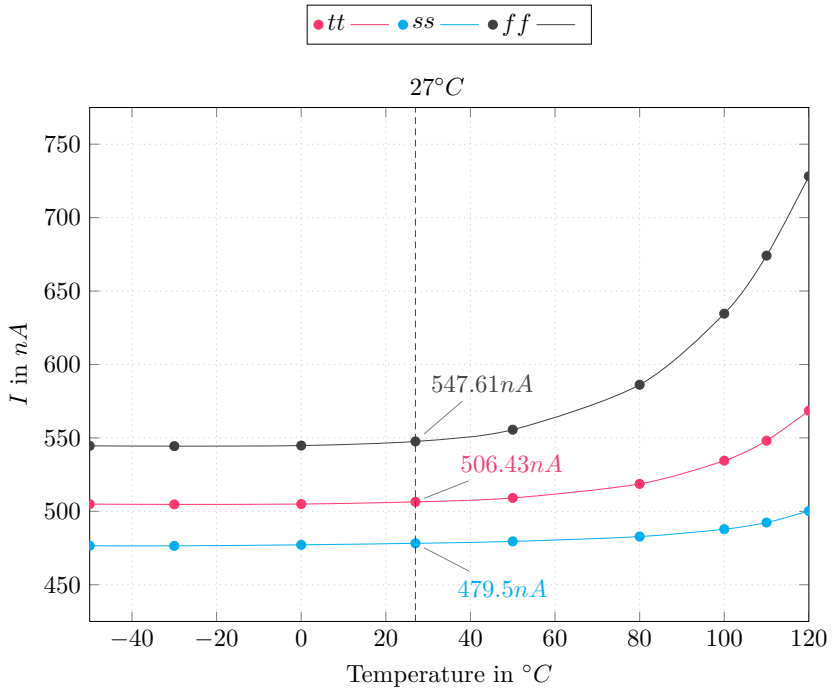
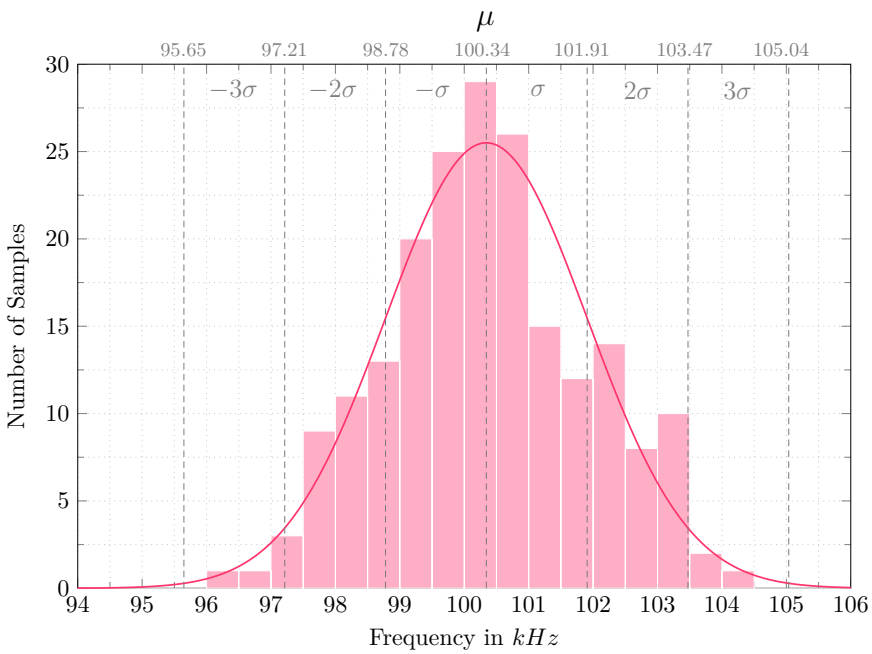


Figure 10.4: Variation of absolute current consumption

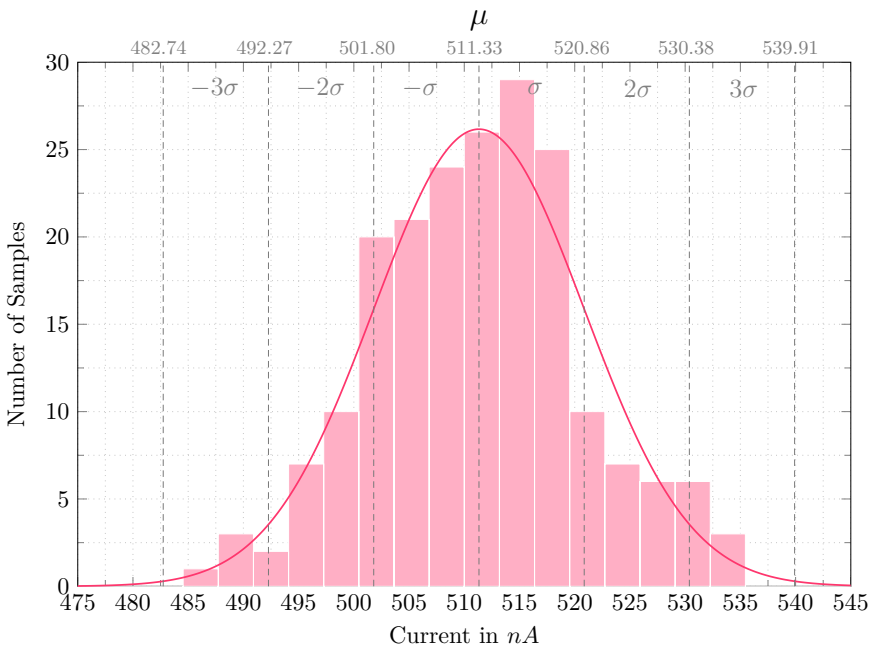
the leakage of the SoC's memory block as well as the digital part exceeds this values by far. In conclusion, this design enables a very low power consumption during the SoC's standby mode.

10.2 Statistical analysis

The statistical analysis over 200 samples proved that the design is robust against mismatch. Both the output frequency and the current consumption follow a Gaussian distribution with standard deviations of 1.5% and 1.9%.



(a) Histogramm - frequency



(b) Histogramm - current consumption

Figure 10.5: Monte Carlo Mismatch Analysis - 200 Samples

10.3 Trimming flowchart

The trimming flowchart for $B = 5$, $N = 9$, $M = 4$ and $X = 5$ is given below. Additional 1-bit capacitive trimming was included, to ensure that the desired variation over process and mismatch is covered. The number of bits is five. Hence 30 states are for current trimming and 2 states for capacitive trim.

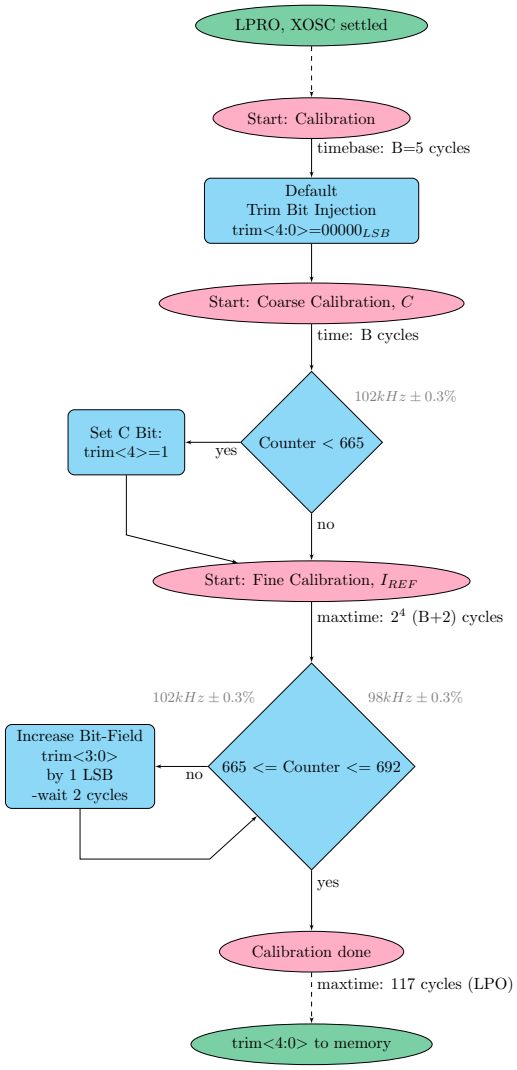


Figure 10.6: Calibration flowchart

10.4 Schematics

Figure shows the schematics of the designed oscillator. Trimming capabilities, the digital decoder, test-interface and power-down devices are not included.

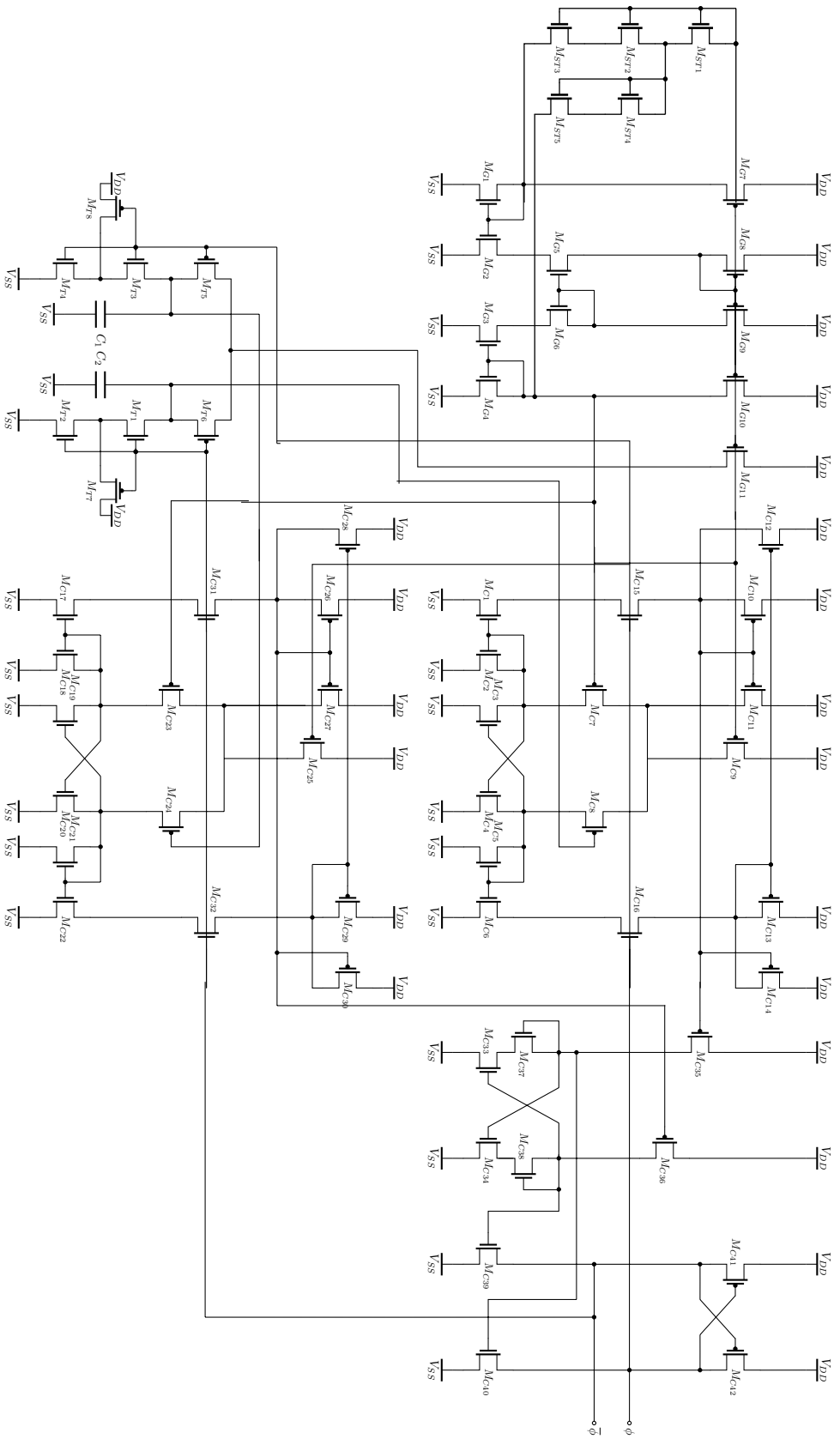


Figure 10.7: Schematics - Low-Power Oscillator

10.5 Layout

It is seen in figure 10.8 that the reference generator with it's large transistors occupies most of the oscillator's area. Throughout the layout it was taken care that the matching is as good as possible. Common-centroid layout and the use of dummy structures was common practise. The area of the full layout is less than $0.075mm^2$.

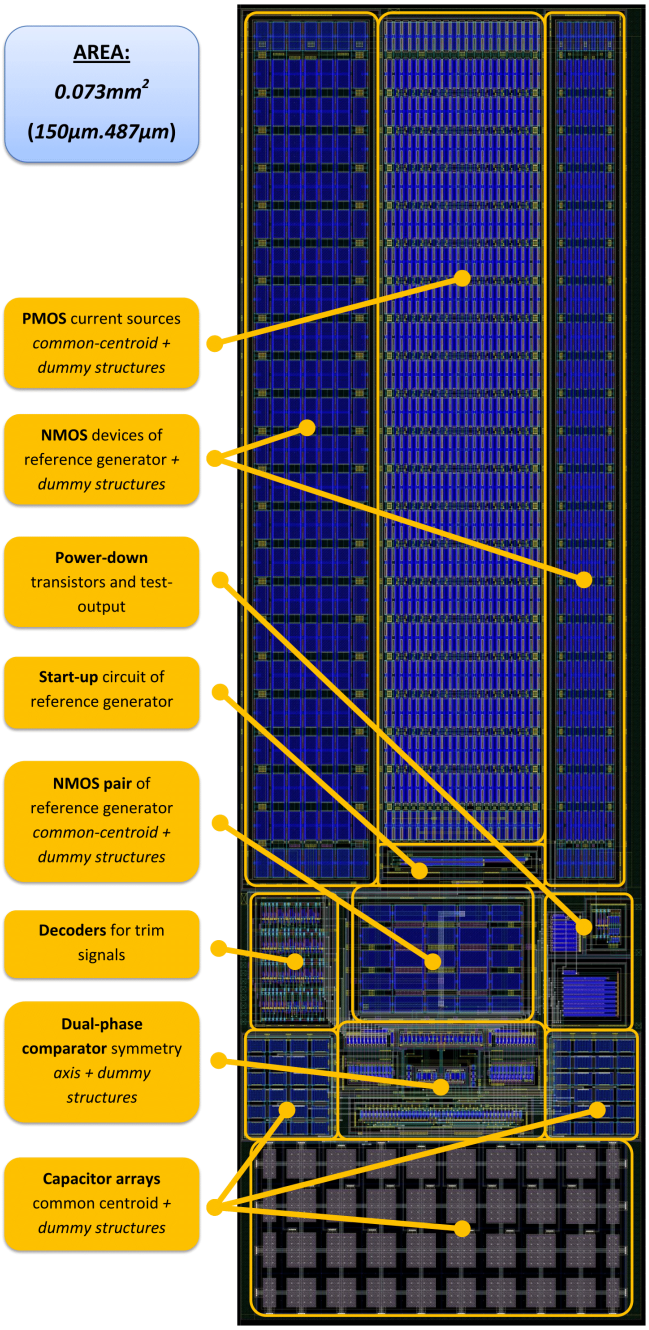


Figure 10.8: Layout of the Low-Power Oscillator

In the figures below parts of the layout are shown in more detail. The symmetric layout of the comparator that combines two pre-amplifiers, a latching and buffering stage can be clearly seen in figure 10.9. The leakage reduced switching structures can also be seen in this view. In figure 10.10 techniques to improve matching are shown. All the current sources of the design are matched in a common-centroid pattern.

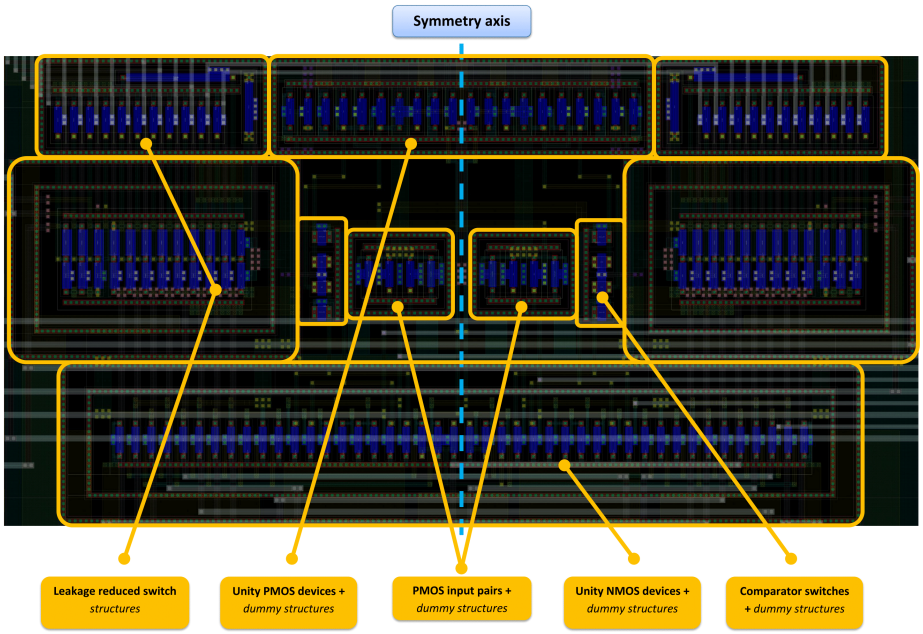


Figure 10.9: Layout of the comparator block

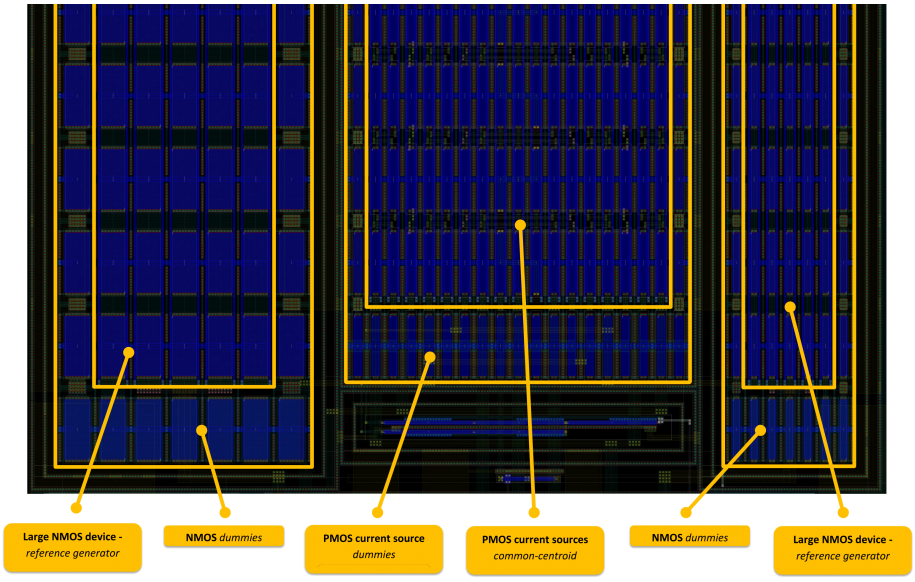


Figure 10.10: Layout view of matched devices

10.6 Summary

This section gives a summary of the most relevant performance parameters of the implemented low-power design, seen in table 10.1. Afterwards it is concluded that all specifications are well met, in reference to table 10.2. Statistical analysis showed that the design is robust, with current consumption way below the specification. The design's accuracy is due to good temperature compensation within range, even if the voltage coefficient is quite high.

	Worst	Info	Reference
$TC_{V_{REF}}\left[\frac{ppm}{°C}\right]$	68	over corners: 36 to 68	figure 7.5b
$TC_{I_{REF}}\left[\frac{ppm}{°C}\right]$	52	over corners: 28 to 52	figure 7.3b
$TC_{f_{LPO}}\left[\frac{ppm}{°C}\right]$	65	over corners: 29 to 65	figure 10.3
$VC_{f_{LPO}}\left[\frac{\%}{V}\right]$	9	over corners: 3.8 to 9	figure 10.2
$3\sigma_{f_{LPO}}\,[\%]$	4.7	tt corner	figure 10.5a
$3\sigma_{I_{LPO}}\,[\%]$	5.6	tt corner	figure 10.5b

Table 10.1: Summary of the system performance

To check against the accuracy specification, the total variation of the output frequency $D_{f_{LPO}}$ after trimming can be calculated as follows.

$$D_{f_{LPO}} = \frac{TC_{f_{LPO}} \cdot 170°C}{10000} + VC_{f_{LPO}} \cdot 0.36V + Q_{DP} + Q_T = \pm 2.87\%$$

Hence, the final comparison of the low-power design against the specification can be made.

	Specification	Design
Operation frequency	100 - $200kHz$	$100kHz$
Accuracy over PVT	$\pm 5\%$	$\pm 2.87\%$
Supply voltage	$1.8V \pm 10\%$	$1.8V \pm 10\%$
Current consumption	1 - $2\mu A$	$500nA$
Trimming	Yes	Yes
Temperature range	-50 to $120°C$	-50 to $120°C$
CMOS-Process	TSMC $180nm$	TSMC $180nm$
Area	less than $0.1mm^2$	$0.073mm^2$

Table 10.2: Design vs. specification

Chapter 11

Conclusion and Future Work

In this thesis, a very low-power relaxation oscillator design for a wide temperature range was presented. Table 10.2 shows that all specifications are met and the current consumption by far not reaches the limit. Nevertheless, the accuracy is better than specified, which could be achieved by the low temperature coefficient of the novel reference circuit, in combination with the current trimming approach and leakage reduction techniques. Additional, the absolute variation of the reference voltage and current over process could be minimized, by the absence of integrated resistors. It can be seen in figure 7.5a and 7.3a that the variation is not more than $\pm 4\%$ for the voltage and $\pm 7\%$ for the current. Hence, this unique MOS-only circuit is very suitable to achieve low-power consumption as well as minimal absolute variation, in combination with a good temperature coefficient. The adaptive biased comparator circuit ensured maximum speed for a given current budget.

It has to be said, that the design aims an industrial product and therefore robustness is also very important. Thus, the target was not to push the design to it's current consumption limits. The low-power oscillator is essential for the boot procedure of the targeted SoC and therefore proper start-up has to be ensured. This can be seen in figure 7.10. This design gets included into a chip, targeting the Internet of Things, to outperform competitors in concern of standby current consumption. This is an important performance parameter, especially for battery powered mobile devices.

11.1 Future work

As the voltage coefficient of the oscillator is high for the ff-corner, seen in figure 10.2, cascode structures can be used to lower it. This parameter with $\pm 1.6\%$ is the main contributor to the design's accuracy $D_{f_{LPO}}$. If the accuracy specifications get tighter this parameter has to be lowered. Figure 10.1 shows the settling time for different corner cases. It can be seen that the start-up circuit of the reference speeds up the settling just for a certain amount of time. Therefore, if faster settling is needed additional circuitry has to be added and analysed.

Appendices

Appendix A

Bibliography

[Abi06] A.A. Abidi, *Phase Noise and Jitter in CMOS Ring Oscillators*, IEEE J. of Solid State Circuits **41** (2006), 1803–1816.

[AH02] R. Aparicio and A. Hajimiri, *A Noise-Shifting Differential Colpitts VCO*, IEEE J. of Solid State Circuits **37** (2002), 1728–1736.

[AK13] M.T. Abuelmaatti and Z.J. Khalifa, *Fully Uncoupled Independent Control of Frequency and Condition of Oscillation: A Caution*, TENCO 2013 - 2013 IEEE Region 10 Conference (2013), 1–4.

[AWVF05] P. Andreani, X. Wang, L. Vandi, and A. Fard, *A study of phase noise in Colpitts and LC-tank CMOS oscillators*, IEEE J. of Solid State Circuits **40** (2005), 1107–1118.

[BB97] K. Bult and A. Buchwald, *An Embedded 240-mW 10-b 50-MS/s CMOS ADC in 1-mm2*, IEEE J. of Solid State Circuits **32** (1997), 1887–1895.

[Bro74] A.P. Brokaw, *A Simple Three-Terminal IC Bandgab Reference*, IEEE J. of Solid State Circuits **6** (1974), 388–393.

[BSU+99] H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, and K. Sakui, *A CMOS Bandgab Reference Circuit with Sub-1-V Operation*, IEEE J. of Solid State Circuits **34** (1999), 670–674.

[Chi14] Y.H. Chiang, *Nanopower CMOS Relaxation Oscillators with Sub-100ppm/cel Temperature Coefficient*, IEEE Trans. on Circuits Syst. II (2014).

[CJWR98] Z. Chen, M. Johnson, L. Wei, and K. Roy, *Estimation of Standby Leakage Power in CMOS Circuits Considering Accurate Modeling of Transistor Stacks*, IEEE Proceedings (1998), 239–244.

[CL11] Z. Chen and T. Lee, *The Design and Analysis of Dual-Delay-Path Ring Oscillators*, IEEE Trans. on Circuits Syst. I **58** (2011), 470–478.

[CRA+07] G. Cusmai, M. Repossi, G. Albasini, A. Mazzanti, and F. Svelta, *A Magnetically Tuned Quadrature Oscillator*, IEEE J. of Solid State Circuits **42** (2007), 2870–2877.

[CSA11] F. Aznar C. Sanchez-Azqueta, S. Celma, *A 0.18um CMOS ring VCO for clock and data recovery applications*, Microelectron. Reliab. **51** (2011), 2351–2356.

[CSGM98] A.I.A. Cunha, M.C. Schneider, and C. Galup-Montoro, *An MOS Transistor Model for Analog Circuit Design*, IEEE J. of Solid State Circuits **33** (1998), 1510–1512.

[CVPHM07] J. Carnes, I. Vytyaz, K. Mayaram P.K. Hanumolu, and U. Moon, *Design and Analysis of Noise Tolerant Ring Oscillators Using Maneatis Delay Cells*, IEEE (2007).

[Dar15] H. Darabi, *Radio Frequency Integrated Circuits and Systems*, vol. 1, May 2015.

[Den10] U. Denier, *Analysis and Design of an Ultralow-Power CMOS Relaxation Oscillator*, IEEE Trans. on Circuits Syst. **8** (2010), 1973–1982.

[Dia09] C. Dias, *Osciladores de rádio frequência em quadratura com acoplamento capacitivo*, Master's thesis - Universidade Nova de Lisboa (2009).

[DR15] S. Dai and J.K. Rosenstein, *A 14.4nw 122khz Dual-phase Current-mode Relaxation Oscillator for Near-Zero-Power Sensors*, IEEE (2015).

[DT11] E. Sanchez-Sinencio D.Z. Turker, S.P. Khatri, *A DCVSL delay cell for fast low power frequency synthesis applications*, IEEE Trans. on Circuits Syst. I **58** (2011), 1225–1238.

[EKV95] C.C. Enz, F. Krummenacher, and E.A. Vittoz, *An Analytical MOS Transistor Model Valid in All Regions of Operation and Dedicated to Low-Voltage and Low-Current Applications*, Analog Integrated Circuits and Sig.Pro. **8** (1995), 83–114.

[ES53] W.A. Edson and R.I. Sarbacher, *Vacuum-Tube Oscillators*, vol. 1, John Wiley and Sons, Inc., 1953.

[ESS10] M.M. Elsayed and E. Sanchez-Sinencio, *A Low THD, Low Power, High Output-Swing Time-Mode-Based Tunable Oscillator Via Digital Harmonic-Cancellation Technique*, IEEE J. of Solid State Circuits **45** (2010), 1061–1071.

[FA01] I. M. Filanosky and A. Allam, *Mutual Compensation of Mobility and Threshold Voltage Temperature Effects with Applications in CMOS Circuits*, IEEE Trans. on Circuits Syst. I **48** (2001), 876–884.

[GM16] B. Goel and S. A. McKee, *A Methodology for Modeling Dynamic and Static Power Consumption for Multicore Processors*, IEEE International Parallel and Distributed Processing Symposium (2016), 273–282.

[GY14] M. Gupta and P. Yadav, *Design and Performance Analysis of a Double-Tail Comparator for Low-Power Applications*, IJSRET (2014), 80–84.

[GZ09] B. Goll and H. Zimmermann, *A Comparator With Reduced Delay Time in 65-nm CMOS for Supply Voltages Down to 0.65V*, IEEE Trans. on Circuits Syst. II **56** (2009), 810–814.

[HL99] A. Hajimiri and T.H. Lee, *The design of low noise oscillators*, Norwell, MA: Kluwer (1999).

[HL08] W.L. Goh-W.M. Lim H.Q. Liu, L. Siek, *A 7-GHz mulitloop ring oscillator in 0.18-um CMOS technology*, Analog Integr. Circuits Sig. Proc. **56** (2008), 179–184.

[HL09] L. Sie-W.M. Lim Y.P. Zhang H.Q. Liu, W.L. Goh, *A low-noise mulit-GHz CMOS multiloop ring oscillator with coarse and fine frequency tuning*, IEEE Trans. VLSI Syst. **17** (2009), 571–577.

[IHT+11] K. Isono, T. Hirose, K. Tsubaki, N. Kuroki, and M. Numa, *A 18.9-na Standby Current Comparator with Adaptive Bias Current Generator*, IEEE Asia SS. C. Conference (2011), 237–240.

[IKT+06] K. Ishida, K. Kanda, A. Tamtrakarn, H. Kawaguchi, and T. Sakurai, *Managing Subthreshold Leakage in Charge-Based Analog Circuits With Low-VTH Transistors by Analog T-Switch (AT-Switch) and Super Cut-off CMOS (SCCMOS)*, IEEE J. of Solid State Circuits **41** (2006), 859–867.

[JJA13] M. Reaz J. Jalil and M. Ali, *CMOS Differential Ring Oscillators*, IEEE microwave magazine (2013).

[KAGM06] H. Klimach, A. Arnaud, and C. Galup-Montoro, *MOSFET mismatch modeling: a new approach*, IEEE Design and Test of Computers **23** (2006), 20–29.

[KNSF93] T. Kobayashi, K. Nogami, T. Shirotori, and Y. Fujimoto, *A Current-Controlled Latch Sense Amplifier and a Static Power-Saving Input Buffer for Low-Power Architecture*, IEEE J. of Solid State Circuits **28** (1993), 523–527.

[LdP07] E. Fabris A.A. Susin L.S. de Paula, S. Bampi, *A high swing low power CMOS differential voltage-controlled ring oscillator*, IEEE Comp. Society Annu. Symp. VLSI **2007** (2007), 467–470.

[Lee96] D.B. Leeson, *A Simple Model of Feedback Oscillator Noise Spectrum*, Proceedings of the IEEE **54** (1996), 329–330.

[Lee98] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, vol. 1, May 1998.

[LK00] J.S. Lee and B. Kim, *A Low-Noise Fast-Lock Phase-Locked Loop with Adaptive Bandwidth Control*, IEEE J. of Solid State Circuits **35** (2000), 1137–1145.

[Lop10] H.F. Lopes, *Low Power Low Voltage Quadrature RC Oscillators For Modern RF Receivers*, Dissertation - Universidade Nova de Lisboa (2010).

[Man90] C.W. Mangelsdorf, *A 400-MHz Input Flash Converter with Error Correction*, IEEE J. of Solid State Circuits **25** (1990), 184–191.

[MH93] J.G. Maneatis and M.A. Horowitz, *Precise Delay Generation Using Coupled Oscillators*, IEEE J. of Solid State Circuits **28** (1993), 1273–1282.

[MP08] A. Nabavi M. Parvizi, A. Khodabakhsh, *Low-power high-tuning range CMOS ring oscillator VCOs*, IEEE ICSE **2008** (2008), 40–44.

[NJ97] W. Nebel and J.Mermet(Editors), *Low Power Design in Deep Submicron Electronics*, vol. 1, Springer, 1997.

[Ody02] M. Odyniec, *RF and Microwave Oscillator Design*, vol. 1, May 2002.

[OFF+08] L.B. Oliveira, J.R. Fernandes, I.M. Filanovsky, C.J.M. Verhoeven, and M.M. Silva, *Analysis and Design of Quadrature Oscillators*, vol. 1, April 2008.

[PK99] C. Park and B. Kim, *A Low-Noise, 900-MHz VCO in 0.6um CMOS*, IEEE J. of Solid State Circuits **34** (1999), 586–591.

[Raz01] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 2001.

[RMMM03] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, *Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-Submicrometer CMOS Circuits*, IEEE Proceedings **91** (2003), 305–327.

[SES88] W.M. Sansen, F. Eynde, and M. Steyaert, *A CMOS Temperature-Compensated Current Reference*, IEEE J. of Solid State Circuits **23** (1988), 821–824.

[SL11] N. Ishihara K.Masu S.Y. Lee, S. Amakawa, *2.4-10GHz low-noise injection-locked ring voltage controlled oscillator in 90 nm complementary metal oxid semiconductor*, Jpn. J. Appl. Phys. **50** (2011), 5.

[SMK+07] D. Schinkel, E. Mensink, E. Klumperink, E.v. Tuijl, and B. Nauta, *A Double-Tail Latch-Type Voltage Sense Amplifier with 18ps Setup+Hold Time*, IEEE Intern. S.-S. Circuits Con. (2007), 314–315.

[SPSS07] F. Bahmani S.W. Park, J.L. Ausin and E. Sanchez-Sinencio, *Nonlinear Shaping SC Oscillator With Enhanced Linearity*, IEEE J. of Solid State Circuits **42** (2007), 2421–2431.

[ST07] H. Shao and C.-Y. Tsui, *A Robust, Input Voltage Adaptive and Low Energy Consumption Level Converter for Sub-threshold Logic*, IEEE European SS. C. Conference (2007), 312–315.

[ST09] ———, *Low Energy Level Converter Design for Sub-Vth Logics*, IEEE Asia South Pacific Des. Auto. Conference (2009), 107–108.

[Sze81] S. M. Sze, *Physics of Semiconductor Devices*, vol. 1, McGraw-Hill, 1981.

[Teo13] H.-N. Teodorescu, *Revisiting and Generalizing Barkhausen's Equality*, Springer-Verlag (2013).

[Tsi87] Y. Tsividis, *Operation and Modeling of the MOS Transistor*, vol. 1, McGraw-Hill, 1987.

[VF77] E.A. Vittoz and J. Fellrath, *CMOS Analog Integrated Circuits Based on Weak Inversion Operation*, IEEE J. of Solid State Circuits **3** (1977), 224–231.

[VN79] E.A. Vittoz and O. Neyroud, *A Low-Voltage CMOS Bandgap Reference*, IEEE J. of Solid State Circuits **3** (1979), 573–577.

[VW48] Valley and Wallman, *Vacuum tube amplifiers*, vol. 1, May 1948.

[WCC06] A. Wang, B.H. Calhoun, and A.P. Chandrakasan, *Sub-threshold Design for Ultra Low-Power Systems*, vol. 1, Springer, 2006.

[WDJF15] H. Wang, Y. Du, X. Jia, and Y. Fan, *A Low-Power Continuous-time Comparator with Enhanced Bias Current at the Flip Point*, IEEE (2015), 0–0.

[WHT04] H.-C. Tsai C.-K. Wang W.-H. Tu, J.-Y. Yeh, *A 1.8V 2.5-5.2 GHz CMOS dual-input two-stage ring VCO*, IEEE Asia-Pacific Conf. Advanced Sys. Int. Cir. **2004** (2004), 467–470.

[WNSL04] B. Wicht, T. Nirschl, and D. Schmitt-Landsiedel, *Yield and Speed Optimization of a Latch-Type Voltage Sense Amplifier*, IEEE J. of Solid State Circuits **39** (2004), 1148–1158.

[WY04] K.-L. J. Wong and C.-K. K. Yang, *Offset Compensation in Comparators With Minimum Input-Referred Supply Noise*, IEEE J. of Solid State Circuits **39** (2004), 837–840.

[WZG+12] Y. Wang, C. Zhao, R. Geiger, D. Chen, and S. Huang, *Performance verification of start-up circuits in reference generators*, IEEE J. of Solid State Circuits (2012), 518–521.

[Yan12] J. Yan, *A low total harmonic distortion sinusoidal oscillator based on digital harmonic cancellation technique*, May 2012.

[YBD98] Y. Ye, S. Borkar, and V. De, *A New Technique for Standby Leakage Reduction in High-Performance Circuits*, IEEE VLSI Circuits (1998), 40–41.

[YST10] M.-L. Sheu Y.-S. Tiao, *Full range voltage-controlled ring oscillator in 0.18um CMOS for low-voltage operation*, Electron. Lett. **46** (2010), 30–32.